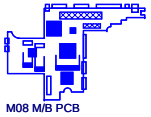
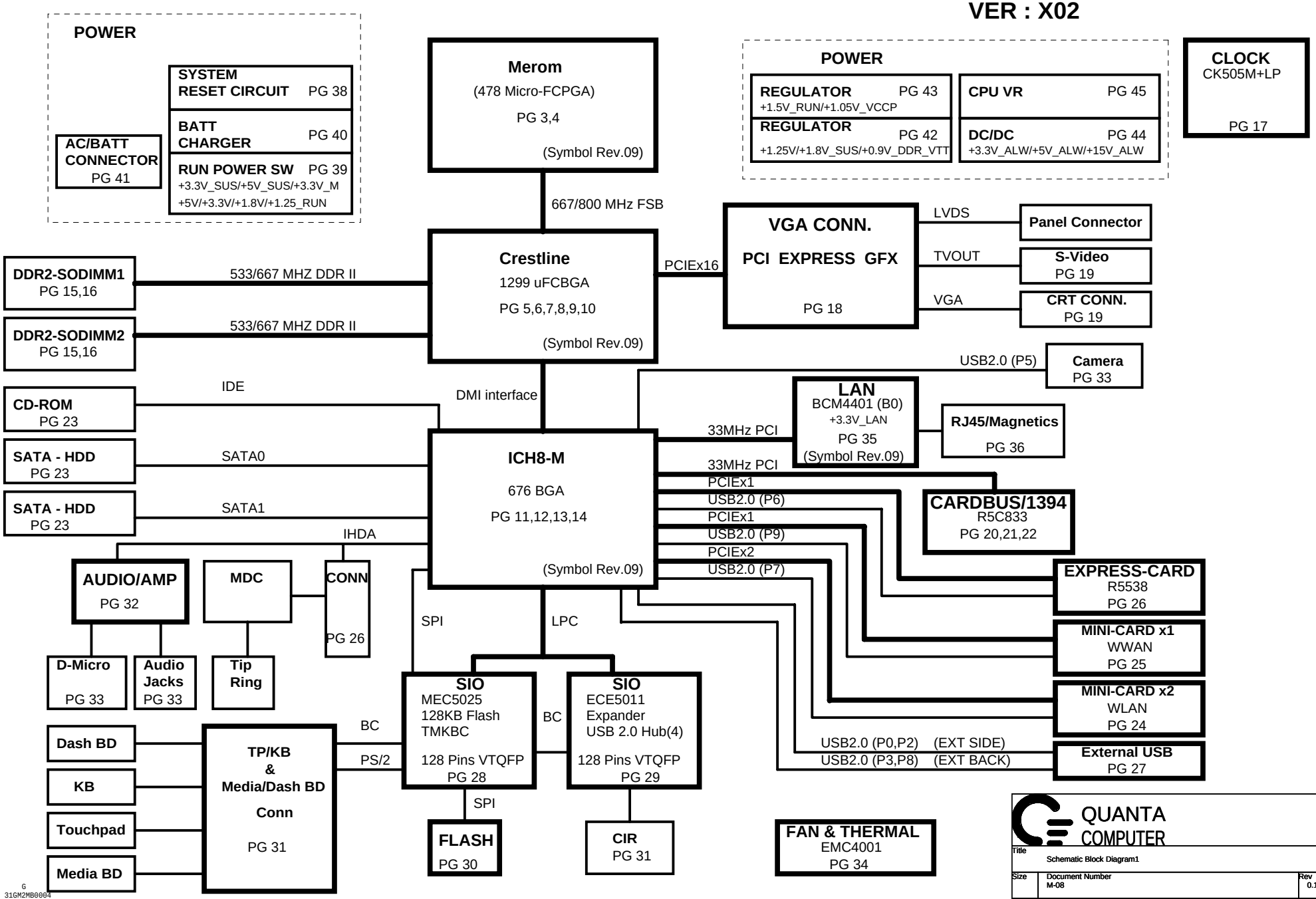
WWW.AliSaler.Com



Corsica\Gilligan - DISCRETE

VER : X02



C G
31FM5MB0011 31GM2MB0004
41FM5SS0017 41GM2SS0000

WWW.AliSaler.Com

WWW.AliSaler.Com

INDEX

Pg#	Description	DNI LIST
1	Schematic Block Diagram	
2	Front Page	
3-4	Merom	
5-10	Crestline	
11-14	ICH8M	
15-16	DDRII SO-DIMM(200P)	
17	Clock Generator	
18-21	VGA	
22	LCD Conn. & SSP	
23	CRT Conn	
24	SATA & IDE Conn	
25	PCCARD/Conn & 1394	
26	Express Card & Smart Card	
27	Mini Card	
28	MDC Conn.	
29	SIO (MEC5004)	
30	SIO (MEC5018)	
31	SERIAL PORT & USB	
32	Flash ROM	
33	TP,BT & FIR	
34	Switch,Keyboard & LED	
35	FAN & Thermal	
36-37	Audio CODEC(STAC9200)/Phone Jack	
38-39	LOM (BCM5752)/Switch	
40-41	Docking Conn/Q-Switch	
42	System Reset Circuit	
43-44	Battery Selector & Charger	
45	DDR2_1.8VSUS, 0.9V	
46	1.5VSUS,1.05V(VTT)	
47	1.25V,1.05VM	
48	CPU_MAX8786(3phase)	
49	D/D Power	
50	RUN Power Switch	
51	VGA DC/DC	
52	DCIN/Batt Conn.	
53	PAD& SCREW	
54	EMI CAP	

Power & Ground

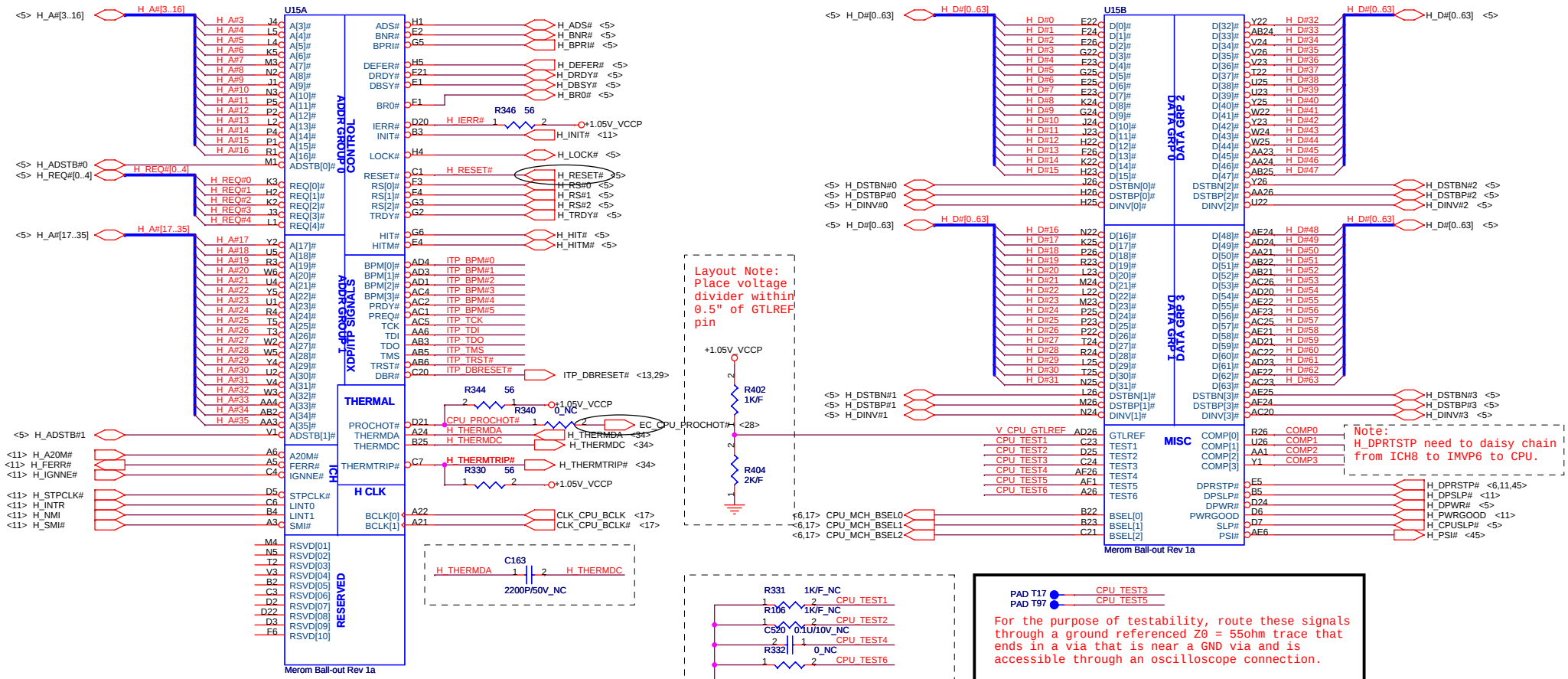
Label	Pg#	Description	Control Signal
DC_IN+		AC ADAPTER (19V)	
PBATT+		MAIN BATTERY + (10~17V)	
PBATT+		SECOND BATTERY + (10~17V)	
PWR_SRC		MAIN POWER (10~19V)	
RTC_PWR3_3V		RTC & +3.3V_RTC_LDO(3.3V)	
+VCC_CORE		CPU CORE POWER (1.5V)	RUNPWROK
+15V_ALW		LARGE POWER (15V)	SUS_ON
+3.3V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+3.3V_SUS		SLP_S5# CTRLD POWER	SUS_ENABLE
+3.3V_ALW		8051 POWER (3.3V)	ALWON/THERM_STP#
+5V_RUN		SLP_S3# CTRLD POWER	RUN_ON
+5V_SUS		SLP_S5# CTRLD POWER	SUS_ON
+5V_HDD		HDD POWER (5V)	+5V_RUN
+5V_MOD		MODULE POWER (5V)	HDDC_EN
+5V_ALW		LCD/CHARGE POWER (5V)	
+VDDA		AUDIO ANALOG POWER (5V)	AUDIO_AVDD_ON
+1.5V_RUN		CALISTOGA/ICH7 POWER	RUN_ON
+1.05V_VCCP		CPU/CALISTOGA/ICH7 POWER	RUN_ON
+1_8V_SUS		SODIMM POWER	SUSPWROK_5V
+1.8V_RUN		SDVO POWER	RUN_ON
+0.9V_DDR_VTT		SODIMM POWER	RUN_ON
+3.3V_LAN		LAN POWER	AUX_EN
GND	ALL PAGES	DIGITAL GROUND	
AGND_ISL6260		CPU GND	
AGND_TPS51120		DC/DC POWER GND	
AGND1		VTT POWER GND	
AGND2		VTT POWER GND	
8731AGND		CHARGER GND	

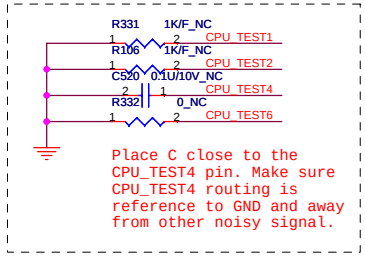
QUANTA COMPUTER

Title	Index, DNI, Power & Ground	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 2 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

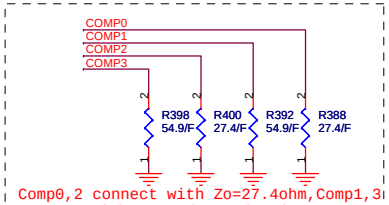




PAD T17 — CPU_TEST3
PAD T97 — CPU_TEST5

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

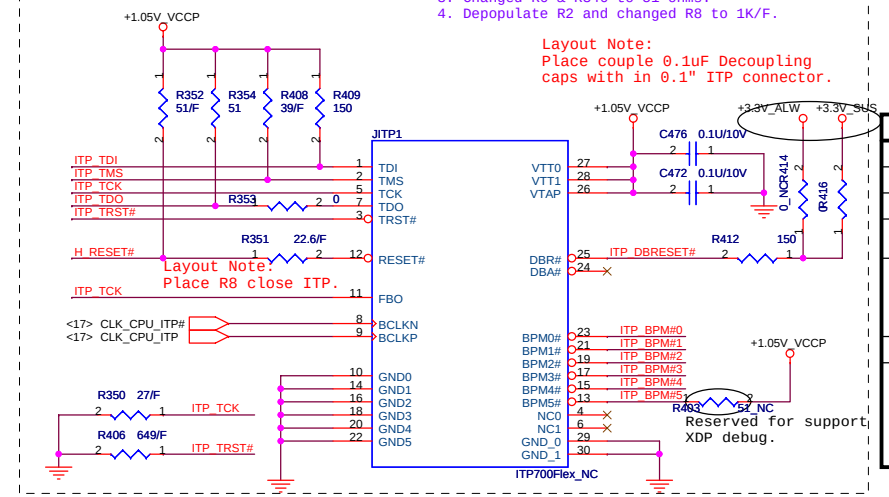


Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

Populate ITP700Flex for bringup

For Support XDP:
1. ITP_BPM#5 need PU 51ohms to +1.05V_VCCP.
2. Change R4 & R361 to 51 ohms.
3. Changed R6 & R346 to 51 ohms.
4. Depopulate R2 and changed R8 to 1K/F.

Layout Note:
Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.



ITP700 layout guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

DELL CONFIDENTIAL/PROPRIETARY

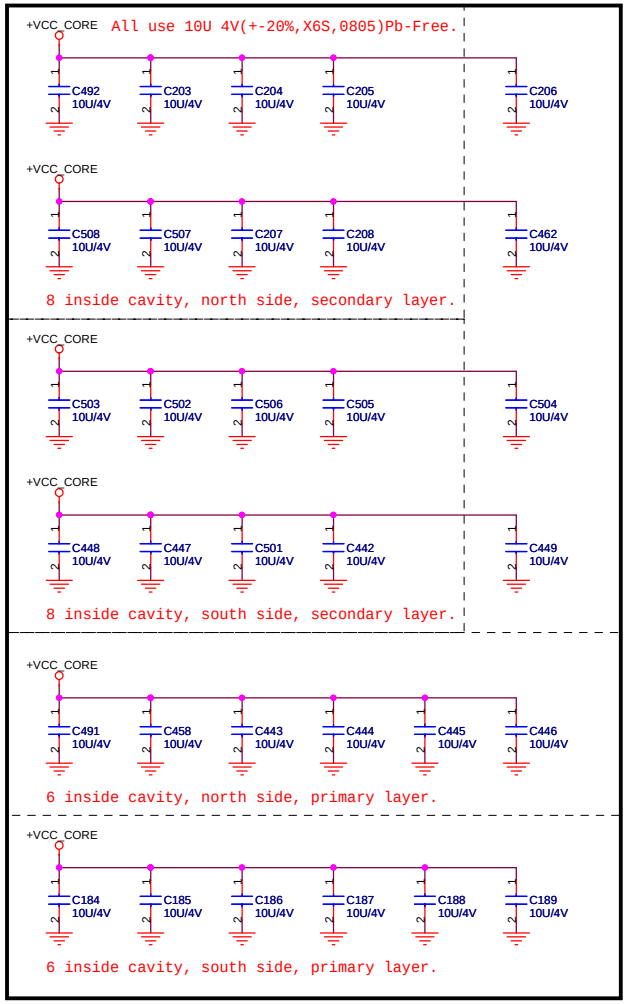
Title: Merom Processor (HOST BUS)

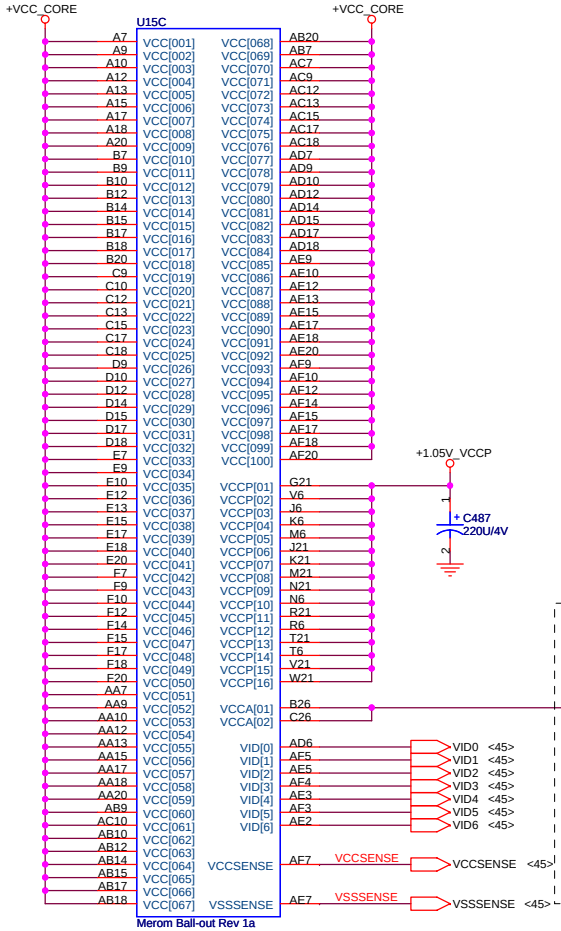
Size: | Document Number: M-08 | Rev: 0.1

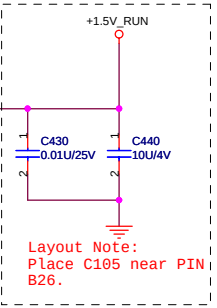
Date: Monday, March 05, 2007 | Sheet 3 of 51

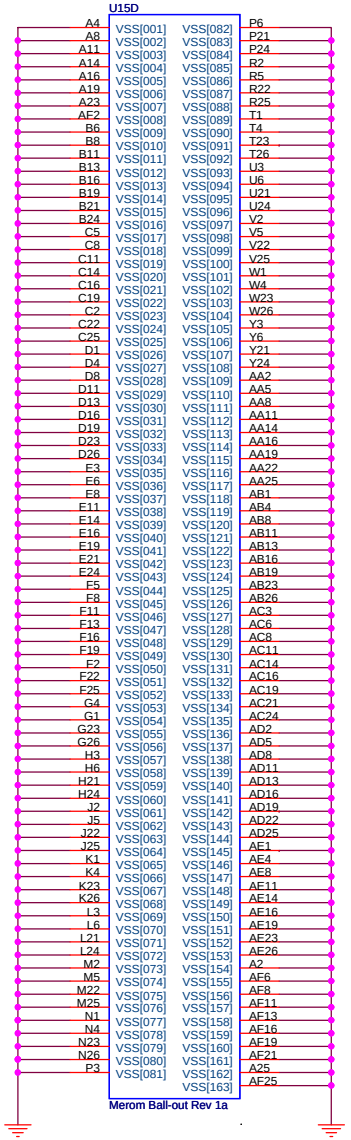
WWW.AliSaler.Com

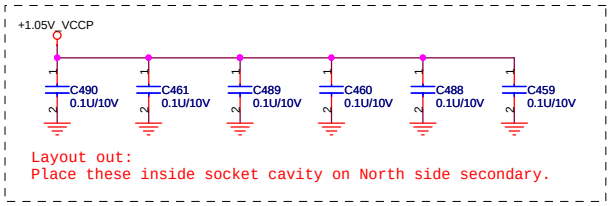
WWW.AliSaler.Com

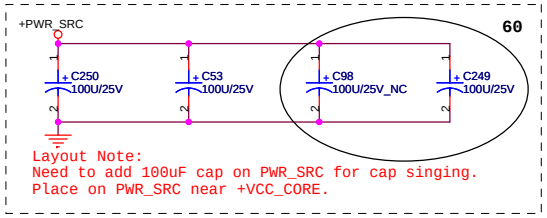


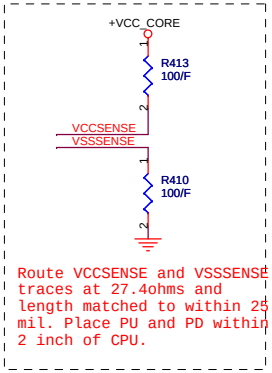










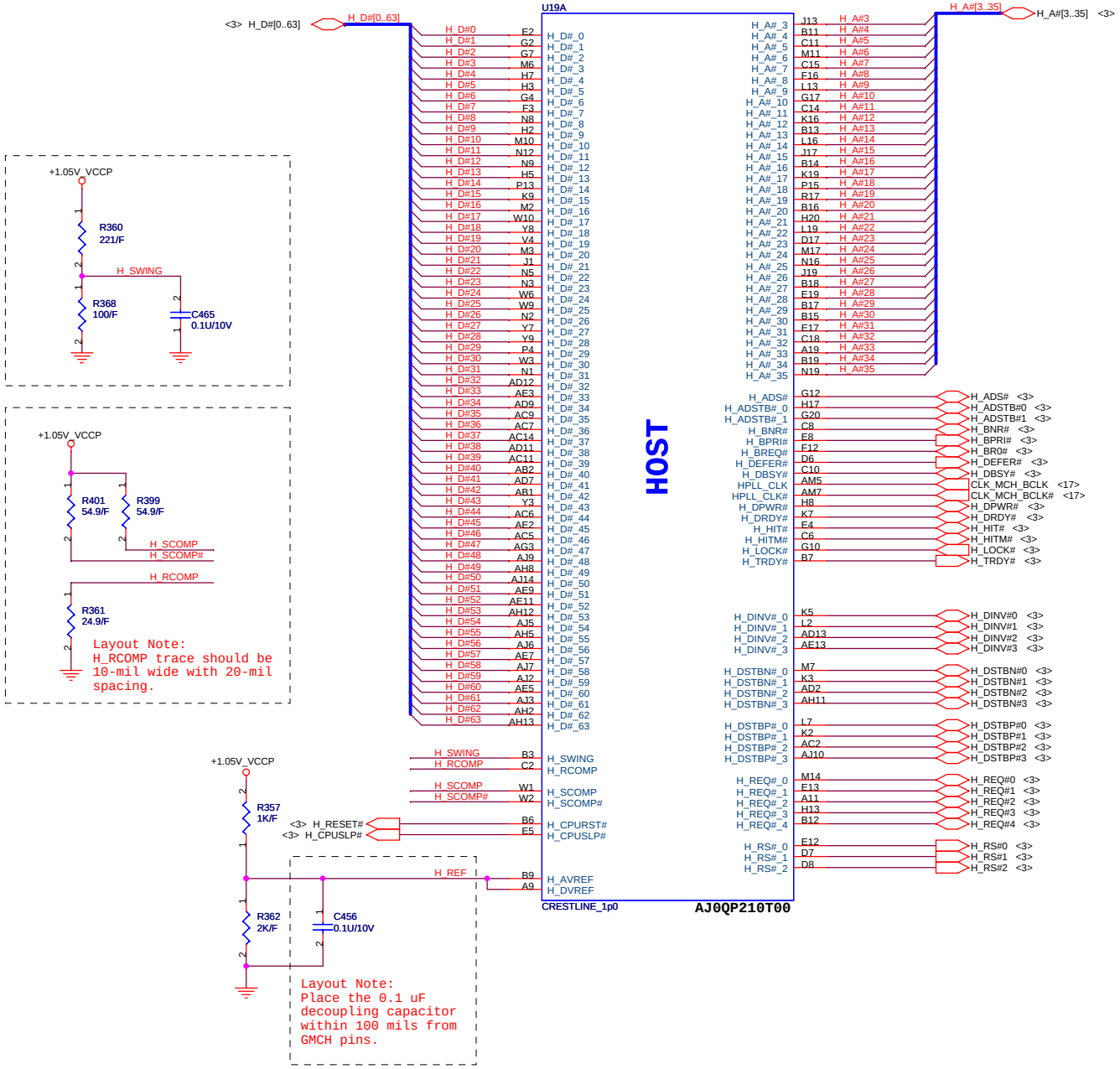


DELL CONFIDENTIAL/PROPRIETARY

Title	Merom Processor (POWER)	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 4 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

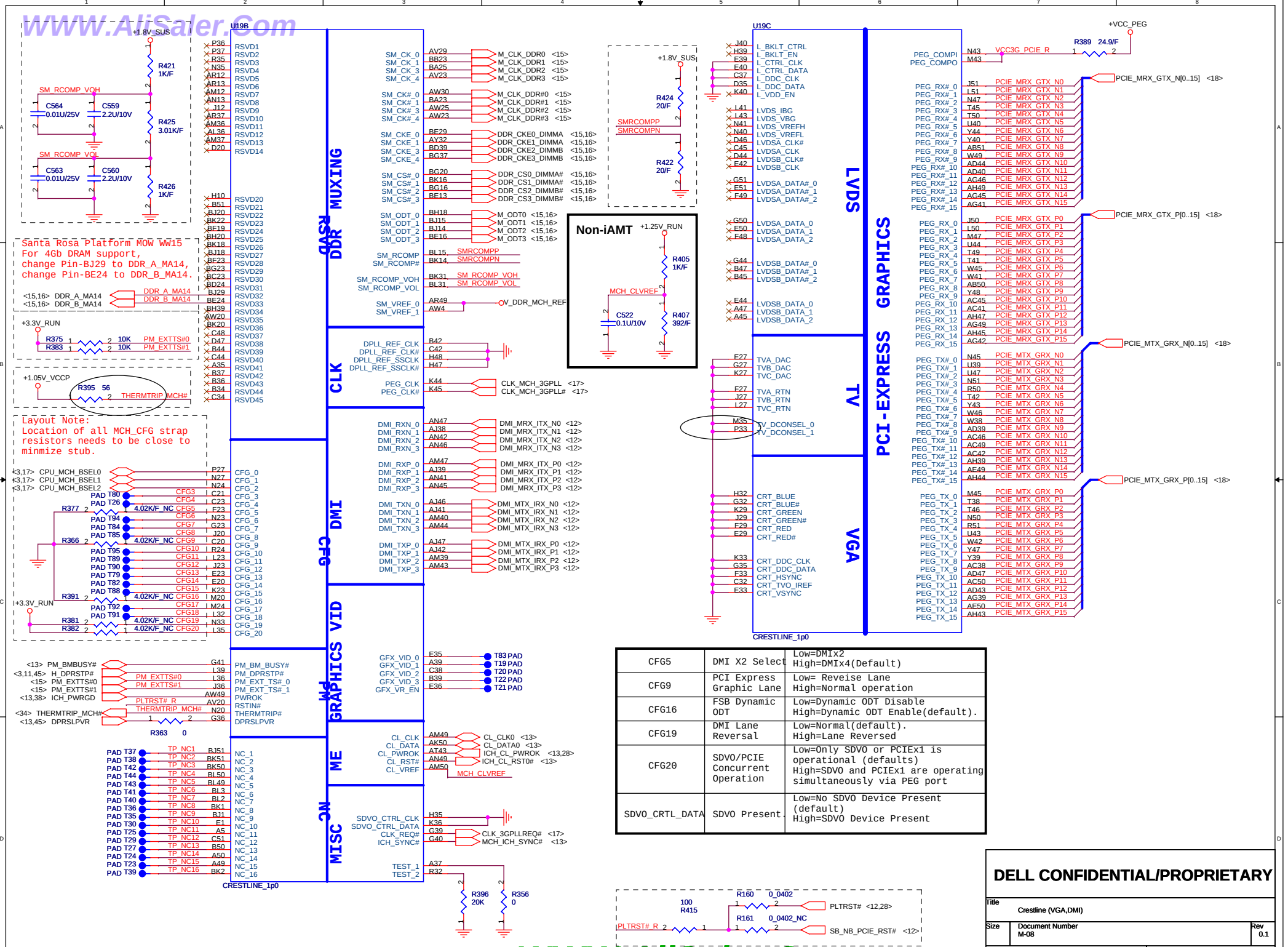


DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (HOST)	
Size	Document Number M-08	Rev 0.1
Date: Tuesday, March 06, 2007	Sheet 5 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

DELL CONFIDENTIAL/PROPRIETARY

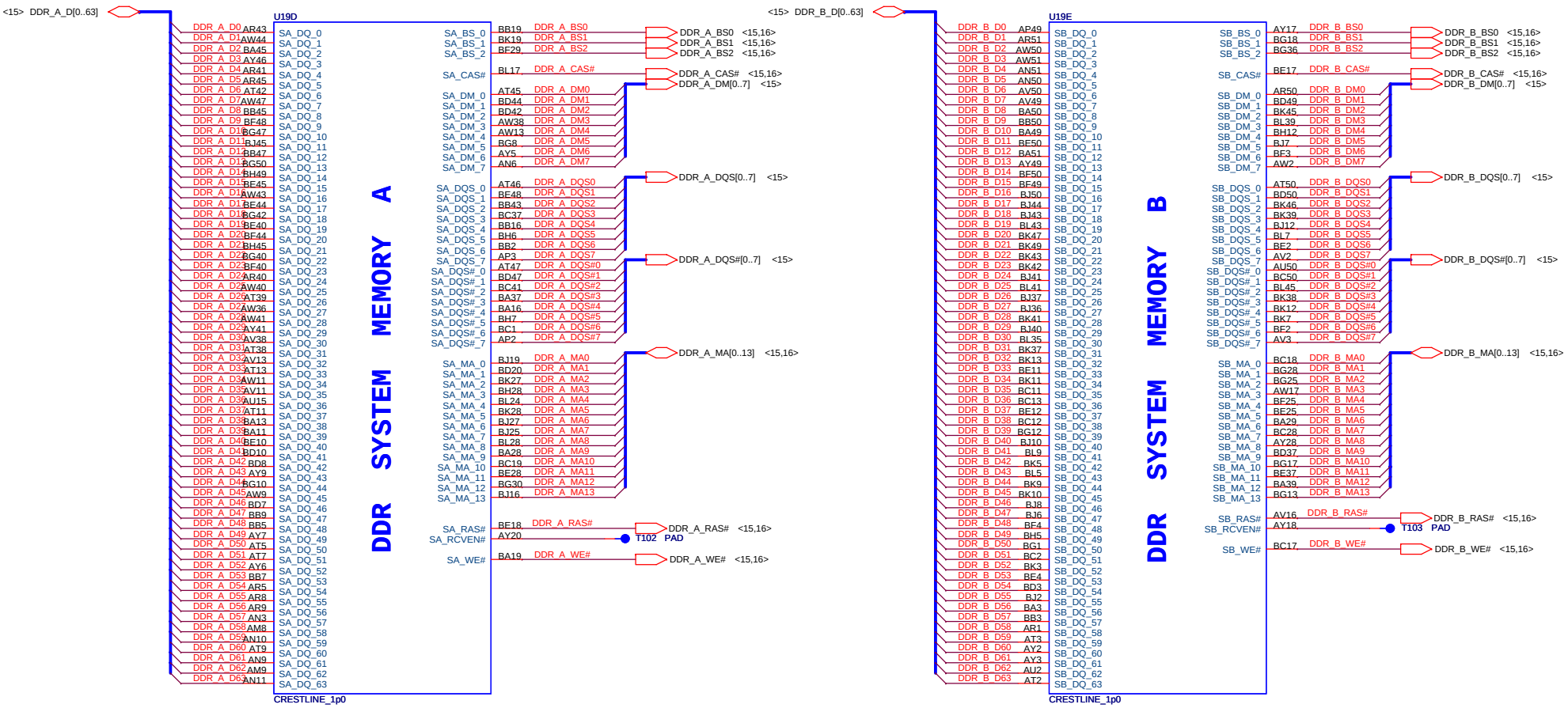
Title: Crestline (VGA,DMI)

Size: | Document Number: M-08 | Rev: 0.1

Date: Tuesday, March 06, 2007 | Sheet 6 of 51

WWW.AliSaler.Com

WWW.AliSaler.Com

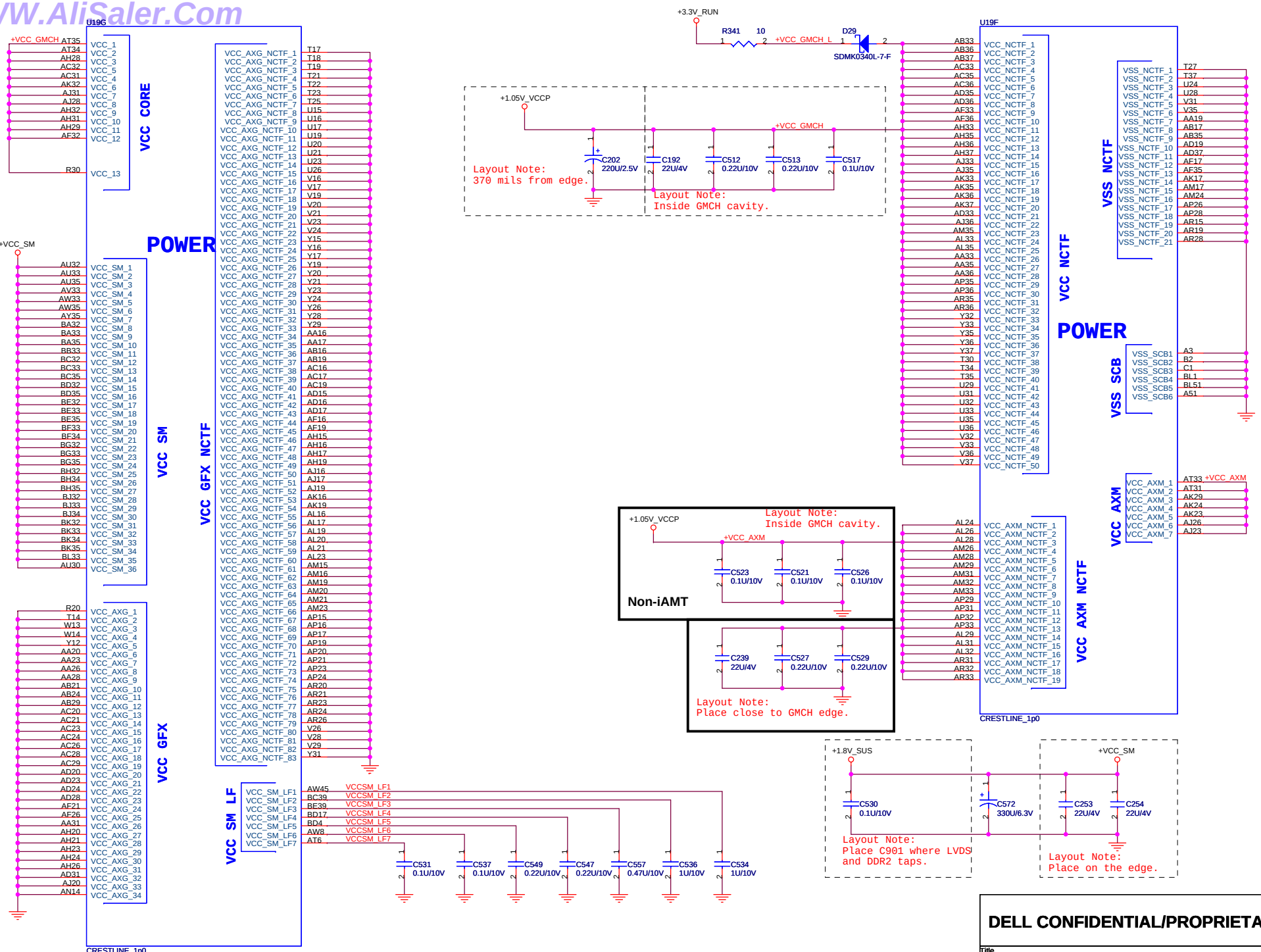


DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (DDR2)		
Size	Document Number M-08		Rev 0.1
Date: Monday, March 05, 2007		Sheet 7 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

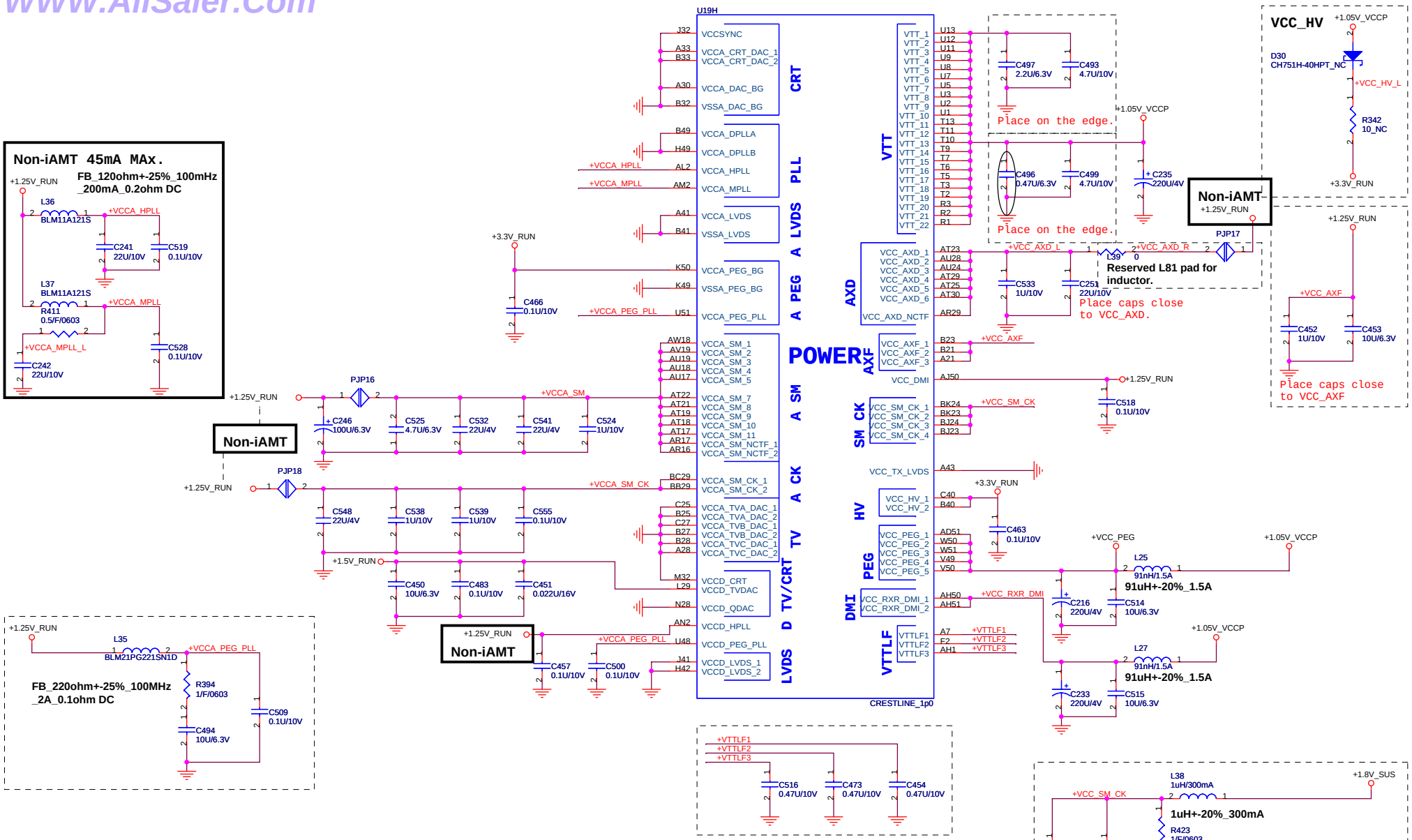


DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (VCC,NCTF)	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 8 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

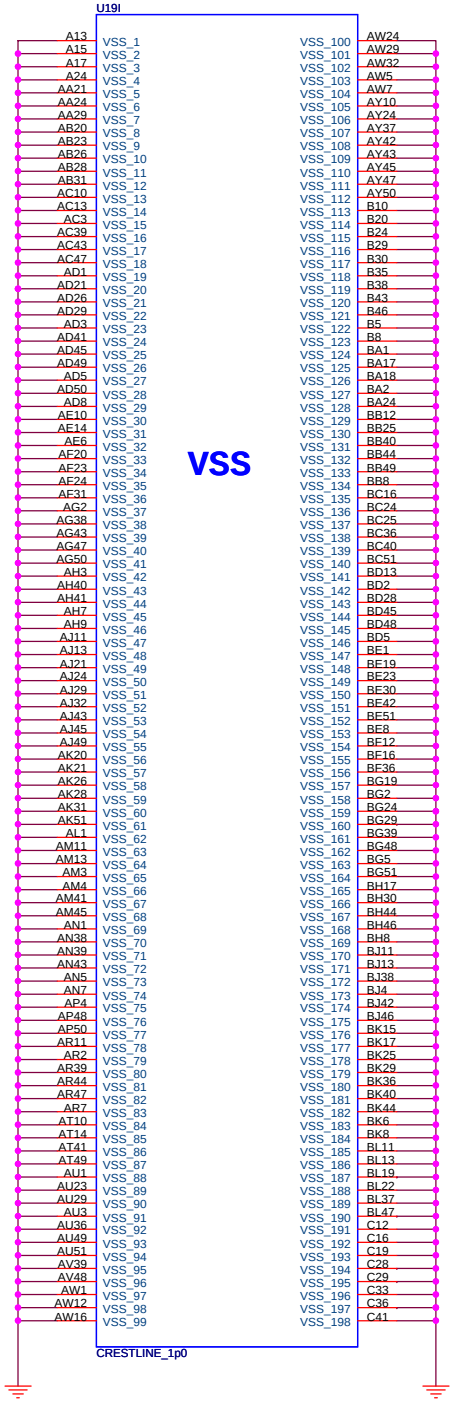


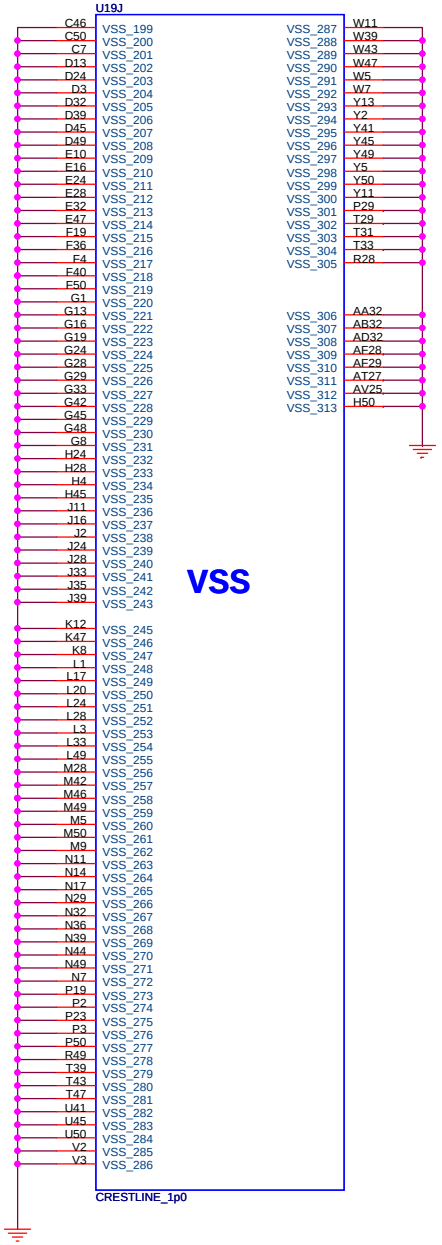
DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (POWER)	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 9 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



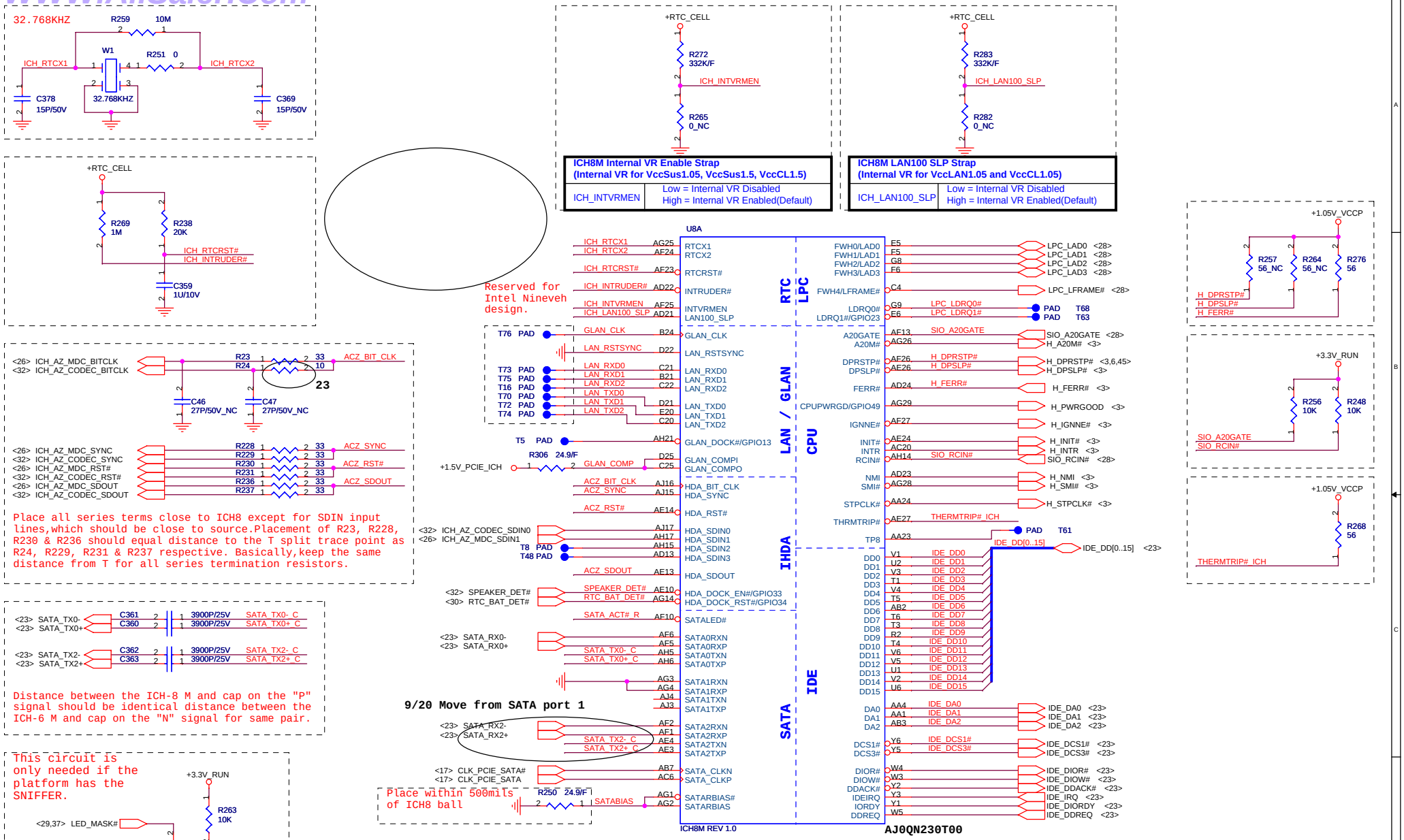


DELL CONFIDENTIAL/PROPRIETARY

Title	Crestline (VSS)	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 10 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



XOR Chain Entrance Strap		
ICH RSVD	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

DELL CONFIDENTIAL/PROPRIETARY

Title: ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)

Size: | Document Number: M-08 | Rev: 0.1

Date: Tuesday, March 06, 2007 | Sheet 11 of 51

WWW.AliSaler.Com

WWW.AliSaler.Com

Place TX DC blocking caps close ICH8.

<25> PCIE_TX1- C90 0.1U/10V PCIE_TXN1_C
<25> PCIE_TX1+ C97 0.1U/10V PCIE_TXP1_C
<24> PCIE_TX2- C101 0.1U/10V PCIE_TXN2_C
<24> PCIE_TX2+ C106 0.1U/10V PCIE_TXP2_C
<24> PCIE_TX3- C114 0.1U/10V PCIE_TXN3_C
<24> PCIE_TX3+ C116 0.1U/10V PCIE_TXP3_C
<26> PCIE_TX4- C127 0.1U/10V PCIE_TXN4_C
<26> PCIE_TX4+ C120 0.1U/10V PCIE_TXP4_C

U8D

<25> PCIE_RX1- P27 PERN1
<25> PCIE_RX1+ P26 PERP1
PCIE_TXN1_C N29 PETN1
PCIE_TXP1_C N28 PETP1
WWAN

<24> PCIE_RX2- M27 PERN2
<24> PCIE_RX2+ M26 PERP2
PCIE_TXN2_C L29 PETN2
PCIE_TXP2_C L28 PETP2
WLAN

<24> PCIE_RX3- K27 PERN3
<24> PCIE_RX3+ K26 PERP3
PCIE_TXN3_C J29 PETN3
PCIE_TXP3_C J28 PETP3
WPAN

<26> PCIE_RX4- H27 PERN4
<26> PCIE_RX4+ H26 PERP4
PCIE_TXN4_C G29 PETN4
PCIE_TXP4_C G28 PETP4
Express Card

F27 PERN5
F26 PERP5
F29 PETN5
F28 PETP5

D27 PERN6/GLAN_RXN
D26 PERP6/GLAN_RXP
C29 PETN6/GLAN_TXN
C28 PETP6/GLAN_TXP

PCI-Express Direct Media Interface

DMI0RXN V27 DMI_MTX_IRX_N0 <6>
DMI0RXP V26 DMI_MTX_IRX_P0 <6>
DMI0TXN U29 DMI_MRX_ITX_N0 <6>
DMI0TXP U28 DMI_MRX_ITX_P0 <6>
DMI1RXN Y27 DMI_MTX_IRX_N1 <6>
DMI1RXP Y26 DMI_MTX_IRX_P1 <6>
DMI1TXN W29 DMI_MRX_ITX_N1 <6>
DMI1TXP W28 DMI_MRX_ITX_P1 <6>
DMI2RXN AB26 DMI_MTX_IRX_N2 <6>
DMI2RXP AB25 DMI_MTX_IRX_P2 <6>
DMI2TXN AA29 DMI_MRX_ITX_N2 <6>
DMI2TXP AA28 DMI_MRX_ITX_P2 <6>
DMI3RXN AD27 DMI_MTX_IRX_N3 <6>
DMI3RXP AD26 DMI_MTX_IRX_P3 <6>
DMI3TXN AC29 DMI_MRX_ITX_N3 <6>
DMI3TXP AC28 DMI_MRX_ITX_P3 <6>
DMI_CLKN T26 CLK_PCIE_ICH# <17>
DMI_CLKP T25 CLK_PCIE_ICH <17>
DMI_ZCOMP Y23
DMI_IRCOMP Y24 DMI_COMP R281 24.9/F +1.5V_PCIE_ICH

Place within 500mils of ICH8

USB

USBP0N G3 ICH_USBP0- <27>
USBP0P G2 ICH_USBP0+ <27> USB[1B]
USBP1N H5 ICH_USBP1- <27>
USBP1P H4 ICH_USBP1+ <27> USB[1A]
USBP2N H2 ICH_USBP2- <27>
USBP2P H1 ICH_USBP2+ <27> USB[2B]
USBP3N J3 ICH_USBP3- <27>
USBP3P J2 ICH_USBP3+ <27> USB[2A]
USBP4N K5 ICH_USBP4- <24>
USBP4P K4 ICH_USBP4+ <24> 3rd MINI CARD
USBP5N K2 ICH_USBP5- <33>
USBP5P K1 ICH_USBP5+ <33> CAMERA
USBP6N L3 ICH_USBP6- <26>
USBP6P L2 ICH_USBP6+ <26> Express Card
USBP7N M5 ICH_USBP7- <37>
USBP7P M4 ICH_USBP7+ <37> BT
USBP8N M2 ICH_USBP8- <27>
USBP8P M1 ICH_USBP8+ <27> USB[3A]
USBP9N N3 ICH_USBP9- <25>
USBP9P N2 ICH_USBP9+ <25> WWAN USB

USBRBIAS# F2
USBRBIAS F3 USBRBIAS

SPI

ICH_EC_SPI_CLK_R C23 SPI_CLK
ICH_SPI_CS# B23 SPI_CS0#
ICH_SPI_CS1_R E22 SPI_CS1#
ICH_EC_SPI_DO_R D23 SPI_MOSI
F21 SPI_MISO

OC0# AJ19 USB_OC0_1#
OC1#/GPIO40 AG16
OC2#/GPIO41 AG15 USB_OC2_3#
OC3#/GPIO42 AE15
OC4#/GPIO43 AF15 OC4#
OC5#/GPIO29 AG17 OC5#
OC6#/GPIO30 AD12 OC6#
OC7#/GPIO31 AJ18 OC7#
OC8# AD14 USB_OC8#
OC9# AH18 OC9#

ICH8M REV 1.0

Non-iAMT

RP27 10P8R-10K +3.3V_SUS
OC7# 6 5 USB_OC0_1#
OC9# 7 4 USB_OC2_3#
OC5# 8 3 OC4#
OC6# 9 2 USB_OC8#
+3.3V_SUS 10 1

Layout Note:
Place R313,R311 and R327
within 500 mils from ICH.

<28> ICH_EC_SPI_CLK R313 15 ICH_EC_SPI_CLK_R
<28> ICH_EC_SPI_DO R311 15 ICH_EC_SPI_DO_R
<28> ICH_EC_SPI_DIN

+3.3V_ALW
<30> SPI_CS0# R328 15_NC U11 7SH08_NC R327 15 ICH_SPI_CS#
R93 0 SIO_SPI_CS# <28>
<27> USB_OC8#

PCI Pullups

RP35 10P8R-8.2K +3.3V_RUN
PCI_STOP# PCI_FRAME# PCI_REQ1#

RP34 10P8R-8.2K +3.3V_RUN
PCI_SERR# SB_WLAN_PCIE_RST# PCI_TRDY# SB_MCARD3_PCIE_RST#
PCI_PIRQD# SB_NB_PCIE_RST# PCI_DEVSEL#

RP31 10P8R-8.2K +3.3V_RUN
PCI_PERR# PCI_IRDY# PCI_PIRQA# PCI_REQ0#
PCI_PIRQC# PCI_PLOCK# PCI_PIRQB#

35

WWAN Noise - ICH improvements 18

OC4# C876 0.1U/10V
OC5# C871 0.1U/10V
OC6# C872 0.1U/10V
OC7# C873 0.1U/10V
OC9# C878 0.1U/10V
USB_OC8# C874 0.1U/10V
USB_OC0_1# C875 0.1U/10V
USB_OC2_3# C877 0.1U/10V

ICH_SPI_CS1_R
PCI_GNT0#
R304 1K R292 1K_NC

Boot BIOS Strap		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

R301 22.6/F

LOM	REQ0	GNT0	PIRQB
1394/MediaCard	REQ1	GNT1	PIRQC PIRQD

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

C84 0.047U/10V +3.3V_SUS U10 7SH32
PCI_RST# G PCI_RST# <20,35>

C357 0.047U/10V +3.3V_SUS U28 7SH32
PCI_PLTRST# PLTRST# <6,28>

C355 0.047U/10V +3.3V_SUS U27 7SH32
PCI_PLTRST# PLTRST1# <24,25,26>

U8B

<20,35> PCI_AD[0..31]

PCI_AD0 D20 AD0
PCI_AD1 E19 AD1
PCI_AD2 D19 AD2
PCI_AD3 A20 AD3
PCI_AD4 D17 AD4
PCI_AD5 A21 AD5
PCI_AD6 A19 AD6
PCI_AD7 C19 AD7
PCI_AD8 A18 AD8
PCI_AD9 B16 AD9
PCI_AD10 A12 AD10
PCI_AD11 E16 AD11
PCI_AD12 A14 AD12
PCI_AD13 G16 AD13
PCI_AD14 A15 AD14
PCI_AD15 B6 AD15
PCI_AD16 C11 AD16
PCI_AD17 A9 AD17
PCI_AD18 D11 AD18
PCI_AD19 B12 AD19
PCI_AD20 C12 AD20
PCI_AD21 D10 AD21
PCI_AD22 C7 AD22
PCI_AD23 F13 AD23
PCI_AD24 E11 AD24
PCI_AD25 E13 AD25
PCI_AD26 E12 AD26
PCI_AD27 D8 AD27
PCI_AD28 A6 AD28
PCI_AD29 E8 AD29
PCI_AD30 D6 AD30
PCI_AD31 A3 AD31

PCI

REQ0# A4 PCI_REQ0# PCI_REQ0# <35>
GNT0# D7 PCI_GNT0# PCI_GNT0# <35>
REQ1#/GPIO50 E18 PCI_REQ1# PCI_REQ1# <20>
GNT1#/GPIO51 C18 PCI_GNT1# PCI_GNT1# <20>
REQ2#/GPIO52 B19 SB_WWAN_PCIE_RST# SB_WWAN_PCIE_RST# <25>
GNT2#/GPIO53 E18
REQ3#/GPIO54 A11 SB_LOM_PCIE_RST# SB_LOM_PCIE_RST#
GNT3#/GPIO55 C10

C/BE0# C17 PCI_C_BE0# <20,35>
C/BE1# E15 PCI_C_BE1# <20,35>
C/BE2# E16 PCI_C_BE2# <20,35>
C/BE3# E17 PCI_C_BE3# <20,35>

IRDY# C8 PCI_IRDY# PCI_IRDY# <20,35>
PAR D9 PCI_PAR <20,35>
PCIRST# G6 PCI_RST# G
DEVSEL# D16 PCI_DEVSEL# PCI_DEVSEL# <20,35>
PERR# A7 PCI_PERR# PCI_PERR# <20,35>
PLOCK# B7 PCI_PLOCK# PCI_PLOCK#
SERR# E10 PCI_SERR# PCI_SERR# <20,35>
STOP# C16 PCI_STOP# PCI_STOP# <20,35>
TRDY# C9 PCI_TRDY# PCI_TRDY# <20,35>
FRAME# A17 PCI_FRAME# PCI_FRAME# <20,35>

PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH CLK_PCI_ICH <17>
PME# G7 ICH_PME# <29>

Interrupt I/F

PIRQA# F9 PIRQE#/GPIO2 E8 SB_MCARD3_PCIE_RST# SB_MCARD3_PCIE_RST# <24>
PIRQB# B5 PIRQF#/GPIO3 G11 SB_WLAN_PCIE_RST# SB_WLAN_PCIE_RST# <24>
PIRQC# C5 PIRQG#/GPIO4 E12 SB_NB_PCIE_RST# SB_NB_PCIE_RST# <6>
PIRQD# A10 PIRQH#/GPIO5 B3 PCIE_MCARD2_DET# PCIE_MCARD2_DET# <25>

<35> PCI_PIRQB#
<20> PCI_PIRQC#
<20> PCI_PIRQD#

ICH8M REV 1.0

35

PCI_PIRQB: for LOM
PCI_PIRQC: for Media Card
PCI_PIRQD: for 1394

SB_NB_PCIE_RST#
R307 1K_NC

A16 away override strap.	
SB_NB_PCIE_RST#	Low = A16 swap override enabled. High = Default.

SB_MCARD3_PCIE_RST# R291 20K_NC
SB_WWAN_PCIE_RST# R314 20K
SB_WLAN_PCIE_RST# R300 20K_NC
SB_LOM_PCIE_RST# R324 20K
SB_NB_PCIE_RST# R302 20K_NC

BIOS should not enable the internal GPIO pull up resistor.

CLK_PCI_ICH
R310 10
C417 9P/50V

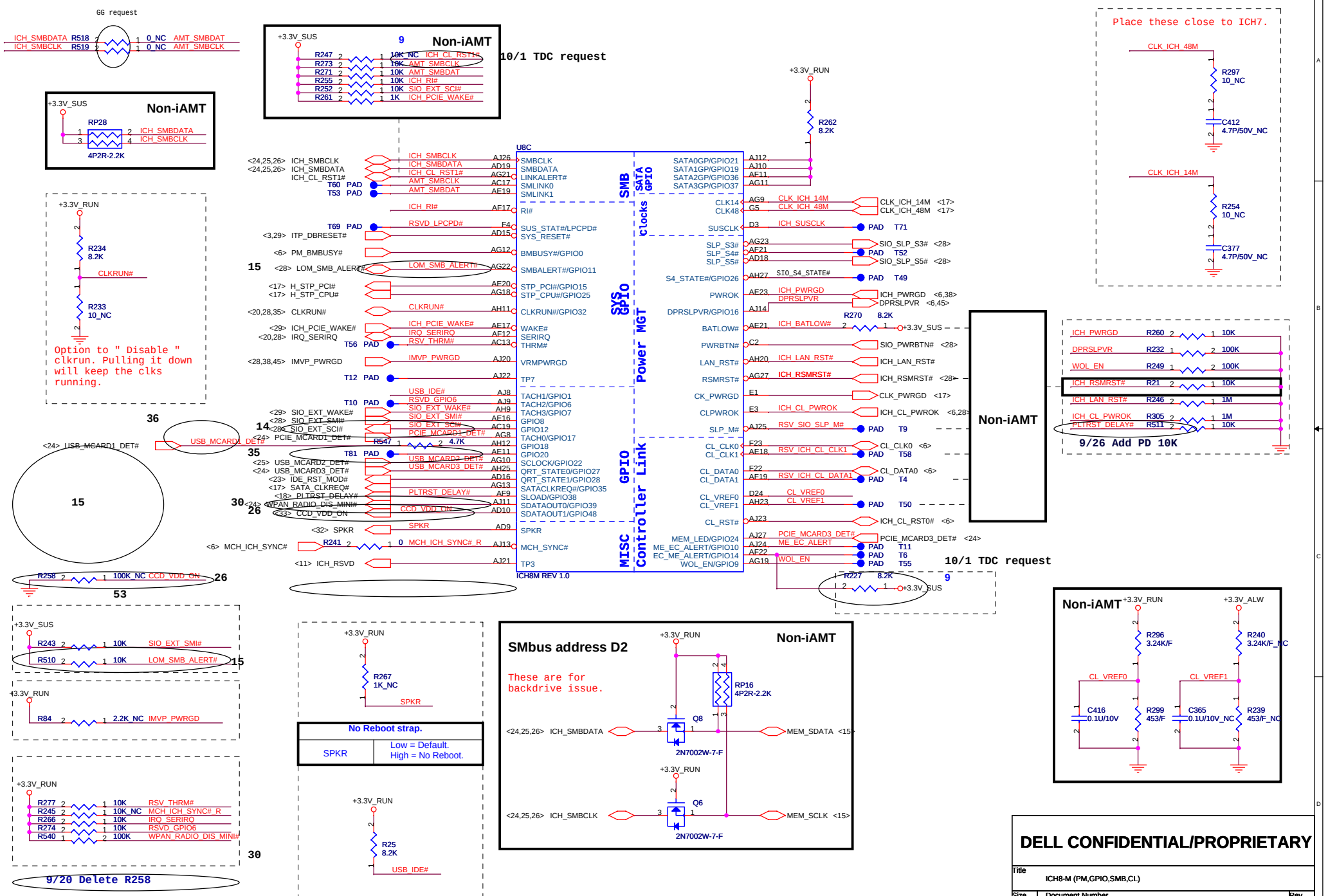
Reserved for EMI. Place resister and cap close to ICH.

DELL CONFIDENTIAL/PROPRIETARY

Title	ICH8-M (USB,DMI,PCIE,PCI)	
Size	Document Number M-08	Rev 0.1
Date: Tuesday, March 06, 2007	Sheet 12 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

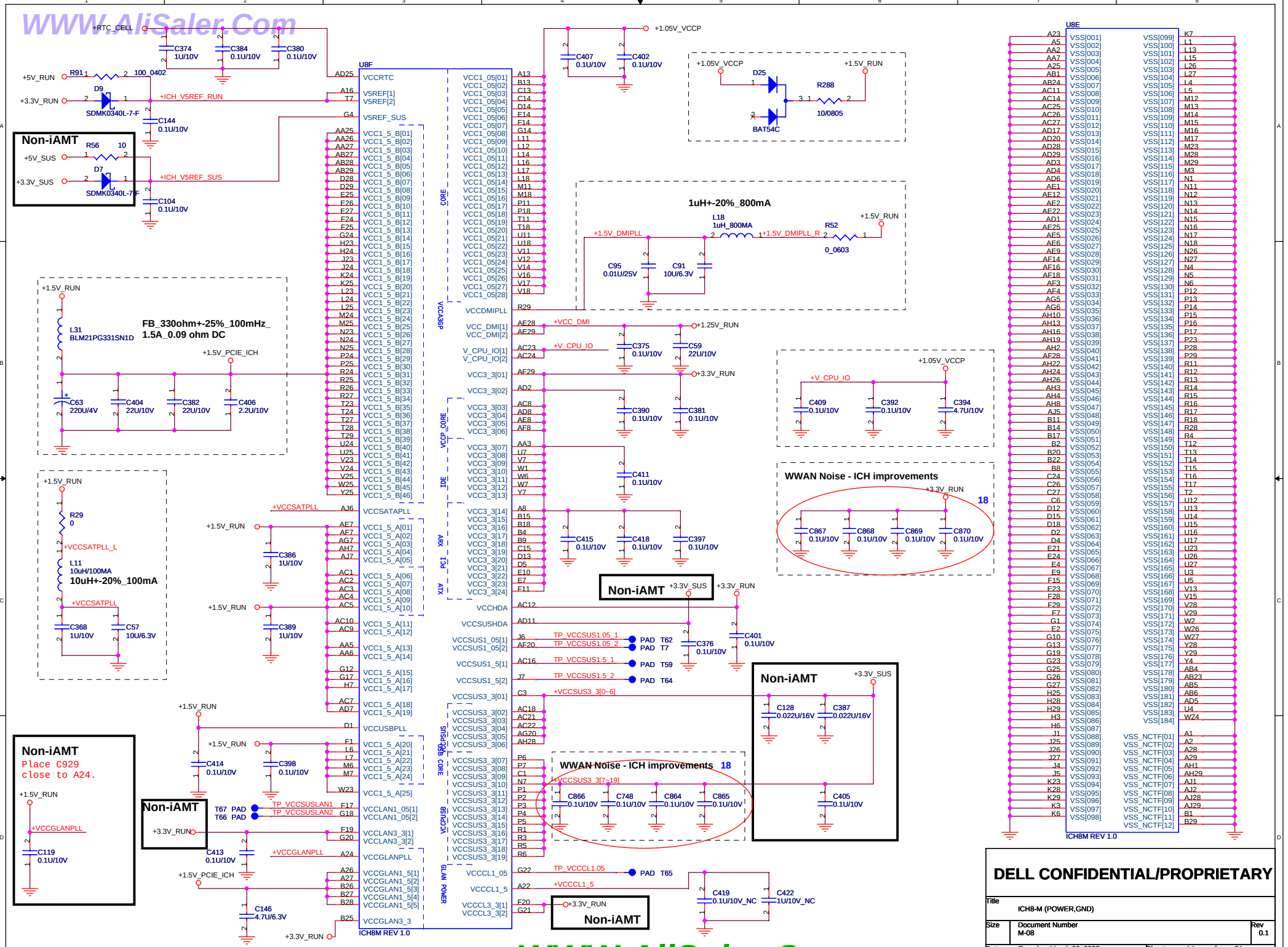


DELL CONFIDENTIAL/PROPRIETARY

Title	ICH8-M (PM,GPIO,SMB,CL)
Size	Document Number M-08
Rev	0.1
Date:	Tuesday, March 06, 2007
Sheet	13 of 51

WWW.AliSaler.Com

WWW.AliSaler.Com



DELL CONFIDENTIAL/PROPRIETARY

Title	ICH8-M (POWER,GND)	
Size	Document Number M-08	Rev 0.1
Date: Tuesday, March 06, 2007	Sheet 14 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

A is required to route to Top SoDIMM for AMTto function.
Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_AS0A426-N2RN-7F

+1.8V_SUS, V_DDR_MCH_REF

DDR_A_DM[0..7] <7>
DDR_A_D[0..63] <7>
DDR_A_DQS[0..7] <7>
DDR_A_DQS#[0..7] <7>
DDR_A_MA[0..14] <6,7,16>

V_DDR_MCH_REF: C277 0.1U/10V, C276 2.2U/6.3V

M_CLK_DDR0 <6>
M_CLK_DDR#0 <6>

PM_EXTTS#0 <6>

<6,16> DDR_CKE0_DIMMA
DDR_CKE1_DIMMA <6,16>
<6,16> DDR_CKE2_DIMMB

<7,16> DDR_A_BS2

<7,16> DDR_A_BS0
<7,16> DDR_A_WE#
<7,16> DDR_A_CAS#
<6,16> DDR_CS1_DIMMA#
<6,16> M_ODT1

DDR_A_BS1 <7,16>
DDR_A_RAS# <7,16>
DDR_CS0_DIMMA# <6,16>
M_ODT0 <6,16>

<13> MEM_SDATA
<13> MEM_SCLK
+3.3V_RUN

R169 10K, R170 10K

SMbus address A0

Non-iAMT

CLOCK 0,1
CKE 0,1

+3.3V_RUN, Non-iAMT: C580 2.2U/6.3V, C579 0.1U/10V

BOT

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_ AS0A426-N2SN-7F

+1.8V_SUS, V_DDR_MCH_REF

DDR_B_DM[0..7] <7>
DDR_B_D[0..63] <7>
DDR_B_DQS[0..7] <7>
DDR_B_DQS#[0..7] <7>
DDR_B_MA[0..14] <6,7,16>

V_DDR_MCH_REF: C274 0.1U/10V, C275 2.2U/6.3V

M_CLK_DDR2 <6>
M_CLK_DDR#2 <6>

PM_EXTTS#1 <6>

<6,16> DDR_CKE3_DIMMB <6,16>

<7,16> DDR_B_BS2

DDR_B_BS1 <7,16>
DDR_B_RAS# <7,16>
DDR_CS2_DIMMB# <6,16>
M_ODT2 <6,16>

<7,16> DDR_B_BS0
<7,16> DDR_B_WE#
<7,16> DDR_B_CAS#
<6,16> DDR_CS3_DIMMB#
<6,16> M_ODT3

M_CLK_DDR3 <6>
M_CLK_DDR#3 <6>

R449 10K

R448 10K

SMbus address A4

Non-iAMT

CLOCK 2,3
CKE 2,3

Place these Caps near So-Dimm1.
+1.8V_SUS: C270 2.2U/6.3V, C269 2.2U/6.3V, C279 2.2U/6.3V, C280 2.2U/6.3V, C281 2.2U/6.3V

Place these Caps near So-Dimm2.
+1.8V_SUS: C588 2.2U/6.3V, C575 2.2U/6.3V, C586 2.2U/6.3V, C587 2.2U/6.3V, C576 2.2U/6.3V

Place these Caps near So-Dimm1.
+1.8V_SUS: C272 0.1U/10V, C278 0.1U/10V, C271 0.1U/10V, C273 0.1U/10V

Place these Caps near So-Dimm2.
+1.8V_SUS: C574 0.1U/10V, C584 0.1U/10V, C578 0.1U/10V, C577 0.1U/10V

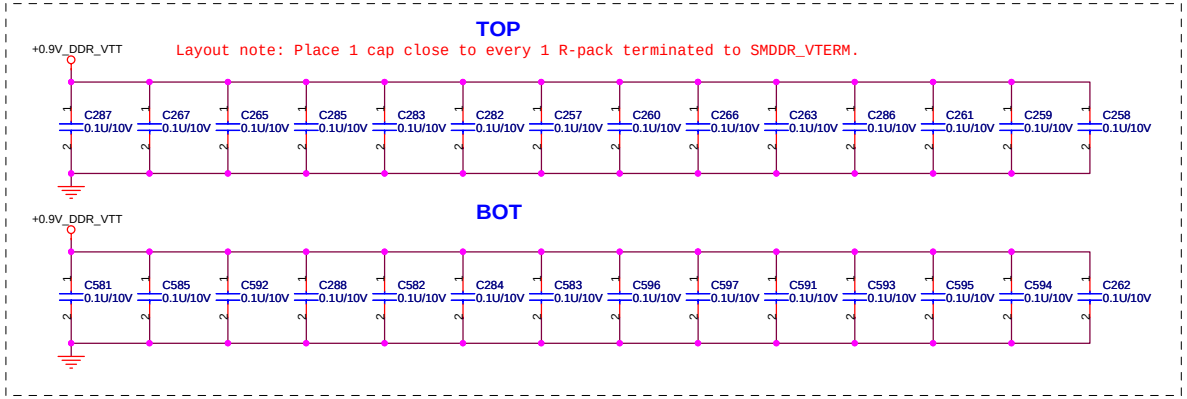
+3.3V_RUN, Non-iAMT: C264 2.2U/6.3V, C268 0.1U/10V

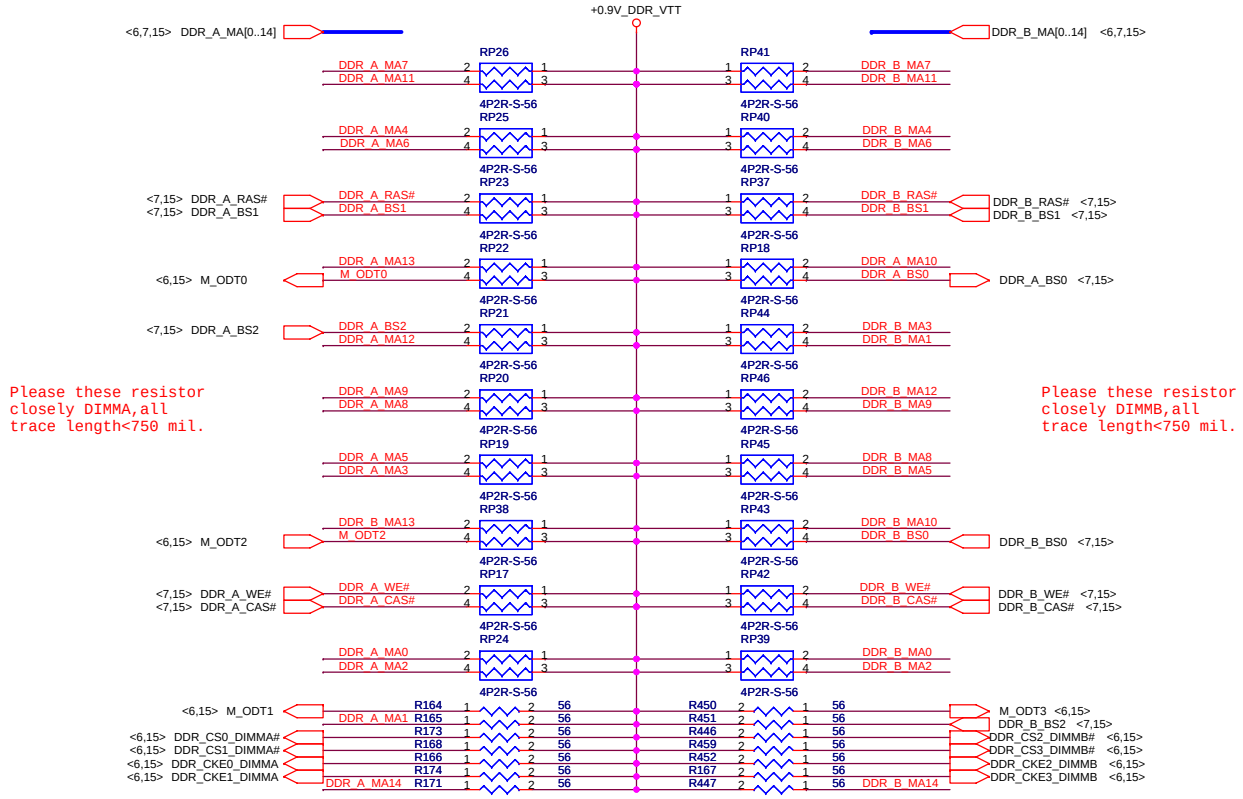
DELL CONFIDENTIAL/PROPRIETARY

Title	DDR2 SO-DIMM (200P) X 2	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 15 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



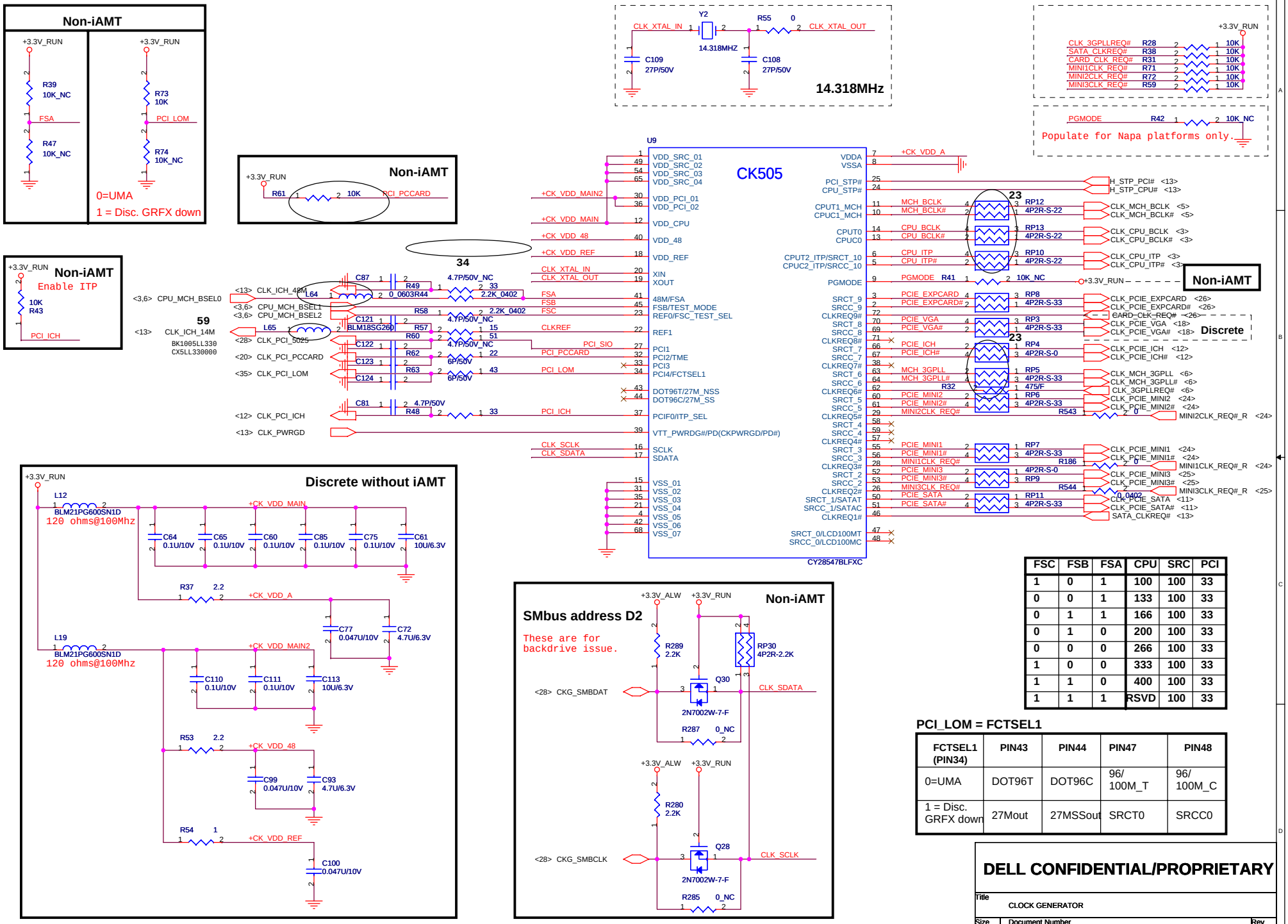


DELL CONFIDENTIAL/PROPRIETARY

Title	DDR2 RES ARRAY	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 16 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

DELL CONFIDENTIAL/PROPRIETARY

Title	CLOCK GENERATOR	
Size	Document Number M-08	Rev 0.1
Date: Wednesday, March 07, 2007	Sheet 17 of 51	

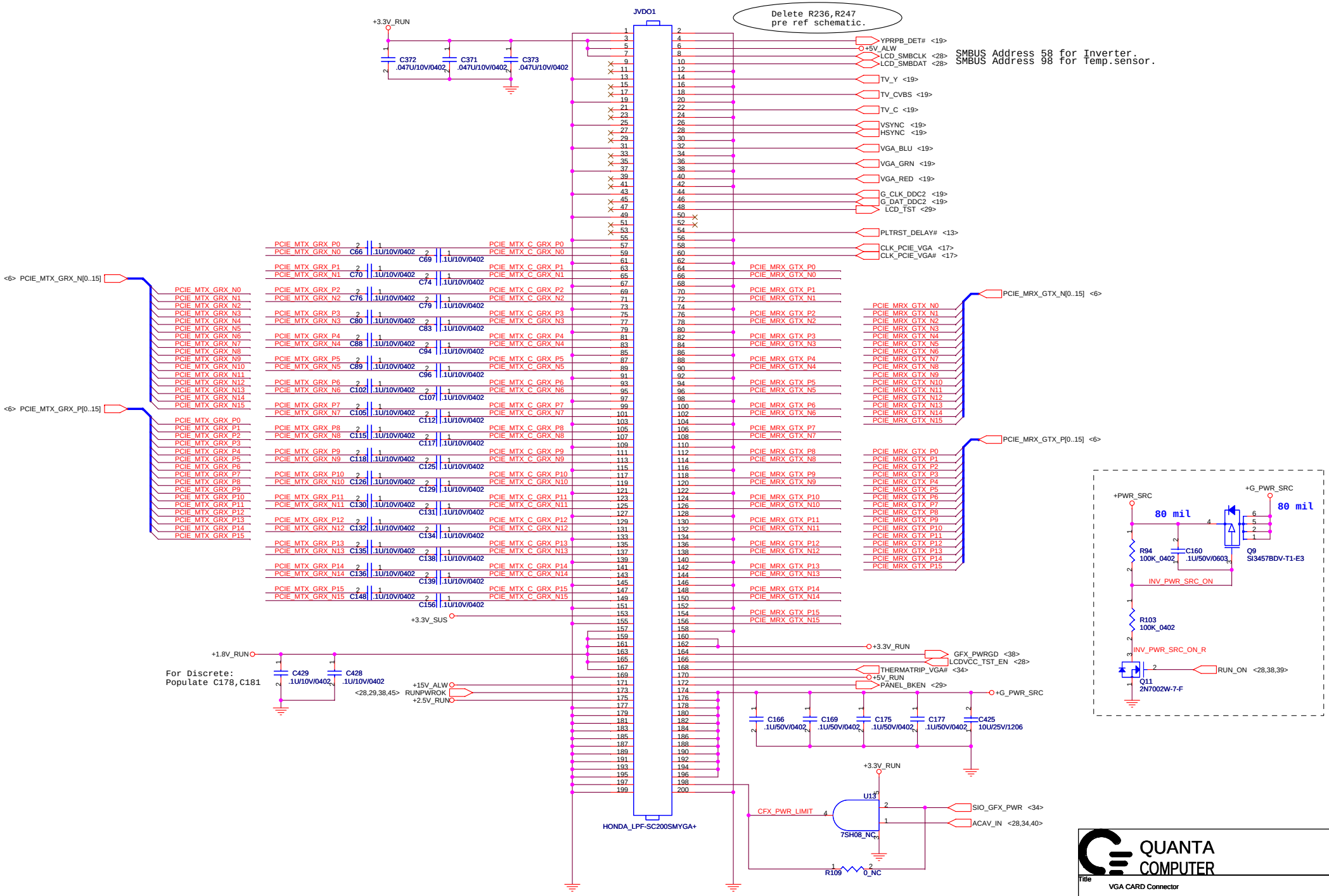
WWW.AliSaler.Com

WWW.AliSaler.Com

YPRPB_DET: SIGNAL FROM SVIDEO CONNECTOR,
TO SWICH TO COMPONENT OUT.

Delete R236,R247
pre ref schematic.

SMBUS Address 58 for Inverter.
SMBUS Address 98 for Temp.sensor.



QUANTA COMPUTER

Title	VGA CARD Connector	
Size	Document Number FM1	Rev 0.1
Date: Monday, March 05, 2007	Sheet 18 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

Setting R,G,B treac
impedance to 50 ohm.

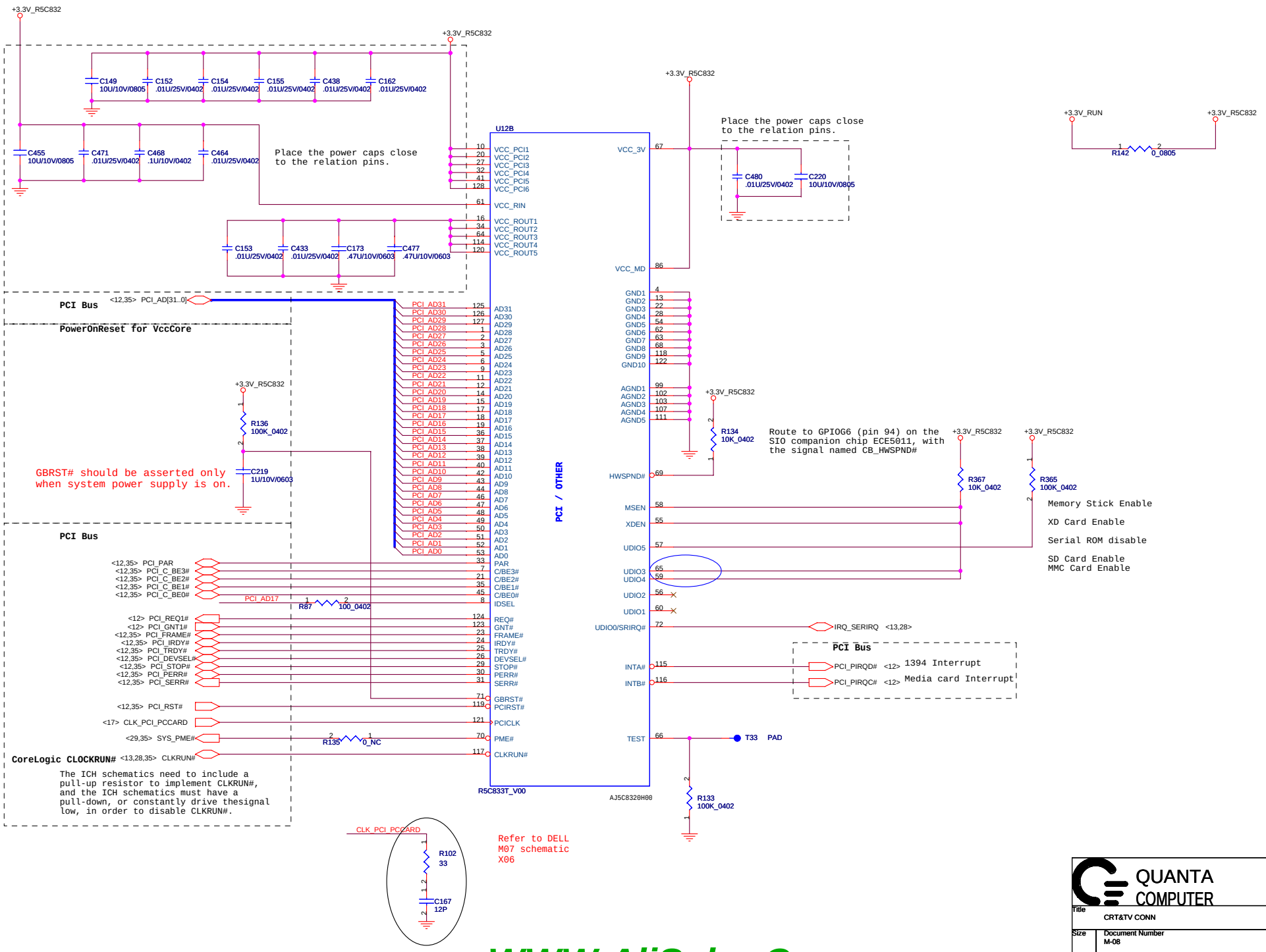
<18> VGA_RED
<18> VGA_GRN
<18> VGA_BLU
L13 BLM11B750SB
L14 BLM11B750SB
L16 BLM11B750SB
R45 150/F
R35 150/F
R33 150/F
C86 22P/50V_NC
C68 22P/50V_NC
C62 22P/50V_NC
C82 10P/50V_NC
C73 10P/50V_NC
C67 10P/50V_NC
RED
GREEN
BLUE
PAD T14 M_SEN# R
PAD T15 M_ID2#
+5V_RUN
D22 SDM10K45-7-F
R279 0/1206
JVGA1
CRT_VCC
FOX_DZ11A91-NB211-9F
Place D23,D24,D26 close
to JVGA1 <200 mils
+3.3V_RUN
D23 DA204U_NC
D24 DA204U_NC
D26 DA204U_NC
CRT_VCC
RP29 4P2R-2.2K
<18> G_DAT_DDC2
<18> G_CLK_DDC2
C395 10P/50V_NC
C399 10P/50V_NC
+5V_RUN
D27 SDM10K45-7-F
R290 1K
C400 0.01U/25V
<18> HSYNC
U29 74AHCT1G125GW
VGAHSYNC_R
R286 10
C408 0.1U/10V
Place near U29
, U30 < 200 mil
<18> VSYNC
U30 74AHCT1G125GW
VGAVSYNC_R
R293 10
L15 BLM11A121S
L17 BLM11A121S
JVGA_HS
JVGA_VS
C78 10P/50V
C92 10P/50V
C103 10P/50V_NC
C71 10P/50V_NC
Place near JVGA1 connector <
200 mil
Place All of those
Inductors Caps close
to JTV <200 mils
<18> TV_C
C5 22P_NC
L4 BLM18BD151SN1D
R6 150/F_0402
C10 6P/50V/0402
C6 6P/50V/0402
SVIDEO_C
SVIDEO_CVBS
<18> TV_Y
C7 22P_NC
L5 BLM18BD151SN1D
R7 150/F_0402
C11 6P/50V/0402
C8 6P/50V/0402
SVIDEO_Y
<18> TV_CVBS
C3 22P_NC
L3 BLM18BD151SN1D
R5 150/F_0402
C9 6P/50V/0402
C4 6P/50V/0402
JTV1
FOX_MH1177L-BG6N-7FL
11/1 Update FP
Update it
per ref
schematic.
+3.3V_RUN
D21 DA204U_NC
D20 DA204U_NC
D19 DA204U_NC
SVIDEO_C
SVIDEO_Y
SVIDEO_CVBS
+5V_RUN
C336 .1U/10V/0402
R212 10K
<32> AUD_SPDIF_OUT
U4 74AHCT1G125GW
SP_DIF
R214 220_0603
SP_DIFB
C337 .01U/25V/0402
SP_DIFC
R213 0_0805
SP_DIF_D
R210 0_0603_NC
R211 110_0603
Add R213 pre
ref
schematic.
+3.3V_RUN
R218 47K_0603
SP_DIF_E
R216 0_0805
YPRPB_DET# <18>
R215 0_NC
C342 300P_NC
Populate R218 & De-populate R216
when component VIDEO is enable.

QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 19 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

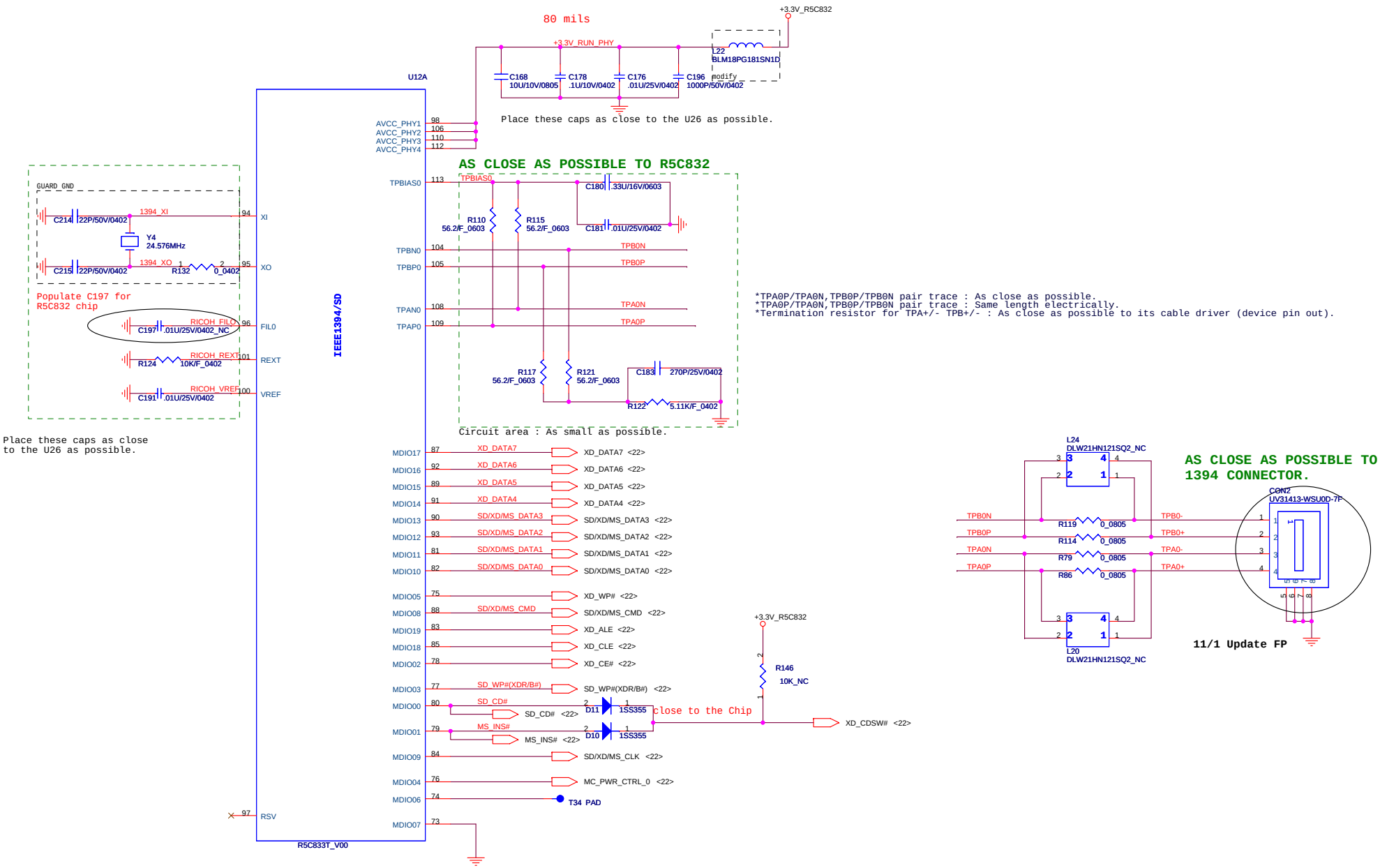


QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 20 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

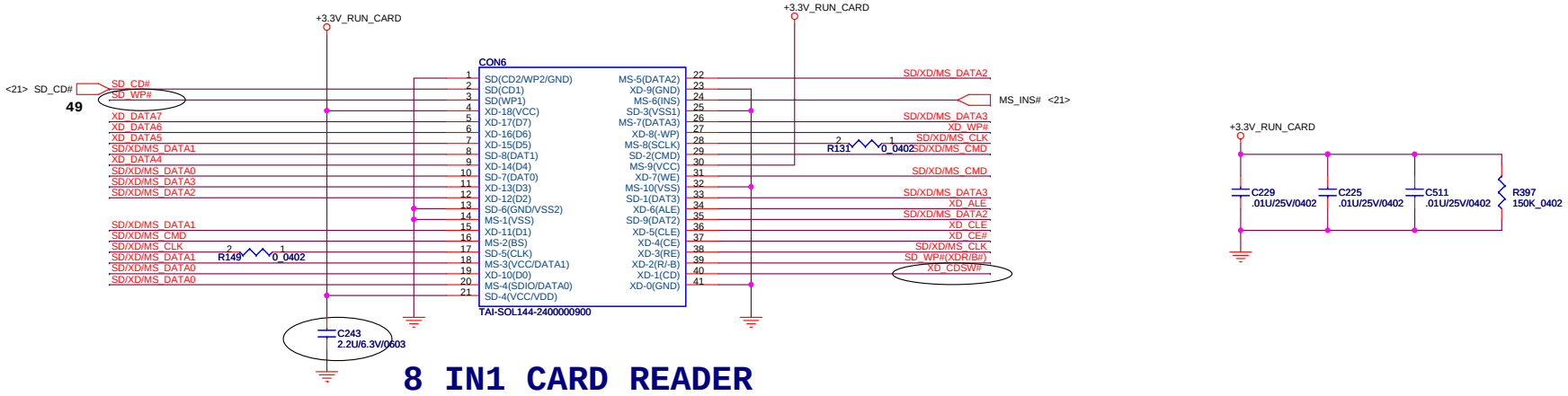


QUANTA COMPUTER

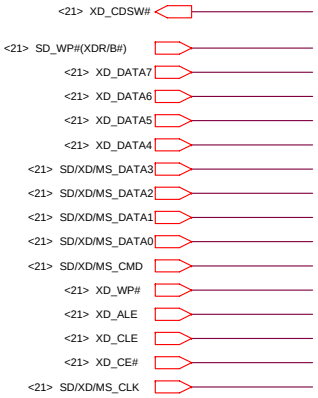
Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 21 of 51	

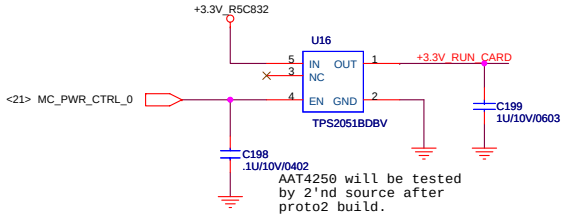
WWW.AliSaler.Com

WWW.AliSaler.Com

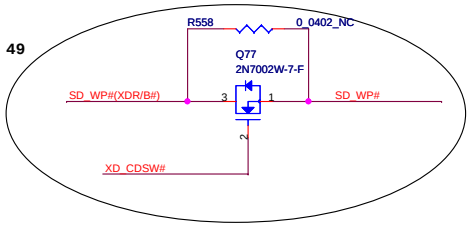


8 IN1 CARD READER





SD Protect



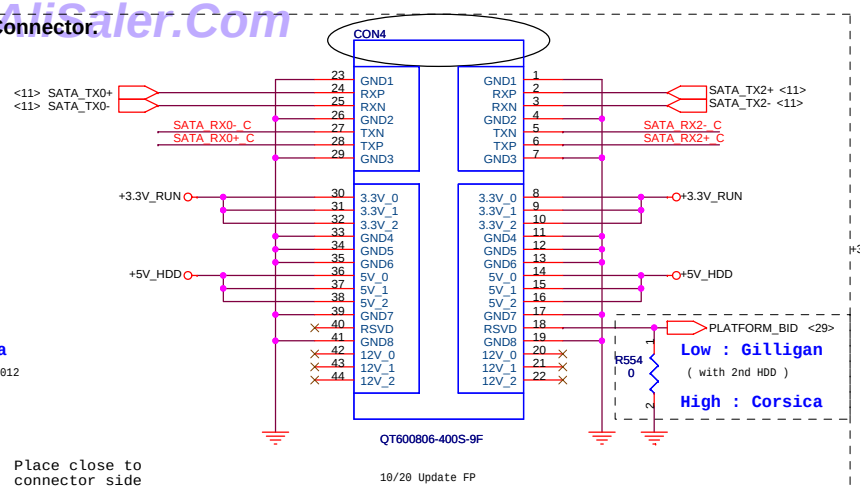
QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 22 of 51	

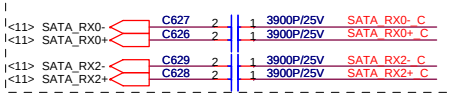
WWW.AliSaler.Com

WWW.AliSaler.Com

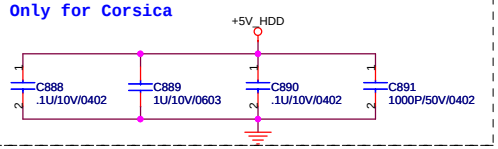
SATA 1 & 2 Connector.



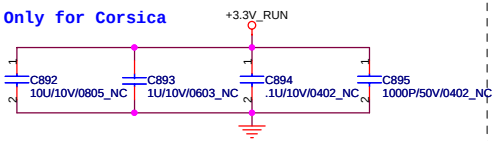
Locate caps C626, C627, C628, C629 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 0 mils.



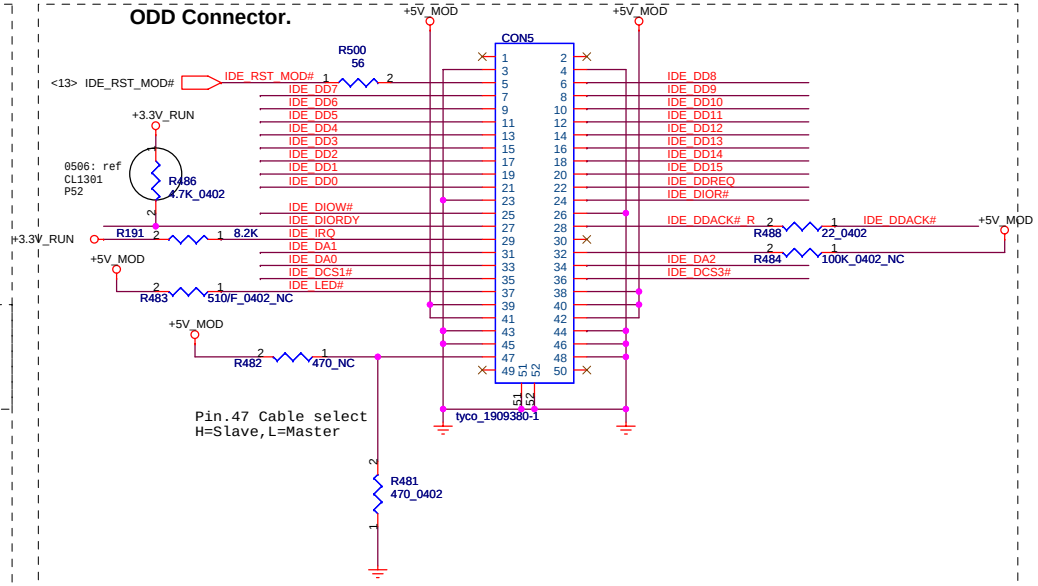
Only for Corsica

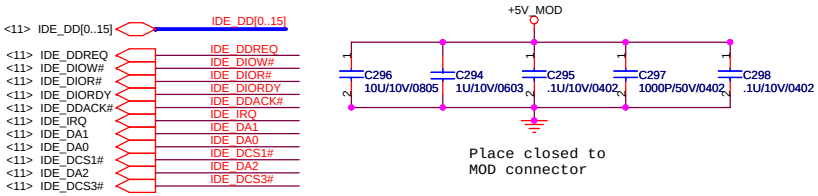


Only for Corsica

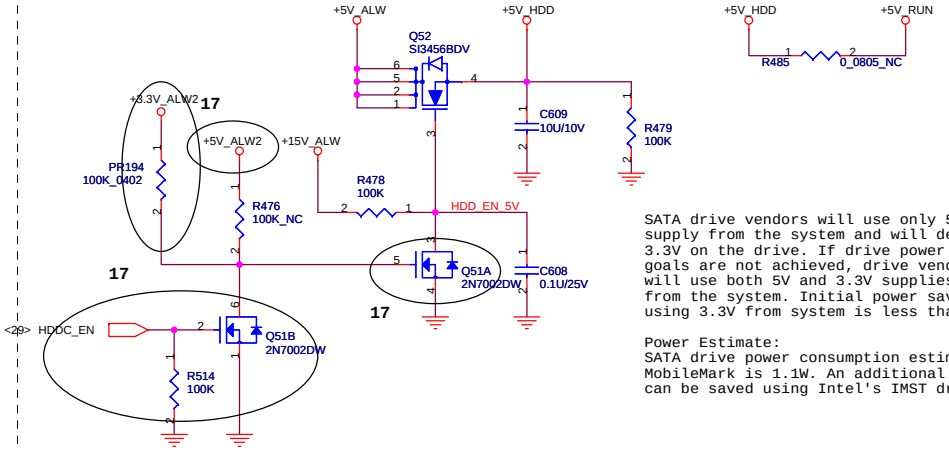


ODD Connector.





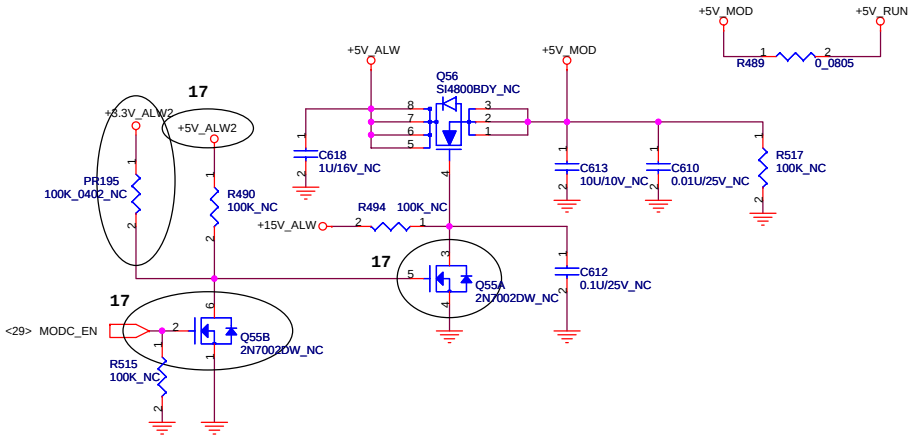
SATA PWR



SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

Power Estimate:
SATA drive power consumption estimate at MobileMark is 1.1W. An additional 150mW can be saved using Intel's IMST driver.

ODD PWR



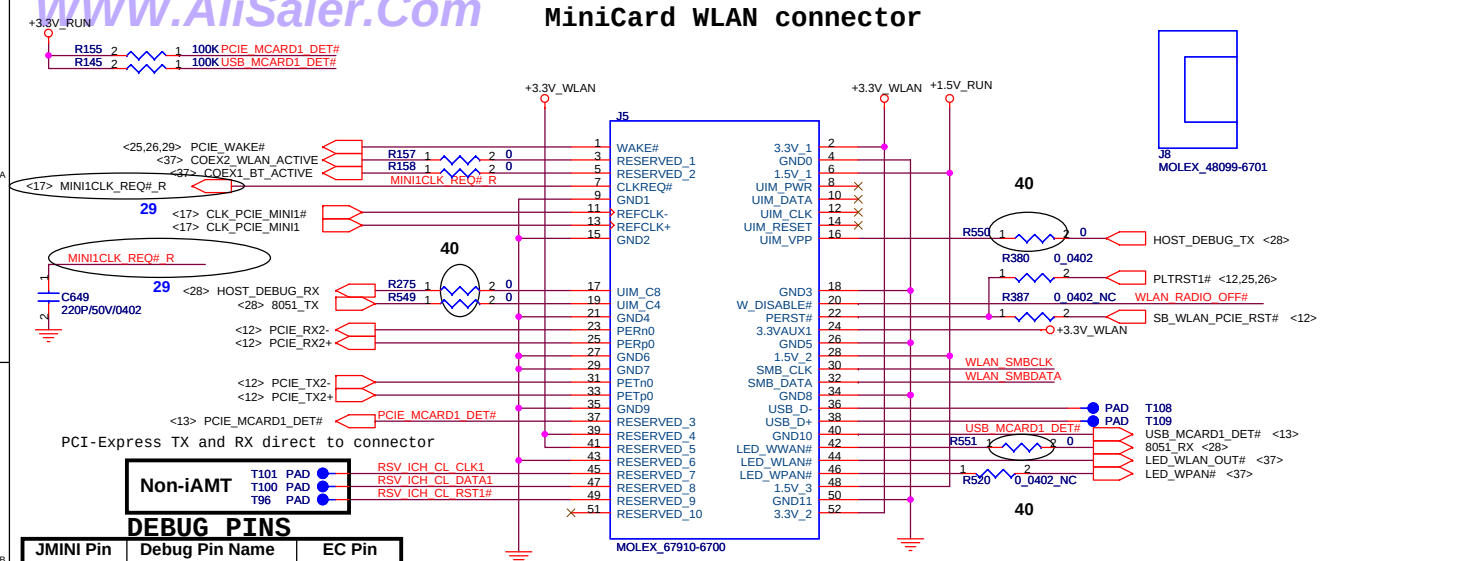
QUANTA COMPUTER

Title	SATA (HDD&CD_ROM)	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 23 of 51	

WWW.AliSaler.Com

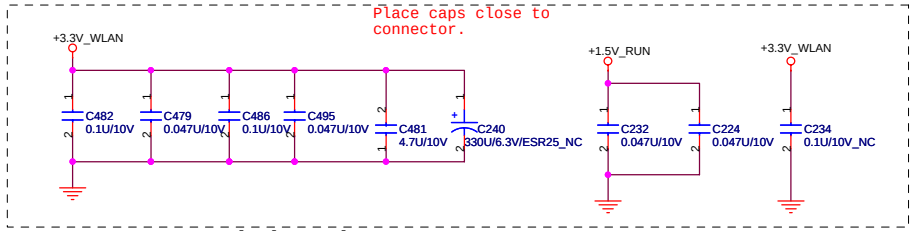
WWW.AliSaler.Com

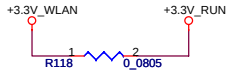
MiniCard WLAN connector

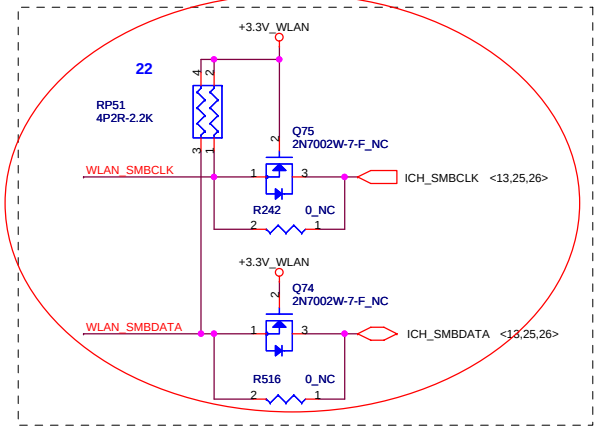


DEBUG PINS

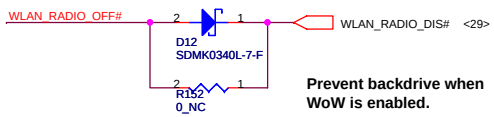
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



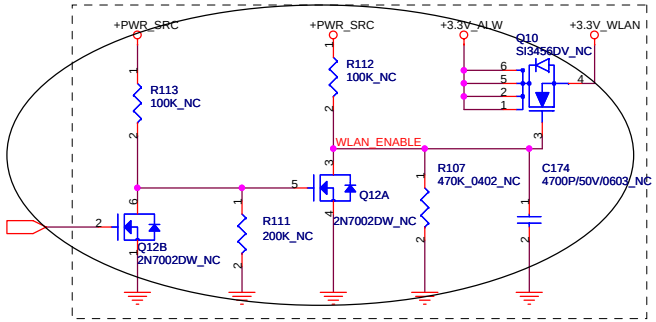




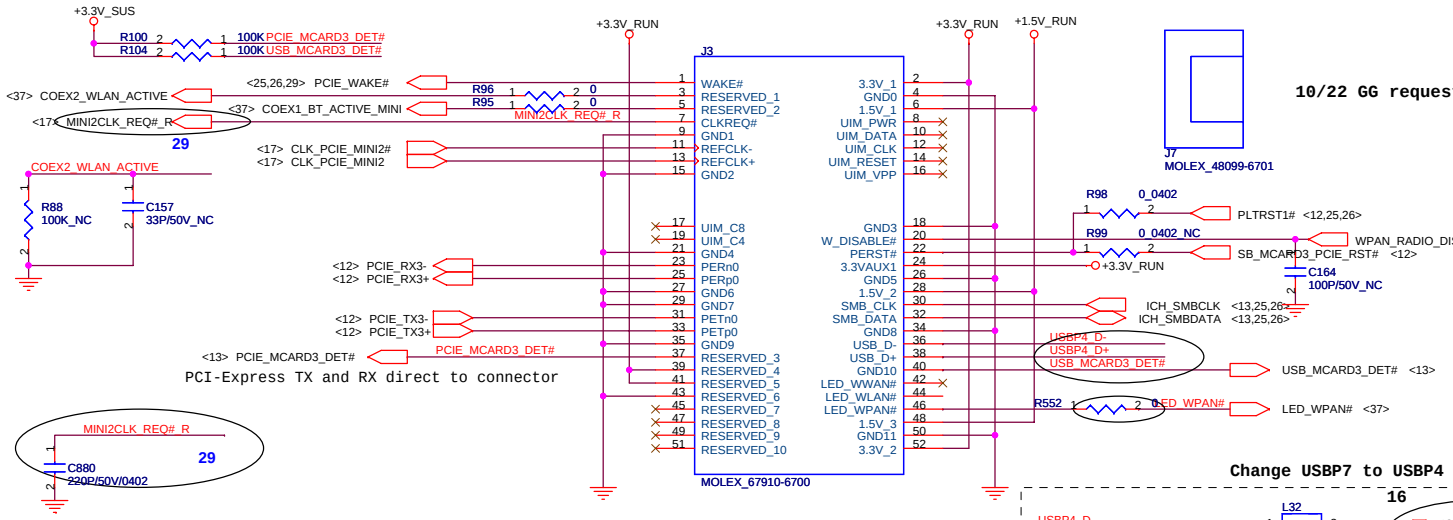
Suport for WoW



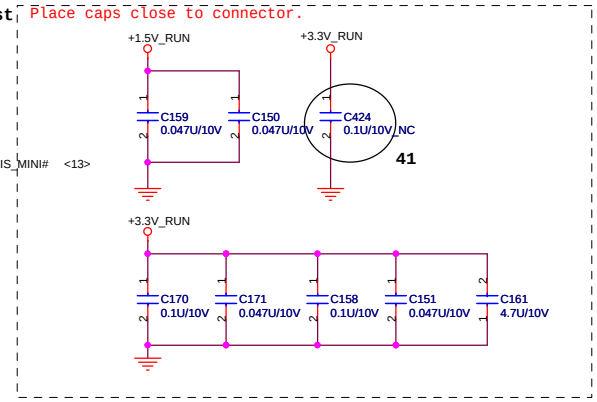
Prevent backdrive when WoW is enabled.



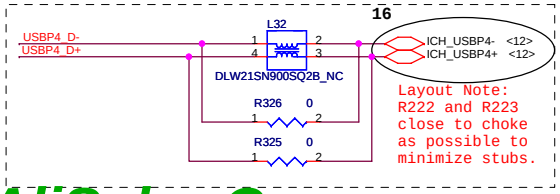
MiniCard WPAN connector



10/22 GG request



Change USBP7 to USBP4

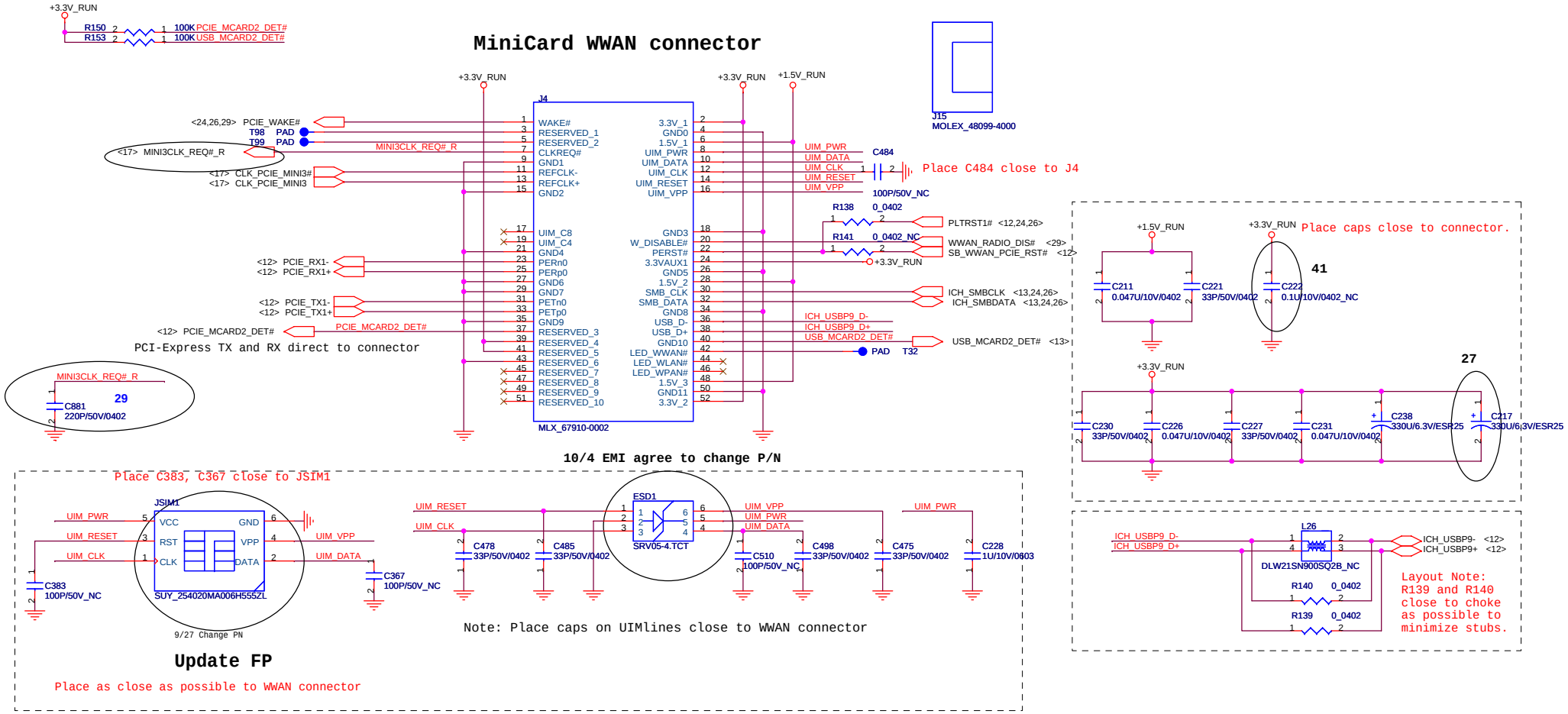


QUANTA COMPUTER

Title	MINI-PCI	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 24 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



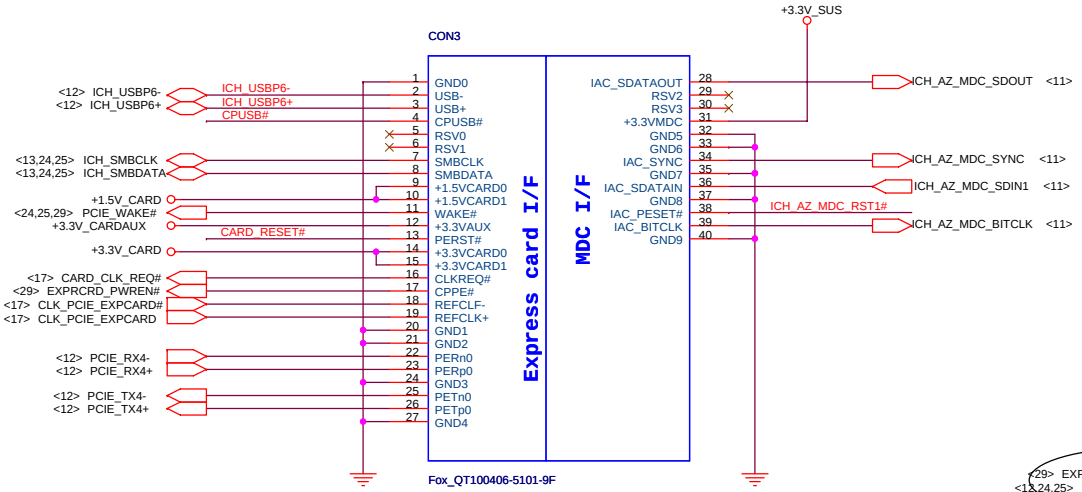
QUANTA COMPUTER

Title	WWAN	
Size	Document Number VC-08B	Rev 0.1
Date: Monday, March 05, 2007	Sheet 25 of 51	

WWW.AliSaler.Com

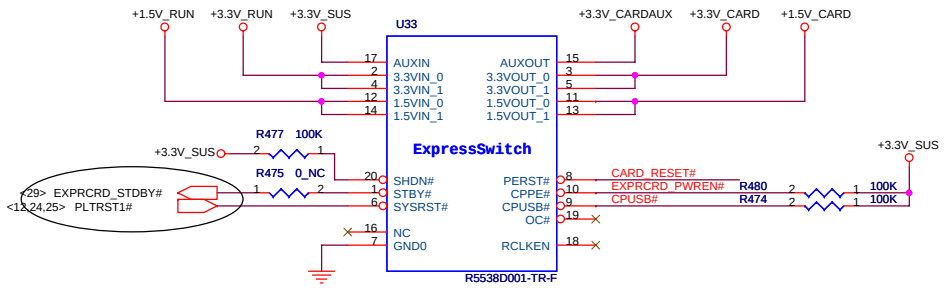
WWW.AliSaler.Com

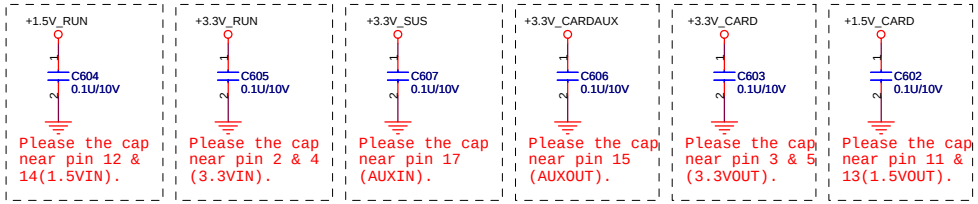
EXPRESS+MDC

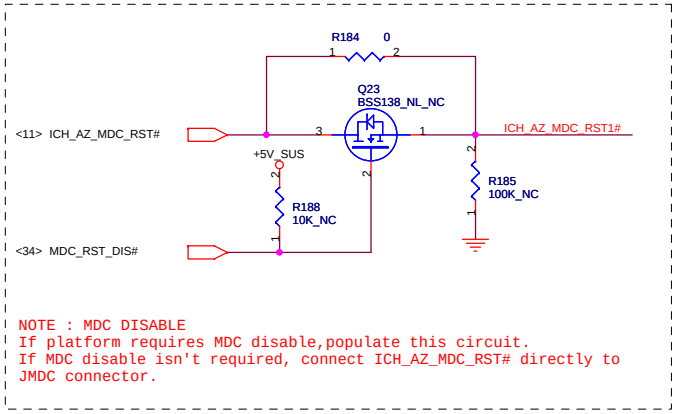


Update PN

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.







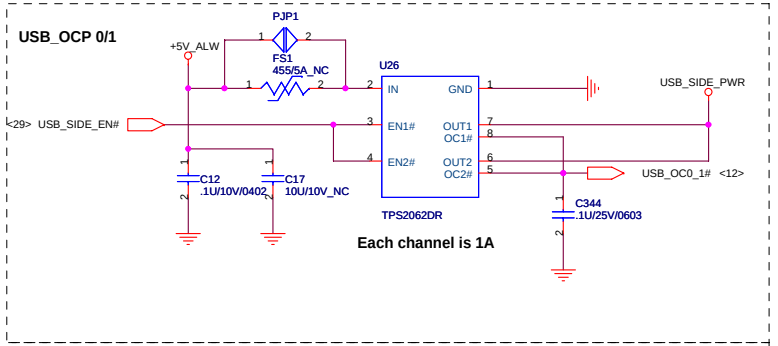
NOTE : MDC DISABLE
If platform requires MDC disable,populate this circuit.
If MDC disable isn't required, connect ICH_AZ_MDC_RST# directly to JMDC connector.

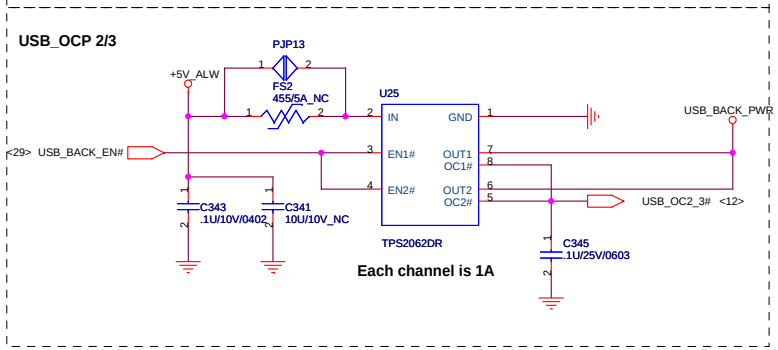
QUANTA COMPUTER

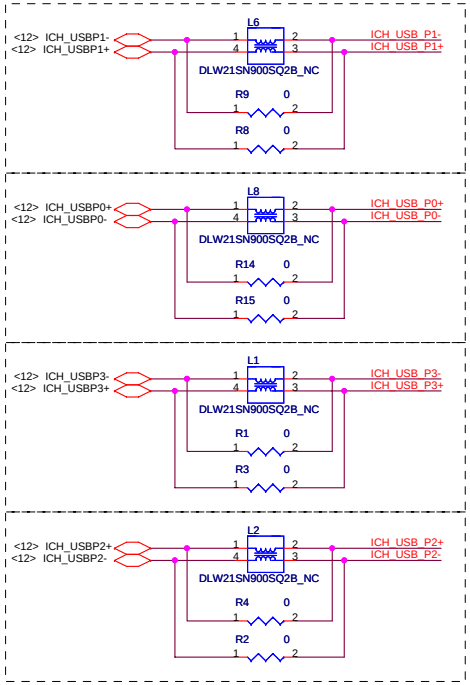
Title	ExpressCard/SmartCard	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 26 of 51	

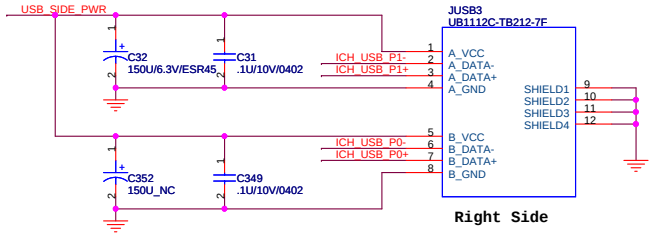
WWW.AliSaler.Com

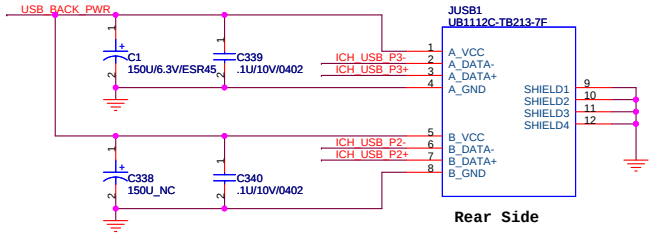
WWW.AliSaler.Com

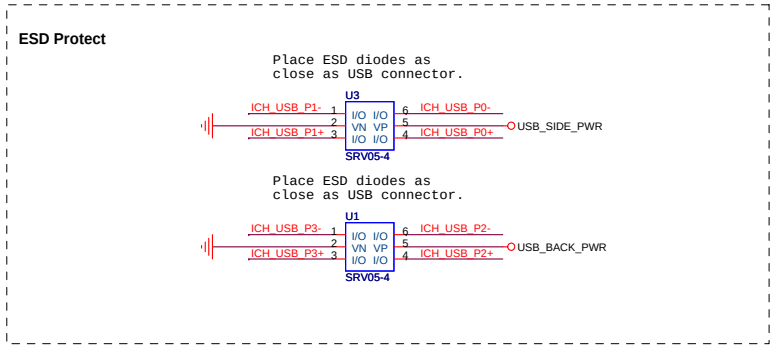


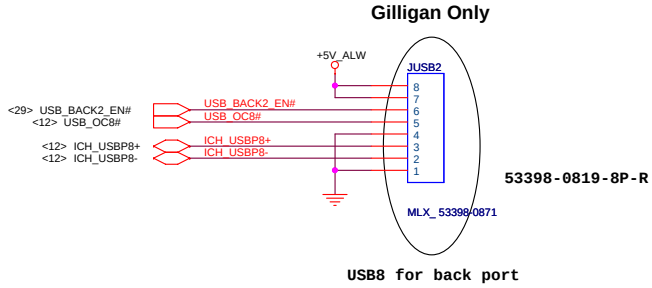












QUANTA COMPUTER

Title	USB & Flash		
Size	Document Number FM1		Rev 0.1
Date: Monday, March 05, 2007		Sheet 27 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

MEC5025 EC-08 128 PIN VTQFP

Net & Part	AMT Intel	Non-AMT Broadcom
3.3V_M_PWRGD	Pin15 of 5025	NC
ICH_RSMRST#	Pin23 of 5025	NC
M_ON	Pin24 of 5025	NC
SIO_SLP_M#	Pin25 of 5025	NC
1.05V_1.25V_M_PWRGD	Pin37 of 5025	NC
R238	Pin24 of 5025	NC
LOM_SUPER_IDDQ	NC	Refer to UMA ref pg 32.
LOM_LOW_PWR#	NC	Refer to UMA ref pg 32.
LOM_CABLE_DETECT	NC	Refer to UMA ref pg 32.

32KHz Clock.

External Work Around Circuit.

For MEC5025 Rev.C: C685=22uF and populate workaround circuit.
For MEC5025 Rev.D: C685=4.7uF and depopulate workaround circuit.

Debug Serial Port
Flash Recovery Port.

Not Stuff 0 ohm when doing Flash recovery.

Place these caps close to MEC5025.

Place close to pin 58.

Place cap close to pin 121.

Populate for flash corruption issue.

1 = Enabled.
0 = Disabled

Flash Recovery.

Low = Write Protected.

Flash Write Protect bottom 4K of internal bootblock flash.

MEC5025
LQFP128-16X16-4-JM6
Rev 0.01 (11/09/05)

DELL CONFIDENTIAL/PROPRIETARY

Title: Ultra I/O Controller MEC5025

Size: | Document Number: M-08 | Rev: 0.1

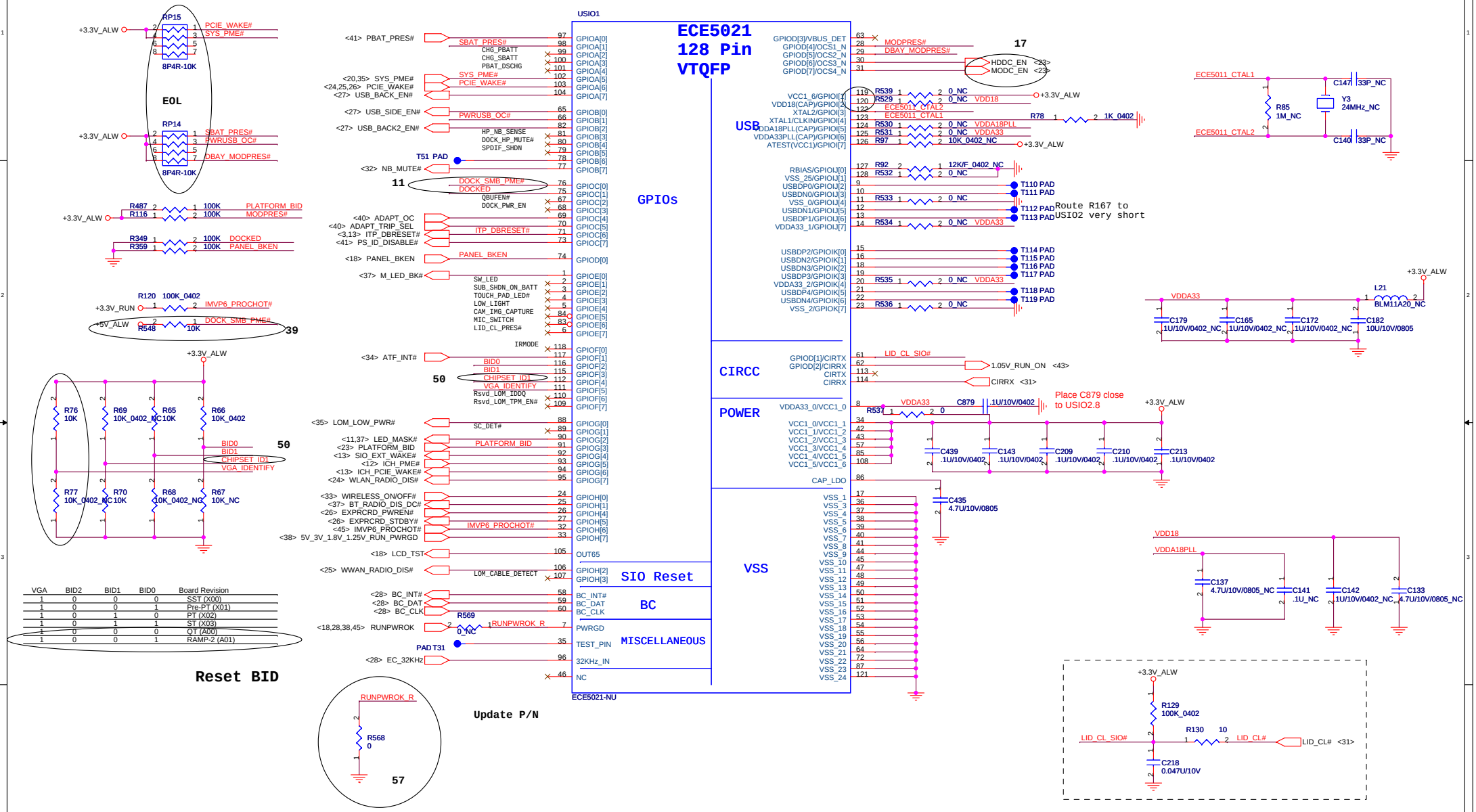
Date: Monday, March 05, 2007 | Sheet 28 of 51

WWW.AliSaler.Com

WWW.AliSaler.Com

Update to 5021

Depopulate R529, R530, R531, R532, R533, R534, R535, R536, R92, R97, C142, C133, C137, C141, C179, C165, C172, L21
Populate R537, C879.



VGA	BID2	BID1	BID0	Board Revision
1	0	0	0	SST (X00)
1	0	0	1	Pre-PT (X01)
1	0	1	0	PT (X02)
1	0	1	1	ST (X03)
1	0	0	0	QT (A00)
1	0	0	1	RAMP-2 (A01)

Reset BID

QUANTA COMPUTER

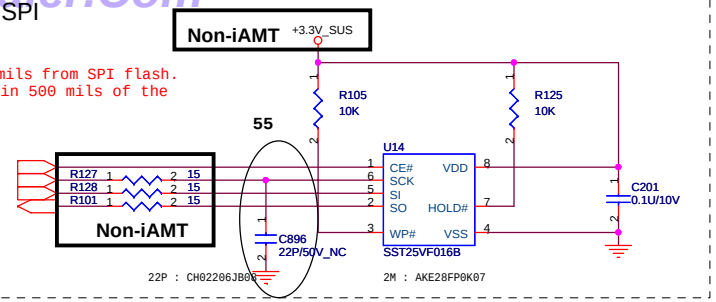
Title	SIO (GPIO/BC/USB/CIRR)		
Size	Document Number FM1		Rev 0.1
Date: Monday, March 05, 2007	Sheet 29 of 51		

WWW.AliSaler.Com

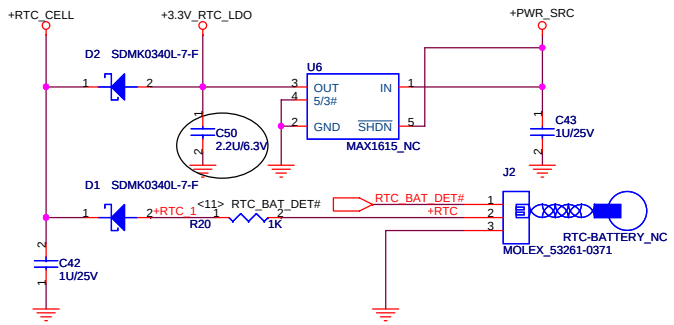
WWW.AliSaler.Com

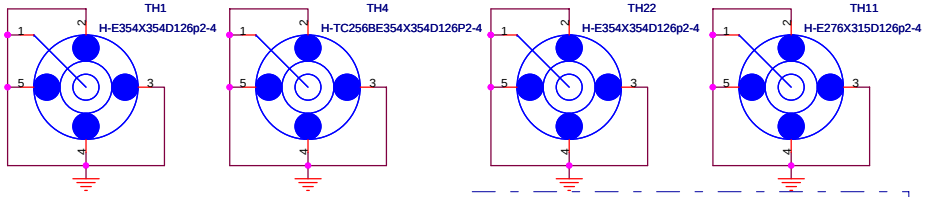
16Mbit (2M Byte), SPI

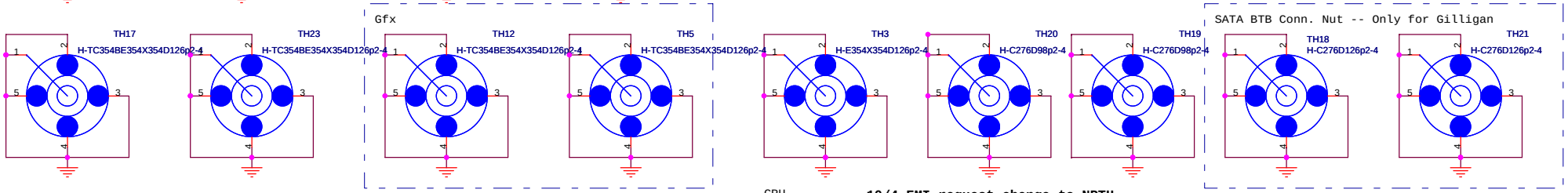
Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.



RTC BATTERY



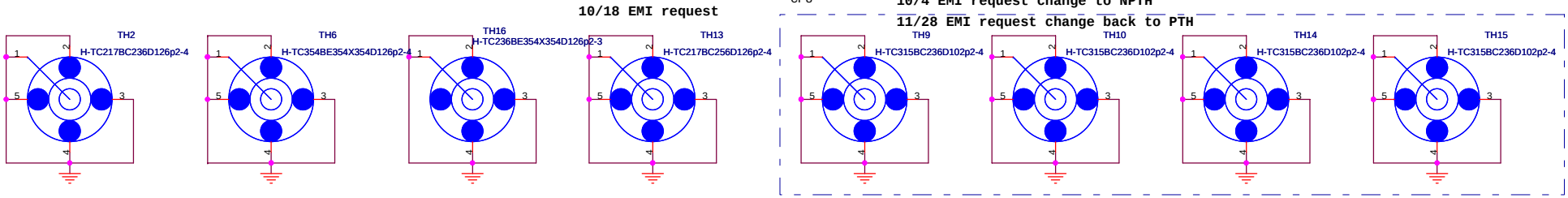


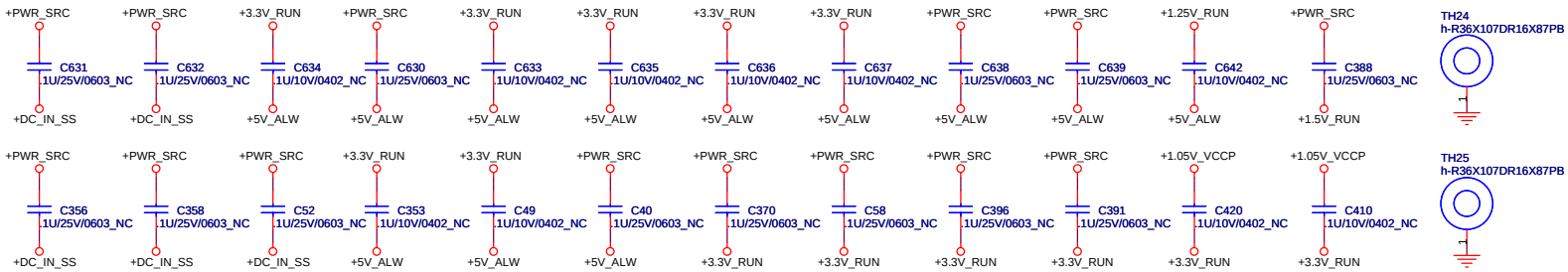


10/18 EMI request

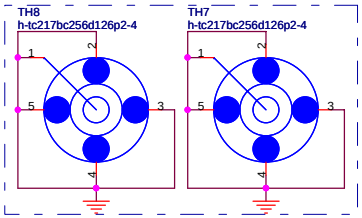
CPU

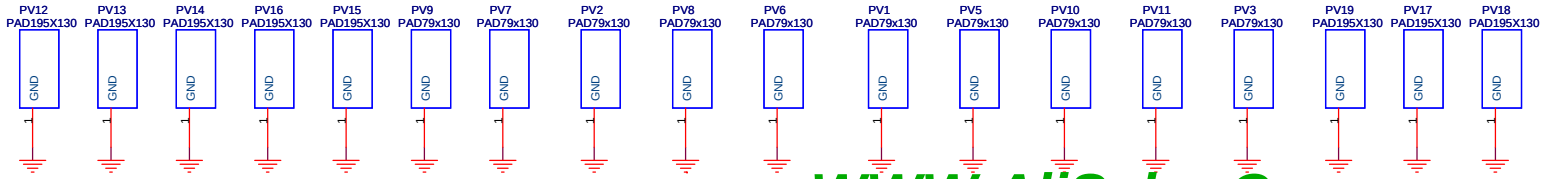
10/4 EMI request change to NPTH
11/28 EMI request change back to PTH





DSUB



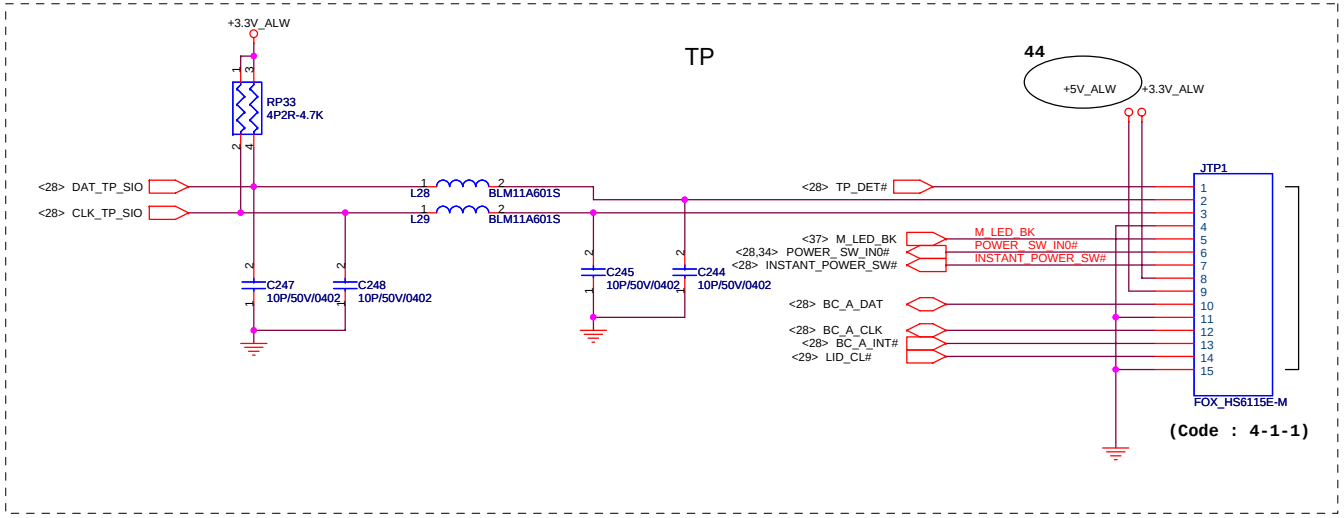


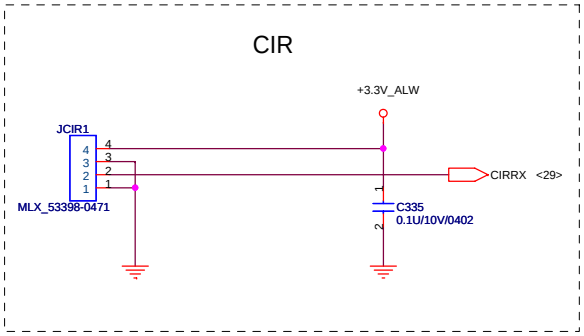
QUANTA COMPUTER

Title	FLASH, RTC & KC	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 30 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com





QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 31 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

INTERNAL SPEAKER AMP

Update PN

52

Package 1206 for THD+N performance for Vista Logo requirements.

AUD_LINE_OUT_L C306 .033U/25V/X7R/1206
AUD_LINE_OUT_R C307 .033U/25V/X7R/1206
AUD_HP_OUT_L C326 1uF/25V/X7R/1206
AUD_HP_OUT_R C329 1uF/25V/X7R/1206

10/18 Change 2.2u if necessary

31

C330 47P/50V_NC C327 47P/50V_NC C312 47P/50V_NC C311 47P/50V_NC

C334 1U/10V

<28> AUD_AMP_MUTE# 32

U23 TPA6040A4 QFN 32PIN

SPKR_INL, SPKR_INR, HP_INL, HP_INR, BIAS, SPKR_EN#, HP_EN, MUTE#, GAIN1, GAIN2, HPVDD, CPVDD, C1P, C1N, CPGND, PVSS, CPVSS

LIN- SPKR_LIN+
RIN- SPKR_RIN+
HP_OUT_L
HP_OUT_R
AUD_SPK_ENABLE#
AMP_HP_EN
AUD_AMP_MUTE#
AUD_AMP_GAIN1
AUD_AMP_GAIN2
REG_EN

OUTL+ AUD_SPK_L1
OUTL- AUD_SPK_L2
OUTR+ AUD_SPK_R1
OUTR- AUD_SPK_R2
HPL AUD_HP_JACK_L <33>
HPR AUD_HP_JACK_R <33>
REGEN REGEN
SET SET
SPKR_LIN-
SPKR_RIN-
VOUT +VDDA
VDD VDD
PVDD_8 +5V_SPK_AMP
PVDD_18 +5V_SPK_AMP
GND_28, PGND_5, PGND_21

+5V_SPK_AMP

C328 1U/10V C616 1U/16V C318 10U/10V

10/18 Depop if not necessary

C324 1U/16V

TPA6040A4

R560 0_0603 R561 0_0603 R562 0_0603 R563 0_0603

<11> SPEAKER_DET# SPEAKER_DET#

AUD_SPK_L1 AUD_SPK_L2 AUD_SPK_R1 AUD_SPK_R2

JSPK1 MLX_53398-0671

C620 100P/50V_NC C621 100P/50V_NC C622 100P/50V_NC C623 100P/50V_NC

For MAX9789A,depop R505,pop R506.

+5V_SPK_AMP R506 100K_NC R505 0 AUDIO_AVDD_ON AUD_AMP_MUTE#

+5V_SPK_AMP C625 0.1U/10V U34 NC7SZ08P5X_NL

+5V_SPK_AMP U36 NC7SZ08P5X_NL_NC

NB_MUTE# AUD_HP_NB_SENSE AUD_HP_NB_SENSE_R CODEC_GPIO_PIN_4 AMP_HP_EN R545 0

L35 FB_600ohm+-25%_100MHz _200mA_0.6ohm DC

+5V_SPK_AMP VDD C316 1U/10V C615 1U/10V C319 0.1U/10V

Layout Note: Place close U22.

+VDDA C617 1U/10V C323 1U/10V

Layout Note: Place close U22.

+5V_SPK_AMP R208 100K R209 100K

AUD_SPK_ENABLE# AUD_EAPD# Q25 2N7002W-7-F

<29> NB_MUTE# Q24 2N7002W-7-F

+5V_SPK_AMP R496 100K_NC R499 100K R197 100K R199 100K_NC

AUD_AMP_GAIN1 AUD_AMP_GAIN2

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

AUDIO_AVDD_ON AUDIO_AVDD_ON <34>

R504 0_NC REGEN C619 0.033U/16V

C1425/C331 value need to match with C326/C290. This value be chosen in PT phase.

For MAX9789A,depop C619,pop R504.

+5V_SPK_AMP +5V_RUN +5V_SPK_AMP

L30 BLM21PG600SN1D

C310 1U/10V C315 10U/10V

Layout Note: Place close to pin 8.

C332 1U/10V C331 10U/10V C333 0.1U/10V

Layout Note: Place close to pin 18.

FB_60ohm+-25%_100MHz _3A_0.05ohm DC

For MAX9789A,depop C614,pop R497.

SET R498 2.2K_NC +VDDA C614 0.033U/16V R497 0_NC

R501 0_0805 R207 0_0603 R189 0_0603 R198 0_0603 R202 0_0603

EMI Request

AZALIA (HD) CODEC

ICH_AZ_CODEC_BITCLK R193 47_NC Close to pin 6. C305 0.1U/10V_NC

<11> ICH_AZ_CODEC_BITCLK
<11> ICH_AZ_CODEC_SDIN0
<11> ICH_AZ_CODEC_SDOUT
<11> ICH_AZ_CODEC_SYNC
<11> ICH_AZ_CODEC_RST#

ICH_AZ_CODEC_BITCLK R192 33 SDIN ICH_AZ_CODEC_SDOUT

49

U22 10/18 Check package STAC9205 LQFP 48PIN

HDA_BITCLK, HDA_SDI_CODEC, HDA_SDO, HDA_SYNC, HDA_RST#, DMIC_CLK, DMIC0/VOL_UP/GPIO1, DMIC1/VOL_DN/GPIO2, SPDIF_IN/EAPD#/GPIO0, SPDIF_OUT, NC_43, NC_44, NC_45, DVDD_CORE_1, DVDD_CORE_9, DVDD_CORE_40, DVDD_IO, AVDD_25, AVDD_38, DVSS, AVSS_26, AVSS_42

SENSE_A AUD_SENSE_A
SENSE_B AUD_SENSE_B
PORT_A_L AUD_HP_OUT_L
PORT_A_R AUD_HP_OUT_R
VREFOUT_A
PORT_B_L AUD_EXT_MIC_L <33>
PORT_B_R AUD_EXT_MIC_R <33>
VREFOUT_B AUD_VREFOUT_B <33>
PORT_C_L AUD_MIC_IN_L
PORT_C_R AUD_MIC_IN_R
VREFOUT_C
PORT_D_L AUD_LINE_OUT_L
PORT_D_R AUD_LINE_OUT_R
PORT_E_L
PORT_E_R DOCK_HP_MUTE#
GPIO4/VREFOUT_E
PORT_F_L
PORT_F_R AUD_SPDIF_SHDN
GPIO3/VREFOUT_F
CD_L
CD_GND
CD_R
PC_BEEP AUD_PC_BEEP
MONO_OUT
VREFFILT AC97VREFI
CAP2 CAP2

<33> AUD_DMIC_CLK
<33> AUD_DMIC_IN0

AUD_DMIC_CLK R555 0 AUD_DMIC_IN0 R556 0 CODEC_GPIO_PIN_4

ICH_AZ_CODEC_SDOUT R195 47_NC Close to pin 5. C308 0.1U/10V_NC

For tuning.

<19> AUD_SPDIF_OUT R204 0 AUD_EAPD# SPDIF_OUT

+3.3V_RUN C317 10U/10V_NC C301 0.1U/10V C313 1U/10V R203 0 R253 100K

+3.3V_RUN C325 4.7U/10V_NC C321 0.1U/10V_NC C643 1000P/50V C309 0.1U/10V

AUD_DMIC_CLK C647 4.7P/50V_NC

49

AUD_DMIC_IN0 C648 4.7P/50V_NC

+VDDA Depop R203 & pop C321 & C325 for AD1984.

C302 0.1U/16V C303 1U/10V C322 10U/10V_NC

+VDDA R201 100K

+VDDA R196 10K R194 10K

+VDDA 10_NC R200

C314 10U/10V C304 10U/10V C320 0.1U/10V_NC

C304 must be 1U & Pop C320 & R200 for AD1984.

Layout Note: Close to U22 Pin 13.

R493 5.1K/F +VDDA AUD_SENSE_A

R491 39.2K/F R492 20K/F C611 1000P/50V

<33> AUD_HP_NB_SENSE AUD_HP_NB_SENSE Q53 2N7002W-7-F Q54 2N7002W-7-F AUD_MIC_SWITCH <33>

Close to U22

+VDDA C300 0.1U/16V

AUD_PC_BEEP C299 0.1U/10V BEEP2 R187 20K BEEP1 R190 10K

BEEP <28> SPKR <13>

U21 74LVC1G86GW

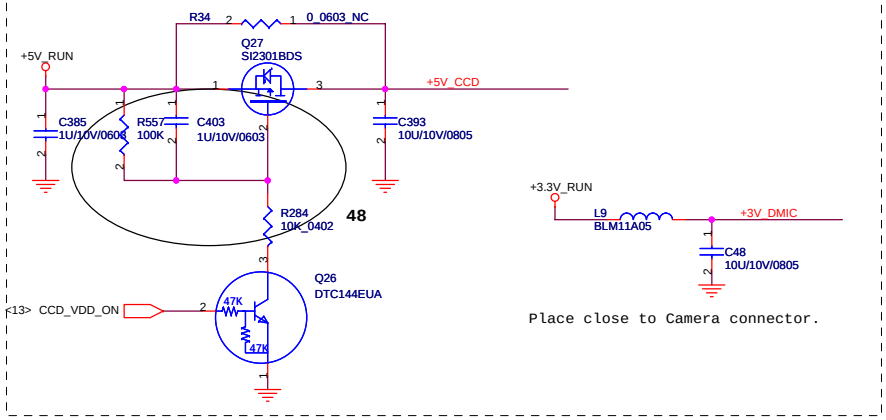
DELL CONFIDENTIAL/PROPRIETARY

Title	Azelia CODEC(STAC9205))	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 32 of 51	

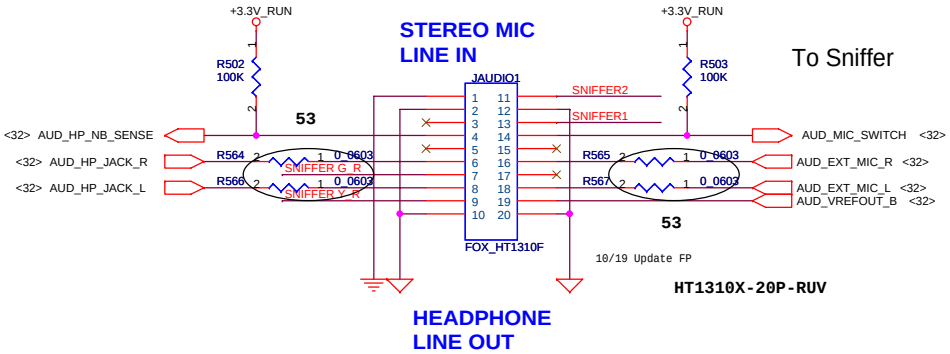
WWW.AliSaler.Com

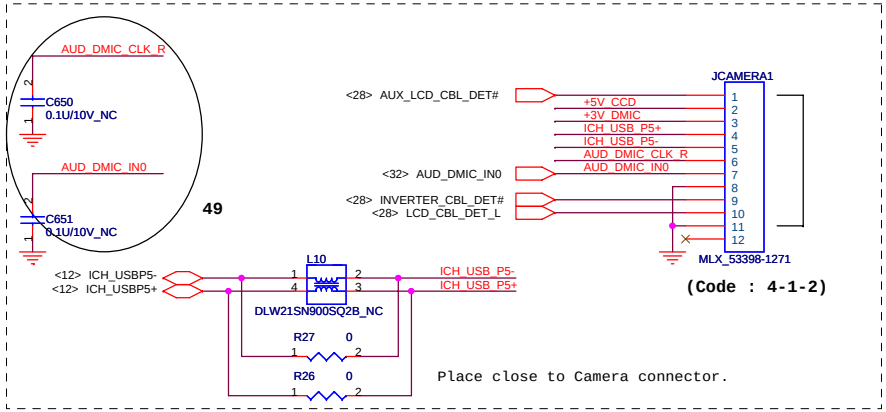
WWW.AliSaler.Com

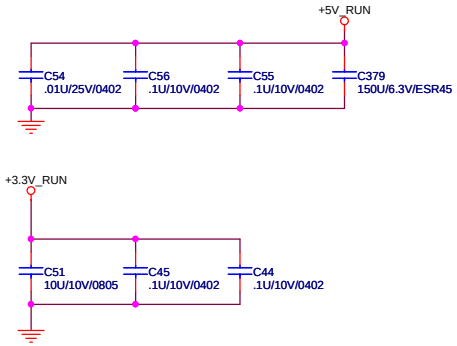
Digital Microphone & Camera

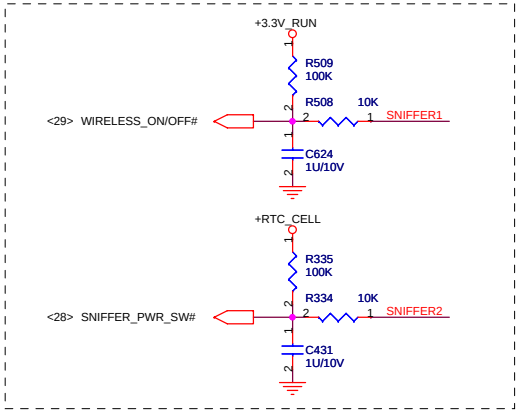


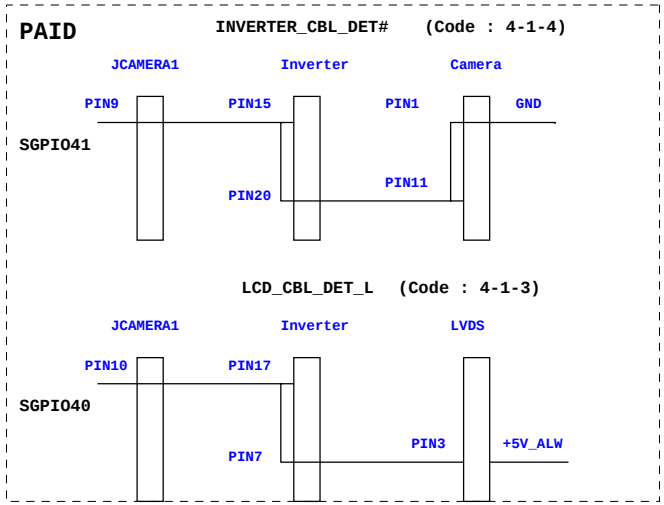
Update PN

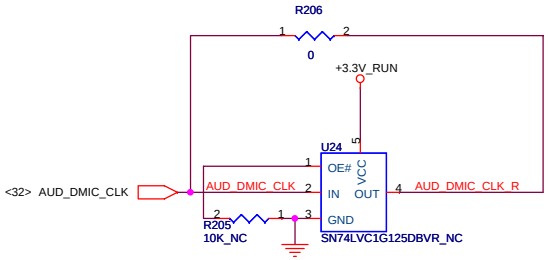


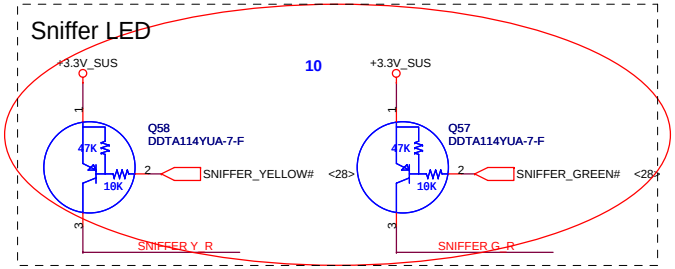










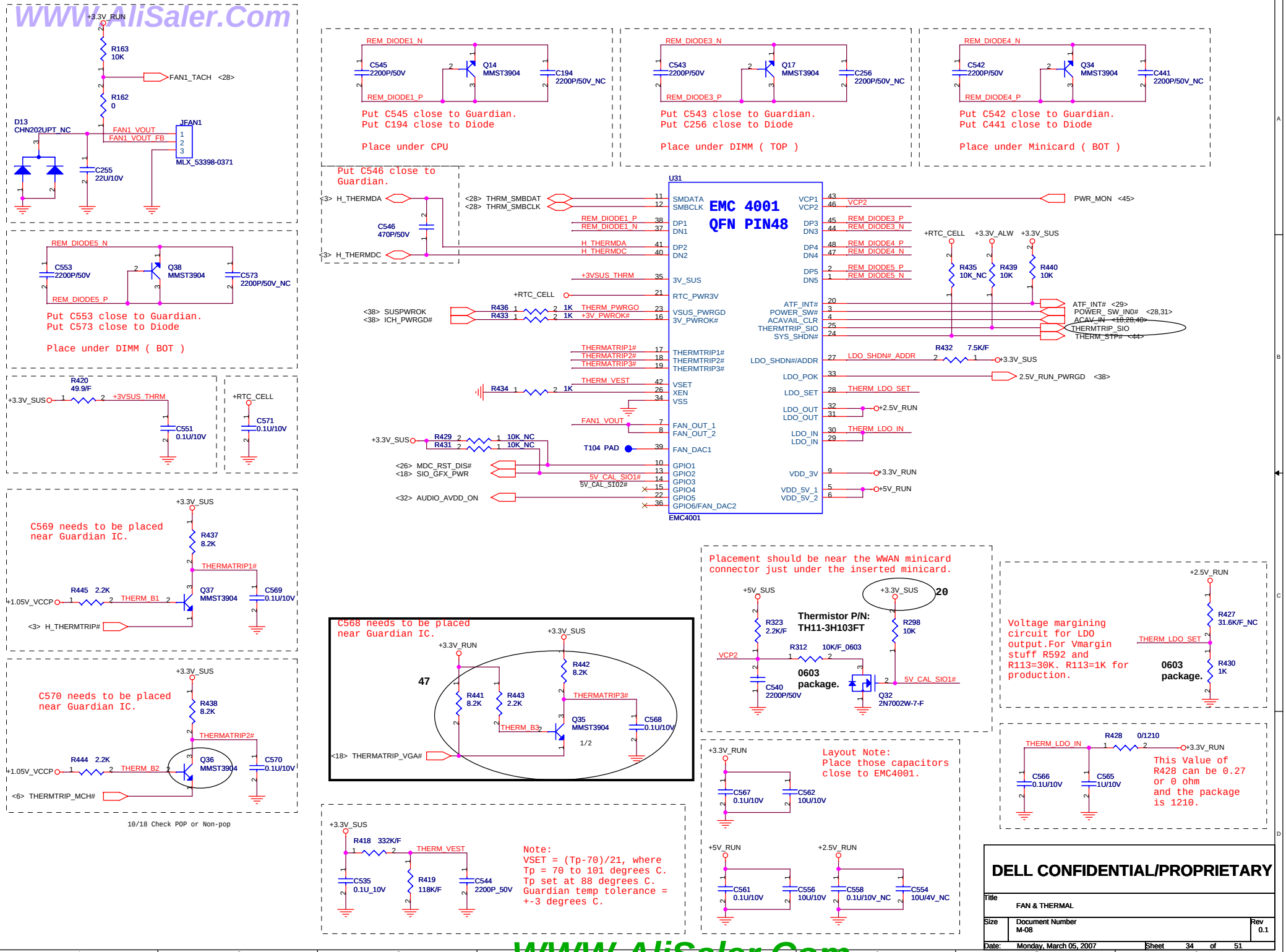


DELL CONFIDENTIAL/PROPRIETARY

Title	AUDIO CONN	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 33 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

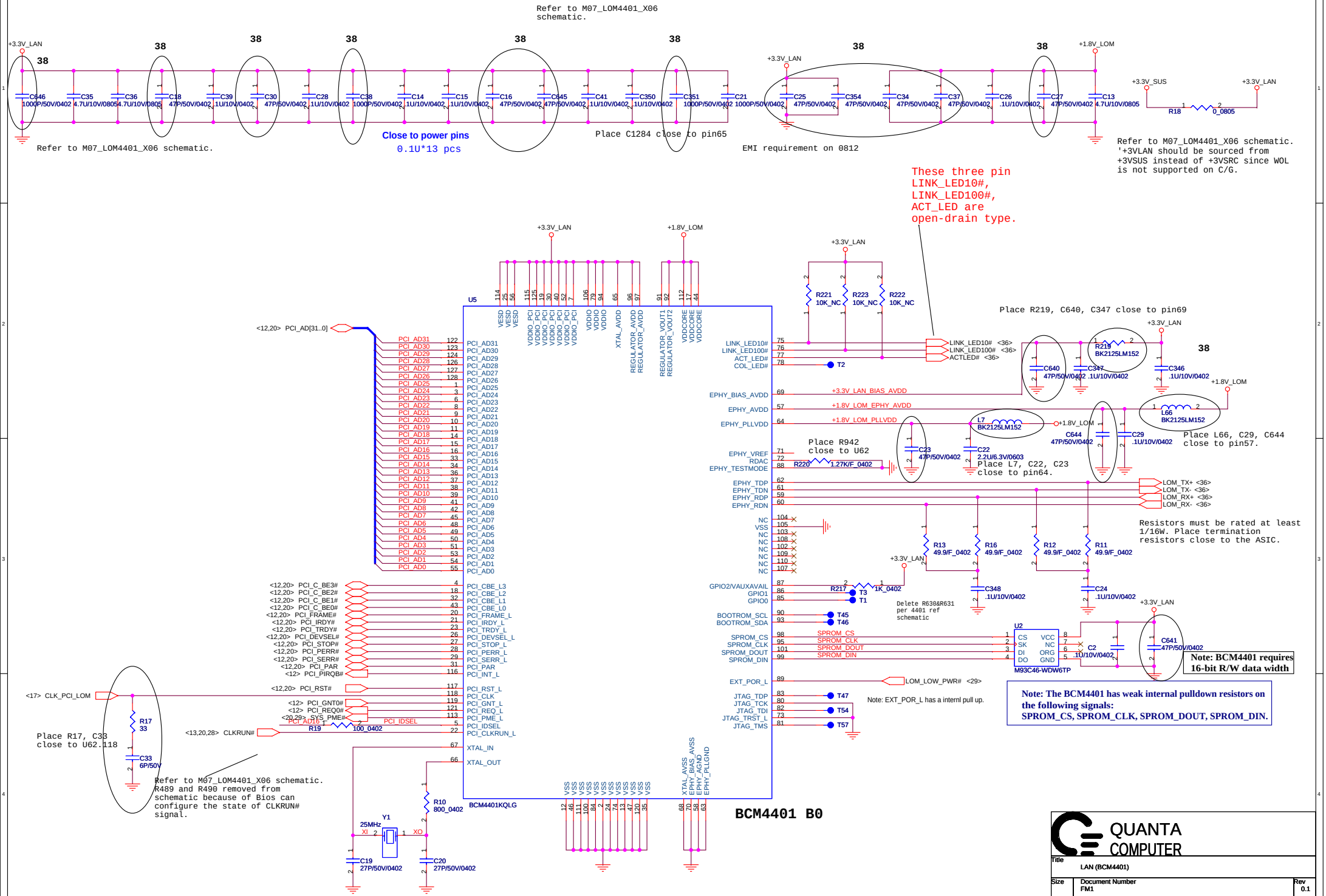


DELL CONFIDENTIAL/PROPRIETARY

Title	FAN & THERMAL	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 34 of 51	

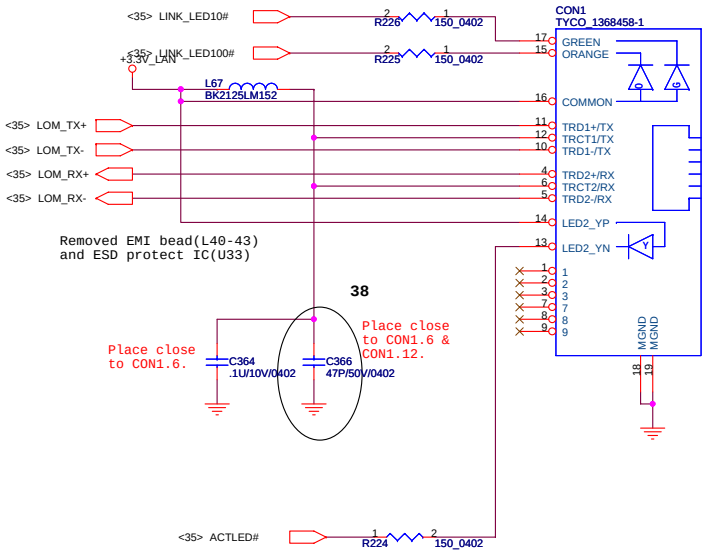
WWW.AliSaler.Com

WWW.AliSaler.Com



WWW.AliSaler.Com

WWW.AliSaler.Com

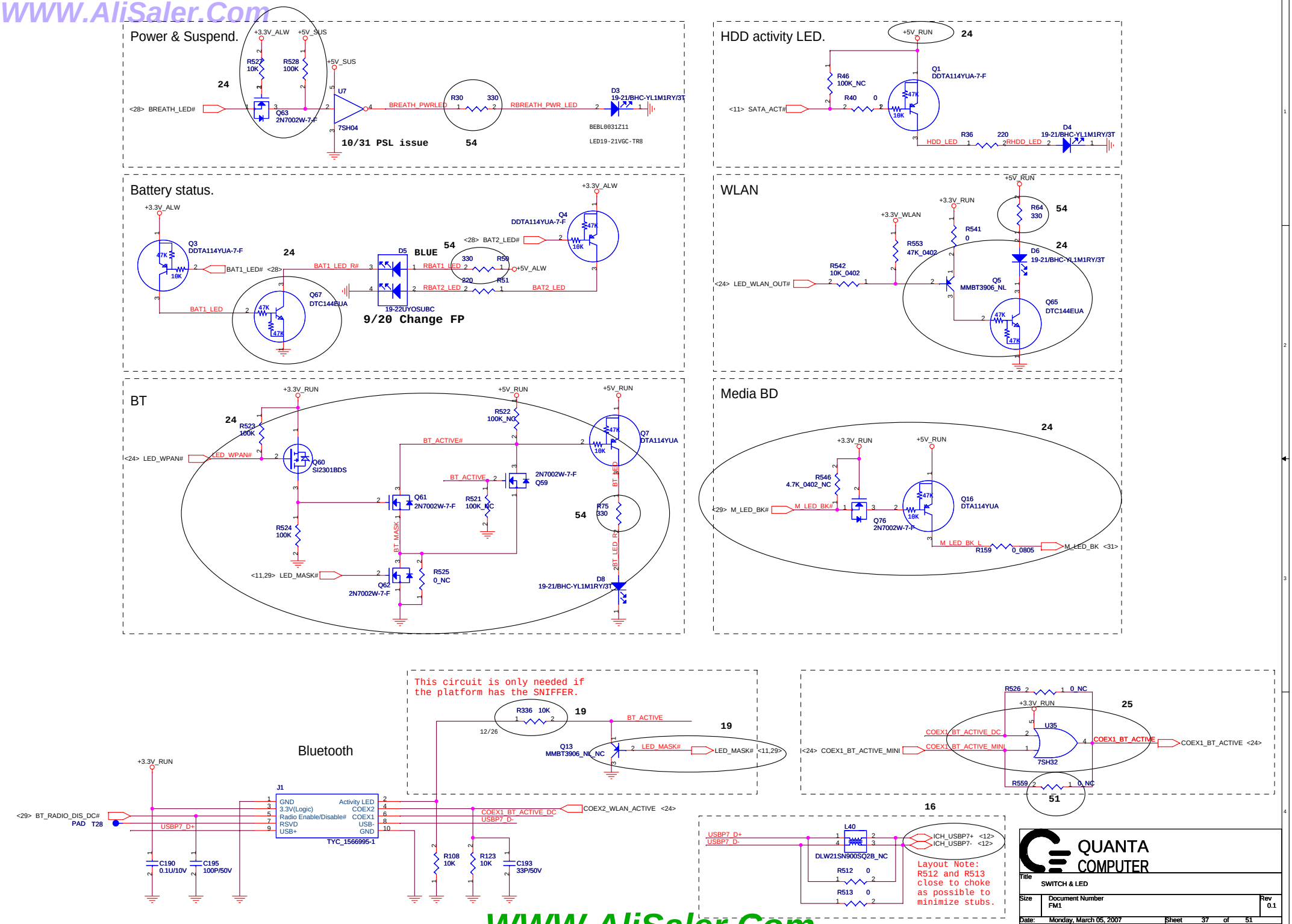


QUANTA COMPUTER

Title	LAN Jack	
Size	Document Number FM1	Rev 0.1
Date: Monday, March 05, 2007	Sheet 36 of 51	

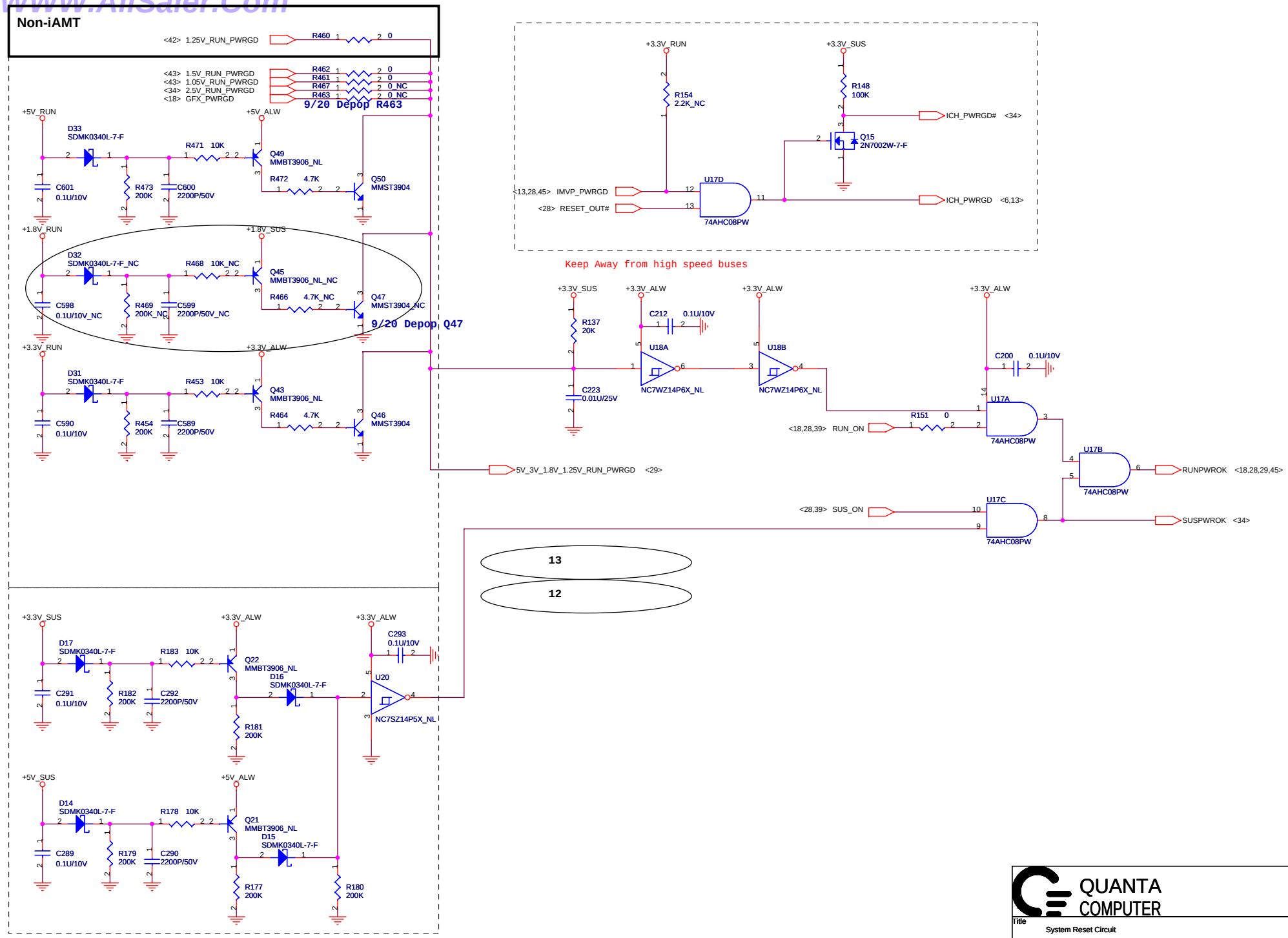
WWW.AliSaler.Com

WWW.AliSaler.Com



WWW.AliSaler.Com

WWW.AliSaler.Com

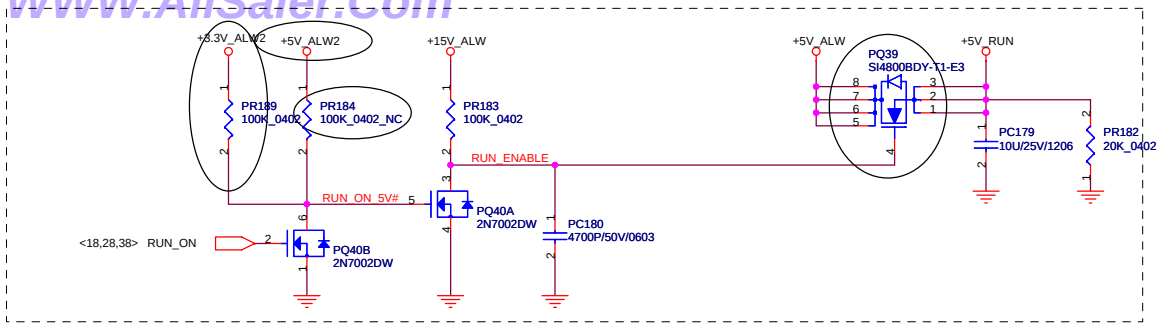


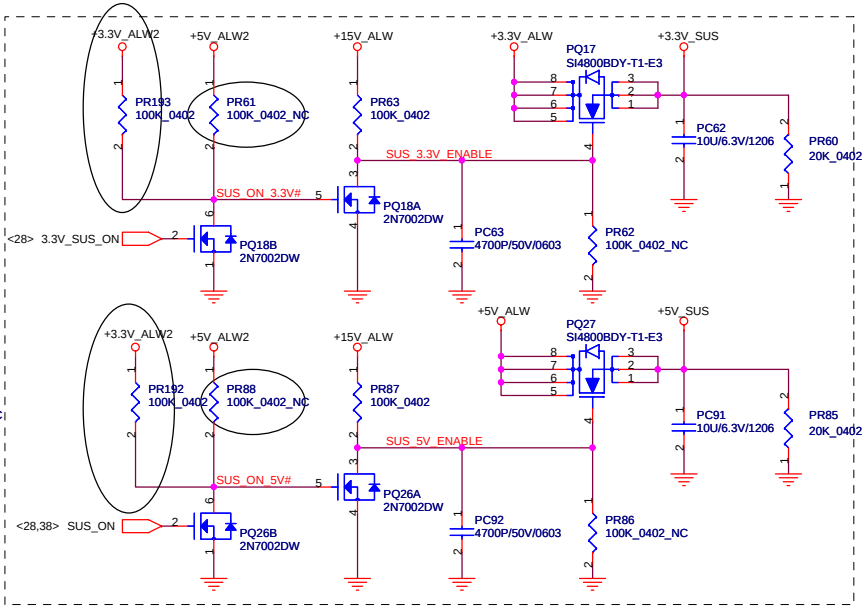
QUANTA COMPUTER

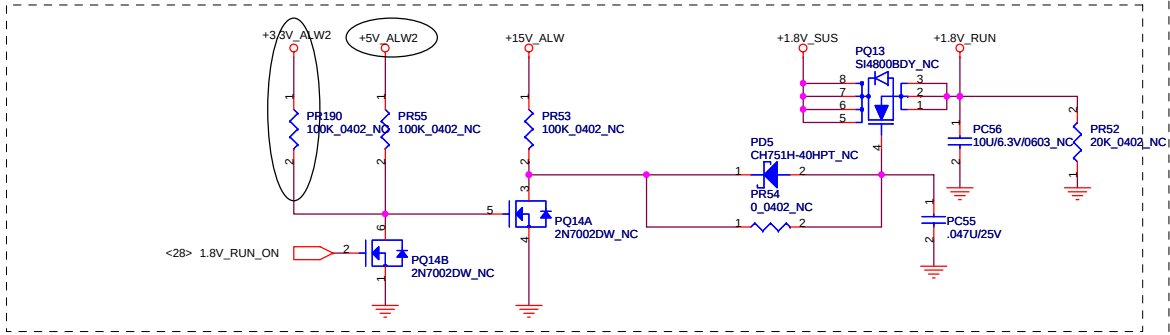
Title	System Reset Circuit	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 38 of 51	

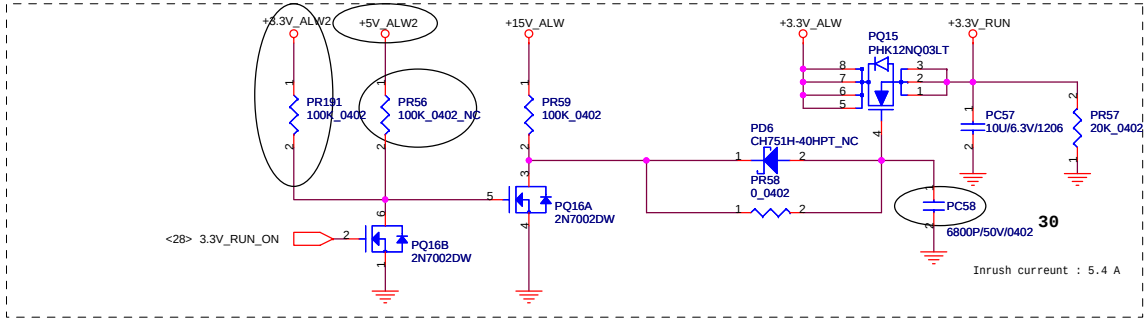
WWW.AliSaler.Com

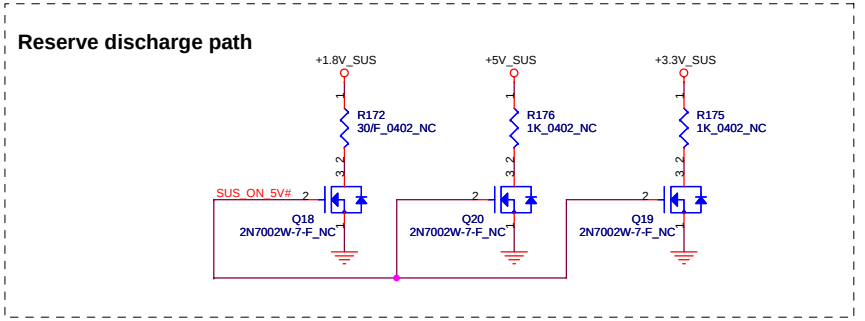
WWW.AliSaler.Com

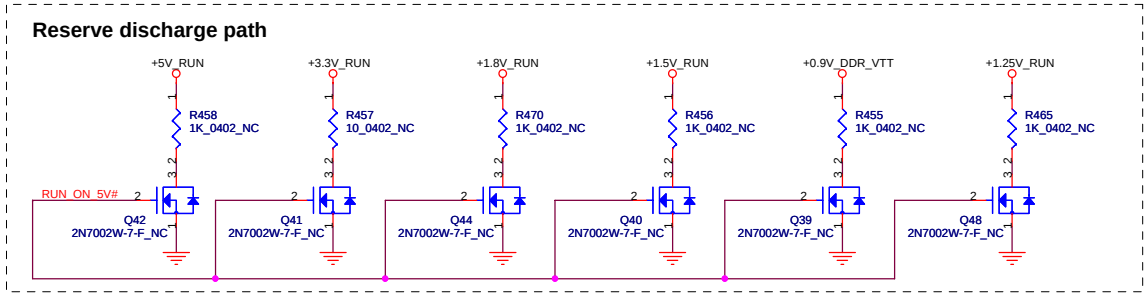












QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number M-08	Rev 0.1
Date: Monday, March 05, 2007	Sheet 39 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

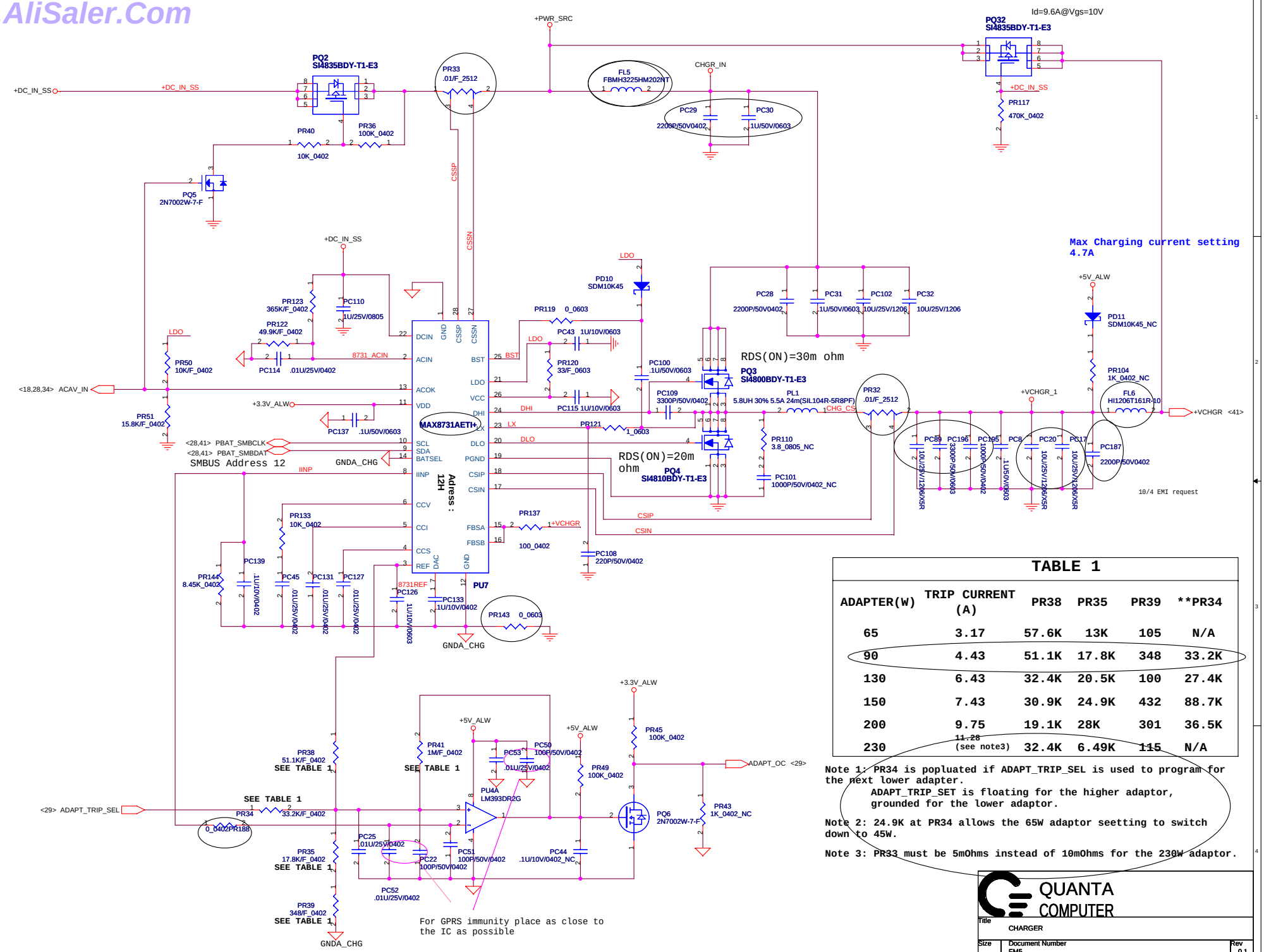


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR38	PR35	PR39	**PR34
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR34 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR34 allows the 65W adaptor seetting to switch down to 45W.

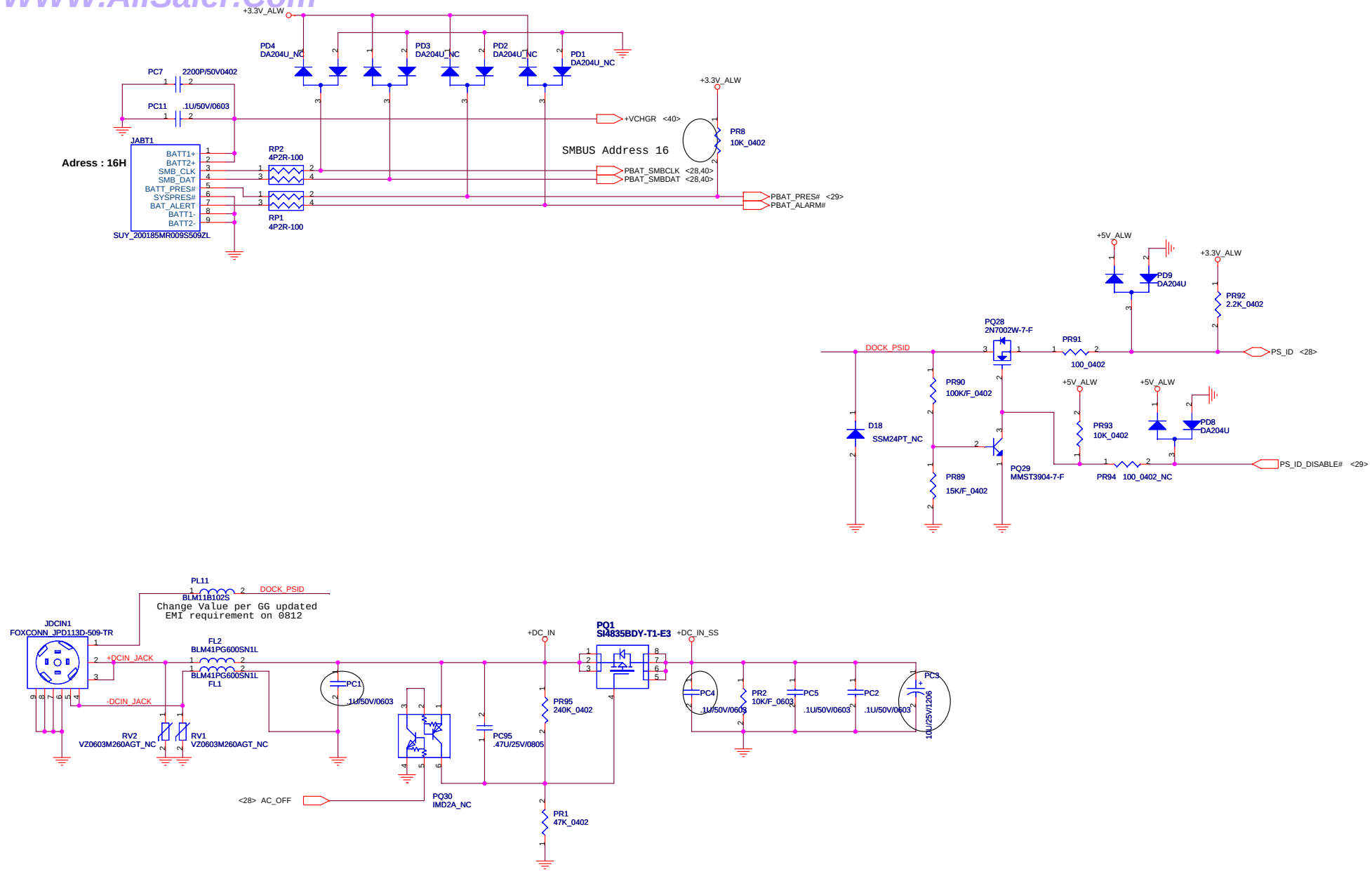
Note 3: PR33 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

Title	CHARGER	
Size	Document Number FM5	Rev 0.1
Date: Monday, March 05, 2007	Sheet 40 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

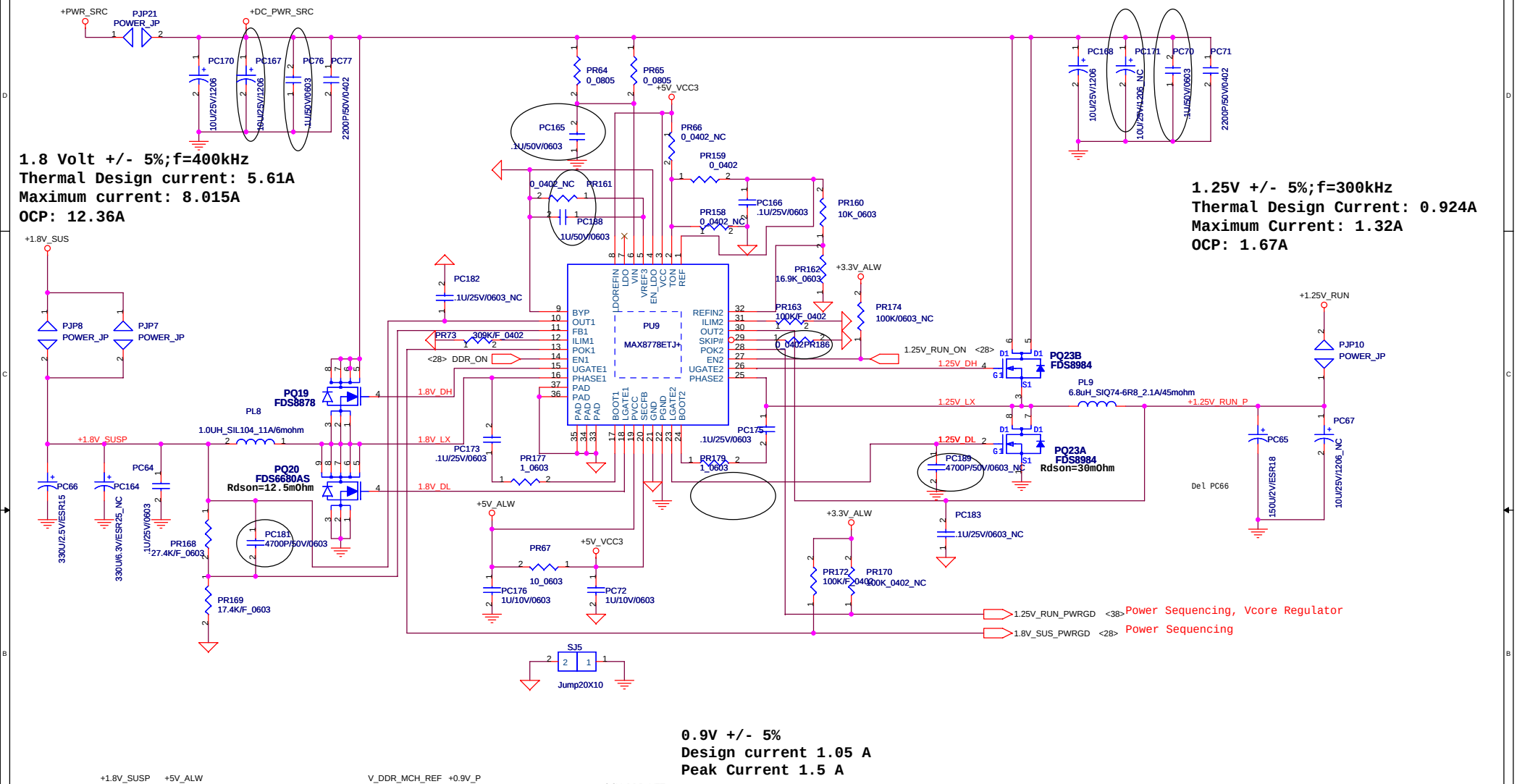


QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
Size	Document Number FM5	Rev 0.1
Date: Monday, March 05, 2007	Sheet 41 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



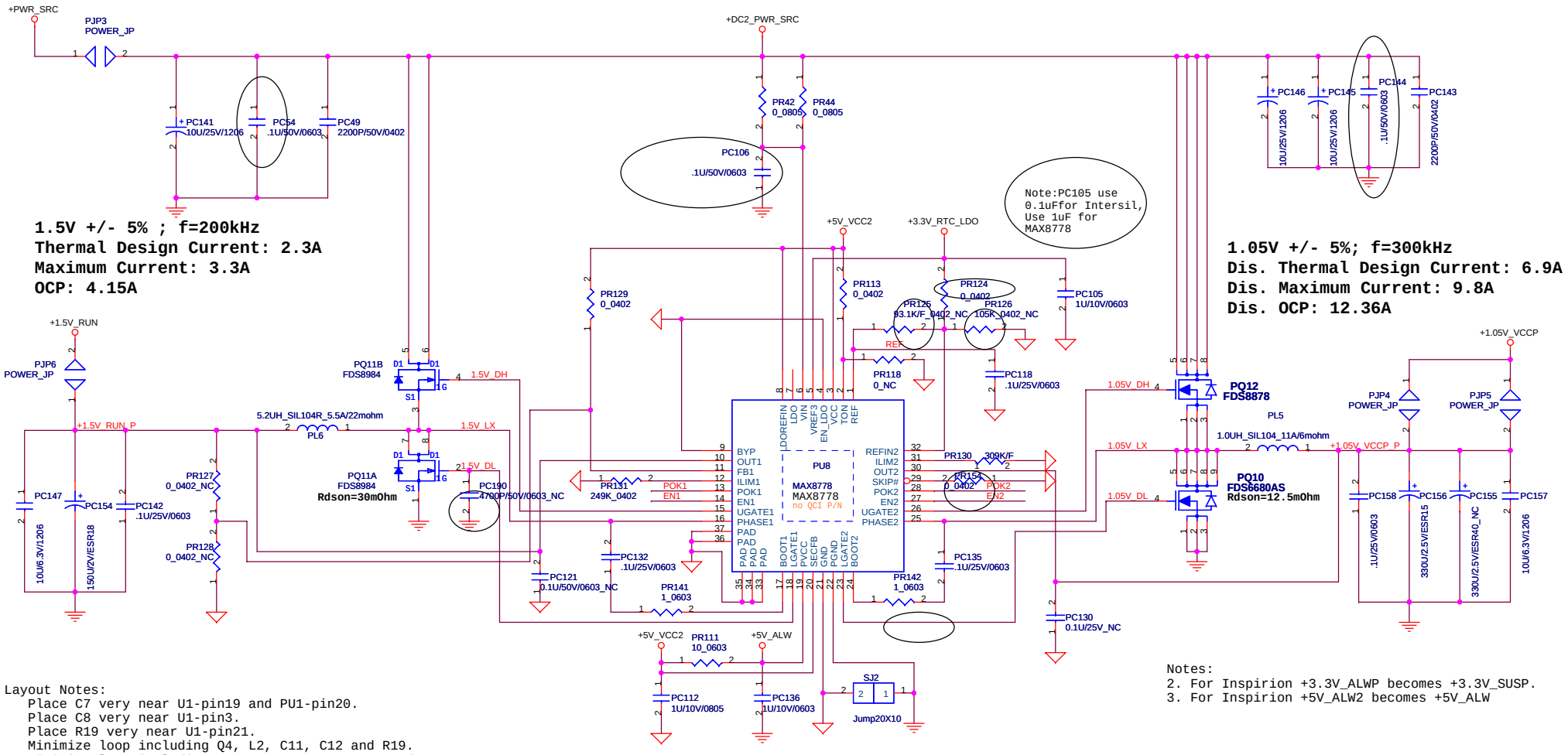
QUANTA COMPUTER

Title	1.25V,1.05V,1.8V,0.9V	
Size	Document Number FM5	Rev 0.1
Date: Monday, March 05, 2007	Sheet 42 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

+1.5V_RUN /+1.05V_VCCP /+3.3V_ALW /+3.3_RTC_LDO



Notes:
2. For Inspirion +3.3V_ALWP becomes +3.3V_SUSP.
3. For Inspirion +5V_ALW2 becomes +5V_ALW

Layout Notes:
- Place C7 very near U1-pin19 and PU1-pin20.
- Place C8 very near U1-pin3.
- Place R19 very near U1-pin21.
- Minimize loop including Q4, L2, C11, C12 and R19.
- Minimize loop including Q2, L3, C17, C18, C19 and R19.
- Route GNDA_DC2 using at least 25 mil trace width.
- Minimize GNDA_DC2 trace length.
- Place C15 near U1-pin7.
- Place C20 near U1-pin5.
- Place R7 near U1-pin11.
- Place R12 near U1-pin31.
- Place R3, C10 near U1-pins 24 and 25.
- Place R2, C9 near U1-pins 16 and 17.
- Route +1.05V_BOOT, +1.05V_BOOST, +1.5V_BOOST, +1.5V_BOOST using 25mil trace width and minimize lengths.
- Connect large copper fill areas to PQ1, PQ2, PQ3 and Q4 signals for thermal improvement.
- Minimize length of +1.5V_RUN_PL and +1.05V_VCCP_PL.
- Place C1, C2, C3, C22 very near Q3-pins 5, 6, 7, 8.
- Place C4, C5, C6, C23 very near Q1-pins 5, 6, 7, 8.
- Route +DC2_PWR_SRC using 50 mil trace width and minimize length.
- Route OUT1 and OUT2 away from inductor and switch-node. Sense Vout directly at output bulk cap.

QUANTA COMPUTER

Title	1.5V,1.05V	
Size	Document Number FM5	Rev 1A
Date: Monday, March 05, 2007	Sheet 43 of 51	

WWW.AliSaler.Com

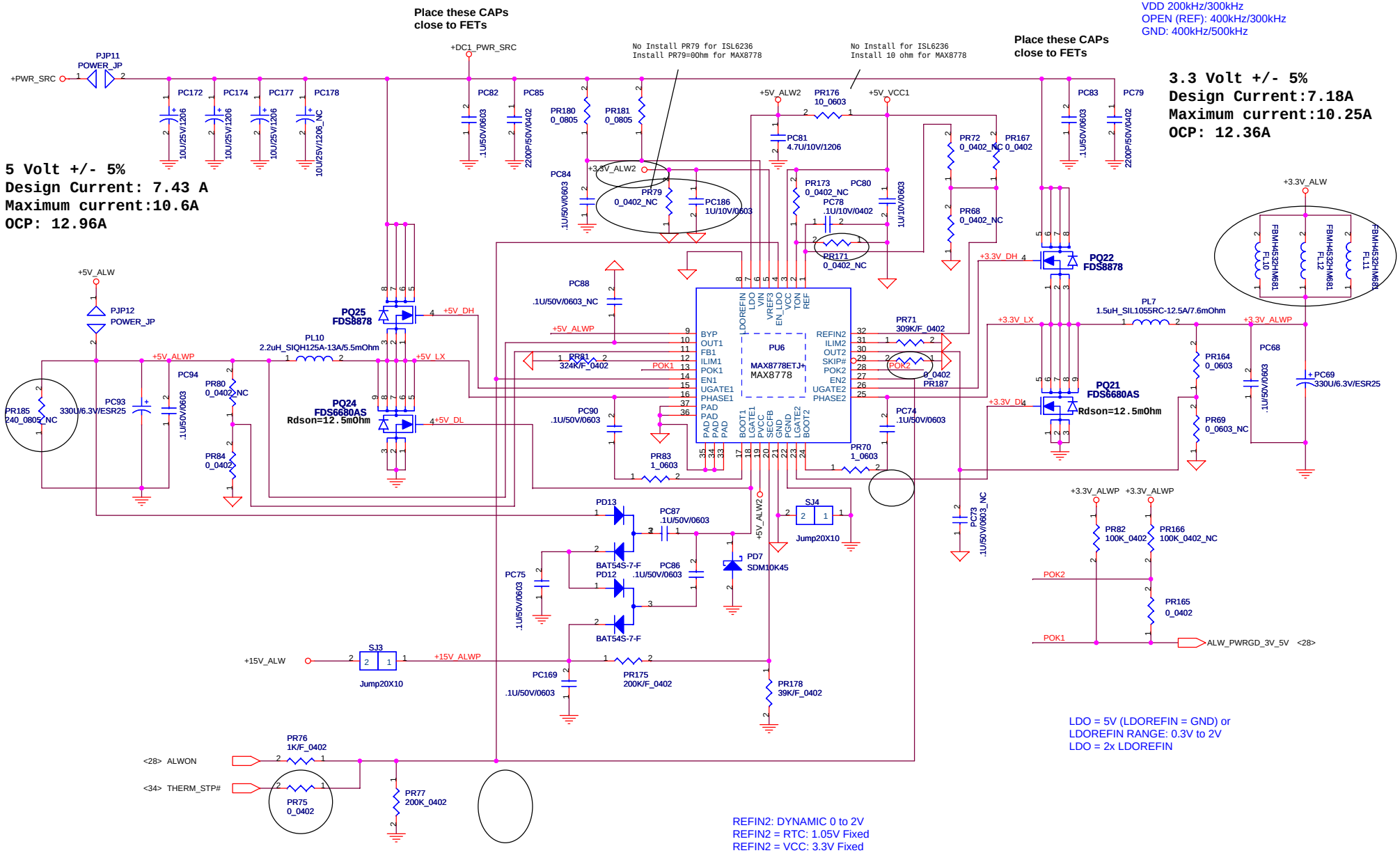
WWW.AliSaler.Com

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Ton:OUT1/OUT2 Switching Frequency
VDD 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz

3.3 Volt +/- 5%
Design Current:7.18A
Maximum current:10.25A
OCP: 12.36A

5 Volt +/- 5%
Design Current: 7.43 A
Maximum current:10.6A
OCP: 12.96A

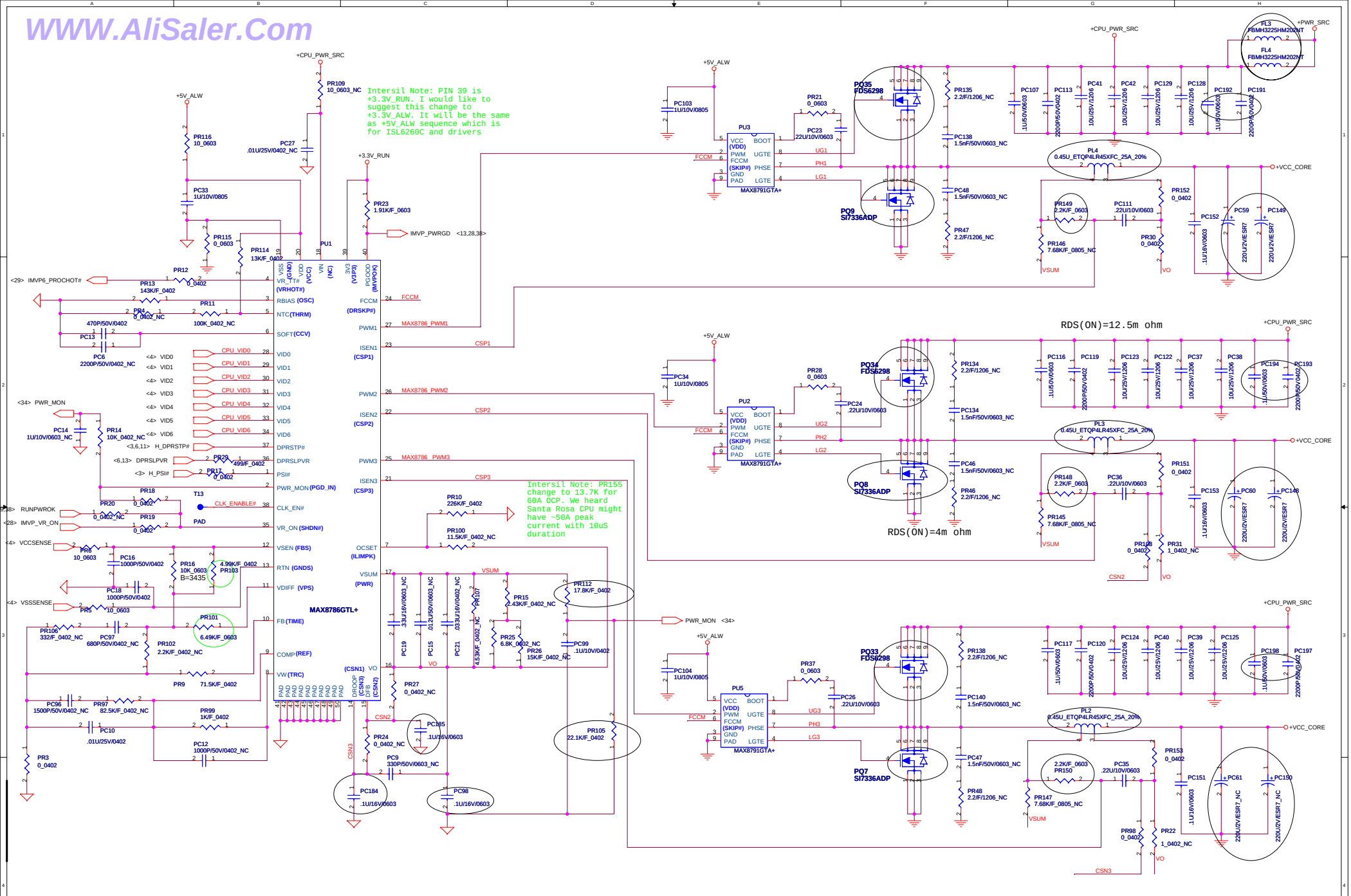


QUANTA COMPUTER

Title	3VALW,5V,3V, power on
Size	Document Number FM5
Rev	1A
Date:	Monday, March 05, 2007
Sheet	44 of 51

WWW.AliSaler.Com

WWW.AliSaler.Com



PHASE 3 populate

QUANTA COMPUTER

Title	CPU POWER		
Size	Document Number FM5		Rev 1A
Date: Tuesday, March 06, 2007		Sheet 45 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	ON
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH	LOW	HIGH	ON	ON	ON	OFF	ON
S5 (SOFT OFF) / M1	LOW	HIGH	LOW	LOW	HIGH	ON	ON	ON	OFF	ON
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
BCM4401B	AD16	REQ#0 / GNT#0	PIRQB
R5C833	AD17	REQ#1 / GNT#1	PIRQC: Card reader PIEQD: 1394

	USB PORT#	DESTINATION
ICH8-M	0	Right Top
	1	Right Bottom
	2	Side TOP
	3	Side Bottom
	4	Ext. USB TOP
	5	DIgital Camera
	6	Express Card
	7	WPAN/Bluetooth
	8	Ext. USB Bottom
	9	WWAN
ECE 5011	1	None
	2	None
	3	None
	4	None

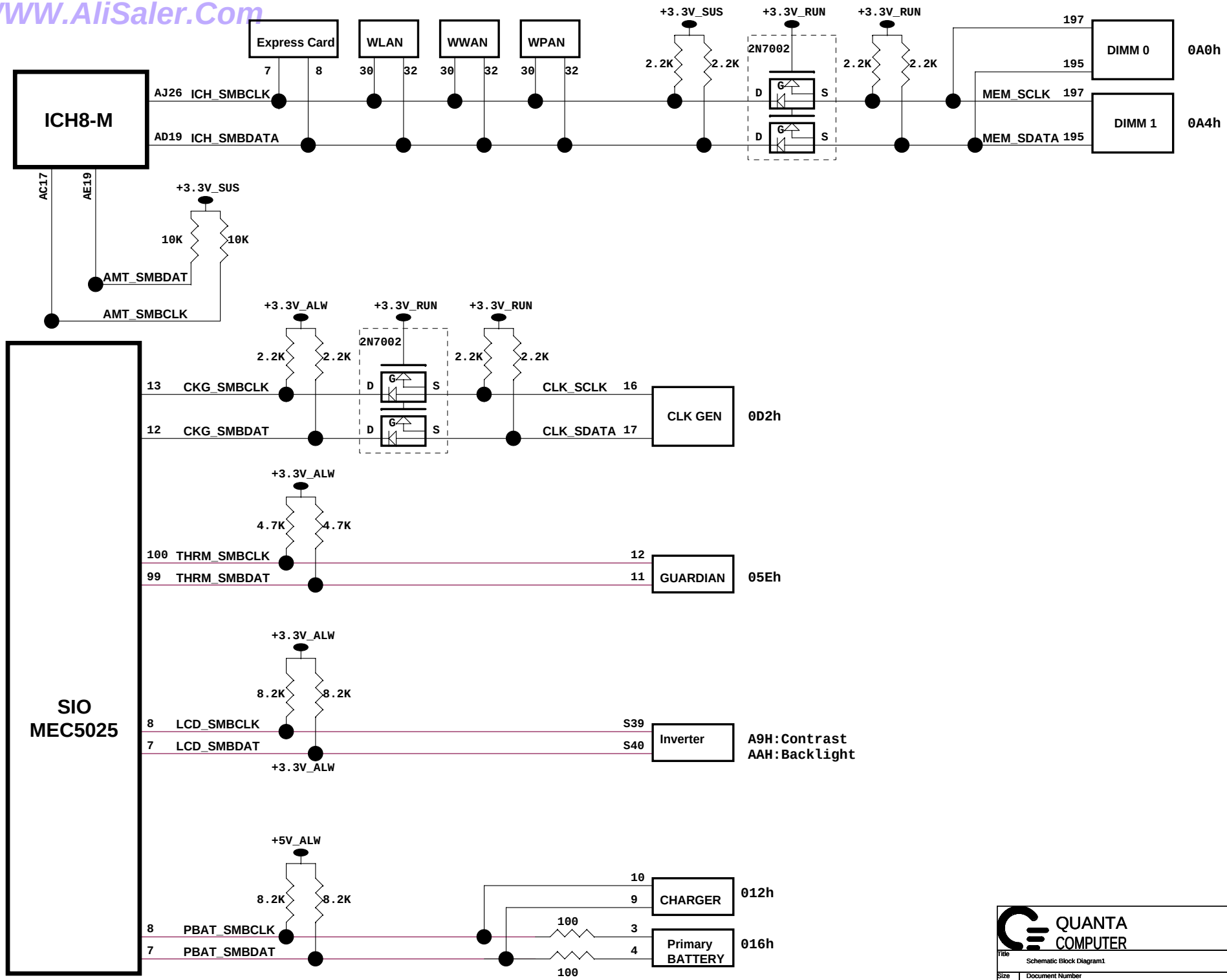
PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number C & G UMA	Rev 1A
Date: Monday, March 05, 2007	Sheet 46 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com



QUANTA COMPUTER

Title	Schematic Block Diagram1	
Size	Document Number C & G UMA	Rev 1A
Date: Monday, March 05, 2007	Sheet 47 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	1	39-45	7/13/2006					Update PWR schematics
	2	13,29	9/20/2006				S3 resume fail	Move PLTRST_DELAY# from EC to ICH8
	3	11	9/20/2006				2nd SATA HDD can't recognize	Move 2nd SATA from port 1 to port 2
	4	38	9/20/2006				Gfx card timing error	Disconnect GFX_PWRGD to system (Delete R463)
	5	38	9/20/2006				Gfx card timing error	Disconnect +1.8V_RUN detect circuit to system (Delete Q47)
	6	39-45	9/21/2006					Update PWR schematics
	7	23	9/21/2006					Add +1.8V_RUN for SATA buffer test (CON4.20-21-22-42-43-44)
	8	37	10/2/2006				Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.
	9	13	10/2/2006				Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Depop R247 & change R227 from 10K ohm to 8.2K ohm
	10	28,33	10/11/2006				In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R507 and R510.
	11	28,29	10/11/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW
	12	28,38	10/11/2006				Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 38 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.
	13	28	10/11/2006					Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29
	14	13	10/11/2006					1) Move SIO_EXT_SCI# from ICH pin AG22 to ICH pin AC19 2) Delete R242 (delete DOCKED# signal)
	15	13	10/11/2006					Reserve LOM_SMBALERT# (ICH8 AG22) & PU resister
	16	24	10/16/2006					Change WPAN USB port from USBP7 to USBP4
	17	23,29	10/18/2006				Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.
	18	12,14	10/18/2006				WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add four .1uF caps in parellel to C813 close to the ICH pins. Add four .1uF caps in parellel to C825 close to the ICH pins.	Add C871~C878 for USB OC. Add C867~C870 in parellel to C825. Add C748,C864~C866 in parellel to C813.
	19	37	10/23/2006				Use LED_MASK# to control BT LED to prevent leakage	Add R336 & change Q13 to BJT
	20	34	10/23/2006				Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R298.
	21	28	10/23/2006				Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k	Change R355,R358 to 2.7K
	22	24	10/23/2006				Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.	

QUANTA COMPUTER

Title	Change List		
Size	Document Number JM7B		Rev 1A
Date:	Monday, March 05, 2007	Sheet 49 of 1	

WWW.AliSaler.Com

WWW.AliSaler.Com

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
C/G DISCRETE	23	17	10/26/2006				Chipset side spec. Differetial CLK raise/fall slew rate is 2.5~8 V/ns, only express card and mini card is 0.6~4V/ns. BITCLK rise/fall slew rate in 1-3 V/ns &	Change serial resistors (PR4,PR5,PR10,PR12,PR13) to meet the CLK SPEC
	24	37	10/26/2006				Change LED control method	
	25	37	10/26/2006				Add OR gate for BT_ACTIVE	
	26	13	10/26/2006				M08 GPIO A14 update. Original EC5011 pin66 CCD_VDD_ON move to IC8 pinAD10 GPIO48 and add 100K ohm pull down.	Move CCD_VDD_ON from EC5011 pin66to IC8 pin AD10 GPIO48 and add 100K ohm pull down.
	27	25	10/26/2006				For Comm team suggestion (GG list), pop C217 for WWAN	
	28	39 - 45	10/31/2006				PWR team updat schemtics - 10/23	

QUANTA COMPUTER

Title	Change List	
Size	Document Number JM7B	Rev 1A
Date: Monday, March 05, 2007	Sheet 50 of 1	

WWW.AliSaler.Com

WWW.AliSaler.Com

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G DISCRETE	29	24 - 25	11/1/2006				For EMI request, add RC circuit for Mini card clk request	Add R543, C880, R186, C649, R544, C181
	30	39	11/1/2006				For +3.3V_RUN inrush current, it may over OCP (12.36 A)	Change PC58 from 470 pF to 6800 pF
	31	32	11/3/2006				For AP - THN+D fail, change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1206	Change C306, 307 to 0.033uF/16V/X7R/1206 & C326, C329 to 1uF/16V/X7R/1207
	32	32	11/3/2006				'PO' noise in resume from S3,S4,S5	Reserved the AUD_AMP_MUTE# for 'PO' noise
	33	39 - 45	11/09/2006				PWR team updat schemtics - 11/08	
	34	17	11/09/2006				Change R44 to 2.2K per Intel recommend value.	
	35	12 - 13	11/21/2006				Due to Intel-ICH8 uses GPIO20 pin AE11 as an Internal Strapping at power up	Move PCIE_MCARD2_DET# from GPIO20 to ICH8 GPIO5/PIRQH# pin B3.
	36	13	11/21/2006				GPIO18 is default as an output at power up, it will drive 1Hz output at power up. Per Intel this GPIO could not be connected to GND	Add 4.7K series - R547 resistor to separate it
	37	32	11/22/2006				There is potential back drive from the codec DVdd back to the AVdd supply due to an internal ESD diode	add 100kohm resistor (R253) between pin 40 and +3.3V_RUN and a 1000pF cap (C643 below) from Pin 40 to ground
	38	35 - 36	11/28/2006				GG list -- COMM team request	1.Change capacitor for U5 pin 79, 94,106 (VDDIO) (C18, C16, C25) to 47pF. 2.Change those three capacitors (C27, C37,C34) to 47pF 3.Add C644 - 47pF capacitor by the pin 57 of U5 4.Change L7 to 0805 package -BK2125LM152. & C23 to 47 pF 5.Add Ferrite Bead BK1608LM152 on 1.8V to EPHY_AVDD pin 57
	39	28-29	11/28/2006				Move DOCK_SMB_PME from MEC5025 SGPIO37 to ECE5018/5011 GPIOC0.Move DOCK_SMB_ALERT# from ECE5018/5011 GPIOC0 to MEC5025 SGPIO37	DOCK_SMB_PME# should be pulled up to +5V_ALW DOCK_SMB_ALERT# should be pulled up to +3.3V_ALW
	40	24	12/01/2006				GG list -- Seperate debug port with MINI-PCI if not necessary	Add 4 0ohm resistors for these pins
	41	24 - 25	12/01/2006				GG list -- Delete decoupling cap	Delete C222 & C424
	42	39 - 45	12/04/2006				PWR team updat schemtics - 12/04	
	43	32	12/08/2006				GG List -- Change audio AMP to TI solution	1.Change codec to TPA9040A4 2.Pop R505, C619 & C614; depop R506, R504 & R497
	44	31	12/13/2006				GG List -- Change power source for LED of dash board	Change JTP1.9 from +3.3V_RUN to +5V_ALW
	45	39 - 45	12/19/2006				PWR team updat schemtics - 12/19	
	46	28	12/25/2006				GG List -- Remove EC5025 pin15 GPIO4 AUD_AMP_MUTE# circuit.	NC R538
	47	34	12/25/2006				GG List -- Add THERMATRIP_VGA# function	Pop R441,442,443 and Q35, C568 for THERMATRIP_VGA# trip.
	48	33	12/28/2006				Modify CCD power control soft start function	Change C403 , R284 connect method

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number C & G UMA	Rev 2A
Date: Monday, March 05, 2007	Sheet 50 of 51	

WWW.AliSaler.Com

WWW.AliSaler.Com

Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	
C/G DISCRETE	49	22	1/11/2006				XD card detect function error	
	50	29	1/11/2006				Base on A16 GPIO : Change net name from BID2 to CHIPSET_ID1	
	51	37	1/24/2007				Add 0ohm_NC(R571) resistor pad connected from Coex1_BT_Active_MINI to Coex1_BT_Active	
	52	32	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R560, R561, R562 and R563 on AUD_SPK_L1, AUD_SPK_L2, AUD_SPK_R1, AUD_SPK_R2 trace
	52	33	1/24/2007				Audio solution for pass EMI 225MHz and 451MHz radiation emission test.	Added R564, R565, R566 and R567 on AUD_LINE_OUT,AUD_HP_OUT
	53	13	1/24/2007				GG List -- CCD_ON pull down R258 100K NC.	
	54	37	2/5/2007				Blue LED brightness is too high	Change R30,R50,R75,R64 & R36 from 220 ohm to 330 ohm
	55	30	2/12/2007				Prevent SPI CLK overshoot/undershoot issue	Add C896 for RC circuit but not pop it
	56	39 - 45	2/12/2007				PWR team updat schemtics - 2/12	
	57	29	2/12/2007				GG List -- CIR function intermidiate issue	ECE5021 pin7 PWRGD need to pull-down to GND with 0 ohm - Add R568 PD resistor & R569 series resistor (NC)
	58	44	3/1/2007				PWR team updat schemtics - 3/1	
	59	17	3/2/2007				Per TDC COMM team request - Change L65 to	Fine tune 14M CLK - Change R57 from 33 to 15 ohm & L65 to BLM18SG260
	60	04	3/2/2007				Per reliability issue - Move C98 to C249	De-pop C98 & pop C249

QUANTA COMPUTER

Title	EMI & Screw hole	
Size	Document Number C & G UMA	Rev 2A
Date: Wednesday, March 07, 2007	Sheet 51 of 51	

WWW.AliSaler.Com