

PCB NO: LA-4232P

BOM P/N:

Half Penny Bridge 13.3

Compal Confidential

Schematic Document

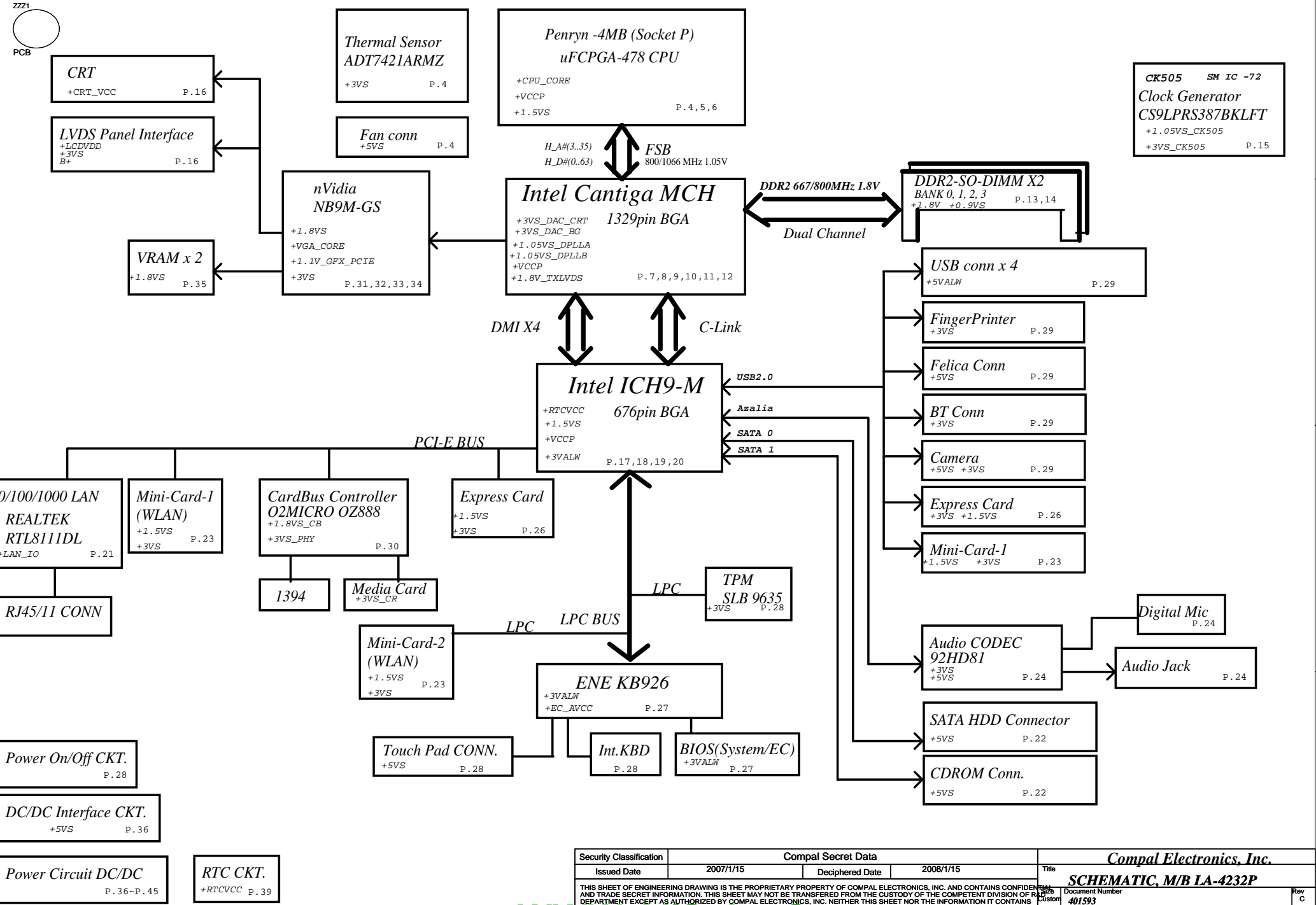
Cantiga + ICH9

2009 / 06 / 01 Rev:1.0(A00)

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Half Penny Bridge 13.3

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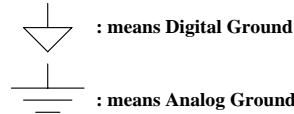


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power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +1.8VS +1.1VS +0.9VGA
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

ICH9-M	USB PORT#	DESTINATION
	0	JUSBP1
	1	CAMERA
	2	JUSBP3(SINGLE)
	3	Felica
	4	Blue Tooth
	5	Finger Printer
	6	JMINI2-WLAN
	7	Express card
	8	JUSBP3(DUEL TOP)
	9	JUSBP3(DUEL BOTTOM)
	10	NA
11	NA	

Symbol Note :



@ : means just reserve , no build
 CONN@: connect
 VGA@: discrete component
 UMA@: uma component
 TPM@: TPM compoent

PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	GLAN RTL8111DL
Lane 3	MINI CARD-2 WLAN
Lane 4	EXPRESS CARD
Lane 5	CARD READER OZ888
Lane 6	NA

SATA	DESTINATION
Lane 0	HDD
Lane 1	ODD
Lane 4	NA
Lane 5	NA

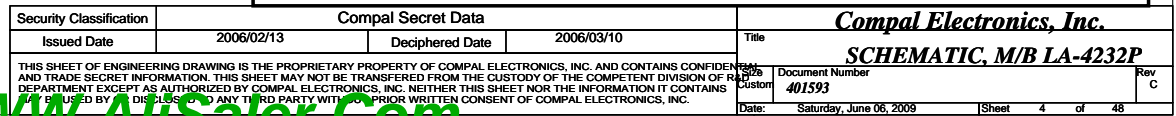
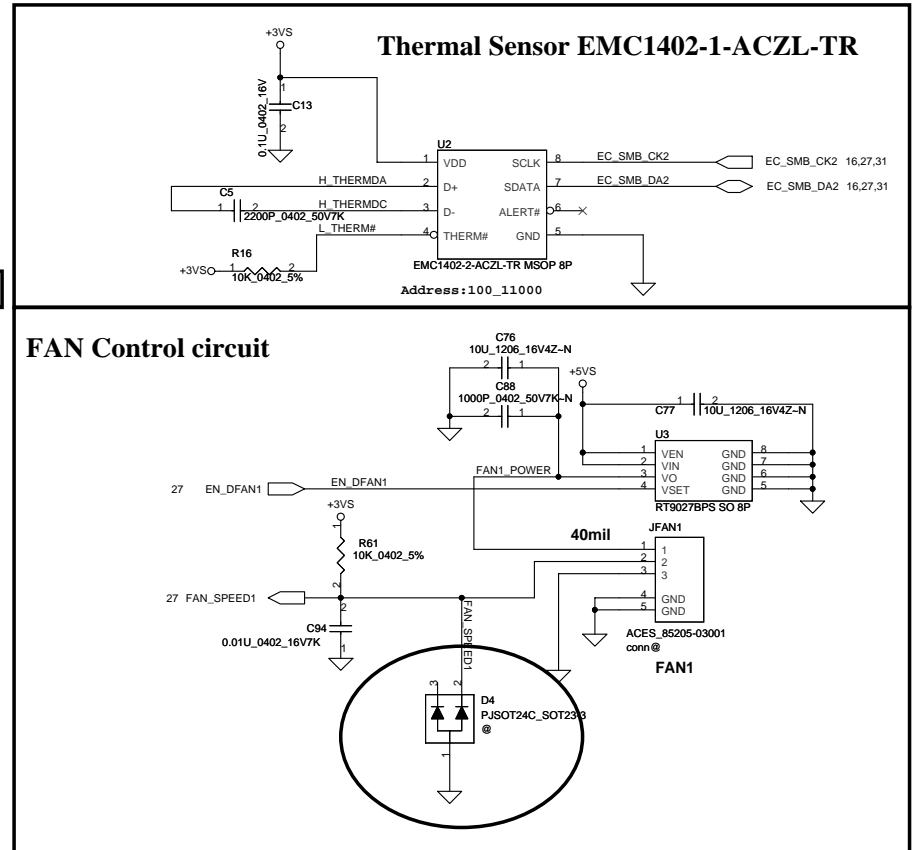
SMBUS Control Table

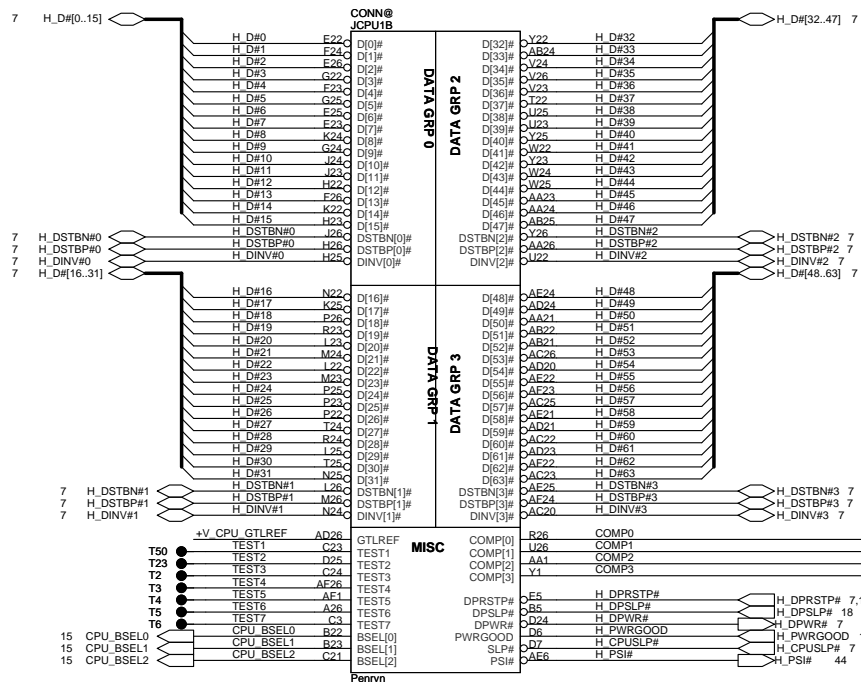
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

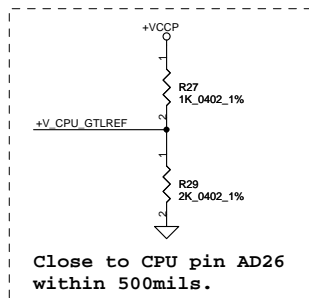
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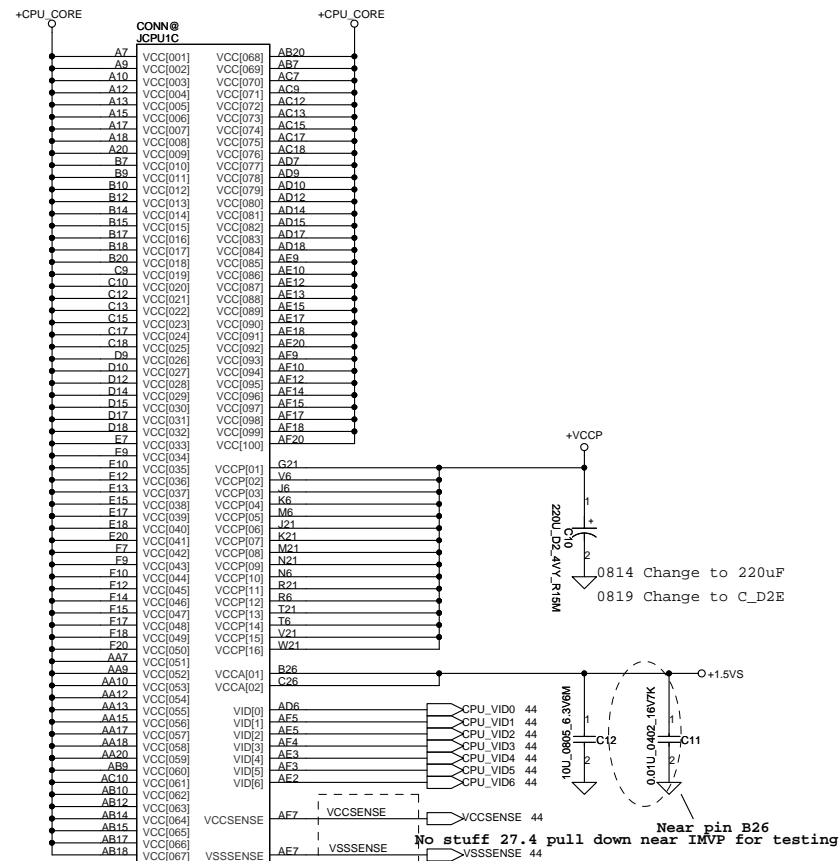


layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU
 layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

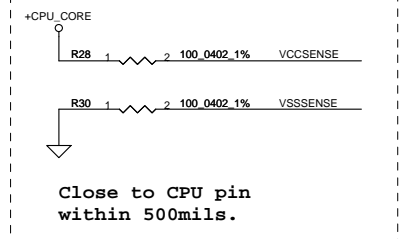
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

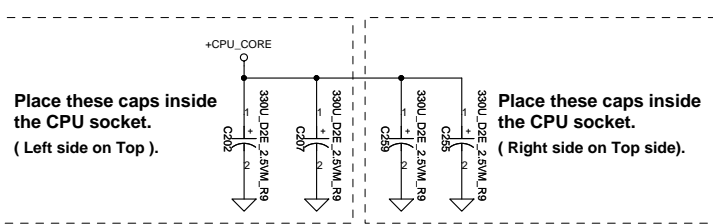
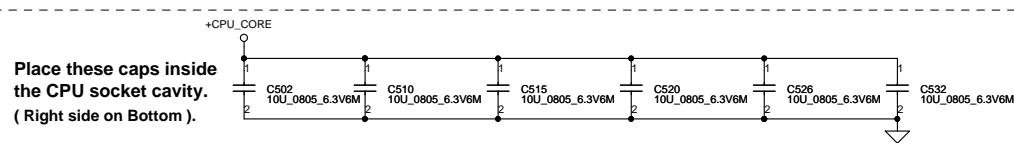
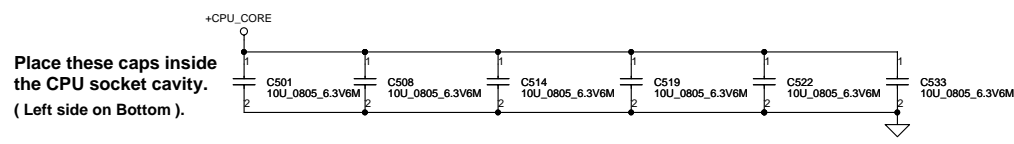
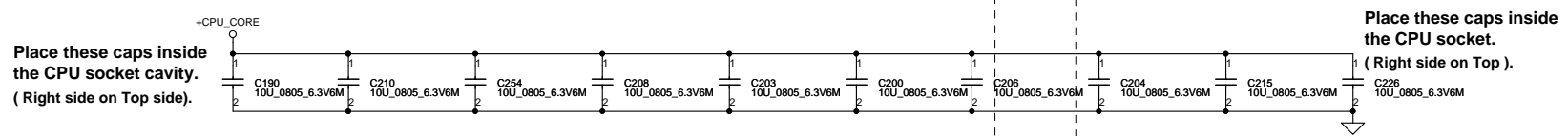
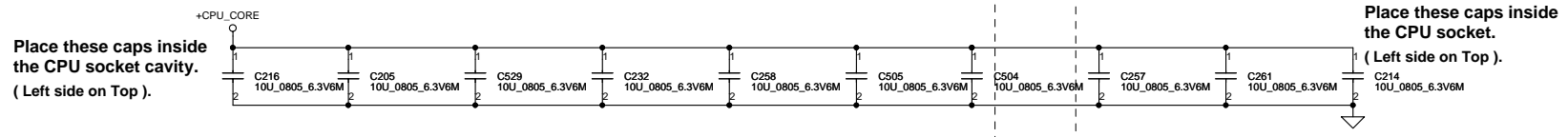
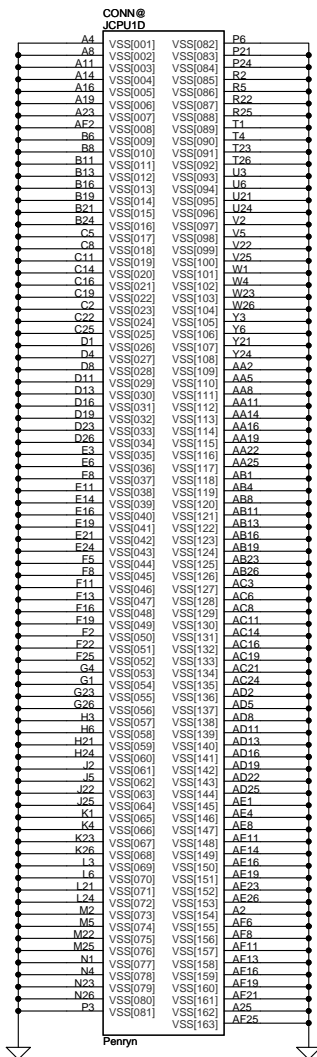


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 21 mils. COMP[1,3] trace width is 5

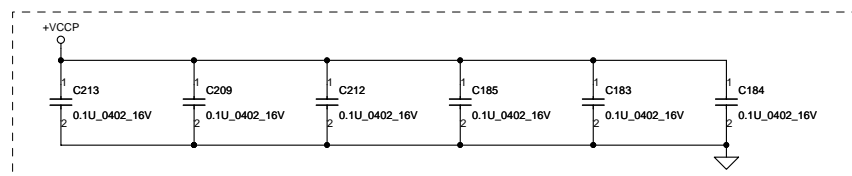


Length match within 25 mils. The trace width/space/other is 20/7/25.

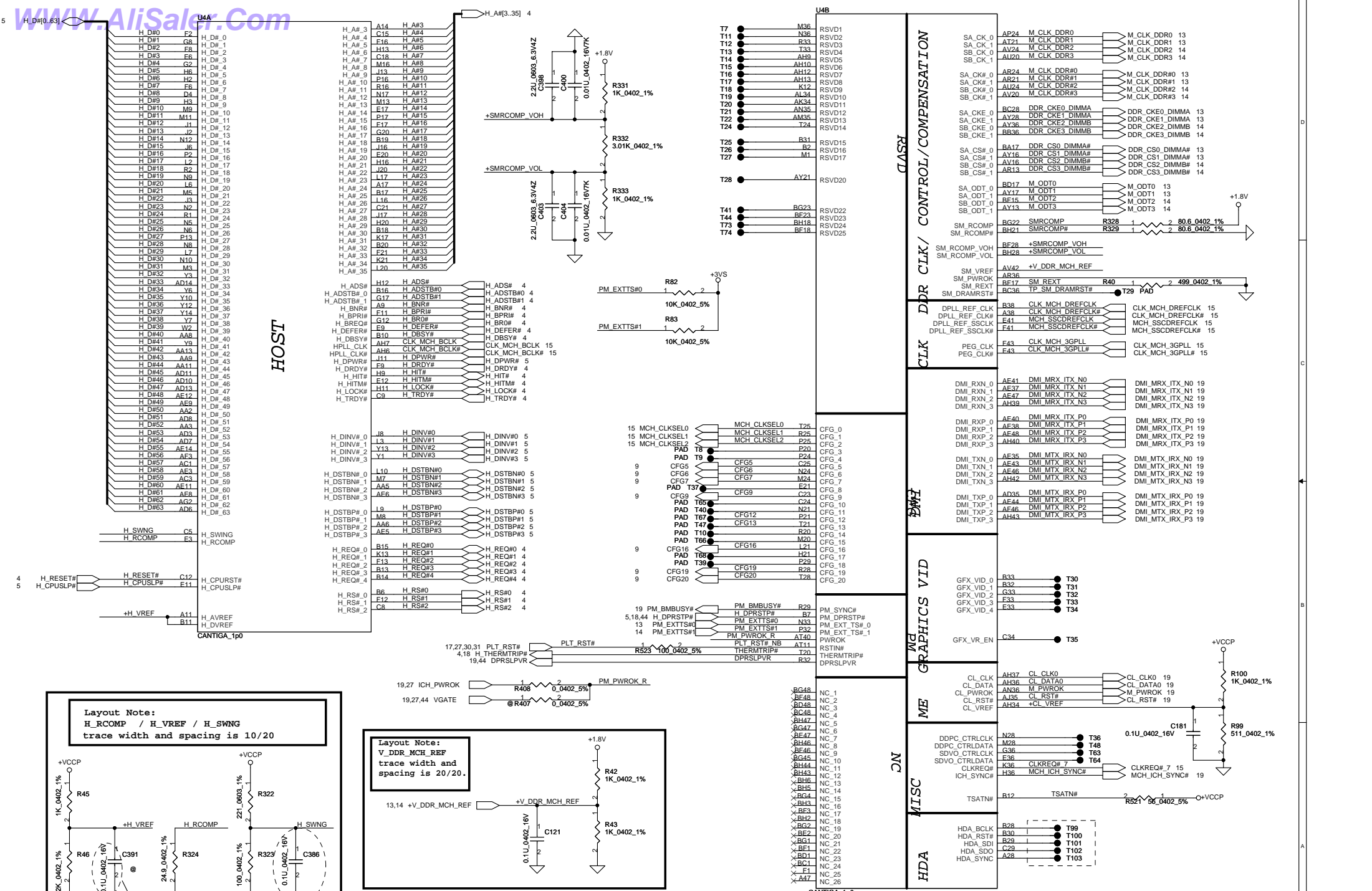


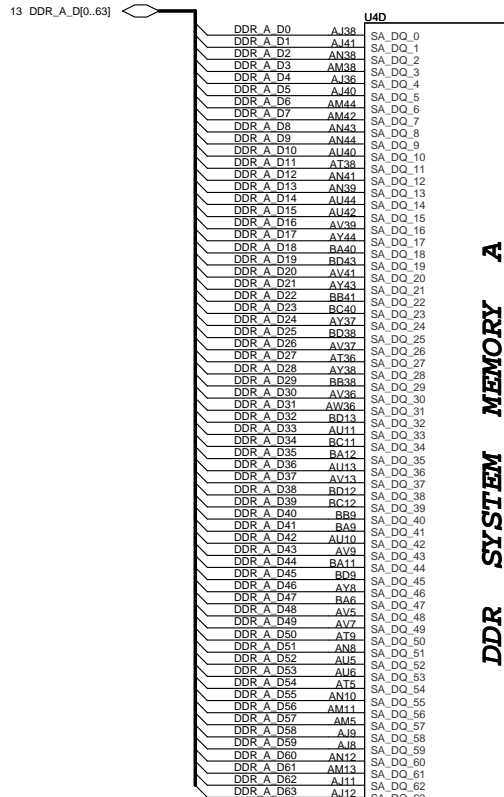


ESR <= 1.5m ohm
Capacitor > 880 uF

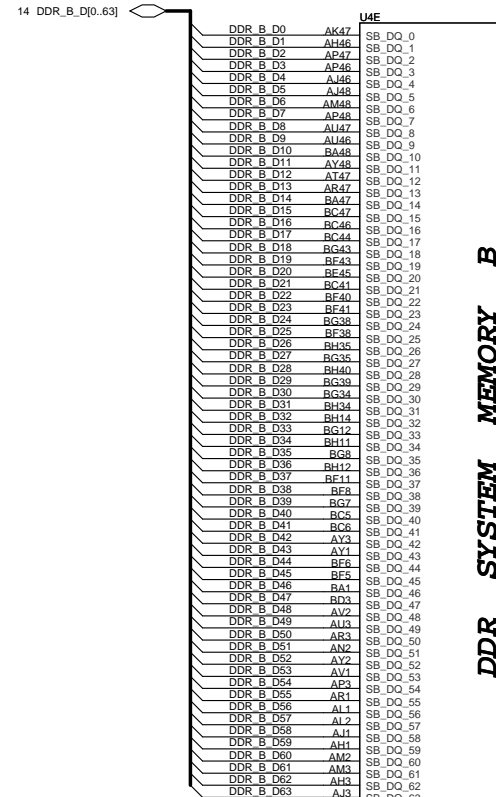


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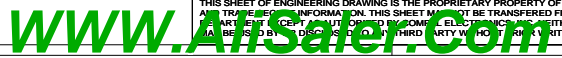


DDR SYSTEM MEMORY A



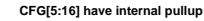
DDR SYSTEM MEMORY B

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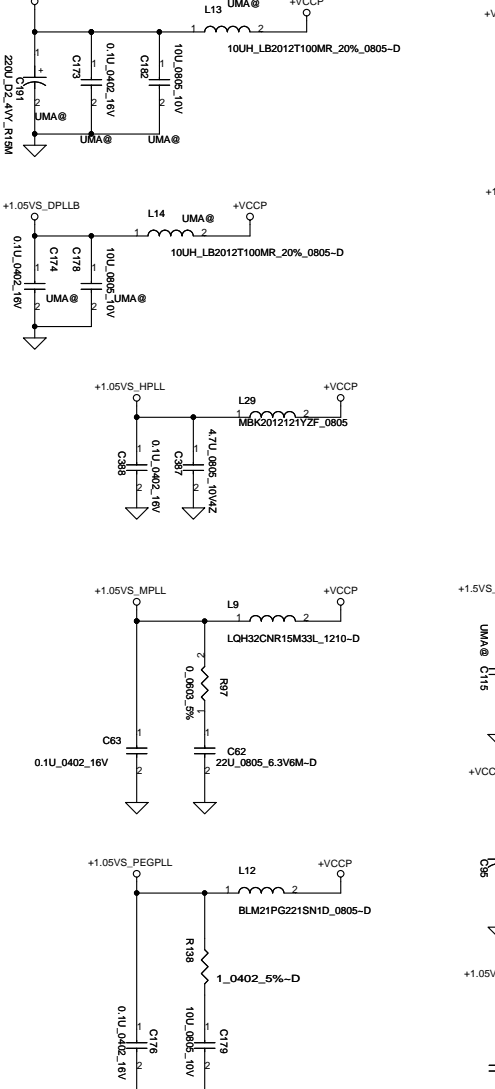
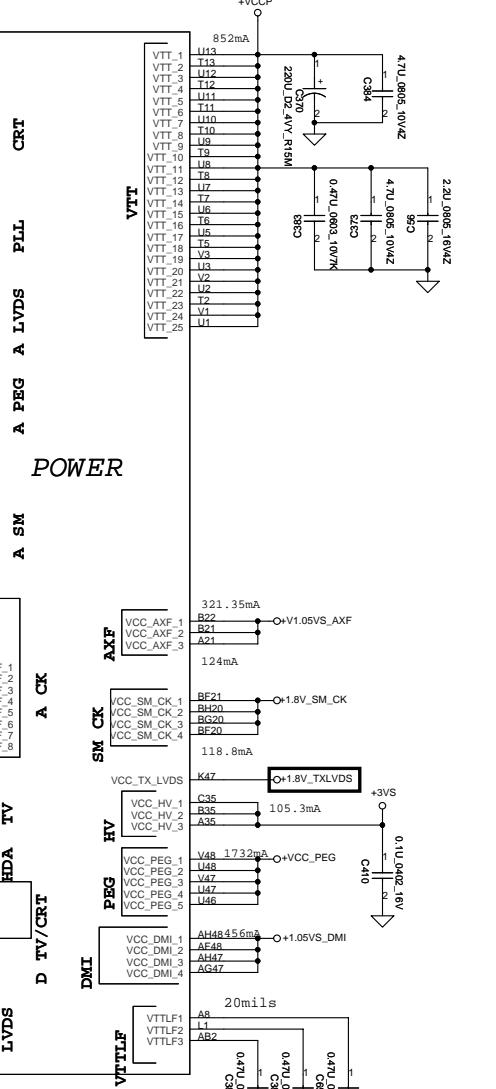
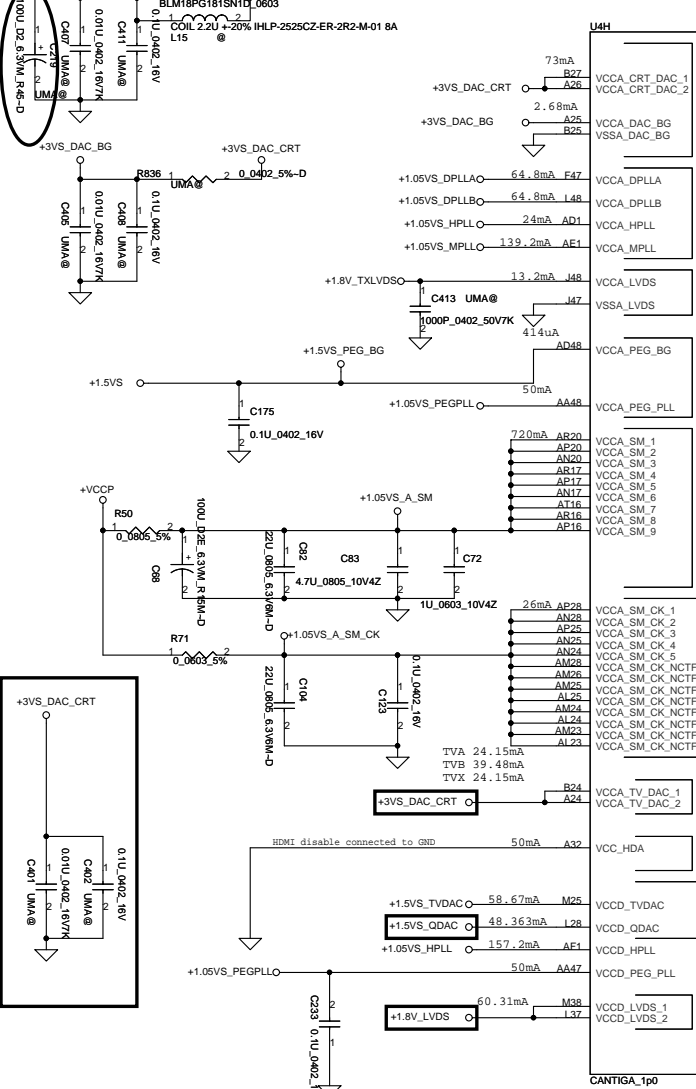
PEGCOMP trace width
and spacing is 20/25 mils.

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The ITPM Host Interface is enable * 1 = The ITPM Host Interface is disable
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipser suite with no confidentiality 1=(TLS)chipser suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

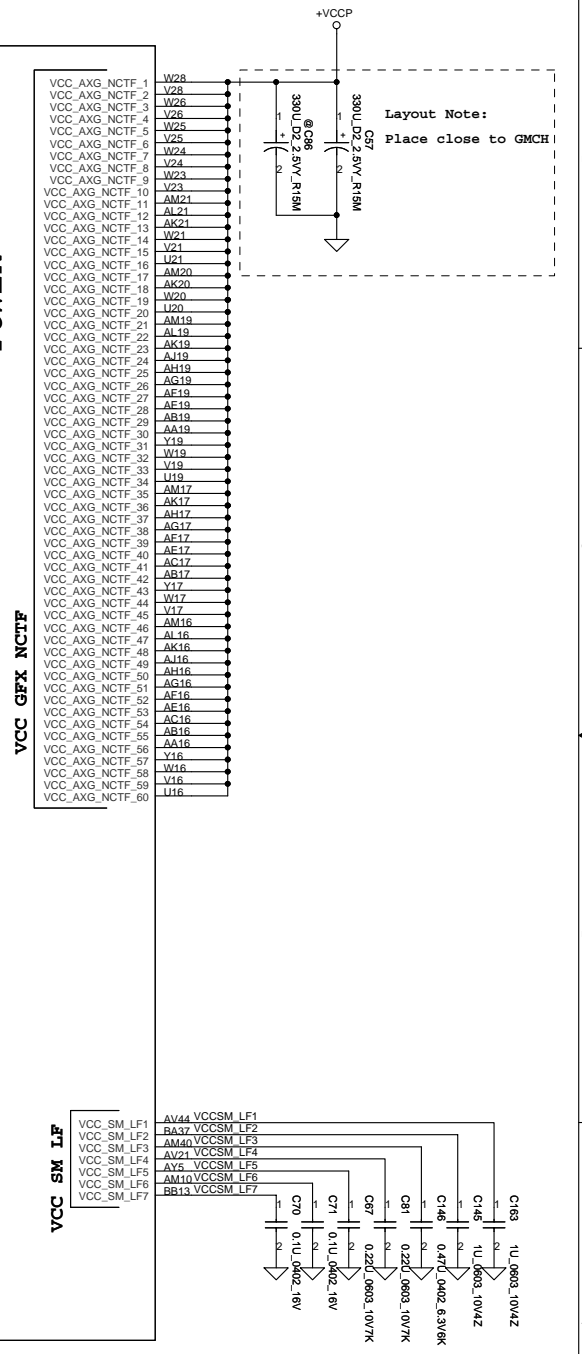
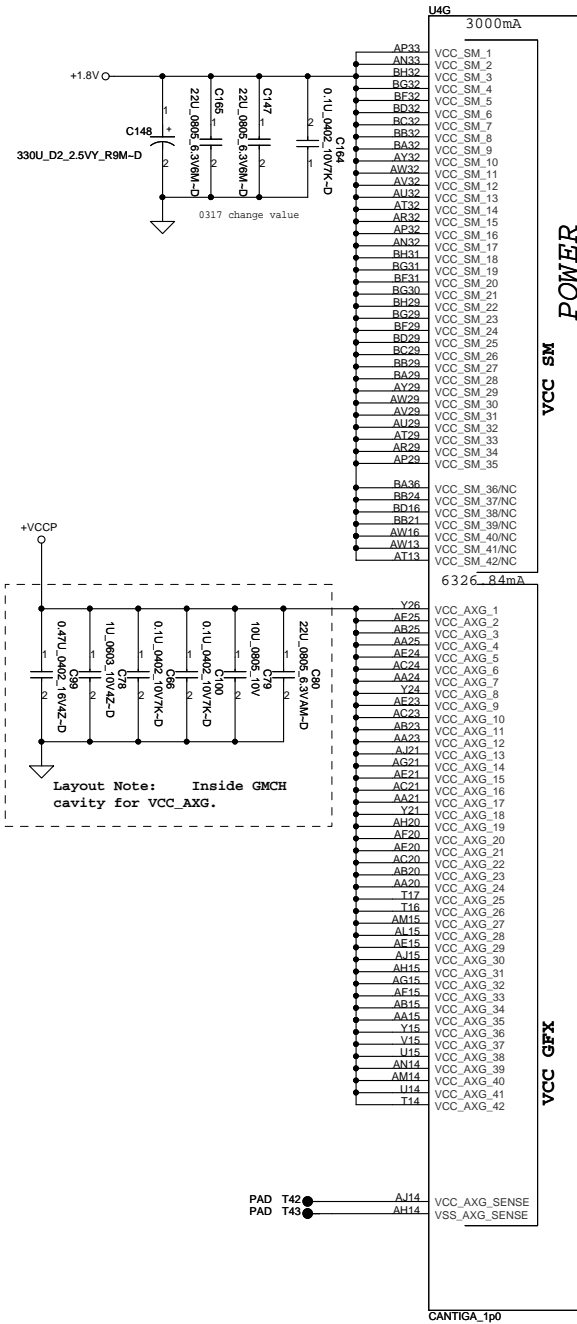
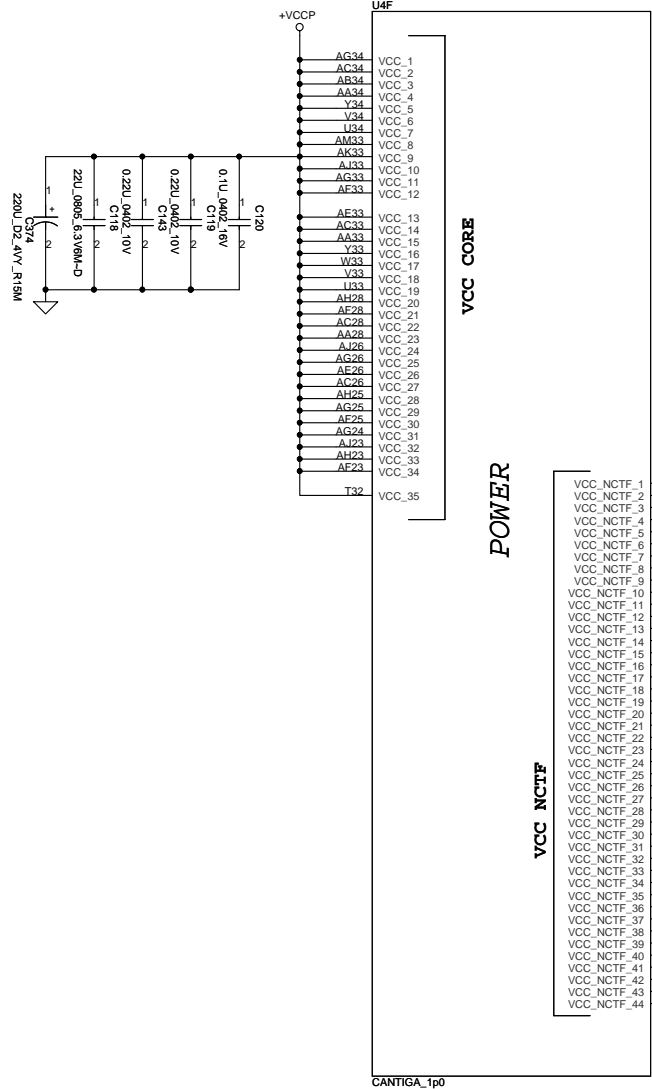


+3VS

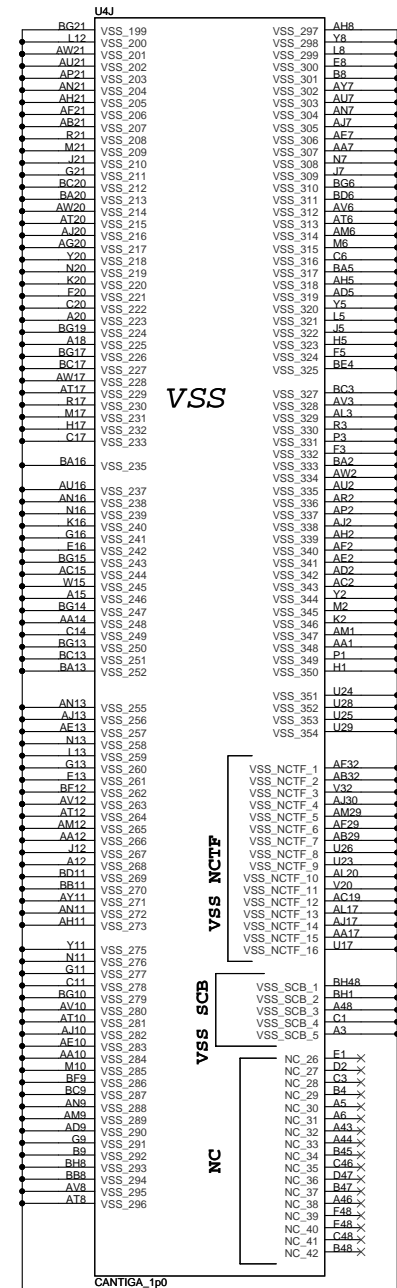
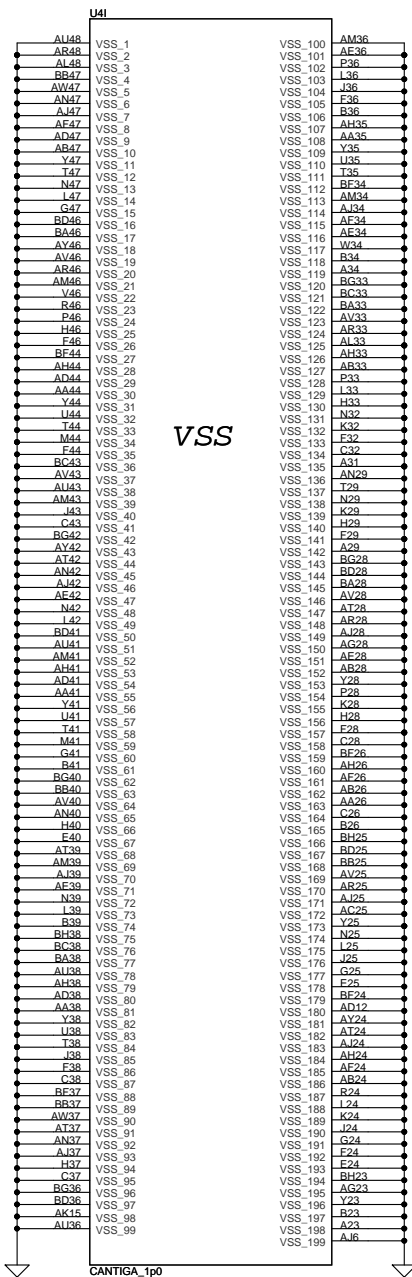
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Extnal Graphic: 1210.34mA
integrated Graphic: 1930.4mA



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The schematic shows a multi-stage common-emitter amplifier circuit. The input signal is applied to the base of the first stage through a coupling capacitor C-20 (2.2μF). The first stage consists of a BC177 NPN transistor with its emitter connected to ground via a 6.8kΩ resistor (R-E1) and its collector connected to a 330kΩ load resistor (C-24) and a 2.5V Zener diode (ZD1) in parallel. A 1.8V supply is connected to the base of the first stage through a 2.2kΩ resistor (R-B1). The output of the first stage is coupled to the second stage through a 0.1μF capacitor (C-21). The second stage also uses a BC177 NPN transistor with a 6.8kΩ emitter resistor (R-E2), a 330kΩ collector load resistor (C-25), and a 2.5V Zener diode (ZD2) in parallel. This pattern repeats for three more stages, each with a 0.1μF coupling capacitor (C-21, C-22, C-23), a 6.8kΩ emitter resistor, and a 330kΩ collector load resistor with a 2.5V Zener diode in parallel. The final output is taken from the collector of the fourth stage through a 0.1μF capacitor (C-24). All transistors are BC177 NPN types.

		+0.9VS			
DDR_A MA5	1	4	3	4	1 DDR_A MA12
DDR_A MA6	2	2	3	2	2 DDR_CKE0 DIMMA
DDR_A MA1	1	4	3	4	1 DDR_A MA7
DDR_A MA3	2	2	3	2	2 DDR_A MA6
DDR_A RAS#	1	4	3	4	1 DDR_A MA9
DDR_CS0 DIMMA#	2	2	3	2	2 DDR_A BS#2
DDR_A BS#0	1	4	3	4	1 DDR_A MA4
DDR_A MA10	2	2	3	2	2 DDR_A MA2
DDR_A CAS#	1	4	3	4	1 DDR_A MA5
DDR_A WE#	2	2	3	2	2 DDR_A BS#1
DDR_CS1 DIMMA#	1	4	3	4	1 DDR_A MA14
M_ODT1	2	2	3	2	2 DDR_A MA13
DDR_CKE1 DIMMA1	1	4	3	4	1 DDR_A MA11
	2	2	3	2	2 DDR_A MA12

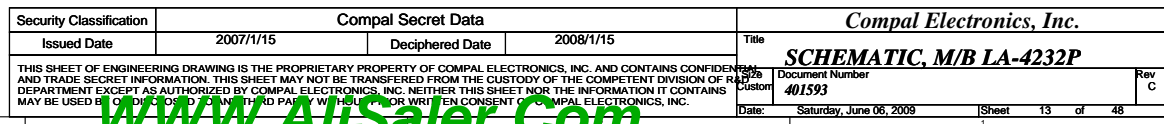
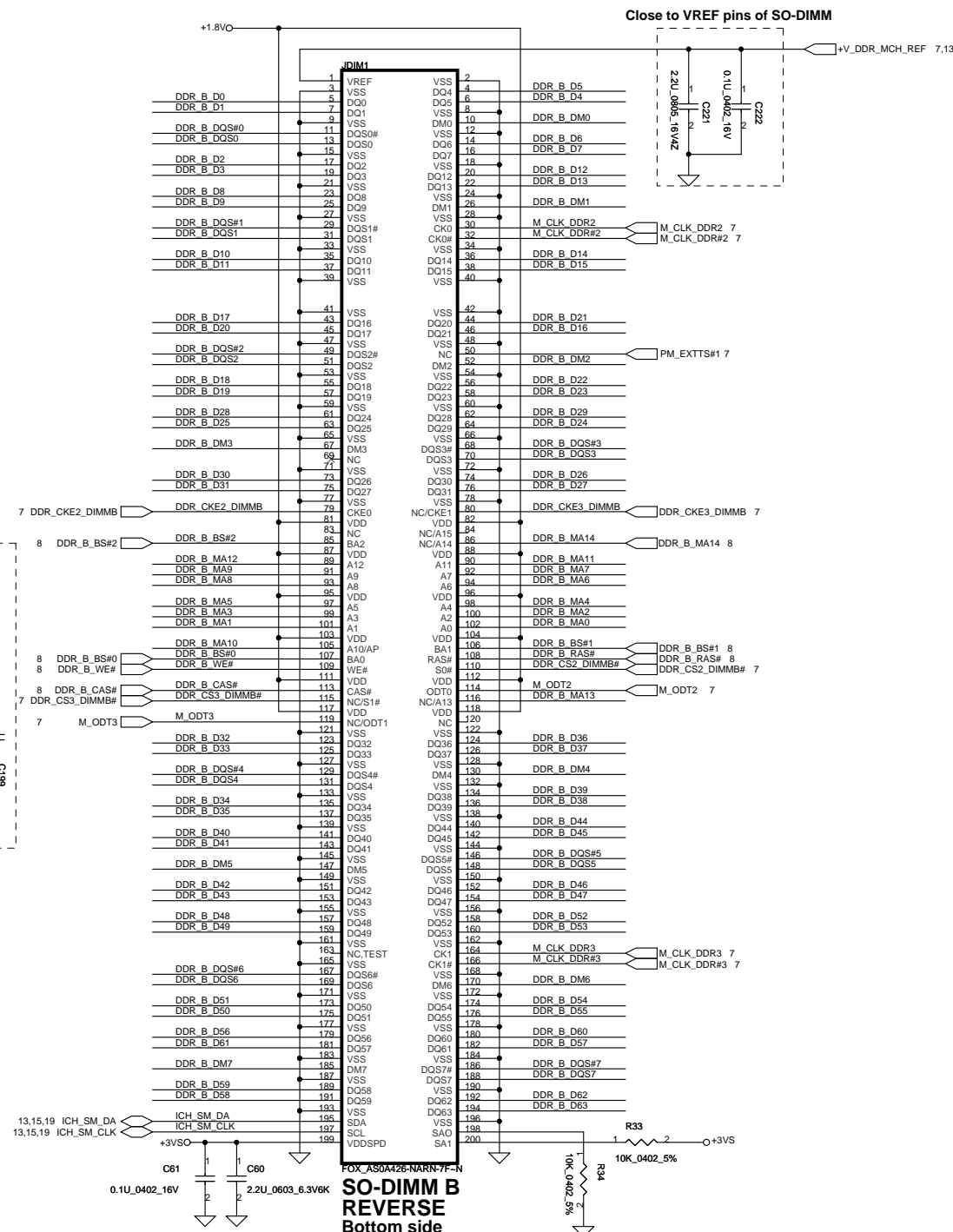


Diagram 1: DDR3 SDRAM Pin Connections. This diagram shows the pin connections for the DDR3 SDRAM components. The components are labeled as follows: RP18, RP10, RP12, RP11, RP9, RP3, RP24, RP26, RP4, and RP25. The connections are as follows:

- RP18: DDR_B MA3 (1), DDR_B MA1 (2), DDR_B BS#0 (1), DDR_B MA10 (2), DDR_B MA0 (1), DDR_B BS#1 (2), DDR_B RAS# (1), DDR_CS2_DIMMB# (2).
- RP10: 56_0404_4P2R_5% (1), 56_0404_4P2R_5% (2).
- RP12: 56_0404_4P2R_5% (1), 56_0404_4P2R_5% (2).
- RP11: 56_0404_4P2R_5% (1), DDR_CS2_DIMMB# (2).
- RP9: DDR_B CAS# (1), DDR_B WE# (2), DDR_CS3_DIMMB# (2), M_ODT3 (1).
- RP3: 56_0404_4P2R_5% (1), 56_0404_4P2R_5% (2).
- RP24: 56_0404_4P2R_5% (1), DDR_B MA12 (2), DDR_B MA9 (2).
- RP26: 56_0404_4P2R_5% (1), DDR_B MA14 (2), DDR_B MA11 (2).
- RP4: 56_0404_4P2R_5% (1), DDR_B MA5 (2), DDR_B MA8 (2), DDR_B MA4 (2), DDR_B MA2 (2).
- RP25: 56_0404_4P2R_5% (1), DDR_B BS#2 (2), DDR_CKE2_DIMMB (2).

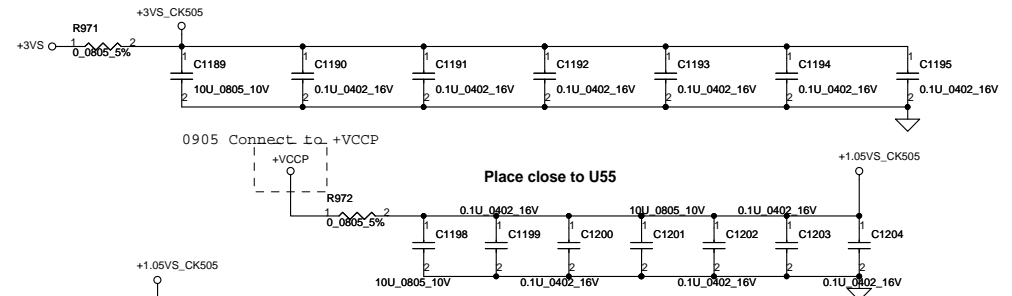
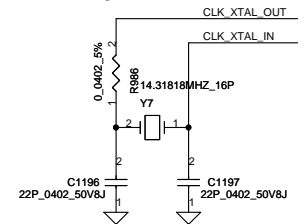
The diagram also shows a +0.9VS power supply connection to the top of the components.



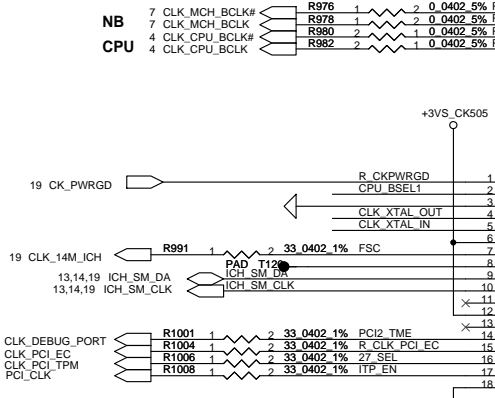
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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

Routing the trace at least 10mil



NB
CPU



Card Bus

Express Card

CPU_STP

ICH_SATA

GLAN

MiniCard_WLAN

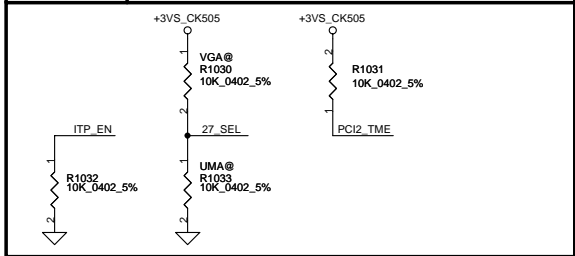
ICH

NB_3GPLL

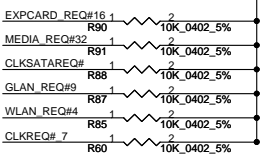
NB_SSC (UMA)

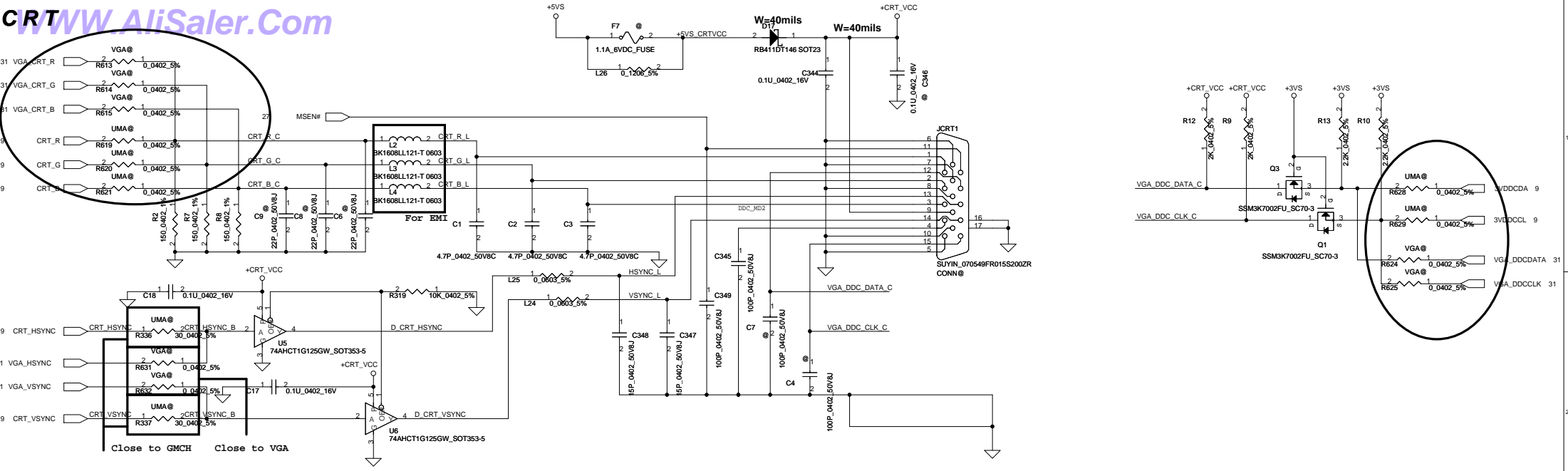
VGA_27M (DIS)

ITP_EN	* 0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)
PCI2_TME	0 = Overclocking of CPU and SRC Allowed *1 = Overclocking of CPU and SRC NOT allowed

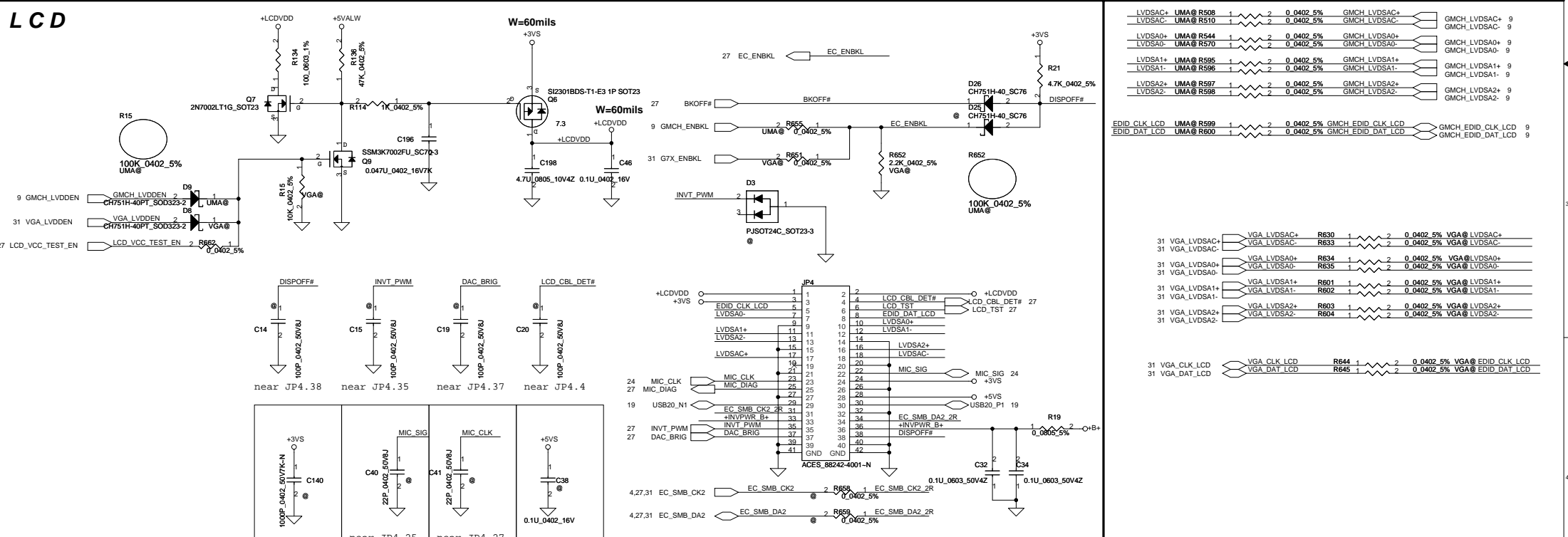


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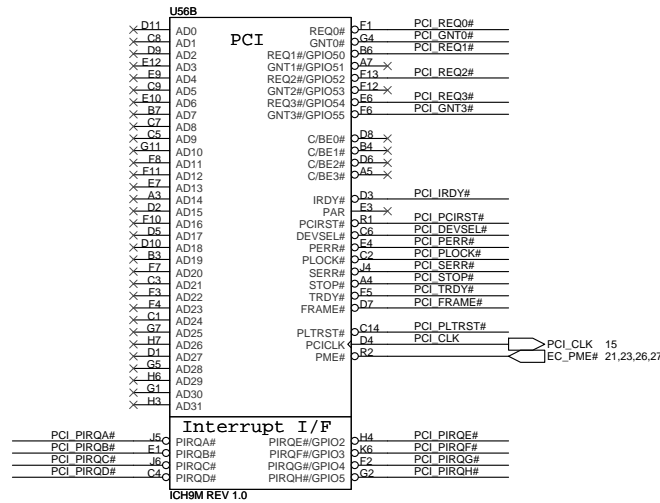
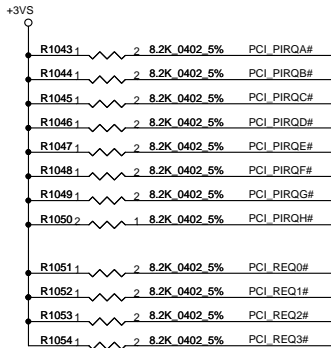
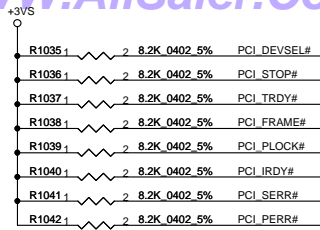




LCD



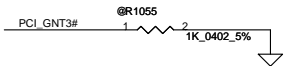
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ICH9M REV 1.0

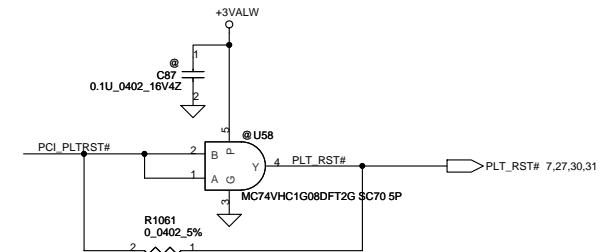
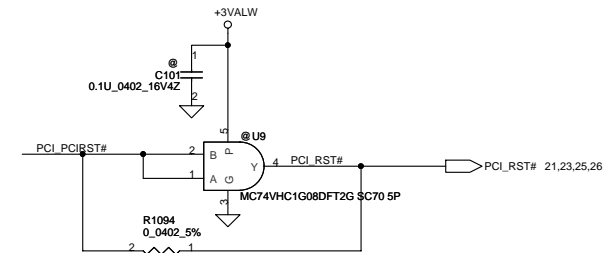
A16 swap override Strap

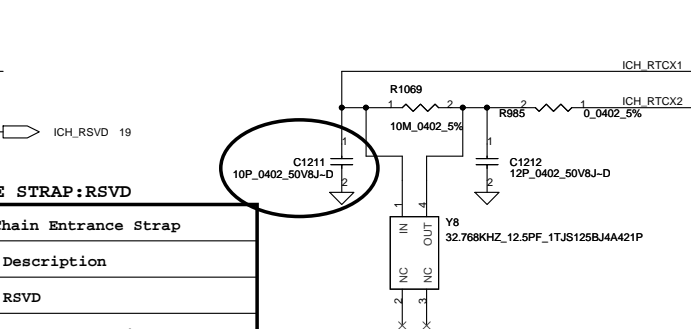
Low= A16 swap override Enable
High= Default *



Boot BIOS Strap

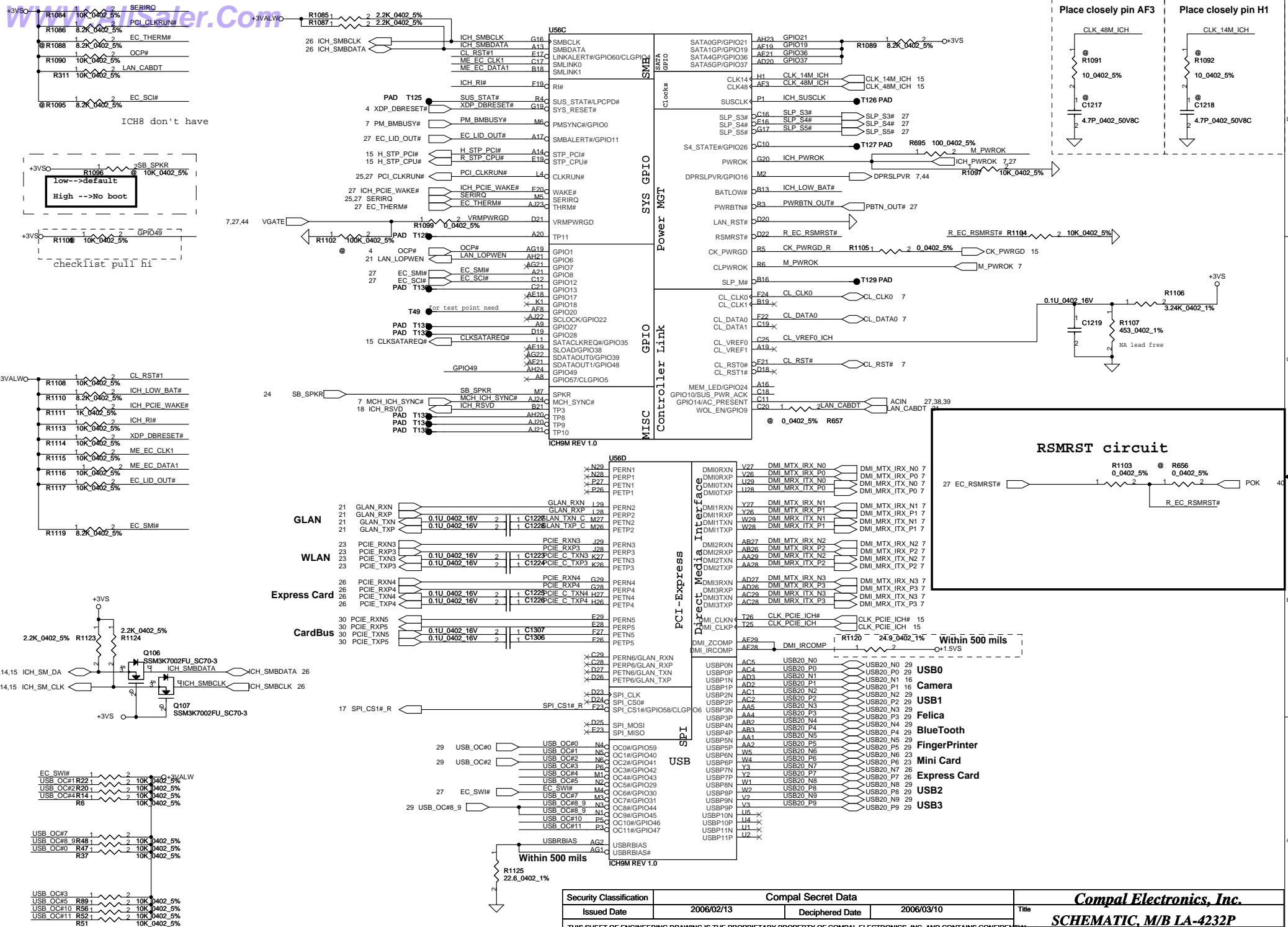
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *





XOR Chain Entrance Strap		
ICH_RSVD_TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

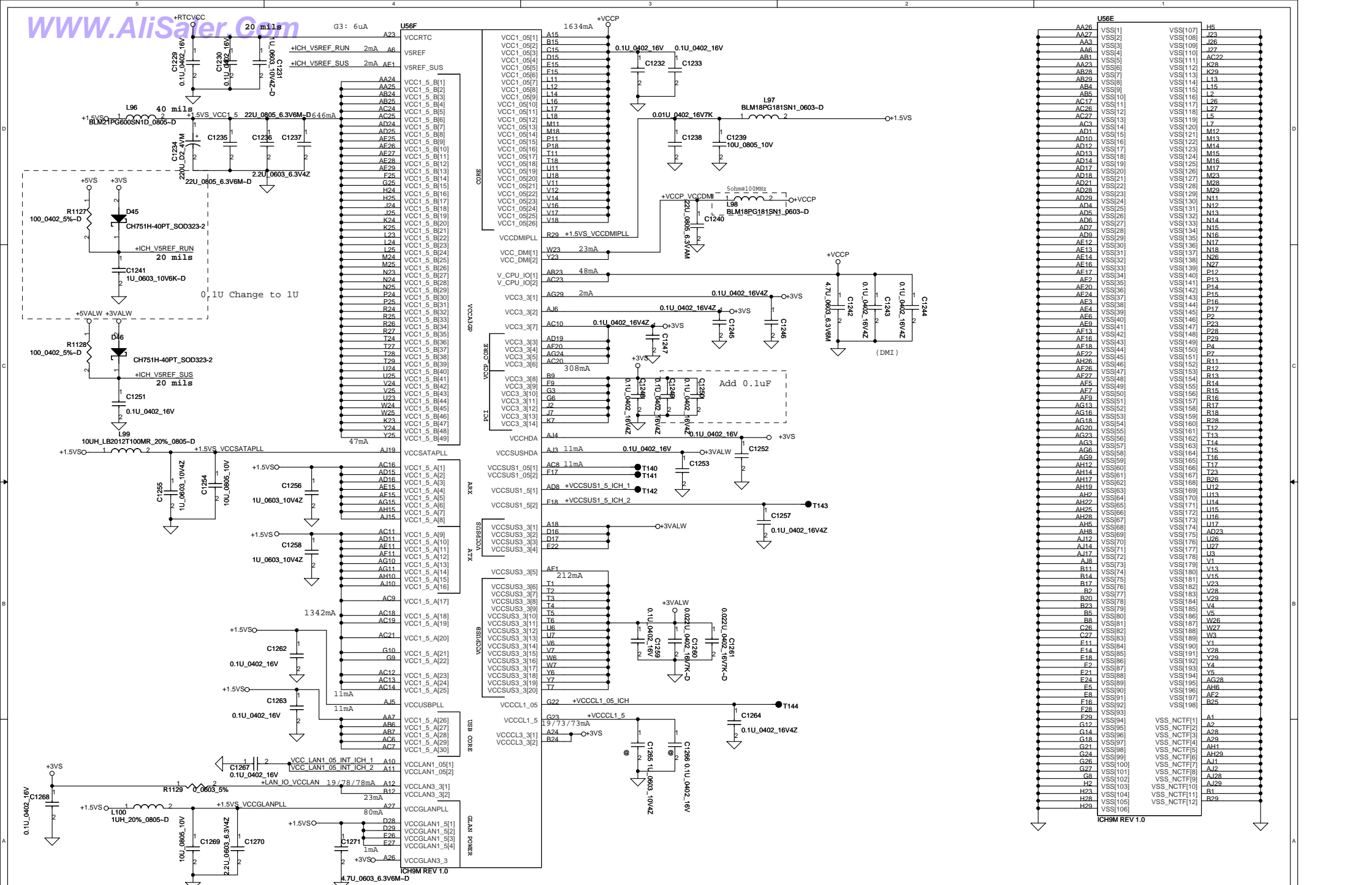
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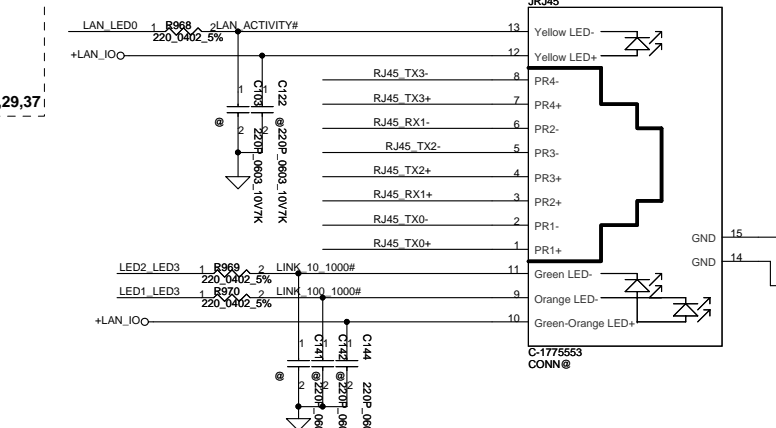
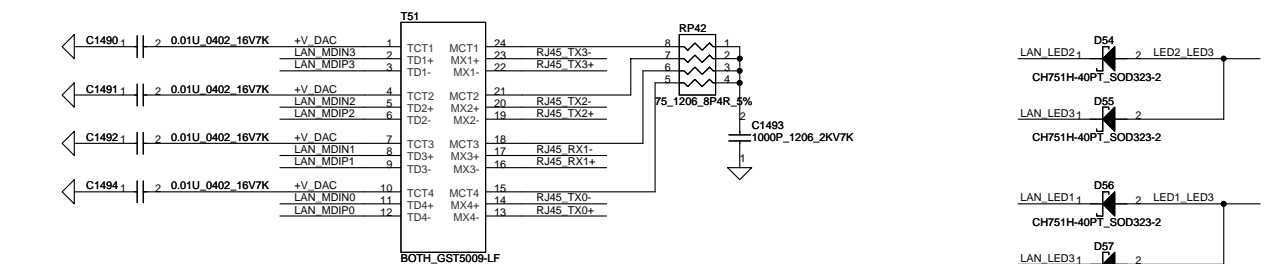
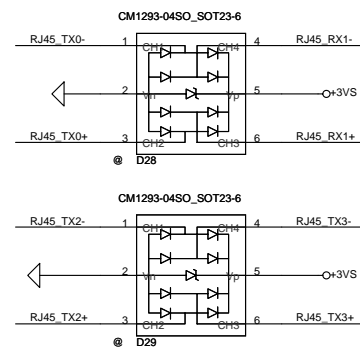
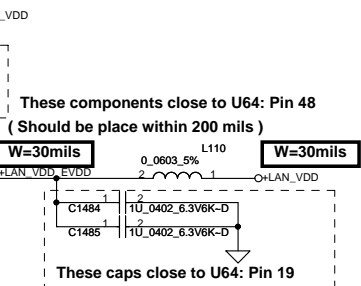
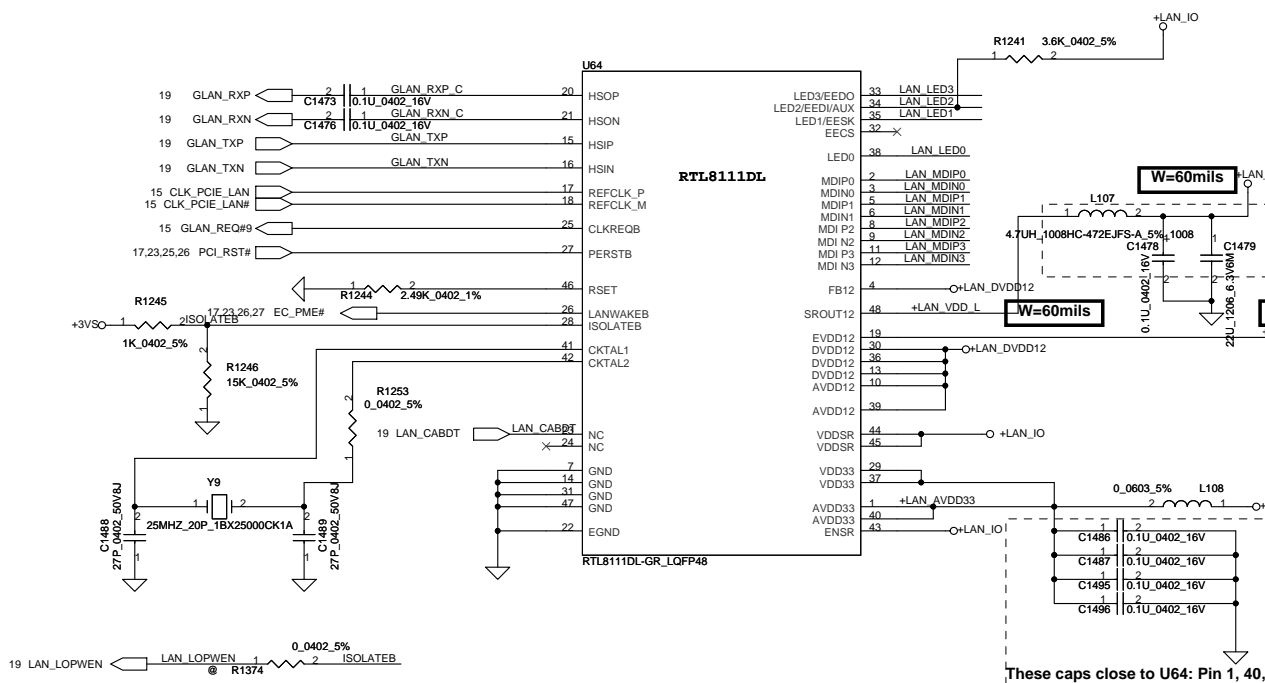
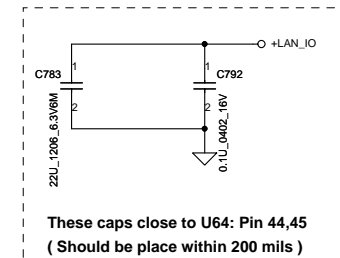
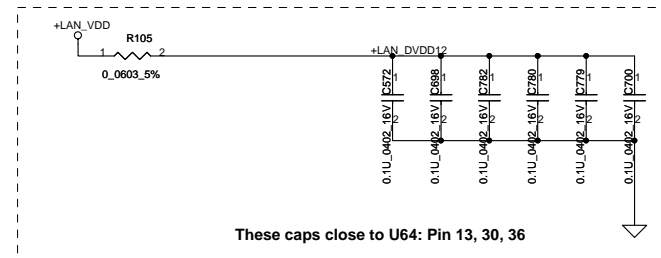
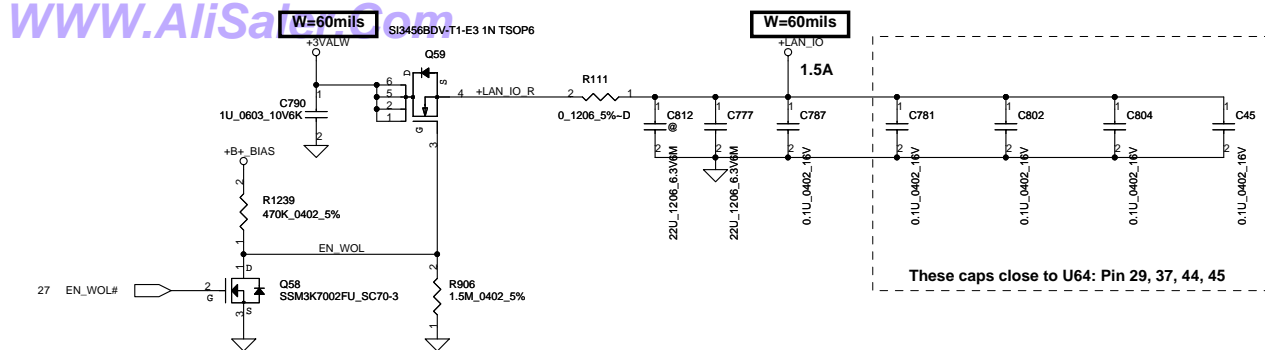
Compal Electronics, Inc.

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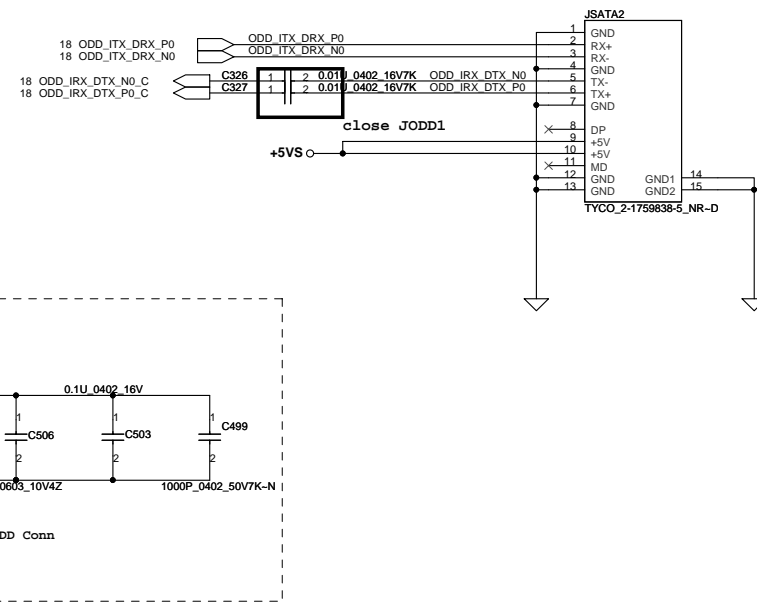


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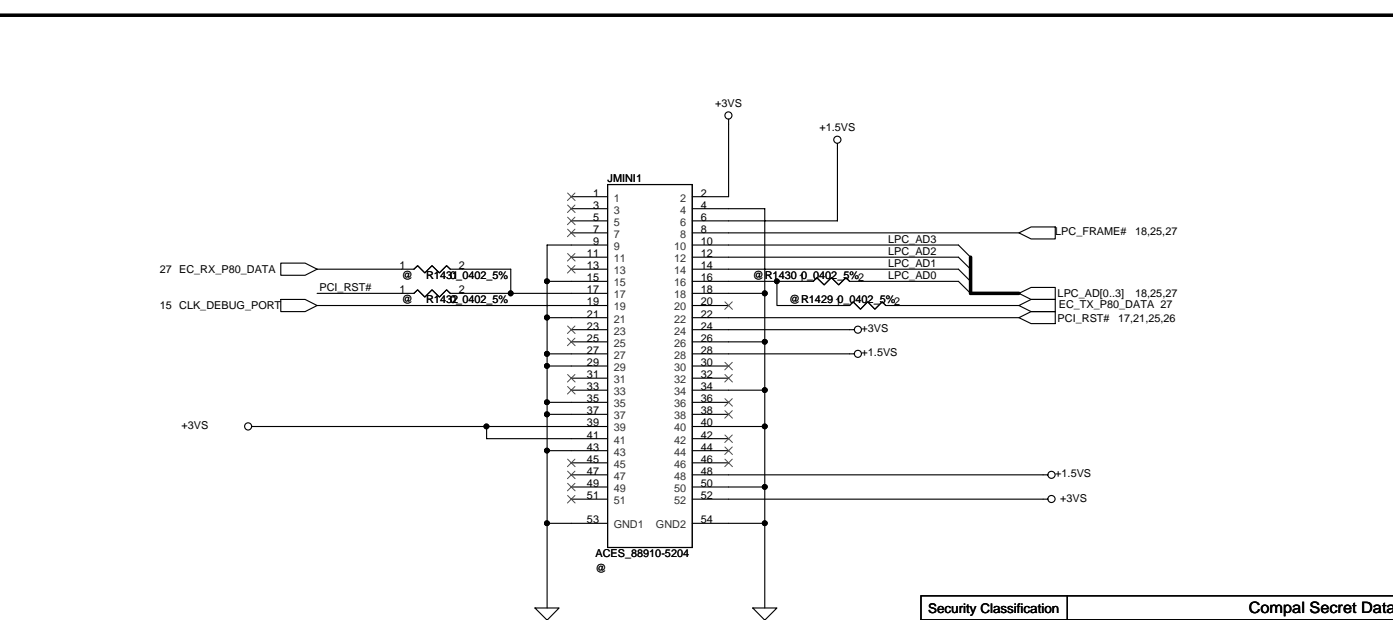
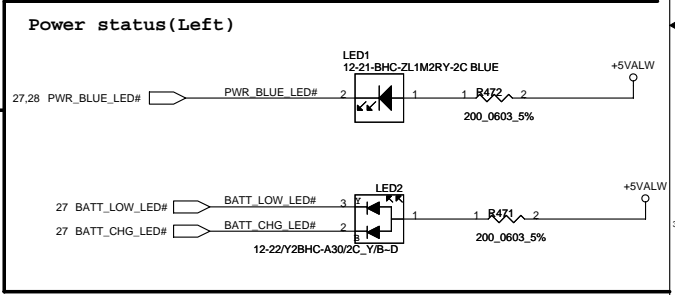
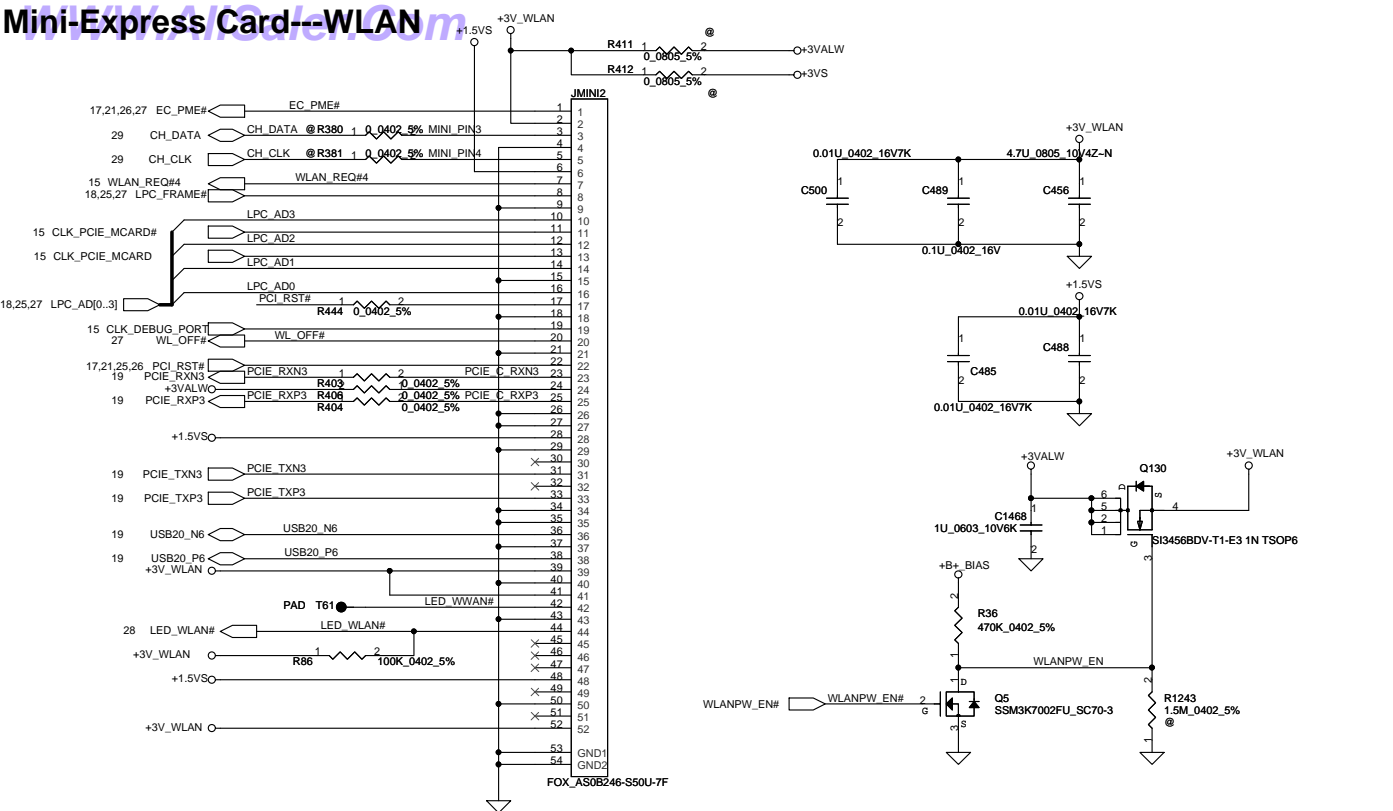
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Rev				C				401593			
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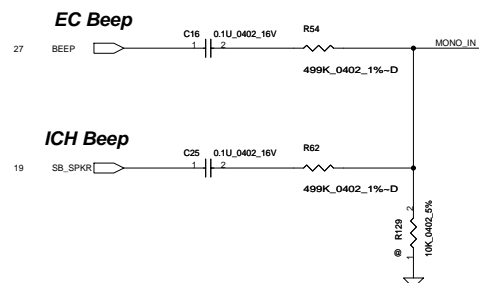
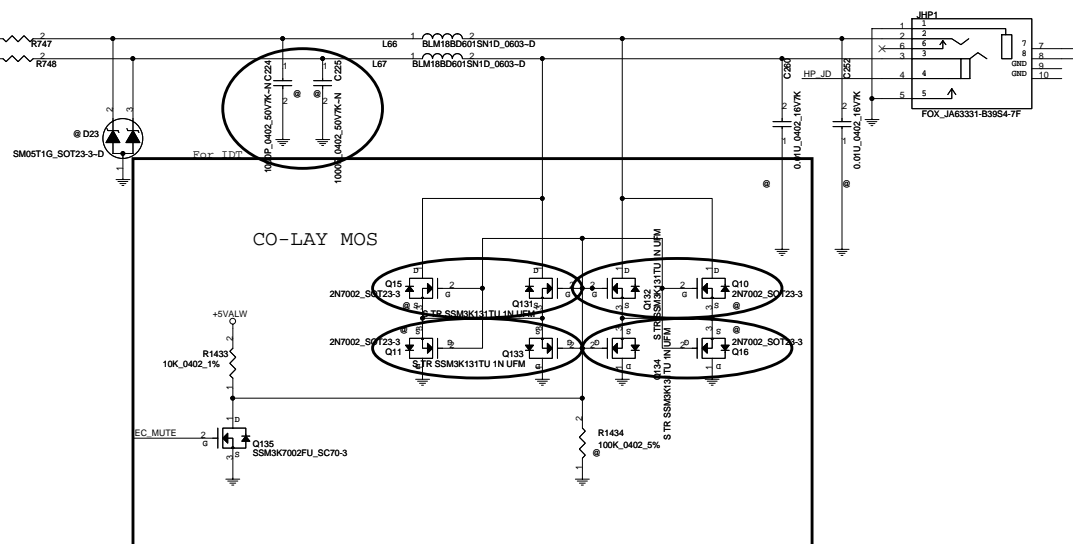
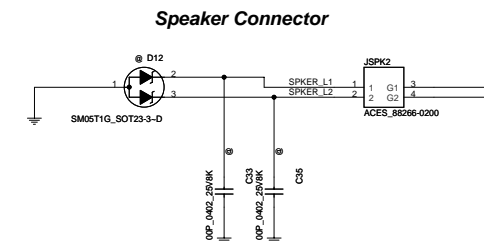
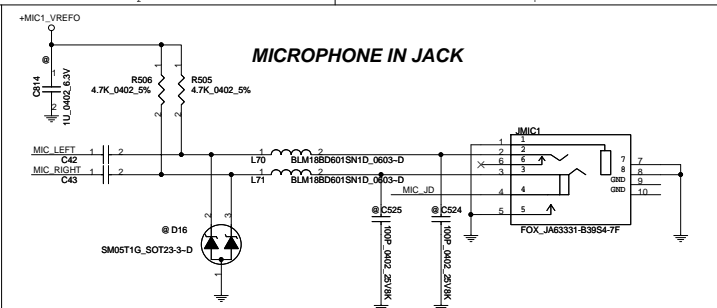
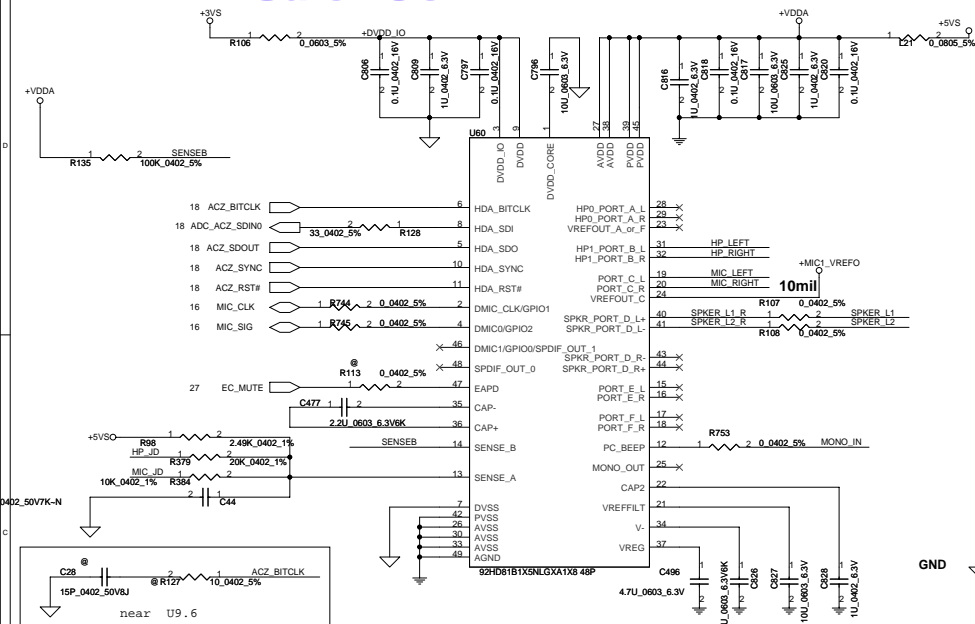


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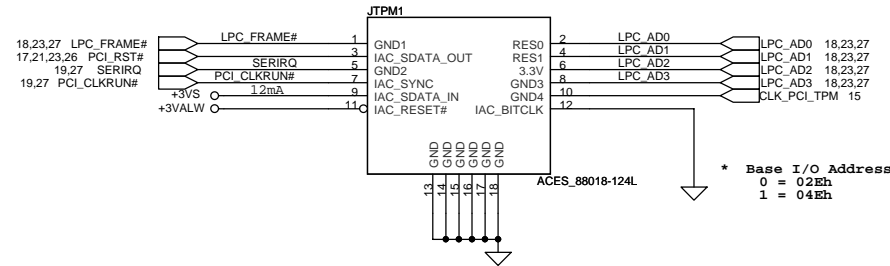


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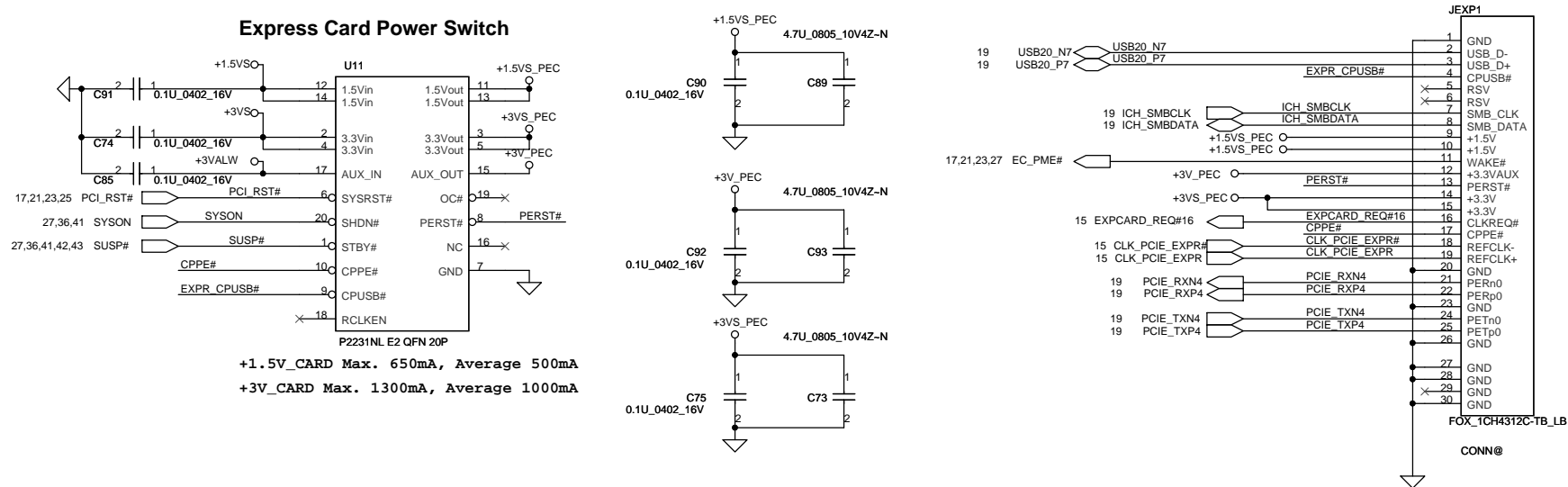


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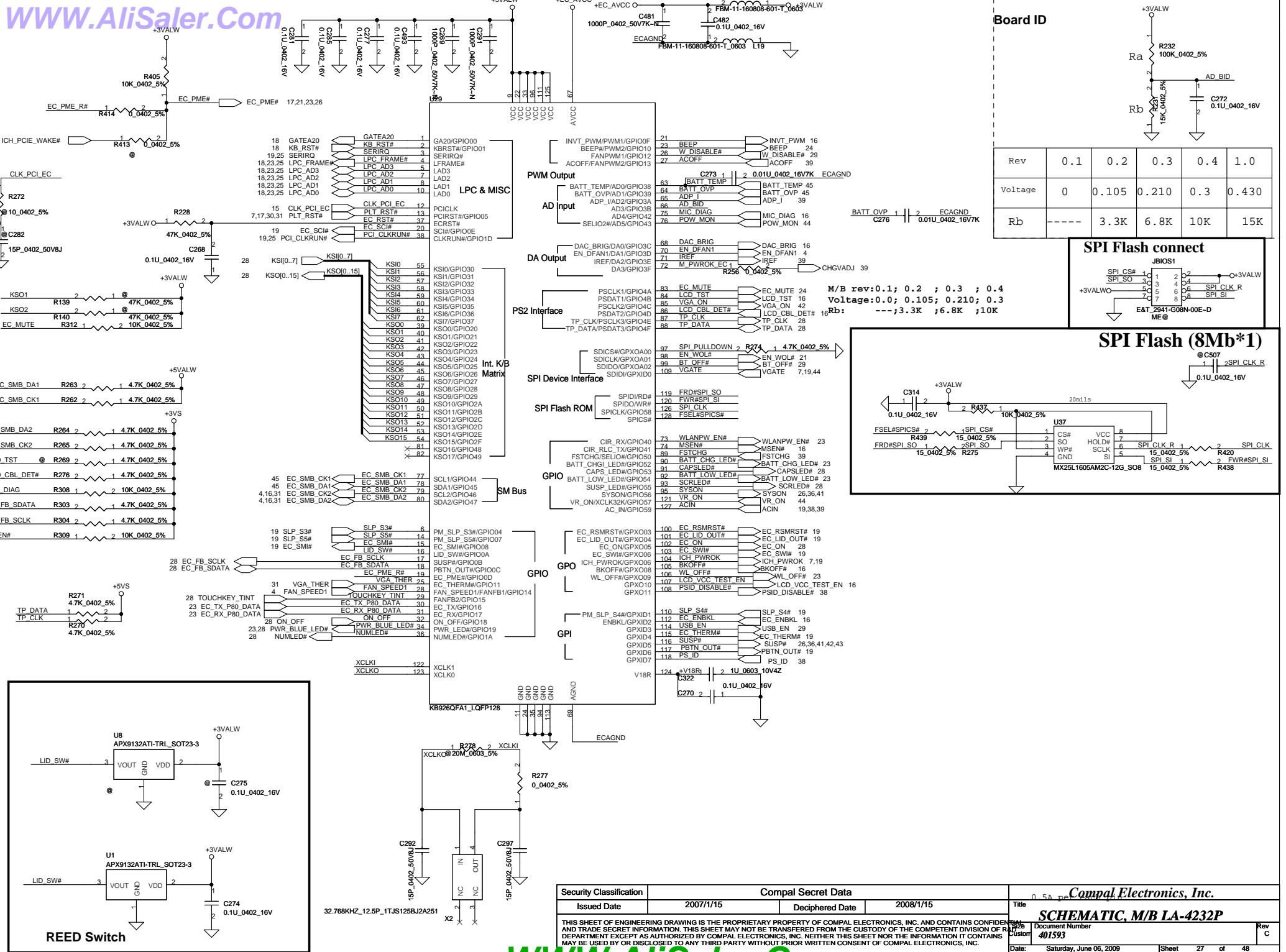
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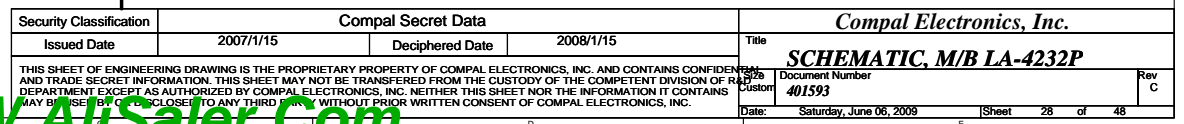
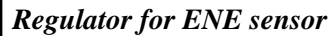


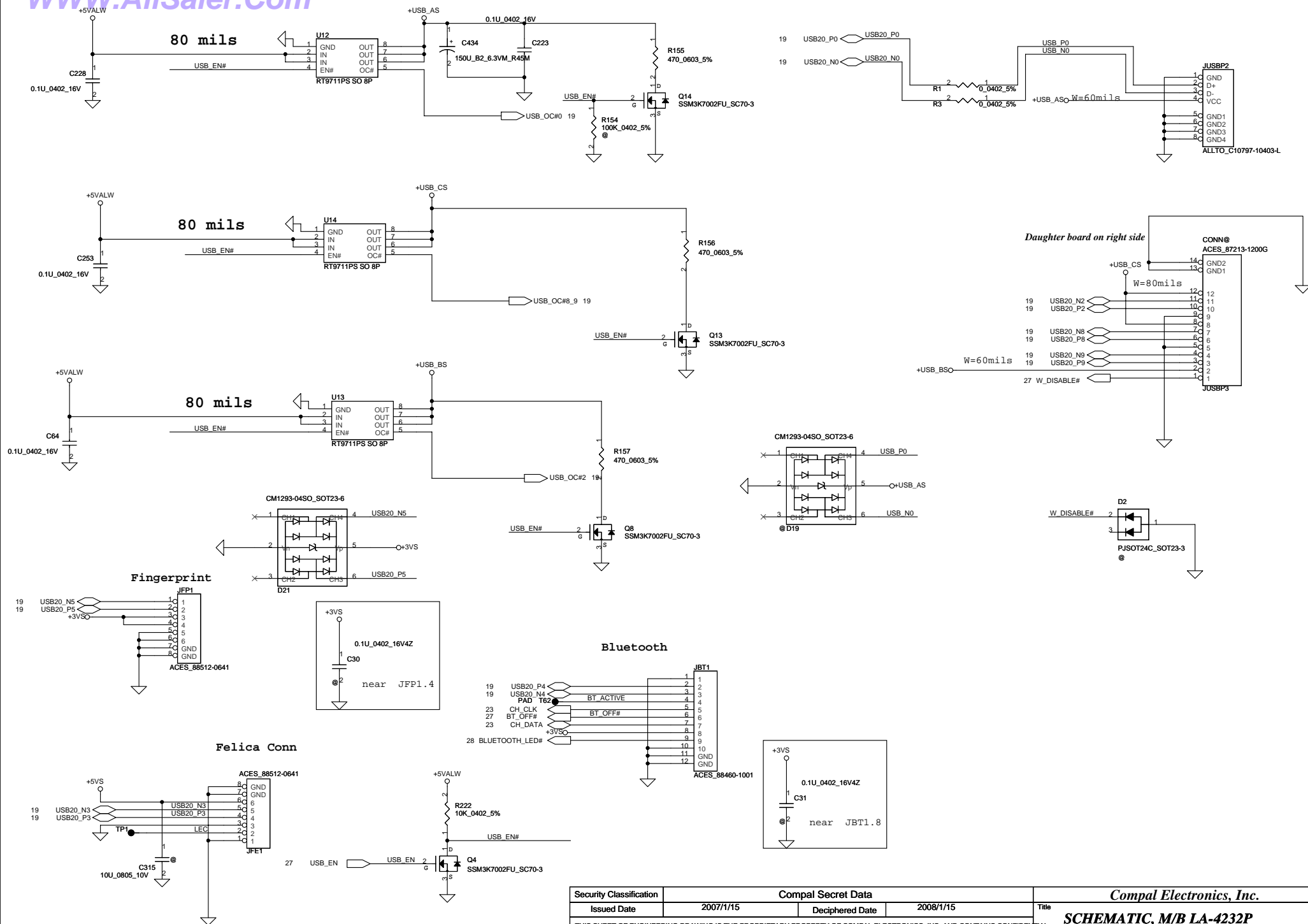
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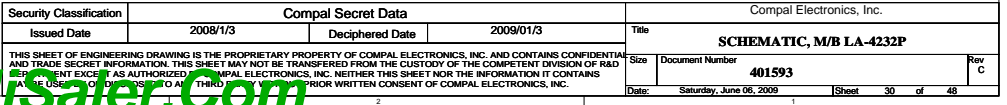
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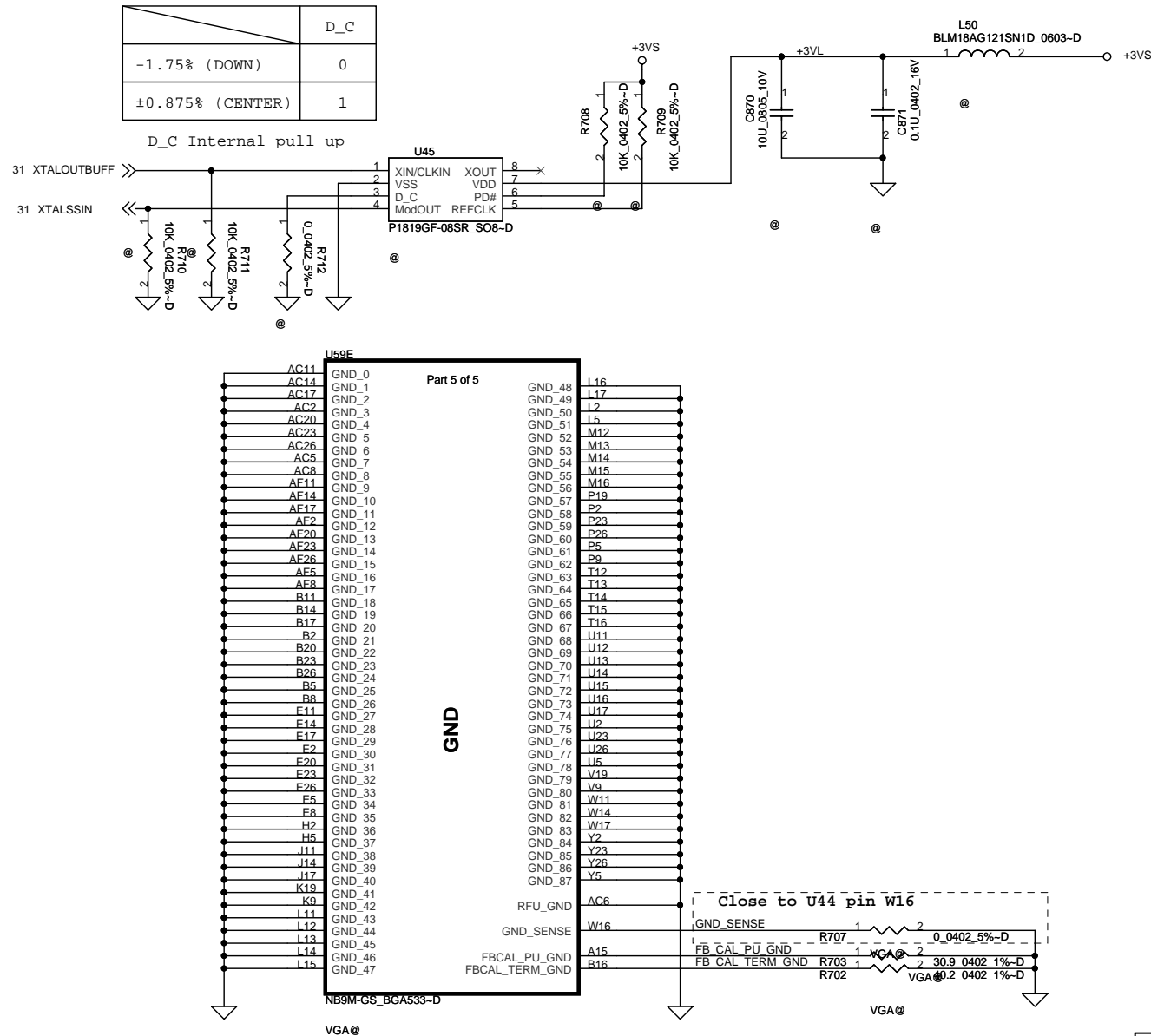
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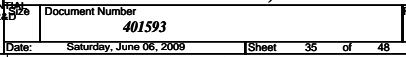
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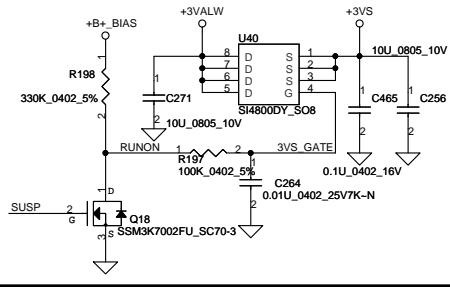
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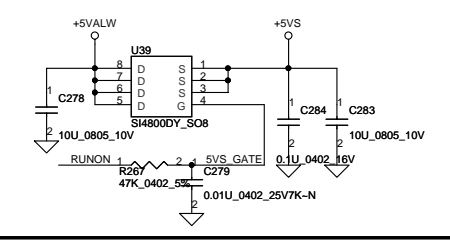
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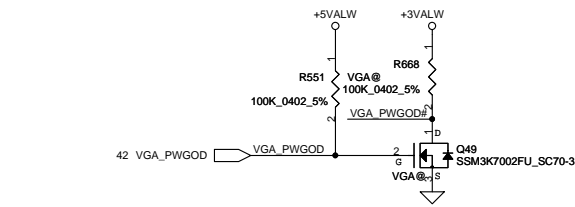
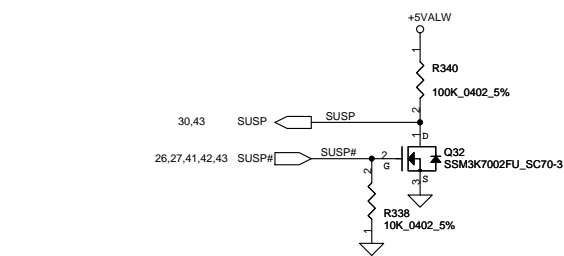
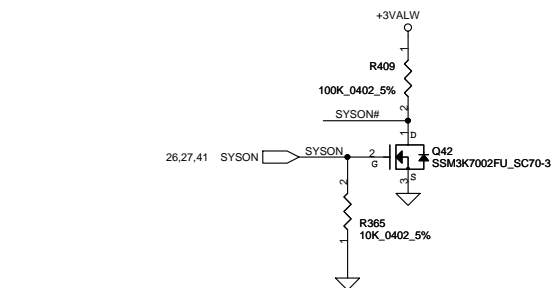
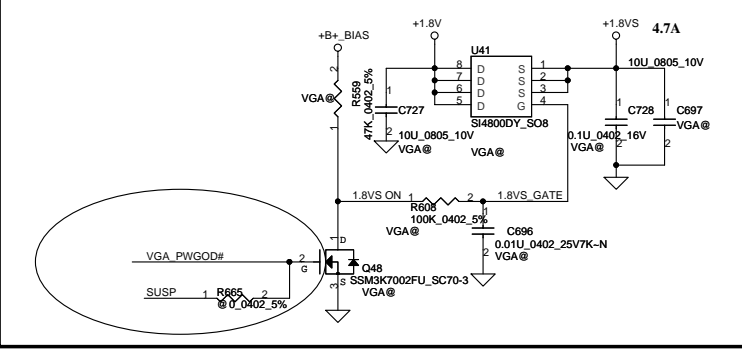
+3VALW to +3VS Transfer



+5VALW to +5VS Transfer

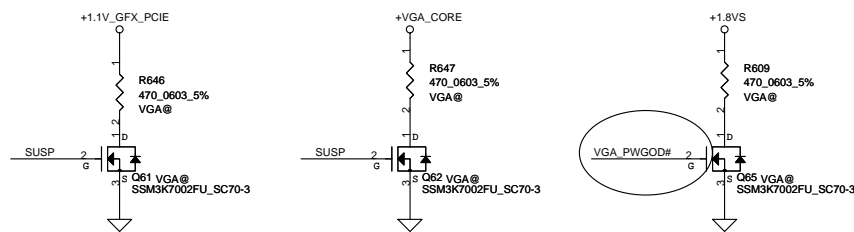


+1.8V to +1.8VS Transfer

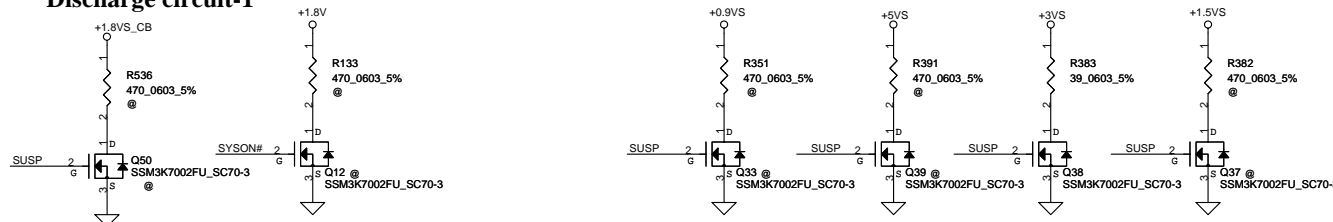


SYSON -> SUSP# -> VGA_ON->VGA_PWGOD

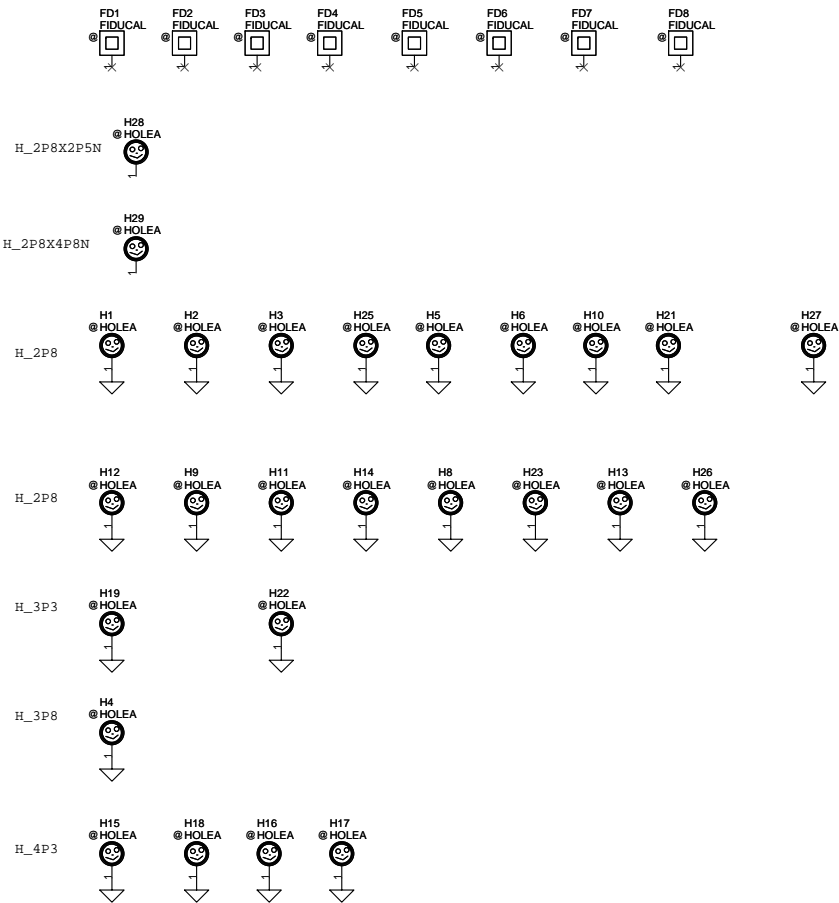
VGA Discharge circuit



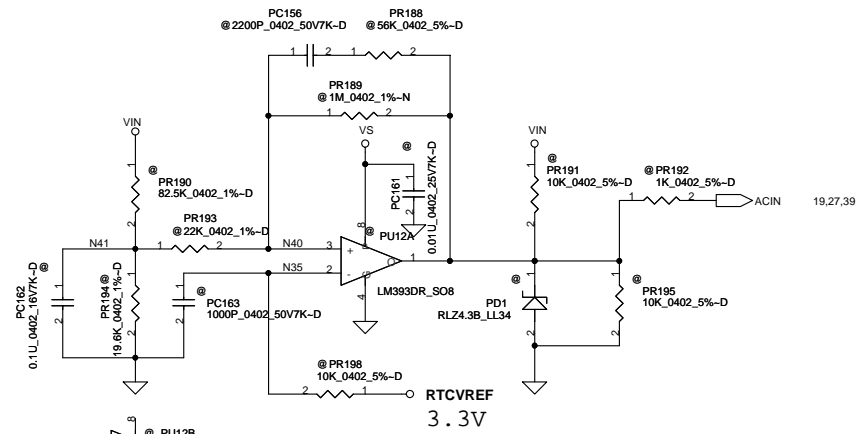
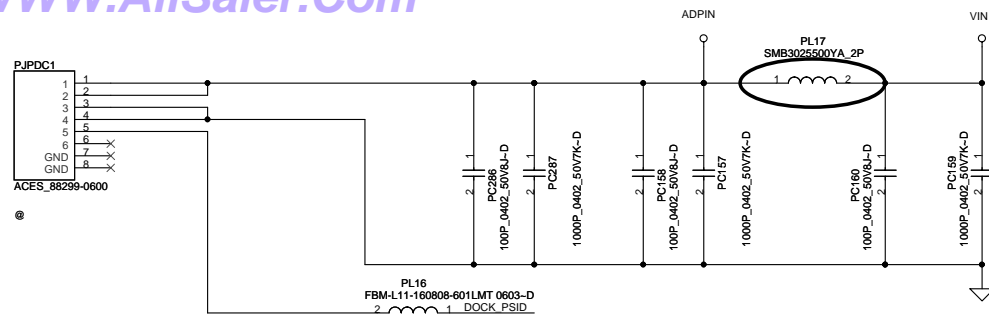
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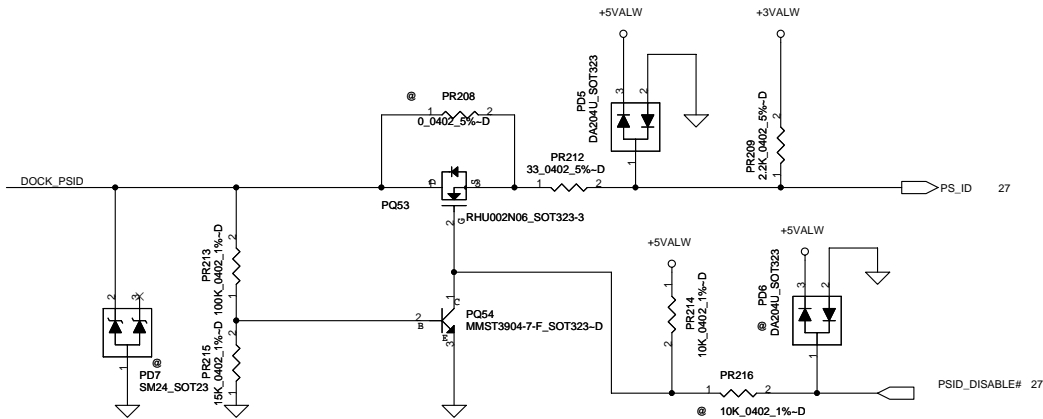
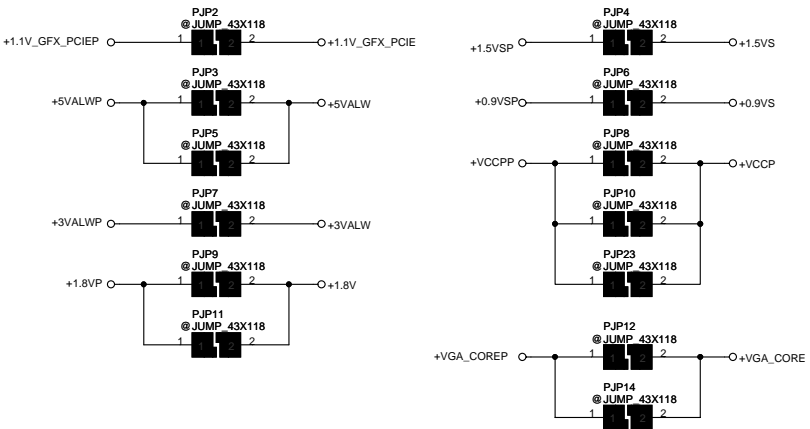
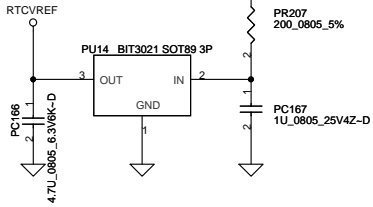
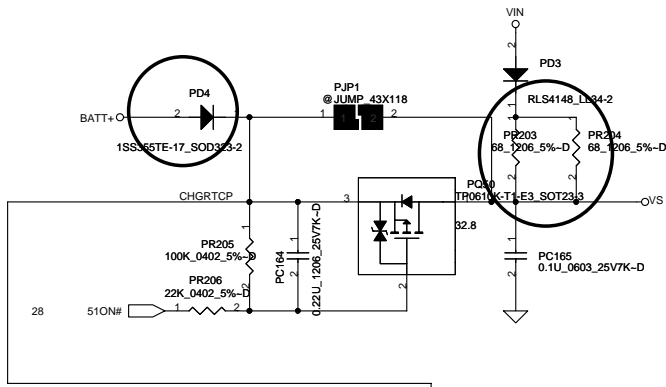
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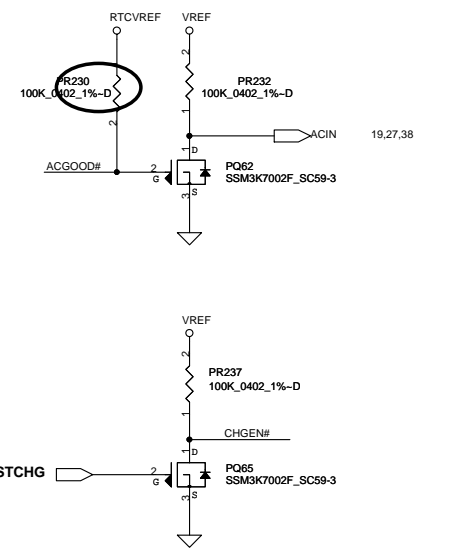
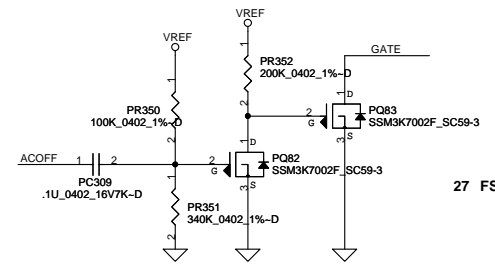
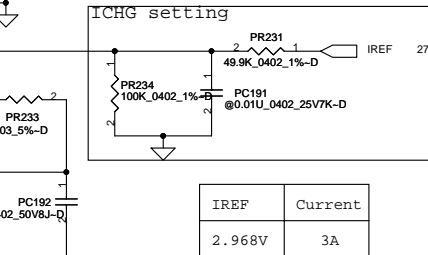
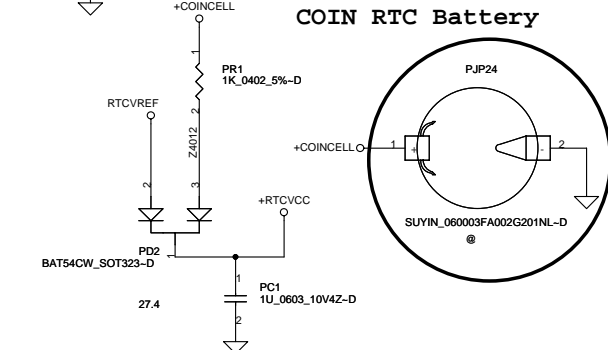
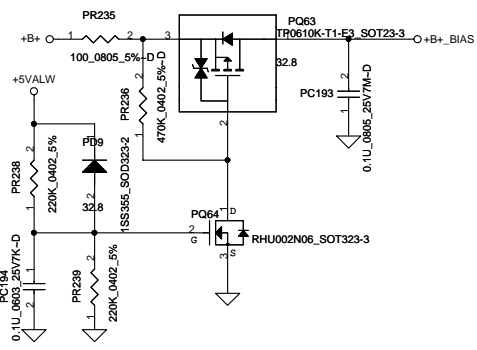
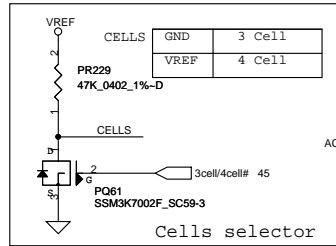


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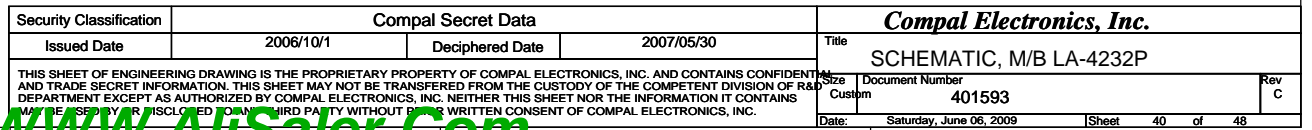


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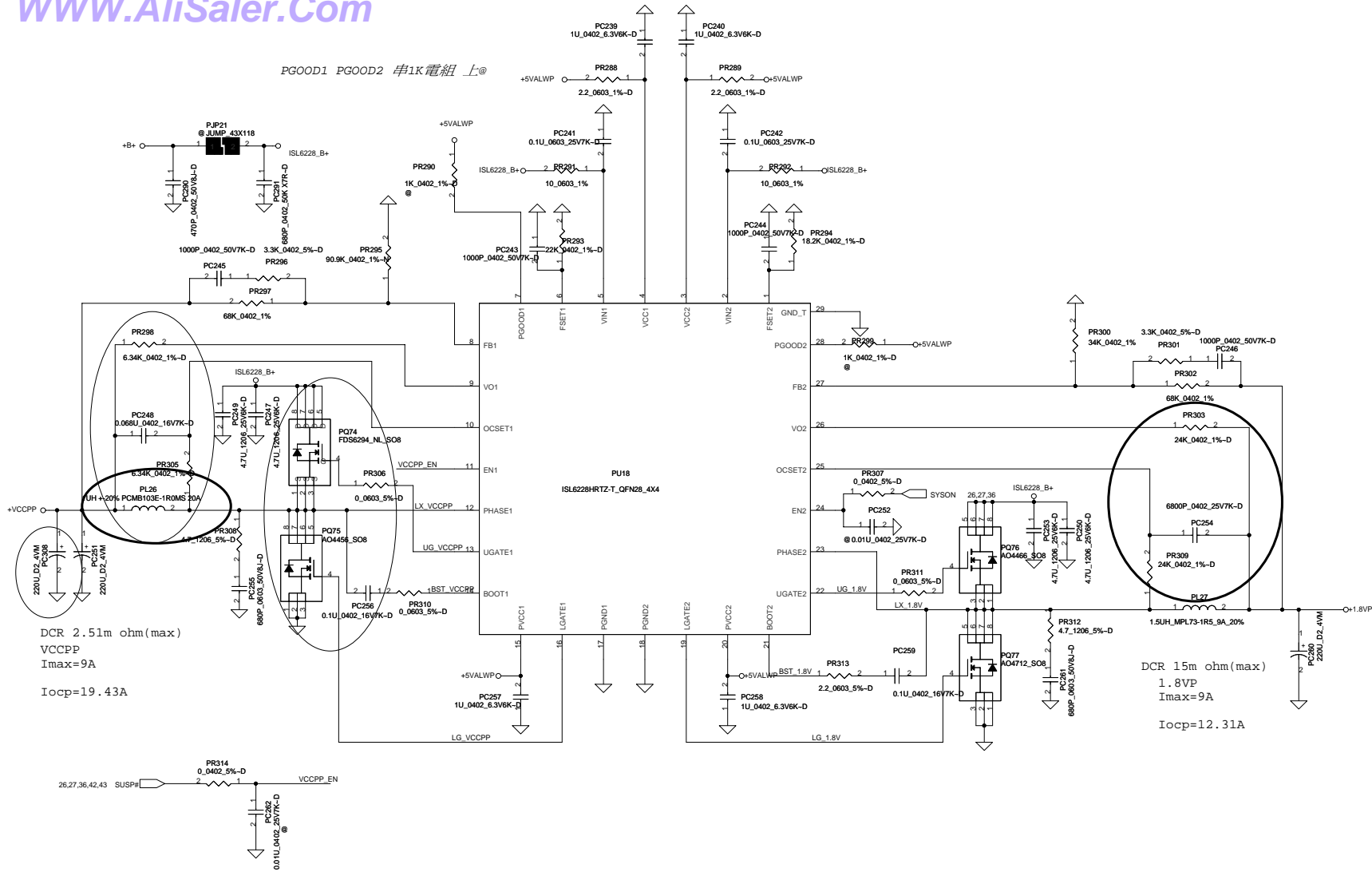
90W adapter
 $I_{charge} = (V_{srset}/V_{vdac}) * (0.1/PR222) = 3.3A$
 $I_{adapter} = (V_{vacset}/V_{vdac}) * (0.1/PR217) = 3.1A$
 Input OVP : 22.3V
 Input UVP : 16.98V
 Fsw : 300KHz



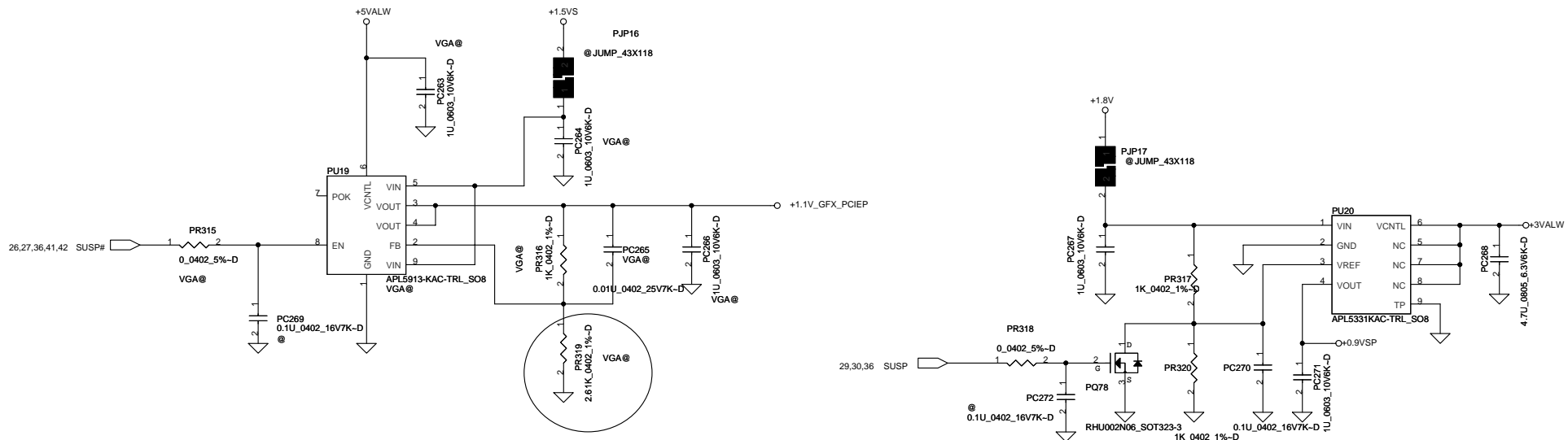
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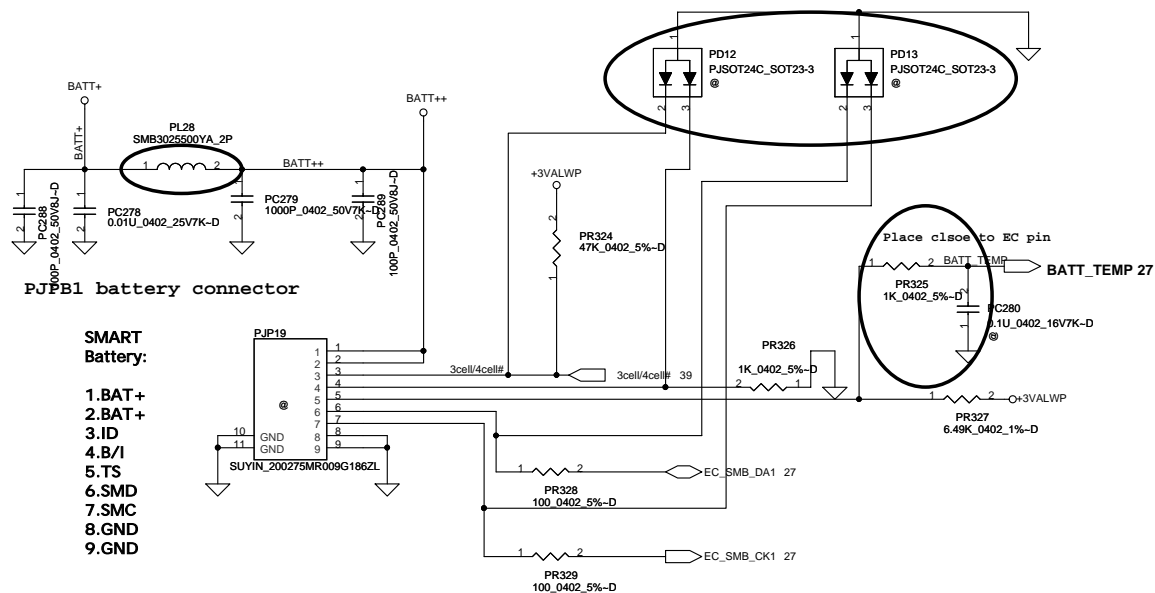
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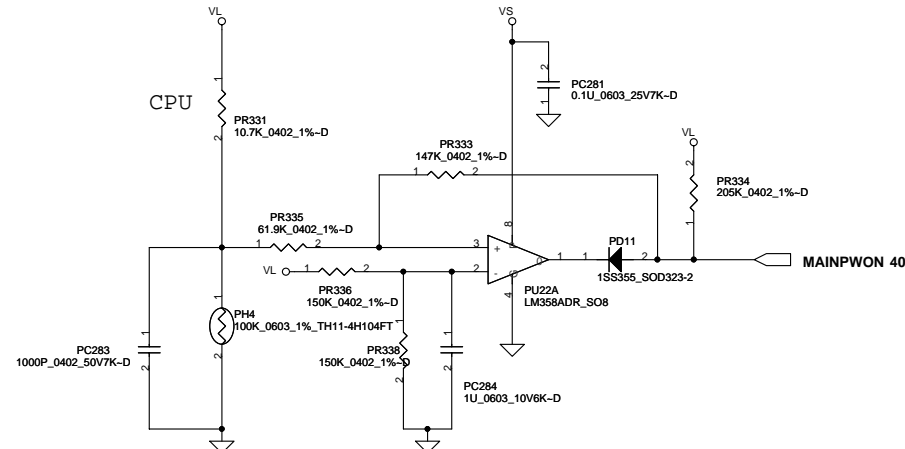
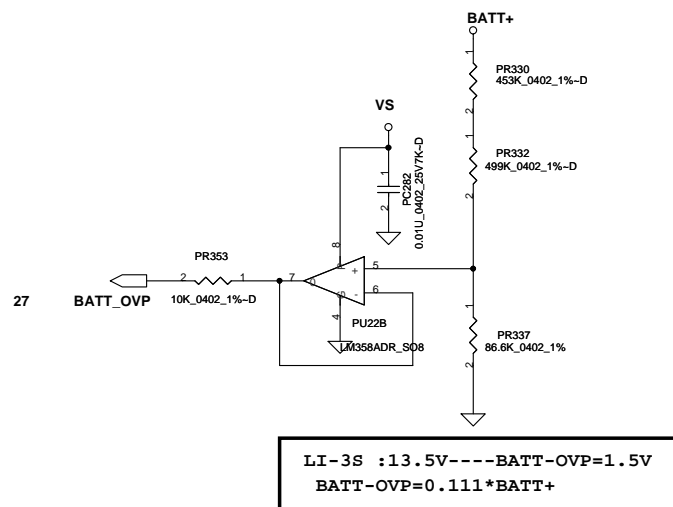


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CPU

PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 50 +-3 degree C



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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	board rev update to 0.2	R231 change to 15K & R232 pop	0.2
2	40	P40-OZ129_Card Reader/1394	07/10/30	compal	CardBus vendor change	CardBus R5C833 change to OZ129	0.2
3	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Change pull up resistance	Change EC pin17,18 pull up to 4.7Kohm	0.2
4	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	Need pull up	NET MIC_DIAG pull up R to 10Kohm 3VS	0.2
5	13,14	DDR2 SODIMM-I,II Socket	07/10/30	compal	Change Capacitance	Change C84,C189 to SGA00002680 330U	0.2
6	29	P29-EC KB926/REED SW/TPM1.2	07/10/30	compal	EC update rev	EC change to 926C	0.2
7	28	P28-Express card	07/10/30	compal	Express card can't detect	POWER IC(U11) ADD PIN10 CPUSB# PIN9 EXPR_CPUSB#S	0.2
8	32	P32-USB/ Bluetooth/ FP/ Felica	07/10/30	compal	Bluetooth can't detect	BLUETOOTH CONN USB+- change	0.2
9	42	P42-Screws	07/10/30	compal	FIDUCAL no enough	ADD FIDUCAL*4	0.2
10	41	P41-DC/DC Interface	07/10/30	compal	Need pull down	SYSON pull down 10K ohm	0.2
11	41	P41-DC/DC Interface	07/11/12	compal	USB can't detect	SUSP change to 5VALW(Q32)	0.2
12	06	P06-Merom(3/3)-GND/Bypass	07/11/12	compal	Change CPU High Freqeunce Decoupling Capacitance	C195 change to C1150-C1181	0.2
13	41	P41-DC/DC Interface	07/11/13	compal	+1.8VS Discharge error	+1.8VS Discharge circuit Q65 net change to VGA_PWGOD#	0.2
14	41	P41-DC/DC Interface	07/11/16	compal	Delete	Remove SIM card connector	0.2
15	42	P42-Screws	07/11/16	compal	Change Holea size	Change Holea size 2.5 to 2.8, change 3.5 to 3.8	0.2
16	31	P31-PWR_OK/ BTN/ KB / TouchPad	07/11/21	compal	Change Touch PAD/B connector	Touch PAD/B connector change net	0.2
17	15	P15-CRT Conn.& LCD Conn.	07/11/21	compal	Add LCD control pin	Add LCD control pin LCD_CBL_DET# & LCD_TST & LCD_VCC_TEST_EN	0.2
18	20	P20-ICH9(4/4)_POWER&GND	08/04/22	compal	+5VS & +3VS have leakage	Change VCCCL3[1] [2] & VCCLAN3_3[1] [2] power source to +LAN_IO	
19	20	P09-Cantiga(3/6)-VGA/LVDS/TV	08/04/22	compal	Can't boot to OS	Add BOM Structure @	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	1.8VP/+VCCPP	08/10/22	COMPAL	adjust +VCCP OCP set	Change PC248 from 0.033u to 0.068u	0.2
2	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	ripple voltage fail	Change PC227 from SF22001M300 to SGA20221150	0.2
3	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	convenient test	Add PR304	0.2
4	44	CPU_CORE	08/10/22	COMPAL	load line fail	Change PR187 from 2.21K to 3.24K	0.2
5	38	DCIN / Precharge	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
6	39	Charger	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
7	40	+3VALWP/+5VALWP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
8	41	1.8VP/+VCCPP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
9	42	1.5VSP/+VGA_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
10	43	+0.9VSP/+1.1V_GFX_PCIEP	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
11	44	CPU_CORE	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
12	45	BATTERY CONN	08/10/22	COMPAL	modify MLCC part number	change part number N0 to 8L	0.2
13	40	+3VALWP/+5VALWP	08/10/24	COMPAL	boost choke current rating	change PL20 PL21 from SH000006380 to SH00000AY00	0.2
14	45	BATTERY CONN	08/10/30	COMPAL	delete diode for EMD request	del PD14 PD15	0.2
15	45	BATTERY CONN	08/10/30	COMPAL	change diode for EMD request	change PD12 PD13 from SC1A204U00L to SCA00000E00	0.2
16	39	Charger	08/10/31	COMPAL	design modify	add PR372 PR373	0.2
17	41	1.8VP/+VCCPP	08/11/03	COMPAL	dynamic fail	change PC233 from SGA20221150 to SGA00001U80	0.2
18	44	CPU_CORE	08/12/08	COMPAL	cost down	change PU11 from SA00001HU80 to SA000031W00 and interrelated components	0.3
19	38	DCIN / Precharge	08/12/08	COMPAL	common circuit design modify	change PR203 from 33 to 68 and add PR204 to 68	0.3
20	39	Charger	08/12/08	COMPAL	vendor FAE suggest	change PR272 PR339 from 1 to 3.3	0.3
21	38	DCIN / Precharge	08/12/08	COMPAL	design modify	change PL17 from SM010018880 to SM010008E10	0.3
22	45	BATTERY CONN	08/12/08	COMPAL	design modify	change PL28 from SM010018210 to SM010008E10	0.3
23	39	Charger	08/12/15	COMPAL	change component for EMD request	change PJP15 to PL19 SM010016410	0.3
24	39	Charger	08/12/15	COMPAL	add capacitor for EMD request	add PC274 0.1u	0.3
25	42	1.5VSP/+VGA_CORE	09/01/19	COMPAL	adjust VGA_CORE OCP set	change PQ72 from SB00000CG00 to SB562940080	0.4
26						change PQ73 from SB00000AJ00 to SB000003W00	0.4
27						change PL24 from SH000008700 to SH000005400	0.4
28						change PR276 PR282 from 24K to 19.6K	0.4
29						change PC230 from 0.022u to 6800p	0.4
30					consumption adjust	change PR269 from 3.3K to 2.2K	0.4
31	44	CPU_CORE	09/01/19	COMPAL	vendor FAE suggest	add PC141 330p	0.4
32	45	BATTERY CONN	09/02/18	COMPAL	delete diode for ESD request	del PD12 PD13	0.4

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