MYALL Block Diagram (Ref. rename from 12/6)

Project Code: 91.4G501.001

PCB: 05244-Rev.

CLK GEN.
IDT CV125
3

Mobile CPU
Dothan
4, 5

G792
19

HOST BUS 400MHz

DDR II
400 MHz
11,12
400MHz

DDR II
400 MHz
11,12
400MHz

Intel 910GM (UMA)
Intel 915PM (DIS)
6,7,8,9,10

RGB → CRT 14

LVDS → LCD 13

Nvidia
G72M-V
24,25

VRAMx4
24,25

DMI I/F 100MHz

Line In 27
Mic In 27
Int. MIC In 27
Line Out 27
Codec
ALC861
26
Azalia

INT.SPKR 27
OP AMP
G1421B 27

MODEM
MDC Card
21

ICH6-M
15,16,17,18

PCI BUS

ENE
CB1410
24,25

PWR SW
CP2211
25

PCMCIA
ONE SLOT
25

Mini-PCI
802.11A/B/G 28

LAN
10/100
RTL8110CL
22, 23

TXFM
23

RJ45 23

PCIE X1

PCI MINI CARD
25

LPC BUS

SATA

PATA

USB

Golden Finger
30

KBC
ENE KB3910
29

Xbus

BIOS ROM
512 K
PM39LV040-70JCE
31

SATA
24,25

HDD
20

CDROM
20

USB
5 PORT
21

SATA
24,25

MINI USB 21
BlueTooth

Touch Pad 30

INT_KB
30

(co-lay)

LED BDx1
(another circuit)

CPU DC/DC ISL6218CV-T 34	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC TPS51120 35	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5912-LAC APL5308-25AC 36	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	1D5V_S0 2D5V_S0

SYSTEM DC/DC ISL6227 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DGQ 37	
5V_S5	DDR_VREF DDR_VREF_S3

CHARGER ISL6255 38	
INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

<Core Design>

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 1 of 52

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

<Core Design>

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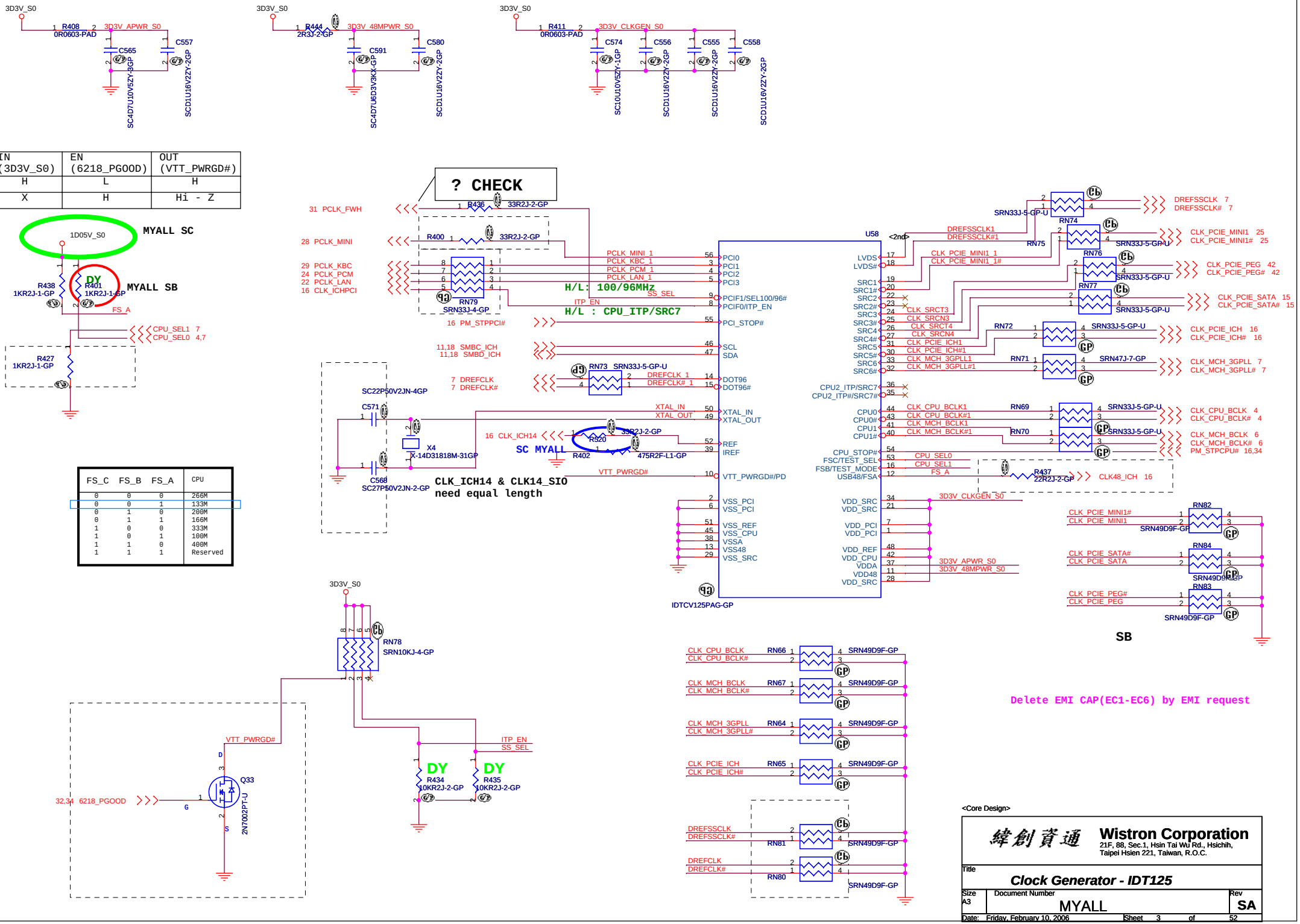
Title: Memo

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 2 of 52


3D3V_S0
R408 0R0603-PAD
3D3V_APWR_S0
C565
C557
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
R444 2R3J-2-GP
3D3V_48MPWR_S0
C591
C580
SC4D7U6D3V3KX-GP
R411 0R0603-PAD
3D3V_CLKGEN_S0
C574
C556
C555
C558
SC10U10V5ZY-1GP
IN (3D3V_S0) | EN (6218_PGOOD) | OUT (VTT_PWRGD#)
H | L | H
X | H | Hi - Z
1D05V_S0
MYALL SC
R438 1KR2J-1-GP
DY
R401 1KR2J-1-GP
MYALL SB
FS_A
CPU_SEL1 7
CPU_SEL0 4,7
R427 1KR2J-1-GP
? CHECK
R436 33R2J-2-GP
31 PCLK_FWH
R400 33R2J-2-GP
28 PCLK_MINI
29 PCLK_KBC
24 PCLK_PCM
22 PCLK_LAN
16 CLK_ICHPCI
RN79 SRN33J-4-GP
PCLK_MINI_1
PCLK_KBC_1
PCLK_PCM_1
PCLK_LAN_1
H/L: 100/96MHz
SS_SEL
ITP_EN
H/L : CPU_ITP/SRC7
16 PM_STPPCI#
11,18 SMBC_ICH
11,18 SMBD_ICH
7 DREFCLK
7 DREFCLK#
RN73 SRN33J-5-GP-U
DREFCLK_1
DREFCLK#_1
SC22P50V2JN-4GP
C571
X4
X-14D31818M-31GP
C568
SC27P50V2JN-2GP
16 CLK_ICH14
R520 33R2J-2-GP
SC MYALL
R402 475R2F-L1-GP
XTAL_IN
XTAL_OUT
REF
IREF
VTT_PWRGD#
CLK_ICH14 & CLK14_SIO
need equal length
PCI0
PCI1
PCI2
PCI3
PCIF1/SEL100/96#
PCIF0/ITP_EN
PCI_STOP#
SCL
SDA
DOT96
DOT96#
VSS_PCI
VSS_REF
VSS_CPU
VSSA
VSS48
VSS_SRC
IDTCV125PAG-GP
U58
<2nd>
LVDS
LVDS#
SRC1
SRC1#
SRC2
SRC2#
SRC3
SRC3#
SRC4
SRC4#
SRC5
SRC5#
SRC6
SRC6#
CPU2_ITP/SRC7
CPU2_ITP#/SRC7#
CPU0
CPU0#
CPU1
CPU1#
CPU_STOP#
FSC/TEST_SEL
FSB/TEST_MODE
USB48/FSA
VDD_SRC
VDD_PCI
VDD_REF
VDD_CPU
VDDA
VDD48
3D3V_CLKGEN_S0
3D3V_APWR_S0
3D3V_48MPWR_S0
DREFSSCLK1
DREFSSCLK#1
CLK_PCIE_MINI1_1
CLK_PCIE_MINI1_1#
CLK_SRCT3
CLK_SRCN3
CLK_SRCT4
CLK_SRCN4
CLK_PCIE_ICH1
CLK_PCIE_ICH#1
CLK_MCH_3GPLL1
CLK_MCH_3GPLL#1
CLK_CPU_BCLK1
CLK_CPU_BCLK#1
CLK_MCH_BCLK1
CLK_MCH_BCLK#1
CPU_SEL0
CPU_SEL1
FS_A
R437 22R2J-2-GP
CLK48_ICH 16
RN74
RN75
RN76
RN77
RN72
RN71
RN69
RN70
SRN33J-5-GP-U
SRN47J-7-GP
DREFSSCLK 7
DREFSSCLK# 7
CLK_PCIE_MINI1 25
CLK_PCIE_MINI1# 25
CLK_PCIE_PEG 42
CLK_PCIE_PEG# 42
CLK_PCIE_SATA 15
CLK_PCIE_SATA# 15
CLK_PCIE_ICH 16
CLK_PCIE_ICH# 16
CLK_MCH_3GPLL 7
CLK_MCH_3GPLL# 7
CLK_CPU_BCLK 4
CLK_CPU_BCLK# 4
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
PM_STPCPU# 16,34
RN82
RN84
RN83
SRN49D9F-GP
CLK_PCIE_MINI1#
CLK_PCIE_MINI1
CLK_PCIE_SATA#
CLK_PCIE_SATA
CLK_PCIE_PEG#
CLK_PCIE_PEG
SB
FS_C FS_B FS_A CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
3D3V_S0
RN78 SRN10KJ-4-GP
VTT_PWRGD#
Q33
2N7002PT-U
32,34 6218_PGOOD
R434 10KR2J-2-GP
R435 10KR2J-2-GP
ITP_EN
SS_SEL
CLK_CPU_BCLK
CLK_CPU_BCLK#
RN66
CLK_MCH_BCLK
CLK_MCH_BCLK#
RN67
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
RN64
CLK_PCIE_ICH
CLK_PCIE_ICH#
RN65
DREFSSCLK
DREFSSCLK#
RN81
DREFCLK
DREFCLK#
RN80
Delete EMI CAP(EC1-EC6) by EMI request
<Core Design>
緯創資通
Wistron Corporation
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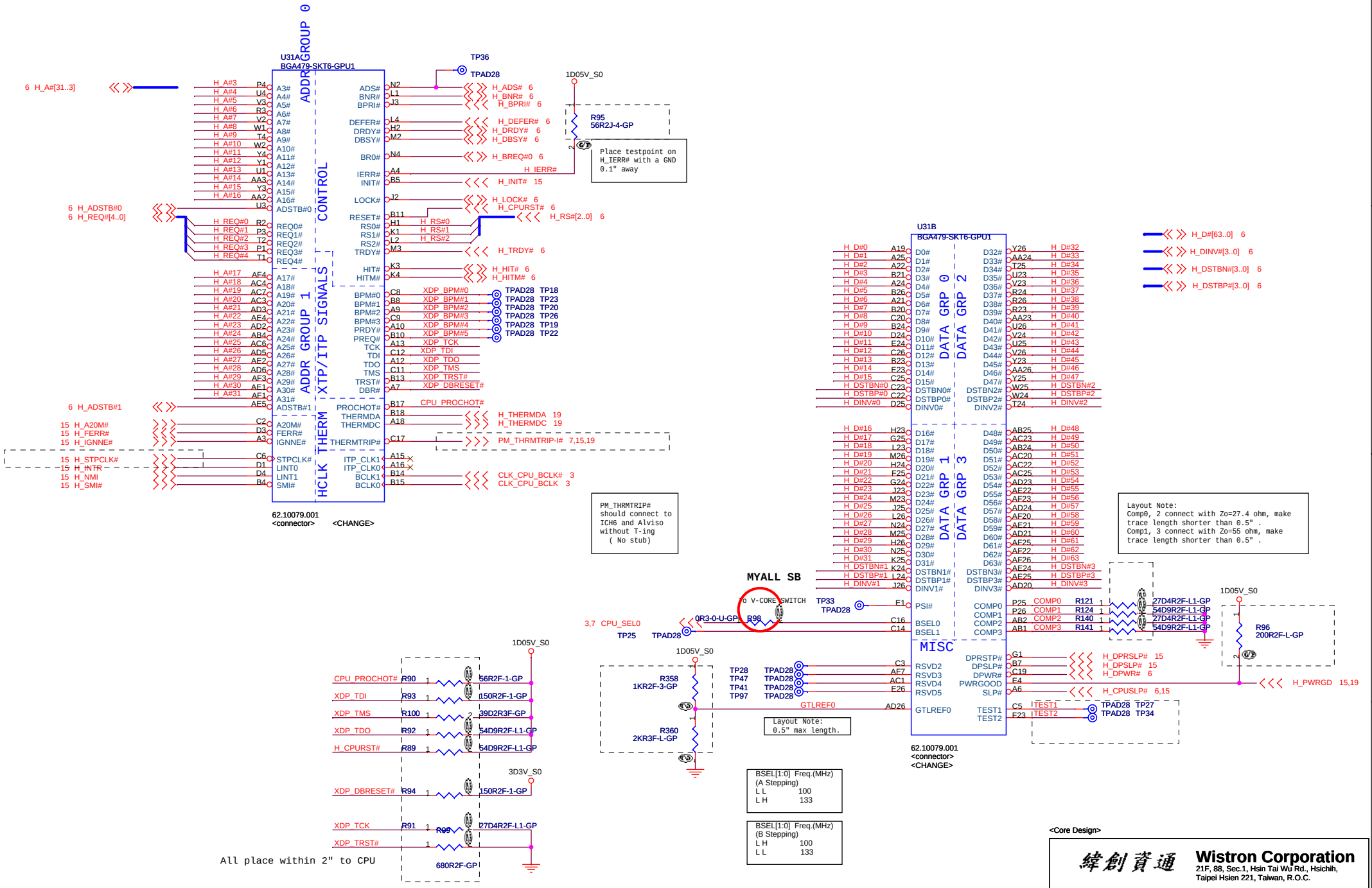
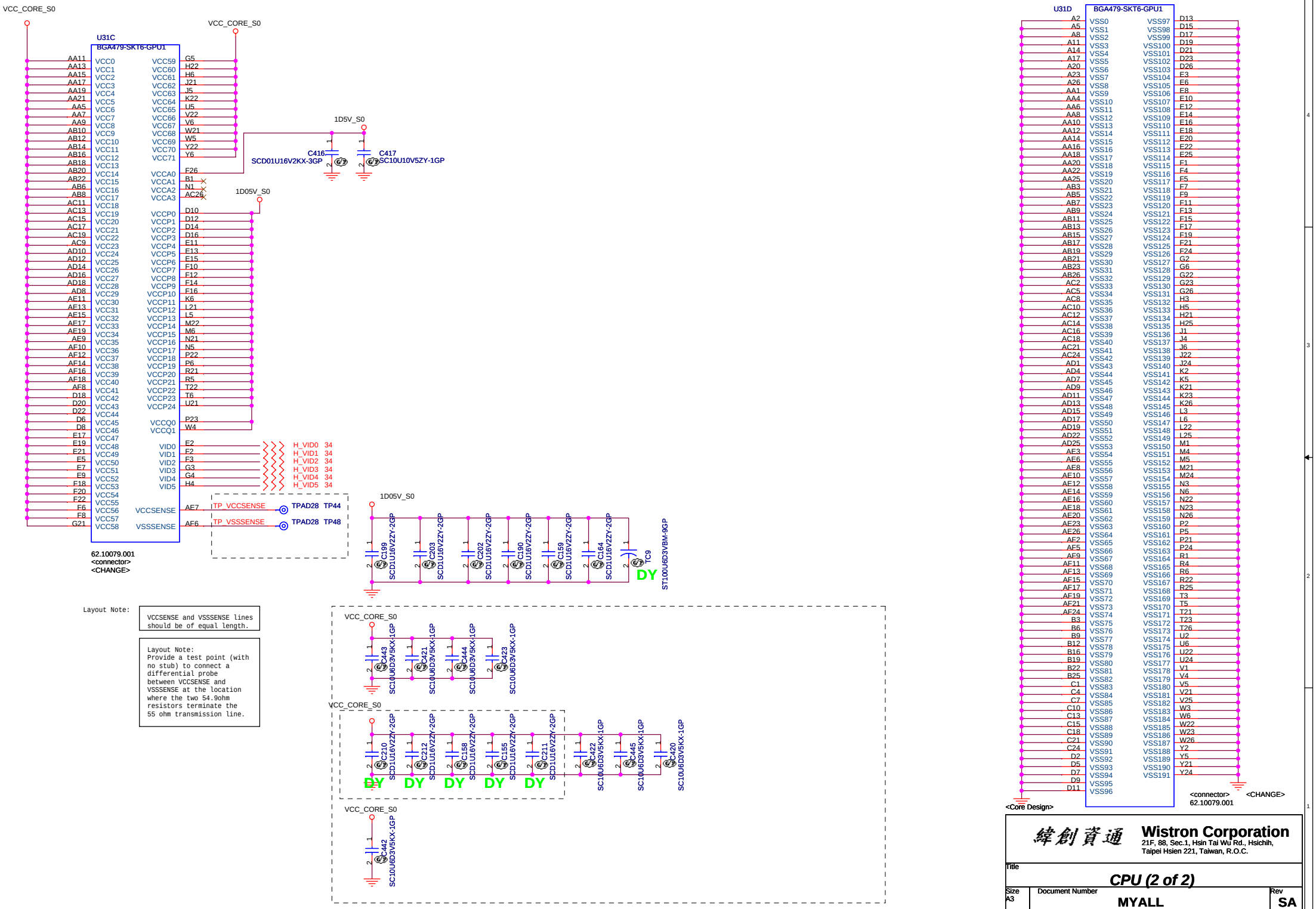
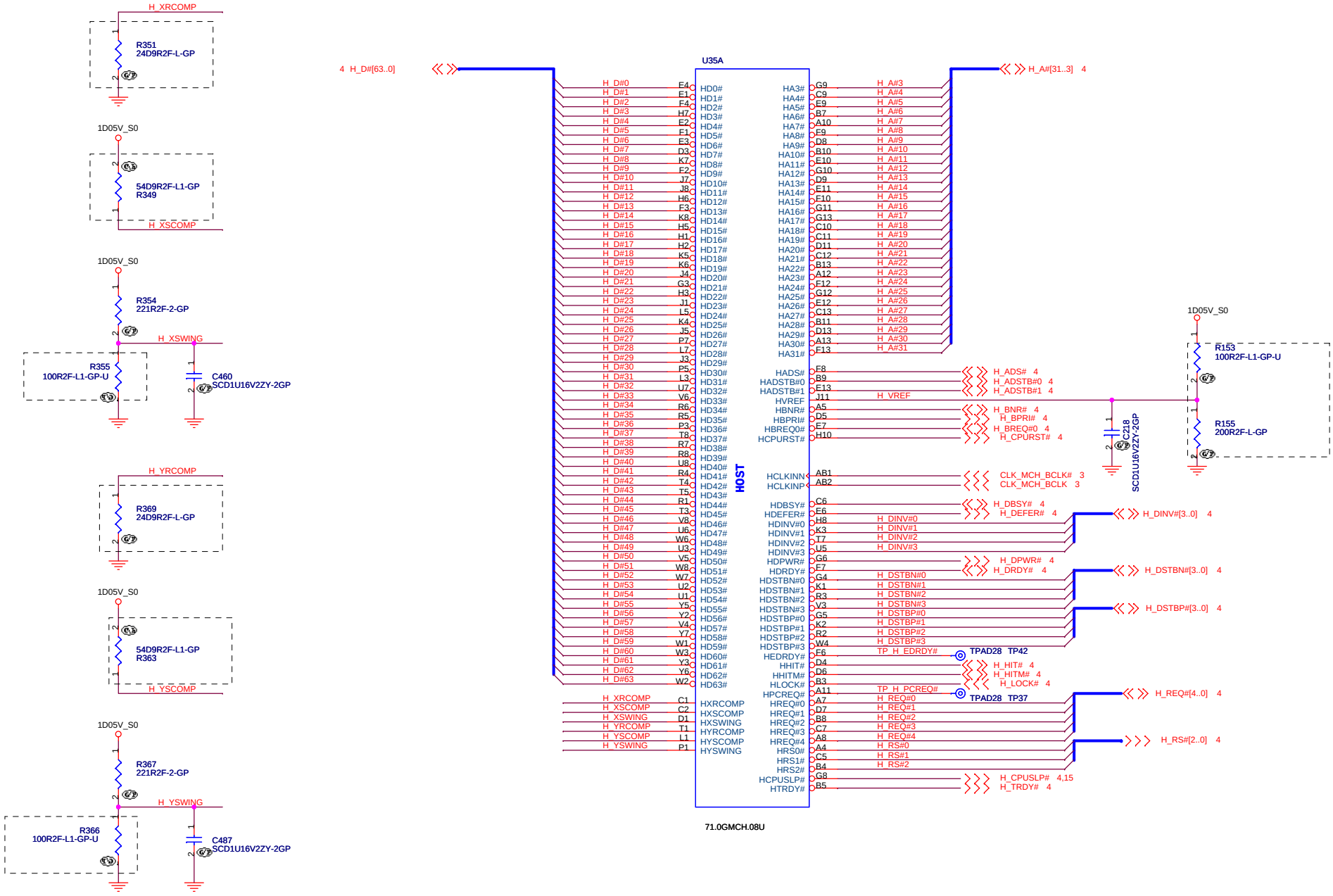
Title
Clock Generator - IDT125
Size A3
Document Number
MYALL
Rev SA
Date: Friday, February 10, 2006
Sheet 3 of 52





Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (2 of 2)	
Size: A3	Document Number: MYALL
Rev: SA	
Date: Friday, February 10, 2006	Sheet 5 of 52



Place them near to the chip

<Core Design>

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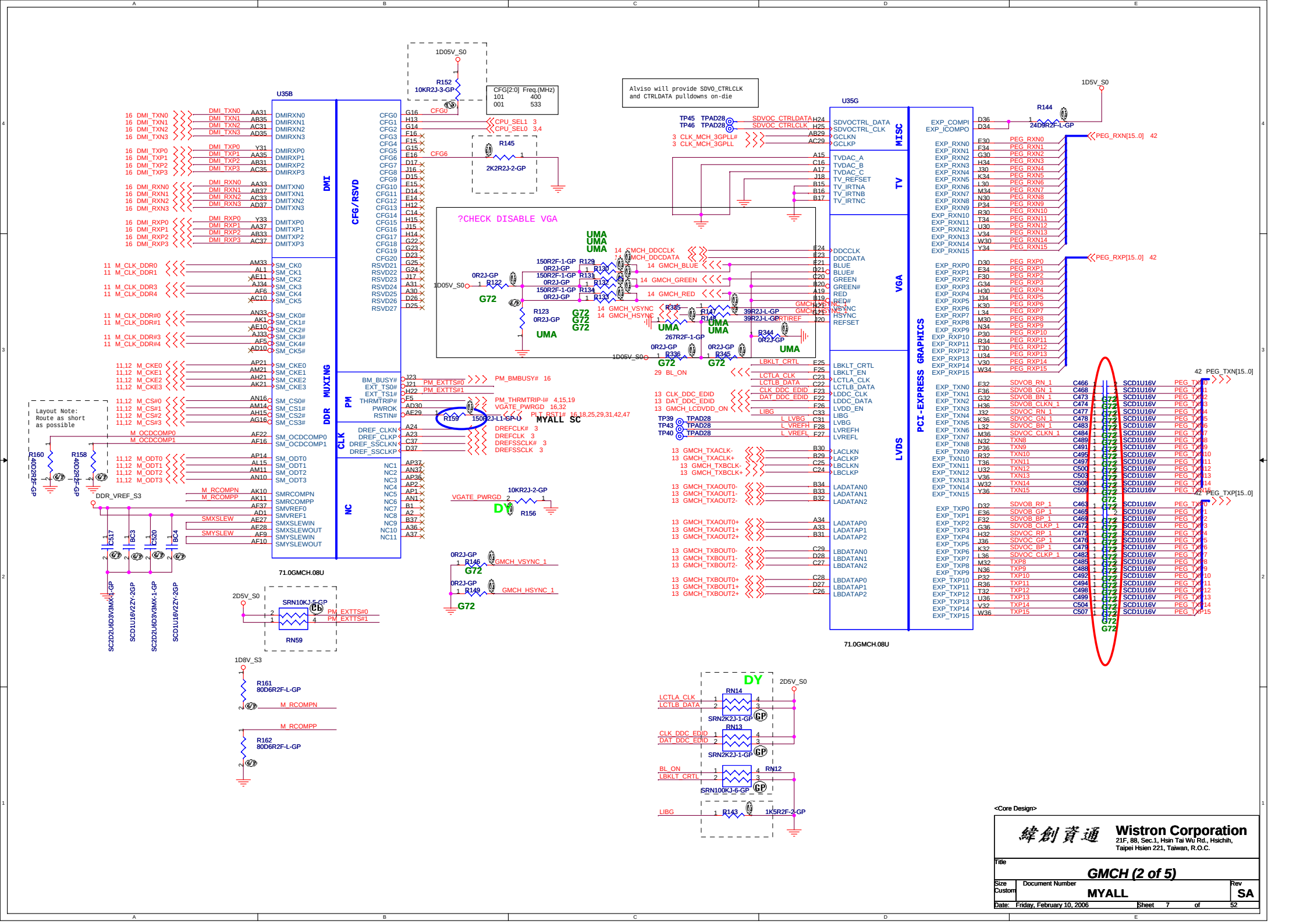
Title: GMCH (1 of 5)

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 6 of 52



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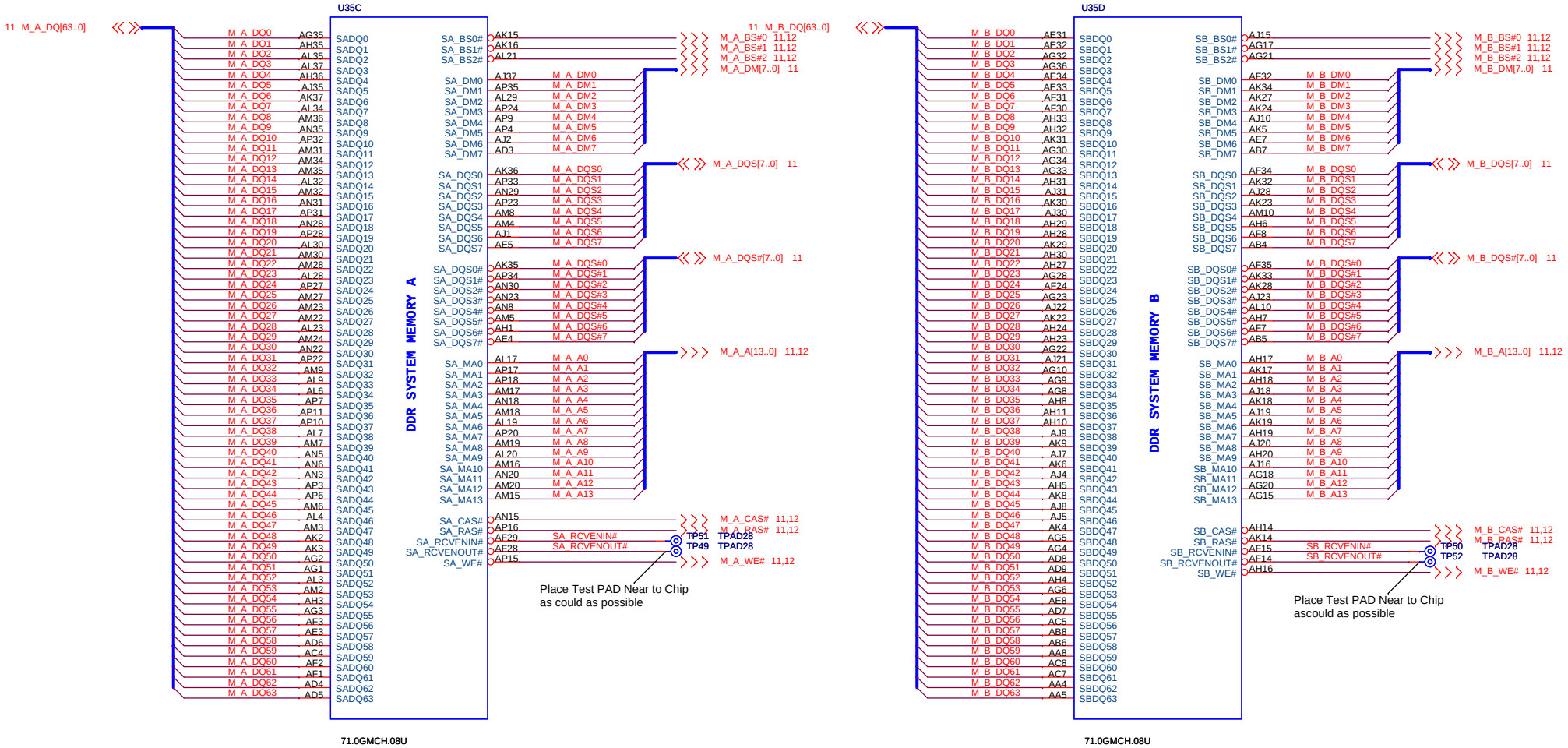
Title: GMCH (2 of 5)

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 7 of 52



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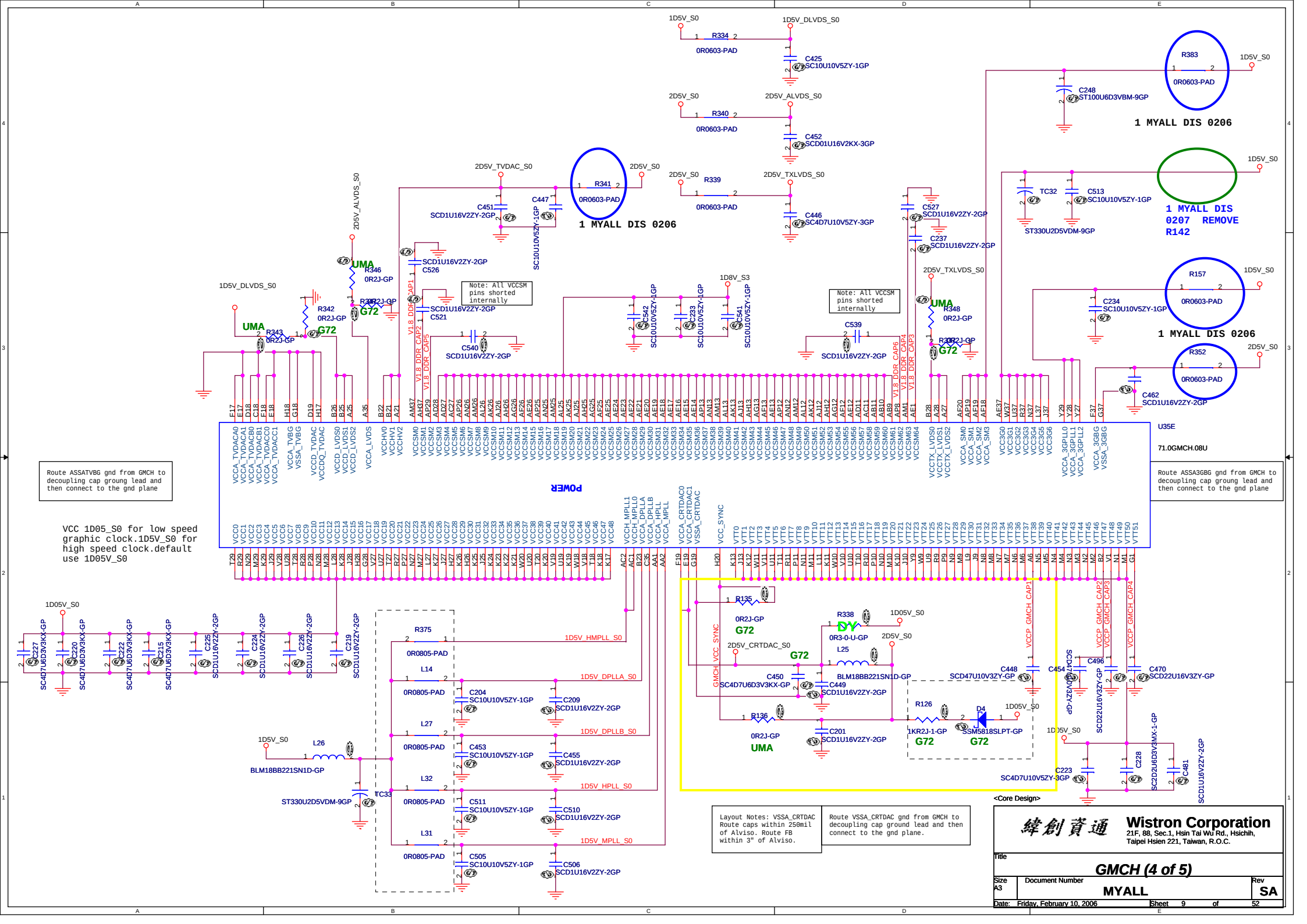
Title: GMCH (3 of 5)

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 8 of 52



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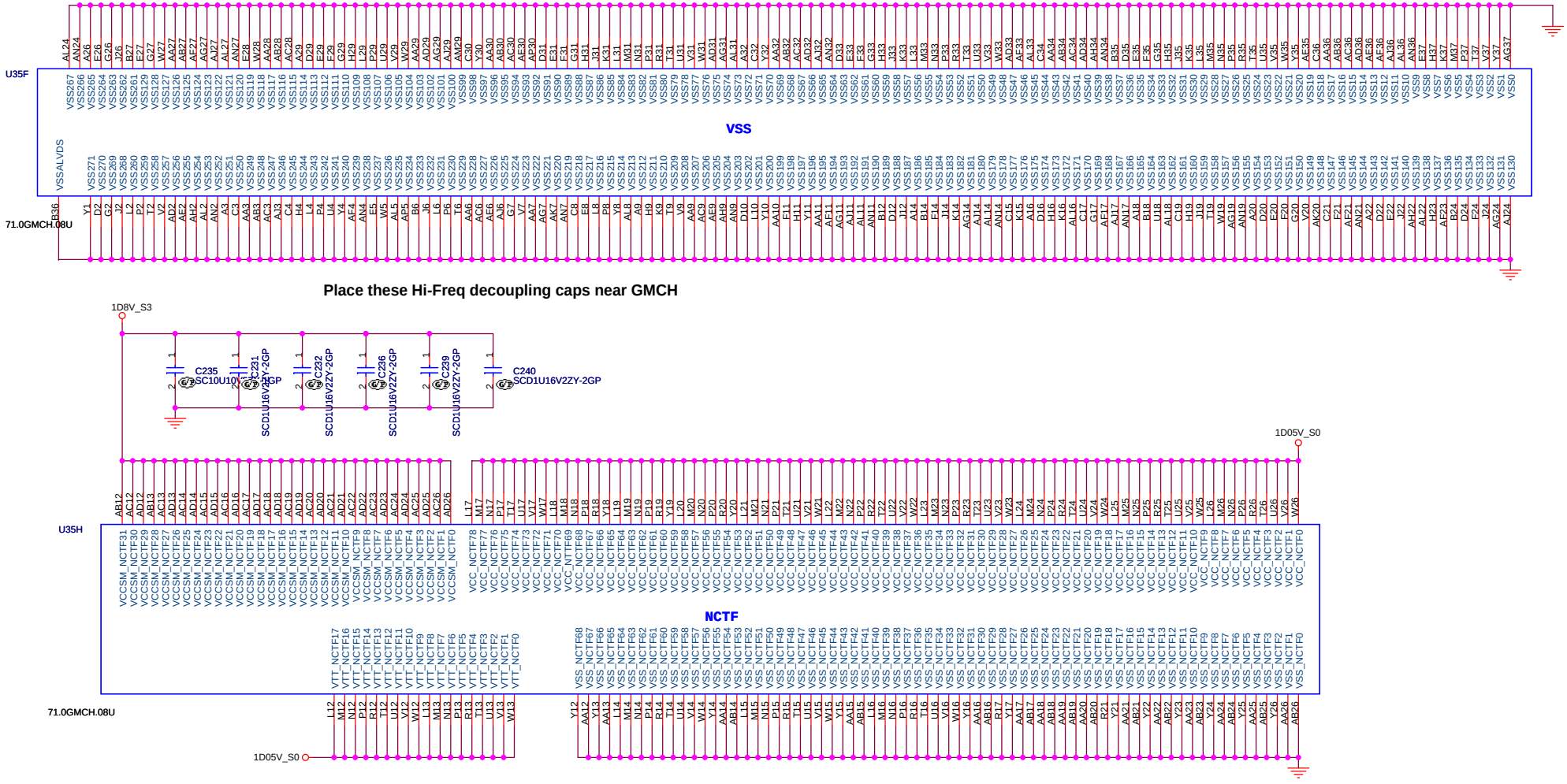
Title	GMCH (4 of 5)	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 9 of 52	



<Core Design>

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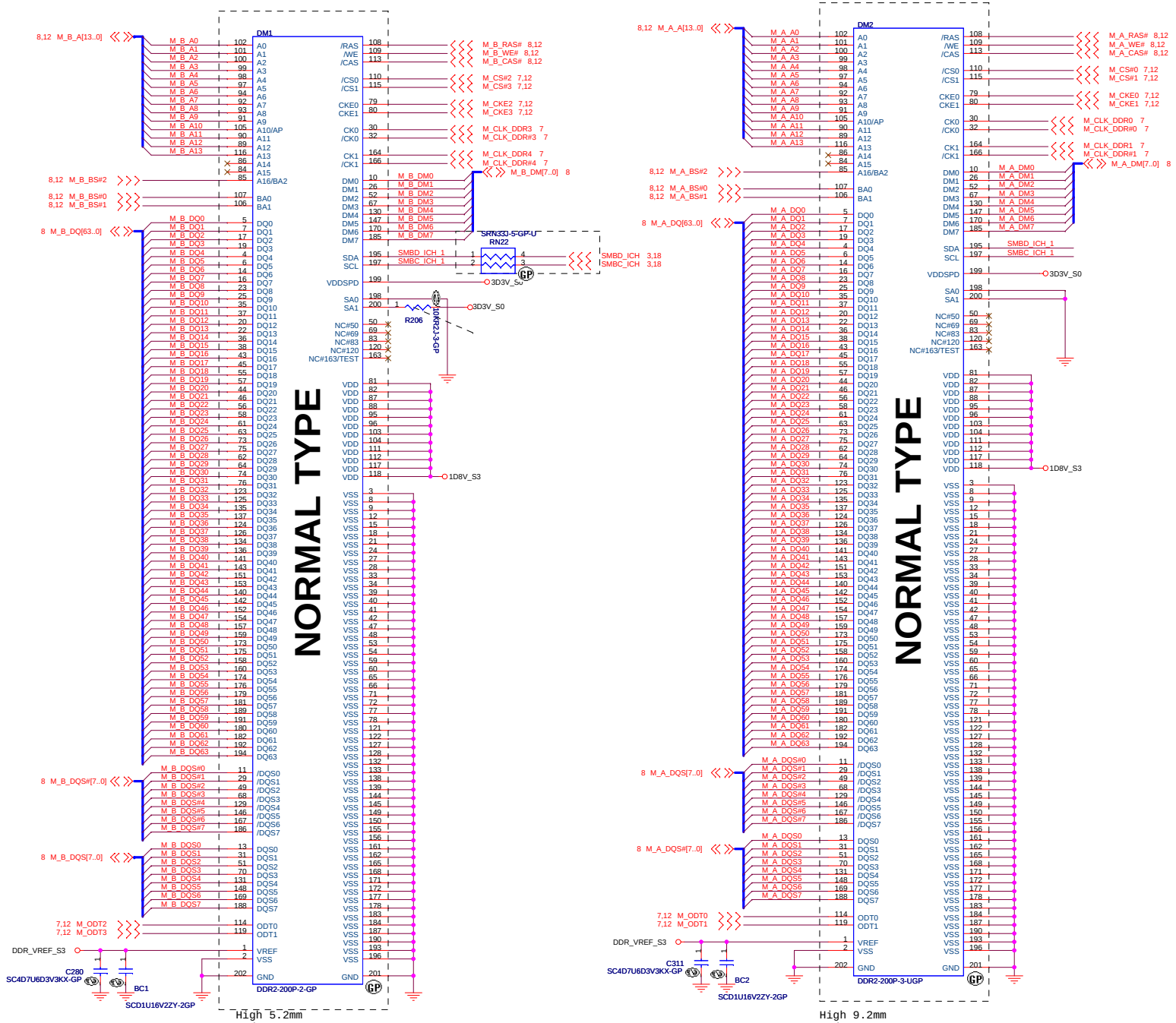
Title: GMCH (5 of 5)

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 10 of 52



High 5.2mm
2nd source:62.10017.661

High 9.2mm
2nd source:62.10017.A61

<Core Design>

緯創資通 **Wistron Corporation**
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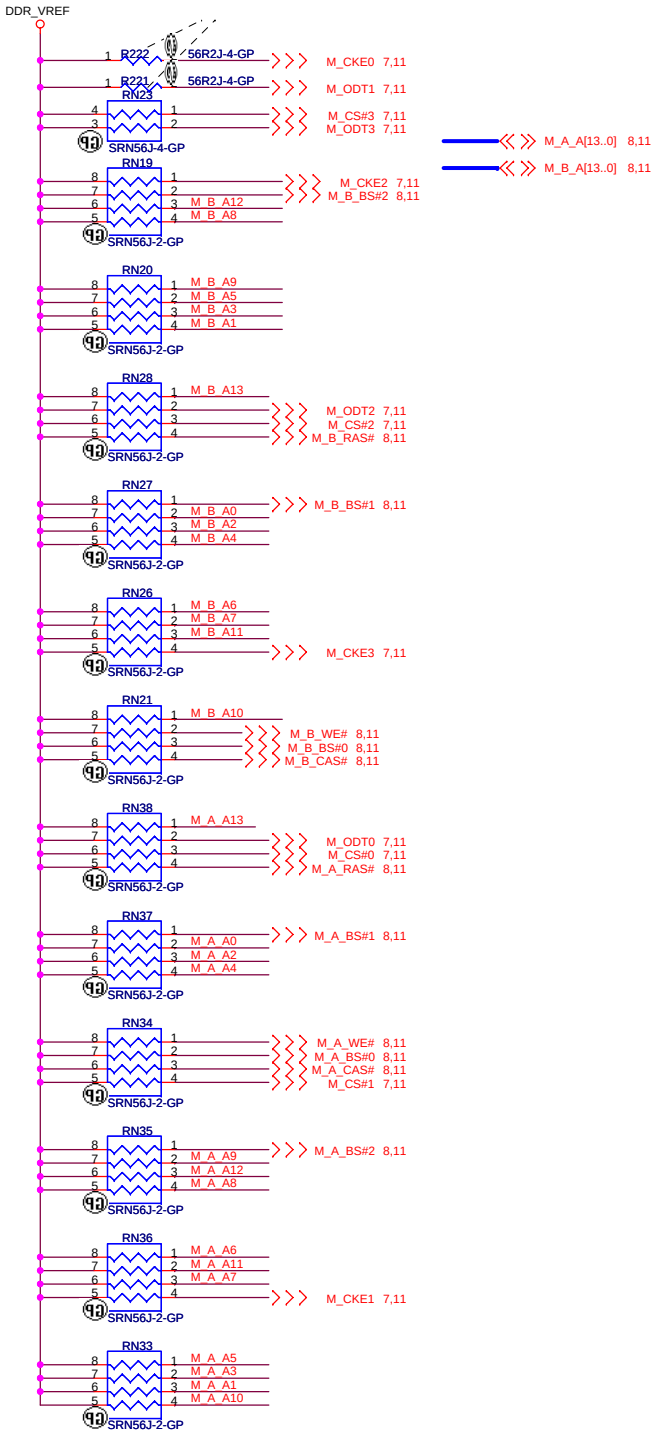
Title: **DDR Socket**

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 11 of 52

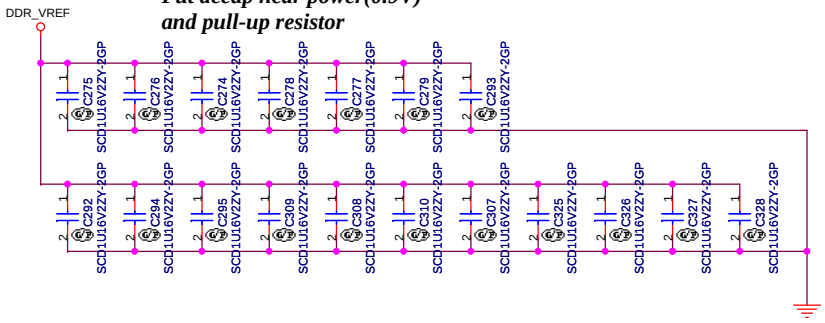
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

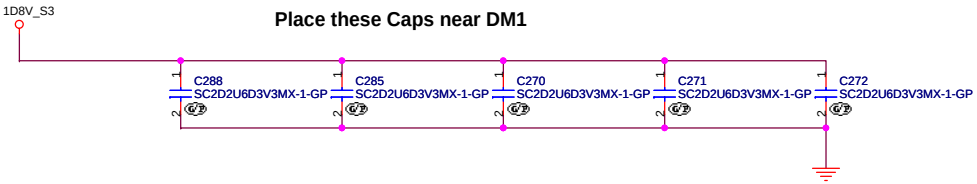


Decoupling Capacitor

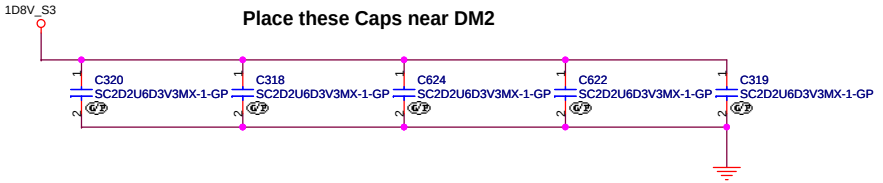
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



<Core Design>

緯創資通 **Wistron Corporation**
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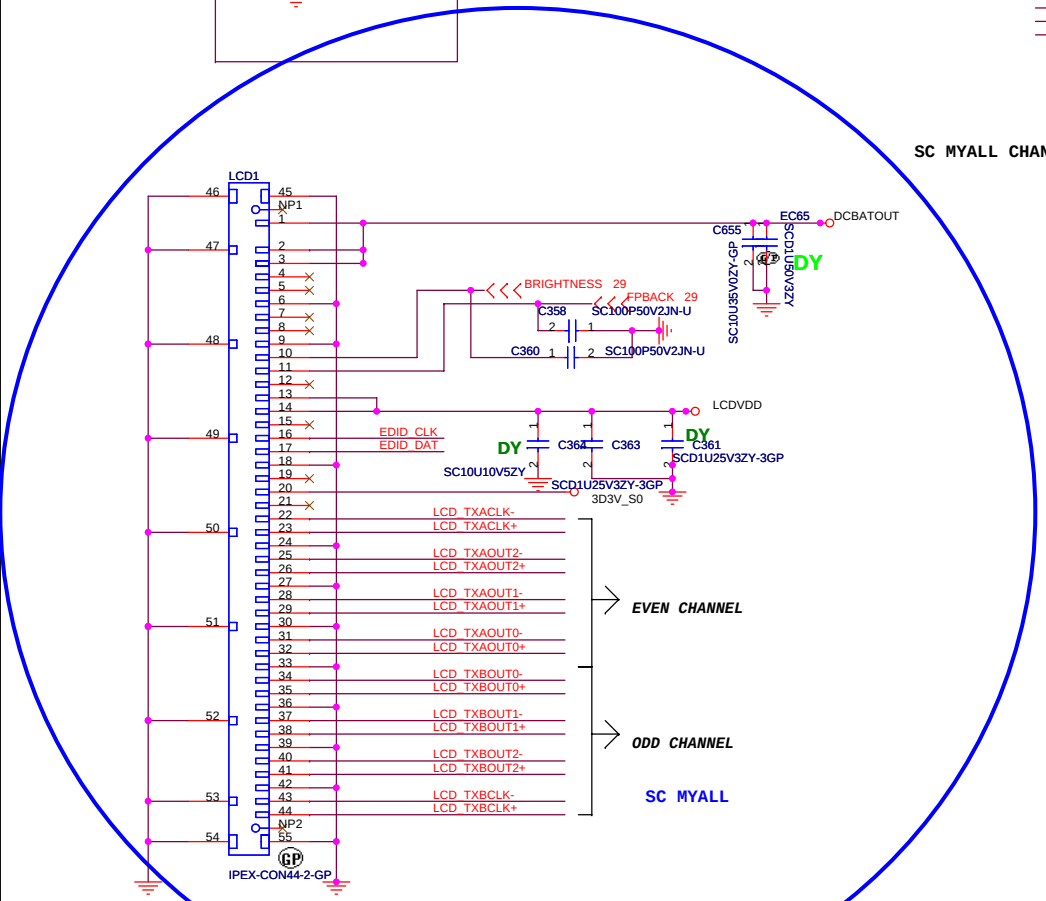
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	MYALL	SA

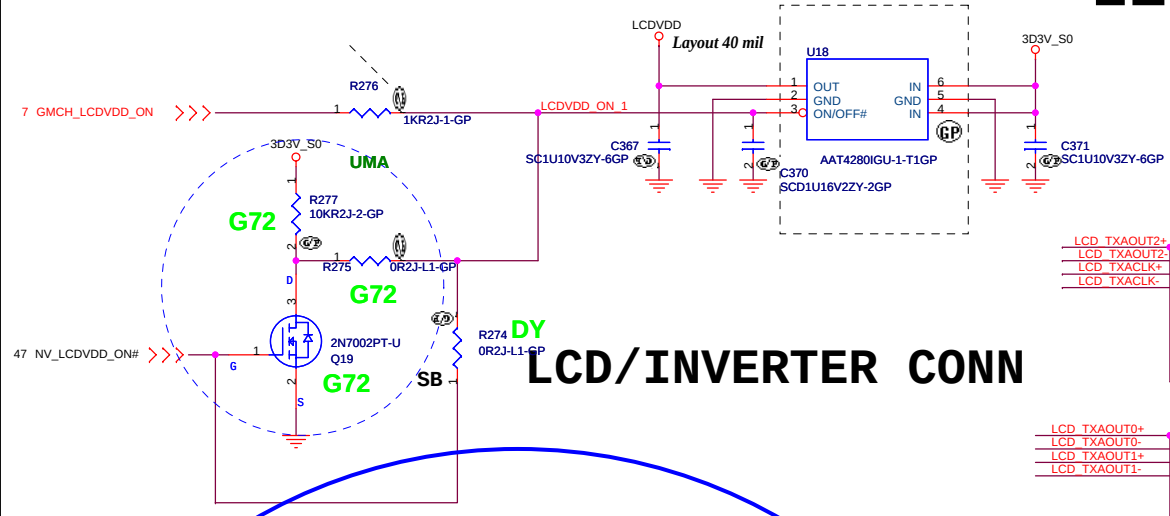
Date: Friday, February 10, 2006 Sheet 12 of 52

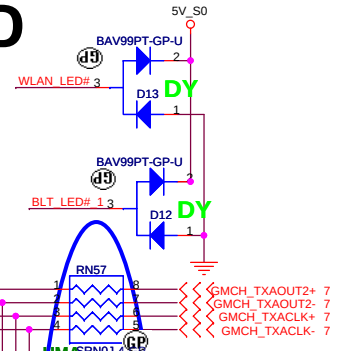
LED

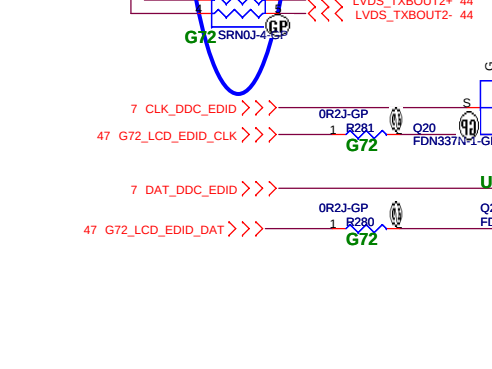
LCD/INVERTER CONN

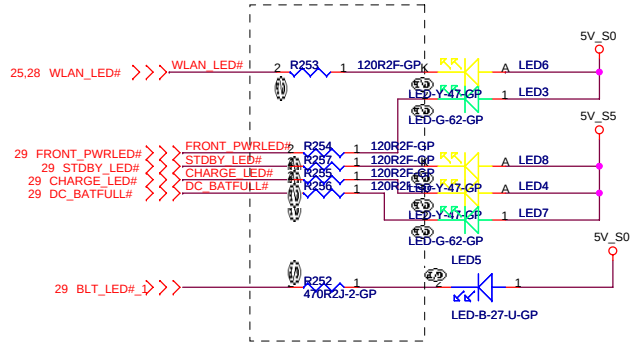


SC MYALL CHANGE 2006.01.11



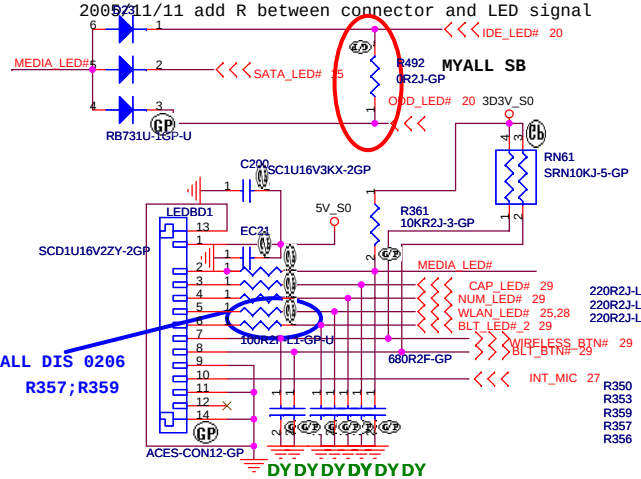




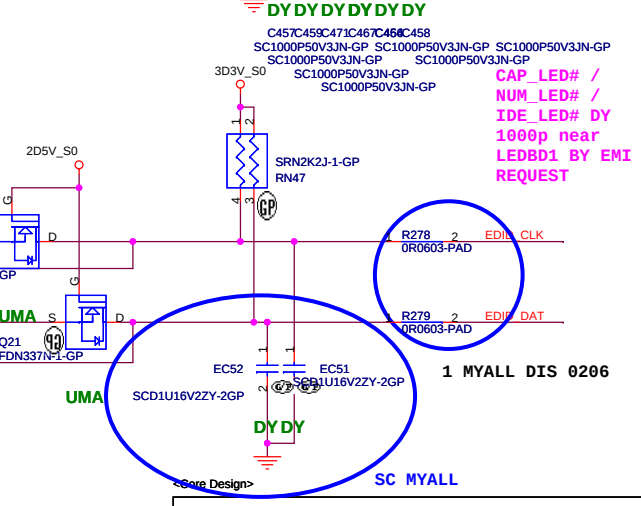


LED BD CONN

2005/11/11 add R between connector and LED signal



1 MYALL DIS 0206
R357;R359



<Core Design>

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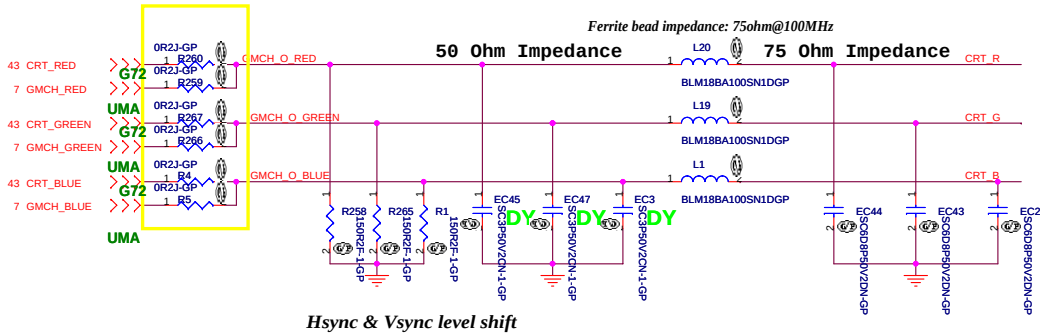
Title: LCD CONN & LED

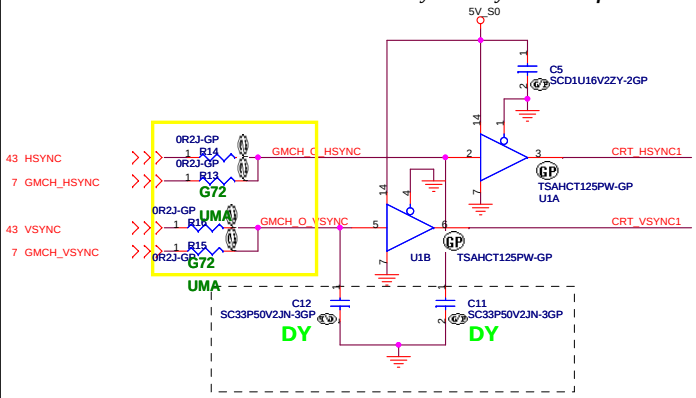
Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 13 of 52

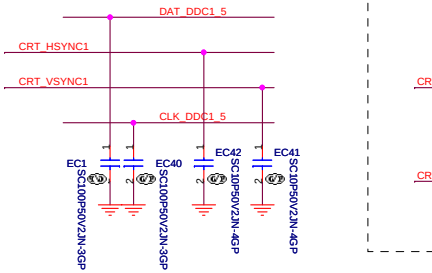
CRT CONNECTOR

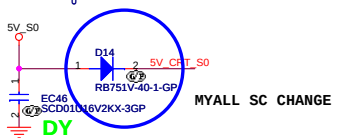


Hsync & Vsync level shift



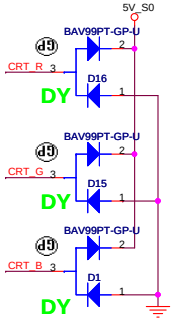
DDC_CLK & DATA level shift

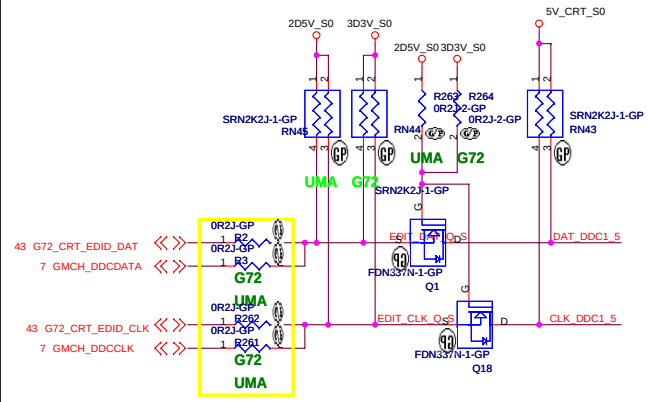




MYALL SC CHANGE

ESD Protection Diode





<Core Design>
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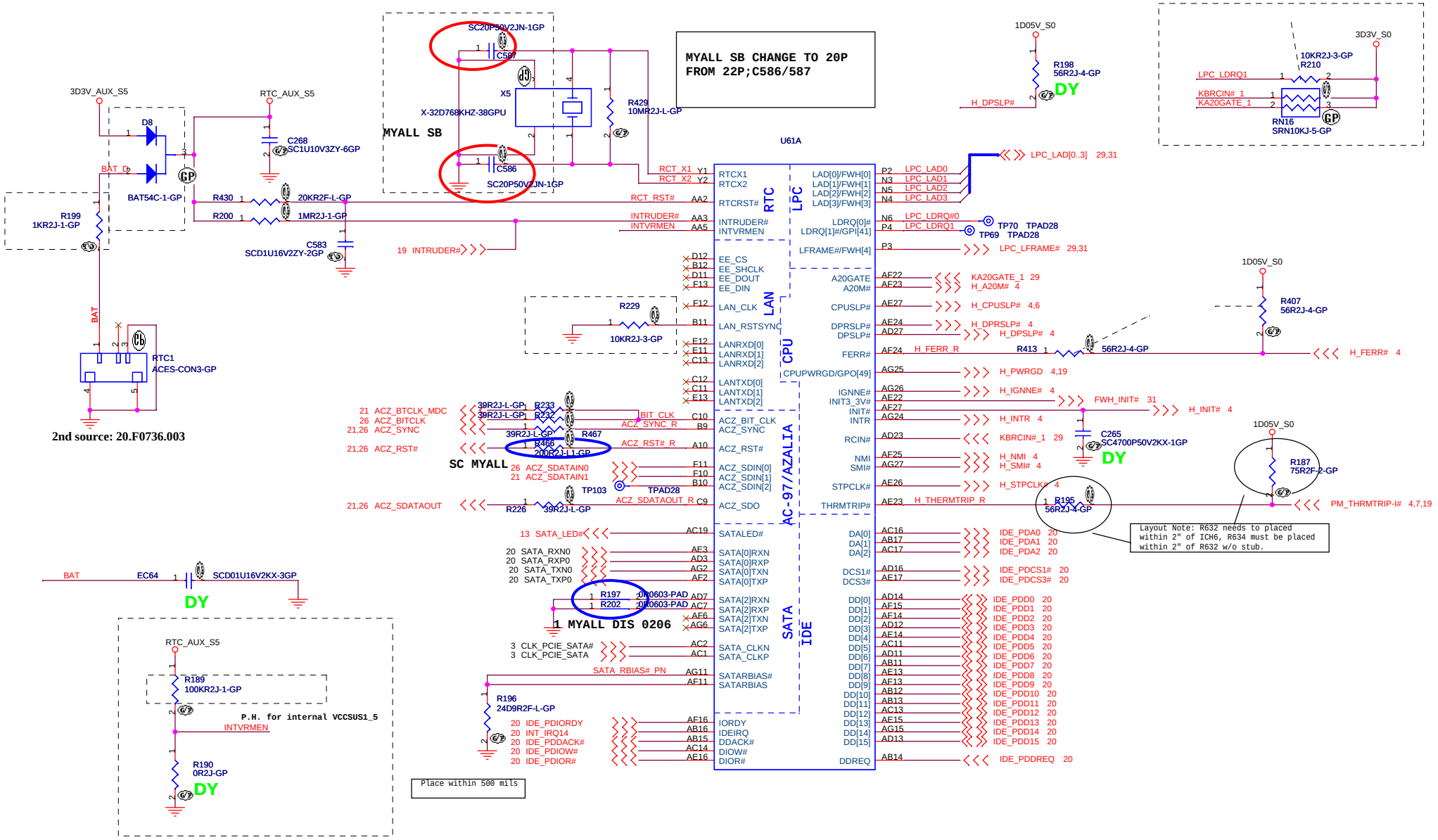
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector		
Size: Custom	Document Number: MYALL	Rev: SA
Date: Friday, February 10, 2006	Sheet 14 of 52	



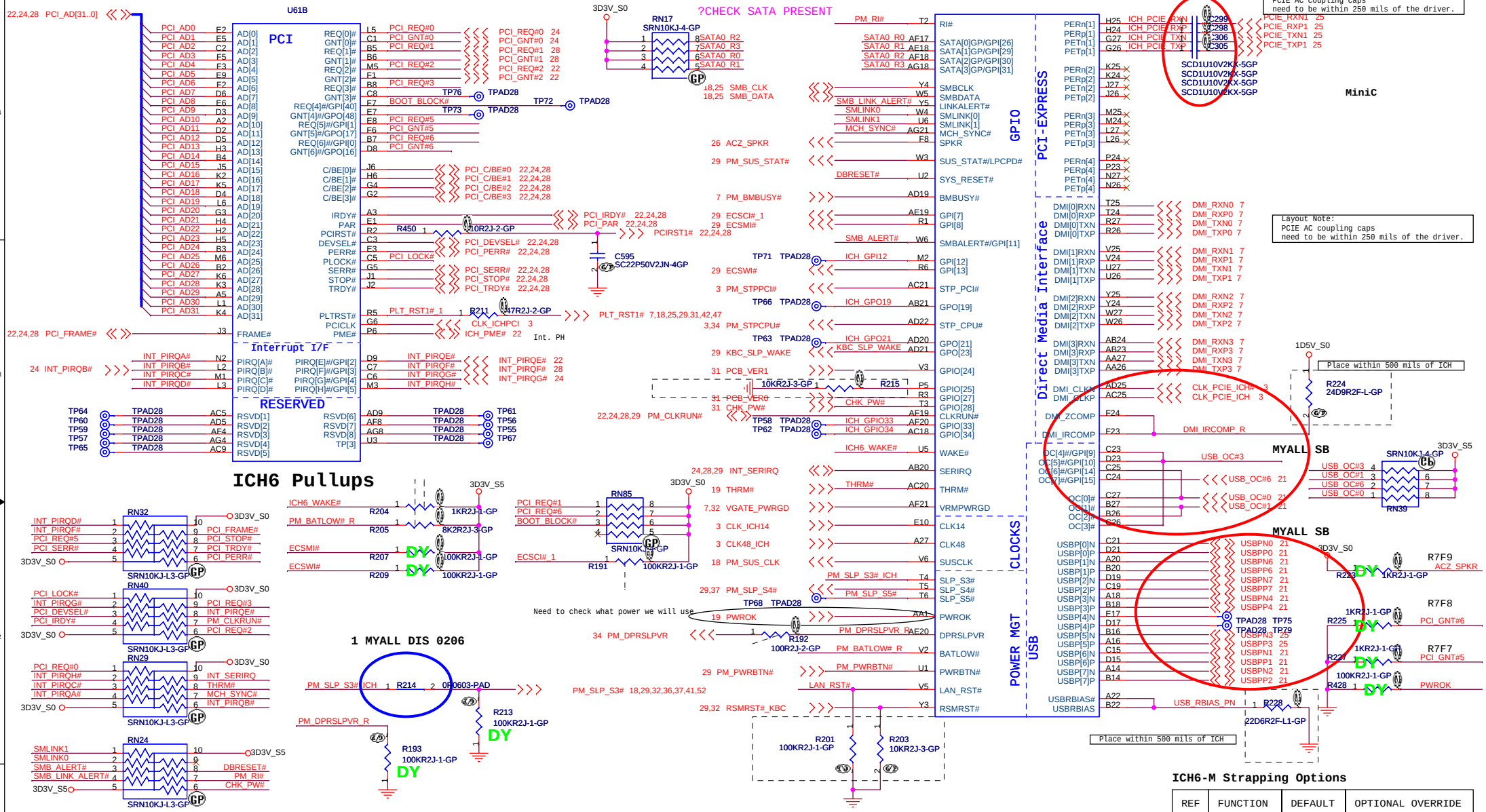
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH6-M (1 of 4)

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 15 of 52



ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

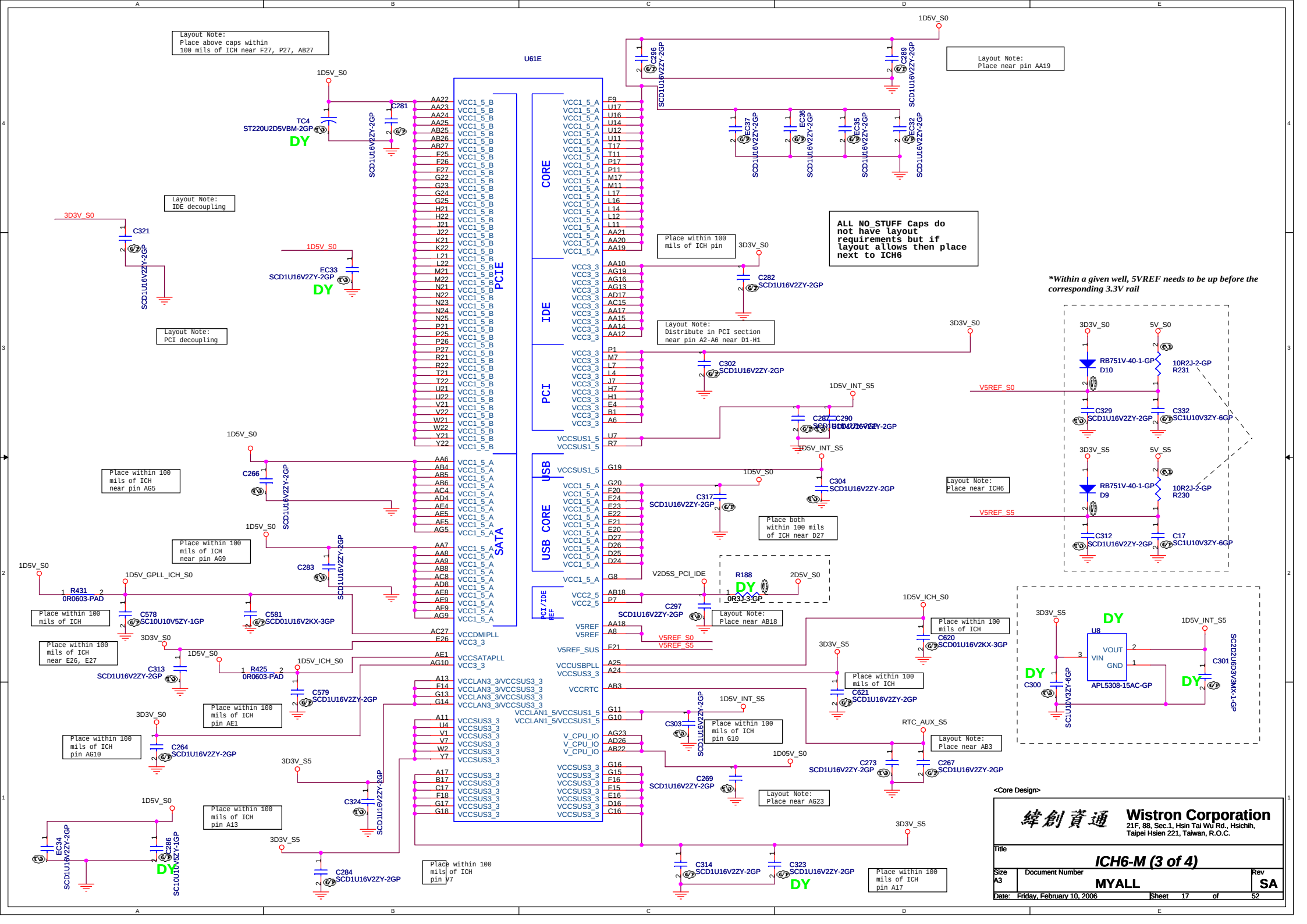
<Core Design>

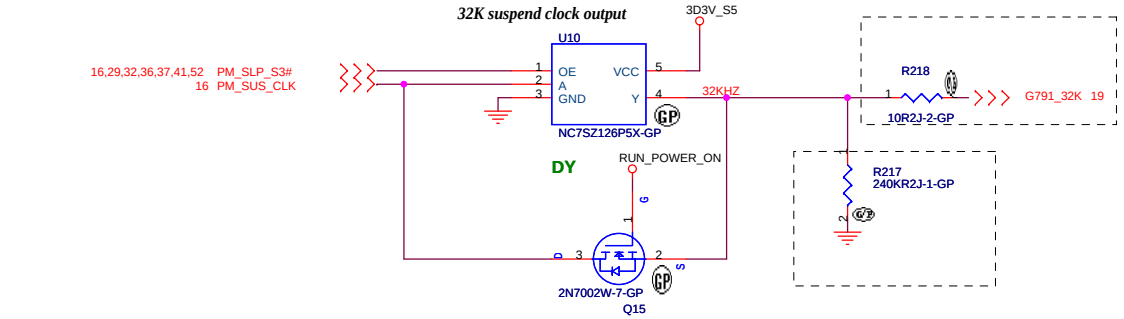
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

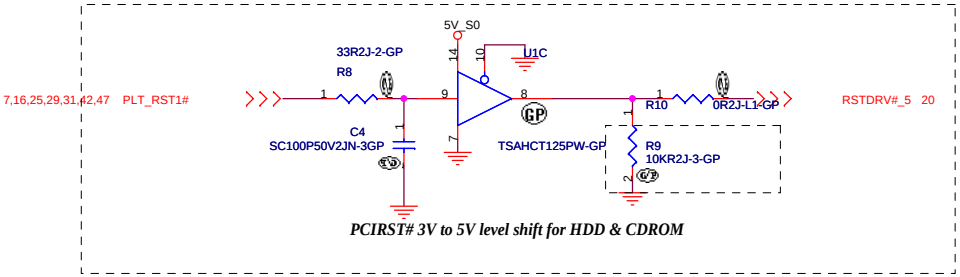
Title: ICH6-M (2 of 4)

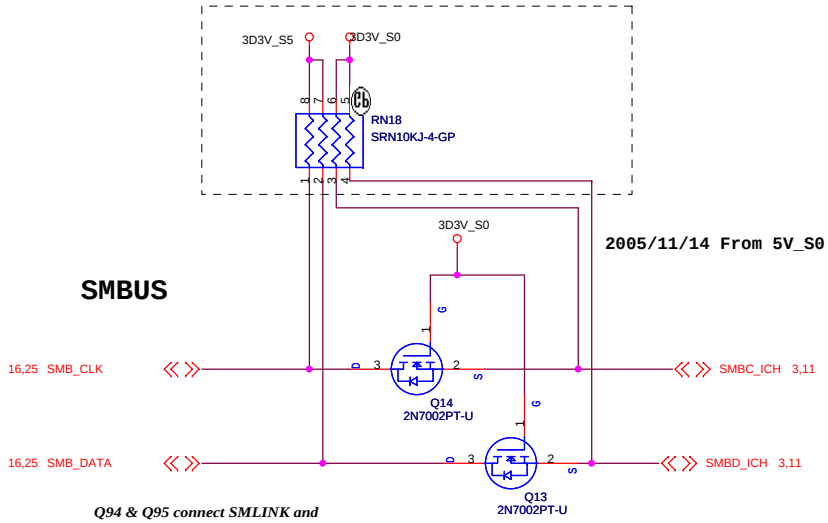
Size: A3 | Document Number: MYALL | Rev: SA

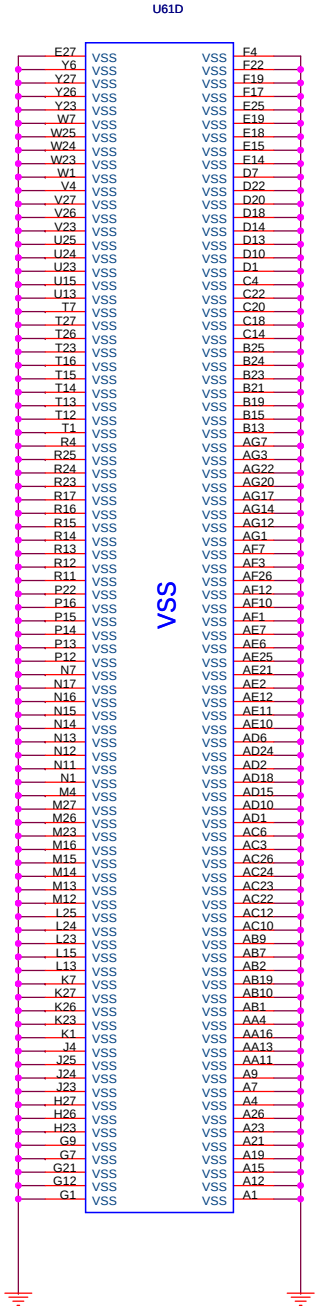
Date: Friday, February 10, 2006 | Sheet 16 of 52


U61E
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near pin AA19
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Layout Note: Place near ICH6
Layout Note: Place near AB18
Layout Note: Place near AB3
Layout Note: Place near AG23
Place within 100 mils of ICH pin
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin A17
Place both within 100 mils of ICH near D27
1D5V_S0
3D3V_S0
1D5V_INT_S5
1D5V_ICH_S0
1D5V_GPLL_ICH_S0
3D3V_S5
5V_S0
5V_S5
1D05V_S0
2D5V_S0
RTC_AUX_S5
V5REF_S0
V5REF_S5
V2D5S_PCI_IDE
DY
SCD1U16V2ZY-2GP
SC1U10V3ZY-6GP
SCD01U16V2KX-3GP
SC10U10V5ZY-1GP
0R0603-PAD
0R3J-3-GP
RB751V-40-1-GP
10R2J-2-GP
APL5308-15AC-GP
SC2D2U6D3V3MX-1-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
Document Number MYALL
Rev SA
Date: Friday, February 10, 2006
Sheet 17 of 52







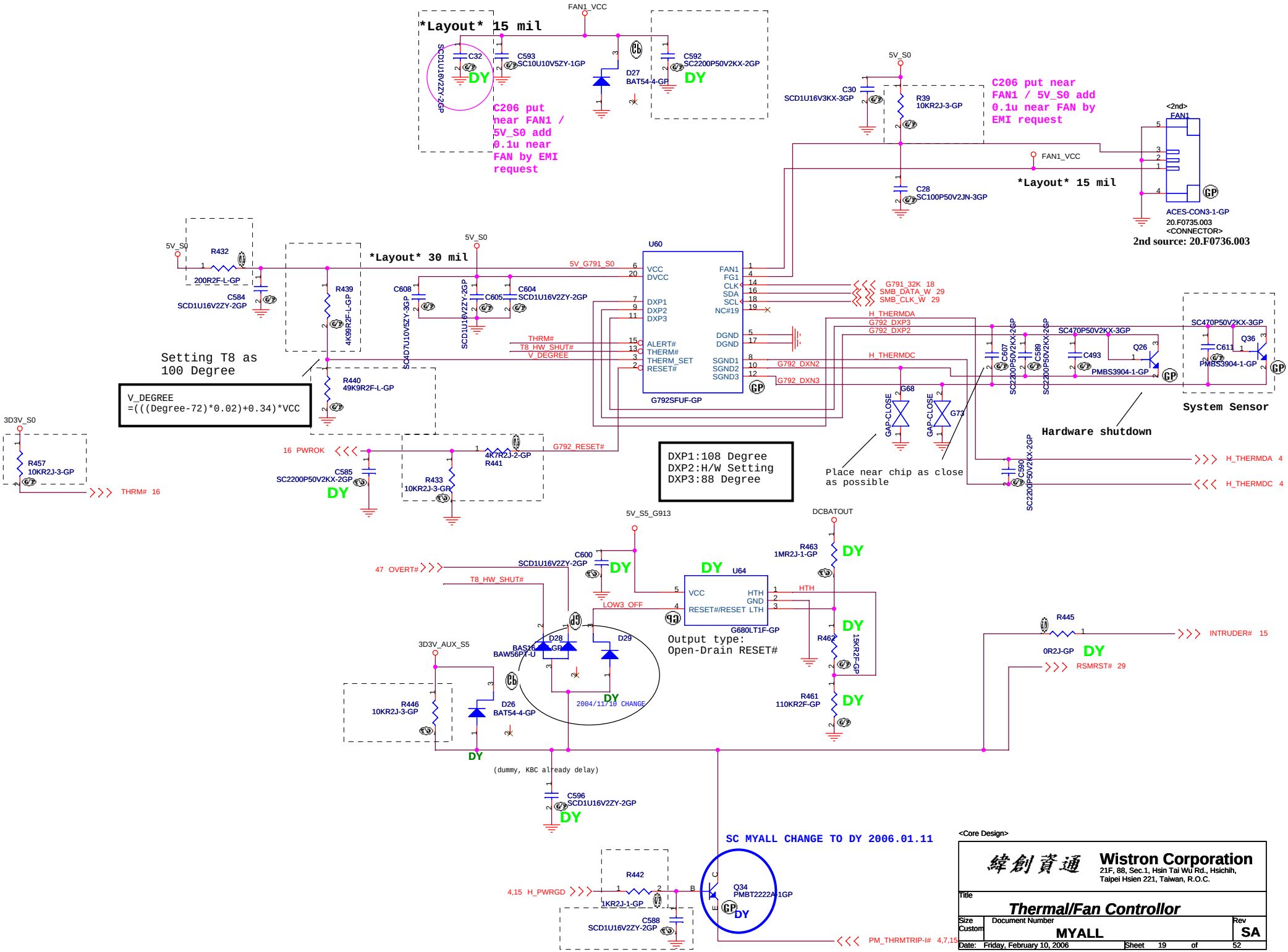


<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

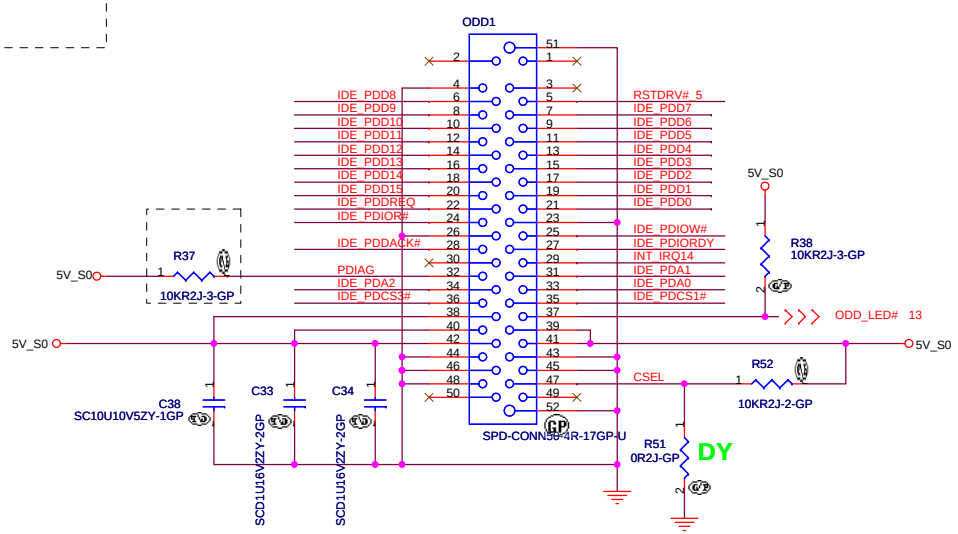
Title: ICH6-M (4 of 4)

Size	Document Number	Rev
A3	MYALL	SA

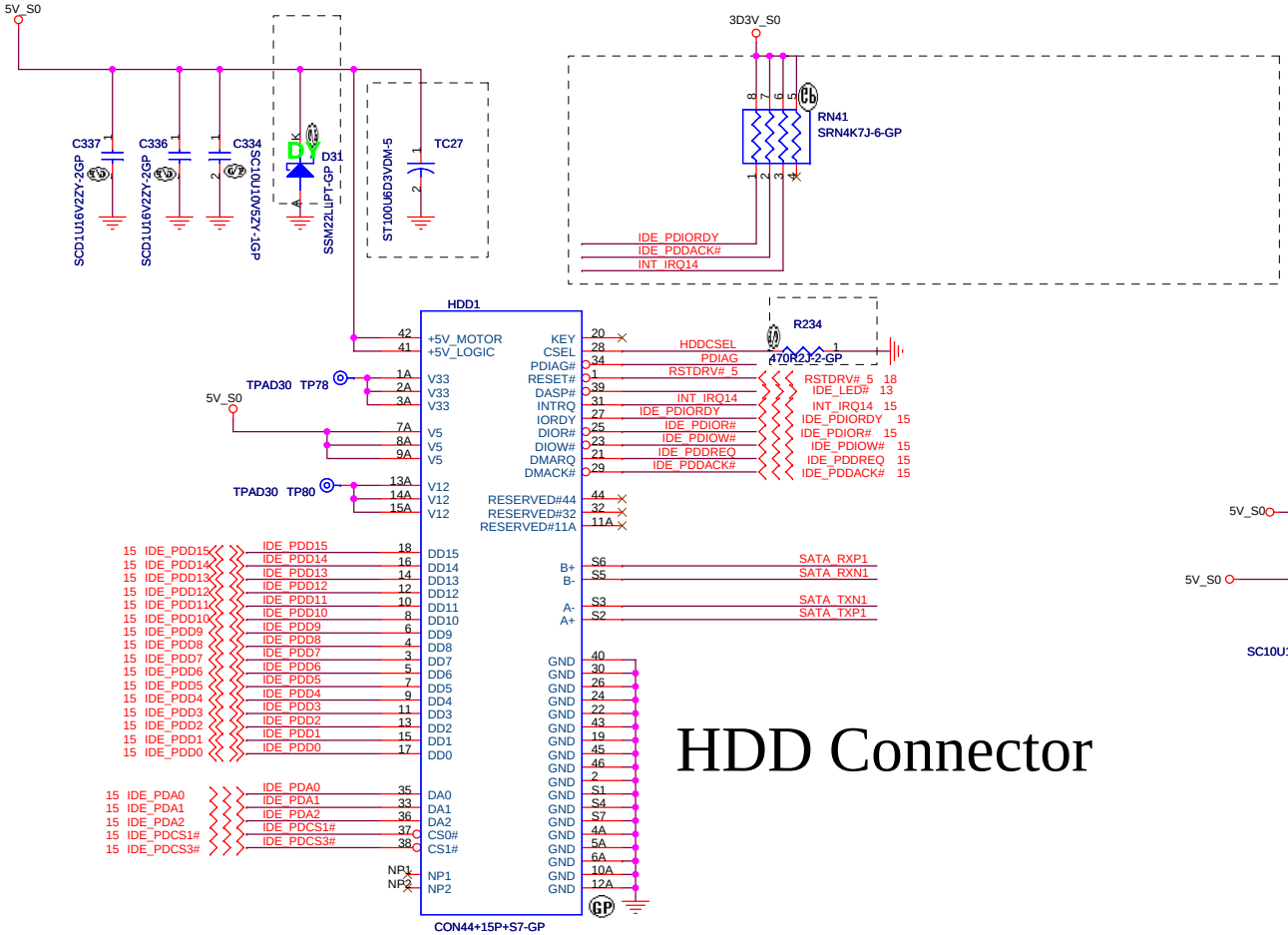
Date: Friday, February 10, 2006 Sheet 18 of 52


Layout 15 mil
FAN1_VCC
C32
SCD1U16V2ZY-2GP
C593
SC10U10V5ZY-1GP
D27
BAT54-4-GP
C592
SC2200P50V2KX-2GP
DY
C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request
5V_S0
C30
SCD1U16V3KX-3GP
R39
10KR2J-3-GP
C206 put near FAN1 / 5V_S0 add 0.1u near FAN by EMI request
<2nd>
FAN1
FAN1_VCC
Layout 15 mil
C28
SC100P50V2JN-3GP
ACES-CON3-1-GP
20.F0735.003
<CONNECTOR>
2nd source: 20.F0736.003
5V_S0
R432
200R2F-L-GP
C584
SCD1U16V2ZY-2GP
Layout 30 mil
R439
4K99R2F-L-GP
C608
SC4D7U10V5ZY-3GP
C605
SCD1U16V2ZY-2GP
C604
SCD1U16V2ZY-2GP
5V_G791_S0
U60
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
G791_32K 18
SMB_DATA_W 29
SMB_CLK_W 29
THRM#
T8_HW_SHUT#
V_DEGREE
H_THERMDA
G792_DXP3
G792_DXP2
H_THERMDC
G792_DXN2
G792_DXN3
Setting T8 as 100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
R440
49K9R2F-L-GP
3D3V_S0
R457
10KR2J-3-GP
THRM# 16
16 PWROK
C585
SC2200P50V2KX-2GP
R433
10KR2J-3-GP
4K7R2J-2-GP
R441
G792_RESET#
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
G68
GAP-CLOSE
G73
GAP-CLOSE
C607
SC2200P50V2KX-2GP
C589
SC2200P50V2KX-2GP
SC470P50V2KX-3GP
C493
Q26
PMBS3904-1-GP
SC470P50V2KX-3GP
C611
Q36
PMBS3904-1-GP
System Sensor
Hardware shutdown
C590
SC2200P50V2KX-2GP
H_THERMDA 4
H_THERMDC 4
5V_S5_G913
C600
SCD1U16V2ZY-2GP
47 OVERT#
T8_HW_SHUT#
LOW3_OFF
U64
VCC
RESET#/RESET
HTH
GND
LTH
G680LT1F-GP
Output type:
Open-Drain RESET#
DCBATOUT
R463
1MR2J-1-GP
R462
15KR2F-GP
R461
110KR2F-GP
HTH
3D3V_AUX_S5
D28
BAS16-GP
BAW56P1-U
D29
D26
BAT54-4-GP
2004/11/10 CHANGE
R446
10KR2J-3-GP
(dummy, KBC already delay)
C596
SCD1U16V2ZY-2GP
R445
0R2J-GP
INTRUDER# 15
RSMRST# 29
SC MYALL CHANGE TO DY 2006.01.11
R442
1KR2J-1-GP
4,15 H_PWRGD
Q34
PMBT2222A-1GP
C588
SCD1U16V2ZY-2GP
PM_THRMTRIP-I# 4,7,15
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Custom
Document Number
MYALL
Rev
SA
Date: Friday, February 10, 2006
Sheet 19 of 52

CD-ROM Connector



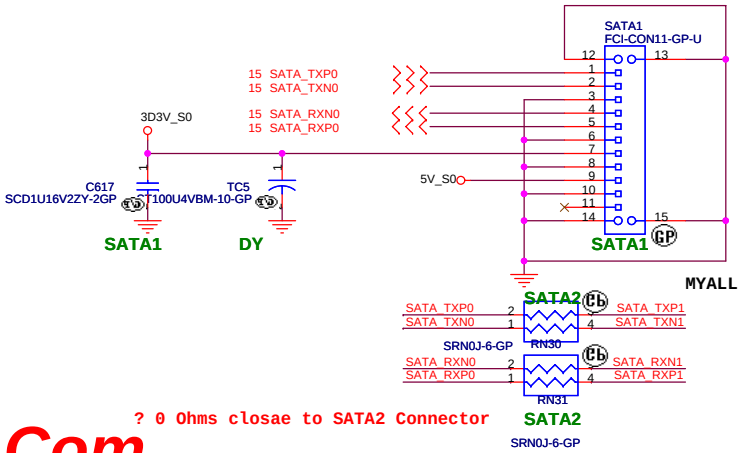
HDD Connector



TC33 CLOSE BETWEEN HDD1 AND SATA1 CONNECTOR.

SATA Connector

PWR TRACE 100mil

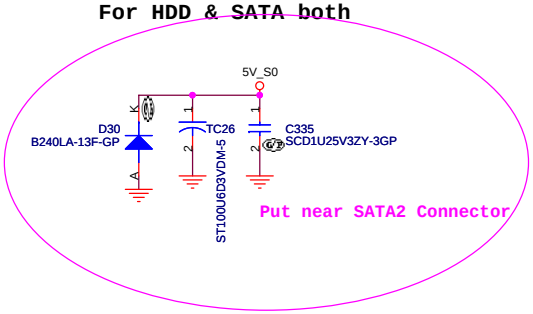


? 0 Ohms closae to SATA2 Connector

MYALL SB RELOAD SYMBOL ADD PIN 12~15

Dummy when use IDE

For HDD & SATA both



ME : 20.F0777.022

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD and CDROM***	
Size A3	Document Number MYALL	Rev SA
Date: Monday, February 13, 2006	Sheet 20 of 52	

USB PORT

100 mil
5V_USB0_S0
TC15 SE100U10VM-4GP
EC25 SCD1U16V2ZY-2GP
EC24 SC1000P50V3JN-GP
DY

5V_S5
U53 G546A2P1UF-GP
GND IN EN1/EN1# EN2/EN2# OC1# OUT1 OUT2 OC2#
29 USB_PWR_EN#
C548 SCD1U16V3KX-3GP
5V_USB0_S0 5V_USB2_S0
SRN0J-6-GP RN68
AG1-910-SB
USB_OC#0 16
USB_OC#6 16
?Check resistance value
EC62 SCD1U16V2ZY-2GP
EC63 SCD1U16V2ZY-2GP
DY DY
AG1-910-SB

MYALL SB CHANGE TO 100U*2 FROM 150U.

100 mil
5V_USB1_S0
TC6 SE100U10VM-4GP
TC30 SE100U10VM-4GP
EC4 SCD1U16V2ZY-2GP
EC5 SC1000P50V3JN-GP
DY

100 mil
5V_USB2_S0
TC22 SE150U6D3VDM-GP
EC60 SCD1U16V2ZY-2GP
EC30 SC1000P50V3JN-GP
DY

5V_USB1_S0
5V_S5
U14 G528P1UF-GP
GND IN IN EN#/EN OUT OUT OUT FLG
29 USB_PWR_EN#
C356 SCD1U16V3KX-3GP
R268 0R0603-PAD
USB_OC#1 16
1 MYALL DIS 0206
EC48 SCD1U16V2ZY-2GP
DY

AG1-910-01
16 USBPN6
16 USBPP6
RN62 SRN0J-6-GP
USB_6-
USB_6+
L16 68.00201.141 DLW21HN900SQ2LGP
DY

16 USBPP0
16 USBPN0
SRN0J-6-GP RN60
USB_0+
USB_0-
L15 68.00201.141 DLW21HN900SQ2LGP
DY

5V_USB0_S0
USB3
USB_0-
USB_0+
SKT-USB-167-GP-U

Right side

5V_USB2_S0
USB4
USB_6-
USB_6+
SKT-USB-167-GP-U

5V_USB2_S0
USB5
USB_7-
USB_7+
SKT-USB-167-GP-U

AG1-A-SA

BLUETOOTH MODULE

3D3V_BT_S0
EC31 SCD1U16V2ZY-2GP
DY
U7 74.04250.A3F AAT4250IGV-T1-GP
OUT GND NC#3 IN ON/OFF#
3D3V_S0
C263 SC4D7U10V5ZY-3GP
BLUETOOTH_EN 29
L18 68.00201.141 DLW21HN900SQ2LGP
DY

EC38 put near BLUE1 / all USB put one choke near connector by EMI request

AG1-A-SA
SRN0J-6-GP RN25
USBPN4 16
USBPP4 16
3D3V_BT_S0
ACES-CON4-1-GP BLUE1

1st source: 20.D0197.104

AG1-910-SB
16 USBPN2
16 USBPP2
SRN0J-6-GP RN42
USB_2-
USB_2+
L2 68.00201.141 DLW21HN900SQ2LGP
DY

16 USBPN7
16 USBPP7
RN63 SRN0J-6-GP
USB_7-
USB_7+
L17 68.00201.141 DLW21HN900SQ2LGP
DY

EC38 put near BLUE1 / all USB put one choke near connector by EMI request

5V_USB1_S0
USB2
USB_1-
USB_1+
SKT-USB-97-UGP

5V_USB1_S0
USB1
USB_2-
USB_2+
SKT-USB-97-UGP

Rear side

MDC 1.5 CONNECTOR

CHANGE TO AZ

1 MYALL DIS 0206
R21 0R0603-PAD
15,26 ACZ_SDATAOUT
ACZ_SDATAOUT
15,26 ACZ_SYNC
15 ACZ_SDATAIN1
15,26 ACZ_RST#
39R2J-1-GP R23
ACZ_SYNC
ACSDATAIN1_A
ACZ_RST#
C14 SC22P50V2JN-4GP
DY
C13 SCD47U10V3ZY-GP
DY
R20 10R2J-2-GP

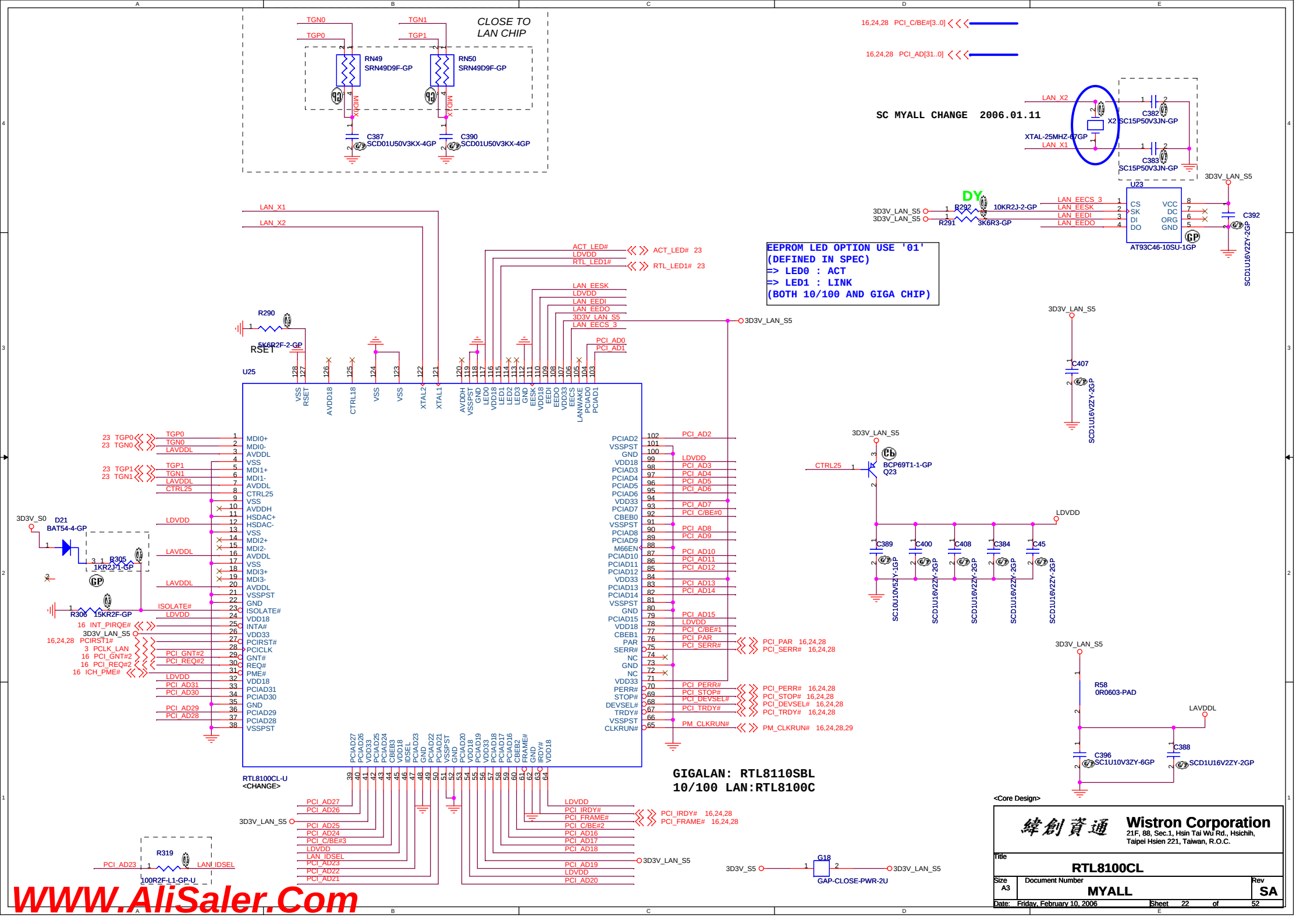
MDC1 <2nd>
MH1 MH2
AMP-CONN12A-GP
<CONNECTOR>
20.F0582.012
2nd source: 20.F0604.012

TP82 TPAD28
TP83 TPAD28
3D3V_S5
ACZ_BITCLK_MDC 15
C375 SC4D7U10V5ZY-3GP
R283 100KR2J-1-GP
C376 DUMMY-C2

AG1-910-01
16 USBPN1
16 USBPP1
SRN0J-6-GP RN1
USB_1-
USB_1+
L21 68.00201.141 DLW21HN900SQ2LGP
DY

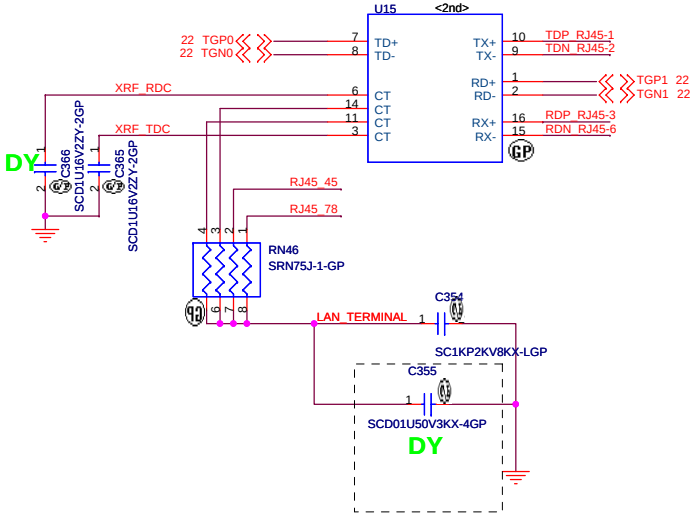
<Core Design>

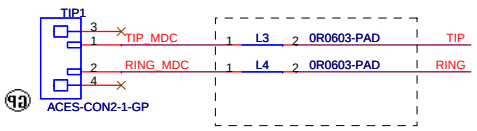
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / MDC / BLUETOOTH		
Size: A3	Document Number: MYALL	Rev: SA
Date: Friday, February 10, 2006	Sheet 21 of 52	



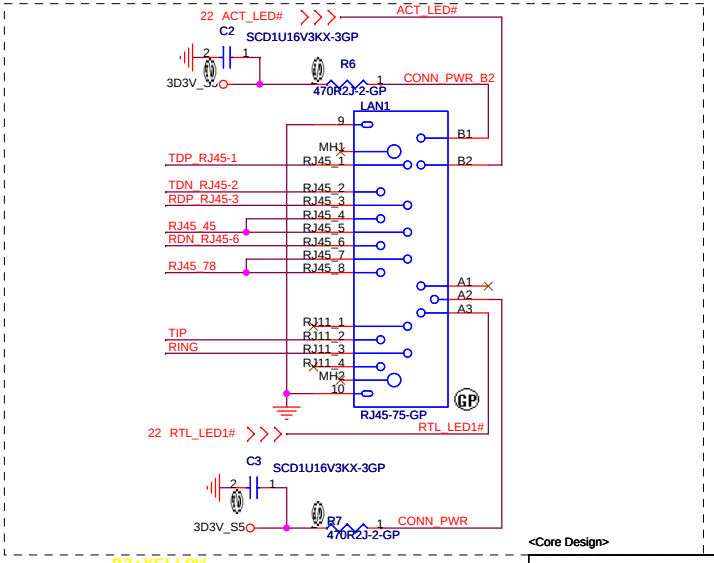
LAN Connector

10/100M Lan Transformer





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

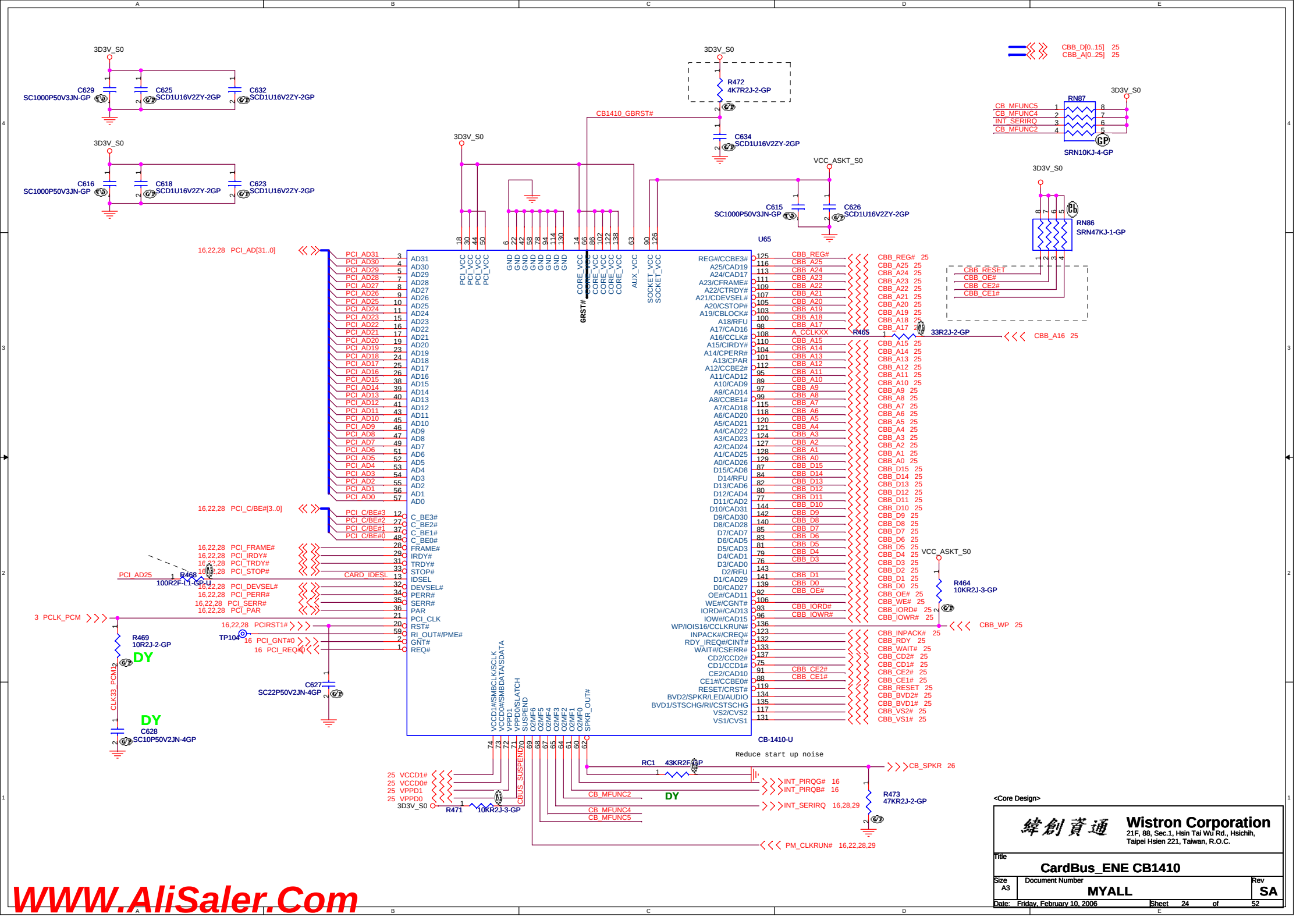


<Core Design>

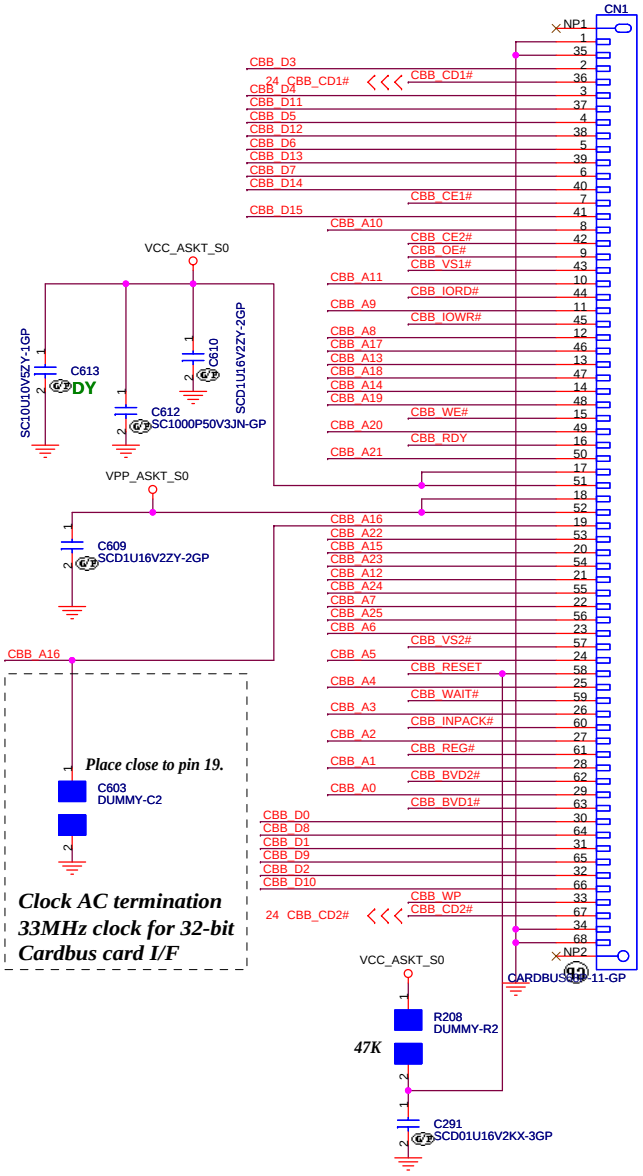
B2:YELLOW
A1:ORANGE
A3:GREEN

3D3V_S5 add 0.1u near LAN1 by EMI request

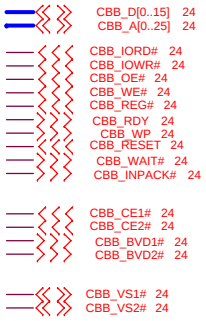
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAN CONN**	
Size A3	Document Number **MYALL**	Rev **SA**
Date: Friday, February 10, 2006	Sheet 23 of 52	

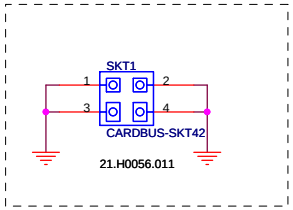


PCMCIA Socket

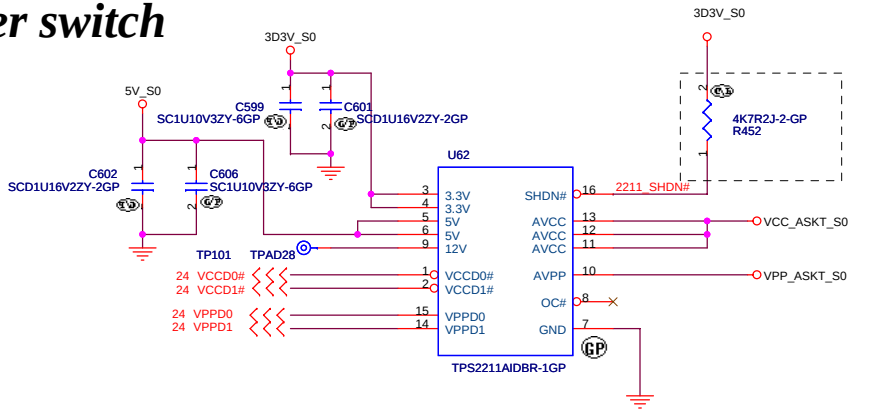


Cardbus I/F

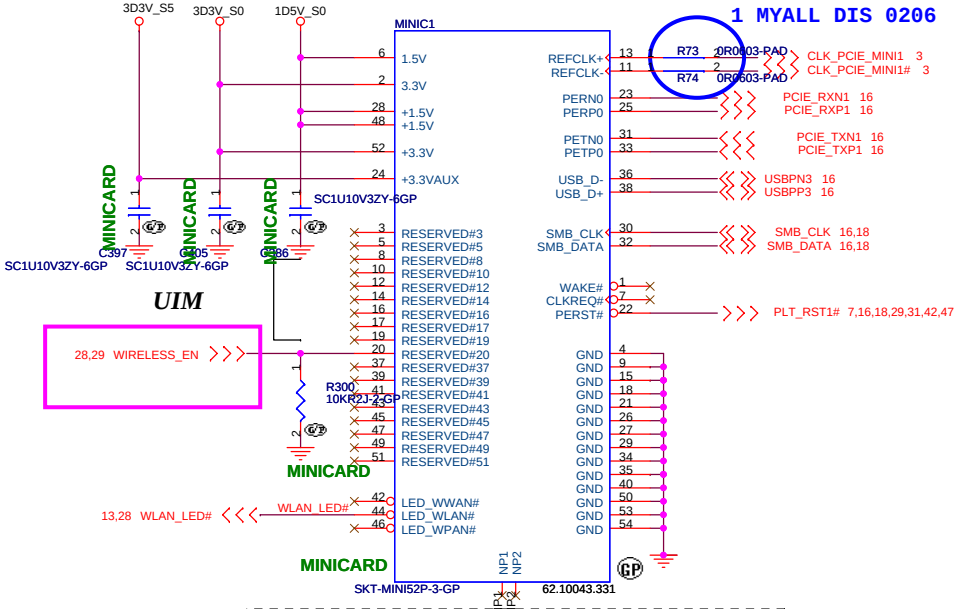




Power switch

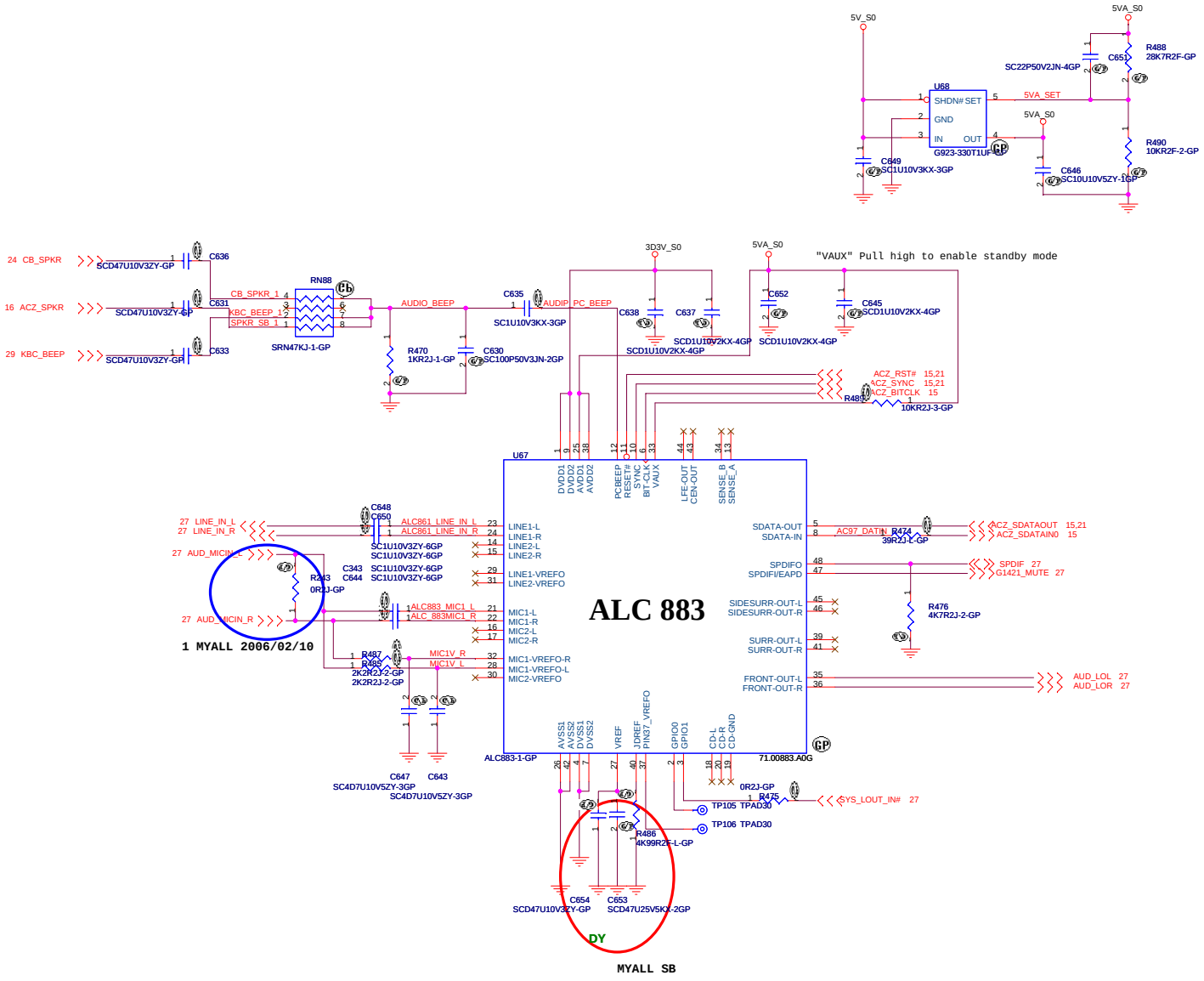


Mini Card Connector



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	PCMCIA /PCIE MINI CARD	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 25 of 52	



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - ALC883

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 26 of 52

AUDIO OP AMPLIFIER

MYALL SB DELETE GAP

I/P signal level need +5V level

5V_S0 R250 0R0603-PAD

C339 SC10U10V5ZY-1GP
C341 SCD1U16V2ZY-2GP
C347 SCD1U16V2ZY-2GP
C348 SC10U10V5ZY-1GP

DY

TP81 TPAD28

AMP_SHUTDOWN 29

R235 10KR2J-2-GP

U12

R238 10KR2J-2-GP
R236 10KR2J-2-GP
SC1U10V3ZY-6GP C338

26 AUD_LOL
SOUND_L2
SOUND_L_OP1
SPKR_L+
SPKR_L-
LIN1
LIN2
LOUT+
LOUT-
NC#6
NC#8
NC#23
MUTE
VOL
LVDD
RVDD
SHUTDOWN
IN1#/IN2
GND/HS
GND
LBYPASS
RBYPBASS
RIN1
RIN2
ROUT+
ROUT-
SOUND_R_OP1
SPKR_R+
SPKR_R-
SOUND_R2
AUD_LOR 26

C342 SC1U10V3ZY-6GP
R240 0R2J-GP
DY

10KR2J-2-GP
R247
SC1U10V3ZY-6GP C350
R242 10KR2J-2-GP
C344 SC1U10V3ZY-6GP

MYALL SC ADDED

5VA_OP_S0
R501 100KR2J-1-GP
R502 49K9R2F-L-GP
Q37 2N3906-3-GP
R503 100KR2J-1-GP
R504 100KR2J-1-GP
R505 49K9R2F-L-GP
Q38 2N3906-3-GP
R506 100KR2J-1-GP

G1432_RBYPASS
G1432Q5U-GP
C349
G1432_LBYPASS
SC2D2U16V5ZY-2GP
C340
SC2D2U16V5ZY-2GP

5V_S0 5VA_OP_S0
G9 GAP-CLOSE-PWR
MYALL SB
CHANGE TO CLOSE GAP
C351 SC4D7U10V5ZY-3GP

29 KBC_MUTE
26 G1421_MUTE
SYS_LOUT_IN
D11 RB731U-1GP-U
MUTE_5
R237 10KR2J-3-GP
R239 10KR2J-3-GP
R241 100KR2J-1-GP

KBC_MUTE_GPIO8

LINE IN

26 LINE_IN_R
26 LINE_IN_L
R481 1KR2J-1-GP AUD_LINE_R
R483 1KR2J-1-GP AUD_LINE_L
R482 10KR2J-3-GP
R480 10KR2J-3-GP
C642 SC100P50V2JN-U
C641 SC100P50V2JN-U
PHONE-JK234-GP
LIN1

LINE OUT

5VA_OP_S0
R249 10KR2J-2-GP
R244 10KR2J-2-GP
SYS_LOUT_IN
SYS_LOUT_IN#
Q16 DTC114EUA-1-GP
U13 AAT4250IGV-T1-GP
ON/OFF# IN NC#3 GND OUT
C352 SCD1U16V2ZY-2GP
5V_SPDIF_S0
5V_S0

EC
MYALL SC CHANGE TO 22U FROM 68U
TC28 SC10U6D3V6MX-2GP
TC29 SC10U6D3V6MX-2GP
AUD_LOL
AUD_LOR
SPKR_L+1
SPKR_R+1
R251 1KR2J-1-GP
R248 1KR2J-1-GP
1 MYALL DIS 0206

26 SPDIF
26 SYS_LOUT_IN#
R246 22R2J-2-GP
R245 22R2J-2-GP
SPKR_L_A1
SPKR_R_A1
LOUT1
GND VCC VIN
PHONE-JK237-GP
C346 SC680P50V2KX-2GP
C345 SC680P50V2KX-2GP
EC38 SC330P50V2KX3GP
EC39 SC330P50V2KX3GP

Internal Speaker

SPKR_L-
SPKR_L+
SPKR_R+
SPKR_R-
SRC100P50V-2-GP ERC11
ACES-CON4-1-GP SPKR1

1st source: 20.D0197.104

MIC IN

MYALL SB
R478;R479 CHANGE TO 0 Ohm FROM 1K

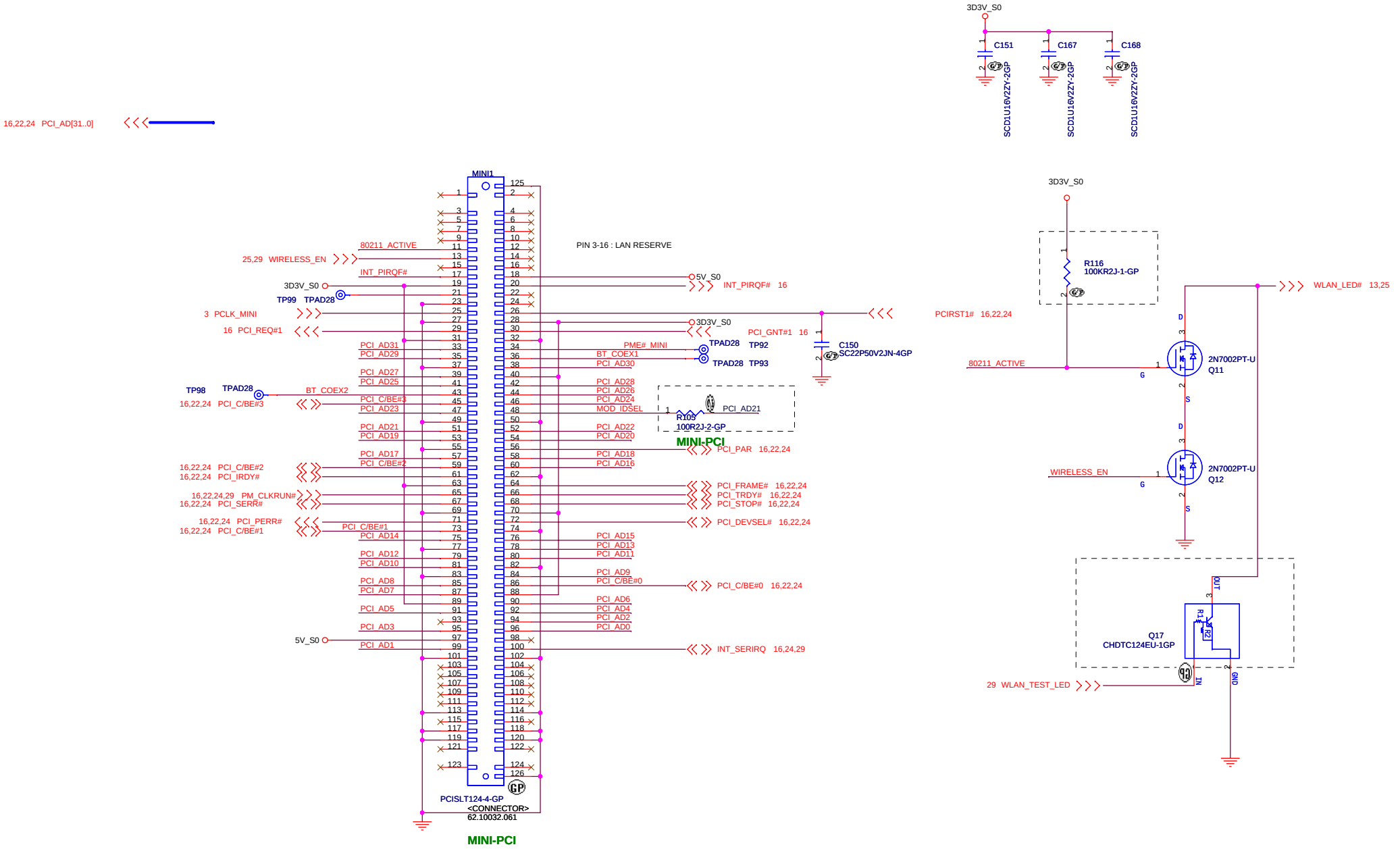
26 AUD_MICIN_R
13 INT_MIC
26 AUD_MICIN_L
R478 0R2J-GP
R479 0R2J-GP
AUD_MIC_R
AUD_MIC_L
R484 10KR2J-3-GP
R477 10KR2J-3-GP
C640 SC100P50V2JN-U
C639 SC100P50V2JN-U
PHONE-JK233-GP
MIC1

R484;R477 CHANGE TO DY
DY DY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK
Size: Document Number: MYALL Rev: SA
Date: Friday, February 10, 2006 Sheet 27 of 52



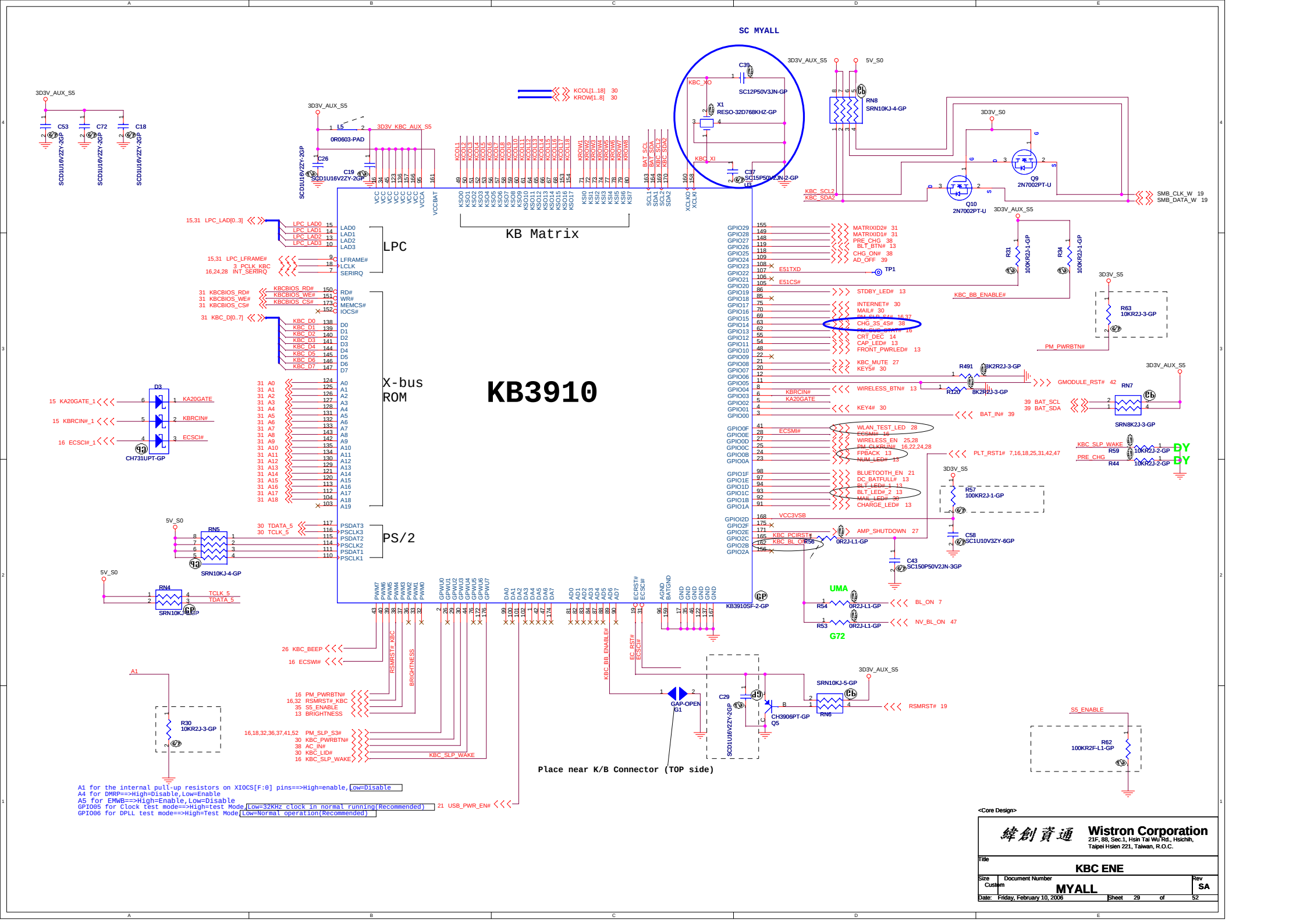
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI-PCI

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 28 of 52


SC MYALL
KB3910
KB Matrix
LPC
X-bus ROM
PS/2
Place near K/B Connector (TOP side)
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable, Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
UMA
G72
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ENE
MYALL
Date: Friday, February 10, 2006
Sheet 29 of 52

LAUNCH BD CONN

Internet Button

Mail Button

Power Button

2nd source: 20.K0185.012

Program Button

E-Button

POWER LED FOR BUTTON SIDE

MAIL LED FOR BUTTON SIDE

SC MYALL

SC MYALL

Cover Up Switch

TOUCH PAD

2nd source: 62.40009.341

EMI Bypass cap.

Internal KeyBoard CONN

CHECK KB SPEC. AND PIN DEFINE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 30 of 52

KBC_D[0..7] 29

29 KBCBIOS_WE#
29 KBCBIOS_RD#
29 KBCBIOS_CS#

3D3V_AUX_S5

C333
SCD1U16V2ZY-2GP

U66

A18 29
A17 29
A16 29

29 KBC_D0
29 KBC_D1
29 KBC_D2
29 KBC_D3
29 KBC_D4
29 KBC_D5
29 KBC_D6
29 KBC_D7

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7

VDD VSS CE# OE# WE# A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A0 A1 A2 A3 A4 A5 A6 A7

A15 29
A14 29
A13 29
A12 29
A11 29
A10 29
A9 29
A8 29

29 A0
29 A1
29 A2
29 A3
29 A4
29 A5
29 A6
29 A7

MYALL SB DELETE BIOS SOCKET

NEED PUT SOCKET
P/N AND FLASH
ROM P/N IN BOM

72.39040.H03 FOR LEAD FREE

ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:

U2762.10054.051SOCKET

TOP VIEW

A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD

5V_S0
U63
GF_RST#
GF_LPC_LFRAME#
GF_PCLK_FWH
GF_FWH_INIT#
GF_LPC_LAD3
GF_LPC_LAD2
GF_LPC_LAD1
GF_LPC_LAD0
EXT_FWH#
TPAD30
TP100
TP102
3D3V_S0
FOX-GF30
ZZ.GF030.XXX

15,29 LPC_LAD[0:3]

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

3D3V_S0
SRN10KJ-5-GP
RN15

7,16,18,25,29,42,47 PLT_RST1#
15,29 LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#

PLT_RST1# R460 10KR2J-2-GP GF_RST#
LPC_LFRAME# R458 10KR2J-2-GP GF_LPC_LFRAME#
PCLK_FWH R462 10KR2J-2-GP GF_PCLK_FWH
FWH_INIT# R459 10KR2J-2-GP GF_FWH_INIT#
LPC_LAD3 R457 10KR2J-2-GP GF_LPC_LAD3
LPC_LAD2 R464 10KR2J-2-GP GF_LPC_LAD2
LPC_LAD1 R463 10KR2J-2-GP GF_LPC_LAD1
LPC_LAD0 R461 10KR2J-2-GP GF_LPC_LAD0
DY

Plz put G12 close SW1
GAP-OPEN
G2

PH at ICH6M

16 CHK_PW#
29 MATRIXID1#
29 MATRIXID2#

SW6
SW-DIP-4

EC23
SC1000P50V3JN-GP
DY

C619 SC10U6D3V5MX
C614 SCD1U16V
C594 SCD1U16V
DY DY DY

Board ID

3D3V_S0
R212 10KR2J-3-GP DY
R443 10KR2J-3-GP DY
16 PCB_VER0
16 PCB_VER1
PCB_VER0
PCB_VER1
R216 10KR2J-3-GP DY
R447 10KR2J-3-GP DY

Planar ID(2,1,0)
SA:
SB:
-1 :

Keyboard matrix (from vendor)

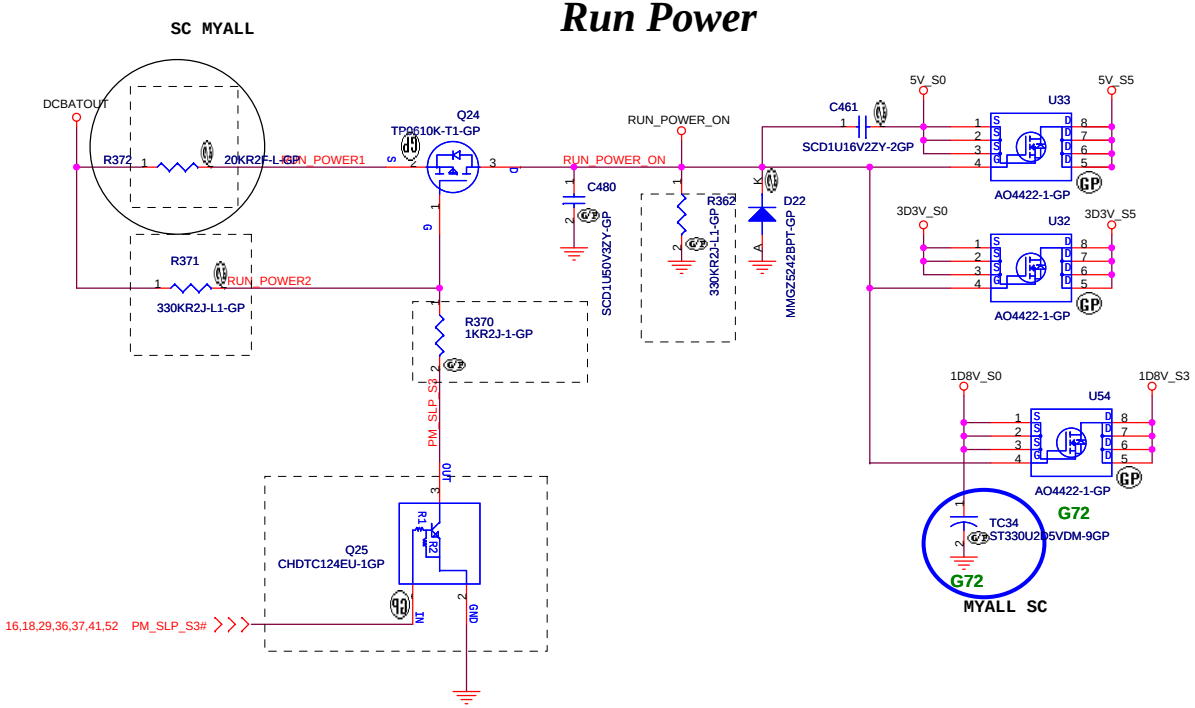
		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

<Core Design>

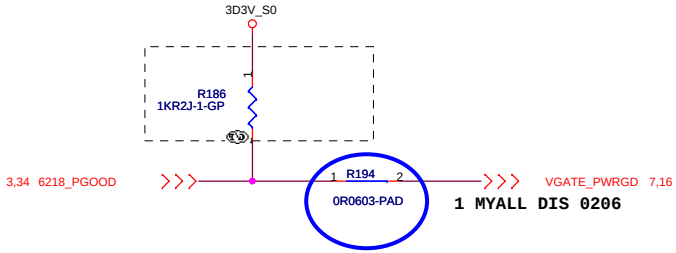
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS ROM
Size: A3
Document Number: MYALL
Rev: SA
Date: Friday, February 10, 2006
Sheet 31 of 52

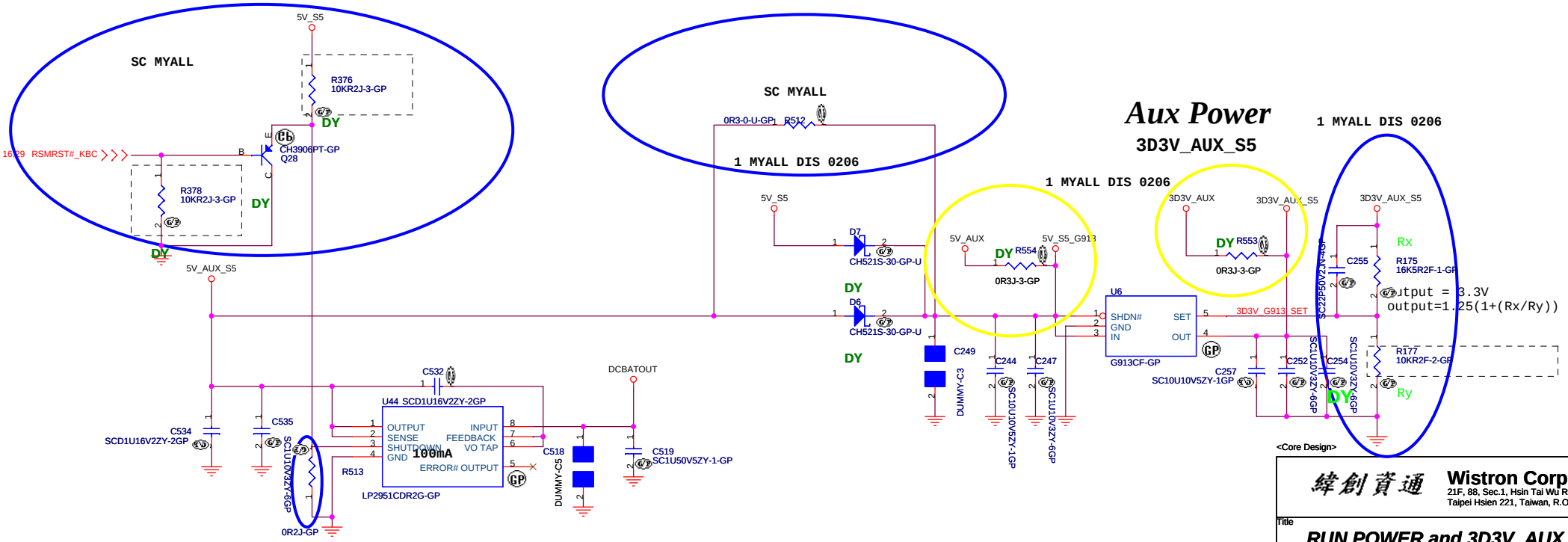
Run Power



PWRGD for NB and SB



PWRGD to Turn on CPU_Core_Power



Aux Power

3D3V_AUX_S5

1 MYALL DIS 0206

1 MYALL DIS 0206

<Core Design>

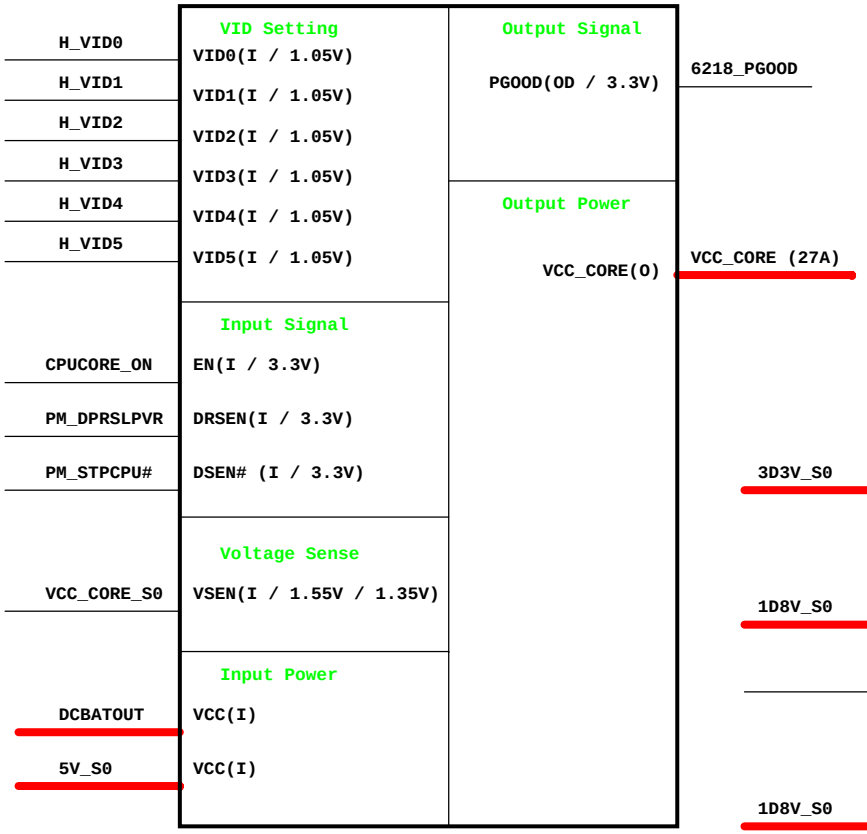
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

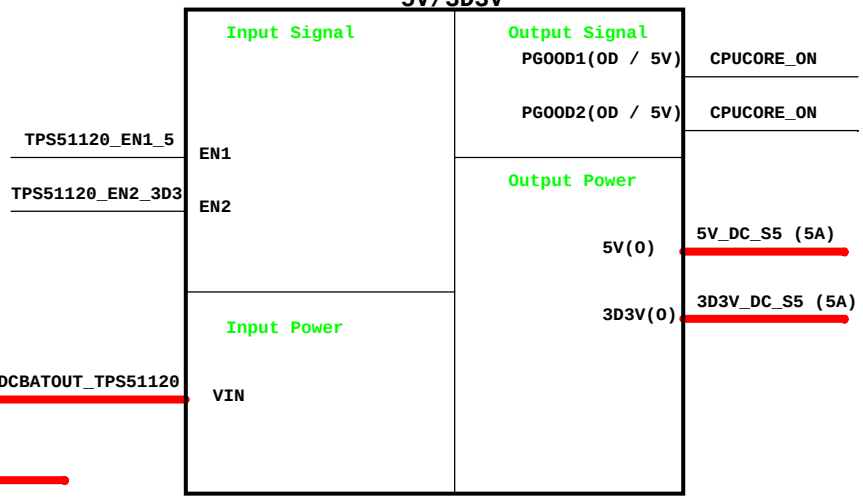
Size: A3 | Document Number: MYALL | Rev: SA

Date: Tuesday, February 14, 2006 | Sheet 32 of 52

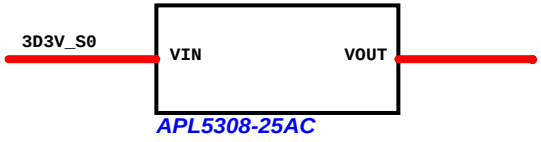
CPU_CORE ISL6218CV



TPS51120 5V/3D3V

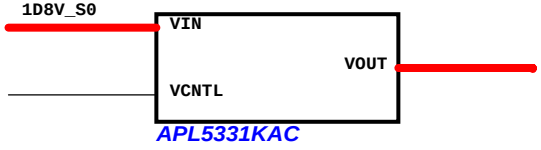


2D5V_S0



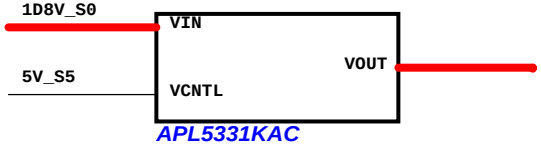
APL5308-25AC

1D5V_S0



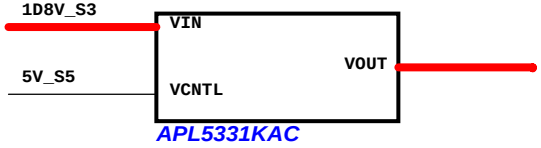
APL5331KAC

1D2V_S0



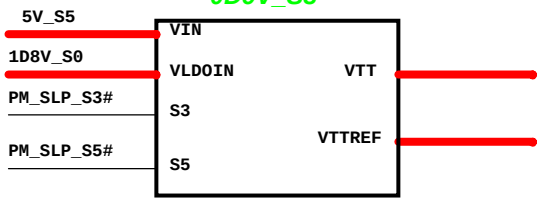
APL5331KAC

1D05V_S0



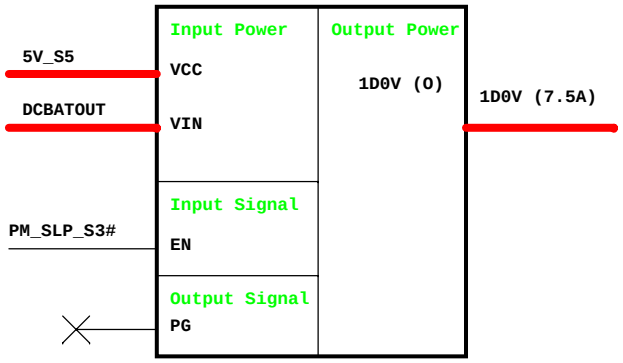
APL5331KAC

0D9V_S3

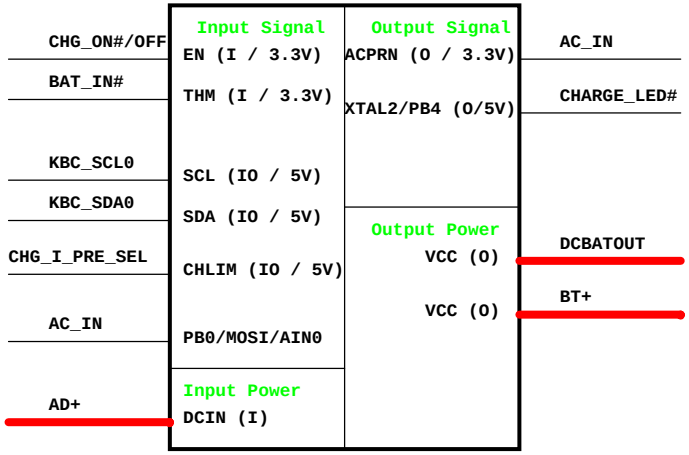


TPS51100

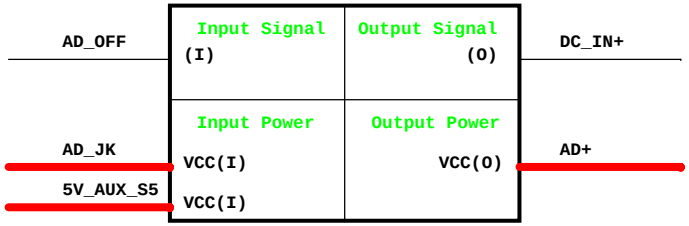
FAN5234_VGA_Core 1D0V or 1D20V



Charger_ISL6255



Adapter



<Core Design>

緯創資通 Wistron Corporation
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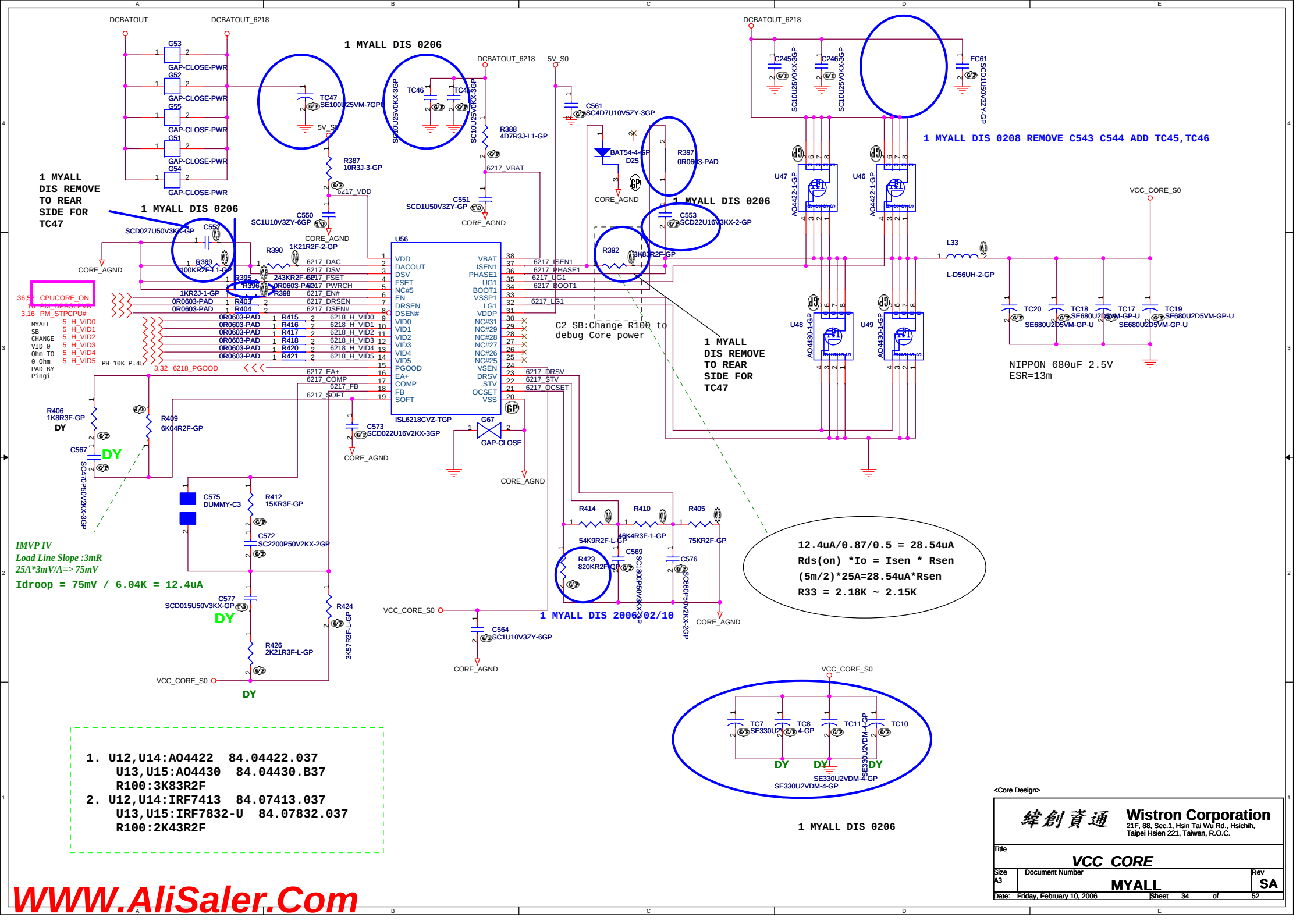
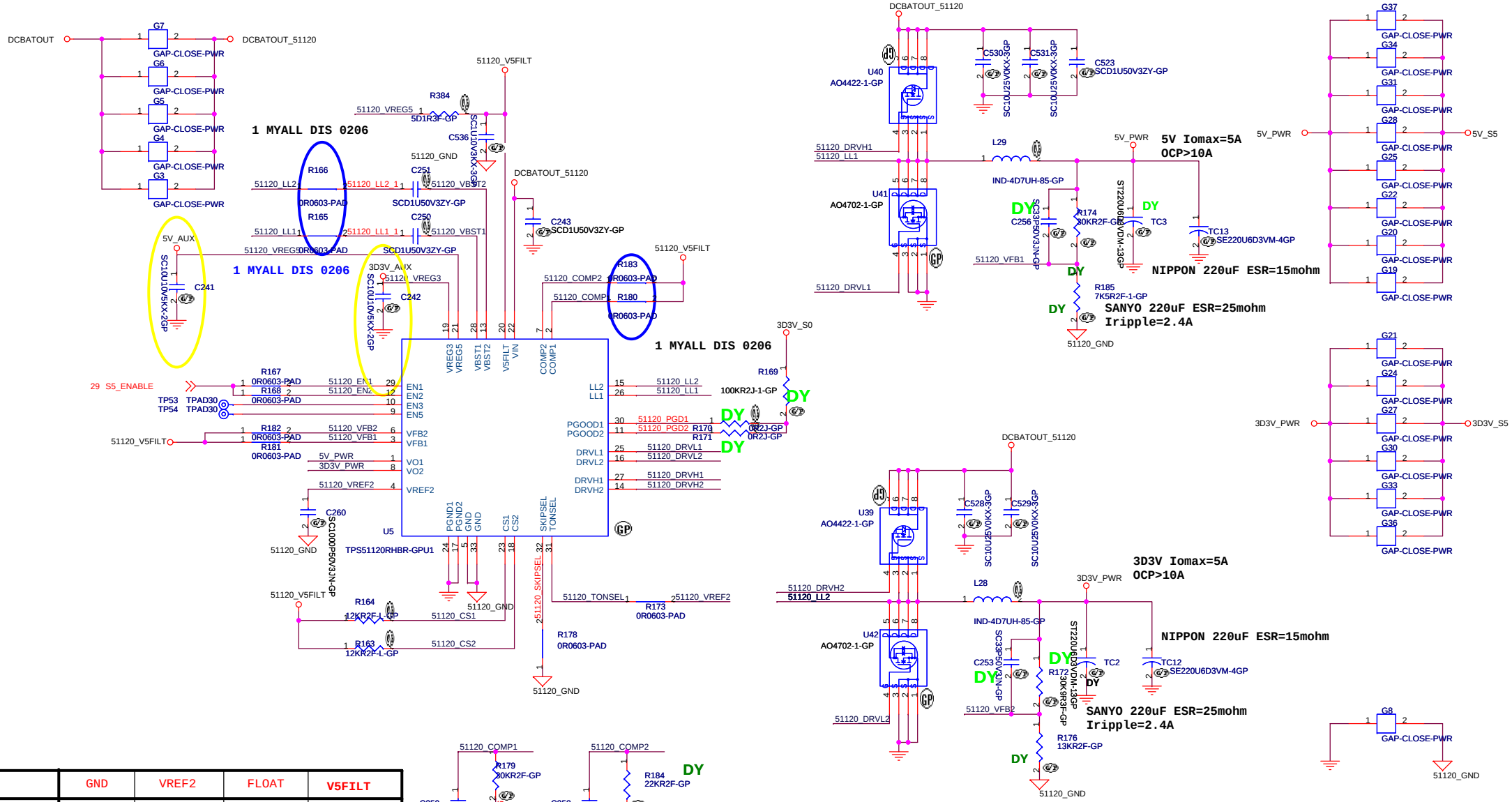
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Diagram**

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 33 of 52


1 MYALL DIS 0206
1 MYALL DIS REMOVE TO REAR SIDE FOR TC47
1 MYALL DIS 0208 REMOVE C543 C544 ADD TC45,TC46
C2_SB:Change R100 to debug Core power
NIPPON 680uF 2.5V ESR=13m
IMVP IV
Load Line Slope :3mR
25A*3mV/A=> 75mV
Idroop = 75mV / 6.04K = 12.4uA
12.4uA/0.87/0.5 = 28.54uA
Rds(on) *Io = Isen * Rsen
(5m/2)*25A=28.54uA*Rsen
R33 = 2.18K ~ 2.15K
1 MYALL DIS 20060202/10
ISL6218CVZ-TGP
1. U12,U14:AO4422 84.04422.037
U13,U15:AO4430 84.04430.B37
R100:3K83R2F
2. U12,U14:IRF7413 84.07413.037
U13,U15:IRF7832-U 84.07832.037
R100:2K43R2F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE
MYALL
SA
Friday, February 10, 2006
34
52
WWW.AliSaler.Com



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	**290k/CH1 440k/CH2**	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

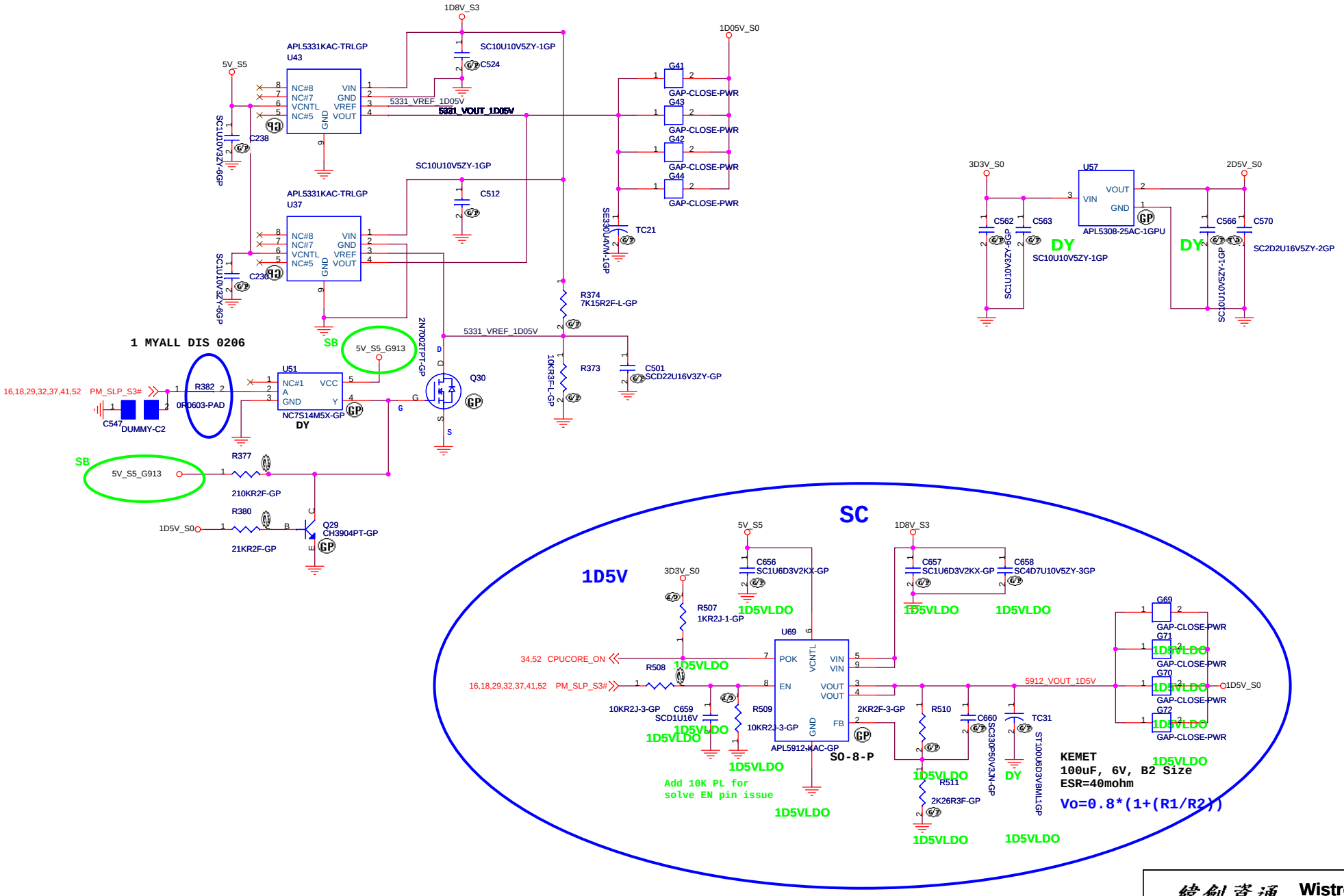
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120 / 3D3V / 5V**

Size	Document Number	Rev
A3	**MYALL**	SC

Date: Friday, February 10, 2006 Sheet 35 of 52

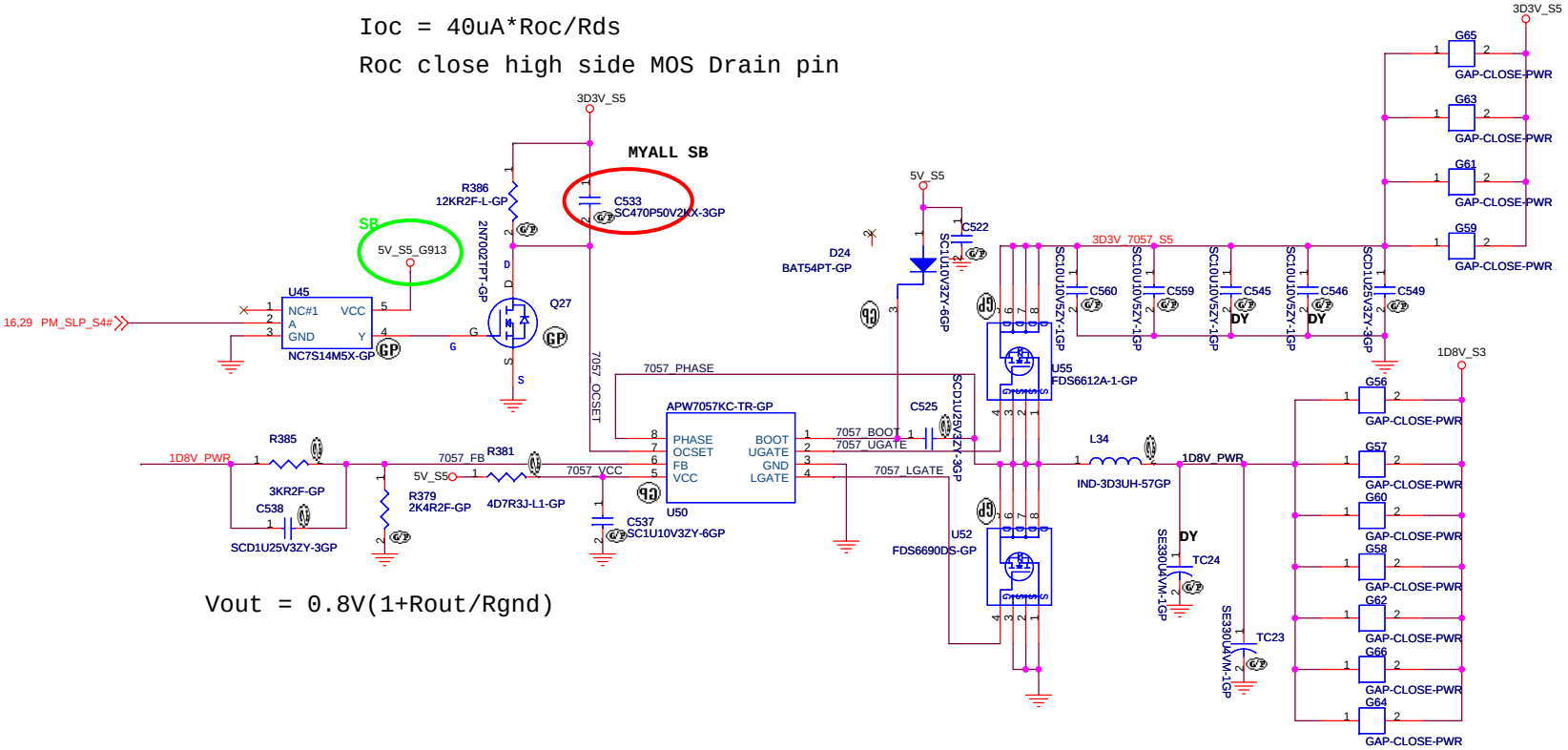


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	1D5V / 1D05V / 2D5V	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 36 of 52	

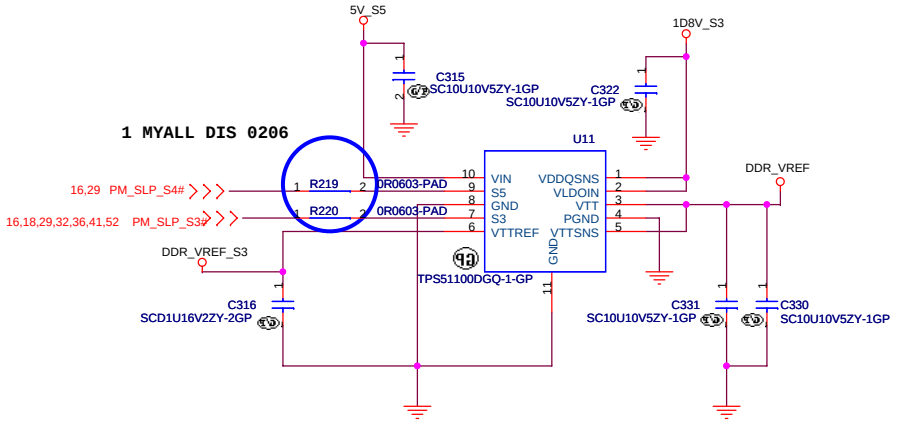
Ioc = 40uA*Roc/Rds

Roc close high side MOS Drain pin

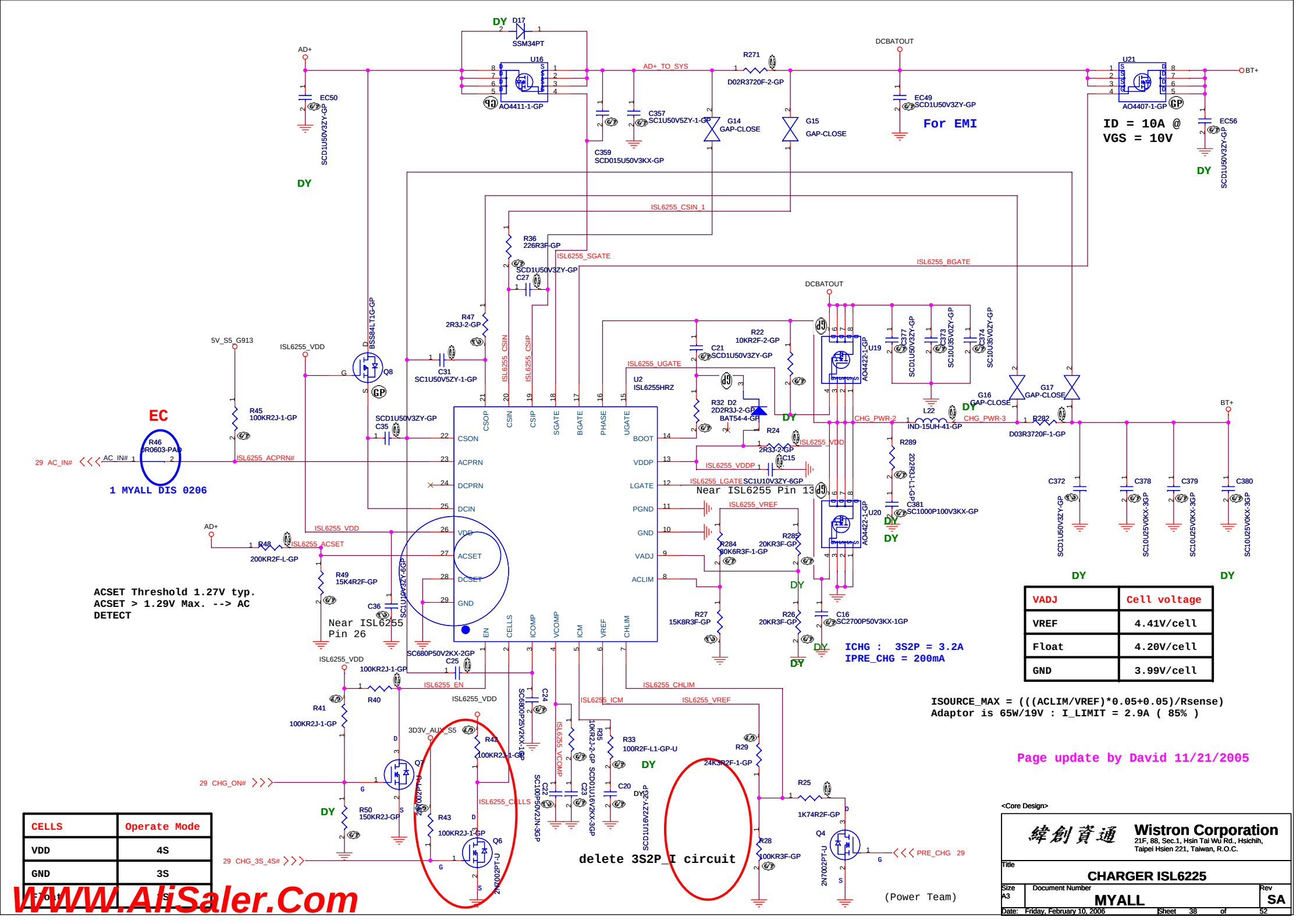


Vout = 0.8V(1+Rout/Rgnd)

0D9V



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**APW7057 / 1D8V/0D9V**	
Size: A3	Document Number: **MYALL**	Rev: SA
Date: Friday, February 10, 2006	Sheet 37 of 52	



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

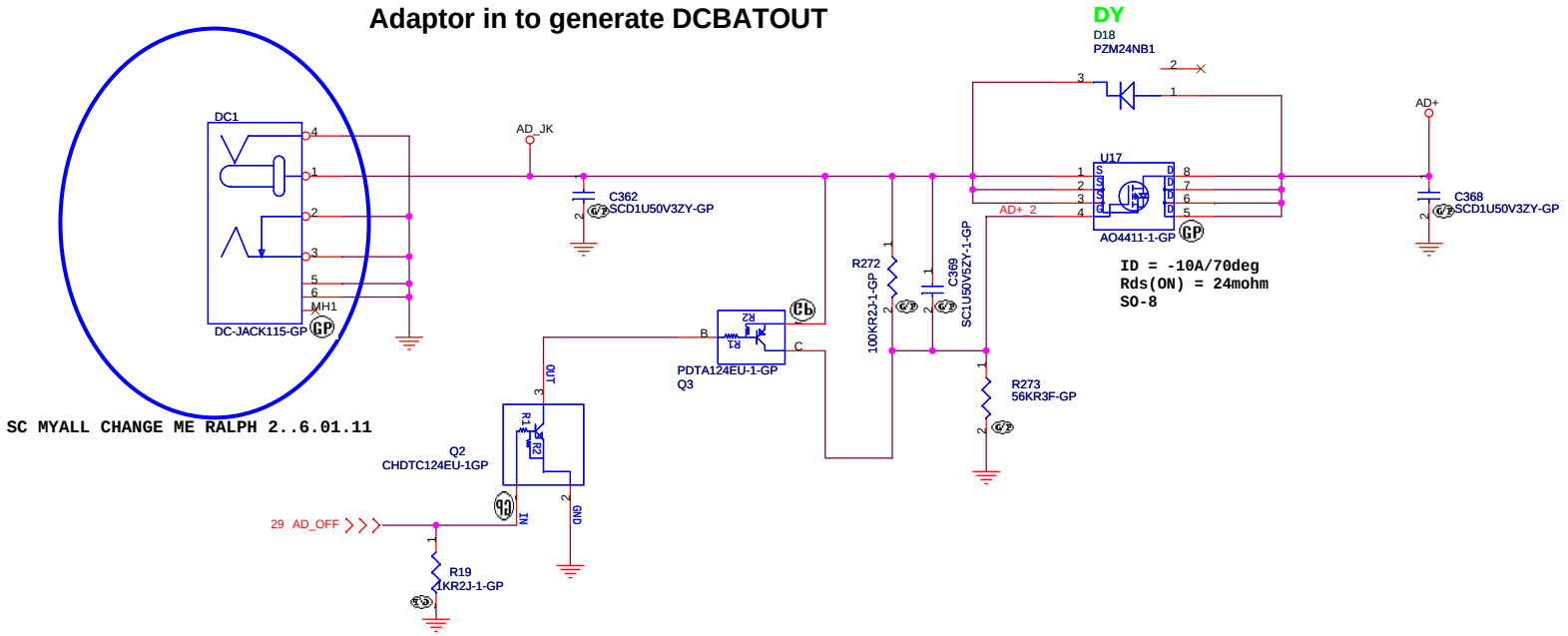
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

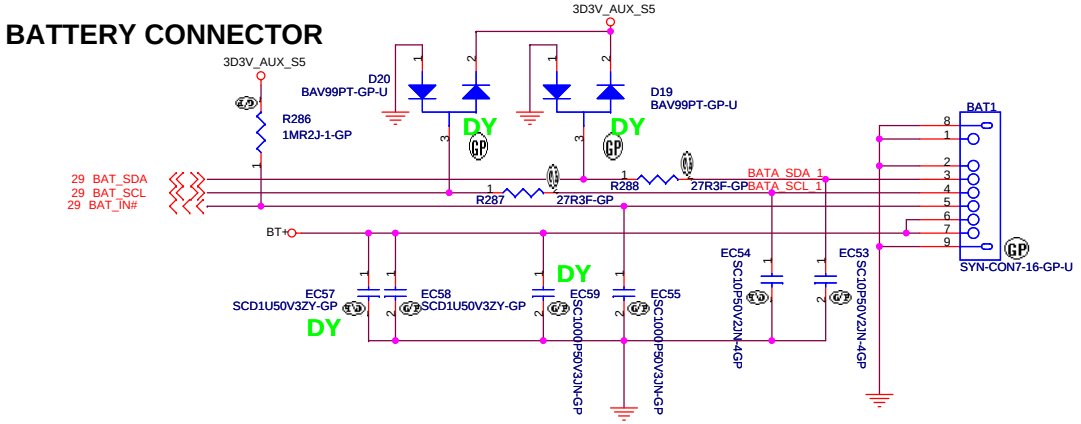
Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 38 of 52

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

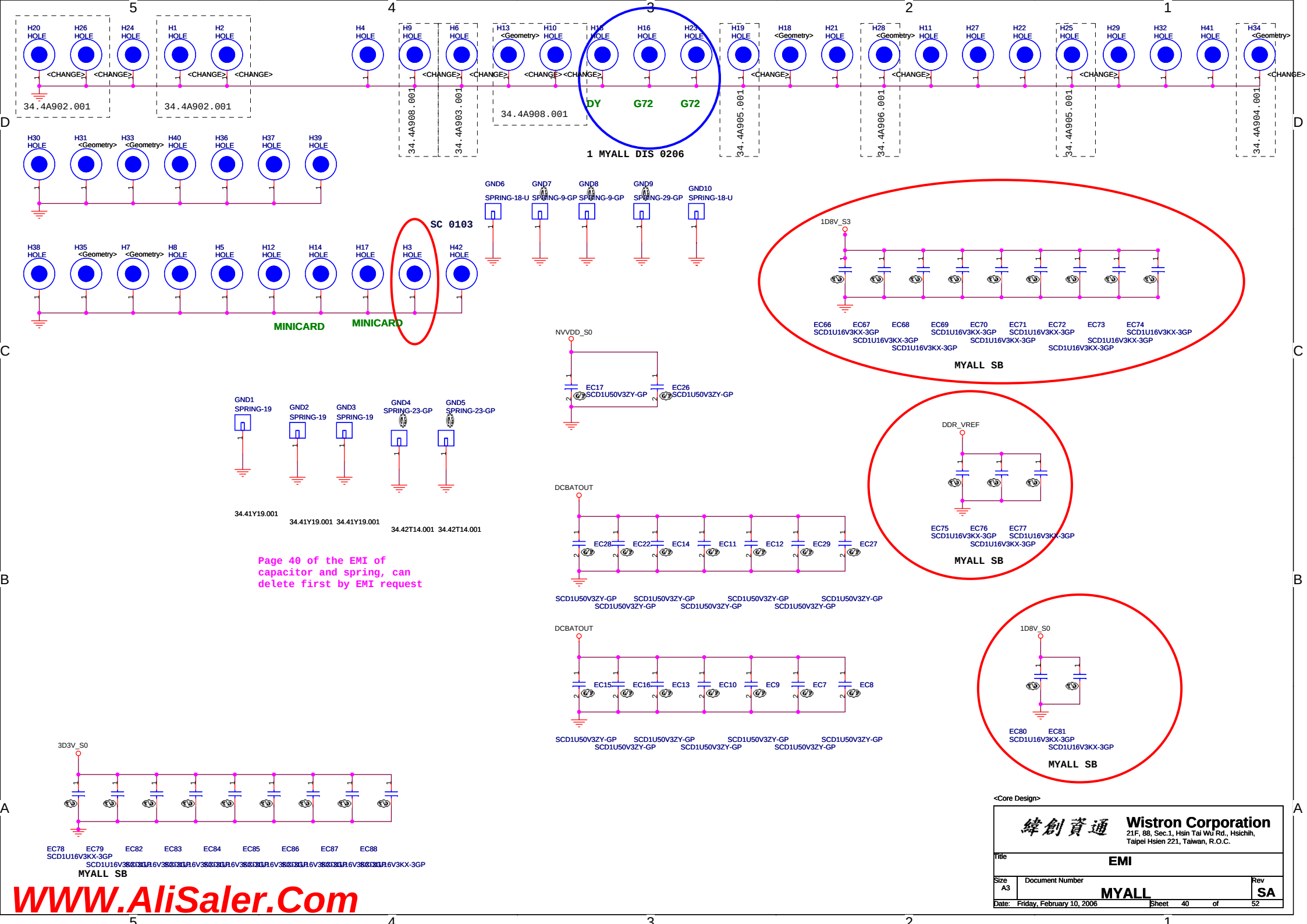


Page update by David 11/21/2005

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 39 of 52	



Page 40 of the EMI of capacitor and spring, can delete first by EMI request

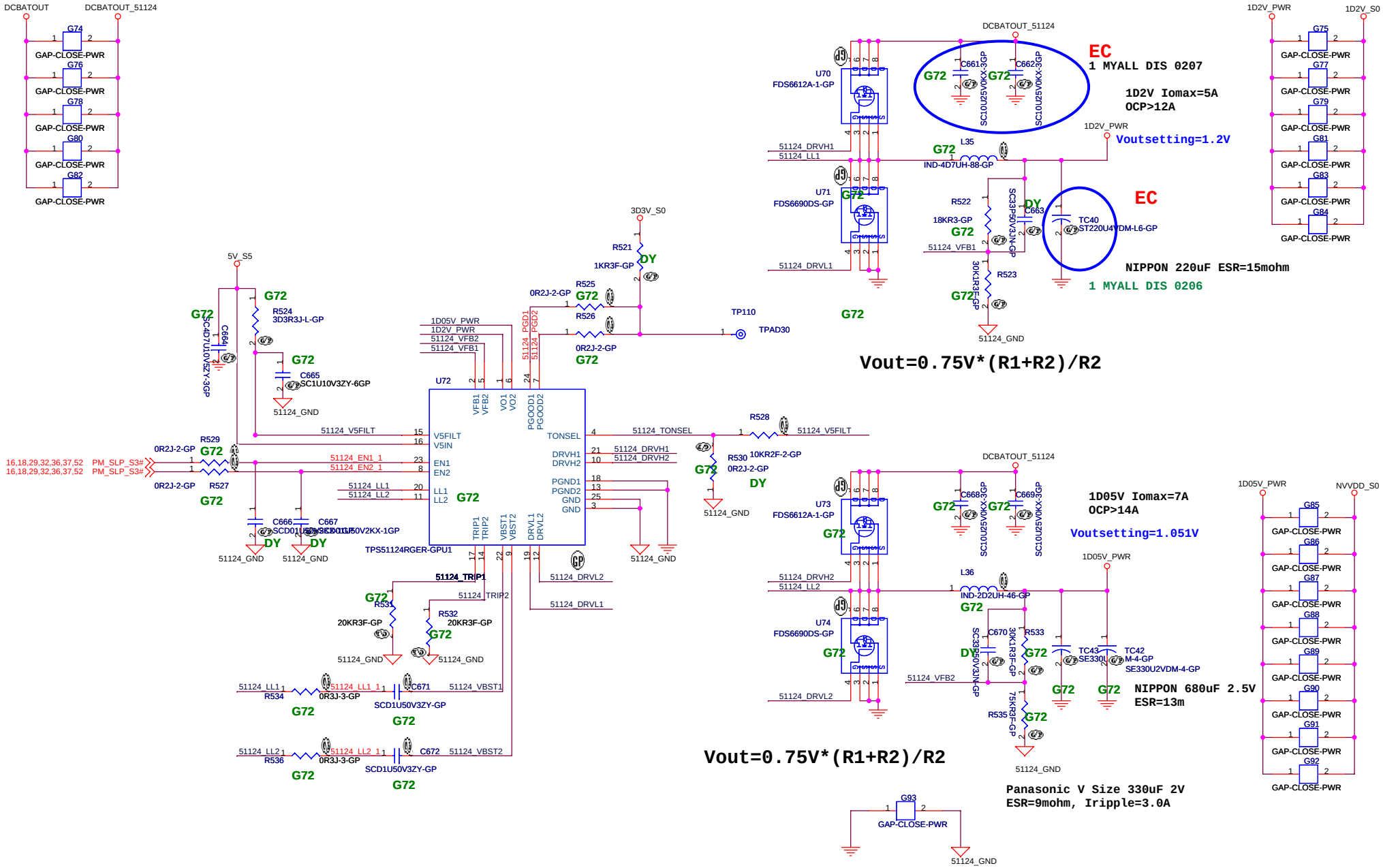
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 40 of 52



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

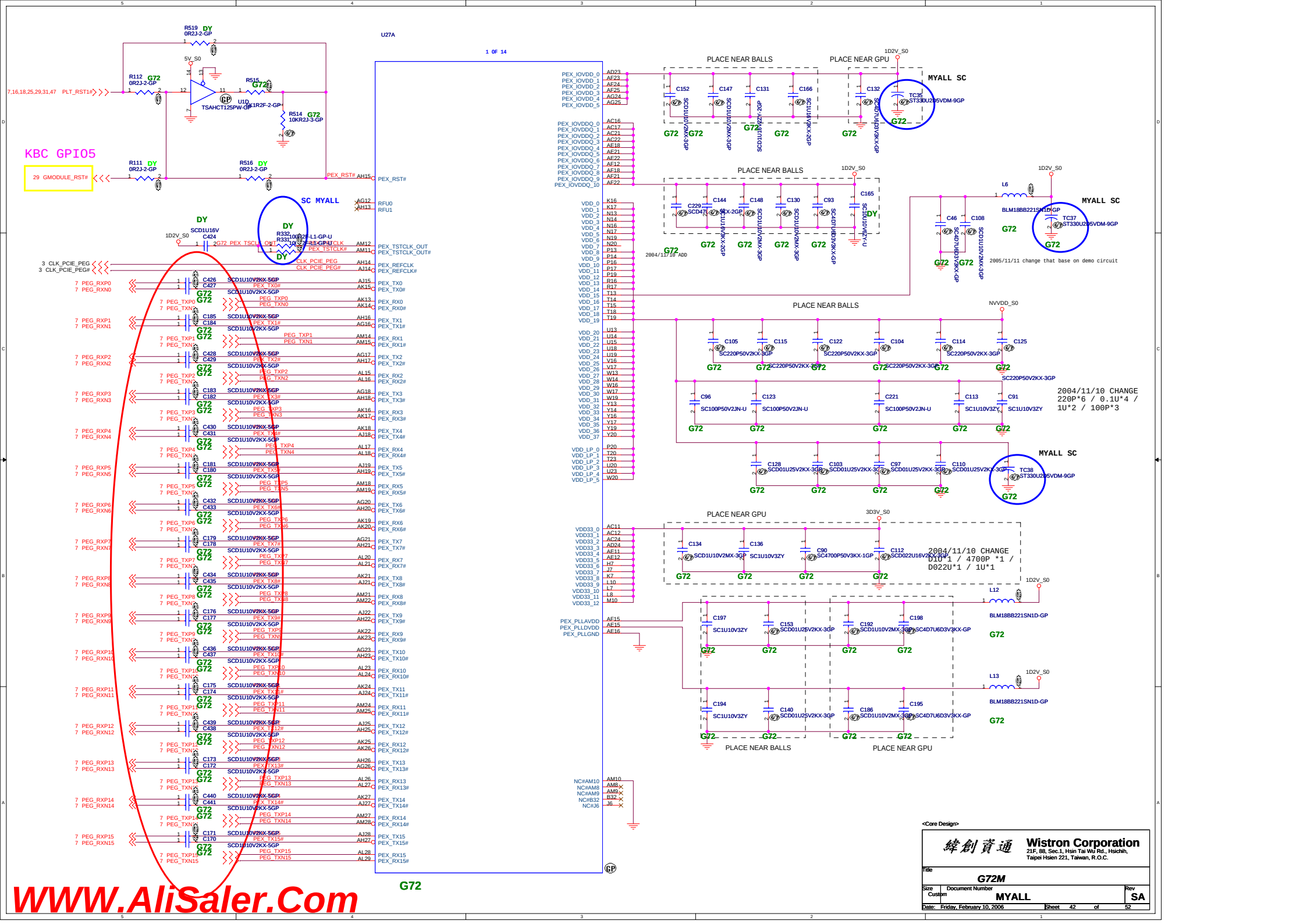
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 / NVDD/1D2V

Size	Document Number	Rev
A3	MYALL	SC

Date: Friday, February 10, 2006 Sheet 41 of 52


KBC GPIO5
29 GMODULE_RST#
7,16,18,25,29,31,47 PLT_RST1#
R519 DY 0R2J-2-GP
R112 G72 0R2J-2-GP
R515 G72 1K1R2F-2-GP
R514 G72 10KR2J-3-GP
R111 DY 0R2J-2-GP
R516 DY 0R2J-2-GP
U1D TSAHCT125PW-GP
5V_S0
U27A
1 OF 14
PEX_RST#
SC MYALL
DY
SCD1U16V
C424
R332 0R2J-L1-GP-U
R331 0R2J-L1-GP-U
PEX_TSCLK
PEX_TSTCLK#
CLK_PCIE_PEG
CLK_PCIE_PEG#
PEX_IOVDD_0
PEX_IOVDD_1
PEX_IOVDD_2
PEX_IOVDD_3
PEX_IOVDD_4
PEX_IOVDD_5
PLACE NEAR BALLS
PLACE NEAR GPU
1D2V_S0
MYALL SC
TC35 ST330U2V5VDM-9GP
C152
C147
C131
C166
C132
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SCD1U16V3KX-2GP
SCD1U10V3KX-GP
G72
PEX_IOVDD_6
PEX_IOVDD_7
PEX_IOVDD_8
PEX_IOVDD_9
PEX_IOVDD_10
C229
C144
C148
C130
C93
C165
SCD47U6D3V3KX-GP
SCD1U10V2MX-2GP
SCD1U10V2MX-3GP
SCD1U10V2MX-3GP
SC4D7U6D3V3KX-GP
SCD1U10V2ZY-U
DY
2004/11/10 ADD
L6
BLM18BB221SN1D-GP
TC37 ST330U2V5VDM-9GP
C46
C108
SCD47U6D3V3KX-GP
SCD1U10V2MX-3GP
2005/11/11 change that base on demo circuit
VDD_0
VDD_1
VDD_2
VDD_3
VDD_4
VDD_5
VDD_6
VDD_7
VDD_8
VDD_9
VDD_10
VDD_11
VDD_12
VDD_13
VDD_14
VDD_15
VDD_16
VDD_17
VDD_18
VDD_19
VDD_20
VDD_21
VDD_22
VDD_23
VDD_24
VDD_25
VDD_26
VDD_27
VDD_28
VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36
VDD_37
NVVDD_S0
C105
C115
C122
C104
C114
C125
SC220P50V2KX-3GP
C96
C123
C221
C113
C91
SC100P50V2JN-U
SC1U10V3ZY
2004/11/10 CHANGE
220P*6 / 0.1U*4 /
1U*2 / 100P*3
C128
C103
C97
C110
SCD01U25V2KX-3GP
TC38 ST330U2V5VDM-9GP
VDD_LP_0
VDD_LP_1
VDD_LP_2
VDD_LP_3
VDD_LP_4
VDD_LP_5
3D3V_S0
VDD33_0
VDD33_1
VDD33_2
VDD33_3
VDD33_4
VDD33_5
VDD33_6
VDD33_7
VDD33_8
VDD33_9
VDD33_10
VDD33_11
VDD33_12
C134
C136
C90
C112
SC1U10V3ZY
SC4700P50V3KX-1GP
SCD022U16V2KX-2GP
2004/11/10 CHANGE
D1U*1 / 4700P *1 /
D022U*1 / 1U*1
L12
BLM18BB221SN1D-GP
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
C197
C153
C192
C198
SC1U10V3ZY
SCD01U25V2KX-3GP
SCD1U10V2MX-3GP
SC4D7U6D3V3KX-GP
L13
BLM18BB221SN1D-GP
C194
C140
C186
C195
SC1U10V3ZY
SCD01U25V2KX-3GP
SCD1U10V2MX-3GP
SC4D7U6D3V3KX-GP
PLACE NEAR BALLS
PLACE NEAR GPU
NC#AM10
NC#AM8
NC#AM9
NC#B32
NC#J6
RFU0
RFU1
PEX_REFCLK
PEX_REFCLK#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_TX0
PEX_TX0#
PEX_RX0
PEX_RX0#
PEX_TX1
PEX_TX1#
PEX_RX1
PEX_RX1#
PEX_TX2
PEX_TX2#
PEX_RX2
PEX_RX2#
PEX_TX3
PEX_TX3#
PEX_RX3
PEX_RX3#
PEX_TX4
PEX_TX4#
PEX_RX4
PEX_RX4#
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PEX_TX5#
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PEX_TX11
PEX_TX11#
PEX_RX11
PEX_RX11#
PEX_TX12
PEX_TX12#
PEX_RX12
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PEX_RX13
PEX_RX13#
PEX_TX14
PEX_TX14#
PEX_RX14
PEX_RX14#
PEX_TX15
PEX_TX15#
PEX_RX15
PEX_RX15#
C426 C427 SCD1U10V2KX-5GP
C185 C184 SCD1U10V2KX-5GP
C428 C429 SCD1U10V2KX-5GP
C183 C182 SCD1U10V2KX-5GP
C430 C431 SCD1U10V2KX-5GP
C181 C180 SCD1U10V2KX-5GP
C432 C433 SCD1U10V2KX-5GP
C179 C178 SCD1U10V2KX-5GP
C434 C435 SCD1U10V2KX-5GP
C176 C177 SCD1U10V2KX-5GP
C436 C437 SCD1U10V2KX-5GP
C175 C174 SCD1U10V2KX-5GP
C439 C438 SCD1U10V2KX-5GP
C173 C172 SCD1U10V2KX-5GP
C440 C441 SCD1U10V2KX-5GP
C171 C170 SCD1U10V2KX-5GP
7 PEG_RXP0
7 PEG_RXN0
7 PEG_RXP1
7 PEG_RXN1
7 PEG_RXP2
7 PEG_RXN2
7 PEG_RXP3
7 PEG_RXN3
7 PEG_RXP4
7 PEG_RXN4
7 PEG_RXP5
7 PEG_RXN5
7 PEG_RXP6
7 PEG_RXN6
7 PEG_RXP7
7 PEG_RXN7
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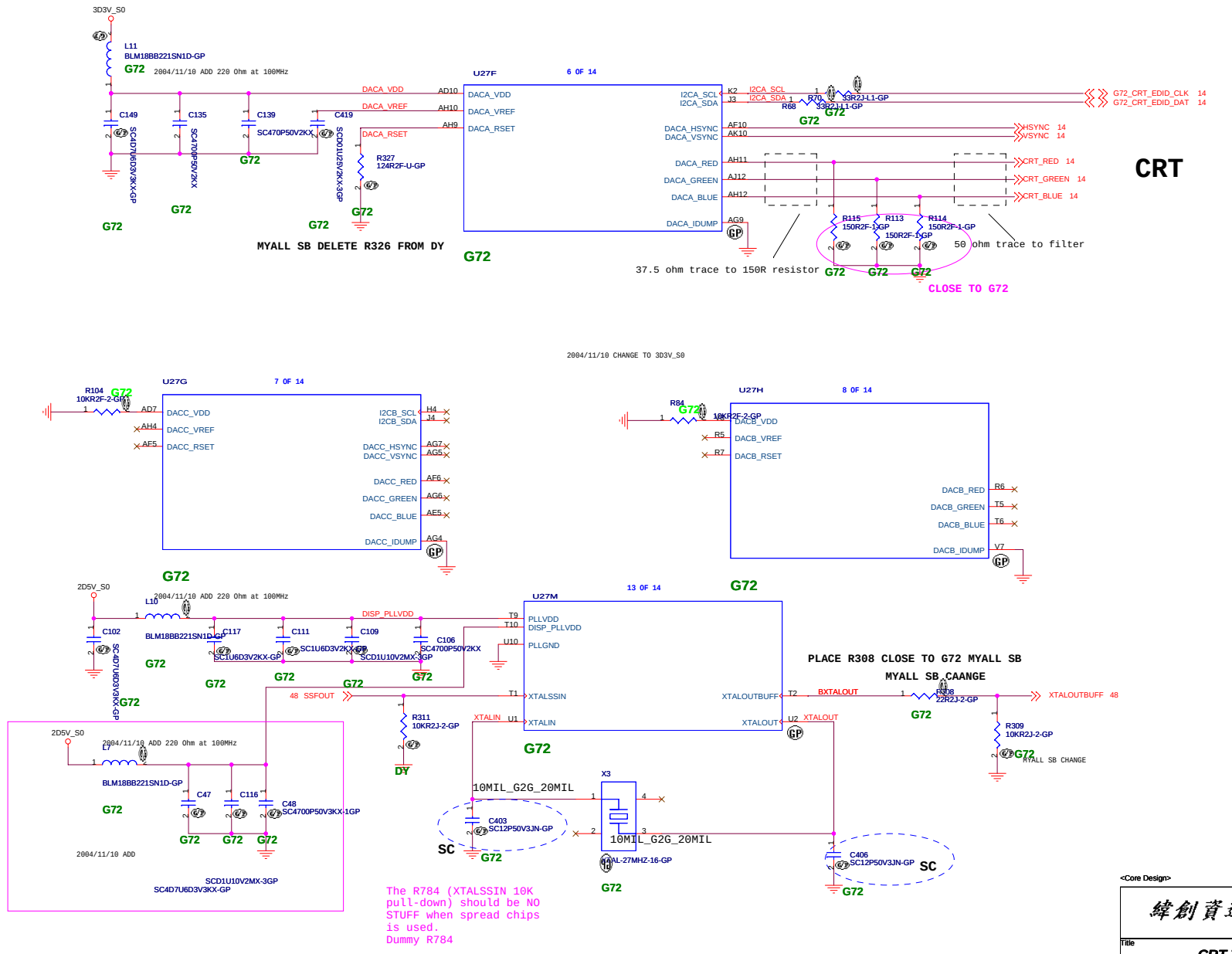
7 PEG_RXN8
7 PEG_RXP9
7 PEG_RXN9
7 PEG_RXP10
7 PEG_RXN10
7 PEG_RXP11
7 PEG_RXN11
7 PEG_RXP12
7 PEG_RXN12
7 PEG_RXP13
7 PEG_RXN13
7 PEG_RXP14
7 PEG_RXN14
7 PEG_RXP15
7 PEG_RXN15
3 CLK_PCIE_PEG
3 CLK_PCIE_PEG#
G72
WWW.AliSaler.Com
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G72M
Size Custom
Document Number MYALL
Rev SA
Date: Friday, February 10, 2006
Sheet 42 of 52



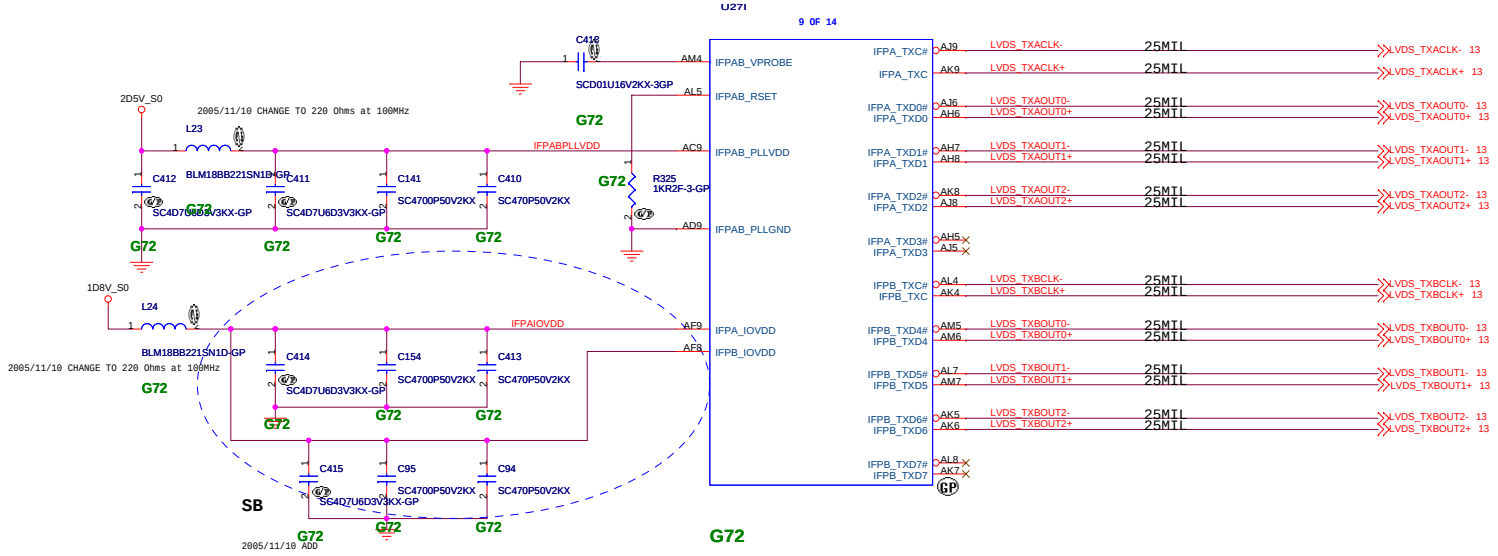
<Core Design>

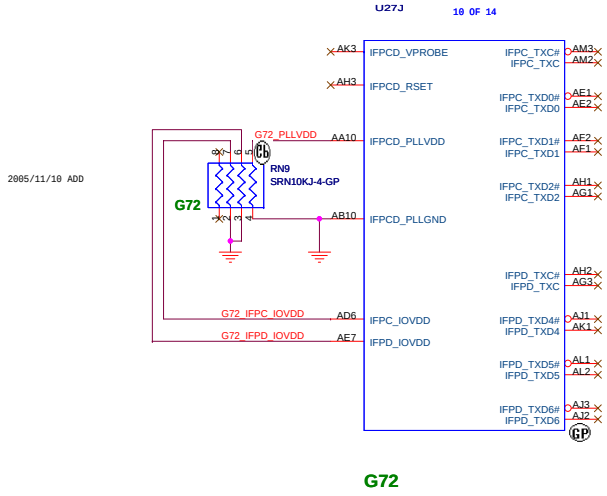
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT,TV OUT

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 43 of 52





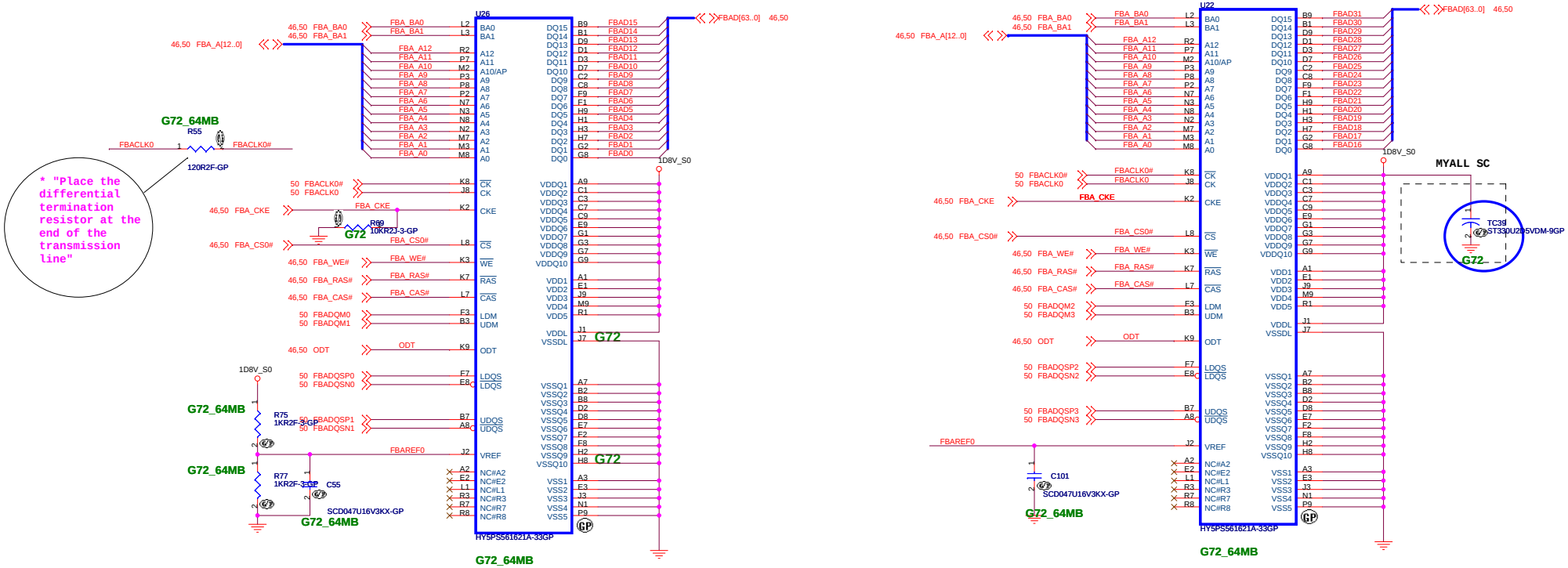
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

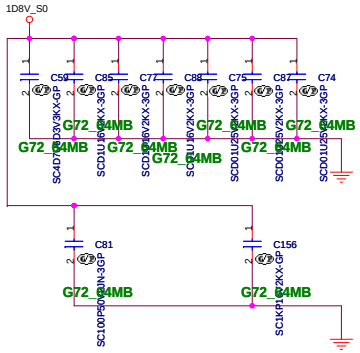
Title: LVDS,TMDS

Size: Custom | Document Number: MYALL | Rev: SA

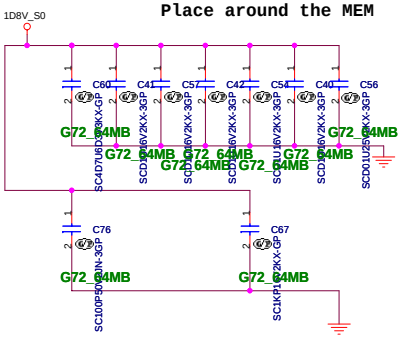
Date: Friday, February 10, 2006 | Sheet 44 of 52



Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



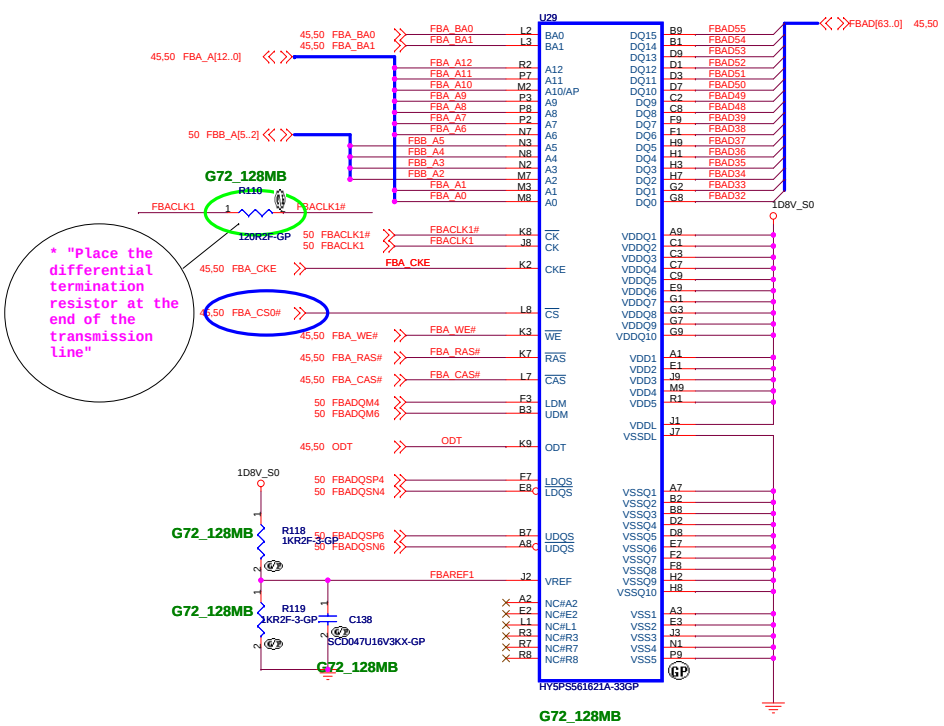
<Core Design>

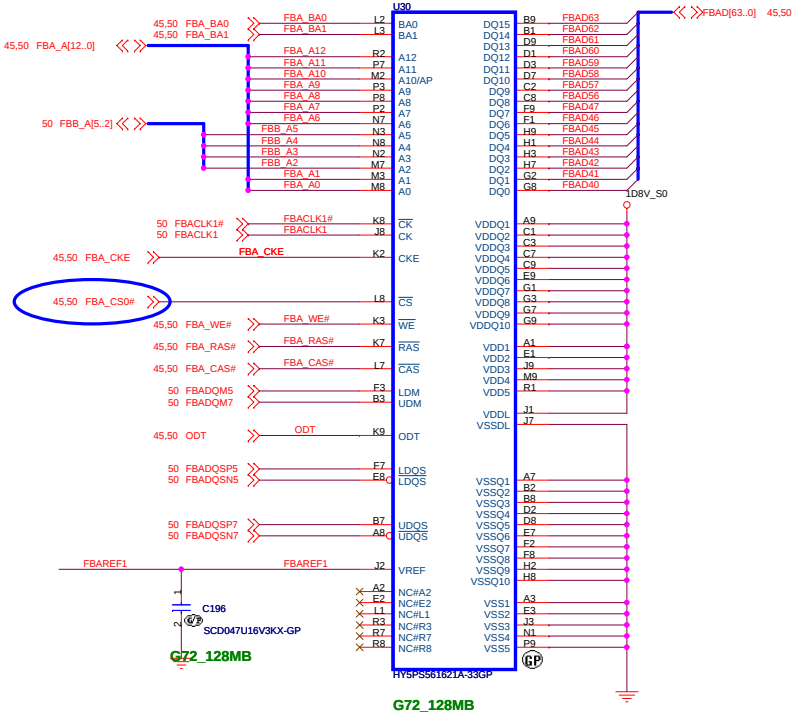
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM (1ST 1/2)

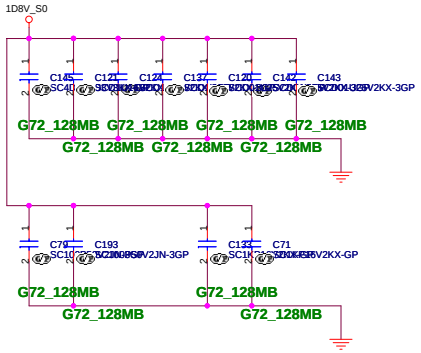
Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 45 of 52

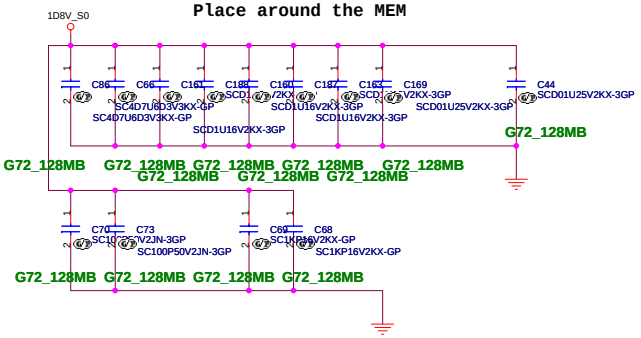




Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



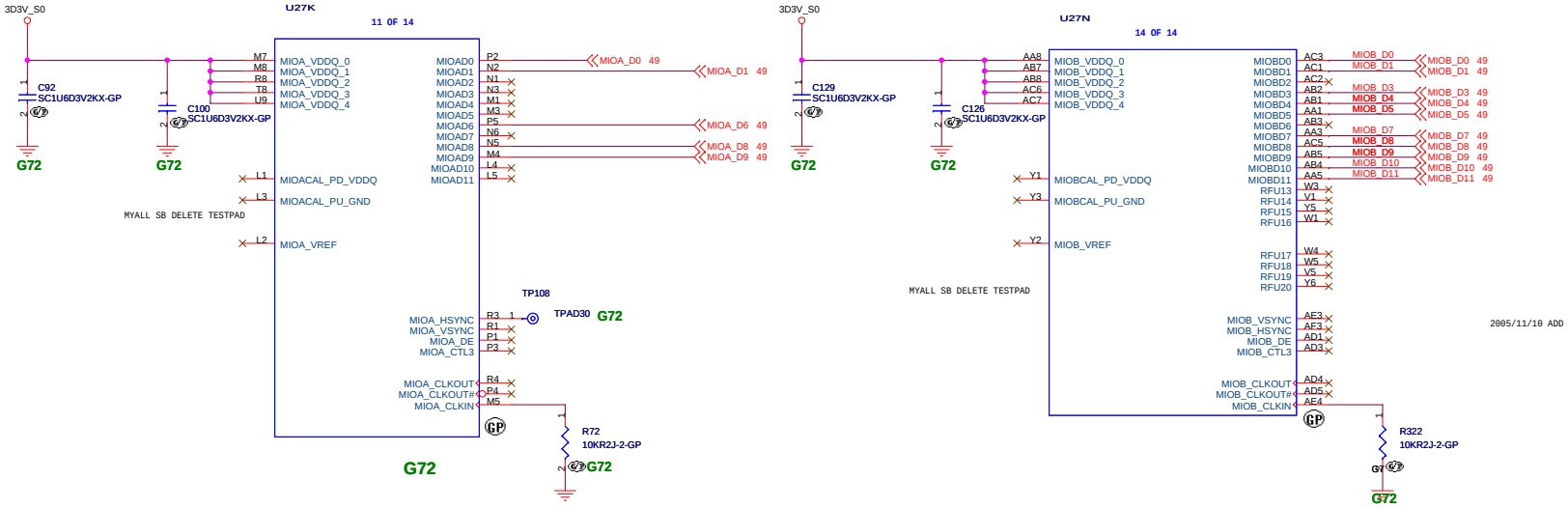
<Core Design>

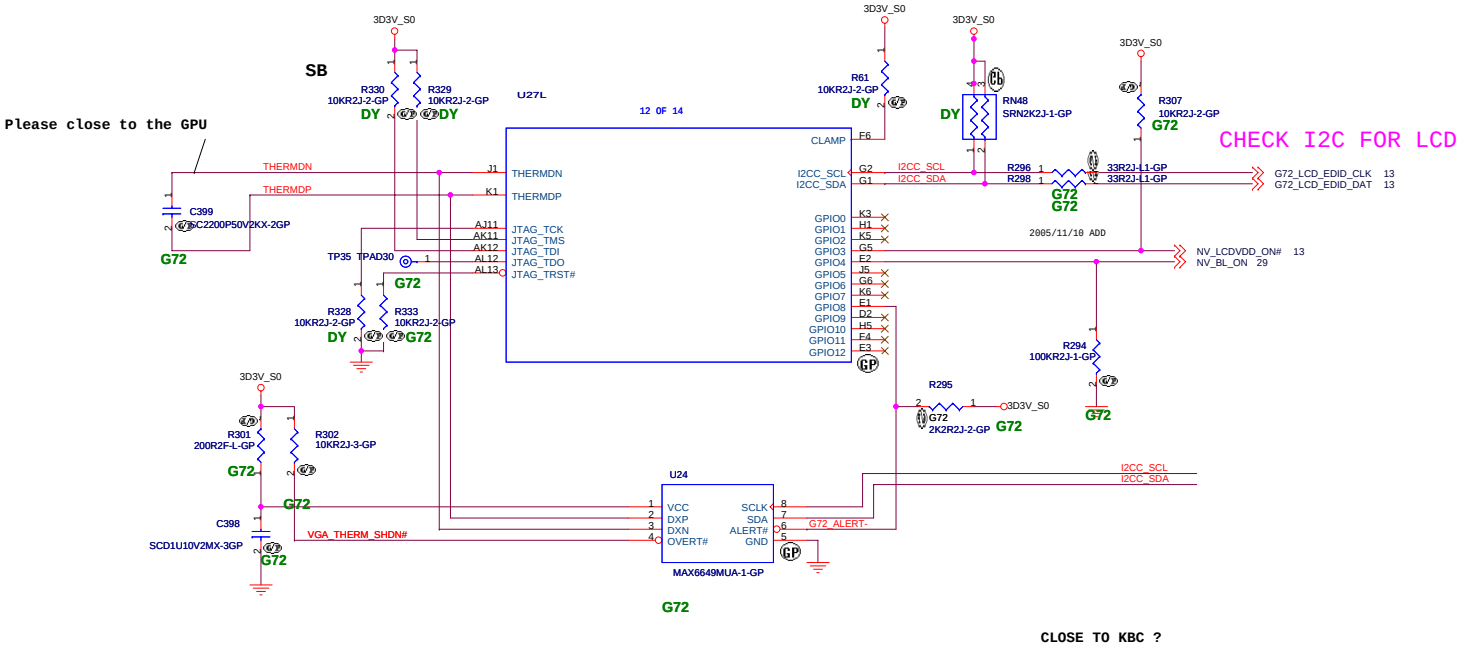
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM (1ST 2/2)

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 46 of 52





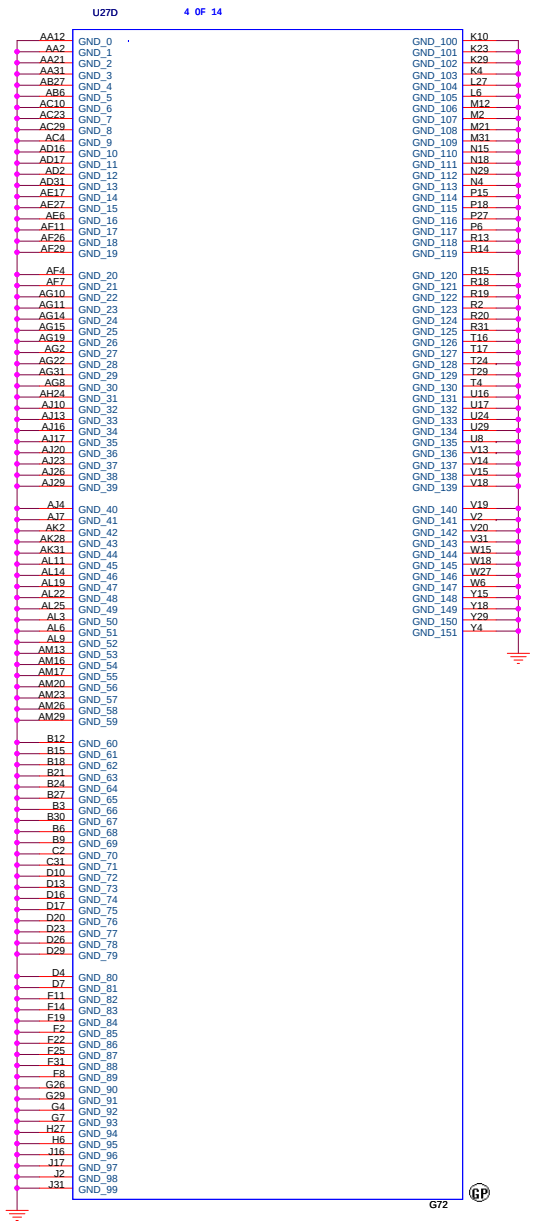
<Core Design>

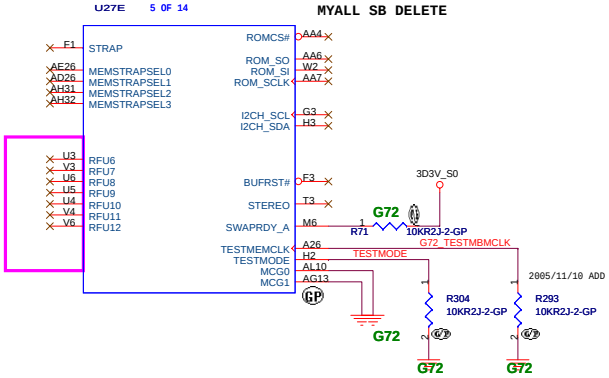
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

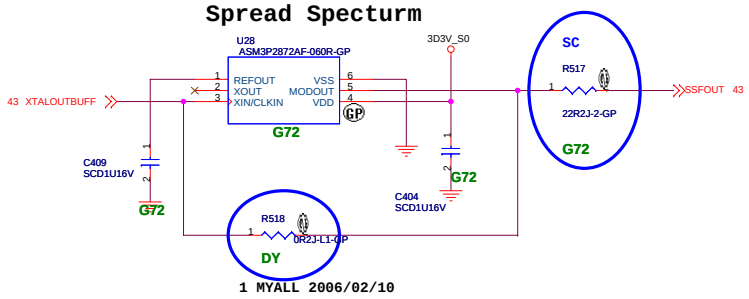
Title: ROM , Spread Specturm

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 47 of 52







<Core Design>

緯創資通 Wistron Corporation
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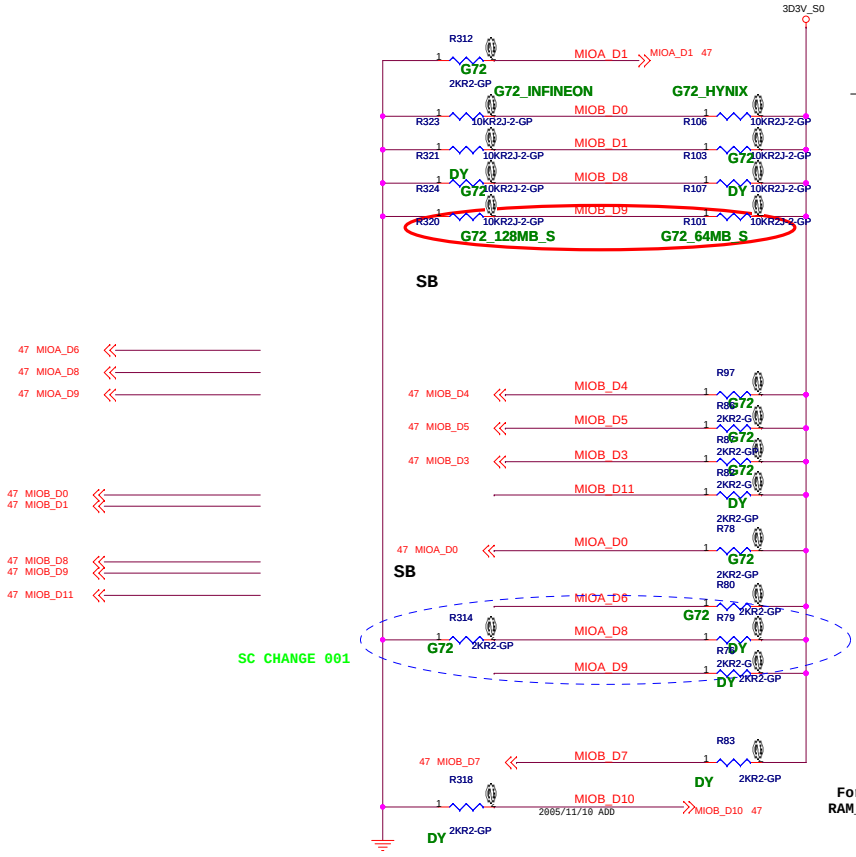
Taipei Hsien 221, Taiwan, R.O.C.

Title: ROM , Spread Specturm

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 48 of 52

STRAPS, Mechanical Parts



	Bit Signal	Values	
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS	
MIOB_D0: MIOB_D1: MIOB_D8: MIOB_D9:	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0000 RFU 0001 8Mx32 BGA 1.8V 0010 RFU 0011 RFU 0100 4Mx32 BGA 1.8V 0101 RFU 0110 RFU 0111 RFU 0011 16MX16	1000 RFU 1001 RFU 1010 RFU 1011 RFU 1100 RFU 1101 RFU 1110 RFU 1111 RFU
MIOB_D2: MIOB_D6:	CRYSTAL_0 CRYSTAL_1	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN	
MIOA_D7: MIOA_D10:	TV_MODE_0 TV_MODE_1	00 SECAM 01 NTSC 10 PAL 11 CRT	
MIOB_D4: MIOB_D5: MIOB_D3: MIOB_D11:	PCI_DEVID_0 PCI_DEVID_1 PCI_DEVID_2 PCI_DEVID_3	1000 (default 0x00FC) 0111 G72MV	
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED	
MIOA_D6: MIOA_D8: MIOA_D9:	3GIO_PADCFG_LUT_ADDR[0] 3GIO_PADCFG_LUT_ADDR[1] 3GIO_PADCFG_LUT_ADDR[2]	0 DESKTOP 1 MOBILE 010 DEFAULT	SC CHANGE 001
MIOB_D7:	MOBILE_GPIO	0 GPIO_PULLDN 1 GPIO_FLOAT	

For MEM strapping, Please use below table,

RAM_CFG[3:0]	Config	FB Bus Width	Definitions
0000	16Mx16 DDR2	64-bit	Elpida
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix

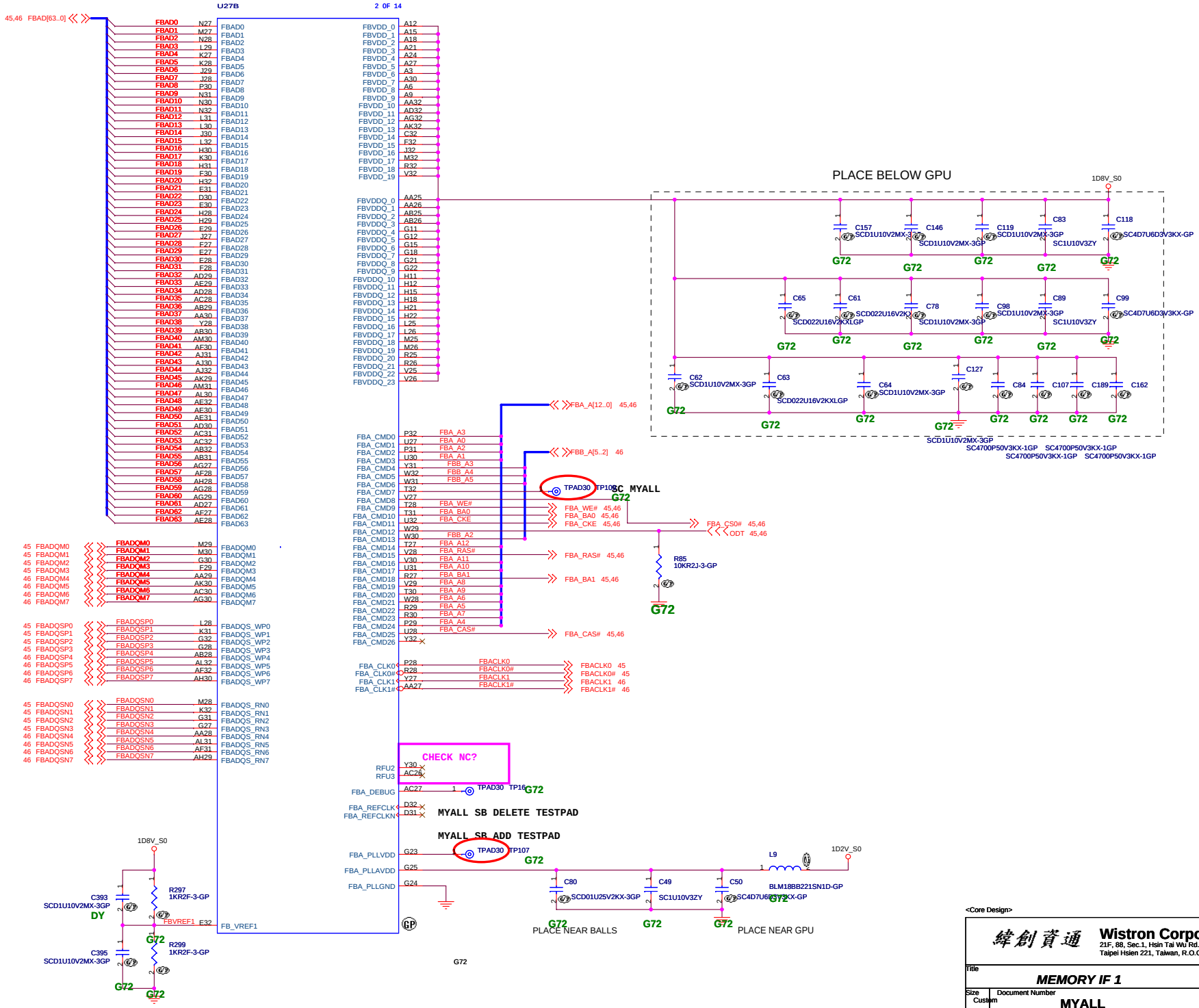
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ROM,Spread Specturn

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 49 of 52



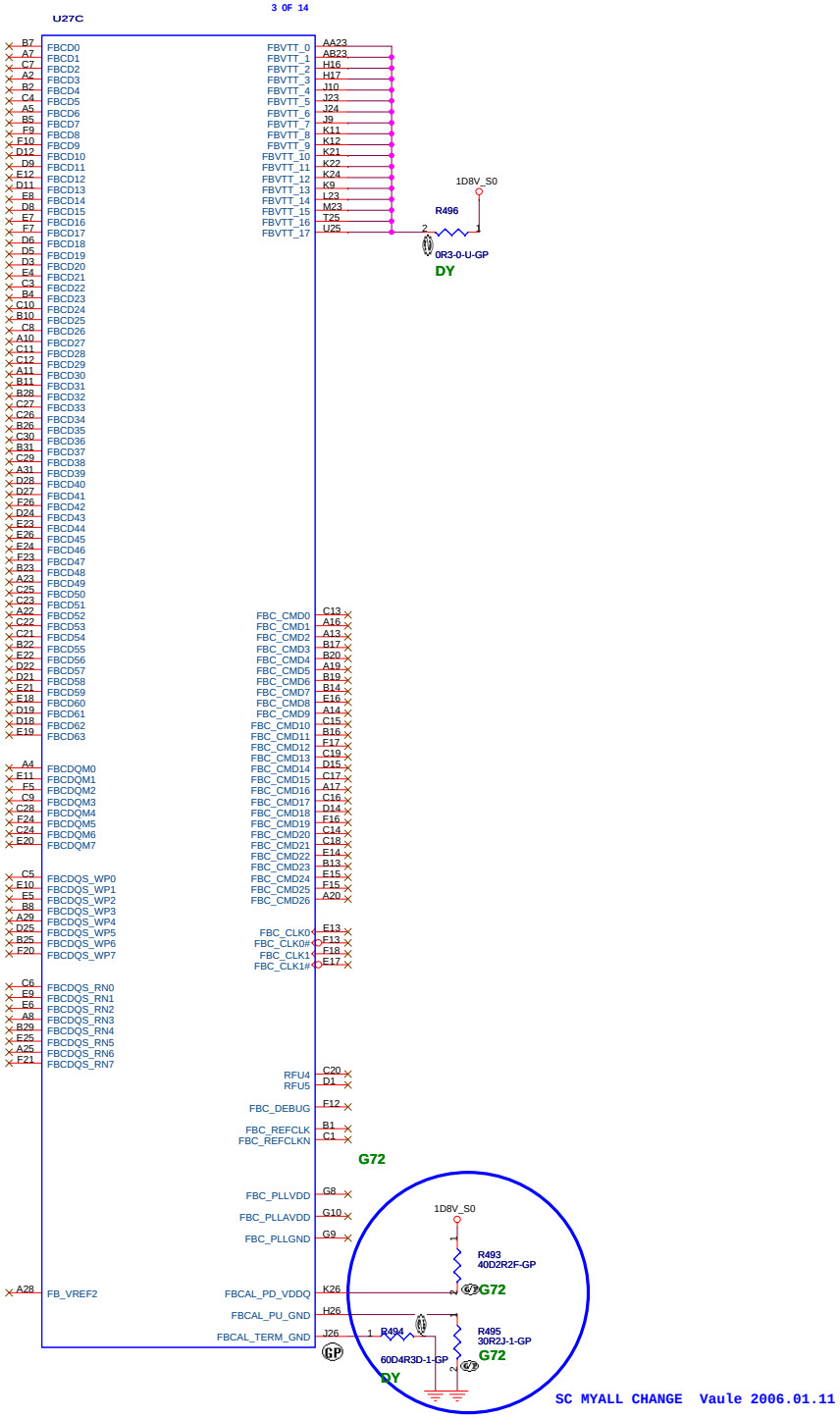
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEMORY IF 1

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 50 of 52



SC MYALL CHANGE Vaule 2006.01.11

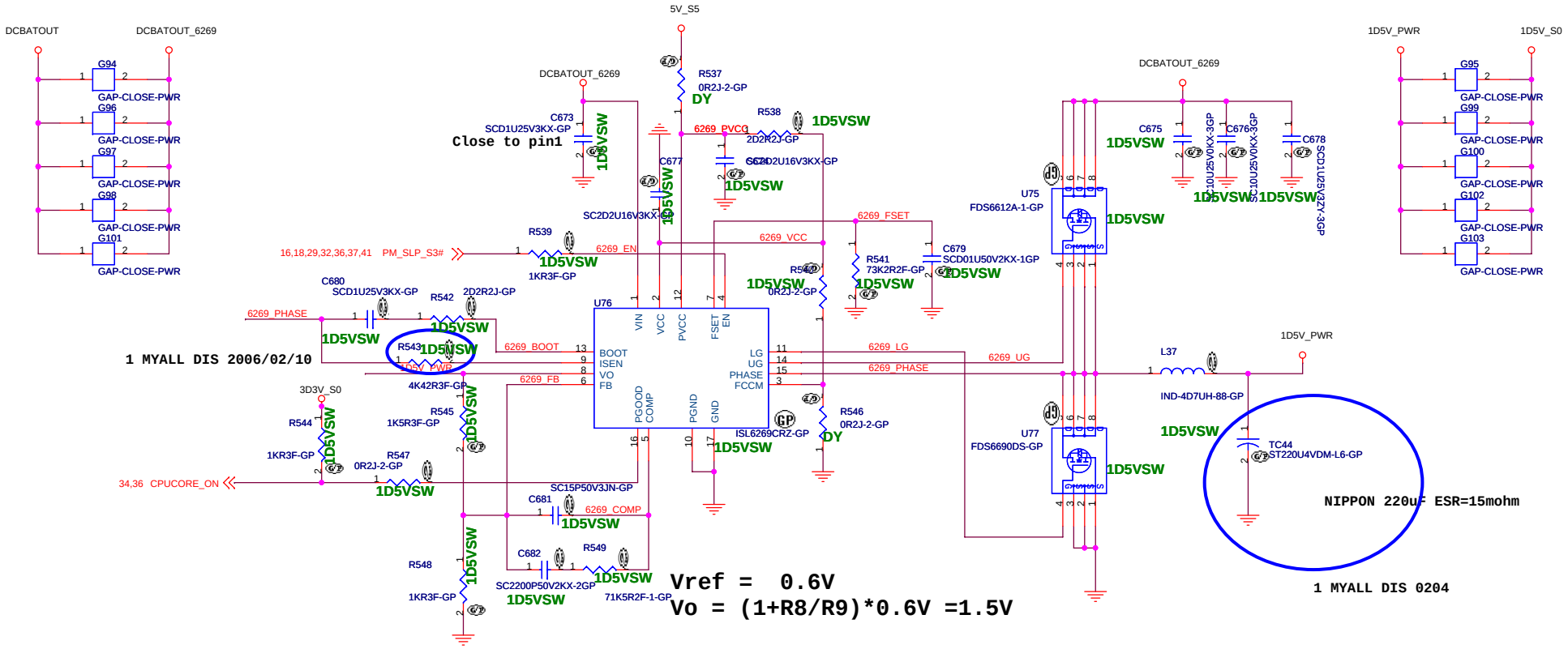
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEMORY IF 2

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 51 of 52



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ISL6269/1D5V**	
Size A3	Document Number **MYALL**	Rev SC
Date: Friday, February 10, 2006	Sheet 52 of 52	