IM3 (Jolie) Discrete 256M & UMA Block Diagram VER : 3A

POWER
- AC/BATT CONNECTOR PG 55
- BATT CHARGER PG 48

HybridSLI POWER
- VGA Core +1.1V_GFX PG 53
- REGULATOR For GDDR3 +1.8V_RUN PG 50
- HybridSLI SW +3.3V_NB9X/+1.8V_FBVDDQ/ +1.1V_GFX_PCIE PG 23

Dual Core CPU
Intel Penryn
(25W)
(478 Micro-FCPGA)
35 x 35 mm
PG 3,4

1066 MHz FSB

SYSTEM POWER
- MCP VR +MCP_CORE PG 50
- CPU VR +VCC_CORE/ +1.05V_VCCP PG 49,54
- REGULATOR For DDR3 +1.5V_DDR/ +0.75V_DDR_VTT PG 51
- REGULATOR +3.3V_ALW/+5V_SRC/ +15V_ALW PG 52
- RUN/SUS POWER SW +5V/+3.3V/+1.5V_RUN +3.3V_SUS PG 56
- LDO +1.1V_SUS PG 53
- LDO +1.1V_RUN PG 51

DDR3-SODIMM -A PG 15 — 1066 MHZ DDR-III
DDR3-SODIMM -B PG 16 — 1066 MHZ DDR-III

NVIDIA
MCP79MX
(1437 Pin PBGA)
35 x 35 mm
PG 5~14

LVDS x 1 Channel → **Panel** PG 26
VGA → **CRT CONN** PG 27
ML_LANE → **MUX/DeMUX Switch Texas SN75DP122** (56 Pin QFN) 8 x 8 mm PG 28
- HDMI → **HDMI Connector** PG 29
- DP → **Display Port** PG 29

PCIEx16 → **NVIDIA GPU NB9M-GE(GB1-64)** (533 BGA) 23 x 23 mm PG 17~23
- **Frame Buffer 32Mx32 Bit x 2** (136 FBGA) 11 x 14 mm
- **GDDR3 256MB** PG 24,25

PCI-E / USB2.0 → **WLAN MINI-CARD Half size** PG 32
PCI-E / USB2.0 → **WWAN MINI-CARD** PG 33
PCI-E / USB2.0 → **UWB/BT MINI-CARD** PG 33
PCI-E / USB2.0 → **Express Card** PG 34 → **Express Switch RICOH R5538D001** (20 QFN) 4 x 4 mm PG 34

RGMII → **PHY Broadcom B5071A2KFBG** (100 BGA) 9 x 9 mm PG 45 → **Magnetic** PG 46 → **RJ45** PG 46

AUDIO IDT 92HD73C (56 LQFP) 9 x 9 mm PG 42 — IHDA
- **Audio Jack -HP1** PG 44 ← **Amplifier Texas TPA4411MRTJR** (20 Pin QFN) PG 43
- **Audio Jack -MIC** PG 44
- **Audio Jack -HP2** PG 44 ← **Amplifier Texas TPA6040A4** (32 Pin QFN) PG 43
- **Internal Speaker** PG 38

- **WebCam+DMIC** PG 38 — USB2.0
- **Fingerprint** PG 38 — USB2.0
- **USB CONN -Left** PG 30 — USB2.0 x 2
- **eSATA/USB COMBO CONN** PG 30 — USB2.0
- **SATA - ODD** PG 31 — SATA2
- **SATA - HDD** PG 31 — SATA2
- 33MHz PCI

PC Card/1394 RICOH R5C833T (128 Pin TQFP) 14 x 14 mm PG 40,41
- **1394 CONN** PG 41
- **CardReader CONN** PG 41

LPC

SIO ITE
ITE8512E
(128 Pin LQFP)
16 x 16 mm
PG 36

SPI → **FLASH Memory SPI, 2MB** (8 Pin SO8W) PG 37

PS/2
- **K/B, CCD, D/B connector** PG 38
- **CIR** PG 37
- **Touchpad** PG 38

GPU THERMAL ADM1032
GPU SS Clock PG1819G-08SR PG 19

CPU Thermal & FAN SMSC1423 (10 TSSOP) 3 x 3 mm PG 35

QUANTA COMPUTER

Title	Schematic Block Diagram	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 1 of 59	

INDEX

Power States

Power Rail	Control Signal	S0	S3	S4	S5	G3
+PWR_SRC	N/A	V	V	V	V	
+0.75V_DDR_VTT	RUN_ON	V				
+1.05V_VCCP	CPUVDD_EN	V				
+1.1V_GFX	+3.3V_NB9X	V				
+1.1V_GFX_PCIE	MXM_PWR_EN	V				
+1.1V_RMGT	SLP_RMGT#	V	V			
+1.1V_RUN	RUN_ON	V				
+1.1V_SUS	+3.3V_SUS	V	V			
+1.5V_RUN	RUN_ON	V				
+1.5V_DDR	SIO_SLP_S5#	V	V			
+1.8V_FBVDDQ	NB9_CORE_PWRGD	V				
+1.8V_RUN	RUN_ON	V				
+15V_ALW	+5V_ALW	V	V			
+3.3V_ALW	+5V_ALW2	V	V	V	V	
+3.3V_NB9X	MXM_PWR_EN	V				
+3.3V_RMGT	SLP_RMGT#	V	V			
+3.3V_RUN	RUN_ON	V				
+3.3V_SUS	SUS_ON	V	V			
+5V_ALW	5V_ALW_ON	V	V			
+5V_ALW2	+PWR_SRC	V	V	V	V	
+5V_HDD	HDDC_EN	V				
+5V_MOD	MODC_EN	V				
+5V_RUN	RUN_ON	V				
+GFX_PWR_SRC	RUN_ON	V				
+LCDVCC	EN_LCDVCC	V				
+MCP_CORE	RUN_ON	V				
+NB9_CORE	+3.3V_NB9X	V				
+RTC_CELL	N/A	V	V	V	V	V
+VCC_CORE	1.05V_VCCP_PWRGD	V				
+USB_RIGHT_PWR	USB_SIDE_EN#	V	V			
+USB_LEFT_PWR	USB_BACK_EN#	V	V			

QUANTA COMPUTER

Title	Index & Power Status	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 2 of 59	

Layout Note: Keep 12 mils spacing and near CPU.

0701_Michael:NV review, depop R103 for B02

Layout Note: Place R380 close to CPU.

0604_Michael:Depop pull-up R380 on H_RESET#

Layout Note: Place voltage divider within 0.5" of GTLREF pin

1022_Michael:Remove H_THERMTRIP connector to MCP79

Note: H_DPRTSTP need to daisy chain from ICH8 to IMVP6 to CPU.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Populate ITP700Flex for bringup

Layout Note: Place couple 0.1uF Decoupling caps with in 0.1" ITP connector.

Layout Note: Place R7000,R7411, R7409, R7410, R7387 , R7386 close to CPU

CPU THERMTRIP Circuit

1022_Michael:Add R355 for voltage low issue

0823_Michael:Follow RM2 to change CPU THERMTRIP circuit

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

ITP disable guidelines

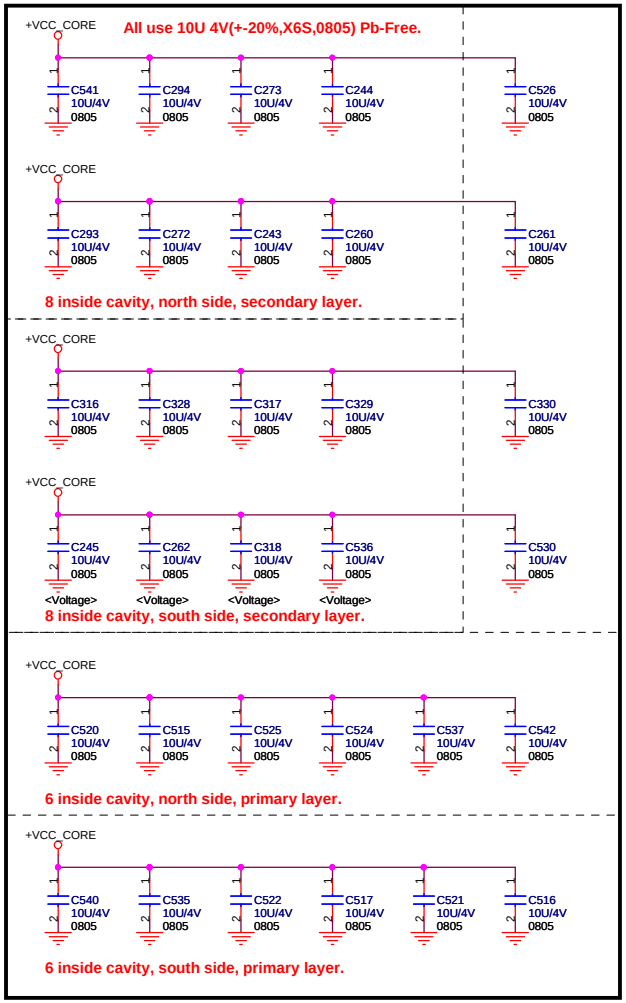
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

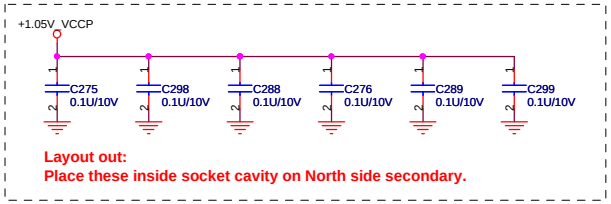
QUANTA COMPUTER

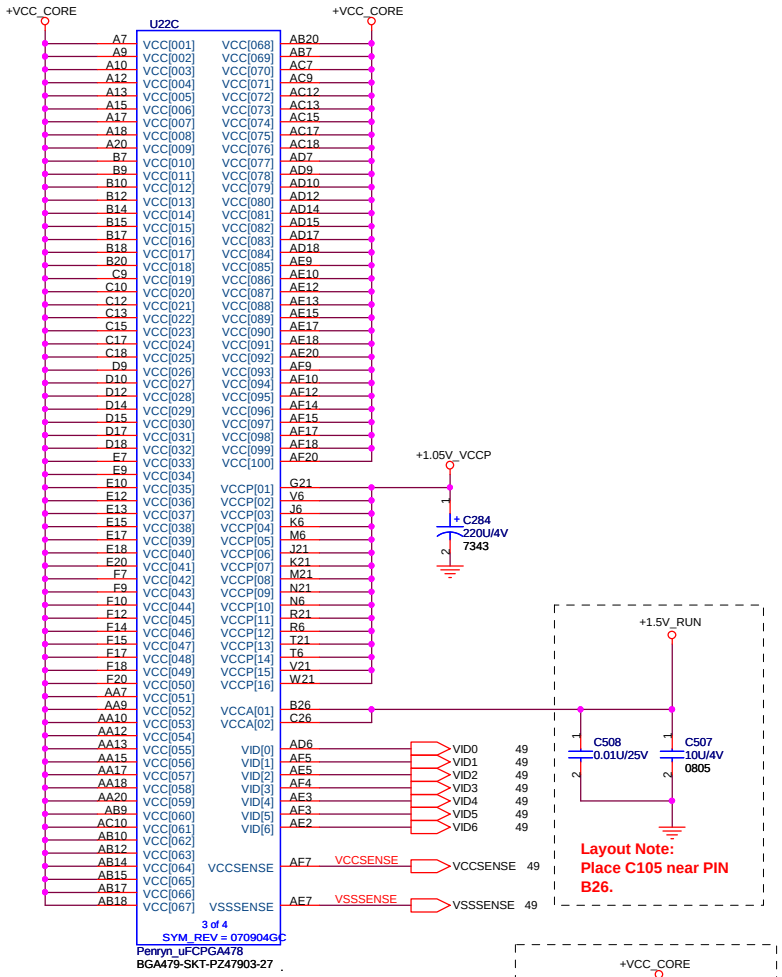
Title: Penryn Processor (HOST BUS)

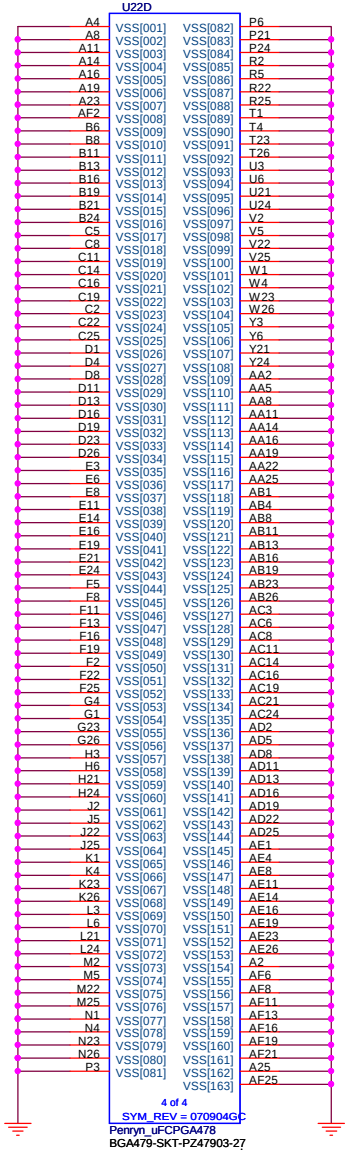
Size: | Document Number: IM3 (XPS-Jolie) | Rev: 2A

Date: Thursday, October 23, 2008 | Sheet 3 of 59









Title	Penryn Processor (POWER)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 4 of 59	

U21A

MCP79_MOBILE_BGA1437

SEC

1 OF 11

SOCKET

FSB

H_D#[0..63]

H_D#[0..63] 3

H_A#[3..35]

Termination

+1.05V_VCCP

R107
62
H_FERR#

+1.05V_VCCP

R405 *1K_NC
R411 *1K_NC
R408 *1K_NC
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
R433 *1K_NC
R435 *1K_NC
R436 *1K_NC

0905_Michael:Add pull-down resistor R433,R435,R436 on CPU_BSEL0~2

+1.1V_RUN

L24
BLM18PG181SN1D
RC0603
+V_PLL_CPU
C212
4.7U/6.3V
C170
2.2U/6.3V
CC0603-C

+1.05V_VCCP

R371
49.9/F
BCLK_VML_COMP_VDD
BCLK_VML_COMP_GND
R376
49.9/F

+1.05V_VCCP

R378
49.9/F
CPU_COMP_VCC
CPU_COMP_GND
R377
49.9/F

1. Route at normal impedance and 8 mils spacing to resistor.
2. 49.9 ohm to GND or VTT_CPU less than 1 inch from MCP79.

R128 1 2 62 H_BR1#

R124 1 2 49.9/F H_FERR#

1022_Michael:Remove H_THERMTRIP connector from CPU, add R124 pull-high to +1.05V_VCCP

0313-Sun_Add pull-up 220 ohm to +1.05V_VCCP on H_DPRSTP#

Termination

+1.05V_VCCP

R117 *150_NC
R132 *150_NC
R120 *150_NC
R125 *51/F_NC
R599 *220/F_NC
H_NMI
H_INTR
H_PWRGOOD
H_CPUSLP#
H_DPRSTP#

0111-Steg: R120_NC.
Remove redundant pull-up R120 on H_PWRGOOD

0313-Sun_Depop pull-up on H_NMI & H_INTR.
(Depop R117,R132)

Length matching w/CLK_CPU_BCLK

C528 *12P/50V_NC
C531 *12P/50V_NC

0605_Michael:NV review,remove pull-down C509 on CLK_ITP_BCLK & C510 on CLK_ITP_BCLK#

+V_DLL_DLCELL_AVDD	+V_PLL_MCLK	+V_PLL_FSB	+V_PLL_CPU
150mA with RUN rail	20mA with RUN rail	29mA with RUN rail	15mA with RUN rail
1 x ferrite bead	1 x ferrite bead	1 x ferrite bead	1 x ferrite bead
1 x 4.7uF X5R ceramic	1 x 1uF X5R ceramic	1 x 4.7uF X5R ceramic	1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic	1 x 2.2uF X7R ceramic

QUANTA COMPUTER

Title	MCP79 (HOST)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 5 of 59	

Layout Notice:

Memory Data Signal Group

MCP79 BGA Breakout (<175ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.

After Breakout: Route at 40 ohm impedance and 4x(Microstrip) or 3x(Stripline) dielectric spacing.

DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

Memory Data Strobes

Route strobes differentially at 66 ohm impedance (42 ohm SE) and 5x dielectric height spacing to other signals.

Memory Clock Signal Group

MCP79 BGA Breakout (<90ps): Route at 50 ohm SE / 100 ohm differential impedance.

After Breakout: Route at 40 ohm SE / 66 ohm differential impedance and 5x dielectric height spacing to other signals.

Memory Address/Command/Control Signal Group

MCP79 BGA Breakout (<90ps): Route at 50 ohm impedance and 1.5x dielectric height spacing.

After Breakout: Route at 40 ohm impedance and 2x dielectric height to other signals and 3x dielectric spacing to other non-associated signals.

DIMM Fan-in (<90ps): Route at 40 ohm impedance and 1.5x dielectric height spacing.

QUANTA COMPUTER

Title	MCP79 (DDR3)	
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Monday, October 20, 2008	Sheet 6 of 59	

+V_VPLL
39mA with RUN rail

+V_PLL_XREF_XS
17mA with RUN rail

+V_PLL_CORE
19mA with RUN rail

+V_PLL_DP
12mA with RUN rail

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

4.3A with ALW rail for S0
318mA for S0 Idle

1 x 2.2uF ceramic
12 x 0.1uF X7R ceramic

U21D SOCKET
MCP79_MOBILE_BGA1437
SEC 4 OF 11

MEMORY CONTROL 0B
MEMORY CONTROL 1B

+1.1V_RUN
L28
BLM18PG181SN1D
RC0603
C250 4.7U/6.3V
C738 4.7U/6.3V
C254 2.2U/6.3V CC0603

0910_Michael:Follow NV check list
add 4.7U C738

0605_Michael:Remove 0ohm R93

MEM_RESET# 15,16

0102-Sun_Change MEM_COMP_VDD & MEM_COMP_GND setting
MEM_COMP_VDD from +1.5V_RUN to GND &
MEM_COMP_GND from GND to +1.5V_RUN

R372 40.2/F
R373 40.2/F

Layout Notice:
1. 40.2 +-1% ohm to +1.5V_SUS less than 1 inch from MCP79 for DDR3.
2. Route with 7 mils trace width and 8 mils spacing to termination reisitor.

0918_Michael:Follow NV checklist
change value from 4.7U to 2.2U

C103 2.2U/6.3V CC0603-C
C160 C157 C159 C152 C151 0.1U/10V
C161 C162 C146 C93 C112 C109 0.1U/10V

1217- AC Stitch Cap
C131 C130 C132 0.1U/10V

QUANTA COMPUTER

Title	MCP79 (MEM POWER)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 19, 2008	Sheet 7 of 59	

17 PCIE_MRX_GTX_P[0..15]
17 PCIE_MRX_GTX_N[0..15]

U21E
MCP79_MOBILE_BGA1437
SOCKET
SEC 5 OF 11

PCIE

PCIE Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline)
dielectric height spacing.

0605_Michael:Remove 0ohm
R185 on MXM_ON#
R433,R435,168 pull-down to GND
R177 on PE_RESET_MXM#
R458 on PCIE_WAKE#

PCIE_MRX_GTX_P0 F7 PE0_RX0_P
PCIE_MRX_GTX_N0 E7 PE0_RX0_N
PCIE_MRX_GTX_P1 D7 PE0_RX1_P
PCIE_MRX_GTX_N1 C7 PE0_RX1_N
PCIE_MRX_GTX_P2 E6 PE0_RX2_P
PCIE_MRX_GTX_N2 F6 PE0_RX2_N
PCIE_MRX_GTX_P3 E5 PE0_RX3_P
PCIE_MRX_GTX_N3 F5 PE0_RX3_N
PCIE_MRX_GTX_P4 E4 PE0_RX4_P
PCIE_MRX_GTX_N4 E3 PE0_RX4_N
PCIE_MRX_GTX_P5 C3 PE0_RX5_P
PCIE_MRX_GTX_N5 D3 PE0_RX5_N
PCIE_MRX_GTX_P6 G5 PE0_RX6_P
PCIE_MRX_GTX_N6 H5 PE0_RX6_N
PCIE_MRX_GTX_P7 J7 PE0_RX7_P
PCIE_MRX_GTX_N7 J6 PE0_RX7_N
PCIE_MRX_GTX_P8 J5 PE0_RX8_P
PCIE_MRX_GTX_N8 J4 PE0_RX8_N
PCIE_MRX_GTX_P9 L11 PE0_RX9_P
PCIE_MRX_GTX_N9 L10 PE0_RX9_N
PCIE_MRX_GTX_P10 L9 PE0_RX10_P
PCIE_MRX_GTX_N10 L8 PE0_RX10_N
PCIE_MRX_GTX_P11 L7 PE0_RX11_P
PCIE_MRX_GTX_N11 L6 PE0_RX11_N
PCIE_MRX_GTX_P12 N11 PE0_RX12_P
PCIE_MRX_GTX_N12 N10 PE0_RX12_N
PCIE_MRX_GTX_P13 N9 PE0_RX13_P
PCIE_MRX_GTX_N13 P9 PE0_RX13_N
PCIE_MRX_GTX_P14 N7 PE0_RX14_P
PCIE_MRX_GTX_N14 N6 PE0_RX14_N
PCIE_MRX_GTX_P15 N5 PE0_RX15_P
PCIE_MRX_GTX_N15 N4 PE0_RX15_N

PE0_TX0_P C5 PCIE_MTX_GRX_C_P0 C347 2 0.1U/10V_DIS PCIE_MTX_GRX_P0
PE0_TX0_N D4 PCIE_MTX_GRX_C_N0 C340 2 0.1U/10V_DIS PCIE_MTX_GRX_N0
PE0_TX1_P C4 PCIE_MTX_GRX_C_P1 C373 2 0.1U/10V_DIS PCIE_MTX_GRX_P1
PE0_TX1_N B4 PCIE_MTX_GRX_C_N1 C384 2 0.1U/10V_DIS PCIE_MTX_GRX_N1
PE0_TX2_P A4 PCIE_MTX_GRX_C_P2 C556 2 0.1U/10V_DIS PCIE_MTX_GRX_P2
PE0_TX2_N A3 PCIE_MTX_GRX_C_N2 C565 2 0.1U/10V_DIS PCIE_MTX_GRX_N2
PE0_TX3_P B3 PCIE_MTX_GRX_C_P3 C552 2 0.1U/10V_DIS PCIE_MTX_GRX_P3
PE0_TX3_N B2 PCIE_MTX_GRX_C_N3 C548 2 0.1U/10V_DIS PCIE_MTX_GRX_N3
PE0_TX4_P C1 PCIE_MTX_GRX_C_P4 C358 2 0.1U/10V_DIS PCIE_MTX_GRX_P4
PE0_TX4_N D1 PCIE_MTX_GRX_C_N4 C367 2 0.1U/10V_DIS PCIE_MTX_GRX_N4
PE0_TX5_P D2 PCIE_MTX_GRX_C_P5 C333 2 0.1U/10V_DIS PCIE_MTX_GRX_P5
PE0_TX5_N E1 PCIE_MTX_GRX_C_N5 C323 2 0.1U/10V_DIS PCIE_MTX_GRX_N5
PE0_TX6_P E2 PCIE_MTX_GRX_C_P6 C547 2 0.1U/10V_DIS PCIE_MTX_GRX_P6
PE0_TX6_N F2 PCIE_MTX_GRX_C_N6 C544 2 0.1U/10V_DIS PCIE_MTX_GRX_N6
PE0_TX7_P F3 PCIE_MTX_GRX_C_P7 C543 2 0.1U/10V_DIS PCIE_MTX_GRX_P7
PE0_TX7_N F4 PCIE_MTX_GRX_C_N7 C539 2 0.1U/10V_DIS PCIE_MTX_GRX_N7
PE0_TX8_P G3 PCIE_MTX_GRX_C_P8 C311 2 0.1U/10V_DIS PCIE_MTX_GRX_P8
PE0_TX8_N H4 PCIE_MTX_GRX_C_N8 C319 2 0.1U/10V_DIS PCIE_MTX_GRX_N8
PE0_TX9_P H3 PCIE_MTX_GRX_C_P9 C534 2 0.1U/10V_DIS PCIE_MTX_GRX_P9
PE0_TX9_N H2 PCIE_MTX_GRX_C_N9 C538 2 0.1U/10V_DIS PCIE_MTX_GRX_N9
PE0_TX10_P H1 PCIE_MTX_GRX_C_P10 C297 2 0.1U/10V_DIS PCIE_MTX_GRX_P10
PE0_TX10_N J1 PCIE_MTX_GRX_C_N10 C307 2 0.1U/10V_DIS PCIE_MTX_GRX_N10
PE0_TX11_P J2 PCIE_MTX_GRX_C_P11 C291 2 0.1U/10V_DIS PCIE_MTX_GRX_P11
PE0_TX11_N J3 PCIE_MTX_GRX_C_N11 C280 2 0.1U/10V_DIS PCIE_MTX_GRX_N11
PE0_TX12_P K2 PCIE_MTX_GRX_C_P12 C532 2 0.1U/10V_DIS PCIE_MTX_GRX_P12
PE0_TX12_N K3 PCIE_MTX_GRX_C_N12 C529 2 0.1U/10V_DIS PCIE_MTX_GRX_N12
PE0_TX13_P L4 PCIE_MTX_GRX_C_P13 C523 2 0.1U/10V_DIS PCIE_MTX_GRX_P13
PE0_TX13_N L3 PCIE_MTX_GRX_C_N13 C527 2 0.1U/10V_DIS PCIE_MTX_GRX_N13
PE0_TX14_P M4 PCIE_MTX_GRX_C_P14 C263 2 0.1U/10V_DIS PCIE_MTX_GRX_P14
PE0_TX14_N M3 PCIE_MTX_GRX_C_N14 C267 2 0.1U/10V_DIS PCIE_MTX_GRX_N14
PE0_TX15_P M2 PCIE_MTX_GRX_C_P15 C519 2 0.1U/10V_DIS PCIE_MTX_GRX_P15
PE0_TX15_N M1 PCIE_MTX_GRX_C_N15 C518 2 0.1U/10V_DIS PCIE_MTX_GRX_N15

PCIE_MTX_GRX_P[0..15] 17
PCIE_MTX_GRX_N[0..15] 17

10 MXM_ON# C9 PE0_PRSNT_16#

Express Card
34 CARD_CLK_REQ# D5 PEB_CLKREQ#/GPIO_49
34,36 EXPRCRD_PWREN# D9 PEB_PRSNT#
D9 1 2 CH751H-40HPT

WLAN
32 MINI1CLK_REQ# E8 PEC_CLKREQ#/GPIO_50
C10 PEC_PRSNT#

UWB/BT
33 MINI2CLK_REQ# M15 PED_CLKREQ#/GPIO_51
B10 PED_PRSNT#

WWAN
33 MINI3CLK_REQ# L16 PEE_CLKREQ#/GPIO_16
L18 PEE_PRSNT#/GPIO_46

17 PE_RESET_MXM# M16 PEF_CLKREQ#/GPIO_17
MXM_PRESENT# M18 PEF_PRSNT#/GPIO_47

38 KB_LED_DET M17 PEG_CLKREQ#/GPIO_18
36,47 MXM_RUNPWRGD M19 PEG_PRSNT#/GPIO_48

32,33,34 PCIE_WAKE# F17 PE_WAKE#

+3.3V_SUS
R211 100K_UMA
MXM_PRESENT#
R210 1K_DIS

0314_Change MXM_PRESENT# pull down RES (R210) from 100k to 1k ohm base on NV suggestion

0825_Michael:Add KB detect function
0918_Michael:Remove KB detect function
0920_Michael:Add KB detect function

Express Card
34 PCIE_RX0_P K9 PE1_RX0_P
34 PCIE_RX0_N J9 PE1_RX0_N

WLAN
32 PCIE_RX1_P H9 PE1_RX1_P
32 PCIE_RX1_N G9 PE1_RX1_N

UWB/BT
33 PCIE_RX2_P F9 PE1_RX2_P
33 PCIE_RX2_N E9 PE1_RX2_N

WWAN
33 PCIE_RX3_P H7 PE1_RX3_P
33 PCIE_RX3_N G7 PE1_RX3_N

PE0_REFCLK_P E11 CLK_PCIE_VGA 17
PE0_REFCLK_N D11 CLK_PCIE_VGA# 17

PE1_REFCLK_P G11 CLK_PCIE_EXPCARD 34
PE1_REFCLK_N F11 CLK_PCIE_EXPCARD# 34

PE2_REFCLK_P J11 CLK_PCIE_MINI1 32
PE2_REFCLK_N J10 CLK_PCIE_MINI1# 32

PE3_REFCLK_P G13 CLK_PCIE_MINI2 33
PE3_REFCLK_N F13 CLK_PCIE_MINI2# 33

PE4_REFCLK_P J13 CLK_PCIE_MINI3 33
PE4_REFCLK_N H13 CLK_PCIE_MINI3# 33

PE5_REFCLK_P L14
PE5_REFCLK_N K14

PE6_REFCLK_P N14
PE6_REFCLK_N M14

0605_Michael:Remove Test pad
T21,T22,T28,T30

PE_RST0# K11 PE_RESET# C

PE1_TX0_P D8 PCIE_TX0_P_C C564 2 0.1U/10V PCIE_TX0_P 34
PE1_TX0_N C8 PCIE_TX0_N_C C563 2 0.1U/10V PCIE_TX0_N 34

PE1_TX1_P B8 PCIE_TX1_P_C C576 2 0.1U/10V PCIE_TX1_P 32
PE1_TX1_N A8 PCIE_TX1_N_C C575 2 0.1U/10V PCIE_TX1_N 32

PE1_TX2_P A7 PCIE_TX2_P_C C561 2 0.1U/10V PCIE_TX2_P 33
PE1_TX2_N B7 PCIE_TX2_N_C C562 2 0.1U/10V PCIE_TX2_N 33

PE1_TX3_P B6 PCIE_TX3_P_C C559 2 0.1U/10V PCIE_TX3_P 33
PE1_TX3_N C6 PCIE_TX3_N_C C560 2 0.1U/10V PCIE_TX3_N 33

+1.1V_RUN
482mA with RUN rail
JP3 SHORT40X18
0312-Sun_Change footprint to normal short type "short40x18"
1 x 2.2uF X5R ceramic
2 x 1uF X7R ceramic
2 x 0.1uF X7R ceramic

+DVDD_PEX
C227 2.2U/6.3V CC0603-C
C740 1U/6.3V
C234 1U/6.3V
C233 0.1U/10V
C253 0.1U/10V

T17 +DVDD0_PEX
W19 +DVDD0_PEX
U17 +DVDD0_PEX
M12 +DVDD0_PEX
V19 +DVDD0_PEX
W16 +DVDD0_PEX
W17 +DVDD0_PEX
W18 +DVDD0_PEX
U16 +DVDD0_PEX
T19 +DVDD1_PEX
U19 +DVDD1_PEX

0918_Michael:Follow NV checklist change value from 4.7U to 2.2U and add 1U

+AVDD_PEX
L6 BLM21PG600SN1D
+1.1V_RUN
1304mA with RUN rail
1x ferrite bead
1x 10uF
1 x 2.2uF X5R ceramic
2 x 1uF X5R ceramic
2 x 0.1uF X7R ceramic

0624_Michael:Change L6 type from BLM21PG331SN1D to BLM21PG600SN1D

+AVDD0_PEX Y12
+AVDD0_PEX AA12
+AVDD0_PEX AB12
+AVDD0_PEX M12
+AVDD0_PEX P12
+AVDD0_PEX R12
+AVDD0_PEX N12
+AVDD0_PEX T12
+AVDD0_PEX U12
+AVDD0_PEX AC12
+AVDD0_PEX AD12
+AVDD0_PEX V12
+AVDD0_PEX W12
+AVDD1_PEX M13
+AVDD1_PEX N13
+AVDD1_PEX P13

C105 10U/6.3V CC0603
C228 0.1U/10V
C183 0.1U/10V
C240 1U/6.3V
C266 1U/6.3V
C216 2.2U/6.3V CC0603

0918_Michael:Follow NV checklist change value from 4.7U to 2.2U

T517 pad-s1 +AVDD_PEX
1221-Sun_Add dummy part for +AVDD_PEX

+1.1V_RUN
L22 BLM18PG181SN1D RC0603
82mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic

+1.1V_PE_PLL
C256 4.7U/6.3V CC0603
C229 2.2U/6.3V CC0603
T16 +V_PLL_PEX

PE_CLK_COMP A11 PE_CLK_COMP
R434 *2.37K/F_NC

+3.3V_SUS
C579 0.047U/10V
U25 TC7SZ32FU(T5L,F,T)
PE_RESET# C
PE_RESET# 17,32,33,34,36

QUANTA COMPUTER

Title	MCP79 (PCIE)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Saturday, September 20, 2008	Sheet 8 of 59	

1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 2.2uF X7R ceramic

+1.1V_RMGT
L25 BLM18PG181SN1D RC0603
C265 4.7U/6.3V CC0603
C255 2.2U/6.3V CC0603

5mA with RUN rail

Layout Notice:
124 ohm +-1% to GND and within 750 mils of MCP79.
0.01uF to GND and within 500 mils of MCP79.

+3.3V_RMGT
R190 10K
RGMII_PWRDWN

RGMII_RESET#
R143 4.7K
0606_Michael:Add DR_PLUG on HPLUG_DET2 for DP detect

0312-Sun_Change footprint to normal short type "short40x18"

+1.8V_RUN
JP5 SHORT40X18

190mA with RUN rail
1 x 2.2uF X5R ceramic
1 x 0.1uF X7R ceramic
0918_Michael:Follow NV checklist change value from 4.7U&0.1U to 2.2U

+1.1V_RUN
95mA with RUN rail
2 x 2.2uF X5R ceramic
0918_Michael:Follow NV checklist change value from 4.7U&0.1U to 2.2U

+3.3V_RUN
JP7 SHORT40X18
8mA with RUN rail
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic
+V_PLL_IFPAB
C371 4.7U/6.3V CC0603
C372 0.1U/10V
C277 0.1U/10V

U21F
MCP79_MOBILE_BGA1437
SEC 6 OF 11

LAN
DACS
FLAT PANEL

45 RGMII_RXD[0..3]
RGMII_RXD0 C23 RGMII_RXD0/MII_RXD0
RGMII_RXD1 B23 RGMII_RXD1/MII_RXD1
RGMII_RXD2 E24 RGMII_RXD2/MII_RXD2
RGMII_RXD3 A24 RGMII_RXD3/MII_RXD3
45 RGMII_RXCLK A23 RGMII_RXC/MII_RXCLK
45 RGMII_RXCTL C22 RGMII_RXCTL/MII_RXDV
R180 47K F23 MII_RXER/GPIO_36
B26 MII_COL/GPIO_20/MSMB_DATA
B22 MII_CRS/GPIO_21/MSMB_CLK
R173 10K J22 RGMII/MII_INTR/GPIO_35
+1.1V_DUAL_PLL_MAC T23 +V_DUAL_MACPLL
+3.3V_RMGT R424 49.9/F MII_COMP_VDD C27 MII_COMP_VDD
R425 49.9/F MII_COMP_GND B27 MII_COMP_GND
R432 124/F RGB_DAC_RSET C39 RGB_DAC_RSET
C558 0.01U/16V RGB_DAC_VREF B38 RGB_DAC_VREF
E36 TV_DAC_RSET
A35 TV_DAC_VREF
C38 XTALIN_TV
D38 XTALOUT_TV

0318-Sun_Connect GPIO6 to DP_PRIORITY, add R604 & del T39
R604 *0_NC
28 DP_PRIORITY E16 GPIO_6/FERR/IGPU_GPIO_6#
28 DP_CABLE_DET# B15 GPIO_7/NFERR/IGPU_GPIO_7#
26 BIA_PWM G39 LCD_BKL_CTL/GPIO_57
36 PANEL_BKEN E37 LCD_BKL_ON/GPIO_59
26 ENVDD F40 LCD_PANEL_PWR/GPIO_58
28 ML_LANE3_P ML_LANE3_P D35 HDMI_TXC_P/ML0_LANE3_P
28 ML_LANE3_N ML_LANE3_N E35 HDMI_TXC_N/ML0_LANE3_N
28 ML_LANE2_P ML_LANE2_P G35 HDMI_TXD0_P/ML0_LANE2_P
28 ML_LANE2_N ML_LANE2_N F35 HDMI_TXD0_N/ML0_LANE2_N
28 ML_LANE1_P ML_LANE1_P F33 HDMI_TXD1_P/ML0_LANE1_P
28 ML_LANE1_N ML_LANE1_N G33 HDMI_TXD1_N/ML0_LANE1_N
28 ML_LANE0_P ML_LANE0_P J33 HDMI_TXD2_P/ML0_LANE0_P
28 ML_LANE0_N ML_LANE0_N H33 HDMI_TXD2_N/ML0_LANE0_N
28 AUX_DP_P D43 DP_AUX_CH0_P
28 AUX_DP_N C43 DP_AUX_CH0_N
28 HDMI_PLUG
R428 22K C31 HPLUG_DET2/GPIO_22
28 DP_HPDET F31 HPLUG_DET3

+VDD_IFPAB
C251 2.2U/6.3V CC0603
C258 0.1U/10V
M27 +VDD_IFPA
M26 +VDD_IFPB
+V_PLL_IFPAB
M28 +V_PLL_IFPAB
M29 +V_PLL_HDMI
T25 +VDD_HDMI
HDMI_REST
HDMI_VPROBE
J31 HDMI_RSET
J30 HDMI_VPROBE
C238 2.2U/6.3V CC0603
C235 2.2U/6.3V CC0603-C
R165 1K
C269 *0.1U/10V_NC

SOCKET
+3.3V_DUAL_RMGT J24
+3.3V_DUAL_RMGT K24
C370 0.1U/10V
C385 4.7U/6.3V CC0603
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic
83mA with ALW rail
+3.3V_RMGT
+V_DUAL_RMGT U23
+V_DUAL_RMGT V23
+1.0V_DUAL_RMGT
MII_VREF E28
RGMII_TXD0/MII_TXD0 B24 RGMII_TXD0
RGMII_TXD1/MII_TXD1 C24 RGMII_TXD1
RGMII_TXD2/MII_TXD2 C25 RGMII_TXD2
RGMII_TXD3/MII_TXD3 D25 RGMII_TXD3
RGMII_TXCLK/MII_TXCLK D24 RGMII_TXCLK_C
RGMII_TXCTL/MII_TXEN C26
RGMII_TXD[0..3] 12,45
0319-Sun_Change RGMII_TXCLK damping RES to 22 ohm for EMI
R194 22
RGMII_TXCLK 45
RGMII_TXCTL 45
RGMII/MII_MDC D21 RGMII_MDC 45
RGMII/MII_MDIO C21 RGMII_MDIO 45
RGMII_PWRDWN
RGMII/MII_PWRDWN#/GPIO_3 G23 RGMII_PWRDWN 45
BUF_25MHz E23 RGMII_25MHz_C
R178 22
RGMII_25MHz 45
MII_RESET# J23 RGMII_RESET#
RGMII_RESET# 45
+V_RGB_DAC J32
+V_TV_DAC K32
+V_RGB_DAC
R460 0
0605_Michael: Follow NV command pull-down to GND
DDC_CLK0 B31 G_CLK_DDC 27
DDC_DATA0 A31 G_DAT_DDC 27
RGB_DAC_RED B39 VGA_RED
RGB_DAC_GREEN A39 VGA_GRN
RGB_DAC_BLUE B40 VGA_BLU
RGB_DAC_HSYNC A40 VGAHSYNC 27
RGB_DAC_VSYNC A41 VGAVSYNC 27
VGA_RED 27
VGA_GRN 27
VGA_BLU 27
TV_DAC_RED A36
TV_DAC_GREEN B36
TV_DAC_BLUE C36
TV_DAC_HSYNC/GPIO_44 D36
TV_DAC_VSYNC/GPIO_45 C37

Reserved EMI Solution
RGMII_TXCLK_C
RGMII_25MHz_C
C351 33P/50V
C312 33P/50V
0319-Sun_Pop RGMII_25Mhz_C & RGMII_TXCLK_C capacitor w/33P for EMI

IFPA_TXC_P B35 LCD_ACLK+ 26
IFPA_TXC_N C35 LCD_ACLK- 26
IFPA_TXD0_P B32 LCD_A0+ 26
IFPA_TXD0_N A32 LCD_A0- 26
IFPA_TXD1_P D32 LCD_A1+ 26
IFPA_TXD1_N C32 LCD_A1- 26
IFPA_TXD2_P D33 LCD_A2+ 26
IFPA_TXD2_N C33 LCD_A2- 26
IFPA_TXD3_P B34
IFPA_TXD3_N C34
0605_Michael:Remove Test pad T65,T67
IFPB_TXC_P L31 LCD_BCLK+ 26
IFPB_TXC_N K31 LCD_BCLK- 26
IFPB_TXD4_P J29 LCD_B0+ 26
IFPB_TXD4_N H29 LCD_B0- 26
IFPB_TXD5_P L29 LCD_B1+ 26
IFPB_TXD5_N K29 LCD_B1- 26
IFPB_TXD6_P L30 LCD_B2+ 26
IFPB_TXD6_N K30 LCD_B2- 26
IFPB_TXD7_P N30
IFPB_TXD7_N M30
0605_Michael:Remove Test pad T24,T26
DDC_CLK2/GPIO_23 C30 LCD_DDCCLK 26
DDC_DATA2/GPIO_24 B30 LCD_DDCDAT 26
DDC_CLK3 D31 DP_DDCSCL
DDC_DATA3 E31 DP_DDCSDA
DP_DDCSCL 28
DP_DDCSDA 28
IFPAB_RSET E32
IFPAB_VPROBE G31
C557 *0.1U/10V_NC
R181 *1K_NC

+1.1V_RMGT
C241 0.1U/10V
C221 2.2U/6.3V CC0603-C
131mA with ALW rail
1 x 2.2uF X5R ceramic
1 x 0.1uF X7R ceramic
0918_Michael:Follow NV checklist change value from 4.7U to 2.2U

+3.3V_RMGT
R205 1.47K/F
MII_VREF
R197 1.47K/F
C346 0.1U/10V

+3.3V_RUN
103mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
2 x 0.1uF X7R ceramic
L43 BLM18PG181SN1D RC0603
+V_RGB_DAC
C283 0.1U/10V
C573 0.1U/10V
C574 4.7U/6.3V CC0603

VGA_RED
VGA_GRN
VGA_BLU
R431 150/F
R430 150/F
R429 150/F
Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

+3.3V_RUN
R338 2.7K/F
R333 2.7K/F
LCD_DDCCLK
LCD_DDCDAT

+3.3V_RUN
R201 100K
R202 100K
DP_DDCSCL
DP_DDCSDA

QUANTA COMPUTER

Title	MCP79 (LAN,DACS,LVDS)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, September 18, 2008	Sheet 9 of 59	

U21G
MCP79_MOBILE_BGA1437
SOCKET
SEC 7 OF 11

PCI

LPC

GND

0630_Michael:Remove Mini PCI CN8 and circuit

Layout Notice:
Cap placed within 500 mil of MCP79.

0319-Sun_Pop PCI_CLK capacitor w/15P for COMM

0605_Michael:NV review,remove pull-up R576 to +3.3V_SUS
0627_Michael:Add pull-up R208 to +3.3V_SUS(Leave Empty)

0606_Michael:Remove Test pad T77 and pull-down C257 to GND

Layout Notice:
Serise resistor placed within 500 mil of MCP79.
Length matching w/PCI_CLK*

Layout Notice:
33 ohm serise resistor placed within 500 mil of MCP79.

0607_Michael:Remove pull-up R126 to +3.3V_RUN

0823_Michael:Follow NV checklist MXM_PWR_EN pull-down 10K to GND

Termination

MCP79 Strapping

0605_Michael:NV review,remove pull-up R237 & R390 to +3.3V_SUS

Boot BIOS Strapping		
	HDA_SDATA_OUT	LPC_FRAME#
LPC BIOS	0	0
PCI BIOS	0	1
SPI BIOS(CS0)	1	0
SPI BIOS(CS1)	1	1

QUANTA COMPUTER

Title	MCP79 (PCI,LPC)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 10 of 59	

0318-Sun_change left USB port from port1 to port0 for NV remote SW debug.

U21H
MCP79_MOBILE_BGA1437
SEC 8 OF 11

SOCKET

SATA

USB

Left Side (froth)
Left Side
Combo (eSATA/USB)
Mini Card (WLAN)
Mini Card (WWAN)
Mini Card (WPAN)
Express Card
Biometric
Camera

1020_Michael:Remove T36,T37

1020_Michael:Remove T23,T29,T32,T34

0605_Michael: Follow NV command change power rail from +3.3V_RUN to +3.3V_SUS
0704_Michael:Move R7 pull-up to +3.3V_SUS close to MCP79

0616_Michael:Cancel fingerprinter and remove MCP_USB10+/-

0625_Michael:Add R403 for debug if have need

SATA Layout Notice:
BGA Breakout:
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals.Maximum brackout distance is 400 mils of MCP79.
BGA Fan-out:
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals.Maximum BGA brackout plus Fan-out distance is 500 mils.
After Brackout:
Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
TX and RX intra-pair skew for a differential pair is 5 mils.

+V_PLL_SATA
163mA with RUN rail
1x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

+V_PLL_USB
18mA with Run rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

0312-Sun_Change footprint to normal short type "short40x18"

0918_Michael:Follow NV checklist change value from 4.7U to 2.2U

+DVDD0_SATA
117mA with RUN rail
1 x 2.2uF X5R ceramic
1 x 0.1uF X7R ceramic

0605_Michael: Remove 0ohm R123

+AVDD0_SATA
363mA with RUN rail
1x ferrite bead
1x 10uF
1 x 2.2uF X5R ceramic
3 x 0.1uF X7R ceramic

0910_Michael:Follow NV check list add 0.1U C510
0918_Michael:Follow NV checklist change value from 4.7U to 2.2U

0605_Michael: Remove 0ohm R109

Layout Notice:
2.49K ohm to GND within 500 mils of MCP79.
Routing 8 mils spacing to resistor.

Layout Notice:
909 ohm +-1% to GND within 1000 mil of MCP79.
Routing trace at least 8 mil wide to resistor.

0311-Sun_Changes USB RBIAS resistor to 806ohm. (NV)

USB Layout Notice:
BGA Breakout:
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals.Maximum brackout distance is 300 mils of MCP79.
BGA Fan-out:
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals.Maximum BGA brackout plus Fan-out distance is 400 mils.
After Brackout:
Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals.
Each USB pair must be length matched to within 50 mil.

QUANTA COMPUTER

Title	MCP79 (SATA,USB)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Monday, October 20, 2008	Sheet 11 of 59	

1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic
6mA with ALW rail

C581 0.1U/10V
C400 0.1U/10V
C302 4.7U/6.3V CC0603-C
+3.3V_SUS

0910_Michael:Follow NV check list add 0.1U C581

U21I
MCP79_MOBILE_BGA1437
SEC 9 OF 11
SOCKET

HDA

42 HDA_SDATA_IN — G15 HDA_SDATA_IN0
35 THERM_ALERT# — J14 HDA_SDATA_IN1/GPIO_2/PS2_KB_CLK
T57 PAD — J15 HDA_SDATA_IN2/GPIO_3/PS2_KB_DATA
+3.3V_SUS
R438 49.9/F
A15 HDA_PULLDN_COMP

HDA_SDATA_OUT — F15 HDA_SDATA_OUT_R — R189 22 — HDA_SDATA_OUT 10,42
HDA_BITCLK_R — R187 22 — HDA_BITCLK 42
HDA_BITCLK — E15
C321 10P/50V
C345 10P/50V

0607_Michael:NV review,remove 0ohm R166 on PE_RESET_MXM#

HDA_RESET# — K15 HDA_RESET#_R — R212 22 — HDA_RESET# 36,42
HDA_SYNC — L15 HDA_SYNC_R — R188 33 — HDA_SYNC 42
HDA_DOCK_EN#/GPIO_4/PS2_MS_CLK — K17
HDA_DOCK_RST#/GPIO_5/PS2_MS_DATA — L17
PAD T518
C356 10P/50V
C310 10P/50V

0229-Sun_Depop R166
0314-Sun_Remove MXM_RUNPWROK from GPIO4 (pin K17) and reserve TP.

+1.1V_RUN
C246 1U/10V CC0603
L18 BLM18PG181SN1D RC0603
1 x ferrite bead
1 x 4.7uF X5R ceramic
2 x 2.2uF X7R ceramic

18mA with RUN rail
15mA with RUN rail
AE18 +V_PLL_NV_H
AE17 +V_PLL_SP_SPREF
C129 4.7U/6.3V CC0603
C196 2.2U/6.3V CC0603-C
C195 2.2U/6.3V CC0603-C

SLP_S3# — G17 — SIO_SLP_S3# 36
SLP_RMGT# — J17 — SLP_RMGT# 14
SLP_S5# — H17 — SIO_SLP_S5# 36,51

0607_Michael:Remove Test pad T60,T58

R309 *22K/F_NC
R442 *22K/F_NC
R320 *22K/F_NC

T31 PAD — L24 GPIO_1/PWRDN_OK/SPI_CS1

0606_Michael:NV review,remove pull-up R577,R578,R586 to +3.3V_SUS

36 SIO_EXT_WAKE# — L26 GPIO_12/SUS_STAT#/ACCLMTR_EXT_TRIG
36 MCP_A20GATE — K13 A20GATE
36 MCP_KBRDRSTIN# — L13 KBRDRSTIN#
36 MCP_PME# — C19 SIO_PME#
36 MCP_EXT_SMI# — C18 EXT_SMI#/GPIO_32
+RTC_CELL — R191 49.9K/F — B20 INTRUDER#

THERM_DIODE_P — B11
THERM_DIODE_N — C11

0607_Michael:NV review,remove pull-up R579,R580 to +3.3V_SUS
0606_Michael:NV review,remove pull-up R581 to +3.3V_SUS

MISC

C344 0.1U/10V
49 DPRSLPVR — M22 CPU_DPRSLPVR
36 MCP_PWRBTN# — R200 0 — T63 PAD — C16 PWRBTN# — D16 RSTBTN#
0606_Michael:Remove pull-up R220 to +3.3V_SUS,add Test pad T63
RTC_RST# — C20 RTC_RST#
36 PWRGD_SB — D20 PWRGD_SB
36 PS_PWRGD — E20 PS_PWRGD
36,49 CPU_PWRGD
C17 CPU_VLD
0606_Michael:Remove pull-up R584,R585 to +3.3V_SUS,add Test pad T65,T35

MCP_VID0/GPIO_13 — L20 MCP_CORE_VID0 — MCP_CORE_VID0 50
MCP_VID1/GPIO_14 — M20 MCP_CORE_VID1 — MCP_CORE_VID1 50
MCP_VID2/GPIO_15 — M21 MCP_CORE_VID2 — MCP_CORE_VID2 50

SPKR — C13 SPKR — SPKR 42

SMB_CLK0 — L19 MCP_SMB_SCL_R — MCP_SMB_SCL_R 13
SMB_DATA0 — K19 MCP_SMB_SDA_R — MCP_SMB_SDA_R 13
SMB_CLK1/MSMB_CLK — G21 SMB_MEM_SCL — SMB_MEM_SCL 15,16
SMB_DATA1/MSMB_DATA — F21 SMB_MEM_SDA — SMB_MEM_SDA 15,16
SMB_ALERT#/GPIO_6 — M23 SMB_ALERT# — R427 2.7K/F — +3.3V_RUN

FANRPM0/GPIO_60 — B12 — PCIE_MCARD1_DET# 32
FANCTL0/GPIO_61 — A12 — USB_MCARD1_DET# 32
FANRPM1/GPIO_63 — D12 — PCIE_MCARD2_DET# 33
FANCTL1/GPIO_62 — C12 — USB_MCARD2_DET# 33

CPUVDD_EN — D17 — CPUVDD_EN 49,54
PCIE_MCARD3_DET# 33
SPI_CS0/GPIO_10 — C14
SPI_CLK/GPIO_11 — D13 — USB_MCARD3_DET# — USB_MCARD3_DET# 33
SPI_DI/GPIO_8 — C15 — MCP_EXT_SCI# 36
SPI_DO/GPIO_9 — B14

0606_Michael:Remove 0ohm R208

T65 PAD
T62 PAD
T35 PAD
R172 10K — MCP_JTAG_TDI — E19 JTAG_TDI
R174 10K — MCP_JTAG_TDO — F19 JTAG_TDO
MCP_JTAG_TMS — J19 JTAG_TMS
MCP_JTAG_TRST# — J18 JTAG_TRST#
MCP_JTAG_TCK — G19 JTAG_TCK

0606_Michael:Remove Test pad T25,T33

XTALIN — A16 XTALIN
XTALOUT — B16 XTALOUT
XTALIN_RTC — A19 XTALIN_RTC
XTALOUT_RTC — B19 XTALOUT_RTC

SUS_CLK/GPIO_34 — B18 PAD T59
BUF_SIO_CLK — AE7 PAD T17
TEST_MODE_EN — K22
PKG_TEST — L22
R156 1K

MCP79 Strapping

+3.3V_RMGT
R356 10K
9,45 RGMII_TXD0

Networking Select	
MII	0
RGMII	1

0606_Michael:NV review, remove pull-down R355 to GND

MCP79 Strapping

0606_Michael:NV review, remove pull-up R491 to +3.3V_SUS
SPKR
R484 10K

Boot Mode Select	
User Mode	0
Safe Mode	1

MCP79 Strapping

HDA_SYNC
R213 10K

SIO Clock Select	HDA_SYNC
14.318MHz	0
24MHz	1

+3.3V_SUS
R255 10K
HDA_RESET#

0910_Michael:Follow NV check list change R244,R245,R12,R14 value from 2.7K to 2.2K

+3.3V_SUS
R244 2.2K
R245 2.2K
MCP_SMB_SCL_R
MCP_SMB_SDA_R

+3.3V_RUN
R12 2.2K
R14 2.2K
SMB_MEM_SCL
SMB_MEM_SDA

0606_Michael:NV review,remove pull-up R437,R281 to +3.3V_SUS

+3.3V_SUS
R368 10K
USB_MCARD3_DET#

0625_Michael:Remove SPI Freq select circuit for SPI ROM function not used

+RTC_CELL
R196 49.9K/F
RTC_RST#
R183 *0_NC

CLEAR CMOS ONLY	RTC_RST#
CLEAR	0
NORMAL	1

25MHz Clock

XTALIN
R421 0
Y2 25MHz
XTALOUT
C566 27P/50V
C555 27P/50V

32KHz Clock

XTALIN_RTC
R422 0
W1 32.768KHZ
XTALOUT_RTC
C567 18P/50V
C568 18P/50V

Layout Notice:
Place cystal within 1000 mil of MCP79.

0709-Steg: Change CAP Vaule from 10p to 18p

QUANTA COMPUTER

Title	MCP79 (HDA,MISC)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, September 18, 2008	Sheet 12 of 59	

1 x 10uF ceramic
2 x 2.2uF X5R ceramic
3 x 1uF X5R ceramic
3 x 0.22uF X5R ceramic
12 x 0.1uF X7R ceramic

17.756A with RUN rail for S0
2850mA for S0 Idle

+VTT_CPU
1139mA for ALW rail

+VTT_CPUCLK
43mA for ALW rail

1 x 10uF ceramic
1 x 2.2uF X5R ceramic
3 x 0.1uF X7R ceramic

U21J
MCP79_MOBILE_BGA1437
SOCKET
SEC
10 OF 11

+MCP_CORE
+VDD_CORE
C148 2.2U/6.3V CC0603
C156 2.2U/6.3V CC0603
C184 1U/6.3V
C188 1U/6.3V
C202 1U/6.3V

0918_Michael:Follow NV checklist
change value from 10U to 2.2U

C149 10U/6.3V CC0603-C
C169 0.22U/6.3V
C186 0.22U/6.3V
C187 0.22U/6.3V

C217 0.1U/10V
C204 0.1U/10V
C173 0.1U/10V
C189 0.1U/10V
C194 0.1U/10V
C220 0.1U/10V

C168 0.1U/10V
C211 0.1U/10V
C206 0.1U/10V
C218 0.1U/10V
C182 0.1U/10V
C225 0.1U/10V

POWER

+1.05V_VCCP
C185 0.1U/10V
C219 2.2U/6.3V CC0603
C353 10U/10V CC0805

0918_Michael:Follow NV checklist
change value from 10U to 2.2U

C150 0.1U/10V
C158 0.1U/10V
C314 1U/6.3V

C282 0.1U/10V
C336 0.1U/10V
C332 1U/6.3V

C303 0.1U/10V
C295 0.1U/10V
C341 0.1U/10V

+3.3V_RUN_MCP
450mA with RUN rail

1 x 4.7uF X5R ceramic
4 x 0.1uF X7R ceramic

0312-Sun_Change footprint to
normal short type "short40x18"

JP4 SHORT40X18
C231 0.1U/10V
C205 0.1U/10V
C200 0.1U/10V
C209 0.1U/10V
C226 4.7U/6.3V CC0603-C

0312-Sun_Change footprint to
normal short type "short40x18"

JP6 SHORT40X18
C386 0.1U/10V
C364 4.7U/6.3V CC0603-C

+3.3V_DUAL
16mA with ALW rail

1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

+3.3V_DUAL_USB
450mA with ALW rail

1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

+VDD_AUXC
105mA with ALW rail

2 x 0.1uF X7R ceramic

JP8 SHORT40X18
C249 0.1U/10V
C236 0.1U/10V

These are for
backdrive issue.

Q35 2N7002W-7-F
Q36 2N7002W-7-F
R257 2.7K/F
R260 2.7K/F

HDCP
U5 *AT24C16BN-SH-T_NC
R23 *10K_NC
R16 *10K_NC
R20 *10K_NC
C30 *0.1U/10V_NC

+RTC_CELL
C368 4.7U/6.3V CC0603
C509 4.7U/6.3V CC0603
C713 0.1U/10V

0229-Sun_Add C713 with 0.1U on +VBAT of MCP79
0829_Michael:Follow NV new DG add C509 on +RTC_CELL of MCP79

0.06mA with ALW rail for S0
2 x 4.7uF X5R ceramic

QUANTA COMPUTER

Title	MCP79 (POWER)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 19, 2008	Sheet 13 of 59	

U21K SOCKET

MCP79_MOBILE_BGA1437

SEC

11 OF 11

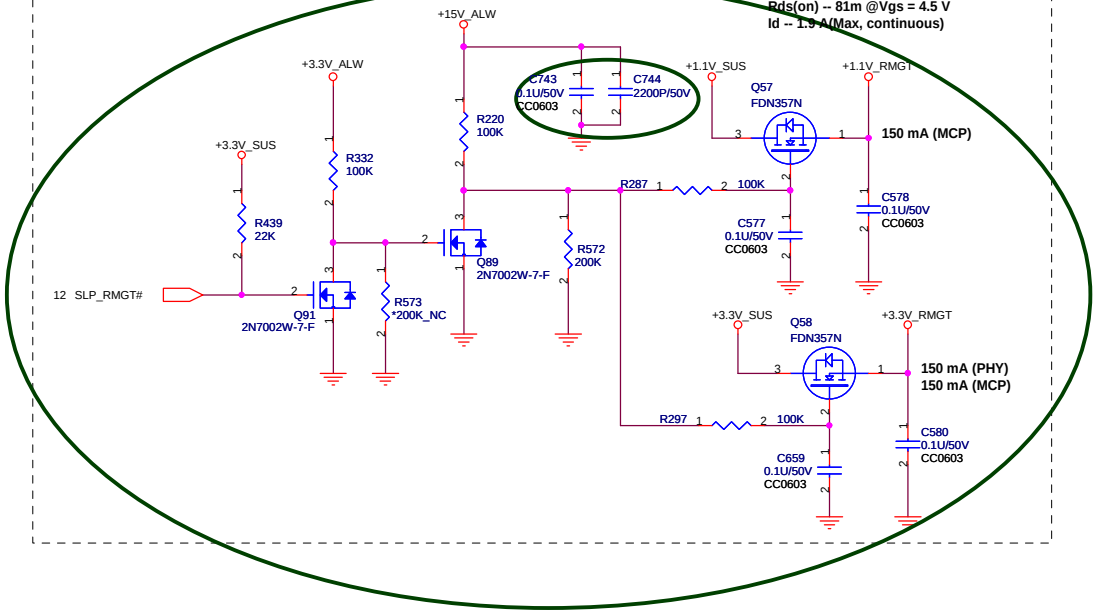
GND

AH26	GND	GND	AV40	AM16	GND	GND	D22
AH33	GND	GND	BA1	AM18	GND	GND	D23
AH34	GND	GND	BA4	AM20	GND	GND	D26
AH37	GND	GND	AW31	AM22	GND	GND	D30
AH38	GND	GND	AY6	AM24	GND	GND	D37
AJ39	GND	GND	L35	AM26	GND	GND	D6
AJ8	GND	GND	BC33	AM30	GND	GND	E13
AK10	GND	GND	BC37	AM34	GND	GND	E17
AK33	GND	GND	BC41	AM35	GND	GND	E21
AK34	GND	GND	AY14	AM37	GND	GND	E25
AK37	GND	GND	BC5	AM38	GND	GND	E29
AK4	GND	GND	C2	AM5	GND	GND	E33
AK40	GND	GND	D10	AM6	GND	GND	F12
AL36	GND	GND	D14	AM7	GND	GND	F16
AL40	GND	GND	D15	AM9	GND	GND	F32
AL5	GND	GND	D18	AP26	GND	GND	F8
AM10	GND	GND	D19	AN28	GND	GND	G10
				AN30	GND	GND	G12
				AN39	GND	GND	G14
				AN4	GND	GND	G16
				Y7	GND	GND	BC12
				AP10	GND	GND	G22
				AU26	GND	GND	G24
				AP14	GND	GND	AW20
				AU14	GND	GND	G34
				AP28	GND	GND	G4
				AP32	GND	GND	G43
				AP34	GND	GND	G6
				AP36	GND	GND	G8
				AP37	GND	GND	H11
				AP4	GND	GND	H15
				AP40	GND	GND	AW35
				AP7	GND	GND	H23
				AW23	GND	GND	AN8
				AR28	GND	GND	G40
				AR32	GND	GND	J12
				AR40	GND	GND	J8
				AT10	GND	GND	K10
				AR12	GND	GND	K12
				AT13	GND	GND	K18
				AT29	GND	GND	K26
				AT33	GND	GND	K37
				AT6	GND	GND	K4
				AT7	GND	GND	K40
				AT9	GND	GND	K8
				AY21	GND	GND	AU1
				AY22	GND	GND	L40
				L12	GND	GND	L43
				AU12	GND	GND	L5
				AU28	GND	GND	M10
				AP33	GND	GND	M34
				AU32	GND	GND	M35
				AR30	GND	GND	M37
				AU36	GND	GND	Y28
				AU38	GND	GND	Y33
				AU4	GND	GND	Y34
				G28	GND	GND	Y35
				F20	GND	GND	Y37
				AV28	GND	GND	Y38
				AV32	GND	GND	AB17
				AV36	GND	GND	AB16
				AV4	GND	GND	AN26
				AV7	GND	GND	AD7
				AW11	GND	GND	M11
				G20	GND	GND	AA4
				AR43	GND	GND	AB19
				AW43	GND	GND	AY13
				AY10	GND	GND	P11
				AV12	GND	GND	Y6
				AY30	GND	GND	T11
				AY33	GND	GND	V11
				AY34	GND	GND	Y11
				AY37	GND	GND	AH16
				AY38	GND	GND	T22
				AY41	GND		

I77

0918_Michael:Add C743 0.1U and C744 2200P reserve decoupling cap for EMI

FDN357N: Vgs(th) -- 1 V(Min), 1.6 V(Typ), 2 V(Max)
Rds(on) -- 81m @Vgs = 4.5 V
Id -- 1.9 A(Max, continuous)

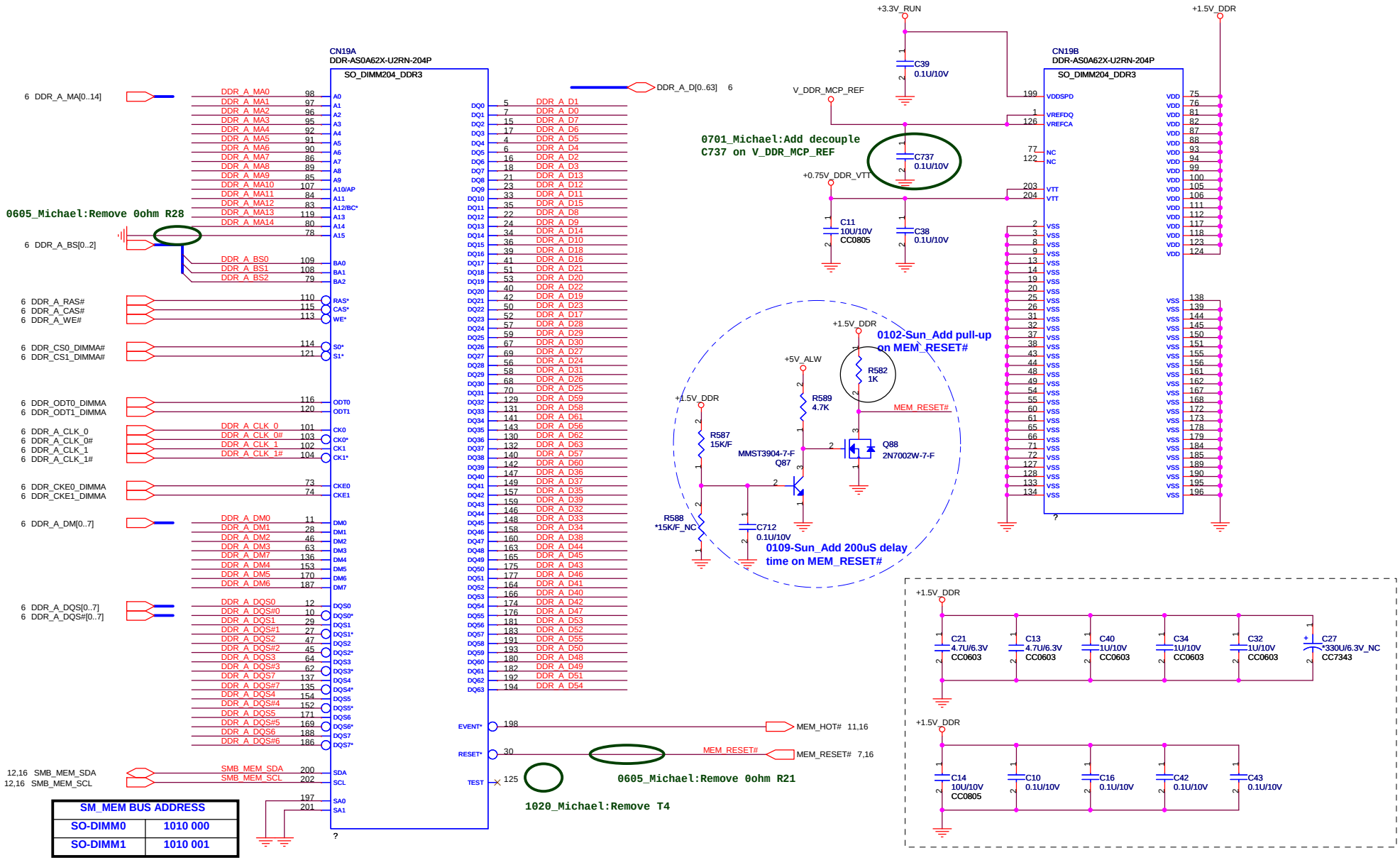


0229-Sun_1.1V_RMGT & +3.3V_RMGT MOSFET Vgs aren't enough issue, modify circuit reference NV CRB (Del JP11,JP12
Change Q57 from SI2304BDS-T1-E3 to FDN357N, Q58 from SI2304BDS-T1-E3 to SI2301BDS-T1-E3
Add Q89 with 2N7002,R591 with 10K)

0825_Michael:Change Q58 type from SI2301BDS to FDN357N and add MOS 2N7002W-7-F,R&C for +1.1V_RMGT and +3.3V_RMGT power low issue

QUANTA COMPUTER

Title	MCP79 (GND)		
Size	Document Number IM3 (XPS-Jolie)		Rev 2A
Date: Friday, September 19, 2008		Sheet 14 of 59	

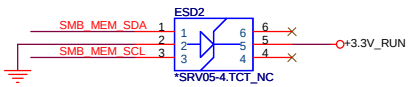


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

For EMI Reserved

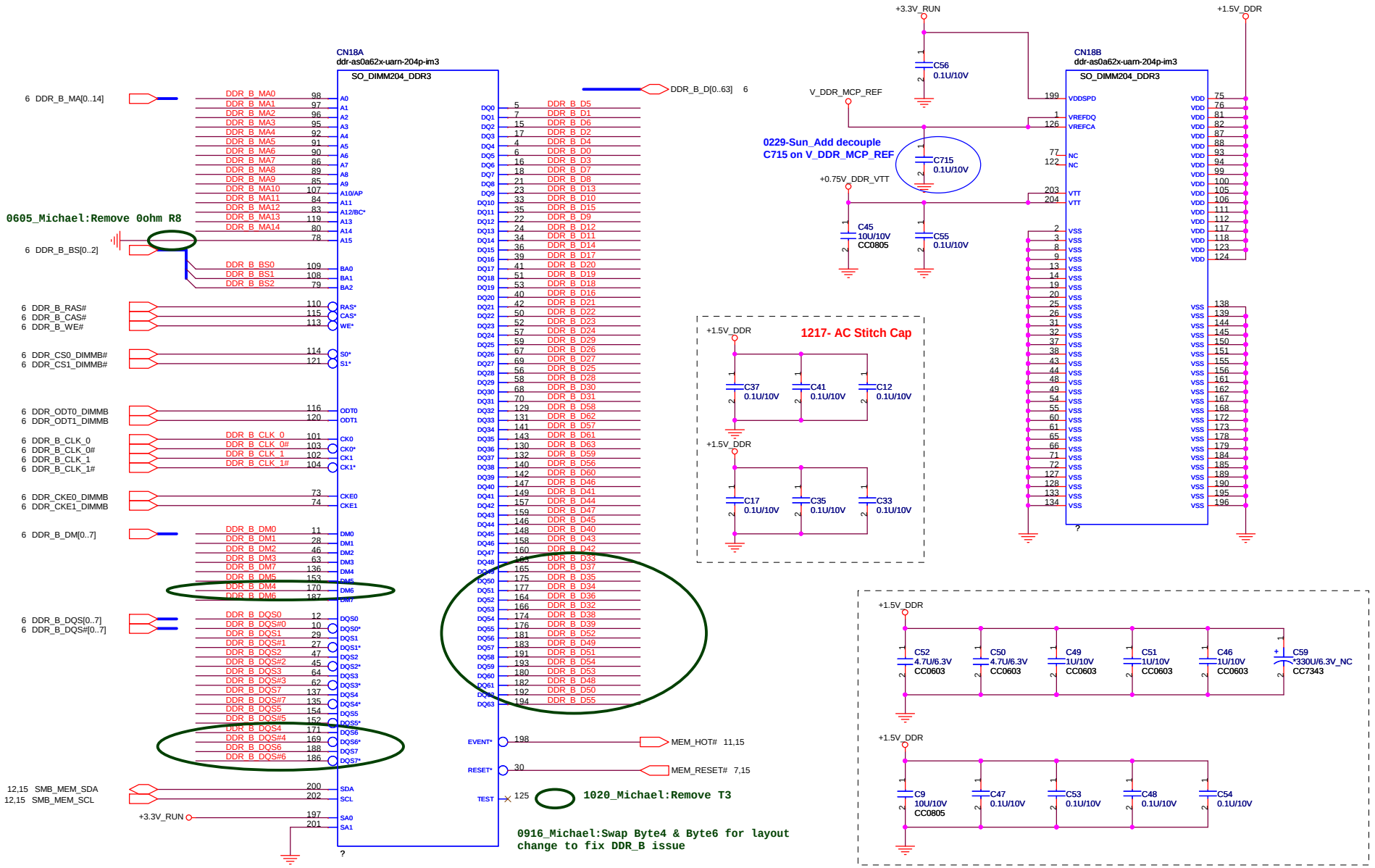
DDR_A_CLK_1 R19 1 2 *200/F_NC DDR_A_CLK_1#
DDR_A_CLK_0 R30 1 2 *200/F_NC DDR_A_CLK_0#

Place ESD Protection diodes.



QUANTA COMPUTER

Title	DDR3 SO-DIMM (204P)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Monday, October 20, 2008	Sheet 15 of 59	



Title	DDR3 SO-DIMM (204P)
Size	Document Number: IM3 (XPS-Jolie)
Rev	2A
Date:	Monday, October 20, 2008
Sheet	16 of 59

QUANTA COMPUTER

IM3 dedicated.

1113-Sun_Swap PEG for routing smooth.

1115-Sun_Follow NV's command to swap PEG for routing

U20A

PART 1 OF 5

PCI-EXPRESS INTERFACE

8 PCIE_MTX_GRX_P[0..15]
8 PCIE_MTX_GRX_N[0..15]

PCIE_MTX_GRX_P15 AE12
PCIE_MTX_GRX_N15 AE12
PCIE_MTX_GRX_P14 AG12
PCIE_MTX_GRX_N14 AG13
PCIE_MTX_GRX_P13 AE13
PCIE_MTX_GRX_N13 AE13
PCIE_MTX_GRX_P12 AE15
PCIE_MTX_GRX_N12 AF15
PCIE_MTX_GRX_P11 AG15
PCIE_MTX_GRX_N11 AG16
PCIE_MTX_GRX_P10 AF16
PCIE_MTX_GRX_N10 AE16
PCIE_MTX_GRX_P9 AE18
PCIE_MTX_GRX_N9 AF18
PCIE_MTX_GRX_P8 AG18
PCIE_MTX_GRX_N8 AG19
PCIE_MTX_GRX_P7 AF19
PCIE_MTX_GRX_N7 AE19
PCIE_MTX_GRX_P6 AE21
PCIE_MTX_GRX_N6 AF21
PCIE_MTX_GRX_P5 AG21
PCIE_MTX_GRX_N5 AG22
PCIE_MTX_GRX_P4 AF22
PCIE_MTX_GRX_N4 AE22
PCIE_MTX_GRX_P3 AE24
PCIE_MTX_GRX_N3 AF24
PCIE_MTX_GRX_P2 AG24
PCIE_MTX_GRX_N2 AF25
PCIE_MTX_GRX_P1 AG25
PCIE_MTX_GRX_N1 AG26
PCIE_MTX_GRX_P0 AF27
PCIE_MTX_GRX_N0 AE27

PEX_RX0 PEX_RX0* PEX_RX1 PEX_RX1* PEX_RX2 PEX_RX2* PEX_RX3 PEX_RX3* PEX_RX4 PEX_RX4* PEX_RX5 PEX_RX5* PEX_RX6 PEX_RX6* PEX_RX7 PEX_RX7*
PEX_RX8 PEX_RX8* PEX_RX9 PEX_RX9* PEX_RX10 PEX_RX10* PEX_RX11 PEX_RX11* PEX_RX12 PEX_RX12* PEX_RX13 PEX_RX13* PEX_RX14 PEX_RX14* PEX_RX15 PEX_RX15*

PEX_TX0 PEX_TX0* PEX_TX1 PEX_TX1* PEX_TX2 PEX_TX2* PEX_TX3 PEX_TX3* PEX_TX4 PEX_TX4* PEX_TX5 PEX_TX5* PEX_TX6 PEX_TX6* PEX_TX7 PEX_TX7*
PEX_TX8 PEX_TX8* PEX_TX9 PEX_TX9* PEX_TX10 PEX_TX10* PEX_TX11 PEX_TX11* PEX_TX12 PEX_TX12* PEX_TX13 PEX_TX13* PEX_TX14 PEX_TX14* PEX_TX15 PEX_TX15*

AD10 PCIE_MRX_GTX_C_P15 C142 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P15
AD11 PCIE_MRX_GTX_C_N15 C155 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N15
AD12 PCIE_MRX_GTX_C_P14 C163 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P14
AC12 PCIE_MRX_GTX_C_N14 C171 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N14
AB11 PCIE_MRX_GTX_C_P13 C139 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P13
AB12 PCIE_MRX_GTX_C_N13 C128 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N13
AD13 PCIE_MRX_GTX_C_P12 C181 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P12
AD14 PCIE_MRX_GTX_C_N12 C190 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N12
AD15 PCIE_MRX_GTX_C_P11 C191 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P11
AC15 PCIE_MRX_GTX_C_N11 C201 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N11
AB14 PCIE_MRX_GTX_C_P10 C172 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P10
AB15 PCIE_MRX_GTX_C_N10 C179 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N10
AC16 PCIE_MRX_GTX_C_P9 C222 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P9
AD16 PCIE_MRX_GTX_C_N9 C215 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N9
AD17 PCIE_MRX_GTX_C_P8 C224 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P8
AD18 PCIE_MRX_GTX_C_N8 C230 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N8
AC18 PCIE_MRX_GTX_C_P7 C213 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P7
AB18 PCIE_MRX_GTX_C_N7 C203 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N7
AB19 PCIE_MRX_GTX_C_P6 C247 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P6
AB20 PCIE_MRX_GTX_C_N6 C239 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N6
AD19 PCIE_MRX_GTX_C_P5 C232 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P5
AD20 PCIE_MRX_GTX_C_N5 C237 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N5
AD21 PCIE_MRX_GTX_C_P4 C290 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P4
AC21 PCIE_MRX_GTX_C_N4 C296 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N4
AB21 PCIE_MRX_GTX_C_P3 C301 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P3
AB22 PCIE_MRX_GTX_C_N3 C309 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N3
AC22 PCIE_MRX_GTX_C_P2 C248 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P2
AD22 PCIE_MRX_GTX_C_N2 C259 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N2
AD23 PCIE_MRX_GTX_C_P1 C271 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P1
AD24 PCIE_MRX_GTX_C_N1 C286 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N1
AE25 PCIE_MRX_GTX_C_P0 C264 1 2 0.1U/10V_DIS PCIE_MRX_GTX_P0
AE26 PCIE_MRX_GTX_C_N0 C268 1 2 0.1U/10V_DIS PCIE_MRX_GTX_N0

PCIE_MRX_GTX_P[0..15] 8
PCIE_MRX_GTX_N[0..15] 8

8 CLK_PCIE_VGA AB10
8 CLK_PCIE_VGA# AC10
PEX_REFCLK
PEX_REFCLK*

PEX_TSTCLK_OUT
PEX_TSTCLK_OUT*

AE10 PEX_TSTCLK_OUT R381 2 1 200/F_DIS
AE10 PEX_TSTCLK_OUT#

1115-Sun_Follow NV's command to swap PEG for routing smooth

8,32,33,34,36 PE_RESET#
8 PE_RESET_MXM#
R382 1 2 *0_NC
AD9 PEX_RST*

PEX_TERMP
AG10 PEX_TERMP R362 1 2 2.49K/F_DIS

GPIO

GPIO0 N1
GPIO1 G1
GPIO2 C1
GPIO3 M2
GPIO4 M3
GPIO5 K3
GPIO6 K2
GPIO7 J2
GPIO8 C2
GPIO9 M1
GPIO10 D2
GPIO11 D1
GPIO12 J3
GPIO13 J1
GPIO14 K1
GPIO15 F3
GPIO16 G3
GPIO17 G2
GPIO18 F1
GPIO19 F2

ROM_CS* B10
ROM_SI A10
ROM_SO C10
ROM_SCLK C9

R110 30K/F_DIS
R115 1 2 5.1K/F_DIS
R106 1 2 15K/F_DIS
+3.3V_NB9X

I2CH_SCL A3
I2CH_SDA A4

BUFRST* N5

R81 2 1 10K_DIS
R92 2 1 10K_DIS

53 GFX_CORE_CNTRL0
53 GFX_CORE_CNTRL1
19 GFX_THERM#
+3.3V_NB9X
R73 2 1 10K_DIS
R398 1 2 0_DIS
19 GFX_THERM_ALERT#
20,21 GDDR3_VREF_SW

PAD T47
PAD T49

0904_Michael:Add R398 on GFX_THERM# and change port type from input to output

+3.3V_NB9X
R108 43K/F_DIS C7
R102 2 1 10K_DIS B9
R116 1 2 5.1K/F_DIS A9
R119 1 2 39K/F_DIS F11
R104 1 2 39K/F_DIS F10

STRAP0
STRAP1
STRAP2
STRAP_REF_3V3
STRAP_REF_MIOB

JTAG

R167 2 1 10K_DIS AD25
TESTMODE

GPU_JTAG_TCLK AF3
GPU_JTAG_TMS AF4
GPU_JTAG_TDI AG4
GPU_JTAG_TDO AE4
GPU_JTAG_TRST# AG3

JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST*

NC_01 C15
NC_02 D15
NC_03 E15
NC_04 F6
NC_05 J5
NC_06 T6
NC_07 AA6
NC_08 AC19
NC_09 AE9
NC_10 AG9

NB9M_DIS
PBGA533-NVIDIA-GEFORCE6250
Footprint: BGA533-NVIDIA-NB9M-GS

VRAM Strap:ROM_SI

ID	ROM_SI	Memory part
01	Pull down 30K	Qimonda 32M*32
02	Pull down 45K	Samsung 32M*32
	QPN:CS34532FB18	
03		

0604_Michael: Follow NV command to modify VRAM Strap resistor vaule

GPIO USAGE

GPIO	I/O	ACTIVE	USAGE	Used
0	IN	N/A	NVGEM HOTPLUG DETECT	
1	IN	N/A	DVI/HDMI LINKC HOTPLUG DETECT	
2	OUT	HIGH	PANEL BACKLIGHT PWM	
3	OUT	HIGH	PANEL POWER ENABLE	
4	OUT	HIGH	PANEL BACKLIGHT ENABLE	
5	OUT	HIGH	NVVDD ALTV0	
6	OUT	HIGH	NVVDD ALTV1	
7	OUT	HIGH	FBVDD VID0	
8	IN	LOW	OVERTEMP ALERT	
9	OUT	LOW	THERMAL ALERT	
10	OUT	HIGH	DYNAMIC FB VREF GDDR3 (not used for DDR2)	
11	OUT	HIGH	SLI SYNC0 (not used for GB1-64)	
12	IN	N/A	AC DETECT	
13	OUT	LOW	POWER SUPPLY CONTROL0	
14	OUT	HIGH	POWER SUPPLY CONTROL1	
15	IN	N/A	HPD_E	
16	IN	N/A	DVI_E	No
17	IN	N/A	HDMI_E	No
18	IN	N/A	DVI_F (not used)	No
19	IN	N/A	HDMI_F (not used)	No

Place together.

JTAG I/F

+3.3V_NB9X
R360 10K_DIS
R359 10K_DIS
GPU_JTAG_TMS
GPU_JTAG_TDI
GPU_JTAG_TDO
T54 PAD
GPU_JTAG_TCLK
GPU_JTAG_TRST#
R88 10K_DIS
R61 10K_DIS

GPU THERMTRIP Circuit

+3.3V_NB9X
R540 10M_DIS
GFX_THERMTRIP# 52
Q43 2N7002W-7-F_DIS
1022_Michael:Add R437 for voltage low issue
GFX_THERM#
R437 1 2 4.7K_DIS
Q18 MMST3904-7-F_DIS
C459 0.1U_DIS 10

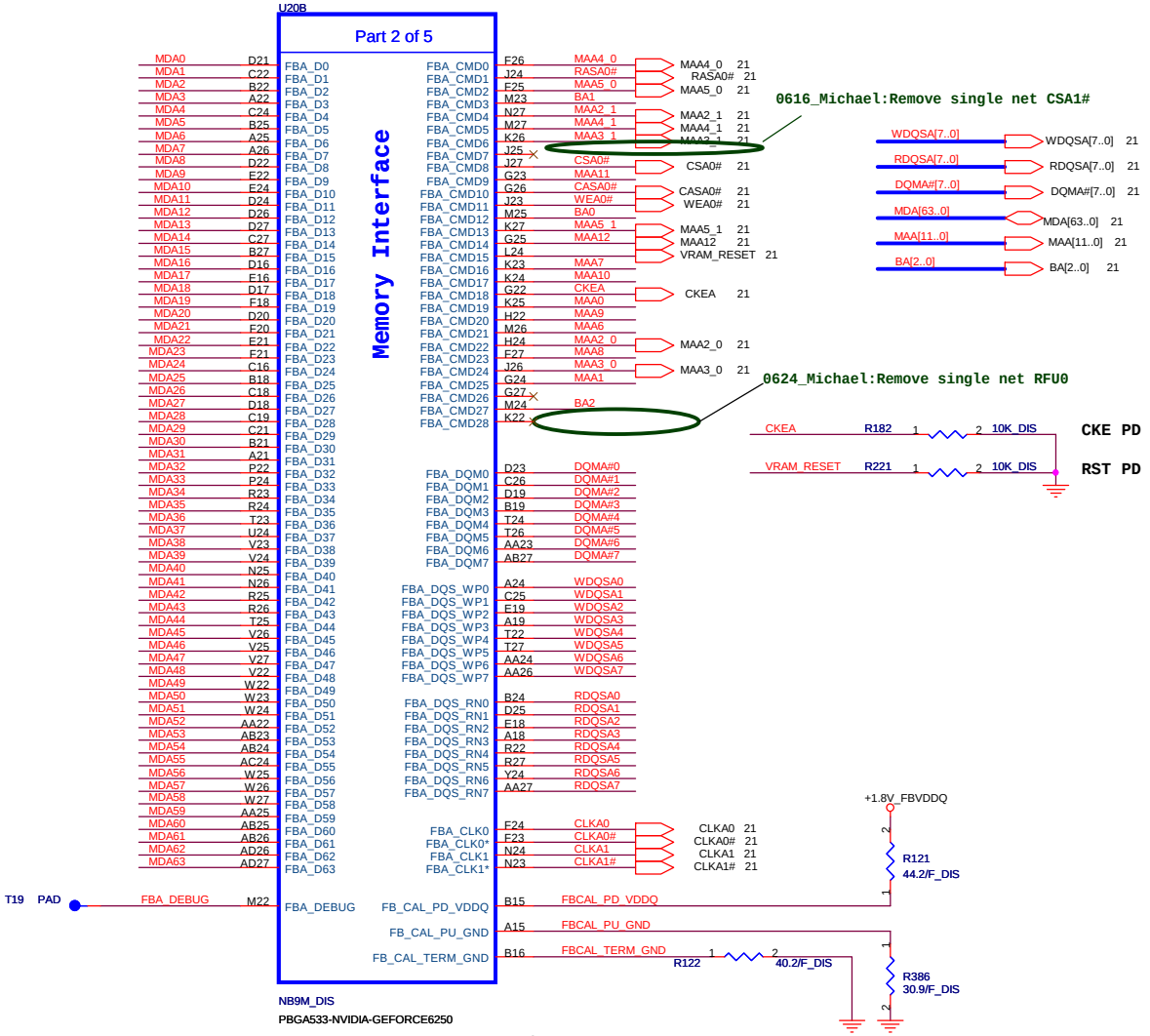
0825_Michael:Modify THERMTRIP circuit,add MOS and CAP

QUANTA COMPUTER

Title: VGA-NB9X GB1-64 (PCIE,PCIE POWER)

Size: | Document Number: IM3 (XPS-Jolie) | Rev: 2A

Date: Thursday, October 23, 2008 | Sheet 17 of 59



Update as "PUN-03303-001_V01".

GPU Driver Calibration			
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ
DDR2	1.8V	30.1	30.1
GDDR3	1.8V	30.9	44.2
GDDR3 DVS	1.8V/1.5V	30.9	44.2

Note: Use only 1% resistors for driver calibration

QUANTA COMPUTER

Title	VGA-NB9X GB1-128 (Frame Buffer Channel A)	
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet 18 of 59	

0627_Michael:Change GPU_Thermal control from SMBus2 to SMBus0

0807_Change R361, R44 from 4.7k to 47k for battery issue

+3.3V_NB9X

R361 47K_DIS

R44 47K_DIS

36,48,55 SMBCLK0

36,48,55 SMBDAT0

GFX_SCLK

GFX_SDATA

Q6 2N7002W-7-F_DIS

Q5 2N7002W-7-F_DIS

THERMAL MONITOR

0708_Michael:Depop U18 circuit for nternal thermal monitor

R54 *10K_NC

R45 *0_NC

17 GFX_THERM_ALERT#

U18 *ADM1032ARM_NC

SCLK SDATA ALERT# GND VDD D+ D- THERM#

C493 *2200P/50V_NC 50

C494 *0.1U/10V_NC

GFX_THERMDP GFX_THERMDN GFX_THERM# 17

0309-Sun_Pop R45 for GFX_THERM_ALERT#

0605_Michael: Add R56 connect to GFX_THERM#

0904_Michael:Remove R56 and change port type from output to input

0708_Michael:Pop R46 & R47 for nternal thermal monitor

R46 0_DIS

R47 0_DIS

R86 R87 R82 R83 R72 R71 R90 R91 R84 R62 10K_DIS

0701_Michael:Remove SPREAD SPECTRUM circuit

Y1 27MHZ_DIS XTL-8X4_5-6_5

R96 1M_DIS

C113 22P/50V_DIS 50

C107 22P/50V_DIS 50

GXTAL_IN GXTAL_OUT

0709-Steg: Change CAP Value from 18p to 22p

U20C

PART 3 OF 5

DVI: IFPC_AUX* IFPC_AUX IFPC_L3* IFPC_L3 IFPC_L2* IFPC_L2 IFPC_L1* IFPC_L1 IFPC_L0* IFPC_L0 IFPC_RSET

DP Port: IFPE_L0 IFPE_L0* IFPE_L1 IFPE_L1* IFPE_L2 IFPE_L2* IFPE_L3 IFPE_L3* IFPE_AUX IFPE_AUX* IFPE_RSET

HDA: HDA_BCLK HDA_SYNC HDA_SDI HDA_SDO HDA_RST* SPDIF

THERMAL: THERMDP THERMDN I2CS_SDA I2CS_SCL

SERIAL BUS: I2CE_SDA I2CE_SCL I2CD_SDA I2CD_SCL I2CC_SDA I2CC_SCL I2CB_SDA I2CB_SCL I2CA_SDA I2CA_SCL

Clock: XTAL_SSIN XTAL_OUTBUFF XTAL_IN XTAL_OUT NB9M_DIS

LVDS: IFPA_TXD0 IFPA_TXD0* IFPA_TXD1 IFPA_TXD1* IFPA_TXD2 IFPA_TXD2* IFPA_TXD3 IFPA_TXD3* IFPA_TXC IFPA_TXC* IFPB_TXD4 IFPB_TXD4* IFPB_TXD5 IFPB_TXD5* IFPB_TXD6 IFPB_TXD6* IFPB_TXD7 IFPB_TXD7* IFPB_TXC IFPB_TXC* IFPAB_RSET

DACA: DACA_RED DACA_GREEN DACA_BLUE DACA_HSYNC DACA_VSYNC DACA_VDD DACA_VREF DACA_RSET

R41 10K_DIS

DACB: DACB_RED DACB_GREEN DACB_BLUE DACB_CSYNC DACB_VDD DACB_VREF DACB_RSET

R101 10K_DIS

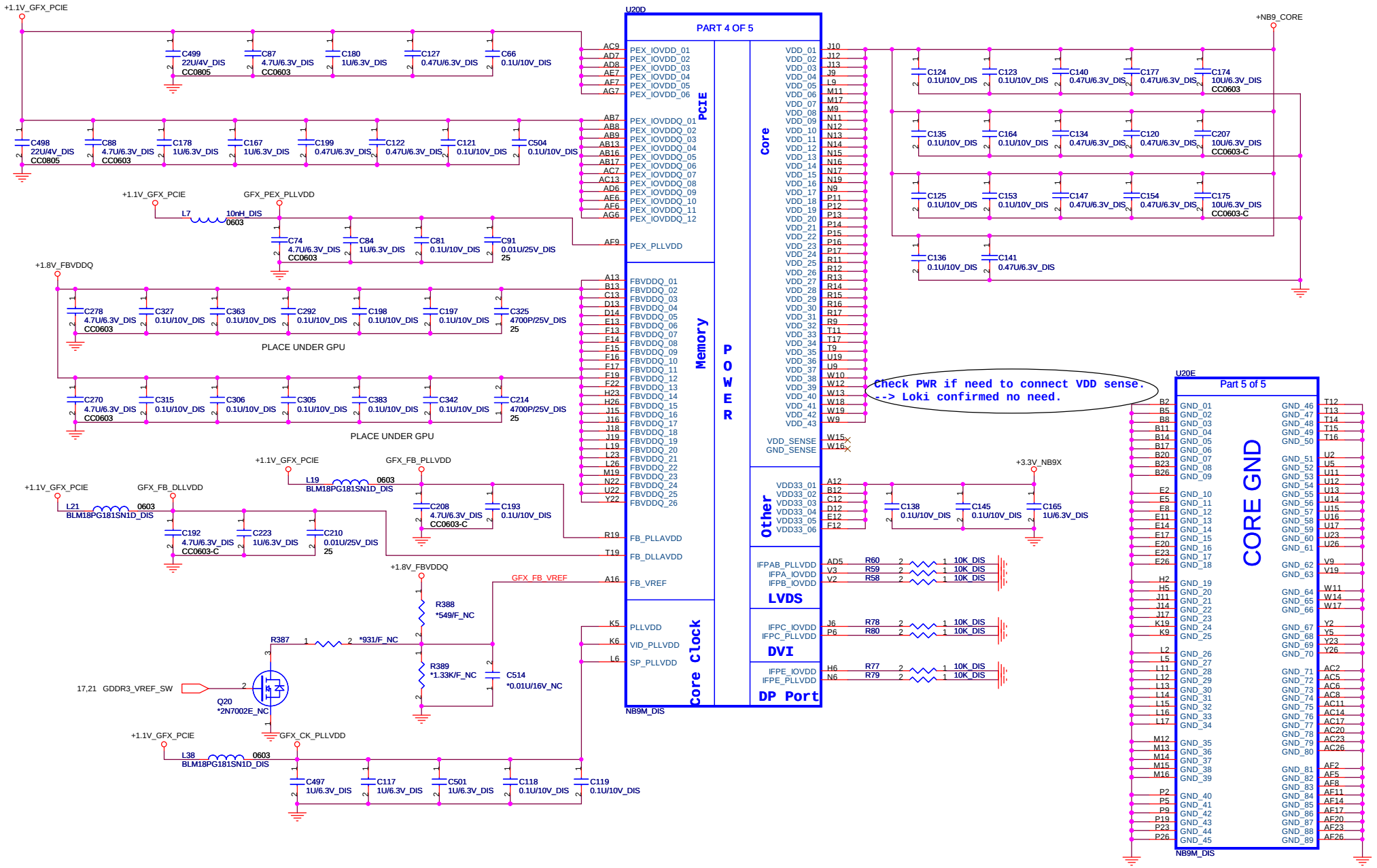
DACC: DACC_RED DACC_GREEN DACC_BLUE DACC_HSYNC DACC_VSYNC DACC_VDD DACC_VREF DACC_RSET

R85 10K_DIS

Reserve CRT for debug on first build.
Remove all of parts except DACA_VDD supply before QT
1020_Michael:Remove T48,T52,T50,T53,T51,R49,C89,R89

QUANTA COMPUTER

Title	VGA-NB9X GB1-64 (OUTPUT)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Monday, October 20, 2008	Sheet 19 of 59	



Title	VGA-NB9X GB1-64 (POWER,GND)
Size	Document Number IM3 (XPS-Jolie) Rev 2A
Date:	Friday, September 05, 2008 Sheet 20 of 59

QUANTA COMPUTER

GDDR3 _M*32

U23

GDDRIII_*32

GDDR3_*32_DIS

PBGA136-SAMSUNG-K4J52324QC-WK1

U24

GDDRIII_*32

GDDR3_*32_DIS

PBGA136-SAMSUNG-K4J52324QC-WK1

1114-Sun_Swap GDDR3 Data for routing smooth.

1114-Sun_Swap GDDR3 Data for routing smooth.

1114-Sun_Swap GDDR3 Data for routing smooth.

1114-Sun_Swap GDDR3 Data for routing smooth.

0604_Michael: Follow NV command pop 0ohm resistor R164

0112-Stanley: Change P/N to DDS: BSS138-7-F.

Title	VGA-NB9X GB1-64 (HybridSLI SWITCH)
Size	Document Number: IM3 (XPS-Jolie) — Rev: 2A
Date:	Monday, September 22, 2008 — Sheet 21 of 59

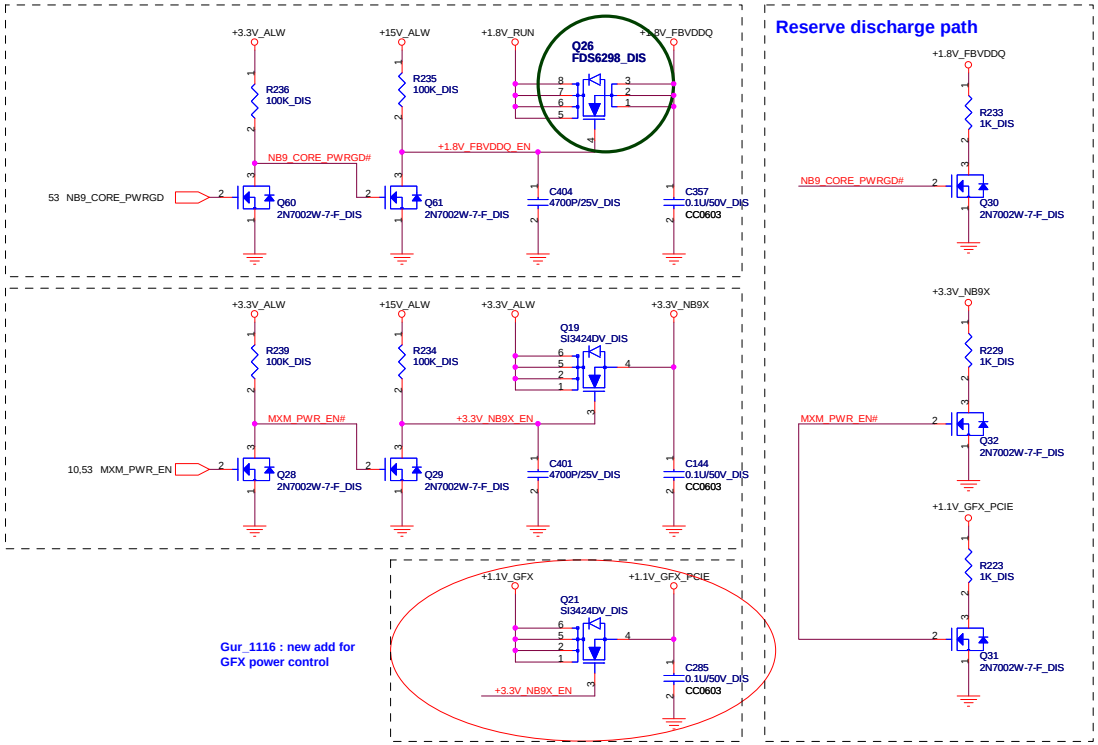
QUANTA COMPUTER

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE

QUANTA COMPUTER

Title		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 22 of 59	

1225-Sun_Chenge Q26 from SI4812BDY to SI4800BDY-T1-E3
1022_Michael:Change Q26 from SI4800BDY-T1-E3 to BAM62980005



QUANTA COMPUTER

Title	VGA-NB9X GB1-128 (PCIE,PCIE POWER)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 23 of 59	

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE

QUANTA COMPUTER

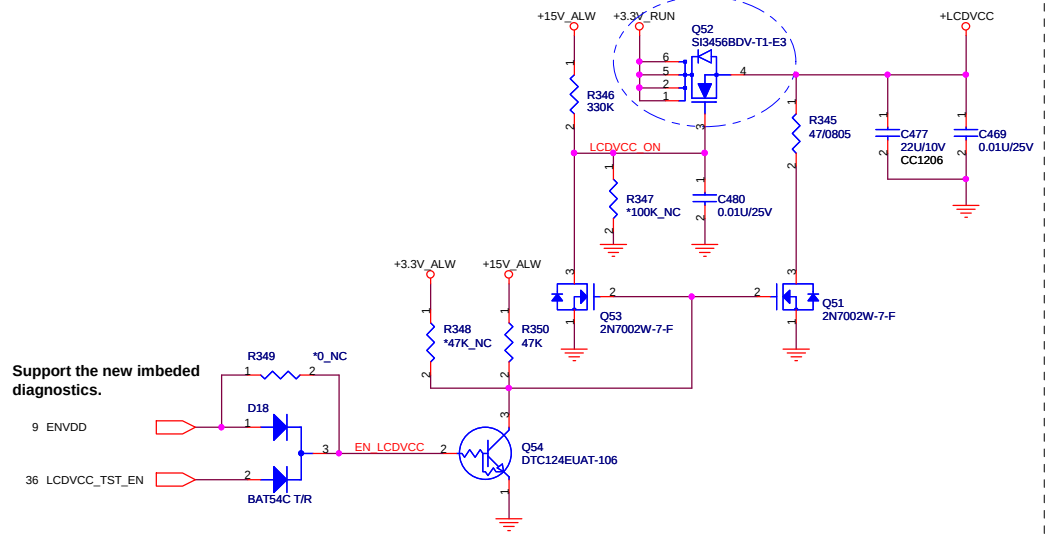
Title		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 24 of 59	

BLANK PAGE FOR PAGE NUMBER SAME AS DISCRETE

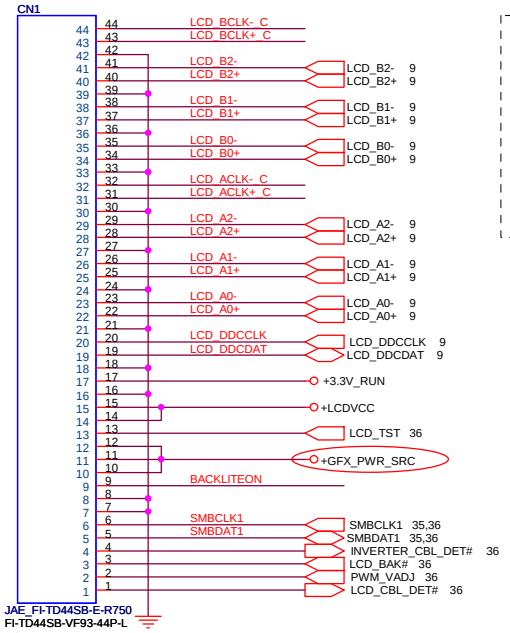
QUANTA COMPUTER

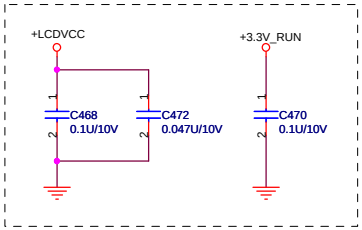
Title		
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 25 of 59	

0112-Stanley: Change BOM for EOL issue (SI3456BDV).



GND,VCC要用最粗的電子線

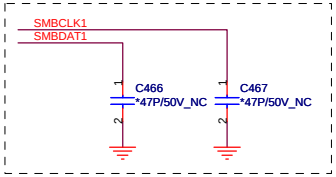




WXGA 1280*800=>70 MHz
WXGA+ 1440*900=>108 MHz
WSXGA+ 1680*1050=>120MHz
WUXGA 1920*1200=>166 MHz

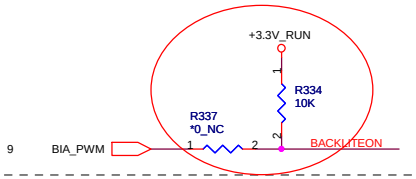
Address : A9H --Contrast
AAH --Backlight

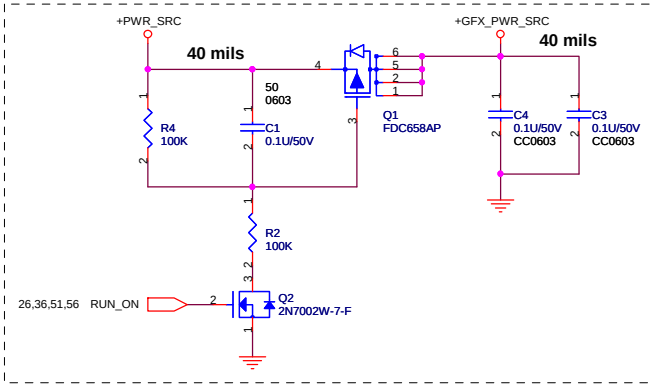
MBRAI specification of antenna gain is 10dBi@474MHz, -7dBi@698MHz, -5dBi@858MHz.



Populate R65 for DPST implementation only.

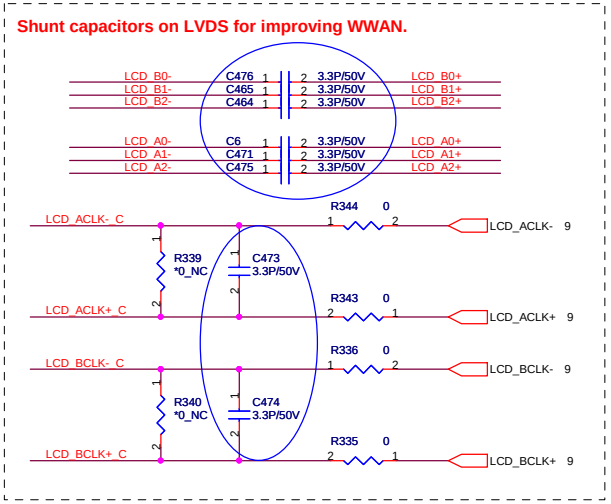
Populate R341 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.



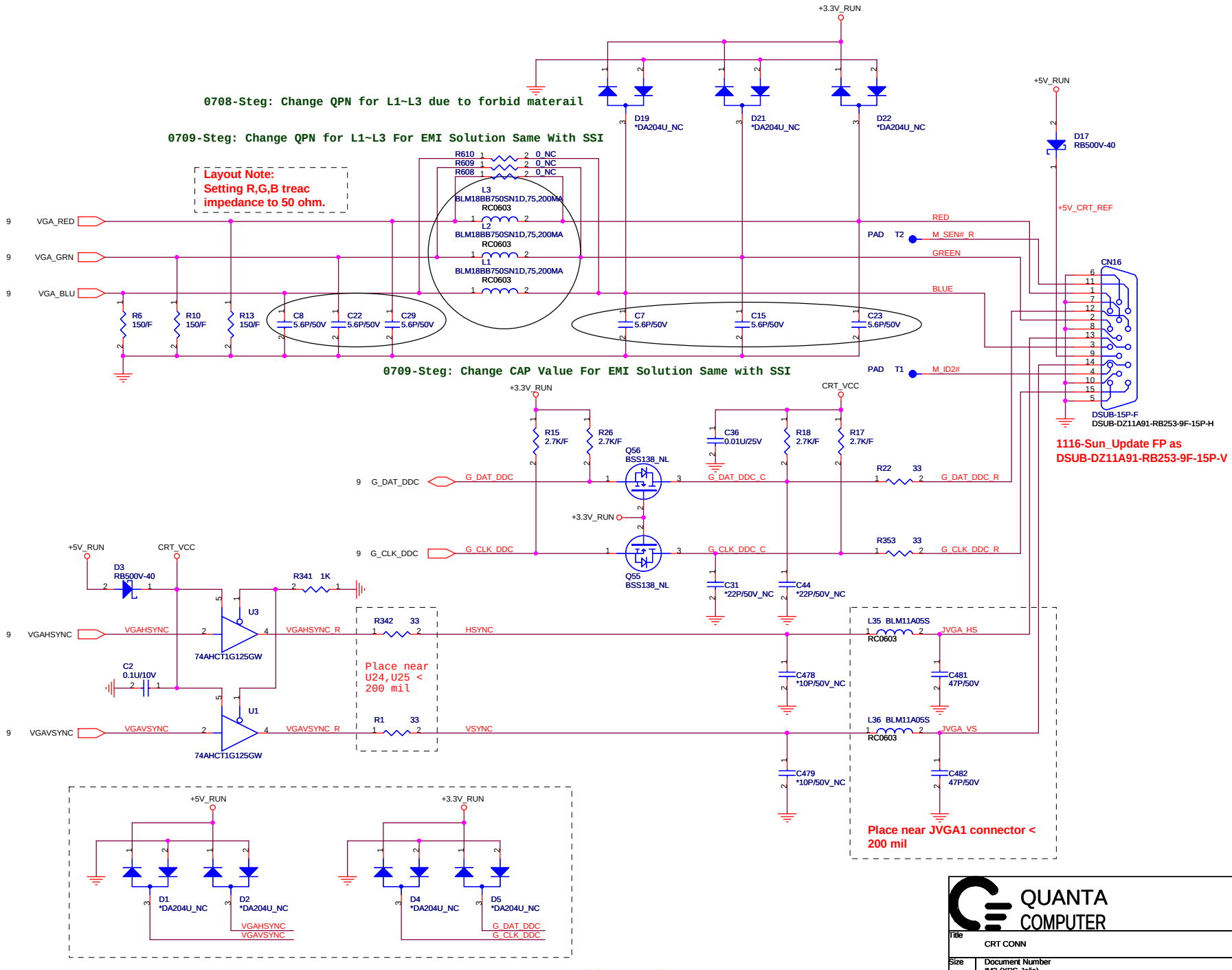


0319-Sun_Pop 3.3P on LVDS bus for COMM team demand

Shunt capacitors on LVDS for improving WWAN.

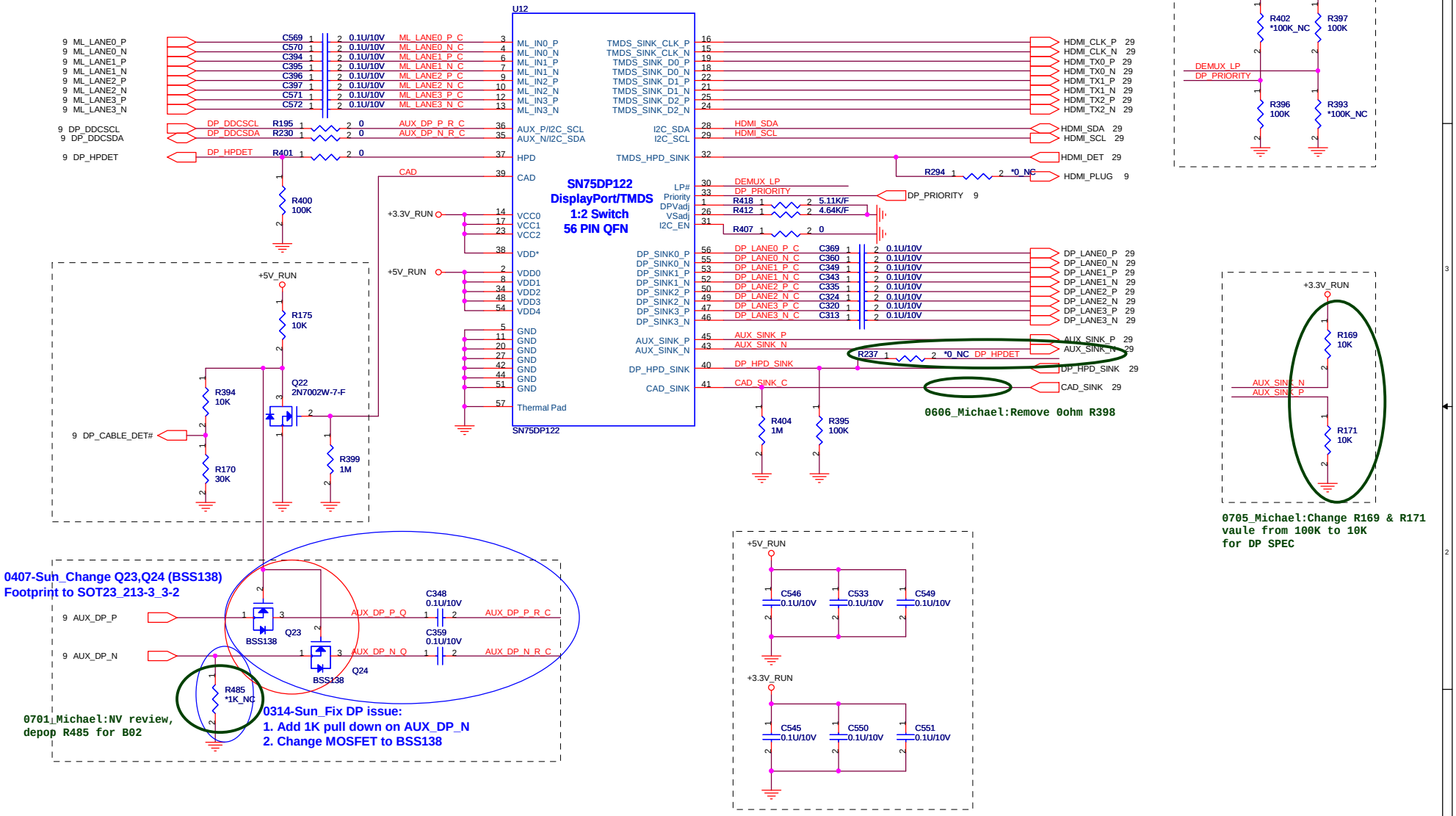


QUANTA COMPUTER		
Title: LCD CONN		
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet 26 of 59	



QUANTA COMPUTER

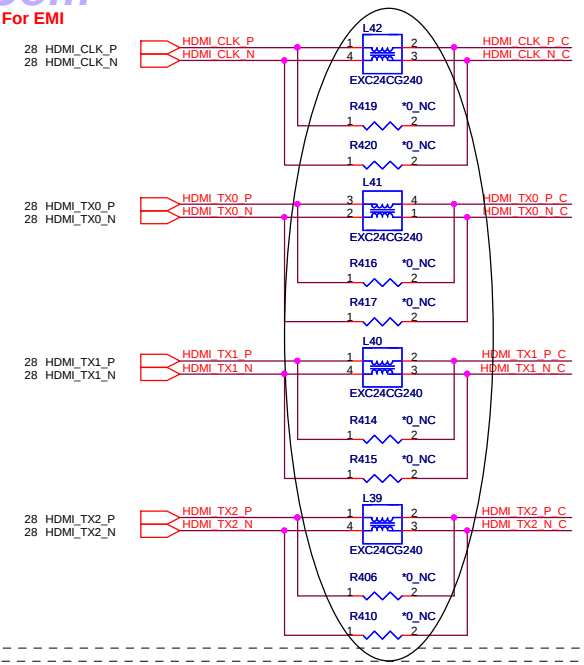
Title	CRT CONN	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 27 of 59	



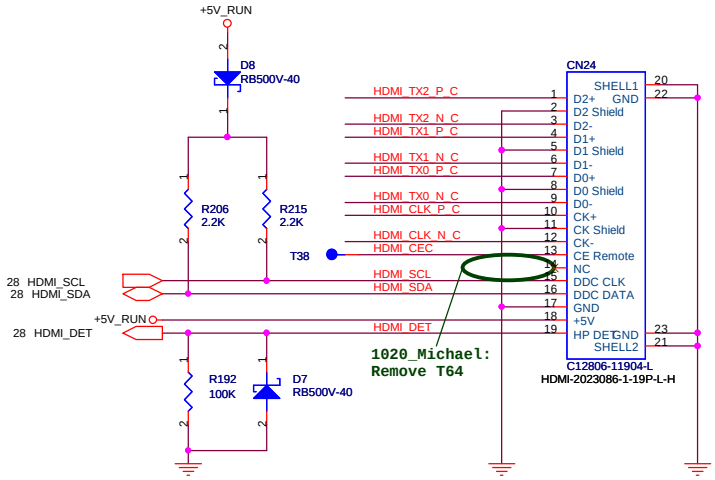
QUANTA COMPUTER		
Title	DeMUX Switch (SN75DP122)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 28 of 59	

0319-Sun_Pop EMI baed
w/EXC24CG240 for HDMI port

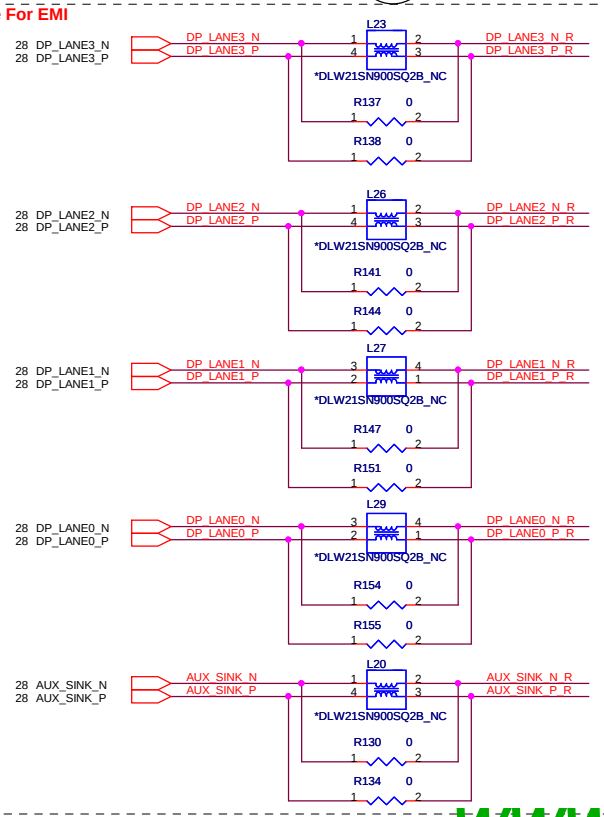
Reserve For EMI



HDMI CONNECTOR

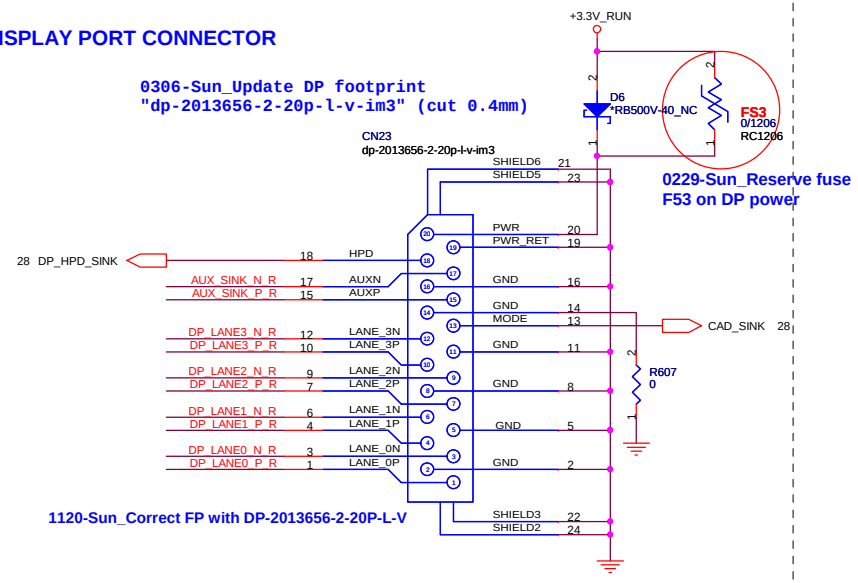


Reserve For EMI



DISPLAY PORT CONNECTOR

0306-Sun_Update DP footprint
"dp-2013656-2-20p-l-v-im3" (cut 0.4mm)



0229-Sun_Reserve fuse
F53 on DP power

1120-Sun_Correct FP with DP-2013656-2-20P-L-V

QUANTA COMPUTER

Title	HDMI & DP CONN	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Monday, October 20, 2008	Sheet 29 of 59	

QFN28-5X5-5-33P -->qfn20-4x4-5-21p-adg786

QFN28-5X5-5-33P
*MAX4951_NC

0310-Sun_Reserve ESATA repeater MAX4951.

EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

USB POWER SW

Place one 150uF cap by each USB connector.

Each channel is 1A
IM3 dedicated.

0630_Michael:Remove JP10 and FS2

TPS2062DR

1115-Sun_Change to 10U and move 150U to ESATA/B..

ESATA/B CONN

Guide pin type.

Need to stagger power & GND if not guide pin type.

HEADER 20
2006114-1-20P-L

0306-Sun_Add detect pin and Swap pin to align ESATA/B on ESATA CONN

GND,VCC要用最粗的電子線

USB BUS SW

FSUSB31K8X

0911_Michael:Add C739

0630_Michael:Modify Correct pin define
pin1=NC
pin2=HSD-
pin3=D-
pin5=D+
pin6=HSD+
pin7=OE

0318-Sun_change left USB port from port1 to port0

DLP11SN900HL2L

Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

Place ESD diodes as close as USB connector.

*SRV05-4.TCT_NC

USB POWER SW

Place one 150uF cap by each USB connector.

Each channel is 1A

0630_Michael:Remove JP9 and FS1

TPS2062DR

0111-Stanley: Change BOM from to 6.3V_3528.

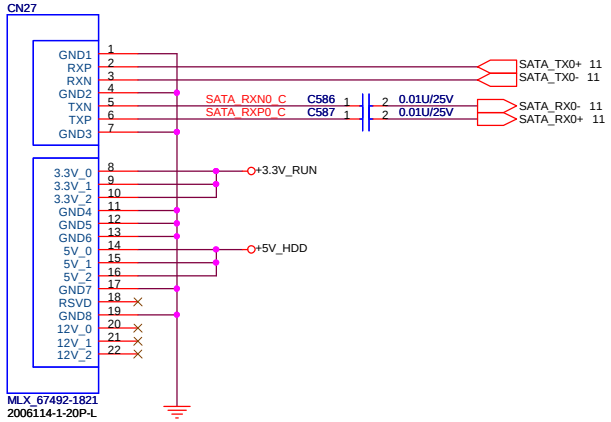
USB CONN

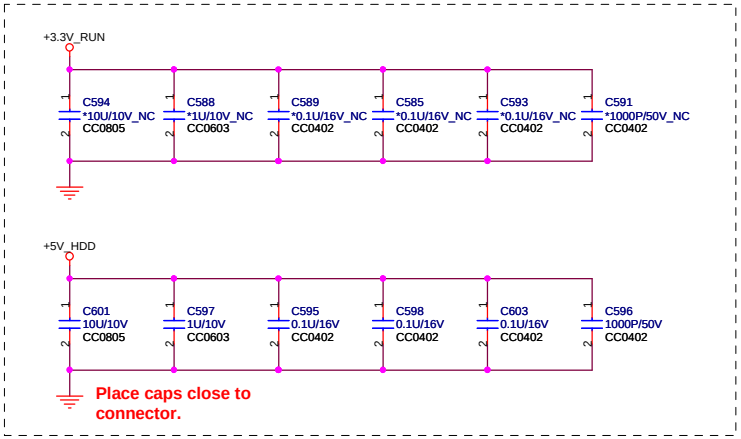
020173MR004G552ZR
USB-1775528-2-4P-R-H

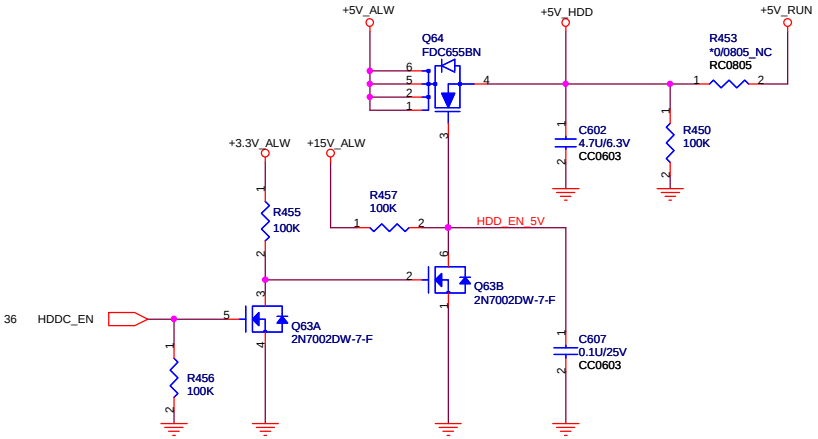
Title	USB, eSATA
Size	Document Number: IM3 (XPS-Jolie)
Rev	2A
Date:	Thursday, September 11, 2008
Sheet	30 of 59

QUANTA COMPUTER

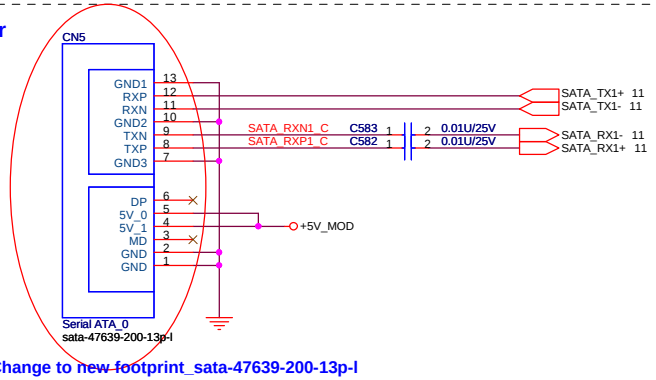
SATA HDD Connector





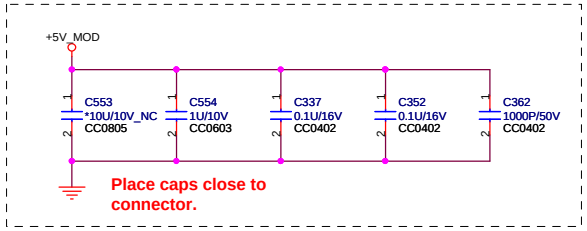


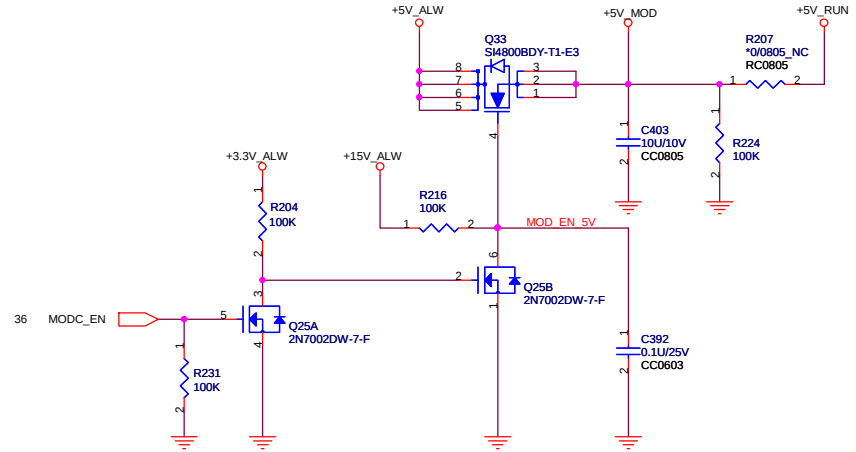
SATA ODD Connector



0306-Sun_Change to new footprint_sata-47639-200-13p-l

0407-Sun_Swap pin assignment due to pin direction is reversed



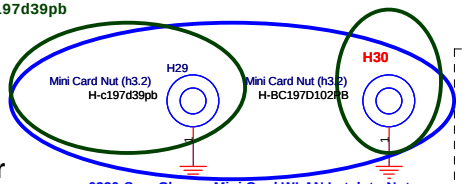


QUANTA COMPUTER

Title	SATA (HDD&CD ROM)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 31 of 59	

0829_Michael:Change Footprint from H-C197PB to H-c197d39pb

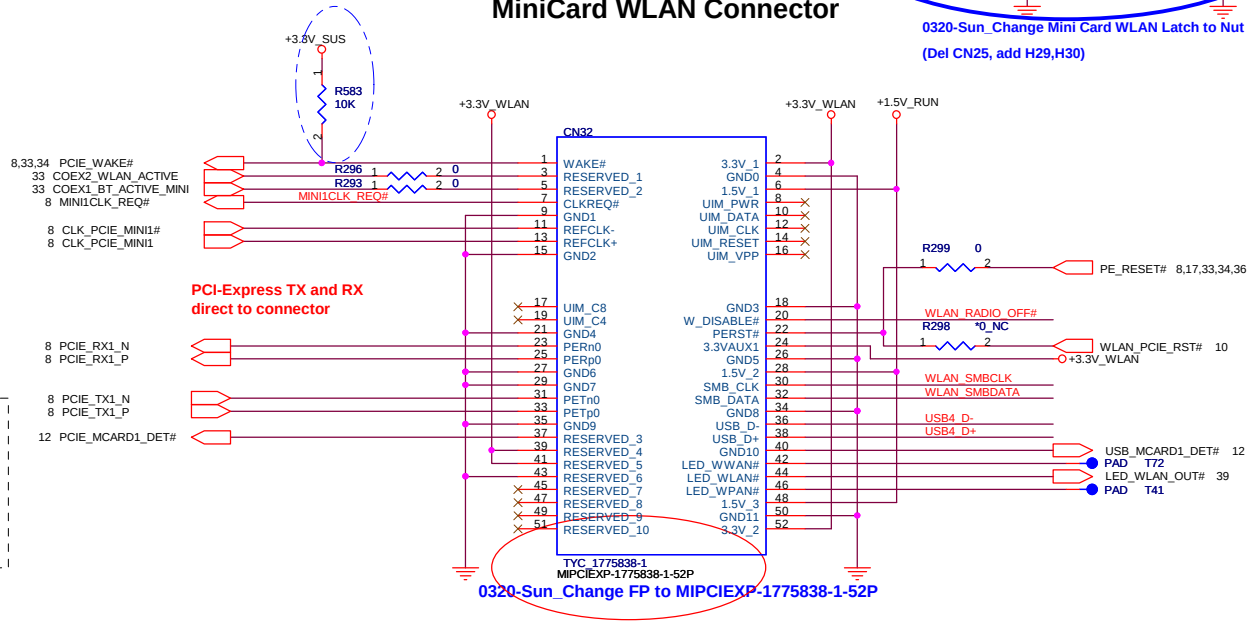
0616_Michael:Change footprint



0320-Sun_Change Mini Card WLAN Latch to Nut

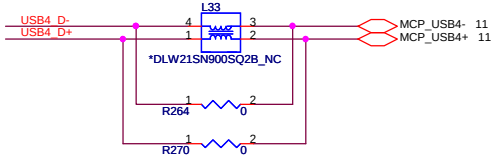
(Del CN25, add H29,H30)

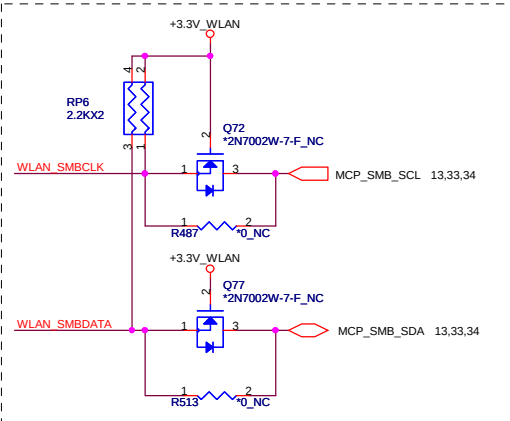
MiniCard WLAN Connector



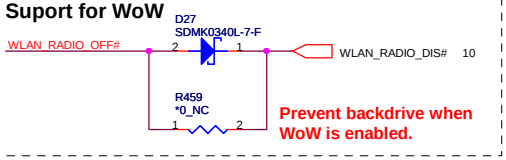
0320-Sun_Change FP to MIPCIEXP-1775838-1-52P

Reserved PAD for EMI

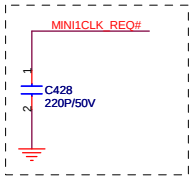


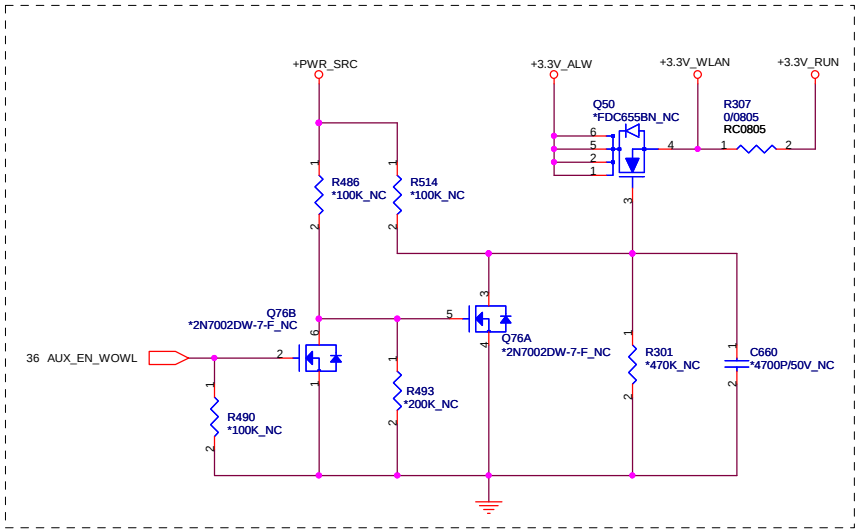


Suport for WoW

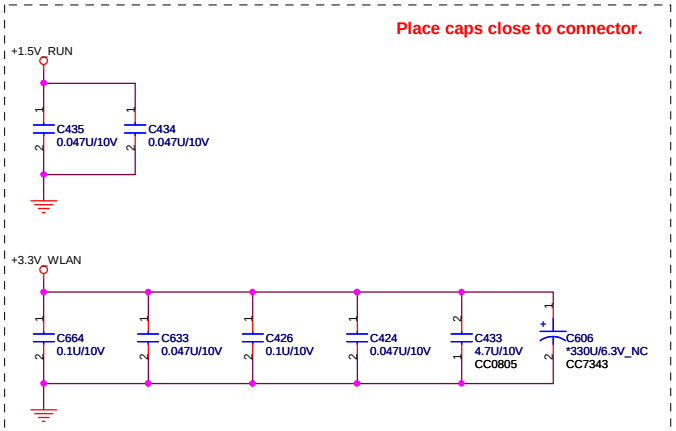


Prevent backdrive when WoW is enabled.





Place caps close to connector.



QUANTA COMPUTER

Title	MINI-CARD (WLAN)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 32 of 59	

0829_Michael:Change Footprint from H-C197PB to H-c197d39pb
0605_Michael: Del MiniCard WPAN latch add Nut H31,H32

MiniCard Robson, BT. UWB Connector

Mini Card Nut
H31 Mini Card Nut (h3.2) H-c197d39pb
H32 Mini Card Nut (h3.2) H-BC197D102PB

0606_Michael:Remove 0ohm R297,R294

CN28
TYC_1775838-1 MIPCIEXP-1775838-1-52P

8,32,34 PCIE_WAKE#
32 COEX2_WLAN_ACTIVE
32 COEX1_BT_ACTIVE_MINI
8 MINI2CLK_REQ#
8 CLK_PCIE_MINI2#
8 CLK_PCIE_MINI2
10 LPC_RESET#
36 CLK_LPC_DEBUG
8 PCIE_RX2_N
8 PCIE_RX2_P
8 PCIE_TX2_N
8 PCIE_TX2_P
12 PCIE_MCARD3_DET#

PCI-Express TX and RX direct to connector

R451 0
C436 *33P/50V_NC
R300 *100K_NC
C281 220P/50V

R286 R284 R279 R276 R273 0
LPC_LFRAME# 10,36
LPC_LAD3 10,36
LPC_LAD2 10,36
LPC_LAD1 10,36
LPC_LAD0 10,36
R268 0 PE_RESET#
R262 *0_NC
WPAN_RADIO_DIS_MINI# 10
WPAN_PCIE_RST# 10
+3.3V_RUN
MCP_SMB_SCL
MCP_SMB_SDA
USB6_D-
USB6_D+
USB_MCARD3_DET# 12
R248 0
LED_WPAN_OUT# 39

0704_Michael:Remove 0ohm R602 & R603

0829_Michael:Change Footprint from H-C197PB to H-c197d39pb
0318-Sun_Correct Nut footprint as "H-TC157BC236D102PB"
0229-Sun_Change Mini Card WWAN Latch to Nut (Del CN31, add H27,H28)

Mini Card Nut
H28 Mini Card Nut (h3.2) H-c197d39pb
H27 Mini Card Nut (h3.2) H-BC197D102PB

0616_Michael:Change footprint

MiniCard WWAN Connector

CN29
TYC_1775838-1 MIPCIEXP-1775838-1-52P

T70 PAD
T69 PAD
PCIE_WAKE#
MINI3CLK_REQ#
8 MINI3CLK_REQ#
8 CLK_PCIE_MINI3#
8 CLK_PCIE_MINI3
8 PCIE_RX3_N
8 PCIE_RX3_P
8 PCIE_TX3_N
8 PCIE_TX3_P
12 PCIE_MCARD2_DET#

0704_Michael:Add C437 on UIM_PWR

0606_Michael:Modify pin defind for 2WM610C1C-DD-7F-6P

UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP

(Place close to CN29)
C257 *15P/50V_NC
PE_RESET# 8,17,32,34,36
R452 0 PE_RESET#
R454 *0_NC
WWAN_RADIO_DIS# 10
WWAN_PCIE_RST# 10
+3.3V_RUN
MCP_SMB_SCL 13,32,34
MCP_SMB_SDA 13,32,34
USB5_D-
USB5_D+
USB_MCARD2_DET# 12
LED_WWAN_OUT# 39

CN17
2WM610C1C-DD-7F
simcard-2wm610c1c-dd-7f-6p

C437 4.7U/6.3V CC0603
C18 33P/50V
C19 33P/50V
ESD1
C24 33P/50V
C25 33P/50V
C28 1U/10V CC0603
C355 220P/50V

Place as close as possible to JMINI connector

1022_Michael:Change ESD1 PN from ALSRV054011-to-AL004220007 for EOL

0704_Michael:Add C257 on UIM_CLK

Reserve For EMI

L32 *DLW21SN900SQ2B_NC
USB6_D-
USB6_D+
MCP_USB6- 11
MCP_USB6+ 11
R254 0
R251 0

Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.

+1.5V_RUN
C409 0.047U/10V
C413 0.047U/10V

+3.3V_RUN
C604 0.1U/10V
C432 0.047U/10V
C414 0.1U/10V
C408 0.047U/10V
C590 4.7U/6.3V CC0603

1020_Michael:Remove C608 (leave empty)

Reserve For EMI

L31 *DLW21SN900SQ2B_NC
USB5_D-
USB5_D+
MCP_USB5- 11
MCP_USB5+ 11
R252 0
R249 0

Layout Note:
R240 and R244 close to choke as possible to minimize stubs.

Place caps close to connector.

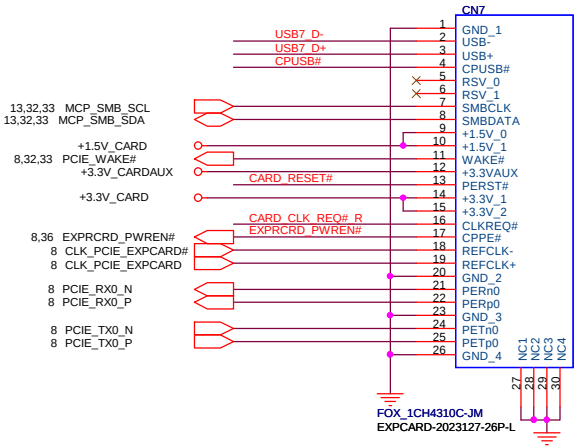
+1.5V_RUN
C429 0.047U/10V
C425 33P/50V

+3.3V_RUN
C592 33P/50V
C630 0.047U/10V
C427 33P/50V
C629 0.047U/10V
C599 330U/6.3V CC7343
C600 *330U/6.3V_NC CC7343

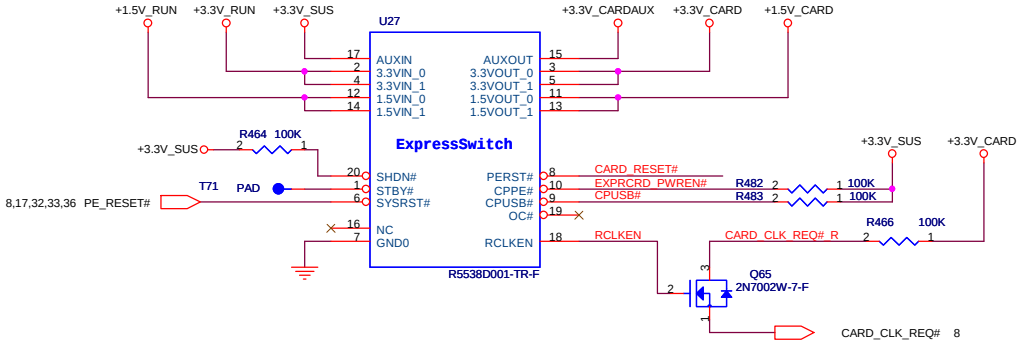
Title	MINI-CARD (WWAN,WPAN)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 33 of 59	

QUANTA COMPUTER

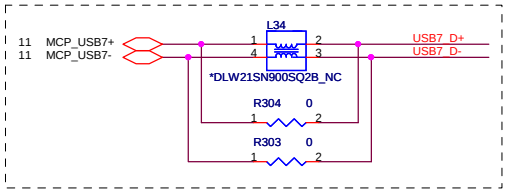
Express Card

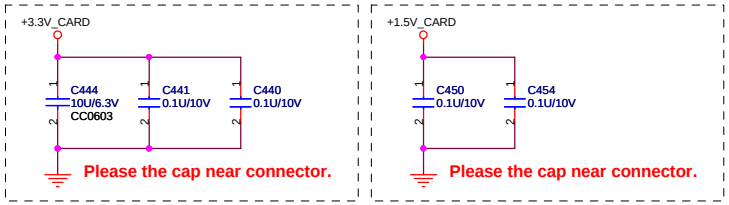


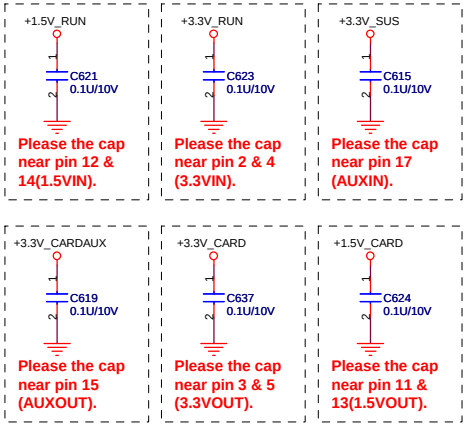
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



PCI-Express TX and RX direct to connector.

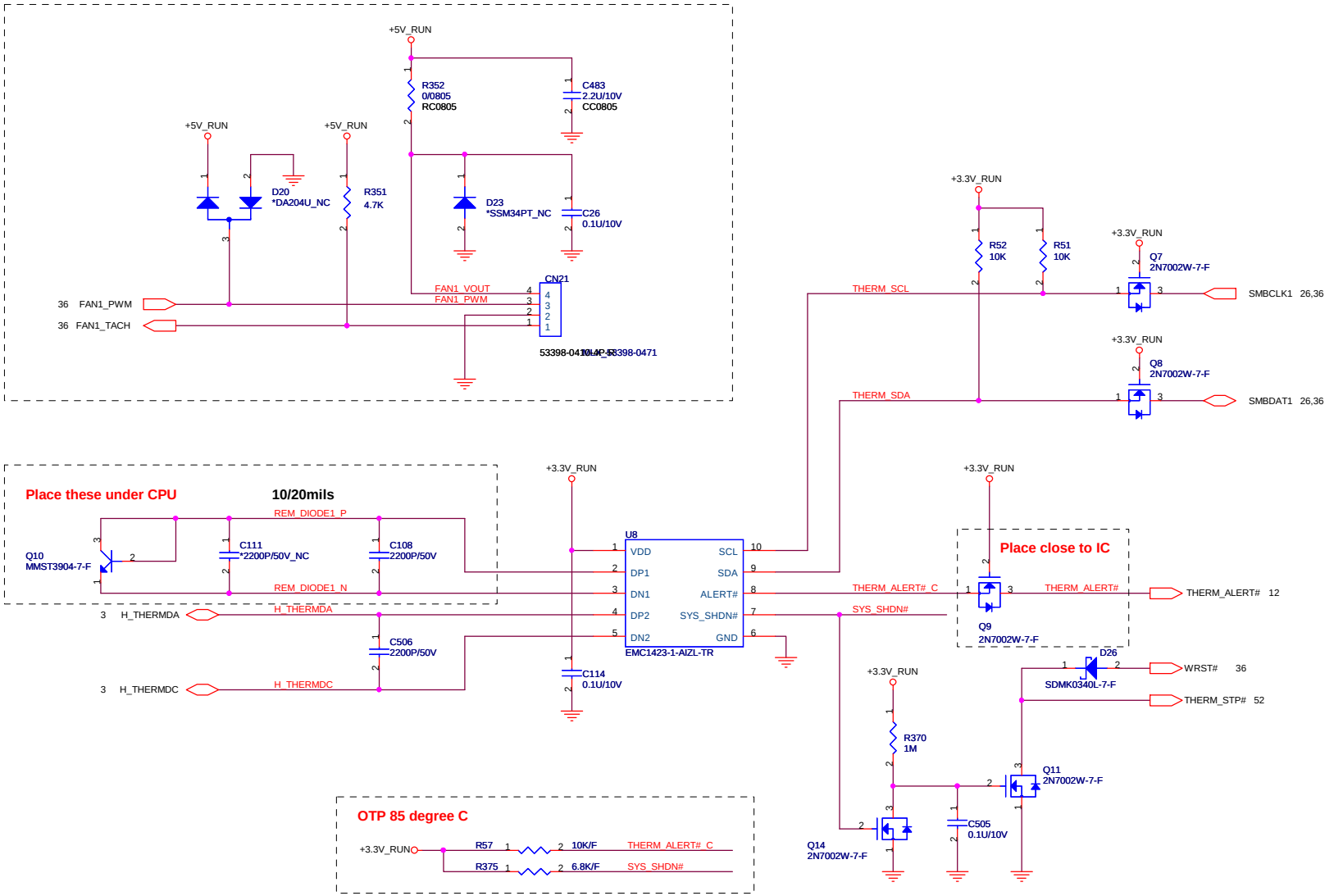






QUANTA COMPUTER

Title	ExpressCard	
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet 34 of 59	



QUANTA COMPUTER		
Title	FAN & THERMAL	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Wednesday, September 17, 2008	Sheet 35 of 59	

ITE8512E LQFP-128L

U32

38 KSO[0..16]
38 KSI[0..7]

39 LED_MASK#

12 MCP_EXT_SMI# — D31 SDMK0340L-7-F — ECSMI#
12 MCP_EXT_SCI# — D29 SDMK0340L-7-F — ECSCI#
12 MCP_A20GATE — D32 SDMK0340L-7-F — GA20
12 MCP_KBRDRSTIN# — D33 SDMK0340L-7-F — GPB6
C733 *220P/50V_NC

0313-Sun_Reserve 220P on MCP_KBRDRSTIN#

33 CLK_LPC_DEBUG — R263 0 — CLK_LPC

0305-Sun_Change ITE8512 pin22 I/P to HDA_RESET#

12,42 HDA_RESET#
10 CLK_LPC
10,33 LPC_LFRAME#
10,33 LPC_LAD0
10,33 LPC_LAD1
10,33 LPC_LAD2
10,33 LPC_LAD3
10,40,57 CLKRUN#
10,40,57 IRQ_SERIRQ
26 LCD_TST
35 WRST#
26 LCD_BAK#
43 NB_MUTE#
8,17,32,33,34 PE_RESET#

R481 0 / R501 0 — CLK_LPC
R567 0

0627_Michael:Del D36 & "MCP_PME#" to connect "PE_RESET#" to R567

+3.3V_ALW — R494 100K — WRST# — C641 1U/10V CC0603

GPU_Thermal and Charge and BAT — 19,48,55 SMBCLK0 / SMBDAT0
LCD and Thermal — 26,35 SMBCLK1 / SMBDAT1
Media button — 38 SMBCLK2 / SMBDAT2

0627_Michael:Change GPU_Thermal control from SMBus2 to SMBus0

51 1.5V_DDR_PWRGD
12,49 CPU_PWRGD
T43 PAD
T73 PAD
38 CLK_TP_SIO
38 DAT_TP_SIO

CLK_LPC — R313 *10_NC — C451 *2.2P/50V_NC

ITE8512_XTAL1
ITE8512_XTAL2
SIO_VSS
SIO_AVCC
SIO_AVSS

KEYBOARD
KSO17/GPC5
KSO16/GPC3
KSO15
KSO14
KSO13
KSO12/SLCT
KSO11/ERR
KSO10/PE
KSO9/BUSY
KSO8/ACK
KSO7/PD7
KSO6/PD6
KSO5/PD5
KSO4/PD4
KSO3/PD3
KSO2/PD2
KSO1/PD1
KSO0/PD0
KSI7
KSI6
KSI5
KSI4
KSI3/SLIN
KSI2/INIT
KSI1/AFD
KSI0/STB

ADC/DAC
ADC0/GPI0
ADC1/GPI1
ADC2/GPI2
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5
ADC6/GPI6
ADC7/GPI7
DAC0/GPJ0
DAC1/GPJ1
DAC2/GPJ2
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5

LPC
LPCRST/WUI4/GPD2
LPCCLK
LFRAME
LAD0
LAD1
LAD2
LAD3
CLKRUN/GPH0/ID0
SERIRQ
ECSMI/GPD4
ECSCI/GPD3
GA20/GPB5
LPCPD/WUI6/GPE6
KBRST/GPB6
WRST
PWUREQ/GPC7
L80HLAT/GPE0
L80LLAT/WUI7/GPE7

PWM
PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/GPA6
PWM7/GPA7
TACH0/GPD6
TACH1/GPD7
TMRI0/WUI2/GPC4
TMRI1/WUI3/GPC6

IR/UART
RXD/GPB0
TXD/GPB1
CRX0/GPC0
CTX0/GPB2
CRX1/GPH1/ID1
CTX1/GPH2/ID2

SMBUS
SMCLK0/GPB3
SMDAT0/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/GPF6
SMDAT2/GPF7

LPC/FWH FLASH
FLFRAME/GPG2/LF
FLRST/GPG0/TM
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE
FLCLK

PS/2
PS2CLK0/GPF0
PS2DAT0/GPF1
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5

EGPC
EGAD/GPE1
EGCS/GPE2
EGCLK/GPE3

GPIO
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
GPG1/ID7
RI1/WUI0/GPD0
RI2/WUI1/GPD1
WUI5/GPE5
RING/PWRFAIL/LPCRST/GPB7
PWRSW/GPE4
GINT/GPD5

CK32K
CK32KE
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7
AVCC
AVSS

ITE8512E LQFP128-16X16-4-FX2

VBAT1
VCC
VSTBY1 VSTBY2 VSTBY3 VSTBY4 VSTBY5 VSTBY6

3 VBAT1 — +RTC_CELL — R326 0
11 VCC — +3.3V_RUN
26 VSTBY1 — +3.3V_ALW
R323 *0_NC
C460 0.1U/10V

0609_Michael:Change SMBus2 pull-up sistor vaule from 2.2K to 10K for ISSP

0310-Sun_Remove 10K ohm on SIO_SLP_S5# to +3.3V_ALW. (Remove R485)

+3.3V_ALW
SMBDAT0 — RP4 2.2KX2 — SMBCLK0
SMBDAT1 — RP3 2.2KX2 — SMBCLK1
SMBDAT2 — RP23 10KX2 — SMBCLK2
LCD_CBL_DET# — R472 100K
INVERTER_CBL_DET# — R476 100K
KB_DET# — R569 10K
LID_SW# — R601 10K

0314-Sun_Add pull up RES on LID_SW# to +3.3V_ALW

66 HWPG — HWPG 47
67 — IMVP6_PROCHOT# 49
68 — MXM_RUNPWROK 8,47
69 LCD_CBL_DET# — LCD_CBL_DET# 26
70 INVERTER_CBL_DET# — INVERTER_CBL_DET# 26
71 — PBAT_PRES# 55
72 ADAPT_OC_IINP — ADAPT_OC_IINP 48
73 SIO_SLP_S5# — SIO_SLP_S5# 12,51

76 — PS_PWRGD 12
77 — SIO_EXT_WAKE# 12
78 — LAN_DISABLE 45
79 — EXPRCRD_PWREN# 8,34
80 PWRGD_SB — PWRGD_SB 12
81 — MCP_PWRBTN# 12
D28 SDMK0340L-7-F

+3.3V_SUS
SIO_SLP_S5# — R590 *10K_NC
SIO_SLP_S3# — R600 *10K_NC

0314-Sun_Reserve 10K pull-up on SIO_SLP_S3# & SIO_SLP_S5#.

0229-Sun_Del BAT_LED2#
0904_Michael:Use for power buttom LED control

24 — BREATH_LED# 39
25 — PWR_LED# 39
28 — FAN1_PWM 35
29 — PWM_VADJ 26
30 — BAT1_LED# 39
31 — KB_BACKLITE_EN 38
32 — CAP_LED# 38
34 — BEEP 42
47 — FAN1_TACH 35
48 — PANEL_BKEN 9
120 — LID_SW# 38
124 — MEDIA_INT# 38

0625_Michael:Change FAN1_TACH pin type from output to input

SUS_ON — R327 100K
HWPG — R469 100K
PWRGD_SB — R317 100K
C736 0.1U/10V

+3.3V_RUN
IRQ_SERIRQ — R325 10K
LCD_BAK# — R314 *10K_NC

0314-Sun_Add bypass capacitor on PWRGD_SW to absorb glitch from EC when +3.3V_ALW boot up.

0310-Sun_Remove T75 and connect GPB0 to ESATA_DETECT#.

108 — ESATA_DETECT# 30
109 — AUX_EN_WOWL 32
119 — CIRRX 37
123 — RUN_ON 26,36,51,56
94 — HDDC_EN 31
95

0612_Michael:Remove net CAMERA_CBL_DET#

EC_FLASH_SPI_CLK — R329 *10_NC
C458 *2.2P/50V_NC

0413-Sun_Reserve MMB power control for MMB ISSP Support
0705_Michael:Change net name from MMB_ISSP to MMB_ISSP#

100 SUS_ON — SUS_ON 56
106 KB_DET# — KB_DET# 30
104 — MMB_ISSP# 38
103 — EC_FLASH_SPI_DO 37
102 — EC_FLASH_SPI_DIN 37
101 — EC_FLASH_SPI_CS# 37
105 EC_FLASH_SPI_CLK — EC_FLASH_SPI_CLK 37

82 — PS_ID 55
83 — 5V_ALW_ON 52
84 — SIO_PWRGD_SB 47

96 GPH3
97 GPH4
98 GPH5
99 GPH6
107 — MODC_EN 31

Default is pull-up

18 — SIO_SLP_S3# 12
21 — ACAV_IN 48
35 — USB_SIDE_EN# 30
112 — USB_BACK_EN# 30
125 — MAIN_PWR_SW# 38
33 — LCDVCC_TST_EN 26

Board ID Straps

+3.3V_ALW

Discrete	BID2	BID1	BID0
	R539 10K_DIS	R318 10K	R552 *10K_NC	R319 10K
	GPH4	GPH5	GPH6	GPH3
	R538 10K_UMA	R328 *10K_NC	R553 10K	R330 *10K_NC

1023_Michael:Change Board ID to 101 for QT.

0424-Steg Add R330

UMA

BID2	BID1	BID0	XPS (UMA)	XPS (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT1 (X01)	PT1 (X01)
0	1	0	PT2 (X01)	PT2 (X01)
0	1	1	ST (X02)	ST (X02)
1	0	0	ST2 (X02)	ST2 (X02)
1	0	1	QT (A00) (A01)	QT (A00) (A01)

VGA_IDENTIFY : USB_SIDE_EN#
1 = Discrete Gfx / 0 = UMA.

32KHz Clock
R529 0 — ITE8512_XTAL2
W2 32.768KHZ — ITE8512_XTAL1
C678 15P/50V
C684 15P/50V

+3.3V_ALW
L46 BLM11A05S RC0603 — SIO_AVCC
L48 BLM11A05S RC0603 — SIO_AVSS
C649 0.1U/10V

ITE8512IX pin12 connect to GND.
ITE8512JX pin12 connect to 0.1uF. (Default on PT1)

SIO_VSS
R510 *0_NC
C656 0.1U/10V
C663 *1U/10V_NC CC0603

+3.3V_ALW
C671 10U/6.3V CC0603
C445 0.1U/10V
C693 0.1U/10V
C617 0.1U/10V
C694 0.1U/10V

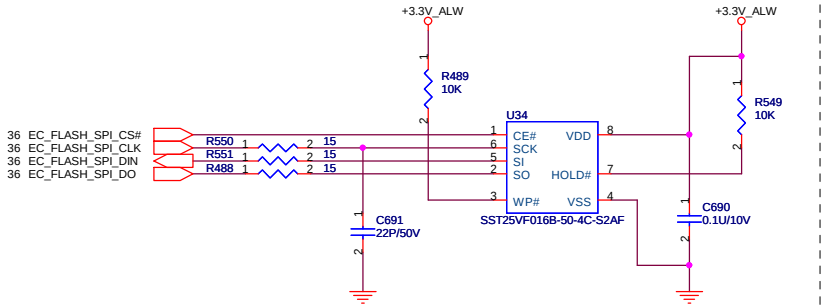
Place these caps close to ITE8512.

0709-Steg: Change CAP value from 10p to 15p

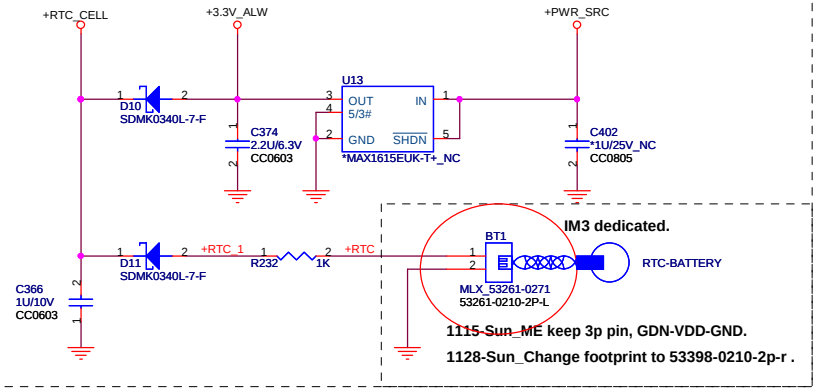
QUANTA COMPUTER

Title	SIO(ITE8512)	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date:	Thursday, October 23, 2008	Sheet 36 of 59

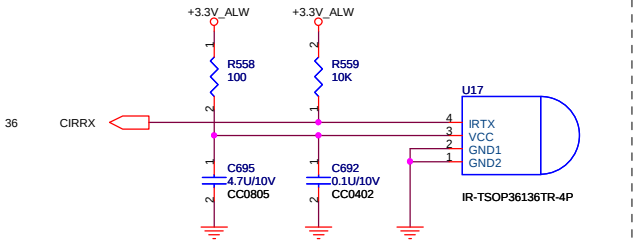
16Mbit (2M Byte), SPI



RTC BATTERY



Consumer IR



QUANTA COMPUTER

Title	FLASH & RTC	
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet 37 of 59	

0605_Michael: Change CN6 from 32pin to 28pin but need to check footprint and PN

BREATH_PWRLED_BOT:
Solid = System On, Normal Activity; "Breathing" = System in Standby; Off = System Off (or in Hibernate)

0920_Michael:Add KB detect function
1023_Michael:Disable KB_LED function depop R722 and change R723 from 200K to 0 ohm

Power Button
Speaker
KB LED
Touch Pad
Media Button

CN6
FH28D-28S-0.5SH(0.5)

0624_Michael:Change net name from +5V_ALW2 to +MMB_PWR
0704_Michael:Swap SMBCLK2 and +MMB_PWR for Ass'y issue

0825_Michael:Add KB detect function
0911_Michael:Change pin from 16 to 8
0918_Michael:Return to LID_SW#

0909_Michael:Remove LID_SW# and connector to GND

0411-Sun_Reserve circuit for MMB ISSP support
0414-Sun_Change MOSFET control voltage level

0701_Michael: Remove Q91 for ISSP

0609_Michael:Add MOS Q92 on +MMB_PWR for ISSP

Power Buttom

D30 *DA204U_NC
R479 100K
R480 10K
C628 1U/10V CC0603

KEYBOARD CONNECTOR

CN9
FH28-60(30)SB-1SH(05)
FH28-30SB-1SH-30P-R

0701_Michael:Remove Q80 and add Q46 & R491 for leakage issue on S3

0310-Sun_CAP_LED +5V_ALW2 change to +5V_RUN

Q46 MMBT3906_NL
Q78 2N7002W-7-F
R511 100K
R491 10K
R533 158

1022_Michael: Change R533 from 2.49K to158ohm for LED brightness

CP1–CP6 *100PX4_NC
C707 *100P/50V_NC

100P CAPS CLOSE TO JKB1

Array Microphone & Camera

L12 BLM11A05S RC0603
L11 *BLM11A05S_NC RC0603
L10 *DLW21SN900SQ2B_NC

GND,VCC要用最粗的電子線

CN3
IPEX coaxial 20374-010e-10p-l

0306-Sun_Change CCD connector to 10pin

0612_Michael:Remove CAMERA DET circuit, R64 pull-up to +3.3V_RUN and connector to U32 pin95

U11 *TPS76301DBVR_NC

Hall Switch

R724 100K
C869 *0.1U/10V_NC
U54 *PT3661-BB_NC

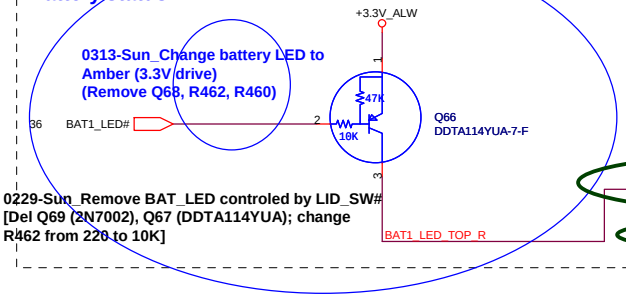
0815_Michael:Add Hall Switch circuit and MEDIA_INT# pull-high at MB side

1023_Michael:Depop U54 Hall switch function on MB side

QUANTA COMPUTER

Title	USER INTERFACE/CIR	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 38 of 59	

Battery status



0229-Sun_Remove BAT_LED controled by LID_SW#
[Del Q69 (2N7002), Q67 (DDTA114YUA); change R462 from 220 to 10K]

0606_Michael:Add R462 connect to CN2 on BAT1_LED

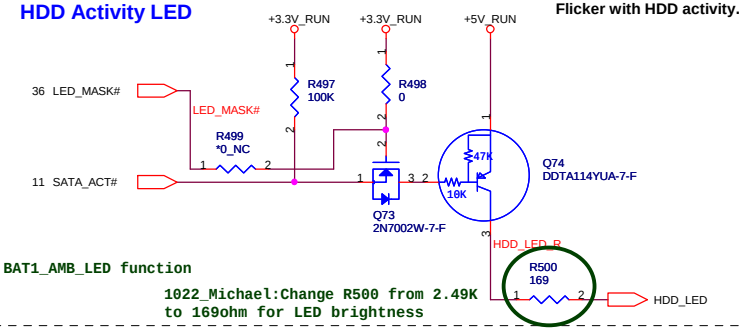
R462 1 2 220 BAT1_LED

0922_Michael:Remove BAT1_AMB_LED function

0229-Sun_Del BAT_LED2
[Del R295,Q48,Q43 (2N7002) and Q46,Q47 (DDTA114YUA)]

HDD Activity LED

Flicker with HDD activity.



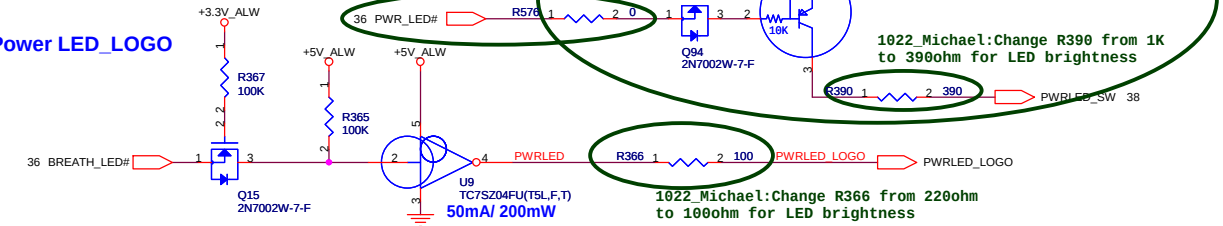
1022_Michael:Change R500 from 2.49K
to 169ohm for LED brightness

0229-Sun_Change PWRLED_SW control same as PWRLED_LOGO
[Del U10 (TC7SZ04F), Q16 (2N7002)]

0904_Michael:Add R576 and connector to
PWR_LED# from ITE8512

0618_Michael:Follow DELL command modify
circuit to change the LED behavior of
Power button

Power LED_LOGO

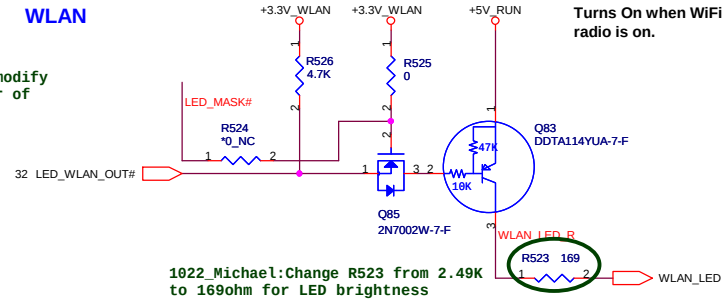


1022_Michael:Change R390 from 1K
to 390ohm for LED brightness

1022_Michael:Change R366 from 220ohm
to 100ohm for LED brightness

WLAN

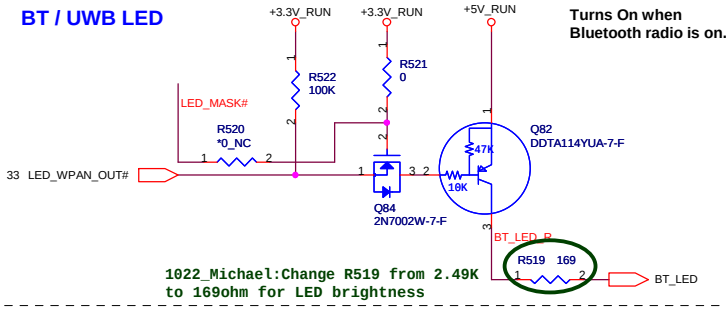
Turns On when WiFi radio is on.



1022_Michael:Change R523 from 2.49K
to 169ohm for LED brightness

BT / UWB LED

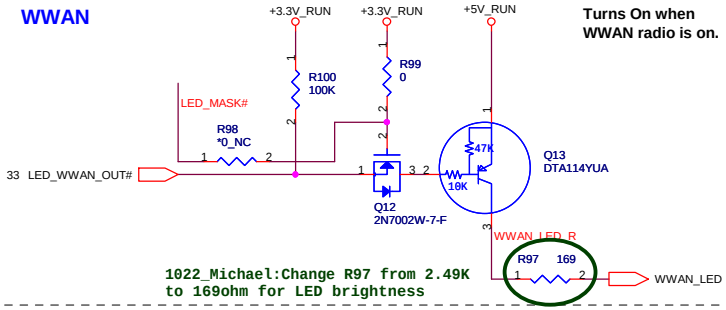
Turns On when Bluetooth radio is on.



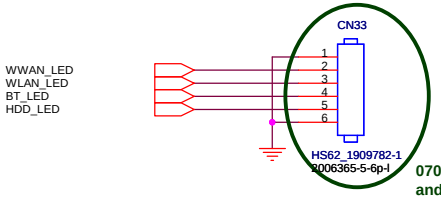
1022_Michael:Change R519 from 2.49K
to 169ohm for LED brightness

WWAN

Turns On when WWAN radio is on.

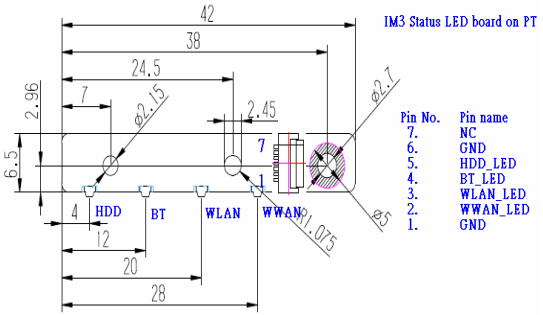


1022_Michael:Change R97 from 2.49K
to 169ohm for LED brightness

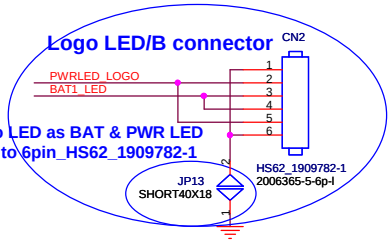


0229-Sun_Remove LED control by LID_SW#
(Del R478,R477,Q75)

0704_Michael:Change CN33 pin number from 7pin to 6pin
and also change type from HEADER7 to HS62_1909782-1
for cost down



Logo LED/B connector



0306-Sun_Change Logo LED as BAT & PWR LED
and change connector to 6pin_HS62_1909782-1

0314-Sun_Add short pad on GND of
Logo LED/B connector for EMI request.

QUANTA COMPUTER		
Title: LED		
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Wednesday, October 22, 2008	Sheet 39 of 59	

Place the power caps close to the relation pins.

+3.3V_R5C833

C666 10U/6.3V CC0603
C639 0.01U/25V
C620 0.01U/25V
C610 0.01U/25V
C614 0.01U/25V
C635 0.01U/25V

C618 10U/6.3V CC0603
C613 0.1U/10V
C688 0.01U/25V
C612 0.01U/25V

Please place capacitors for VCC_ROUTx as close to R5C833 as possible.

C611 0.01U/25V
C674 0.01U/25V
C631 0.47U/10V CC0603
C625 0.47U/10V CC0603

+3.3V_RUN
+3.3V_R5C833
JP11 SHORT40X18

0606_Michael:Change footprint from 0ohm R468 to normal short type JP11 (short40x18)

C661 0.1U/10V
C642 10U/6.3V CC0603

Place the power caps close to the relation pins.

U29B

VCC_PCI1 10
VCC_PCI2 20
VCC_PCI3 27
VCC_PCI4 32
VCC_PCI5 41
VCC_PCI6 128
VCC_RIN 61
VCC_ROUT1 16
VCC_ROUT2 34
VCC_ROUT3 64
VCC_ROUT4 114
VCC_ROUT5 120
VCC_3V 67
VCC_MD 86

GND1 4
GND2 13
GND3 22
GND4 28
GND5 54
GND6 62
GND7 63
GND8 68
GND9 118
GND10 122

AGND1 99
AGND2 102
AGND3 103
AGND4 107
AGND5 111

10 PCI_AD[31..0]

PCI_AD31 125 AD31
PCI_AD30 126 AD30
PCI_AD29 127 AD29
PCI_AD28 1 AD28
PCI_AD27 2 AD27
PCI_AD26 3 AD26
PCI_AD25 5 AD25
PCI_AD24 6 AD24
PCI_AD23 9 AD23
PCI_AD22 11 AD22
PCI_AD21 12 AD21
PCI_AD20 14 AD20
PCI_AD19 15 AD19
PCI_AD18 17 AD18
PCI_AD17 18 AD17
PCI_AD16 19 AD16
PCI_AD15 36 AD15
PCI_AD14 37 AD14
PCI_AD13 38 AD13
PCI_AD12 39 AD12
PCI_AD11 40 AD11
PCI_AD10 42 AD10
PCI_AD9 43 AD9
PCI_AD8 44 AD8
PCI_AD7 46 AD7
PCI_AD6 47 AD6
PCI_AD5 48 AD5
PCI_AD4 49 AD4
PCI_AD3 50 AD3
PCI_AD2 51 AD2
PCI_AD1 52 AD1
PCI_AD0 53 AD0

PCI / OTHER

+3.3V_R5C833

R546 100K
GBRST#
C685 1U/10V CC0603

GBRST# should be asserted only when system power supply is on.

HWSPND# 69
R562 10K
+3.3V_R5C833
R502 10K
+3.3V_R5C833
R505 100K
+3.3V_R5C833

MSEN 58 — Memory Stick Enable
XDEN 55 — XD Card Enable
UDIO5 57 — Serial ROM disable
UDIO3 65 — SD Card Enable
UDIO4 59 — MMC Card Enable
UDIO2 56
UDIO1 60
UDIO0/SRIRQ# 72 — IRQ_SERIRQ 10,36

INTA# 115 — 1394 Interrupt — PCI_INTW# 10
INTB# 116 — Media card Interrupt — PCI_INTX# 10

TEST 66 — PAD T74
R563 100K

10 PCI_PAR 33 PAR
10 PCI_C_BE3# 7 C/BE3#
10 PCI_C_BE2# 21 C/BE2#
10 PCI_C_BE1# 35 C/BE1#
10 PCI_C_BE0# 45 C/BE0#
PCI_AD23 R463 1 2 100 8 IDSEL

10 PCI_REQ0# 124 REQ#
10 PCI_GNT0# 123 GNT#
10 PCI_FRAME# 23 FRAME#
10 PCI_IRDY# 24 IRDY#
10 PCI_TRDY# 25 TRDY#
10 PCI_DEVSEL# 26 DEVSEL#
10 PCI_STOP# 29 STOP#
10 PCI_PERR# 30 PERR#
10 PCI_SERR# 31 SERR#

GBRST# 71 GBRST#
10 PCI_RST# 119 PCIRST#
10 CLK_PCI_PCCARD R473 1 2 0 121 PCICLK
10 PCI_PME# R561 1 2 *0_NC 70 PME#
10,36 CLKRUN# 117 CLKRUN#

R5C833T_V00

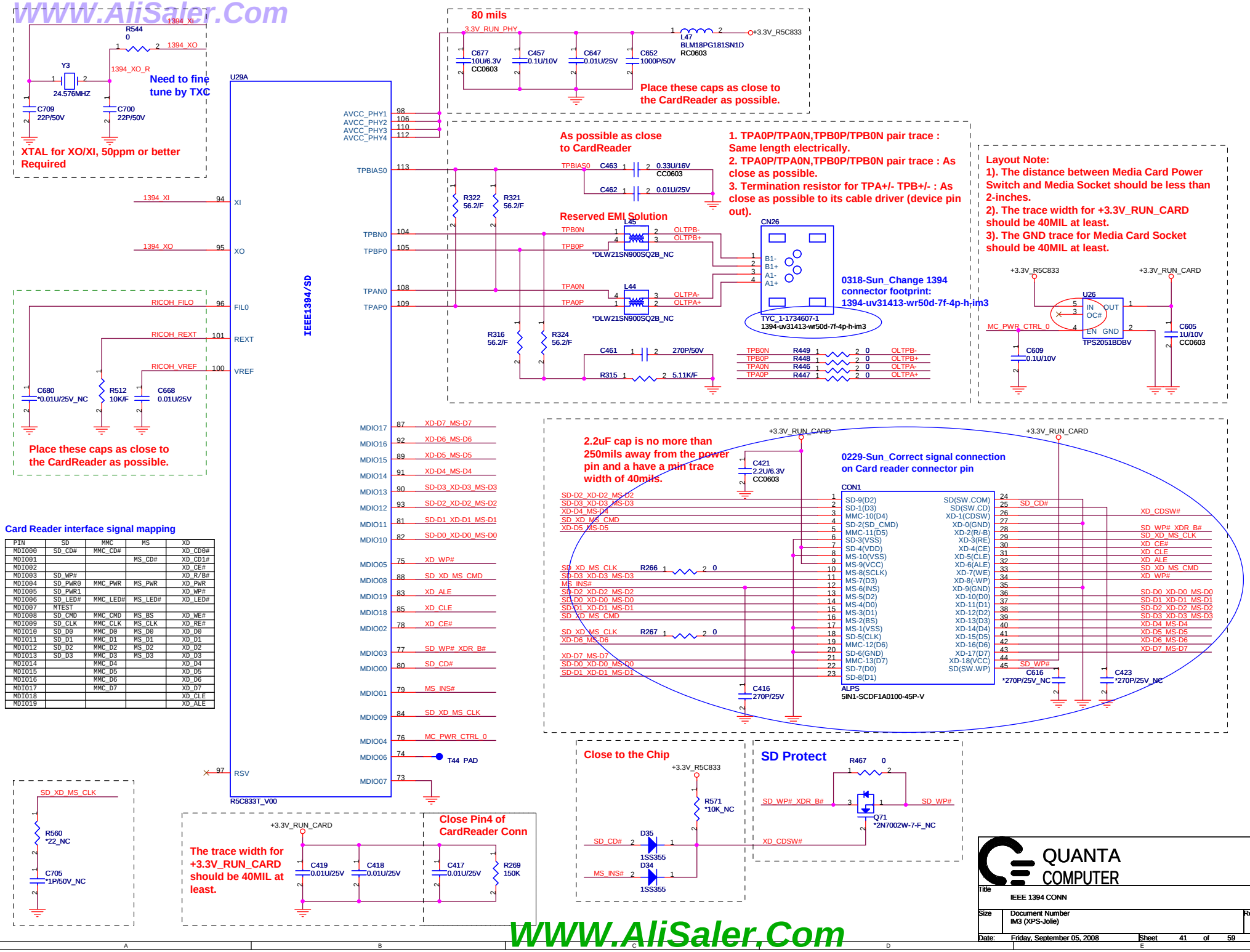
CLK_PCI_PCCARD
R470 *22_NC
C622 *1P/50V_NC

0630_Michael:Remove Mini PCI CN8 and circuit

0707_Michael:Depop R561 for leakage issue

QUANTA COMPUTER

Title	CARDREADER FOR 8 IN 1 CONTROLLER	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 40 of 59	

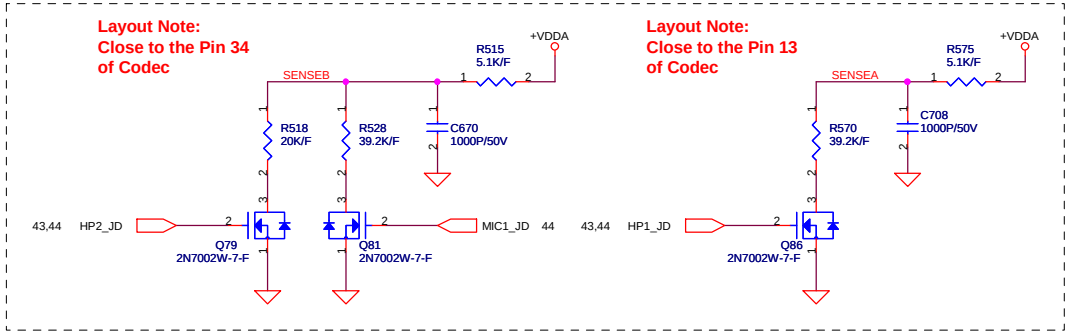


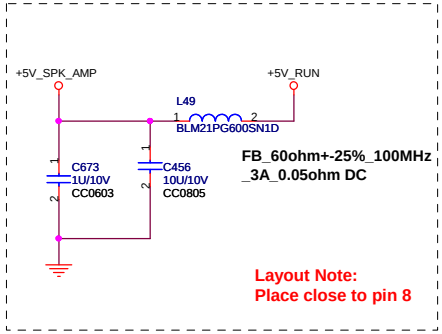
PIN	SD	MMC	MS	XD
MDIO00	SD_CD#	MMC_CD#		XD_CD0#
MDIO01			MS_CD#	XD_CD1#
MDIO02				XD_CE#
MDIO03	SD_WP#			XD_R/B#
MDIO04	SD_PWR0	MMC_PWR	MS_PWR	XD_PWR
MDIO05	SD_PWR1			XD_WP#
MDIO06	SD_LED#	MMC_LED#	MS_LED#	XD_LED#
MDIO07	MTEST			
MDIO08	SD_CMD	MMC_CMD	MS_BS	XD_WE#
MDIO09	SD_CLK	MMC_CLK	MS_CLK	XD_RE#
MDIO10	SD_D0	MMC_D0	MS_D0	XD_D0
MDIO11	SD_D1	MMC_D1	MS_D1	XD_D1
MDIO12	SD_D2	MMC_D2	MS_D2	XD_D2
MDIO13	SD_D3	MMC_D3	MS_D3	XD_D3
MDIO14		MMC_D4		XD_D4
MDIO15		MMC_D5		XD_D5
MDIO16		MMC_D6		XD_D6
MDIO17		MMC_D7		XD_D7
MDIO18				XD_CLE
MDIO19				XD_ALE

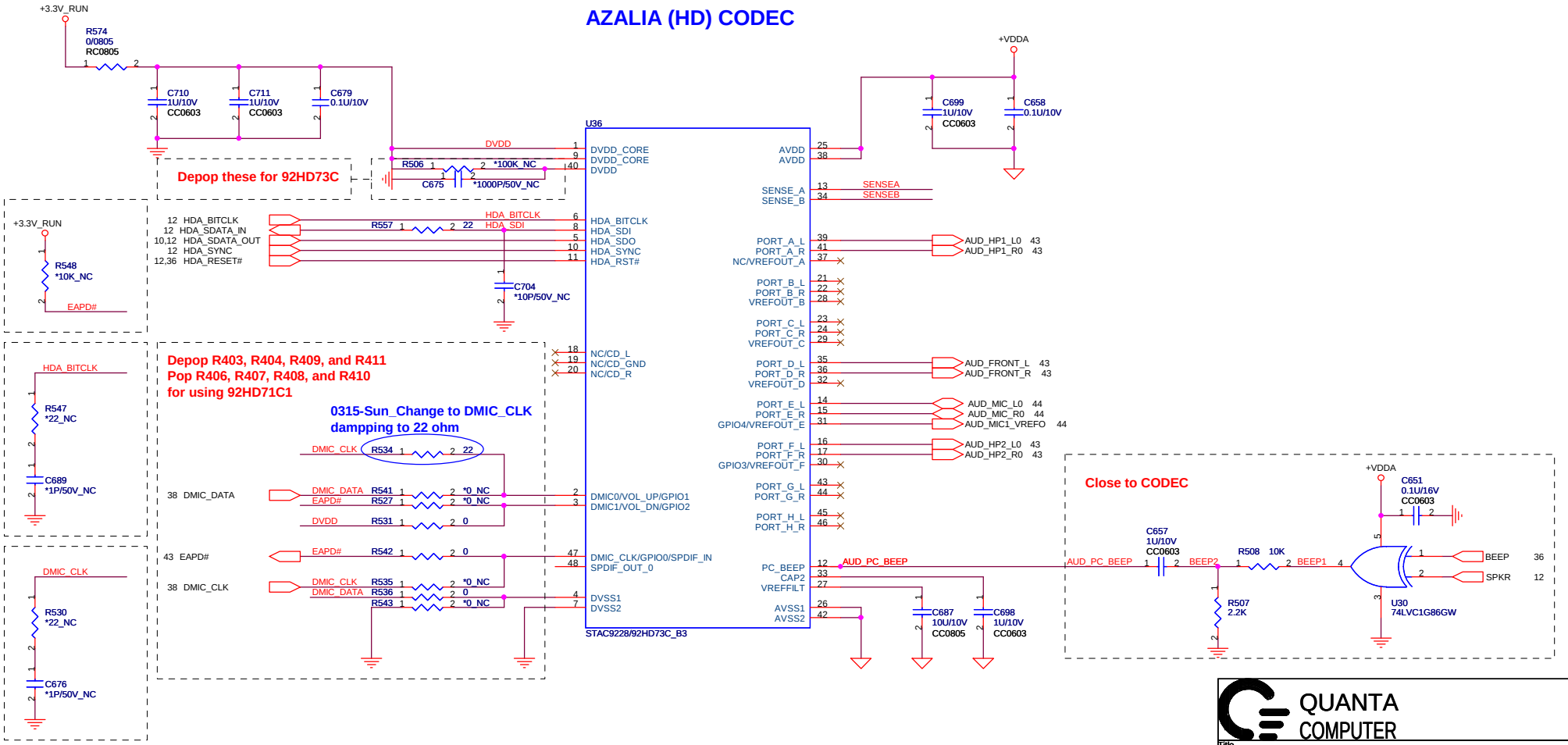
QUANTA COMPUTER

Title	IEEE 1394 CONN	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Friday, September 05, 2008	Sheet 41 of 59	

AZALIA (HD) CODEC

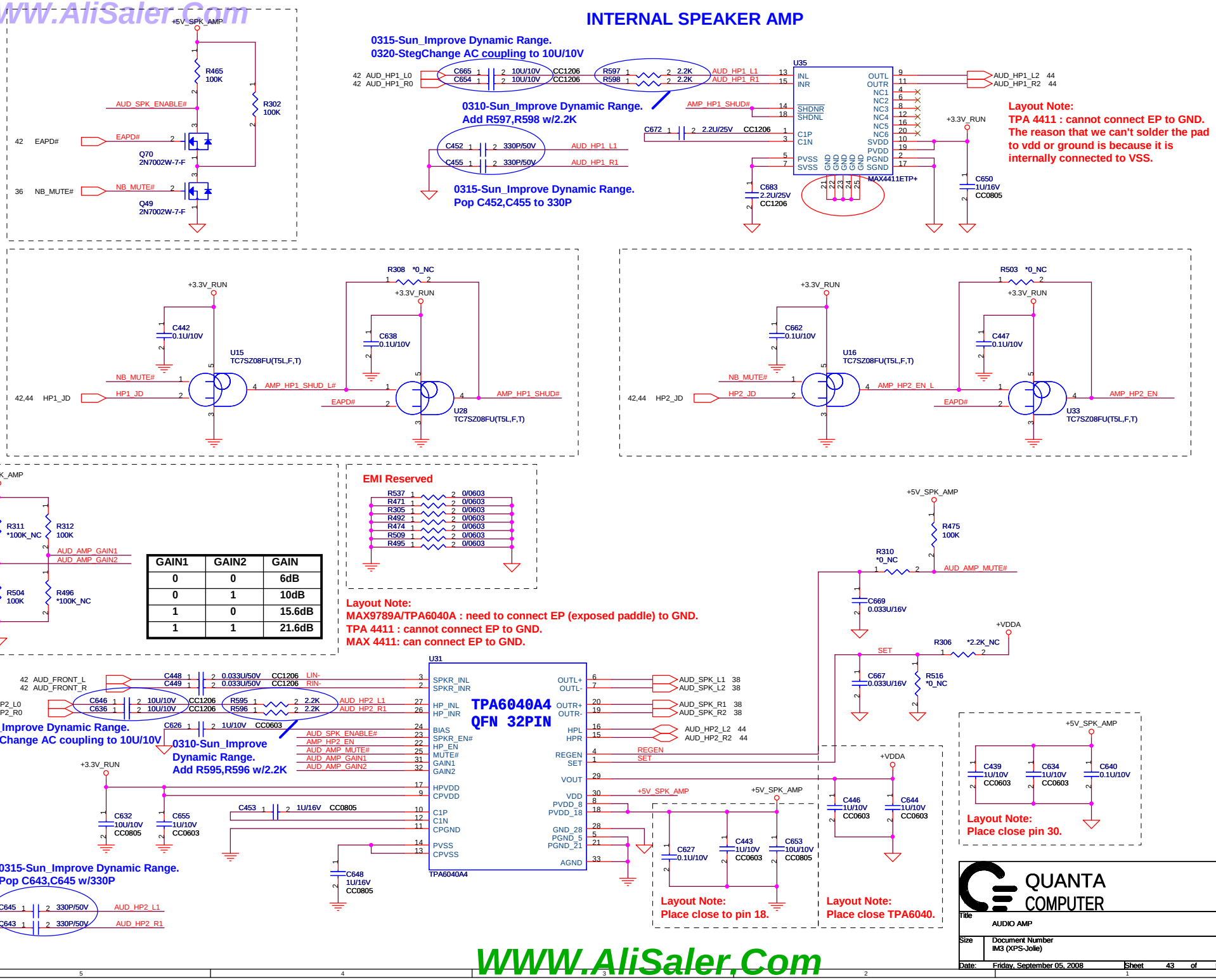






QUANTA COMPUTER		
Title: Azelia CODEC		
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet 42 of 59	

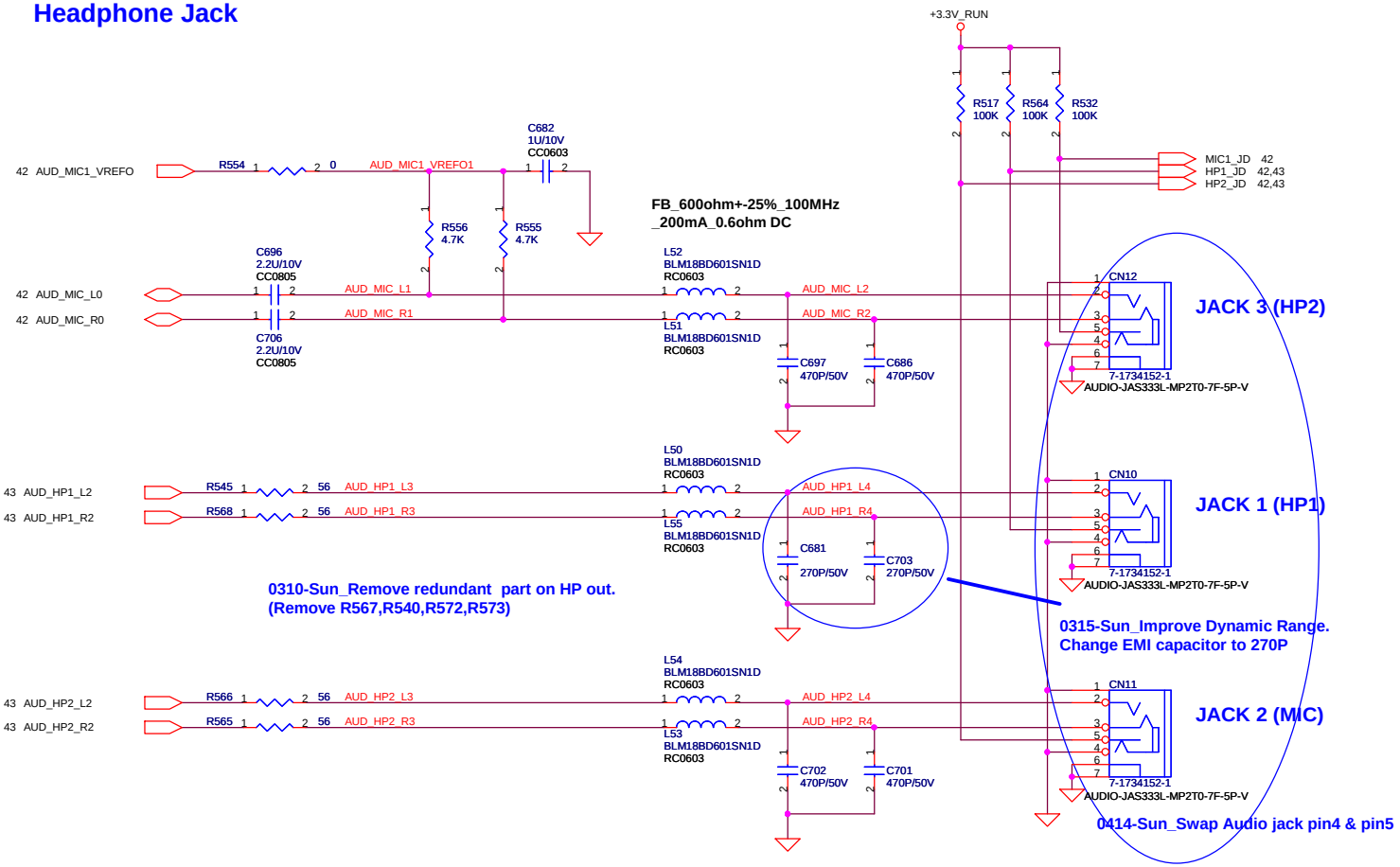
INTERNAL SPEAKER AMP



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

QUANTA COMPUTER		
Title	AUDIO AMP	
Size	Document Number: IM3 (XPS-Jolie)	Rev: 2A
Date: Friday, September 05, 2008	Sheet 43 of 59	

Headphone Jack



QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 44 of 59	

Layout Note:
1.Use 50 ohm impedance for all trace.
2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
3.The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.

Reserved EMI
0319-Sun_Pop 6.8P on LAN bus

TRD0+ TRD0- TRD1+ TRD1- — C490 6.8P/50V, C491 6.8P/50V, C486 6.8P/50V, C487 6.8P/50V
TRD2+ TRD2- TRD3+ TRD3- — C502 6.8P/50V, C503 6.8P/50V, C492 6.8P/50V, C495 6.8P/50V

B5071A2KFBG PHY 100 BALL BGA (U19)

RGMII_TXCLK, RGMII_TXCTL, RGMII_TXD0, RGMII_TXD1, RGMII_TXD2, RGMII_TXD3 → GTXCLK, TX_EN, TX_ER, TXD[0]–TXD[7]

0319-Sun_Change RGMII_RXCLK damping RES to 22 ohm for EMI
RGMII_RXCLK — R63 22 — RGMII_RXCLK_C
RGMII_RXCTL — R152 0 — RGMII_RXCTL_C
RXC, RX_DV, RX_ER

RGMII_RXD0–RGMII_RXD3 → RXD[0]–RXD[7]
RGMII_MDC, RGMII_MDIO → MDC, MDIO
RGMII_25MHz → XTALI
0312-Sun_Remove R76 on RGMII_25MHz
XTALO
T56 PAD, T55 PAD → CLK_125
T6 PAD, T46 PAD, T5 PAD, T45 PAD → TDI, TMS, TCK, TDO, TRST
R43 0 — RGMII_RESET#
+3.3V_PHY — R55 10K — MODE_SEL[1], MODE_SEL[0]
RGMII_PWRDWN, LAN_DISABLE — R31 0, R33 *0_NC — LOWPWR, TEST0, TEST1
RESET
0312-Sun_Remove R56 on RGMII_RESET#
NC_1 … NC_12

TRD[0]+ … TRD[3]- → TRD0+ … TRD3- (46)
LED[1] SPD10LED#, LED[2] SPD100LED#, LED[3] PHY_ACTLED, LED[4] PHY_LED[4] → SPD10LED# 46, SPD100LED# 46, PHY_ACTLED 46
REGOUT[1], DVDD_1, DVDD_2, DVDD_3 → +1.2V_PHY
AVDDL_1, AVDDL_2, VREF → PHY_AVDDL
PLLVDD → PHY_PLLVDD
REGOUT[2], AVDD_2, AVDD_1 → +2.5V_PHY
BIASVDD, XTALVDD, RDAC — R369 1.24K/F
OVDD1, OVDD2, REGSUPPLY[1], REGSUPPLY[2] → +3.3V_PHY (3.3V)
GND_1, GND_2, GND_3
AGND_1, AGND_2, AGND_3, PLLGND
NC_13 … NC_22 — R34 *10K_NC — +3.3V_PHY

Pull-High: Address 1
NC : Address 0

Pace 0.1u close PHY
+3.3V_PHY — C70 0.1U/10V, C68 0.1U/10V

Pace 0.1u close DVDD pins
Pace 10u close pin F3 "REGOUT[1]"
+1.2V_PHY, 1.2V — C62 0.1U/10V, C67 0.1U/10V, C73 0.1U/10V, C85 10U/10V CC0805

Pace close AVDDL pins
1.2V, PHY_AVDDL — L16 BLM18AG601SN1D — C80 0.1U/10V, C78 0.1U/10V, C104 10U/10V CC0805

1.2V, PHY_PLLVDD — L15 BLM18AG601SN1D — C97 0.1U/10V, C90 10U/10V CC0805

Layout Note:
Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.

Pace 10u close pin H3 "REGOUT[2]"
+2.5V_PHY, 2.5V — C64 0.1U/10V, C60 0.1U/10V, C485 10U/10V CC0805

2.5V, BIASVDD — L17 BLM18AG601SN1D — C99 0.1U/10V

2.5V, XTALVDD — L14 BLM18AG601SN1D — C95 0.1U/10V

Reserved EMI
RGMII_RXCLK — C79 33P/50V
0319-Sun_Pop RGMII_RXCLK capacitor w/33P for EMI
RGMII_25MHz — R75 22 — C100 10P/50V
0616_Michael:Change net name connector to RGMII_25MHz
0319-Sun_Pop AC termination on PHY_XTALI for EMI

0312-Sun_Remove R74 on PHY_XTALI.

+3.3V_PHY — R53 1.5K/F — RGMII_MDIO

0311-Sun_Add EMI bead on +3.3V_PHY. (Place on JP1)
+3.3V_RMGT — L56 HCB2012KF-601T20 RC0805 — +3.3V_PHY
JP1 SHORT40X12
C69 10U/10V CC0805
GB2012091601

0709-Steg: Change QPN for L56 due to forbid material.

+3.3V_PHY — R50 *4.7K_NC — PHY_RESET# — C76 *1P/50V_NC

0320-Steg_Add EMI capacitor on +3.3V_RGMT & +3.3V_PHY. (Place close to JP1/L56)
+3.3V_RMGT: C714 10P/50V, C717 47P/50V, C718 3300P/50V, C721 0.01U/25V, C722 1000P/16V
+3.3V_PHY: C730 33P/50V, C731 3300P/50V, C729 0.01U/25V

Auto-Negotiate 10/100/1000BASE-T
0319-Sun_Pop 3300P on SPD10LED# and SPD100LED# for EMI
SPD10LED#, PHY_LED[4], PHY_ACTLED — C732 33P/50V, R48 4.7K, R35 33P/50V, R42 3300P
0311-Sun_Add EMI capacitor on PHY_ACTLED (Place close to CN20)

Title	LAN Broadcom PHY B5071
Size	Document Number: IM3 (XPS-Jolie) — Rev: 2A
Date:	Friday, September 05, 2008 — Sheet 45 of 59

QUANTA COMPUTER

TRANSFORMER

+2.5V_PHY

R354 *0/0603_NC

L37 BLM18AG601SN1D

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace immpedance.

L5 — Pulse H5120NL

CHIP SIDE / MEDIA SIDE

45	TRD3+	TD0+	1	TX0+ 24 RJ45-TX3+
45	TRD3-	TD0-	2	TX0- 23 RJ45-TX3-
		TDCT	3	TXCT0 22 TXCT3 — R364 75/F
		TDCT	4	TXCT1 21 TXCT2 — R363 75/F
45	TRD2+	TD1+	5	TX1+ 20 RJ45-TX2+
45	TRD2-	TD1-	6	TX1- 19 RJ45-TX2-
45	TRD1+	TD2+	7	TX2+ 18 RJ45-TX1+
45	TRD1-	TD2-	8	TX2- 17 RJ45-TX1-
		TDCT	9	TXCT2 16 TXCT1 — R358 75/F GND_LAN
		TDCT	10	TXCT3 15 TXCT0 — R357 75/F
45	TRD0+	TD3+	11	TX3+ 14 RJ45-TX0+
45	TRD0-	TD3-	12	TX3- 13 RJ45-TX0-

C484 1000P/3K CC1808

C488 4700P/25V, C496 4700P/25V, C500 4700P/25V, C489 4700P/25V

Pace 0.1u physically close to transformer

0319-Sun_Change Transformer TDCT bypass capacitor to 4700P

0111-Stanley: Change BOM to Pulse H5120NL.

RJ-45 Connector

0314-Sun_Change RJ45 LED power to +3.3V_RMGT for EMI request

CN20

45 PHY_ACTLED — R29 100 — +3.3V_RMGT

LED_YN 10, LED_YP 9

RJ45-TX3- 8, RJ45-TX3+ 7, RJ45-TX1- 6, RJ45-TX2- 5, RJ45-TX2+ 4, RJ45-TX1+ 3, RJ45-TX0- 2, RJ45-TX0+ 1

LED_GND 12

45 SPD100LED# — D24 CH751H-40HPT — Q3 DDTA114YUA-7-F (47K / 10K) — R27 330 — LED_GN/AP 13, LED_GP/AN 11

0314-Sun_Add EMI capacitor on SPD100LED#

C734 33P/50V

+3.3V_RMGT

45 SPD10LED# — D25 CH751H-40HPT — Q4 DDTA114YUA-7-F (47K / 10K) — R38 330

0314-Sun_Add EMI capacitor on SPD10LED#

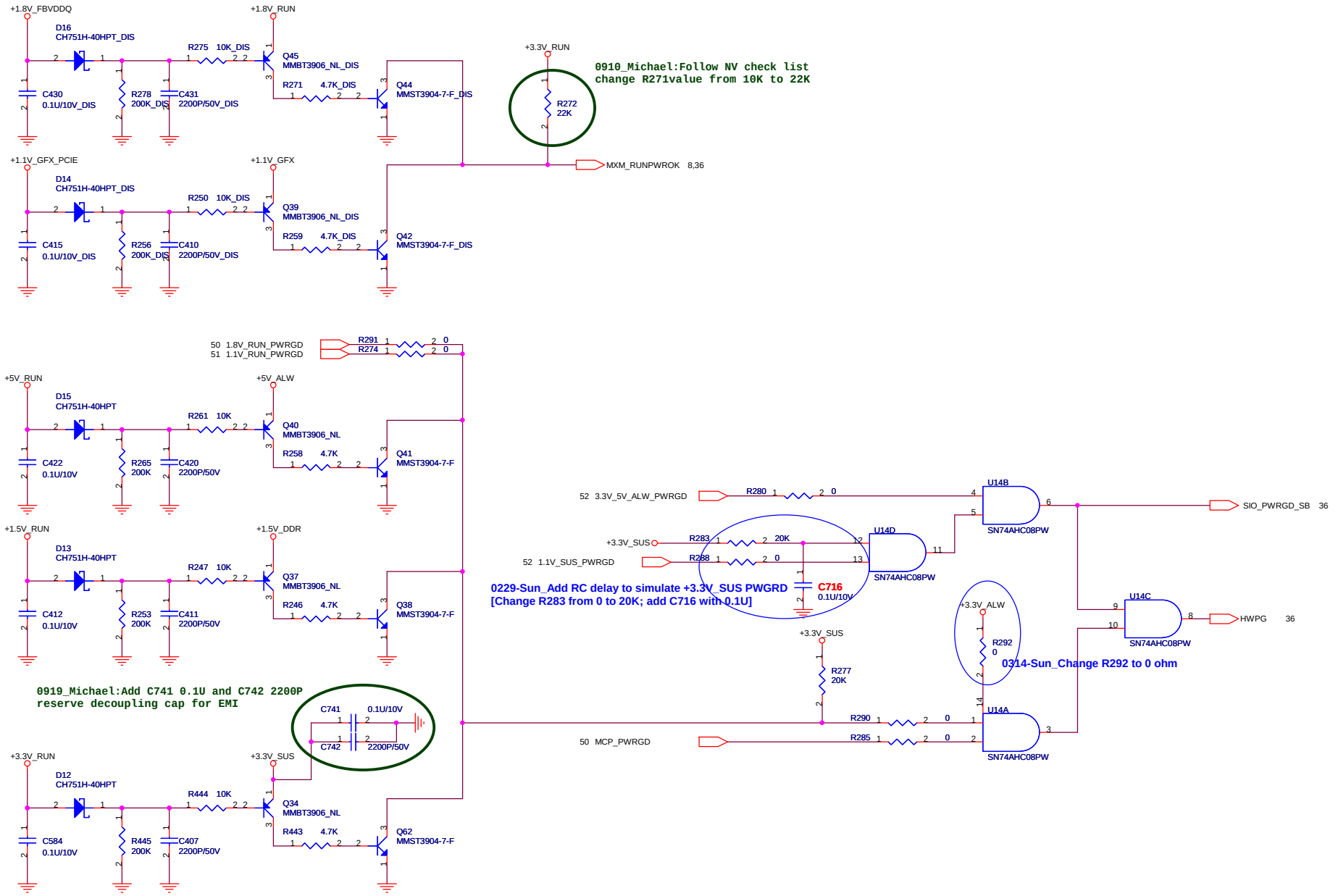
C735 33P/50V

CHSGND1 14, CHSGND2 15

LAN_CONN_14
RJ45-JM3611L-R0455-7F-13P-H

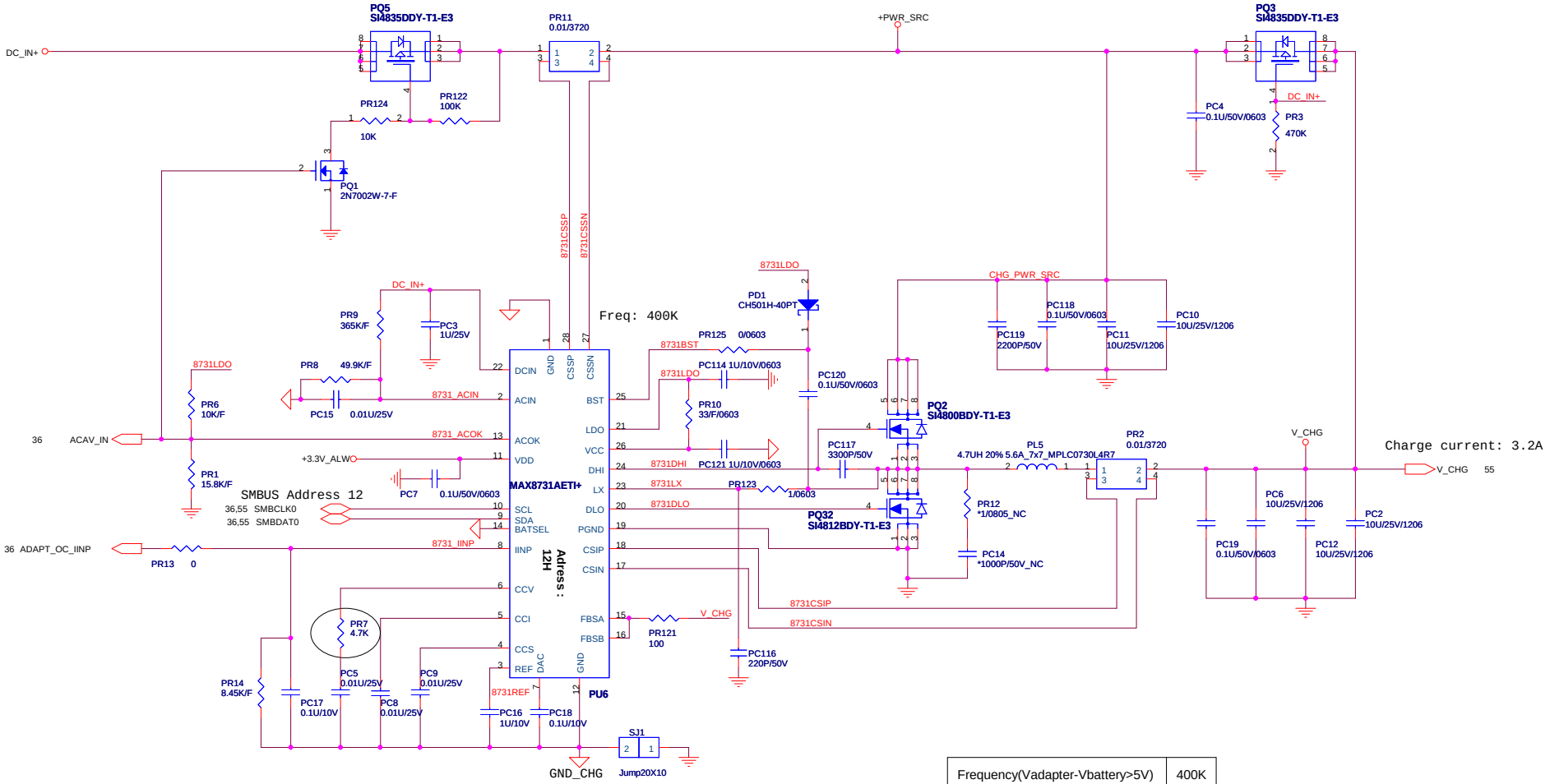
QUANTA COMPUTER

Title	LAN SWITCH		
Size	Document Number IM3 (XPS-Jolie)		Rev 2A
Date:	Friday, September 05, 2008	Sheet 46 of 59	



QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 47 of 59	

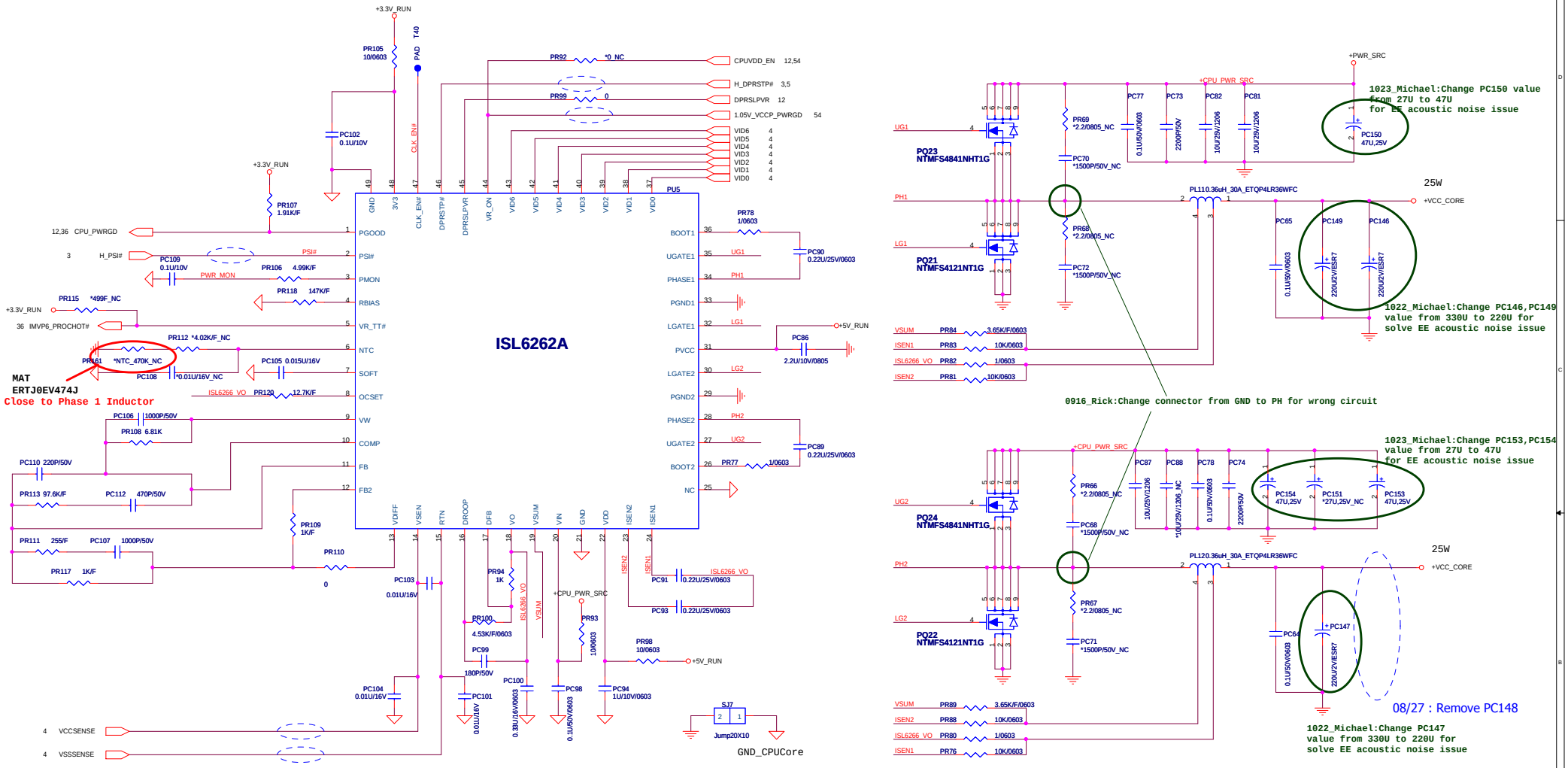


Frequency(Vadapter-Vbattery>5V)	400K

QUANTA COMPUTER

Title	CHARGER	
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date: Tuesday, September 09, 2008	Sheet 48 of 59	

08/27 : Remove 0 ohm (PR102, PR97, PR119, PR104, PR103)



VW	PR37
Frequency	270KHZ@0A / 310KHZ@44A

Title	CPU_Core_2Phase (ISL6262)
Size	Document Number: IM3 (XPS-Jolie) — Rev: 1A
Date:	Thursday, October 23, 2008 — Sheet 49 of 59

QUANTA COMPUTER

08/27 : Remove 0 ohm (PR46)

+MCP_CORE — +MCP_CORE 13
+1.8V_RUN — +1.8V_RUN 9,23,38,47,53

VID2	VID1	VID0	+MCP_Core
L	L	L	+1.0595 V
L	L	H	+1.0097 V
L	H	L	+0.9597 V
L	H	H	+0.9186 V
H	L	L	+0.8622 V
H	L	H	+0.8289 V
H	H	L	+0.7949 V
H	H	H	+0.7665 V

TDC: 8.12A
OCP: 11.6A

TDC: 2.95A
OCP: 4.22A

1022_Michael:Change PR140 value from 15.8K to 16.5K for improve +1.8V_FBVDDQ voltage too low issue

1022_Michael:Change PC42 value from 150U to 330U for improve +1.8V_FBVDDQ voltage too low issue

TON1	PR73 = 200K
Frequency	297K

TON2	PR75 = 200K
Frequency	297K

QUANTA COMPUTER

Title	MCP/1.8V (MAX17007)	
Size	Document Number IM3 (XPS-Jolie)	Rev 1B
Date: Thursday, October 23, 2008	Sheet 50 of 59	

+1.5V_DDR → +1.5V_DDR 15,16,47,56
+0.75V_DDR_VTT → +0.75V_DDR_VTT 15,16,56
+1.1V_RUN → +1.1V_RUN 5,7,8,9,11,12
V_DDR_MCP_REF → V_DDR_MCP_REF 15,16

08/27 : Remove PJP20, PJP21, PR48(0 ohm)

0709-Steg: Change PR39 Value for EMI Solution

1A

TDC: 11.19A
OCP: 15.98A

PU7 TPS51116
VLDOIN, VTT, VTTSNS, GND, VTTGND, MODE, VTTREF, COMP, VDDSNS, VDDQSET, DRVH, VBST, LL, DRVL, PGND, S3, S5, V5IN, PGOOD, CS

PQ15 FDS8878
PQ34 FDS6680AS
PL8 1UH 11.0A (MPLC0730L1R0)

PR39 2/0603
PR130 *0_NC
PR38 0
PR131 0
PR133 100K
PR34 11K/F
PR30 76.8K/F
PR36 75K/F
PR27 0
PR28 *0_NC
PR199 *0/0805_NC
PR145 *0/0805_NC
PC193 *2200P/50V_NC
PC132 *2200P/50V_NC
PC40 *0.1U/50V_NC
PC126 10U/25V/1206
PC38 2200P/50V
PC37 0.1U/50V/0603
PC46 0.1U/50V/0603
PC195 0.1U/50V/0603
PC194 0.1U/50V/0603
PC47 220U/4V/ESR25
PC25 10U/4V
PC24 10U/4V
PC122 0.033U/25V
PC26 *0.1U/50V_NC
PC30 *1000P/50V_NC
PC32 4.7U/10V/0805
PC33 0.1U/50V/0603
PC27 *18P/50V_NC

+1.5V_DDR
+1.5V_PWR_SRC
+PWR_SRC
+1.5V_DH
+1.5V_LX
+1.5V_DL
+1.5V_DDR_P
+5V_ALW
+3.3V_SUS
1.5V_DDR_PWRGD 36
STR_EN# 10,56
SIO_SLP_S5# 12,36
RUN_ON
DIS_MODE
V_DDR_MCP_REF
5VIN
0.75V

Frequency(Fixed)	400K

SJ2 Jump20X10
GND_DDR

(Note 1) Current Limiting Setting :
Rtrip(Kohm)=100*(Iocp-0.5*Iripple)*Rds(on)

PQ47 SI4800BDY-T1-E3

PU11 RT9024PE
PGD, DRV, EN, FB, VCC, GND

PR148 100K/0402
PR208 0/0402
PR146 6.8K/F/0402
PR147 20K/F/0402
PC138 10U/4V/0805
PC203 0.1U/10V/0402
PC201 100P/50V/0402
PC202 1U/10V/0603
PC51 0.1U/10V
PC204 22U/6.3V/0805

+1.1V_RUN
TDC : 1.81A
NDV : 1.072V
0.8V
(45) 1.1V_RUN_PWRGD
26,36,50,56 RUN_ON

QUANTA COMPUTER

Title	1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date: Tuesday, September 09, 2008	Sheet 51 of 59	

+1.1V_SUS +1.1V_SUS 13,14
+5V_ALW +5V_ALW 15,30,31,38,39,47,50,51,53,54,56
+3.3V_ALW +3.3V_ALW 23,26,31,32,36,37,38,39,47,48,55,56

08/27 : Remove PR169, PR173 (0 ohm)
08/27 : Add Zener Diode (PD12), PR173 and change PR184=68K, PR181=200K to fix +3.3V_ALW glitch issue when adapter unplug

0916_Rick:Change PC177 value from 0.1U to 1U

Reserve for MAX17020
Reserve for MAX17020
Reserve for MAX17020

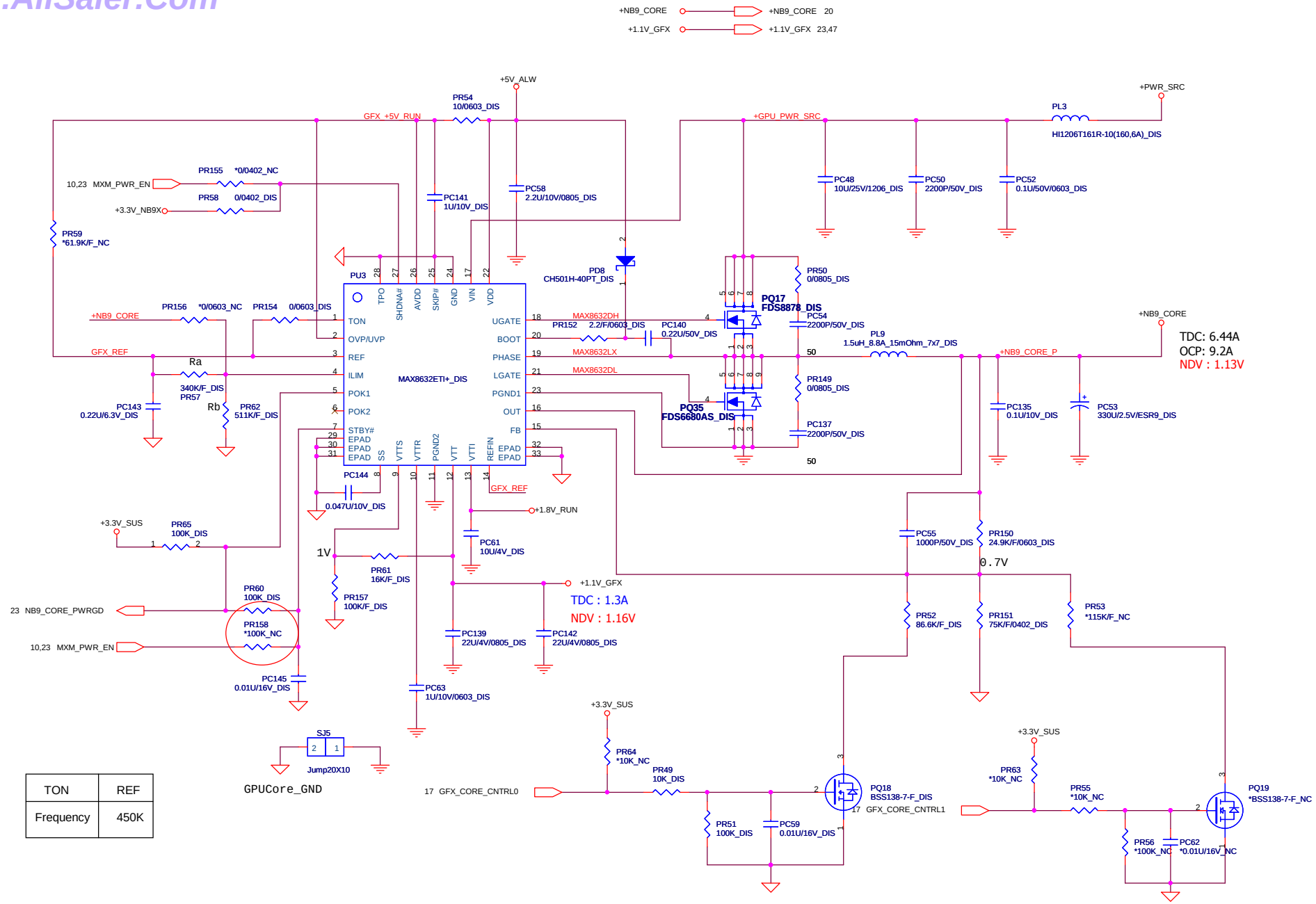
+PWR_SRC
+5V_PWR_SRC
PC173 10U/25V/1206
PC174 10U/25V/1206
PC172 2200P/50V
PC175 0.1U/50V/0603
PR173 *0_NC
PD12 UDZST5-175.6B
6236_VIN
PC181 0.1U/10V
+5V_ALW2
PR178 10/0603
PC182 4.7U/10V/0805
+5V_VCC
PC176 1U/10V
PR188 *0_NC
PC167 0.1U/10V
2VREF
PR187 0
PR197 0
PR198 *0_NC
PC179 0.1U/50V
PC177 1U/6.3V
PR184 68K
EN_LDO
PR181 200K/F
+5V_ALW
TDC: 4.77A
OCP: 6.81A
PQ46 SI4800BDY-T1-E3
PL14 3.3u_13.5A_30mOhm_MPLC0730L3R3
+5V_SRC_P
PR180 *0_NC
PC164 0.1U/50V/0603
PC170 220U/6.3V/ESR25
PR182 0
PR175 *0/0805_NC
PC169 *1500P/50V_NC
PQ44 SI4812BDY-T1-E3
PU9 MAX17020
PAD PAD PAD PAD BYP OUT1 FB1 ILIM1 PGOOD1 ON1 DH1 LX1 PAD PAD PAD
PAD LDOREFIN LDO VIN RTC ONLDO VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 ON2 DH2 LX2
BST1 DL1 VDD SECFB AGND PGND DL2 BST2
+5V_FB1 +5V_ILIM1 +5V_POK1 +5V_EN1 +5V_DH +5V_LX
+3.3V_OUT +3.3V_POK2 +3.3V_EN2 +3.3V_DH +3.3V_LX
PR185 237K/F
PR172 340K/F
PC184 0.1U/50V/0603
PC166 0.1U/50V/0603
PR177 1/0603
PR174 1/0603
+5V_BOOT
+3.3V_BOOT
+3.3V_DL
+5V_DL
+5V_ALW2
SJ3
Jump20X10
GND_SYS
PR205 0
PR206 *0_NC
PC180 1U/10V
PR207 0
PR183 *0_NC
PR186 0
PQ43 SI4800BDY-T1-E3
PQ42 SI4812BDY-T1-E3
PL13 2.2UH_8.2A(MPLC0730L2R2)
+3.3V_SRC
PR168 *0/0805_NC
PR170 0
PC162 *1500P/50V_NC
PR171 *0_NC
+3.3V_ALW
TDC: 6.67A
OCP: 9.53A
PC158 0.1U/50V/0603
PC159 220U/6.3V/ESR25
+3.3V_PWR_SRC
PC160 10U/25V/1206
PC161 10U/25V/1206
PC163 2200P/50V
PC165 0.1U/50V/0603

TON	GND
Frequency	OUT1@400K , OUT2@500K

PR192 39K/F
+5V_ALW2
PR191 0
+3.3V_EN2
PR190 0
THERM_STP# 35
36 5V_ALW_ON
PD11 BAS316
+5V_EN1
PR189 200K/F
PR193 *0_NC
CPU_THERMTRIP# 3
PR179 *0_NC
PR201 *0_NC
GFX_THERMTRIP# 17
PC185 0.1U/50V/0603
PC186 0.1U/50V/0603
PD10 DA204U
PD9 DA204U
+5V_ALW
PC183 0.1U/50V/0603
+3.3V_SUS
PR194 100K
PR195 0
+3.3V_POK2
PR196 0
+5V_POK1
3.3V_5V_ALW_PWRGD 47
PR176 0/0603
+15V_ALW
PC178 0.1U/50V/0603
PR200 *200K/F_NC
2V
PR204 *39K/F_NC
08/27 : Add PR209, PC196 for RC delay

+3.3V_SUS
PR164 100K
47 1.1V_SUS_PWRGD
PU8 MAX1935ETA+
POK OUT2 OUT1 IN1 IN2 SET SHDN GND GND
+3.3V_SUS
PR209 0
PC196 *0.1U/10V_NC
PC156 1U/10V/0603
PR71 0/0603
+1.1V_SUS_P
+1.1V_SUS
TDC: 74mA
NDV : 1.072V
PR163 3.32K/F/0603
0.8V
PR162 10K/F
PC155 10U/4V

QUANTA COMPUTER
Title: SYS 5V/3V(MAX17020)
Size: Document Number IM3 (XPS-Jolie) Rev 1A
Date: Wednesday, September 17, 2008 Sheet 52 of 59



TON	REF
Frequency	450K

ILIM	Iovp=(2*(Rb/(Ra+Rb))*0.1*(1/RDSON)+(I_DELTA/2)
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

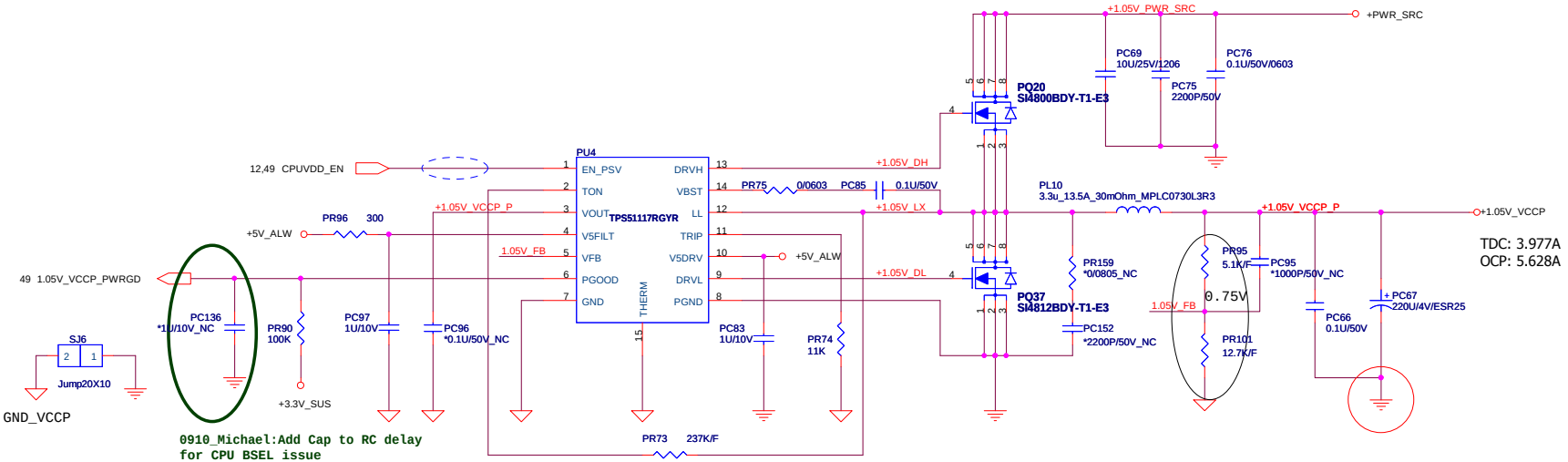
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+NB9_CORE
LOW	LOW	0.9
HIGH	LOW	0.9
HIGH	HIGH	1.1V

QUANTA COMPUTER

Title	VGA DC/DC	
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date: Wednesday, September 17, 2008	Sheet 53 of 59	

+1.05V_VCCP +1.05V_VCCP 3,4,5,13

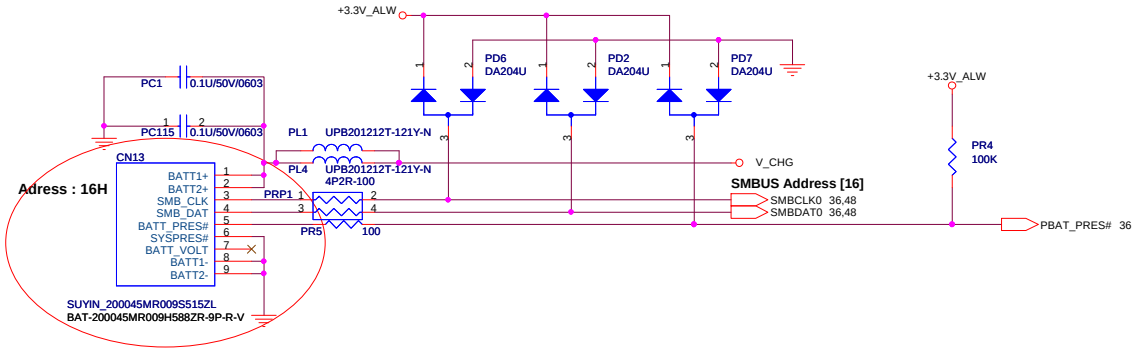
08/27 : Remove 0 ohm (PR79)

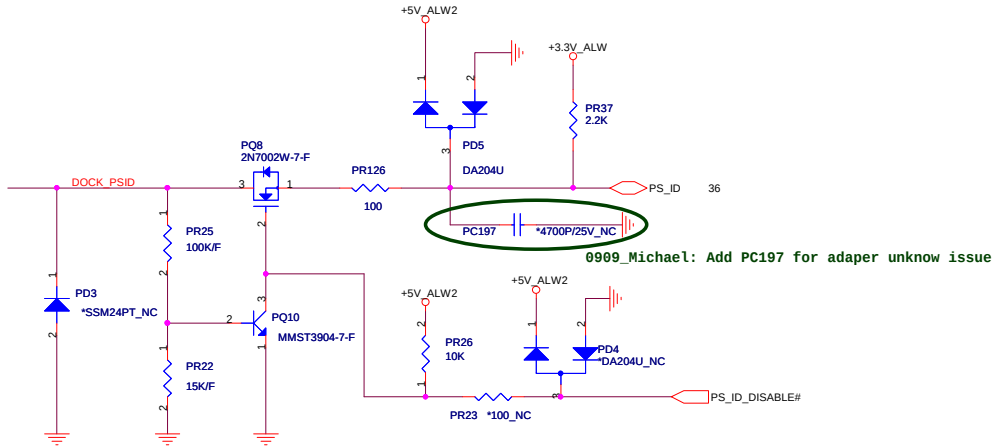


TON	PR185=237K
Frequency	300K

QUANTA COMPUTER

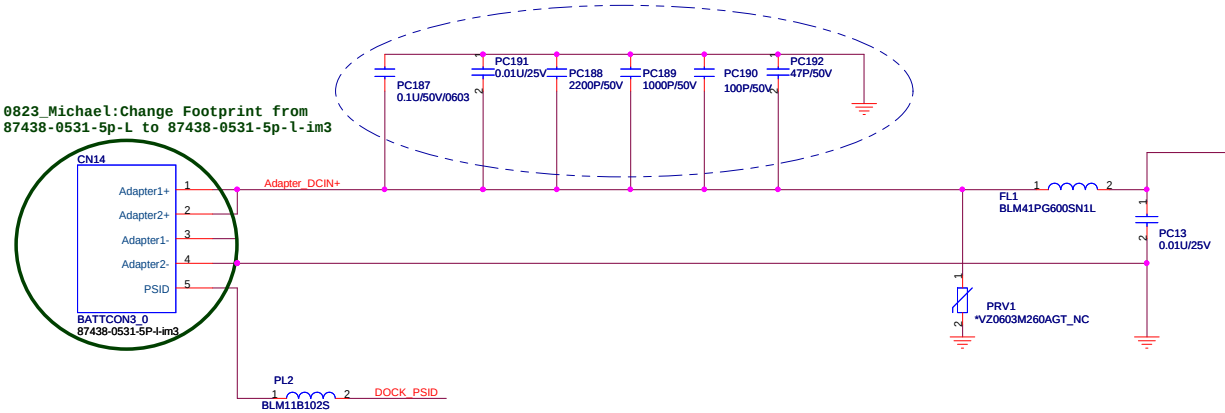
Title	CPUVTT_Core (TPS51117)	
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date: Thursday, September 11, 2008	Sheet 54 of 59	



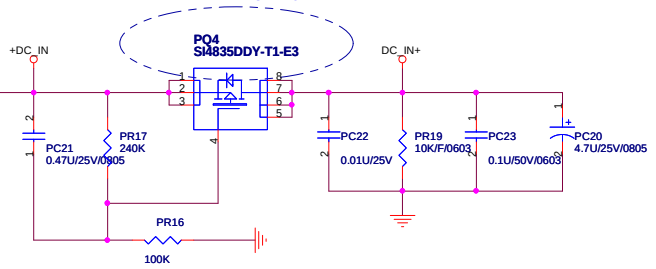


0311-Rick: Add PC187~PC192 for EMC

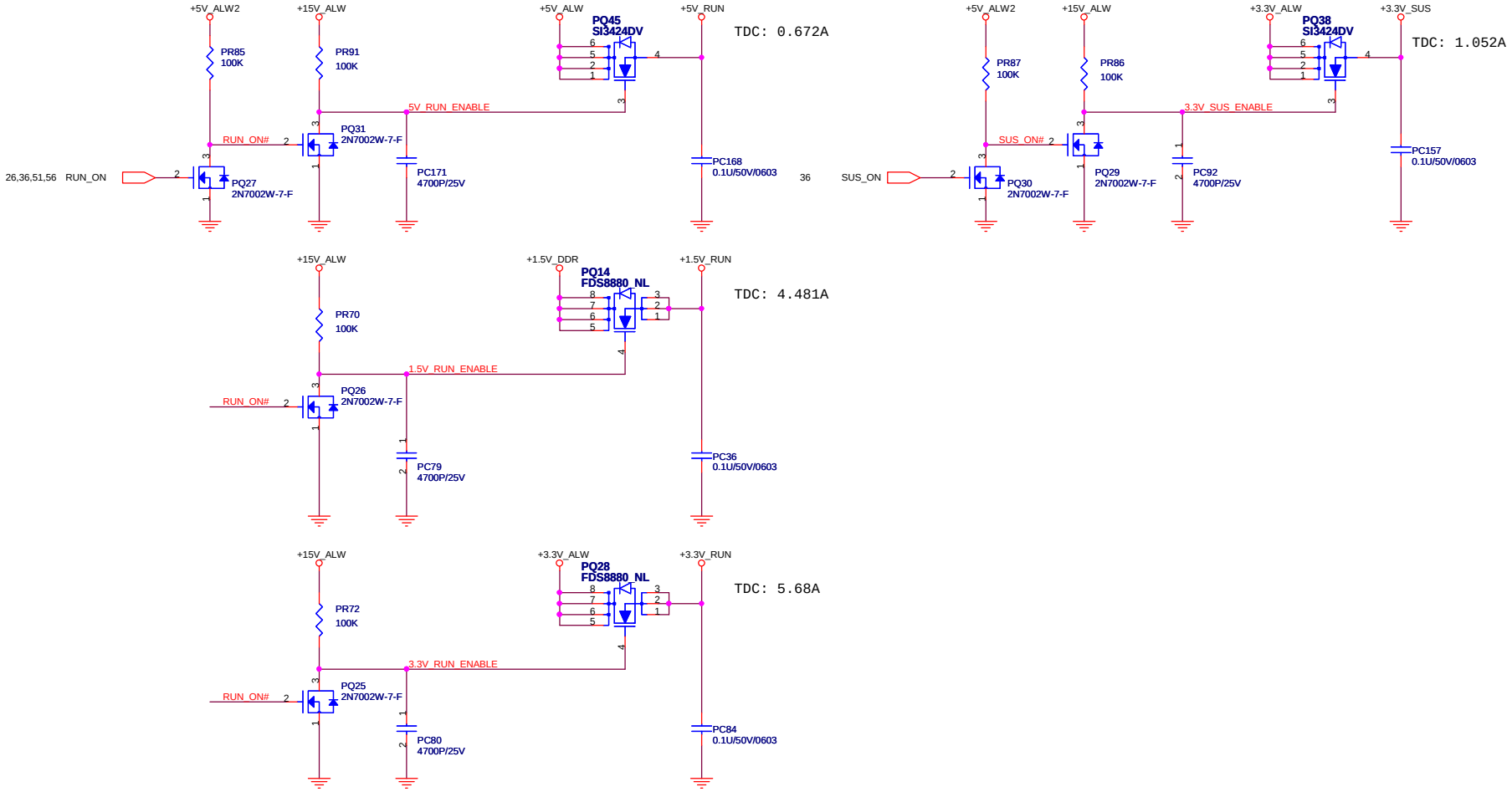
0823_Michael:Change Footprint from 87438-0531-5p-L to 87438-0531-5p-l-im3



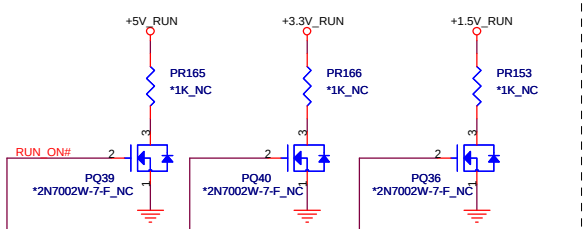
0709-Rick: Change PQ4 Value



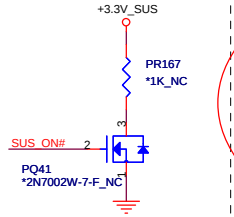
QUANTA COMPUTER		
Title	DCIN,Batt	
Size	Document Number IM3 (XPS-Jolie)	Rev 1A
Date: Thursday, October 23, 2008	Sheet 55 of 59	



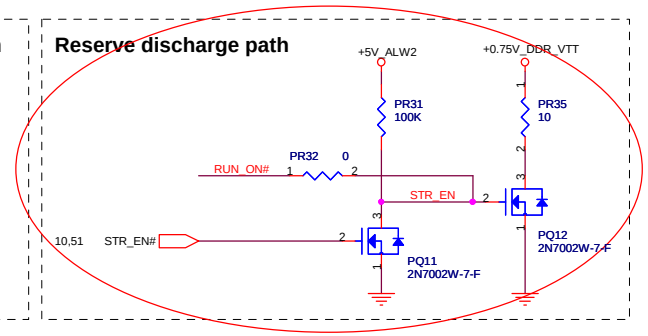
Reserve discharge path



Reserve discharge path

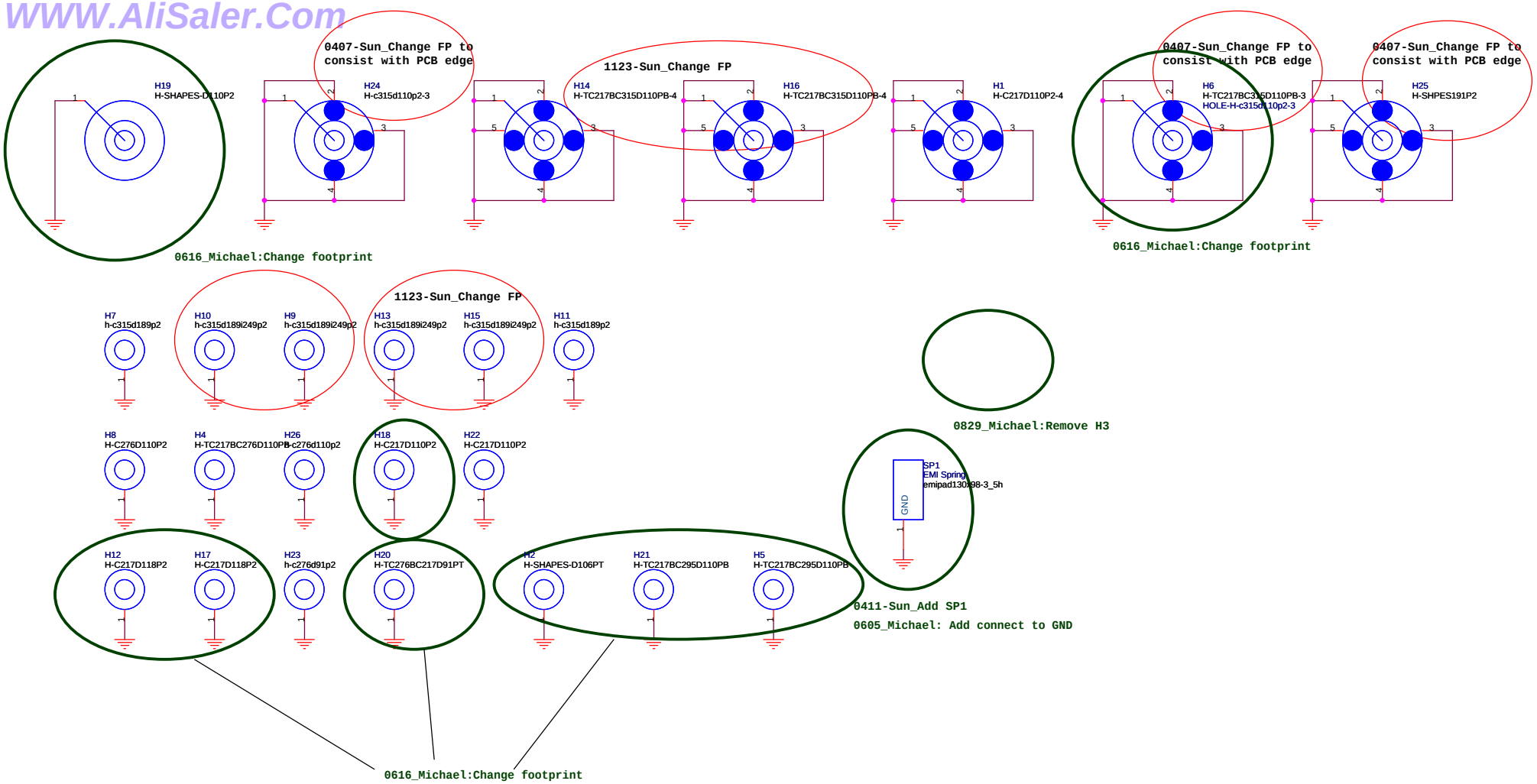


Reserve discharge path



QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number: IM3 (XPS-Jolie)	Rev: 1A
Date: Tuesday, September 09, 2008	Sheet 56 of 59	



QUANTA COMPUTER

Title	SCREW PAD	
Size	Document Number IM3 (XPS-Jolie)	Rev 2A
Date: Thursday, October 23, 2008	Sheet 58 of 59	