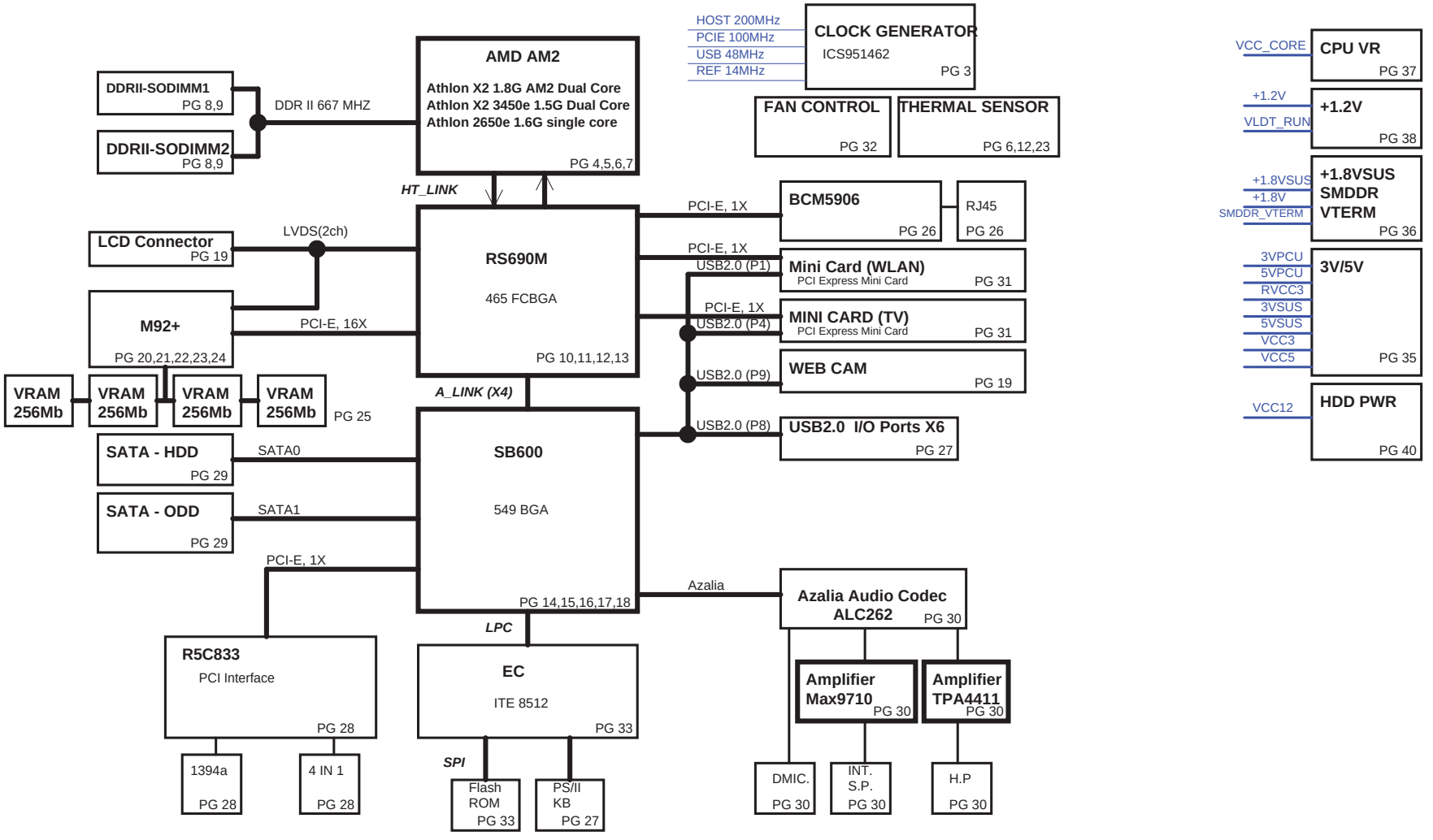
SYSTEM BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	BLOCK DIAGRAM	A

Date: Saturday, February 21, 2009 Sheet 1 of 44

Voltage Rails

Power	Voltage	S0~S2	S3	S4	S5	Ctl Signal
VIN	19V	V	V	V	V	
5VPCU	5V	V	V	V	V	3V5V_EN
3VPCU	3V	V	V	V	V	3V5V_EN
15VPCU	15V	V	V	V	V	3V5V_EN
+3.3VALW	3V	V	V	V	V	STB_ON
+1.2VALW	1.2V	V	V	V	V	STB_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC2.5	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC_NB	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VCC1.1	1.1V	V				MAINON

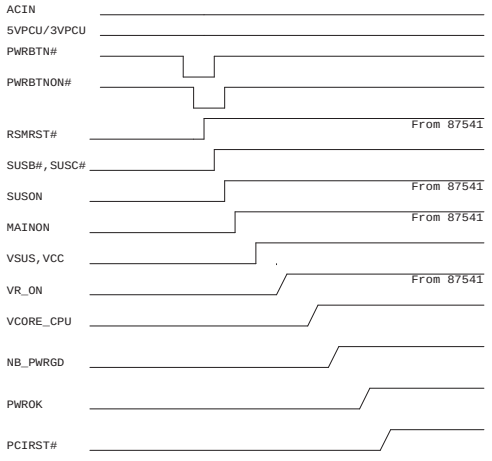
PCI DEVICES IRQ ROUTING

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLK
NB VGA	NA	A		
SB	AD31(INT)	NA	NA	
AC97/AZALIA	AD31	NA	B	INT
USB	AD30	NA	D	INT
R5C843	AD16	0	E/F/G	PCLK0

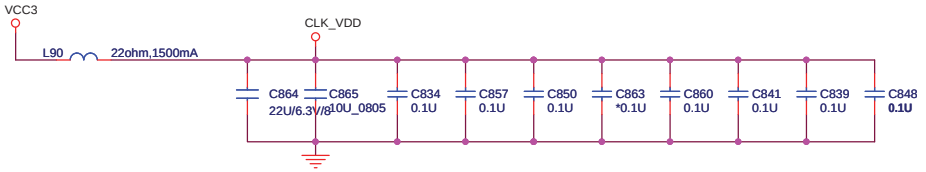
PCB STACK UP

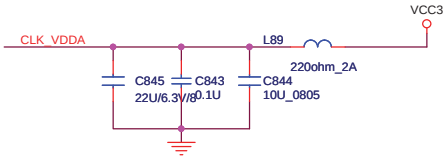
LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : GND
LAYER 5 : VCC
LAYER 6 : IN2
LAYER 7 : GND
LAYER 8 : BOT

Power On Sequence

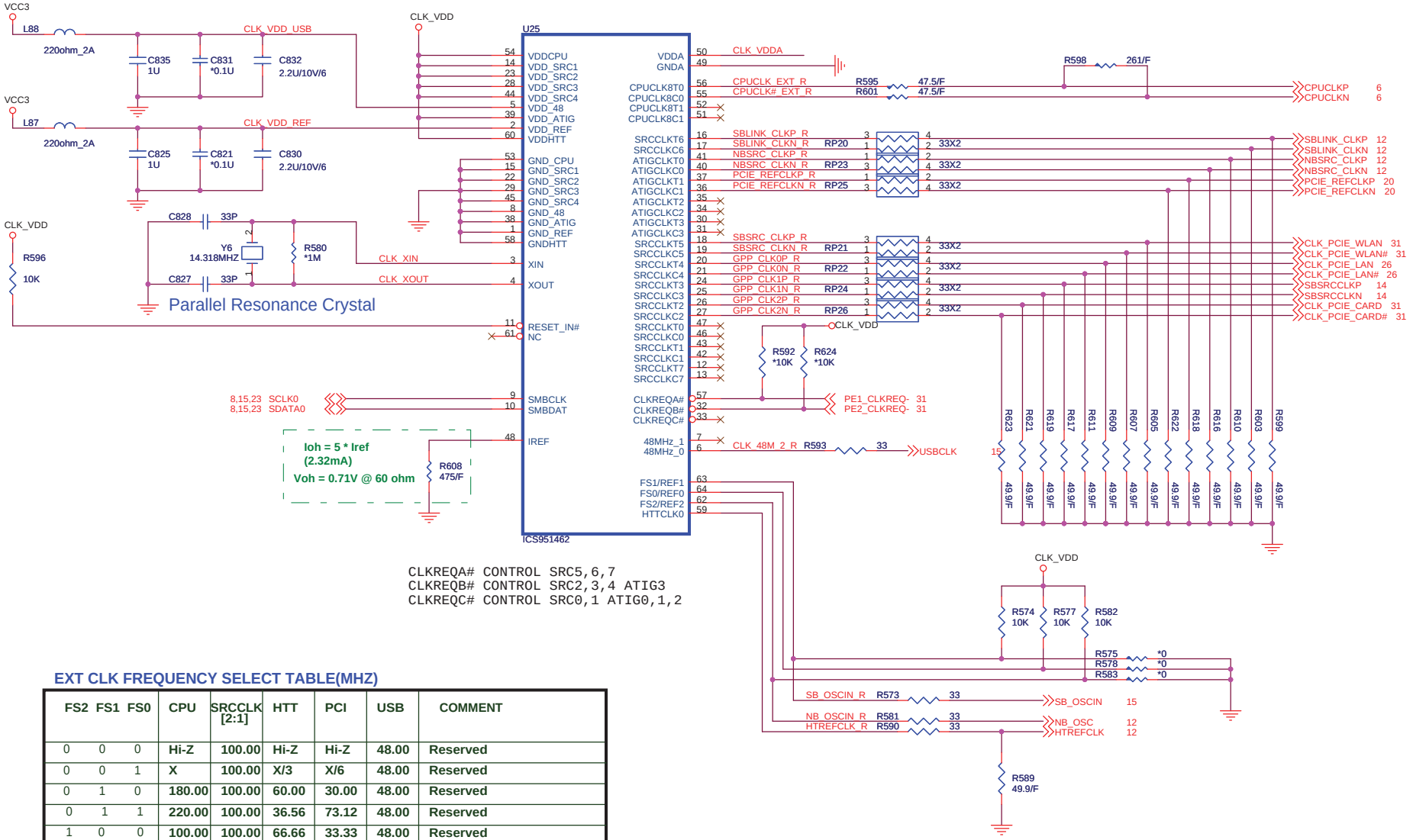


Quanta Computer Inc.
PROJECT : QU1
Size | Document Number: SYSTEM INFORMATION | Rev A
Date: Saturday, February 21, 2009 | Sheet 2 of 44





Put Decoupling Caps close to Clock Fen. power pin



CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4 ATIG3
CLKREQC# CONTROL SRC0,1 ATIG0,1,2

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

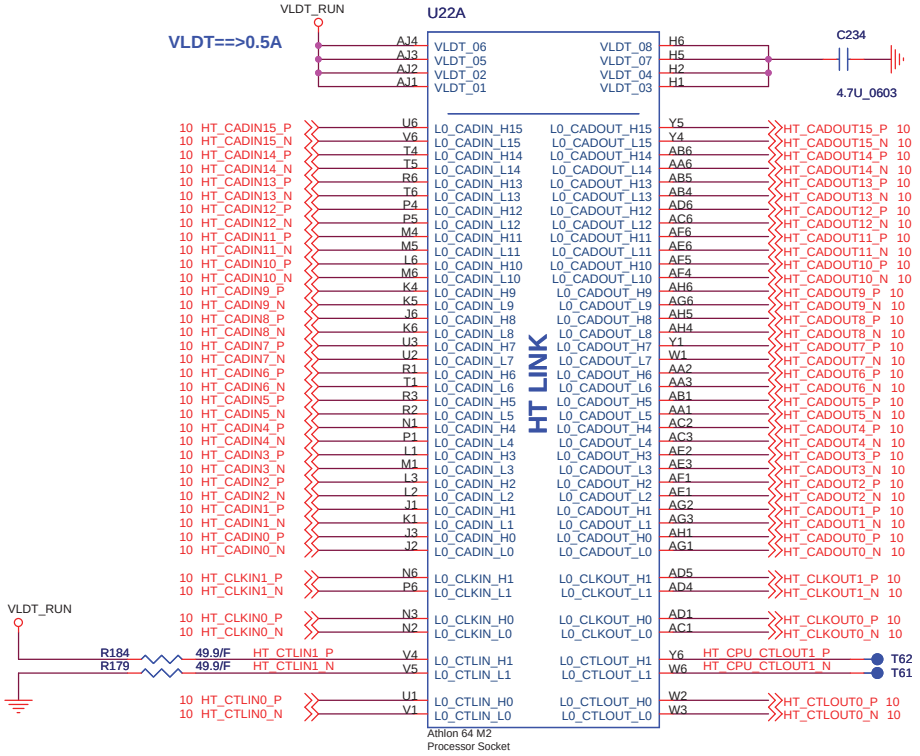
Quanta Computer Inc.
PROJECT : QU1

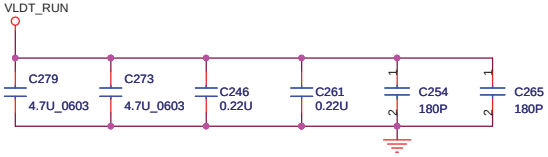
Size	Document Number	Rev
	Clock Generator	C

Date: Saturday, February 21, 2009 Sheet 3 of 44

CPU HyperTransport Interface

VDDLDTRUNCPU is connected to the VDD_LDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.





Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	AMD M2+ HT I/F	C

Date: Saturday, February 21, 2009 Sheet 4 of 44

Processor DDR2 Memory Interface

To SODIMM socket B (Far)

To SODIMM socket A (near)

U22C

DDRII: DATA

8 M_B_DQ[0..63]

M_B_DQ63 AH13
M_B_DQ62 AL13
M_B_DQ61 AL15
M_B_DQ60 AJ15
M_B_DQ59 AF13
M_B_DQ58 AG13
M_B_DQ57 AL14
M_B_DQ56 AK15
M_B_DQ55 AL16
M_B_DQ54 AL17
M_B_DQ53 AK21
M_B_DQ52 AL21
M_B_DQ51 AH15
M_B_DQ50 AJ16
M_B_DQ49 AH19
M_B_DQ48 AL20
M_B_DQ47 AJ22
M_B_DQ46 AL22
M_B_DQ45 AL24
M_B_DQ44 AK25
M_B_DQ43 AJ21
M_B_DQ42 AH21
M_B_DQ41 AH23
M_B_DQ40 AJ24
M_B_DQ39 AL27
M_B_DQ38 AK27
M_B_DQ37 AH31
M_B_DQ36 AG30
M_B_DQ35 AL25
M_B_DQ34 AL26
M_B_DQ33 AJ30
M_B_DQ32 AJ31
M_B_DQ31 E31
M_B_DQ30 E30
M_B_DQ29 B27
M_B_DQ28 A27
M_B_DQ27 F29
M_B_DQ26 F31
M_B_DQ25 A29
M_B_DQ24 A28
M_B_DQ23 A25
M_B_DQ22 A24
M_B_DQ21 C22
M_B_DQ20 D21
M_B_DQ19 A26
M_B_DQ18 B25
M_B_DQ17 B23
M_B_DQ16 A22
M_B_DQ15 B21
M_B_DQ14 A20
M_B_DQ13 C16
M_B_DQ12 D15
M_B_DQ11 C21
M_B_DQ10 A21
M_B_DQ9 A17
M_B_DQ8 A16
M_B_DQ7 B15
M_B_DQ6 A14
M_B_DQ5 E13
M_B_DQ4 E13
M_B_DQ3 C15
M_B_DQ2 A15
M_B_DQ1 A13
M_B_DQ0 D13

MB_DATA63 MB_DATA62 MB_DATA61 MB_DATA60 MB_DATA59 MB_DATA58 MB_DATA57 MB_DATA56 MB_DATA55 MB_DATA54 MB_DATA53 MB_DATA52 MB_DATA51 MB_DATA50 MB_DATA49 MB_DATA48 MB_DATA47 MB_DATA46 MB_DATA45 MB_DATA44 MB_DATA43 MB_DATA42 MB_DATA41 MB_DATA40 MB_DATA39 MB_DATA38 MB_DATA37 MB_DATA36 MB_DATA35 MB_DATA34 MB_DATA33 MB_DATA32 MB_DATA31 MB_DATA30 MB_DATA29 MB_DATA28 MB_DATA27 MB_DATA26 MB_DATA25 MB_DATA24 MB_DATA23 MB_DATA22 MB_DATA21 MB_DATA20 MB_DATA19 MB_DATA18 MB_DATA17 MB_DATA16 MB_DATA15 MB_DATA14 MB_DATA13 MB_DATA12 MB_DATA11 MB_DATA10 MB_DATA9 MB_DATA8 MB_DATA7 MB_DATA6 MB_DATA5 MB_DATA4 MB_DATA3 MB_DATA2 MB_DATA1 MB_DATA0

MA_DATA63 AE14 M_A_DQ63
MA_DATA62 AG14 M_A_DQ62
MA_DATA61 AG16 M_A_DQ61
MA_DATA60 AD17 M_A_DQ60
MA_DATA59 AD13 M_A_DQ59
MA_DATA58 AE13 M_A_DQ58
MA_DATA57 AG15 M_A_DQ57
MA_DATA56 AE16 M_A_DQ56
MA_DATA55 AG17 M_A_DQ55
MA_DATA54 AE18 M_A_DQ54
MA_DATA53 AD21 M_A_DQ53
MA_DATA52 AG22 M_A_DQ52
MA_DATA51 AE17 M_A_DQ51
MA_DATA50 AF17 M_A_DQ50
MA_DATA49 AF21 M_A_DQ49
MA_DATA48 AE21 M_A_DQ48
MA_DATA47 AF23 M_A_DQ47
MA_DATA46 AF23 M_A_DQ46
MA_DATA45 AJ26 M_A_DQ45
MA_DATA44 AG26 M_A_DQ44
MA_DATA43 AF22 M_A_DQ43
MA_DATA42 AG23 M_A_DQ42
MA_DATA41 AH25 M_A_DQ41
MA_DATA40 AF25 M_A_DQ40
MA_DATA39 AJ28 M_A_DQ39
MA_DATA38 AJ29 M_A_DQ38
MA_DATA37 AF29 M_A_DQ37
MA_DATA36 AE26 M_A_DQ36
MA_DATA35 AJ27 M_A_DQ35
MA_DATA34 AH27 M_A_DQ34
MA_DATA33 AG29 M_A_DQ33
MA_DATA32 AF27 M_A_DQ32
MA_DATA31 E29 M_A_DQ31
MA_DATA30 E28 M_A_DQ30
MA_DATA29 D27 M_A_DQ29
MA_DATA28 C27 M_A_DQ28
MA_DATA27 G26 M_A_DQ27
MA_DATA26 F27 M_A_DQ26
MA_DATA25 C28 M_A_DQ25
MA_DATA24 E27 M_A_DQ24
MA_DATA23 F25 M_A_DQ23
MA_DATA22 E25 M_A_DQ22
MA_DATA21 E23 M_A_DQ21
MA_DATA20 D23 M_A_DQ20
MA_DATA19 E26 M_A_DQ19
MA_DATA18 C26 M_A_DQ18
MA_DATA17 G23 M_A_DQ17
MA_DATA16 F23 M_A_DQ16
MA_DATA15 E22 M_A_DQ15
MA_DATA14 E21 M_A_DQ14
MA_DATA13 F17 M_A_DQ13
MA_DATA12 G17 M_A_DQ12
MA_DATA11 G22 M_A_DQ11
MA_DATA10 F21 M_A_DQ10
MA_DATA9 G18 M_A_DQ9
MA_DATA8 E17 M_A_DQ8
MA_DATA7 G16 M_A_DQ7
MA_DATA6 E15 M_A_DQ6
MA_DATA5 G13 M_A_DQ5
MA_DATA4 H13 M_A_DQ4
MA_DATA3 H17 M_A_DQ3
MA_DATA2 E16 M_A_DQ2
MA_DATA1 E14 M_A_DQ1
MA_DATA0 G14 M_A_DQ0

M_A_DQ[0..63] 8

MB_CHECK7 K29
MB_CHECK6 K31
MB_CHECK5 G30
MB_CHECK4 G29
MB_CHECK3 L29
MB_CHECK2 L28
MB_CHECK1 H31
MB_CHECK0 G31

MA_CHECK7 K25
MA_CHECK6 J26
MA_CHECK5 G28
MA_CHECK4 G27
MA_CHECK3 L24
MA_CHECK2 K27
MA_CHECK1 H29
MA_CHECK0 H27

8 M_B_DM[0..7]

M_B_DM7 AJ14
M_B_DM6 AH17
M_B_DM5 AJ23
M_B_DM4 AK29
M_B_DM3 C30
M_B_DM2 A23
M_B_DM1 B17
M_B_DM0 B13

MB_DM8 J29
MB_DM7
MB_DM6
MB_DM5
MB_DM4
MB_DM3
MB_DM2
MB_DM1
MB_DM0

MA_DM8 J25
MA_DM7 AF15 M_A_DM7
MA_DM6 AF19 M_A_DM6
MA_DM5 AJ25 M_A_DM5
MA_DM4 AH29 M_A_DM4
MA_DM3 B29 M_A_DM3
MA_DM2 E24 M_A_DM2
MA_DM1 E18 M_A_DM1
MA_DM0 H15 M_A_DM0

M_A_DM[0..7] 8

MB_DQS_H8 J31
MB_DQS_L8 J30
MB_DQS_H7
MB_DQS_L7
MB_DQS_H6
MB_DQS_L6
MB_DQS_H5
MB_DQS_L5
MB_DQS_H4
MB_DQS_L4
MB_DQS_H3
MB_DQS_L3
MB_DQS_H2
MB_DQS_L2
MB_DQS_H1
MB_DQS_L1
MB_DQS_H0
MB_DQS_L0

MA_DQS_H8 J28
MA_DQS_L8 J27
MA_DQS_H7 AD15 M_A_DQS7
MA_DQS_L7 AE15 M_A_DQS#7
MA_DQS_H6 AG18 M_A_DQS6
MA_DQS_L6 AG19 M_A_DQS#6
MA_DQS_H5 AG24 M_A_DQS5
MA_DQS_L5 AG25 M_A_DQS#5
MA_DQS_H4 AG27 M_A_DQS4
MA_DQS_L4 AG28 M_A_DQS#4
MA_DQS_H3 D29 M_A_DQS3
MA_DQS_L3 C29 M_A_DQS#3
MA_DQS_H2 C25 M_A_DQS2
MA_DQS_L2 D25 M_A_DQS#2
MA_DQS_H1 E19 M_A_DQS1
MA_DQS_L1 F19 M_A_DQS#1
MA_DQS_H0 F15 M_A_DQS0
MA_DQS_L0 G15 M_A_DQS#0

M_A_DQS0 M_A_DQS1 M_A_DQS2 M_A_DQS3 M_A_DQS4 M_A_DQS5 M_A_DQS6 M_A_DQS7

M_A_DQS[0..7] 8

M_A_DQS#0 M_A_DQS#1 M_A_DQS#2 M_A_DQS#3 M_A_DQS#4 M_A_DQS#5 M_A_DQS#6 M_A_DQS#7

M_A_DQS#[0..7] 8

8 M_B_DQS[0..7]

M_B_DQS0 M_B_DQS7 AK13
M_B_DQS1 M_B_DQS#7 AJ13
M_B_DQS2 M_B_DQS6 AK17
M_B_DQS3 M_B_DQS#6 AJ17
M_B_DQS4 M_B_DQS5 AK23
M_B_DQS5 M_B_DQS#5 AL23
M_B_DQS6 M_B_DQS4 AL28
M_B_DQS7 M_B_DQS#4 AL29

8 M_B_DQS#[0..7]

M_B_DQS#0 M_B_DQS3 D31
M_B_DQS#1 M_B_DQS2 C24
M_B_DQS#2 M_B_DQS#2 C23
M_B_DQS#3 M_B_DQS1 D17
M_B_DQS#4 M_B_DQS#1 C17
M_B_DQS#5 M_B_DQS0 C14
M_B_DQS#6 M_B_DQS#0 C13
M_B_DQS#7

Athlon 64 M2
Processor Socket

1.8VSUS

R136 2K/F

CPU_M_VREF

C189 0.1U
C188 1000P
R137 2K/F

SMDDR_VTERM

VTT==>1.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

1.8VSUS

R167 39.2F

R163 39.2F

T35

U22B

DDR II: CMD/CTRL/CLK

D12 VTT1
C12 VTT2
B12 VTT3
A12 VTT4
AK12 VTT5
AJ12 VTT6
AH12 VTT7
AG12 VTT8
AL12 VTT9

CPU_M_VREF F12 MEMVREF

VTT_SENSE E12 VTT_SENSE

M_ZN AH11 MEMZN
M_ZP AJ11 MEMZP

8,9 M_A_CS#3 AD27 PMA1_CS_L1
8,9 M_A_CS#2 AA25 PMA1_CS_L0
8,9 M_A_CS#1 AC25 PMA0_CS_L1
8,9 M_A_CS#0 AA24 PMA0_CS_L0

8,9 M_B_CS#3 AE29 PMB1_CS_L1
8,9 M_B_CS#2 AB31 PMB1_CS_L0
8,9 M_B_CS#1 AE30 PMB0_CS_L1
8,9 M_B_CS#0 AC31 PMB0_CS_L0

8,9 M_CKE3 M31 MB_CKE1
8,9 M_CKE2 M29 MB_CKE0
8,9 M_CKE1 L27 MA_CKE1
8,9 M_CKE0 M25 MA_CKE0

8,9 M_A_A[0..15]

M_A_A15 M27 MA_ADD15
M_A_A14 N24 MA_ADD14
M_A_A13 AC26 MA_ADD13
M_A_A12 N26 MA_ADD12
M_A_A11 P25 MA_ADD11
M_A_A10 Y25 MA_ADD10
M_A_A9 N27 MA_ADD9
M_A_A8 R24 MA_ADD8
M_A_A7 P27 MA_ADD7
M_A_A6 R25 MA_ADD6
M_A_A5 R26 MA_ADD5
M_A_A4 R27 MA_ADD4
M_A_A3 T25 MA_ADD3
M_A_A2 U25 MA_ADD2
M_A_A1 T27 MA_ADD1
M_A_A0 W24 MA_ADD0

8,9 M_A_BS#2 N25 MA_BANK2
8,9 M_A_BS#1 Y27 MA_BANK1
8,9 M_A_BS#0 AA27 MA_BANK0

8,9 M_A_RAS# AA26 PMA_RAS_L
8,9 M_A_CAS# AB25 PMA_CAS_L
8,9 M_A_WE# AB27 PMA_WE_L

Athlon 64 M2
Processor Socket

MA1_CLK_H2 AE20
MA1_CLK_L2 AE19
MA1_CLK_H1 G20
MA1_CLK_L1 G21
MA1_CLK_H0 V27
MA1_CLK_L0 W27
MA0_CLK_H2 AG21 M_CLKOUT1 8
MA0_CLK_L2 AG20 M_CLKOUT1# 8
MA0_CLK_H1 G19 M_CLKOUT0 8
MA0_CLK_L1 H19 M_CLKOUT0# 8
MA0_CLK_H0 U27
MA0_CLK_L0 U26

MB1_CLK_H2 AL19
MB1_CLK_L2 AL18
MB1_CLK_H1 C19
MB1_CLK_L1 D19
MB1_CLK_H0 W29
MB1_CLK_L0 W28
MB0_CLK_H2 AJ19 M_CLKOUT4 8
MB0_CLK_L2 AK19 M_CLKOUT4# 8
MB0_CLK_H1 A18 M_CLKOUT3 8
MB0_CLK_L1 A19 M_CLKOUT3# 8
MB0_CLK_H0 U31
MB0_CLK_L0 U30

MB1_ODT0 AD31
MB0_ODT0 AD29
MA1_ODT0 AC27 M_ODT1 8,9
MA0_ODT0 AC28 M_ODT0 8,9

M_B_A[0..15] 8,9

MB_ADD15 N28 M_B_A15
MB_ADD14 N29 M_B_A14
MB_ADD13 AE31 M_B_A13
MB_ADD12 N30 M_B_A12
MB_ADD11 P29 M_B_A11
MB_ADD10 AA29 M_B_A10
MB_ADD9 P31 M_B_A9
MB_ADD8 R29 M_B_A8
MB_ADD7 R28 M_B_A7
MB_ADD6 R31 M_B_A6
MB_ADD5 R30 M_B_A5
MB_ADD4 T31 M_B_A4
MB_ADD3 T29 M_B_A3
MB_ADD2 U29 M_B_A2
MB_ADD1 U28 M_B_A1
MB_ADD0 AA30 M_B_A0

MB_BANK2 N31
MB_BANK1 AA31 M_B_BS#1 8,9
MB_BANK0 AA28 M_B_BS#0 8,9

MB_RAS_L AB29 M_B_RAS# 8,9
MB_CAS_L AC29 M_B_CAS# 8,9
MB_WE_L AC30 M_B_WE# 8,9

SMDDR_VTERM

C180 4.7U_0603
C182 4.7U_0603
C179 4.7U_0603
C34 4.7U_0603
C35 0.22U
C122 0.22U
C170 0.22U
C26 0.22U

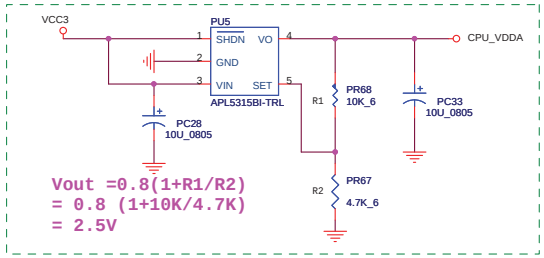
C795 1000P
C774 1000P
C796 1000P
C779 1000P
C797 180P
C784 180P
C800 180P
C787 180P

Quanta Computer Inc.

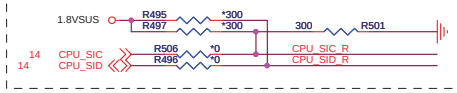
PROJECT : QU1

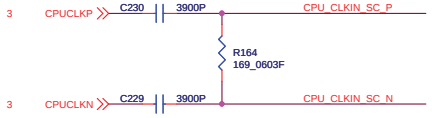
Size	Document Number	Rev
	AMD M2+ DDR II Memory I/F	C
Date: Saturday, February 21, 2009	Sheet 5 of 44	

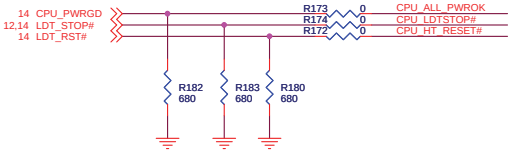
ATHLON Control and Debug

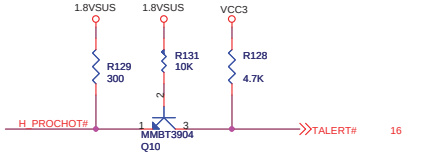


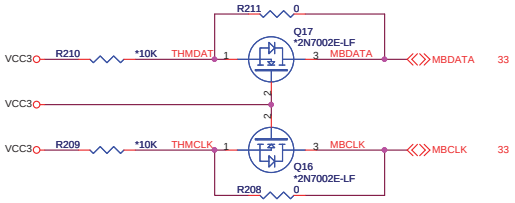
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

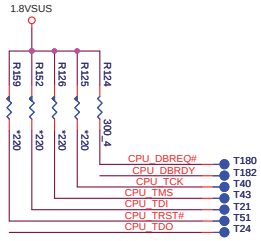




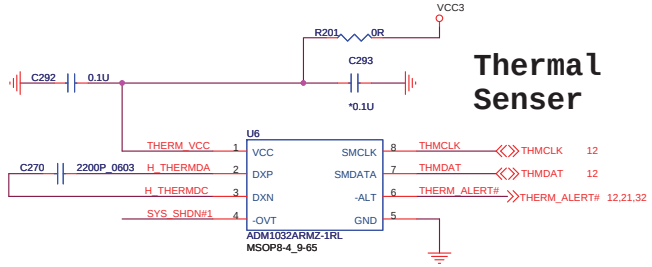




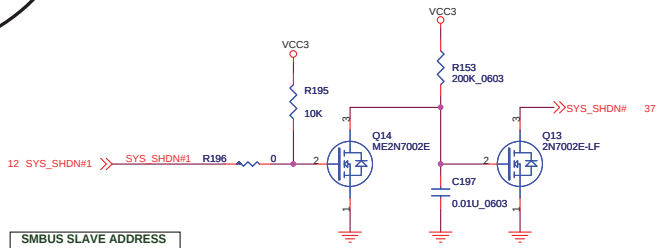




NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.



Thermal Senser



SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)

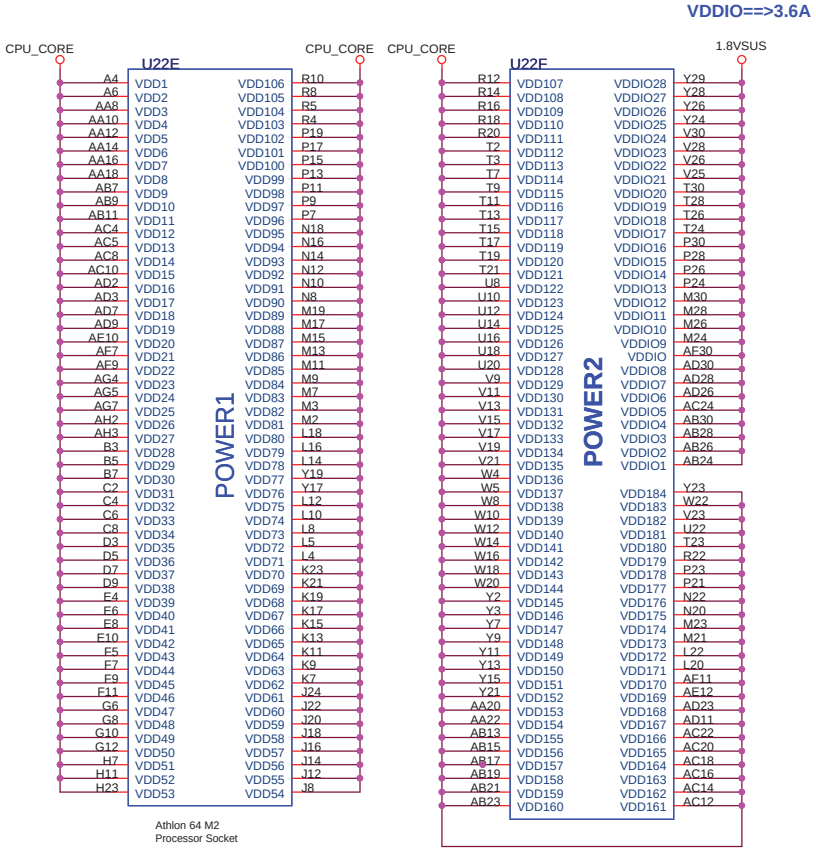
Quanta Computer Inc.
PROJECT : QU1

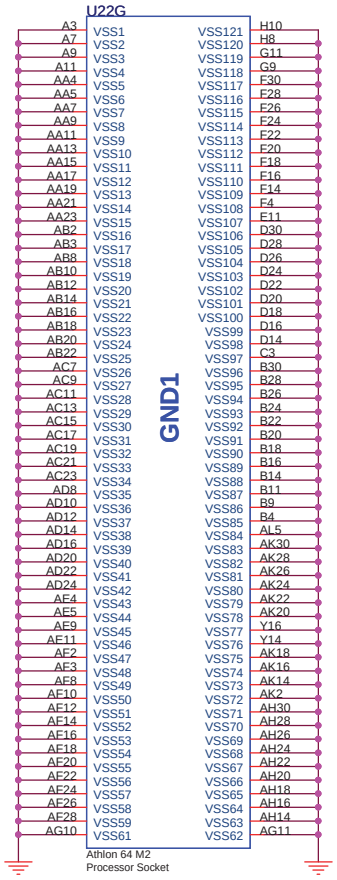
Size	Document Number	Rev
	AMD M2+ CTRL & DEBUG	C

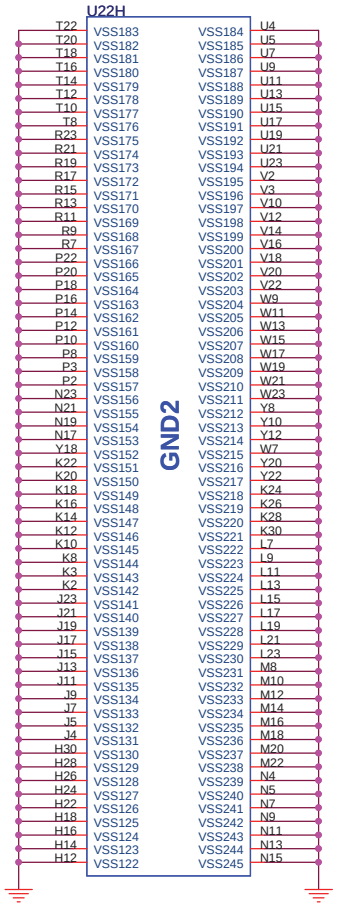
Date: Saturday, February 21, 2009 Sheet 6 of 44

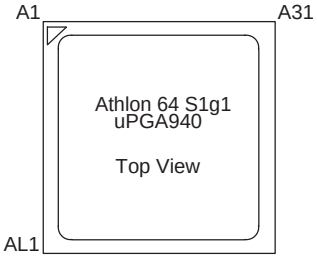
PROCESSOR POWER AND GROUND

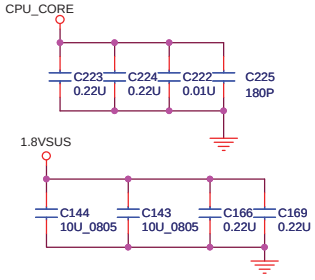
VDDIO==>3.6A



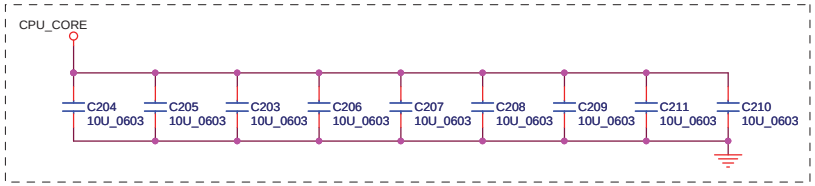


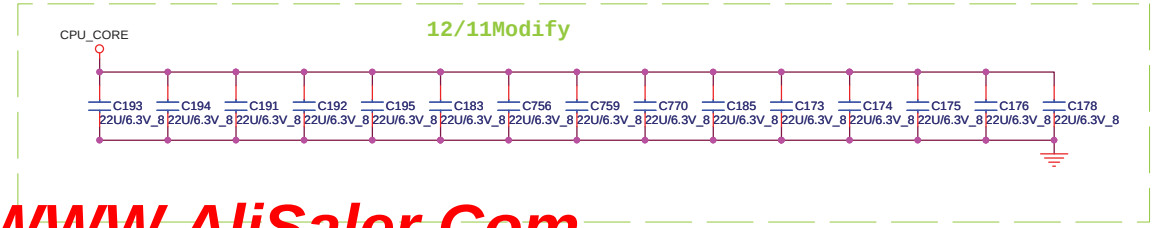




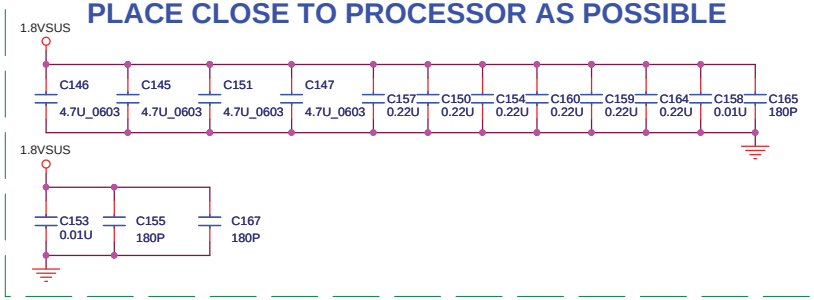


BOTTOMSIDE DECOUPLING





DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



Quanta Computer Inc.

PROJECT : QU1

Size	Document Number	Rev
	AMD M2+ PWR & GND	C

Date: Saturday, February 21, 2009 Sheet 7 of 44

12/01 change CN14 footprint (ddr-as0a426-nfsb-7f-20

SA_A : 00

SA_B : 10

CN15

SO-DIMM

(H=6.5)

ES2 1121

CN14

SO-DIMM

(H=11)

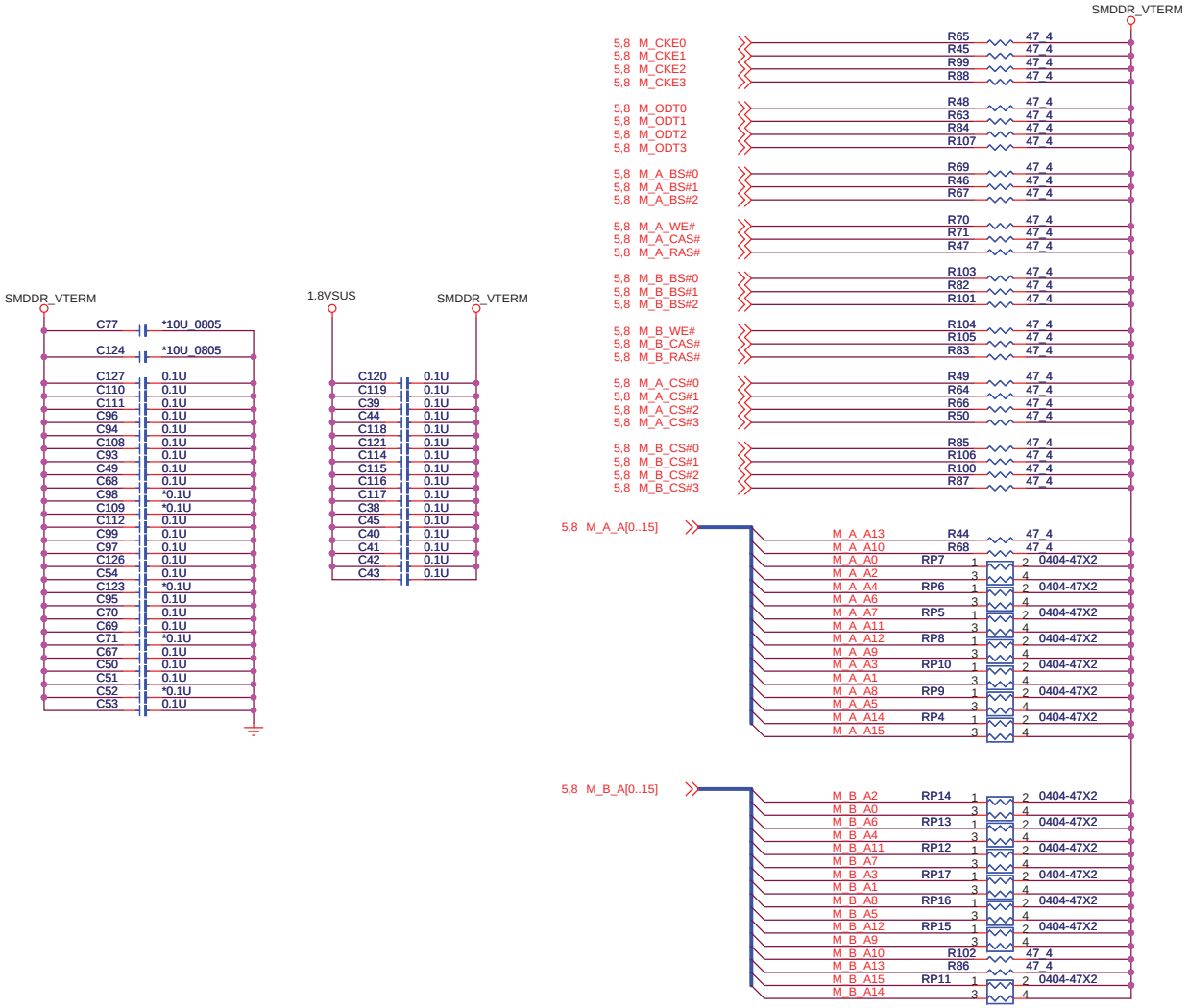
For EMI

DDRII_SODIMM_R

1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : QU1

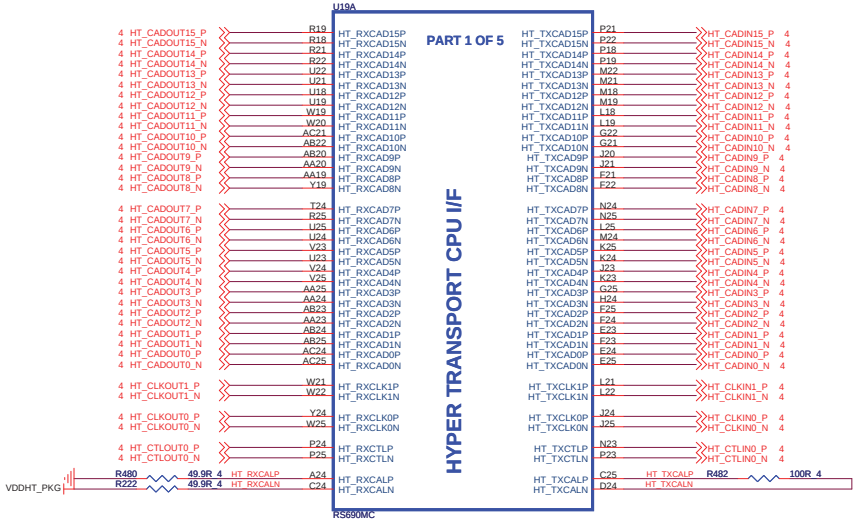
Size	Document Number	Rev
	DDRII SODIMM x2	C
Date: Saturday, February 21, 2009	Sheet 8 of 44	



Quanta Computer Inc.

PROJECT : QU1

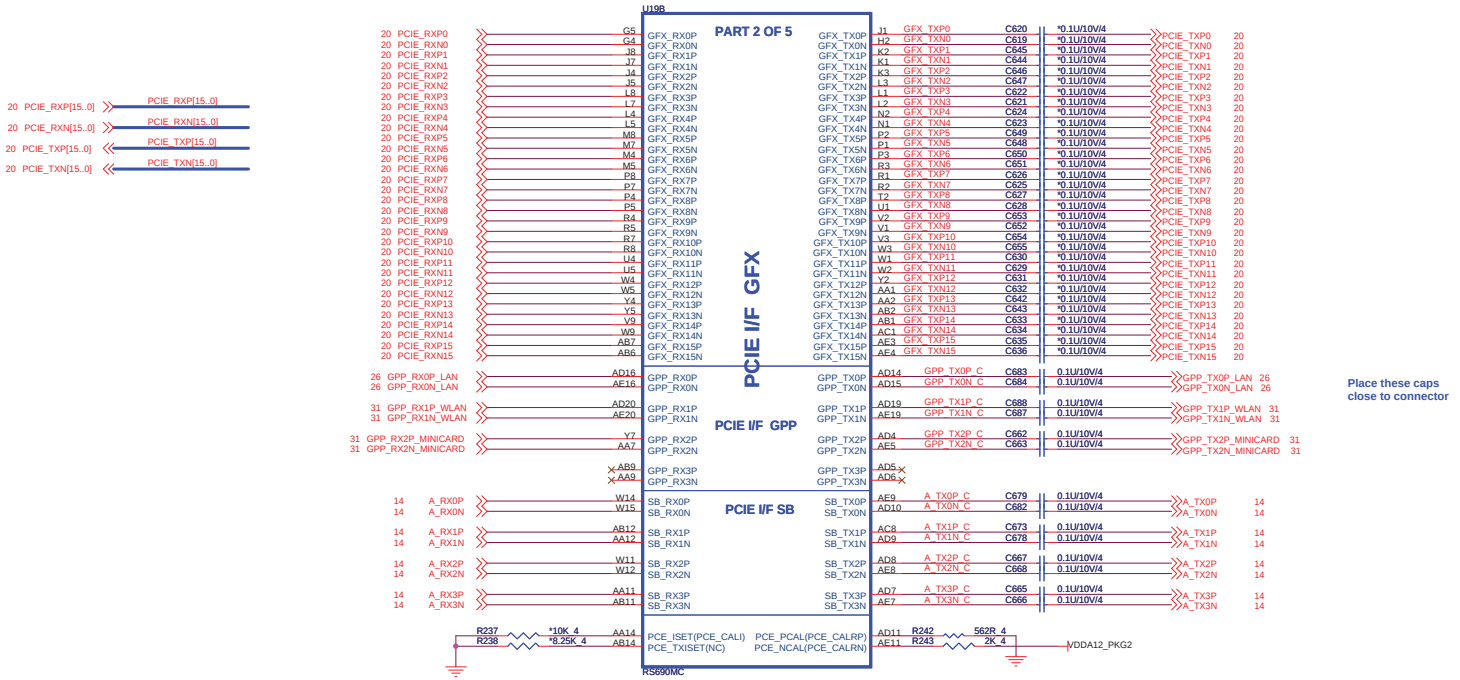
Size	Document Number	Rev
	DDRII TERMINATION	C
Date: Saturday, February 21, 2009	Sheet 9 of 44	



Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	RS690MC HT LINK I/F	A

Date: Saturday, February 21, 2009 Sheet 10 of 44



Quanta Computer Inc.			
PROJECT : QU1			
Size	Document Number		Rev
	RS690MC PCIE LINK I/F		A
Date: Saturday, February 21, 2009	Sheet 11 of 44		

HTPVDD==>2.98mA(min)/3.03mA(MAX)

VCC1.8 — L24 220ohm_2A — HTPVDD — C313 *10U/6.3V/6 — C311 2.2U/10V/6

PLLVDD==>3.54mA(min)/3.61mA(MAX)

VCC1.8 — L64 220ohm_2A — PLLVDD — C670 *10U/6.3V/6 — C669 2.2U/10V/6

AVDDQ==>0.1mA(min)/0.11mA(MAX)

VCC1.8 — L70 220ohm_2A — AVDDQ — C694 *10U/6.3V/6 — C693 2.2U/10V/6

AVDD_NB==>5.42mA(min)/5.44mA(MAX)

VCC3 — L26 22ohm,1500mA — AVDD_NB — C321 2.2U/10V/6 — C323 *0.1U/25V/4

VCC1.8 — R473 0R_6 — AVDDI — C689 2.2U/10V/6

AVDDI==>0mA(min)/0mA(MAX)

VCC1.8 — R260 10K_4 — VCC3 — R259 10K_4

6,14 LDT_STOP# — Q21 MMBT3904 — LDT_STOP# NB

PLLVDD12 — C671 2.2U/10V/6

U19C

RS690MC

AVDD_NB — B22 AVDD1, C22 AVDD2

AVDDI — G17 AVSSN1, H17 AVSSN2, A20 AVDDDI, B20 AVSSDI

AVDDQ — A21 AVDDQ, A22 AVSSQ — C692 *0.1U/25V/4

CRT/TVOUT

T148 T129 T102 — C21 C, C20 Y, D19 COMP

T101 T106 T103 T128 T124 — E19 RED, F19 GREEN, G19 BLUE, C6 DACVSYNC, A5 DACHSYNC

R474 715R_4 — B21 RSET

T126 T127 — B6 DACSCL, A6 DACSDA

PLLVDD — A10 PLLVDD18, B10 PLLVSS

HTPVDD — B24 HTPVDD, B25 HTPVSS

PWR

14 NB_RST# — C10 SYSRESET#

19,33 NB_PWRGD — C11 POWERGOOD

LDT_STOP# NB — C5 LDTSTOP#

14 ALLOW_LDTSTOP — B5 ALLOW_LDTSTOP

CLOCKs

R219 10K_4 — 3 HTREFCLK — C23 HTTSTCLK, B23 HTREFCLK

TV_SWITCH — C2 TVCLKIN

3 NB_OSC — B11 OSCIN

VDDA12 — L65 60ohm,500mA — PLLVDD12 — A11 OSCOUT(PLLVDD12)

3 NBSRC_CLKP — F2 GFX_CLKP

3 NBSRC_CLKN — F1 GFX_CLKN

3 SBLINK_CLKP — G1 SB_CLKP

3 SBLINK_CLKN — G2 SB_CLKN

MIS.

R250 *3K_4 — R256 *3K_4 DFT_GPIO0 — D6 DFT_GPIO0

LOAD_ROM# — D7 DFT_GPIO1

R471 *3K_4 DFT_GPIO2 — C8 DFT_GPIO2

R253 *3K_4 DFT_GPIO3 — C7 DFT_GPIO3

R469 *3K_4 DFT_GPIO4 — B8 DFT_GPIO4

R470 *3K_4 DFT_GPIO5 — A8 DFT_GPIO5

R467 *0R_4 — 14 BMREQ# — B2 BMREQ#

19 NB_LVDS_CLK — A2 I2C_CLK

19 NB_LVDS_DAT — B4 I2C_DATA

NB_THERMDA — AA15 THERMALDIODE_P

23 NB_THERMDA

NB_THERMDC — AB15 THERMALDIODE_N

23 NB_THERMDC

T111 T125 — C14 TMDS_HPD, B3 DDC_DATA, C3 TESTMODE

41 STRP_DATA — STRP_DATA — A3 STRP_DATA

R261 4.7K_4

LVDS

PART 3 OF 5

TXOUT_L0P B14 — R239 *0 — NB_TXLOUT0+ 19

TXOUT_L0N B15 — R240 *0 — NB_TXLOUT0- 19

TXOUT_L1P B13 — R245 *0 — NB_TXLOUT1+ 19

TXOUT_L1N A13 — R246 *0 — NB_TXLOUT1- 19

TXOUT_L2P H14 — R241 *0 — NB_TXLOUT2+ 19

TXOUT_L2N G14 — R244 *0 — NB_TXLOUT2- 19

TXOUT_L3P D17 — R247 *0 — NB_TXLOUT3+ 19

TXOUT_L3N E17 — R248 *0 — NB_TXLOUT3- 19

TXOUT_U0P A15 — R227 *0 — NB_TXUOUT0+ 19

TXOUT_U0N B16 — R225 *0 — NB_TXUOUT0- 19

TXOUT_U1P C17 — R233 *0 — NB_TXUOUT1+ 19

TXOUT_U1N C18 — R231 *0 — NB_TXUOUT1- 19

TXOUT_U2P B17 — R220 *0 — NB_TXUOUT2+ 19

TXOUT_U2N A17 — R218 *0 — NB_TXUOUT2- 19

TXOUT_U3P A18 — R226 *0 — NB_TXUOUT3+ 19

TXOUT_U3N B18 — R223 *0 — NB_TXUOUT3- 19

TXCLK_LP E15 — R232 *0 — NB_TXLCLKOUT+ 19

TXCLK_LN D15 — R234 *0 — NB_TXLCLKOUT- 19

TXCLK_UP H15 — R236 *0 — NB_TXUCLKOUT+ 19

TXCLK_UN G15 — R235 *0 — NB_TXUCLKOUT- 19

LPVDD==>4.86mA(min)/4.9mA(MAX)

LPVDD D14, LPVSS E14 — C358 0.1U/25V/4 — C359 4.7U/6.3V/6 — L30 220ohm_2A — LPVDD — VCC1.8

LVDDR18D==>40.2mA(min)/43.84mA(MAX)

LVDDR18D_1 A12, LVDDR18D_2 B12 — GND_LPVSS — VCC1.8

LVDDR33_1 C12, LVDDR33_2 C13 — L67 220ohm_2A — VCC3

LVDDR33==>76.77mA(min)/78.64mA(MAX)

LVSSR1 A16, LVSSR3 A14, LVSSR5 D12, LVSSR6 C19, LVSSR7 C15, LVSSR8 C16, LVSSR12 F14, LVSSR13 F15

C680 0.1U/25V/4 — C681 4.7U/6.3V/6 — C685 0.1U/25V/4 — C686 4.7U/6.3V/6

R472 0R_6 — GND_LVSSR

LVDS_DIGON F12 — DIGON 19

LVDS_BLON G12 — BLON 19

LVDS_BLEN F12 — T114

R249 0R_6 — GND_LPVSS

DEBUG

DEBUG_6 AE15 — T110

DEBUG_9 AC17 — T107

DEBUG_10 AD18 — T104

DEBUG_15 AE21 — T136

DEBUG_0 AD13 — T112

DEBUG_2 AC13 — T109

DEBUG_1 AE13 — T113

DEBUG_14 AE17 — T108

DEBUG_13 AD17 — T105

NB Thermal Senser

3VPCU — C318 0.1U/25V/4 — C319 *0.1U/25V/4

U7 ADM1032ARMZ-2R MSOP8-1_9-65

THERM_NB_VCC 1 — VCC — SMCLK 8 — THMCLK

C325 2200P/50V/4 — NB_THERMDA 2 — DXP — SMDATA 7 — THMDAT

NB_THERMDC 3 — DXN — -ALT 6 — THERM_ALERT# 6,21,32

6 SYS_SHDN#1 — 4 -OVT — GND 5

VCC3 — R689 10K_4

VCC3 — R468 *10K_4 STRP_DATA

R465 10K_4 TV_SWITCH

LOAD_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE

Low, LOAD ROM STRAP ENABLE

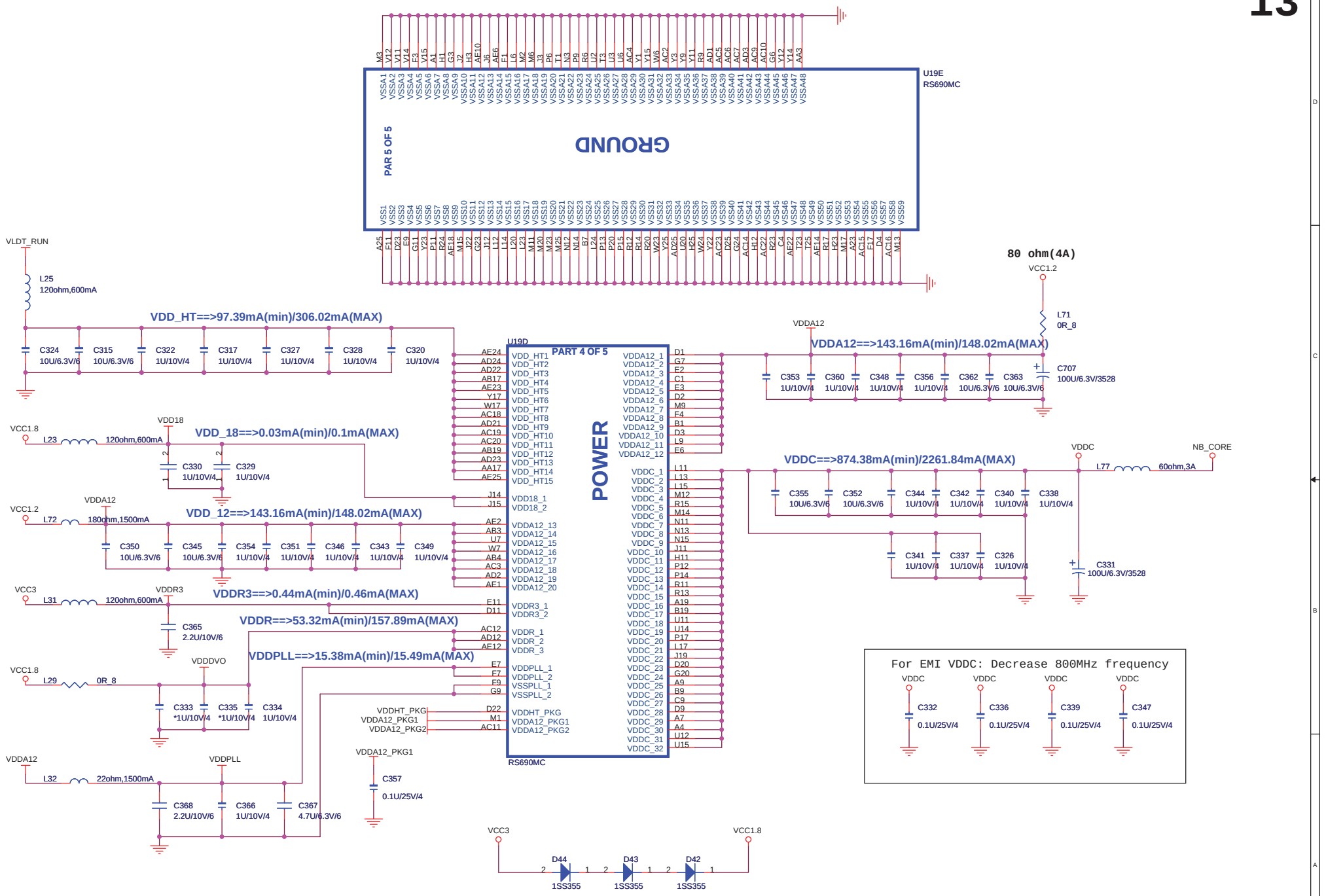
12/29 ADD R689 to link VCC3(Therm_Alert# must push Hi)

Quanta Computer Inc.

PROJECT : QU1

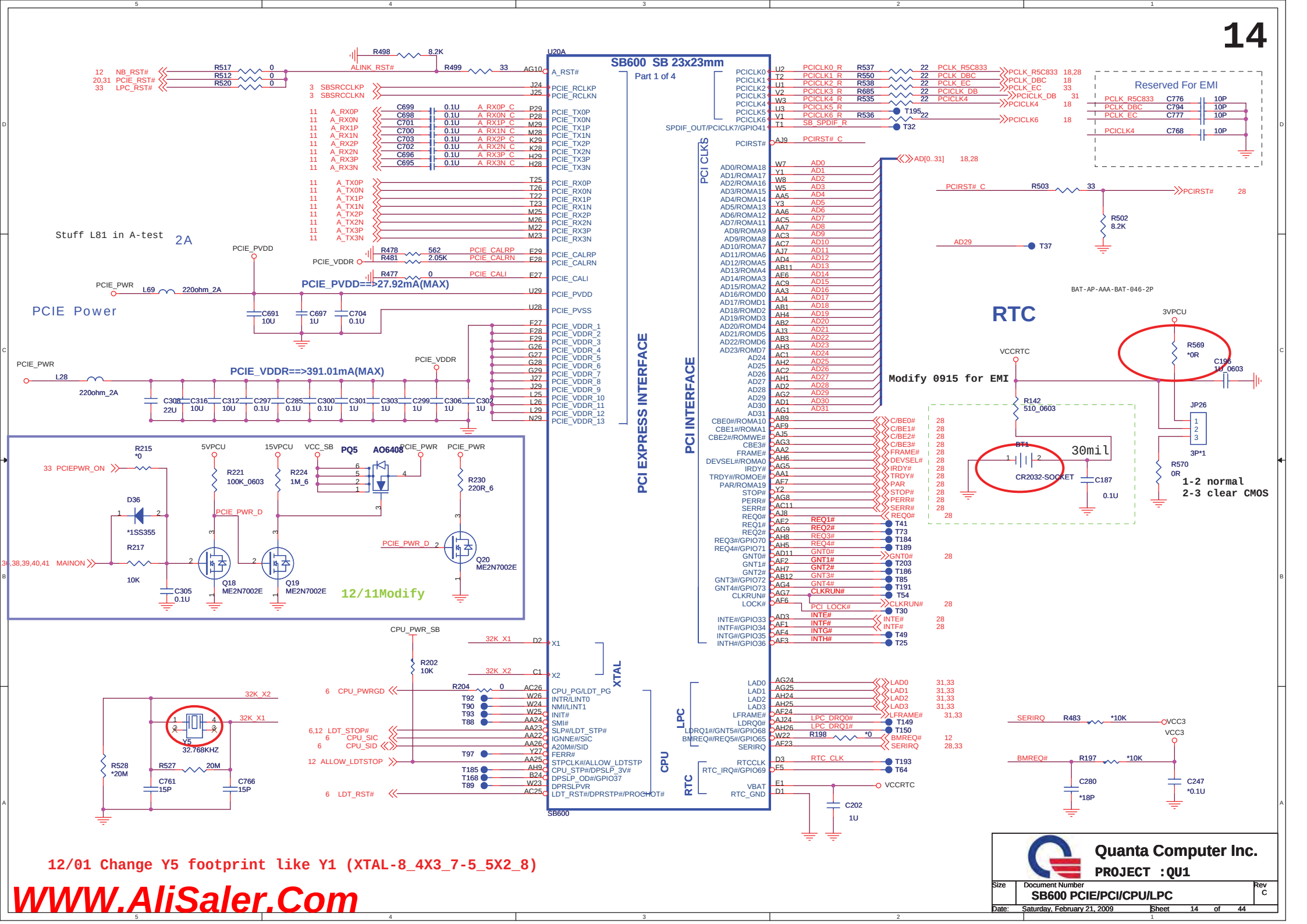
Size	Document Number	Rev
	RS690MC PLL & VEDIO I/F	A

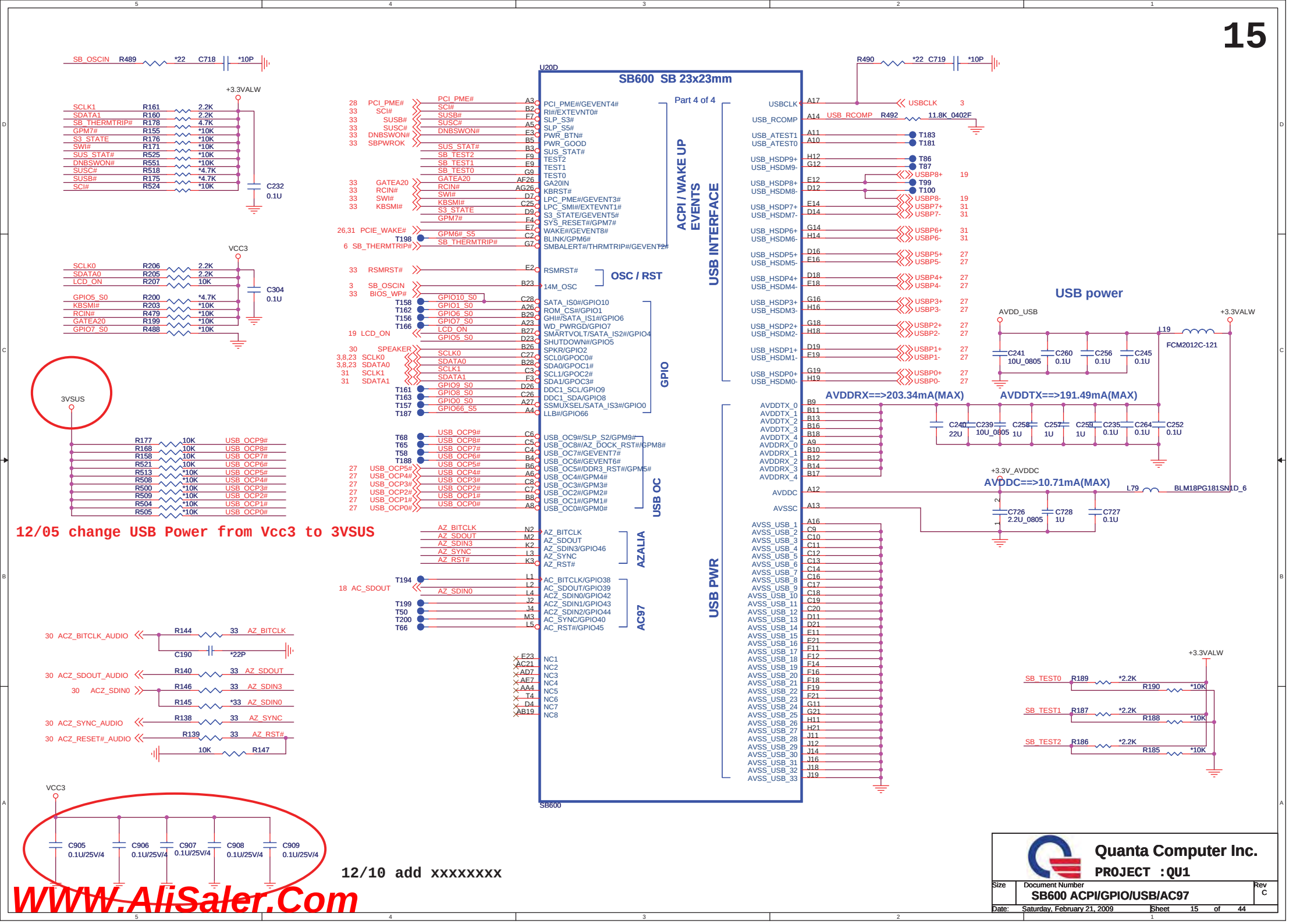
Date: Saturday, February 21, 2009 Sheet 12 of 44



Quanta Computer Inc.
PROJECT : QU1

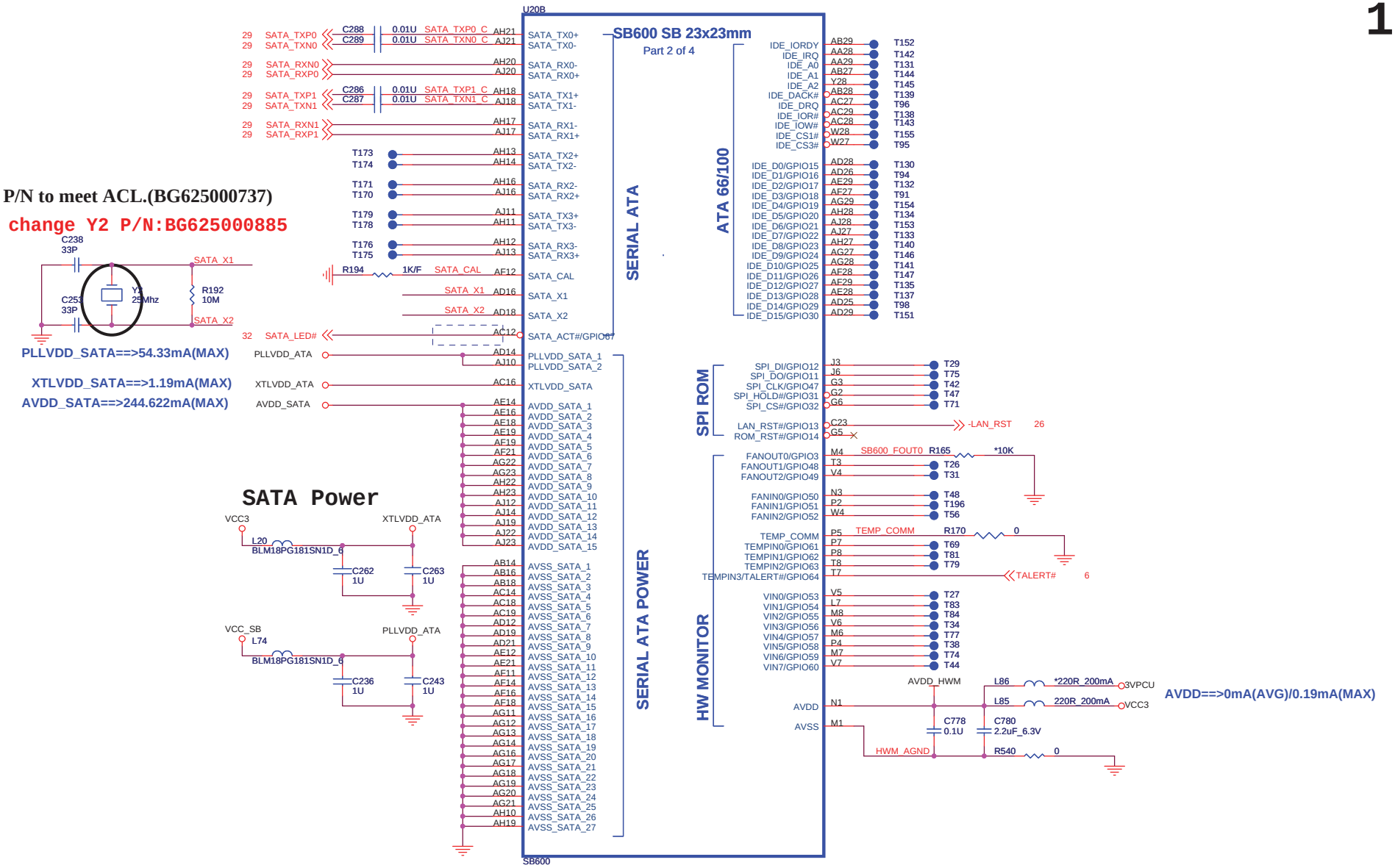
Size	Document Number	Rev
	RS690MC POWER	A
Date: Saturday, February 21, 2009	Sheet 13 of 44	


SB600 SB 23x23mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
LPC
CPU
RTC
XTAL
SB600
Stuff L81 in A-test
2A
PCIE Power
PCIE_PVDD==>27.92mA(MAX)
PCIE_VDDR==>391.01mA(MAX)
RTC
Modify 0915 for EMI
1-2 normal
2-3 clear CMOS
Reserved For EMI
12/11Modify
12/01 Change Y5 footprint like Y1 (XTAL-8_4X3_7-5_5X2_8)
WWW.AliSaler.Com
Quanta Computer Inc.
PROJECT :QU1
SB600 PCIE/PCI/CPU/LPC
Rev C
Date: Saturday, February 21, 2009
Sheet 14 of 44


SB600 SB 23x23mm
U20D
Part 4 of 4
SB600
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
USB power
AVDDRX==>203.34mA(MAX)
AVDDTX==>191.49mA(MAX)
AVDDC==>10.71mA(MAX)
12/05 change USB Power from Vcc3 to 3VSUS
12/10 add xxxxxxxx
WWW.AliSaler.Com
Quanta Computer Inc.
PROJECT : QU1
SB600 ACPI/GPIO/USB/AC97
Date: Saturday, February 21, 2009
Sheet 15 of 44

12/26 change Y2 P/N to meet ACL.(BG625000737)

12/02 change Y2 P/N:BG625000885



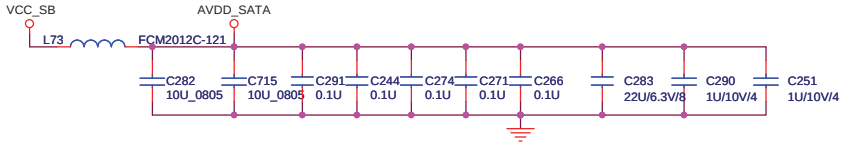
PLLVDD_SATA==>54.33mA(MAX)

XTLVDD_SATA==>1.19mA(MAX)

AVDD_SATA==>244.622mA(MAX)

AVDD==>0mA(AVG)/0.19mA(MAX)

SATA Power

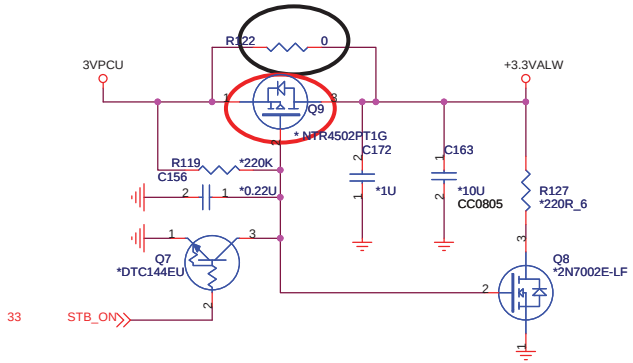


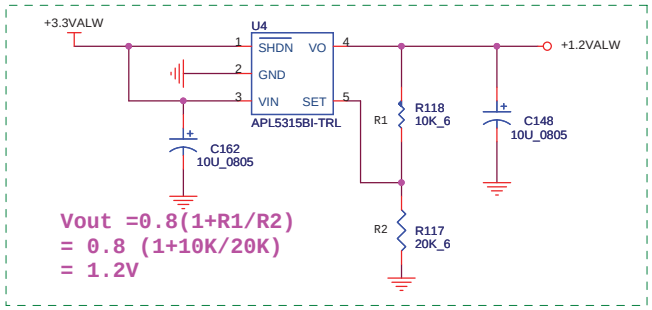
Quanta Computer Inc.

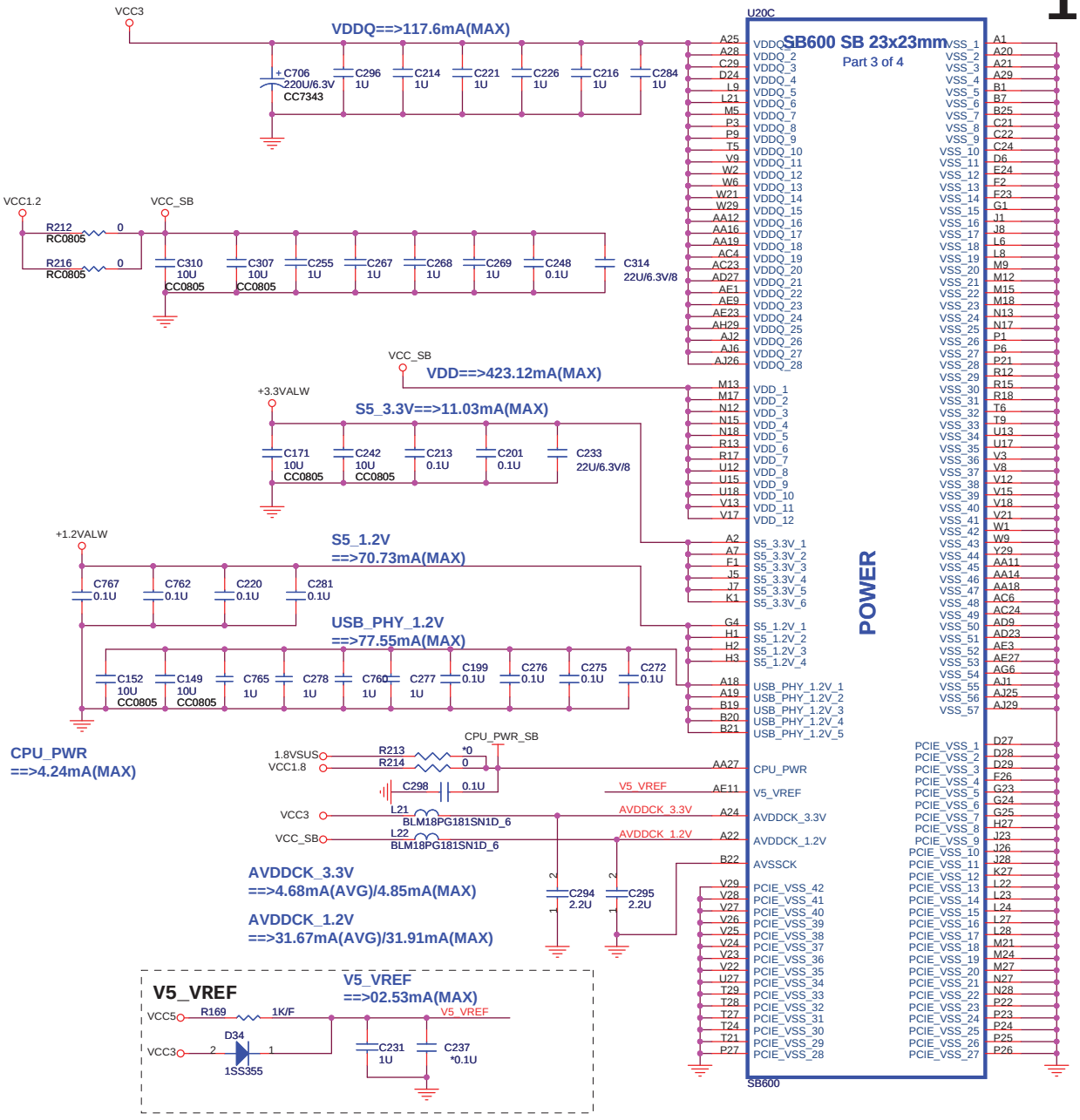
PROJECT : QU1

Size	Document Number	Rev
	SB600 HDD	C
Date: Saturday, February 21, 2009	Sheet 16 of 44	

12/21 ADD R122 for HW Lose





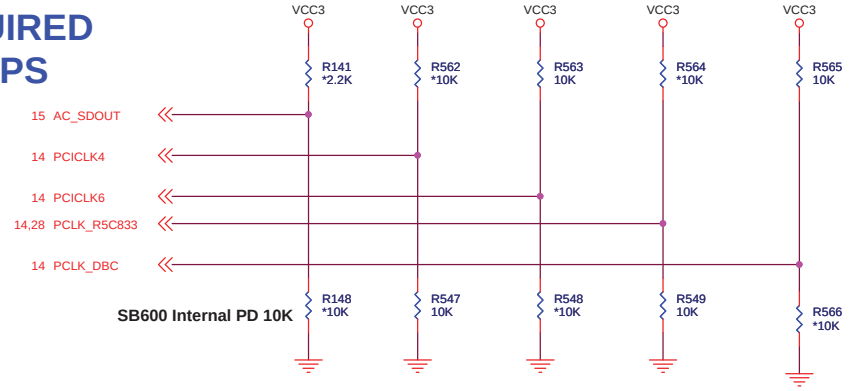


Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	SB600 POWER/DECOUPLING	C

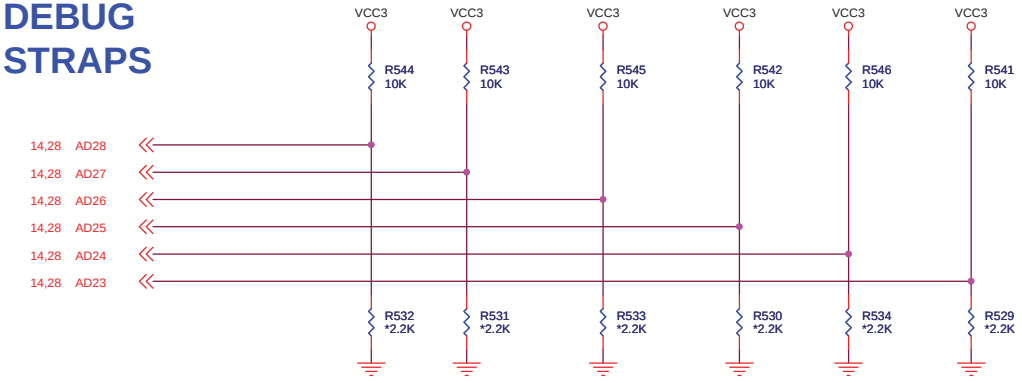
Date: Saturday, February 21, 2009 Sheet 17 of 44

REQUIRED STRAPS



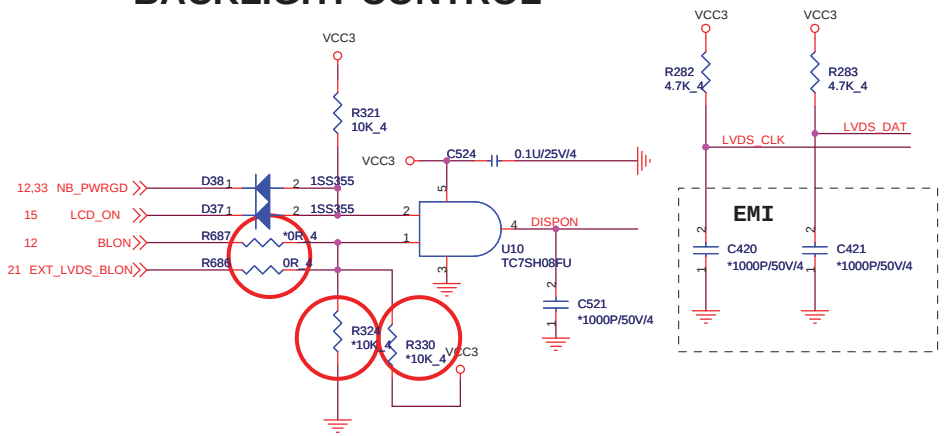
				PCLK_R5C843	PCLK_DBC
	AC_SDOUT	PCICLK4	PCICLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

BACKLIGHT CONTROL

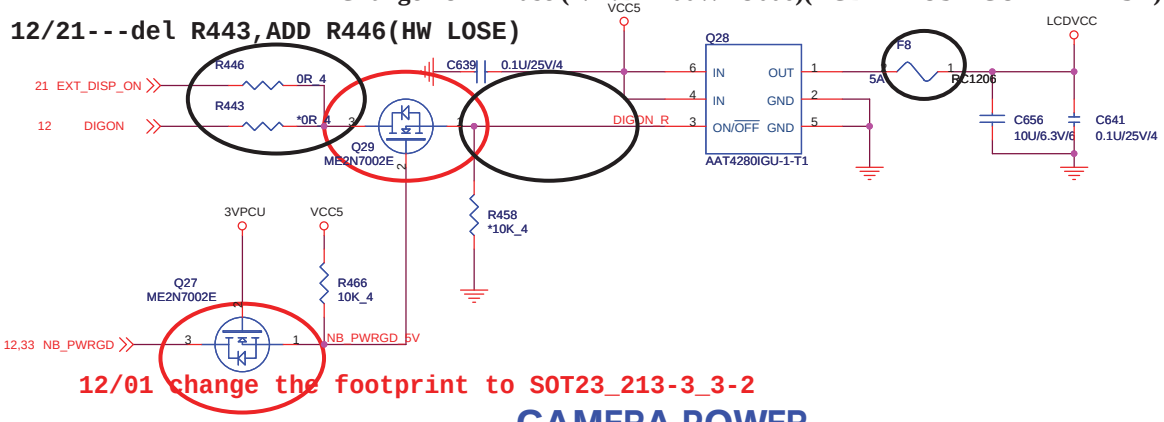


12/05---del R330,R324(white screen issue)
12/05---exchange D35,D36 to R686,R687(white screen issue)

PANEL VCC CONTROL

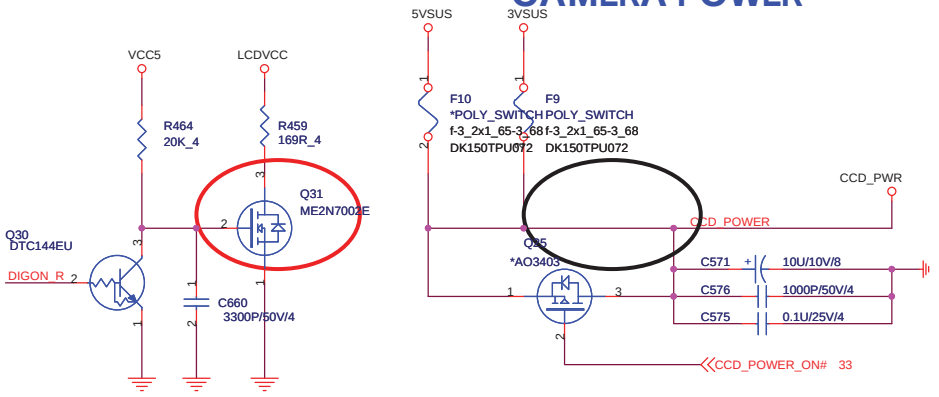
Change F8=7A fuse (P/N:DK700WFU006)(LCD INRUSH CURRENT=3A)

12/21---del R443,ADD R446(HW LOSE)



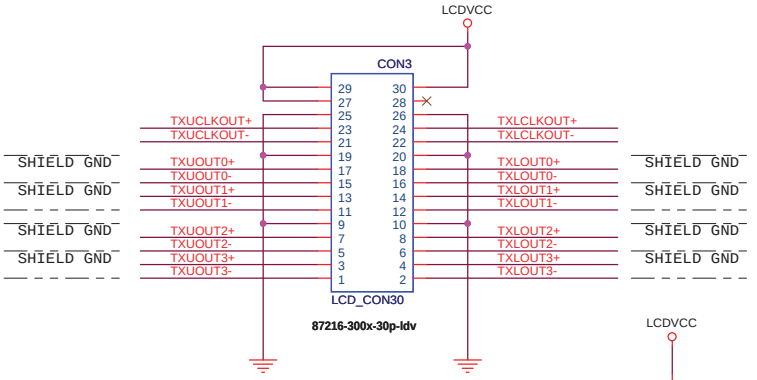
12/01 change the footprint to SOT23_213-3_3-2

CAMERA POWER

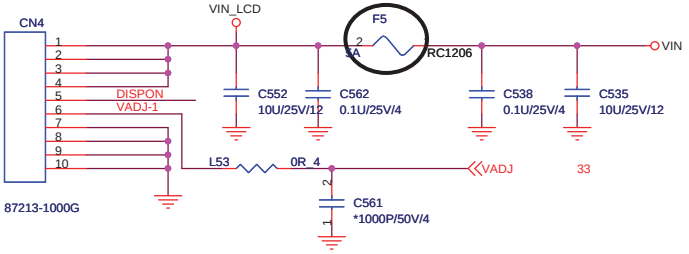


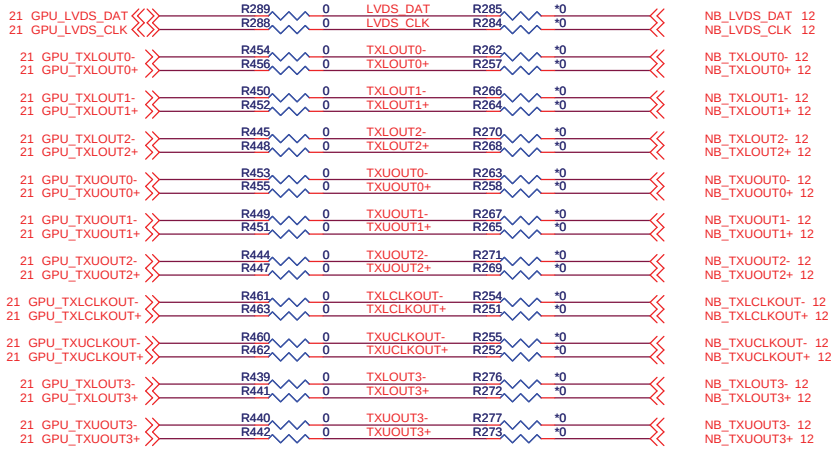
12/01 change the footprint to SOT23_213-3_3-2

LCD CONNECTOR



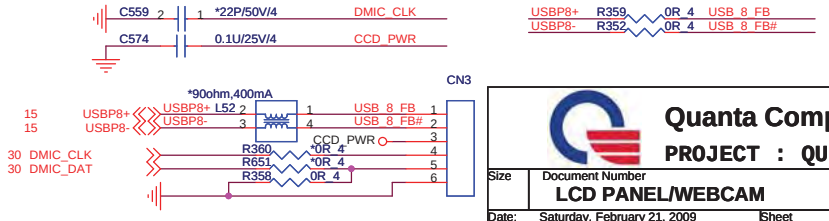
TO INVERTER POWER





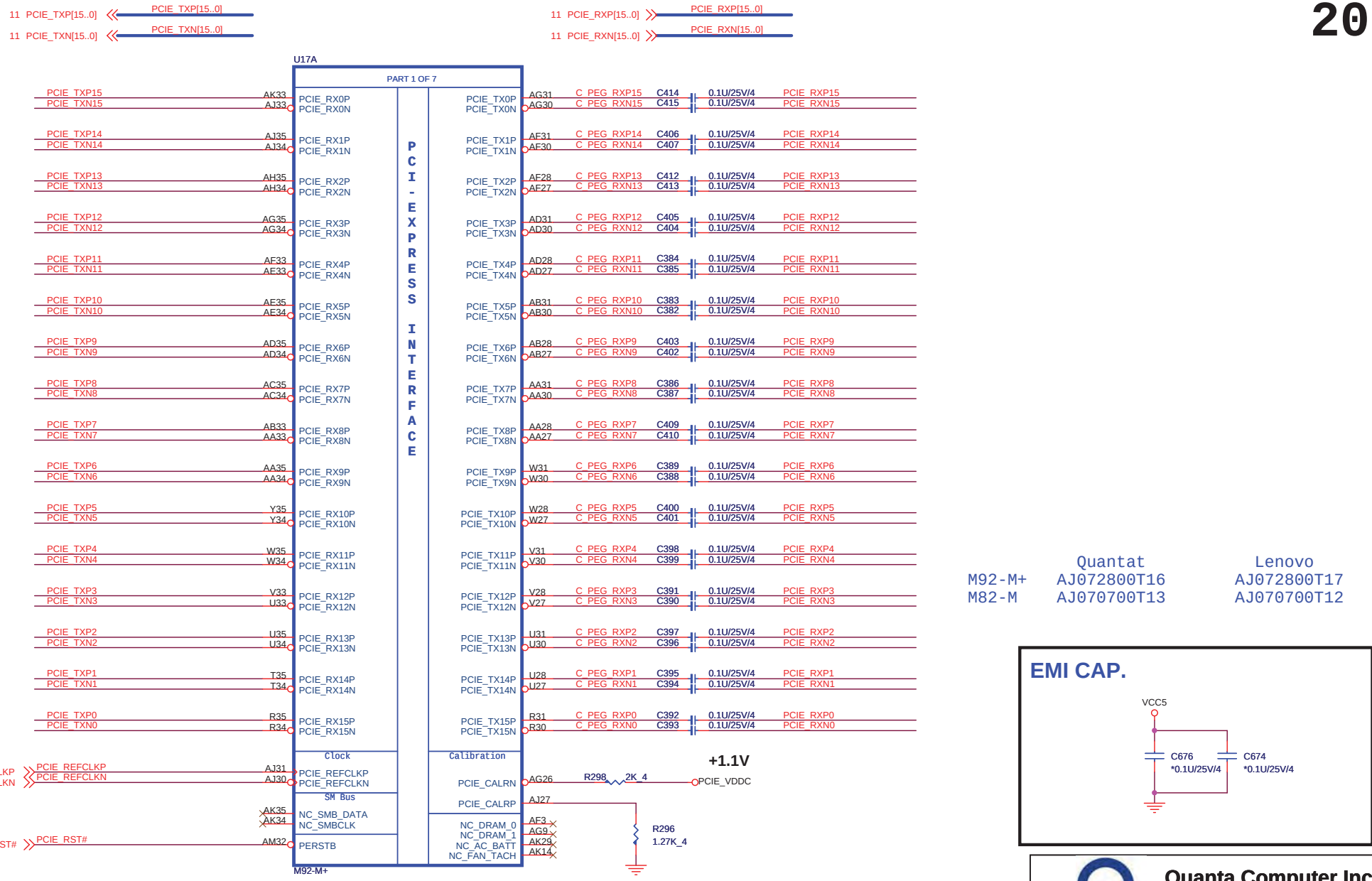
WEB CAM MODULE

FOR EMI



Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	LCD PANEL/WEBCAM	A
Date: Saturday, February 21, 2009	Sheet 19 of 44	



	Quantat	Lenovo
M92-M+	AJ072800T16	AJ072800T17
M82-M	AJ070700T13	AJ070700T12

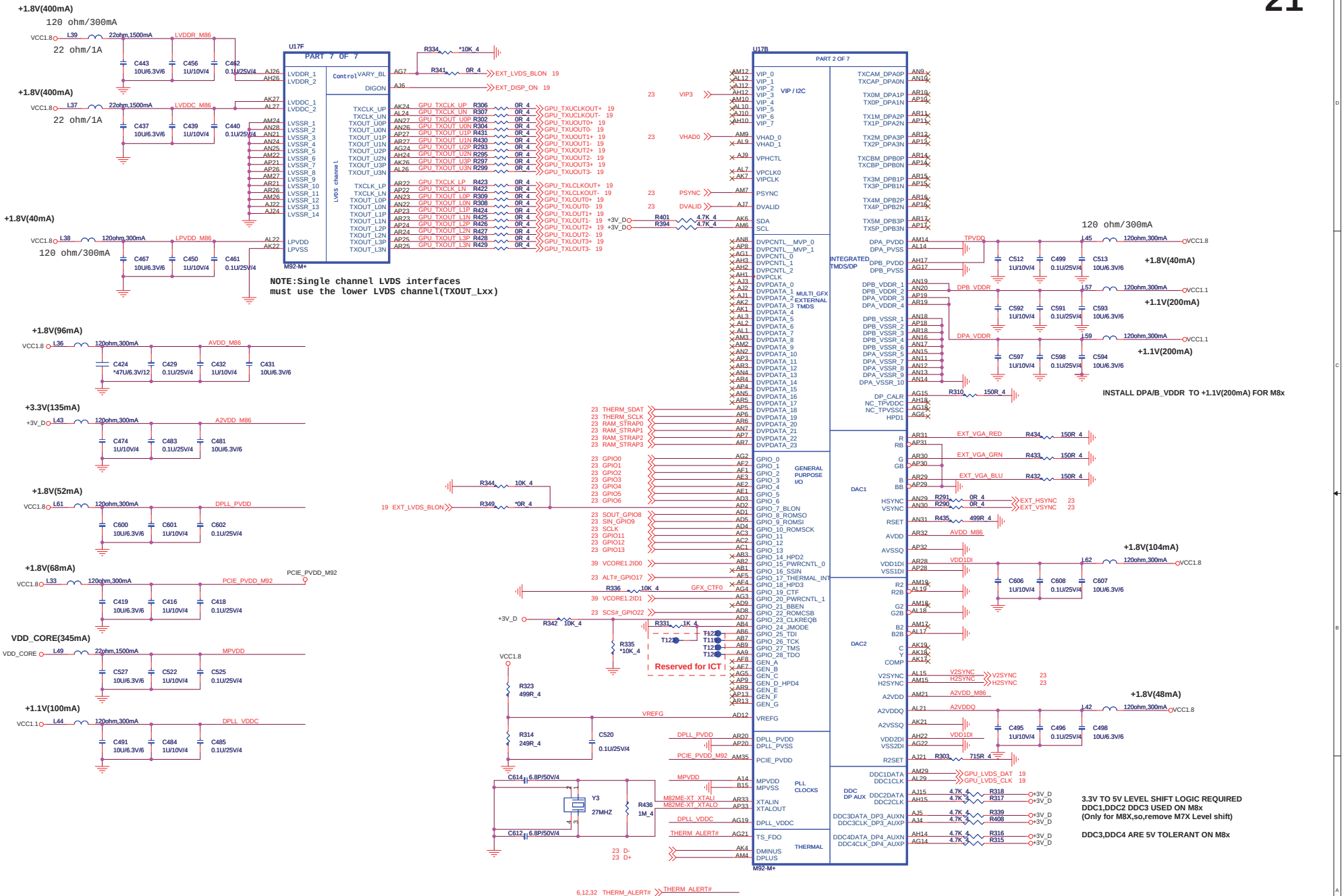
EMI CAP.

Quanta Computer Inc.

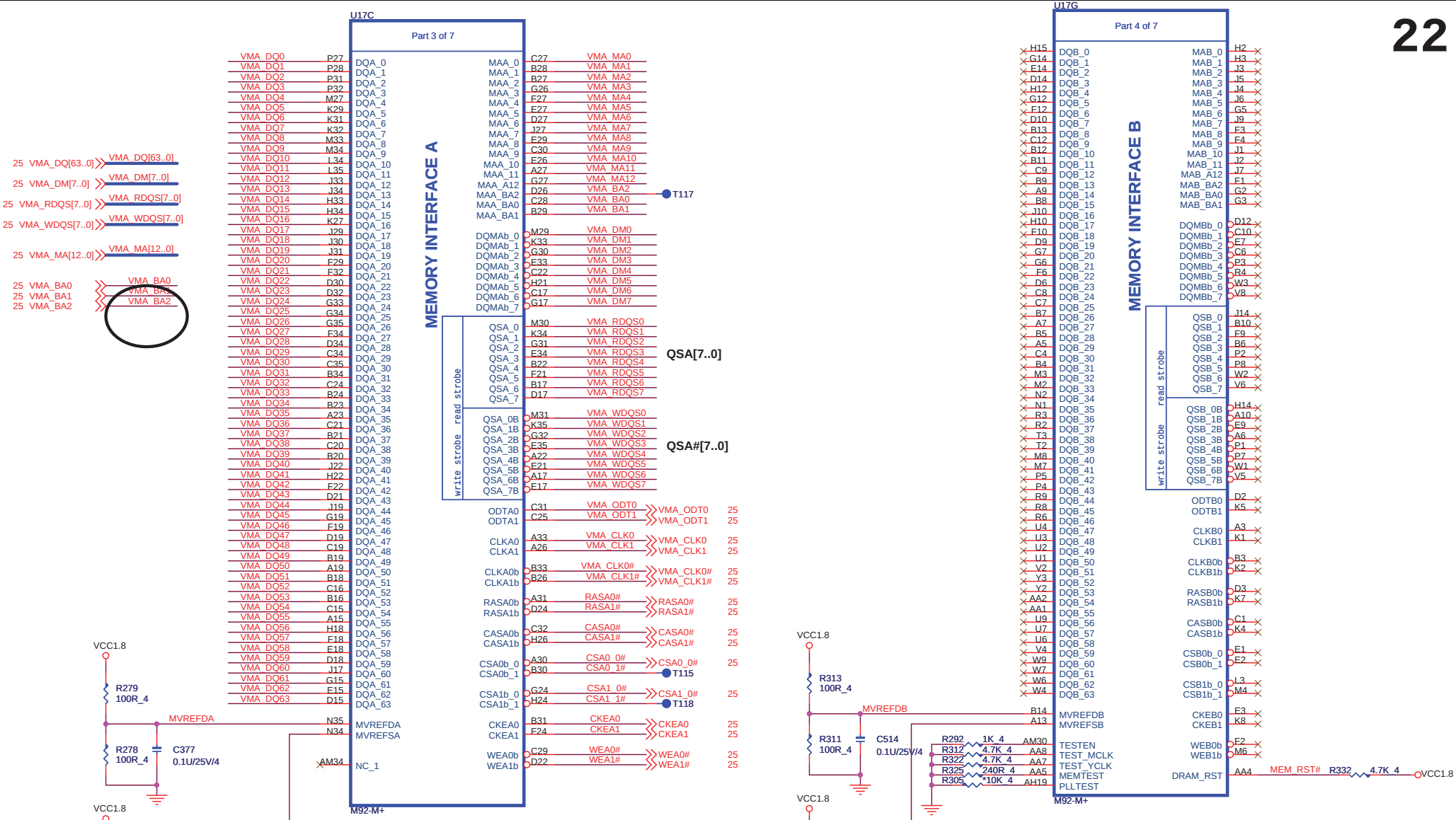
PROJECT : QU1

Size	Document Number	Rev
	M82-M PCI-E	A

Date: Saturday, February 21, 2009 Sheet 20 of 44



Quanta Computer Inc.		
PROJECT : QU1		
Size	Document Number: M82-M LVDS\RGB\TMDS	Rev: A
Date: Saturday, February 21, 2009	Sheet 21 of 44	



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

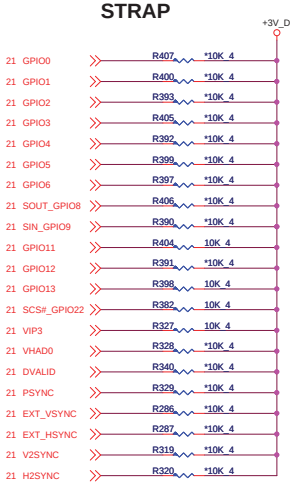
0.5*VDDQ 0.713*VDDQ

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	M82-M MEMORY I/F	A

Date: Saturday, February 21, 2009 Sheet 22 of 44

STRAP



CONFIGURATION STRAPS

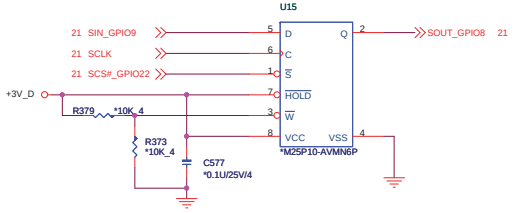
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7x/M8x-M)	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82-S)	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA_DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

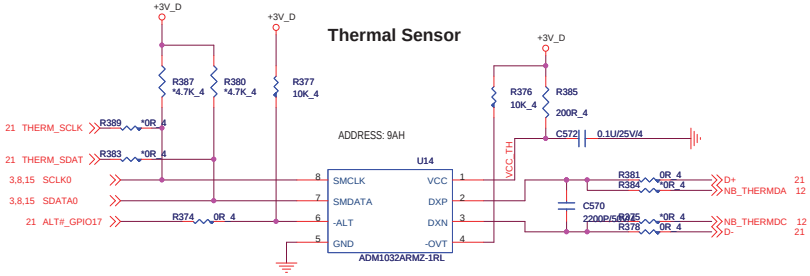
HDCP FUNCTION

W#	HDCP
0	**Enable**
1	Disable

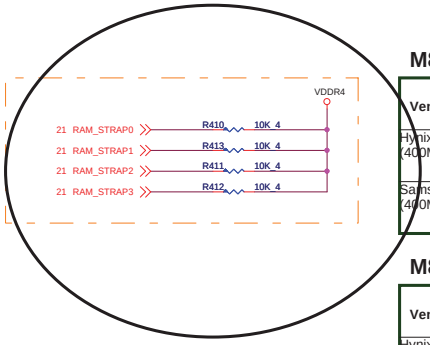
EEPROM



Thermal Sensor



Need to pull-high +3VPCU in M/B side(ALT#_GPIO17,SYSFANON#)



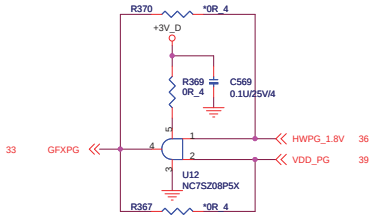
M86 DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Hynix (400MHZ)	**256M**	**1**	**1**	**1**	**1**
Samsung (400MHz)	**256M**	**1**	**1**	**1**	**0**

M82 DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Hynix (500MHZ)	**512M**	**1**	**1**	**0**	**1**
Samsung (500MHz)	**512M**	**1**	**0**	**1**	**1**

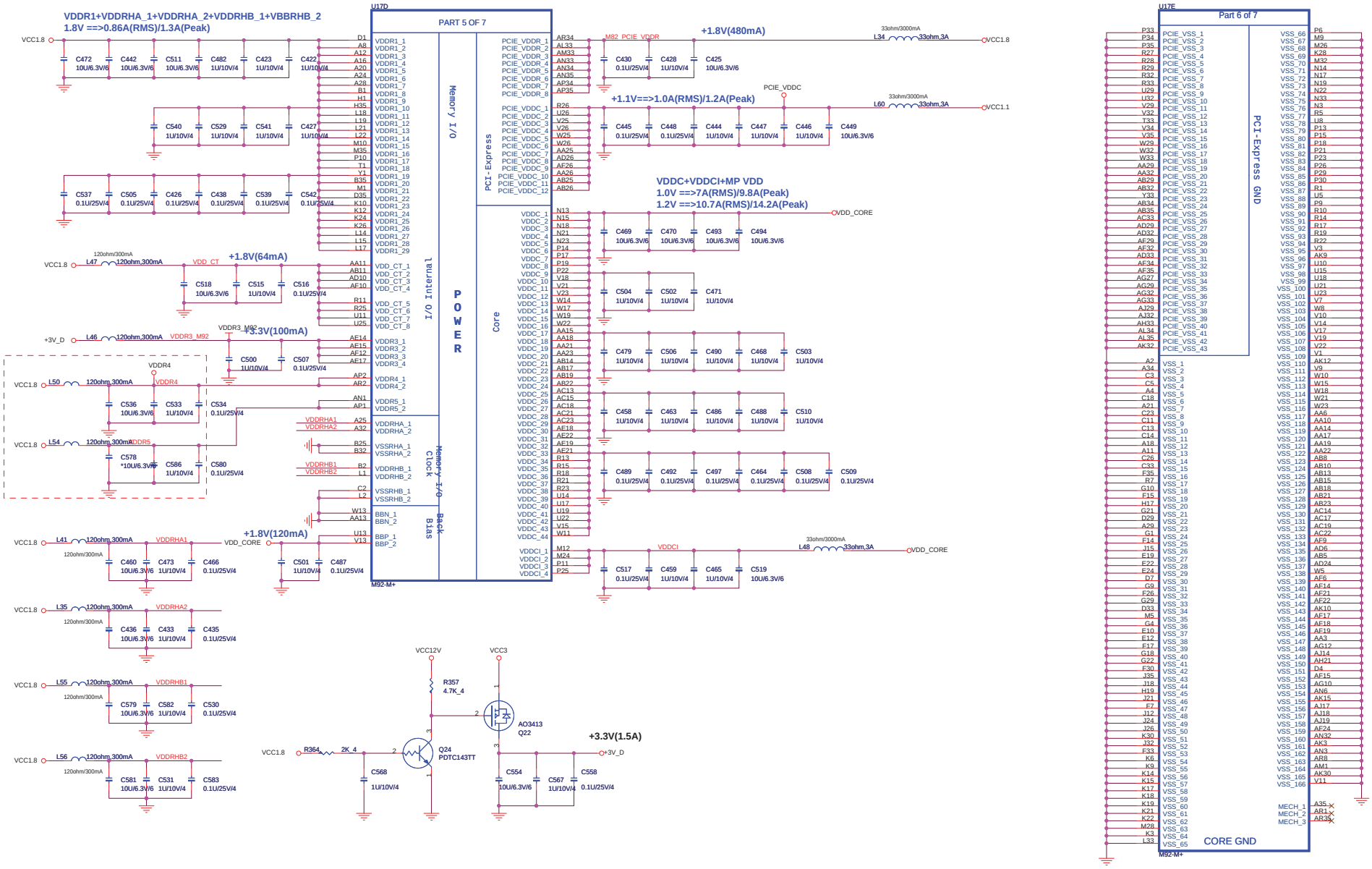
Fine-tune Power-on sequence



Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	M82-M Thermal\Strap\EEPROM	A

Date: Saturday, February 21, 2009 Sheet 23 of 44

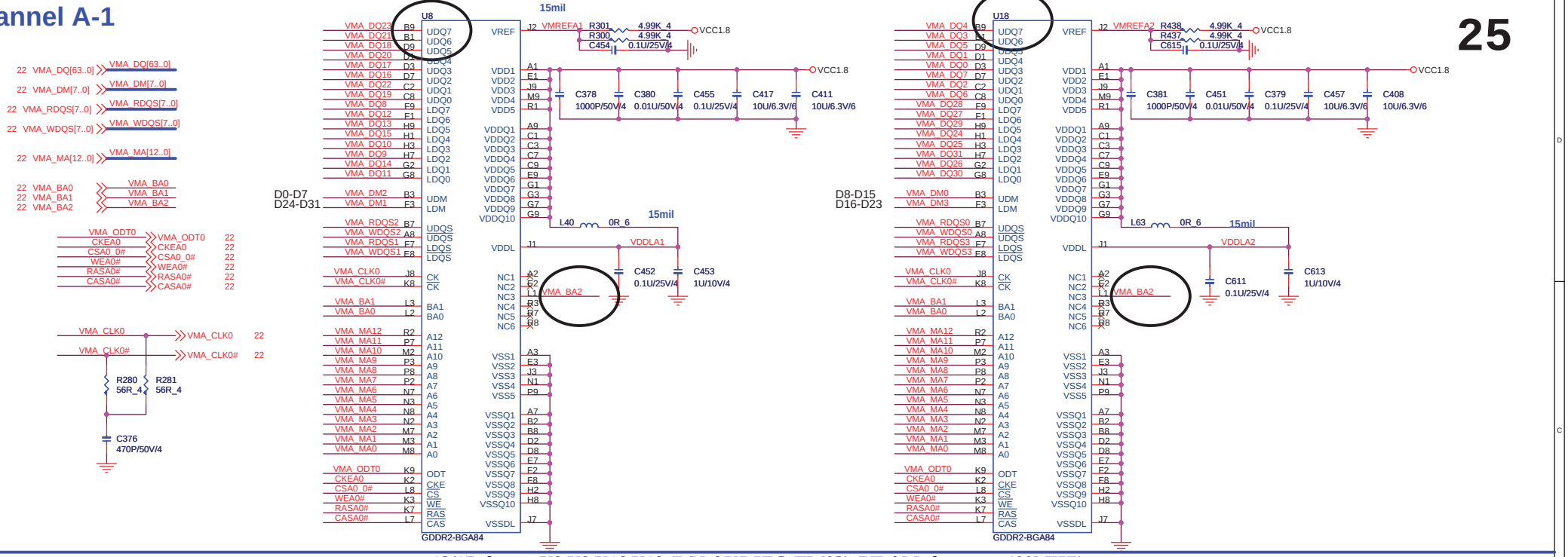


Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	M82-M Power and GND	A

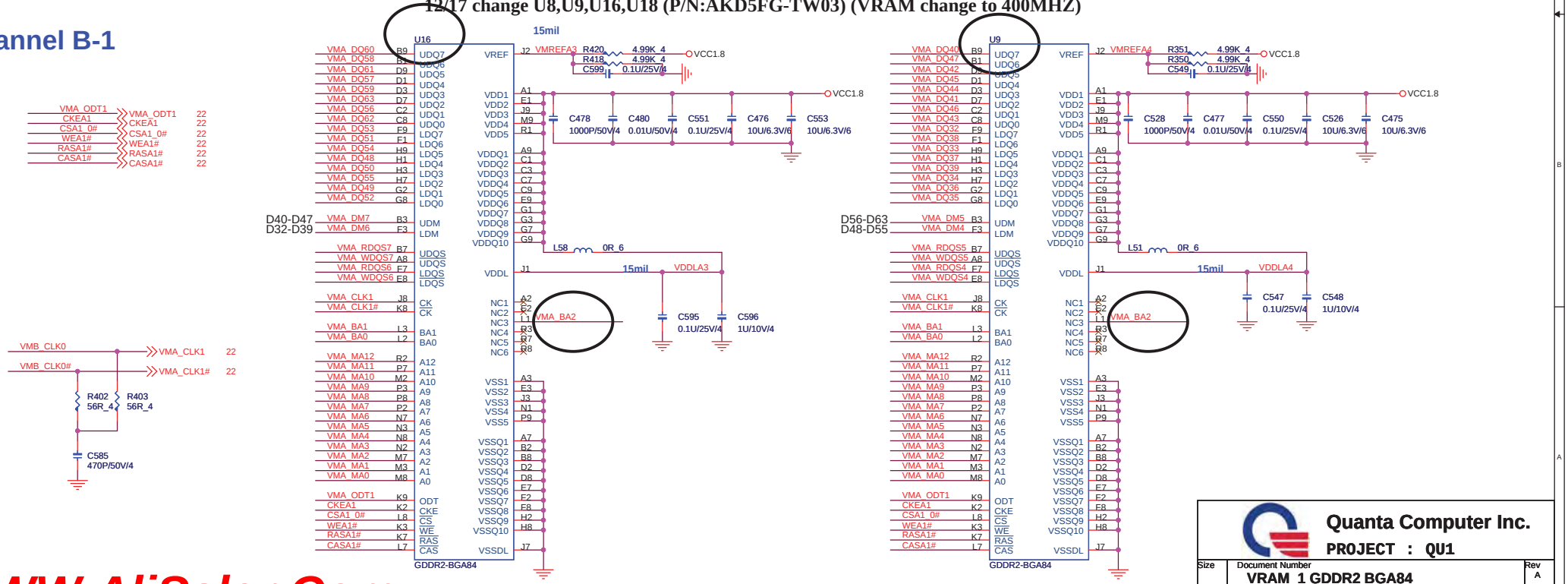
Date: Saturday, February 21, 2009 Sheet 24 of 44

Channel A-1



12/17 change U8,U9,U16,U18 (P/N:AKD5FG-TW03) (VRAM change to 400MHZ)

Channel B-1



Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	VRAM_1 GDDR2 BGA84	A

Date: Saturday, February 21, 2009 Sheet 25 of 44

VDDC+AVDLL+GPHY_PLLVDD+PCIE_VDD+PCIE_PLLVDD==>375mA

AVDD+VDDP+XTALVDD+BIASVDD==>90mA

VAUX_12 decoupling CAPs

BCM5906M
10mm X 10mm
68-Pin QFN

BCM5906MKMLG

Broadcom recommended cost down solution

EB1213-0027

EB1213-0028

EB1213-0029

LANVCC

LAN Power
15mils(331mA)
WIDE TRACE

10/100 Transformer

RJ45

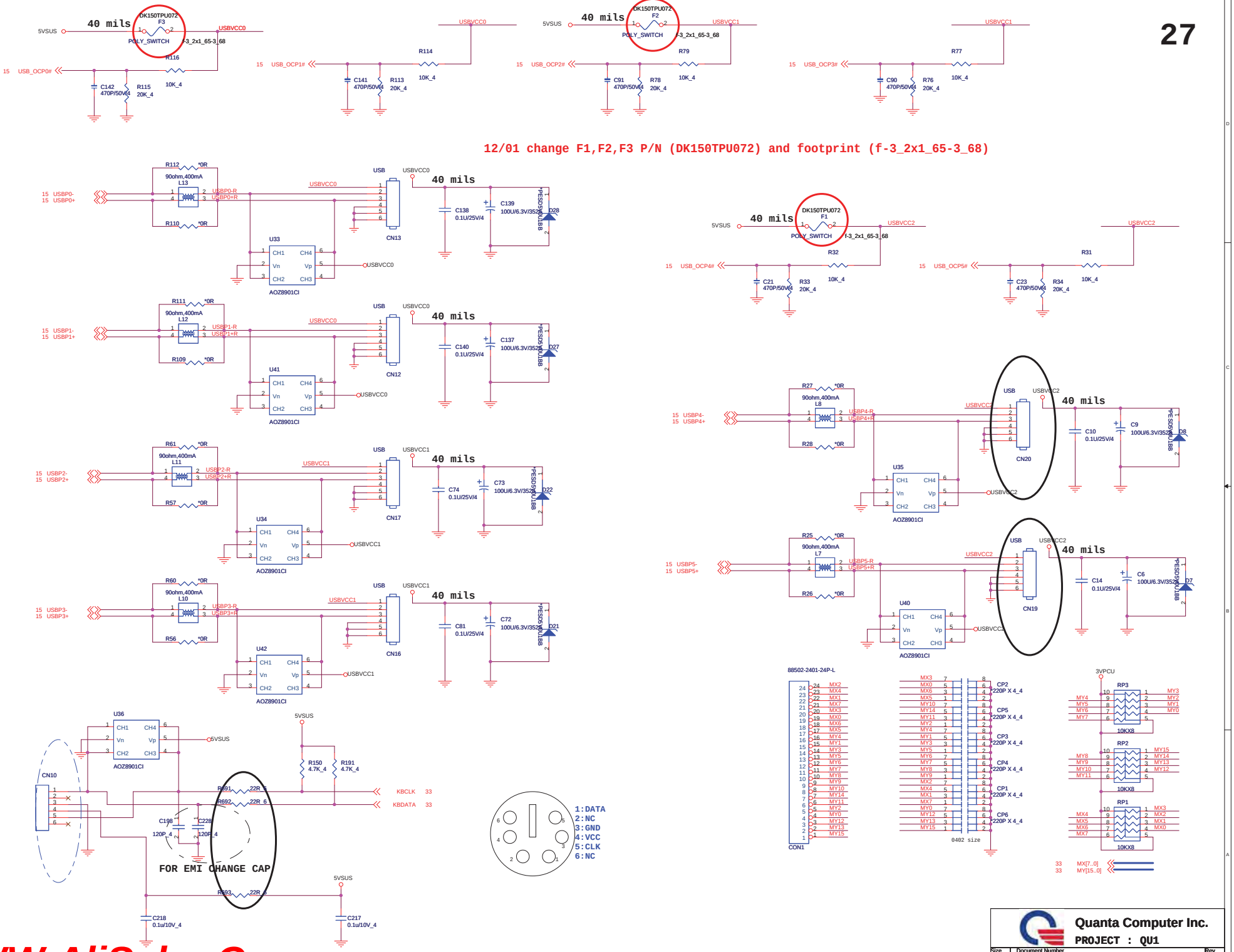
12/23 del R587(LAN link issue)
EB1213-0030
12/05 Layout update the CN11 Footprint
12/29 P26---change CN11 (P/N:DFTJ12FS001)(Change LED color)

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	LAN_BCM5906	A

Date: Saturday, February 21, 2009 Sheet 26 of 44

12/01 change F1,F2,F3 P/N (DK150TPU072) and footprint (f-3_2x1_65-3_68)



Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	USB Port	A

Date: Saturday, February 21, 2009 Sheet 27 of 44

12/10 Change Q35 PN:BAM45020007

500mA

ES1

UDIO4=GND : MMC Controller Disable
R600 => N/A

Shield to GND

R5C837-->INTE# Pin115
R5C833-->INTF# Pin116

Note:

	SD/MMC	MS	XD
	SD_CD#		XD-CD#
MDIO00			
MDIO01		MS_INS	
MDIO02			
MDIO03	SD_WP#		
MDIO04	SD_PWR0		
MDIO05	SD_PWR1		
MDIO06	SD_LED#		
MDIO07	SD_EXTCK		
MDIO08	SD_CMD	MS_BS	
MDIO09	SD_CLK	MS_CLK	
MDIO10	SD_DAT0	MS_DAT0	XD_DAT0
MDIO11	SD_DAT1	MS_DAT1	XD_DAT1
MDIO12	SD_DAT2	MS_DAT2	XD_DAT2
MDIO13	SD_DAT3	MS_DAT3	XD_DAT3
MDIO14			XD_DAT4
MDIO15			XD_DAT5
MDIO16			XD_DAT6
MDIO17			XD_DAT7
MDIO18			XD_CLE
MDIO19			XD_ALE

CLOSED CHIP

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

R5C837-->Pin94,pin95,pin101,pin100 NC
R5C833-->Add 833 PLL could support 50Mhz SD

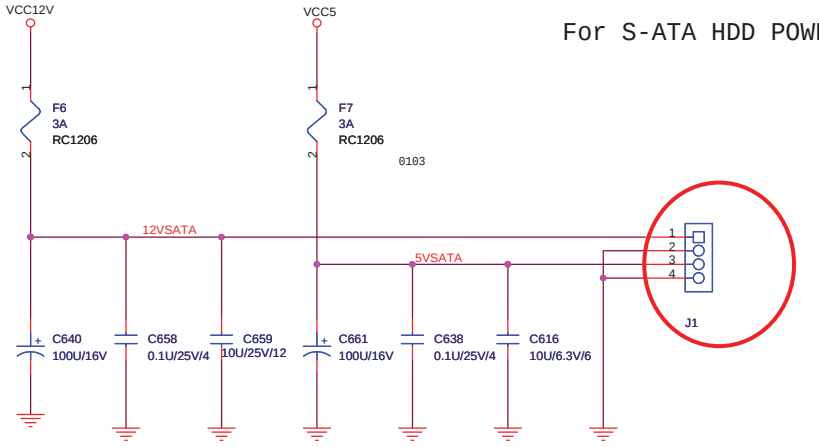
Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	R5C833 / 1394	A

Date: Saturday, February 21, 2009 Sheet 28 of 44

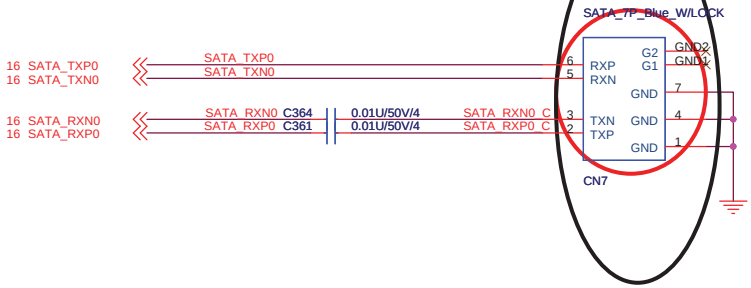
60 mils

For S-ATA HDD POWER

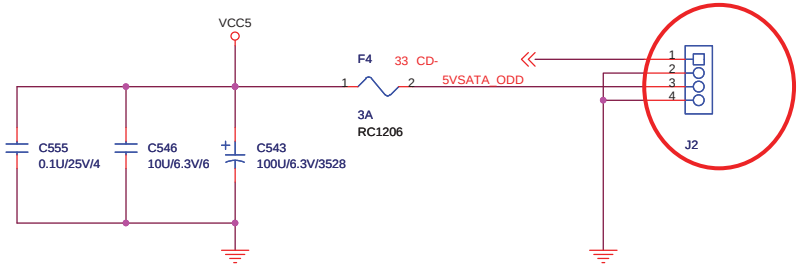


12/05 change CN6,CN7 Footprint sata-aba-sat-010-k07-7p-r

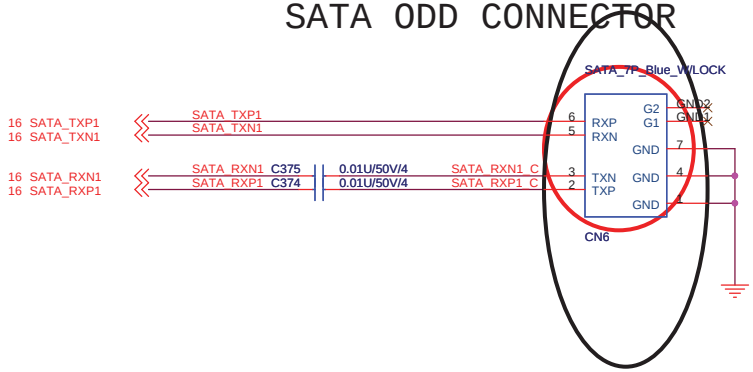
SATA HDD CONNECTOR



12/02 change J1,J2 PN:DFHS04FR207



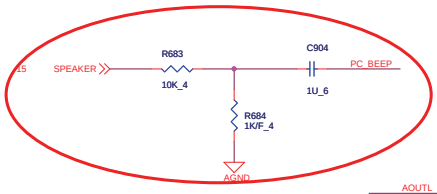
SATA ODD CONNECTOR

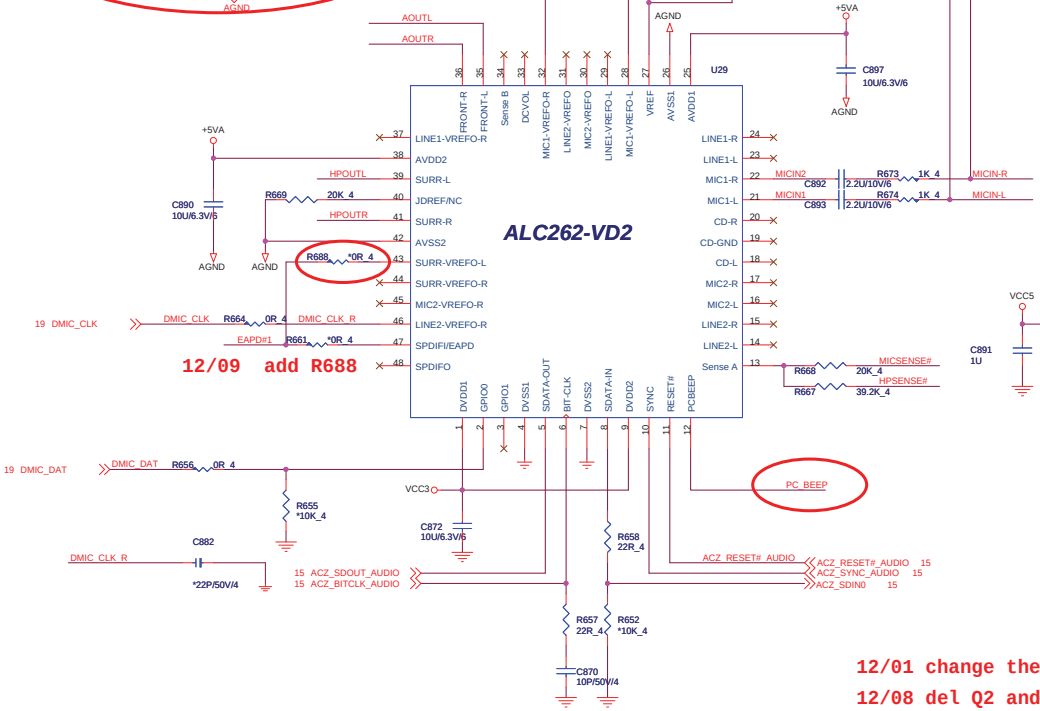


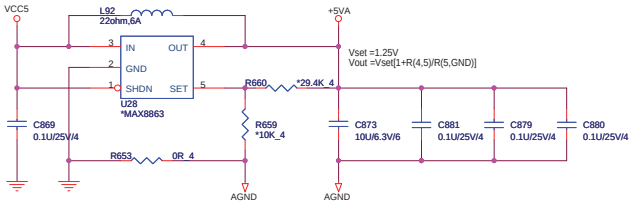
Quanta Computer Inc.
PROJECT : QU1

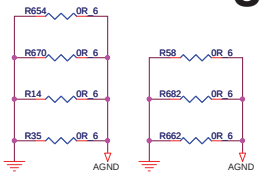
Size	Document Number	Rev
	SATA HDD/ODD	A
Date: Saturday, February 21, 2009	Sheet 29 of 44	

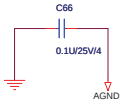
11/28 add Speaker function





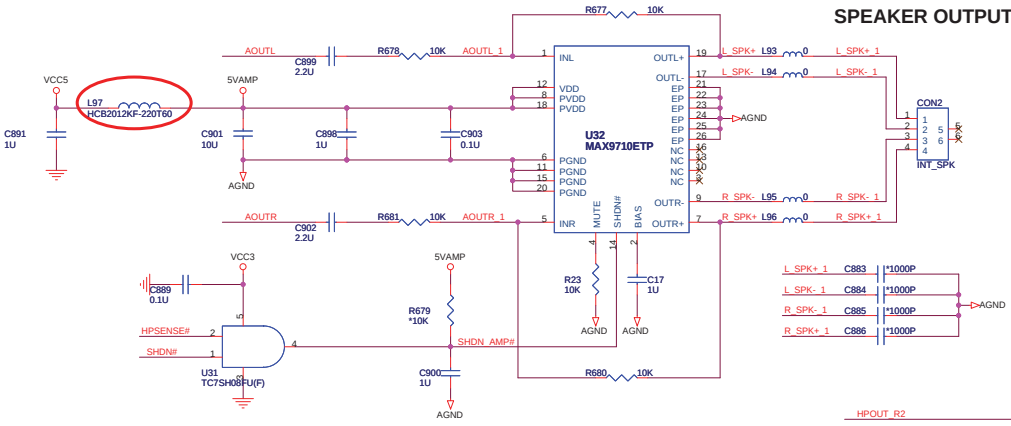






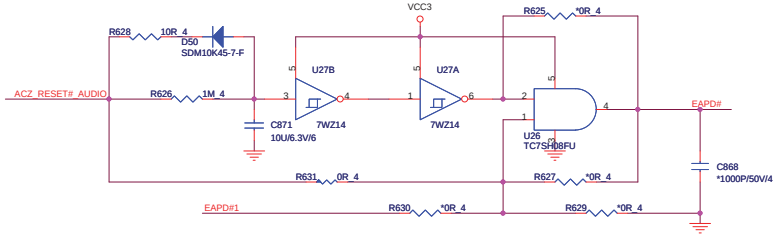
AUDIO AMPLIFIER

SPEAKER OUTPUT

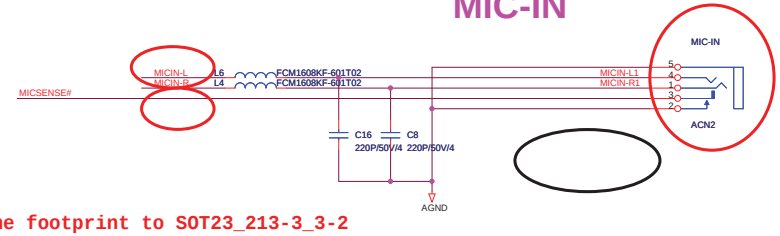


12/01 change the footprint to SOT23_213-3_3-2

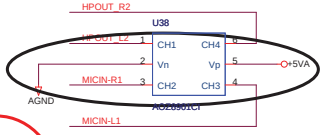
12/08 del Q2 and R16



MIC-IN



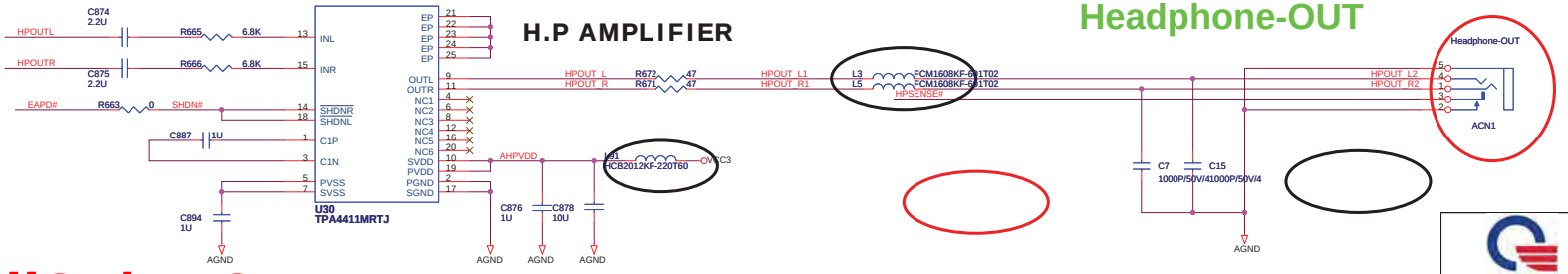
12/01 change the footprint to SOT23_213-3_3-2



12/08 Change ACN1,ACN2 P/N and Footprint

H.P AMPLIFIER

Headphone-OUT



12/08 del Q3 and R18

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	HD ALC262	A

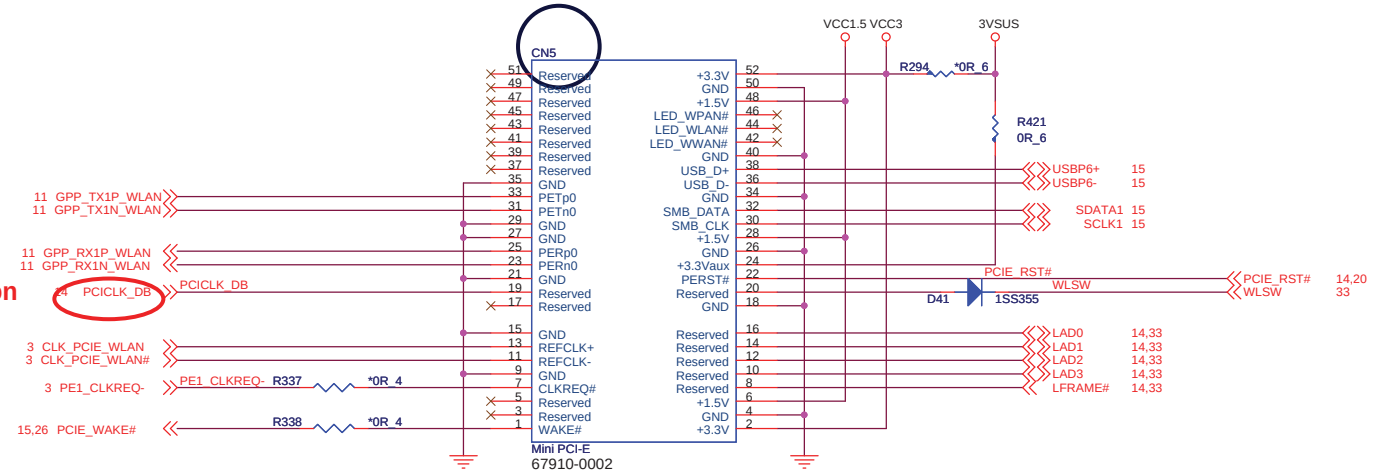
Date: Saturday, February 21, 2009 Sheet 30 of 44

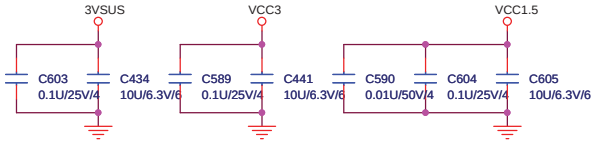
30

Mini Card (WLAN)

12/26 change CN5,CN8 P/N to meet ACL.(DFHD52MS057)

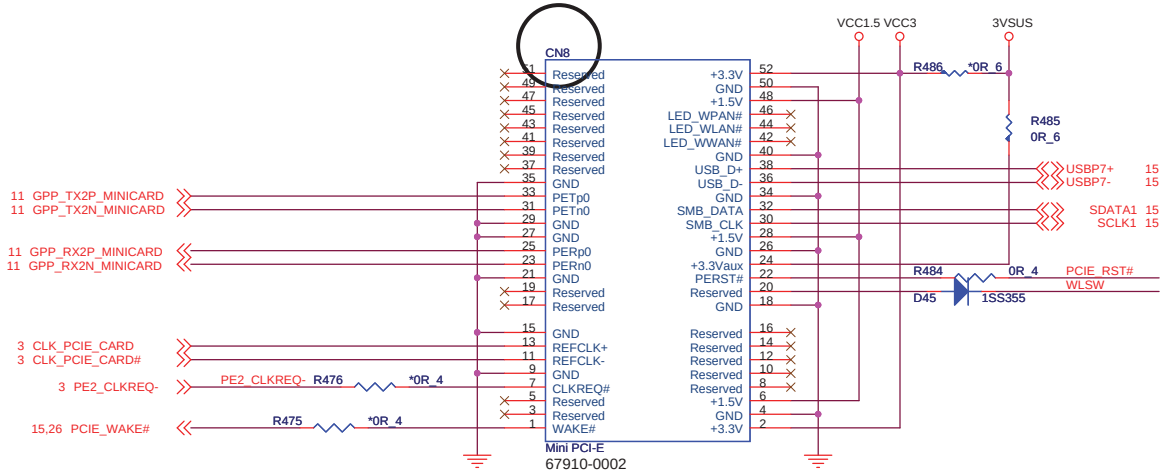
12/04 ADD debug port function

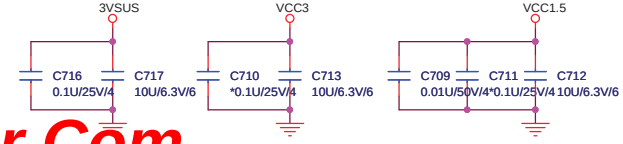




Mini Card (TV Card)

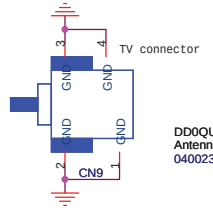
12/26 change CN5,CN8 P/N to meet ACL.(DFHD52MS057)





TV ANTENNA CONNECTOR

ANT. CONNECTOR



Z = 75 OHM

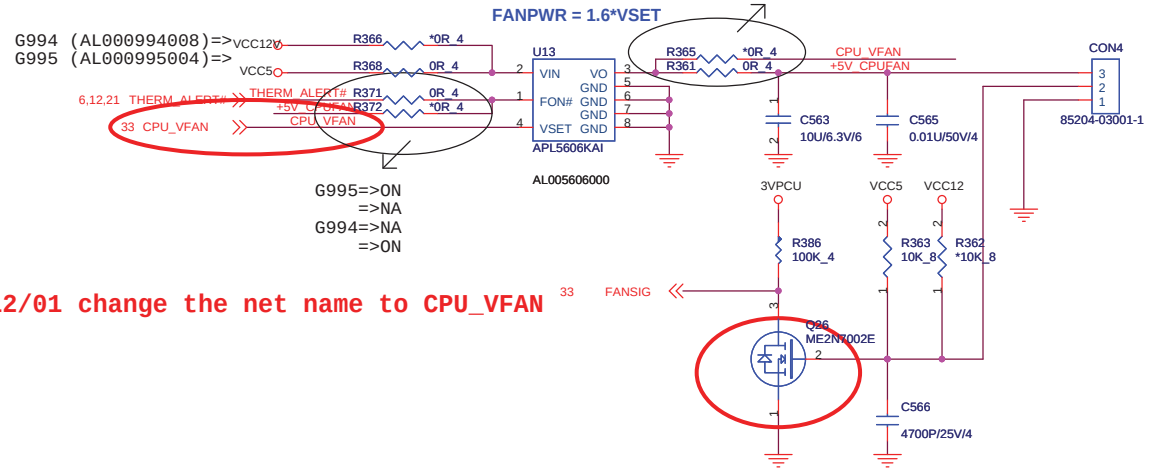
DD0QU1TH000
Antenna-040023fs001g105-4p-nb3
040023FS001G105NA

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	MINI CARD	A
Date: Saturday, February 21, 2009	Sheet 31 of 44	

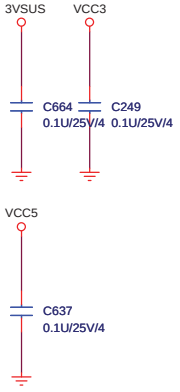
FAN CONN

G994=> ON
=> NA
G995=> NA
=> ON

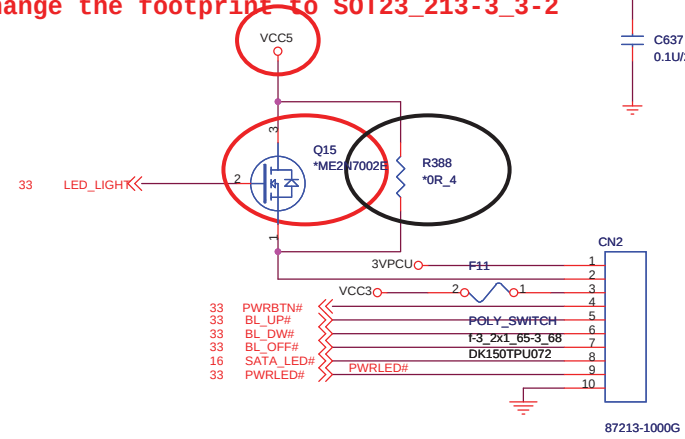


12/01 change the net name to CPU_VFAN

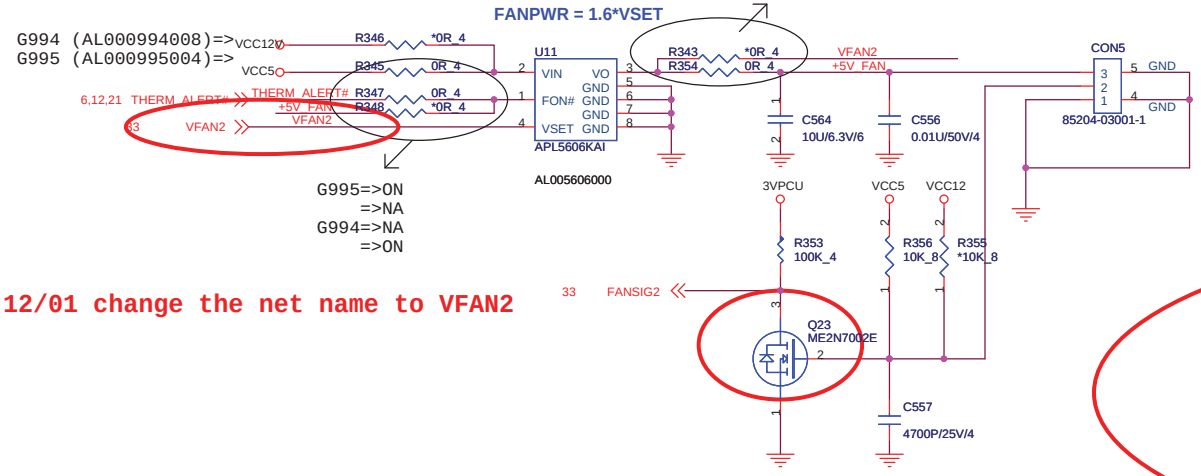
12/01 change the footprint to SOT23_213-3_3-2



12/01 DEL Q15(Lenovo Del the Light Bar function
12/01 change the power From VCC3 to VCC5
12/01 change the footprint to SOT23_213-3_3-2



G994=> ON
=> NA
G995=> NA
=> ON



12/01 change the net name to VFAN2

12/01 change the footprint to SOT23_213-3_3-2

12/01 del U1,Q1,Q3,R13,C11,R21,R11,R29

Quanta Computer Inc.		
PROJECT : QU1		
Size	Document Number: FAN\LED\Switch	Rev A
Date: Saturday, February 21, 2009	Sheet 32 of 44	

Layout Note:
Place all capacitors close to IT8512.

(For PLL Power)

3VPCU_EC 3VPCU

C20 0.1U/25V/4 C3 0.1U/25V/4 C22 0.1U/25V/4 C18 0.1U/25V/4 C56 0.1U/25V/4 C19 0.1U/25V/4

L2 120ohm,300mA C1 1000P/50V/4 C2 0.1U/25V/4

L1 120ohm,300mA 3VPCU

L9 120ohm,300mA 3VPCU

C36 0.1U/25V/4

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

C65 *10P/50V/4 PCLK_EC R54 *22R_4

C60 0.1U/25V/4

VCC3 3VPCU_EC VCCRTC

R690 *0R_4

CD- 29
HWPG 38
SUSC# 15
NB_PWRGD 12,19
RSMRST# 15
VRON 37
SBPWROK 15
MAINON 14,35,36,38,39,40,41
SUSON 35,36
HWSPND# 28
STB_ON 17

MY16 MY17

SMBUS

MBCLK R24 10K_4
MBDATA R30 10K_4

Pull Up for Low Active Pin

HWPG R42 *10K_4
PWRBTN# R40 10K_4

BL_UP# R7 10K_4
BL_DW# R8 10K_4
BL_OFF# R9 10K_4
WLSW R51 *10K_4

3VPCU

MY16 R22 10K_4
MY17 R19 10K_4

VCC3 R43 10K_4

23 GFXPG D14 1SS355 HWPG

PWRBTN# HWPG SUSC#

C57 *39P/50V/4 C37 *39P/50V/4 C24 *39P/50V/4

14,31 LAD0 LAD1 LAD2 LAD3
14 LPC_RST#
14 PCLK_EC
14,31 LFRAME#
LPCRST#/WUI4/GPD2
LPCCLK
LFRAME#
LPCPD#/WUI6/GPE6

15 GATEA20
14,28 SERIRQ
15 KBSMI#
15 SCI#
PCURST#
15 RCIN#
D11 1SS355
D20 1SS355
D16 1SS355
D19 1SS355

GA20/GPB5
SERIRQ
ECSMI#/GPD4
ECSCI#/GPD3
WRST#
KBRST#/GPB6
PWUREQ#/GPC7

GPIO

SM BUS
SMCLK0/GPB3 MBCLK 6
SMDAT0/GPB4 MBDATA 6
SMCLK1/GPC1
SMDAT1/GPC2 CCD_POWER_ON# 19
SMCLK2/GPF6 DNBSWON# 15
SMDAT2/GPF7

PS/2
PS2CLK0/GPF0 KBCLK 27
PS2DAT0/GPF1 KBDATA 27
PS2CLK1/GPF2
PS2DAT1/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5

12/01 Add R52(CS00002JB38) for PWRLED function

Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.

8Mbit , SPI

12/04 change U3 PN:AKE3GZN0N00

IT8512

T4 GPC0/CRX GPB2/CTX CIR

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

PWM
PWM0/GPA0 R52 0R_4 VADJ 19
PWM1/GPA1 PWRLED# 32
PWM2/GPA2 LED_LIGHT 32
PWM3/GPA3
PWM4/GPA4 D15 1SS355 WLSW 31
PWM5/GPA5 SWI# 15
PWM6/GPA6
PWM7/GPA7

TACH0/GPD6 FANSIG 32
TACH1/GPD7 FANSIG2 32
TMR0/WUI2/GPC4
TMR1/WUI3/GPC6

WAKE UP
PWRSW/GPE4 PWRBTN# PWRBTN# 32
RI1#/WUI0/GPD0 SUSB# 15
RI2#/WUI1/GPD1 ACIN 35
WUI5/GPE5
RING#/PWRFAIL#/LPCRST#/GPB7 PCIEPWR_ON 14

UART
TXD/GPB1 UART_TXD T3
RXD/GPB0 UART_RXD T2

Please reserve this connector for serial debug port & KBS download usage.

A/D D/A
ADC0/GPI0 MID1
ADC1/GPI1 MID2
ADC2/GPI2 MID3
ADC3/GPI3
ADC4/GPI4
ADC5/GPI5 BL_UP# BL_UP# 32
ADC6/GPI6 BL_DW# BL_DW# 32
ADC7/GPI7 BL_OFF# BL_OFF# 32

12/08 del MID3(The netmname is unnecessary)

DAC0/GPJ0
DAC1/GPJ1 CPU_VFAN 32
DAC2/GPJ2 VFAN2 32
DAC3/GPJ3
DAC4/GPJ4
DAC5/GPJ5

CLOCK
CK32KE PMUX2
CK32K PMUX1

Y1 32.768KHZ C55 18P/50V/4 C64 18P/50V/4

IT8512 U2

3VPCU R53 470K_4 PCURST# C58 0.1U/25V/4

R20 10K_4 8512_SCK
R12 *100K_4 8512_SO 8512_SI 8512_SCE#

FLASH
FLRST#/WUI7/GPG0/TM
FLCLK/SCK
FLAD3/GPG6
FLAD2/SO
FLAD1/SI
FLAD0/SCE#
FLFRAME#/GPG2

KBMX
KSO0/PD0 MY0
KSO1/PD1 MY1
KSO2/PD2 MY2
KSO3/PD3 MY3
KSO4/PD4 MY4
KSO5/PD5 MY5
KSO6/PD6 MY6
KSO7/PD7 MY7
KSO8/ACK# MY8
KSO9/BUSY MY9
KSO10/PE MY10
KSO11/ERR# MY11
KSO12/SLCT MY12
KSO13 MY13
KSO14 MY14
KSO15 MY15

27 MY[15..0]
27 MX[7..0]

KSO0/ST8# KSO1/AFD# KSO2/INIT# KSO3/SLIN# KSI4 KSI5 KSI6 KSI7
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

VSS AVSS

R10 0R_4
C59 0.1U
R55 *0R_4
R62 0R_4

Model ID

3VPCU
R2 100K_4 R4 100K_4 R5 100K_4
MID1 R1 *0R_4
MID2 R3 *0R_4
MID3 R6 *0R_4

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

3VPCU
R95 10K_4
R59 10K_4
8512_SCE# 8512_SCK R17 47R_4 8512_SI R15 47R_4 8512_SO R90 15R_4
U3 CE# SCK SI SO WP# VDD HOLD# VSS
MX25L1605A
C63 0.1U/25V/4

VCC3 3VPCU
R89 10K_4 R94 10K_4
15 BIOS_WP#
Q6 DTC144EU
Q5 ME2N7002E

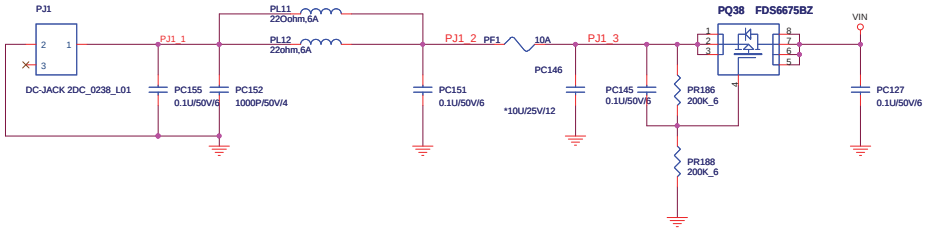
12/01 change the footprint to SOT23_213-3_3-2

Quanta Computer Inc.
PROJECT : QU1

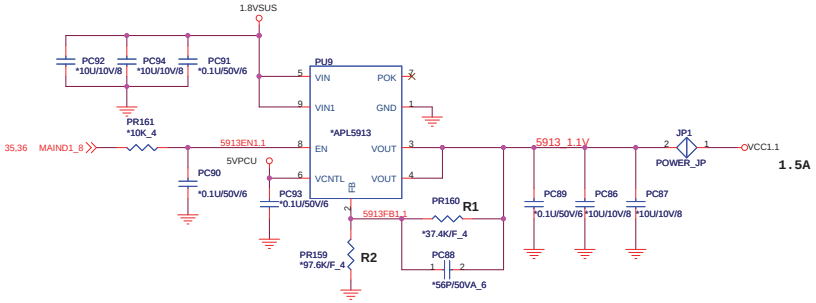
Size	Document Number	Rev
	EC ITE 8512	A

Date: Saturday, February 21, 2009 Sheet 33 of 44

ACIN

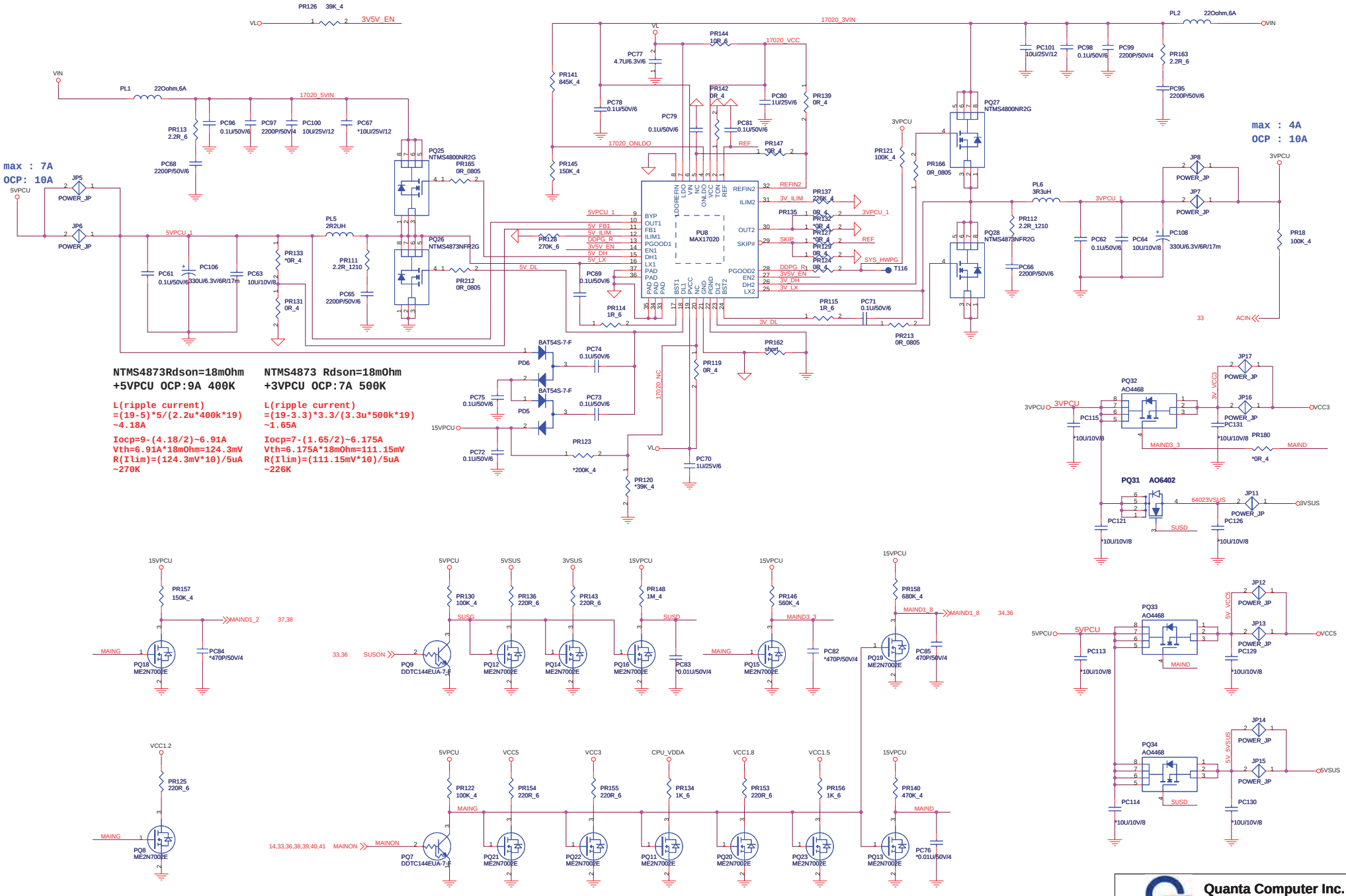


+1.1V

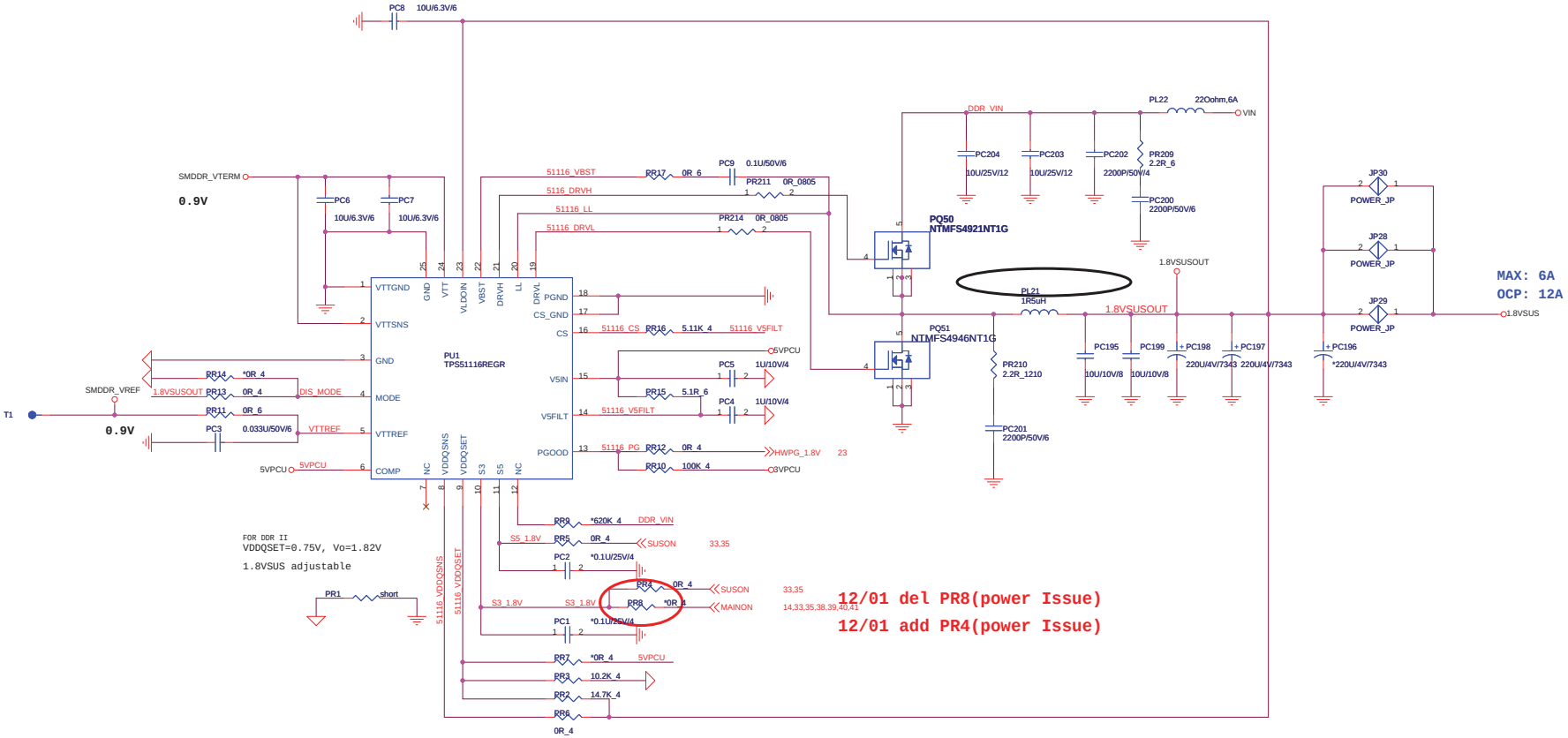


Vo=0.8(1+R1/R2)

Quanta Computer Inc.		
PROJECT : QU1		
Size	Document Number: FAN\LED\Switch	Rev: A
Date: Saturday, February 21, 2009	Sheet 34 of 44	

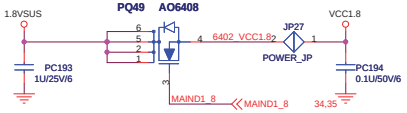


Quanta Computer Inc.		
PROJECT : QU1		
Size	Document Number: FAN\LED\Switch	Rev: A
Date: Saturday, February 21, 2009	Sheet 35 of 44	



NTMFS4946Rdson=3.8~4.6mOhm

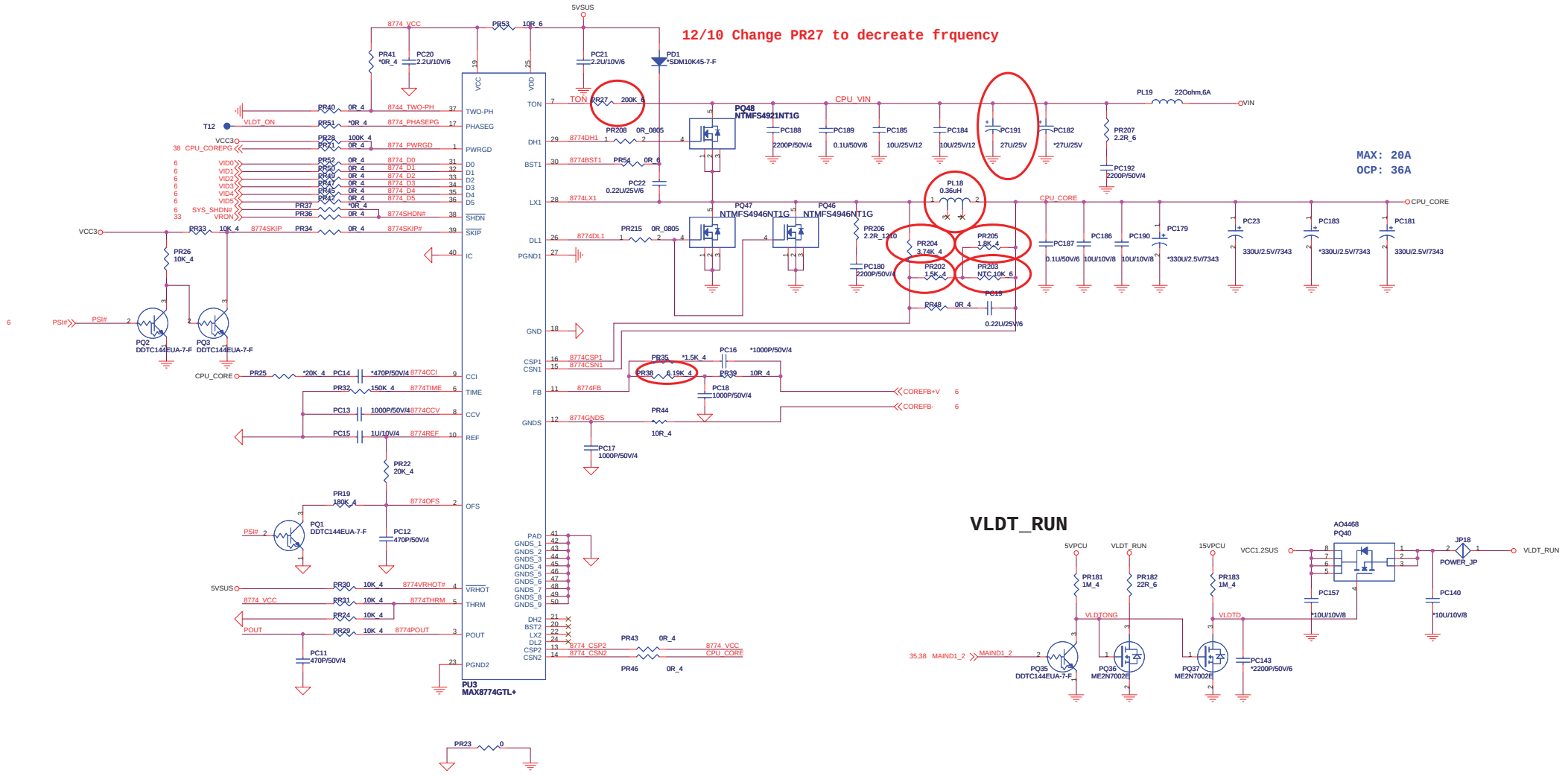
L(ripple current)
=(19-1.8)*1.8/(1.5u*400k*19)
~2.72A
4.6m*(12-(2.72/2))=RILIM*10uA
RILIM=5.11K
((10u*PR67)/Rdson)+(Delta_I/2)=Iocp



Quanta Computer Inc.
PROJECT : QU1

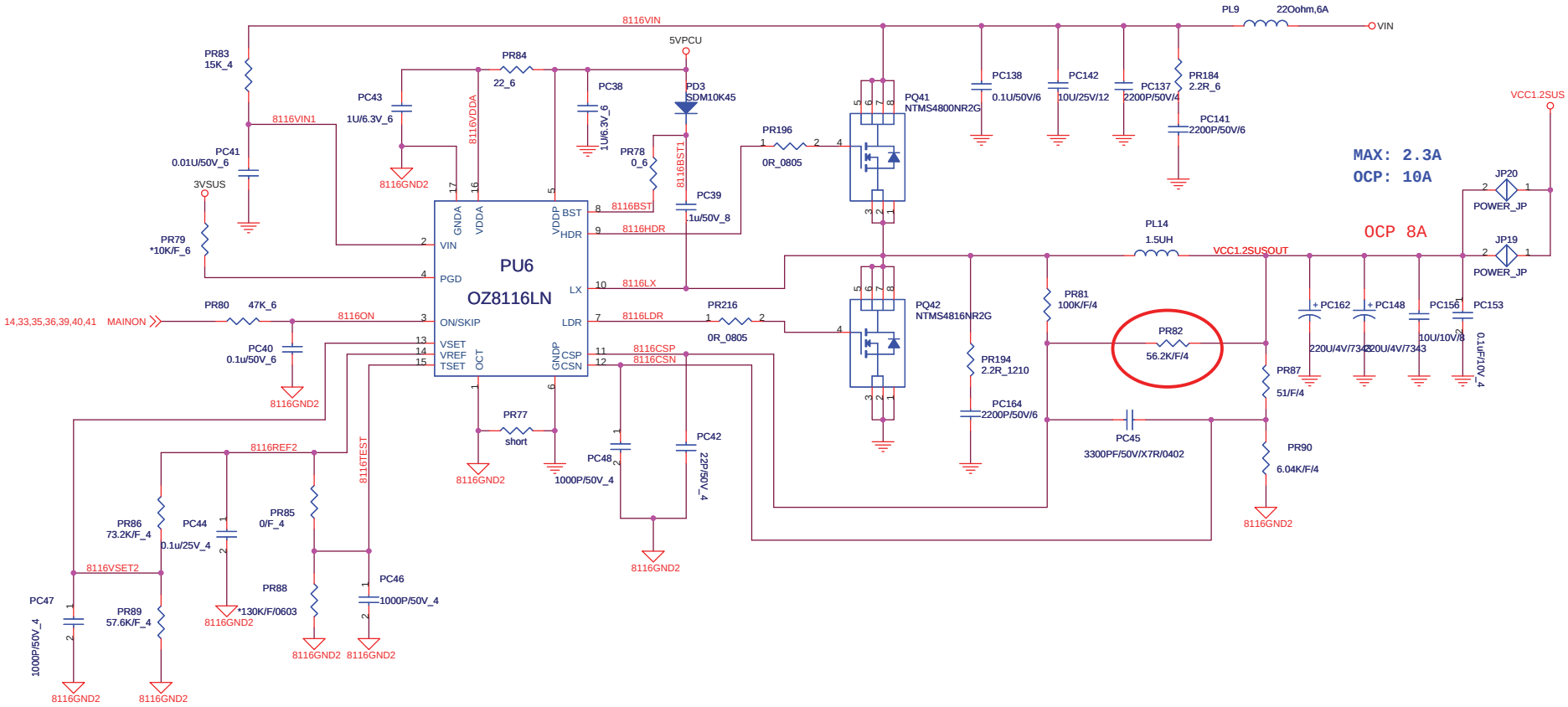
Size	Document Number	Rev
	FAN\LED\Switch	A

Date: Saturday, February 21, 2009 Sheet 36 of 44

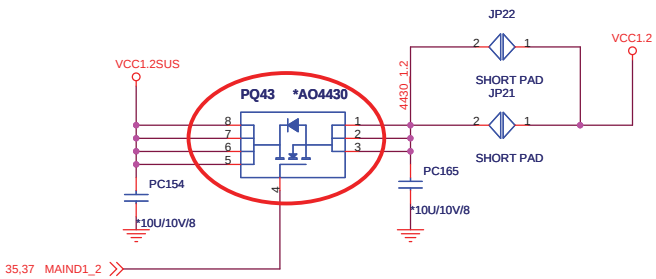


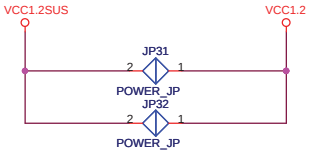
VLDT_RUN

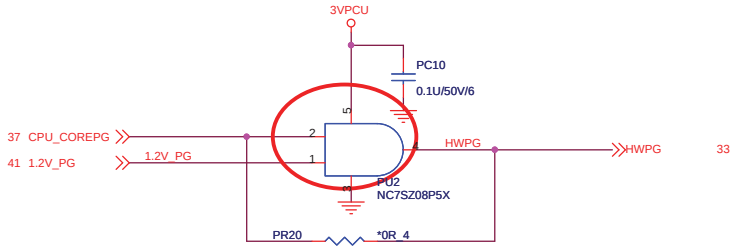
Quanta Computer Inc.		
PROJECT : QU1		
Size	Document Number: FAN\LED\Switch	Rev: A
Date: Saturday, February 21, 2009	Sheet 37 of 44	



12/01 del PQ43(Power Issue)





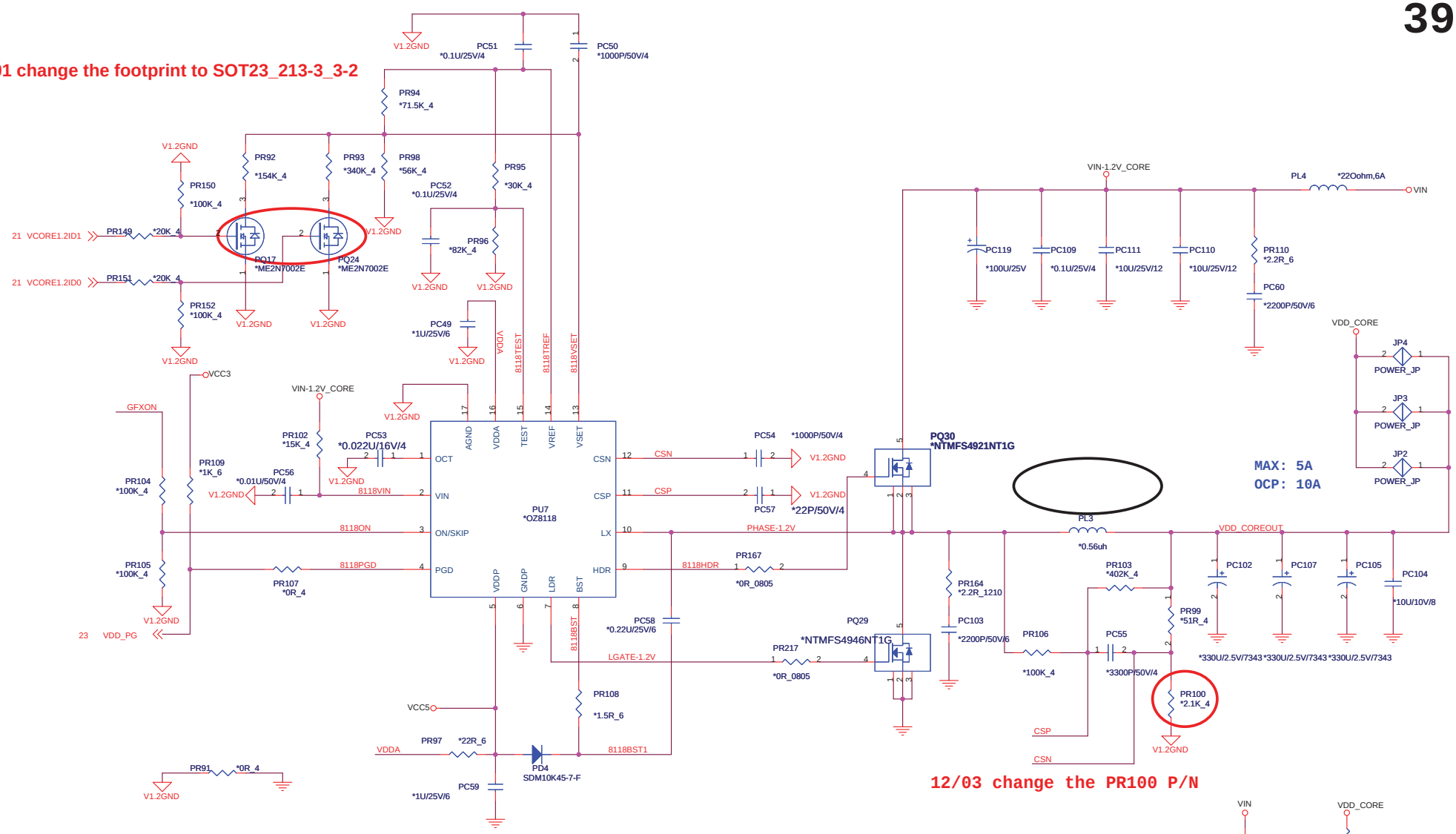


12/01 change PU2 p/n to AL17SZ08006(Buyer request)

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	FAN\LED\Switch	A
Date: Saturday, February 21, 2009	Sheet 38 of 44	

12/01 change the footprint to SOT23_213-3_3-2



12/03 change the PR100 P/N

M86 TABLE

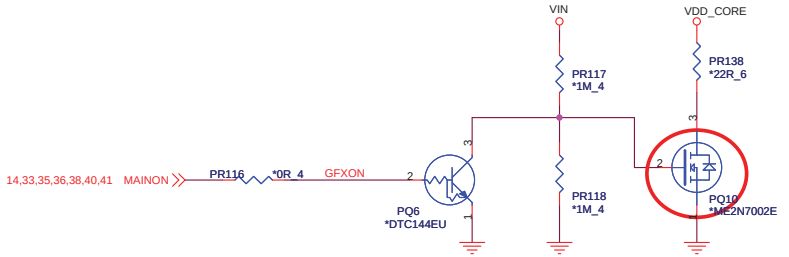
PR228: 82.5K
PR229: 226K
PR230: 374K

VID[1:0]		
VID1	VID0	
0	0	1.1V
0	1	1.0V
1	0	0.95V
1	1	0.9V

M92 TABLE

PR228: 71.5K
PR229: 154K
PR230: 340K

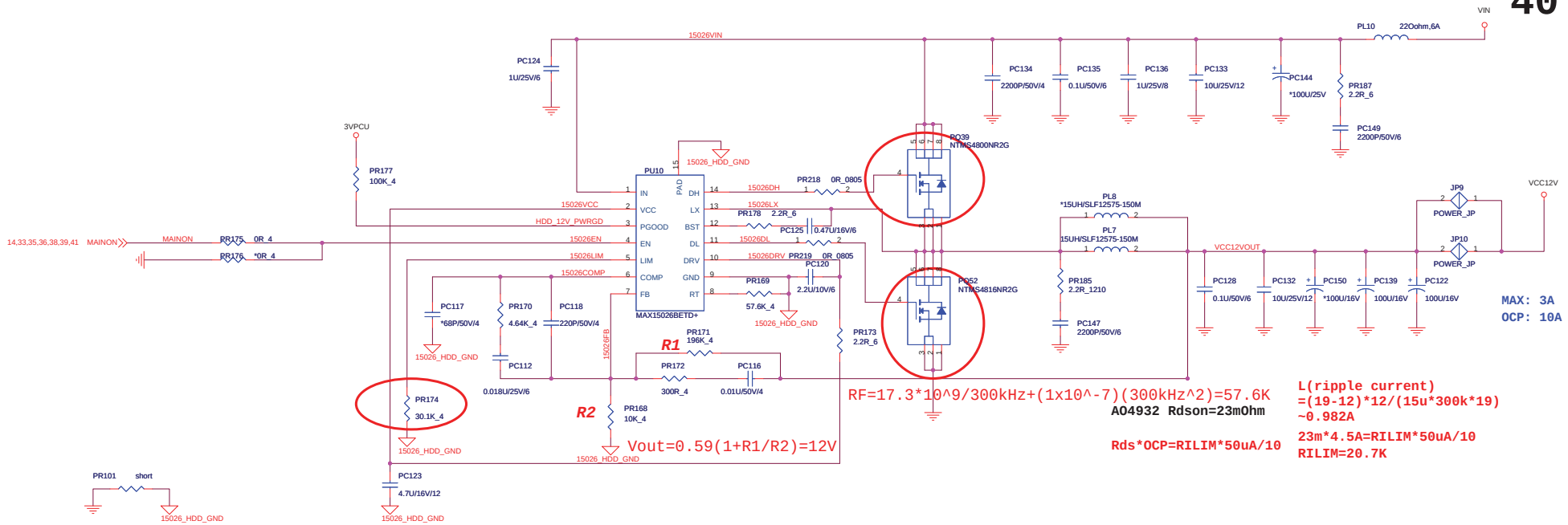
VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V



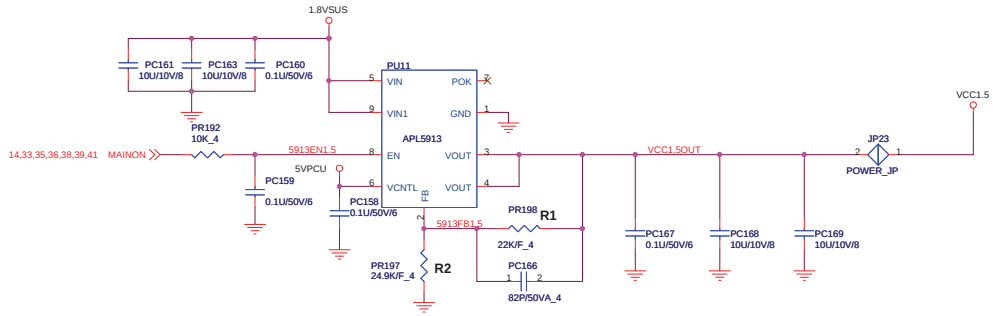
12/01 change the footprint to SOT23_213-3_3-2

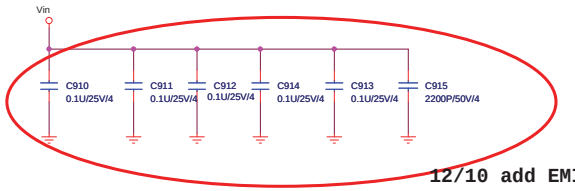
Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	FAN\LED\Switch	A
Date: Saturday, February 21, 2009	Sheet 39 of 44	



MINI CARD POWER

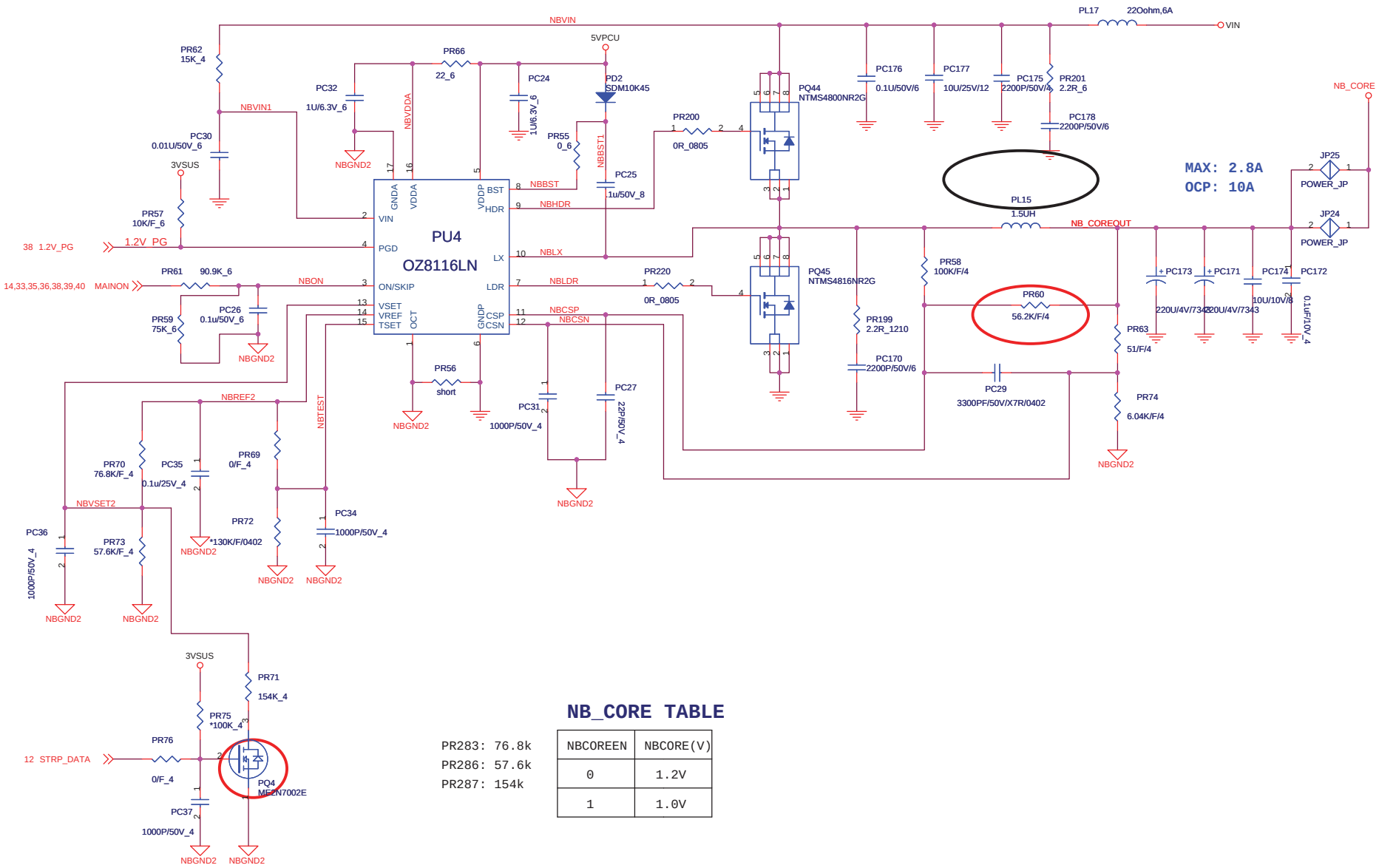




12/10 add EMI soluation

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	FAN\LED\Switch	A
Date: Saturday, February 21, 2009	Sheet 40 of 44	



NB_CORE TABLE

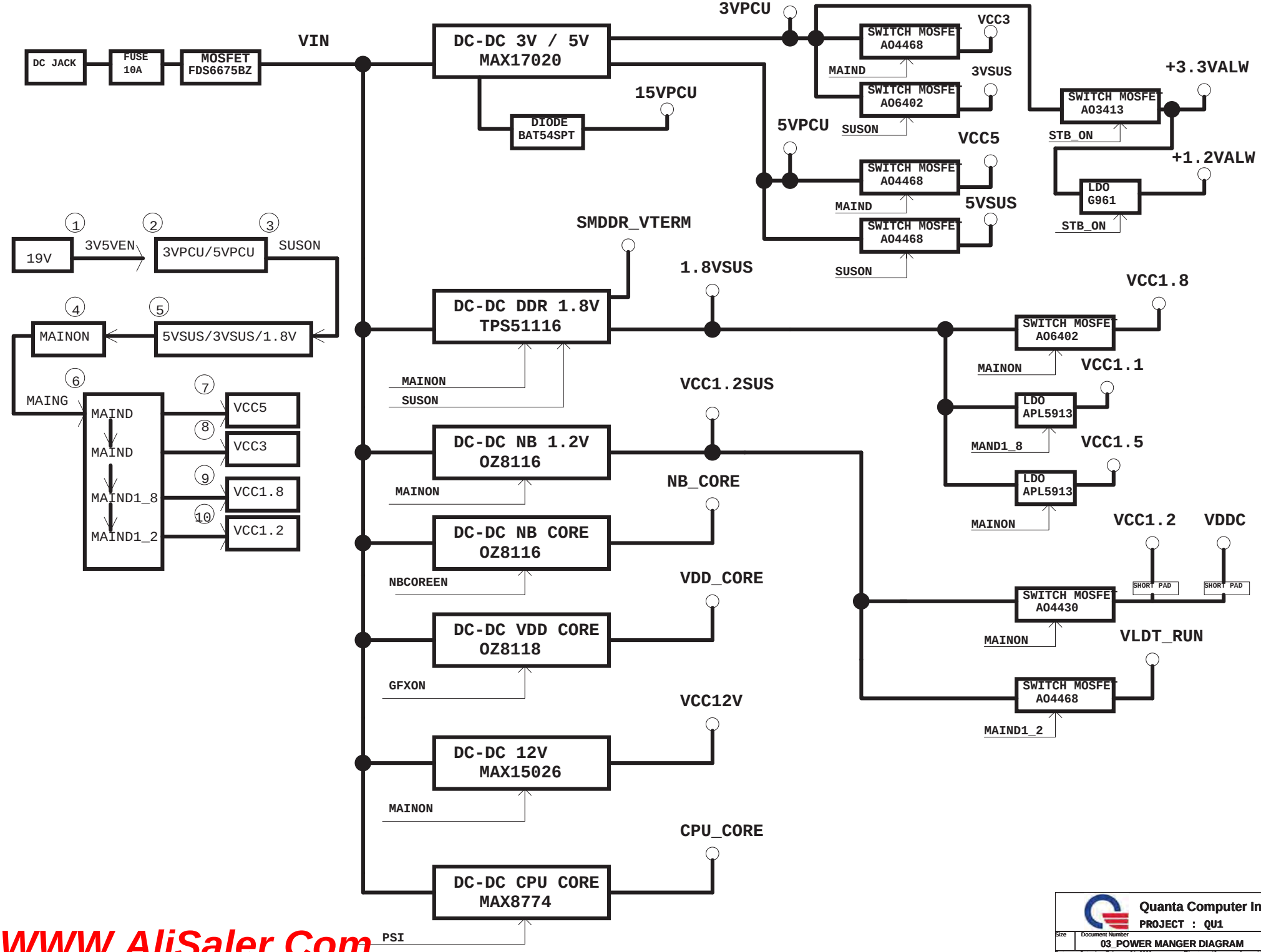
PR283: 76.8k
PR286: 57.6k
PR287: 154k

NBCOREEN	NBCORE(V)
0	1.2V
1	1.0V

12/01 change the footprint to SOT23_213-3_3-2

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	FAN\LED\Switch	A
Date: Saturday, February 21, 2009	Sheet 41 of 44	



Quanta Computer Inc.
PROJECT : QU1
Size | Document Number: 03_POWER MANGER DIAGRAM | Rev A
Date: Saturday, February 21, 2009 | Sheet 42 of 44

H5 H-C276D154P2
H9 h-c394d126p2
H11 H-C276D154P2
H12 H-C276D154P2
H14 H-C276D154P2
H15 H-C276D154P2
H17 h-c394d138p2
H18 h-c394d138p2
H21 h-c394d138p2
H22 h-c394d138p2

H8 h-c394d138p2
H13 h-c394d177p2
H20 h-c394d138p2

12/02 ME DEL H10 Location

H23 h-c236d236n
H24 H-C118D118N
H25 spad-pad400x100np

H6 H-C276D79P2
H7 H-C276D79P2
H3 H-C276D79P2
H2 H-C276D79P2

12/02 change H2,H3,H6,H7 footprint to ????(waitting Layout team confirm)

12/02 change H5,H11,H12,H14,H15 footprint to ???(waitting Layout team confirm)

H1 H-C276D154P2
H4 H-C276D154P2
H16 H-C276D154P2
H19 H-C276D154P2

3VPCU C573 0.1U/25V/4
3VPCU C560 0.1U/25V/4
3VPCU C5 0.1U/25V/4
3VPCU C250 0.1U/25V/4
3VPCU C829 0.1U/25V/4
3VPCU C4 0.1U/25V/4
3VPCU C161 0.1U/25V/4

VIN C750 0.1U/25V/4
VIN C837 0.1U/25V/4
VIN C584 0.1U/25V/4
VIN C372 0.1U/25V/4
VIN C532 0.1U/25V/4
VIN C888 0.1U/25V/4

VCC12V C618 0.1U/25V/4
VCC12V C370 0.1U/25V/4
VCC12V C369 0.1U/25V/4
VCC12V C371 0.1U/25V/4

VCC3 C677 *0.1U/25V/4
VCC3 C862 0.1U/25V/4
VCC3 C227 0.1U/25V/4
VCC3 C705 0.1U/25V/4

5VSUS C103 0.1U/25V/4
5VSUS C672 0.1U/25V/4
5VSUS C219 0.1U/25V/4
5VSUS C168 0.1U/25V/4

VCC1.2 C309 0.1U/25V/4
VCC1.2 C708 0.1U/25V/4

VCC5 C617 0.1U/25V/4
VCC5 C587 0.1U/25V/4
VCC5 C690 0.1U/25V/4
VCC5 C867 0.1U/25V/4

VCC5 C588 0.1U/25V/4
VCC5 C544 0.1U/25V/4
VCC5 C675 0.1U/25V/4
VCC5 C545 0.1U/25V/4

1.8VSUS C13 0.1U/25V/4
1.8VSUS C12 0.1U/25V/4
1.8VSUSOUT C877 0.1U/25V/4

VDD_CORE C610 0.1U/25V/4
VDD_CORE C609 0.1U/25V/4

CPU_CORE C803 0.1U/25V/4
CPU_CORE C754 0.1U/25V/4
CPU_CORE C807 0.1U/25V/4
CPU_CORE C714 0.1U/25V/4

Quanta Computer Inc.
PROJECT : QU1

Size	Document Number	Rev
	SCREW HOLE & EMI	A
Date: Saturday, February 21, 2009	Sheet 43 of 44	

A (EVT) stage :

Issue **Root Cause**

1.change Y2 to BG625000885 ==> wrong footprint,change component.

2.change F1,F2,F3 to BG625000885 ==> wrong footprint, modify layout.

3.change CN5,CN8 to DFHS52FR009 ==> ME request connector move to TOP layer.Top layer have high limit so change component.

4. 12/01 P8----change CN14 footprint (ddr-as0a426-nfst-7f-200p)---SMT issue

5. 12/02 P12---change U7 P/N:AL001032002

6. 12/01 P14---Update the Y5 footprint (XTAL-8_4X3_7-5_5X2_8)(footprint error)

7. 12/02 P14---Update the BT1 footprint---pindefine error issue

8. 12/05 P15---Change USB Power from Vcc3 to 3VSUS(HW change)

9. 12/02 P16---change Y2 P/N:BG625000885 (footprint not match)

10.12/05 P17---del Q9 for RD debug(HW Change)

11. 11/28 P19---del R330,R324(white screen issue)

12. 11/28 P19---exchange D35,D36 to R686,R687(white screen issue)

13. 12/01 P19---change Q2,Q3 footprint to SOT23_213-3_3-2(footprint error)

14. 12/01 P20---change Q27,Q31 footprint to SOT23_213-3_3-2(footprint error)

15. 12/01 P23---change U12 p/n to AL17SZ08006(Buyer request)

16.12/05 P26---Layout update the CN11 footprint

17. 12/01 P27---change F1,F2,F3 P/N (DK150TPU072) and footprint (f-3_2x1_65-3_68)

18. 12/02 P29---change J1,J2 PN:DFHS04FR207(SMT issue)

19. 12/05 P29---change CN6,CN7 Footprint sata-aba-sat-010-k07-7p-r(footprint error)

20. 11/28 P30---add Speaker function(Add R683,R684,C904)

21.12/01 P30---change Q2,Q3 footprint to SOT23_213-3_3-2(footprint error)

22. 12/01 P30---Exchange MICIN-R and MICIN-L

23. 12/02 P31---change CN5,CN8 P/N because this CONN H=8(DFHS52FS000)

24.12/02 P31---12/04 ADD debug port function(Add net--PCICLK_DB)

25. 12/01 P32---del U1,Q1,Q3,R13,C11,R21,R11,R29

26.12/01 P32---change Q15,Q23,Q26 footprint to SOT23_213-3_3-2(footprint error)

27. 12/01 P32---12/01 change the net name to VFAN2 and CPU_VFAN

28. 12/01 P32--- DEL Q15(Lenovo Del the Light Bar function)

29. 12/01 P32---change the power From VCC3 to VCC5

30. 12/01 P33---Add R52(CS00002JB38) for PWRLED function

31. 12/04 P33---change U3 PN:AKE3GZN0N00

32. 12/01 P33---change Q5 footprint to SOT23_213-3_3-2

33. 12/01 P36-- ADD PR4,Del PR8(power Issue)

34. 12/01 P37---del PR37(power Issue)

35. 12/03 P37---Change the PR204 ,PR205 P/N

36. 12/01 P38---Del PQ43(Power Issue)

37. 12/01 P38---change PU2 p/n to AL17SZ08006(Buyer request)

38. 12/01 P39---change PQ10,PQ17,PQ24 footprint to SOT23_213-3_3-2

39. 12/03 P39---change the PR100 (2.1K); M92/M82 DEL this part.

40. 12/01 P40---del PC150 and Add PC122(near to the VCC12V)

41. 12/01 P41---change PQ4 footprint to SOT23_213-3_3-2

42. 12/02 P43--- ME request to Del H10 Location

43. 12/17 change U8,U9,U16,U18 (P/N:DFTJ12FS001) (VRAM change to 400MHZ)

B (DVT) stage :

44. 12/21 P19---del R443,ADD R446(HW LOSE)

45. 12/26 P16---change Y2 P/N to meet ACL.(BG625000737)

46. 12/21 P17---ADD R122 for HW lose

47. 12/23 P19---Add R324 for LCD white screen issue

48. 12/27 P19---Change F8=7A fuse (P/N:DK700WFU006)(LCD INRUSH CURRENT=3A)

49. 12/23 P26---del R587(LAN link issue)

50. 12/29 P26---change CN11 (P/N:DFTJ12FS001)(Change LED color)

51. 12/26 P31---change CN5,CN8 P/N to meet ACL.(DFHD52MS057)

52. 12/29 P12---ADD R689 to link VCC3(Therm_Alert# must push Hi)

Quanta Computer Inc.

PROJECT : QU1

Size	Document Number	Rev
	History	A

Date: Saturday, February 21, 2009 Sheet 44 of 44