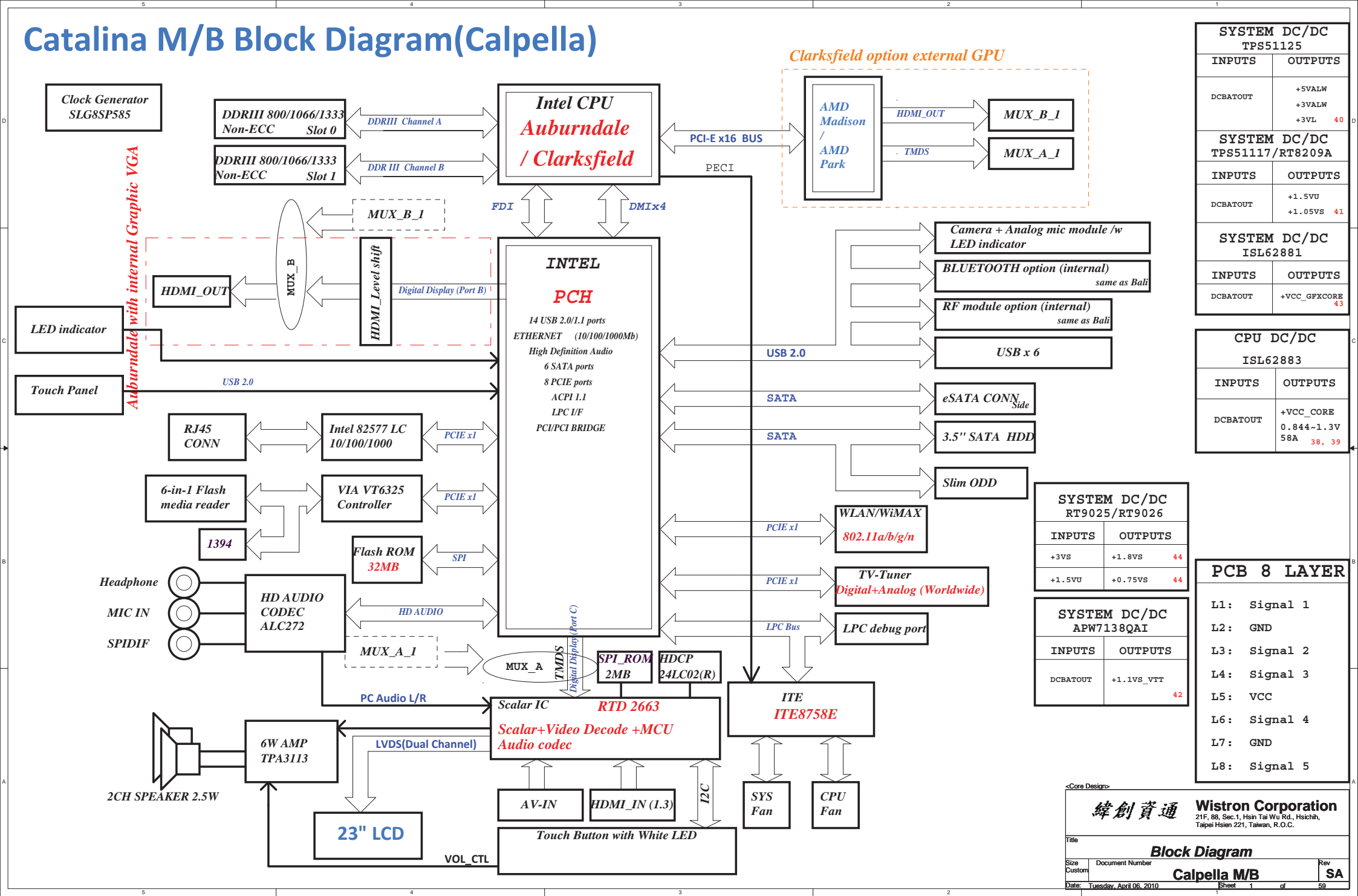


Catalina M/B Block Diagram(Calpella)



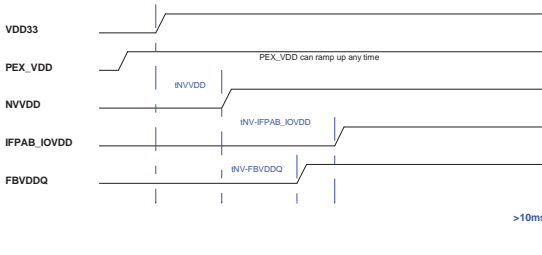
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

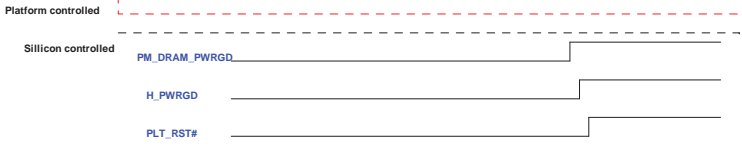
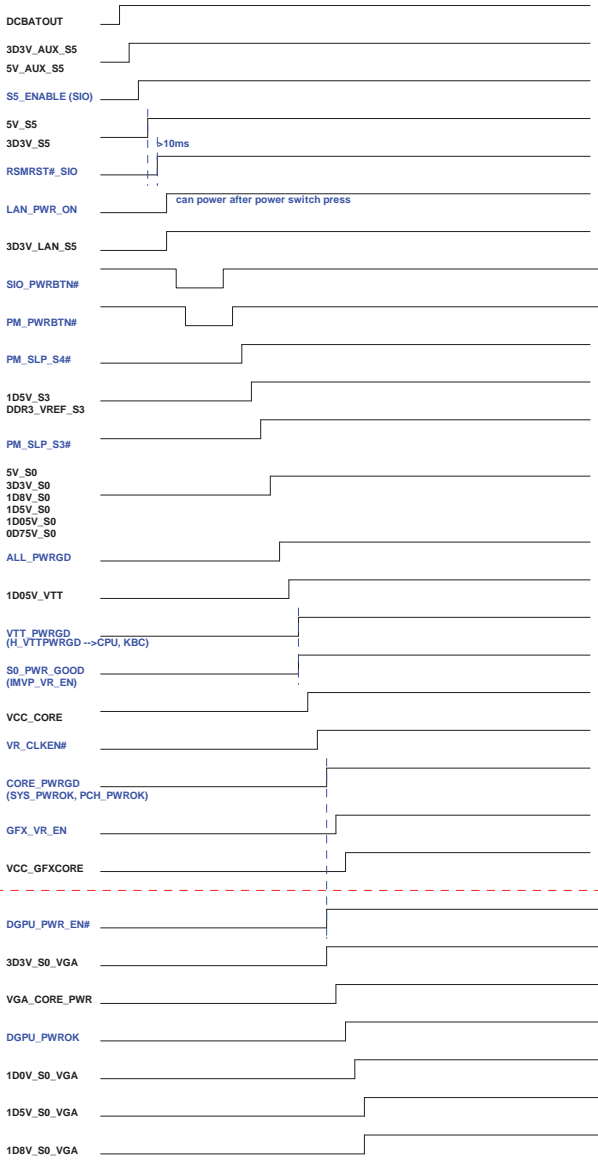
PCH Strapping

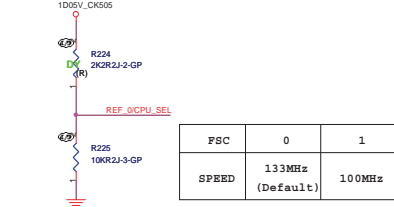
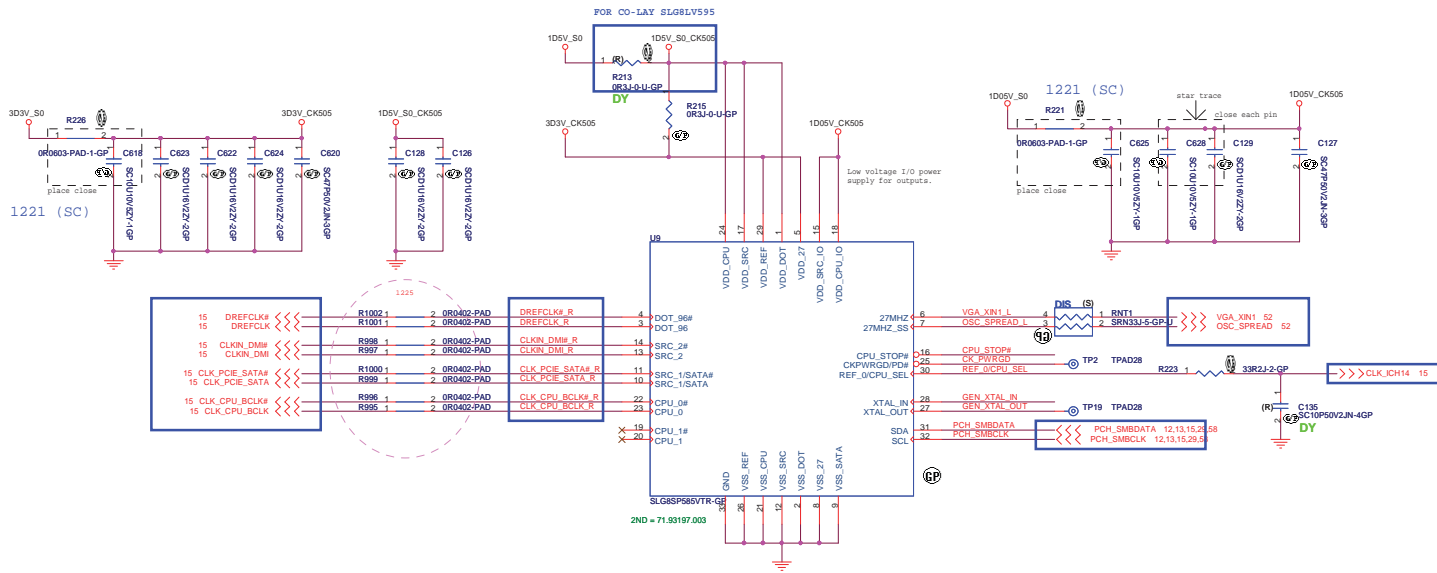
Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

N11M-GE Power Sequence



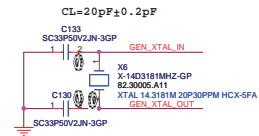
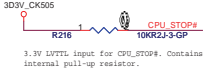
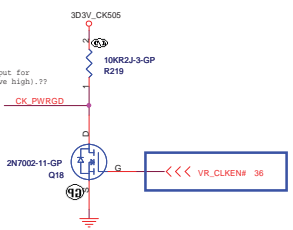
Power Sequence





FSC	0	1
SPEED	133MHz (Default)	100MHz

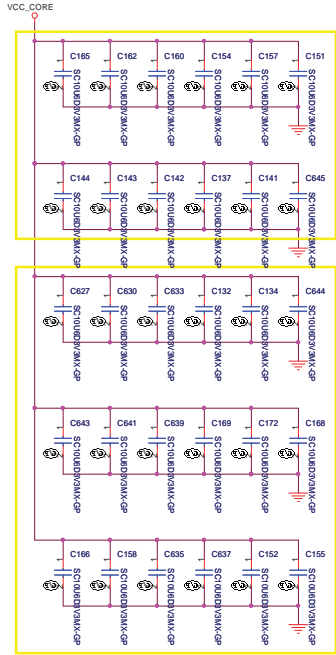
it becomes a real time input for asserting power down (active high).??



Layout Notes:
Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.

30pcs : 10uF 6.3V X5R

PROCESSOR CORE POWER
48A -->Arrandale



VCC_CORE

CPUIF

6 OF 9

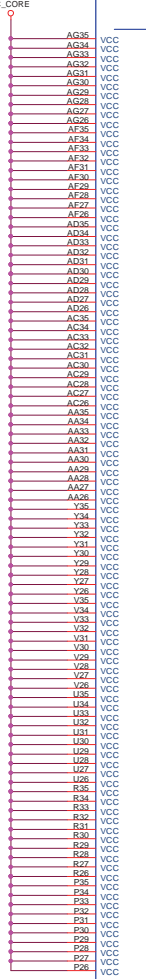
AUBURNDALE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

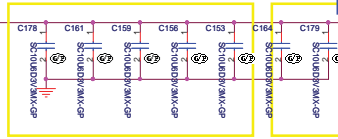
SENSE LINES



6 OF 9

1D05V_S0

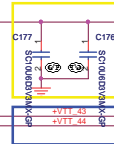
1D05V_VTT



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

1D05V_S0

1D05V_VTT



1D05V_S0

1D05V_VTT

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarkfield VTT=1.1V

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6 OF 9

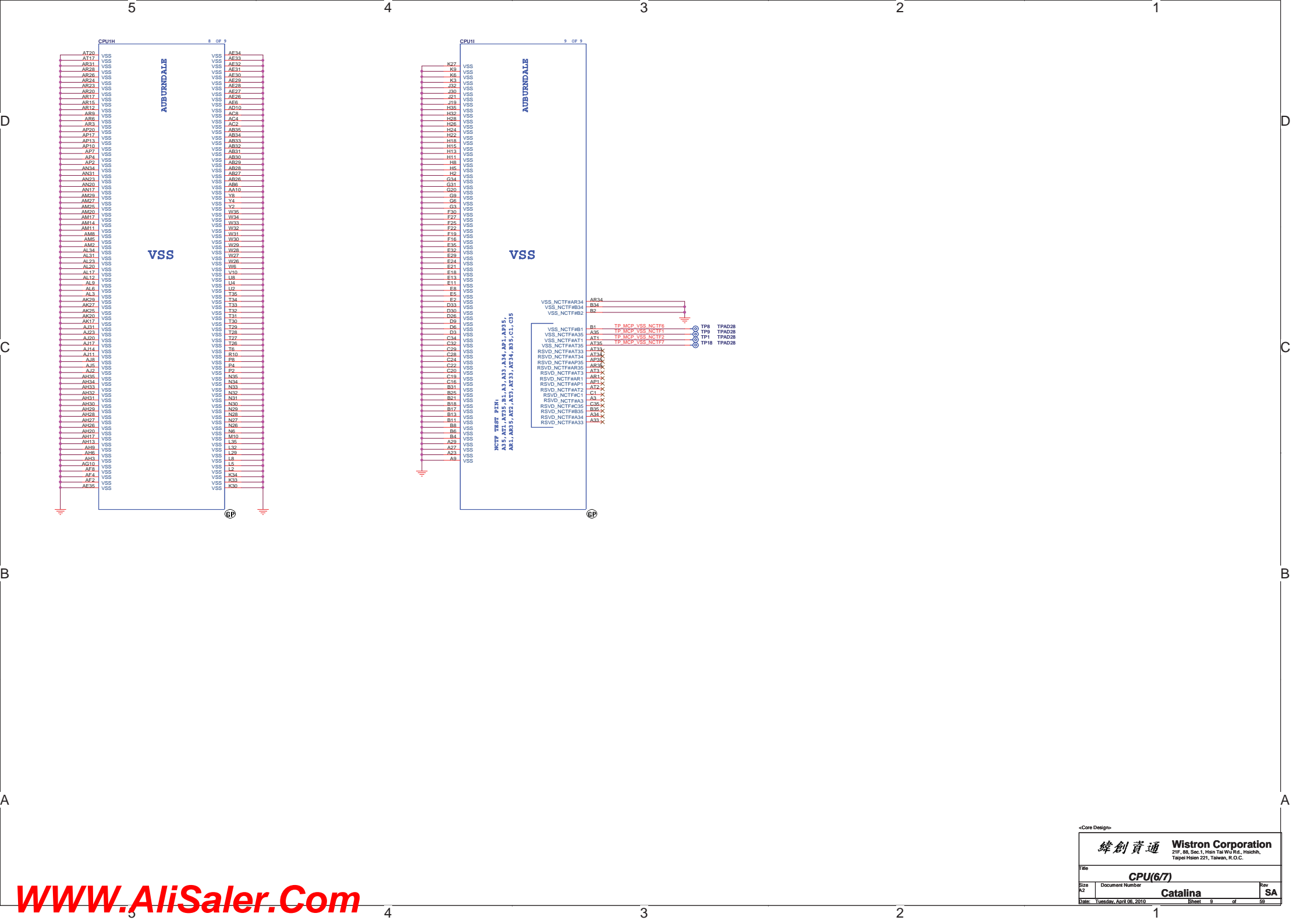
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6 OF 9

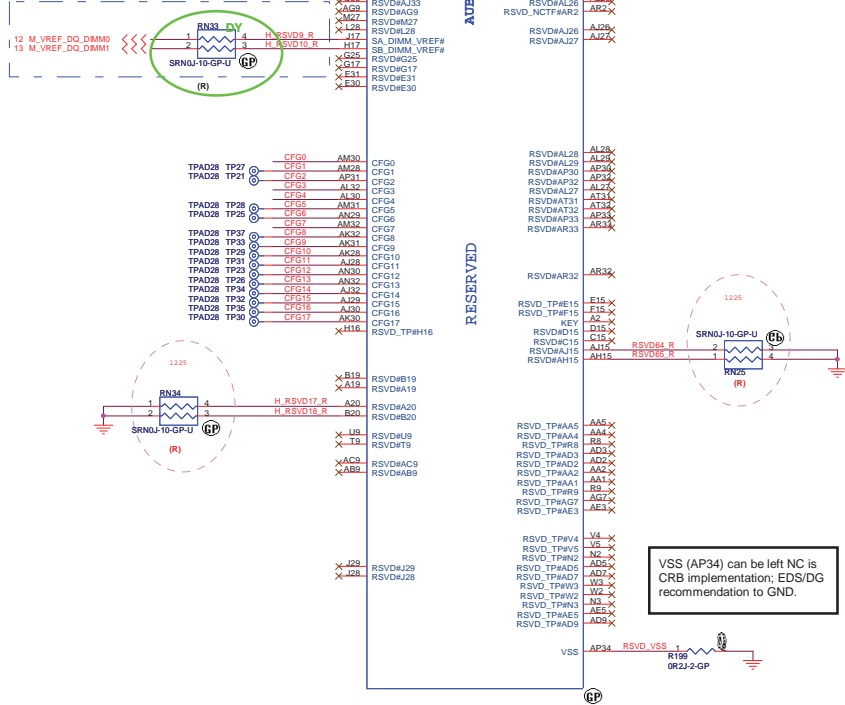
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6 OF 9

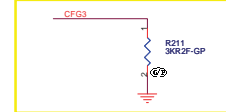
6 OF 9



SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm 5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) (For details please refer to the WW33 MoW and sighting report). For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

5

4

3

2

1

D

C

B

A

D

C

B

A

<Variant Name>		
<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 301, Taiwan, R.O.C</div>		
Title <Title>		
Size A2	Document Number <Doc>	Rev <Rev>Code
Date: Tuesday, April 06, 2010	Sheet 11 of 59	

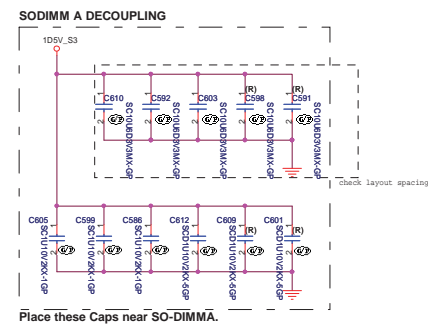
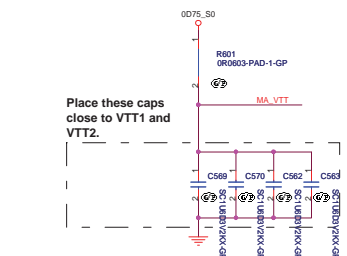
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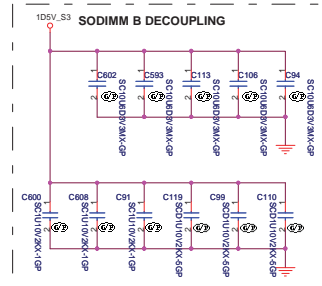
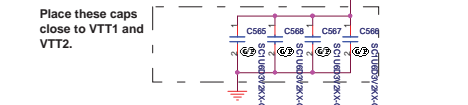
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3

2

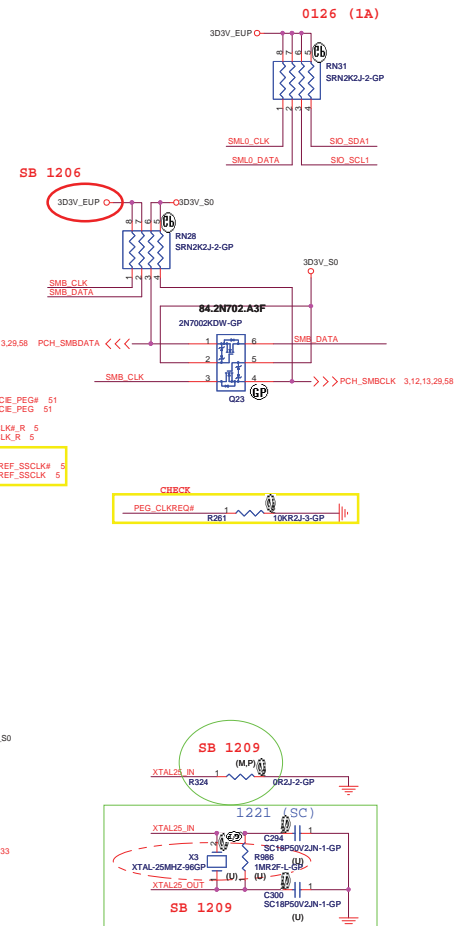
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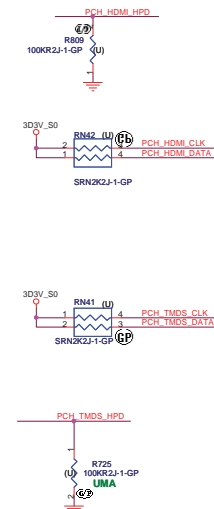
<p>Note: SO-DIMMB SPD Address is 0xA4 SO-DIMMB TS Address is 0x34</p>		<p>SO-DIMMB is placed farther from the Processor than SO-DIMMA</p>
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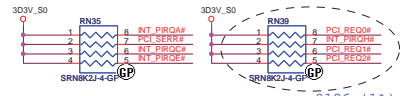
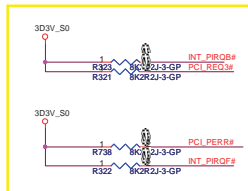
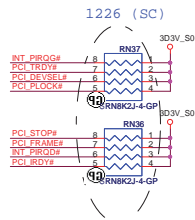
H = 5.2mm 5.2mm REVERSE



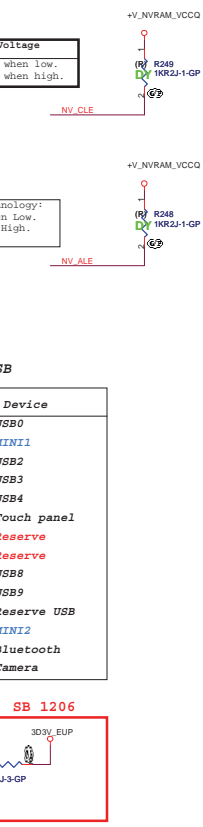
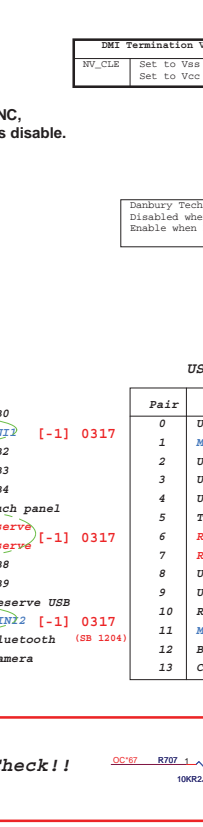
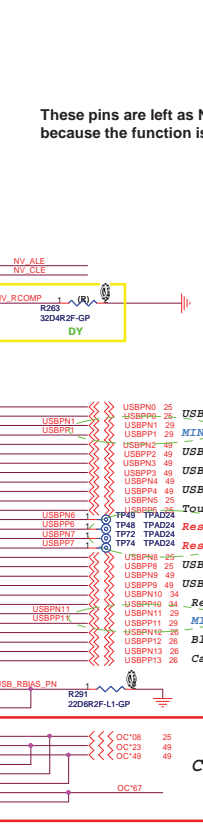
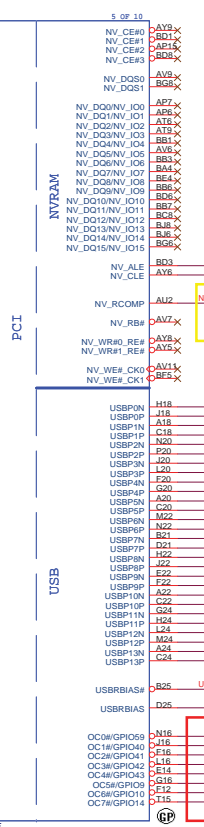
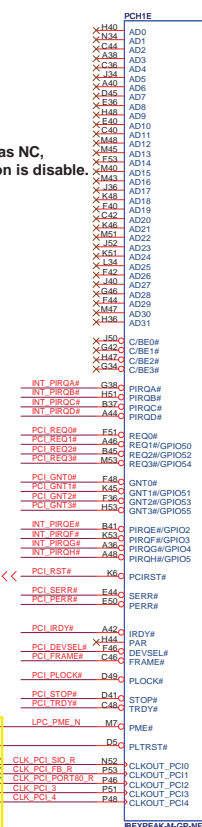
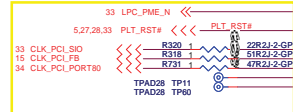
SB 1206
Delete!!

SB 1206





BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



DMX Termination Voltage
NV_CLE Set to Vss when low.
Set to Vcc when high.

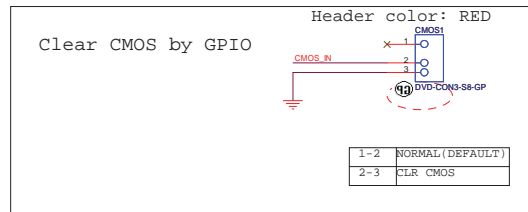
Danbury Technology:
Disabled when Low.
Enable when High.

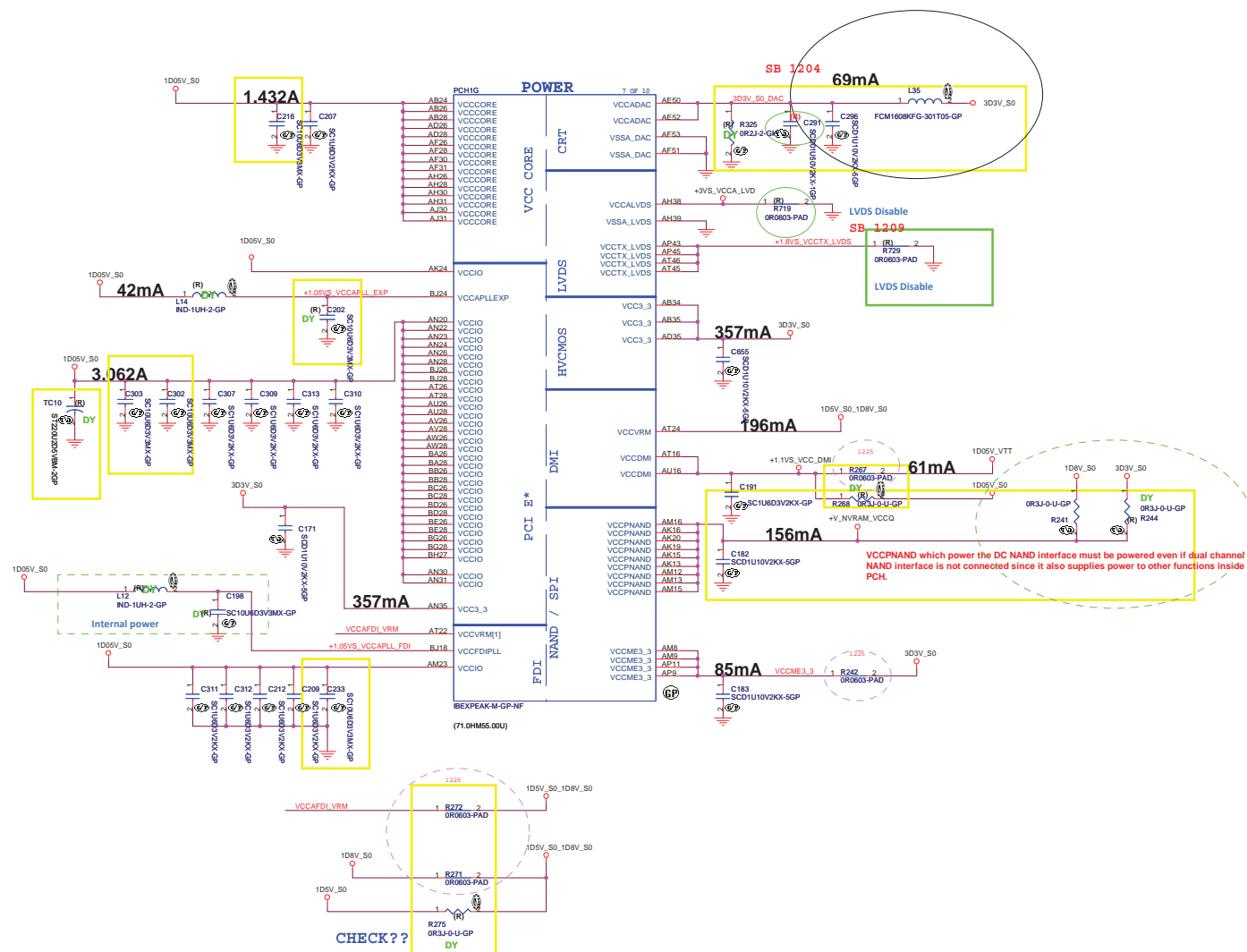
Pair	Device
0	USB0
1	MINI1
2	USB2
3	USB3
4	USB4
5	Touch panel
6	Reserve
7	Reserve
8	USB8
9	USB9
10	Reserve USB
11	MINI2
12	Bluetooth
13	Camera

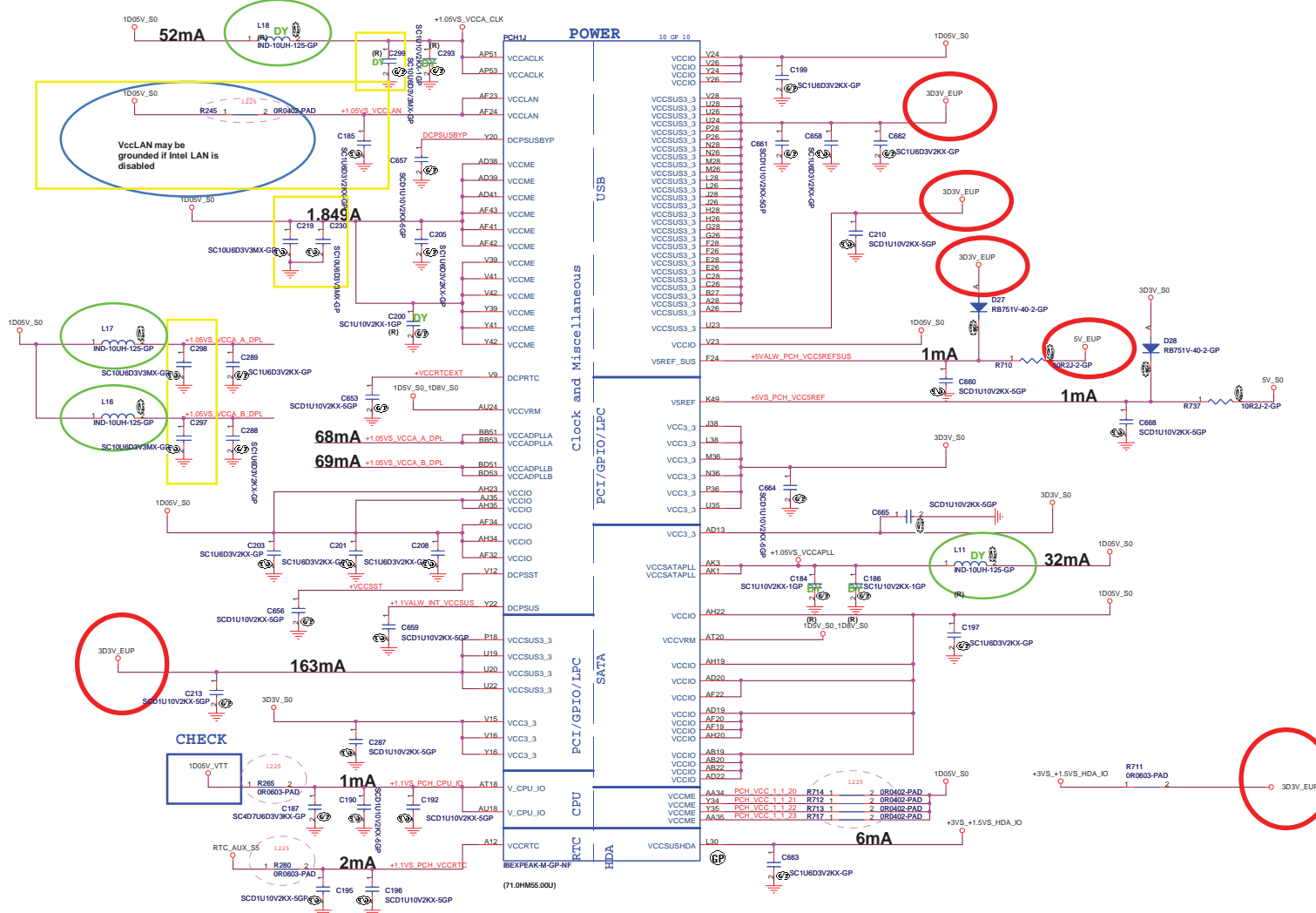
Check !!

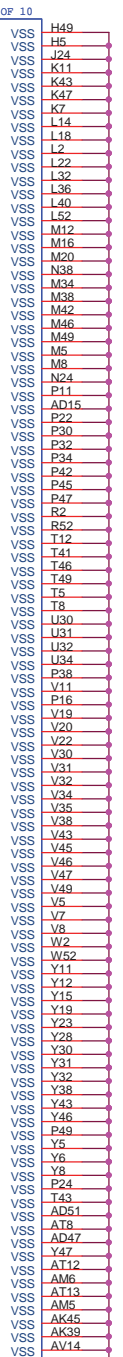
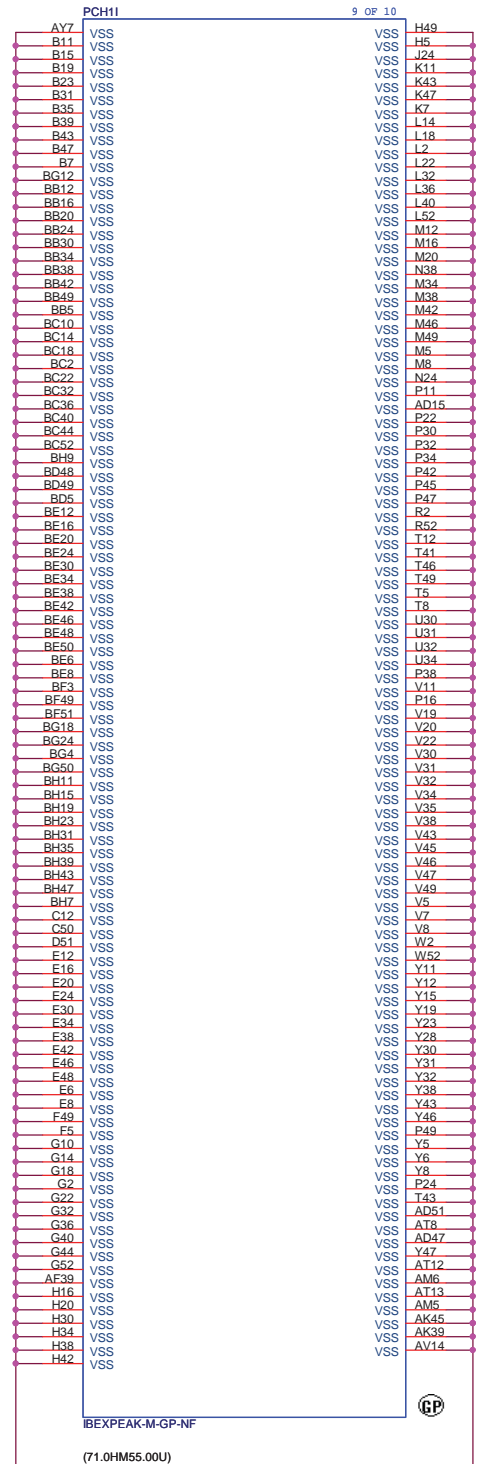
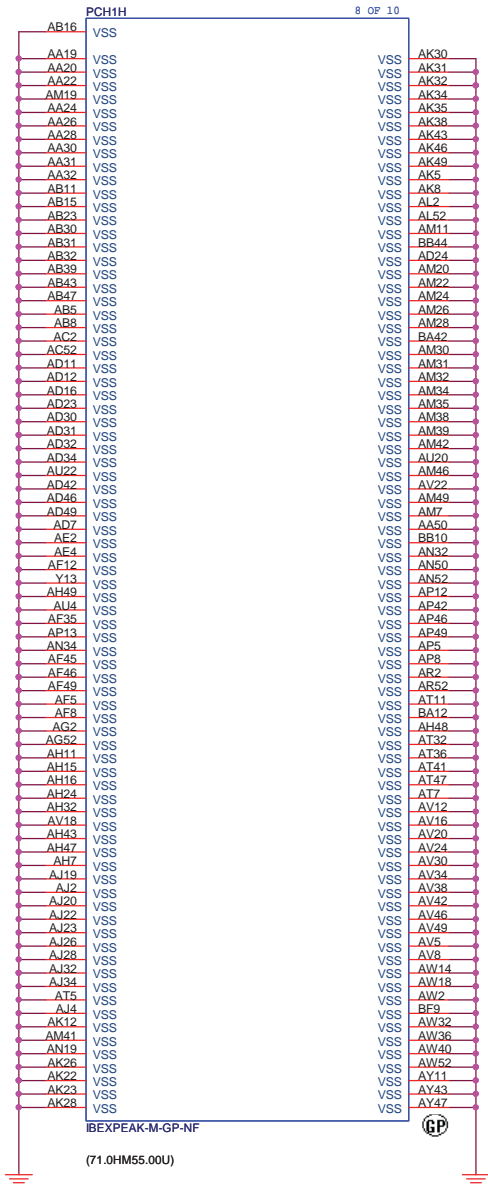
A16 swap override Strap/Top-Block
Swap Override jumper

PCI_GNT#3 Low = A16 swap
override/Top-Block
Swap Override enabled
High = Default









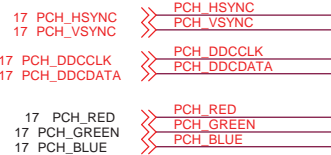
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

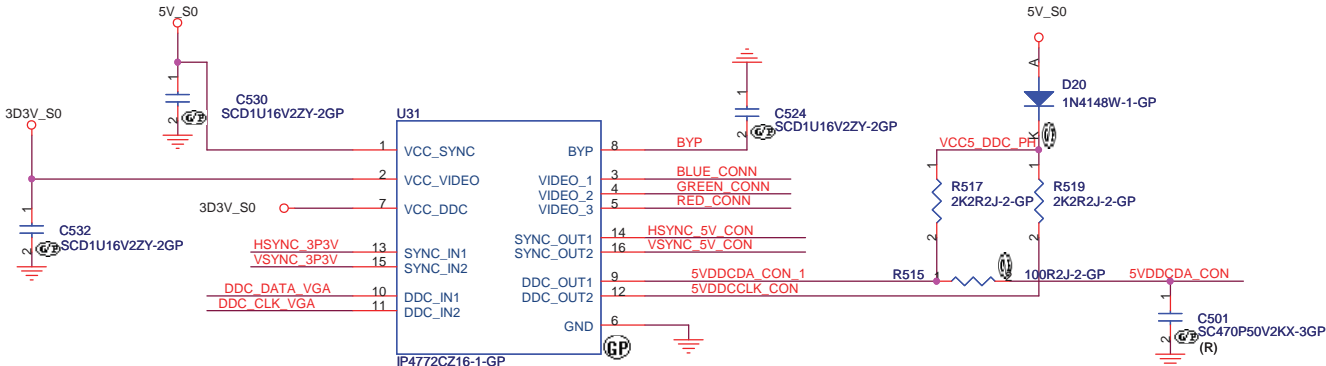
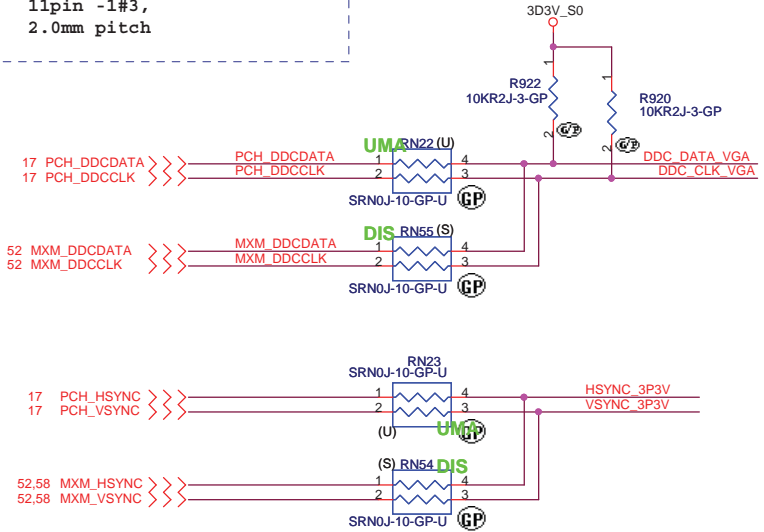
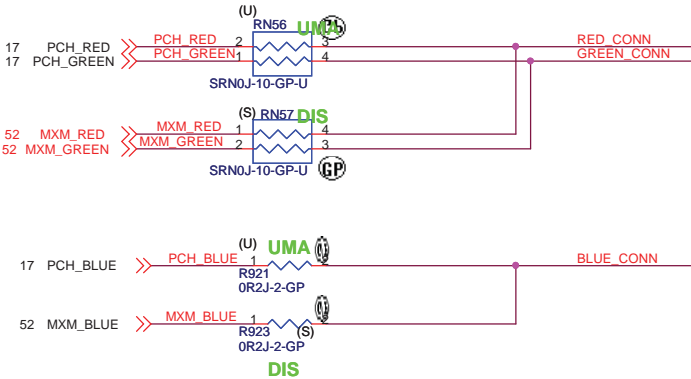
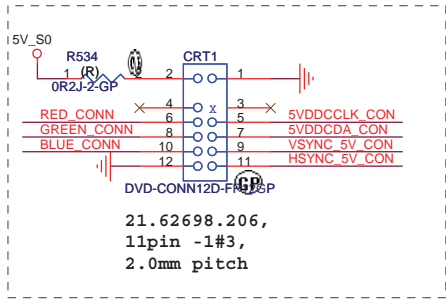
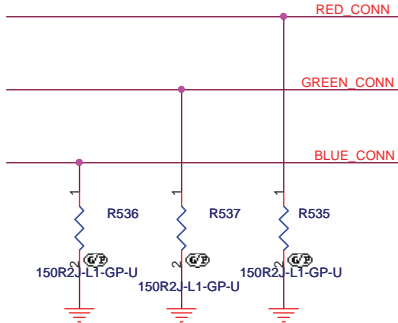
Title		
PCH(9/9)		
Size	Document Number	Rev
A3		SA
Catalina		
Date:	Tuesday, April 06, 2010	Sheet 22 of 59

CRT header for debug

From PCH



From MXM

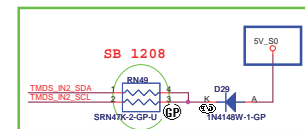
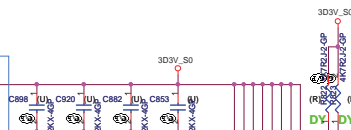
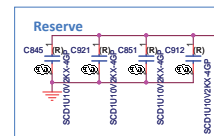
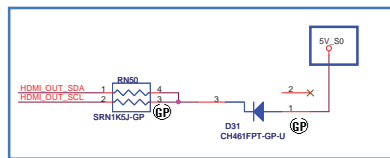
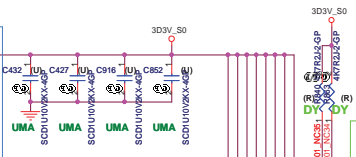
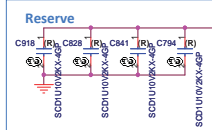
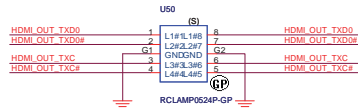
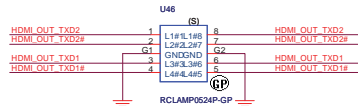


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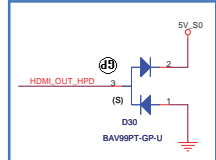
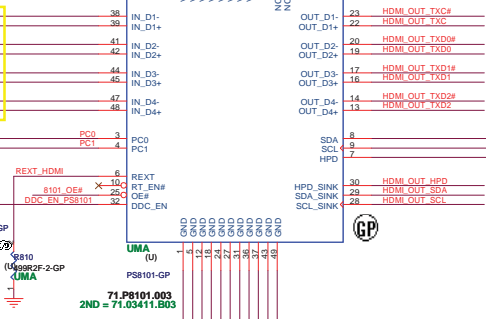
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
VGA header	
Size B	Document Number
Catalina	
Date: Tuesday, April 06, 2010	Sheet 23 of 59

CHECK UMA AND DIS !!

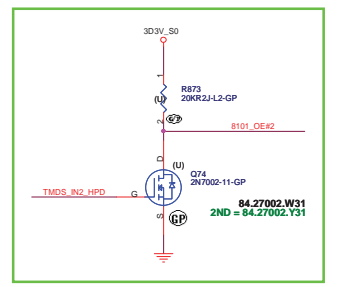
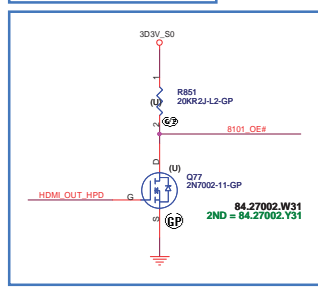
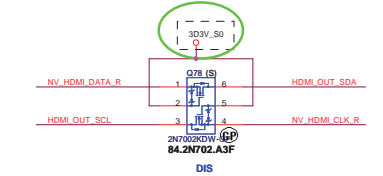
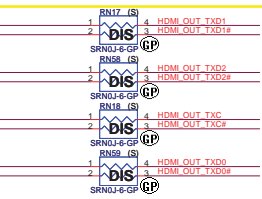
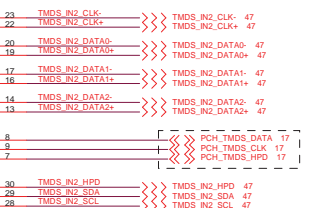
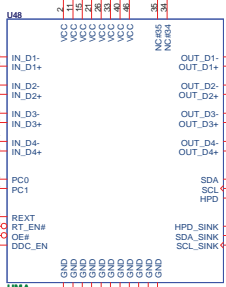
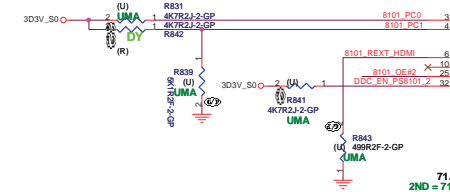
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HDMI_OUT_TXD0 >>> HDMI_OUT_TXD0 49
HDMI_OUT_TXD0# >>> HDMI_OUT_TXD0# 49
HDMI_OUT_TXC >>> HDMI_OUT_TXC 49
HDMI_OUT_TXC# >>> HDMI_OUT_TXC# 49
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HDMI_OUT_SDA >>> HDMI_OUT_SDA 49
HDMI_OUT_HPD >>> HDMI_OUT_HPD 49



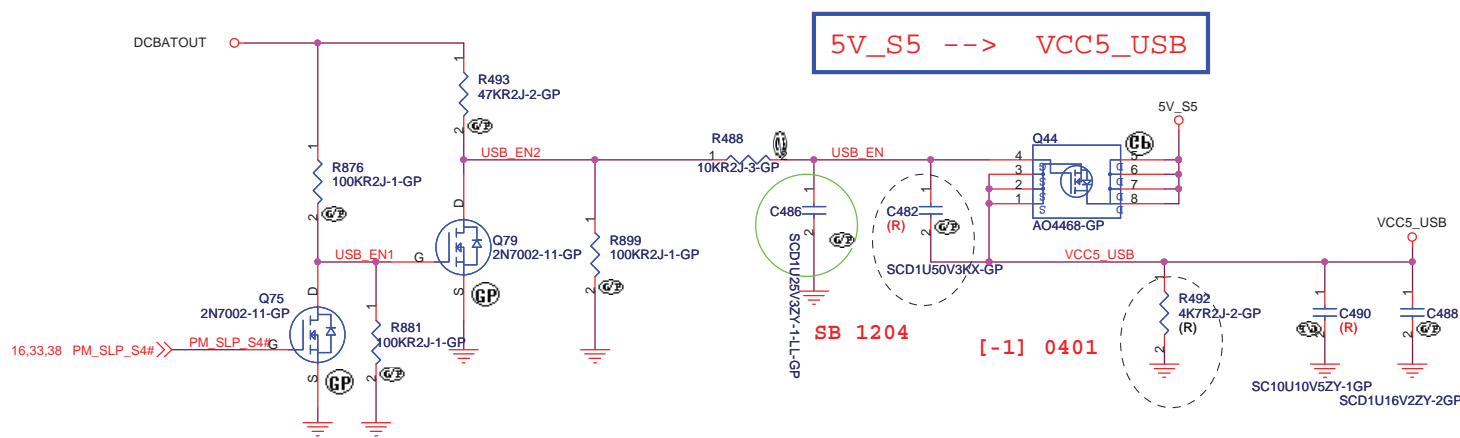
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[PC1,PC0]=01, 4dB



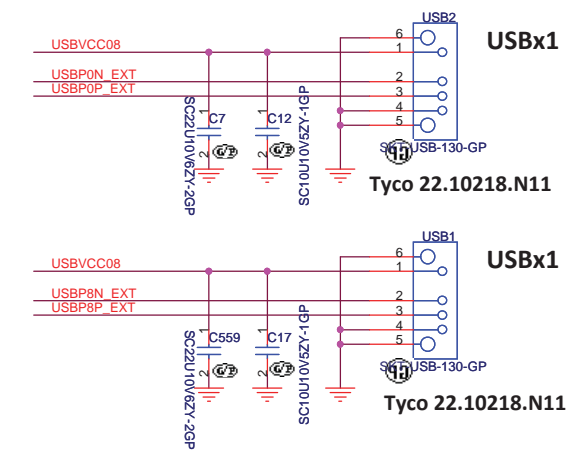
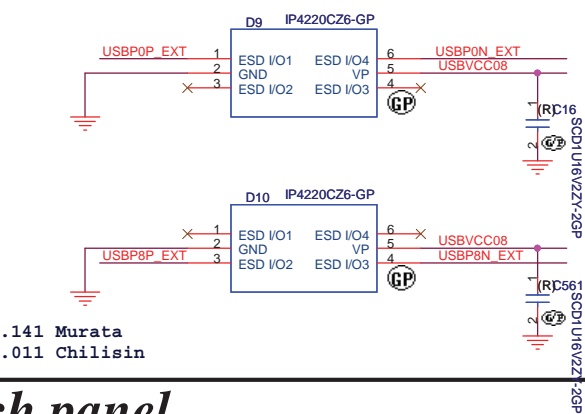
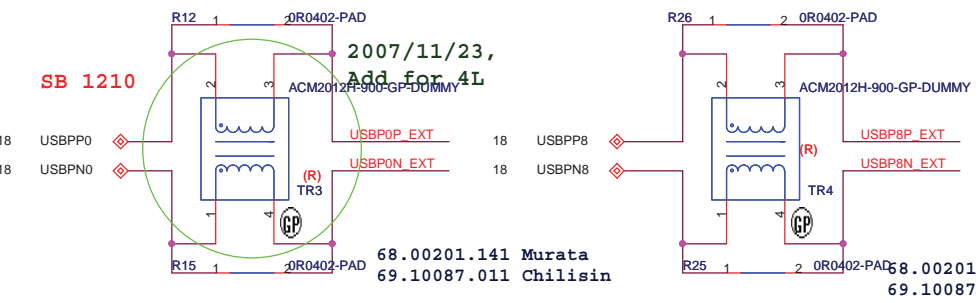
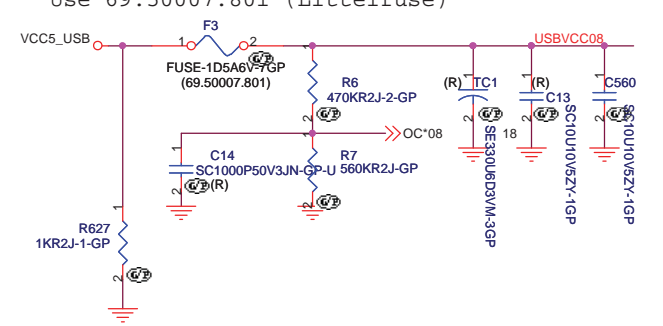
Recommended Equalization:
[PC1,PC0]=01, 4dB



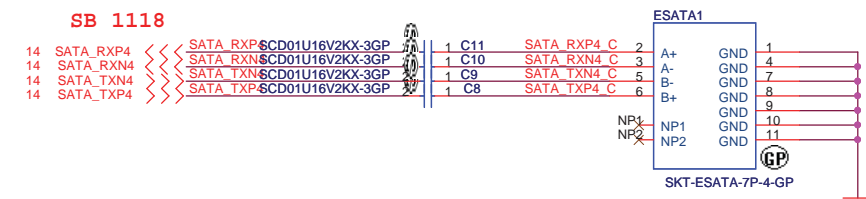
USB PORT Side 2 USB PORT (0/1)



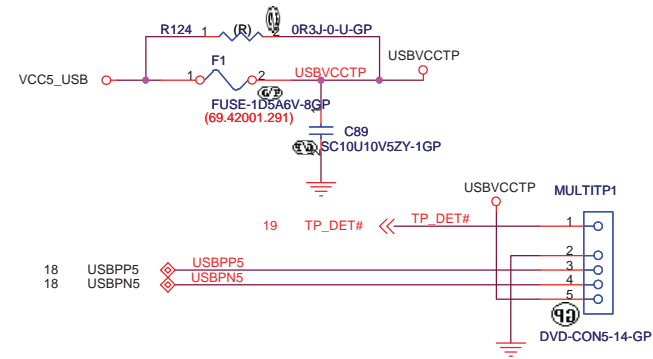
USB Power



eSATA PORT



Touch panel



<Core Design>

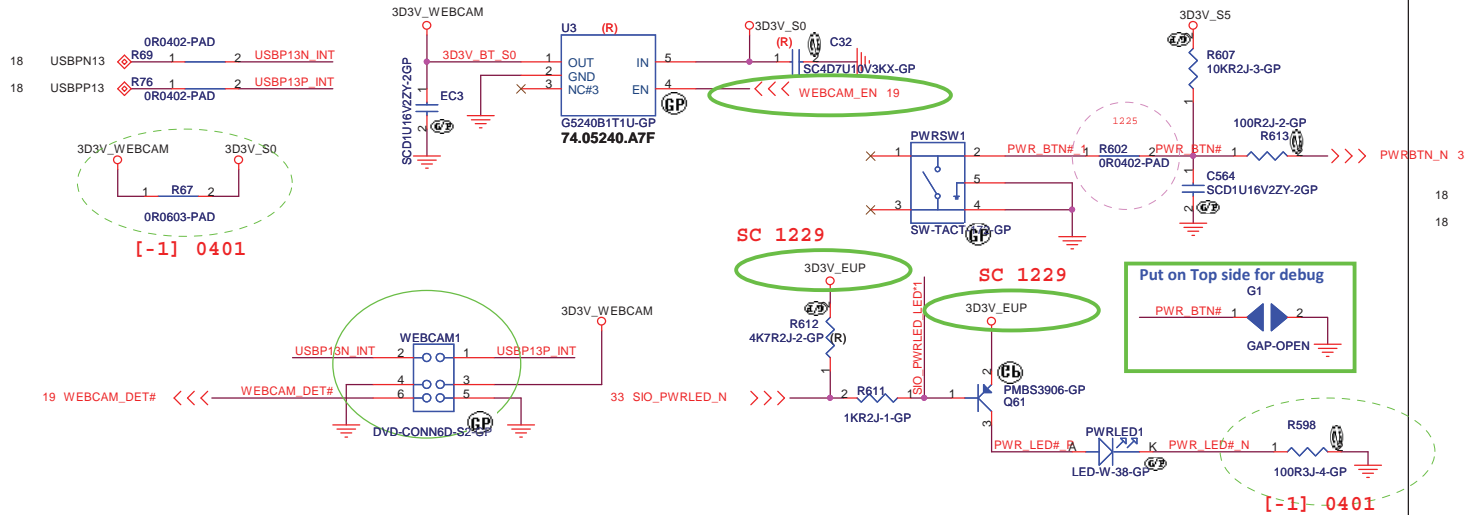
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB IO/eSATA/TP**

Size: B Document Number: **Catalina** Rev: **SA**

Date: Tuesday, April 06, 2010 Sheet 25 of 59

CAMERA



RF->Wireless KB/MS

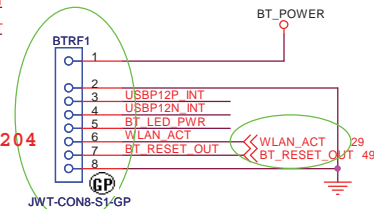
REMOVE!!

SB 1204

Blue tooth



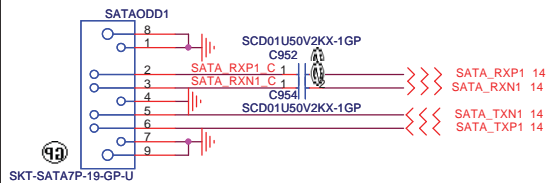
SB 1204



CD-ROM CONNECTOR

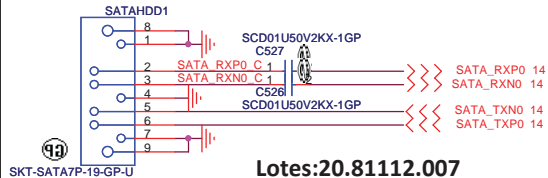
Check HD power(+12V) and connector type

Check connection!!



MAIN HDD Connector

Check connection!!

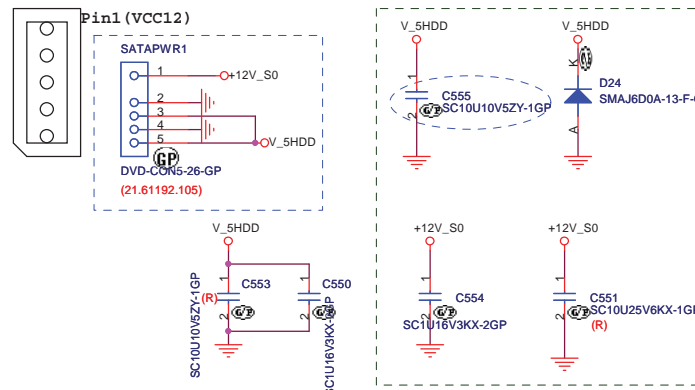


Lotes:20.81112.007

Molex: 20.80618.007

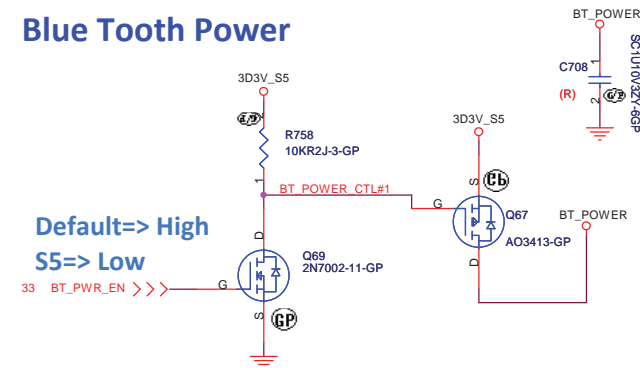
HDD Power Connector

Layout: Please put them together

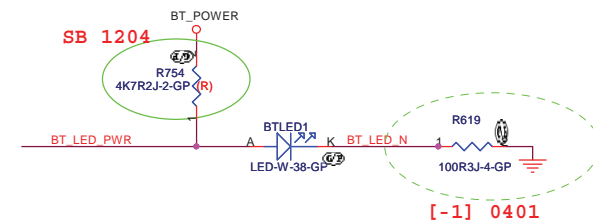


Blue Tooth Power

Default=> High
S5=> Low



SB 1204



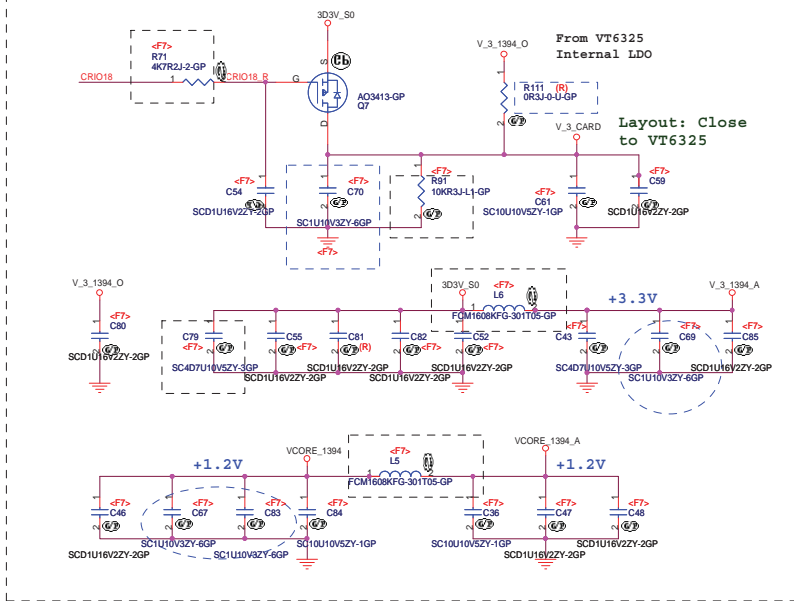
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緯創資通

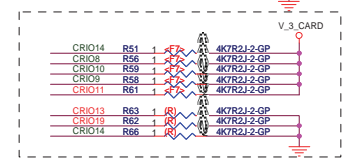
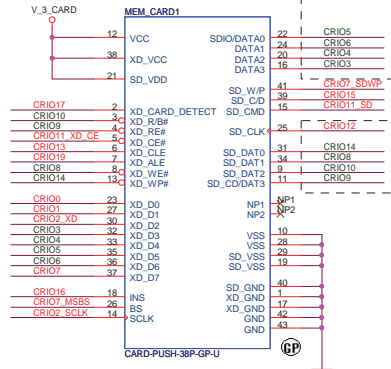
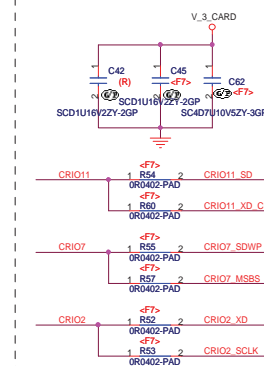
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Taipei Hsien 221, Taiwan, R.O.C.

HDD/ODD IF+USB device			
Size A3	Document Number	Catalina	Rev SA
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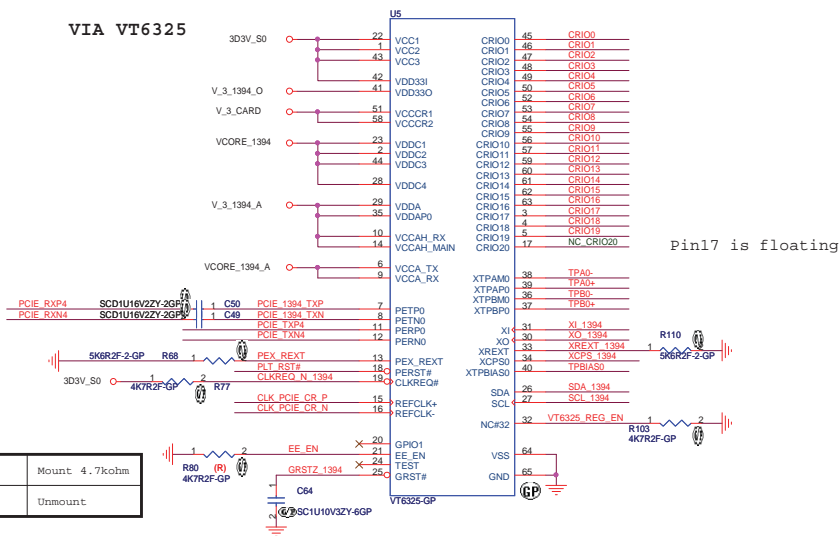
15 CLK_PCIE_CR_P
15 CLK_PCIE_CR_N
15 PCIE_RXP4
15 PCIE_RXN4
15 PCIE_TXP4
15 PCIE_TXN4
5,18,27,33 PLT_RST#



Layout: Close to Card connector

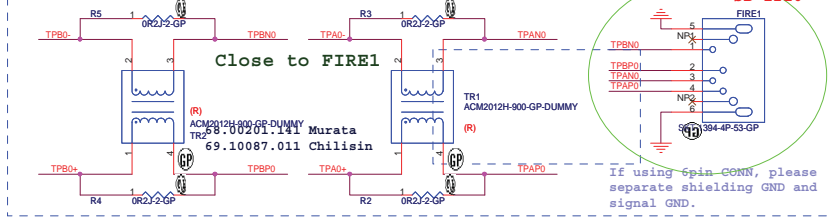


VIA VT6325

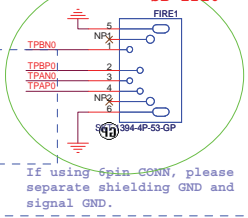


Pin17 is floating

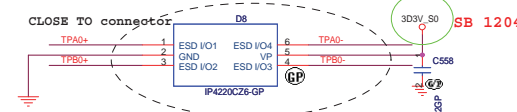
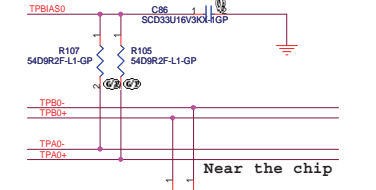
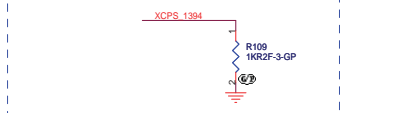
1394 port Common Choke



Front 4pin SB 1210

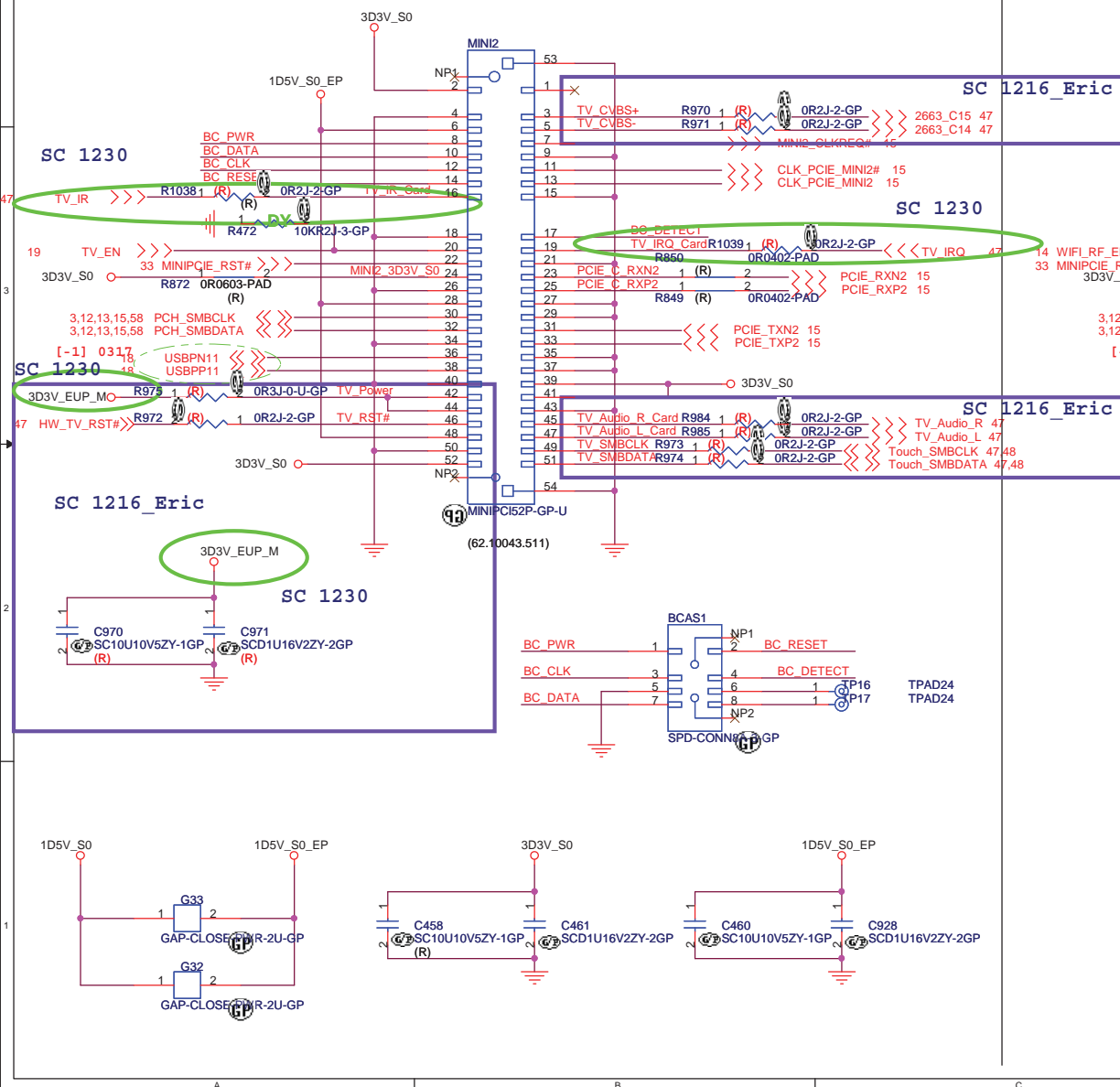


XCPS Definition:
For 6pin type of 1394, mount 11kohm res to +12V.
For 4pin type, unmount 11kohm res.
Both of type need mount 1kohm to GND.

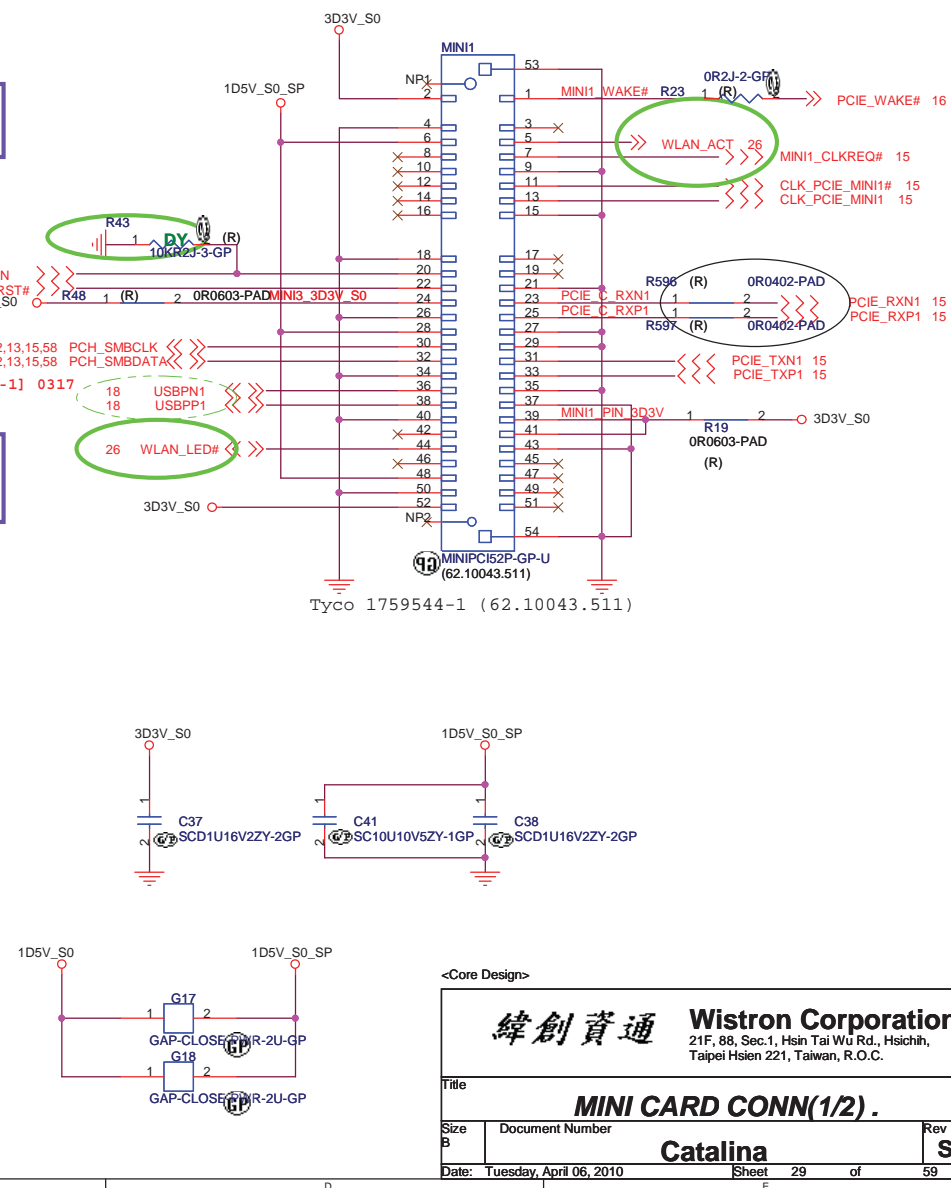


Mini PCI-E Connector

TV-TUNER Card



Wireless Card(Present support EP/SP)



```

14 ACZ_RST#_AUDIO >>> ACZ_RST#_AUDIO
14 ACZ_SYNC_AUDIO >>> ACZ_SYNC_AUDIO
14 ACZ_SDATAIN0 >>> ACZ_SDATAIN0
14 ACZ_BITCLK_AUDIO >>> ACZ_BITCLK_AUDIO
14 ACZ_SDATAOUT_AUDIO >>> ACZ_SDATAOUT_AUDIO
14 ACZ_SPKR >>> ACZ_SPKR

```

```

32 MIC_R_JACK >>> MIC_R_JACK
32 MIC_L_JACK >>> MIC_L_JACK

```

49 SPDIF <<< SPDIF

```

32 MIC_IN_JD >>> MIC_IN_JD
32 HP_OUT_JD >>> HP_OUT_JD

```

32 EAPD# <<< EAPD#



	A	B	C	D	E
4					
3					
2					
1					
	A	B	C	D	E

<Core Design>

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Title			
Reserve			
Size B	Document Number		Rev
	Catalina		SA
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```

30 MIC_L_JACK >>>
30 MIC_R_JACK >>>

```

30 ALC272_HP_OUT_L >> ALC272 HP_OUT L
30 ALC272_HP_OUT_R >> ALC272 HP_OUT R

30 MIC_IN_JD >> MIC_IN_JD

30 HP_OUT_JD >> HP_OUT_JD

30 EAPD#  EAPD#

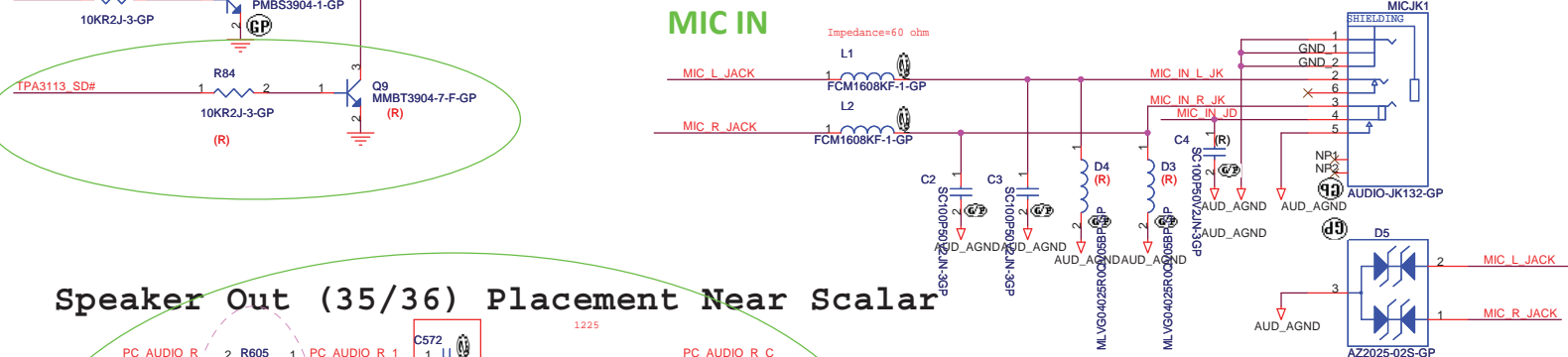
47,48 TPA3113_SD# >> TPA3113_SD#

```

30 PC_AUDIO_R  >>> PC_AUDIO_R
30 PC_AUDIO_L  >>> PC_AUDIO_L

47 PC_AUDIO_R_C <<< PC_AUDIO_R_C
47 PC_AUDIO_L_C <<< PC_AUDIO_L_C

```



The diagram illustrates the internal structure of the SC1225 codec block, which is part of the SB 1209 system. The block is divided into two main sections: the top section for the right channel (R) and the bottom section for the left channel (L).

Top Section (Right Channel):

- Inputs:** PC_AUDIO_R (2 pins) and R605 (1 pin) are connected to the 0R0402-PAD.
- Outputs:** PC_AUDIO_R_C (1 pin) is connected to the 1225 output.
- Internal Components:** C572 (1 pin) and SC22U6D3V5MX-2GP are shown. The text "near codec" is present.

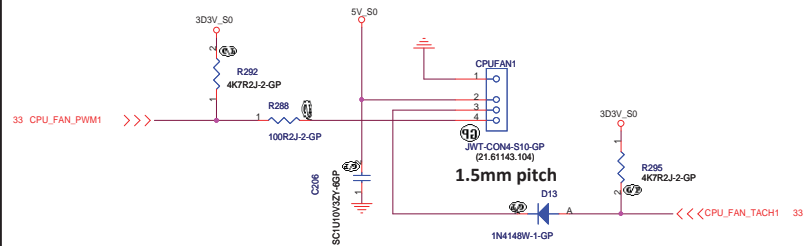
Bottom Section (Left Channel):

- Inputs:** PC_AUDIO_L (2 pins) and R604 (1 pin) are connected to the 0R0402-PAD.
- Outputs:** PC_AUDIO_L_C (1 pin) is connected to the 1223 output.
- Internal Components:** C571 (1 pin) and SC22U6D3V5MX-2GP are shown. The text "near codec" is present.

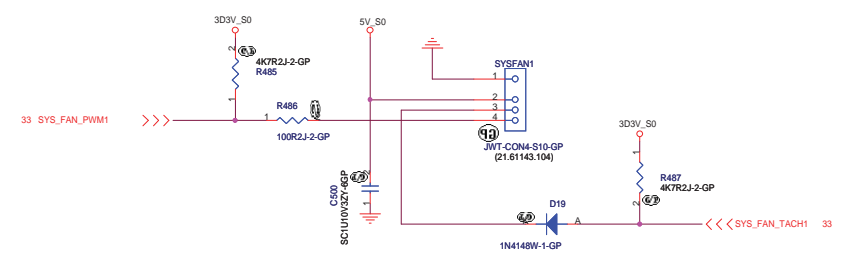
System Context:

- The entire block is labeled **SB 1209**.
- The overall system is labeled **SC 1226**.

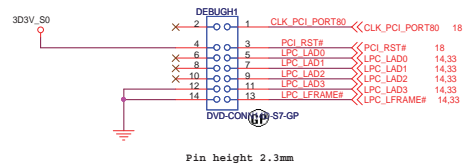
CPU_FAN



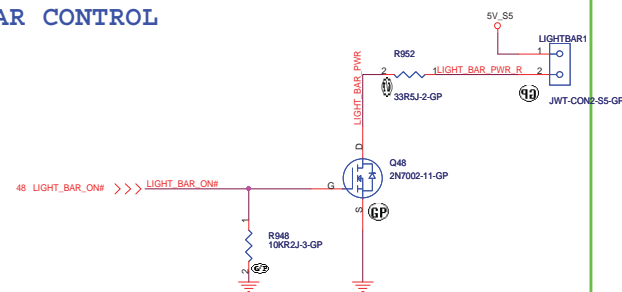
MXM_SYS_FAN



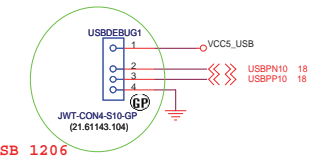
LPC DEBUG PORT



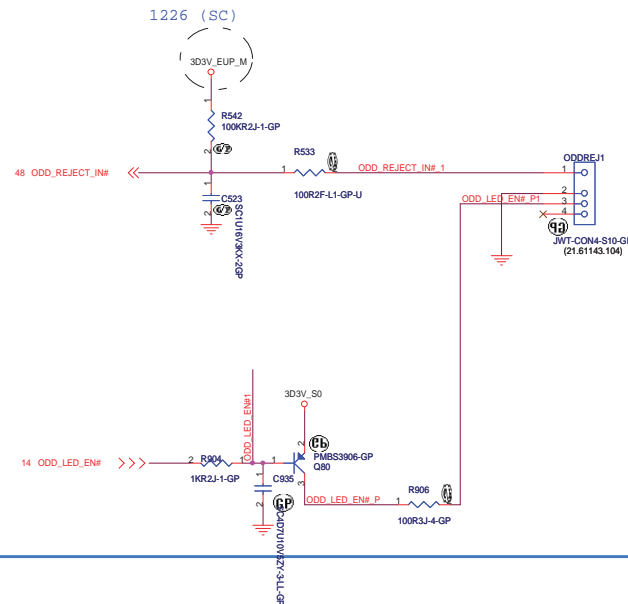
LIGHT BAR CONTROL



USB RESERVE



ODD REJECTION

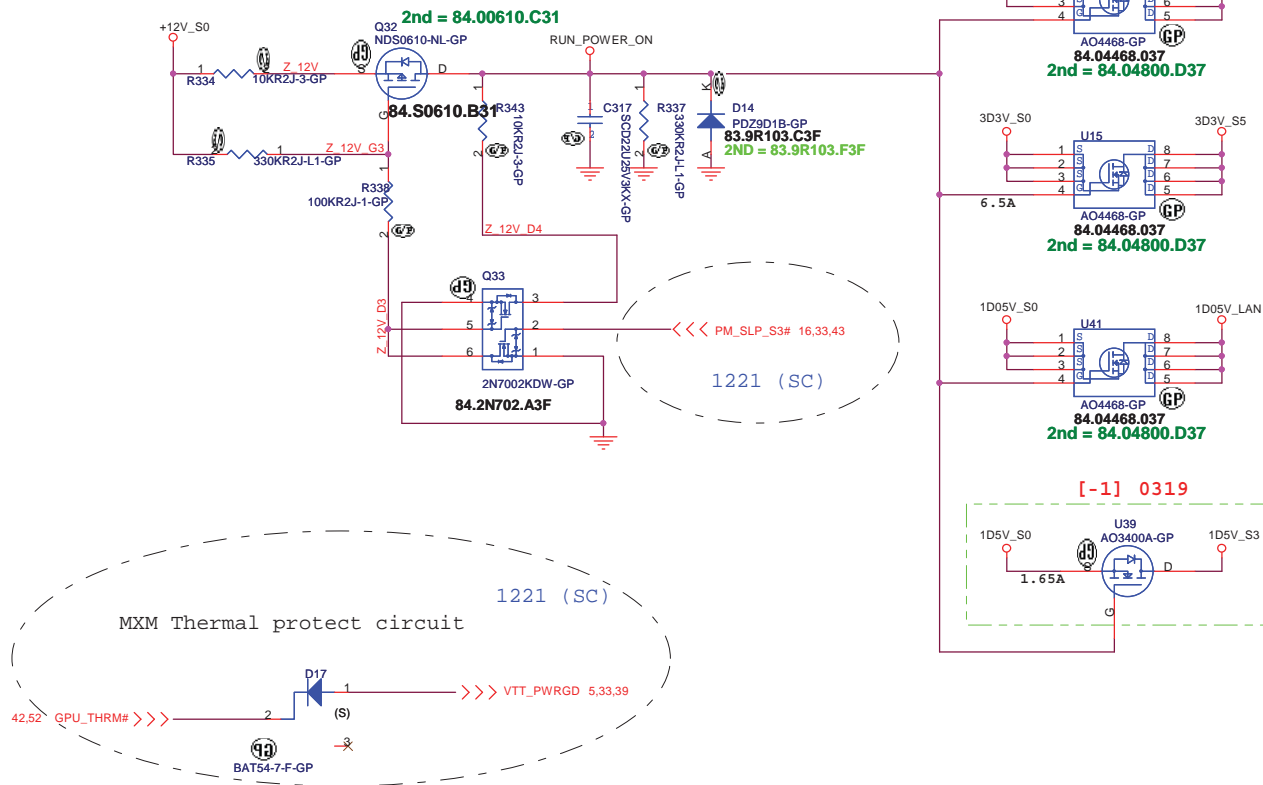


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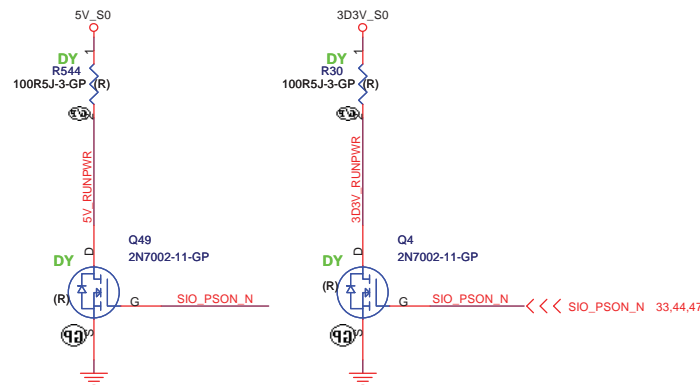
緯創資通 Wistron Corporation
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Fan control			
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C			
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Run Power



Reserved for Discharge

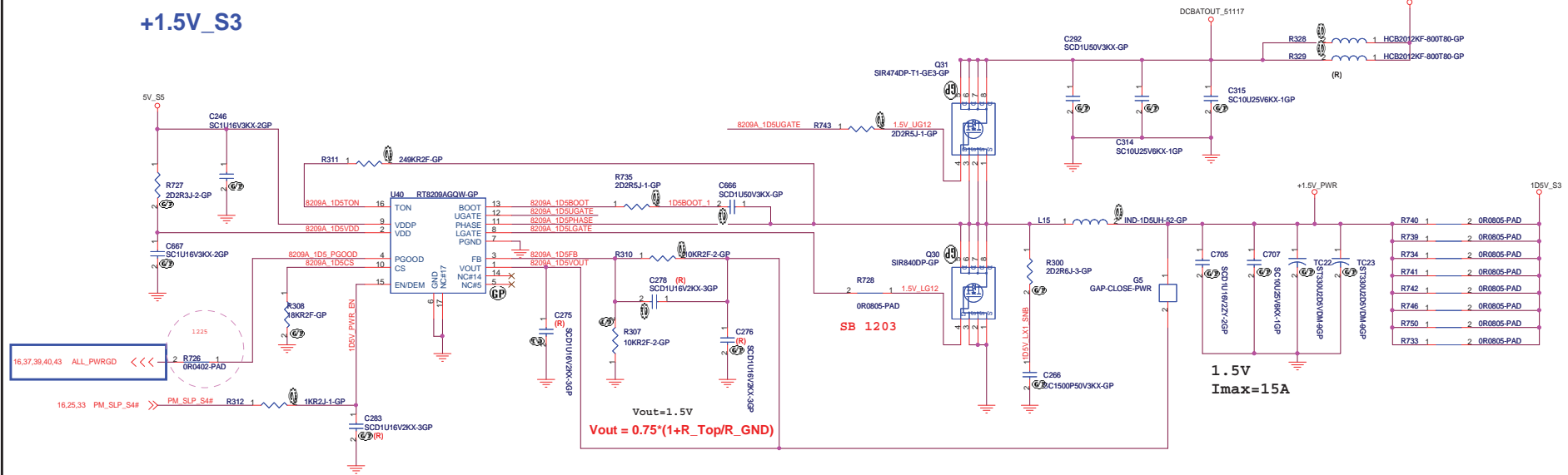


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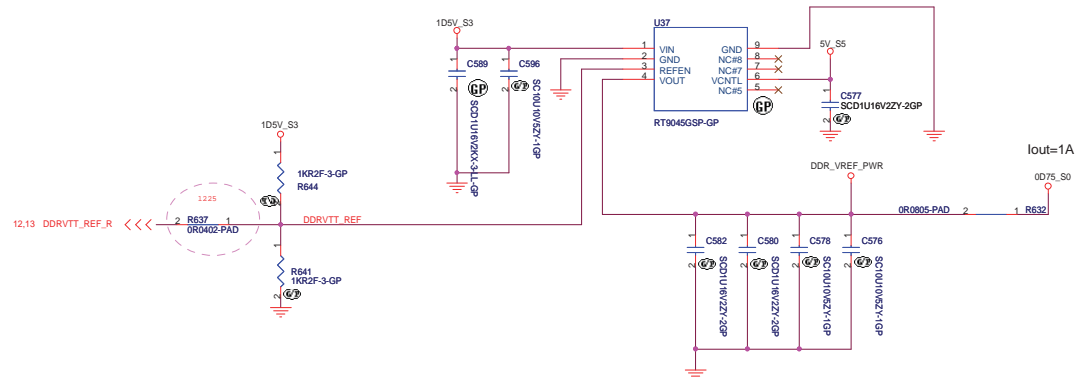
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Run Power		
Size	Document Number	Rev
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Date: Tuesday, April 06, 2010		
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+1.5V_S3



+0.75V_MEM_VTT



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

+1.5V/+0.75V

Size

e	Document Number
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Catalina

Rev

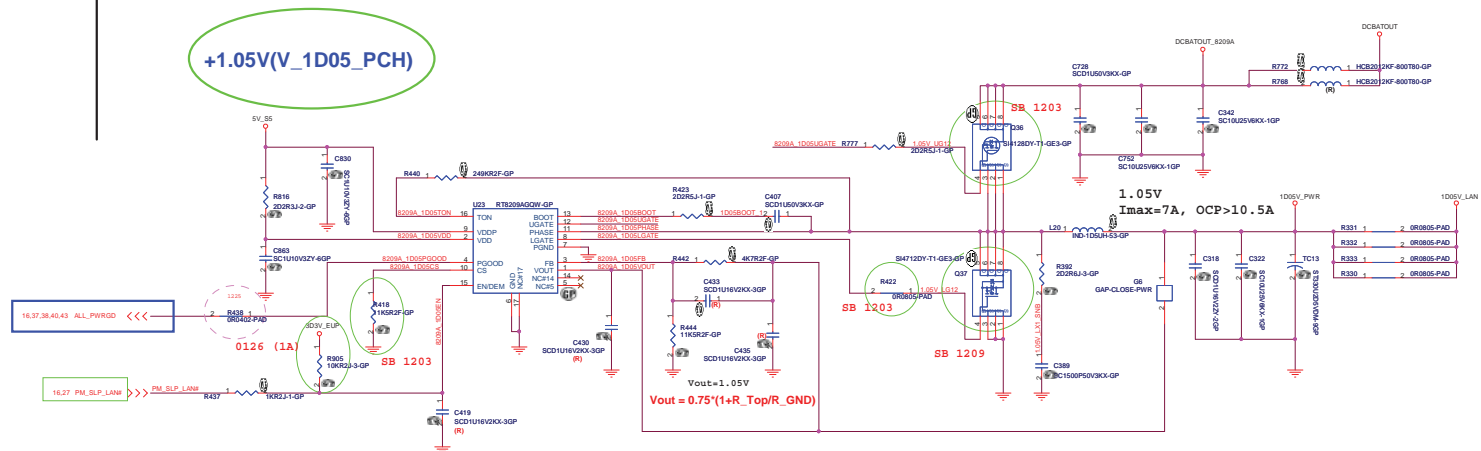
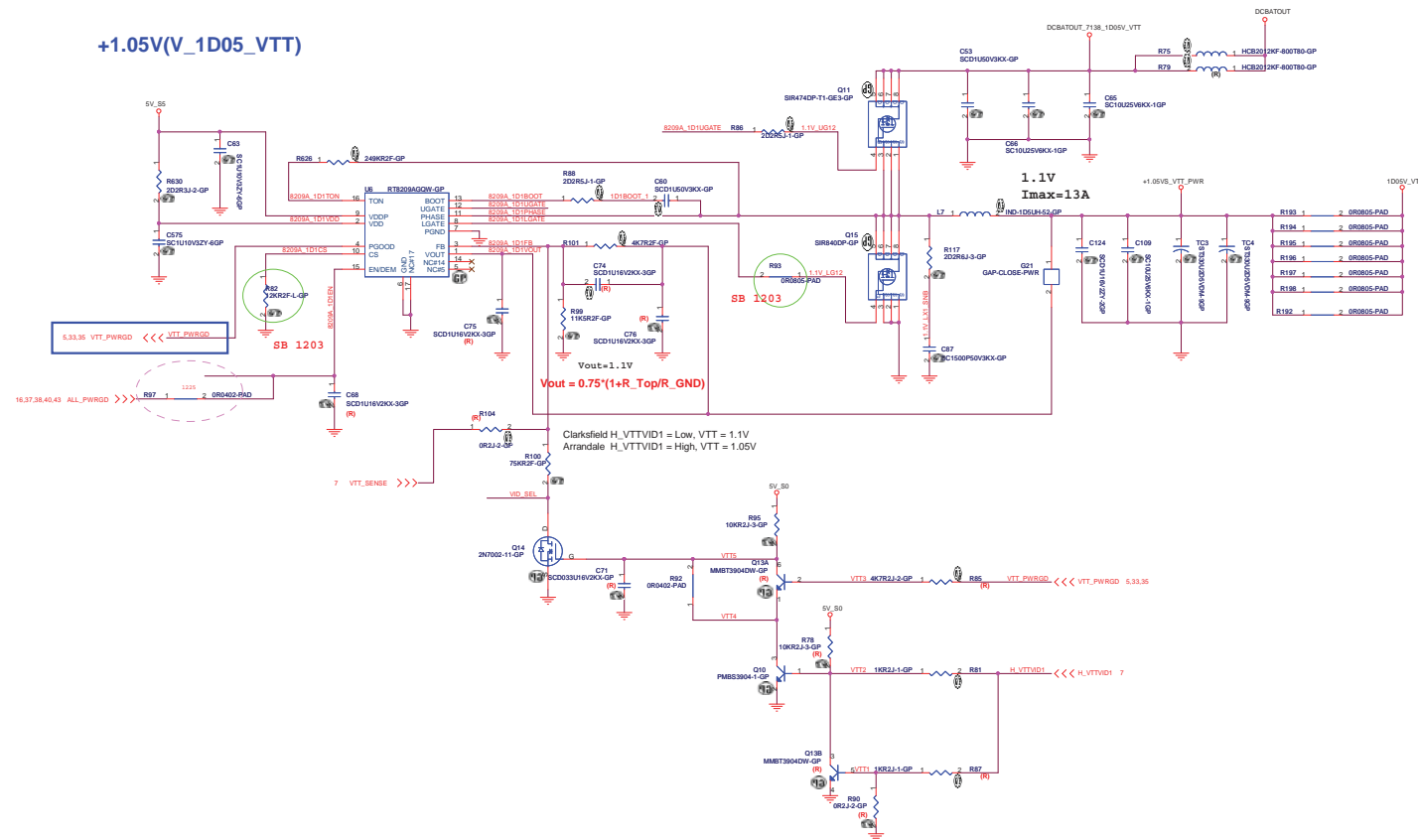
SA

Date: Tuesday, April 06, 2010

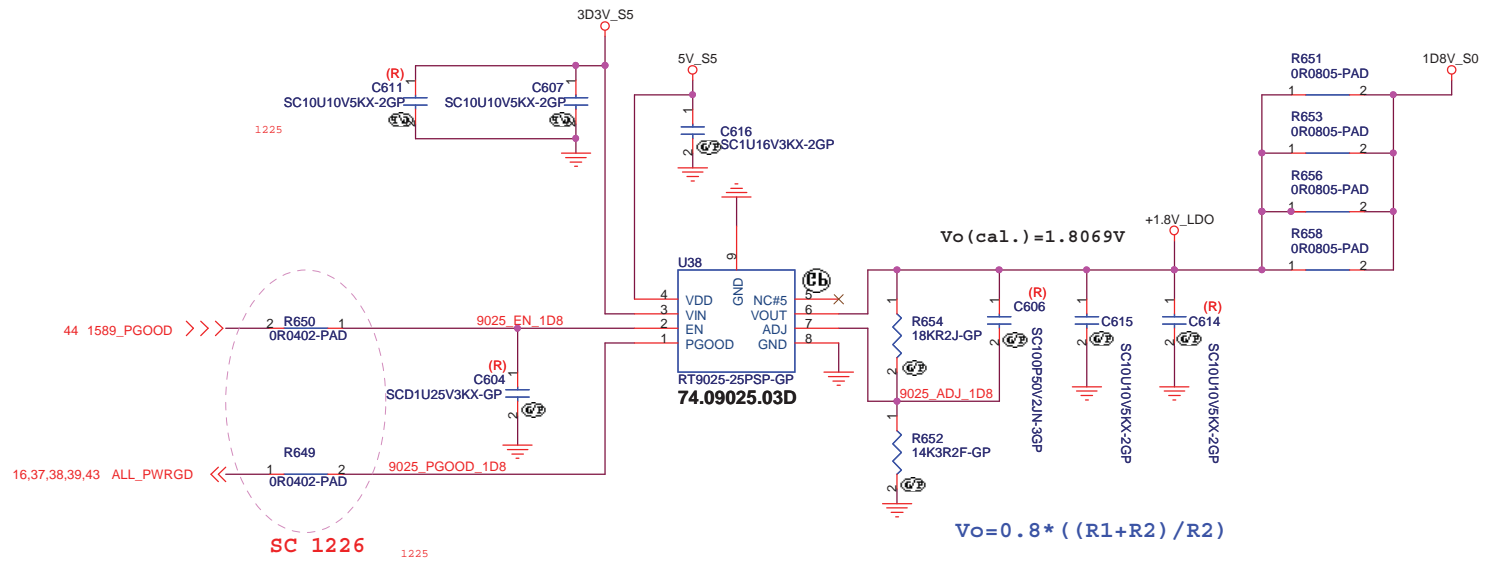
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59

59



1D8V_S0 (RT9025)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

1D8V POWER

Size
B

Document Number

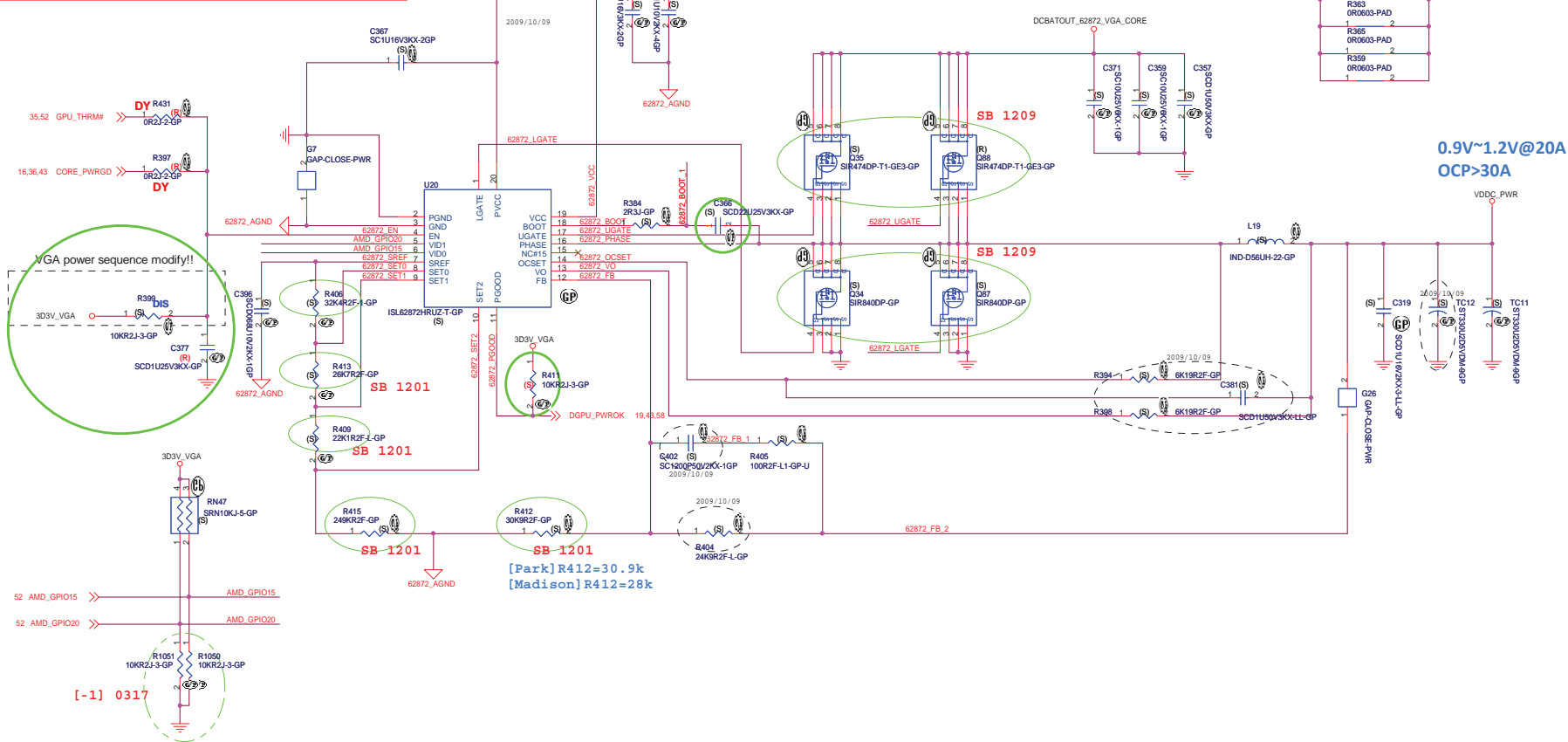
Catalina

Rev
SA

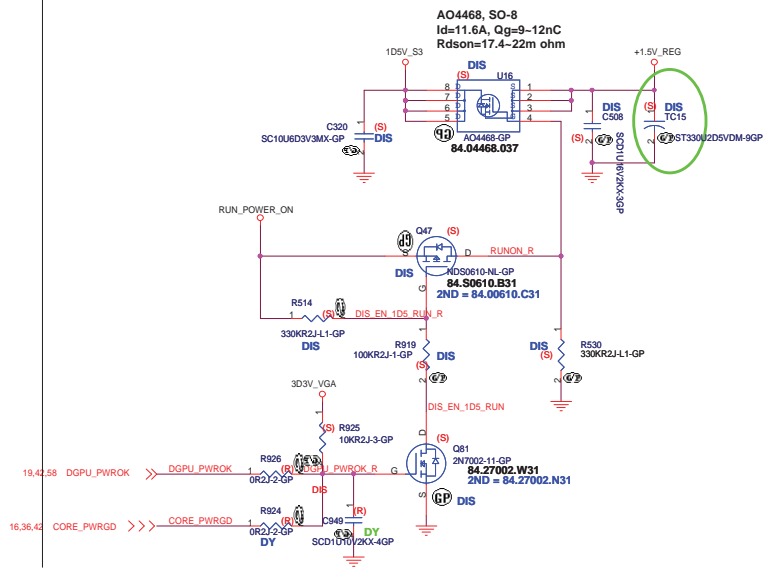
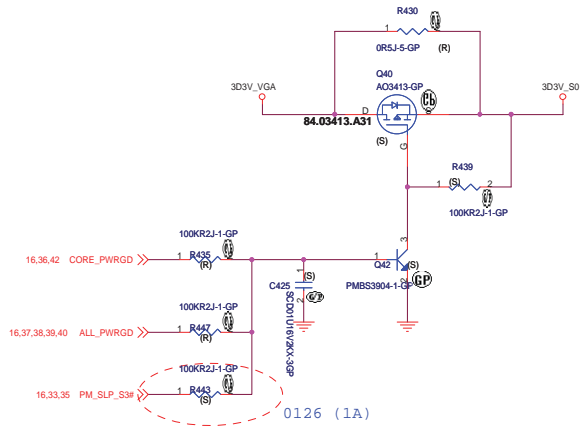
Date: Tuesday, April 06, 2010

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VID1(GPIO20)	VID0(GPIO15)	Core
0	0	1.22V
0	1	1.02V
1	0	1.12V
1	1	0.92V

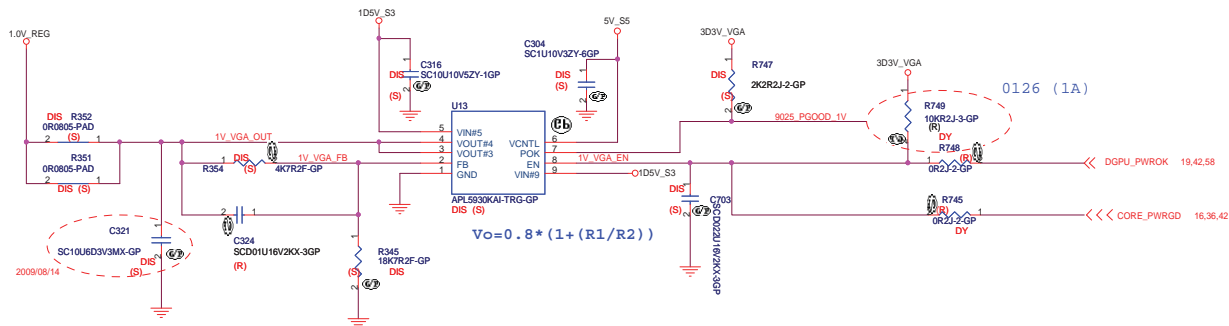


3D3V_S0 to 3D3V_DELAY Transfer



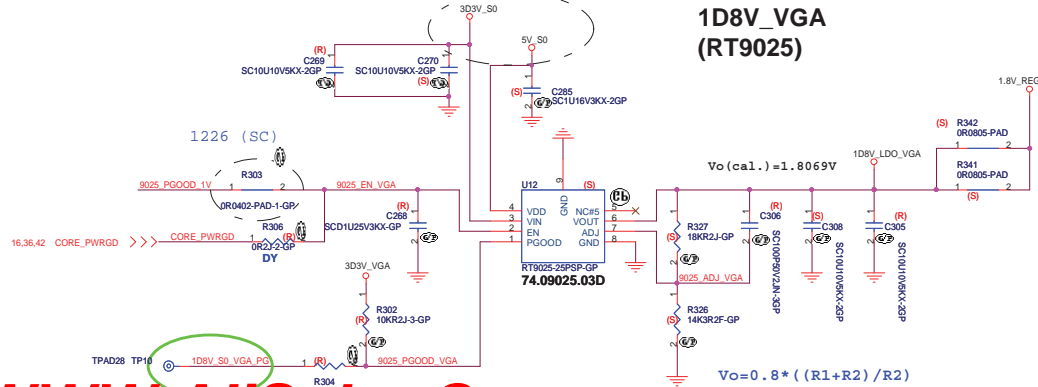
Iout=1.5A

Vout= 1V_VGA



1226 (SC)

1D8V_VGA
(RT9025)



<Core Design>

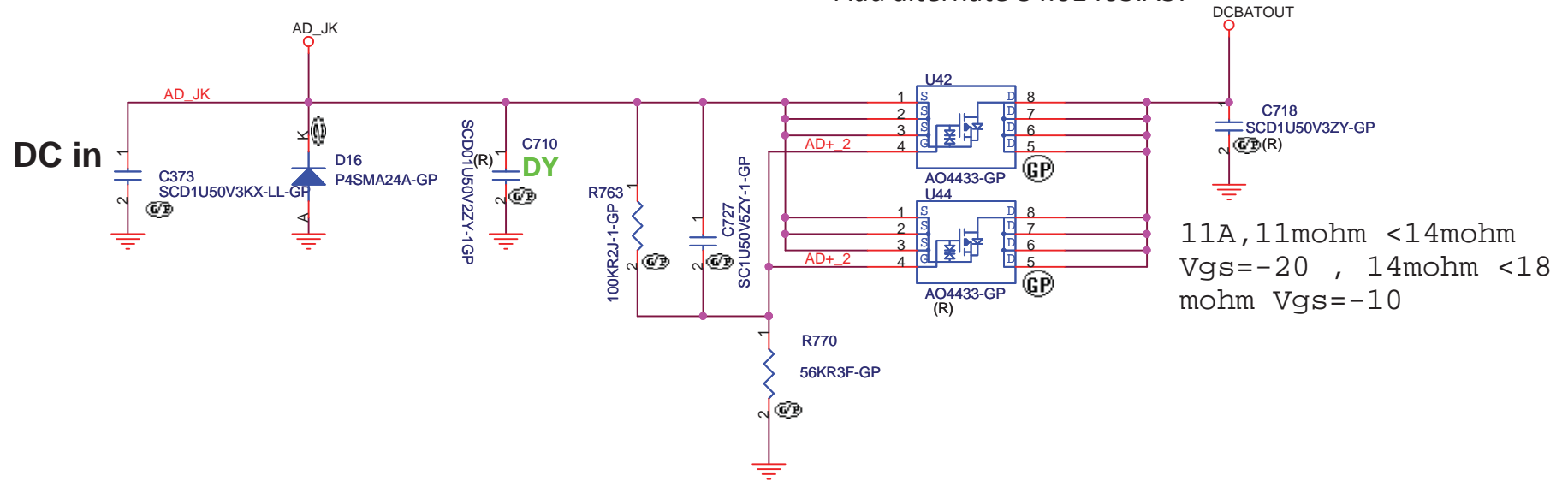
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Taipei Hsien 221, Taiwan, R.O.C.

File	1.8V_REG/1V_PCIE	Rev	SA
Size	Document Number		
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Adaptor in to generate DCBATOUT

Add alternate 84.01403.A37



<Core Design>

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Title

DC IN

Size
A4

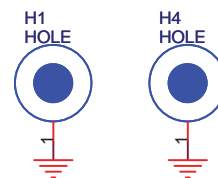
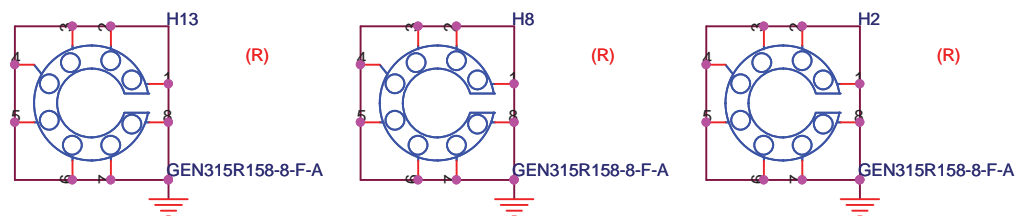
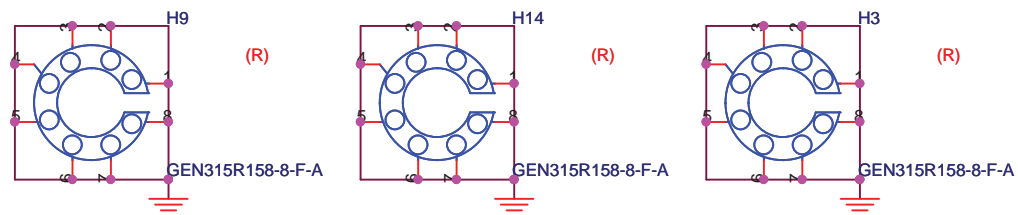
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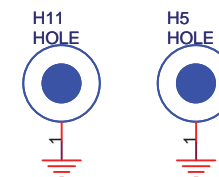
Rev
SA

Date: Tuesday, April 06, 2010

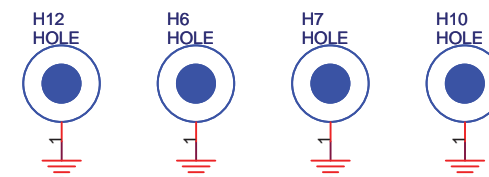
Sheet 45 of 59



Mini PCIE holder



FAN holder



<Core Design>

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Title

Screw hole

Size
A4

Document Number

Catalina

Rev

SA

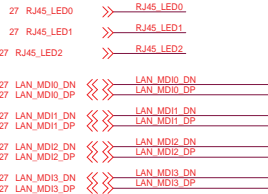
Date: Tuesday, April 06, 2010

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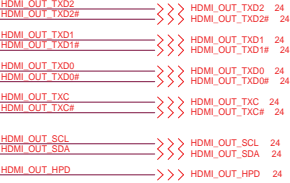
REAR USB



LAN



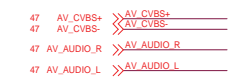
HDMI OUT



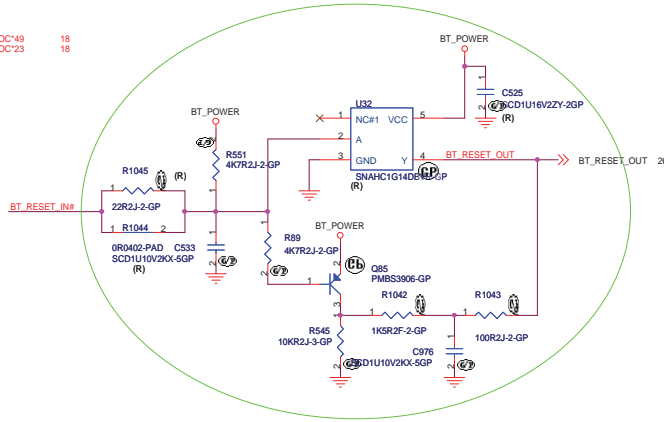
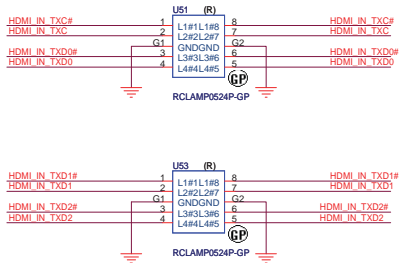
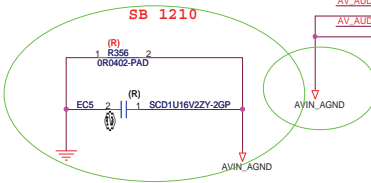
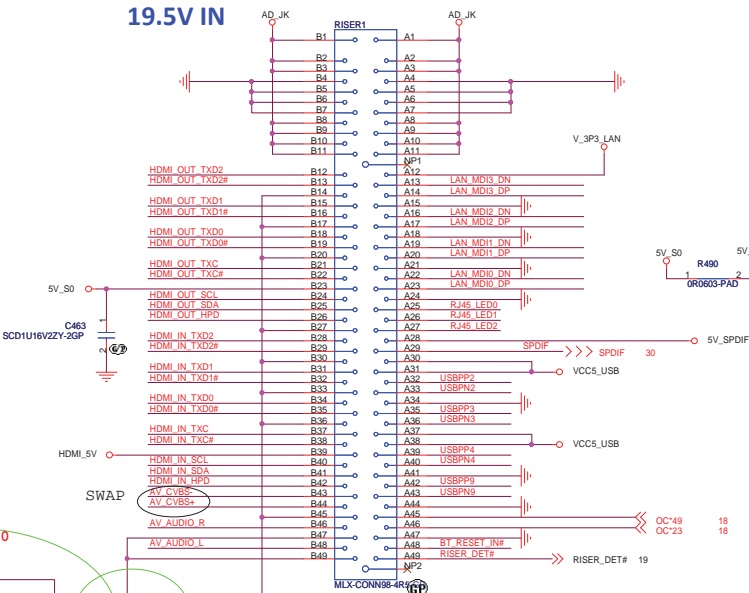
HDMI IN



AV IN



19.5V IN



0126 (1A)

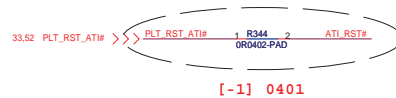
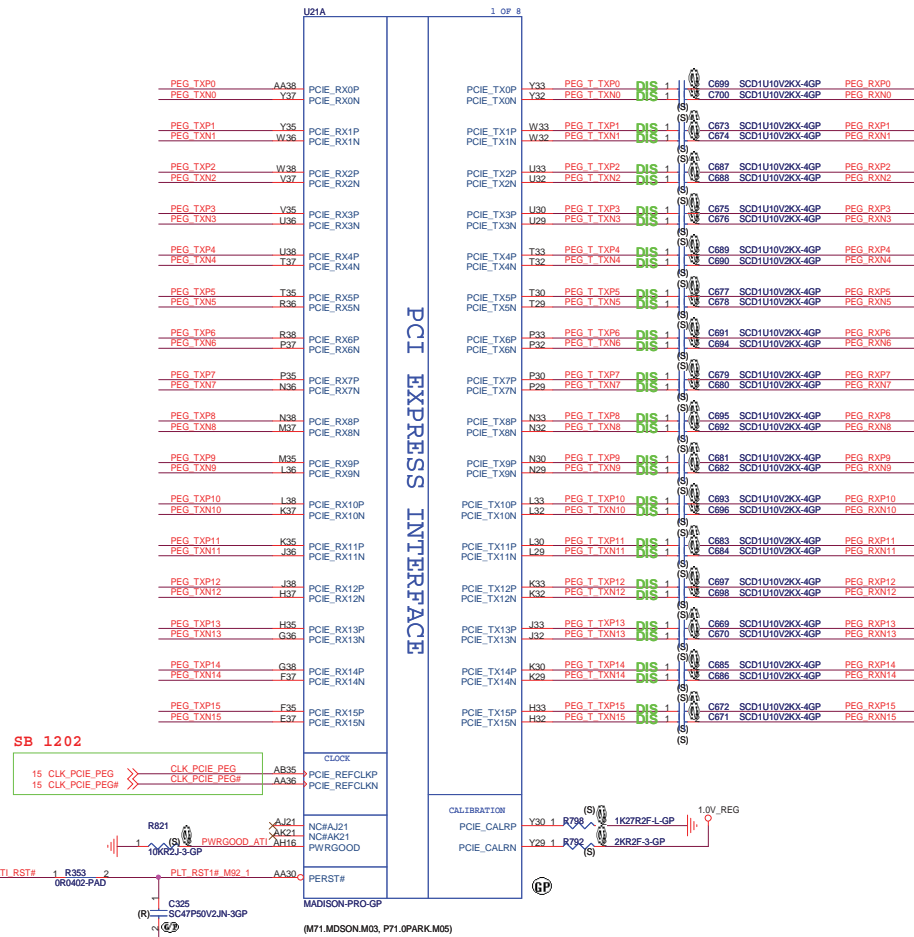
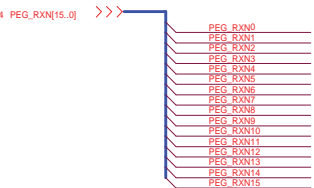
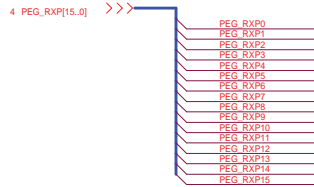
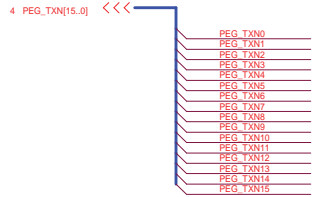
POWER REGULATORS		
+3.3V 190 mA	VDDR3	60 mA
	A2VDD	130 mA
+0.95/+1V 33 A	VDDC	29 A
	VDDCI	4 A
+1.5V	VDDR1	TBD
	MVDDQ/C	
+1.8V 1.384 A	VDD_CT	17 mA
	DP[F:A]_PVDD	20 mA
	DP[D:A]_VDD18	130 mA
	DP[F:E]_VDD18	130 mA
	SPV18	50 mA
	MPV18	150 mA
	DPLL_PVDD	75 mA
	PCIE_PVDD	40 mA
	PCIE_VDDR	400 mA
	TSVDD	5 mA
	VDDR4	
	AVDD	TBD
	VDD1DI	70 mA
	VDD2DI	45 mA
	VDD2DI	50 mA
	A2VDDQ	1.5 mA
+1.0V 1.42 A	DP[D:A]_VDD10	110 mA
	DP[F:E]_VDD10	110 mA
	SPV10	100 mA
	DPLL_VDDC	
	PCIE_VDDC	1.1 A

<Core Design>

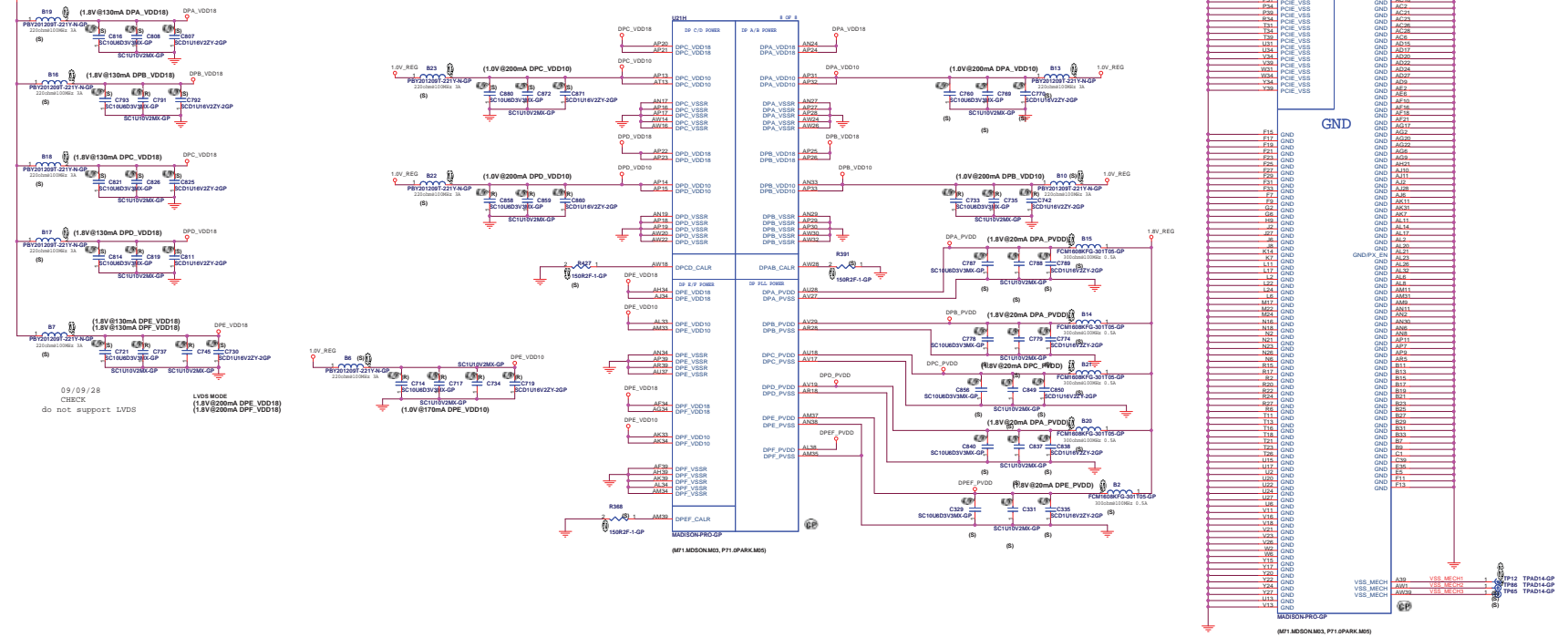
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
ATI Power rail			
Size	Document Number		Rev
C	Catalina		SA
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Diagram illustrating the connection of the PEG_TXP[15..0] bus to individual PEG_TXP signals. The bus is shown on the left, and the individual signals are listed on the right, connected by a vertical line.

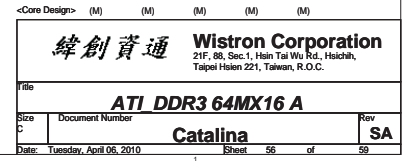
- PEG_TXP0
- PEG_TXP1
- PEG_TXP2
- PEG_TXP3
- PEG_TXP4
- PEG_TXP5
- PEG_TXP6
- PEG_TXP7
- PEG_TXP8
- PEG_TXP9
- PEG_TXP10
- PEG_TXP11
- PEG_TXP12
- PEG_TXP13
- PEG_TXP14
- PEG_TXP15




```
09/09/28
For dual-link TMDS, the associated power supply rails can
share the filters/decoupling capacitors.
we use single HDMI, share or ?
need check!
```

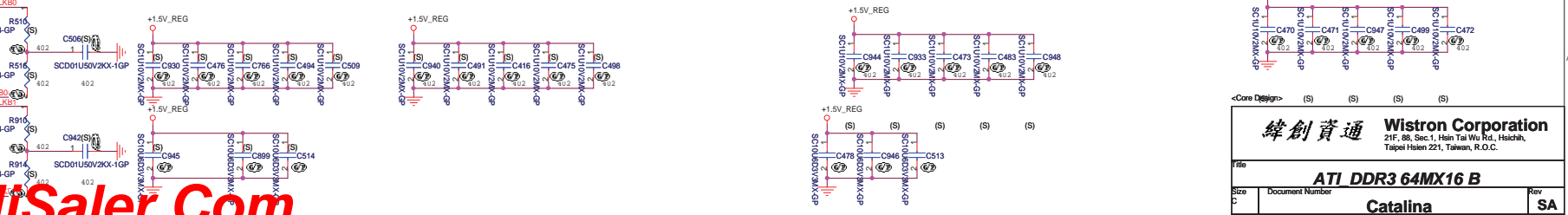
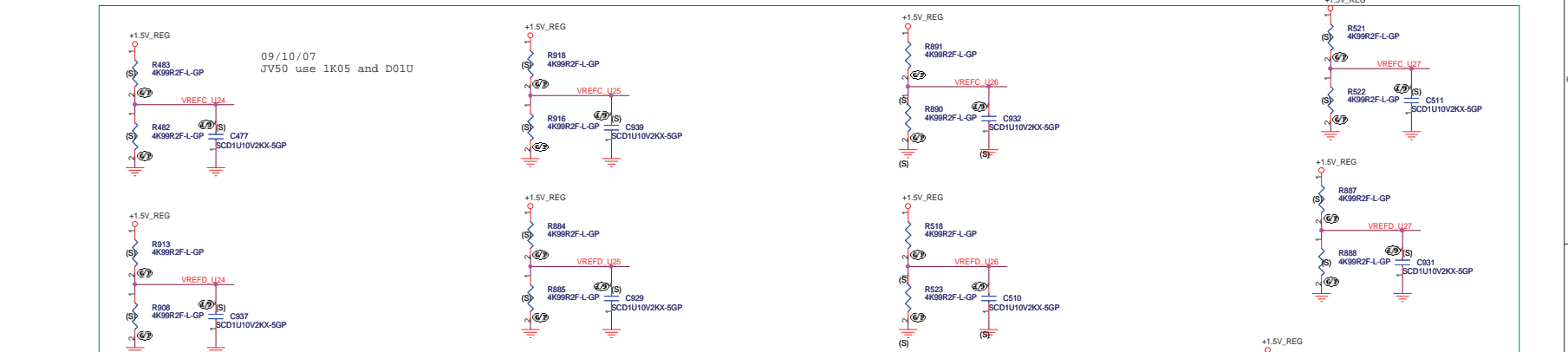
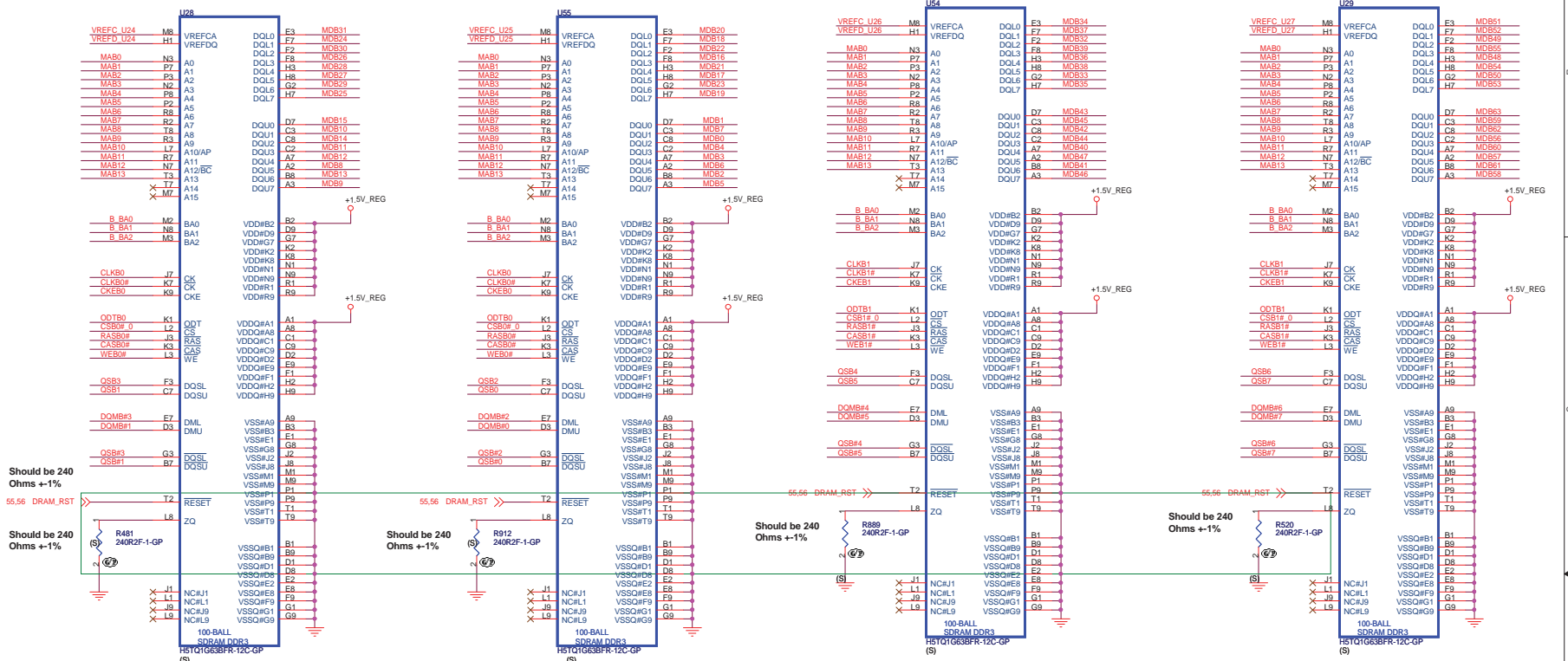


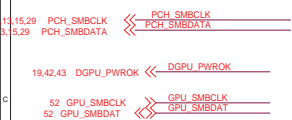

```
72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12
```



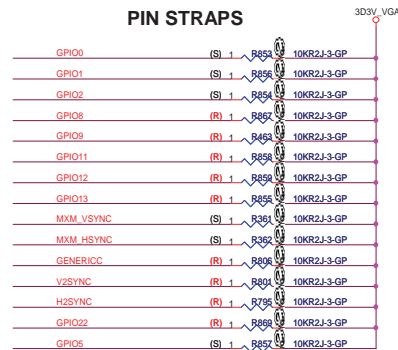
CHANNEL B: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.HOU gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12





PIN STRAPS



	Manufacturer	Part Number	Size	CONFIG[2]
STRAP	ST Microelectronics	M25P05A	512 kbit	100

		MSYNC
		VSYNC
STRAP	Audio for both DisplayPort and HDMI.	11
	Audio for DisplayPort and HDMI if dongle is detected	10

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[3:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	1 0 0
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERIC0C		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSNC	Audio function present	1

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERIC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO_28_TDO	GPIO21_BB_EN

