

JIWA3/A4

Compal Confidential

Schematics Document

Mobile Penryn uFCPGA

Intel Cantiga_GM/PM+ICH9-M

Wednesday, May 14, 2008

REV:1.0

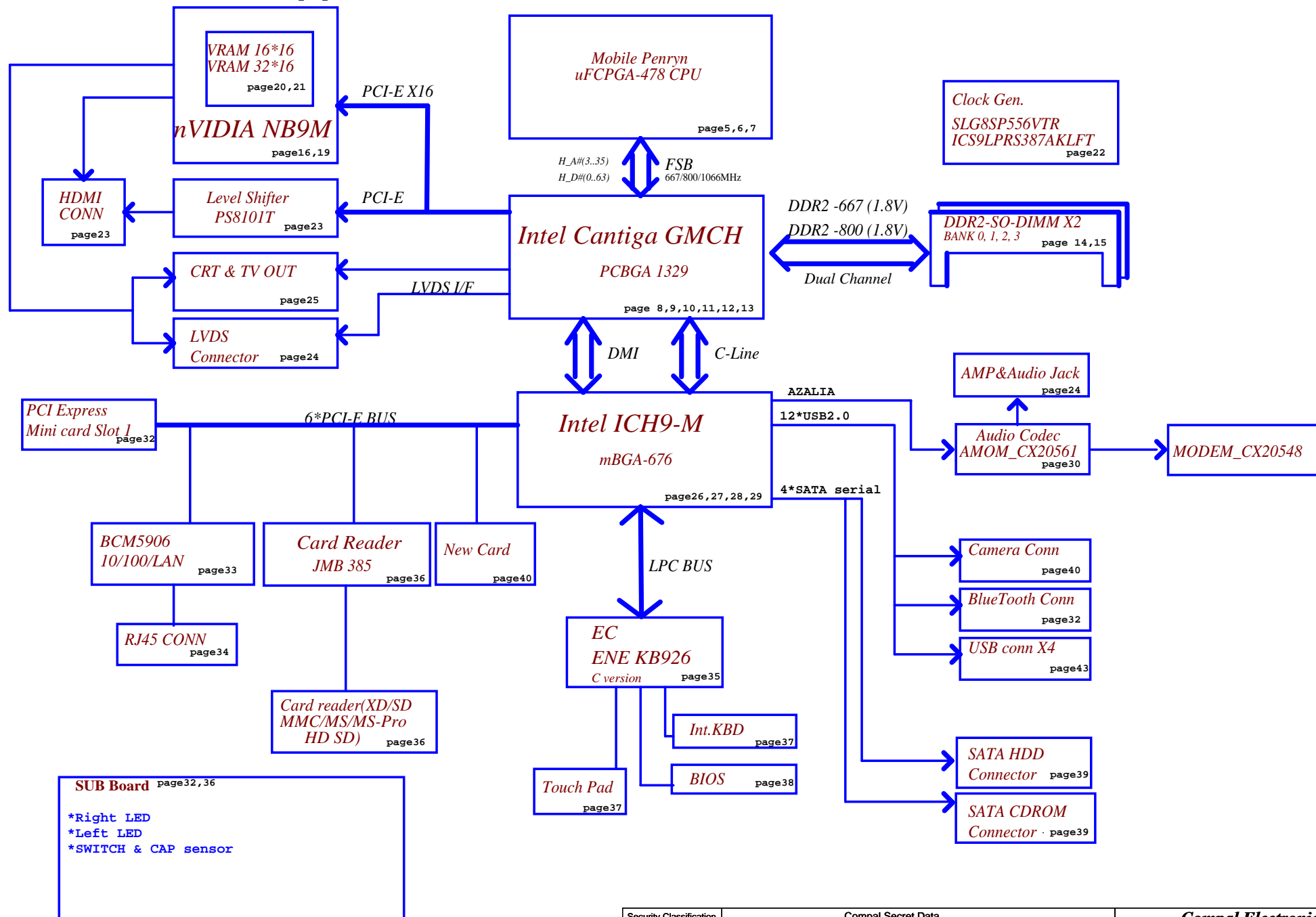
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	Cover Sheet	
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ZZZ1
15W_PCB_LA4212P

Right LED Board

Switch & CAP SENSE LEDs Board

Left LED Board



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM@
GM@
X76@
CARD@
WLAN@
HDMI@
HDMI_PM@
HDMI_GM@
BT@

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD	CAP BRD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	V
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V	X

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
	(V)	GDDR3	DDR2	GDDR3	DDR2
NVVD	Variable	12.68A	11.57A	10.52A	9.59A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1400mA			
PEX_PLLVDD	1.1	110mA			
PLLVD	1.1	65mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.225A			
FBVDD/Q	1.8	3080mA	1720mA	3010mA	1680mA
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	3.6A	2.24A	3.53A	2.2A
DACA_VDD	3.3	130mA			
DACB_VDD	3.3	255mA			
DACC_VDD	3.3	130mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	110mA			
TOTAL	3.3	0.645A			

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

POWER SEQUENCE

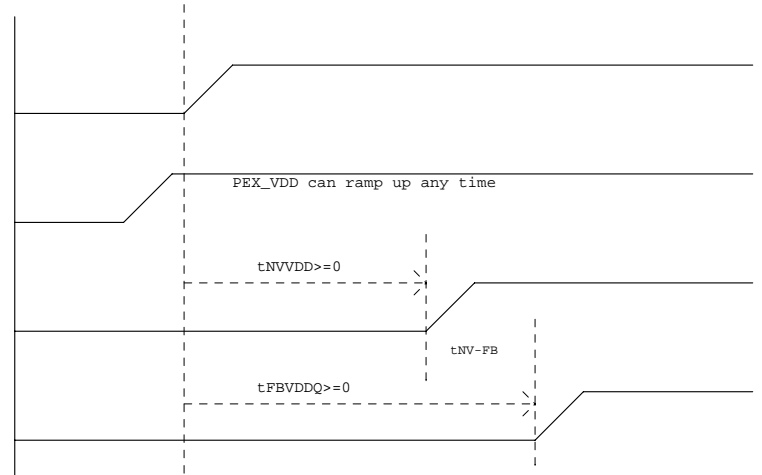
The ramp time for any rail must be more than 40us

(+3VS) VDD33

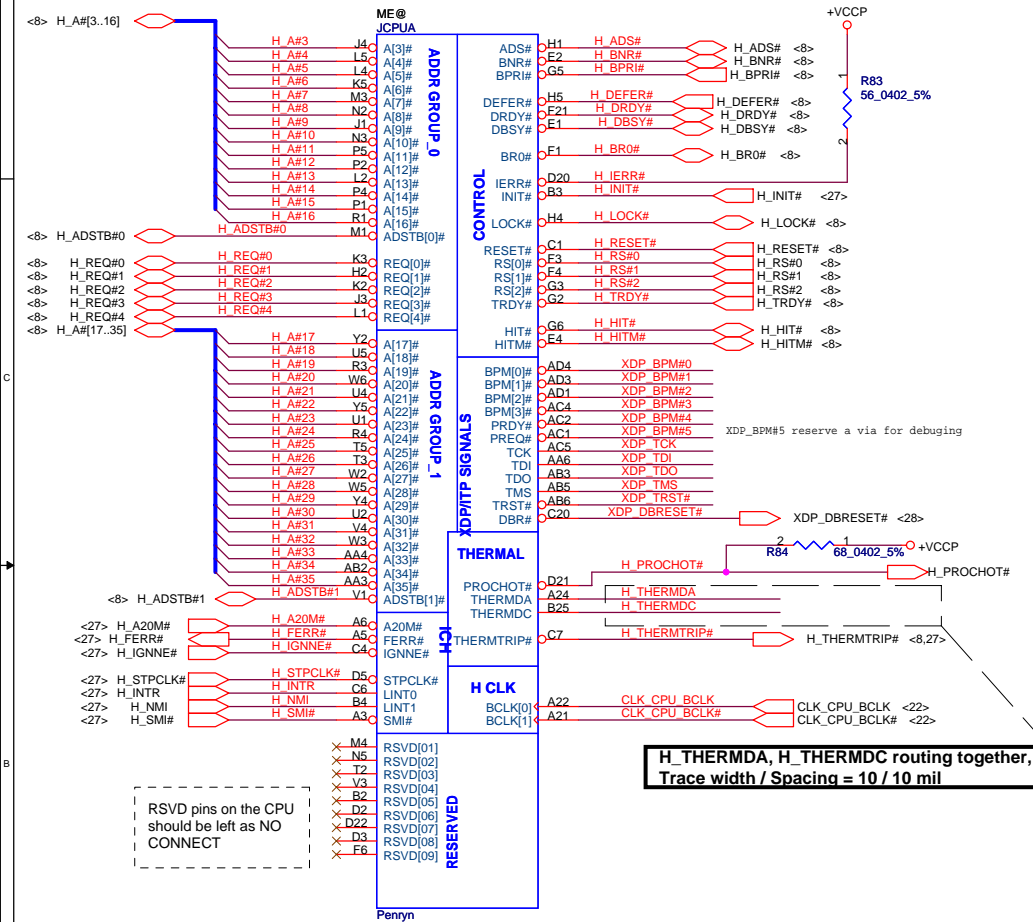
(1.1VS) PEX_VDD

(+VGA_CORE) NVVD

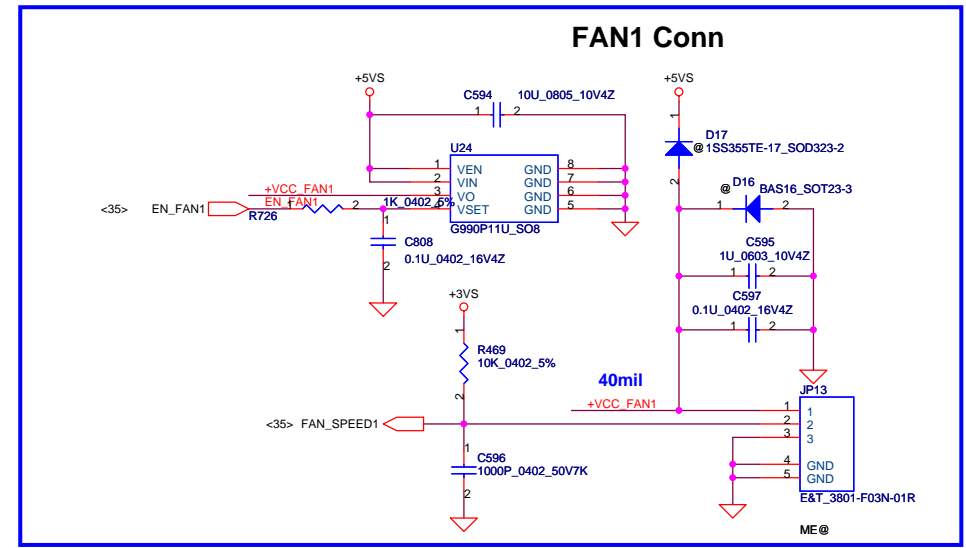
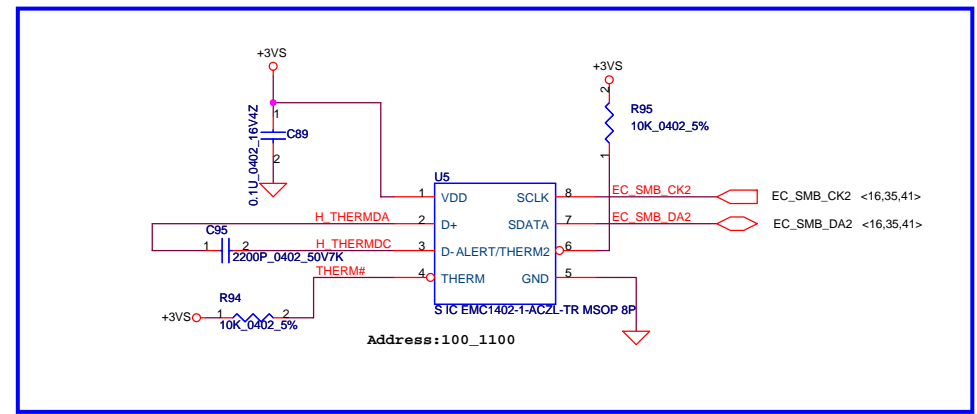
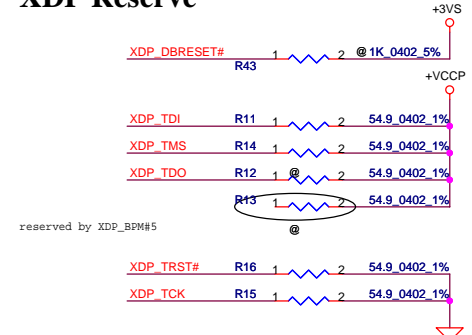
(1.8VS) FBVDDQ



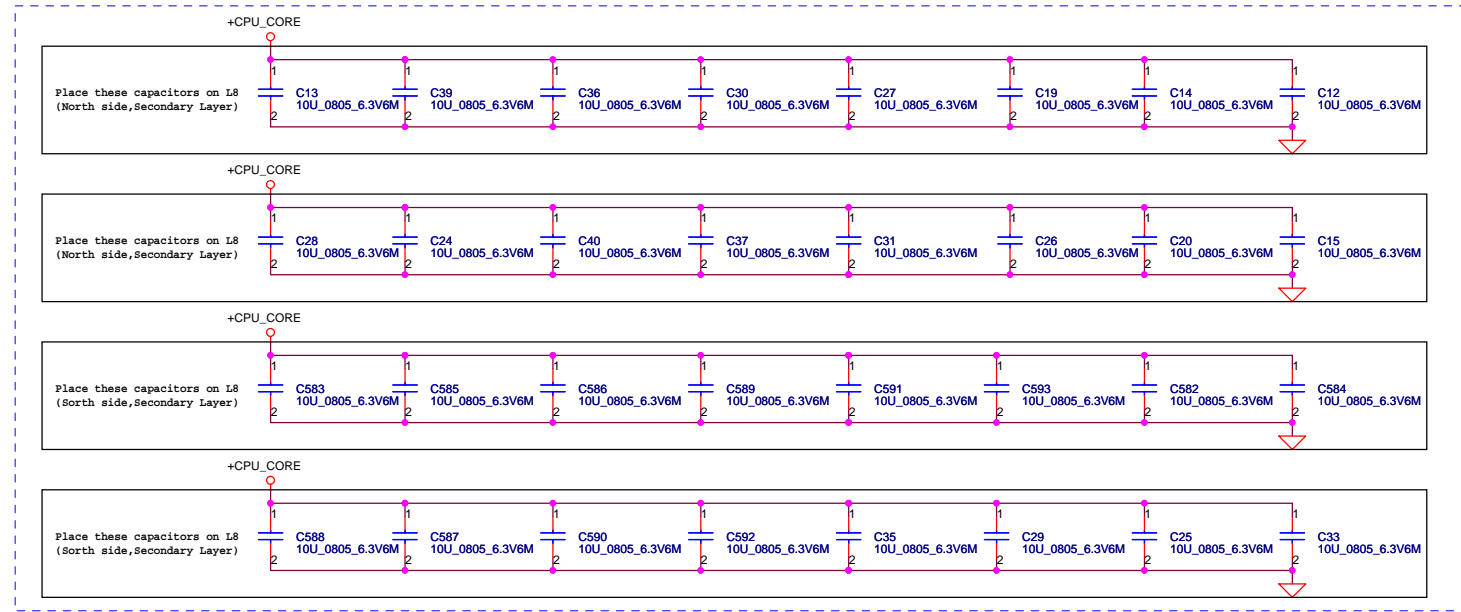
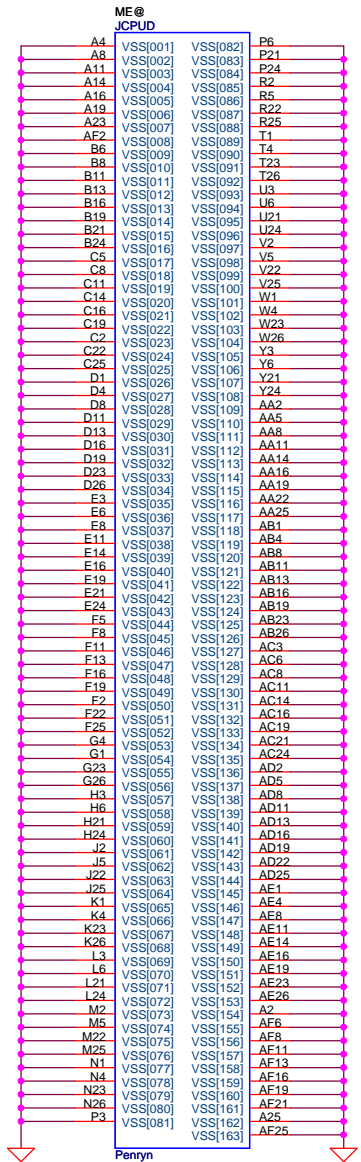
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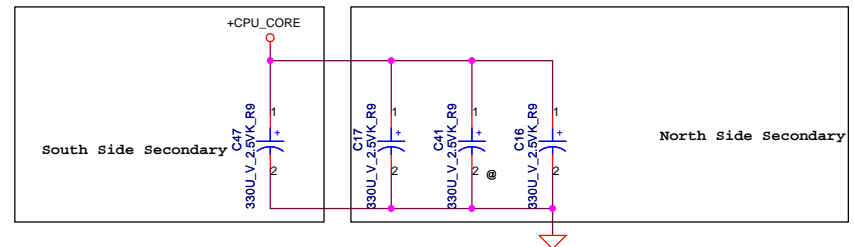
XDP Reserve



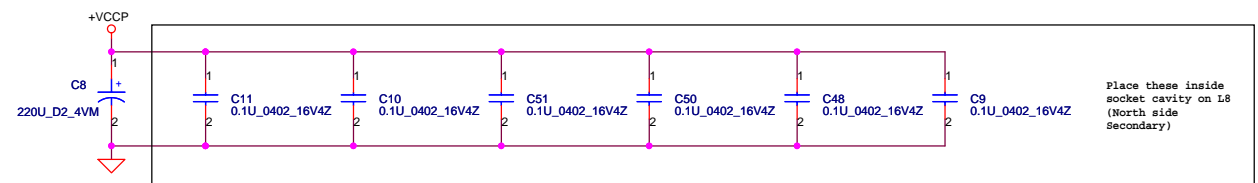
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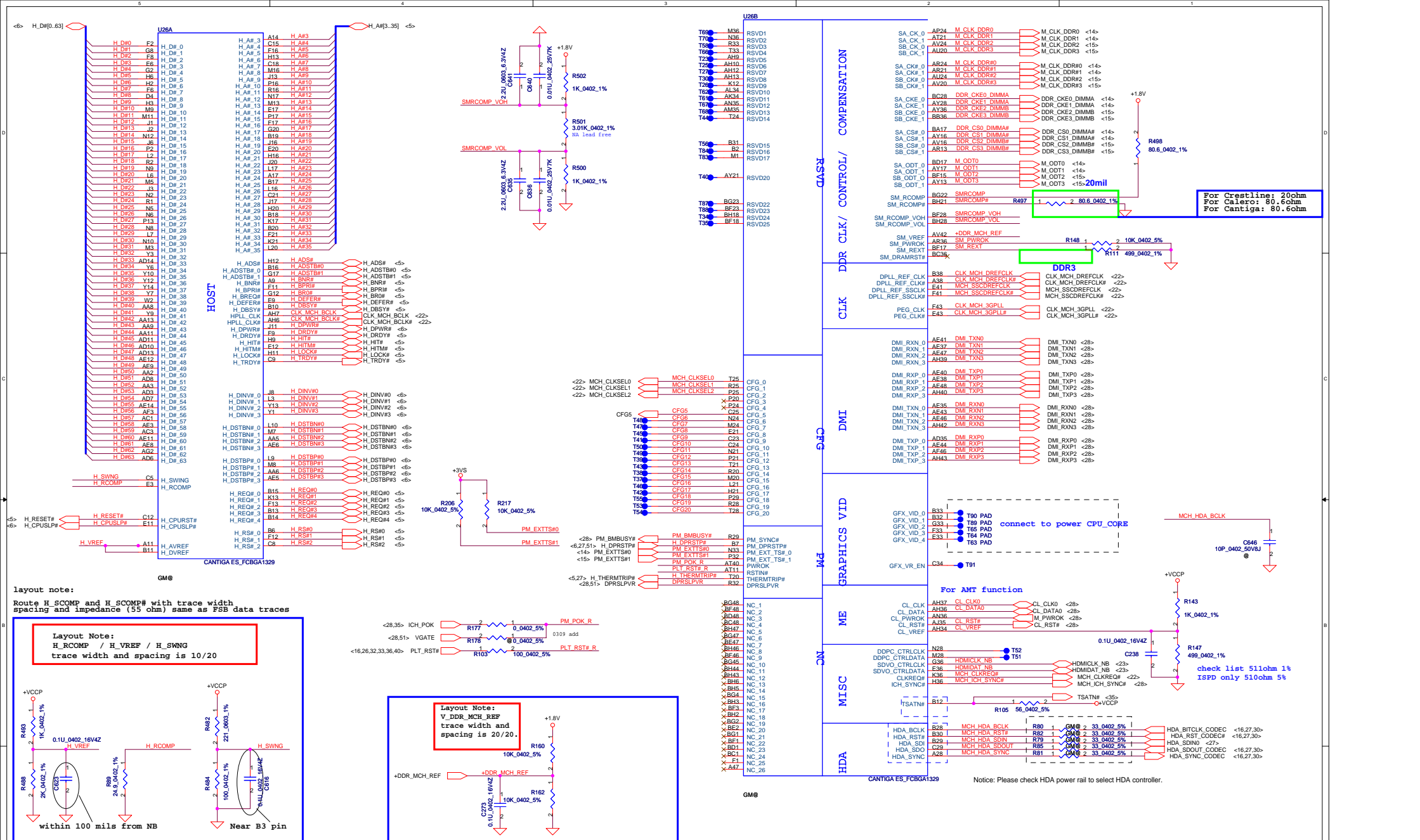


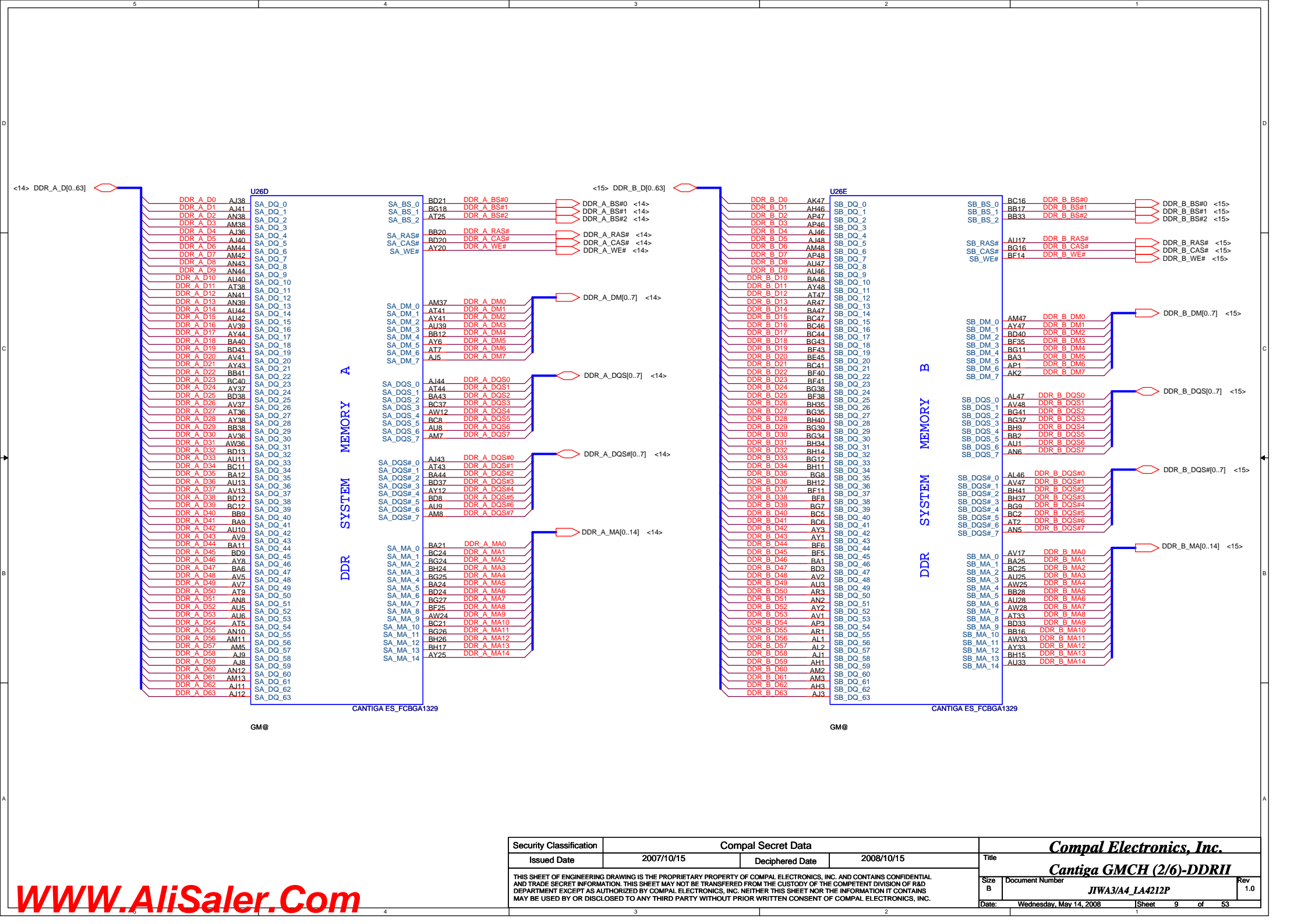
Mid Frequency Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

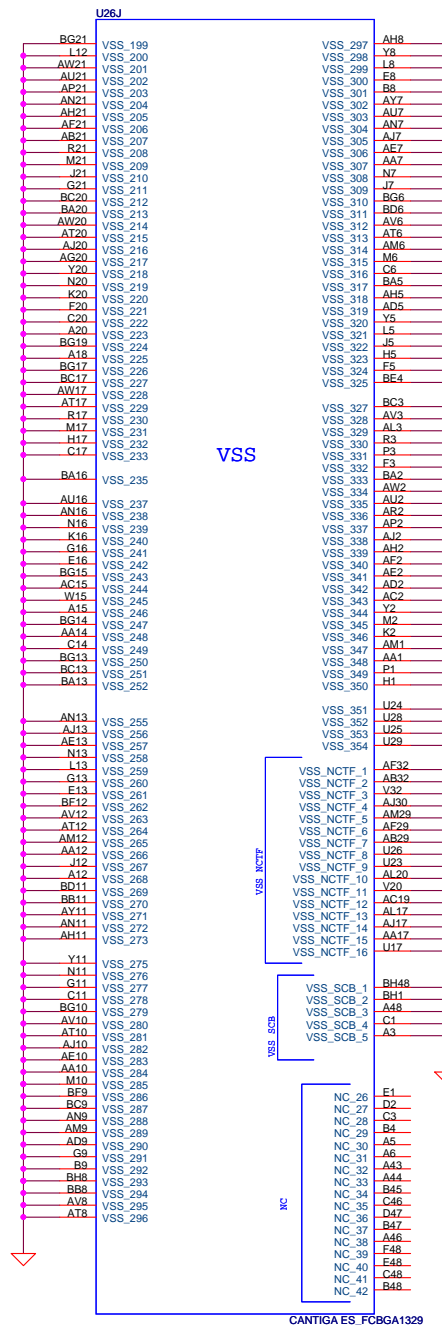
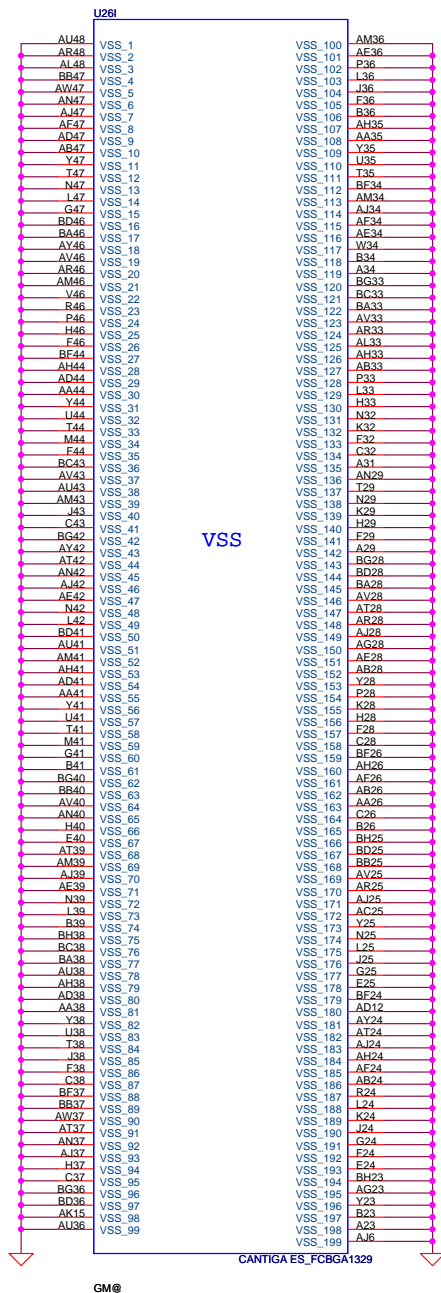








Compal Electronics, Inc.			
Title			
Crestline GMCH (5/6)-VCC			
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<9> DDR_B_DQS#[0..7]

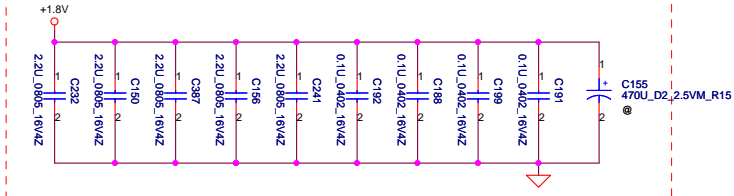
<9> DDR_B_D[0..63]

<9> DDR_B_DM[0..7]

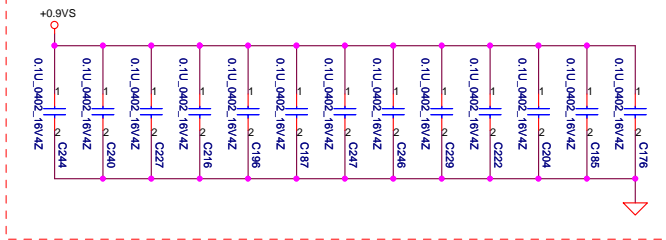
<9> DDR_B_DQS[0..7]

<9> DDR_B_MA[0..13]

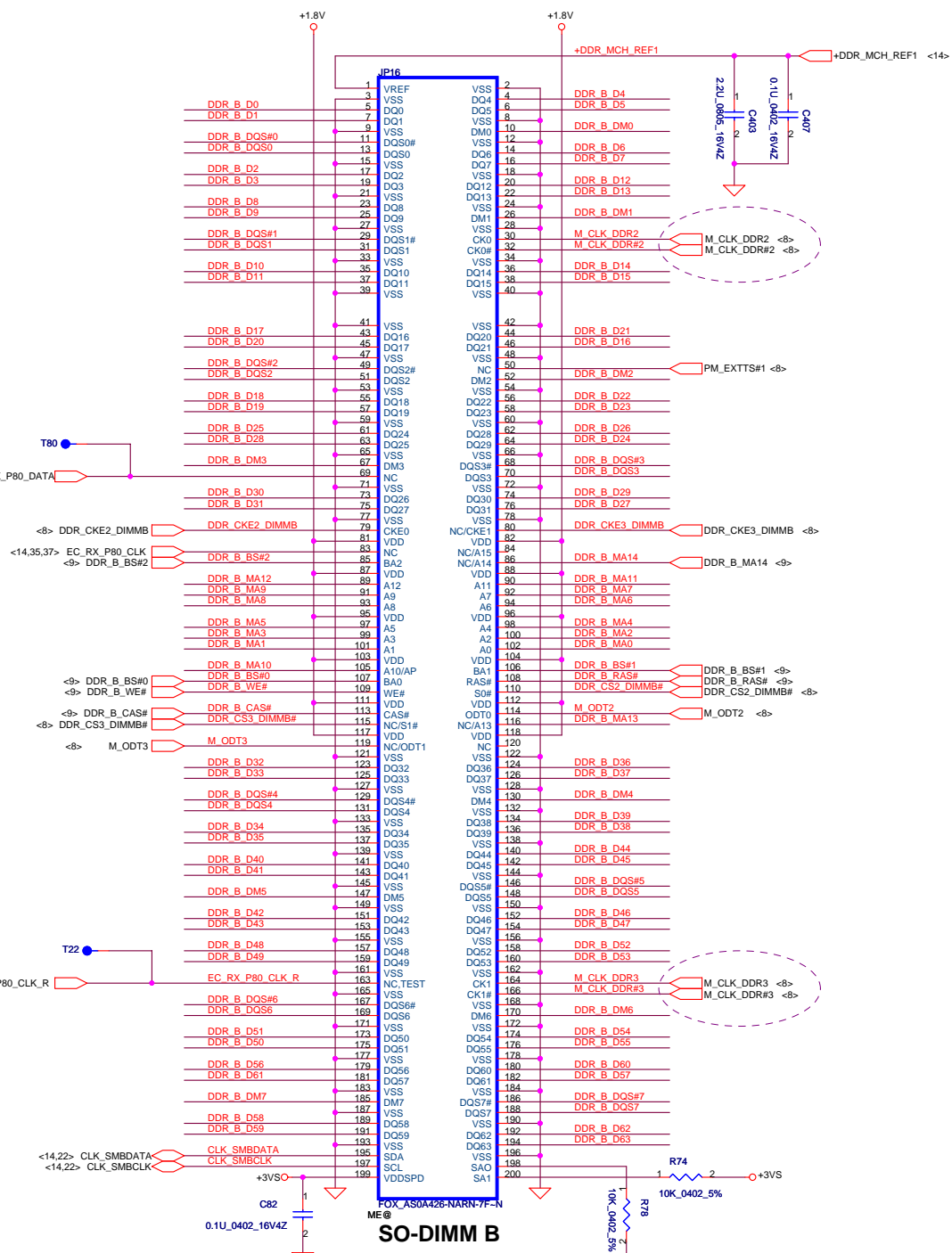
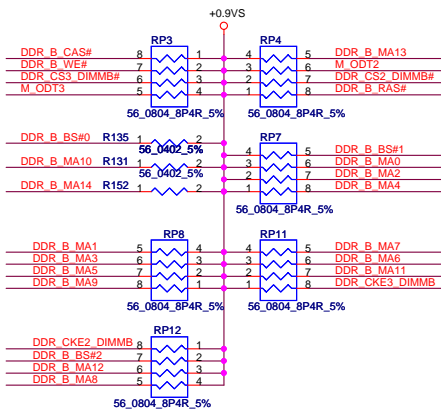
Layout Note:
Place near JP42



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



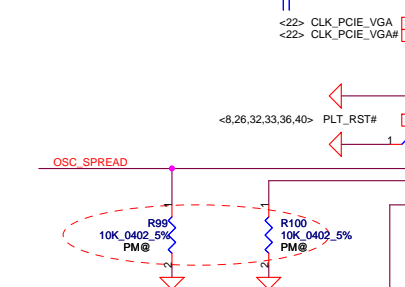
Layout Note:
Place these resistor closely JP42, all trace length Max="1.5"



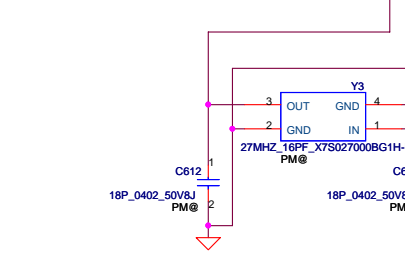
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<10> PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
<10> PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
<10> PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
<10> PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

PCIE_GTX_C_MRX_P0 C261 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N0 C260 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P1 C294 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N1 C293 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P2 C259 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N2 C258 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P3 C292 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N3 C291 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P4 C257 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N4 C256 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P5 C290 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N5 C289 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P6 C255 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N6 C254 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P7 C287 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N7 C288 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P8 C253 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N8 C252 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P9 C285 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N9 C286 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P10 C251 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N10 C250 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P11 C284 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N11 C283 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P12 C249 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N12 C248 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P13 C282 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N13 C281 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P14 C267 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N14 C266 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_P15 C280 PM@ 1 2 0.1U_0402_10V7K
PCIE_GTX_C_MRX_N15 C279 PM@ 1 2 0.1U_0402_10V7K



If External Spread Spectrum not stuff than stuff resistor

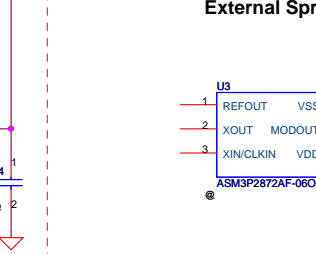


U27A
PCIE_MTX_C_GRX_P0 AE12
PCIE_MTX_C_GRX_N0 AE12
PCIE_MTX_C_GRX_P1 AG12
PCIE_MTX_C_GRX_N1 AG12
PCIE_MTX_C_GRX_P2 AE13
PCIE_MTX_C_GRX_N2 AE13
PCIE_MTX_C_GRX_P3 AE15
PCIE_MTX_C_GRX_N3 AE15
PCIE_MTX_C_GRX_P4 AG15
PCIE_MTX_C_GRX_N4 AG15
PCIE_MTX_C_GRX_P5 AE16
PCIE_MTX_C_GRX_N5 AE16
PCIE_MTX_C_GRX_P6 AE18
PCIE_MTX_C_GRX_N6 AE18
PCIE_MTX_C_GRX_P7 AG18
PCIE_MTX_C_GRX_N7 AG18
PCIE_MTX_C_GRX_P8 AE19
PCIE_MTX_C_GRX_N8 AE19
PCIE_MTX_C_GRX_P9 AE21
PCIE_MTX_C_GRX_N9 AE21
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PCIE_MTX_C_GRX_N11 AE22
PCIE_MTX_C_GRX_P12 AE24
PCIE_MTX_C_GRX_N12 AE24
PCIE_MTX_C_GRX_P13 AG24
PCIE_MTX_C_GRX_N13 AG24
PCIE_MTX_C_GRX_P14 AE25
PCIE_MTX_C_GRX_N14 AE25
PCIE_MTX_C_GRX_P15 AE27
PCIE_MTX_C_GRX_N15 AE27

PCIE_GTX_MRX_P0 AD10
PCIE_GTX_MRX_N0 AD10
PCIE_GTX_MRX_P1 AD12
PCIE_GTX_MRX_N1 AD12
PCIE_GTX_MRX_P2 AB11
PCIE_GTX_MRX_N2 AB11
PCIE_GTX_MRX_P3 AD13
PCIE_GTX_MRX_N3 AD13
PCIE_GTX_MRX_P4 AD15
PCIE_GTX_MRX_N4 AD15
PCIE_GTX_MRX_P5 AB14
PCIE_GTX_MRX_N5 AB14
PCIE_GTX_MRX_P6 AC18
PCIE_GTX_MRX_N6 AC18
PCIE_GTX_MRX_P7 AD17
PCIE_GTX_MRX_N7 AD17
PCIE_GTX_MRX_P8 AC18
PCIE_GTX_MRX_N8 AC18
PCIE_GTX_MRX_P9 AB19
PCIE_GTX_MRX_N9 AB19
PCIE_GTX_MRX_P10 AD19
PCIE_GTX_MRX_N10 AD19
PCIE_GTX_MRX_P11 AD21
PCIE_GTX_MRX_N11 AD21
PCIE_GTX_MRX_P12 AB21
PCIE_GTX_MRX_N12 AB21
PCIE_GTX_MRX_P13 AC22
PCIE_GTX_MRX_N13 AC22
PCIE_GTX_MRX_P14 AD22
PCIE_GTX_MRX_N14 AD22
PCIE_GTX_MRX_P15 AE25
PCIE_GTX_MRX_N15 AE25

CLK_PCIE_VGA AE10
CLK_PCIE_VGA# AC10
PEX_RST_N AD8
PEX_RST_N AD8
XTAL_OUT D11
XTAL_OUT D11
XTAL_IN D10
XTAL_IN D10

External Spread Spectrum



GPIO
GPIO0 N1
GPIO1 G1
GPIO2 C1
GPIO3 M2
GPIO4 M3
GPIO5 K3
GPIO6 K2
GPIO7 J2
GPIO8 M1
GPIO9 D2
GPIO10 D1
GPIO11 J3
GPIO12 J1
GPIO13 K1
GPIO14 F3
GPIO15 G3
GPIO16 G2
GPIO17 E1
GPIO18 F2
GPIO19 E2

DACA
DACA_HSYNC AD2
DACA_VSYNC AD1
DACA_RED AD2
DACA_BLUE AD3
DACA_GREEN AE3
DACA_VREF AE1
DACA_RESET AE1

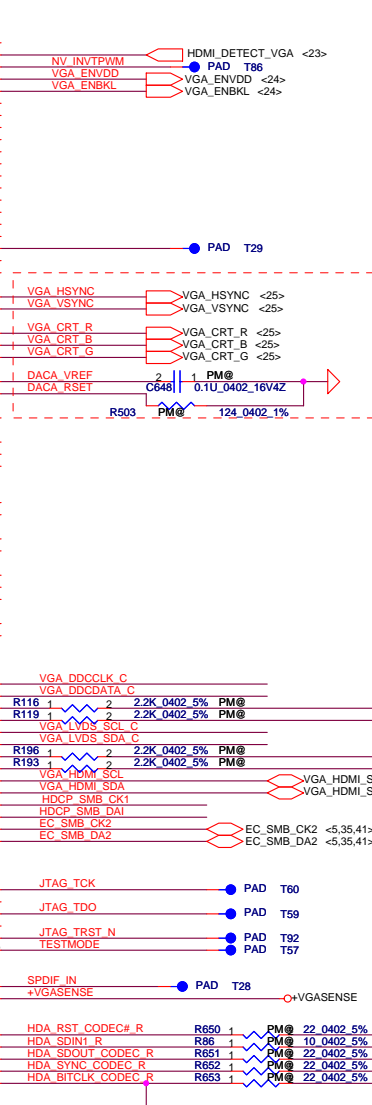
DACB
DACB_RED F7
DACB_BLUE E6
DACB_GREEN E7
DACB_VREF G6
DACB_RESET F8

DACC
DACC_HSYNC U6
DACC_VSYNC U4
DACC_RED T5
DACC_BLUE R4
DACC_GREEN T4
DACC_VREF R6
DACC_RESET V6

I2C
I2C_SCL R1
I2C_SDA T3
I2CB_SCL R2
I2CB_SDA R3
I2CC_SCL A2
I2CC_SDA B1
I2CD_SCL N2
I2CD_SDA N3
I2CE_SCL Y6
I2CE_SDA W6
I2CH_SCL A3
I2CH_SDA A4
I2CS_SCL T1
I2CS_SDA T2

TEST
JTAG_TCK AF3
JTAG_TDO AG4
JTAG_TMS AE4
JTAG_TRST_N AG3
TESTMODE AD25

HDA
SPDIF_IN F9
VDD_SENSE W15
HDA_RST_N C6
HDA_SDI AG6
HDA_SDO B6
HDA_SYNC_CODEC A7
HDA_BITCLK_CODEC A7

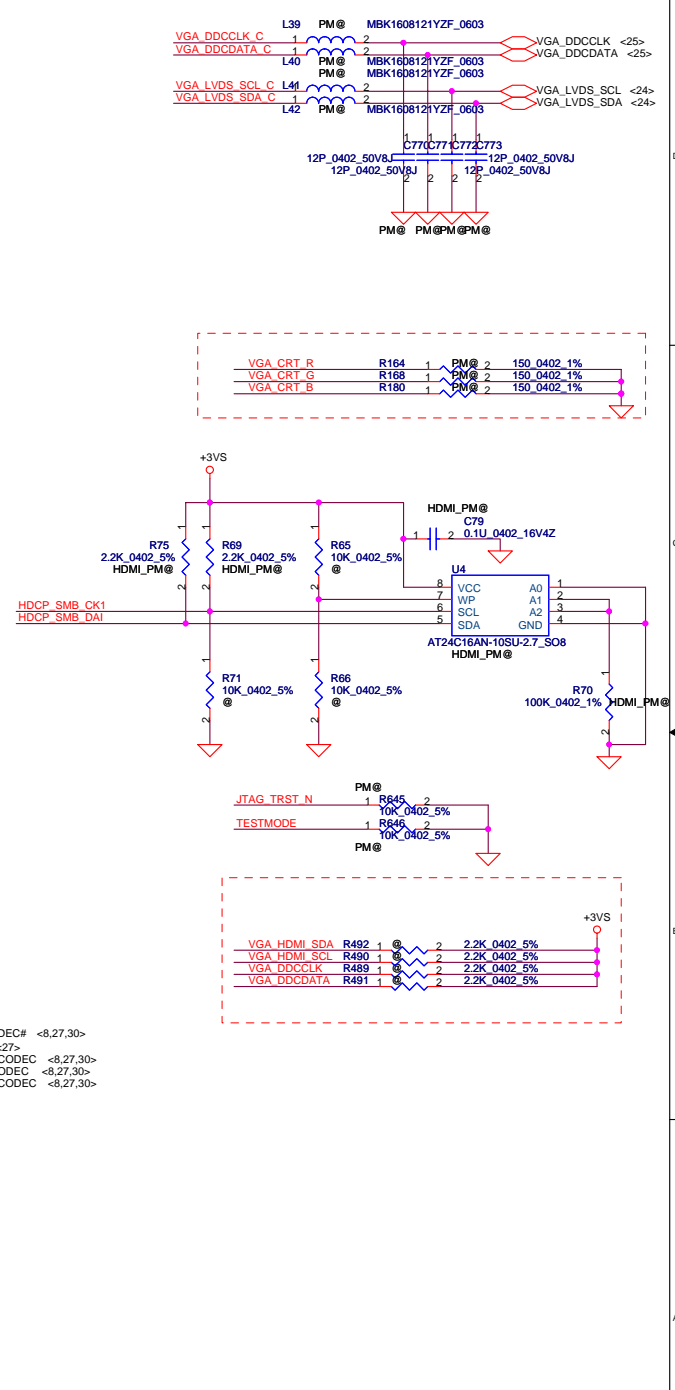


CRT OUT

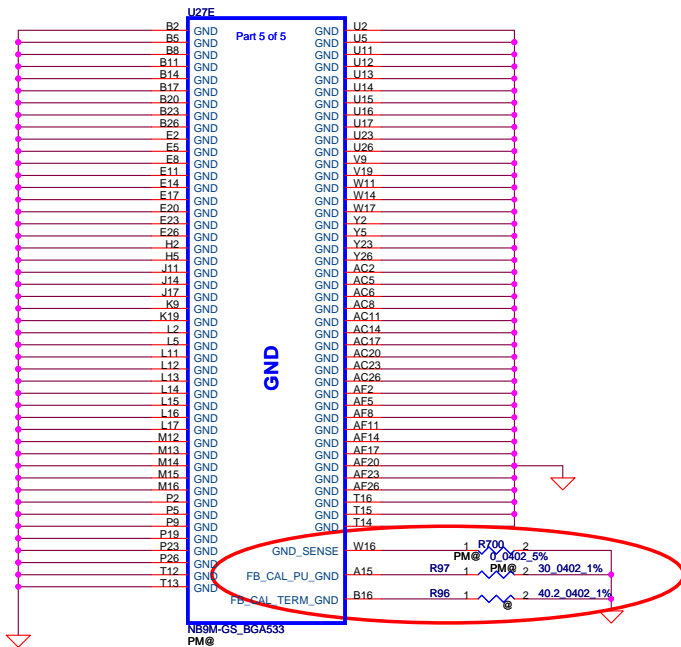
+3VS

+3VS

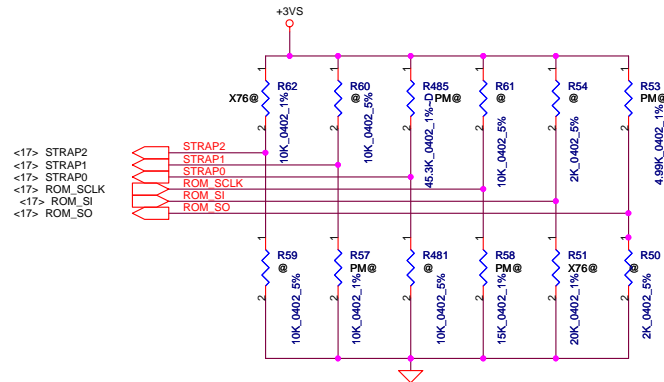
+3VS



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Title			
NB9M-GS PCIE, LVDS, GPIO, CLK			
Size B			
J1WA3/A4 LA4212P			
Date: Wednesday, May 14, 2008			
Sheet 16 of 53			



A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available

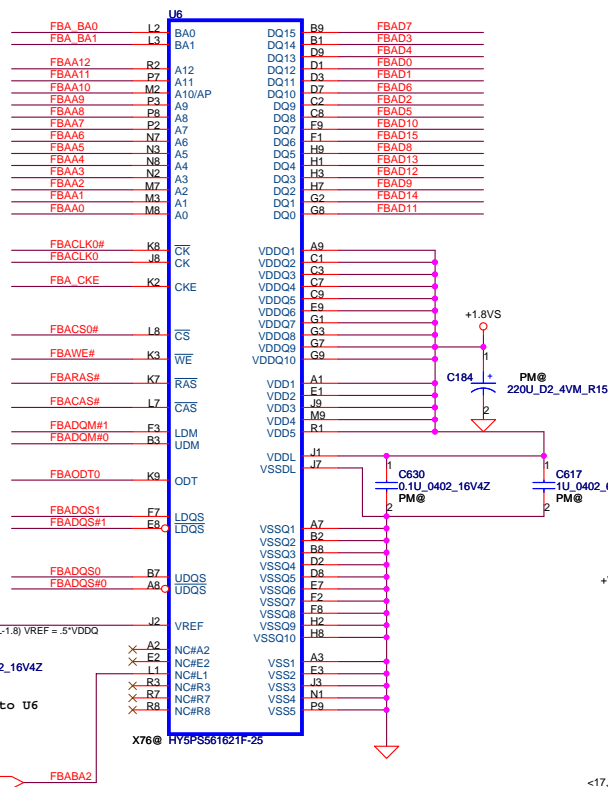


GB1 Family GPU Strap Options

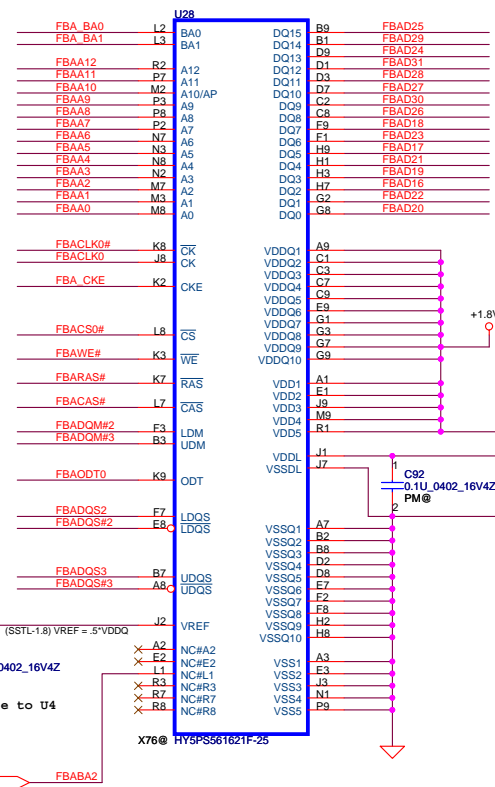
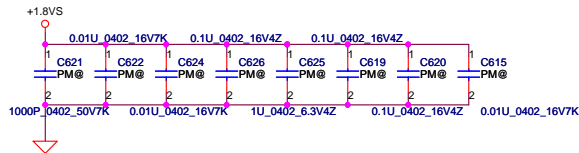
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	32Mx16 (5)	PU 5K	PD 15K	PD 30K	PU 10K	PD 10K
		64Mx16	PU 5K	PD 15K	PD 5K	PU 10K	PD 10K
	Hynix	32Mx16 (7)	PU 5K	PD 15K	PD 45K	PU 10K	PD 10K
		64Mx16	PU 5K	PD 15K	PD 10K	PU 10K	PD 10K
	Qimonda	32Mx16 (6)	PU 5K	PD 15K	PD 35K	PU 10K	PD 10K

Component	Manufacturer	Compal PN
DDR2 VRAM (32M*16)	Hynix	SA00000FF30
	Qimonda	SA00000S820
	Samsung	SA00001VX10

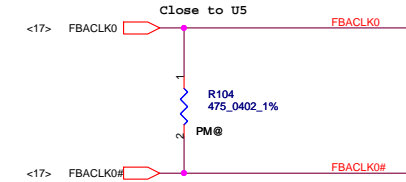
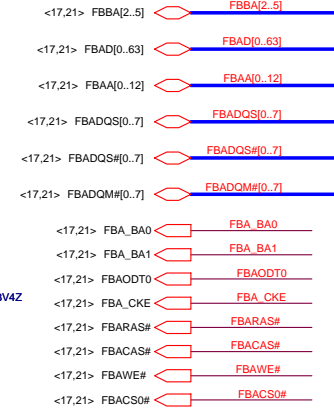
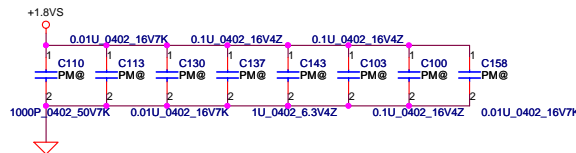
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	NB9M-GE GND & STRAP	
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				Date:	Monday, May 12, 2008	Sheet 19 of 53



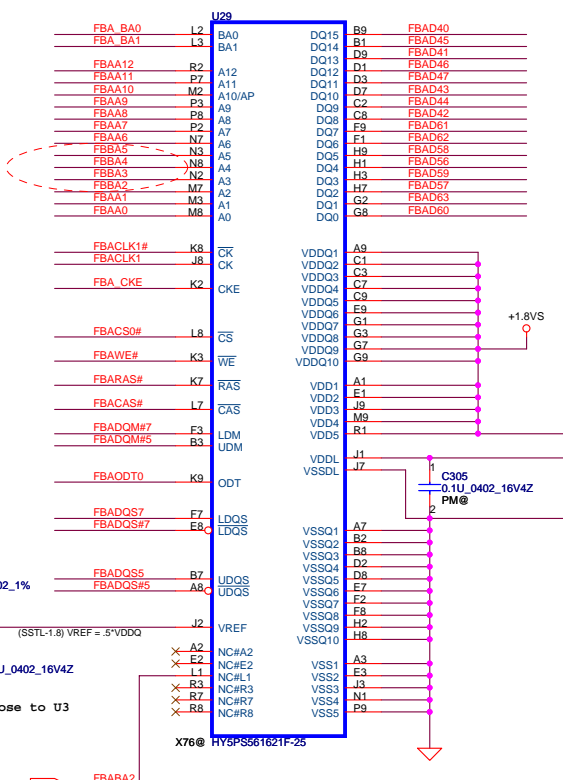
DDR2 BGA MEMORY



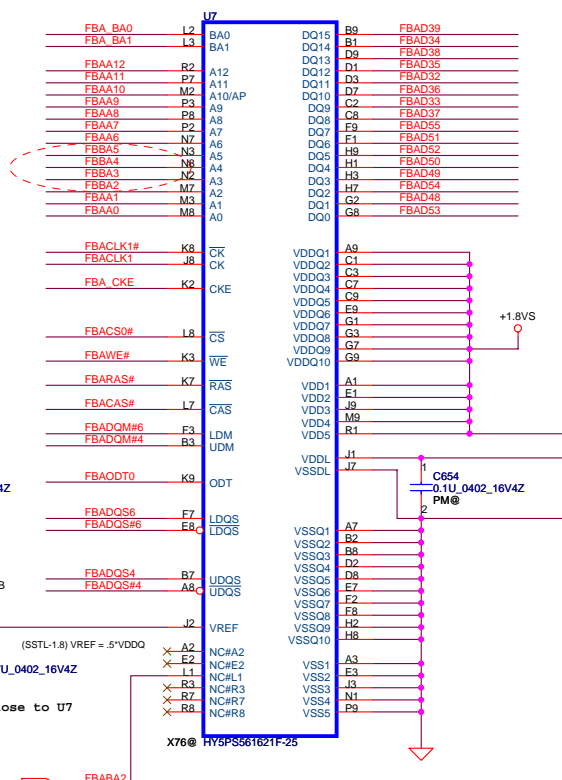
DDR2 BGA MEMORY



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				Custom	JIWA3/A4_LA4212P
				Date:	Monday, May 12, 2008
				Sheet	20 of 53
				Rev	1.0

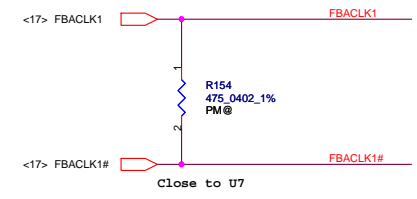
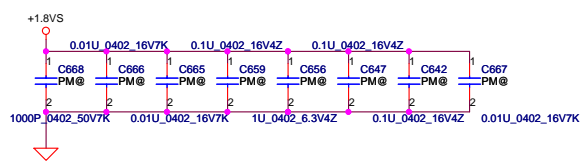
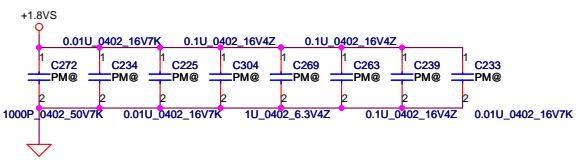


DDR2 BGA MEMORY



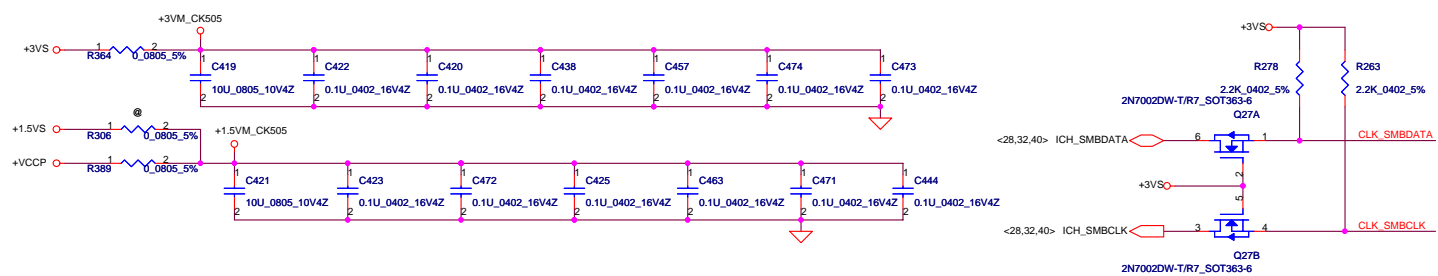
DDR2 BGA MEMORY

- <17,20> FBAD[0..63] FBAD[0..63]
- <17,20> FBAA[0..12] FBAA[0..12]
- <17> FBBA[2..5] FBBA[2..5]
- <17,20> FBADQS[0..7] FBADQS[0..7]
- <17,20> FBADQS[0..7] FBADQS[0..7]
- <17,20> FBADQM[0..7] FBADQM[0..7]
- <17,20> FBA_BA0 FBA_BA0
- <17,20> FBA_BA1 FBA_BA1
- <17,20> FBAODT0 FBAODT0
- <17,20> FBA_CKE FBA_CKE
- <17,20> FBARAS# FBARAS#
- <17,20> FBACAS# FBACAS#
- <17,20> FBAWE# FBAWE#
- <17,20> FBACS0# FBACS0#

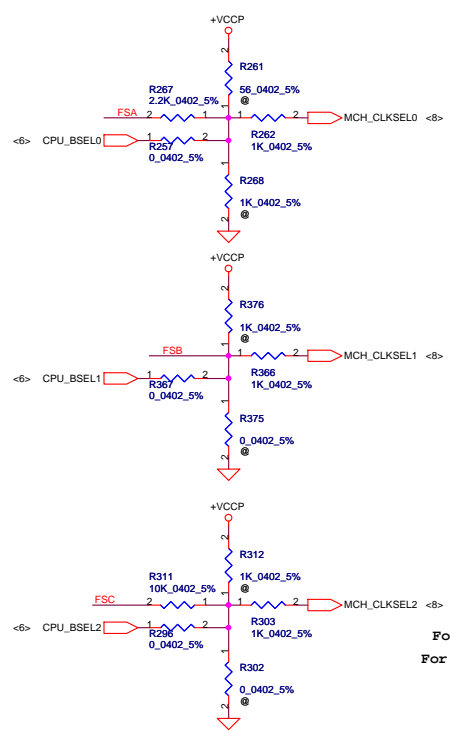


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				Date:	Monday, May 12, 2008
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				Rev	1.0

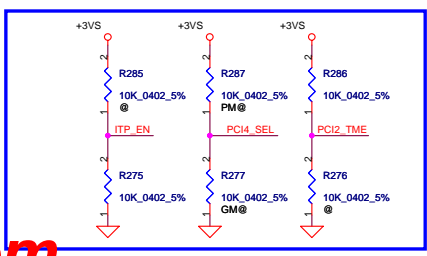
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

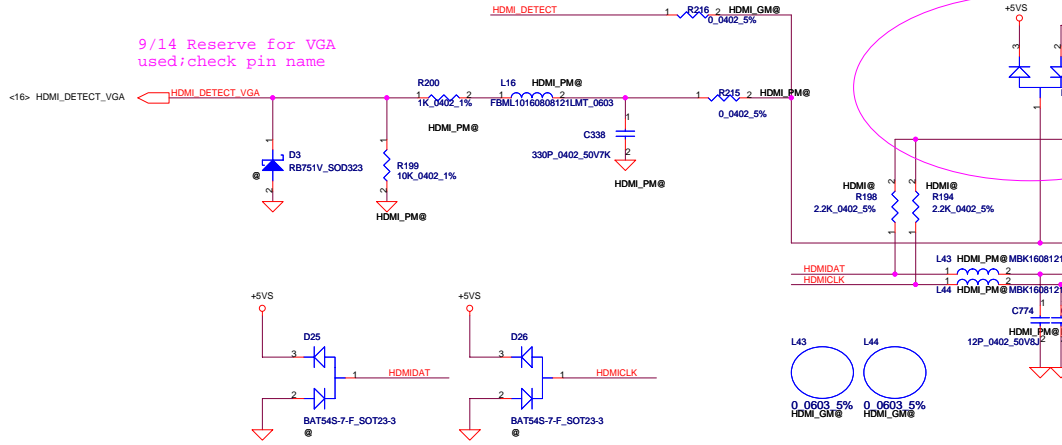
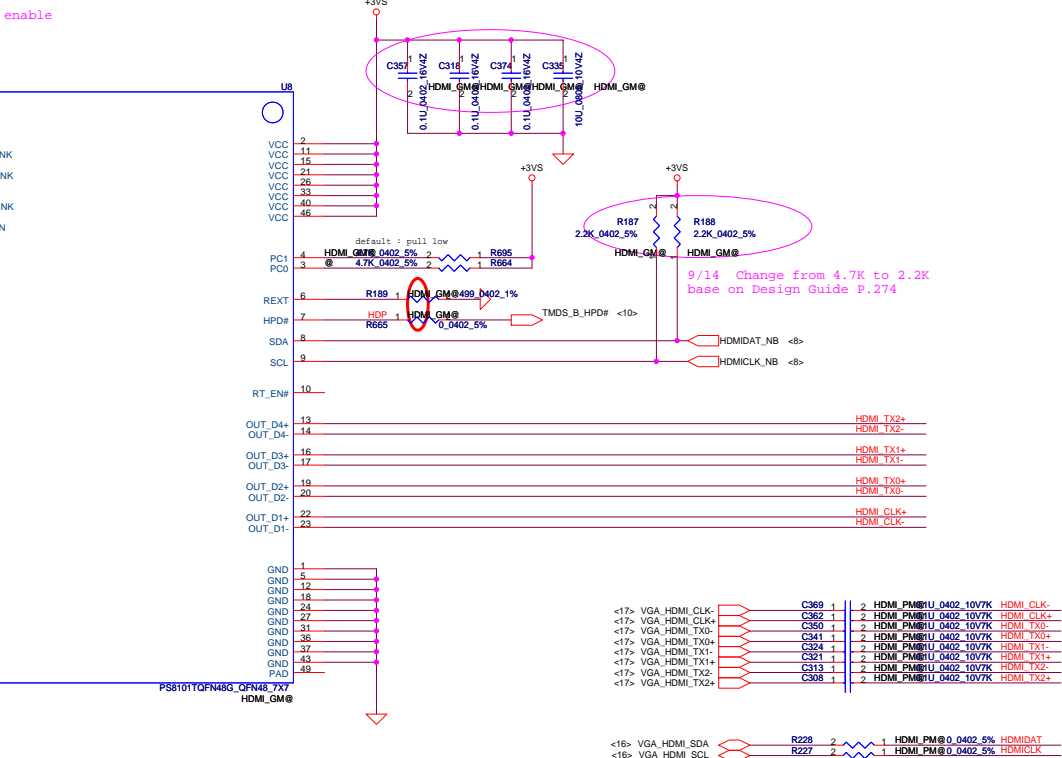
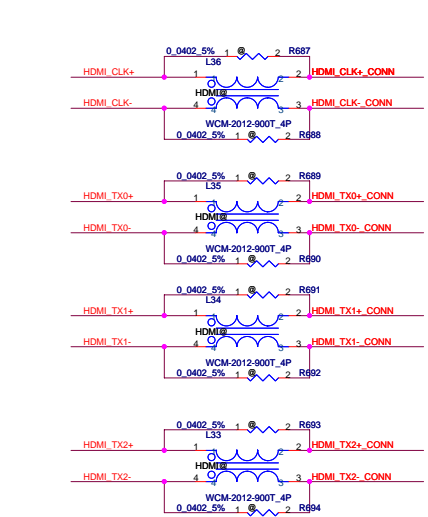
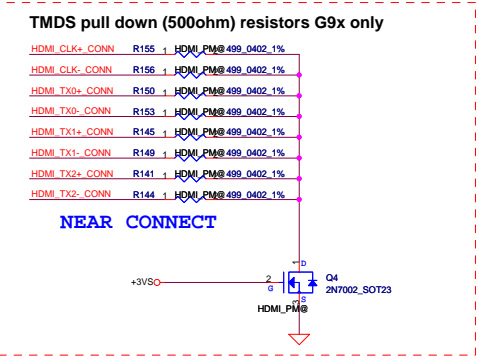
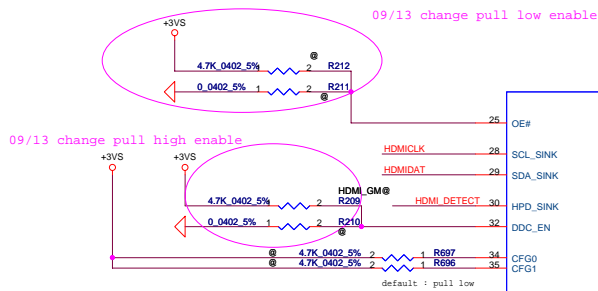


SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

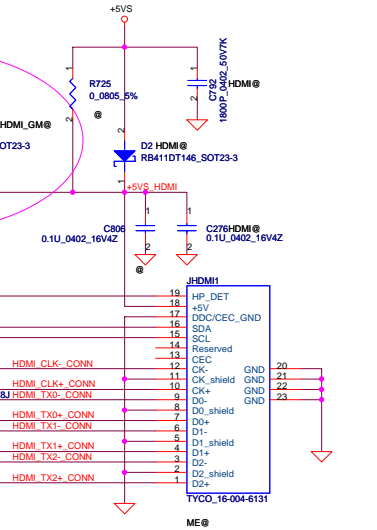
REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

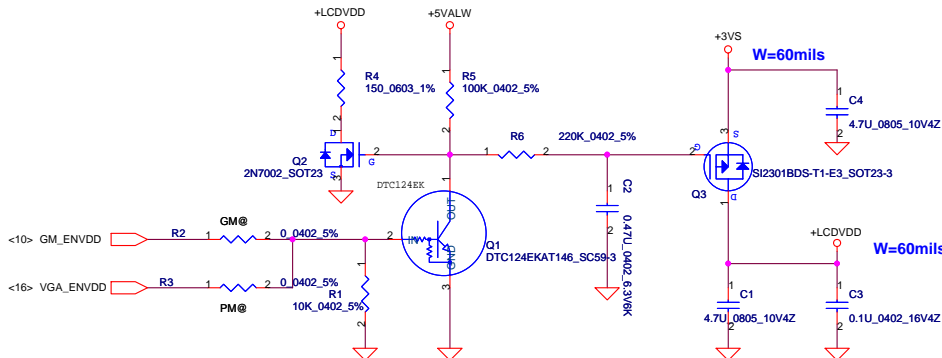


9/13 Add inverting level shift circuit base on Design Guide P.277

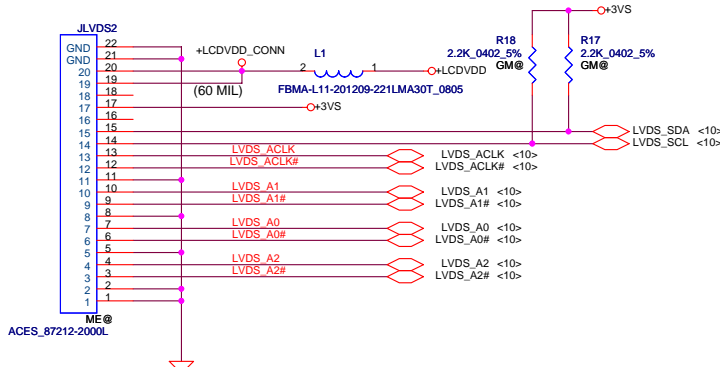
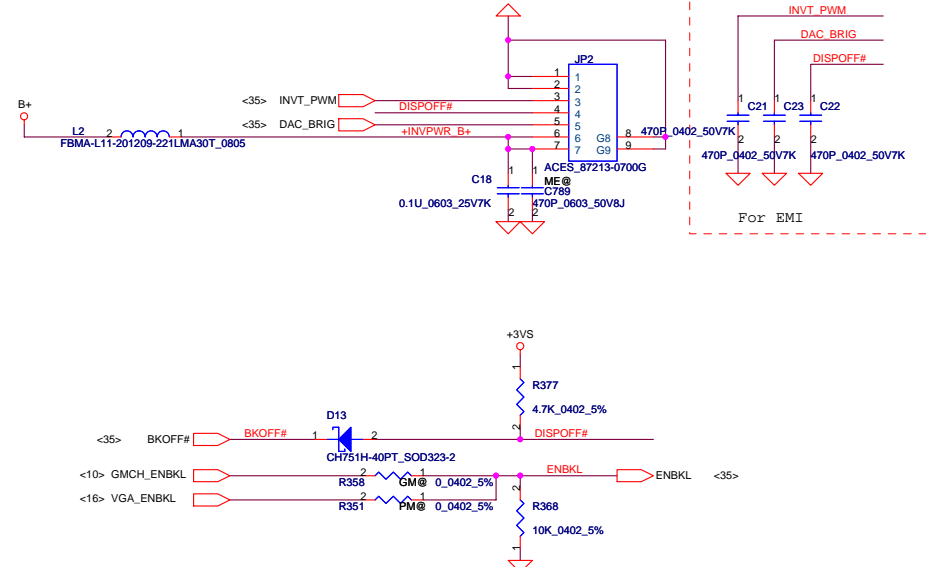
9/14 Change from 4.7K to 2.2K base on Design Guide P.274



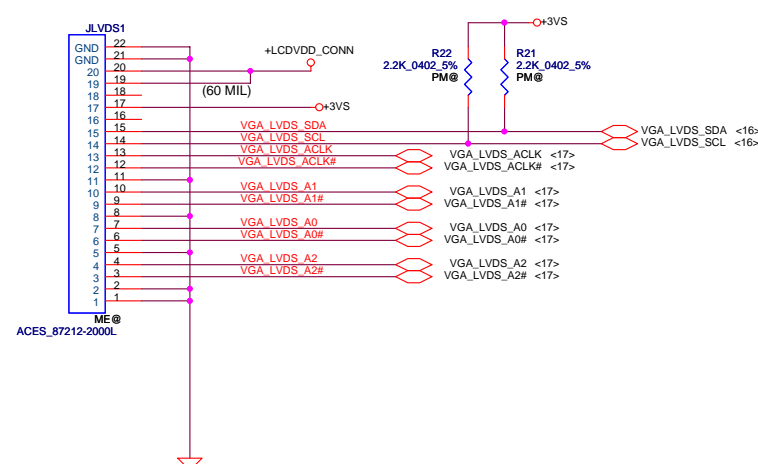
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.

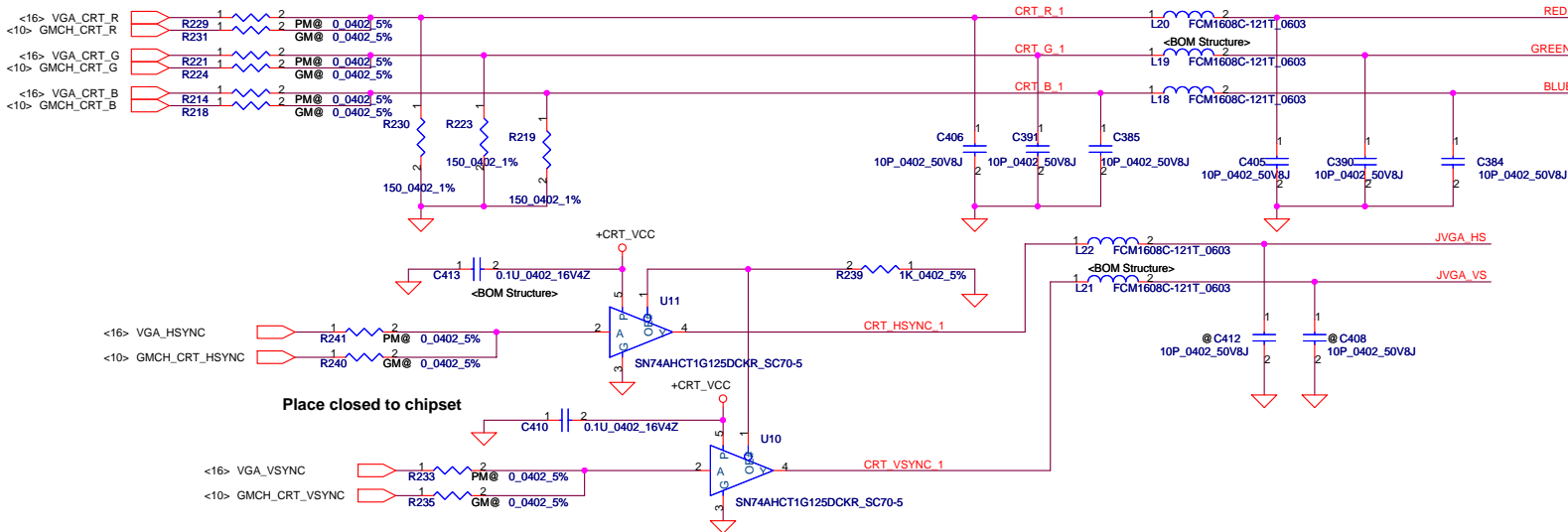
***INVERTER Conn.***

LCD/PANEL BD. Conn.

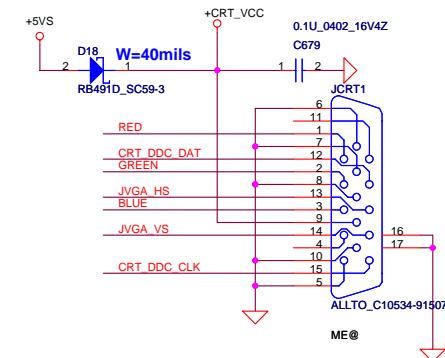
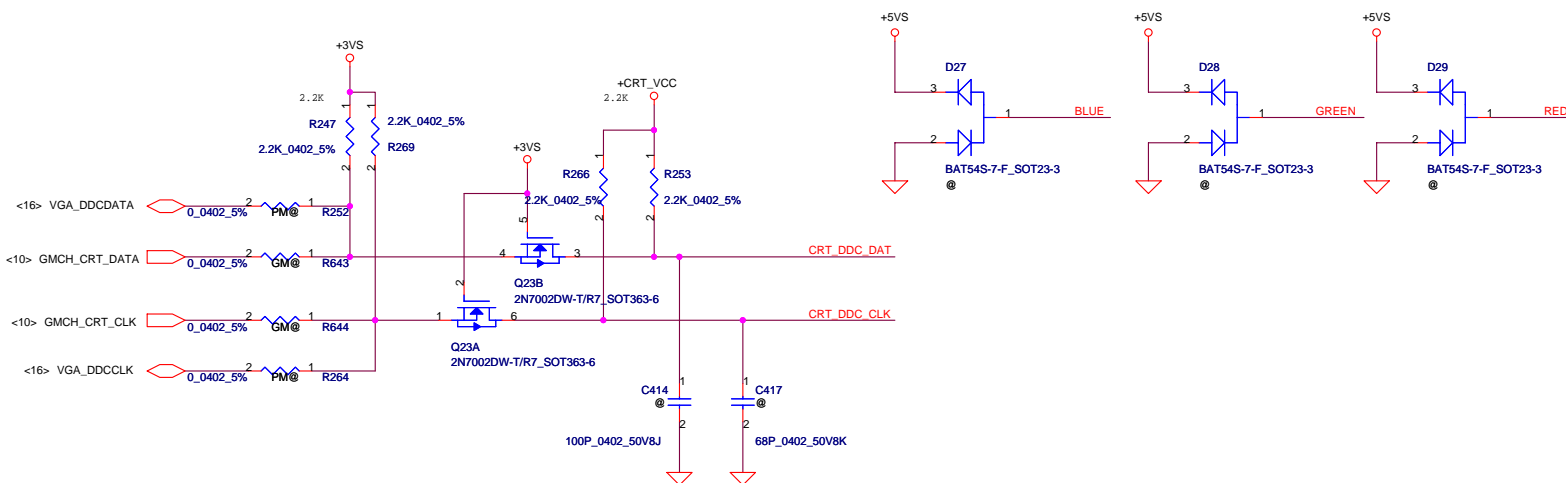


CRT Connector

Place closed to chipset



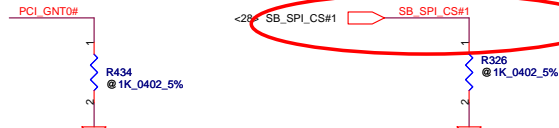
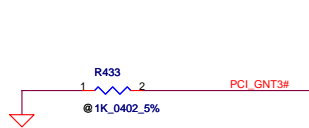
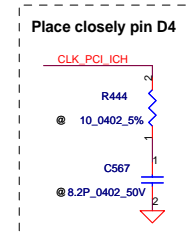
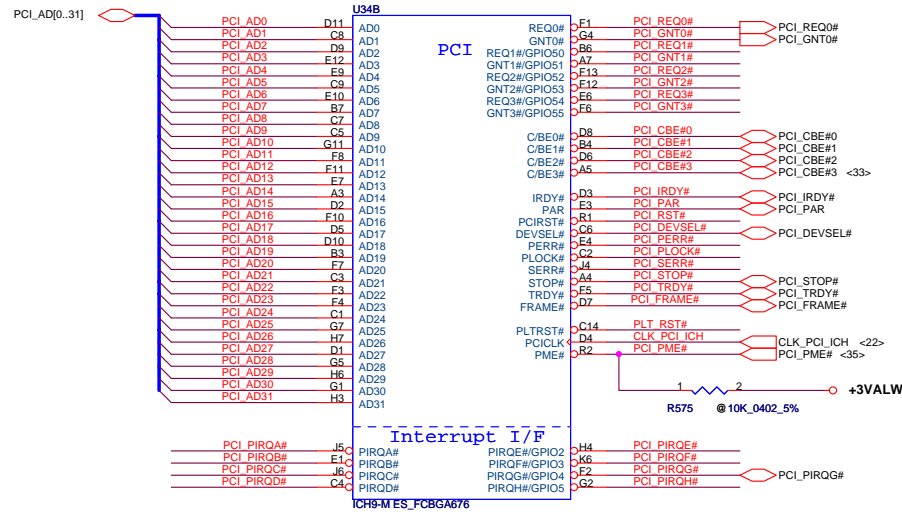
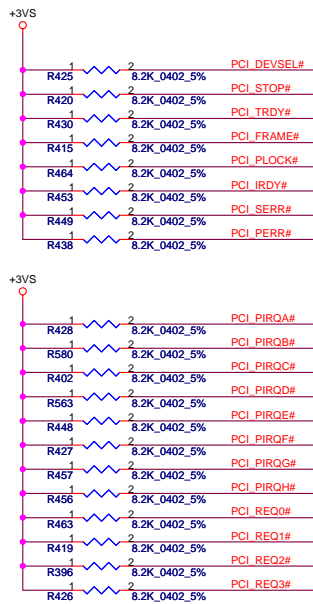
Place closed to chipset



PIN ASSIGMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

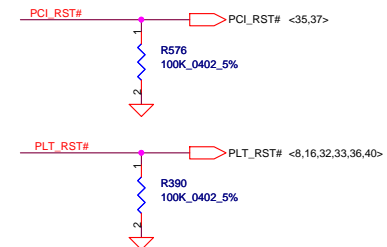
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
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Size	Document Number	JIWA3/A4_LA4212P		Rev
Custom				1.0
Date:	Monday, May 12, 2008	Sheet	25	of 53



Pull high?

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

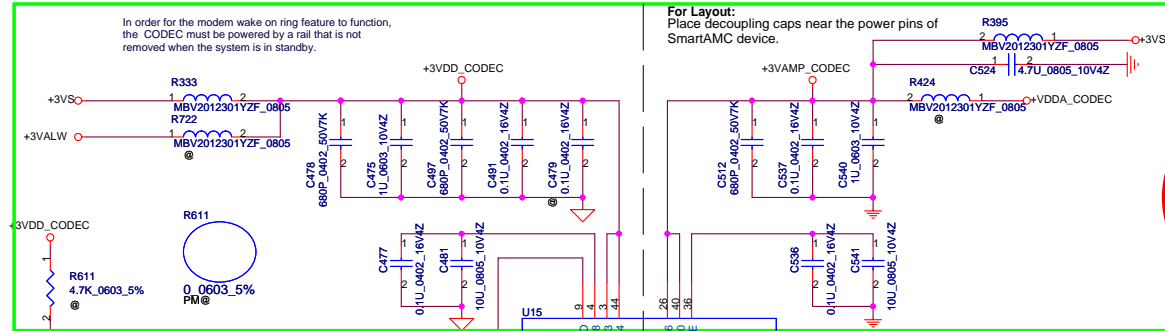






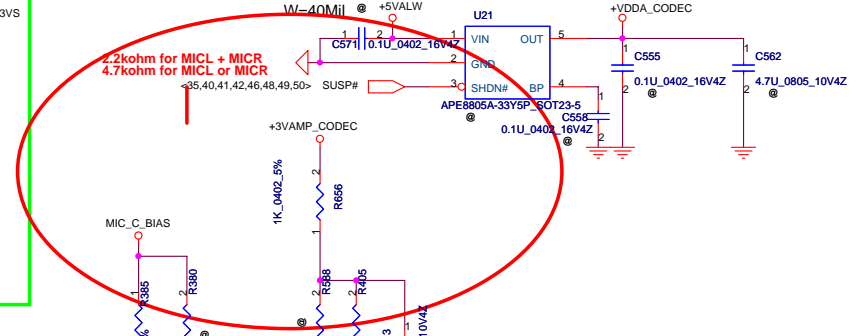
AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p



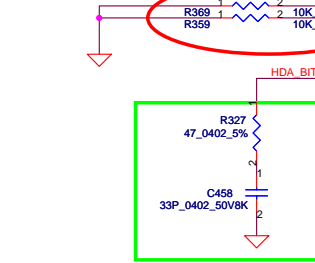
CODEC POWER

(3.33V)
250mW

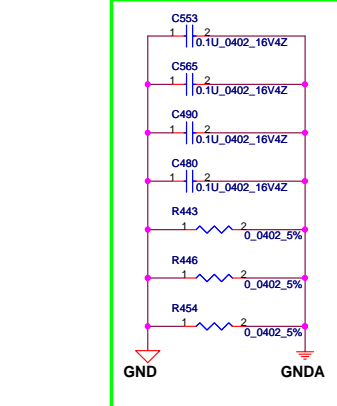


CX20548
AMOM DAA

PC_BEEP dB control



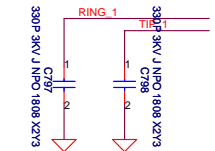
DIGITAL ANALOG



Place these C and R around AGND and DGND, then choose the one which is close to Codec

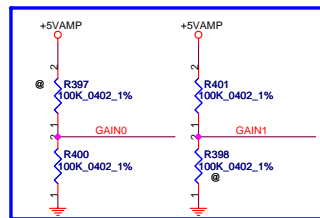
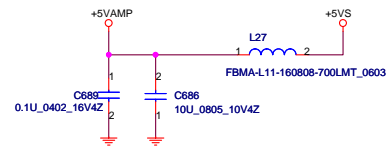
WWW.AliSaler.Com

CX20548
AMOM DAA

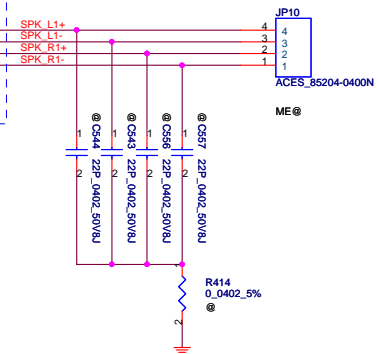
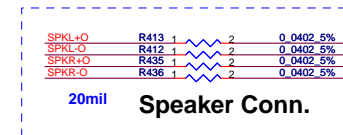


Speaker Amplifier

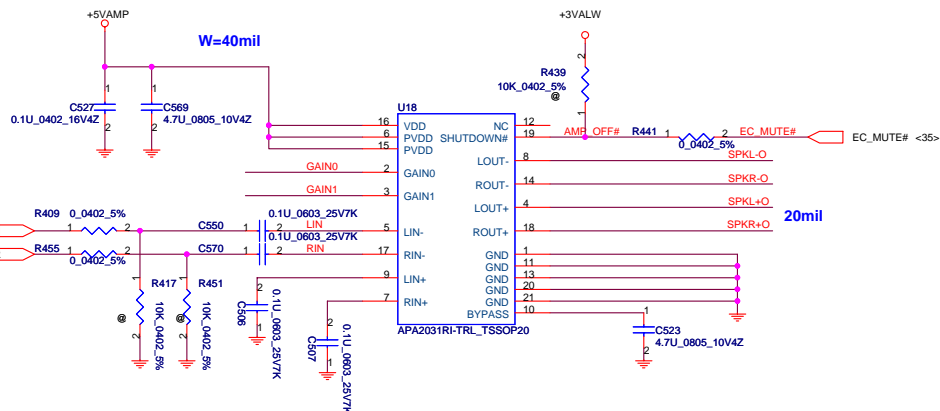
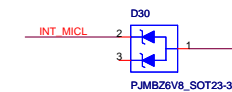
1nd = APA2031 (SA00001RZ00)
2nd = G1431F2U (SA000012Y00)



GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

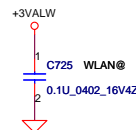
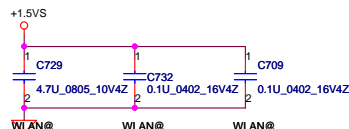
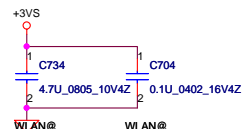


INT MIC

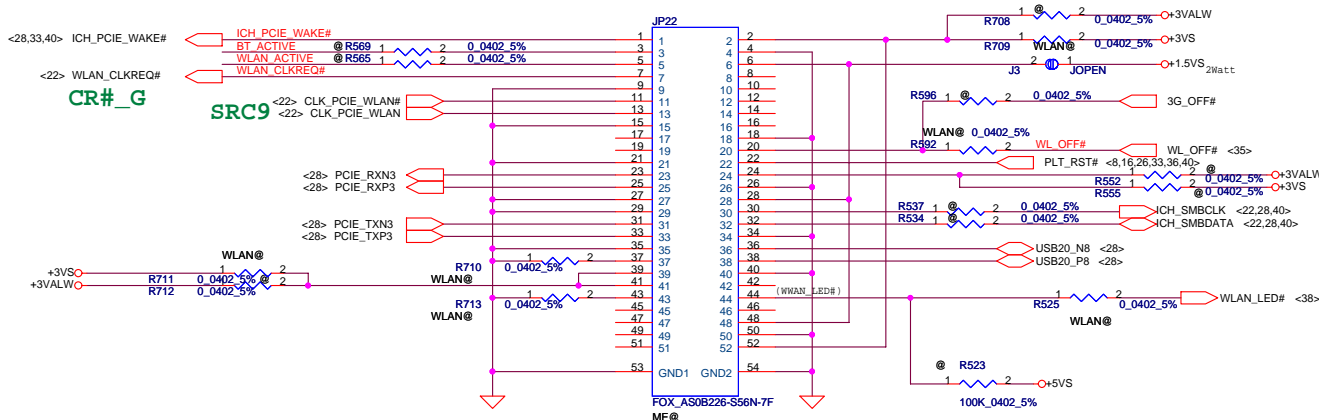


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Date:	Monday, May 12, 2008	Sheet	31	of 53

Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN

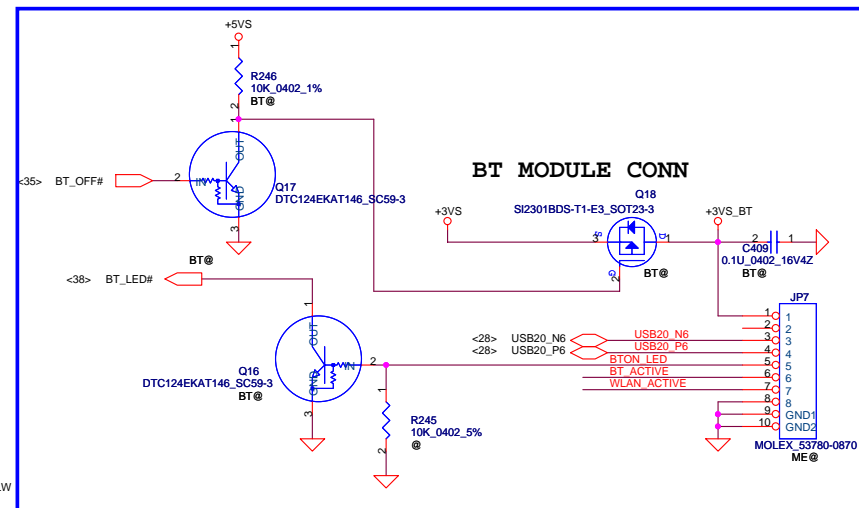


Mini-Express Card(Slot 1-WLAN)



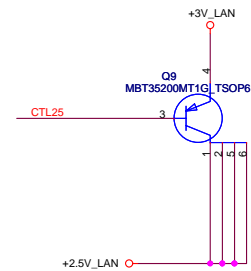
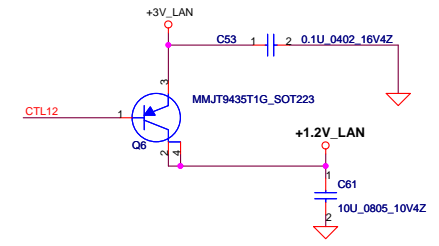
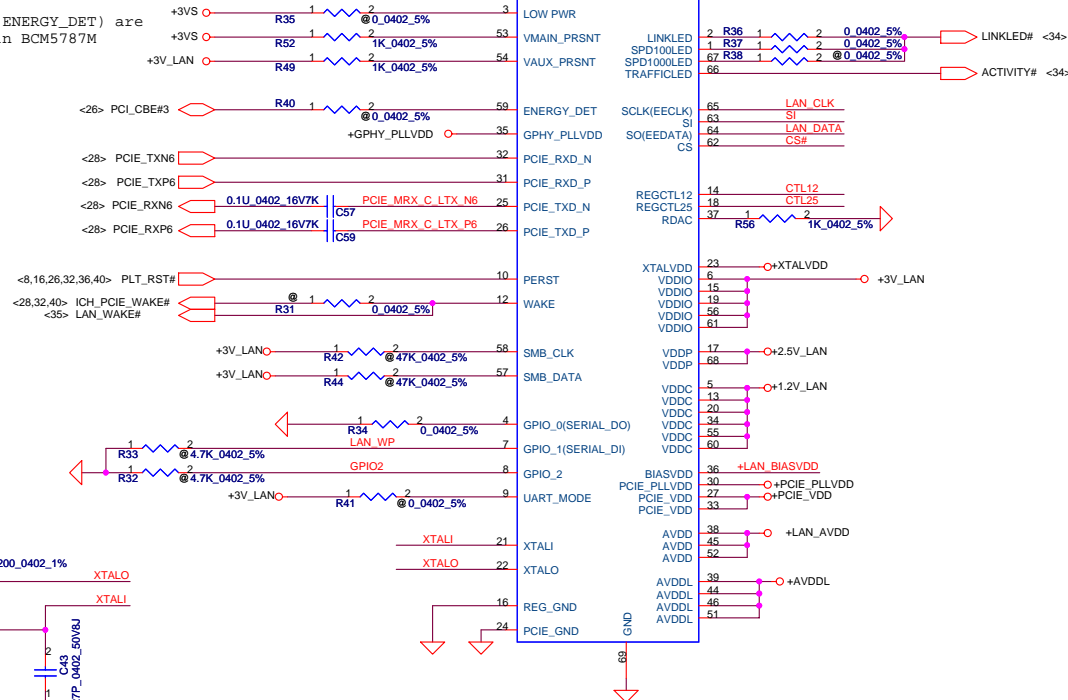
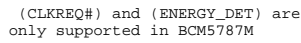
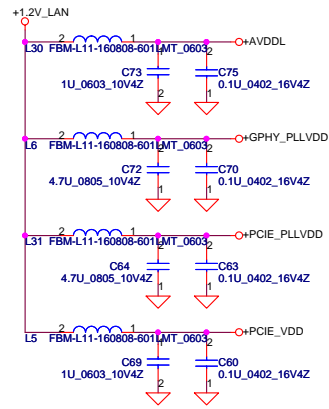
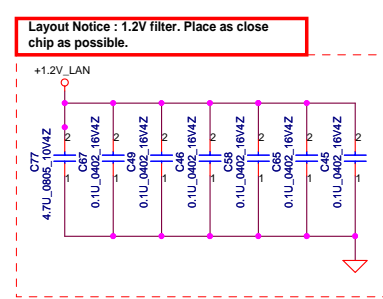
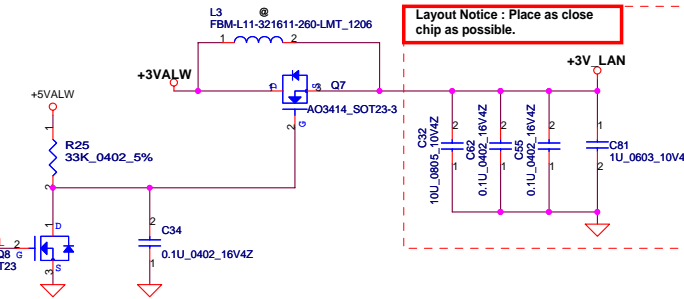
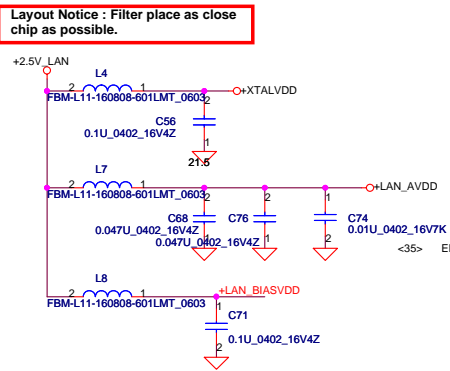
2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

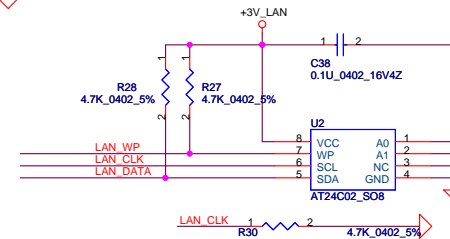
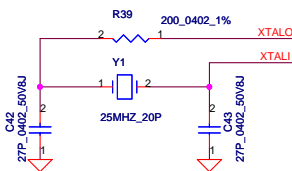
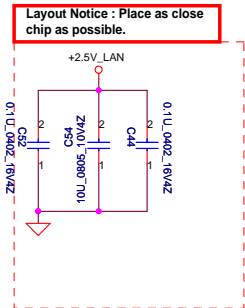


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				Date:	Tuesday, May 20, 2008
				Sheet	32 of 53
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Layout Notice : Filter place as close chip as possible.



Notice : 4.7u 6.3V capactor Thickness 1.25mm



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				Custor	JIWA3/A4_LA4212P	1.0	
				Date:	Monday, May 12, 2008 [Sheet 33 of 53]		



INT_KBD Conn.

KSII[0..7]

KSOI[0..15]

KSII[0..7] <35>

KSOI[0..15] <35>

KSI				KSO			
KSO2	C396	1	2 @ 100P_0402_50V8J	KSO1	C401	1	2 @ 100P_0402_50V8J
KSO15	C334	1	2 @ 100P_0402_50V8J	KSO7	C398	1	2 @ 100P_0402_50V8J
KSO6	C400	1	2 @ 100P_0402_50V8J	KSI2	C392	1	2 @ 100P_0402_50V8J
KSO8	C399	1	2 @ 100P_0402_50V8J	KSO5	C394	1	2 @ 100P_0402_50V8J
KSO13	C330	1	2 @ 100P_0402_50V8J	KSI3	C393	1	2 @ 100P_0402_50V8J
KSO12	C329	1	2 @ 100P_0402_50V8J	KSO14	C331	1	2 @ 100P_0402_50V8J
KSO11	C332	1	2 @ 100P_0402_50V8J	KSI7	C377	1	2 @ 100P_0402_50V8J
KSO10	C333	1	2 @ 100P_0402_50V8J	KSI6	C378	1	2 @ 100P_0402_50V8J
KSO3	C328	1	2 @ 100P_0402_50V8J	KSI5	C381	1	2 @ 100P_0402_50V8J
KSO4	C397	1	2 @ 100P_0402_50V8J	KSI4	C380	1	2 @ 100P_0402_50V8J
KSI0	C395	1	2 @ 100P_0402_50V8J	KSO9	C379	1	2 @ 100P_0402_50V8J
KSO0	C382	1	2 @ 100P_0402_50V8J	KSI1	C376	1	2 @ 100P_0402_50V8J

JP6

KSI1	1
KSI7	2
KSI6	3
KSO9	4
KSI4	5
KSI5	6
KSO0	7
KSI2	8
KSI3	9
KSO5	10
KSO1	11
KSI0	12
KSO2	13
KSO4	14
KSO7	15
KSO8	16
KSO6	17
KSO3	18
KSO12	19
KSO13	20
KSO14	21
KSO11	22
KSO10	23
KSO15	24

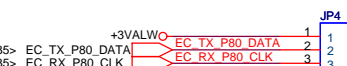
ACES_85202-2405

To TP/B Conn.

The diagrams illustrate the connection of TP_CLK and TP_DATA signals to different components:

- Diagram 1 (JP5):** Shows the connection of TP_CLK and TP_DATA to the JP5 connector. TP_CLK is connected to pin 1, TP_DATA to pin 2, SW/L to pin 4, and SW/R to pin 5. The +5VS signal is connected to pin 7. Pins 3, 6, and 8 are connected to GND. The component is identified as ACES_85201-06051.
- Diagram 2 (ME@):** Shows the connection of TP_CLK and TP_DATA to the ME@ connector. TP_CLK is connected to pin 1 of C327, and TP_DATA is connected to pin 2 of C327. The +5VS signal is connected to pin 1 of C245. The component is identified as 0.1U_0402_16V4Z.
- Diagram 3 (D31):** Shows the connection of TP_CLK and TP_DATA to the D31 component. TP_CLK is connected to pin 1, and TP_DATA is connected to pin 2. The component is identified as PJDLC05_SOT23-3.

EC DEBUG PORT



The diagram illustrates the connections for the EC Debug Port. It features a blue component labeled 'JP4' with four pins numbered 1 through 4. Pin 1 is connected to a red line labeled 'EC_TX_P80_DATA'. Pin 2 is connected to a red line labeled 'EC_RX_P80_CLK'. Pin 3 is connected to a red line labeled 'EC_RX_P80_CLK'. Pin 4 is connected to a red line labeled 'EC_RX_P80_CLK'. A red arrow points from the bottom of the JP4 component to a red arrow pointing downwards, labeled 'ACES_85205-0400 ME@'. The text '+3VALW' is positioned above the red line for EC_TX_P80_DATA. The text '<14,15,35>' is positioned to the left of the red lines for EC_TX_P80_DATA and EC_RX_P80_CLK.

+3VALW

<14,15,35> EC_TX_P80_DATA

<14,15,35> EC_RX_P80_CLK

JP4

1

2

3

4

ACES_85205-0400

ME@

FOR LPC SIO DEBUG PORT

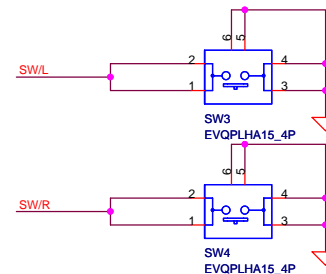
FOR LPC SIO DEBUG PORT

JP11

Pin	Signal	Directionality	Notes
1			
2			
3			
4			
5			
6			
7	LPC AD0	Bidirectional	CLK_14M_SIO <22>
8	LPC AD1	Bidirectional	LPC AD0 <27,35>
9	LPC AD2	Bidirectional	LPC AD1 <27,35>
10	LPC AD3	Bidirectional	LPC AD2 <27,35>
11	LPC FRAME#	Bidirectional	LPC AD3 <27,35>
12	LPC DRQ0#	Bidirectional	LPC FRAME# <27,35>
13	PCI_RST#	Bidirectional	LPC DRQ0# <27>
14			PCI_RST# <26,35>
15	CLK_PCI_DB	Bidirectional	
16	SERIRQ	Bidirectional	CLK_PCI_DB <22>
17			SERIRQ <28,35>
18			
19			
20			

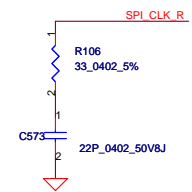
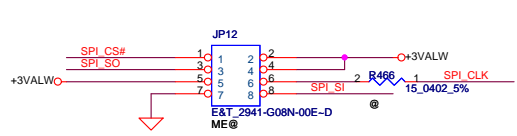
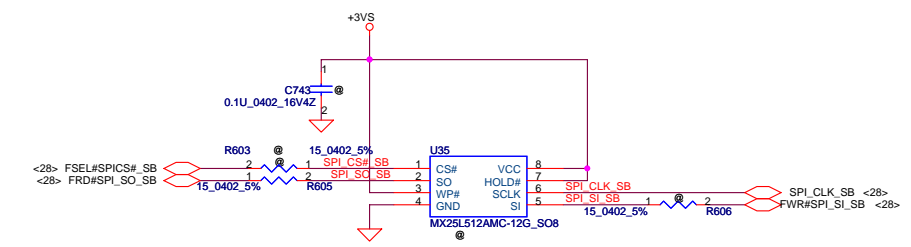
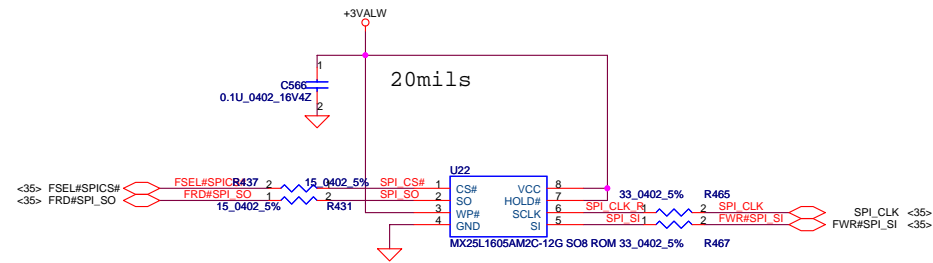
ACES_85201-2005

ME@

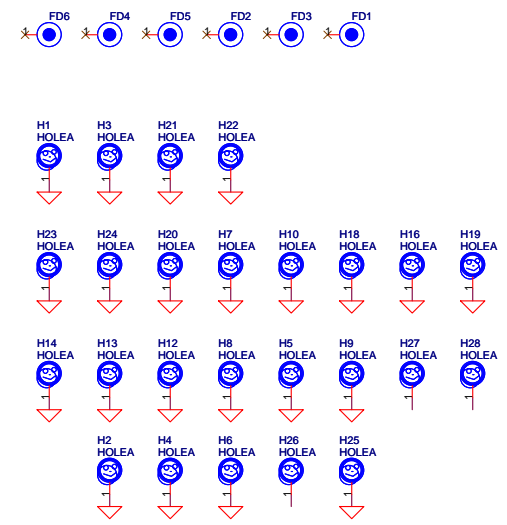
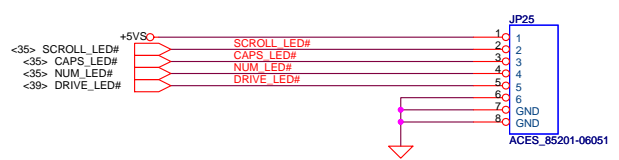
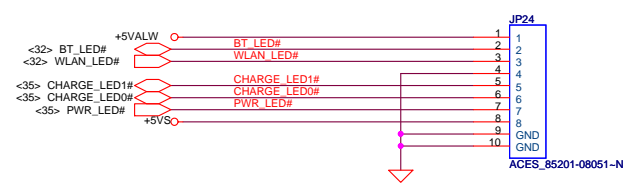


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				Document Number	1.0
				JIWA3/A4_LA4212P Date: Monday, May 12, 2008 Sheet 37 of 53	

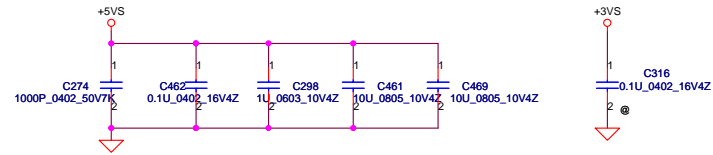
FOR EC 8M SPI ROM



LED

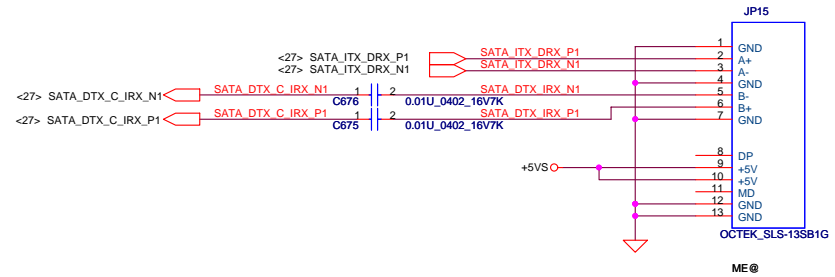
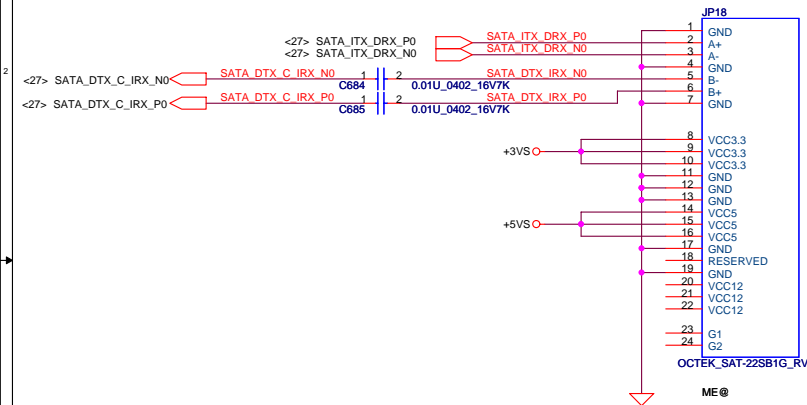


Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2007/10/15		Deciphered Date		2008/10/15		Title	
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										Size	Document Number
										B	J1WA3/A4_LA4212P
										Rev	1.0
										Date:	Wednesday, May 14, 2008
										Sheet	38 of 53



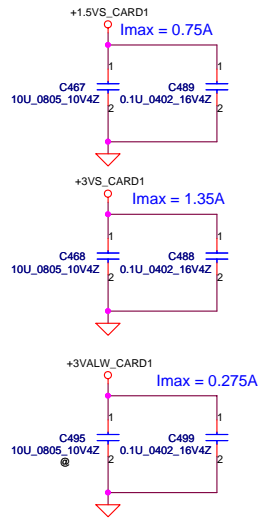
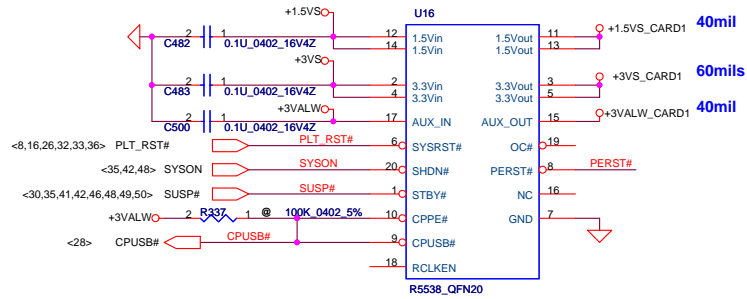
SATA HDD Conn.

SATA ODD Conn.

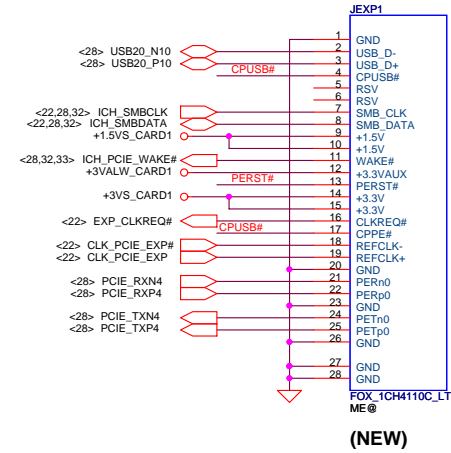


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				JIWA3/A4_LA4212P	
				Date: Monday, May 12, 2008	Rev 1.0
				Sheet 39	of 53

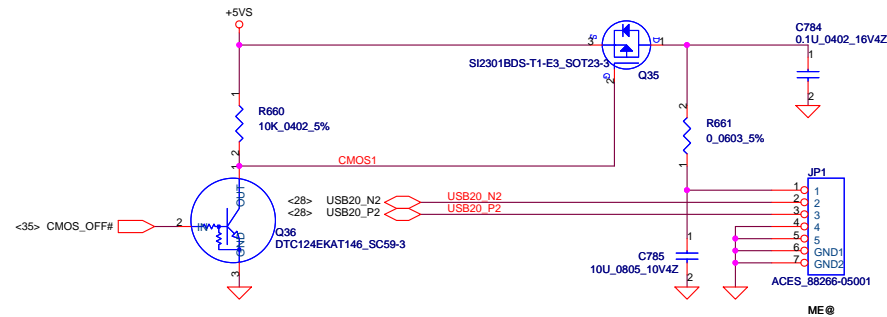
Express Card Power Switch



New Card Socket (Left/TOP)



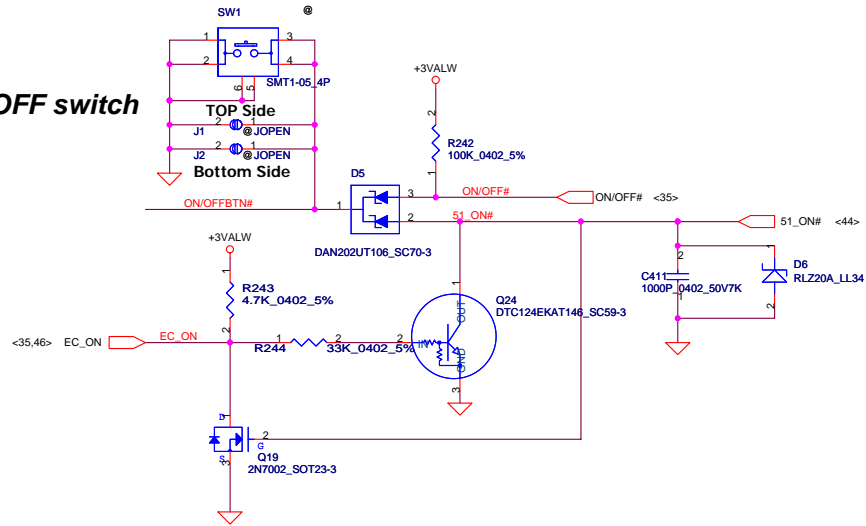
CMOS Camera Conn



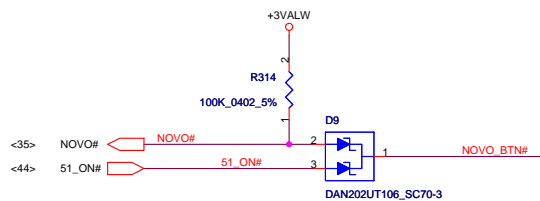
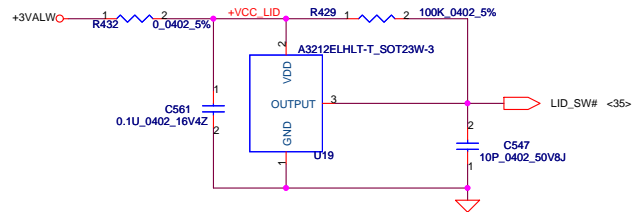
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				NEW CARD & CMOS Connector	
				JIWA3/A4_LA4212P	
				Rev 1.0	
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Power Button

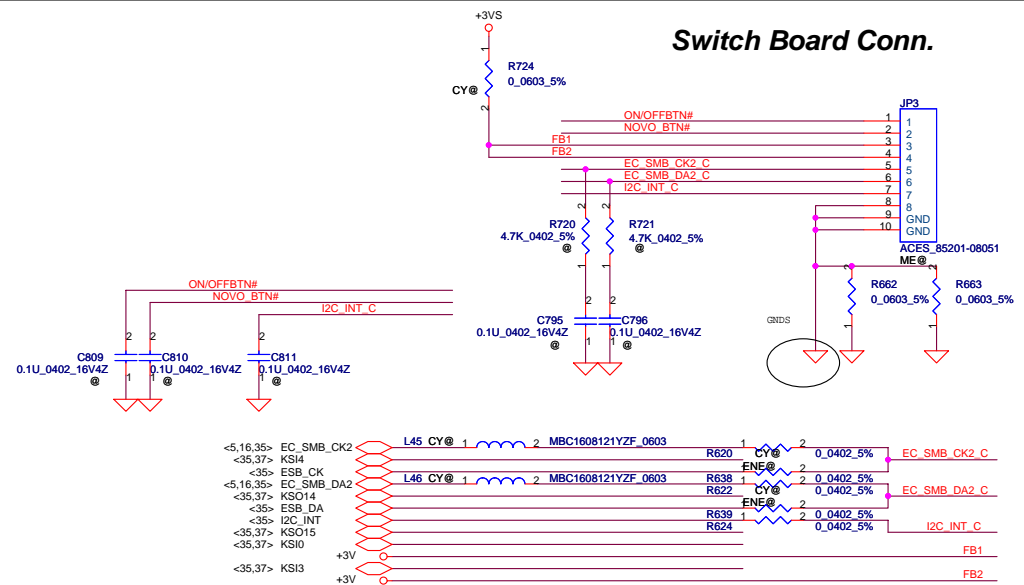
ON/OFF switch



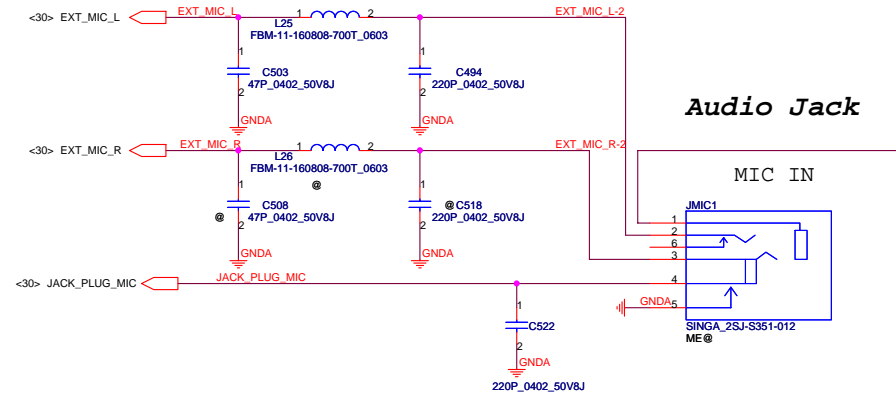
Lid Switch



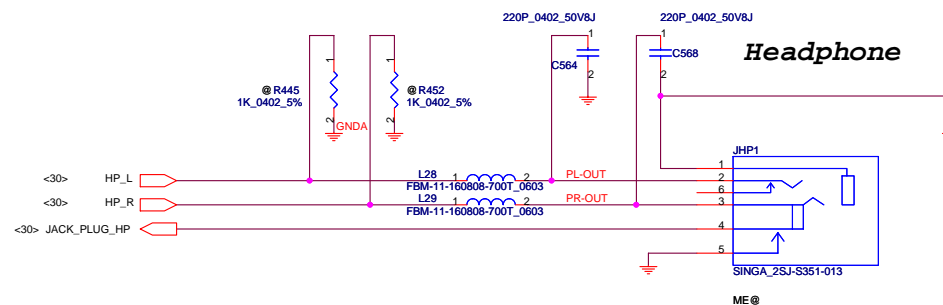
Switch Board Conn.



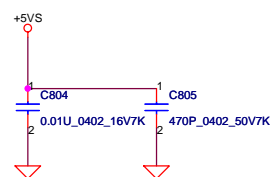
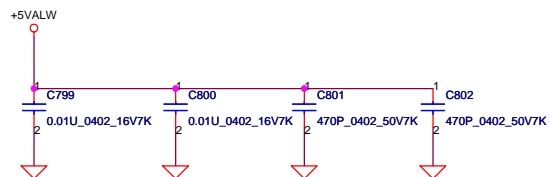
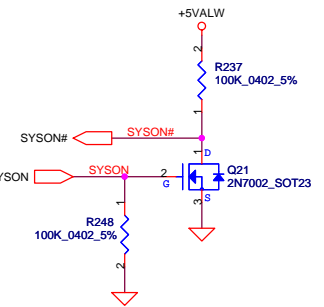
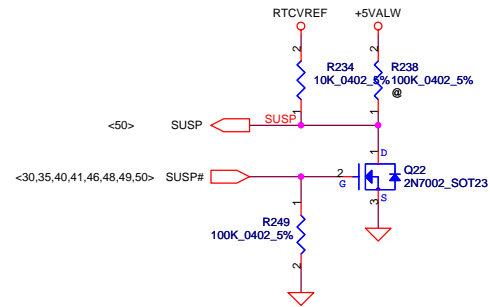
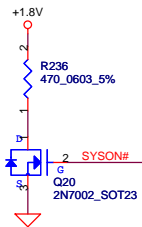
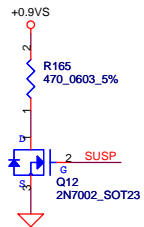
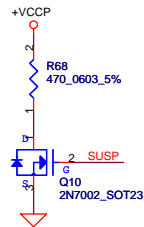
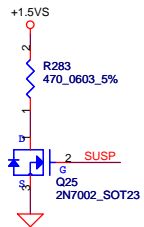
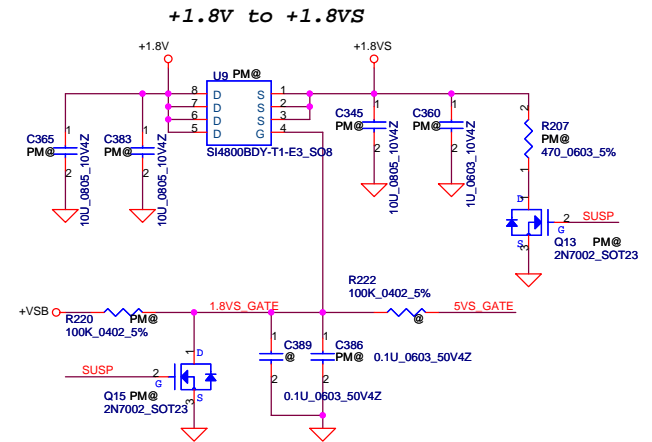
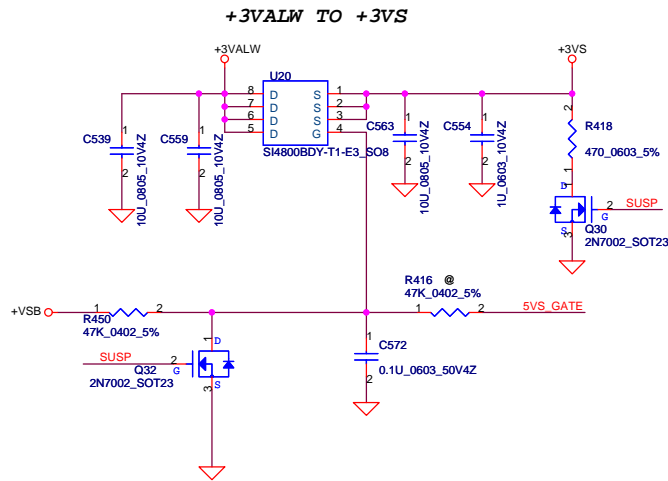
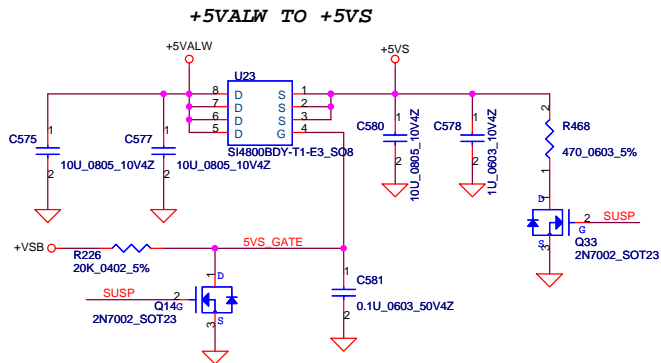
Audio Jack



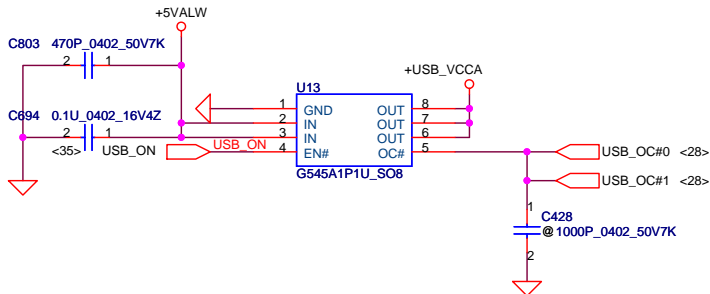
Headphone



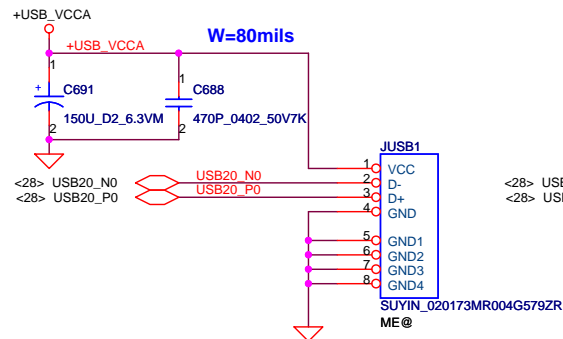
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	Audio Jack & SW connector	
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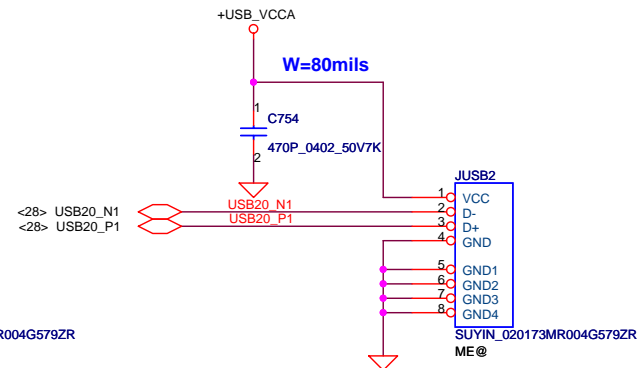
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Size	Document Number	JiWA3/A4_LA4212P		Rev	1.0
Date:	Monday, May 12, 2008	Sheet	42 of 53		



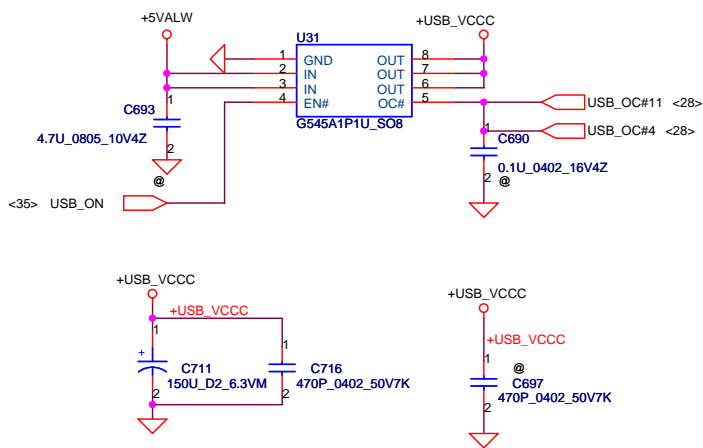
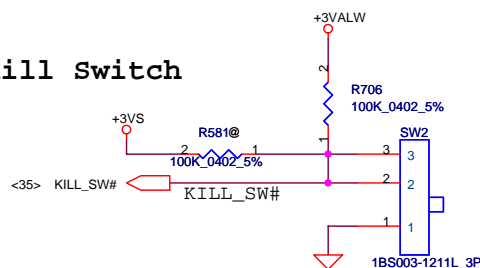
LIFT USB CONN. 1



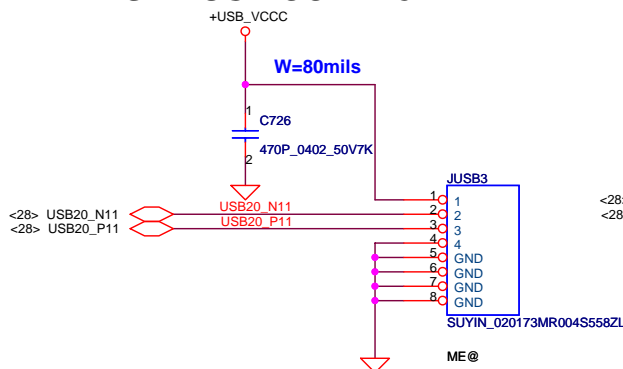
LIFT USB CONN. 2



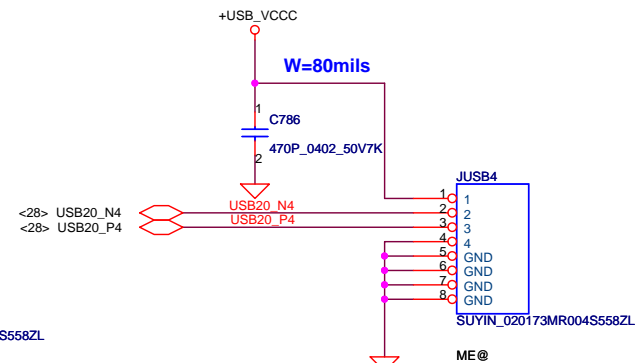
Kill Switch



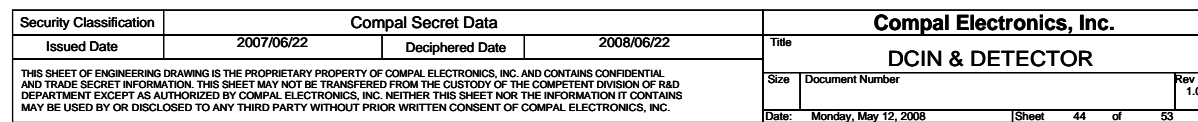
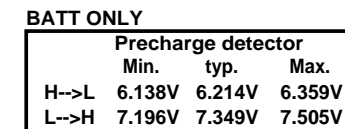
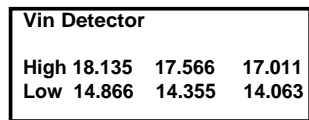
RIGHT USB CONN. 3



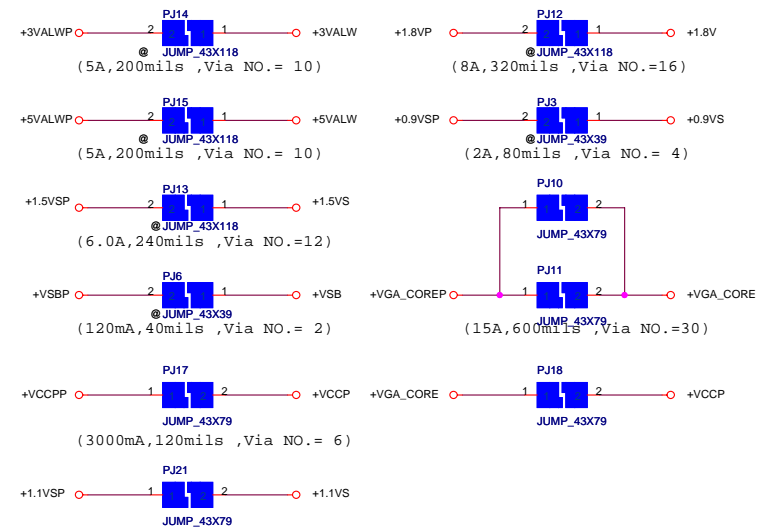
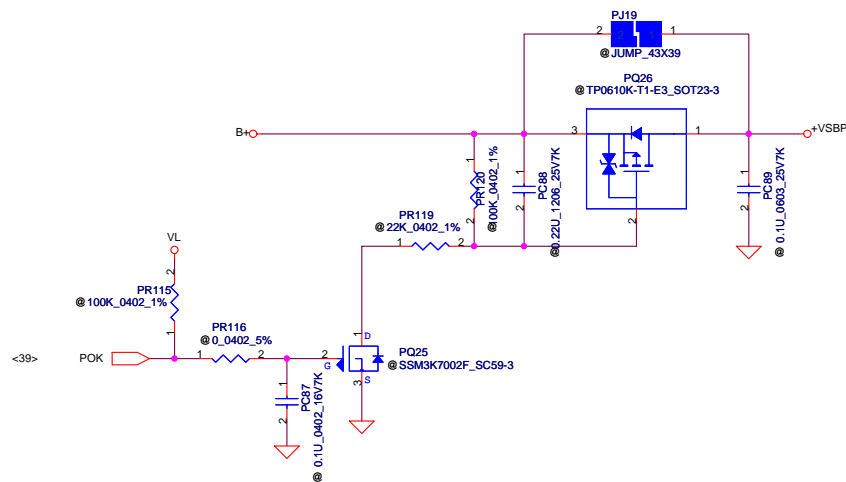
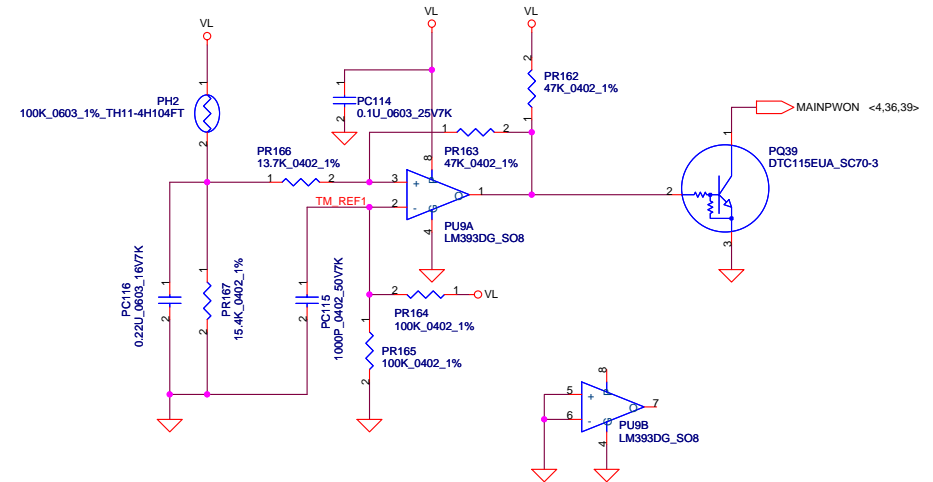
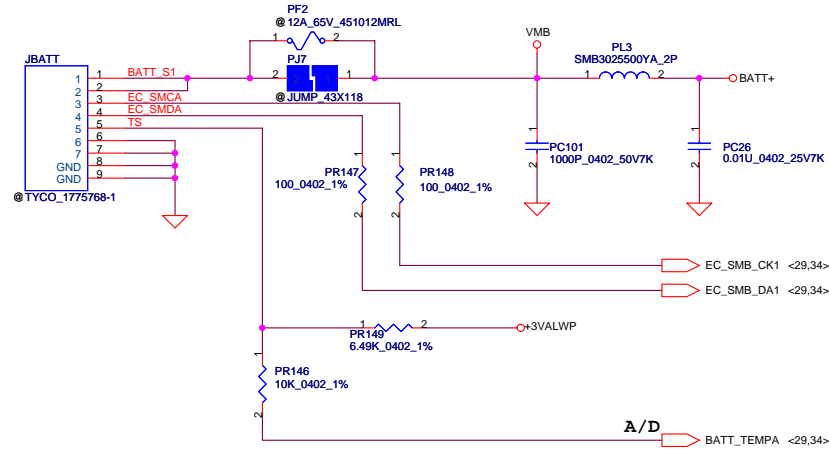
RIGHT USB CONN.4



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				Custom	JWA3/A4_LA4212P
				Date:	Wednesday, May 14, 2008
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				Rev	1.0



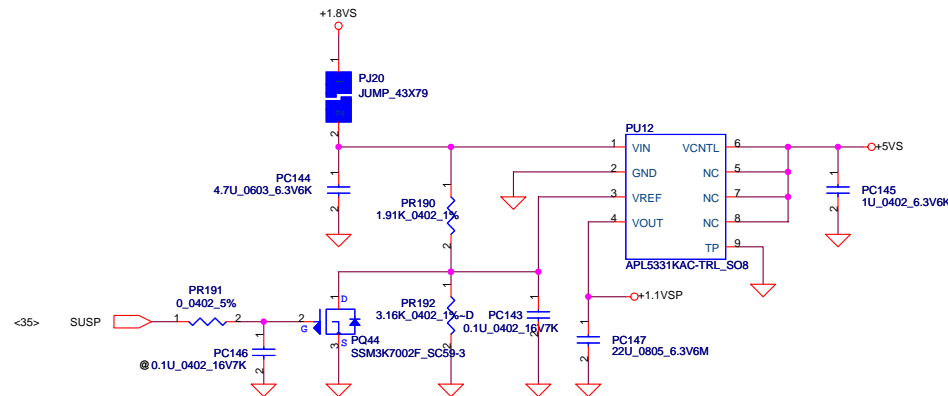
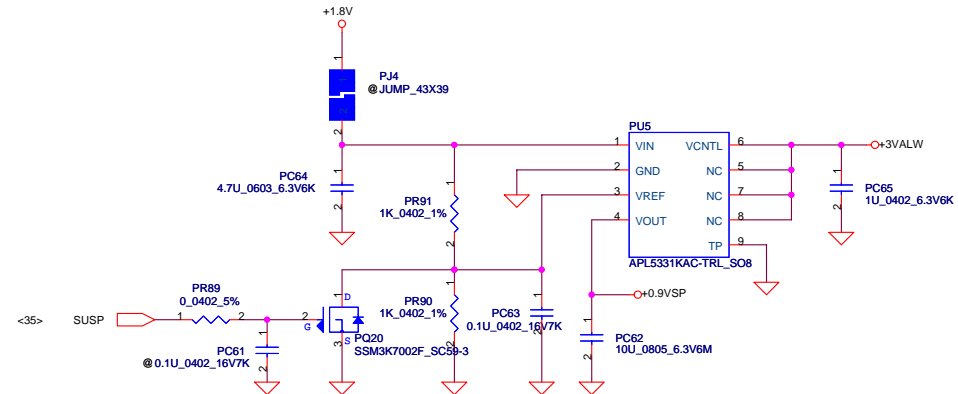
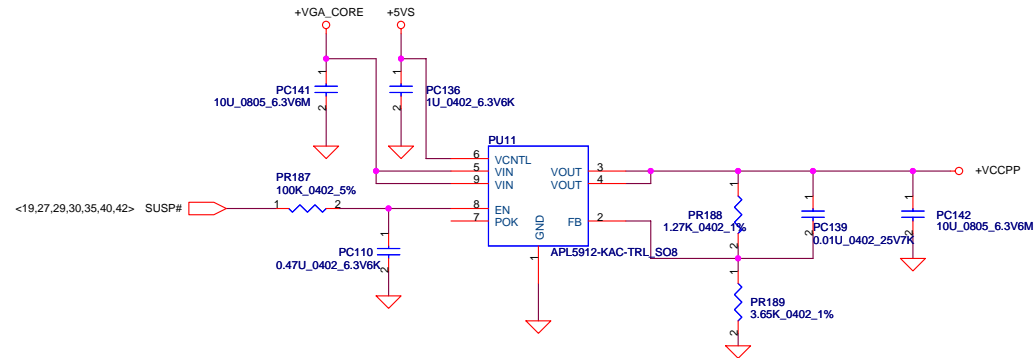
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CPU thermal protection at 92 degree C
Recovery at 56 degree C
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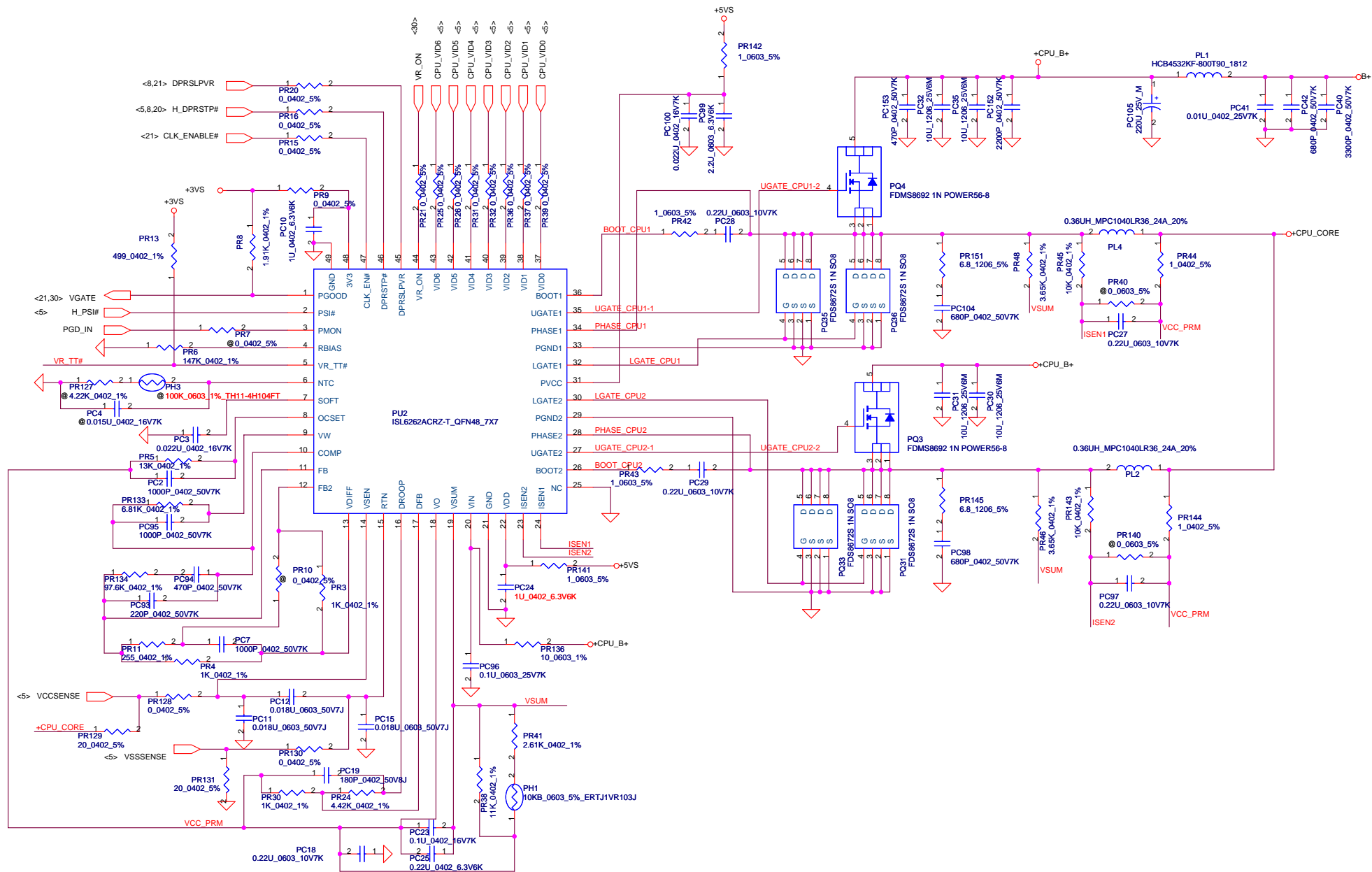


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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V

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2005/06/01		2006/06/01		Power PIR		
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