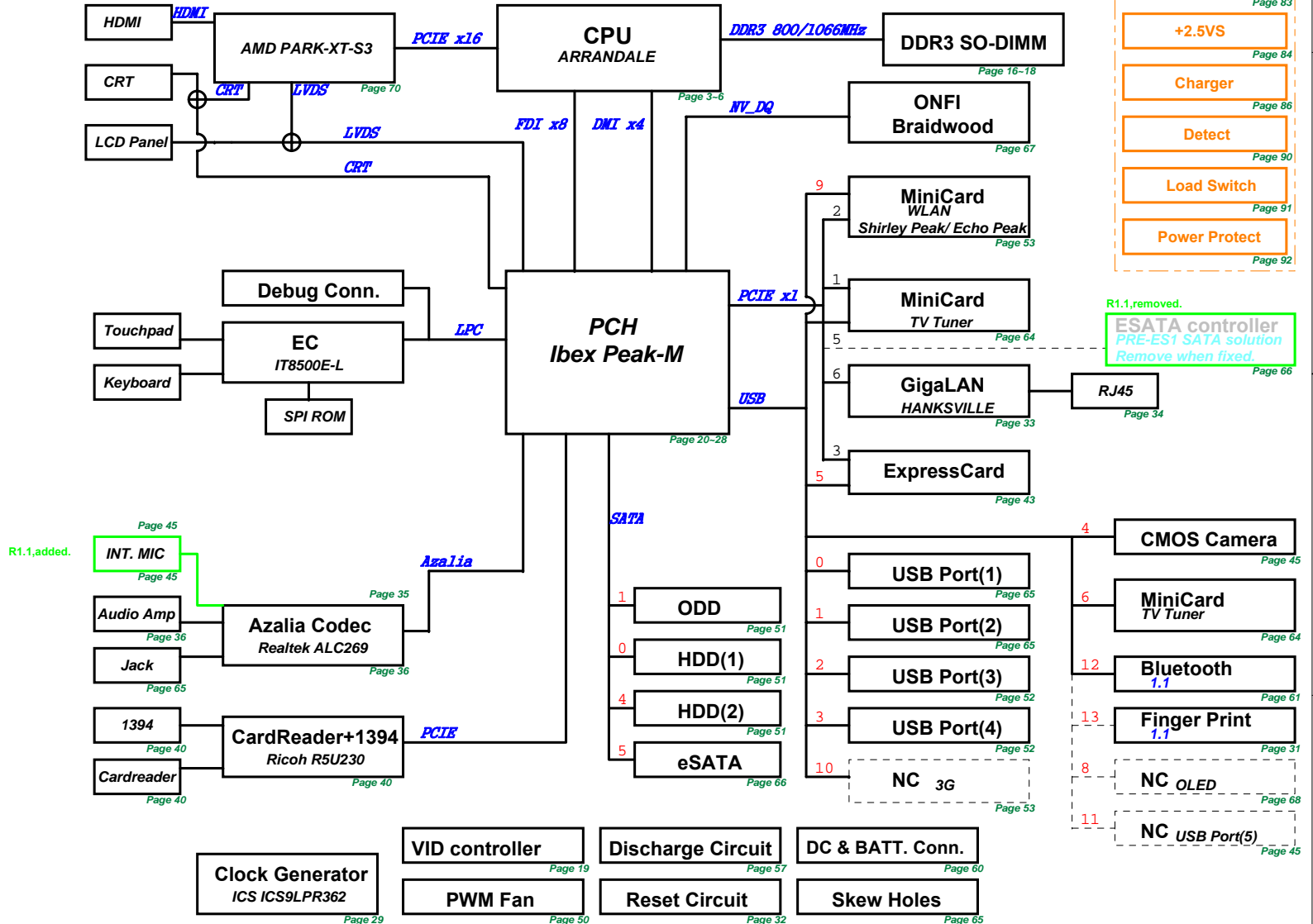


K42F SCHEMATIC For BOM Rev1.0

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51_Power_for test
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55_Power_VGFX_CORE
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58_Power On Timing--AC mode
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BLOCK DIAGRAM



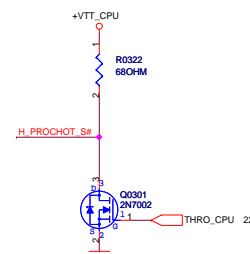
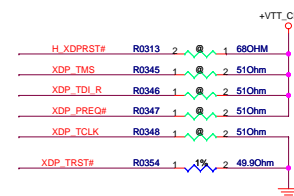
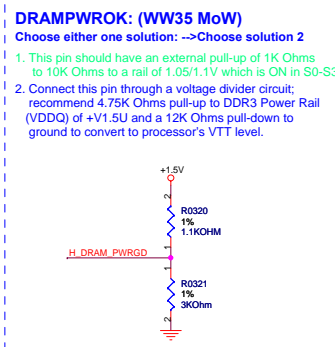
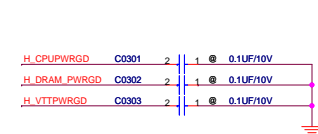
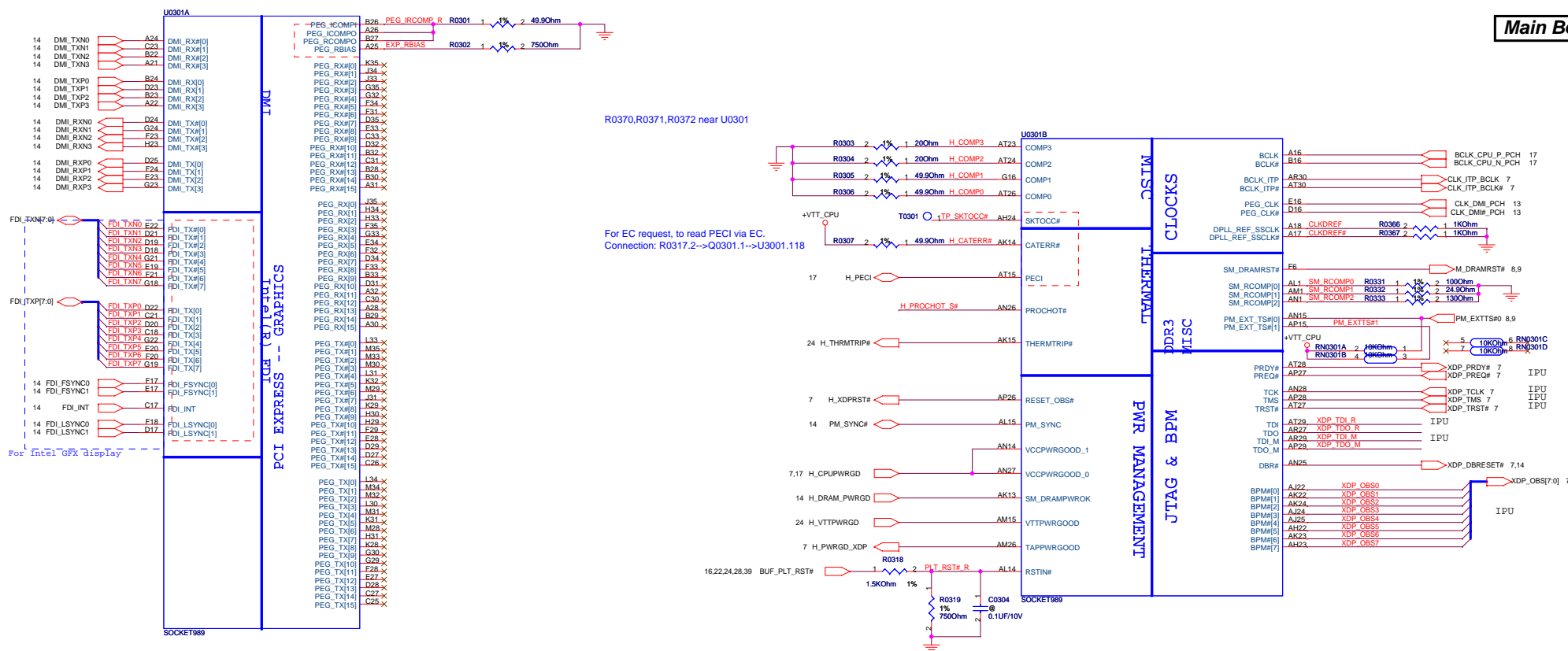
PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	GPO	-	-	+3VS
GPIO 01	GPO	-	INT TBD	+3VS
GPIO [2:5]	Native	-	EXT PU	+5VS
GPIO 06	GPO	DGPU_HPD_INTR#	INT TBD	+3VS
GPIO 07	GPO	-	INT TBD	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	Native	PM_LAPPHY_EN	EXT PU	+3VSUS
GPIO 13	GPO	-	-	+3VSUS
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS
GPIO 18	Native	CLKREQ1#_TV	EXT PU(DNI)/PD	+3VS
GPIO 19	GPO	-	-	+3VS
GPIO 20	Native	CLKREQ2#_WLAN	EXT PU(DNI)/PD	+3VS
GPIO 21	GPO	-	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	Native	LDRQ1#	INT PU	+3VS
GPIO 24	GPO	-	-	+3VSUS
GPIO 25	Native	CLKREQ3#_NEWCARD	EXT PU(DNI)/PD	+3VSUS
GPIO 26	Native	CLKREQ4#	EXT PU (Not used)	+3VSUS
GPIO 27	GPO	-	INT WEAK PU	+3VSUS
GPIO 28	GPO	BT_LED	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI) / PD(DNI)	+3VSUS
GPIO 30	Native	ME_Sus_PwrDnAck	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	GPO	-	-	+3VS
GPIO 34	Native	STP_PCI#	-	+3VS
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	GPI	DGPU_PRSNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5#	EXT PU (Not used)	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	Native	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	GPO	-	-	+3VS
GPIO 49	GPO	GPU_RST#	-	+3VS
GPIO 50	Native	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS
GPIO 52	GPO	-	-	+5VS
GPIO 53	GPO	-	INT PU	+3VS
GPIO 54	GPO	-	-	+5VS
GPIO 55	GPO	-	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SM11_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	GPO	-	-	+3VSUS
GPIO 61	Native	PM_SUS_STAT#	-	+3VSUS
GPIO 62	Native	SUS_CLK	-	+3VSUS
GPIO 63	Native	PM_SLP_S5#	-	+3VSUS
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS
GPIO 66	Native	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_OUT3	INT TBD	+3VS
GPIO 72	GPO	-	-	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	GPO	-	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SM11_DATA	EXT PU	+3VSUS

EC GPIO	Use As	Signal Name
GPA0	0	PWR_LED#
GPA1	0	CHG_LED#
GPA2		-
GPA3		-
GPA4	0	LCD_BL_PWM
GPA5	0	FAN0_PWM
GPA6		-
GPA7		-
GPB0	0	SUSC_EC#
GPB1	0	SUSB_EC#
GPB2		-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	0	A20GATE
GPB6	0	RC_IN#
GPB7	0	PM_RSMRST#
GPC0		-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	0	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5		OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0		-
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	0	EXT_SCI#
GPD4	0	EXT_SMI#
GPD5	0	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	0	VSUS_ON
GPE1	0	EGAD (IT8301 Address/Data connect)
GPE2	0	EGCS (IT8301 Cycle Start connect)
GPE3	0	EGCLK (IT8301 Clock connect)
GPE4	I	PWR_SW#
GPE5		-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPF0		-
GPF1		-
GPF2	I	EXP_GATE#
GPF3		-
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	0	THRO_CPU
GPF7		-
GPG0		-
GPG1	I	PM_SUSB#
GPG2		-
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1		-
GPH2	0	GFX_VR_ON
GPH3	0	BAT_LEARN
GPH4		-
GPH5	0	NUM_LED#
GPH6	0	CAP_LED#
GPI0		-
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	GFX_VR
GPI5	I	ALS_AD
GPI6		-
GPI7		-
GPJ0	0	CPU_VRON
GPJ1	0	PM_PWROK
GPJ2	0	VSET_EC
GPJ3	0	ISET_EC
GPJ4	0	TP_LED
GPJ5		-

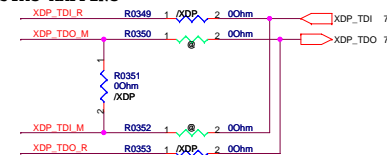
EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SusPwrDnAck
GPIO2		-
GPIO3		-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7		-
GPIO8		-
GPIO9		-
GPIO10		-
GPIO11		-
GPIO12	O	ME_PWROK
GPIO13		-
GPIO14	O	ME_SLP_M_EC#
GPIO15		-
GPIO16		-
GPIO17		-
GPIO18		-
GPIO19		-
GPIO20		-
GPIO21		-
GPIO22		-
GPIO23		-
GPIO24		-
GPIO25		-
GPIO26		-
GPIO27		-
GPIO28		-
GPIO29		-
GPIO30		-
GPIO31		-
GPIO32		-
GPIO33		-
GPIO34		-
GPIO35		-
GPIO36		-
GPIO37		-

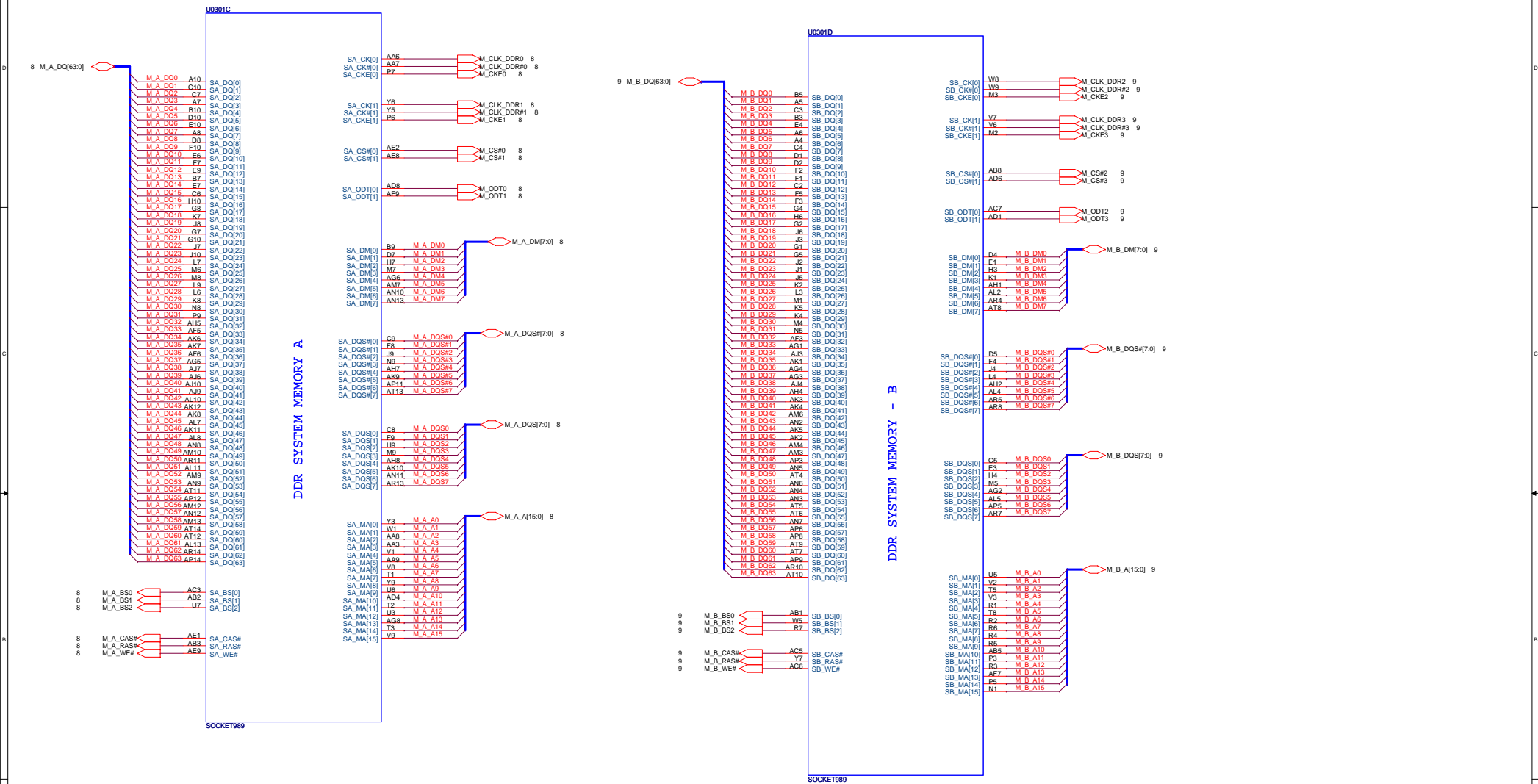
PCH Master		
SM-Bus Device	SM-Bus Address	
Clock Generator (ICS9LPR362)	1101001x	(D2)
SO-DIMM 0	1010000x	(A0)
SO-DIMM 1	1010001x	(A2)
VID Controller (ASM8272)	0011011x	(36)
WiFi/WiMax	N/A	
EC Master (SMB1)		
SM-Bus Device	SM-Bus Address	
CPU Thermal Sensor (G780)	1001100x	(98)
VGA Thermal IC (G781-1)	1001101x	(9A)

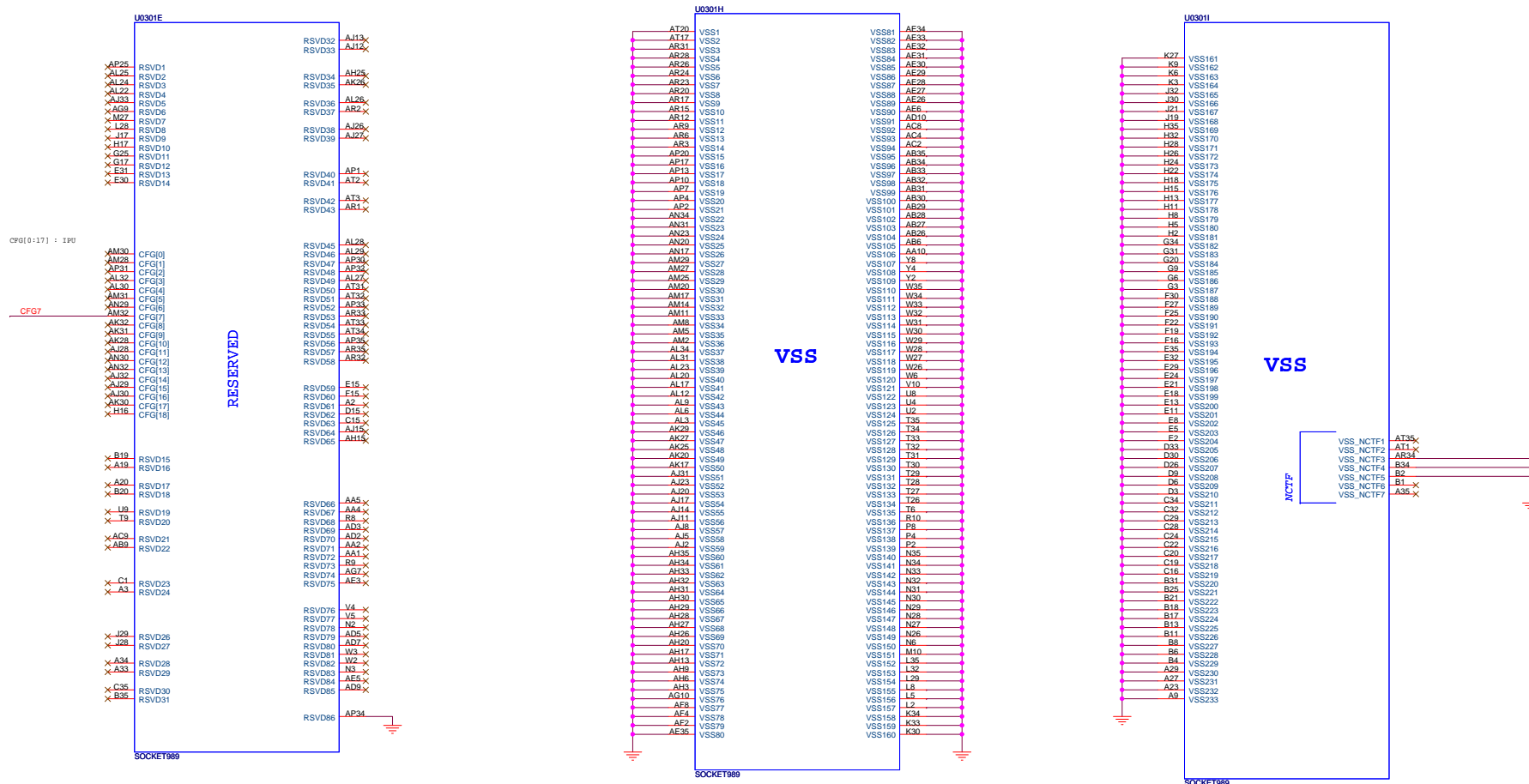
PCIE 1	Minicard TV Tuner	USB 0	USB Port (1)
PCIE 2	Minicard WLAN	USB 1	USB Port (2)
PCIE 3	Newcard	USB 2	USB Port (3)
PCIE 4		USB 3	USB Port (4)
PCIE 5	ESATA (for pre-ES1)	USB 4	CMOS Camera
PCIE 6	GLAN	USB 5	NewCard
PCIE 7		USB 6	Minicard TV Tuner
PCIE 8		USB 7	
		USB 8	
		USB 9	WLAN
		USB 10	
		USB 11	
		USB 12	Bluetooth
		USB 13	Finger Printer



JTAG MAPPING







CFG strapping information:

CFG[1:0]: PCI Express Port Bifurcation:(Clarksfield Only)
 - 11 = 1 x 16 PEG (Default)
 - 10 = 2 x 8 PEG

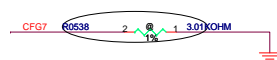
CFG[3]: PCIE Static Numbering Lane Reversal.(Arrandale Only)
 - 1:Normal Operation (Default)
 - 0:Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG[4]: Embedded DisplayPort Detection (Arrandale Only)
 - 1: Disabled - No Physical Display Port attached to Embedded DisplayPort
 - 0: Enabled - An external Display Port device is connected to the Embedded Display Port

CFG[7]: Fixed for PCI Express 2.0 jitter specifications (Clarksfield)
Clarksfield (only for early samples pre-EST-1) Connect to GND with 3.01K Ohm/5% resistor
For a common motherboard design (for AUB and CFD),
the pull-down resistor should be used. Does not impact Arrandale functionality.
Unmount if Intel has fixed this issue.

Note: (Auburndale)Hardware Straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

Note: (Clarksfield)Hardware Straps are sampled after RSTIN# de-assertion.



CFG strapping information:

For Arrandale

CFG[2:0] - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design.

CFG[3] – PCI Express* Static Lane

Numbering Reversal. Lane Reversal will be applied across all 16 Lanes.

- 1: No lane reversal
- 0: Reversal

CFG[4] - Embedded DisplayPort Detection:
This is used to detect the presence of a device on the Embedded DisplayPort.

CFG[17:5] - Reserved configuration pins.

Note: Hardware straps are sampled on the

asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.

For Clarksfield

CFG[1:0] - PCI Express* Port Bifurcation:

- 11 = 1 x16 PEG
- 10 = 2 x8 PEG

CFG[2] - Reserved Configuration pin.

CFG[3] – Reserved (Used by Arrandale Pprocessors for PCI Express* Static Lane Numbering Reversal)

CFG[11:4] - Reserved configuration pins.

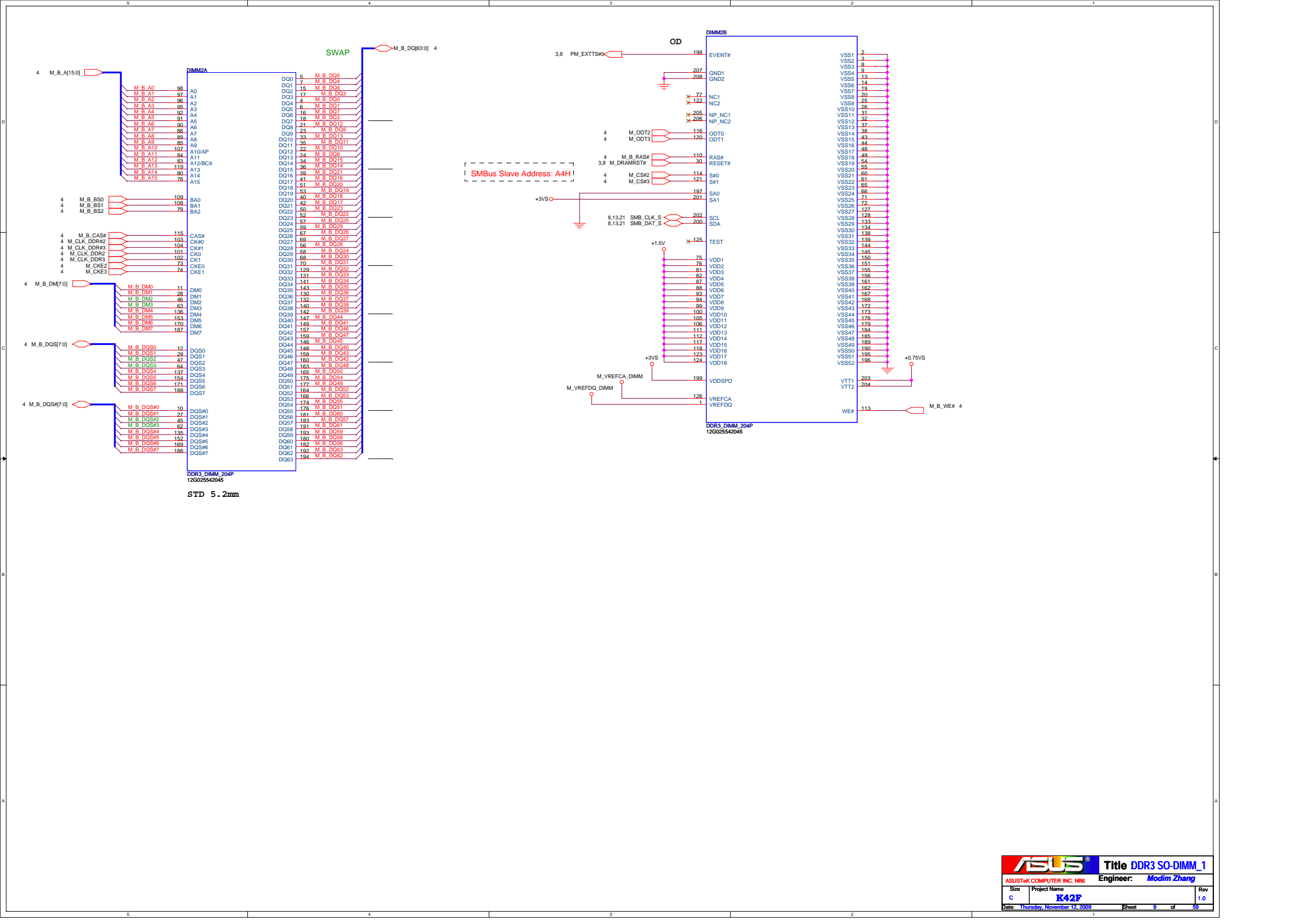
CFG[12] - N/A on Clarksfield processors.

CFG[17:13] - Reserved configuration pins.

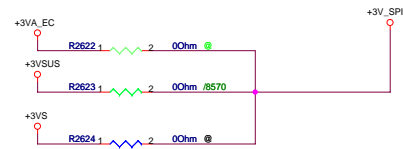
Note: Hardware straps are sampled after RSTIN# de-assertion.







PCH SPI ROM



PCH SPI ROM

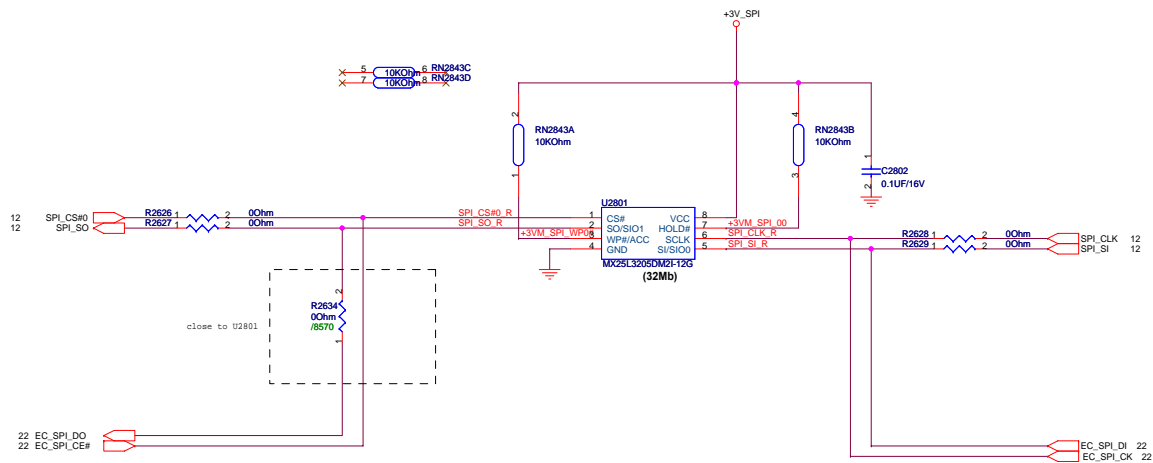


Table 2-28. Functional Strap Definitions (Sheet 1 of 5)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	This signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# de-asserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (the PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: Offset 3410h:bit 5).
INT3_3V#	Reserved	Rising edge of PWROK	This signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# de-asserts. NOTE: This signal should not be pulled low.
GNT[3]# / GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	The signal has a weak internal pull-up. Note: the internal pull-up is disabled after PCIRST# de-asserts. If the signal is sampled low, this indicates that the system is strapped to the "topblock-swap" mode (the PCH inverts A16 for all cycles targeting BIOS space). The status of this strap is readable using the Top Swap bit (Chipset Config Registers: Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	Integrated 1.05 V VRMs is enabled when high. NOTE: This signal should always be pulled high.

Table 2-28. Functional Strap Definitions (Sheet 2 of 5)

Signal	Usage	When Sampled	Comment
GNT1# / GPIO1	Boot BIOS Strap bit [1] BBS[1]	Rising edge of PWROK	This signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <div> <div>Bit11</div> <div>Bit 10</div> <div>Boot BIOS Destination</div> <div>0 1 Reserved</div> <div>1 0 PCI</div> <div>1 1 SPI</div> <div>0 0 LPC</div> </div> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC, however, all platforms with the PCH require SPI flash connected directly to the PCH SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® Management Engine or Integrated GBE LAN.

Table 2-28. Functional Strap Definitions (Sheet 5 of 5)

Signal	Usage	When Sampled	Comment
SDVO_CTRLDA TA	Digital Display Port (Port B)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port B is enabled when sampled high. When sampled low Port B is Disabled.
DDPC_CTRLDA TA	Digital Display Port (Port C)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port C is enabled when sampled high. When sampled low Port C is Disabled.
DDPD_CTRLDA TA	Digital Display Port (Port D)	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. Port D is enabled when sampled high. When sampled low Port D is Disabled.

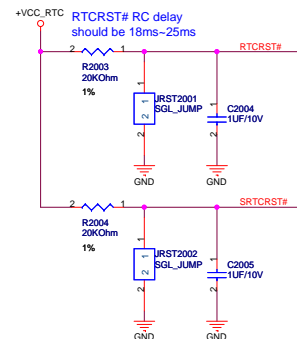
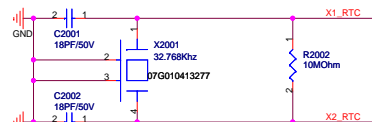
Table 2-28. Functional Strap Definitions (Sheet 3 of 5)

Signal	Usage	When Sampled	Comment
GNT[0]#	Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. This field determines the destination of accesses to the BIOS memory range. Also, controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <div> <div>Bit11</div> <div>Bit 10</div> <div>Boot BIOS Destination</div> <div>0 1 Reserved</div> <div>1 0 PCI</div> <div>1 1 SPI</div> <div>0 0 LPC</div> </div> NOTE: If option 00 LPC is selected, BIOS may still be placed on LPC, however, all platforms with the PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debug/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GBE LAN.
GNT2# / GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	This Signal has a weak internal pull-up. Note that the internal pull-up is disabled after PCIRST# de-asserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
NV_ALE	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high.

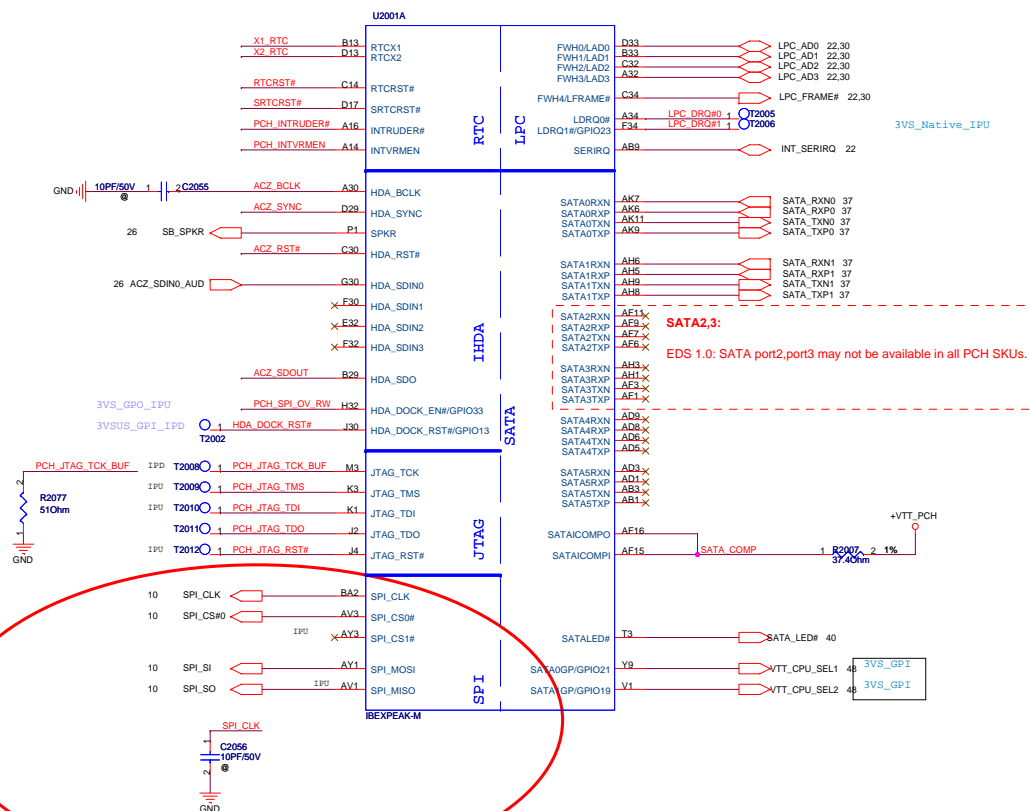
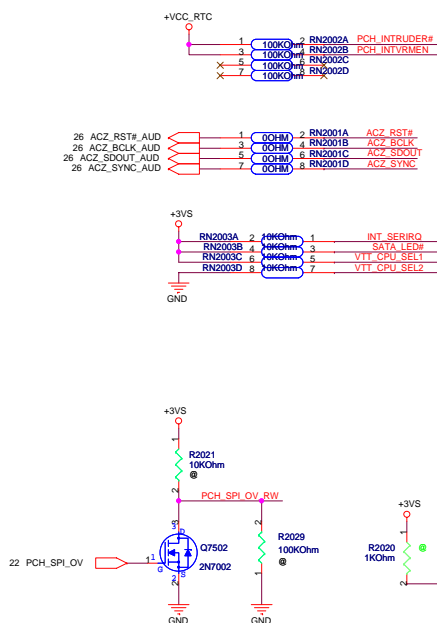
Table 2-28. Functional Strap Definitions (Sheet 4 of 5)

Signal	Usage	When Sampled	Comment
HDA_DOCK_E N# / GPIO[33]	Flash Descriptor Security Override / ME Debug Mode	Rising edge of PWROK	Signal has a weak internal pull-up. If strap is sampled high, the security measures defined in the Flash Descriptor will be in effect (default). If sampled low, the Flash Descriptor Security will be overridden. This strap should only be asserted low using external pull down in manufacturing/ debug environments ONLY. NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel® Management Engine after chipset bringup and disable runtime Intel® Management Engine features. This is a debug mode and must not be asserted after manufacturing/debug.
SPI_MOSI	TPM Functionality Disable	Rising edge of MEPWROK	This signal has a weak internal pull-down resistor. This signal must be sampled low.
NV_CLE	DMI Termination Voltage	Rising edge of PWROK	This signal has a weak internal pull-down.
HDA_SDO	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull down. NOTE: This signal should not be pulled high.
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull up. Note that the weak internal pull-up is disabled after RSMRST# de-asserts. NOTE: This signal should not be pulled low.
GPIO27	Reserved	Rising edge of RSMRST# pin	This signal should be left as a No Connect.
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	This signal has a weak internal pull down. On-Die PLL VR is supplied by 1.5 V when sampled high; 1.8 V when sampled low.
GPIO15	Reserved	Rising edge of RSMRST# pin	Low = Intel® Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel® Management Engine Crypto TLS cipher suite with confidentiality This signal has a weak internal pull down. NOTE: A strong pull up may be needed for GPIO functionality.
L_DOC_DATA	LVDS	Rising Edge of PWROK	This signal has a weak internal pull-down. Note that the weak internal pull-down is disabled after PLTRST# de-asserts. LVDS is enabled when sampled high. When sampled low LVDS is Disabled.

<i>CMOS Settings</i>	<i>JRST2001</i>	<i>TPM Settings</i>	<i>JRST2002</i>
<i>Clear CMOS</i>	<i>Shunt</i>	<i>Clear ME RTC Registers</i>	<i>Shunt</i>
<i>Keep CMOS</i>	<i>Open (Default)</i>	<i>Keep ME RTC Registers</i>	<i>Open (Default)</i>



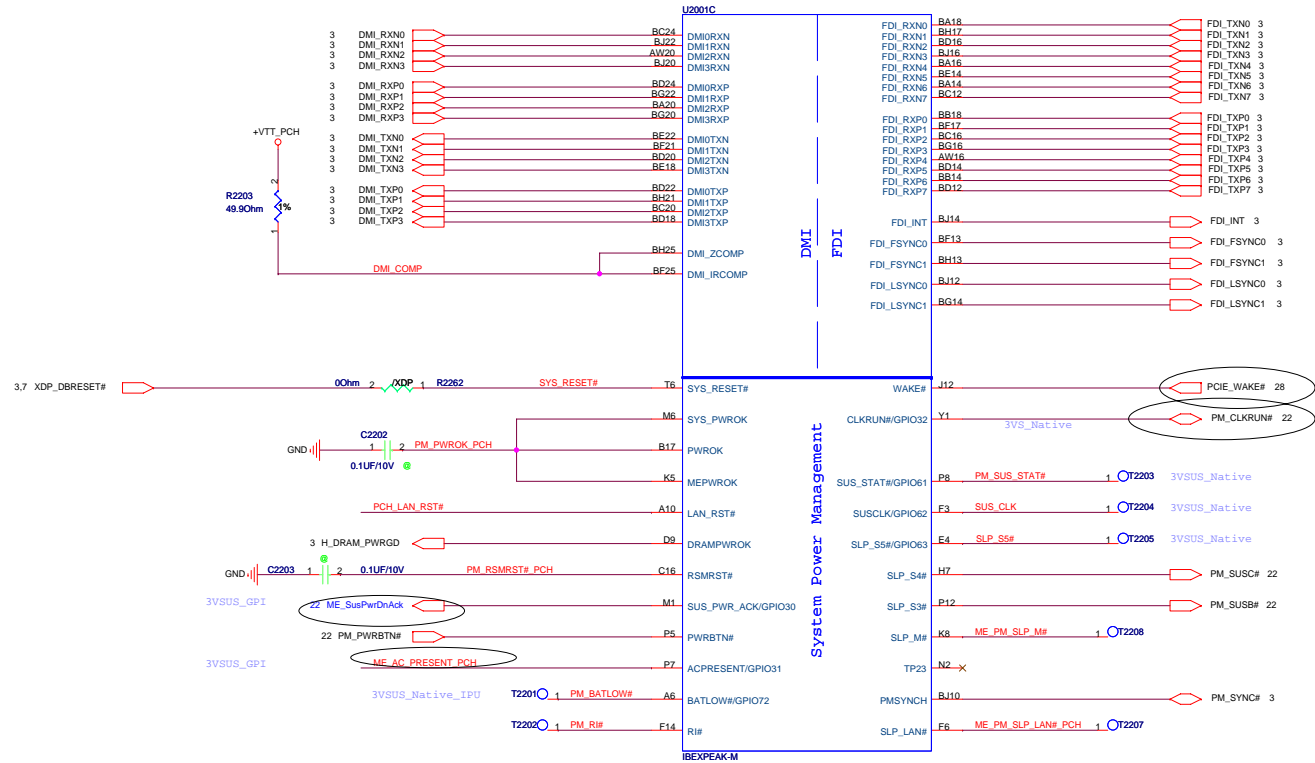
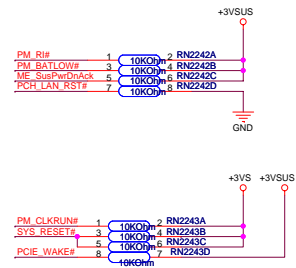
Strap information:		
	H	L
PCI_STRAP: Select VCCVBM 1.5V or 1.8V (IPD)	1.5V	1.8V
SR_STRAP: No reboot strap (IPD)	No reboot	Disable No reboot
FW_STRAP_OV_BW: (IPD)	No Flash ME FW	Flash ME FW
FW_STRAP_IPWM strap: (IPD)	Enable	Disable
FW_STRAP_INTVBM Integrated 1.05 V VBM Enable /Disable	Enable	Disable



PCH SPI ROM

CUT OFF


```
pre-ES1 not support
Reversal Feature
```



R1.1,item L15

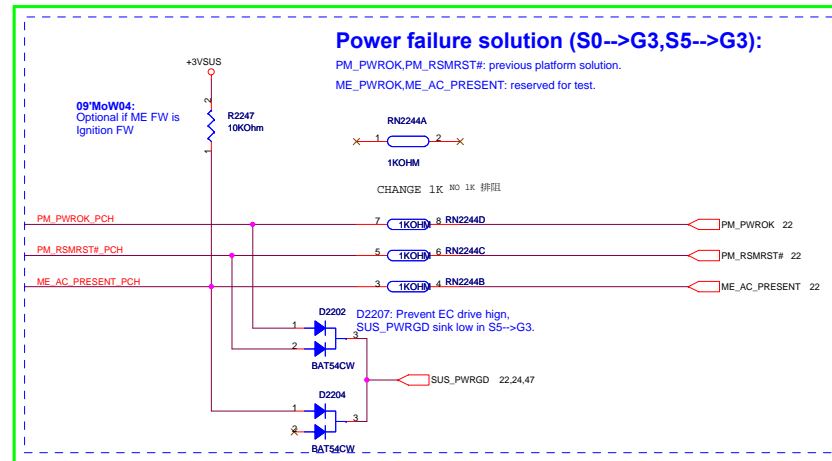


Table 112. Intel ME-EC Interaction Signal List with and without M3 Support

Signal Name	Platform with M3 Support (e.g., Intel® AMT)	Platform without M3 Support (e.g., Intel® ME Ignition Firmware)
SUS_PWR_DN_ACK (GPIO30)	Required	Required
ACPRESENT (GPIO31)	Required	Required Note: Optional if Intel ME is Ignited, Intel Ignition Firmware
SLP_M#	Required	Optional (Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_M# becomes required from Intel's ME-EC perspective.
SLP_S3#	Optional	Required Note: If SLP_M# is routed from PCH to EC, then SLP_S3# can be optional from Intel ME-EC perspective

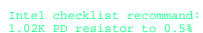
NOTE: Optional means that these signals are optional from Intel ME-EC interaction point of view. However, they are platform critical signals and are still required to be routed on the platform.

ME Ignition Firmware is for 2MB SPI core, only PM55 can support on it.

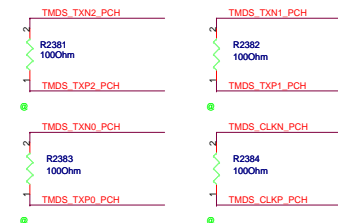
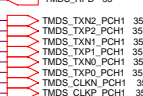


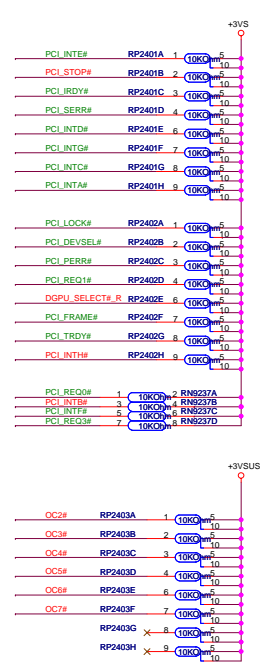
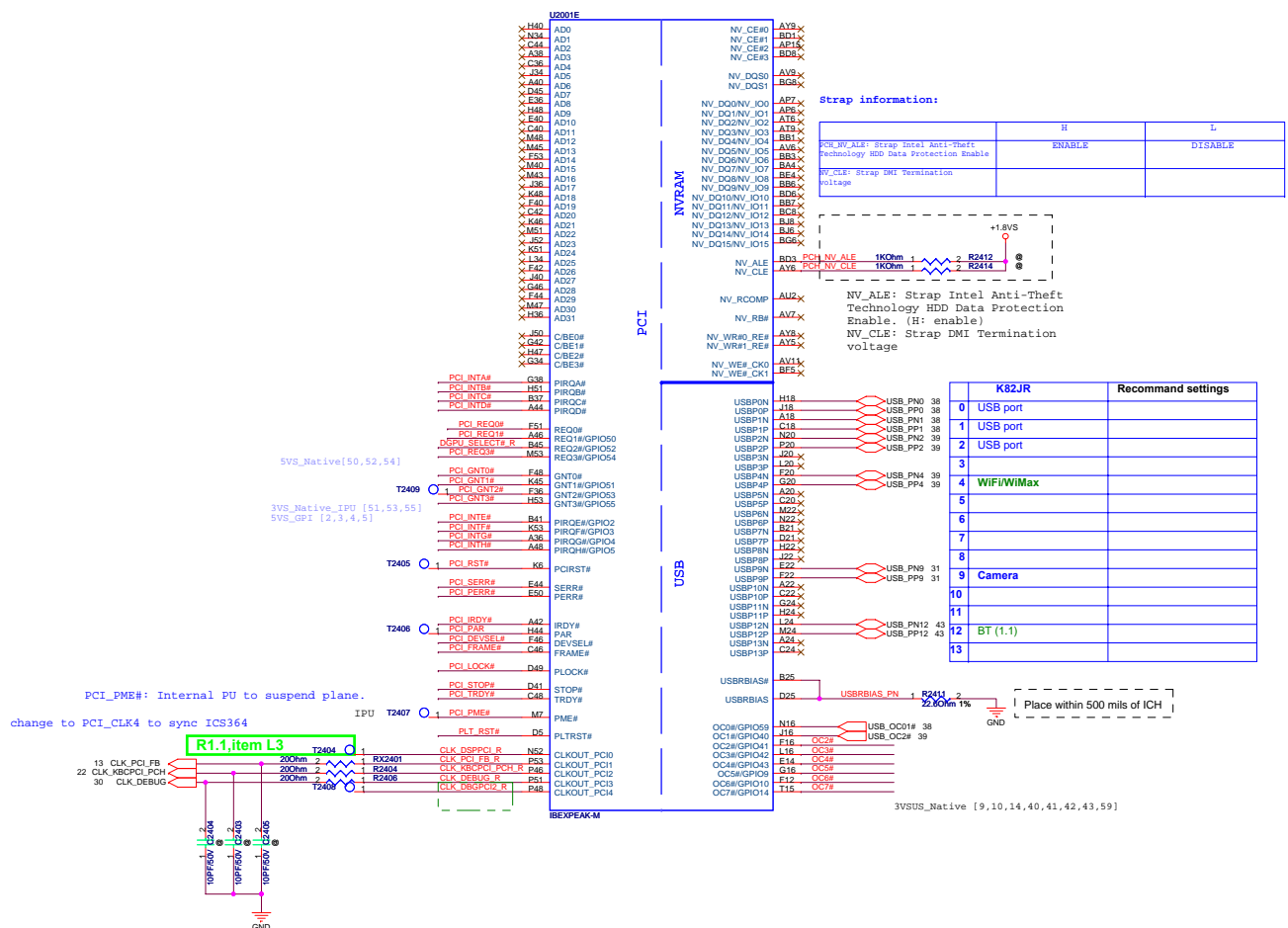
1. NC:
LVDSA_DATA [3:0], LVDSA_DATA# [3:0],
LVDSA_CLK, LVDSA_CLK#, LVDSB_DATA [3:0],
LVDSB_DATA# [3:0], LVDSB_CLK, LVDSB_CLK#
L_VDD_EN, L_BKLTEN, L_BKLTCTL, LVD_VREFH
LVD_VREFL, LVD_IBG, LVD_VBG

2. Connected to GND:
VccALVDS,VccTX LVDS



1. **NC:**
CRT_RED,CRT_GREEN,CRT_BLUE
CRT_HSYCN,CRT_VSYNC
2. **1-k Ω \pm 0.5% pull-down to GND:**
DAC_IREF
3. **Connected to GND:**
CRT_ITRN
4. **Connect to +V3.3:**
VCCADAC





GNT0#,GNT1#: Boot BIOS Strap.		
Boot BIOS Strap		
PCI_GNT0#	PCI_GNT1#	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved
1	1	SPI (PCH)

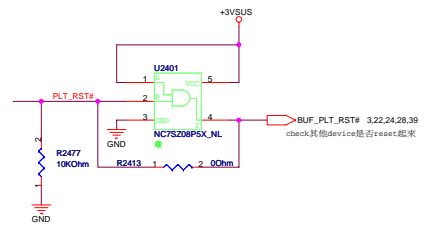
Sampled on rising edge of PWROK.

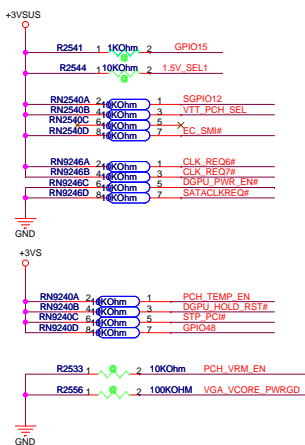
PCI_GNT0# R2440 1 2 1KΩ

PCI_GNT1# R2441 1 2 1KΩ

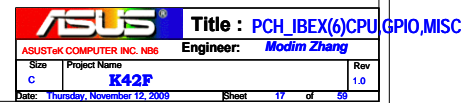
GNT3#: A16 swap override Strap/ Top-Block swap override jumper	
Low=Enabled A16 swap override/ Top-Block swap override	
High=Default	

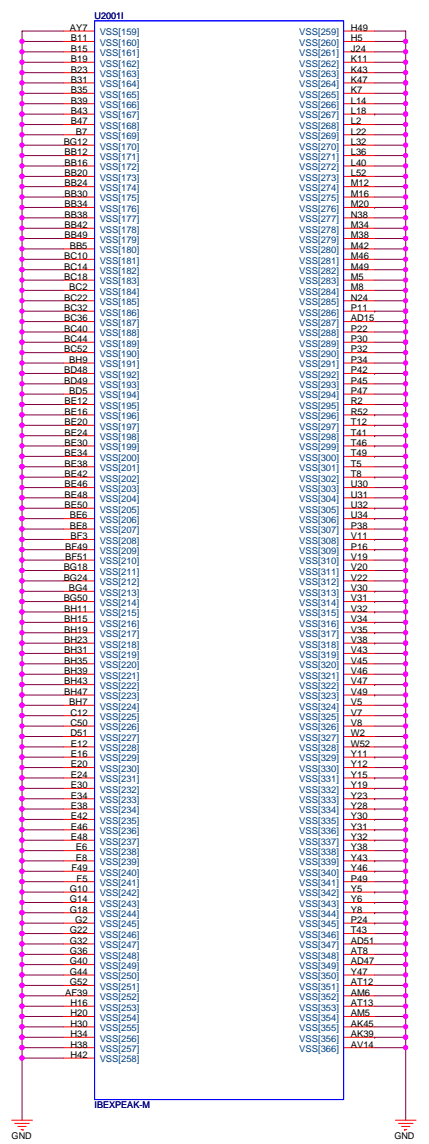
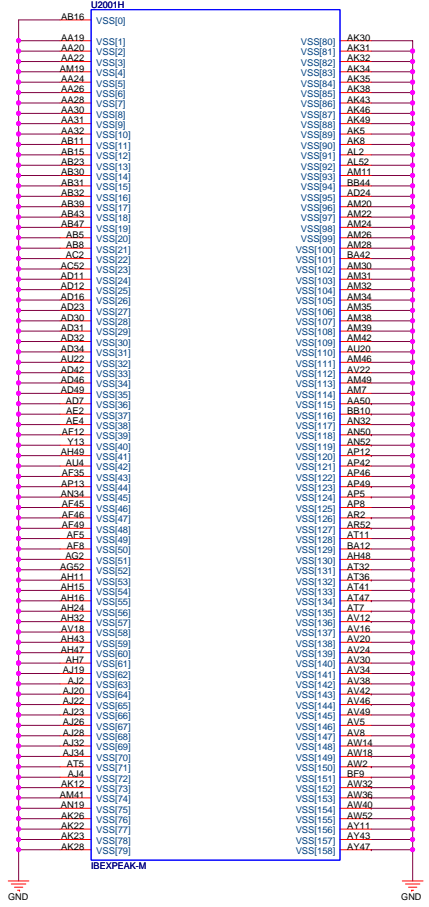
PCI_GNT3# R2444 1 2 1KΩ

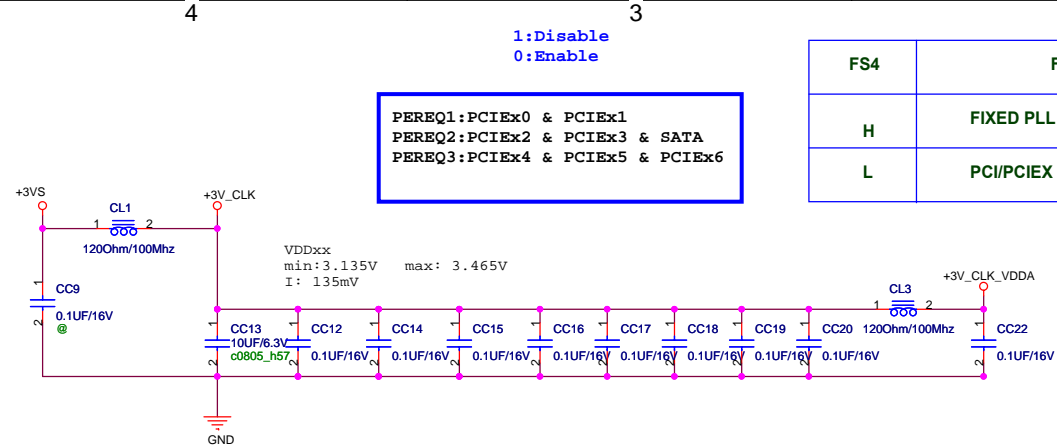




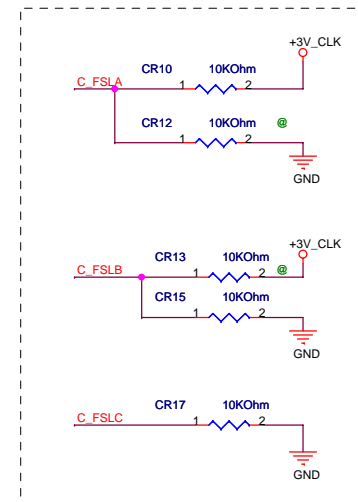
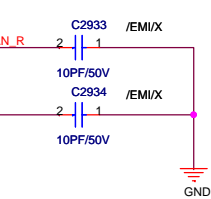
POWER按照提供的default值調節電壓




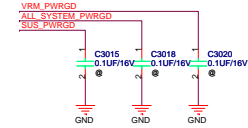




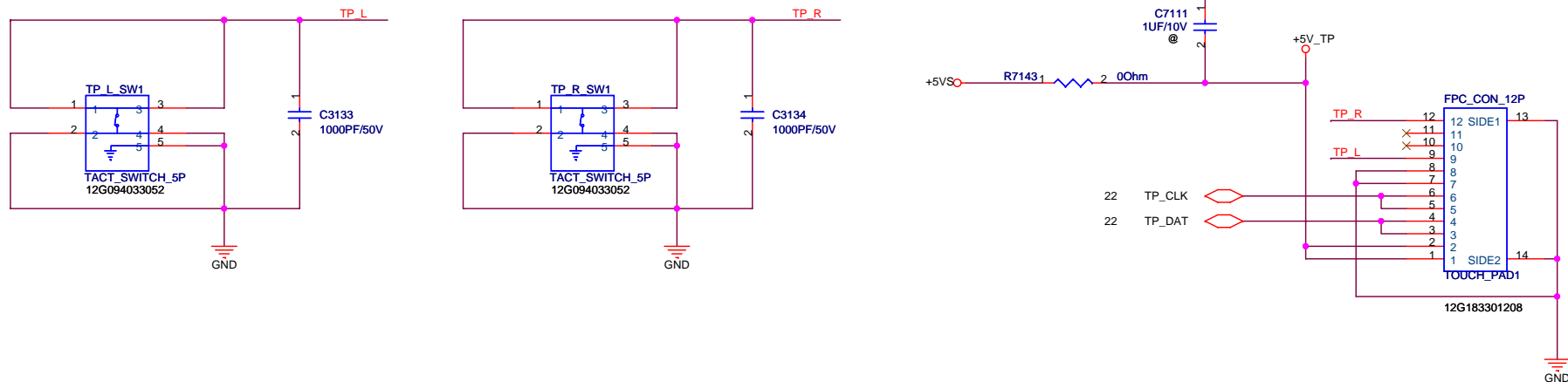
```
PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6
```



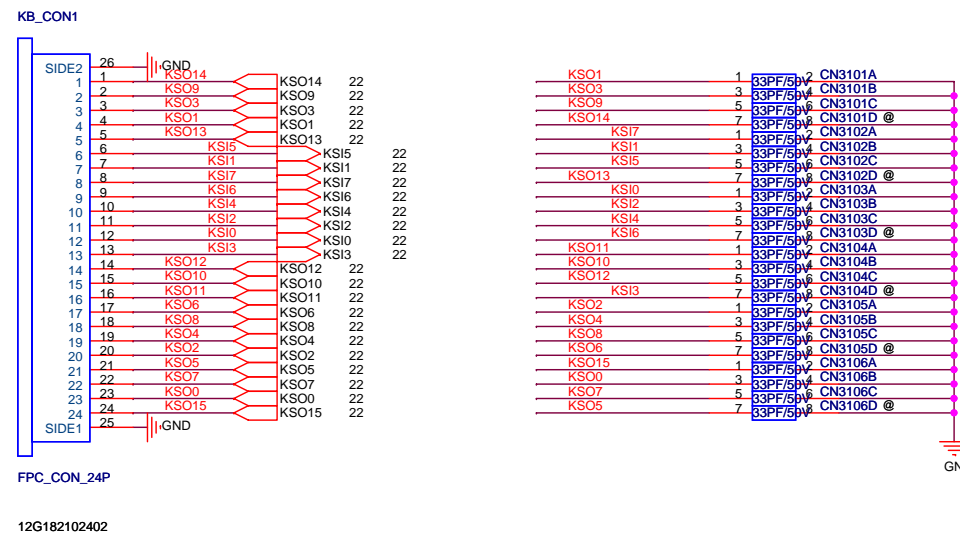
<Variant Name>			
		Title : ICS9LPRS427C	
ASUSTek Computer INC.		Engineer: <u>Modim Zhang</u>	
Size	Project Name		Rev
A3	K42F		1.0
Date:	Thursday, November 12, 2009	Sheet	21 of 59



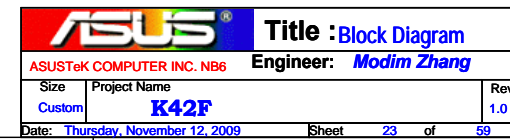
TouchPad



Keyboard Connector



<Variant Name>

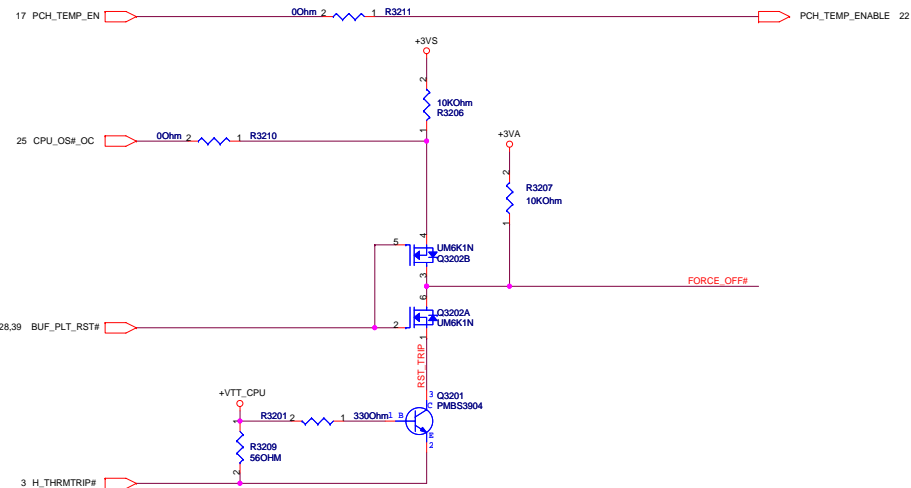


Thermal Policy

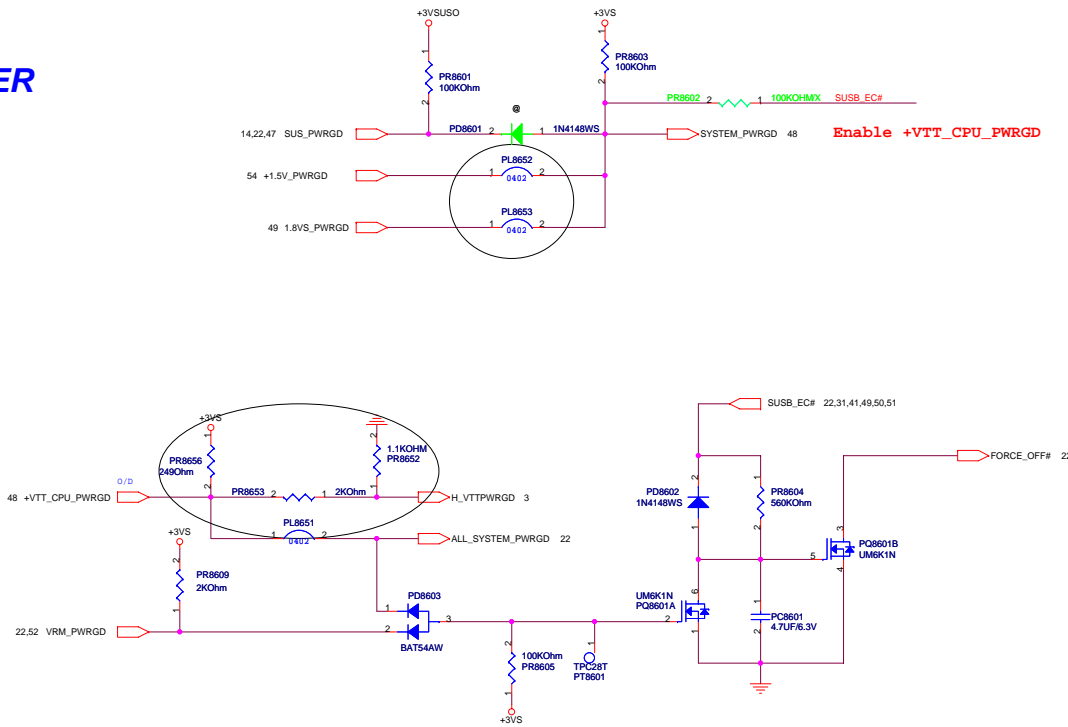
Input 1(sensor)

Input 2(thermtrip)

Output (shut down)

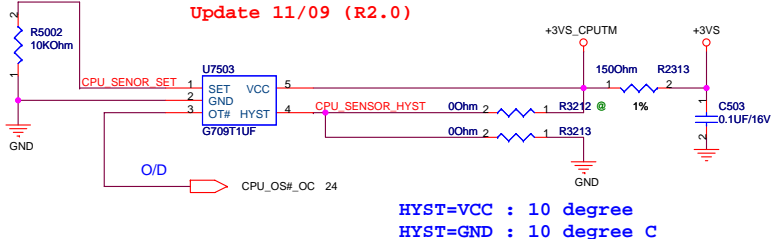


POWER GOOD DETECTOR



GPU Thermal Sensor

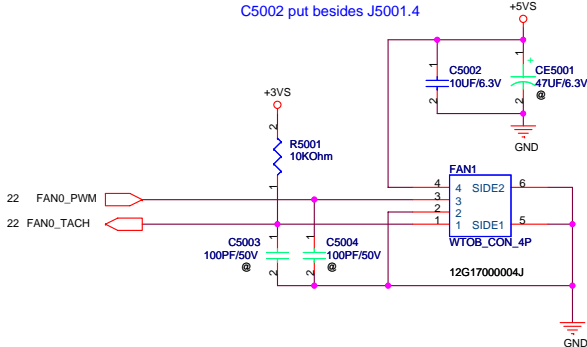
CPU Thermal Sensor

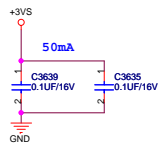


U7503 under CPU socket

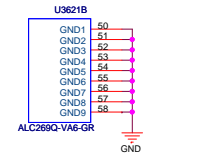
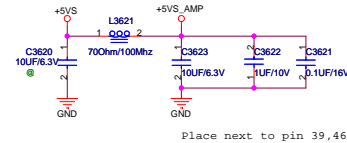
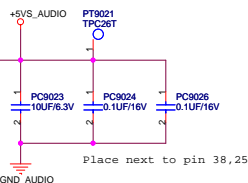
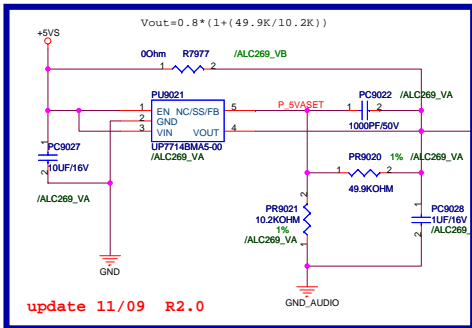
PWM Fan

Remove diode(+5Vs to GND)
for using 4-wires PWM FAN.

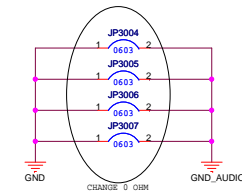




Close to pin1,9

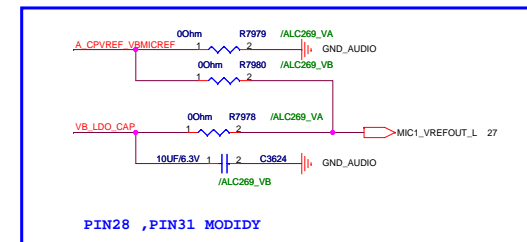


For EMI

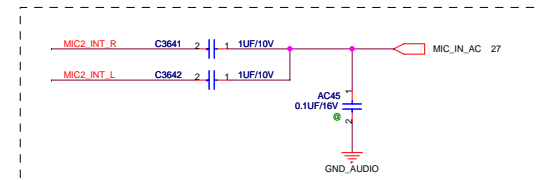


ANALOG MOAT

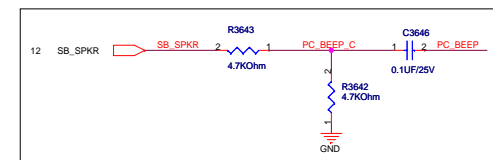
update 11/09 R2.0



INTERNAL MIC



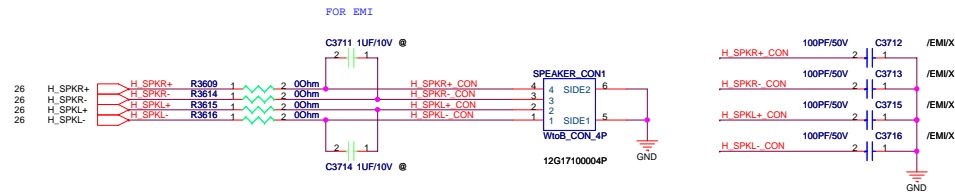
PC BEEP



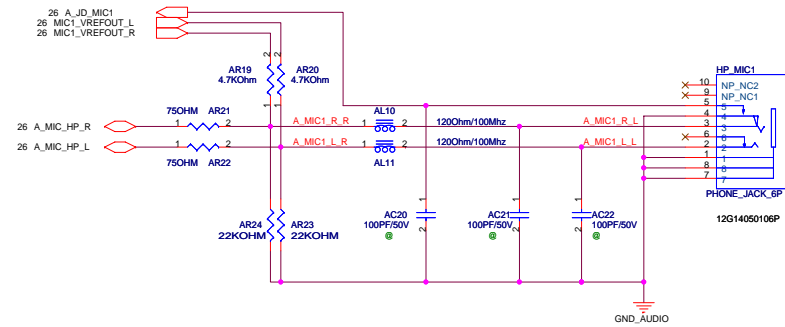
<Variant Name>

ASUS		Title : CODEC ALC 269	
ASUSTeK COMPUTER INC. NB2		Engineer: Modim Zhang	
Size C	Project Name K42F	Date: Thursday, November 12, 2009	Rev 1.0
Sheet 26 of 59			

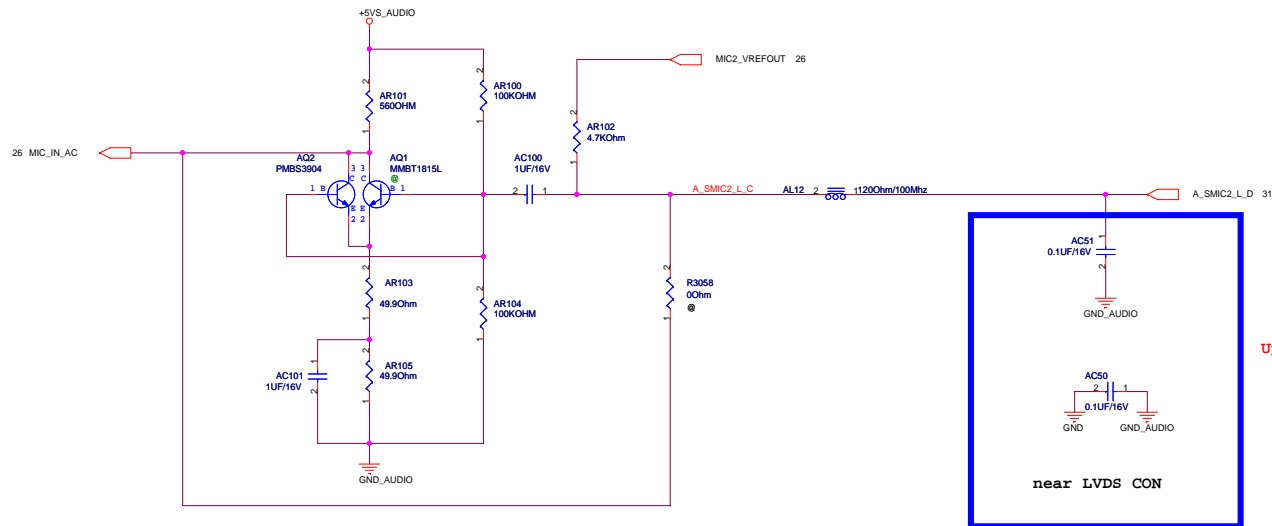
SPEAKER



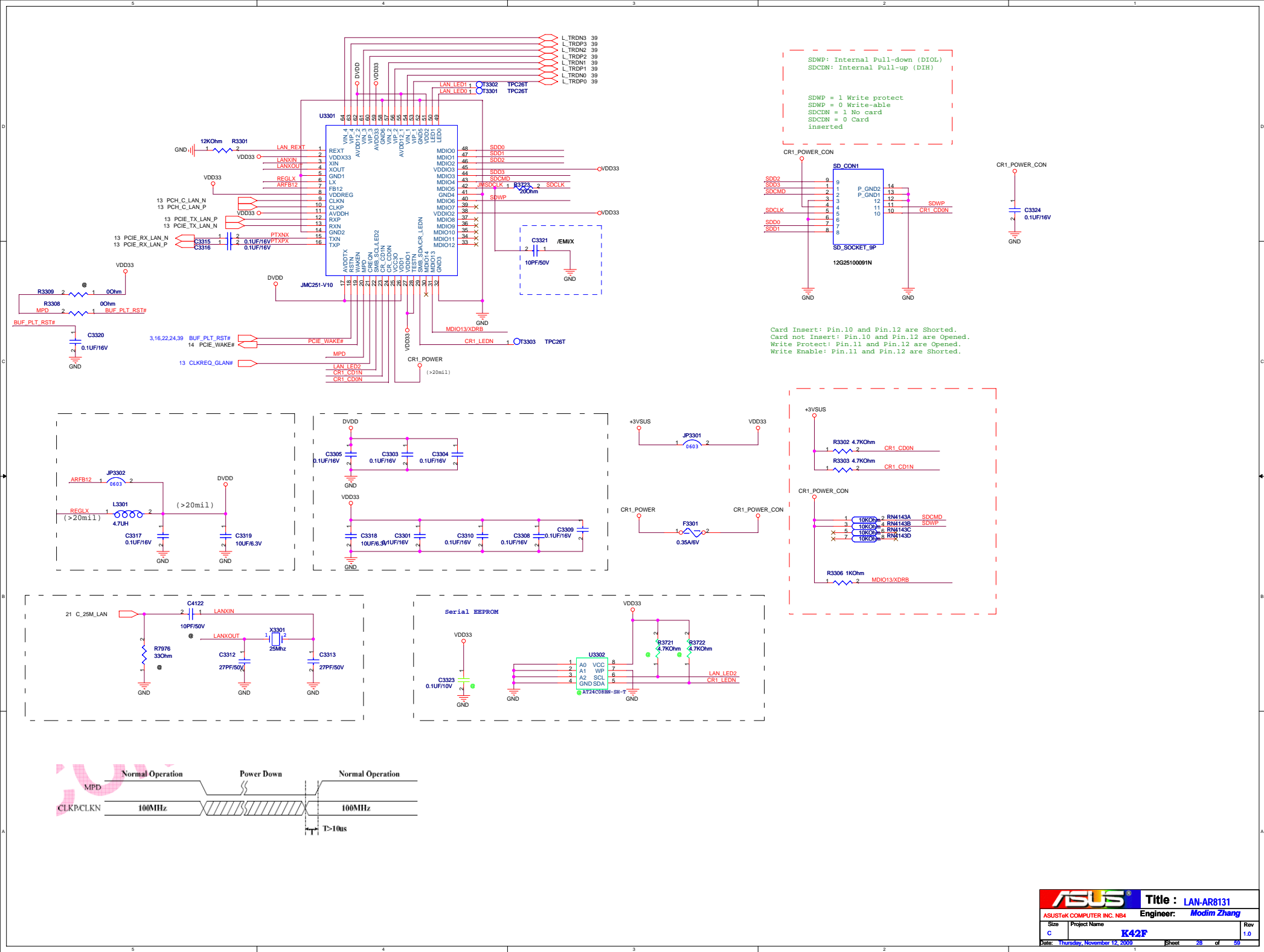
HP and MIC

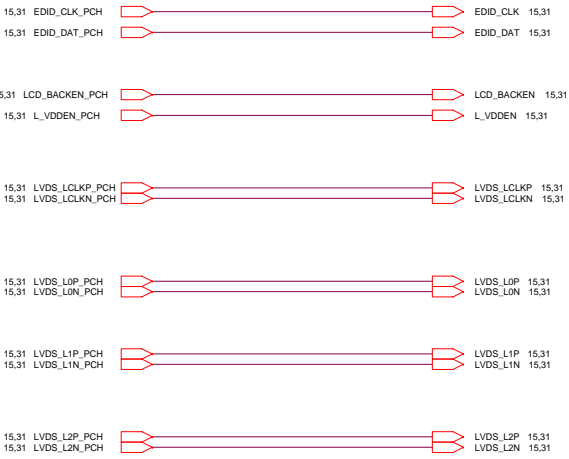


Internal MIC and AMP

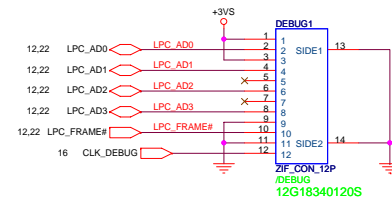


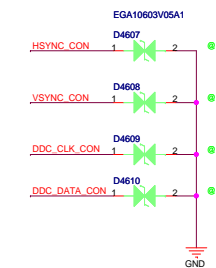
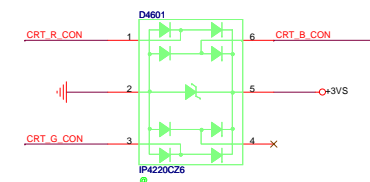
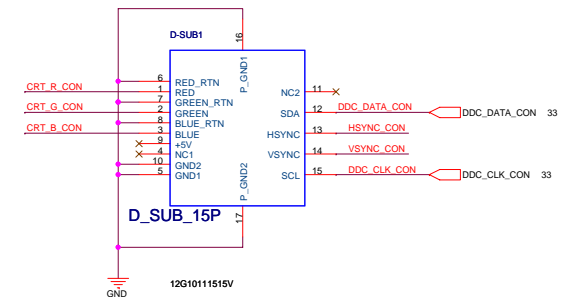
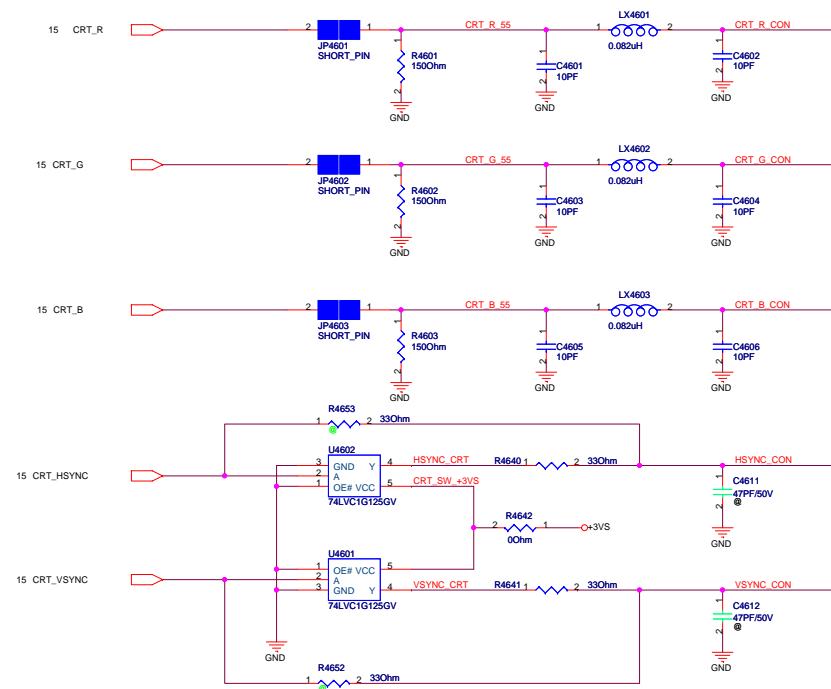
Update 11/09 R2.0





LPC Debug Port



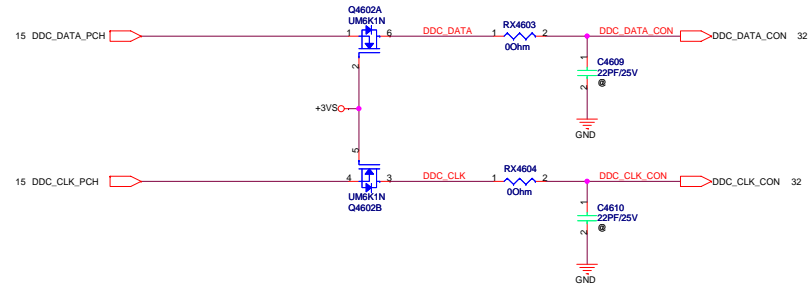
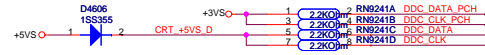


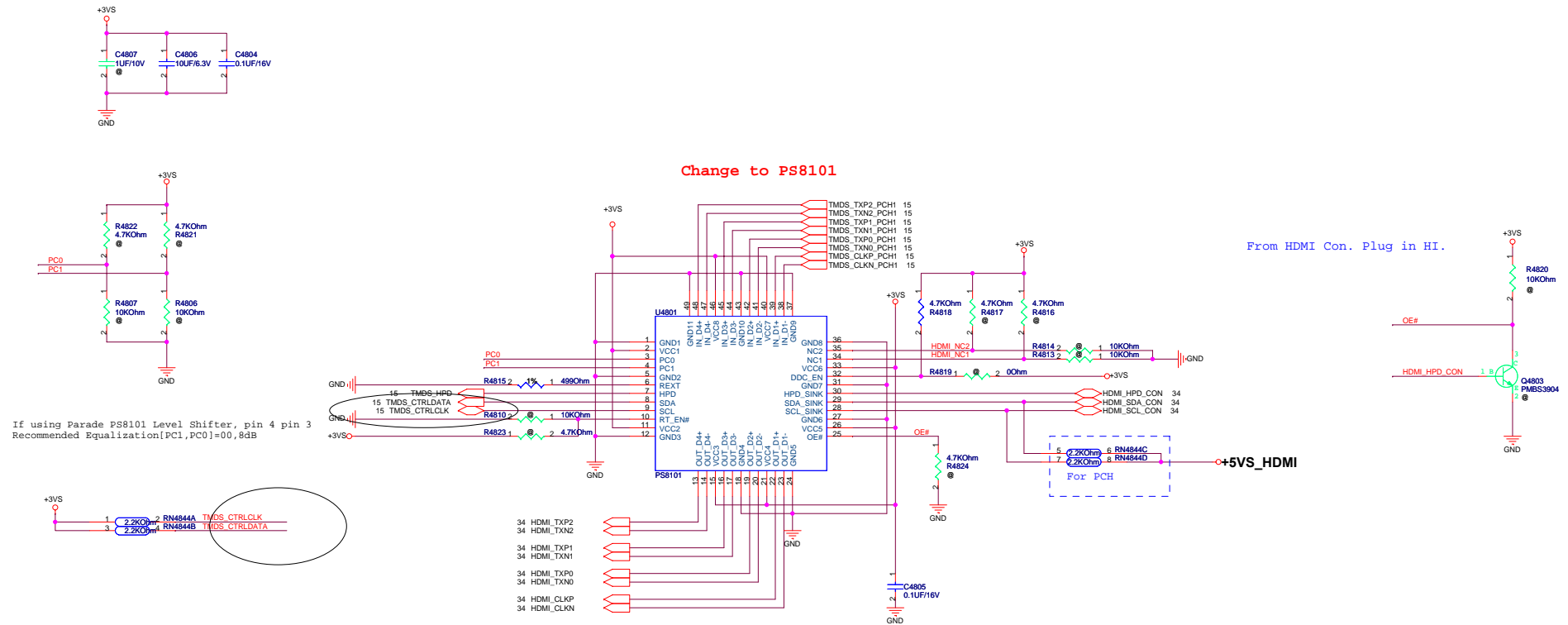
15,32 CRT_VSYNC_PCH
15,32 CRT_HSYNC_PCH

CRT_VSYNC 15,32
CRT_HSYNC 15,32

15,32 CRT_R_PCH
15,32 CRT_G_PCH
15,32 CRT_B_PCH

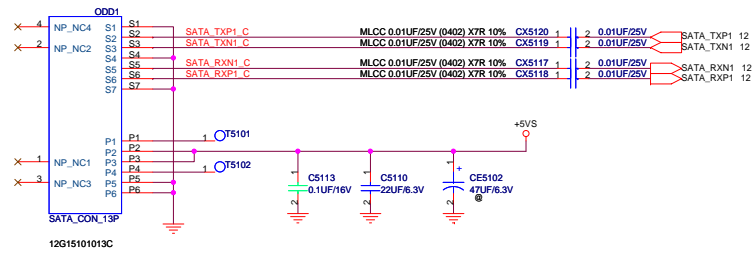
CRT_R 15,32
CRT_G 15,32
CRT_B 15,32



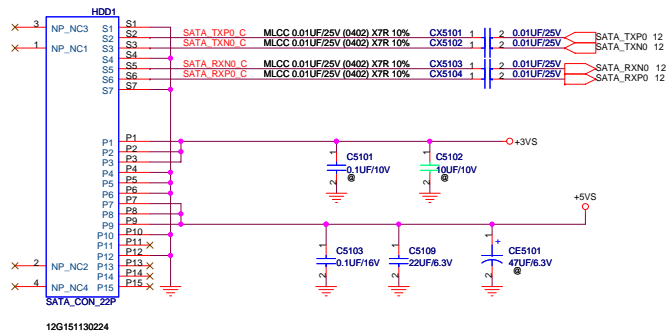




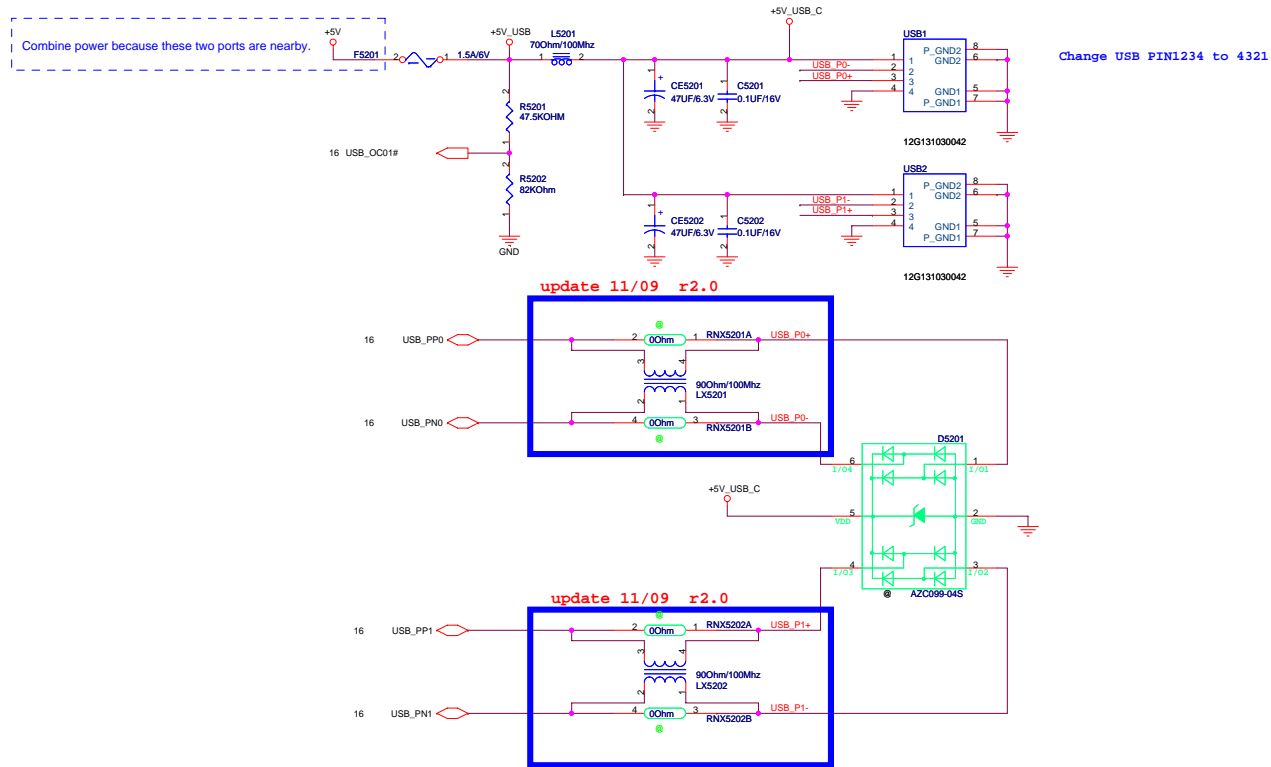
ODD

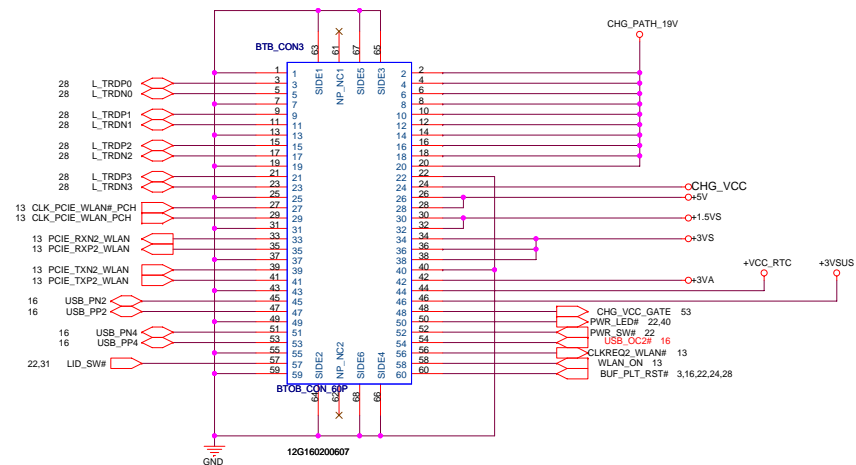


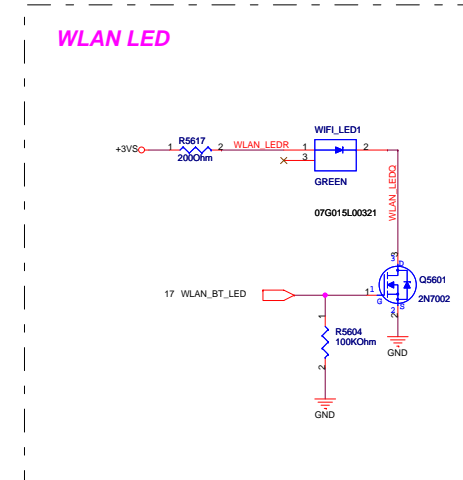
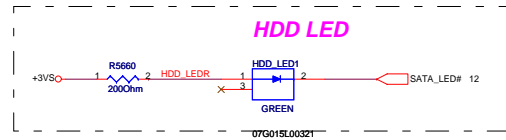
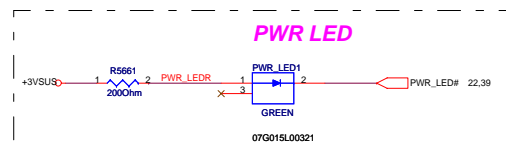
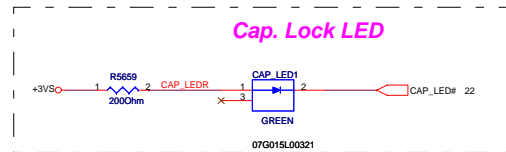
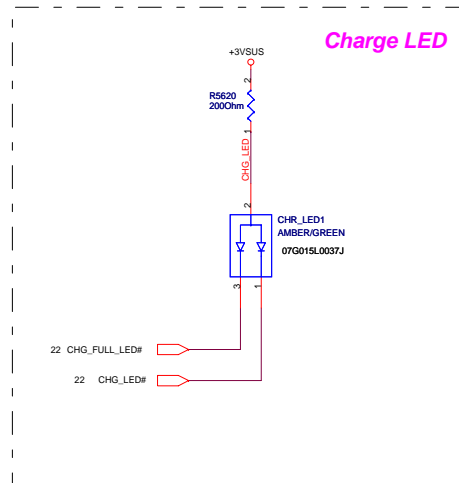
HDD (1st)



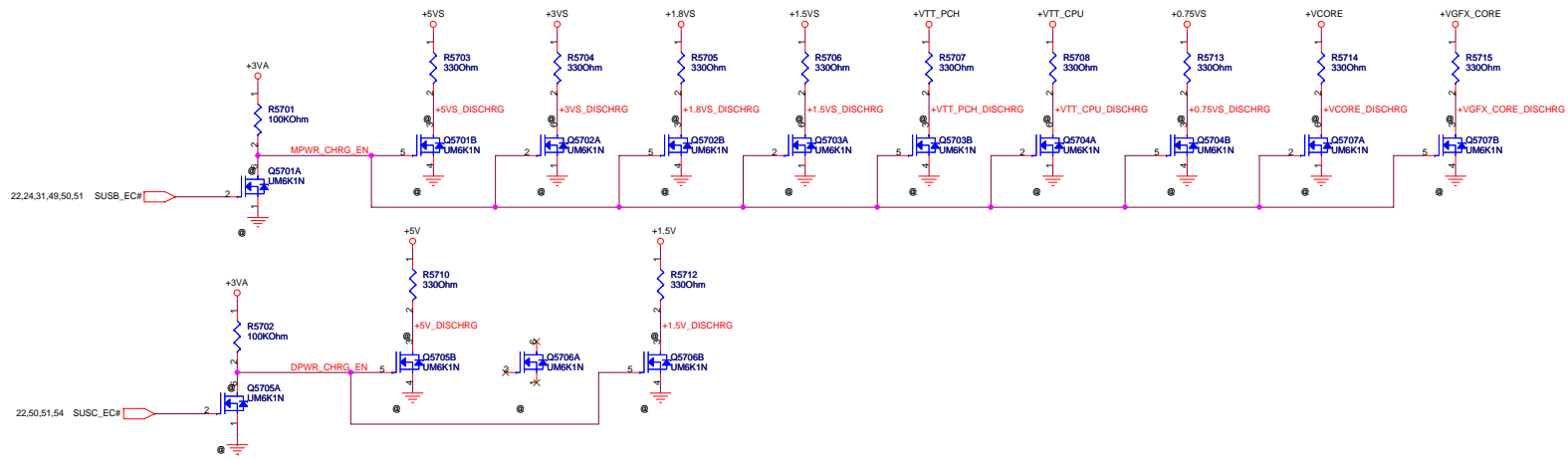
USB ports



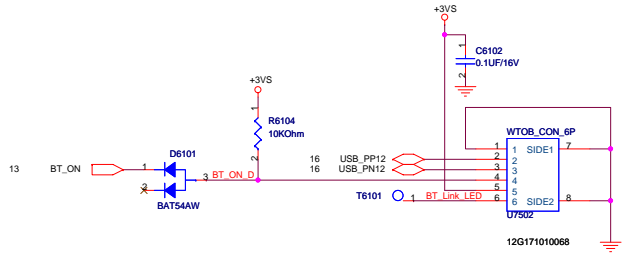




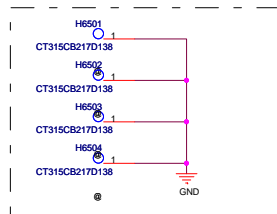
Main Board



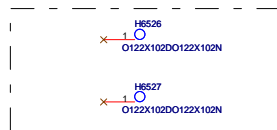
BLUETOOTH



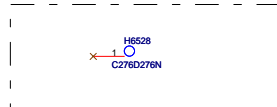
For CPU



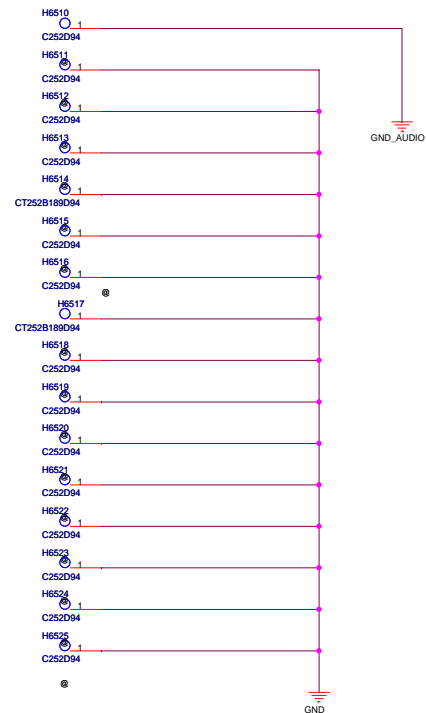
For 橢圓定位孔

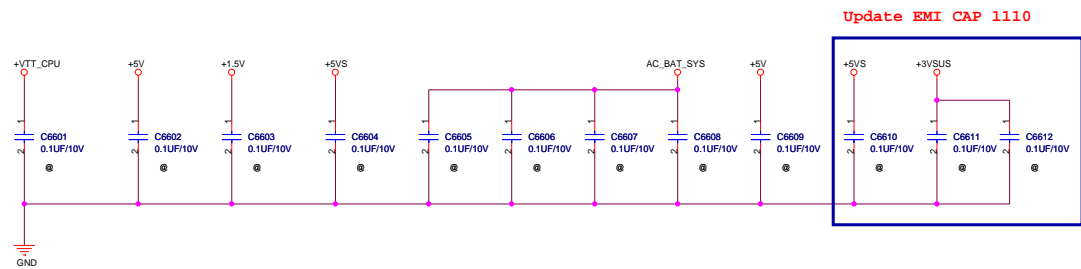


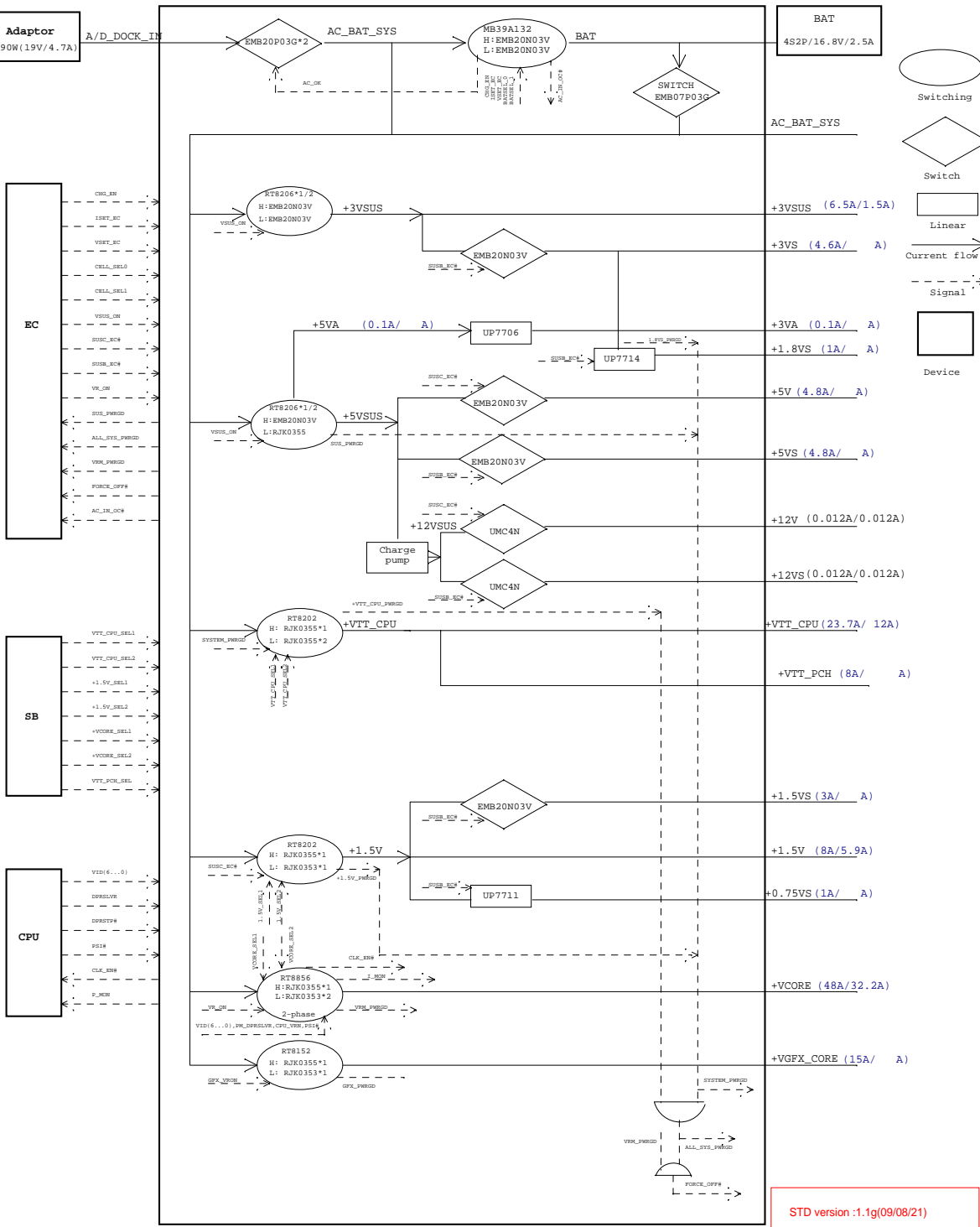
HDD 呼吸孔



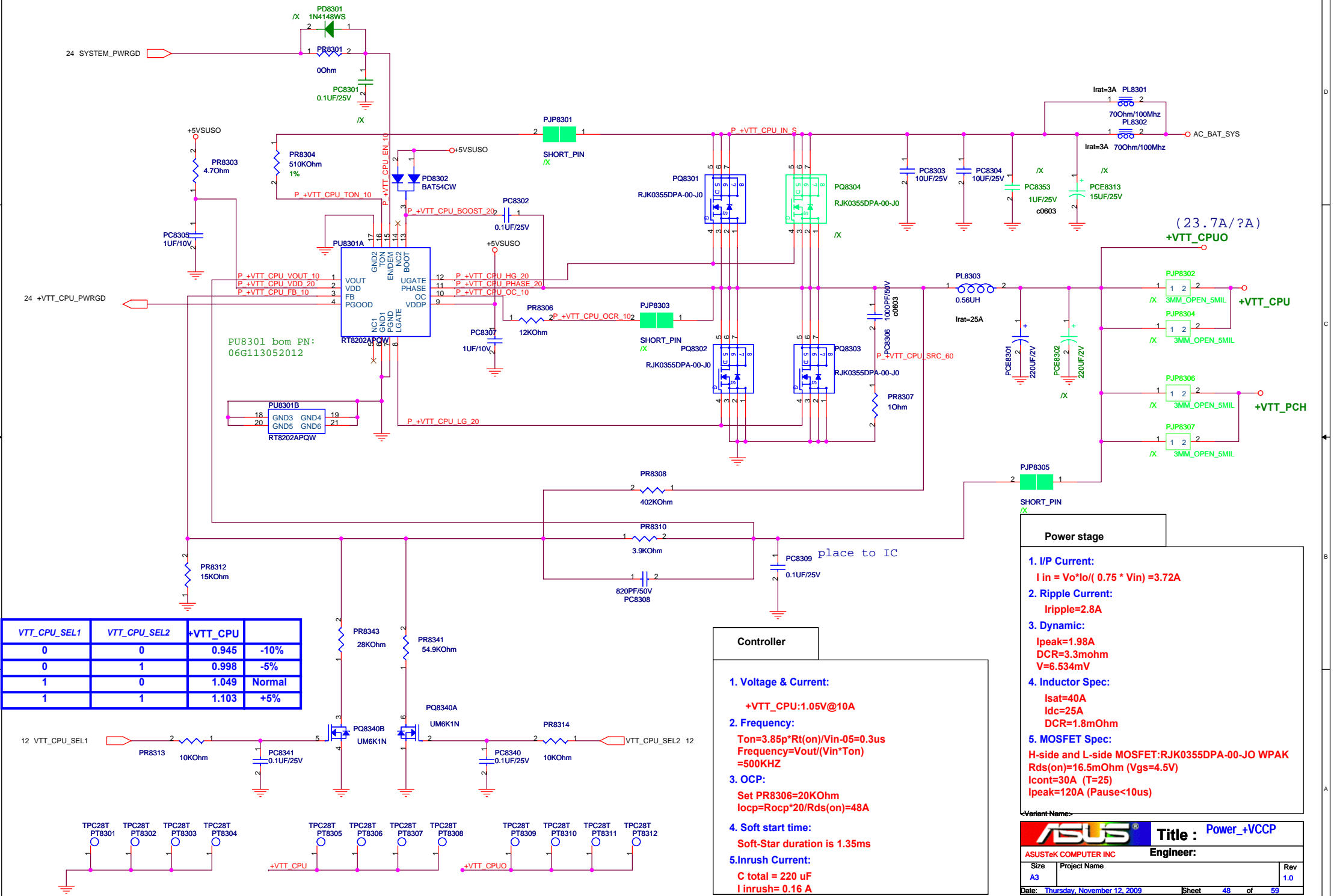
Main Board



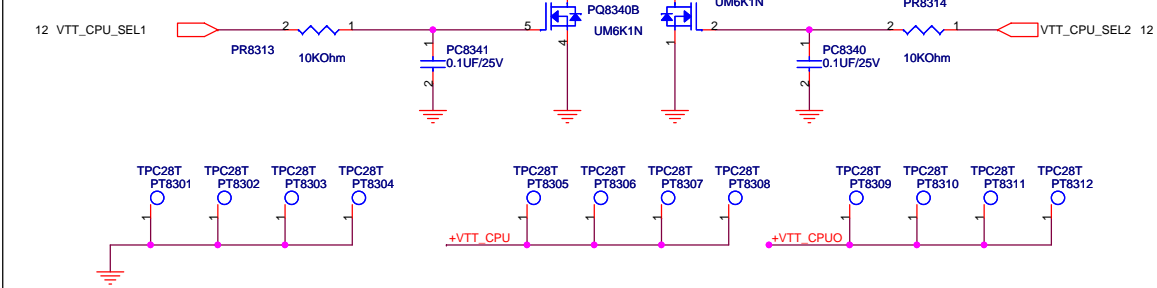




STD version :1.1g(09/08/21)



VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%



Controller

1. Voltage & Current:
+VTT_CPU:1.05V@10A

2. Frequency:
Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:
Set PR8306=20KOhm
Iocp=Rocp*20/Rds(on)=48A

4. Soft start time:
Soft-Star duration is 1.35ms

5.Inrush Current:
C total = 220 uF
I inrush= 0.16 A

Power stage

1. I/P Current:
I in = Vo*Io/(0.75 * Vin) =3.72A

2. Ripple Current:
Iripple=2.8A

3. Dynamic:
Ipeak=1.98A
DCR=3.3mohm
V=6.534mV

4. Inductor Spec:
Isat=40A
Idc=25A
DCR=1.8mOhm

5. MOSFET Spec:
H-side and L-side MOSFET:RJK0355DPA-00-JO WPAK
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

Variant Name:

ASUS®

Title : Power_VCCP

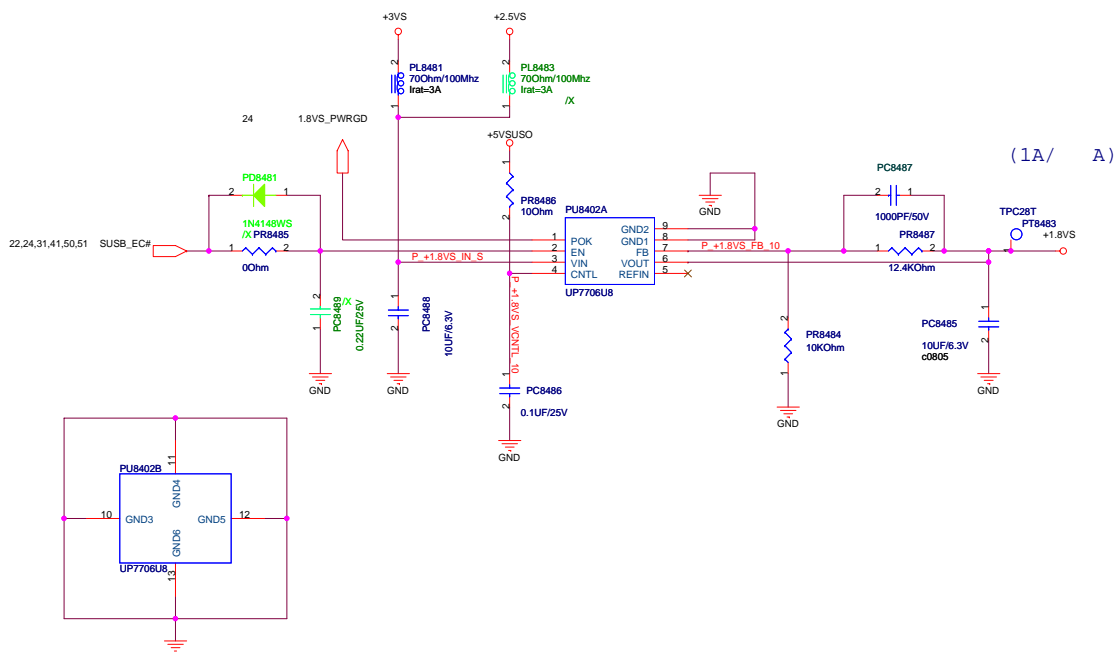
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A3		1.0

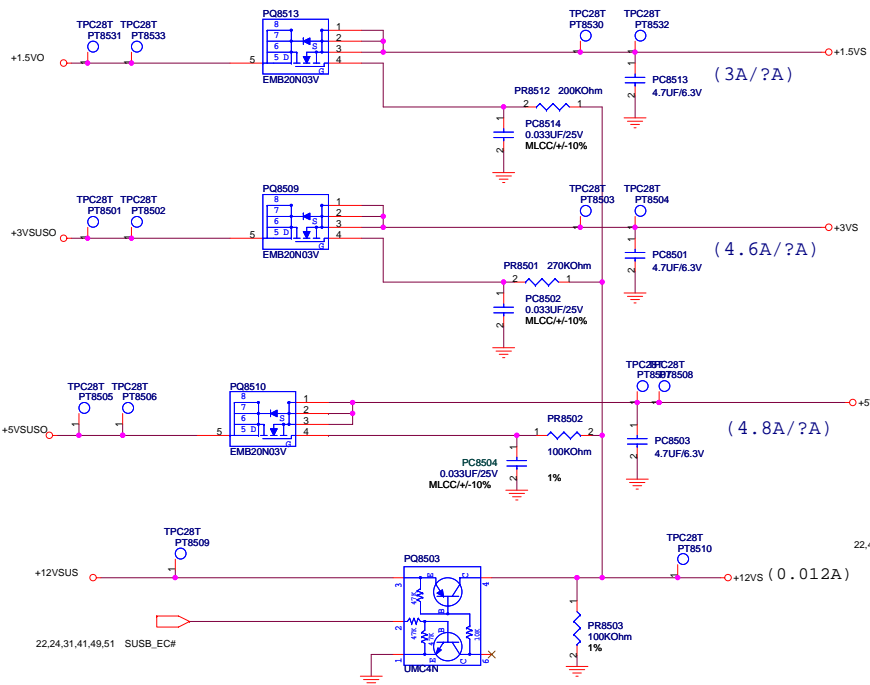
Date: Thursday, November 12, 2009

Sheet 48 of 59

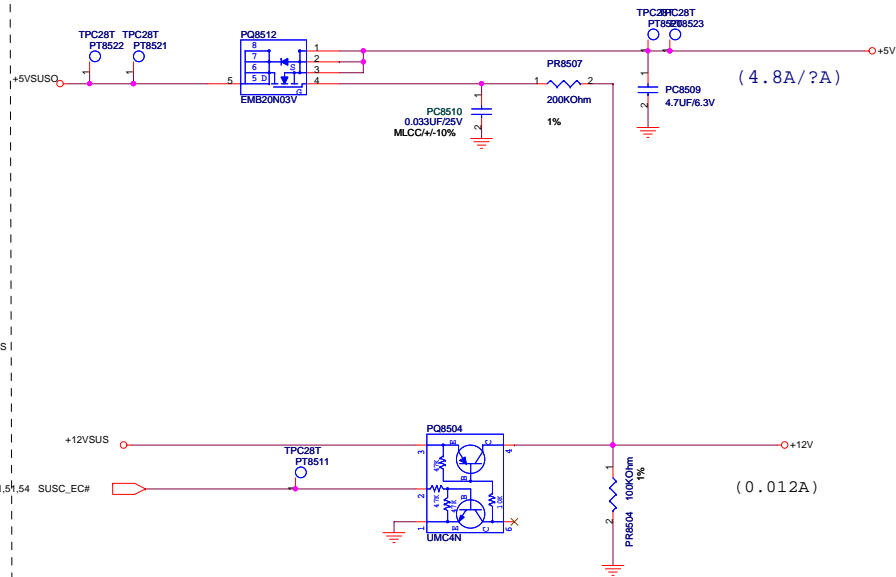


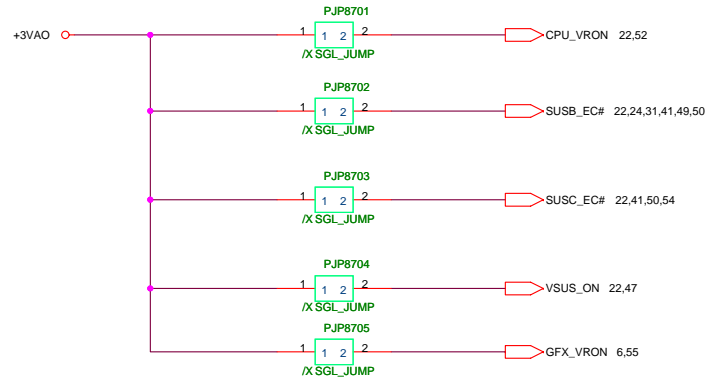
<Variant Name>

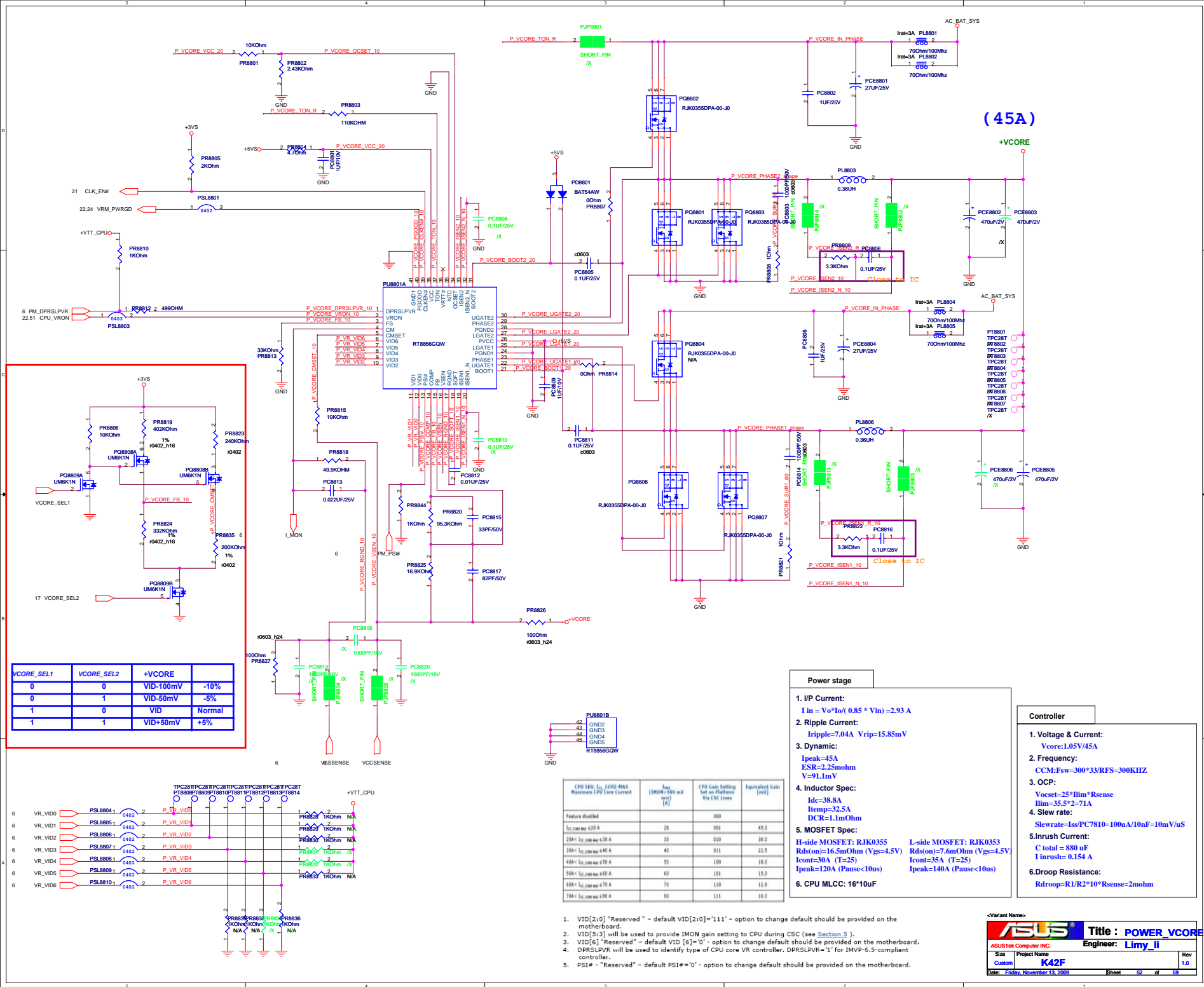
SUSB#_PWR POWER



SUSC#_PWR POWER







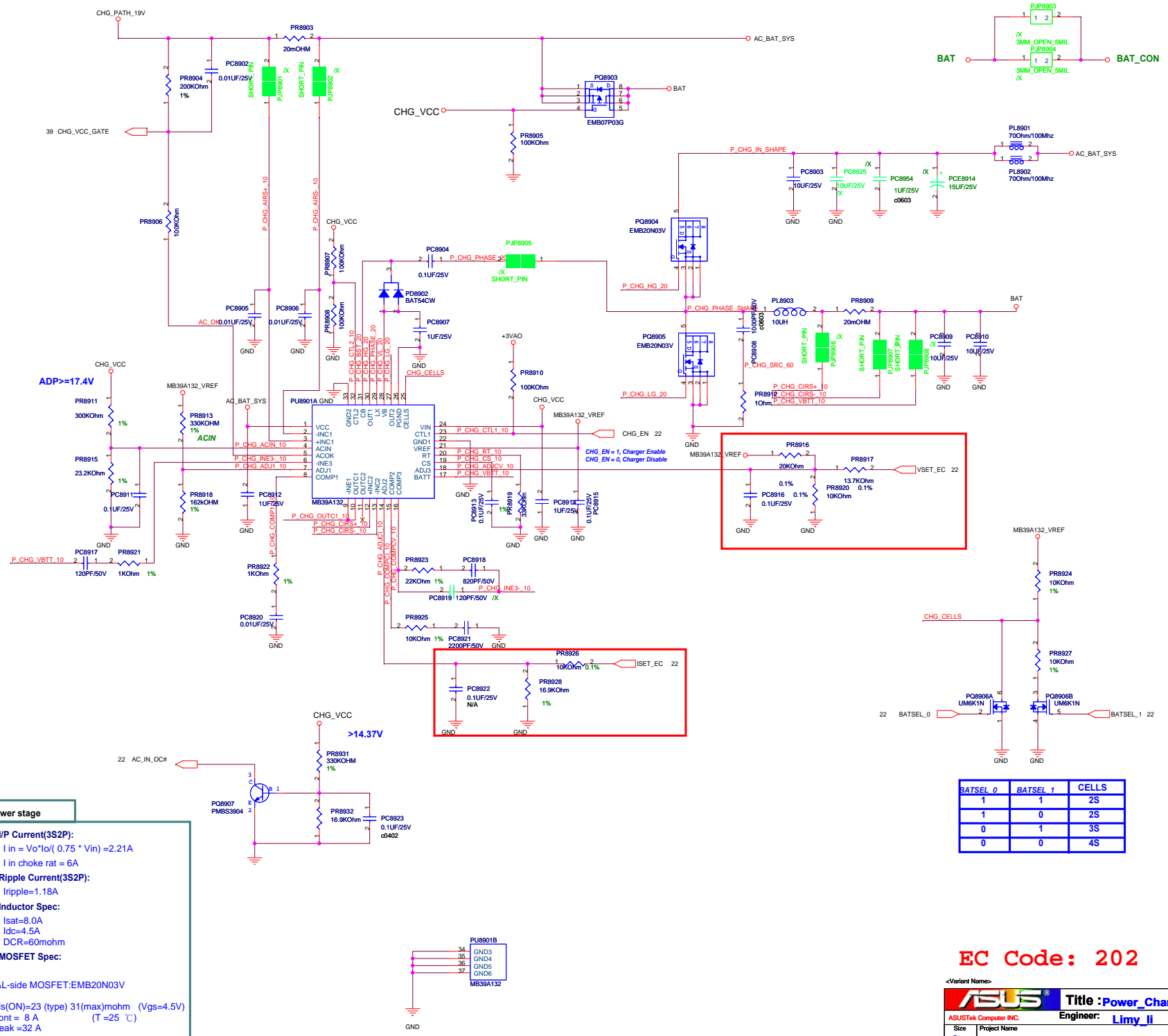
1. Adapter Threshold: 17.41V
 $17.41 = (PR9213 + PR9216) / PR9216 * 1.25$
2. AP4835 ID=9.2A
3. MB39A132_VREF= 5.0V
4. Input limit:
 65W: $I_{limit_current} = (V_{adj} - 1.075) / (25 * R_s) = (1.646 - 0.075) / 25 / 0.02 = 3.14A$
 330K~162K
 90W: $100K \sim 86.6K : I_{limit_current} = 4.49A$
5. Charging Voltage L

VSET_EC	2S	3S	4S
2.9894	3.399	12.598	16.797
6. Charging current L

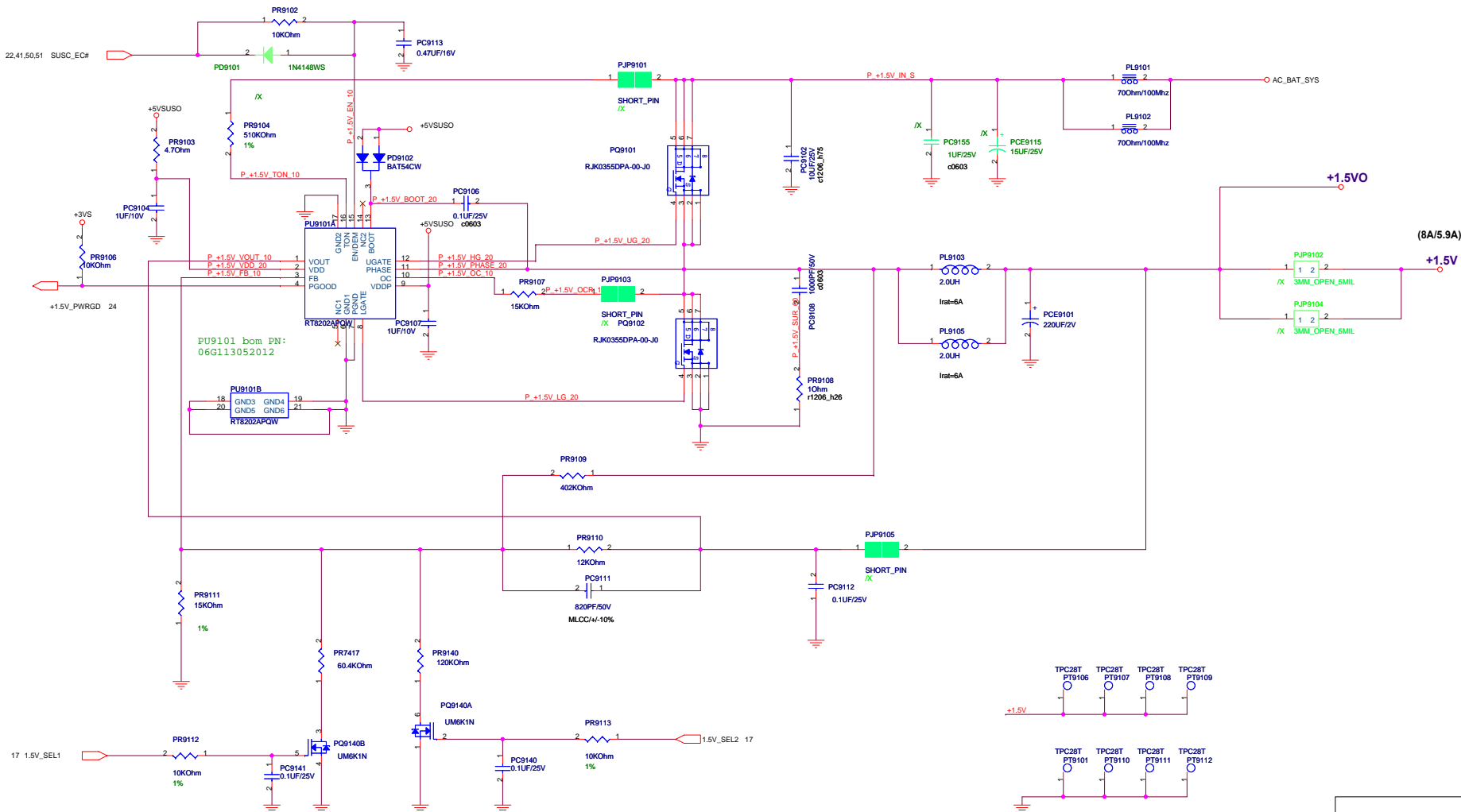
ISET_EC	ICHG	Ps
1.3071	1492	1P
2.1094	2500	2P
3.3	3996	3P

- Controller**
1. Frequency:
 $f_{osc}(KHz) = 17000 / RT (K\Omega h)$
 $f_{osc}(KHz) = 17000 / 33K = 515KHz$
 2. OCP:
 $I_{oc} = 0.2 / R_s = 10A$
 3. Soft start time:
 $t_s(s) = 0.26 * CS(uF) = 0.26 * 0.1 = 26ms$
 4. Inrush current(3S):
 $I_{inrush} = C * V / t = 9.7mA$

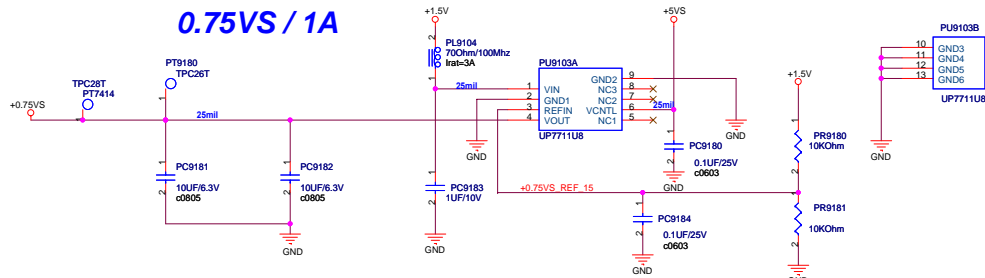
- Power stage**
1. I/P Current(3S2P):
 $I_{in} = V_o * I_o / (0.75 * V_{in}) = 2.21A$
 I_{in} choke rat = 6A
 2. Ripple Current(3S2P):
 $I_{ripple} = 1.18A$
 3. Inductor Spec:
 $I_{sat} = 8.0A$
 $I_{dc} = 4.5A$
 $DCR = 60mohm$
 4. MOSFET Spec:
 H&L-side MOSFET: EMB20N03V
 $R_{ds(ON)} = 23 (type) 31 (max) mohm (V_{gs} = 4.5V)$
 $I_{cont} = 8A (T = 25^{\circ}C)$
 $I_{peak} = 32A$



EC Code: 202



0.75VS / 1A



1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

Controller

- 1. Voltage & Current:**
1.5V: 8A
- 2. Frequency:**
Ton=3.85p*Rt(on)/Vin-0.5=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ
- 3. OCP:**
Set PR9107=20kohm
Iocp=Rocp*20/Rds(on)=24A
- 4. Soft start time:**
Soft-Star duration is 1.35ms
- 5. Inrush Current:**
C total =220uF
I inrush=0.163A

Power stage

- 1. I/P Current:**
 $I_{in} = V_o \cdot I_o / (0.75 \cdot V_{in}) = 1.33A$
- 2. Ripple Current:**
Iripple=3.74A
- 3.ripple voltage:**
 $I_{peak} = (v_{in} - v_o) \cdot D / (L \cdot F_{sw}) = 2.07A$
DCR=3.3mohm
V=6.831mV
- 4. Inductor Spec:**
Isat=22A
Idc=11A
DCR=10mohm
- 5. MOSFET Spec:**
H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

VTT_CPU_SEL1 Default : H
VTT_CPU_SEL2 Default : L

VTT_CPU_SEL1	VTT_CPU_SEL2	+VTT_CPU	
0	0	0.945	-10%
0	1	0.998	-5%
1	0	1.049	Normal
1	1	1.103	+5%

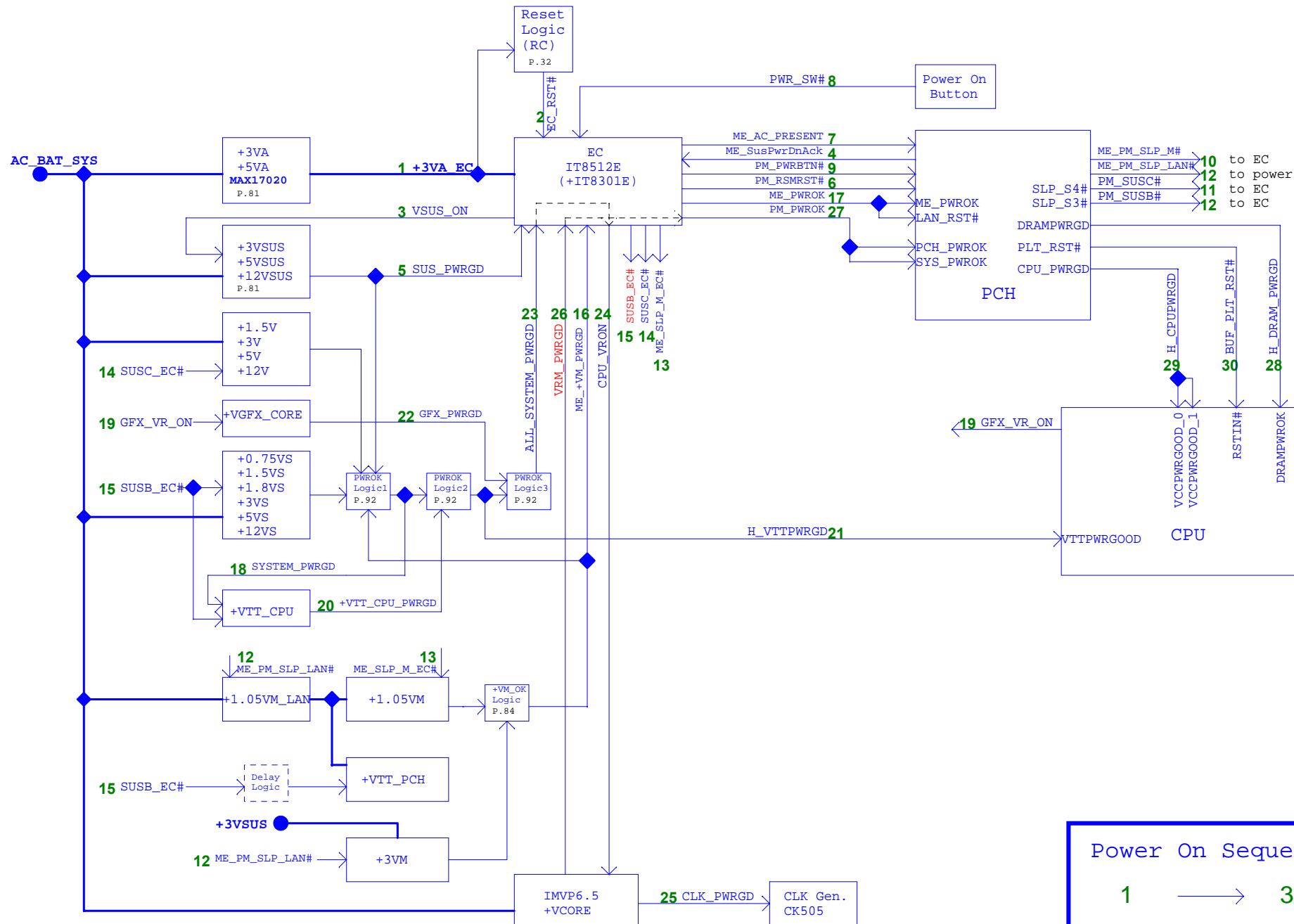
VCORE_SEL1 Default : H
VCORE_SEL2 Default : L

VCORE_SEL1	VCORE_SEL2	+VCORE	
0	0	VID-100mV	-10%
0	1	VID-50mV	-5%
1	0	VID	Normal
1	1	VID+50mV	+5%

1.5V_SEL1 Default : H
1.5V_SEL2 Default : L

1.5V_SEL1	1.5V_SEL2	+1.5V	
0	0	1.35	-10%
0	1	1.425	-5%
1	0	1.5	Normal
1	1	1.575	+5%

<Variant Name>

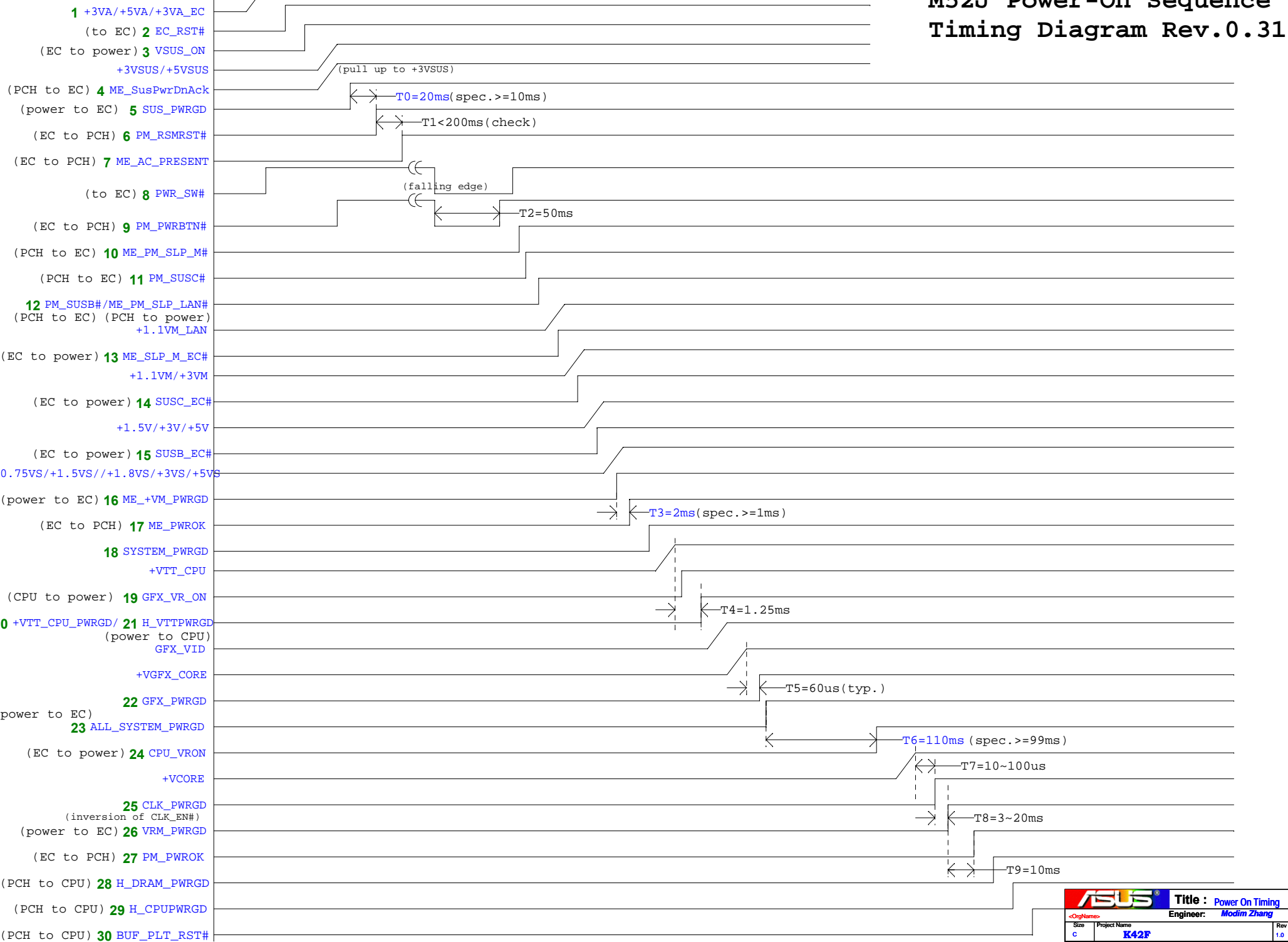


Power On Sequence

1 → 30

AC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31



DC-IN Mode

M52J Power-On Sequence
Timing Diagram Rev.0.31

