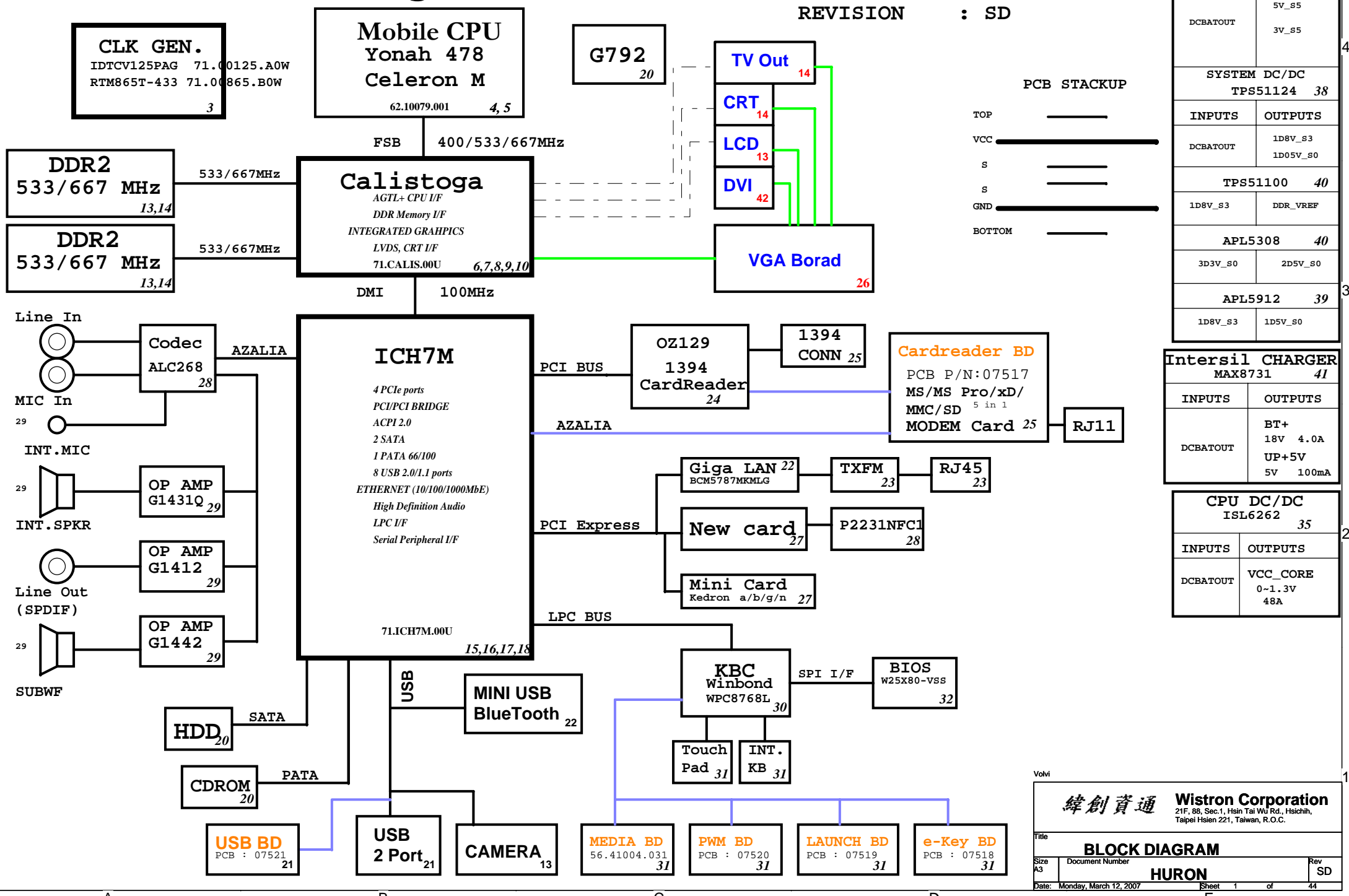
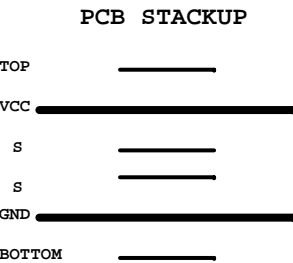


Huron Block Diagram



Project code: 91.4V301.001
PCB P/N : 07205
REVISION : SD



SYSTEM DC/DC TPS51120 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5

SYSTEM DC/DC TPS51124 38	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0

TPS51100 40	
1D8V_S3	DDR_VREF

APL5308 40	
3D3V_S0	2D5V_S0

APL5912 39	
1D8V_S3	1D5V_S0

Intersil CHARGER MAX8731 41	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 48A

A

B

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0]	ICH7 internal 20K pull-ups
LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

3

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

2

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.

C

RTM865T-433 100Mhz/LCDCLK Spread and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	0.8% Down
0	0	0	1	1.0% Down
0	0	1	0	1.25% Down
0	0	1	1	1.50% Down
0	1	0	0	1.75% Down
0	1	0	1	2.0% Down
0	1	1	0	2.5% Down
0	1	1	1	3.0% Down
1	0	0	0	+ -0.3% Center
1	0	0	1	+ -0.4% Center
1	0	1	0	+ -0.5% Center
1	0	1	1	+ -0.6% Center
1	1	0	0	+ -0.8% Center
1	1	0	1	+ -1.0% Center
1	1	1	0	+ -1.25% Center
1	1	1	1	+ -1.5% Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
OZ129TZ	AD22	A-G	REQ0# ->REQ0#

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

D

Calistoga Strapping Signals and Configuration

E

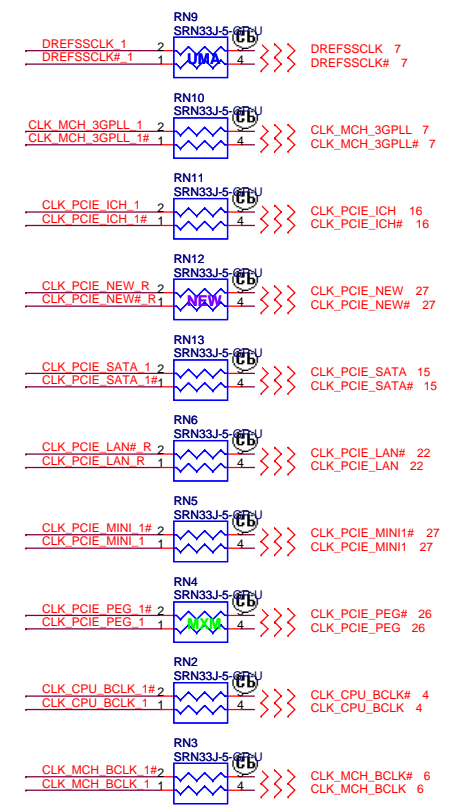
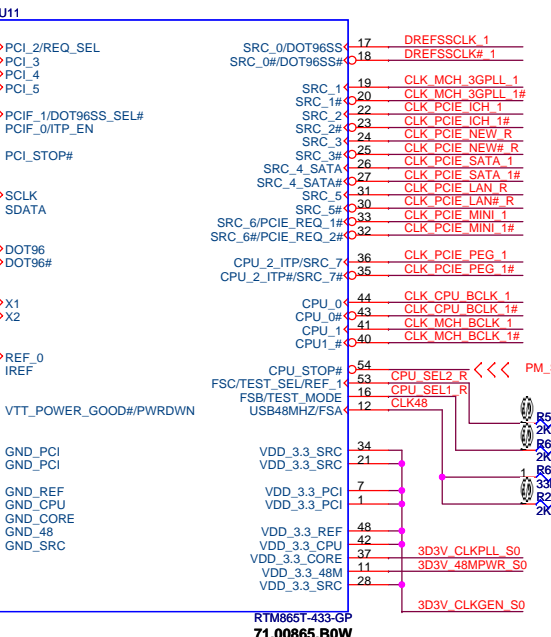
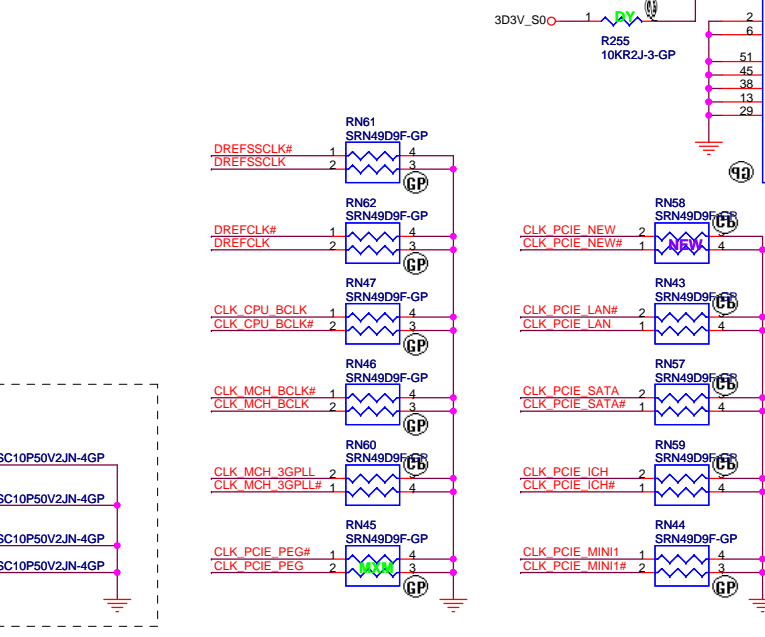
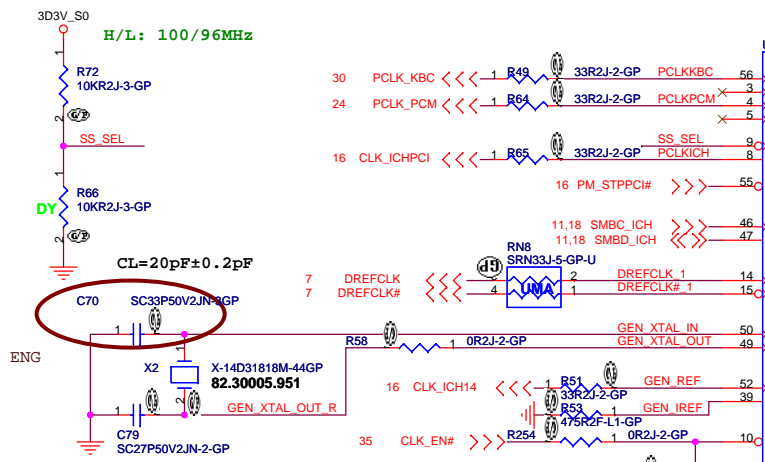
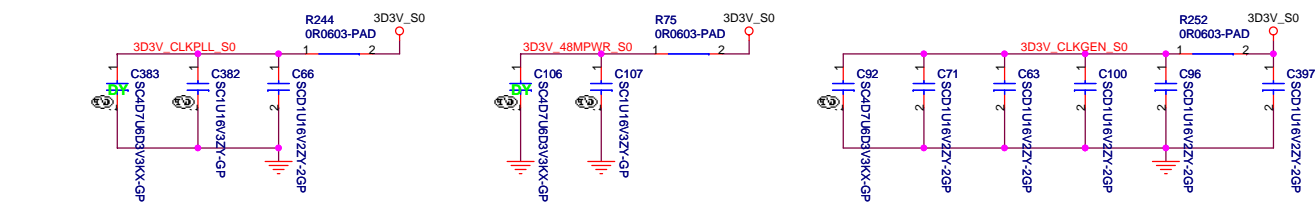
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

<Core Design>

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reference		
Size	Document Number HURON	Rev
Date: Monday, March 12, 2007	Sheet 2 of 44	SD



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

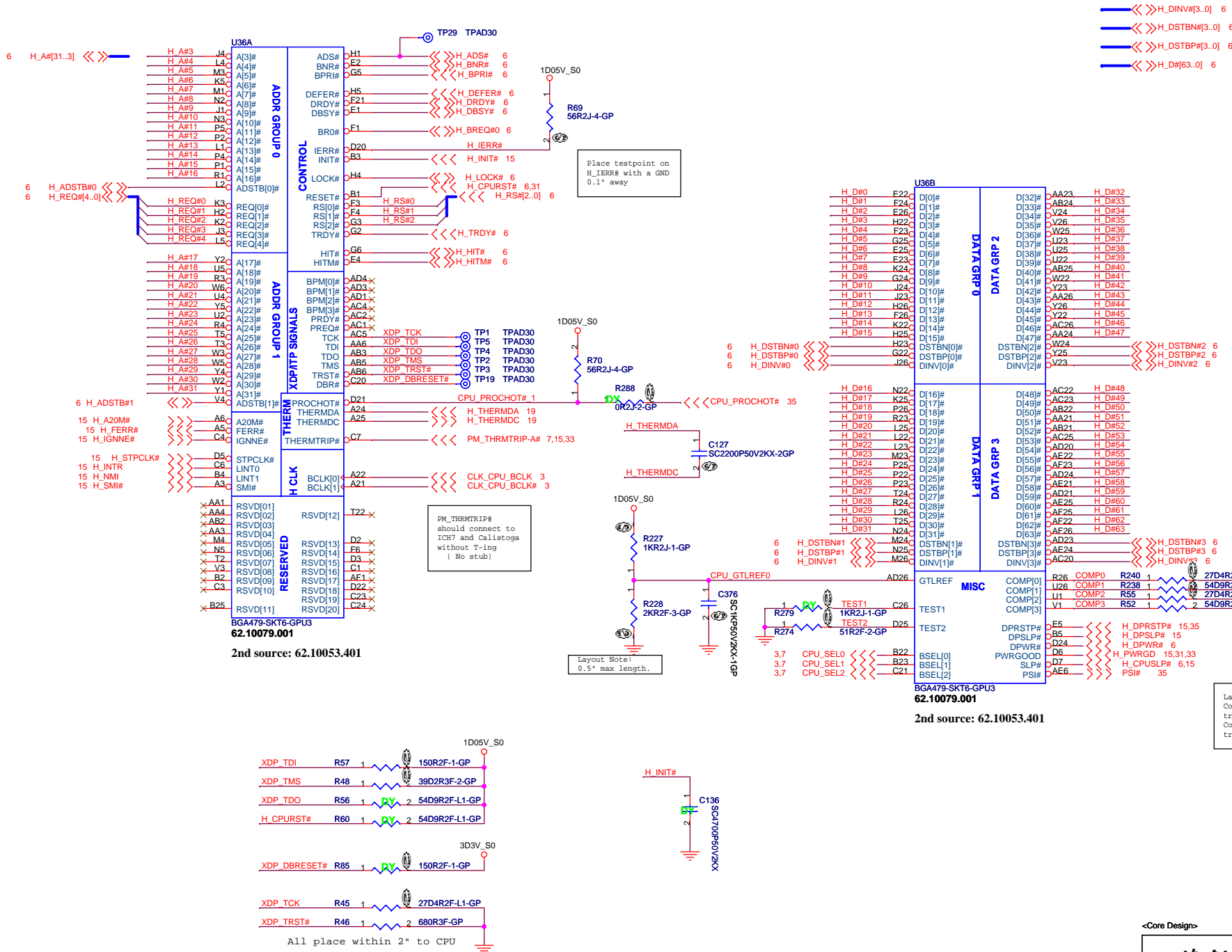
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Clock Generator

Title: **HURON**

Size: Document Number: **HURON**

Date: Monday, March 12, 2007 Sheet 3 of 44



2nd source: 62.10053.401

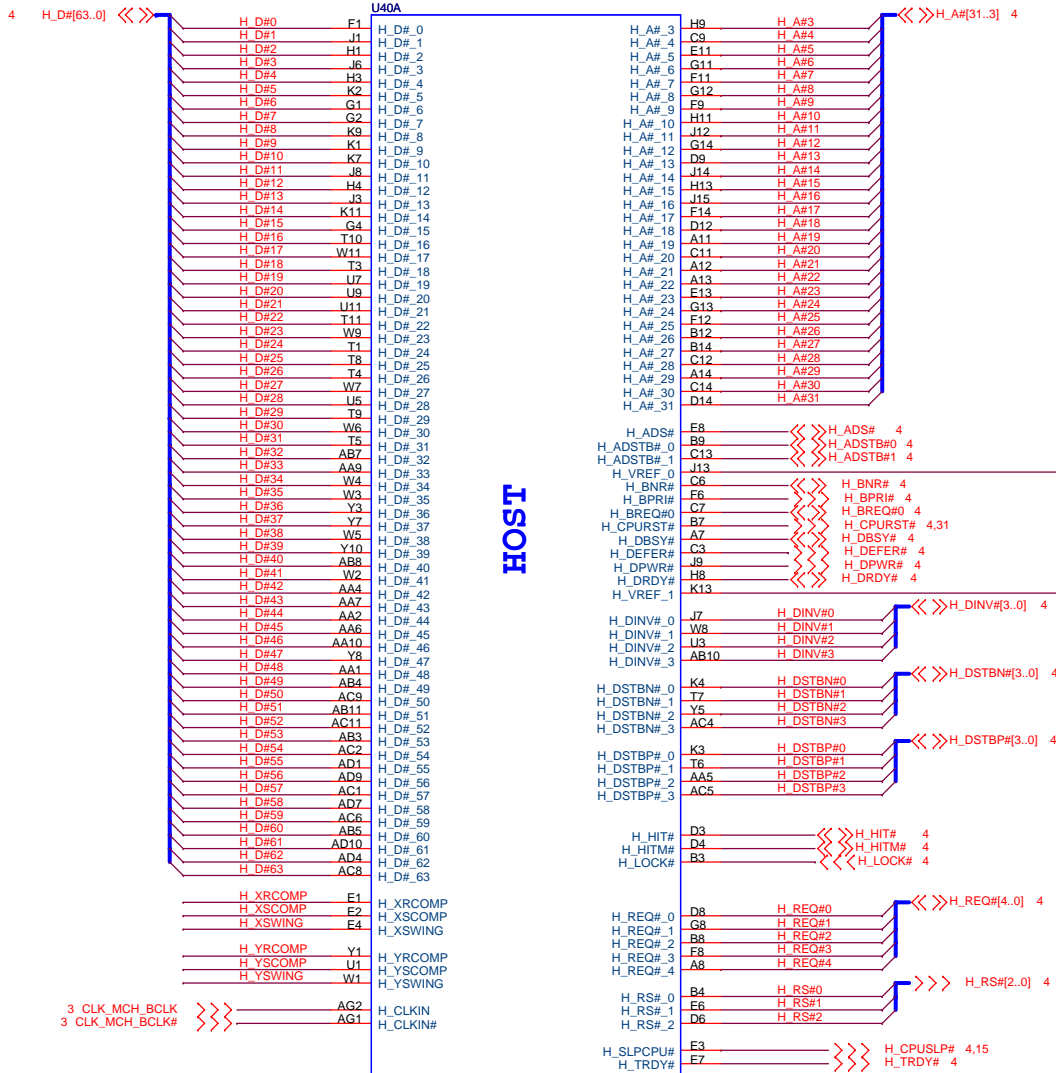
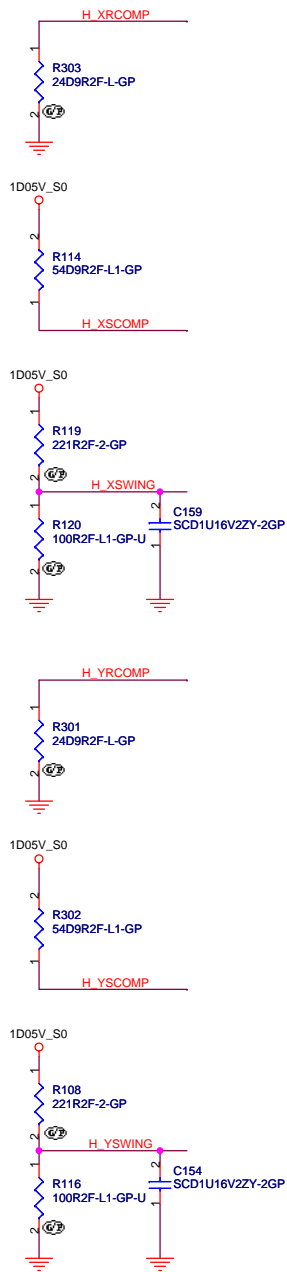
2nd source: 62.10053.401

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU (1 of 2)		Rev
Size	Document Number	HURON		SD
Date:	Monday, March 12, 2007	Sheet	4	of 44



71.CALIS.00U

DIS : 945PN P/N is KI.94501.006
UMA : 945GM P/N is KI.94501.005

Place them near to the chip (< 0.5")

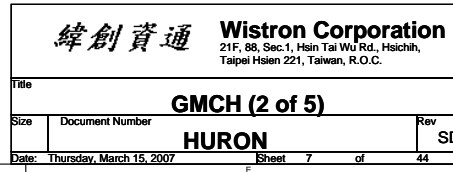
<Core Design>

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Title: **GMCH (1 of 5)**

Size: Document Number: **HURON** Rev: **SD**

Date: Monday, March 12, 2007 Sheet 6 of 44





1D05V_S0	AA33	VCC_0	U40G
	W33	VCC_1	
	P33	VCC_2	
	N33	VCC_3	
	L33	VCC_4	
	J33	VCC_5	
	AA32	VCC_6	
	V32	VCC_7	
	W32	VCC_8	
	P32	VCC_9	
	N32	VCC_10	
	L32	VCC_11	
	J32	VCC_12	
	AA31	VCC_13	
	W31	VCC_14	
	P31	VCC_15	
	N31	VCC_16	
	L31	VCC_17	
	J31	VCC_18	
	AA30	VCC_19	
	W30	VCC_20	
	P30	VCC_21	
	N30	VCC_22	
	L30	VCC_23	
	J30	VCC_24	
	AA29	VCC_25	
	W29	VCC_26	
	P29	VCC_27	
	N29	VCC_28	
	L29	VCC_29	
	J29	VCC_30	
	AA28	VCC_31	
	W28	VCC_32	
	P28	VCC_33	
	N28	VCC_34	
	L28	VCC_35	
	J28	VCC_36	
	AA27	VCC_37	
	W27	VCC_38	
	P27	VCC_39	
	N27	VCC_40	
	L27	VCC_41	
	J27	VCC_42	
	AA26	VCC_43	
	W26	VCC_44	
	P26	VCC_45	
	N26	VCC_46	
	L26	VCC_47	
	J26	VCC_48	
	AA25	VCC_49	
	W25	VCC_50	
	P25	VCC_51	
	N25	VCC_52	
	L25	VCC_53	
	J25	VCC_54	
	AA24	VCC_55	
	W24	VCC_56	
	P24	VCC_57	
	N24	VCC_58	
	L24	VCC_59	
	J24	VCC_60	
	AA23	VCC_61	
	W23	VCC_62	
	P23	VCC_63	
	N23	VCC_64	
	L23	VCC_65	
	J23	VCC_66	
	AA22	VCC_67	
	W22	VCC_68	
	P22	VCC_69	
	N22	VCC_70	
	L22	VCC_71	
	J22	VCC_72	
	AA21	VCC_73	
	W21	VCC_74	
	P21	VCC_75	
	N21	VCC_76	
	L21	VCC_77	
	J21	VCC_78	
	AA20	VCC_79	
	W20	VCC_80	
	P20	VCC_81	
	N20	VCC_82	
	L20	VCC_83	
	J20	VCC_84	
	AA19	VCC_85	
	W19	VCC_86	
	P19	VCC_87	
	N19	VCC_88	
	L19	VCC_89	
	J19	VCC_90	
	AA18	VCC_91	
	W18	VCC_92	
	P18	VCC_93	
	N18	VCC_94	
	L18	VCC_95	
	J18	VCC_96	
	AA17	VCC_97	
	W17	VCC_98	
	P17	VCC_99	
	N17	VCC_100	
	L17	VCC_101	
	J17	VCC_102	
	AA16	VCC_103	
	W16	VCC_104	
	P16	VCC_105	
	N16	VCC_106	
	L16	VCC_107	
	J16	VCC_108	
	AA15	VCC_109	
	W15	VCC_110	
	P15	VCC_111	
	N15	VCC_112	
	L15	VCC_113	
	J15	VCC_114	
	AA14	VCC_115	
	W14	VCC_116	
	P14	VCC_117	
	N14	VCC_118	
	L14	VCC_119	
	J14	VCC_120	
	AA13	VCC_121	
	W13	VCC_122	
	P13	VCC_123	
	N13	VCC_124	
	L13	VCC_125	
	J13	VCC_126	
	AA12	VCC_127	
	W12	VCC_128	
	P12	VCC_129	
	N12	VCC_130	
	L12	VCC_131	
	J12	VCC_132	
	AA11	VCC_133	
	W11	VCC_134	
	P11	VCC_135	
	N11	VCC_136	
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	J11	VCC_138	
	AA10	VCC_139	
	W10	VCC_140	
	P10	VCC_141	
	N10	VCC_142	
	L10	VCC_143	
	J10	VCC_144	
	AA9	VCC_145	
	W9	VCC_146	
	P9	VCC_147	
	N9	VCC_148	
	L9	VCC_149	
	J9	VCC_150	
	AA8	VCC_151	
	W8	VCC_152	
	P8	VCC_153	
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	J6	VCC_168	
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	W4	VCC_176	
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	L4	VCC_179	
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	J3	VCC_186	
	AA2	VCC_187	
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	J0	VCC_276	
	AA0	VCC_277	
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	W0	VCC_320	
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	J0	VCC_324	
	AA0	VCC_325	
	W0	VCC_326	
	P0	VCC_327	
	N0	VCC_328	
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	J0	VCC_330	
	AA0	VCC_331	
	W0	VCC_332	
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	J0	VCC_336	
	AA0	VCC_337	
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	AA0	VCC_343	
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	J0	VCC_348	
	AA0	VCC_349	
	W0	VCC_350	
	P0	VCC_351	
	N0	VCC_352	
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	AA0	VCC_355	
	W0	VCC_356	
	P0	VCC_357	
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	L0	VCC_359	
	J0	VCC_360	

1D05V_S0	U40F		

REVERSE TYPE

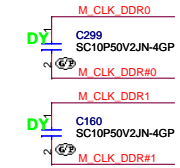
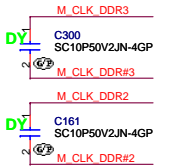
REVERSE TYPE

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **DDR2 Socket**
Size Document Number **HURON** Rev **SD**
Date: Monday, March 12, 2007 Sheet 11 of 44

Place near DM2

Place near DM1



3D3V_S0

3D3V_S0

1D8V_S3

1D8V_S3

M_CS0# 7,12
M_CS1# 7,12
M_CKE0 7,12
M_CKE1 7,12
M_A_RAS# 8,12
M_A_CAS# 8,12
M_A_WE# 8,12

M_CS0# 110,115
M_CS1# 110,115
M_CKE0 79,80
M_CKE1 80,81
M_A_RAS# 108,113
M_A_CAS# 113,109
M_A_WE# 109,108

SMBC_ICh 197
SMBC_OCh 195

SMBC_ICh 197
SMBC_OCh 195

M_ODT0 7,12
M_ODT1 7,12

M_ODT0 114
M_ODT1 119

VREF 1
VSS 2

VREF 1
VSS 2

GND 201

GND 201

MH2

MH2

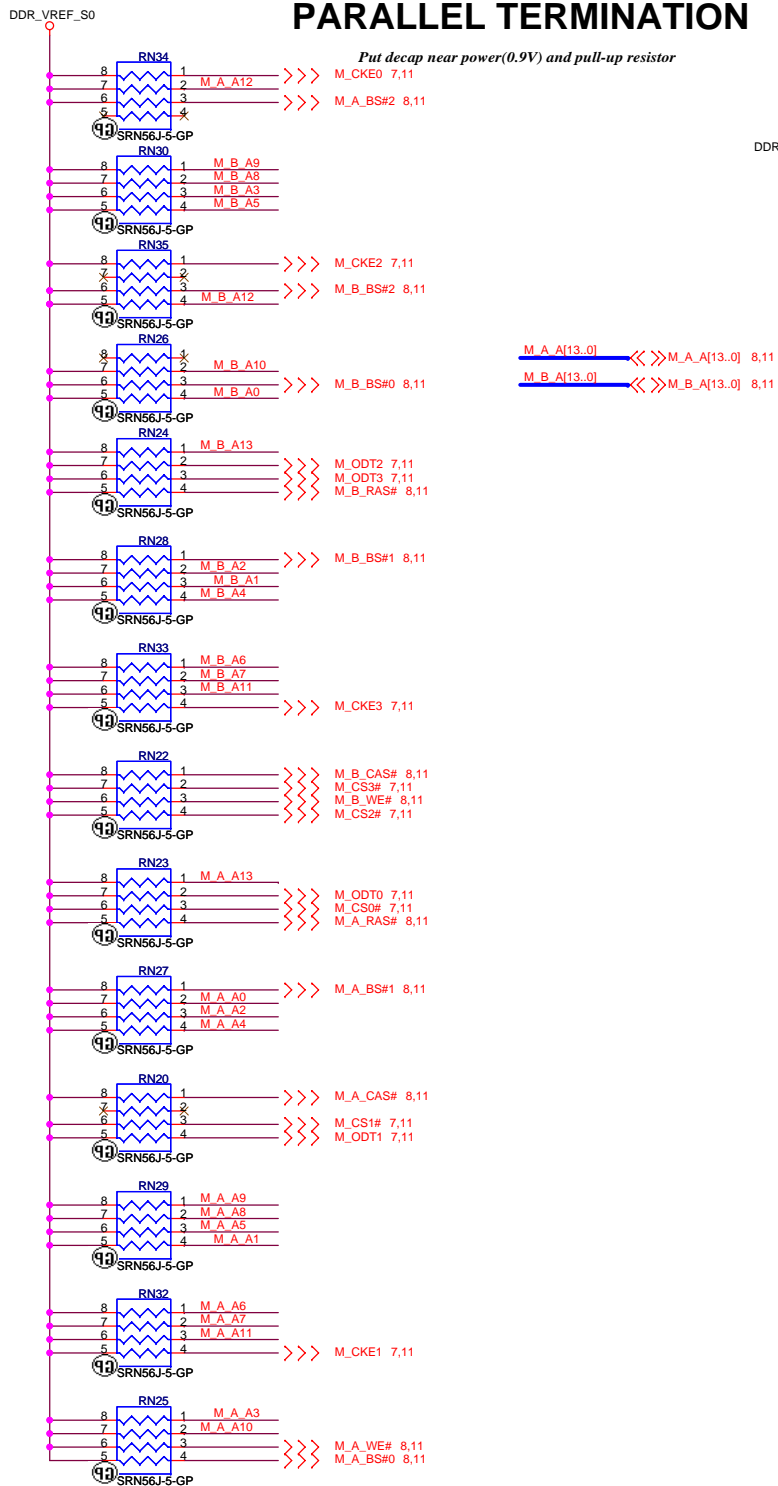
62.10017.691

62.10017.691

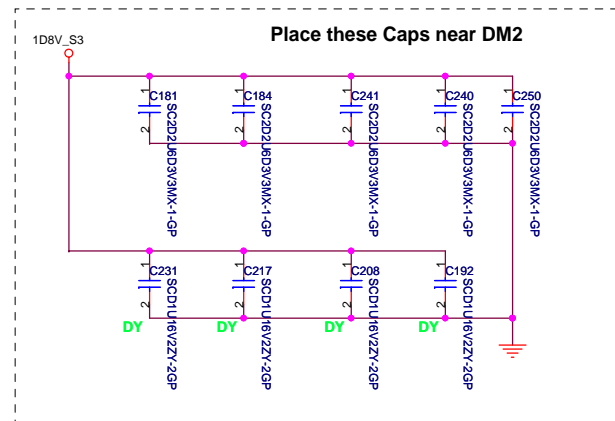
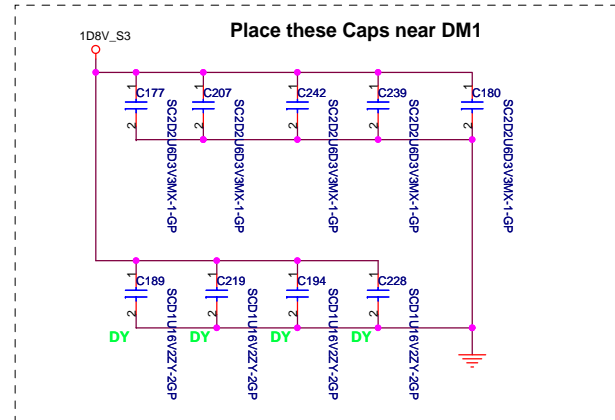
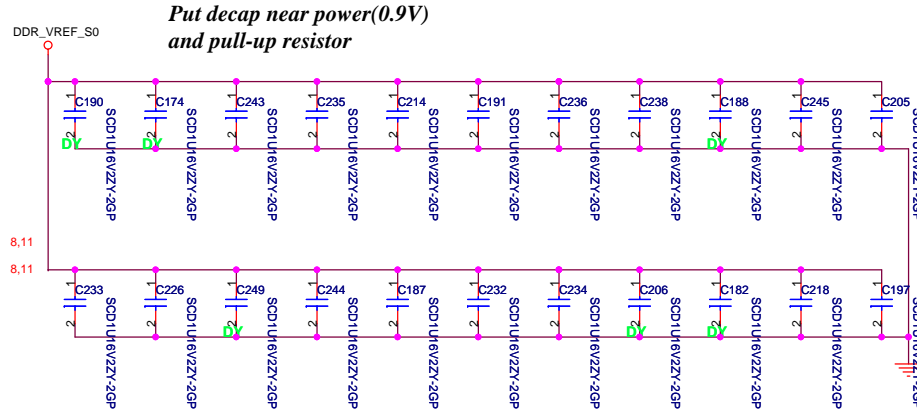
High 9.2mm

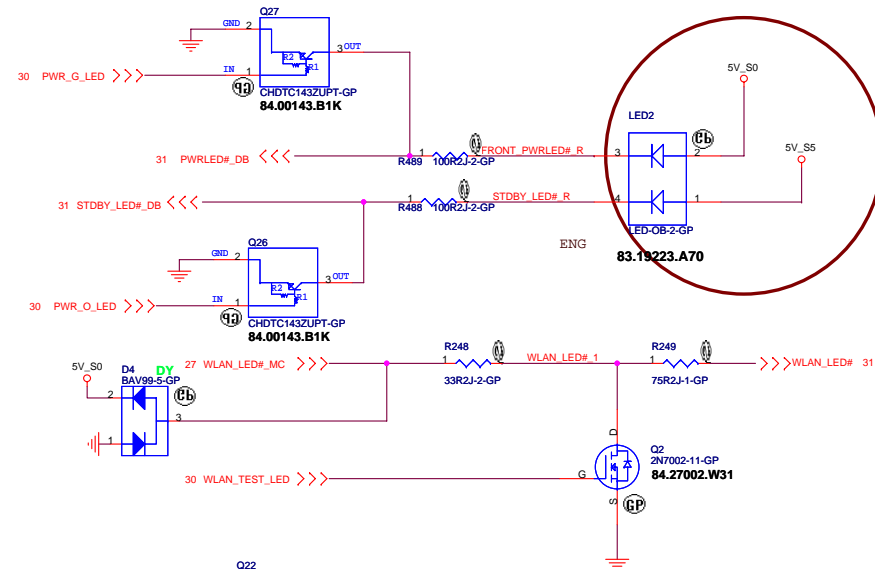
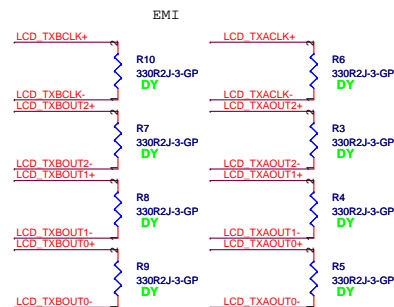
High 5.2mm

PARALLEL TERMINATION



Decoupling Capacitor

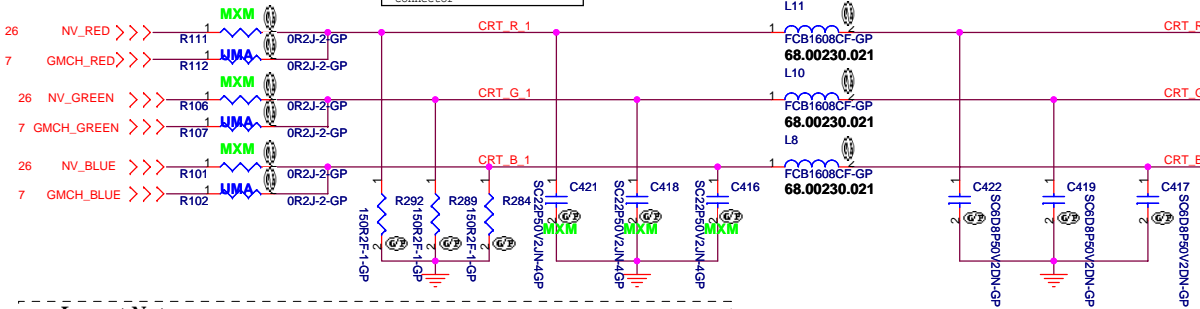


[illegible]

CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

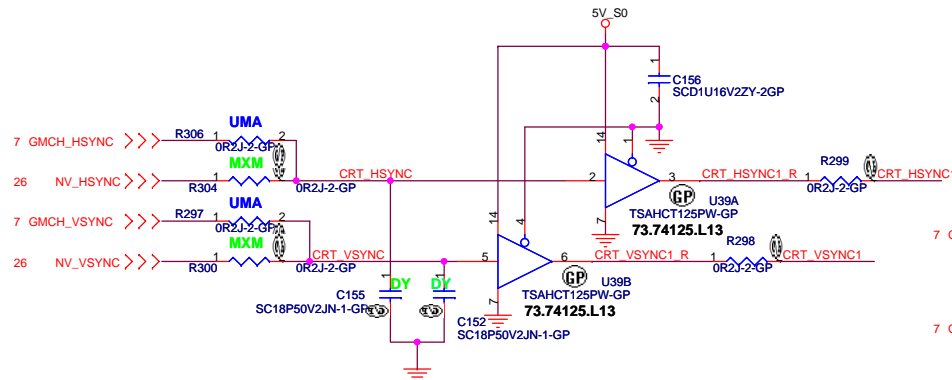
Ferrite bead impedance: 10 ohm@100MHz



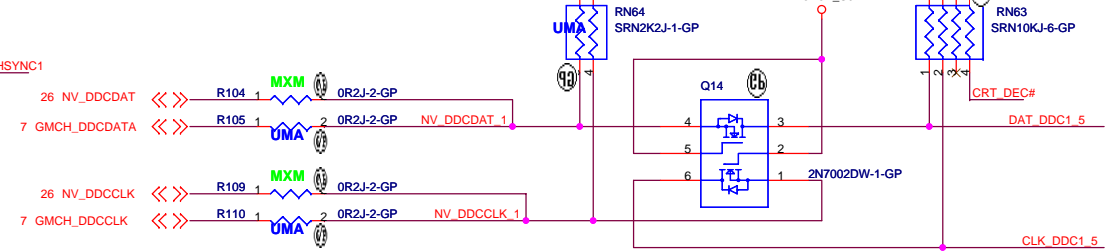
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

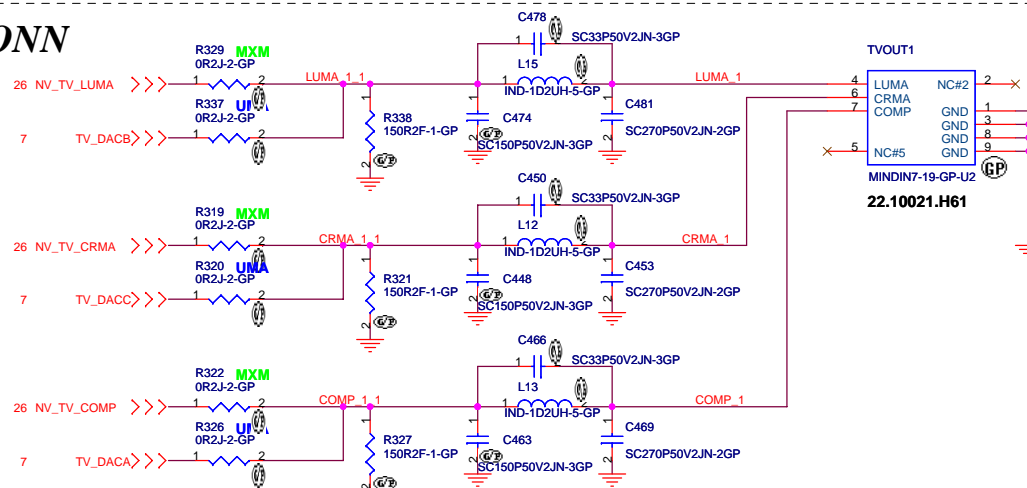
Hsync & Vsync level shift



DDC_CLK & DATA level shift

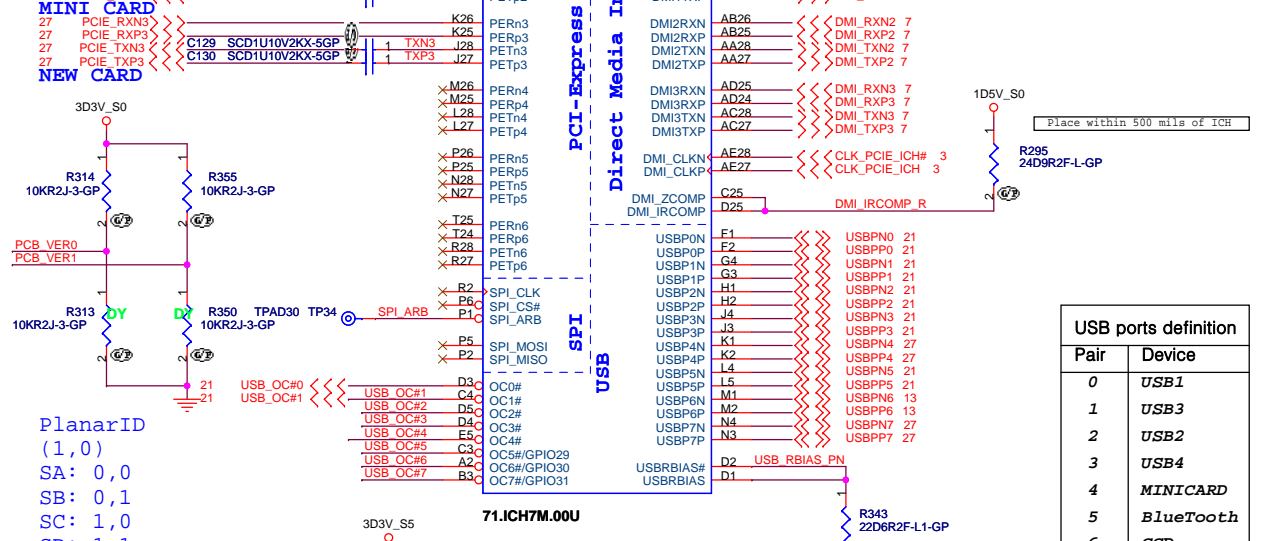
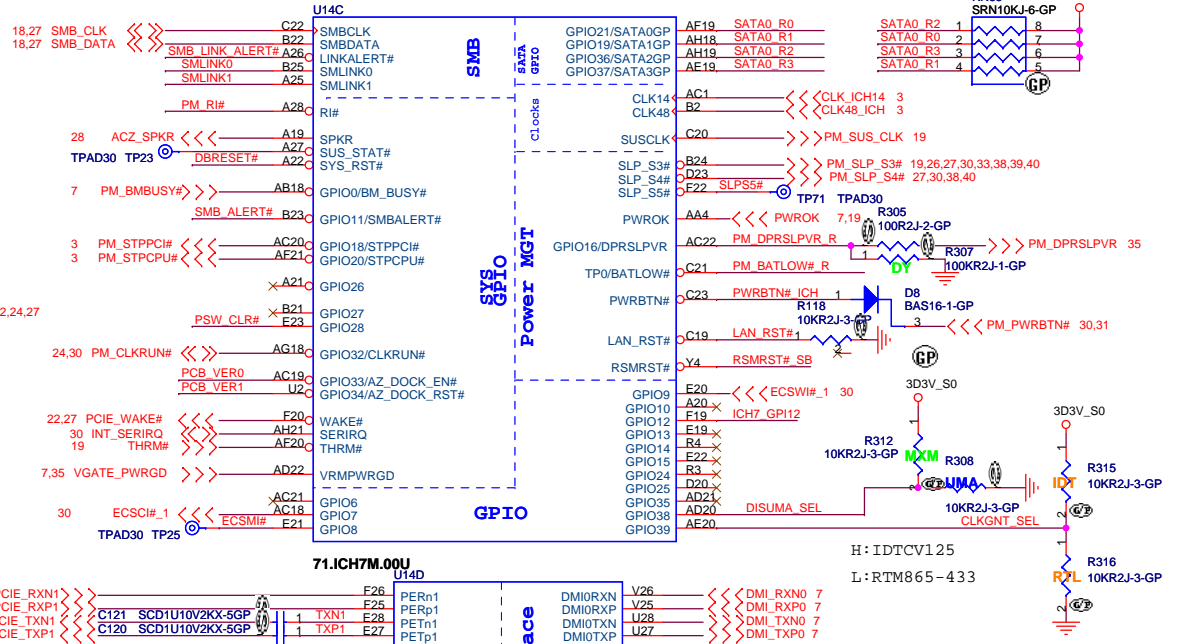



TV CONN

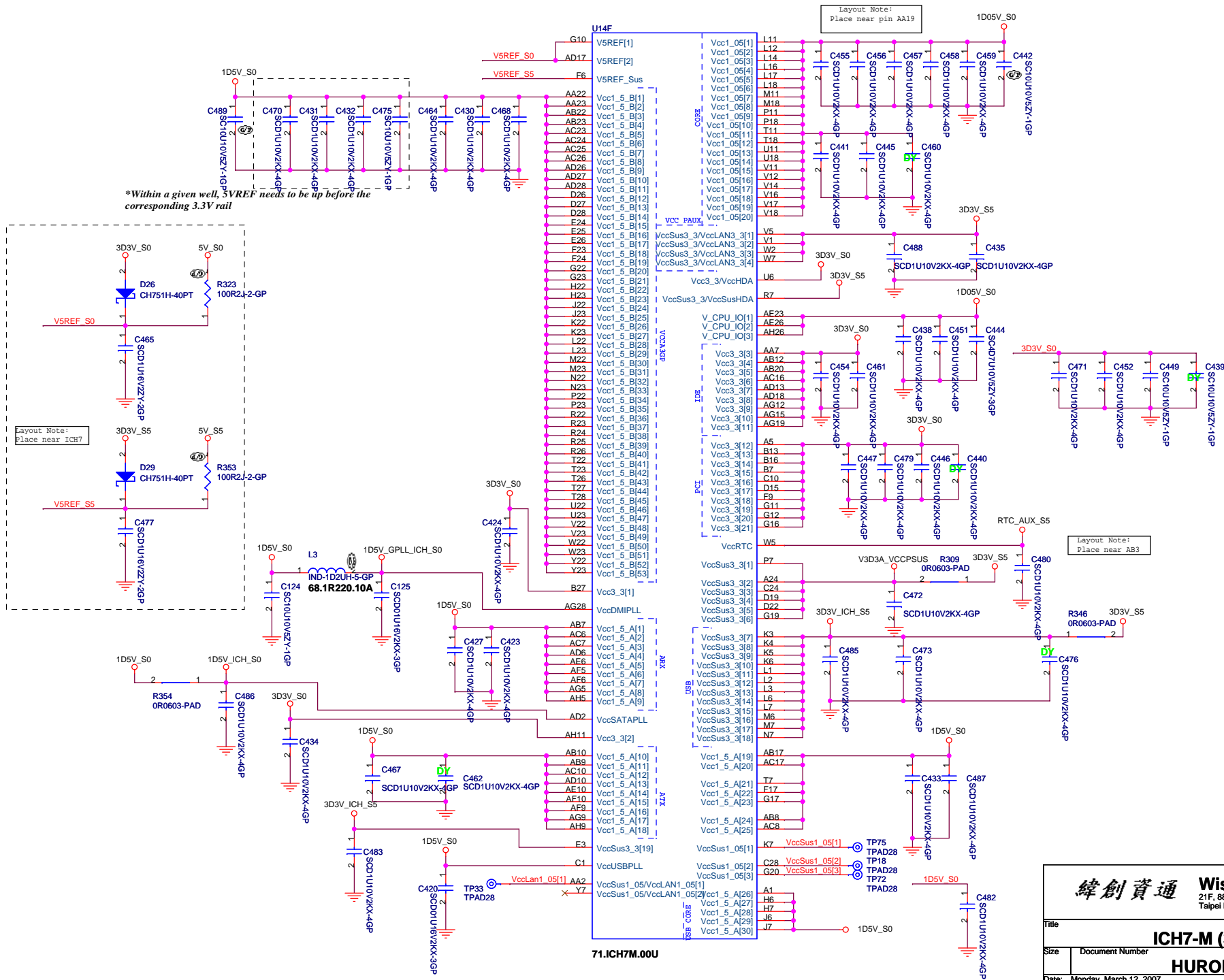


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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT/TV Connector		
Size	Document Number	Rev
		SD
Date: Monday, March 12, 2007	Sheet 14	of 44



			
			
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Size		Rev	
Document Number		ST	
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*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

Layout Note:
Place near ICH7

Layout Note:
Place near AB3

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Title

ICH7-M (3 of 4)

Size

Document Number

Date

Monday, March 12, 2007

Sheet

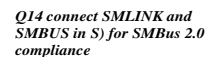
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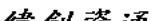
of

44

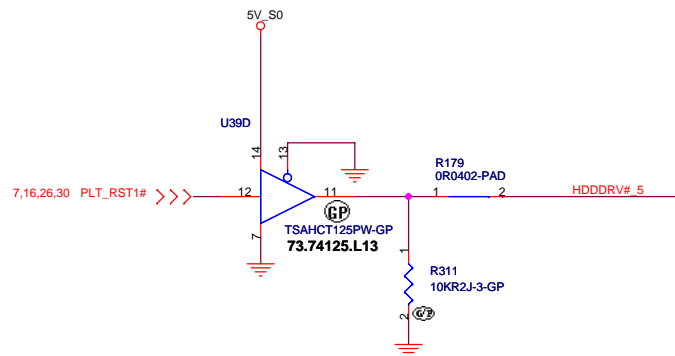
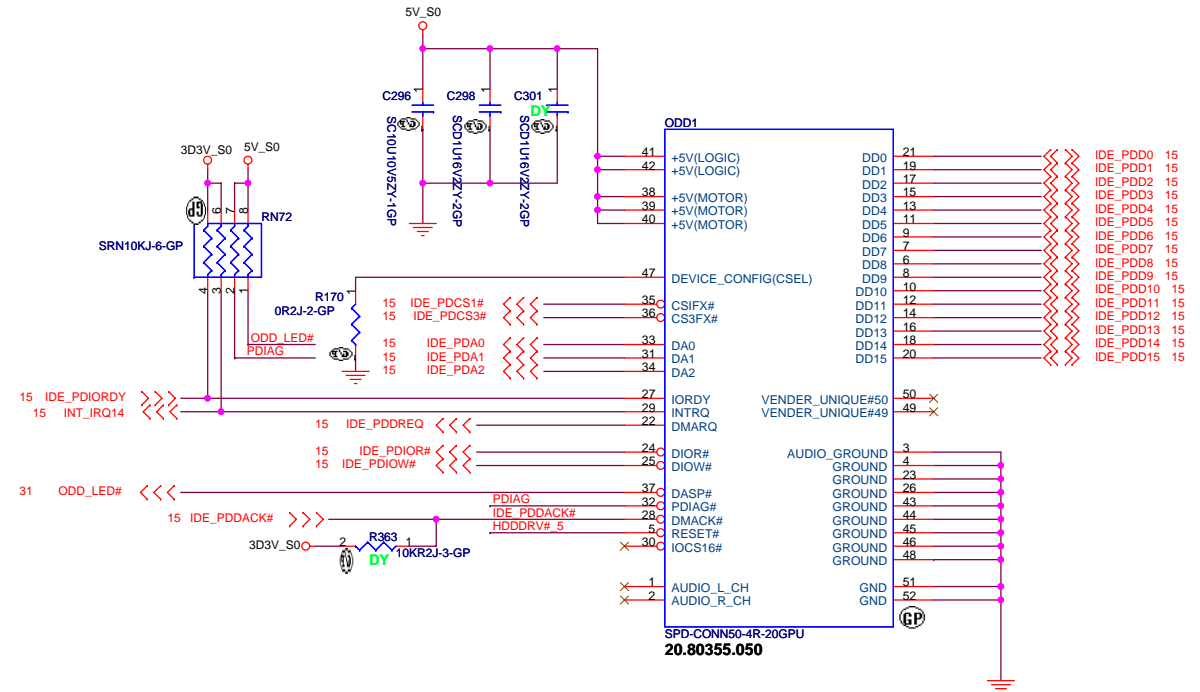
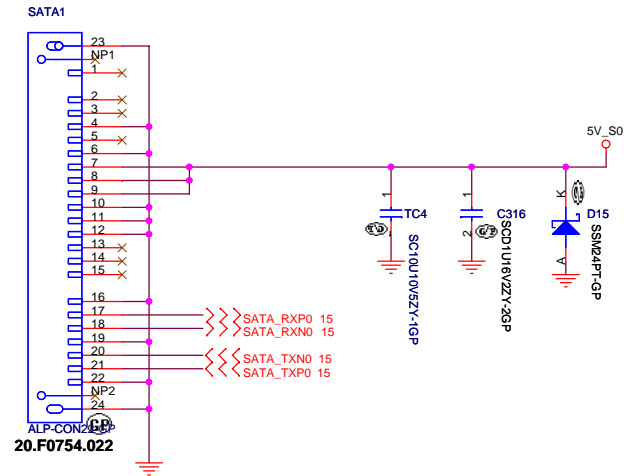
Rev

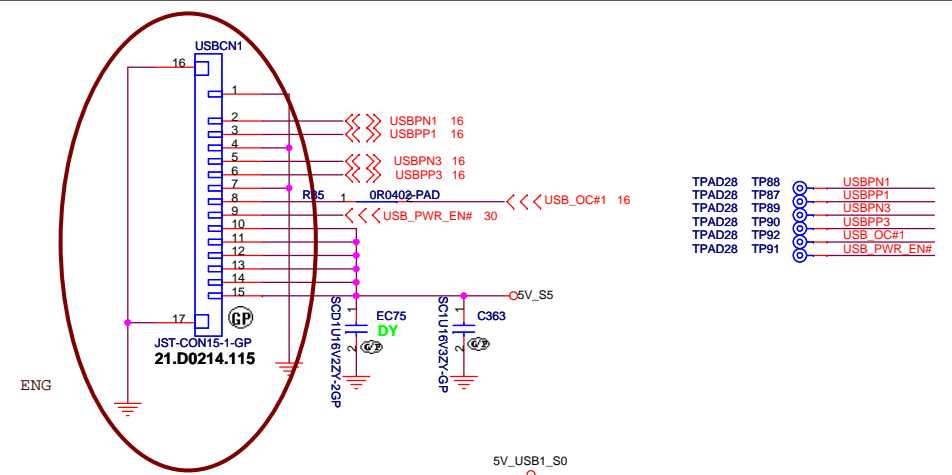
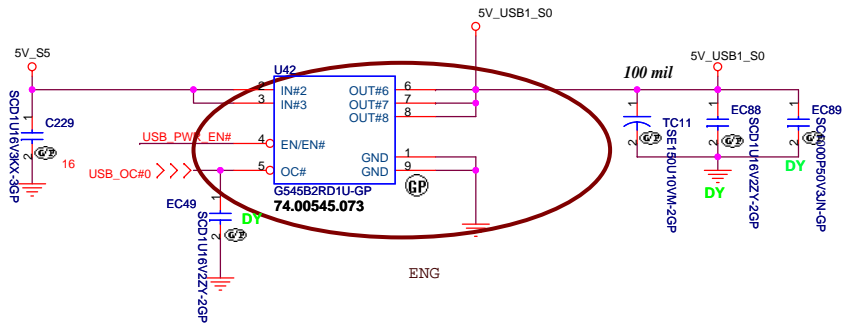
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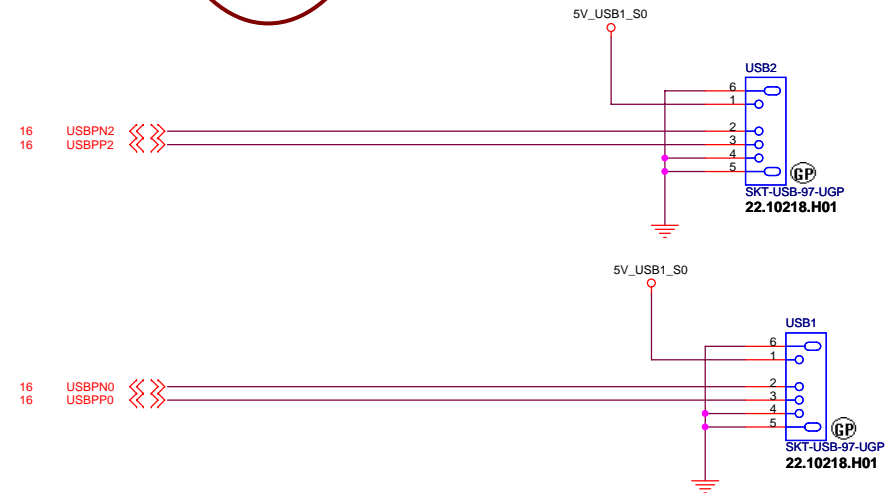
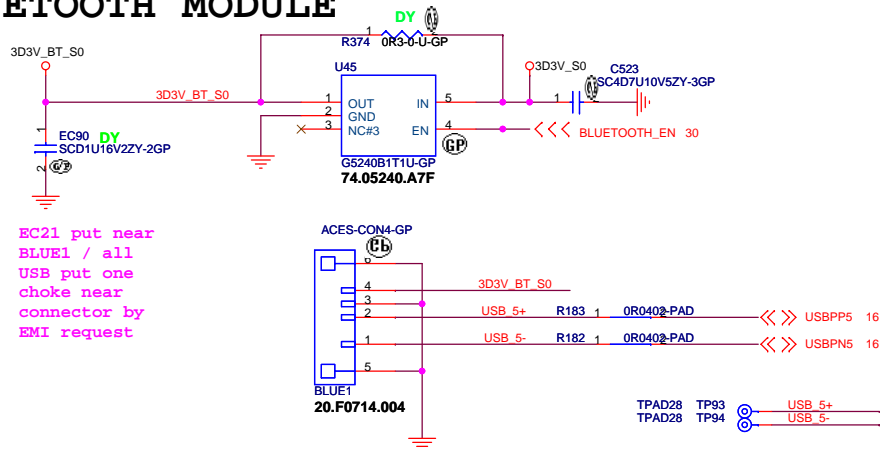
 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsien Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ICH7-M (4 of 4)			
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ODD Connector



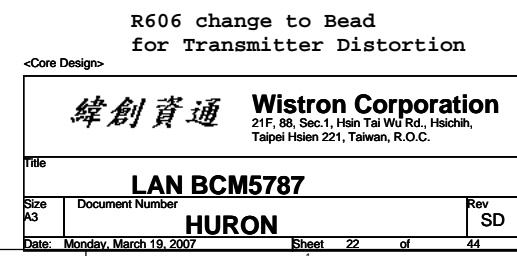


BLUETOOTH MODULE



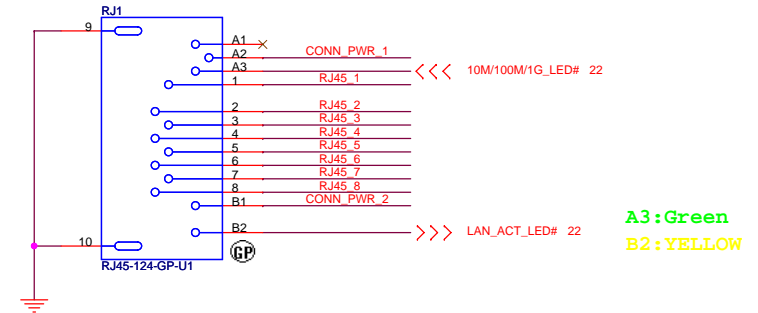
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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB / BLUETOOTH			
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HURON		HURON	
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Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

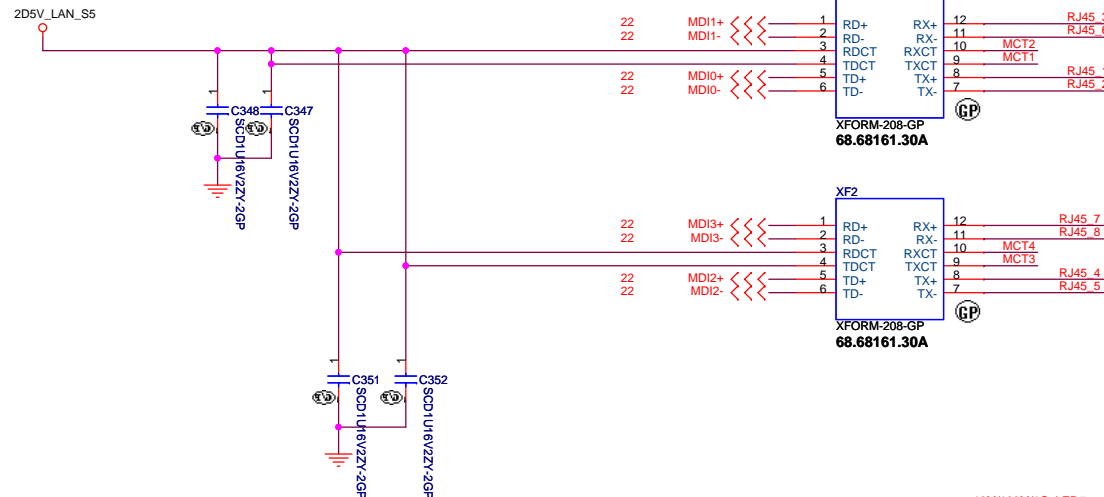
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is
transferring data.

GIGA Lan Transformer

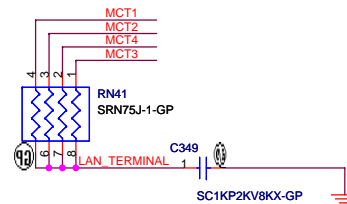
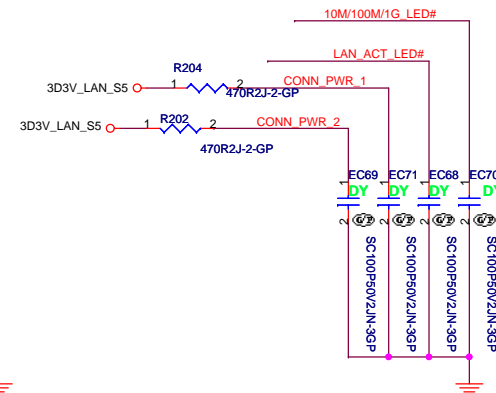


1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAn Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Core Design>

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Title

LAN Connector

Size
A3

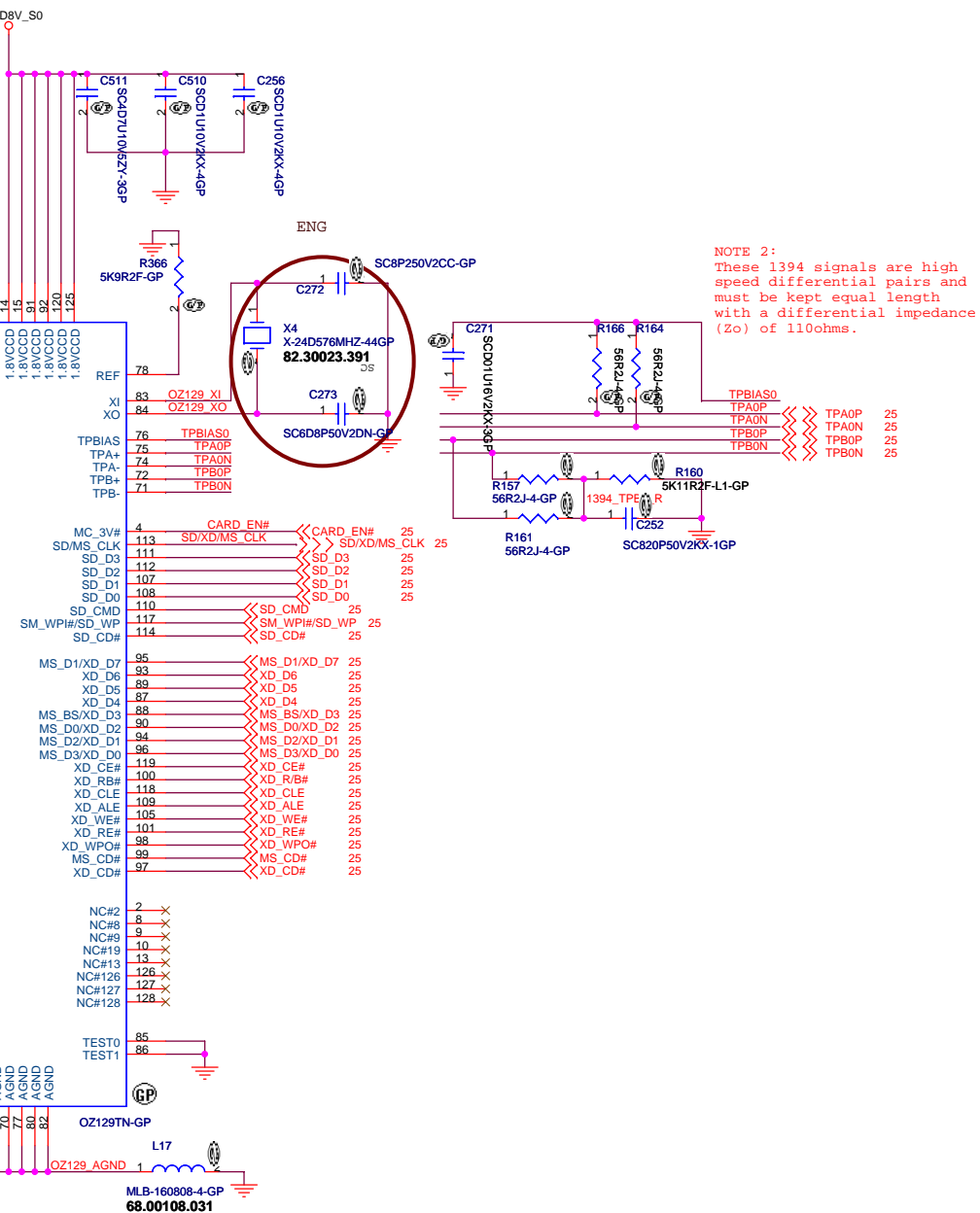
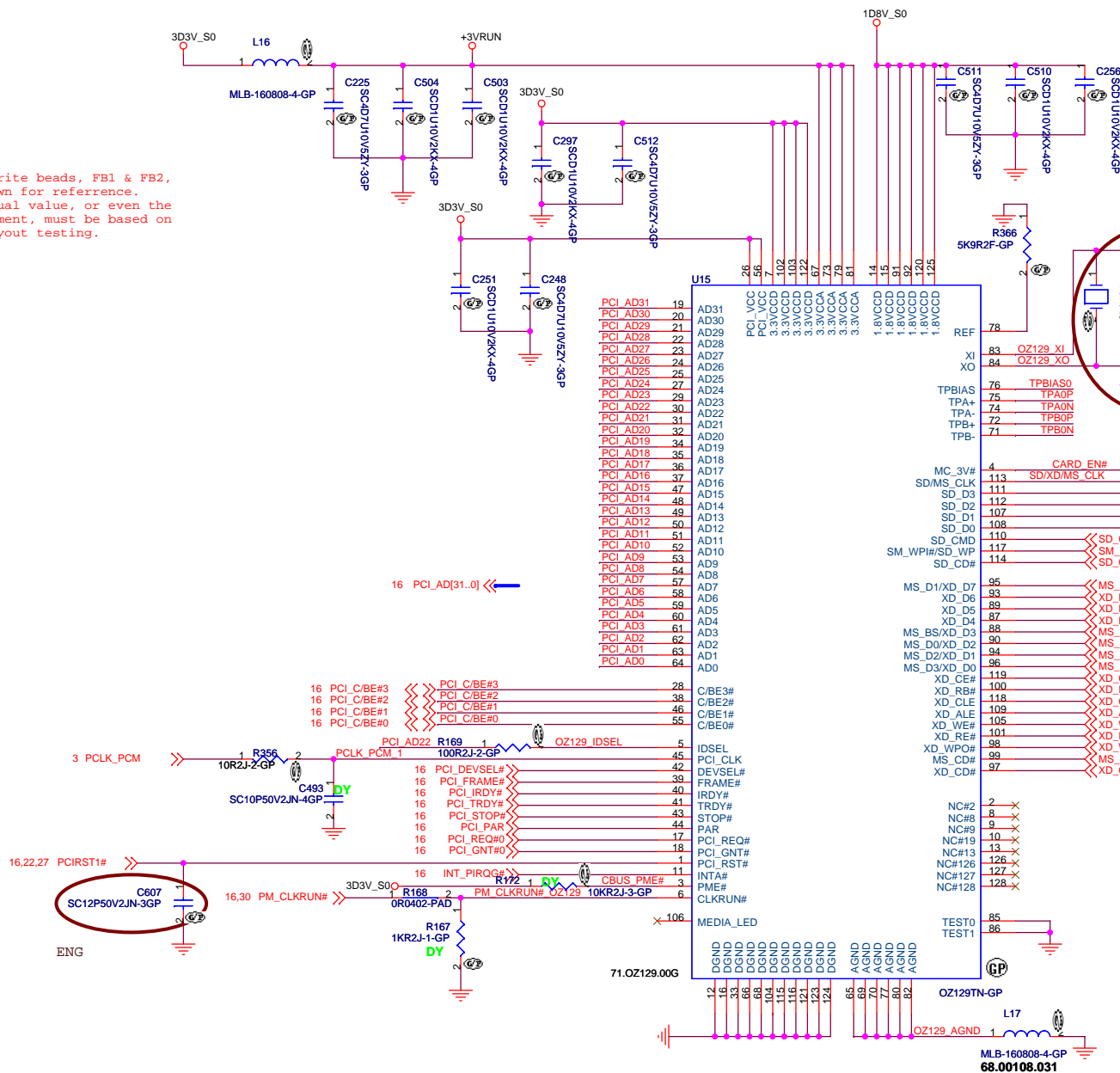
Document Number

HURON

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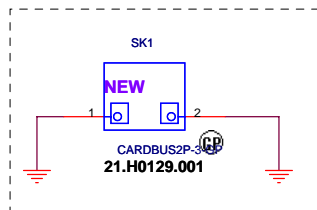
Rev
SD



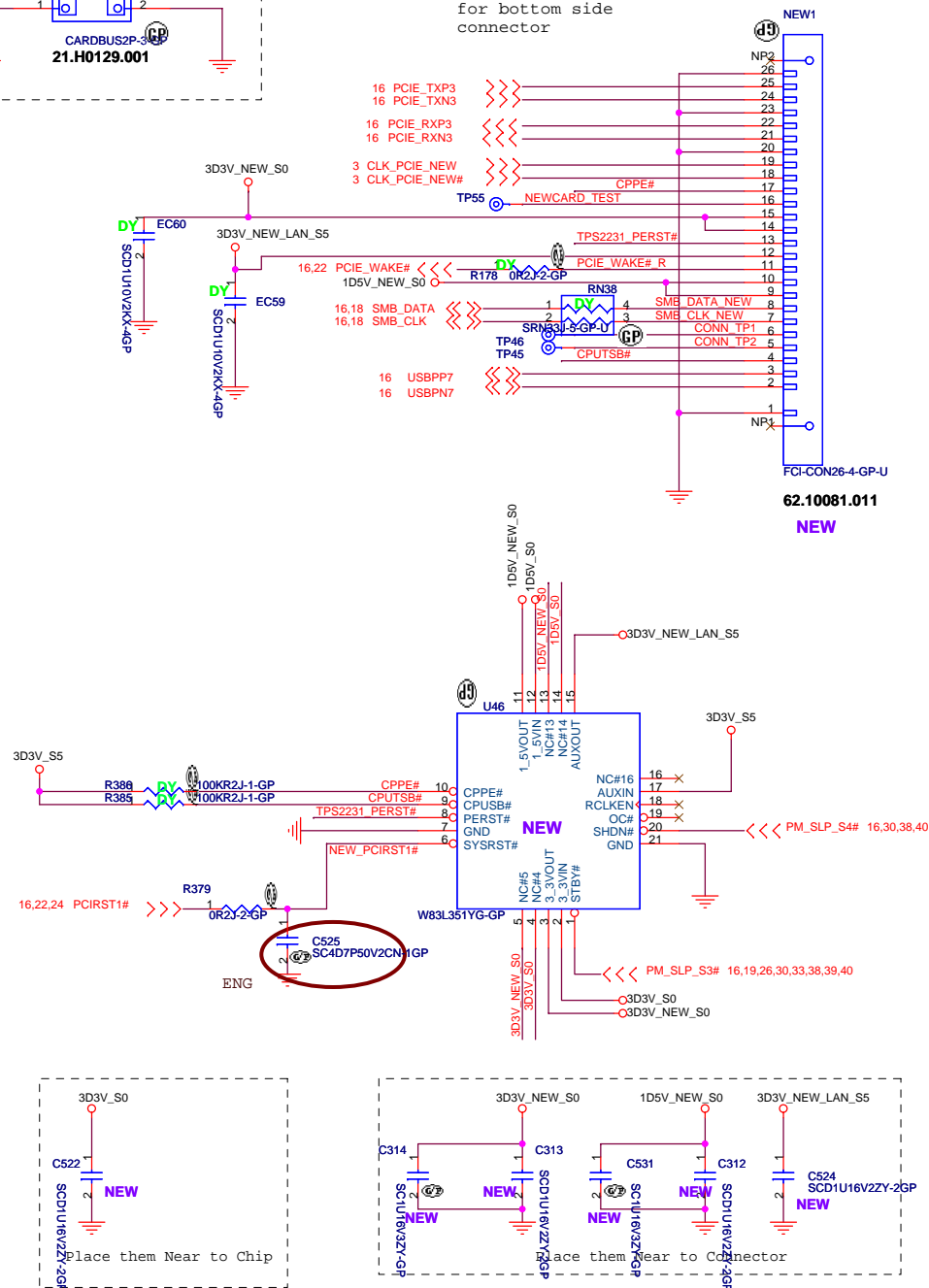
```
IDSEL:AD22
INTA-->:INT_PIRQ#
GNT:PCI_GNT#0
REQ:PCI_REQ#0
```



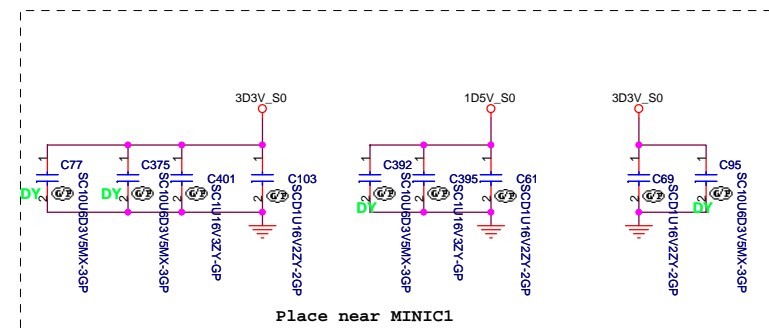
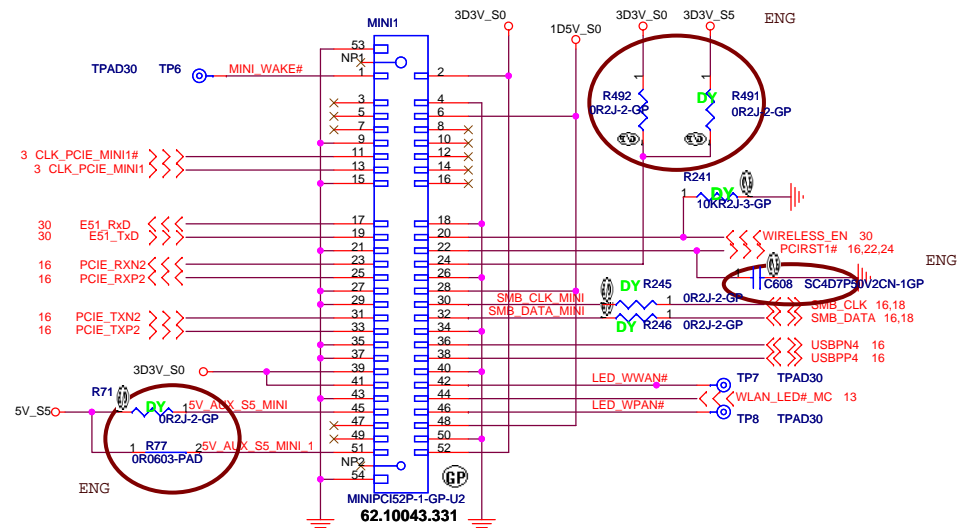

NEWCARD Connector



Reserve the symbol
for bottom side
connector



Mini Card Connector

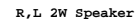


<Core Design>

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Title		
MINI CARD / NEW CARD		
Size	Document Number	Rev
	HURON	SD
Date: Wednesday, March 14, 2007		
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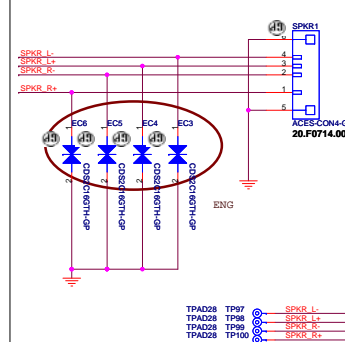
KBC_MUTE_GPI08



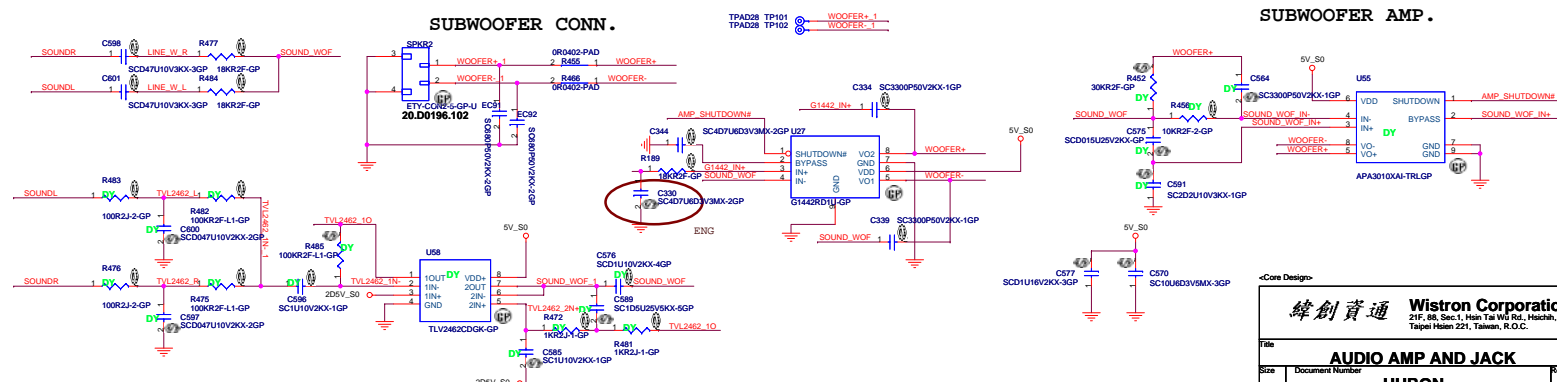
Internal Microphone

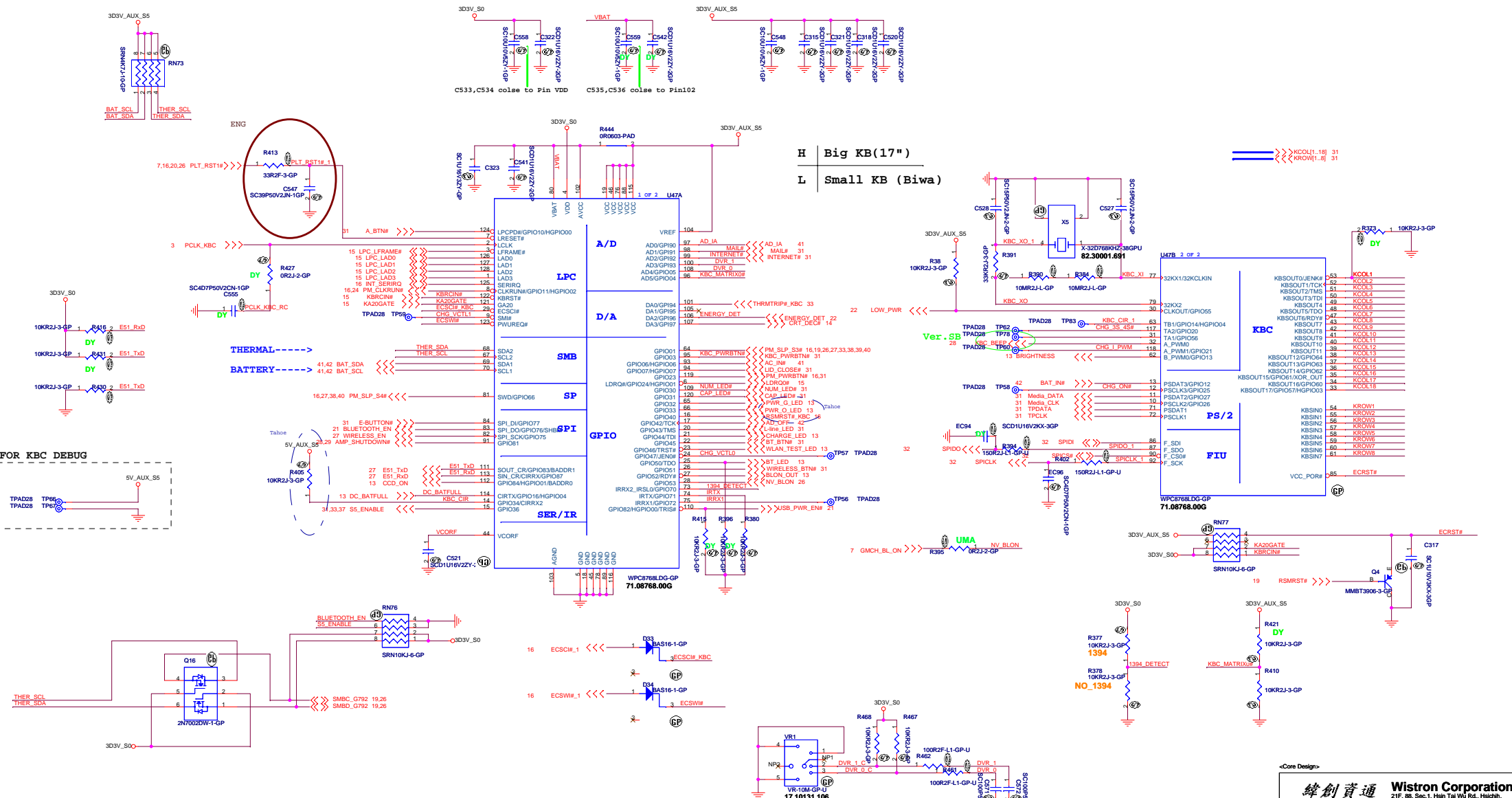


TPAD28	TP97	SPKR L-
TPAD28	TP98	SPKR L+
TPAD28	TP99	SPKR R-
TPAD28	TP100	SPKR R+



SUBWOOFER AMP.



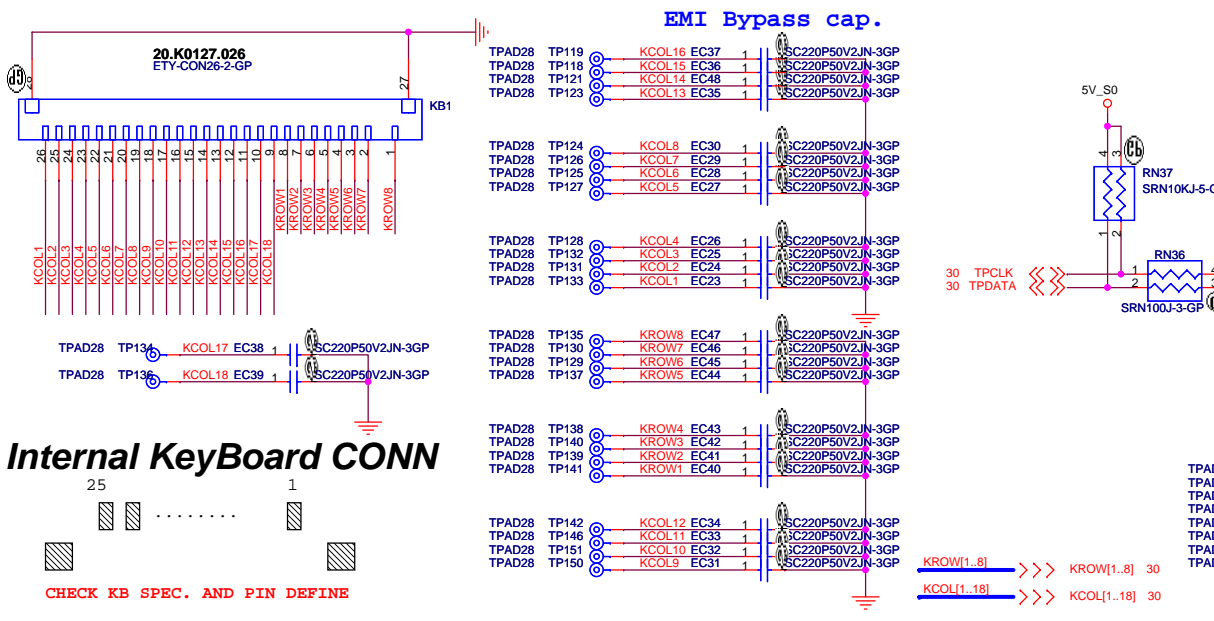
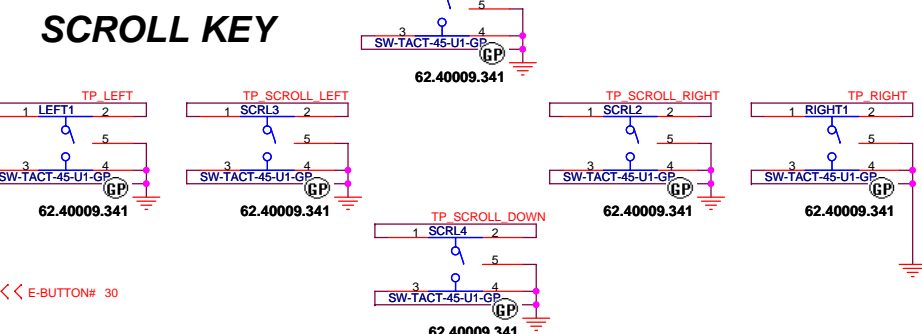
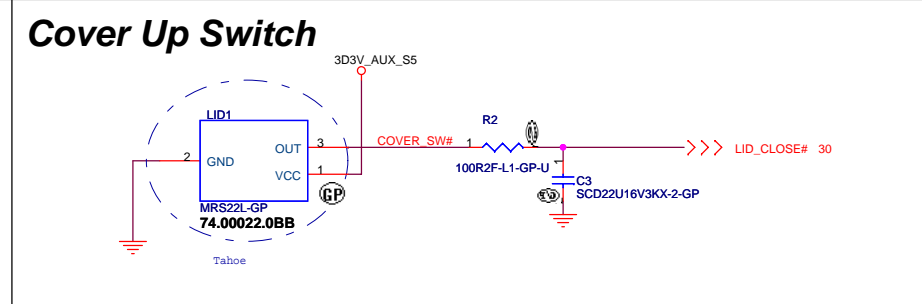
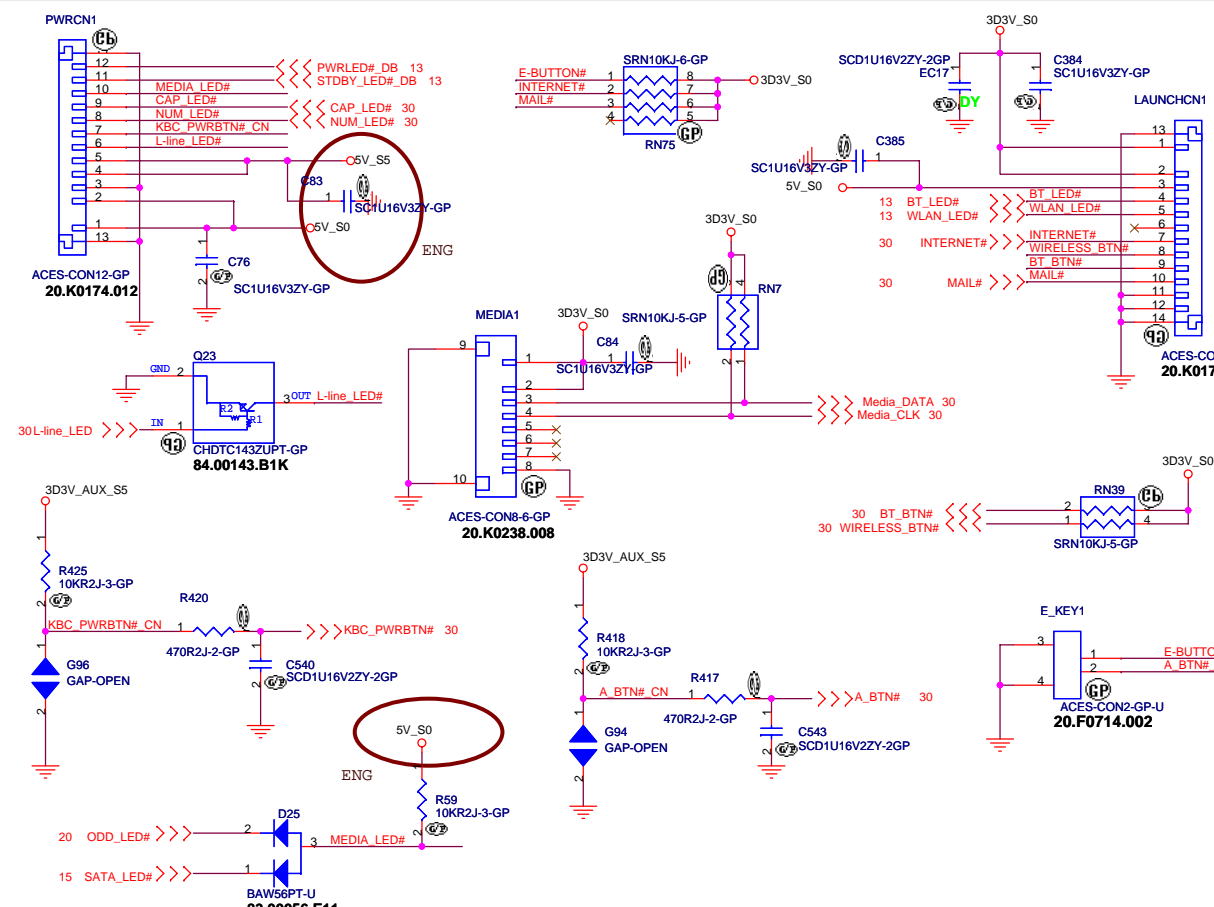


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Taipei Hsin 221, Taiwan, R.O.C.

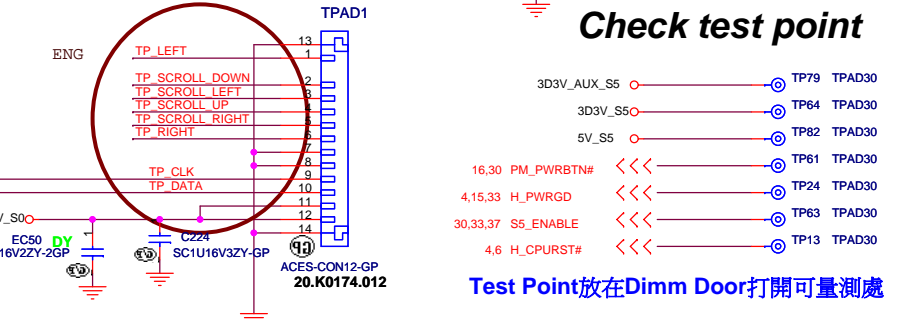
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Size	Document Number	Rev
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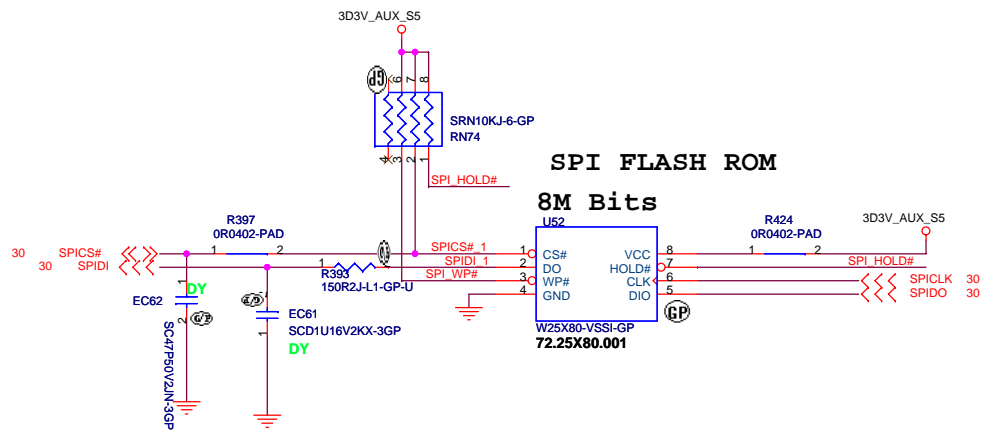


TPAD28	TP103	MAIL#	SC100P50V2JN-3GP	EC86
TPAD28	TP105	INTERNET#	SC100P50V2JN-3GP	EC85
TPAD28	TP104	WLAN_LED#	SC100P50V2JN-3GP	EC82
TPAD28	TP106	BT_LED#	SC100P50V2JN-3GP	EC83
TPAD28	TP108	MEDIA_LED#	SC100P50V2JN-3GP	EC18
TPAD28	TP110	STDBY_LED#_DB	SC100P50V2JN-3GP	EC77
TPAD28	TP109	A_BTN#_CN	SC100P50V2JN-3GP	EC76
TPAD28	TP111	E-BUTTON#	SC100P50V2JN-3GP	EC8
TPAD28	TP113	L-line_LED#	SC100P50V2JN-3GP	EC81
TPAD28	TP112	KBC_PWRBTN#_CN	SC100P50V2JN-3GP	EC78
TPAD28	TP115	NUM_LED#	SC100P50V2JN-3GP	EC79
TPAD28	TP114	CAP_LED#	SC100P50V2JN-3GP	EC80
TPAD28	TP116	Media_DATA	SC100P50V2JN-3GP	EC100
TPAD28	TP117	Media_CLK	SC100P50V2JN-3GP	EC99
TPAD28	TP120	WIRELESS_BTN#	SCD1U16V2ZY-2GP	EC93
TPAD28	TP122	BT_BTN#	SCD1U16V2ZY-2GP	EC95



Internal KeyBoard CONN

CHECK KB SPEC. AND PIN DEFINE



<Core Design>

緯創資通

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Title

BIOS

Size
A3

Document Number

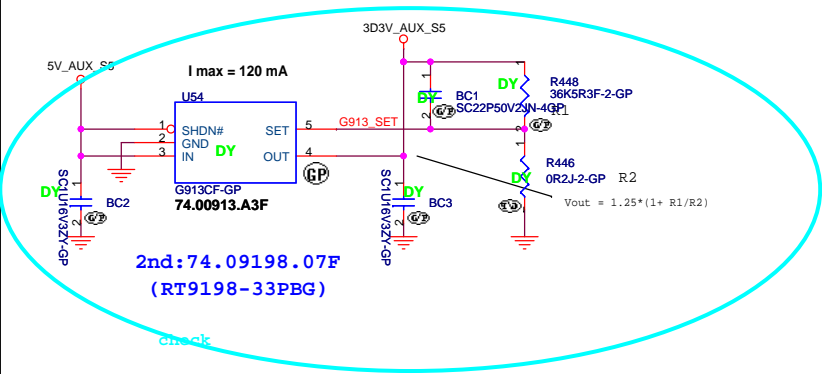
HURON

Rev
SD

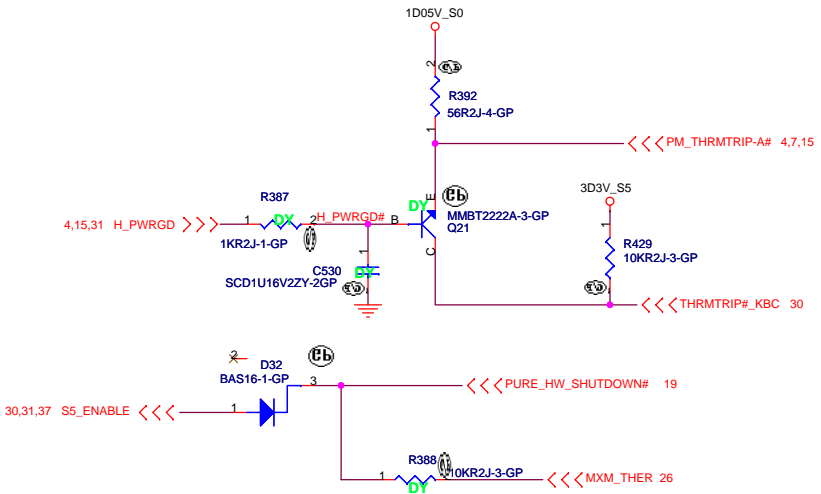
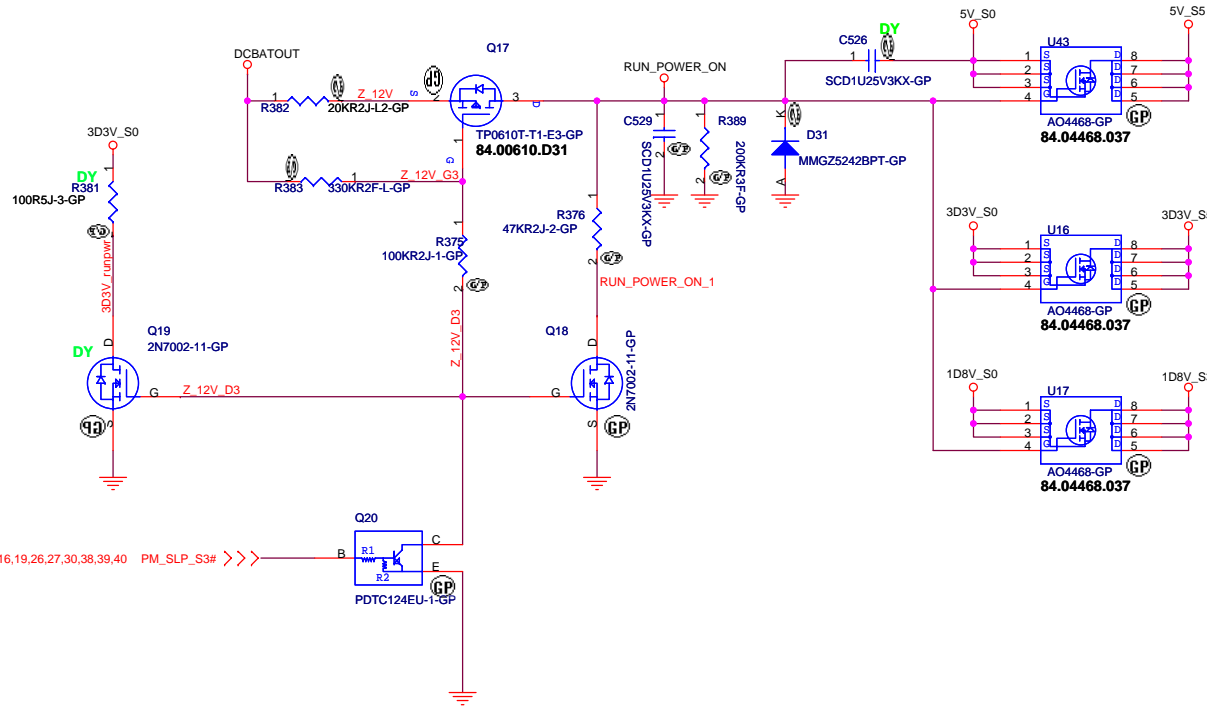
Date: Monday, March 12, 2007

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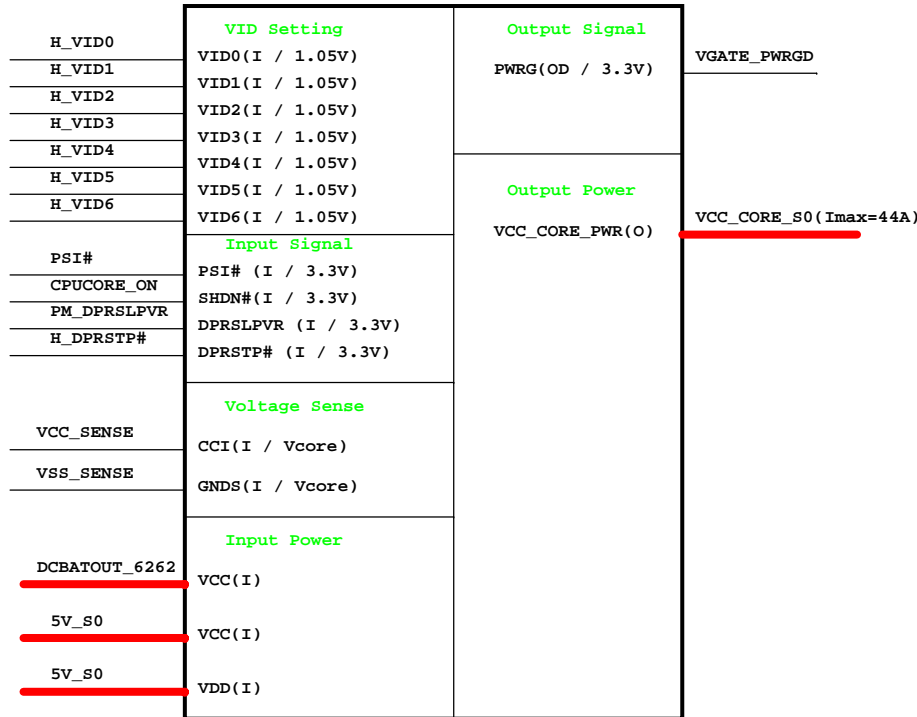
Aux Power 3D3V_AUX_S5



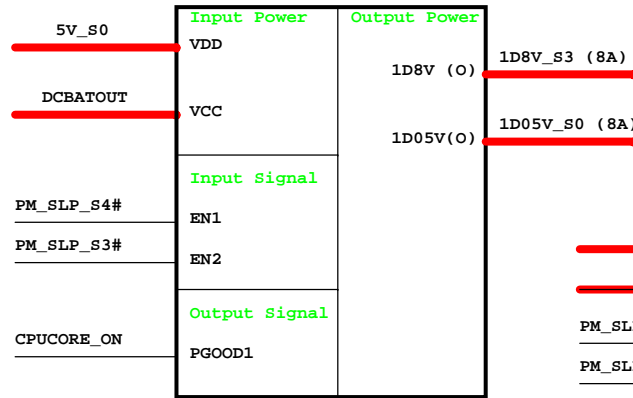
Run Power



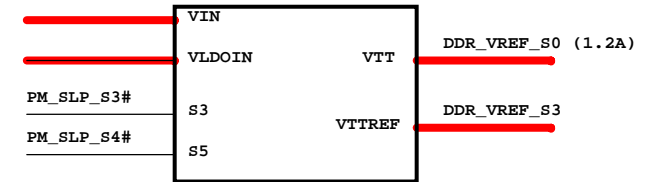
CPU_CORE
ISL6262



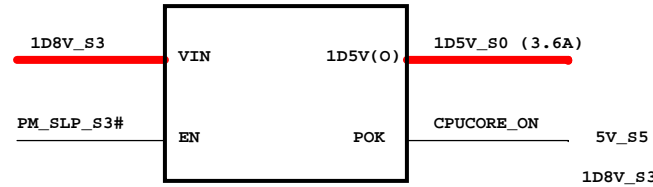
TPS51124
1D8V_S3 / 1D05V_S0



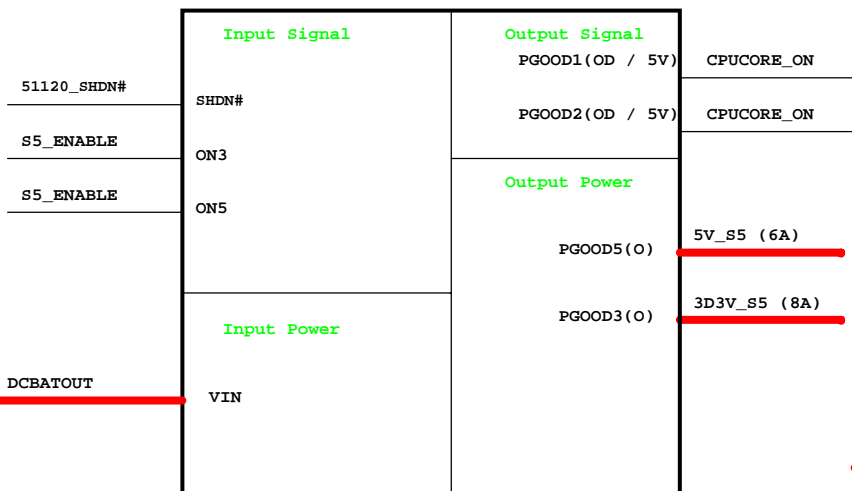
TPS51100
DDR_VREF_S0



API5912
1D5V_S0



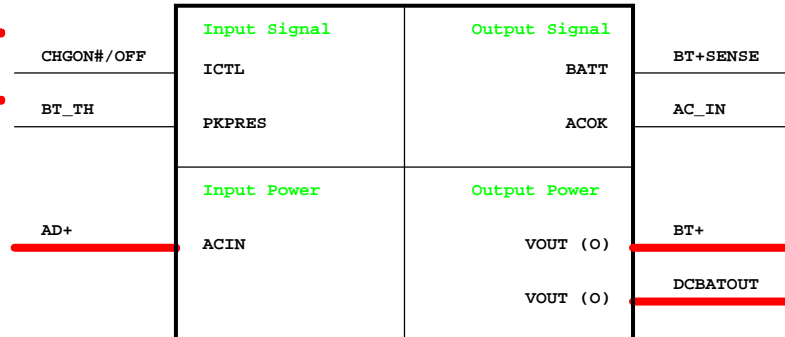
TPS51120
5V_S5 / 3D3V_S5



APL5308
2D5V_S0



Charger MAX8731A

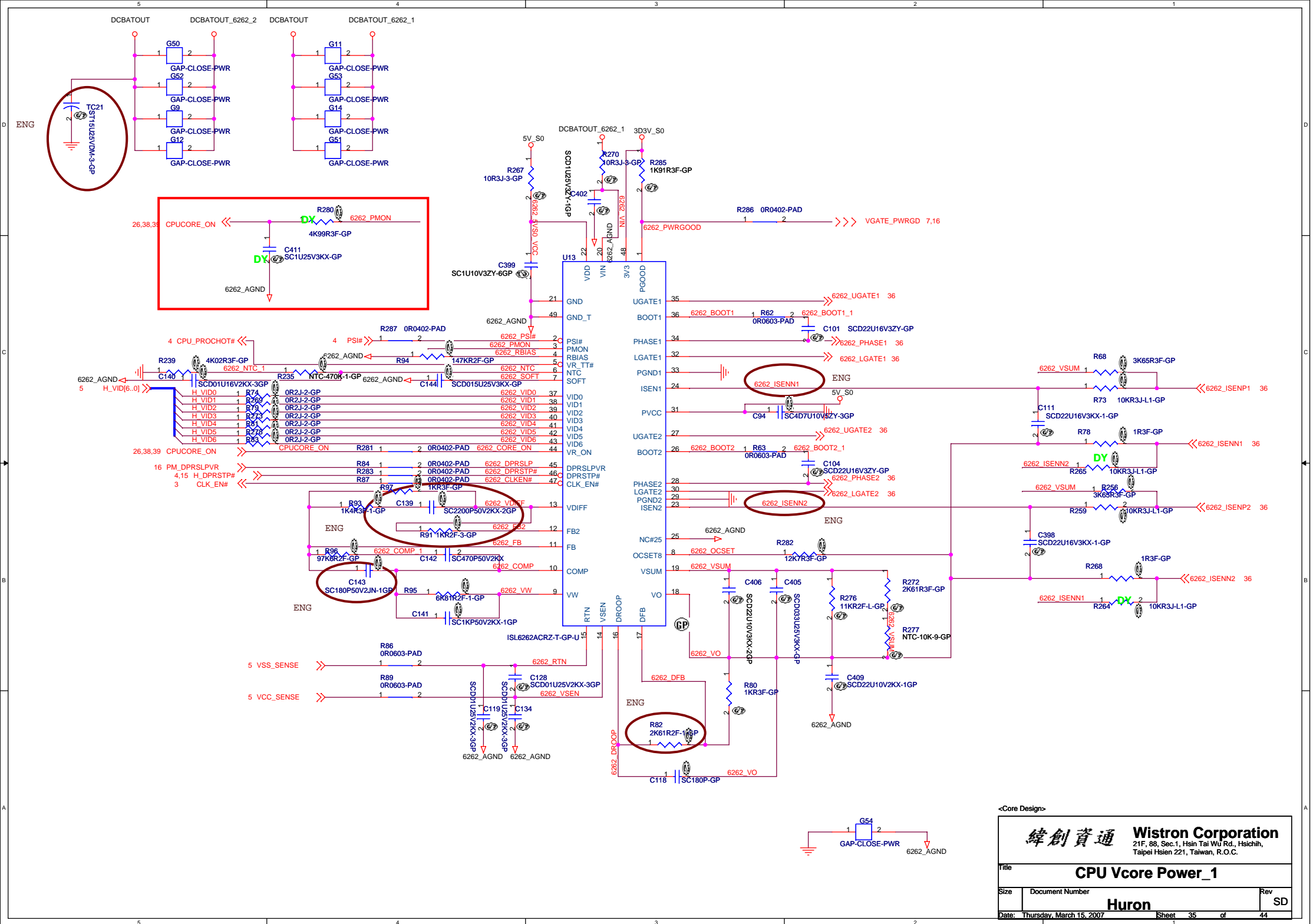


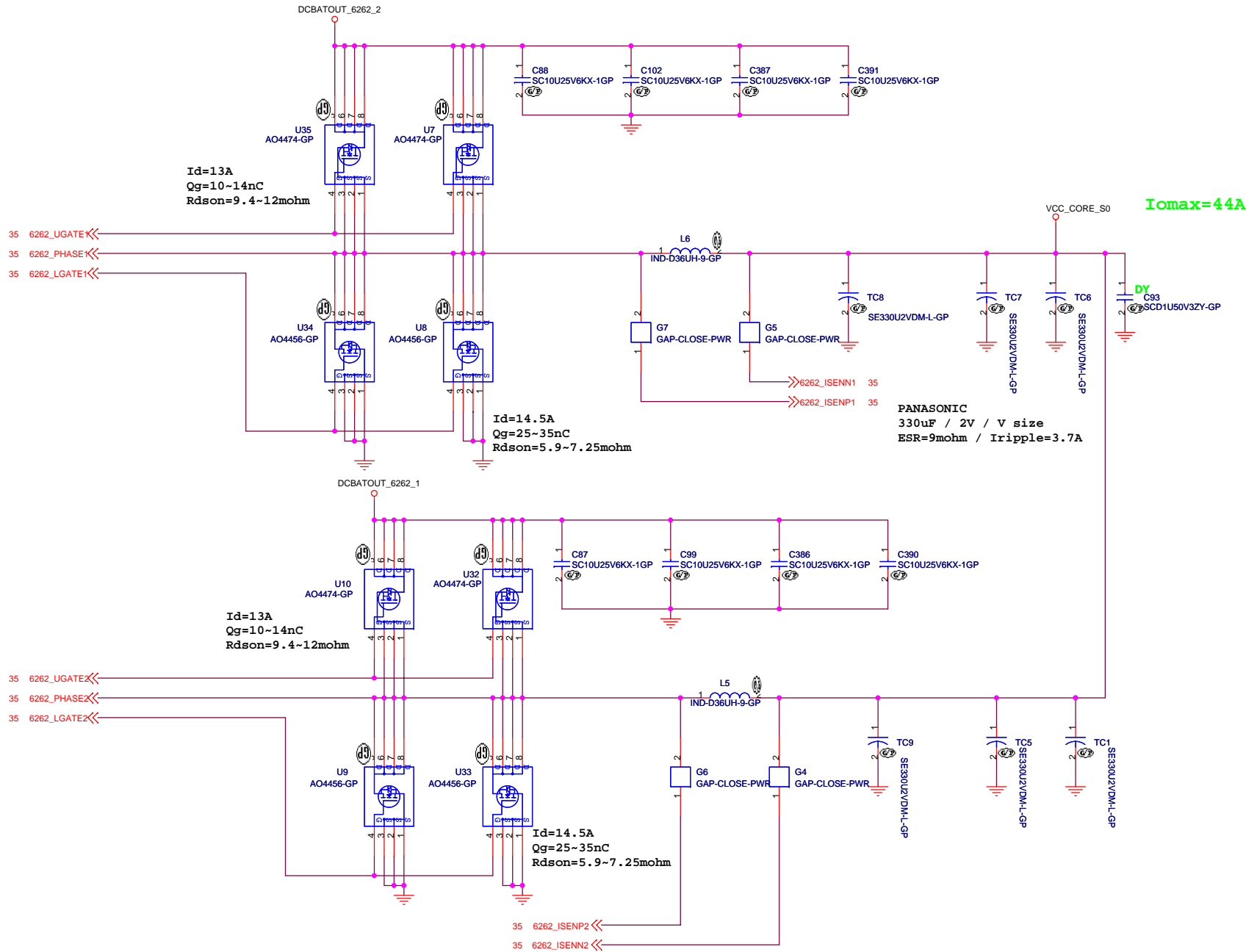
<Core Design>

緯創資通

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Title			Power Block Diagram	
Size	Document Number	Huron		Rev
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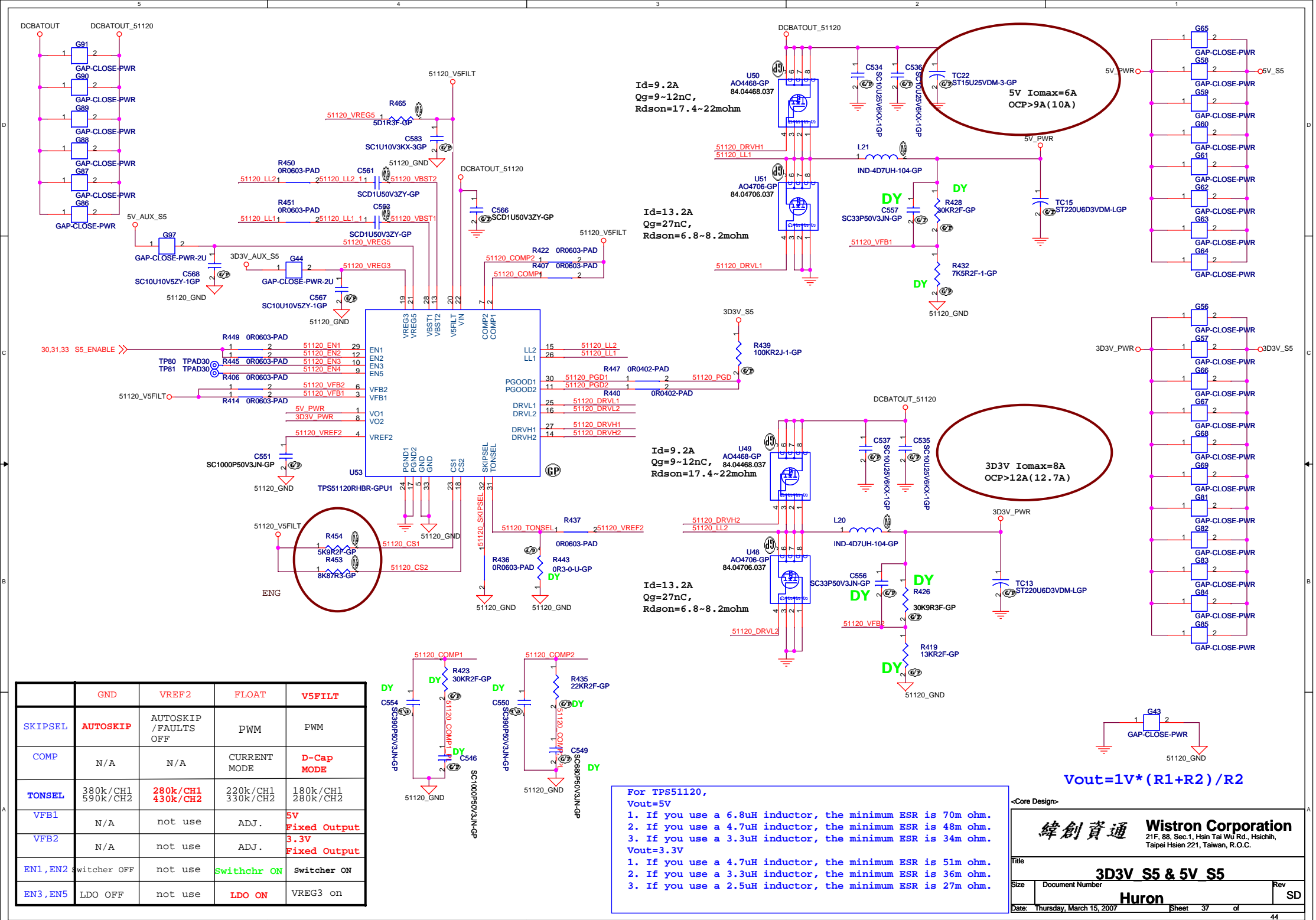


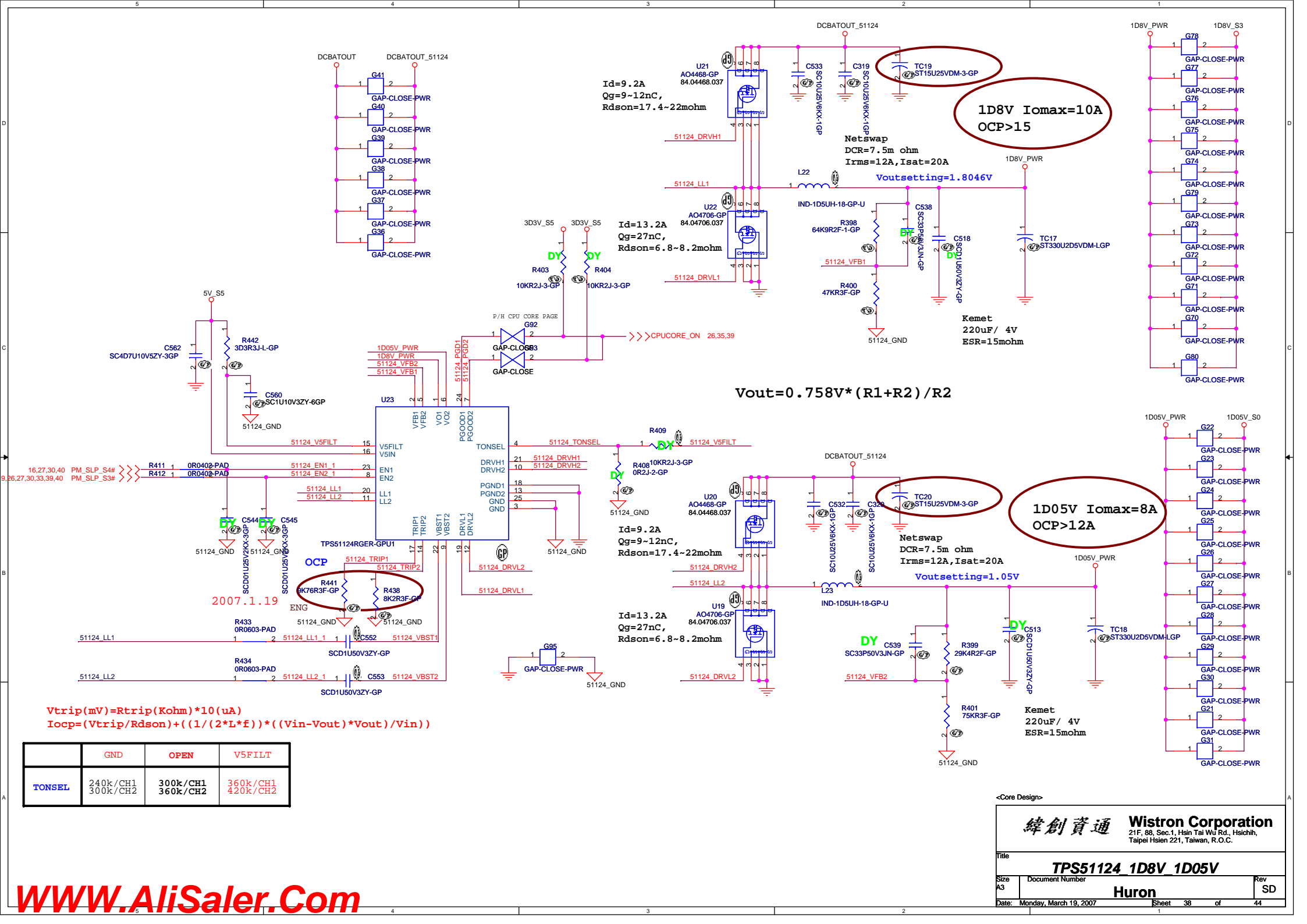


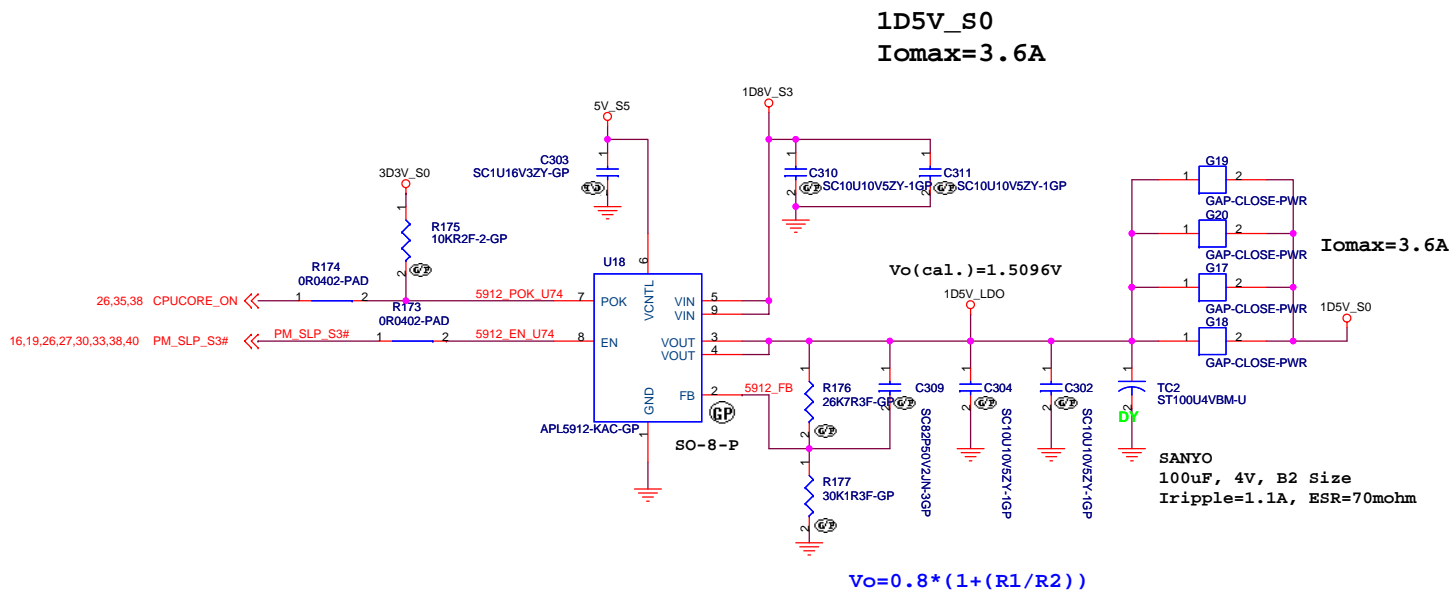
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Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU Vcore Power_2	
Size	Document Number		Rev	
	Huron		SD	
Date:	Monday, March 12, 2007		Sheet	36 of 44



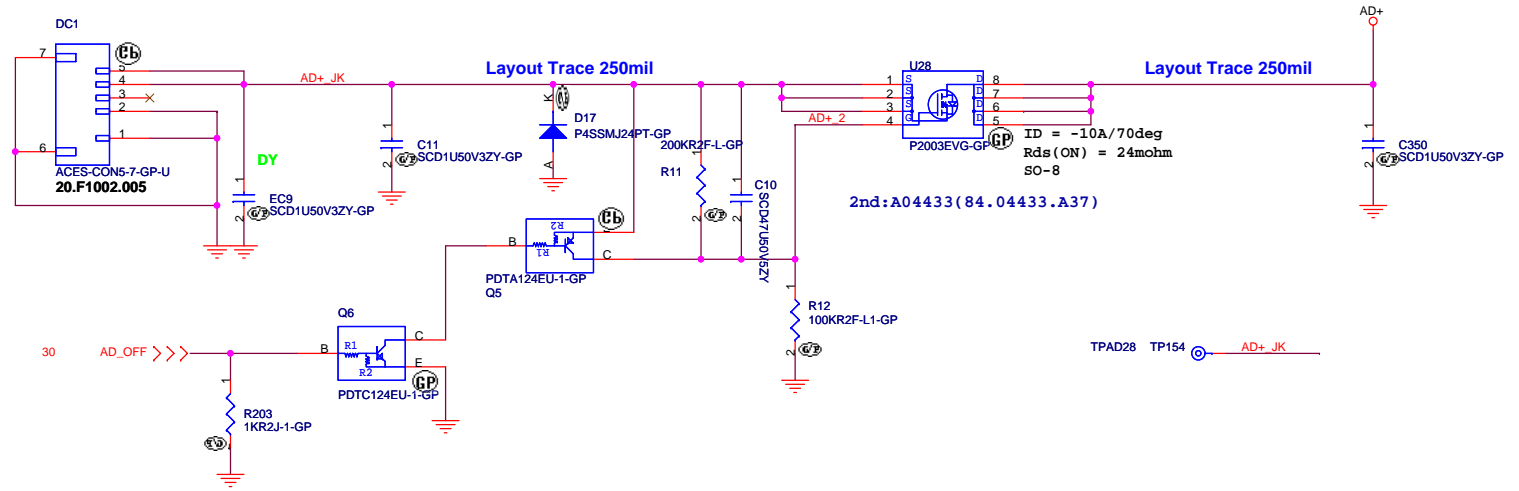




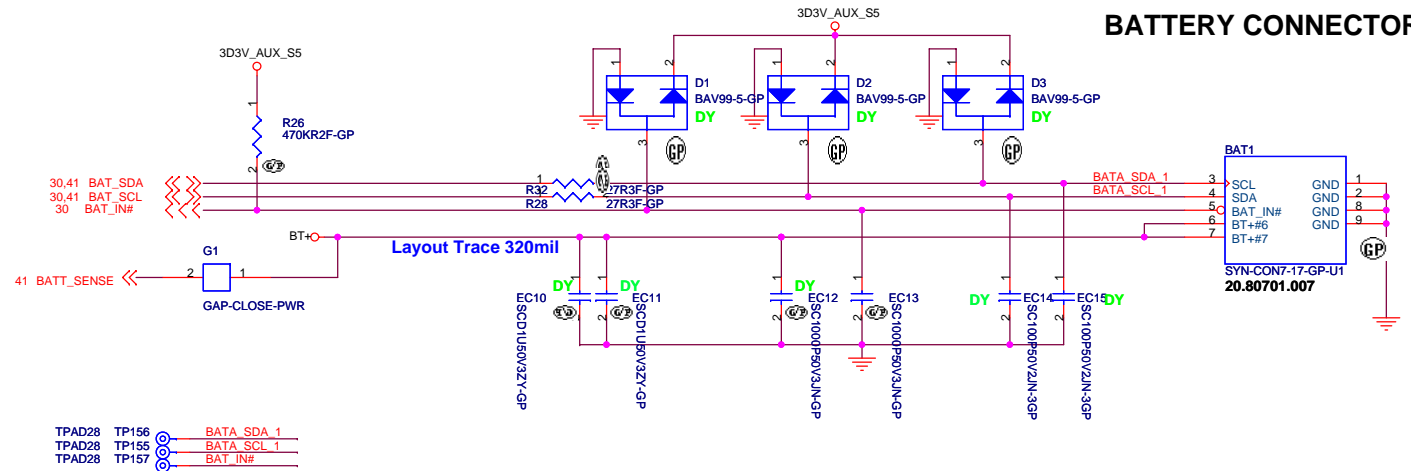
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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
APL5912_1D5V			
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Adaptor in to generate DCBATOUT



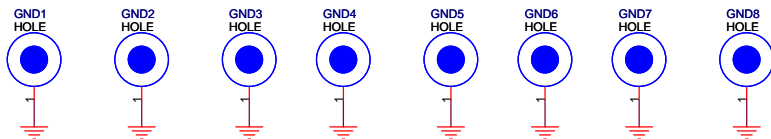
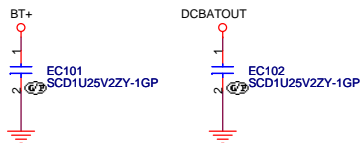
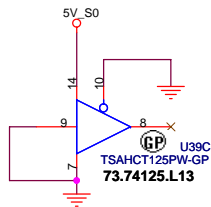
BATTERY CONNECTOR



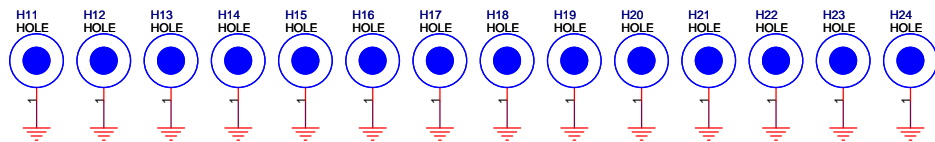
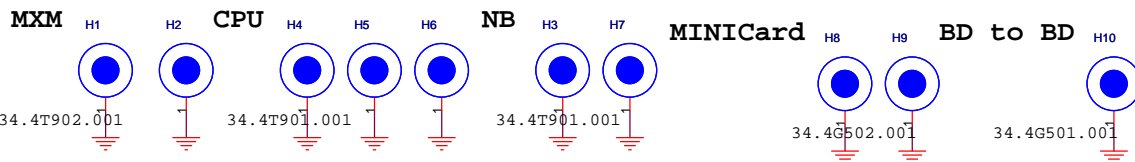
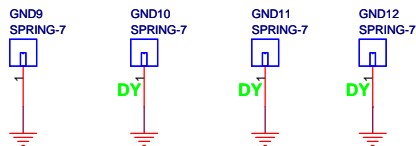
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緯創資通 Wistron Corporation
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Title		AD/BATT CONN	
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A3		SD	
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Spring



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