Compal Confidential

Model Name : P5LJ0 & P5LS0
File Name : LA-7221P

Compal Confidential

JM50-HR M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P-GS/GV

2010-02-16

REV:0.5

MB PCB

Part Number	Description
DA80000MA00	PCB 0IN LA-7221P REV0 M/B

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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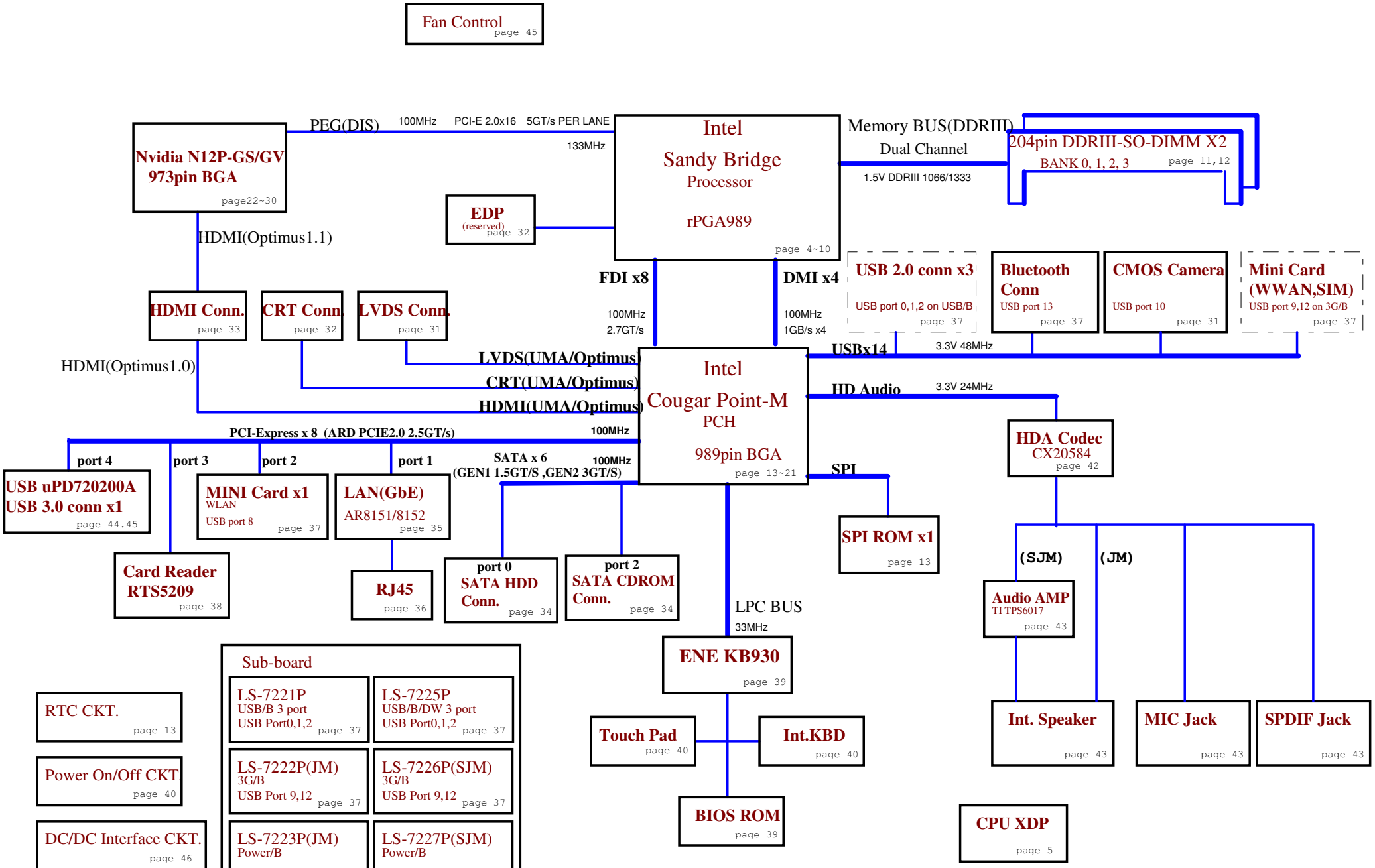
Title	Cover Page	
Size: Custom	Document Number: LA-7221P	Rev: 0.2
Date: Friday, February 18, 2011	Sheet 1 of 59	



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
UMA with OPTIMUS	UMA@
OPTIMUS1.0	OPT@
OPTIMUS1.1	OPT11@
N12P-GS@	GS@
N12P-GV@	GV@
VRAM	X76@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
EDP	EDP@
LAN Chip AR8151	8151@
LAN Chip AR8152	8152@
JM Board	JM@
SJM Board	SJM@
Unpop	@
Power GPU	VGA@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	Mini Card(WWAN)
	UHCI5	10	Camera
		11	
	UHCI6	12	SIM Card
		13	Blue Tooth

3G & BT Config

3G SKU: 3G@

BT SKU: BT@

BOM Config

JM UMA Only: BT@/3G@/UMA@/UMAO@/JM@/8151@

JM OPTIMUS: BT@/3G@/UMA@/OPT@/JM@/8151@/GV@/GS@

SJM UMA Only: BT@/3G@/UMA@/UMAO@/SJM@/8151@

SJM OPTIMUS: BT@/3G@/UMA@/OPT@/SJM@/8151@/GV@/GS@

BOM P/N(JM/SJM)

4319BOBOL01/L21 UMA W3G HDMI
4319BOBOL02/L22 UMA N3G HDMI
4319BOBOL03/L23 N12PGS 1GW3G HDMI
4319BOBOL04/L24 N12PGS 1GN3G HDM
4319BOBOL05/L25 N12PGS 2GW3G HDMI
4319BOBOL06/L26 N12PGS 2GN3G HDMI
4319BOBOL07/L27 N12PGV 512W3G HDMI
4319BOBOL08/L28 N12PGV 512N3G HDMI

VRAM BOM Config

X76289BOL01 512M SAM 64M16
X76289BOL02 512M HYN 64M16
X76289BOL03 1G SAM 64M16
X76289BOL04 1G HYN 64M16
X76289BOL05 2G SAM 128M16
X76289BOL06 2G HYN 128M16

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Title: Notes List

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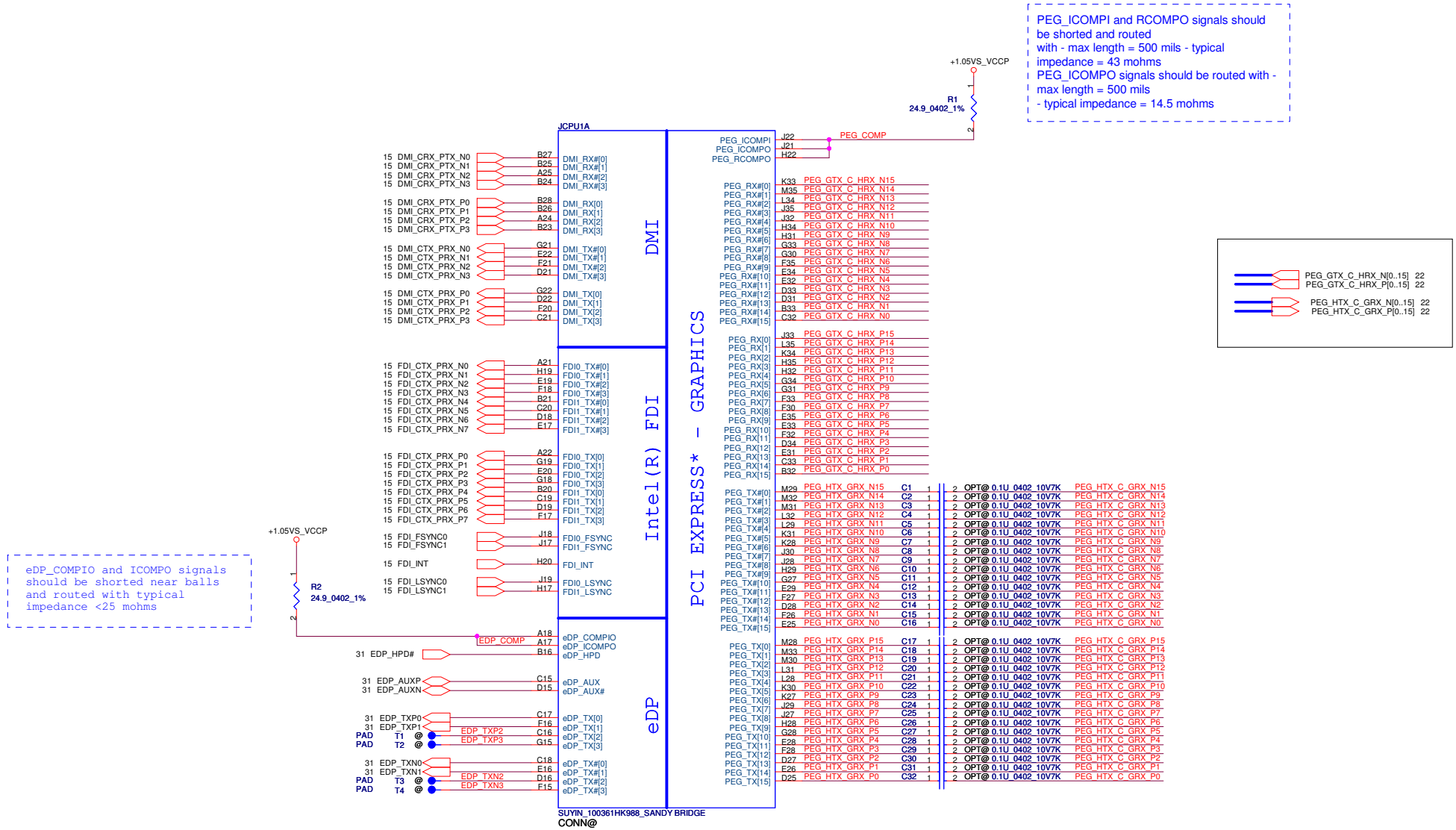

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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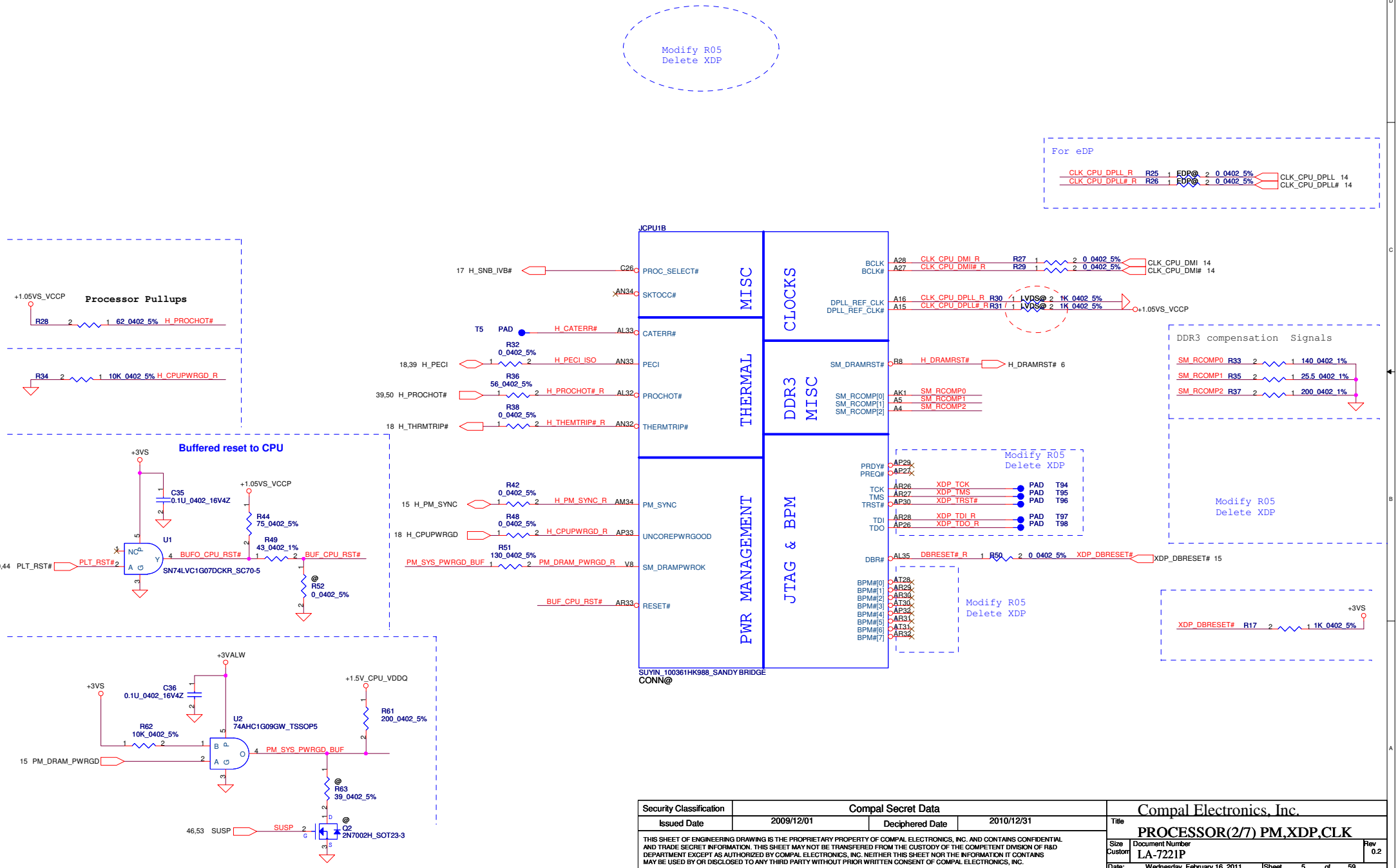

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Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

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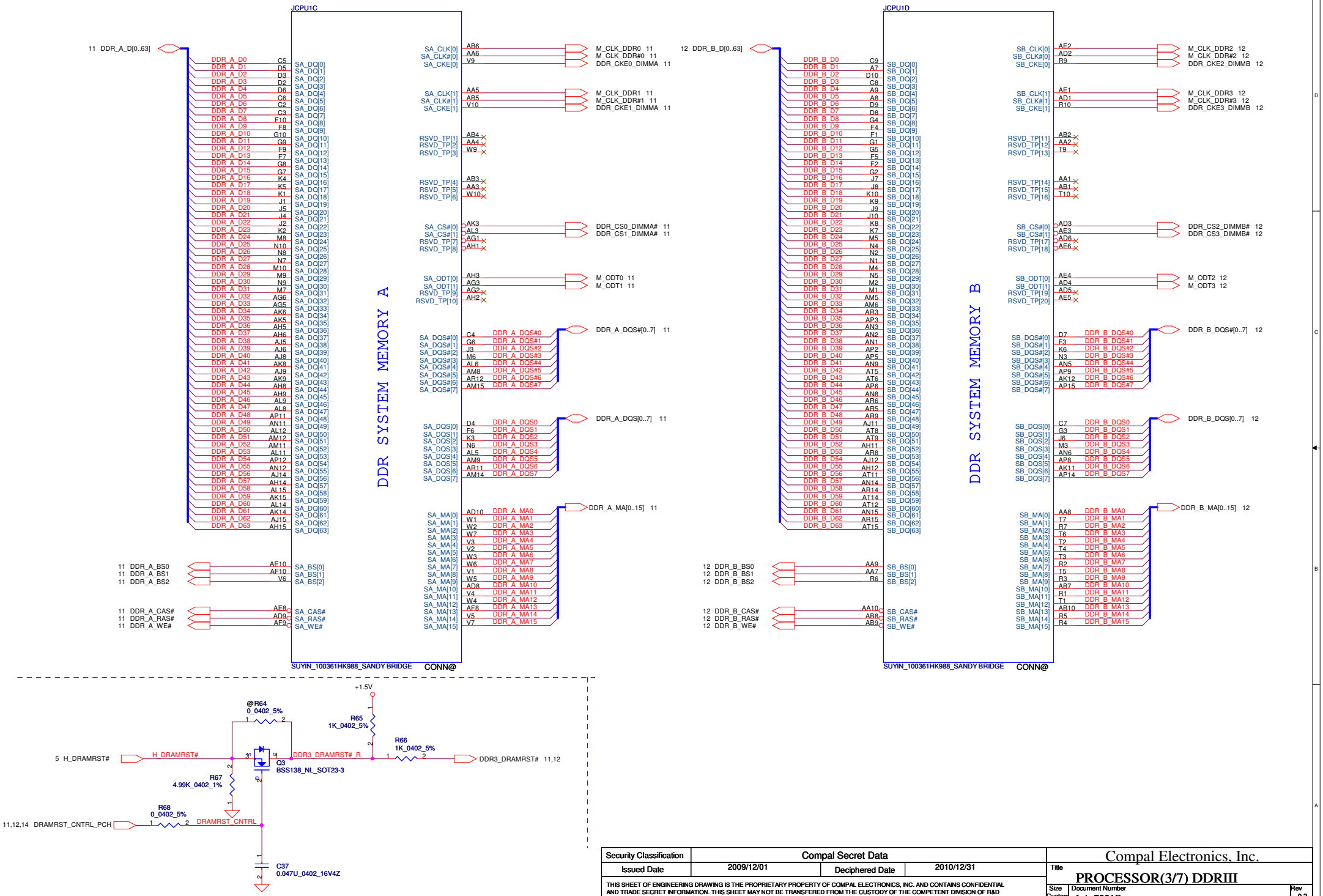

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Title: PROCESSOR(3/7) DDRIII

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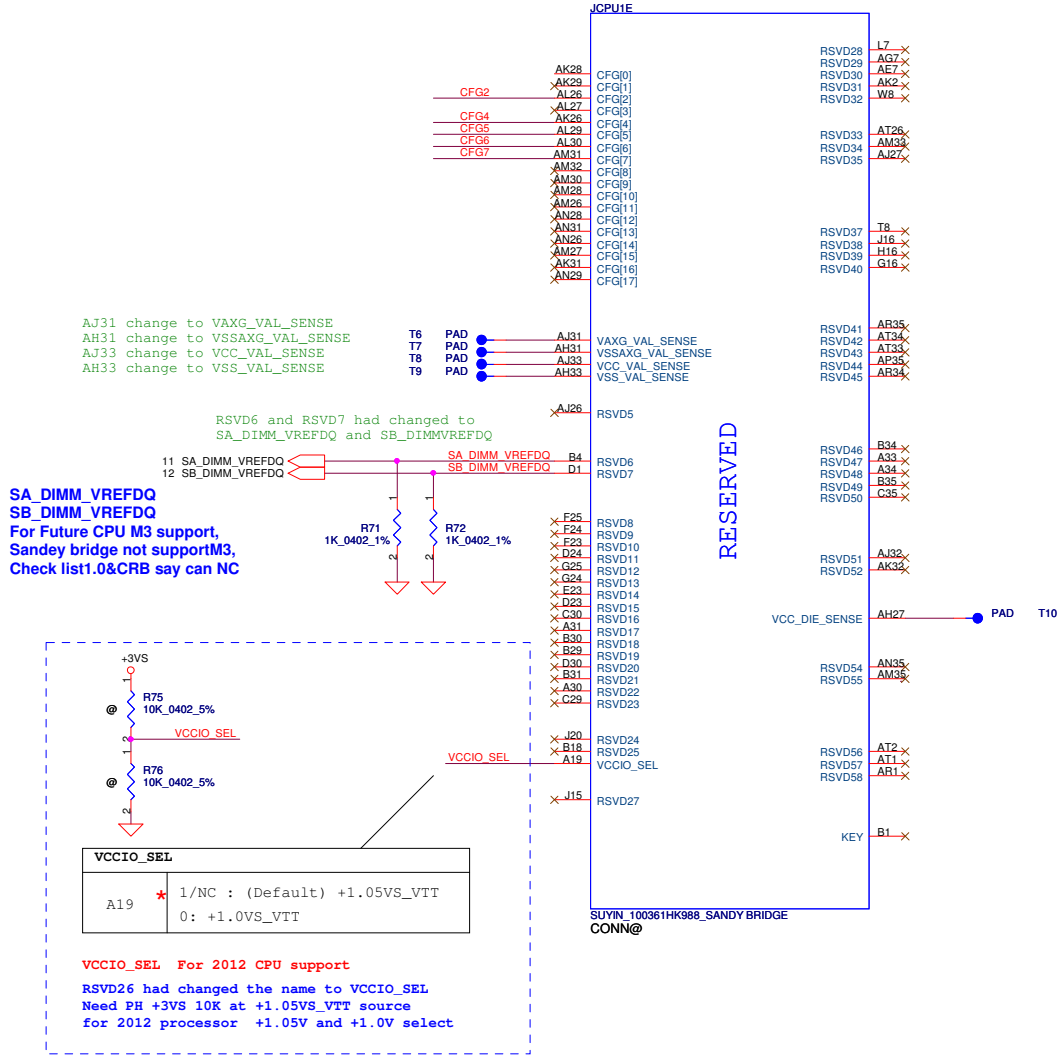
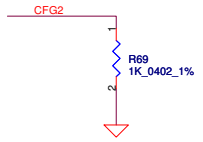
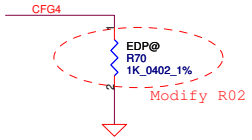
CFG Straps for Processor

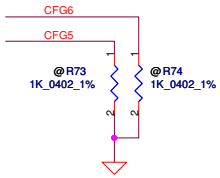




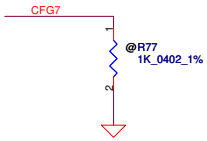
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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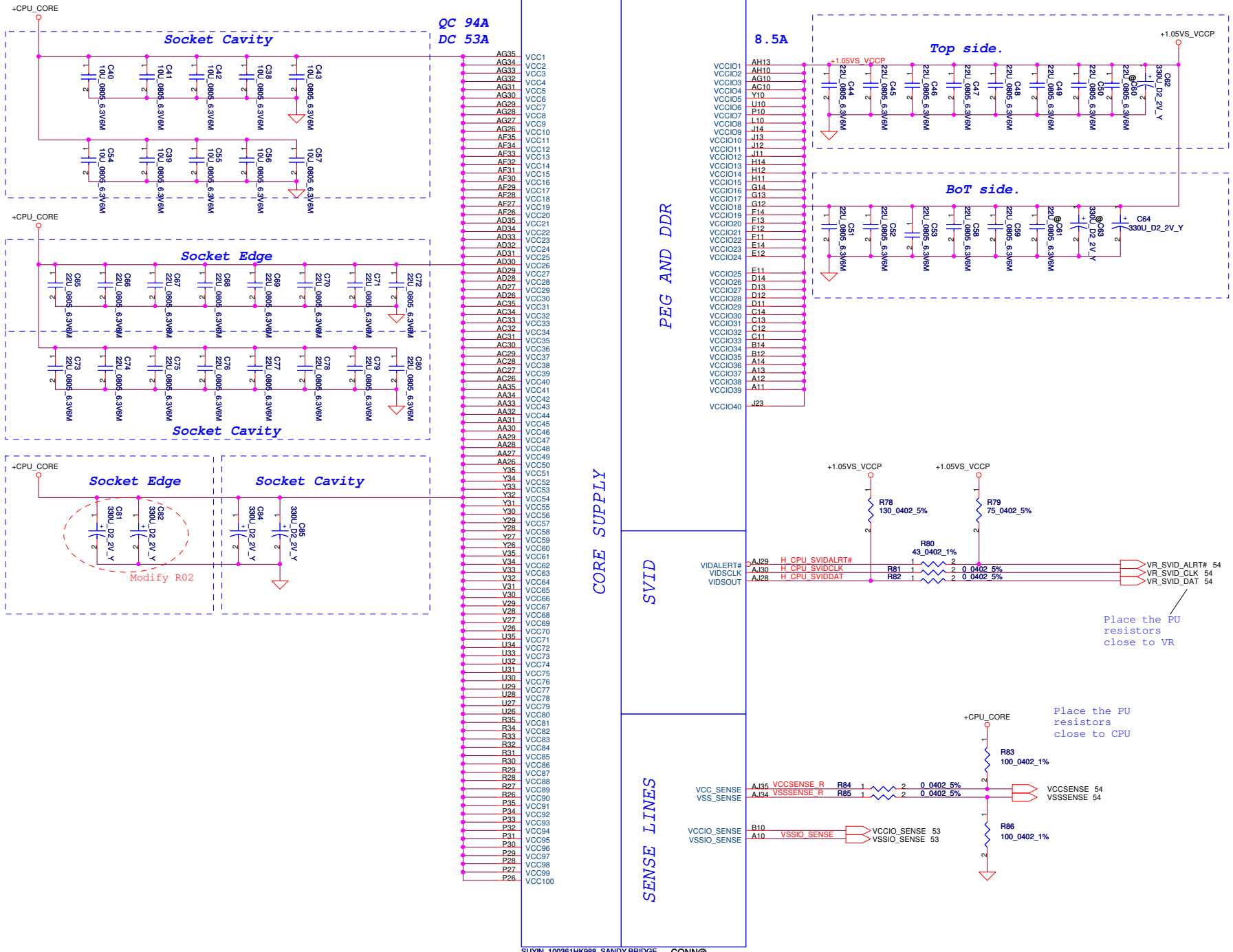
POWER

SV type CPU

QC 94A
DC 53A

4x 470 µF Bottom Socket Edge
8x 22 µF Top Socket Cavity
8x 22 µF Top Socket Edge
10x 10 µF Bottom Socket Cavity



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Title: PROCESSOR(5/7) PWR,BYPASS

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Delete
+1.5V_CPU_VDDQ Source

POWER

QC 33A
DC 26A

JCPU1G

+VGFX_CORE

2x 470 µF Bottom Socket Edge
2x 22 µF Top Socket Cavity
4x 22 µF Top Socket Edge
2x 470 µF Bottom Socket Cavity
4x 22 µF Bottom Socket Edge

C95 22U_0805_6.3V6M, C89 22U_0805_6.3V6M, C90 22U_0805_6.3V6M, C96 22U_0805_6.3V6M, C91 22U_0805_6.3V6M, C92 22U_0805_6.3V6M
C93 22U_0805_6.3V6M, C97 22U_0805_6.3V6M, C98 22U_0805_6.3V6M, C94 22U_0805_6.3V6M, C99 22U_0805_6.3V6M, C100 22U_0805_6.3V6M
C102 330U_D2_2V_Y, C103 330U_D2_2V_Y, @C104 22U_0805_6.3V6M, @C105 22U_0805_6.3V6M

Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

GRAPHICS

SENSE LINES: VAXG_SENSE AK35 → VCC_AXG_SENSE 54; VSSAXG_SENSE AK34 → VSS_AXG_SENSE 54

VREF: SM_VREF AL1 — +V_SM_VREF

+V_SM_VREF should have 20 mil trace width

C101 0.1U_0402_16V4Z

+1.5V_CPU_VDDQ: R94 1K_0402_1%, R95 1K_0402_1%

9/30 DG1.5

DDR3 -1.5V RAILS: 5A
VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

C108 10U_0603_6.3V6M, C109 10U_0603_6.3V6M, C110 10U_0603_6.3V6M, C111 10U_0603_6.3V6M, C112 10U_0603_6.3V6M, C113 10U_0603_6.3V6M, C114 330U_D2_2V_Y

@JP2 PAD-OPEN 4x4m — +1.5VS

Modify R03

SA RAIL: 6A
VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

+VCCSA: C115 10U_0603_6.3V6M, C116 10U_0603_6.3V6M, C117 10U_0603_6.3V6M, @C118 10U_0603_6.3V6M, C119 330U_D2_2V_Y

R96 0_0402_5% VCCSA_SENSE; R97 0_0402_5% VSSSA_SENSE 52

Modify R04

1.8V RAIL: 1.5A
VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

+1.8VS R98 0_0805_5% → +1.8VS_VCCPLL: C120 330U_D2_2V_Y, C121 10U_0603_6.3V6M, C122 1U_0402_6.3V6K, C123 1U_0402_6.3V6K

Modify R05

MISC: VCCSA_SENSE H23 → VCCSA_SENSE 52; FC_C22 C22, VCCSA_VID1 C24 — H_FC_C22 → VCCSA_VID1 52

R99 10K_0402_5%, @R100 0_0402_5%

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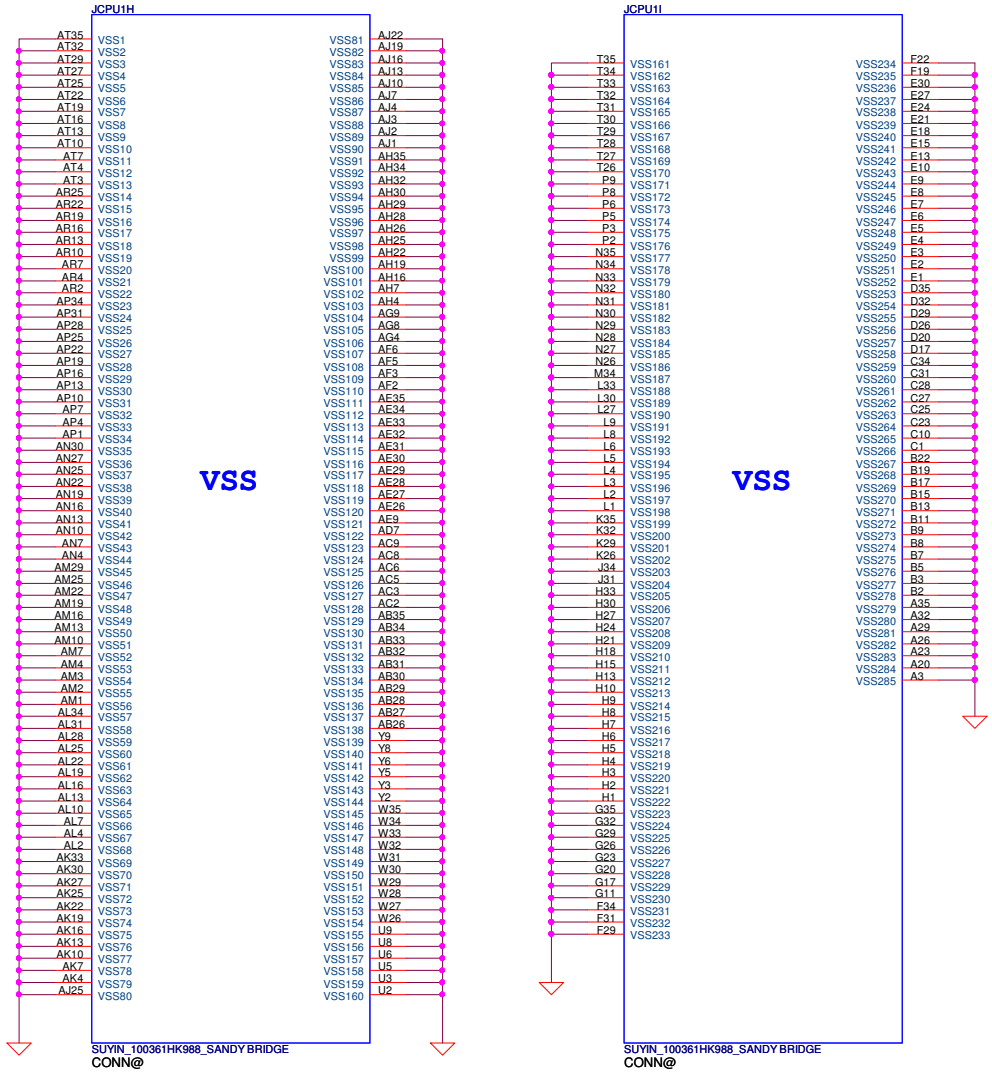

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Title: PROCESSOR(7/7) VSS

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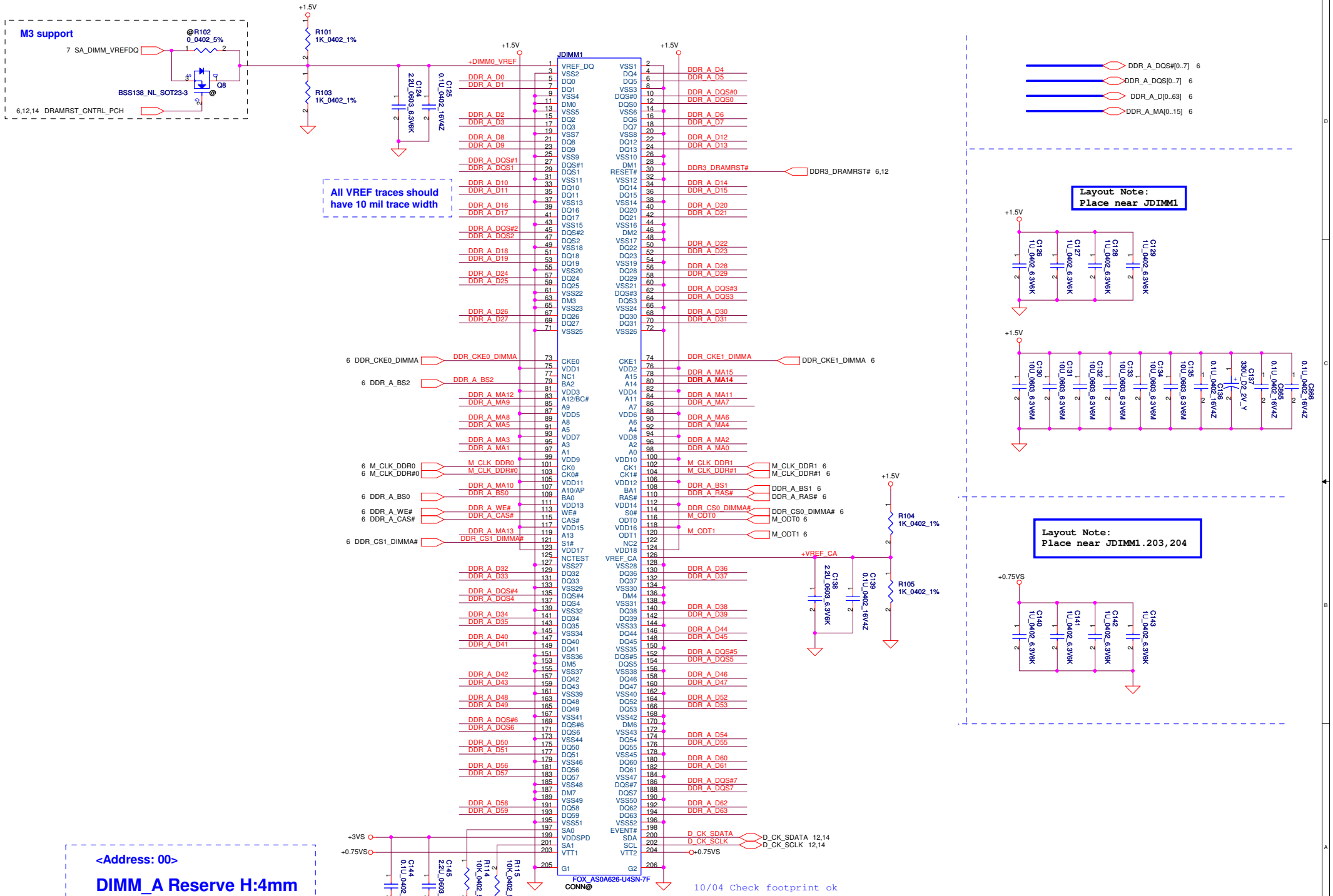

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Title: DDRIII DIMMA

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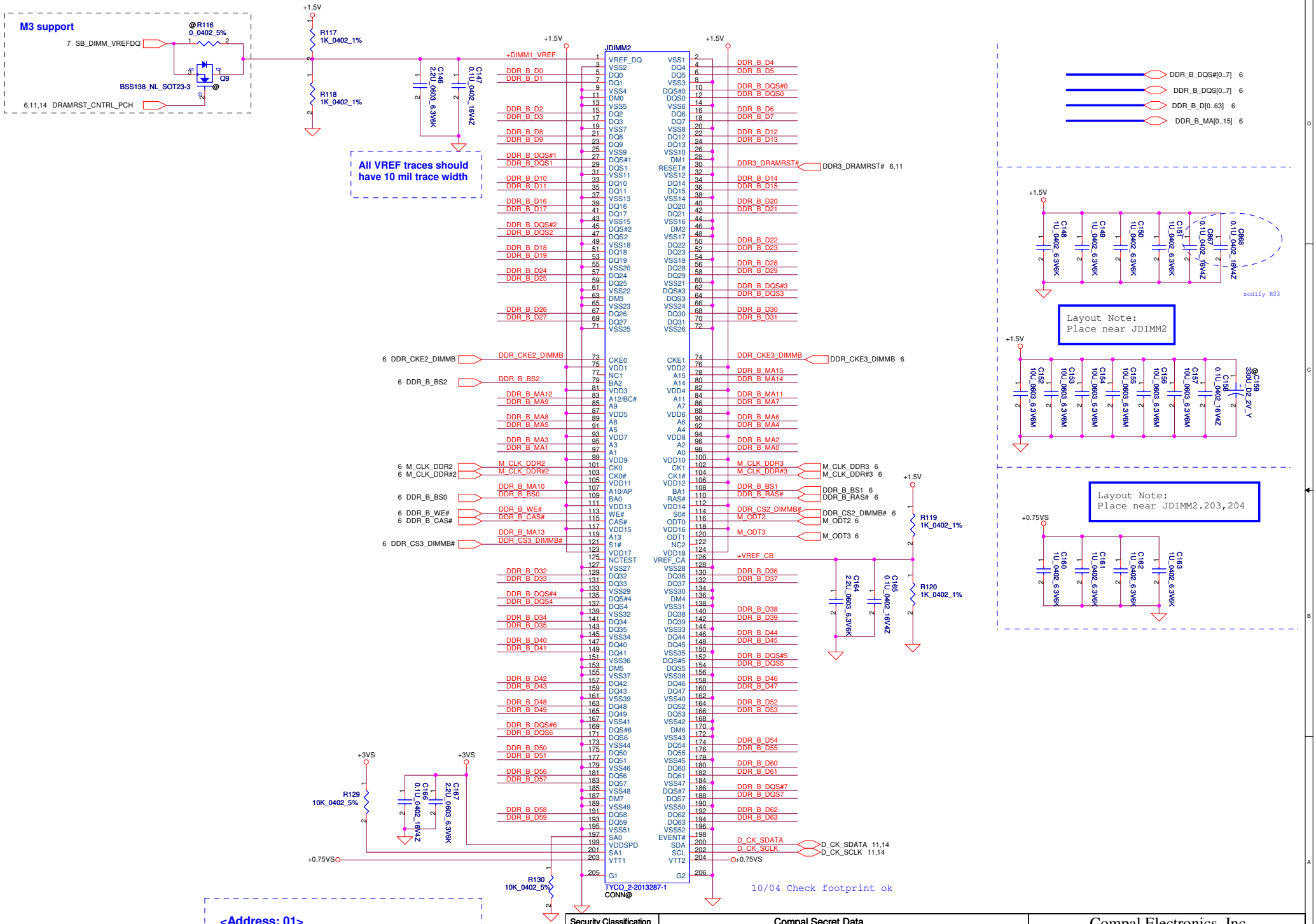

<Address: 01>

DIMM_B Reverse type H:4mm

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Compal Electronics, Inc.

Title: DDRIII DIMMB

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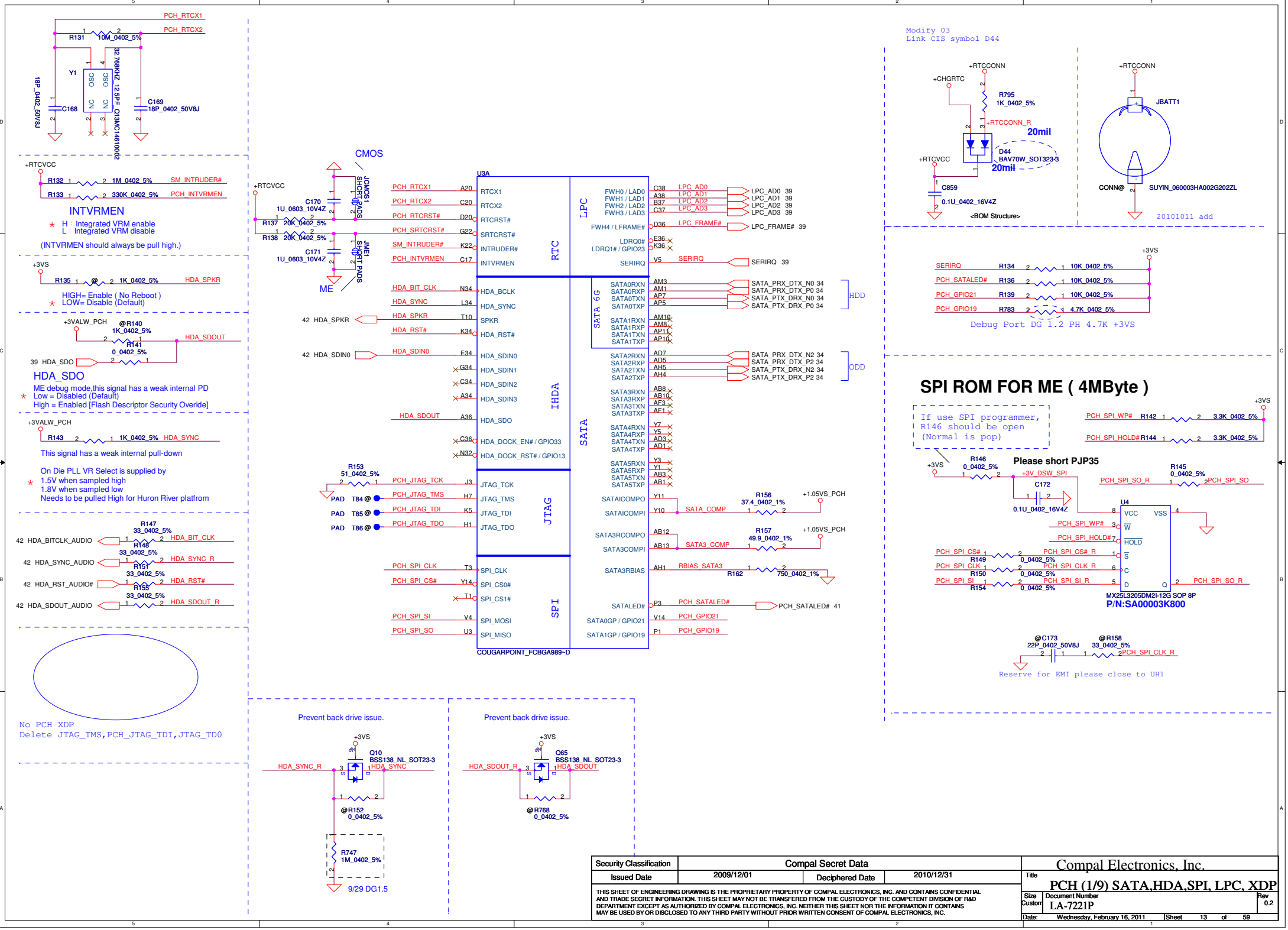

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Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

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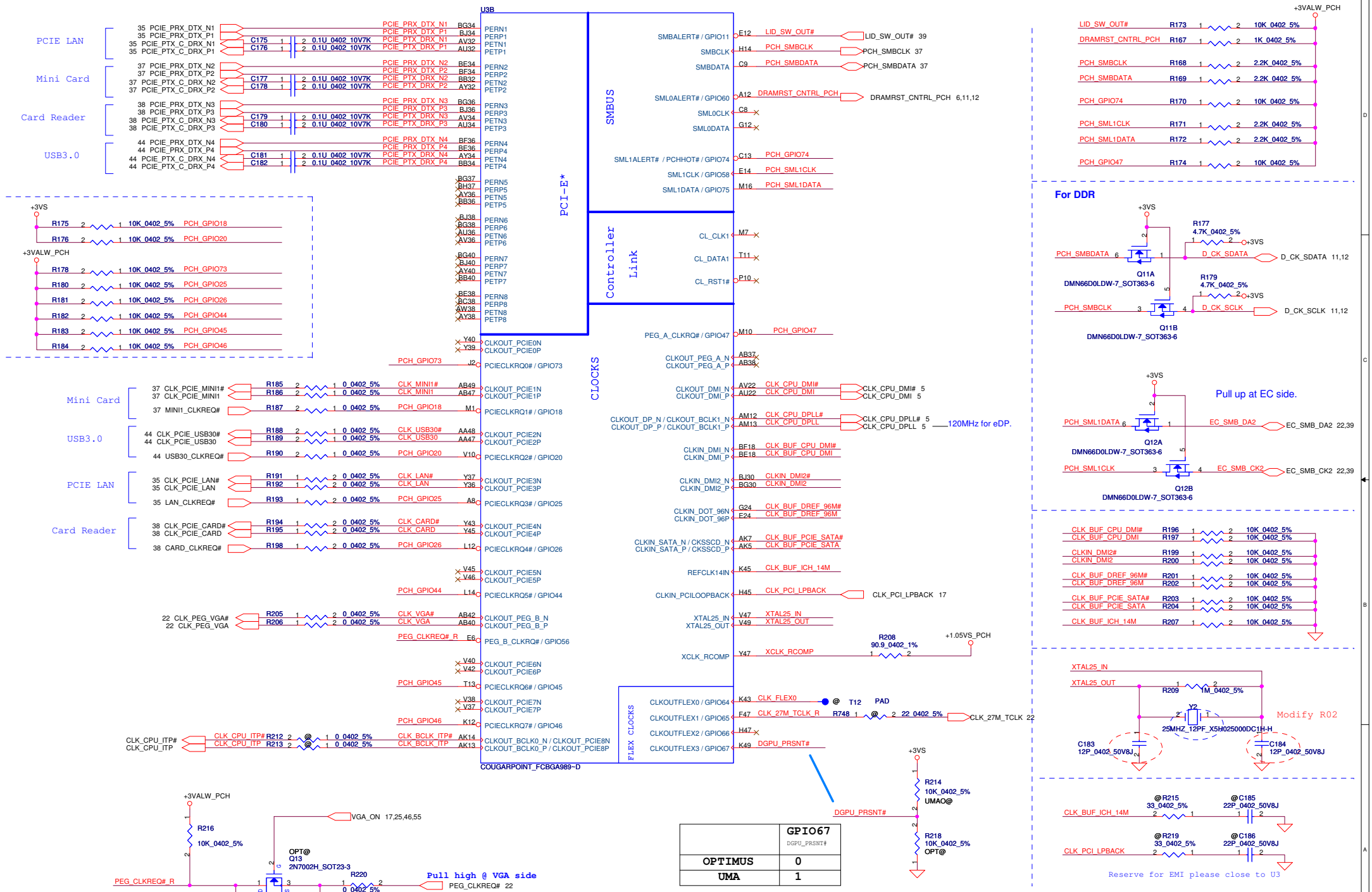

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Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

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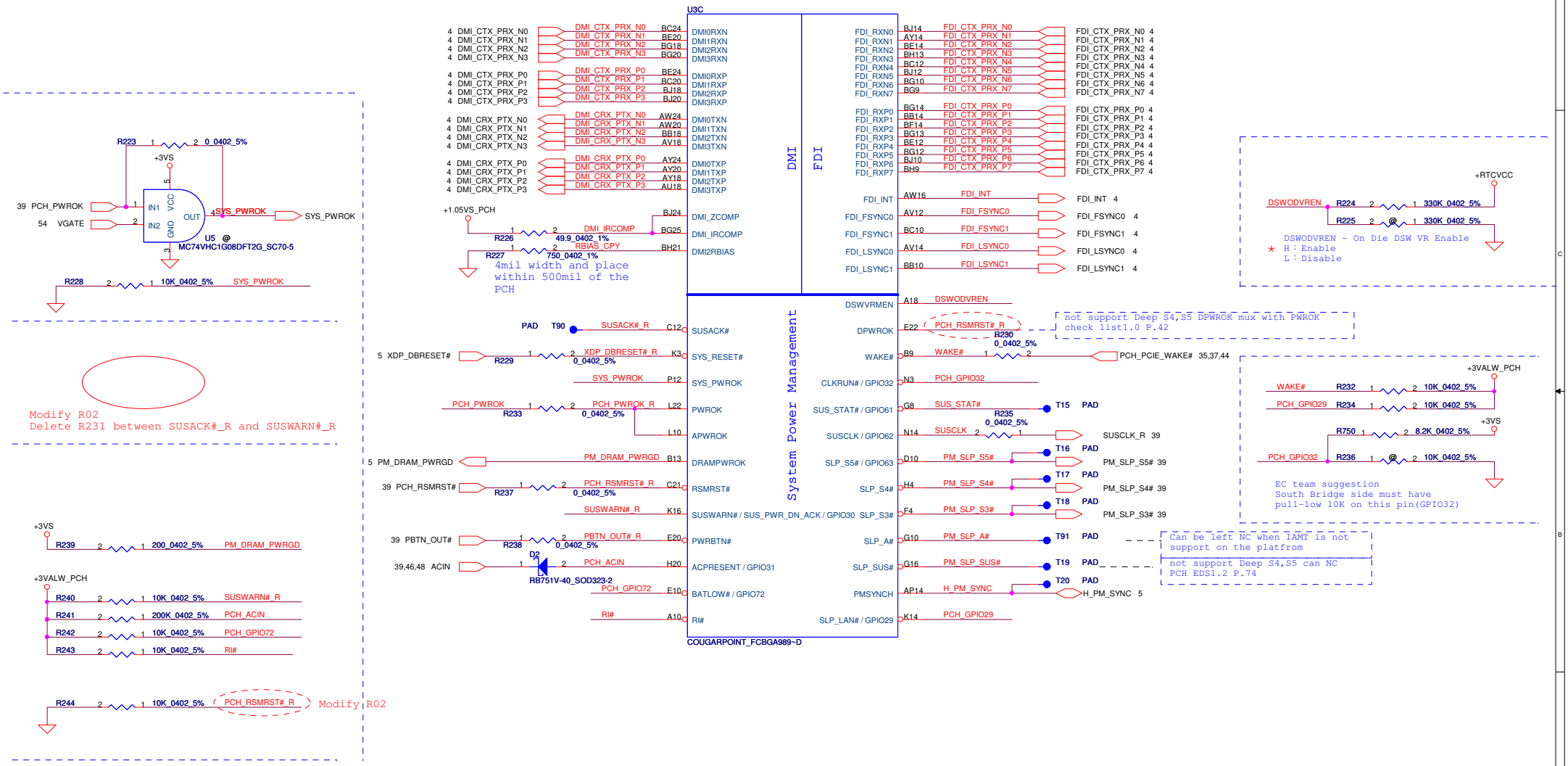

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Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

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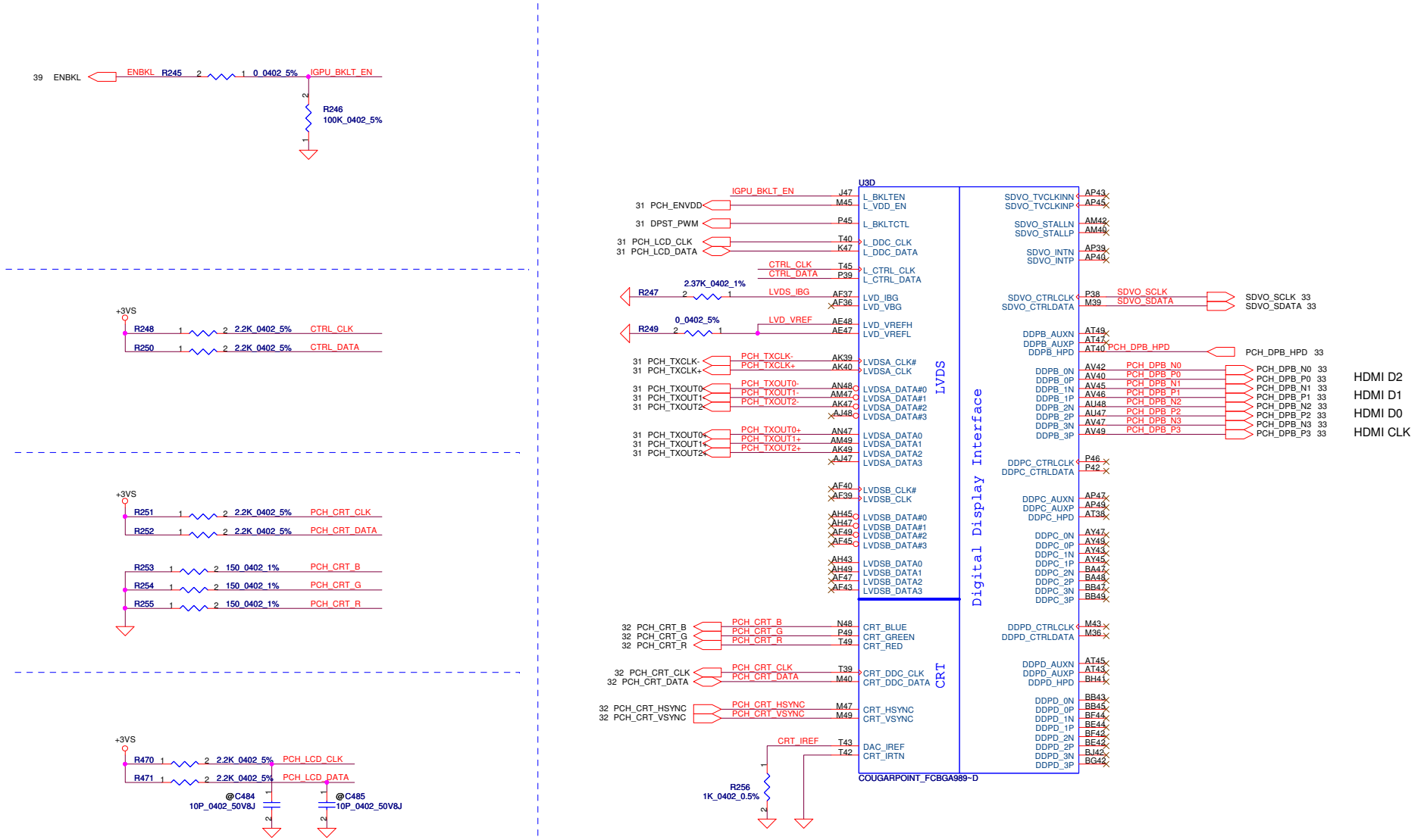

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Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

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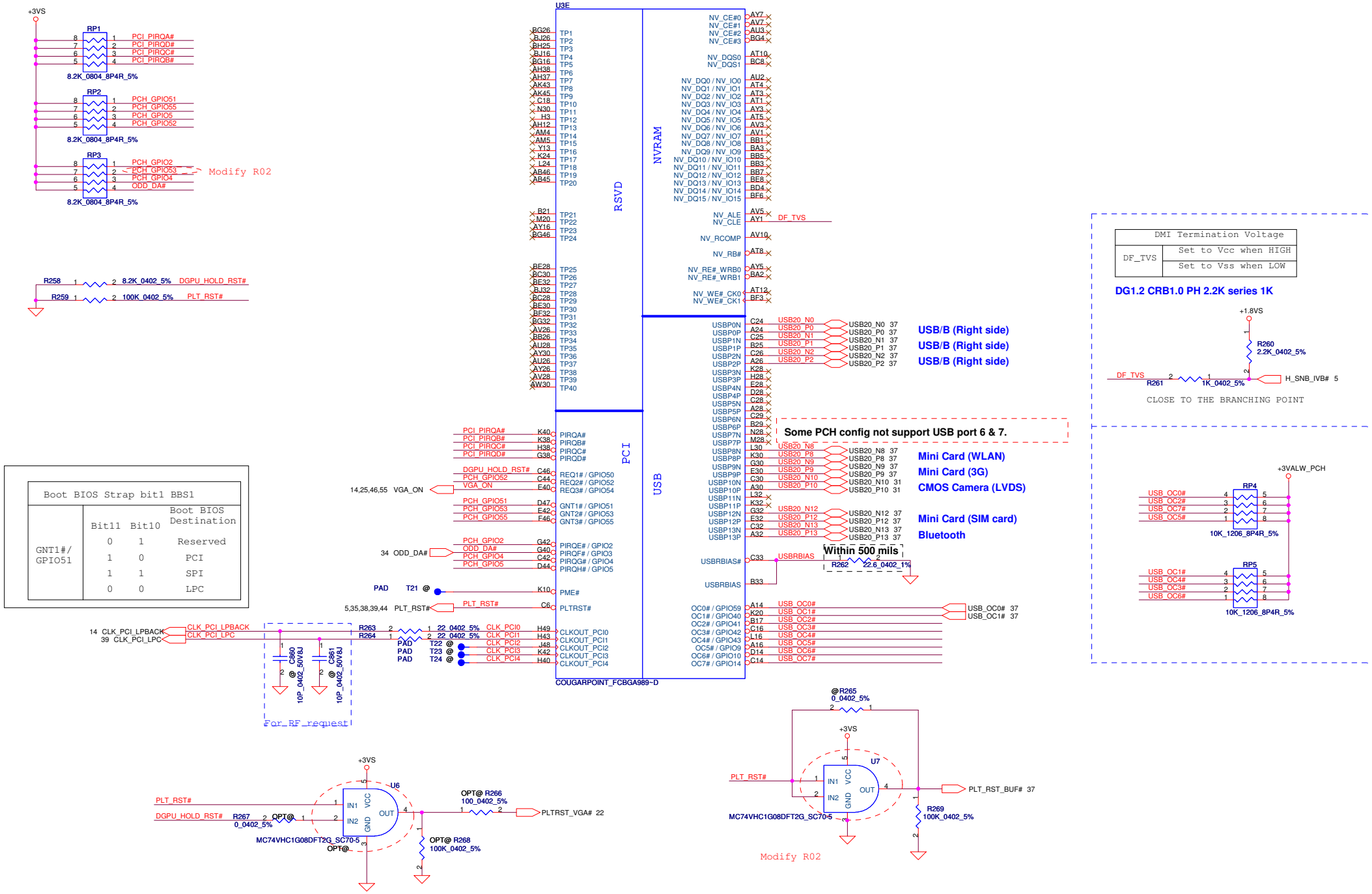

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Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: LA-7221P | Rev: 0.2

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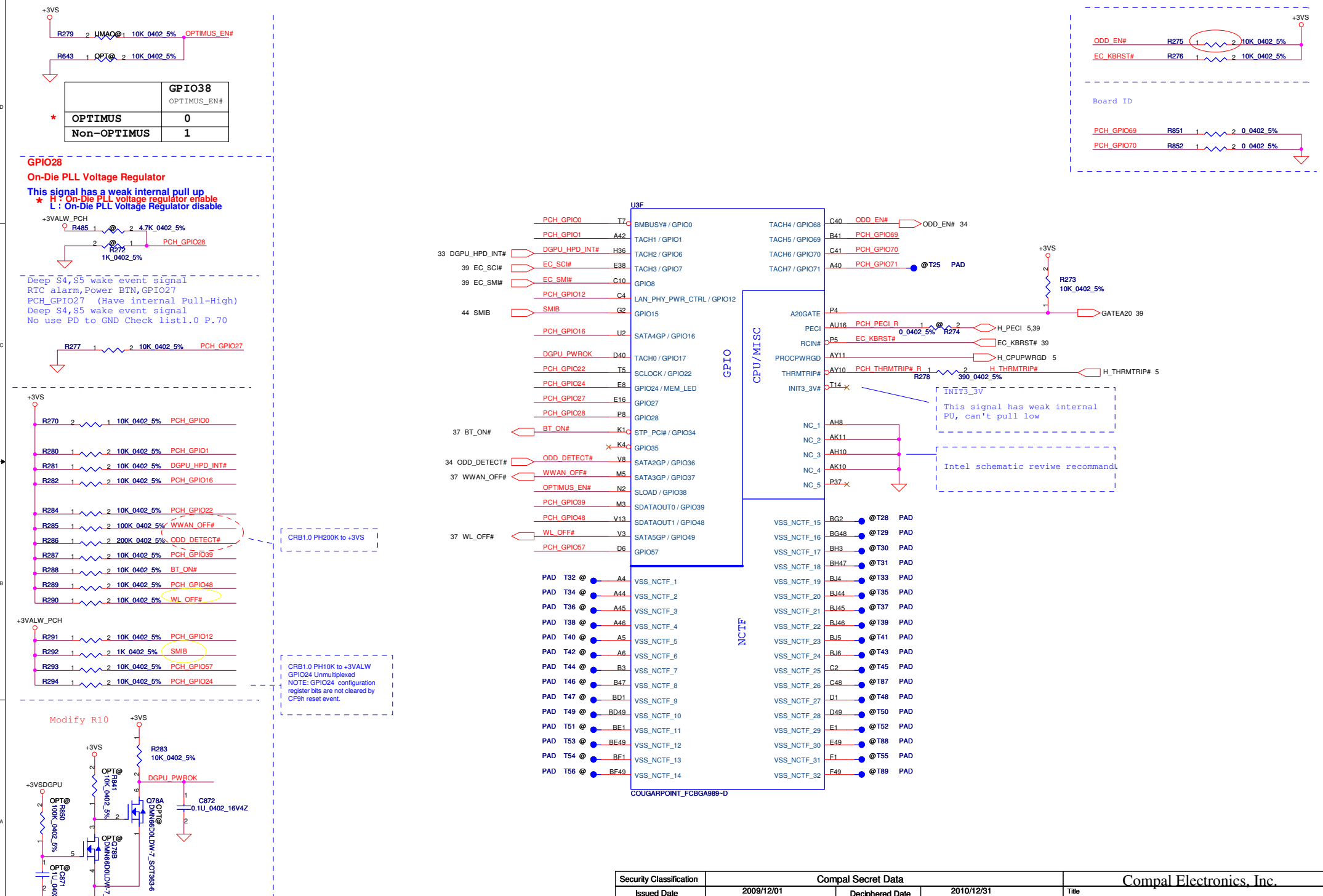

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Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

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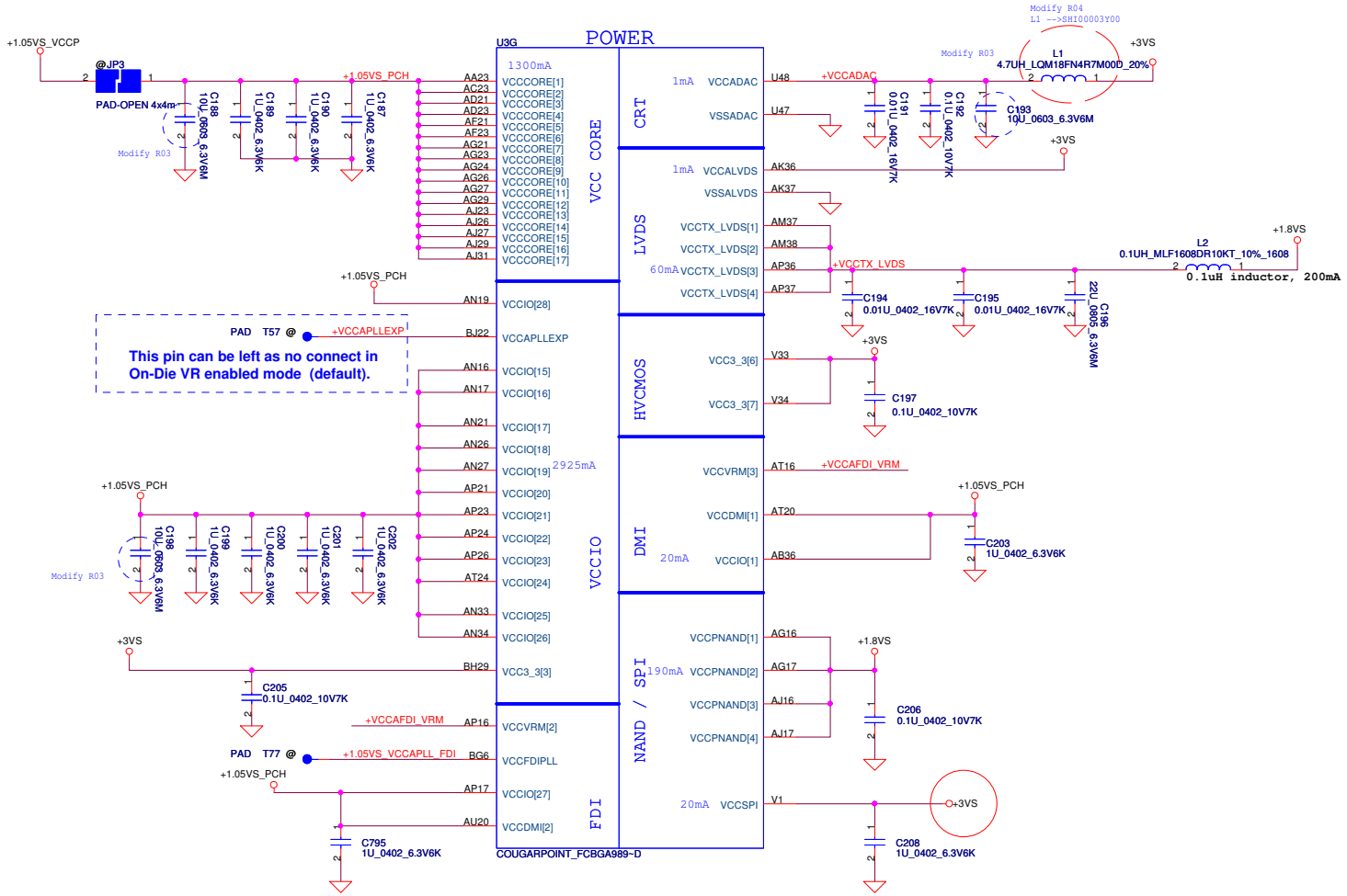

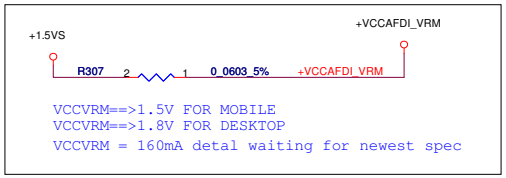

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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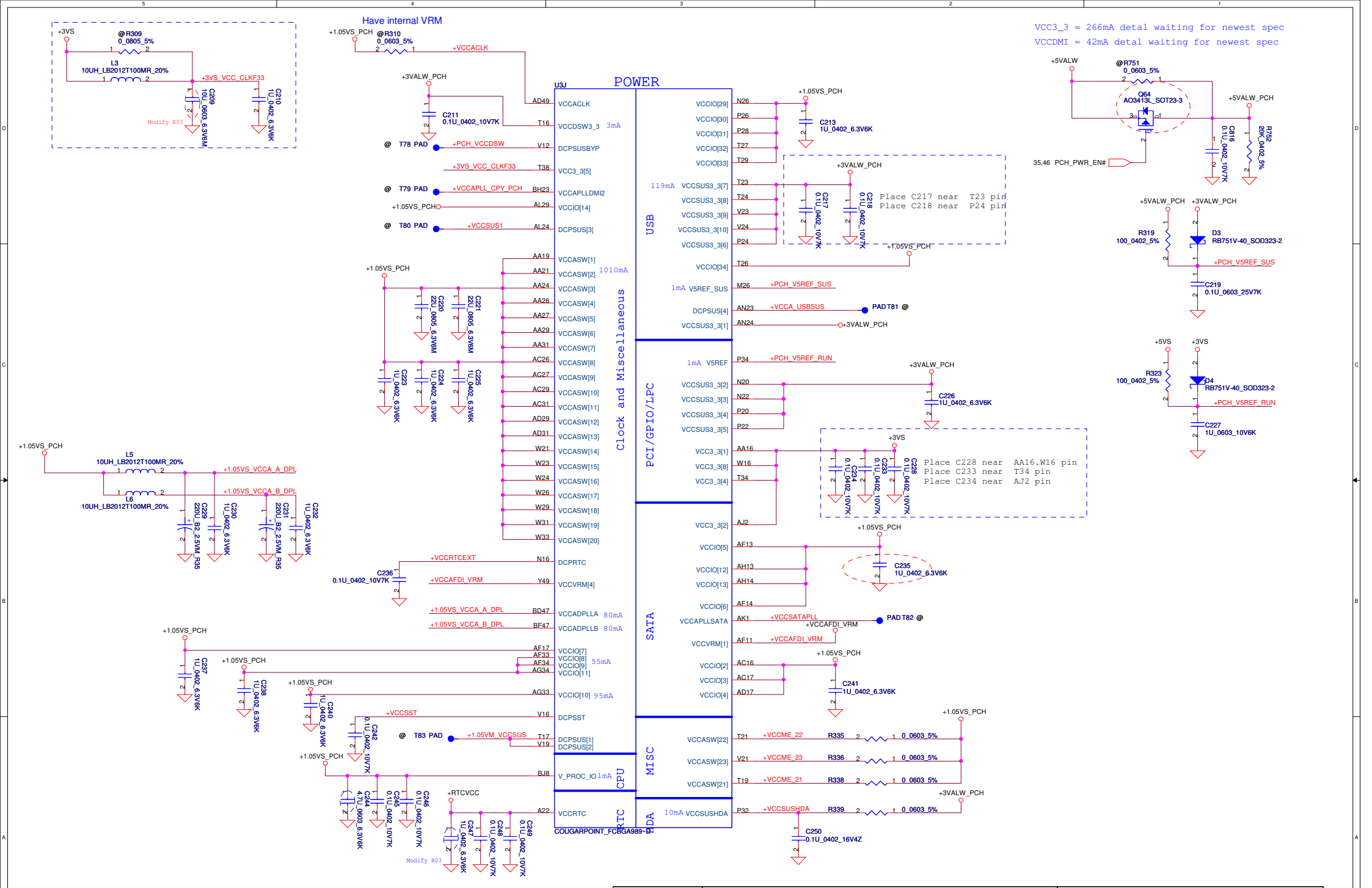

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Compal Electronics, Inc.

Title: PCH (8/9) PWR

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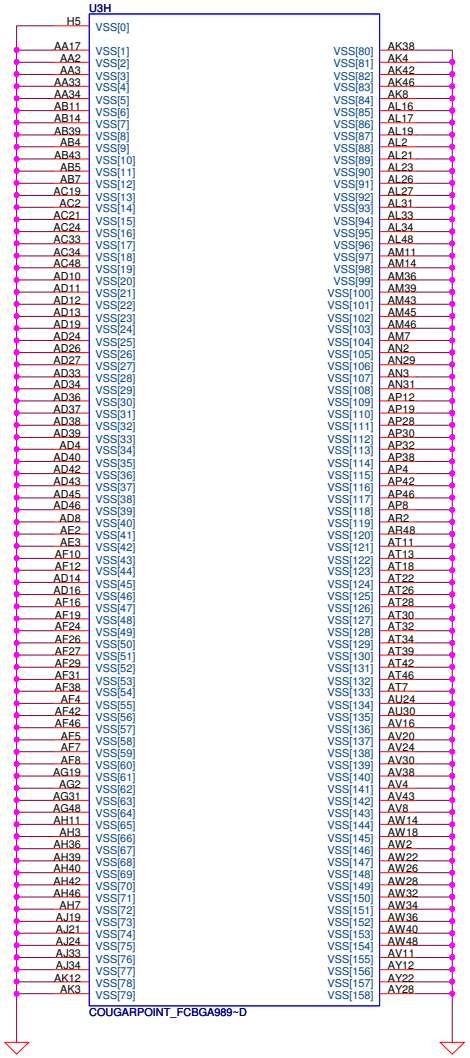

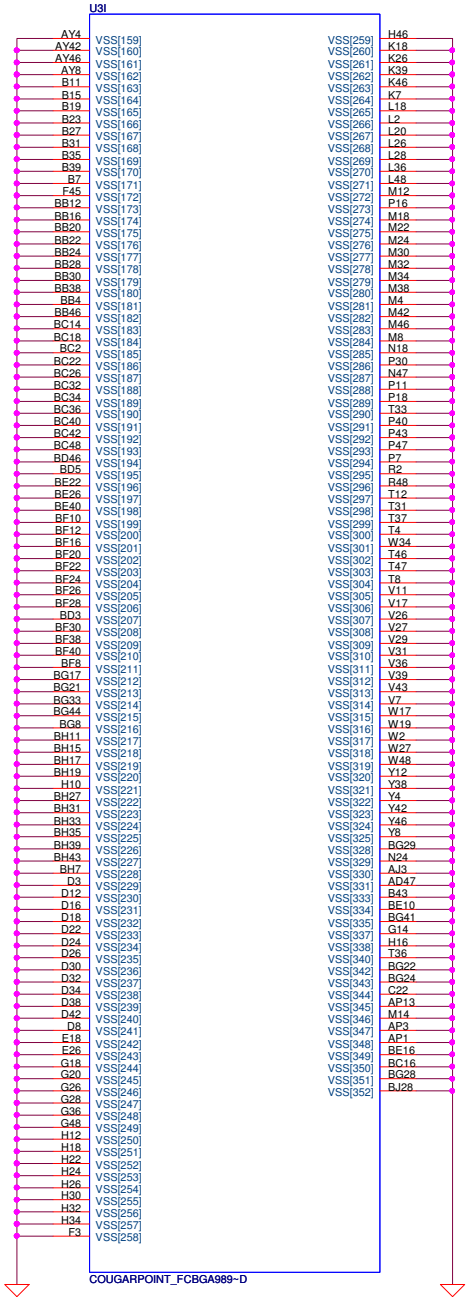

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Issued Date	2009/12/01	Deciphered Date	2010/12/31	Title: PCH (9/9) VSS
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				Date: Wednesday, February 16, 2011; Sheet 21 of 59

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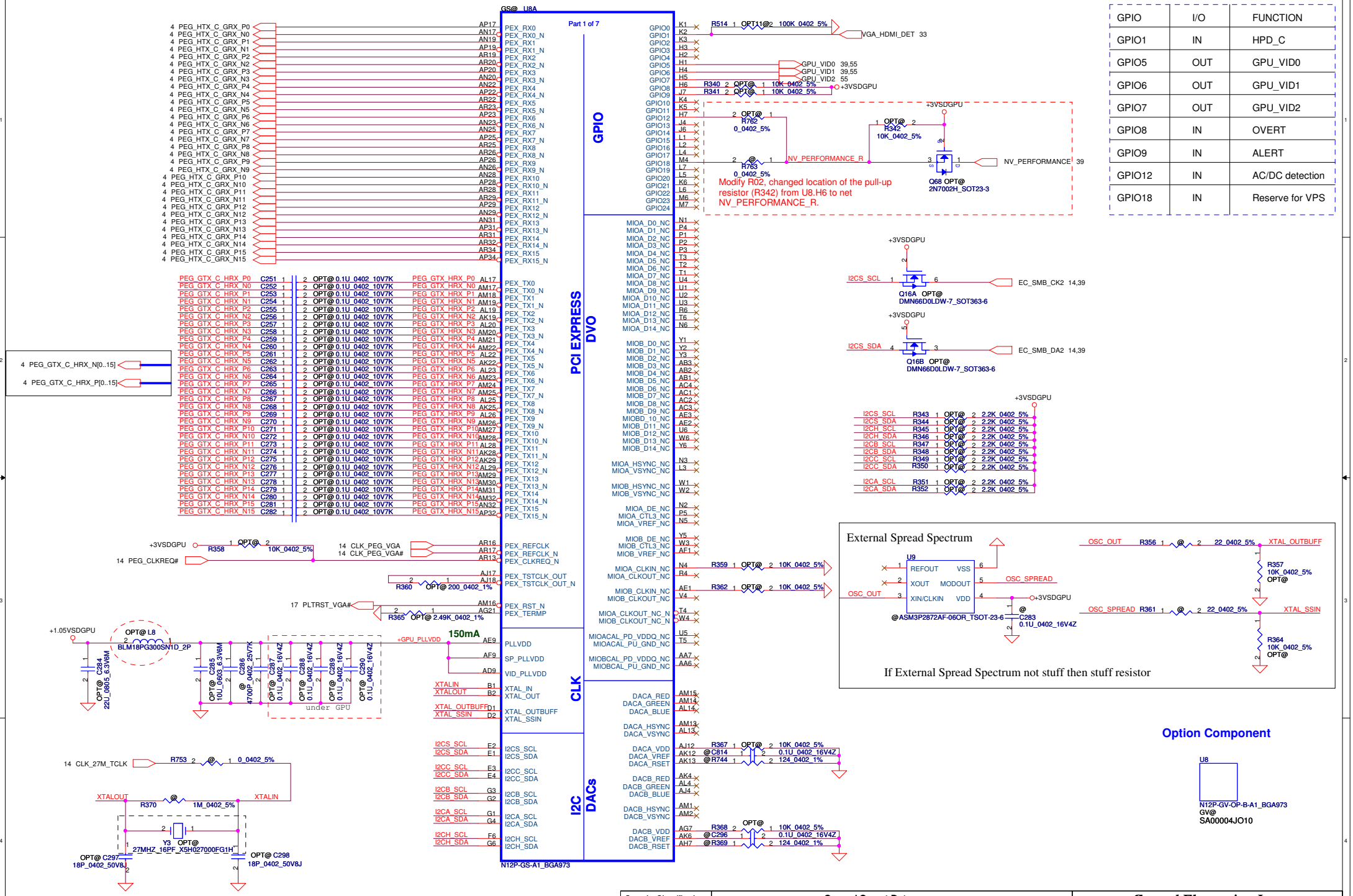

GPIO	I/O	FUNCTION
GPIO1	IN	HPD_C
GPIO5	OUT	GPU_VID0
GPIO6	OUT	GPU_VID1
GPIO7	OUT	GPU_VID2
GPIO8	IN	OVERT
GPIO9	IN	ALERT
GPIO12	IN	AC/DC detection
GPIO18	IN	Reserve for VPS

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Compal Electronics, Inc.

Title: N12P PEG 1/9

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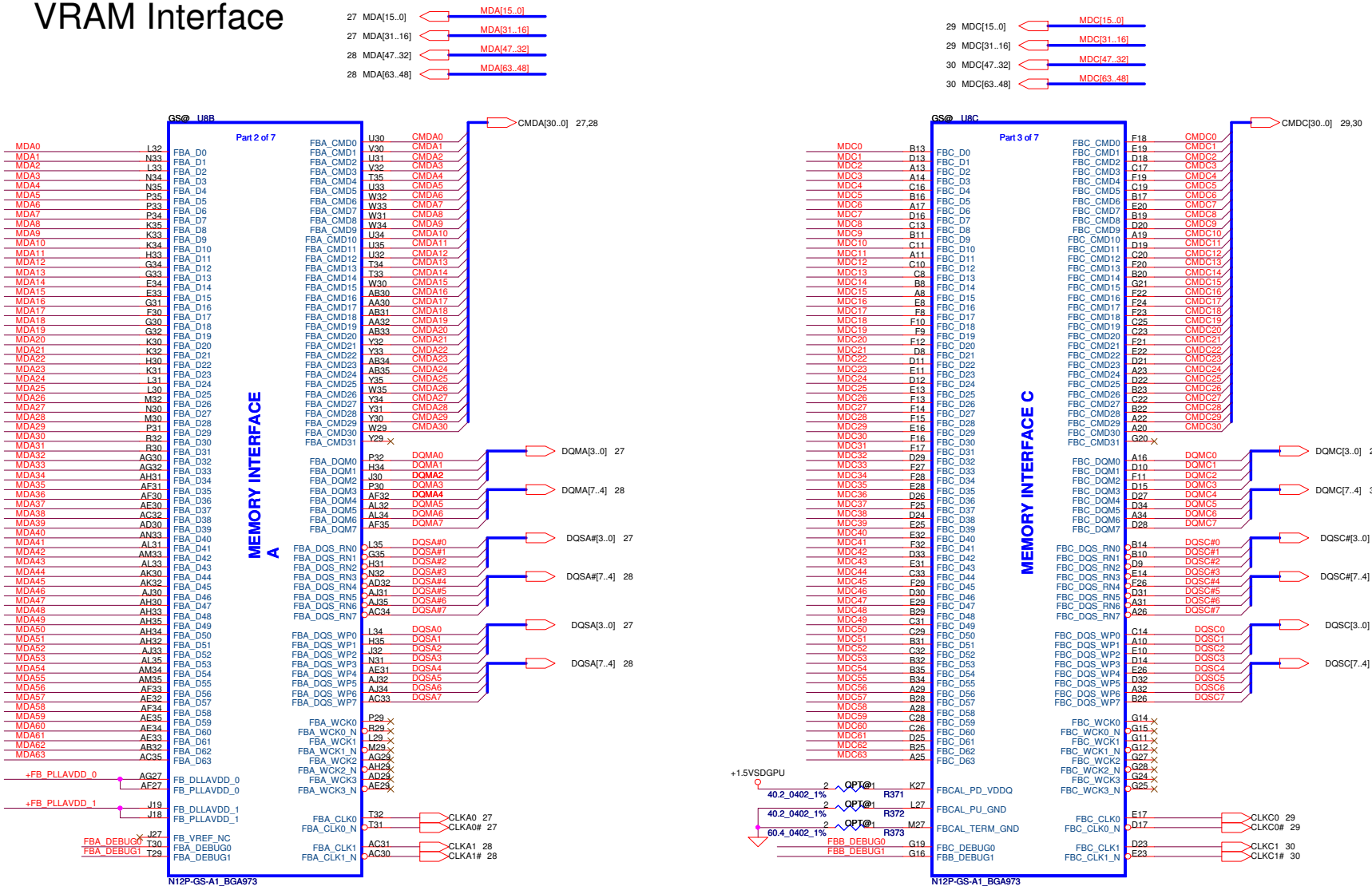
VRAM Interface



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Title: N12P VRAM 2/9

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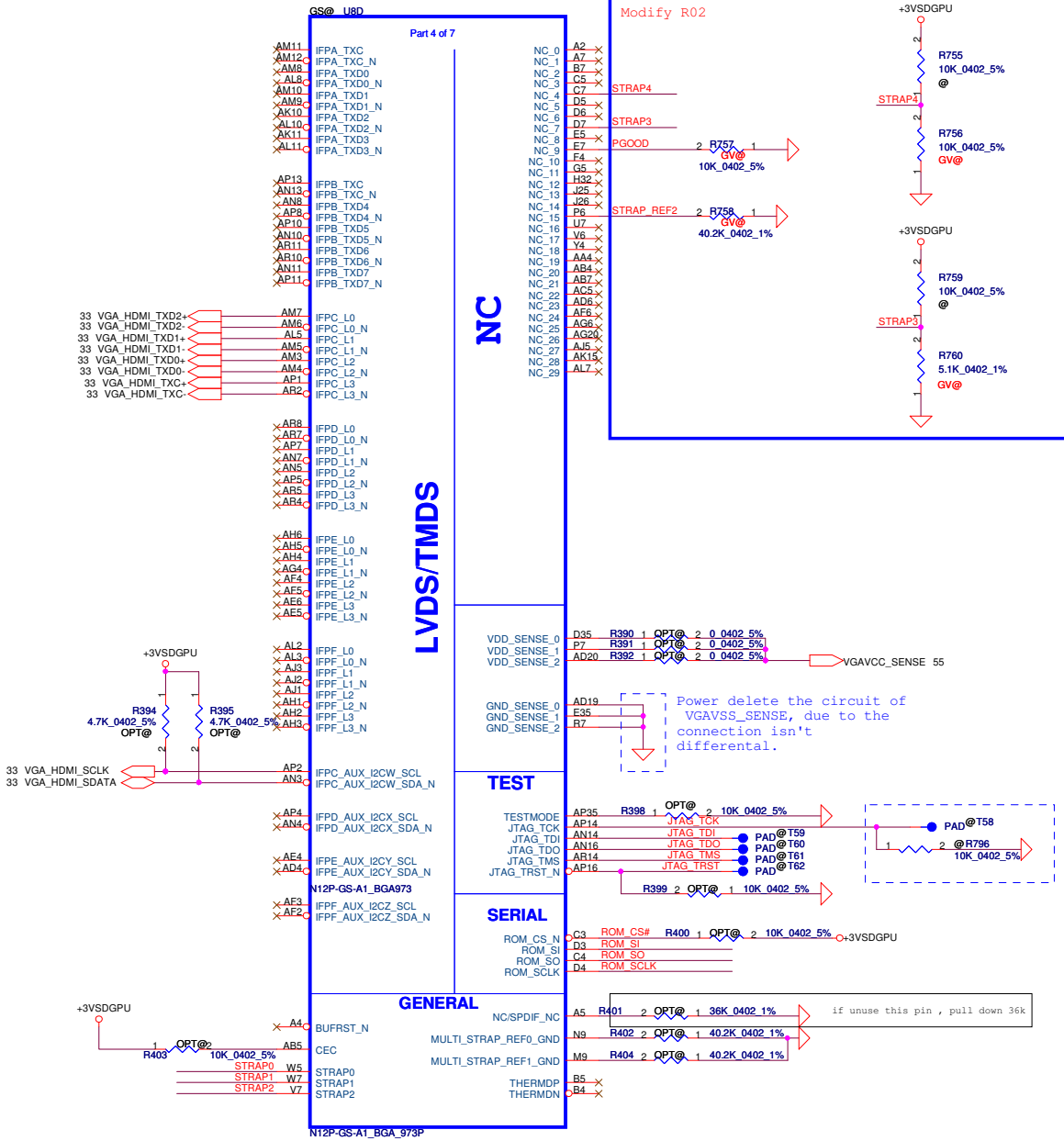
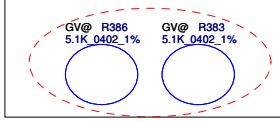
11/8, For GB2-128(GS) & GB2b-128(GV) colayout.
the circuit isfor GB2b-128(GV-B) package.

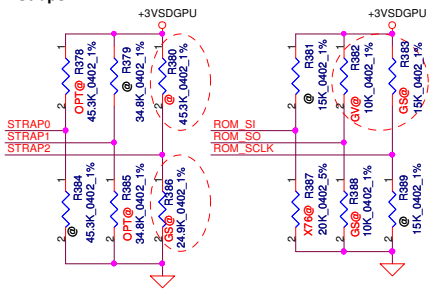


N12P-GV QS DevID: 0x1050, detail additional strap setting, please refer to N12P-GV DG and PUN-05515-001_v03

1. ROM_SCLK: pull up 5K ohm.
2. STRAP2: pull down 5K ohm.
3. ROM_SO: pull up 10K ohm.
4. STRAP3: pull down 5K ohm.
5. STRAP4: pull down 10K ohm.
6. STRAP_REF2, need to stuff with 40K ohm 1%.
7. PGOOD (pin E7) stuff 10K ohm.



Straps MULTI LEVEL STRAPS



N11P-GS	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA00004GS10	H 45K	L 35K	L 25k(GS@) L 5k (GV@)	L 20K	H (GV@) L (GS@)	H 15K(GS@) H 5K(GV@)
64MX16 Hynix SA000041S40	H 45K	L 35K	L 25k(GS@) L 5k (GV@)	L 15K	H (GV@) L (GS@)	H 15K(GS@) H 5K(GV@)
128MX16 Samsung SA00003MQ60	H 45K	L 35K	L 25k(GS@)	L 45K	H (GV@) L (GS@)	H 15K(GS@)
128MX16 Hynix SA00003VS10	H 45K	L 35K	L 25k(GS@)	L 35K	H (GV@) L (GS@)	H 15K(GS@)

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GE	0x0DF5	Pull up 15K	Pull down 30K
N12P-GV	0x1050	Pull up 5K	Pull down 5K

Hynix (900MHZ) 64MX16 H5TQ1G63DFR-11C SA000041S40	512MB	0010	PD 15K (SD034150280)
	1GB	0010	PD 15K (SD034150280)
Hynix 2G 128MX16 H5TQ2G63BFR-12C SA00003VS10	2GB	0110	PD 34.8k(SD034348280)
Samsung (900MHZ) 64MX16 K4W1G1646G-BC11 SA00004GS10	512MB	0011	PD 20K (SD028200280)
	1GB	0011	PD 20K (SD028200280)
Samsung 2G 128M16 K4W2G1646C-HC12 SA00003MQ60	2GB	0111	PD 45.3K(SD034453280)

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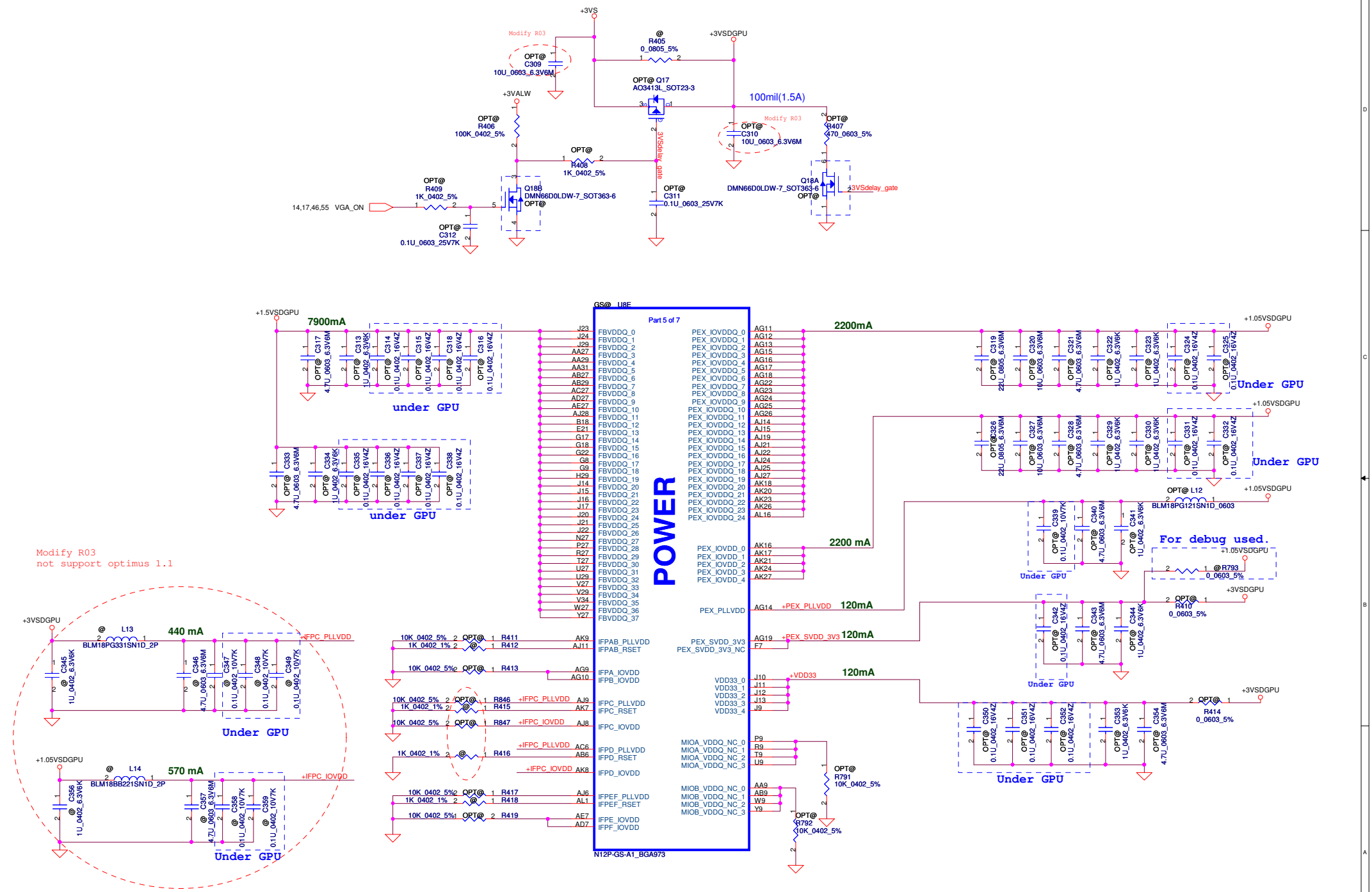

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Title: N12P POWER & GND 4/9

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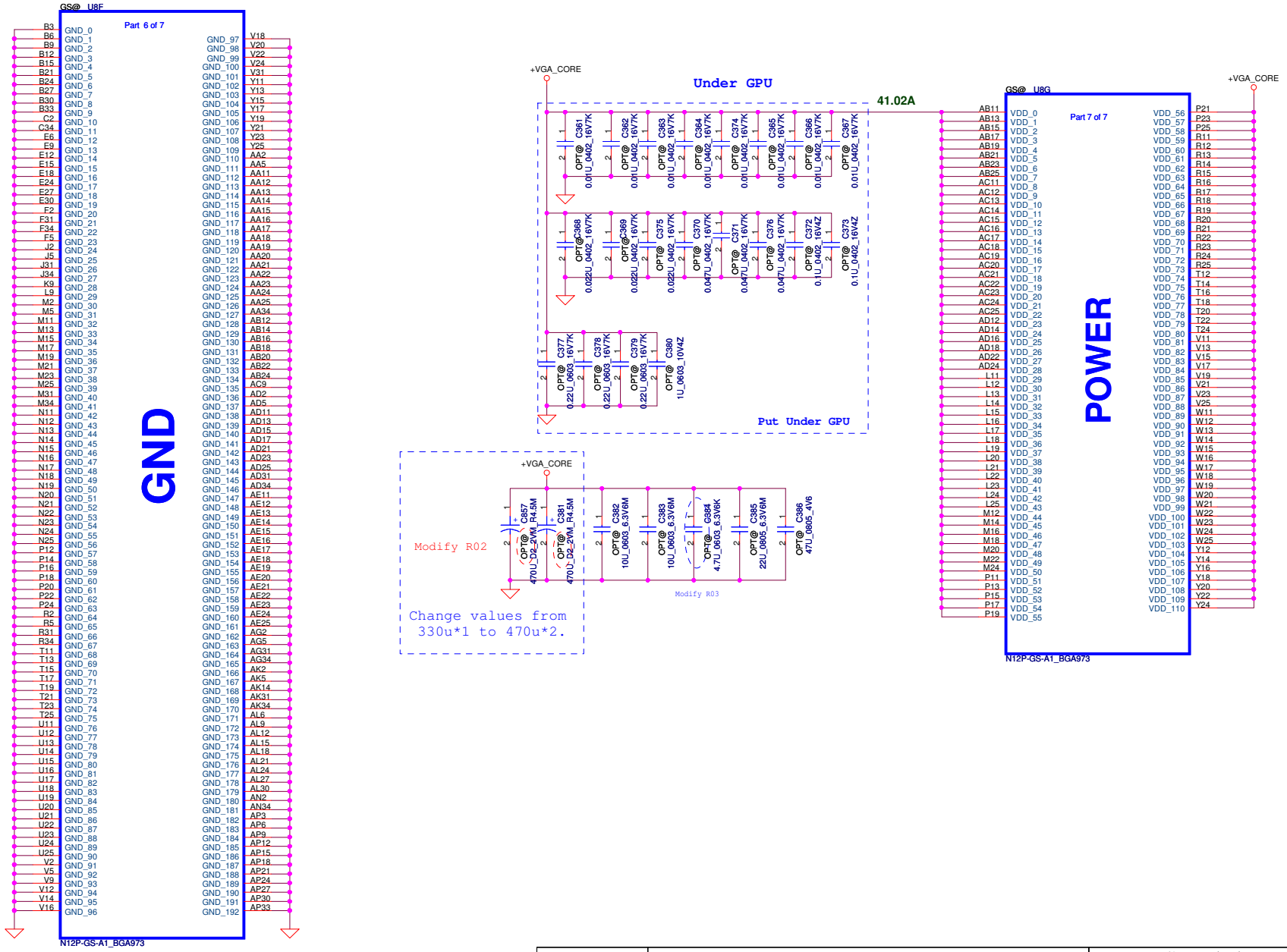

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Title: N12P POWER & GND 5/9

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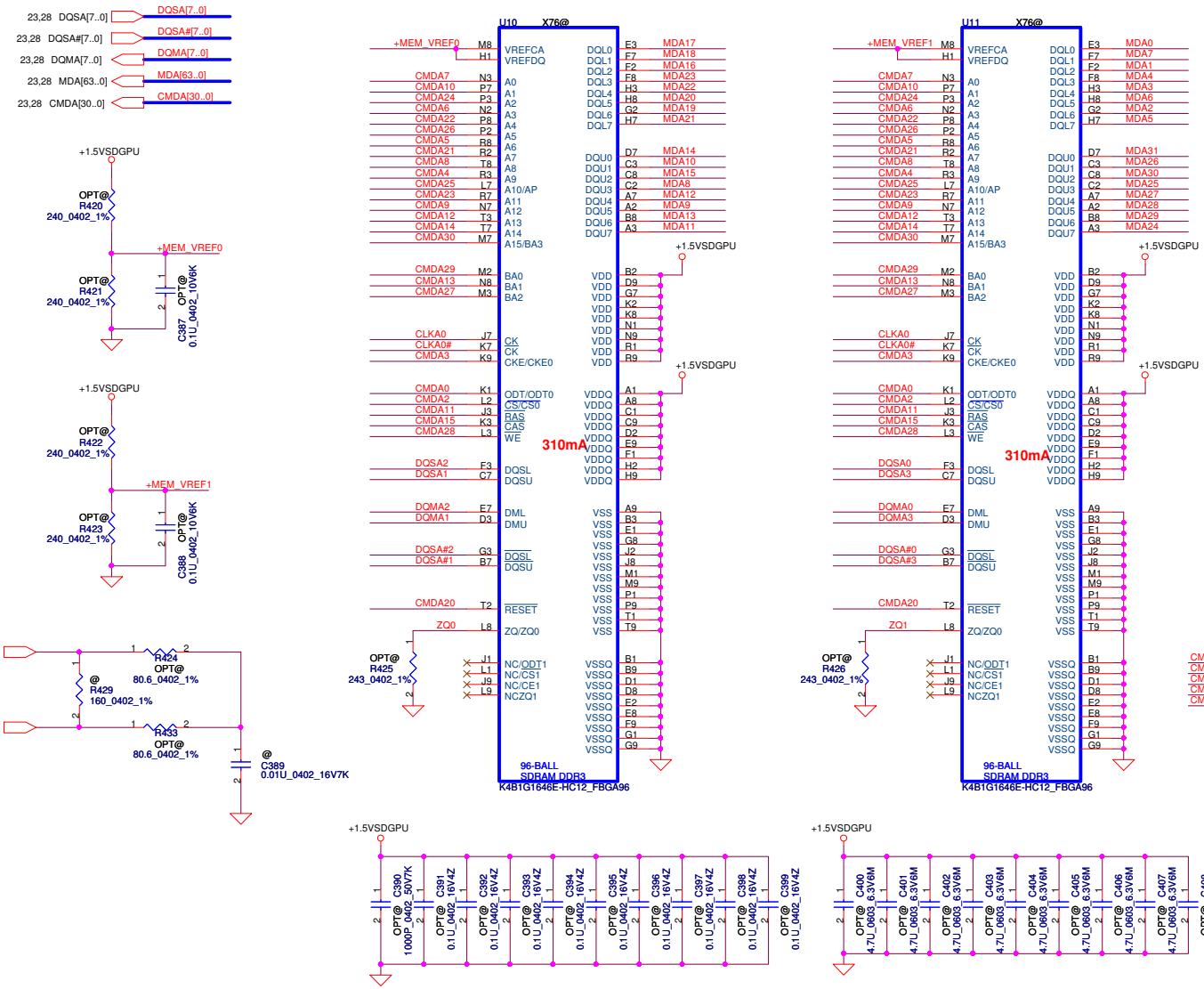
VRAM DDR3 chips (GS=1GB, GV=512M)

128Mx16 DDR3*8==>2GB (GS)
64Mx16 DDR3*8==>1GB (GS)
64Mx8 DDR3*4==>512M
(The 512M DDR3*4 are used at MEMORY INTERFACE A for GV)



**Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

CMDA3	R427	1	OPT@	2	10K_0402_5%
CMDA0	R428	1	OPT@	2	10K_0402_5%
CMDA16	R430	1	OPT@	2	10K_0402_5%
CMDA20	R431	1	OPT@	2	10K_0402_5%
CMDA19	R432	1	OPT@	2	10K_0402_5%

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung :
SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA ABO!)
SA000047Q20 (S IC D3 128M16 K4W2G1646C-HC11 FBGA 96P ABO!)
Hynix :
SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA ABO!)
SA00003YO20 (S IC D3 128M16 H5TQ2G63BFR-11C FBGA ABO!)

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Issued Date	2009/11/23	Deciphered Date 2010/11/23	Title N21P DDR3 6/9
			Size Custom / Document Number LA-7221P / Rev 0.2
			Date: Wednesday, February 16, 2011 / Sheet 27 of 59

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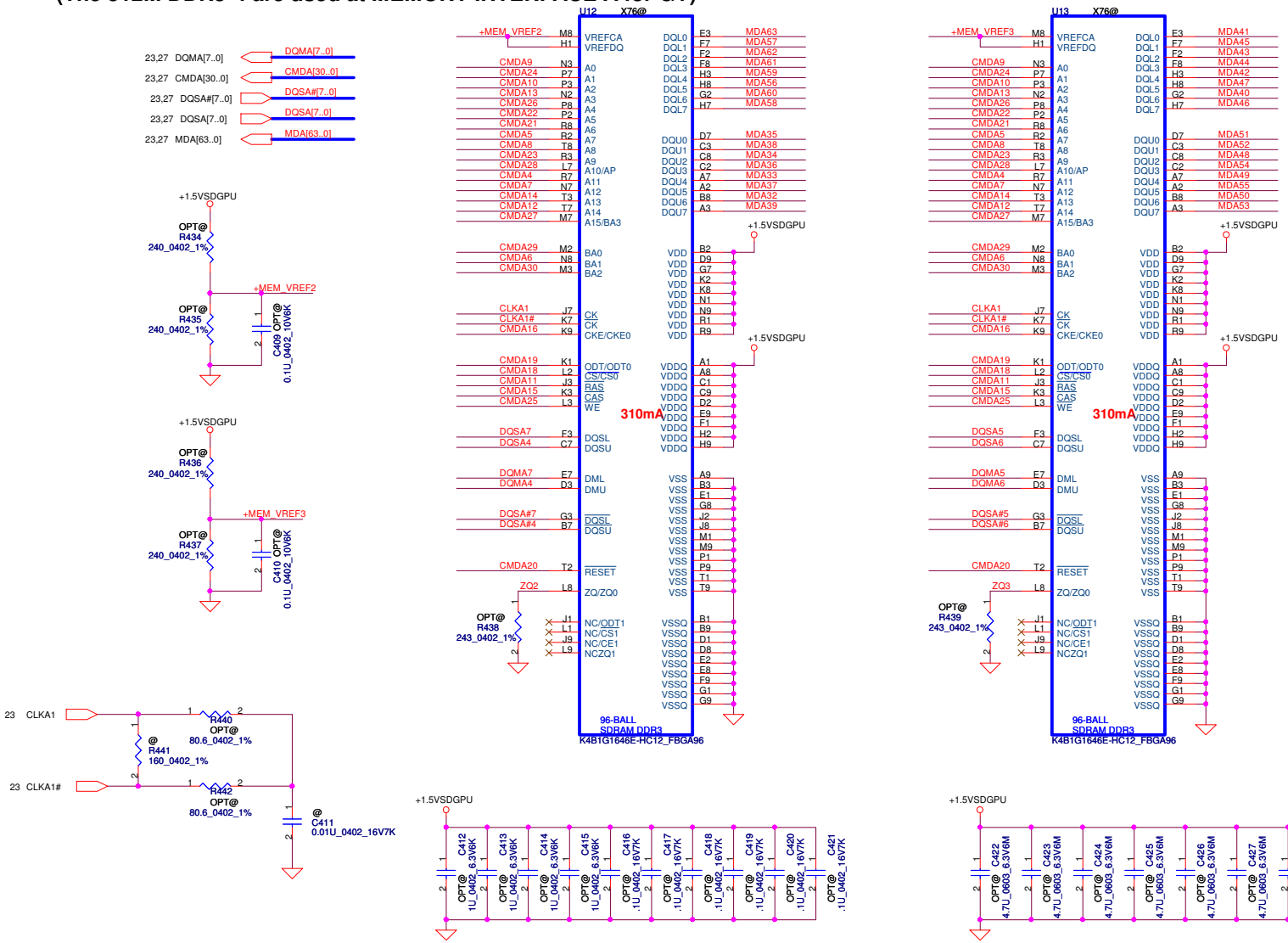
VRAM DDR3 chips (GS=1GB, GV=512M)

128Mx16 DDR3*8==>2GB (GS)
64Mx16 DDR3*8==>1GB (GS)
64Mx8 DDR3*4==>512M
(The 512M DDR3*4 are used at MEMORY INTERFACE A for GV)



Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

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Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

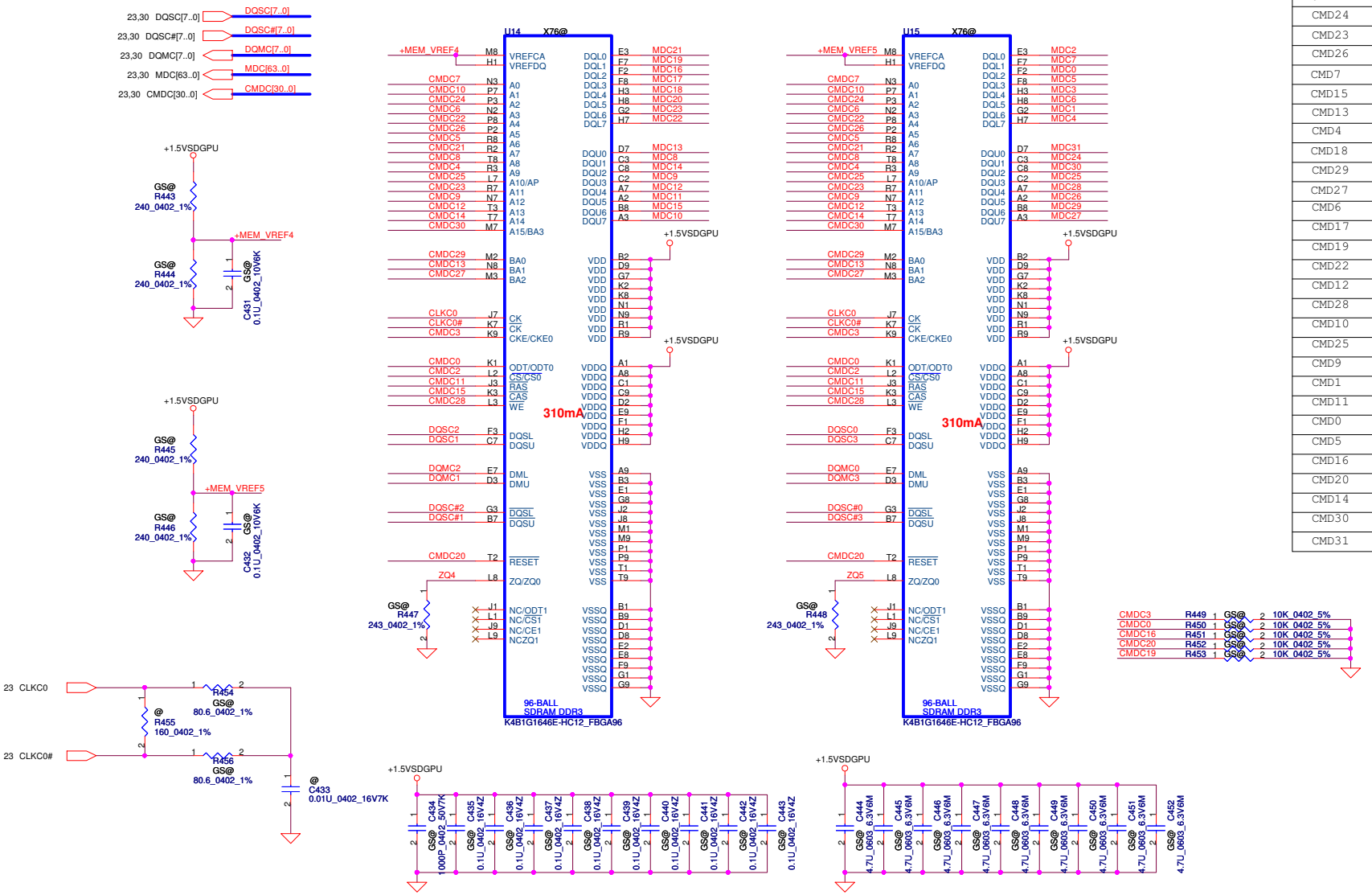
Title: N12P DDR3 7/9

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 28 of 59

VRAM DDR3 chips (GS=1GB, GV=512M)

128Mx16 DDR3*8==>2GB (GS)
64Mx16 DDR3*8==>1GB (GS)

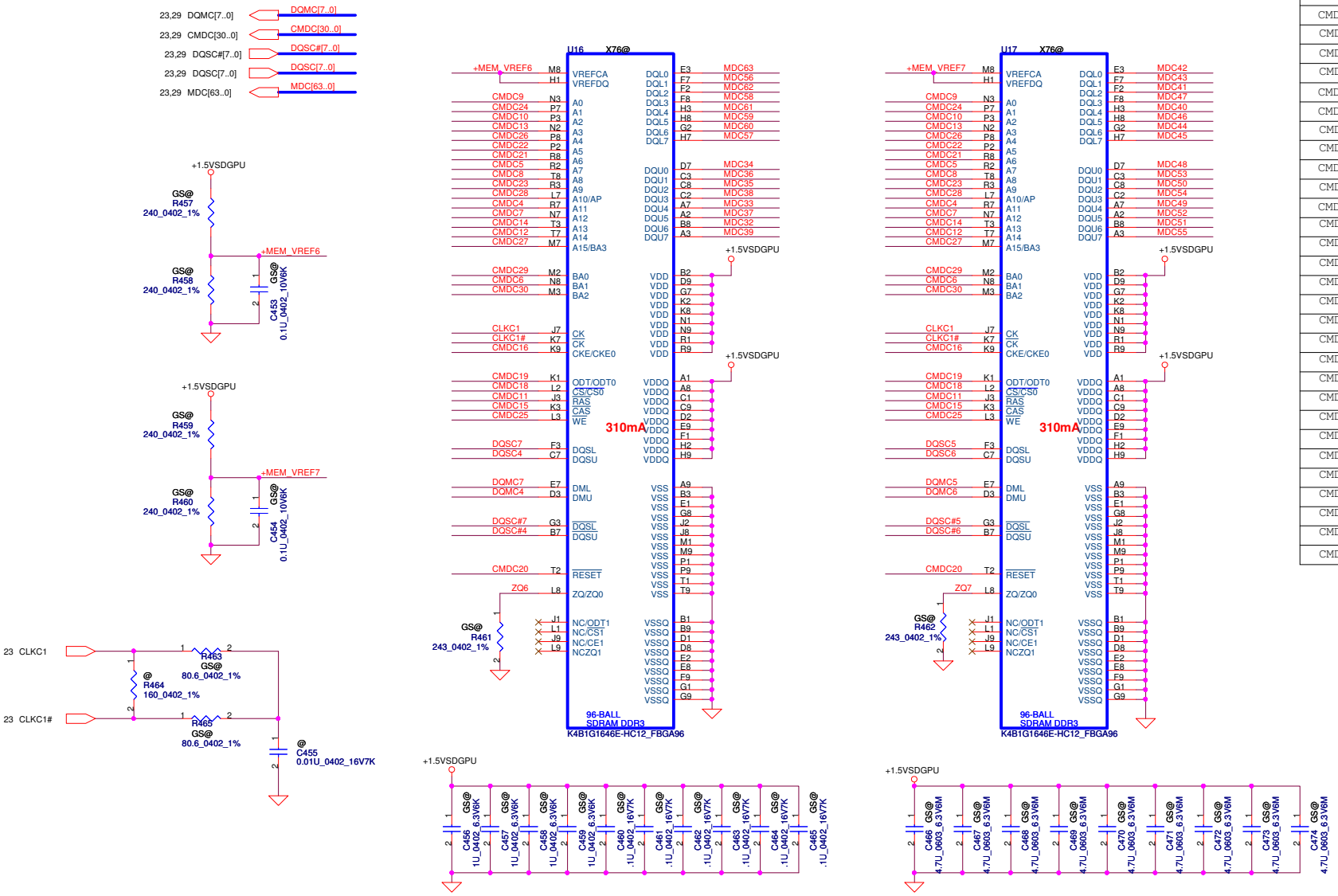


Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

VRAM DDR3 chips (GS=1GB, GV=512M)

128Mx16 DDR3*8==>2GB (GS)
64Mx16 DDR3*8==>1GB (GS)



Mode E Address	Mode C Address	0..31	32..63
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CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

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Security Classification	Compal Secret Data		
Issued Date	2009/11/23	Deciphered Date	2010/11/23

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Compal Electronics, Inc.

Title: N12P DDR3 9/9

Size: Custom | Document Number: LA-7221P | Rev: 0.2

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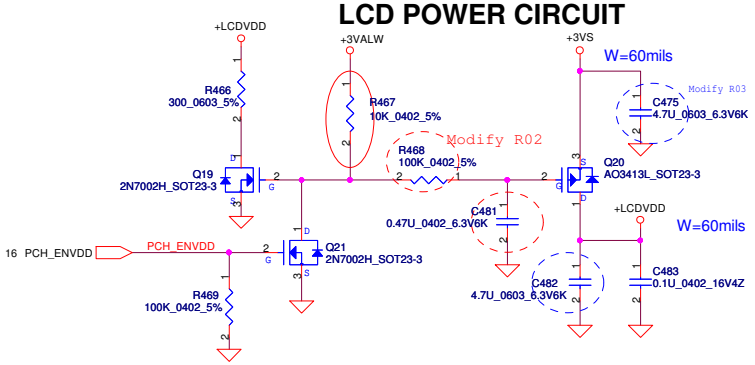
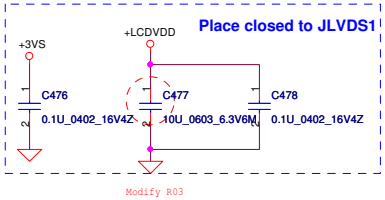
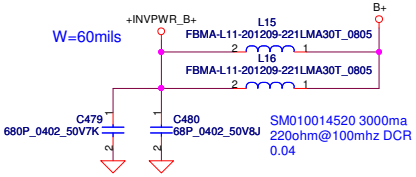
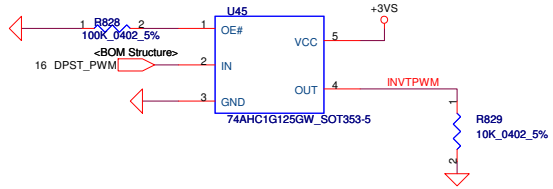
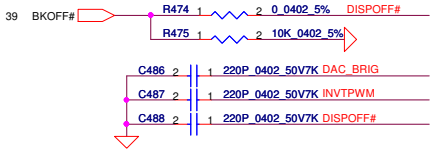
LCD POWER CIRCUIT



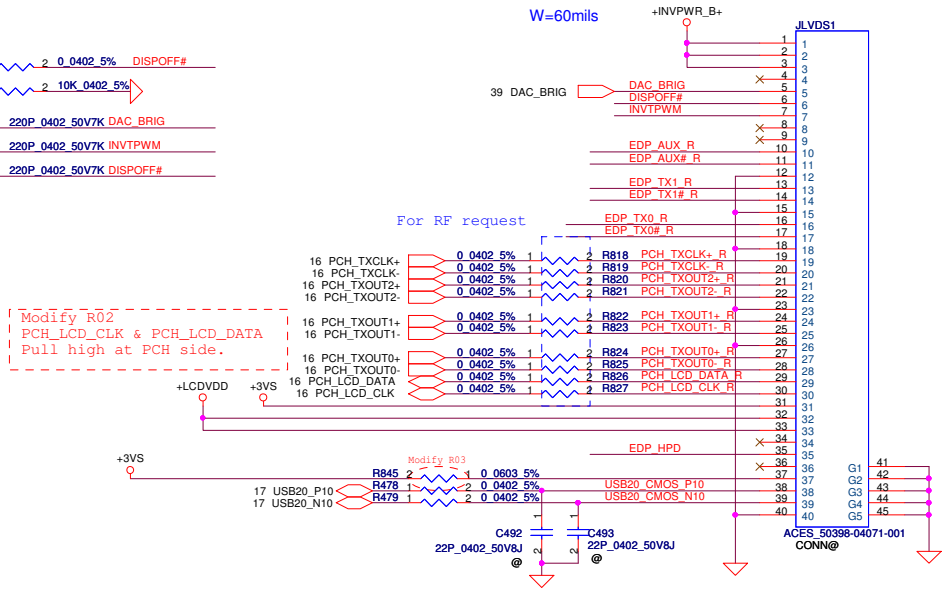






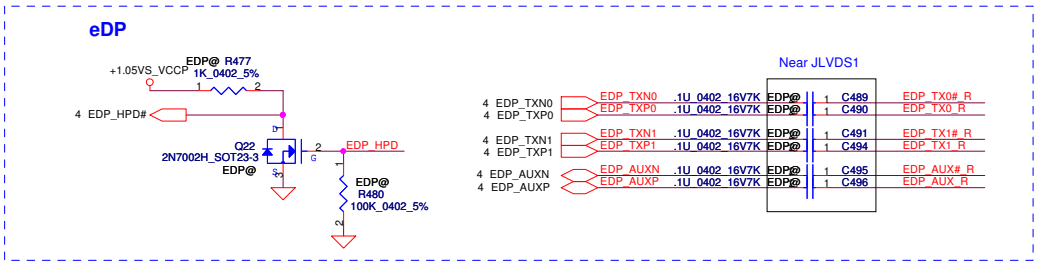


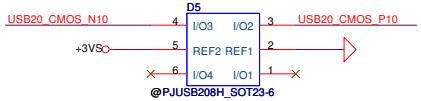
LCD/LED PANEL Conn.



10/01 Check footprint OK

eDP





SC300000D00--> EOL
Change to SC300000B10

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Issued Date	2009/08/01	Deciphered Date	2010/08/01

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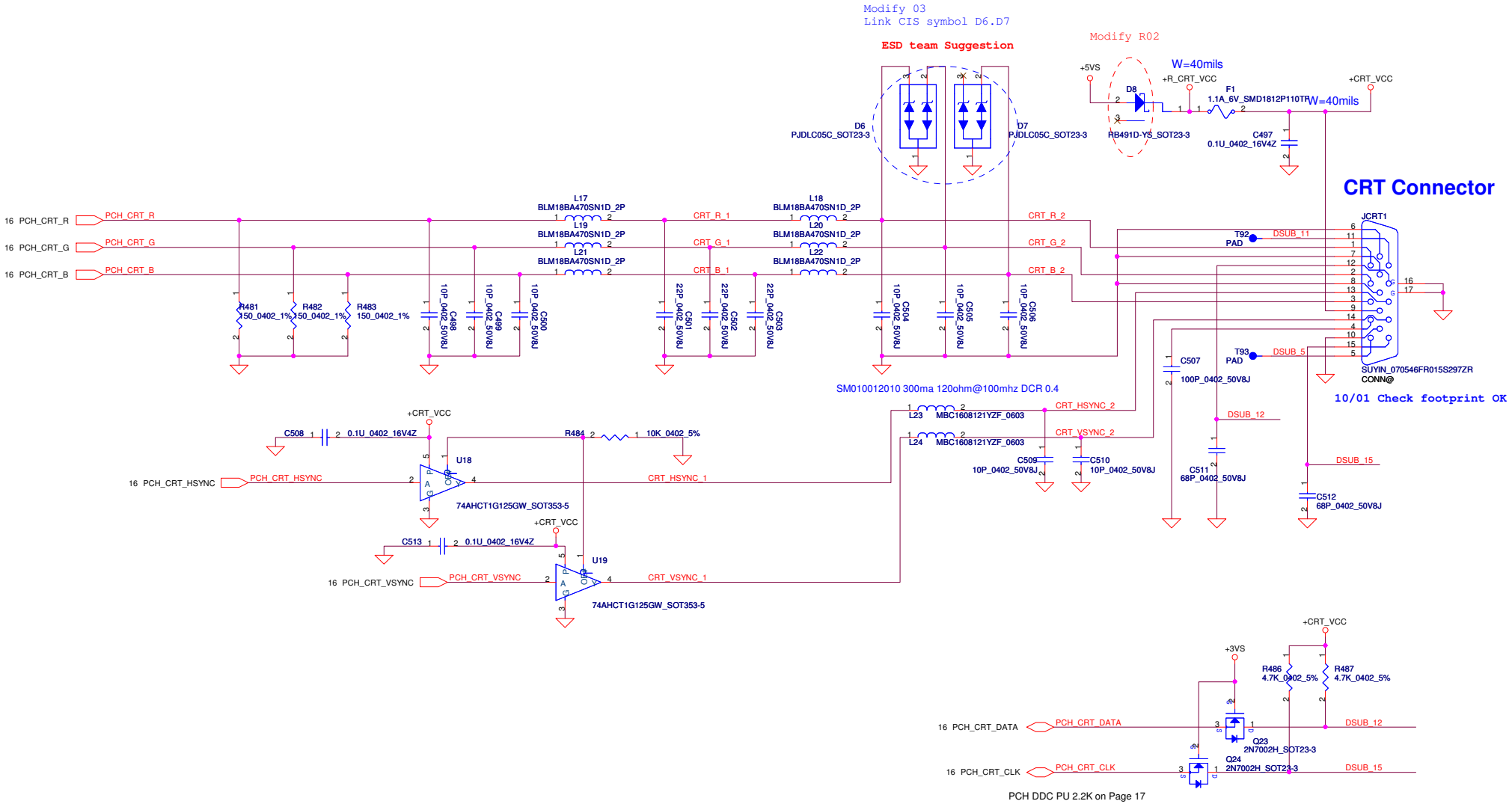
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 31 of 59



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 32 of 59

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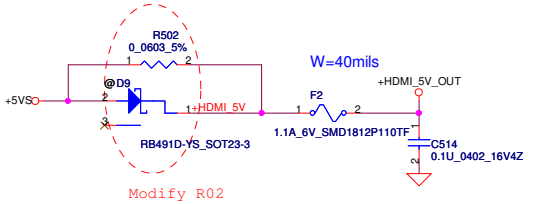
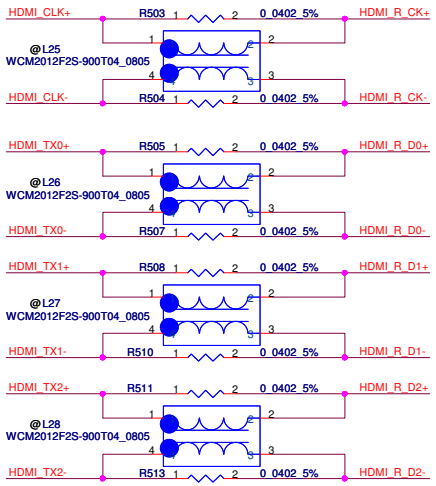
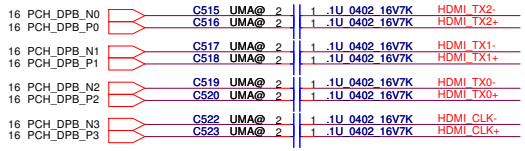


Modify 03
Link CIS symbol L25.L26.L27.L28

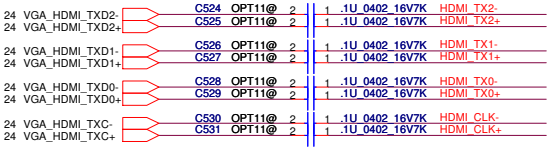
SM070001310 400ma 90ohm@100mhz DCR 0.3



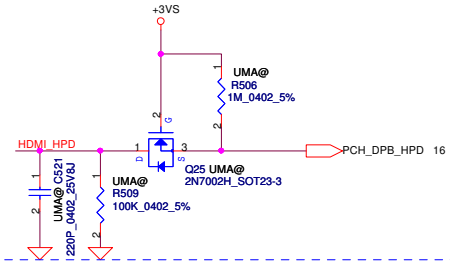
UMA & Optimus 1.0



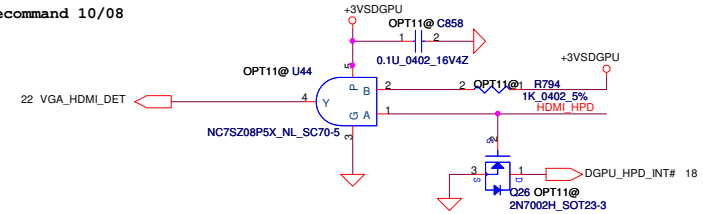
Optimus 1.1

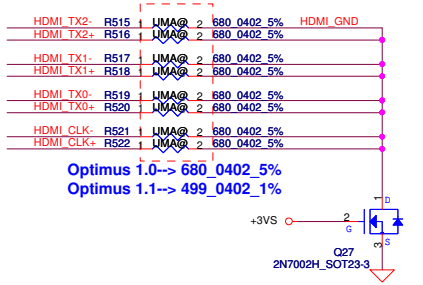


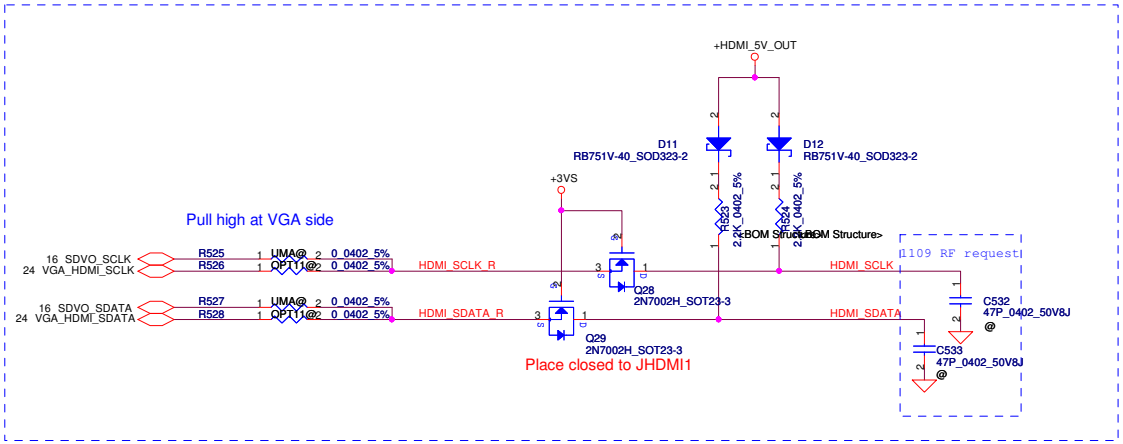
UMA/OPT1.0



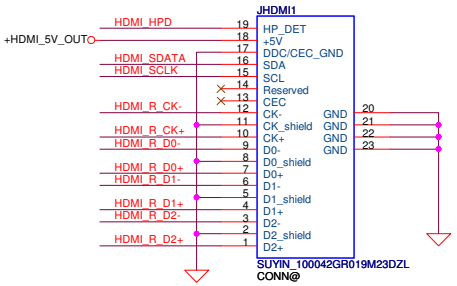
NVIDA Recommand 10/08
OPT1.1





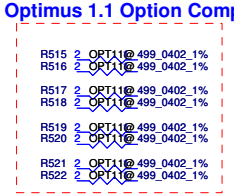


HDMI connector



10/13 Link CIS symbol OK!

Optimus 1.1 Option Component



Modify R02
SDVO_CTRL.DATA strap pull high at PCH side

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Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title: HDMI Conn
				Size: Custom; Document Number: LA-7221P; Rev: 0.2
				Date: Wednesday, February 16, 2011; Sheet 33 of 59

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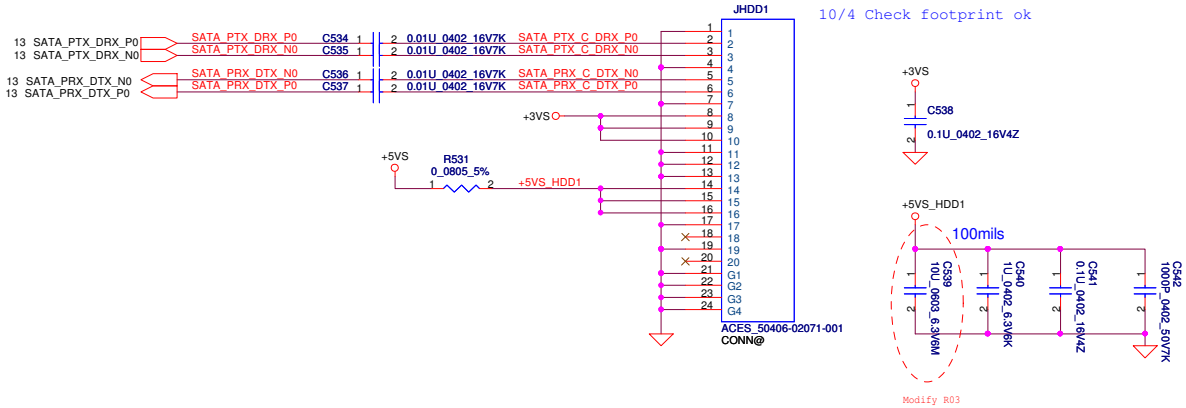
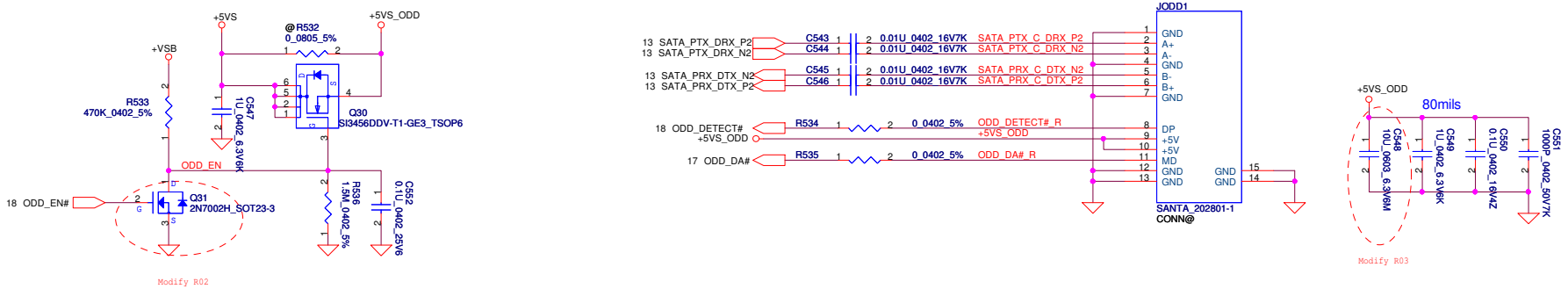
SATA HDD1 Conn.

CL 4.0 mm



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 34 of 59

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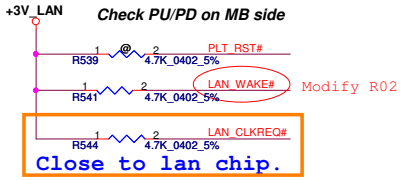
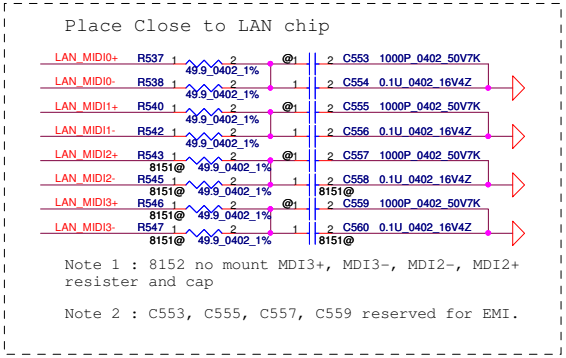
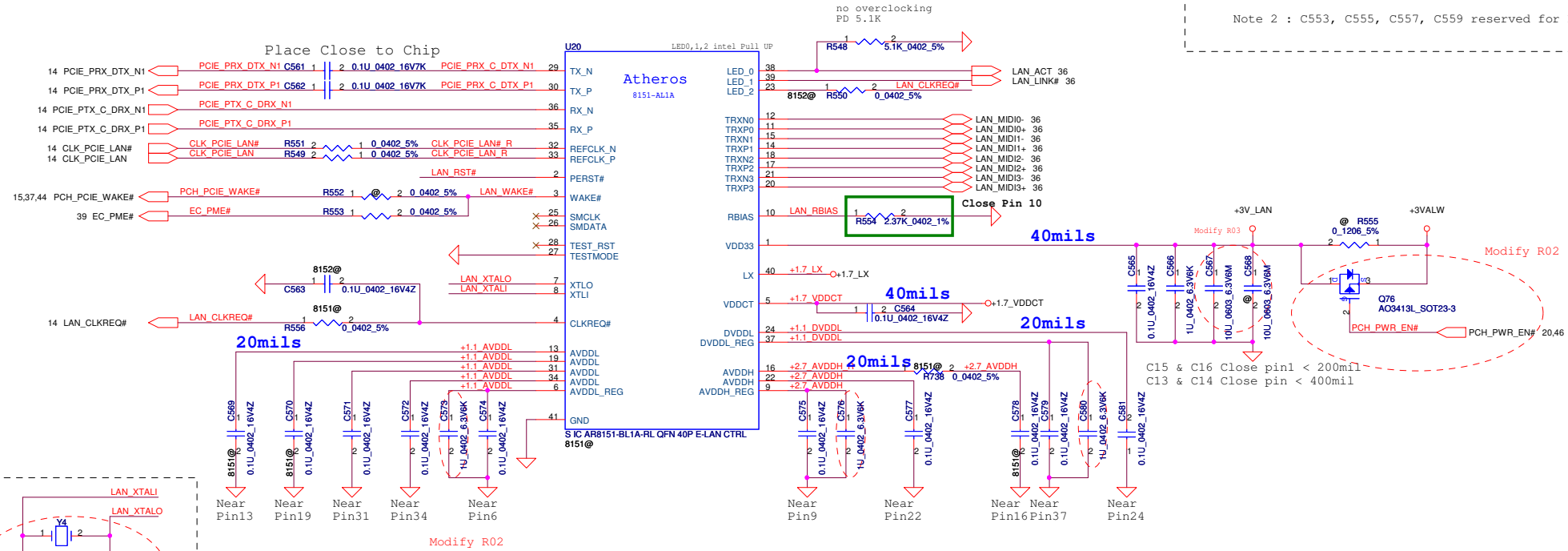
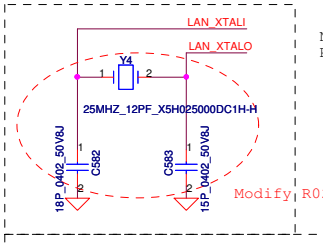


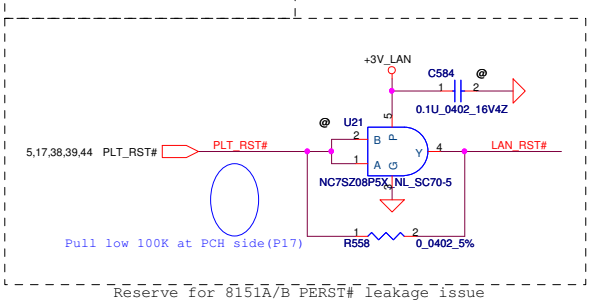
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable ★	H
LED1	H:SWR Switch mode regulator Select AR8151 Pin39 ★ H: switch regulator applied. L: switch regulator isn't applied. AR8152, Pin23 is CLKREQ	AR8151-BL1A applies switch mode regulator.



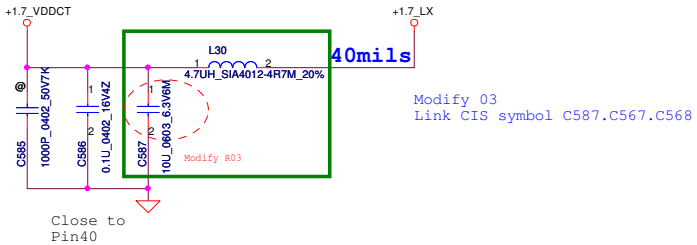






	Pin4	Configure R556	Configure C563		Pin23	Configure R550
AR8152	VDDCT_REG		★		CLKREQn	★
AR8151	CLKREQn	★			LED[2]	

Note: Place Close to LAN chip
L2 DCR< 0.15 ohm
Rate current > 1A



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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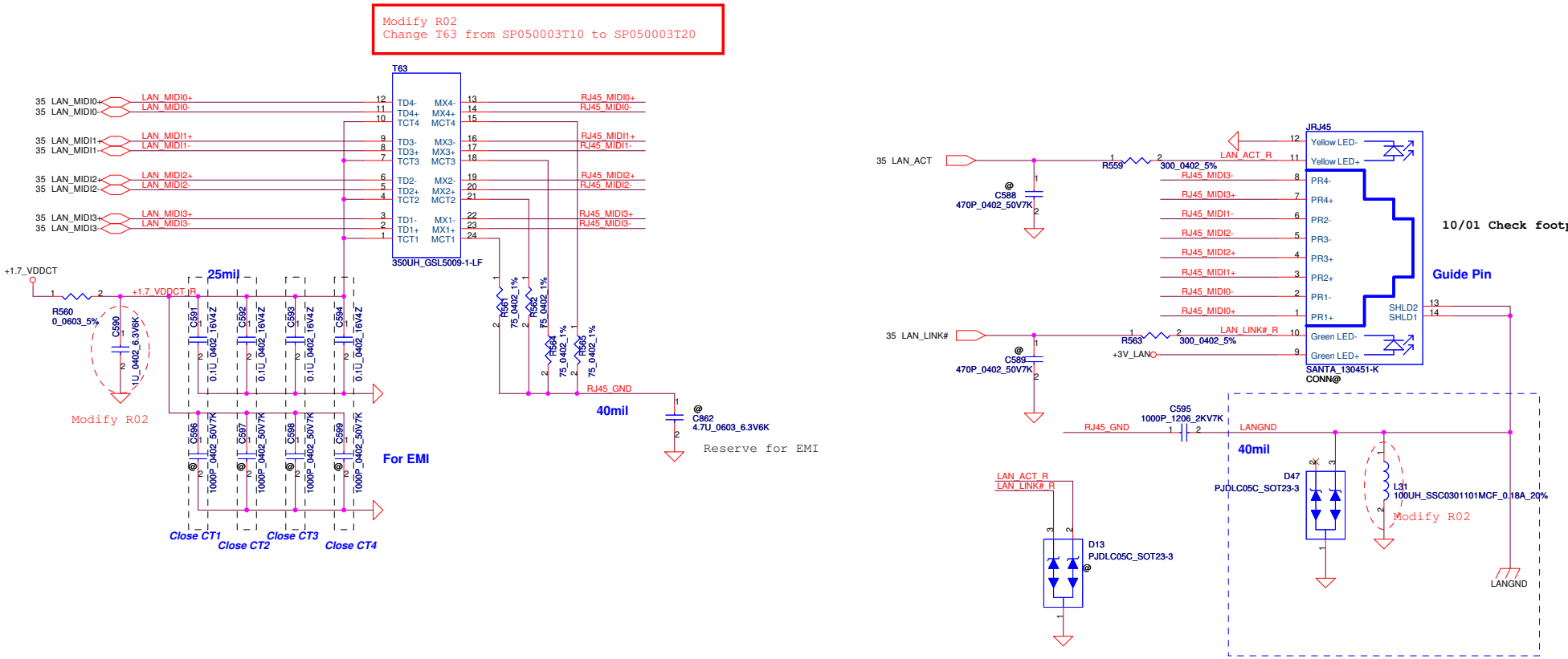
Compal Electronics, Inc.

Title: LAN Board AR8151 RevB

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 35 of 59



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 36 of 59

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For Wireless LAN

Modify R03

+3VS R566 0_0805_5% 60mil +3VS_WLAN

C602 4.7U_0603_6.3V6K, C603 0.1U_0402_16V4Z (+3VS_WLAN)
C604 4.7U_0603_6.3V6K, C605 0.1U_0402_16V4Z, C606 0.1U_0402_16V4Z (+1.5VS)
C607 0.1U_0402_16V4Z (+3VS_WLAN)

@R568 0_0402_5%

JMINI1 — ACES_88910-5204 CONN@

4 mm High

10/04 Check footprint ok
Footprint: BELLW_80003-1021_52P

15,35,44 PCH_PCIE_WAKE#
14 MINI1_CLKREQ#
14 CLK_PCIE_MINI1#
14 CLK_PCIE_MINI1
(WLAN_BT_DATA)
(WLAN_BT_CLK)
14 PCIE_PRX_DTX_N2
14 PCIE_PRX_DTX_P2
14 PCIE_PTX_C_DRX_N2
14 PCIE_PTX_C_DRX_P2
39 E51TXD_P80DATA
39 E51RXD_P80CLK
R574 0_0402_5% E51TXD_P80DATA1_R
R816 0_0402_5% E51RXD_P80CLK_R
R576 100K_0402_5%
R817 1K_0402_5% <BOM Structure>

WL_OFF# 18
PLT_RST_BUF# 17
R569 0_0603_5% +3VS
MINI1_SMBCLK R570 0_0402_5% PCH_SMBCLK 14
MINI1_SMBDATA R571 0_0402_5% PCH_SMBDATA 14
USB20_N8 17
USB20_P8 17
R573 0_0402_5% MINI1_LED# 39
(9~16mA)
R575 100K_0402_5% +3VS_WLAN

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

D45 RB751V-40_SOD323-2
39,46,52,53 SUSP# BT_CTRL
BT_ON# Q70 2N7002H_SOT23-3 <BOM Structure>

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H

For 3G / GPS
To 3G Module Connect

J3G1 — ACES_88242-2001 CONN@

+3VS
18 WWAN_OFF#
39 WWAN_LED#
+VSB
USB20_N9 USB20_N9 17
USB20_P9 USB20_P9 17
USB20_N12 USB20_N12 17
USB20_P12 USB20_P12 17
UIM_DET_EC UIM_DET_EC 39
EC_SIM_DETECT# 39
WWAN_DET#_EC 39

Modify R02
Change 3G Power to 3G board
Change L49 . L50.R764.R765.R766.R767 to 3G Board.(RF suggestion)

Modify R03

+5VALW C612 4.7U_0603_6.3V6K
U22 AP2301MPG-13_MSOP8 — GND VIN VIN EN VOUT VOUT VOUT FLG EPAD
+USB_VCCB
R578 0_0402_5% USB_OC0# 17
46 SYSON# SYSON#

+5VALW C815 4.7U_0603_6.3V6K
U40 AP2301MPG-13_MSOP8 — GND VIN VIN EN VOUT VOUT VOUT FLG EPAD
+USB_VCCA
R746 0_0402_5% USB_OC1# 17
46 SYSON# SYSON#

Follow HW3 Standard Part
(AP2301MPG-13_MSOP8)

USB/B Conn.

(Port 0,1,2)

W=100mils

JUSB1 — ACES_85201-2005N CONN@

+USB_VCCA
+USB_VCCB
17 USB20_N0 USB20_N0
17 USB20_P0 USB20_P0
17 USB20_N1 USB20_N1
17 USB20_P1 USB20_P1
17 USB20_N2 USB20_N2
17 USB20_P2 USB20_P2
39,40,50 BI R838 0_0402_5% BI_R
40 BI_RESET R839 0_0402_5%
41 BI_R
Modify R02 -->D-Door

+3VALW C613 0.1U_0402_16V4Z
+3VS C614 1U_0603_10V4Z
18 BT_ON# BT_ON# R579 10K_0402_5% Q32 AO3413L_SOT23-3
C615 0.1U_0402_16V4Z
W=40mils
+BT_VCC
C616 4.7U_0603_6.3V6K, C617 0.1U_0402_16V4Z
R580 300_0603_5%
Q33 2N7002H_SOT23-3

BT Conn.

(Port 13)

+BT_VCC
JBT1 — ACES_87213-0600G CONN@
USB20_P13 17
USB20_N13 17

10/01 Check footprint OK

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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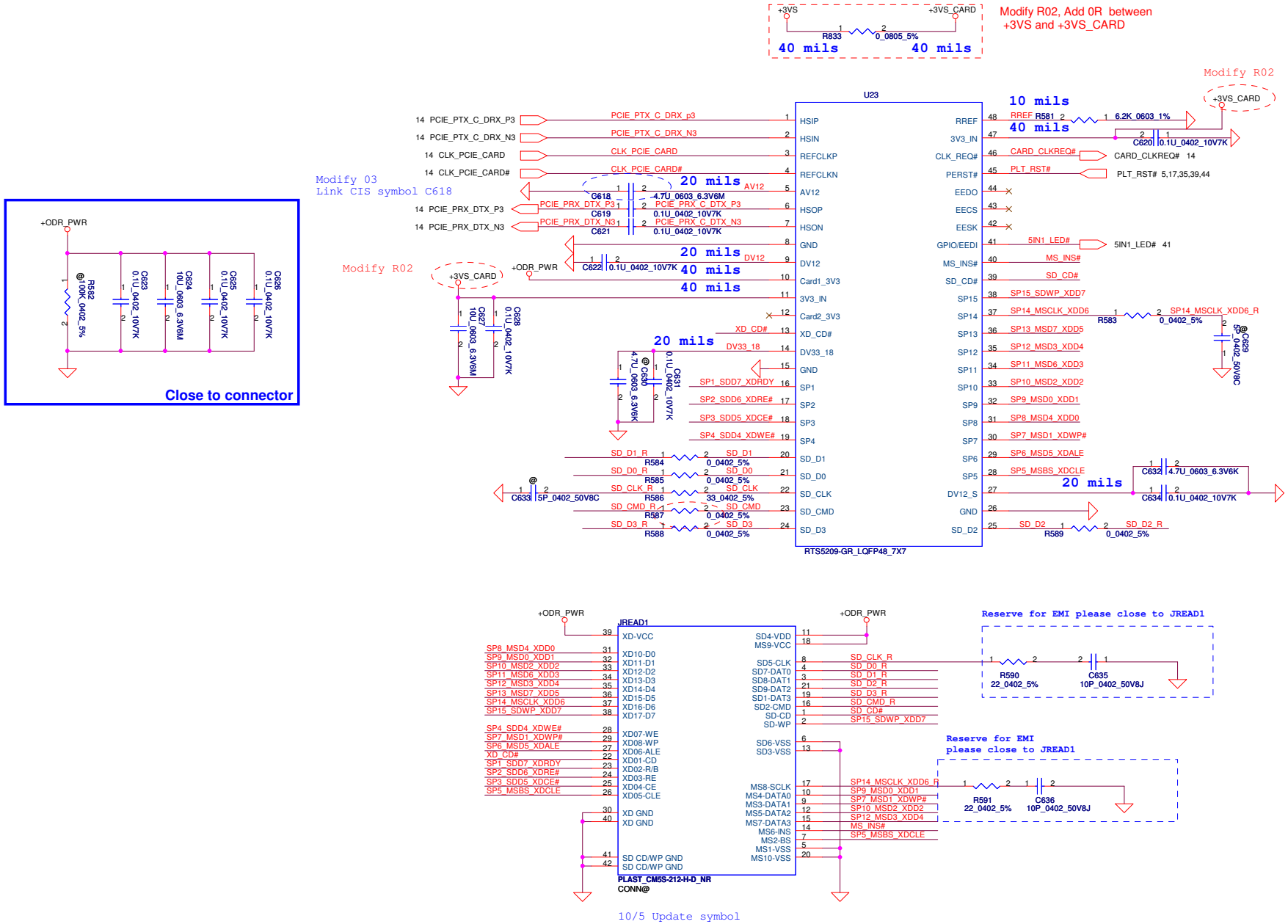
Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)/USB/BT

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 37 of 59

Card Reader



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/08/10	Deciphered Date 2010/08/01	Title: Card Reader RTS5209
			Size: Custom; Document Number: LA-7221P; Rev: 0.2
			Date: Wednesday, February 16, 2011; Sheet 38 of 59

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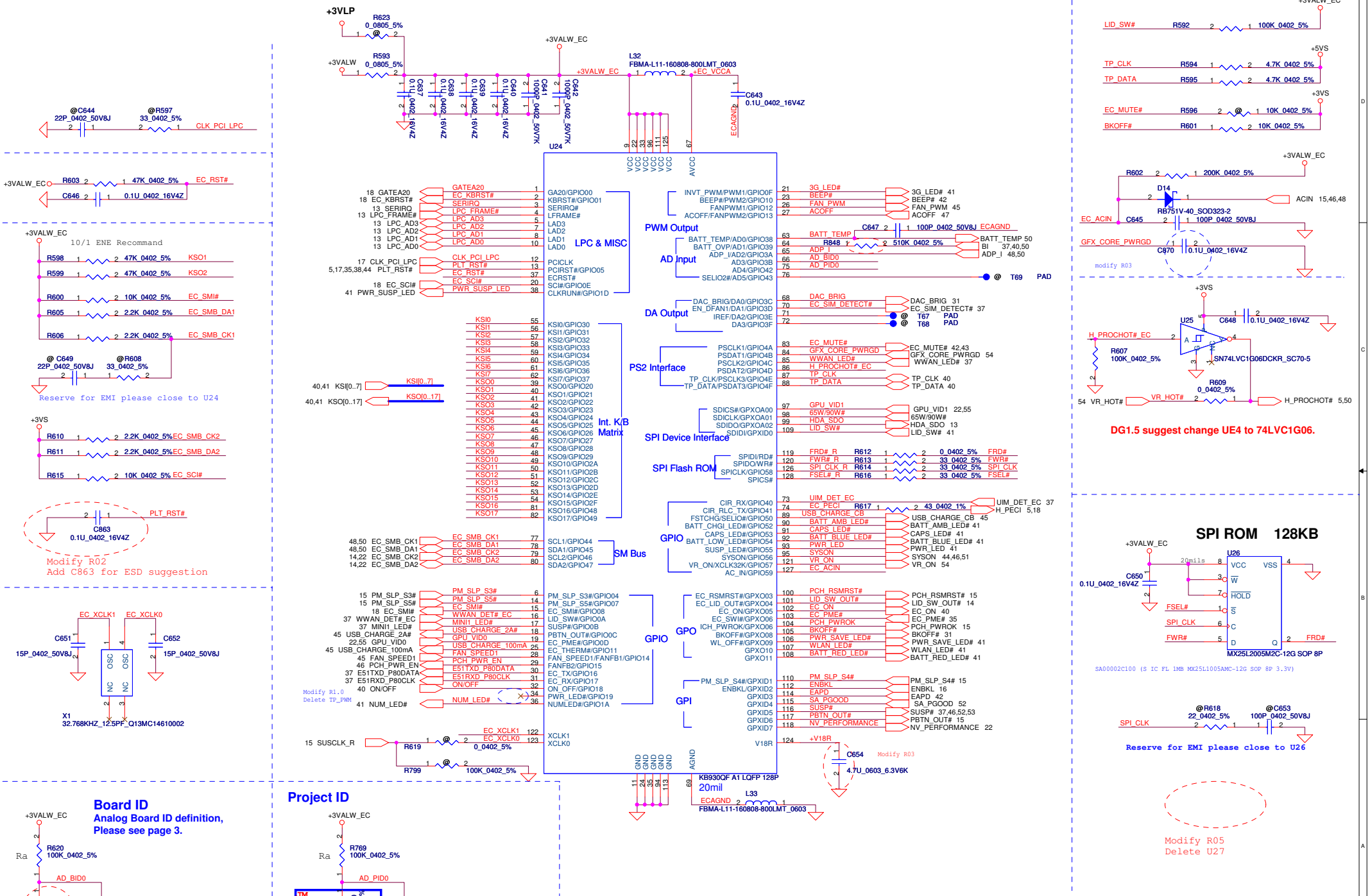

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

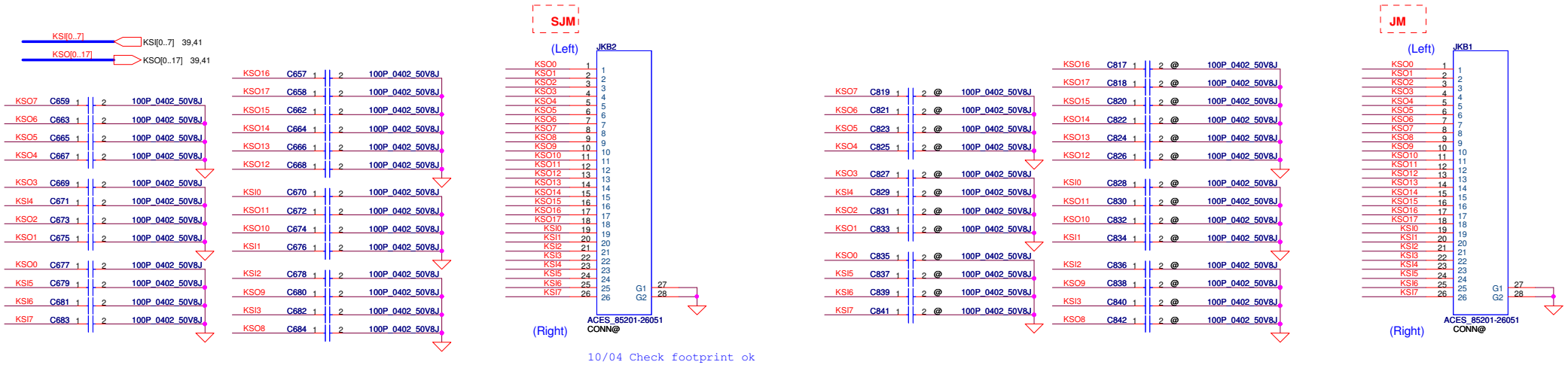
Title: EC ENE-KB930

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 39 of 59

INT_KBD Conn.

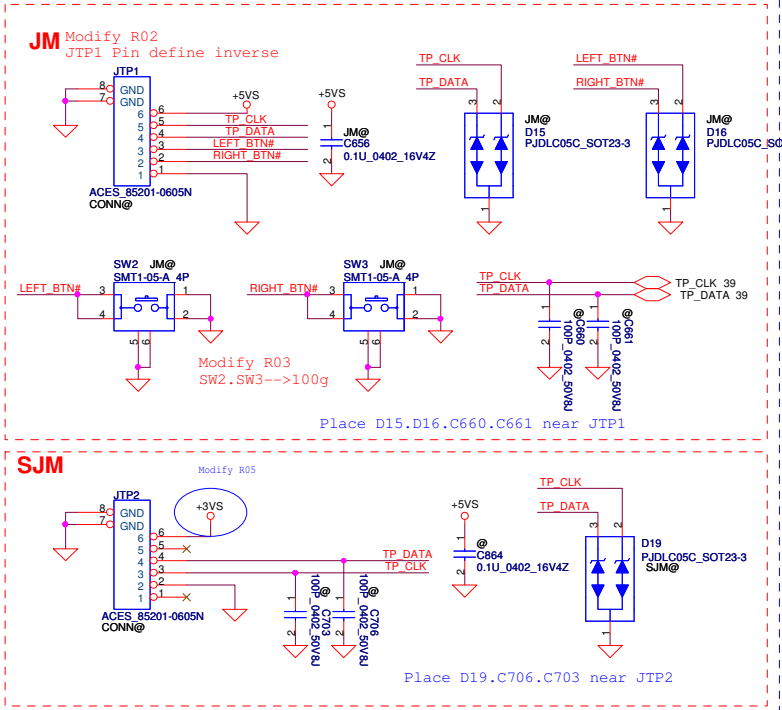
Modify R02
KB connector use JKB2,JKB1 reserved.



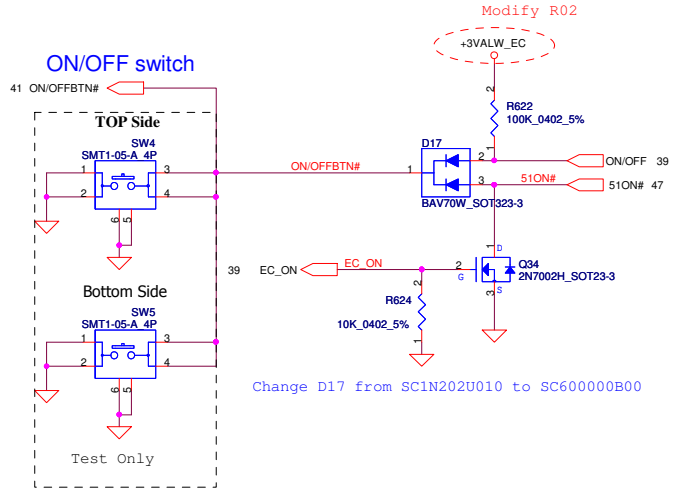
10/04 Check footprint ok

To TP/B Conn.

10/04 Check footprint ok

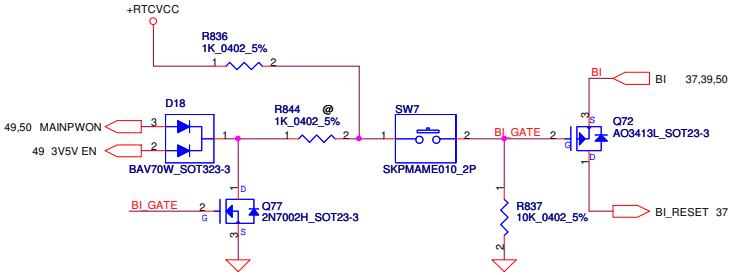


Power Button



Reset Button

Modify R02



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2008/08/10	Deciphered Date	2010/08/01	Title: I/O Port & K/B Connector/PWR OK
				Size: Custom; Document Number: LA-7221P; Rev: 0.2
				Date: Wednesday, February 16, 2011; Sheet 40 of 59

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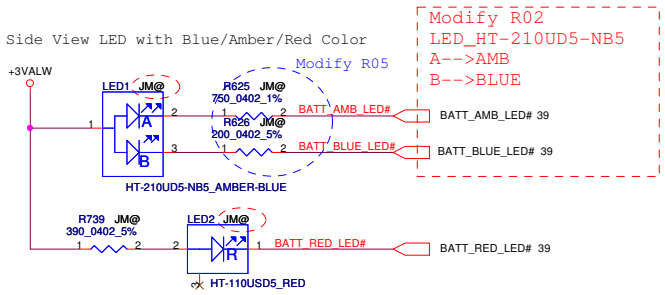
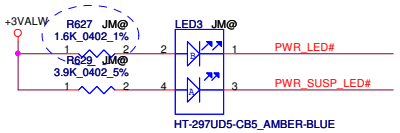
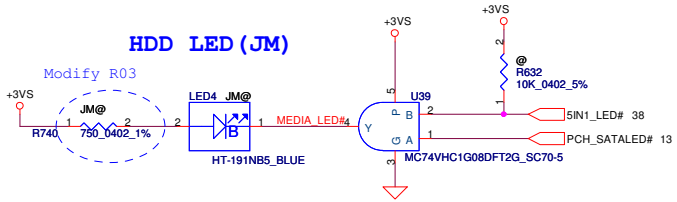
Battery LED(JM)



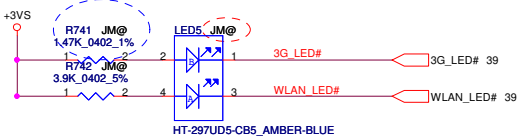
Power LED(JM)

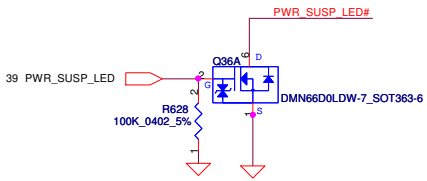


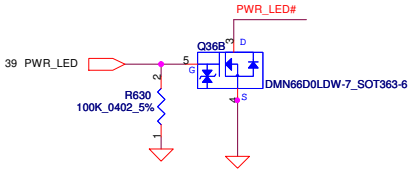
HDD LED(JM)



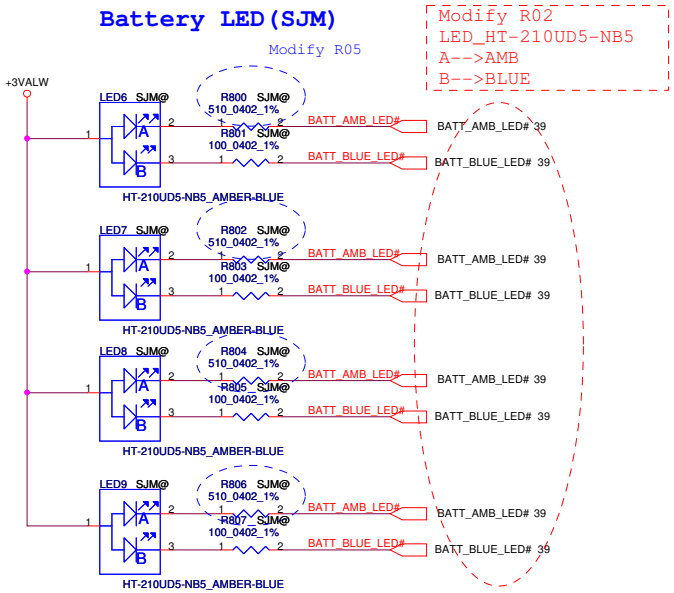
3G/Wireless LED(JM)



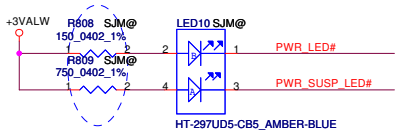




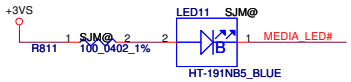
Battery LED(SJM)



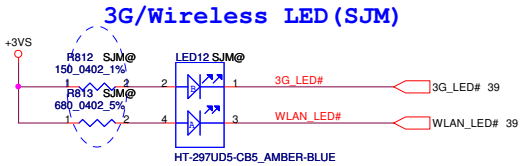
Power LED(SJM)



HDD LED(SJM)

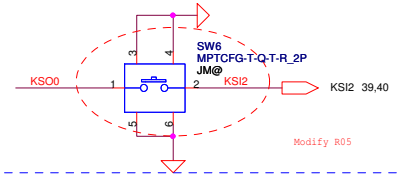


3G/Wireless LED(SJM)



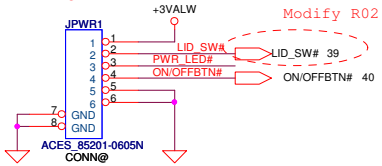
LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
	Blue	Amber	Blue	Amber	Blue	Amber		

Battery Indicator BTN (JM only)

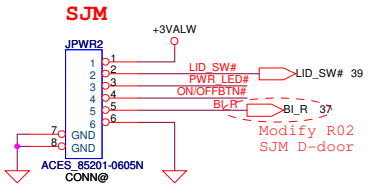


PWR/B

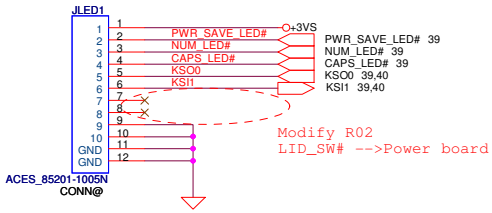
JM



SJM



LED Board (JM only)



	KSO0
KSI0	Battery BTN#
KSI1	PWR SAVE BTN#

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/08/10	Deciphered Date 2010/08/01	Title LED/PWR/B
			Size Custom / Document Number LA-7221P / Rev 0.2
			Date: Wednesday, February 16, 2011 / Sheet 41 of 59

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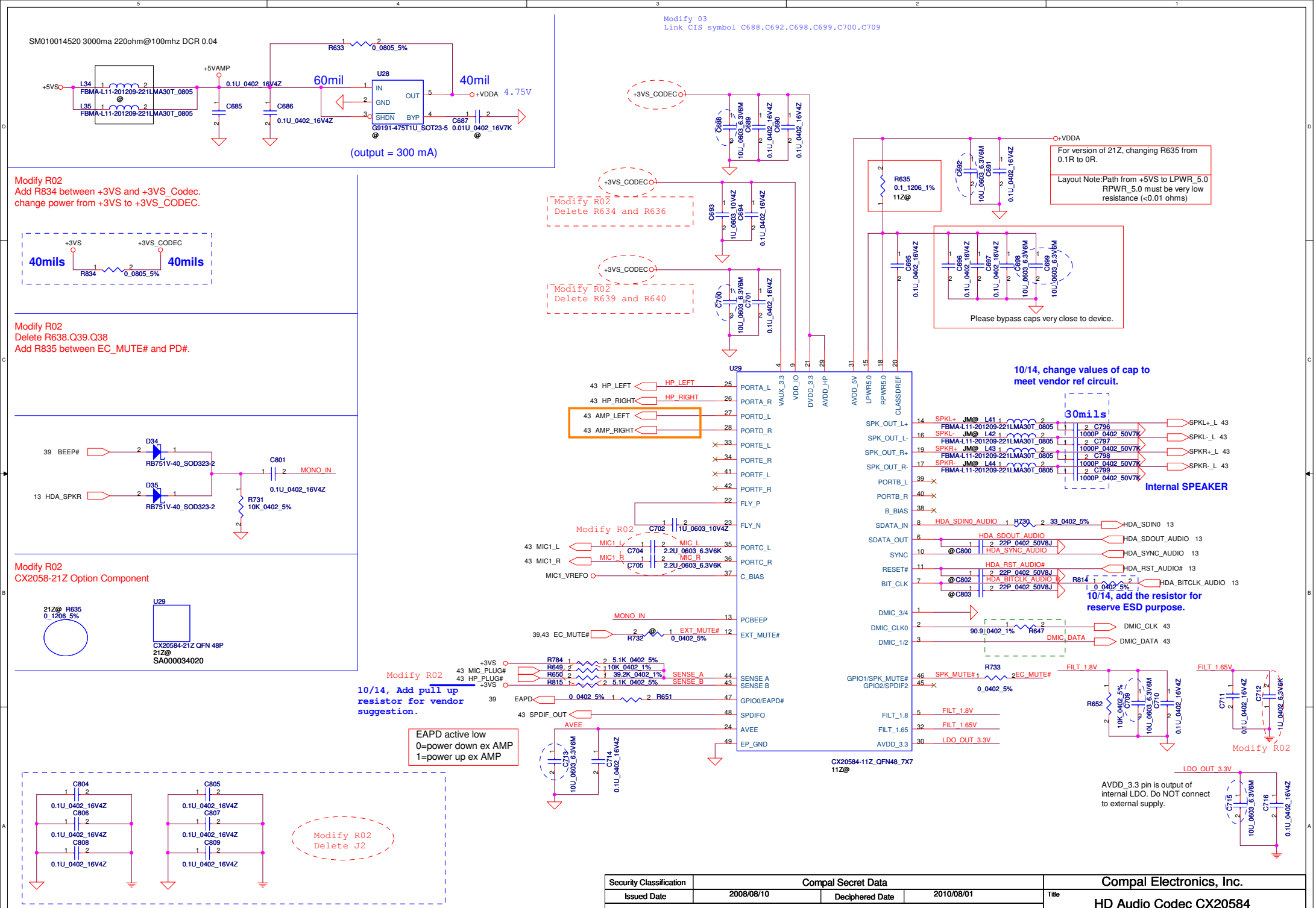

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: HD Audio Codec CX20584

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 42 of 59

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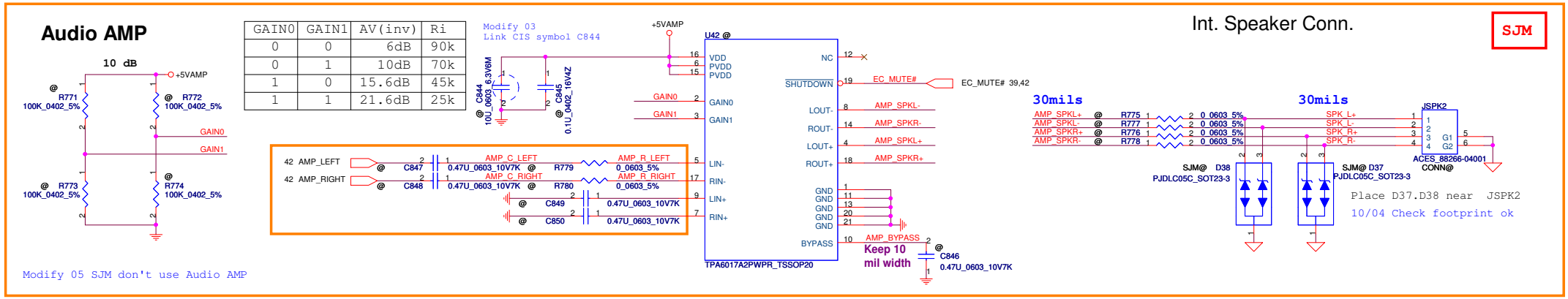
Audio AMP

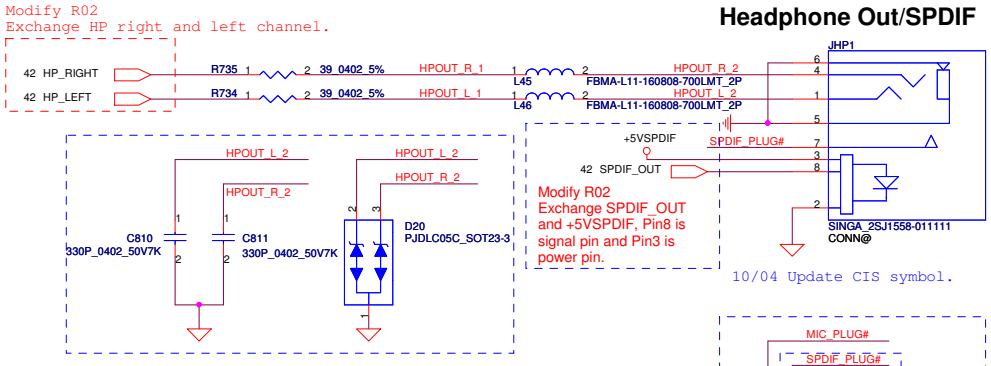
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

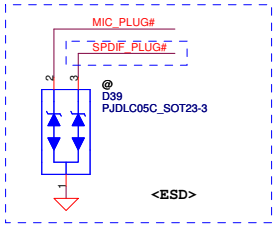


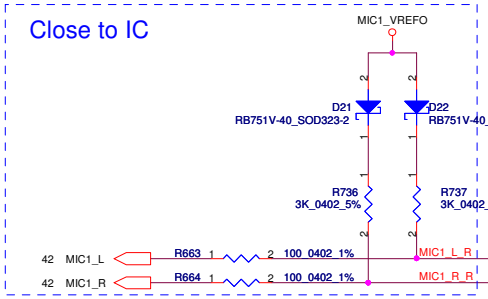
Int. Speaker Conn.

SJM

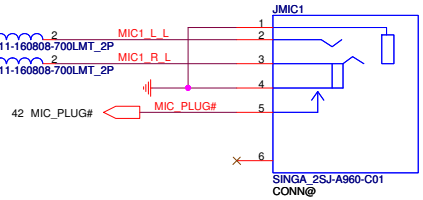
Headphone Out/SPDIF

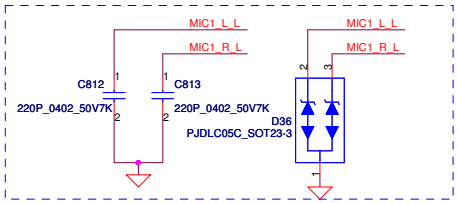






MIC JACK

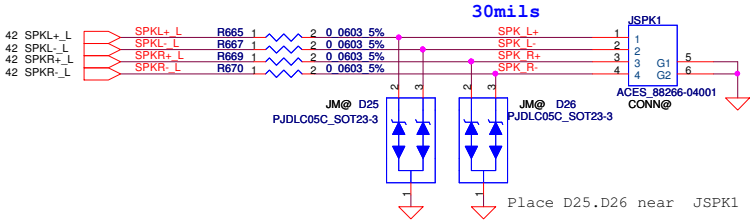




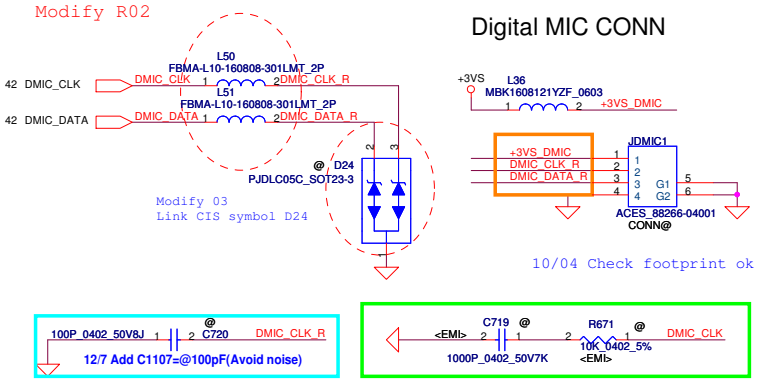
10/04 Check footprint ok
Footprint:SINGA_2SJ-0960-D06_6P

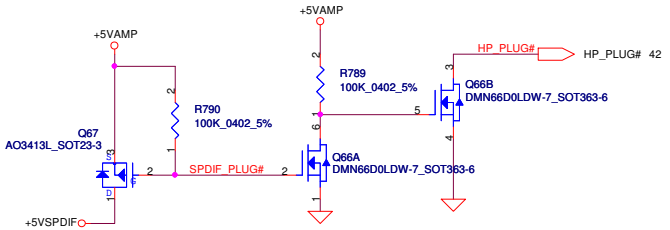
Int. Speaker Conn.

JM



Digital MIC CONN





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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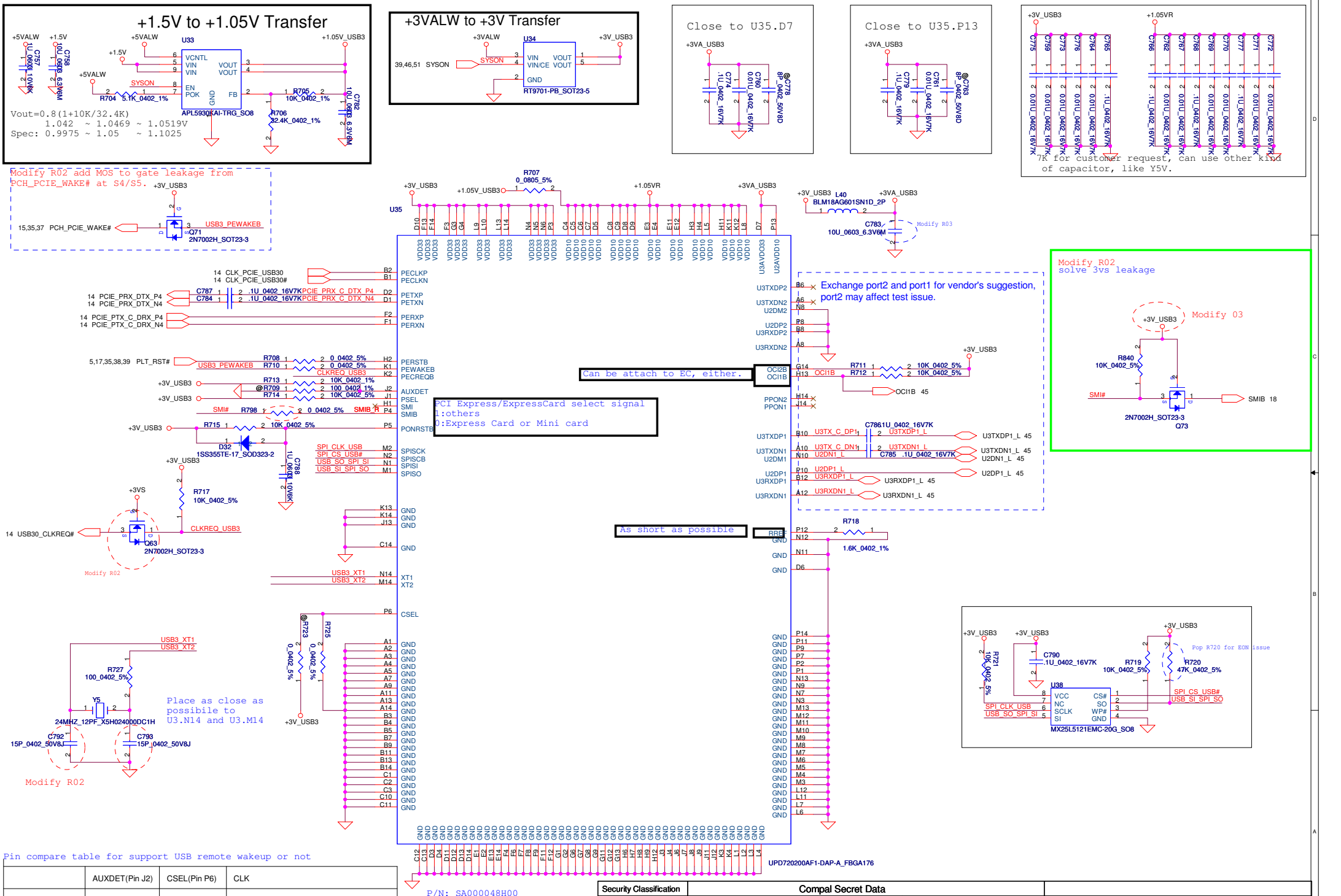
Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 43 of 59



Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R23

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Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

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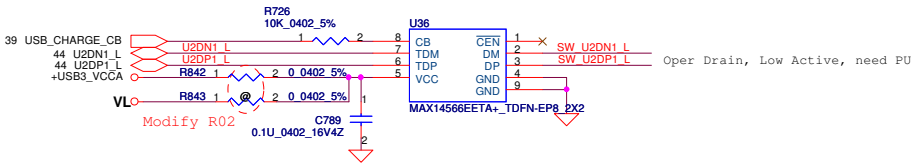
Title: USB3.0 PD720200A

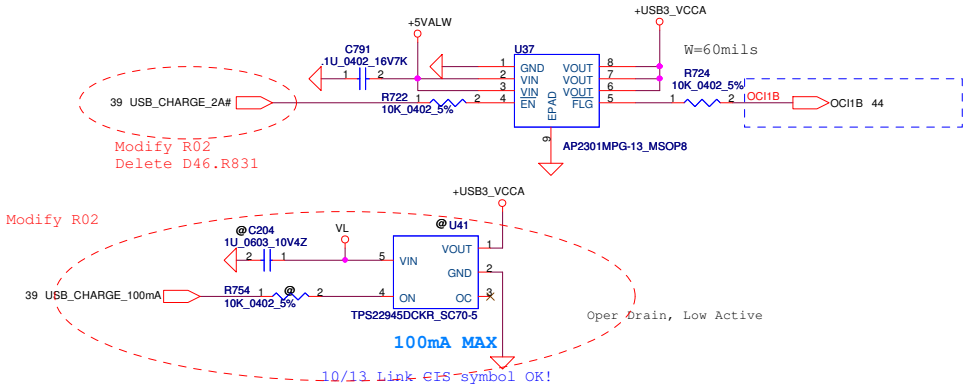
Size	Document Number	Rev
Custom	LA-7221P	0.2

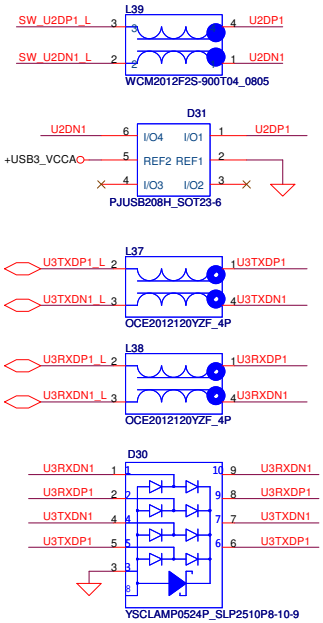
Date: Wednesday, February 16, 2011 | Sheet 44 of 59

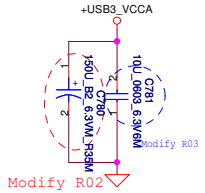
USB Host Charger



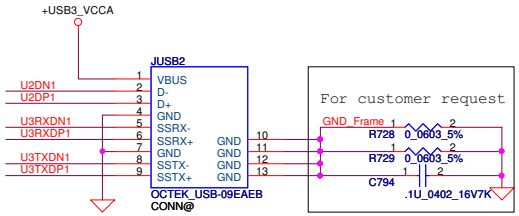
CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM





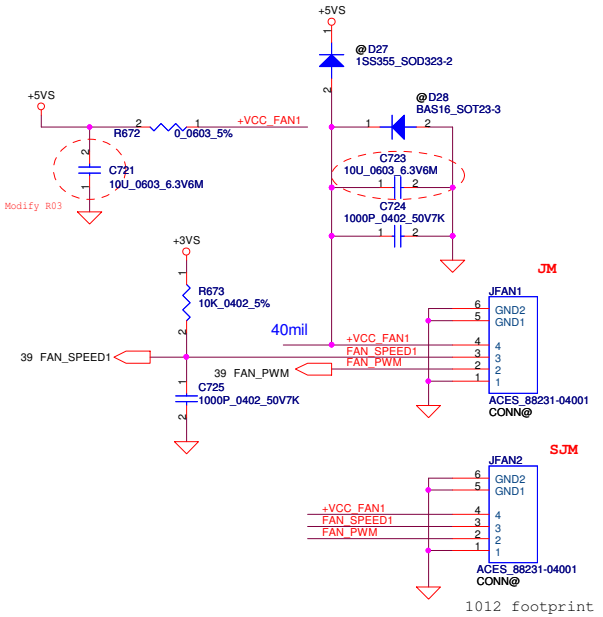


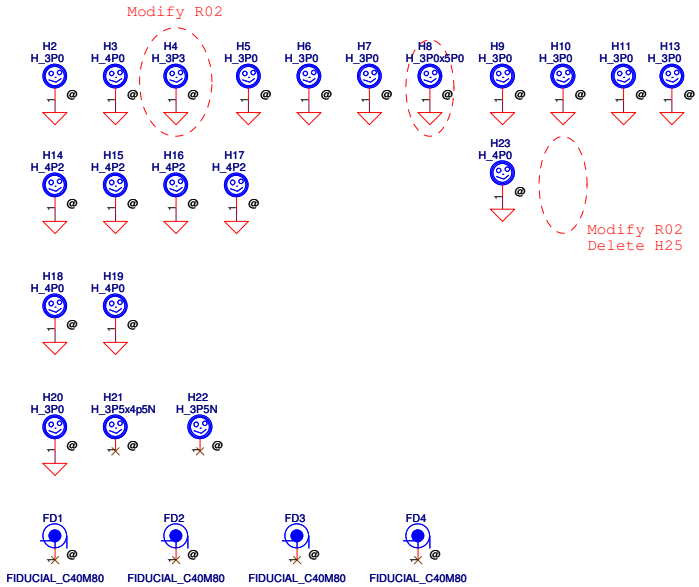
USB3.0 Connector



10/05 Update symbol .

FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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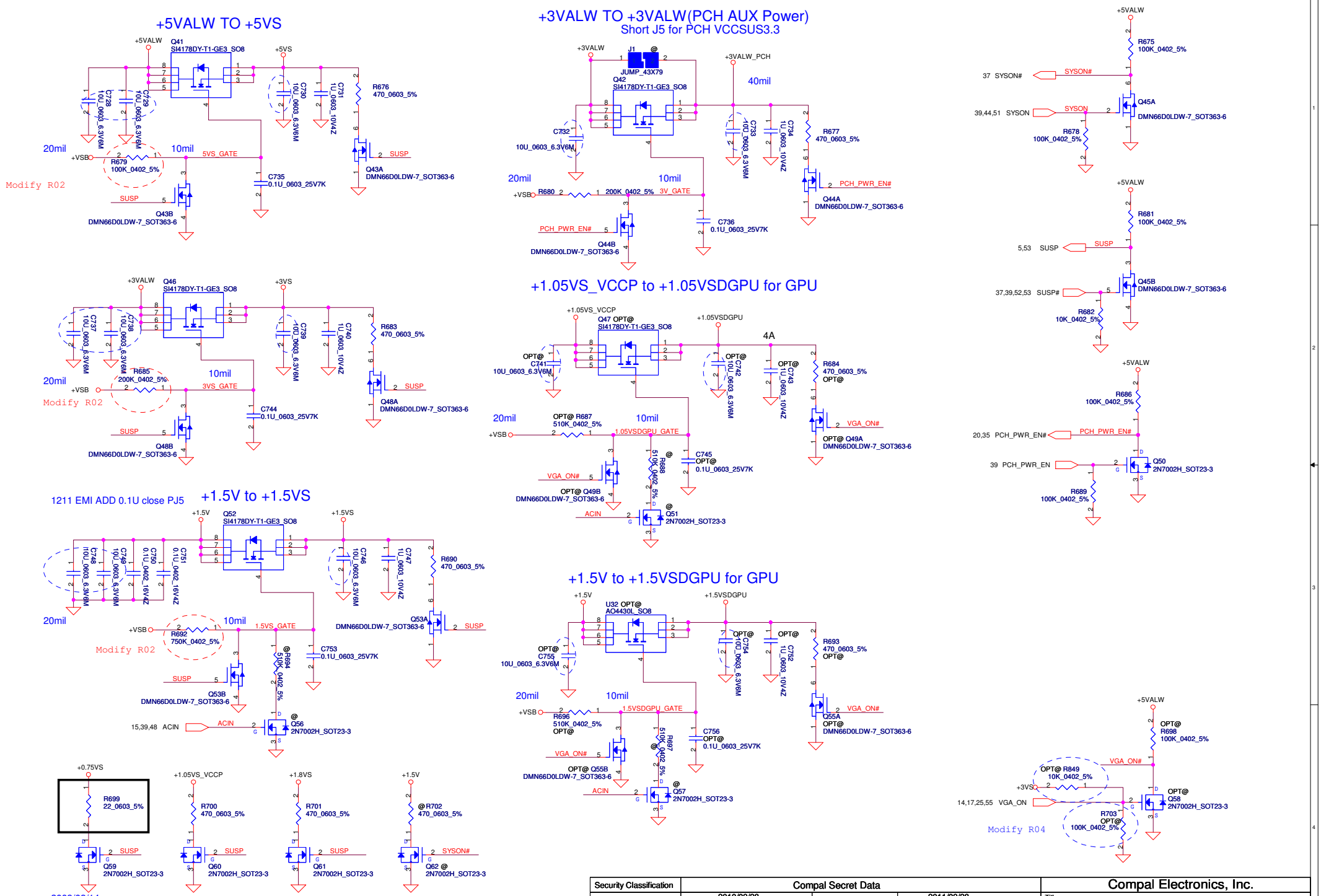
Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 45 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

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Compal Electronics, Inc.

Title: DC Interface

Size: Custom | Document Number: LA-7221P | Rev: 0.2

Date: Wednesday, February 16, 2011 | Sheet 46 of 59

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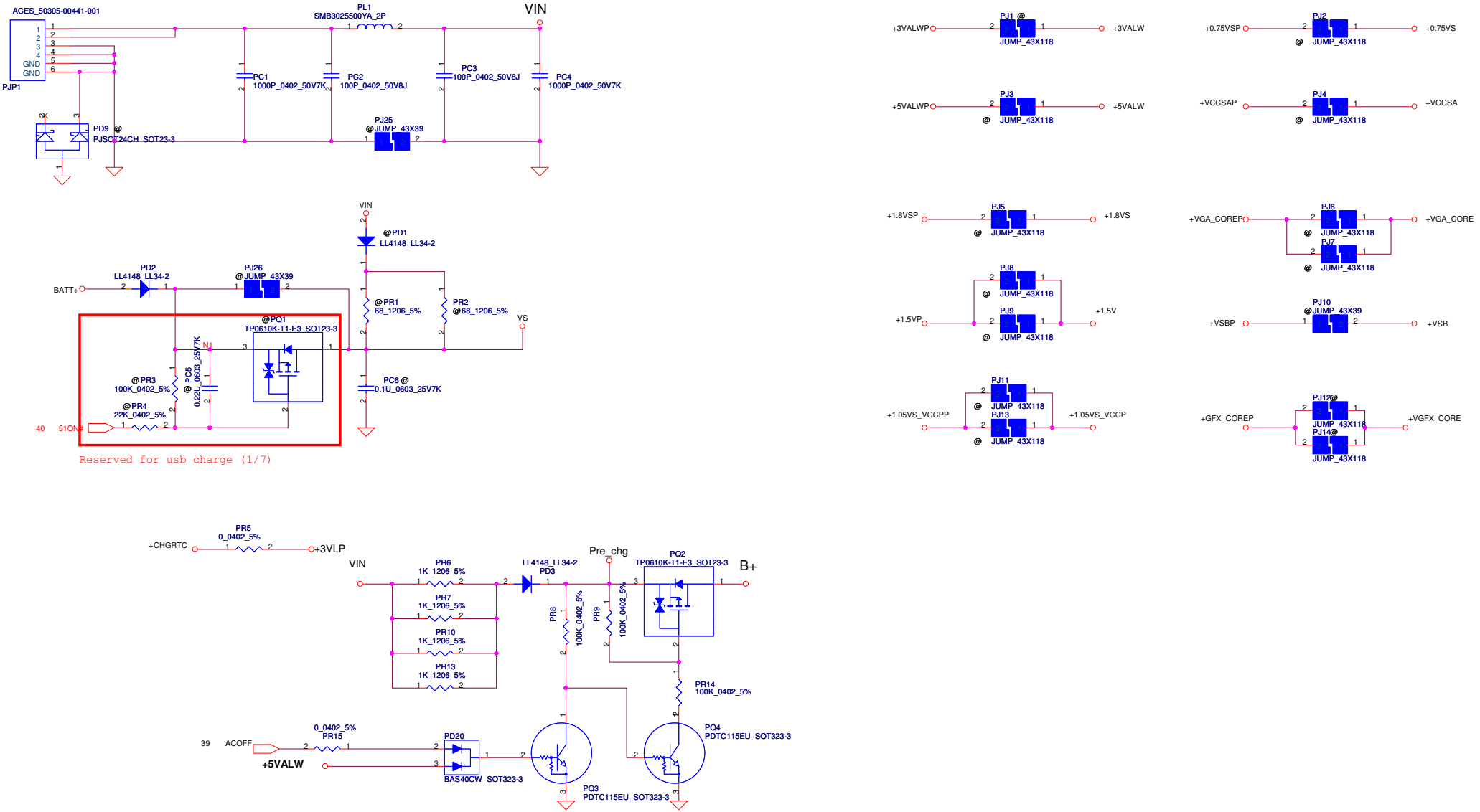

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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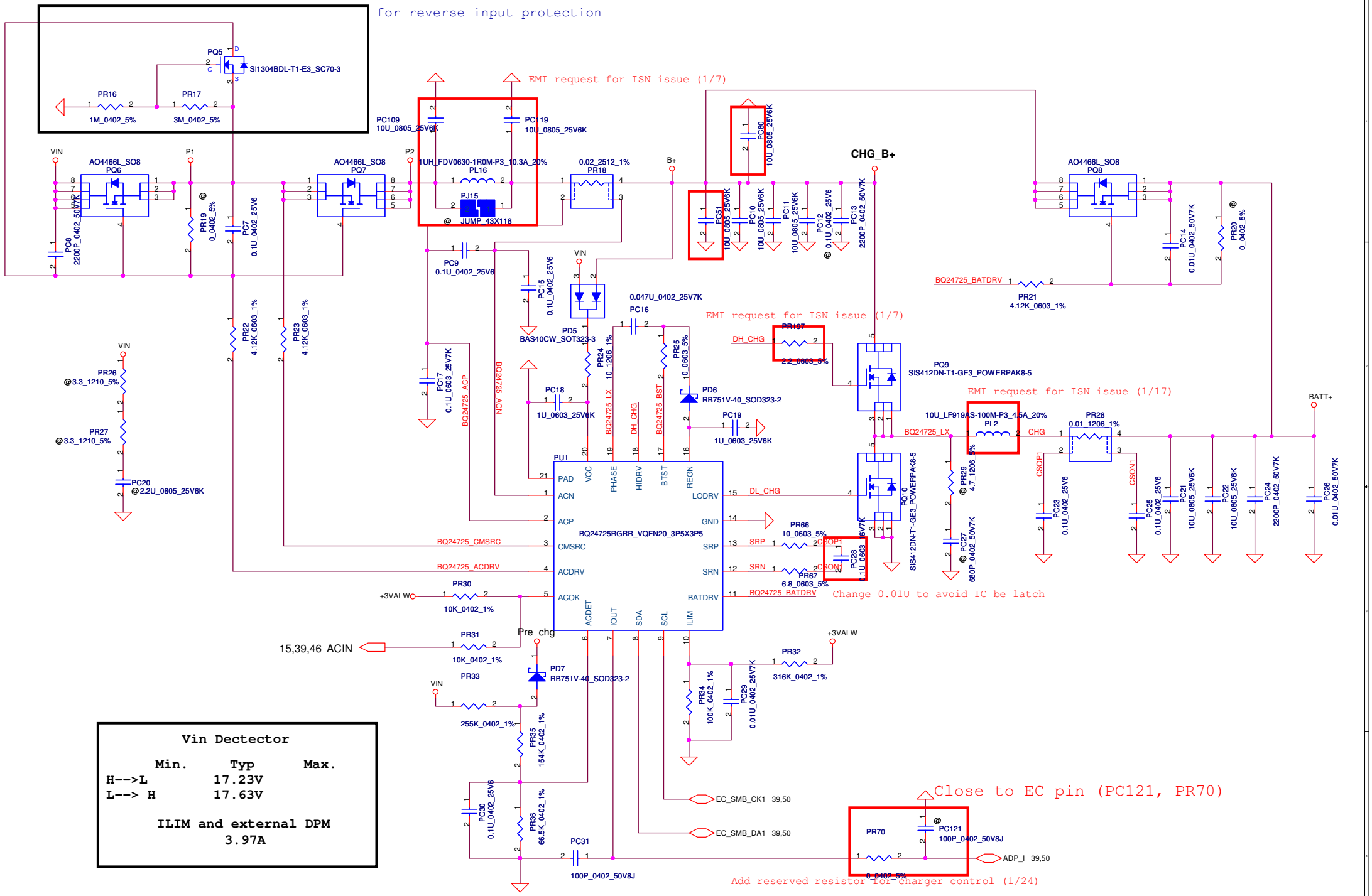
Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 47 of 59



Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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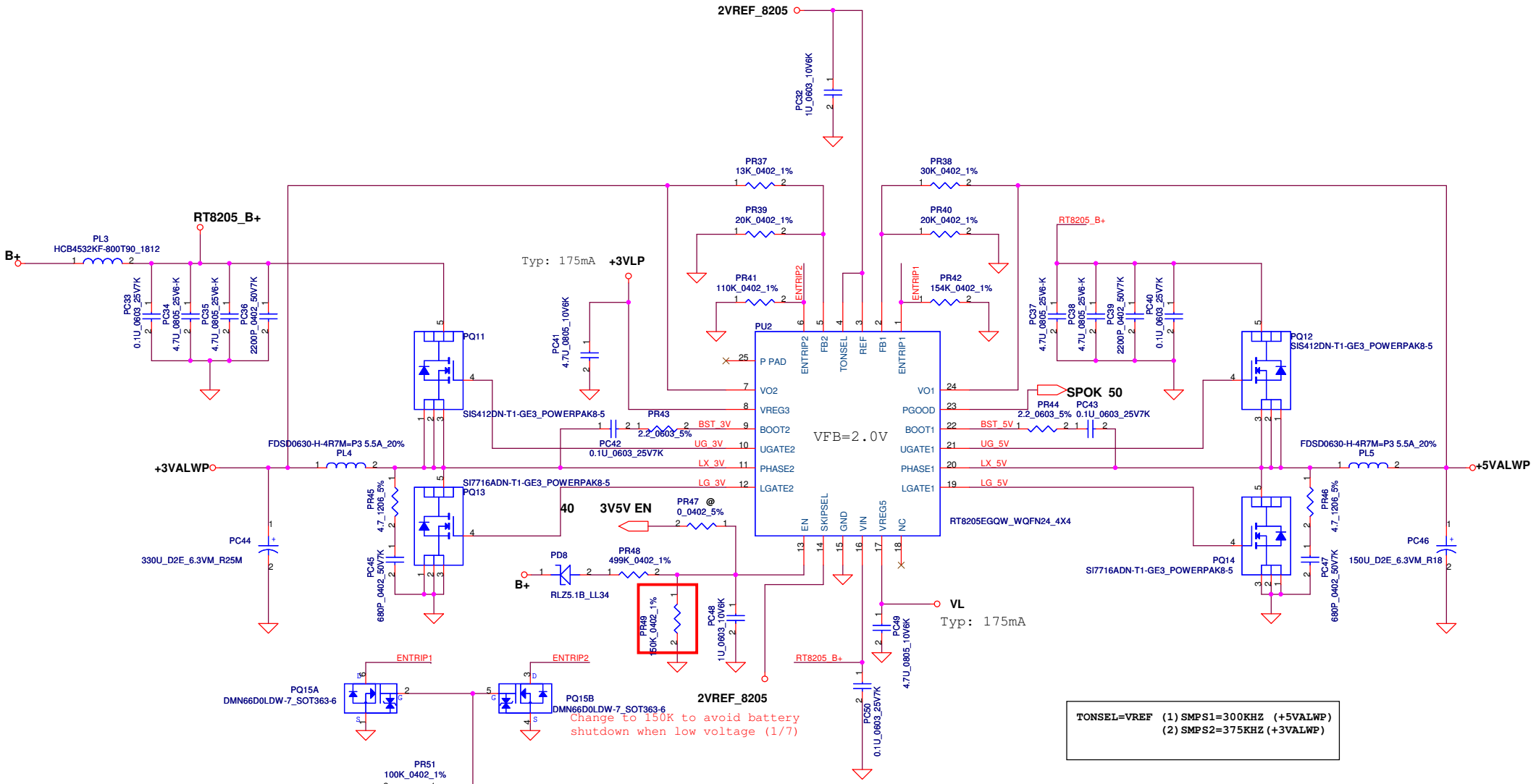
Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 48 of 59



TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

+3.3VALWP
Ipeak=5.78A ; 1.2Ipeak=6.94A; Imax=4.05A
f=375KHz, L=4.7UH
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-3)*(3/19)/(375KHz*4.7UH)=0.716A
Vlimit=10*10^-6*110Kohm/10=0.11V
Ilimit=0.11/(18m*1.2)~0.11/(15m)=6.34A~9.13A
Iocp=7.06A~9.85AA (7.06A>6.94A -> ok) -DVT-

+5VALWP
Ipeak=7A ; 1.2Ipeak=8.4A; Imax=4.9A
f=300KHz, L=4.7UH,Rentrip=154k ohm
Rdson=15~18m ohm
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vlimit=10*10^-6*154Kohm/10=0.15V
Ilimit=0.15/(18m*1.2)~0.15/(15m)=7.13~10.26A
Iocp=8.44~11.57A (8.44>8.4 -> OK)

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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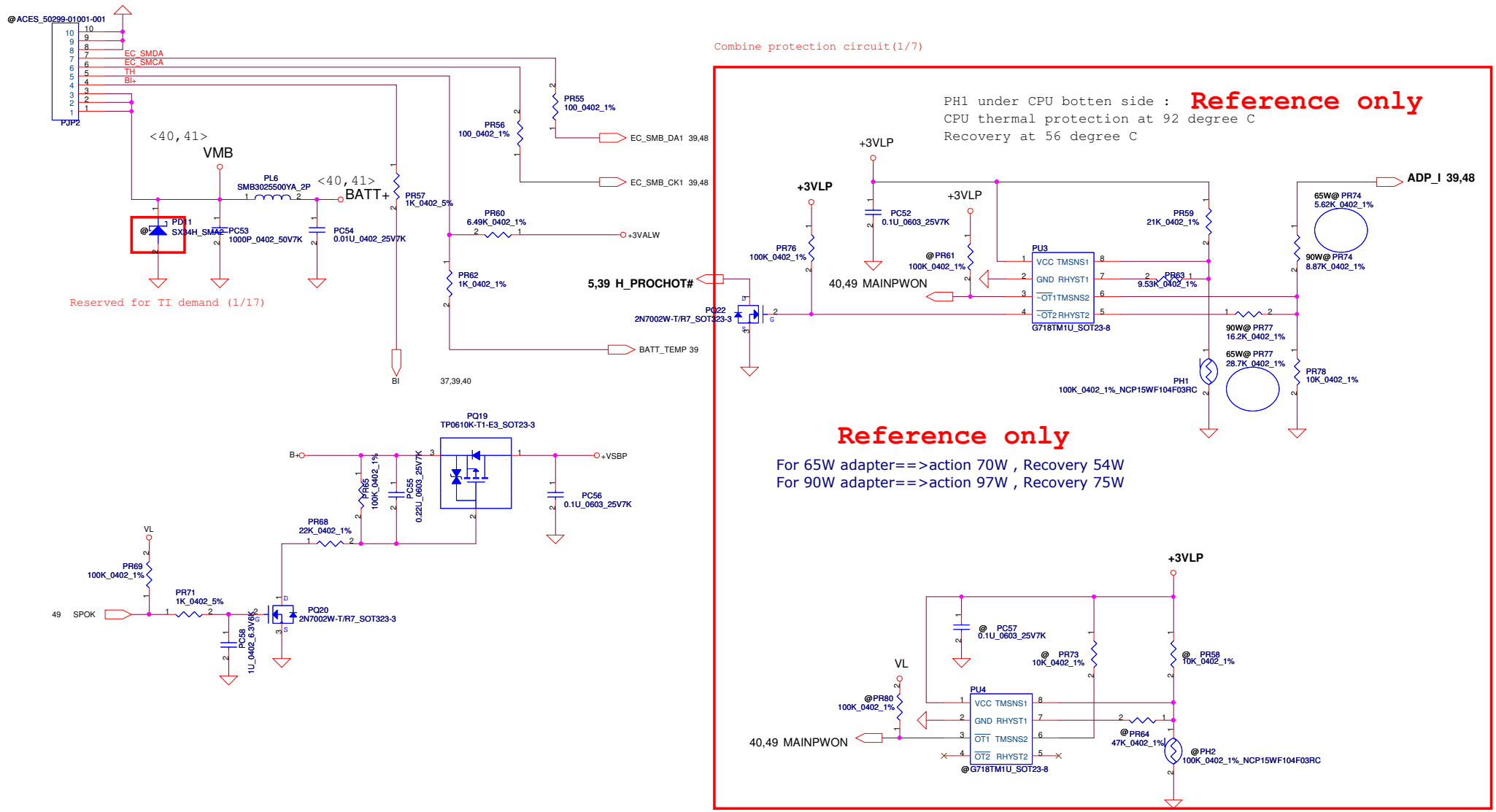
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 49 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

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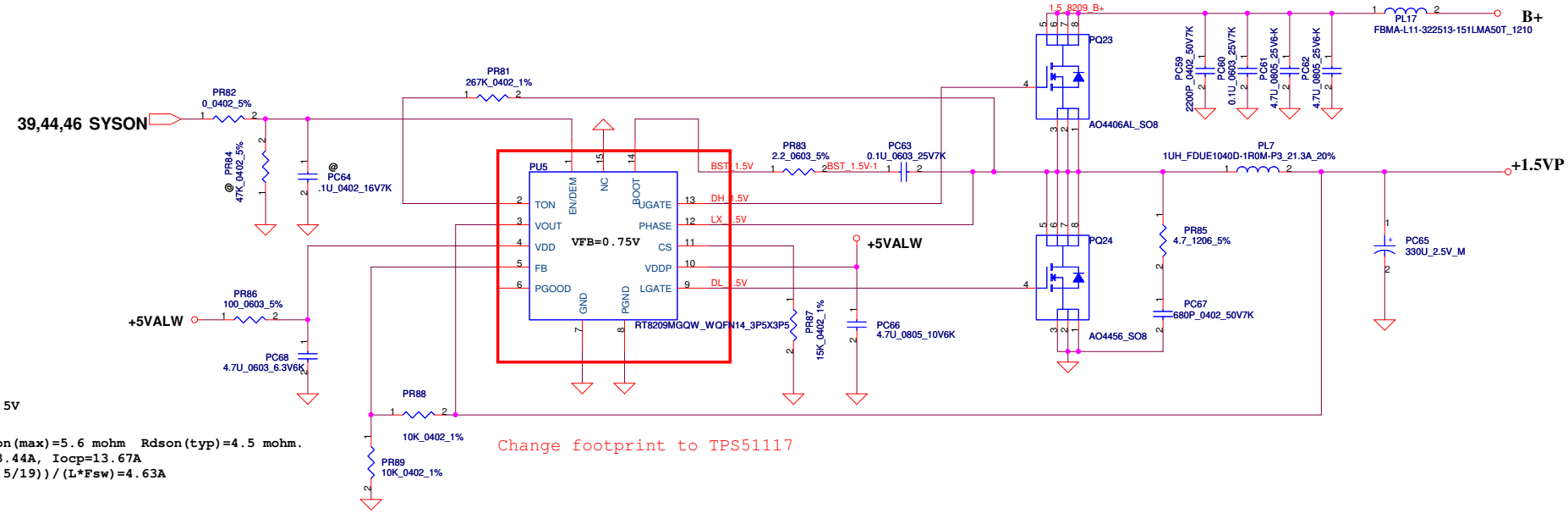
Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 50 of 59



Change footprint to TPS51117

```
<Vo=1.5V>  VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm  Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A
```

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/07/13	Deciphered Date	2011/07/13	Title: PWR-+1.5VP

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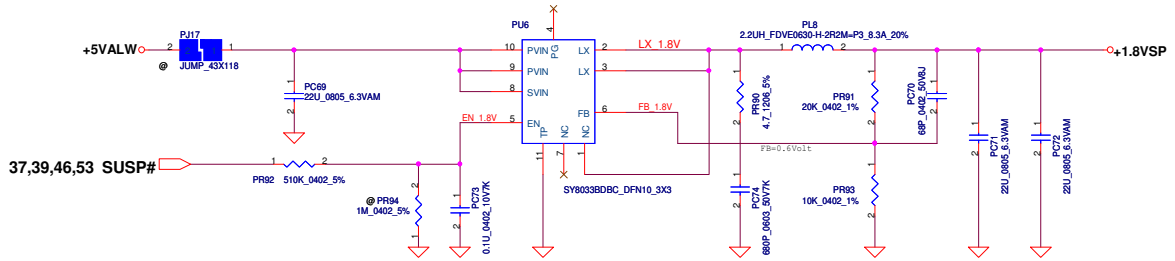
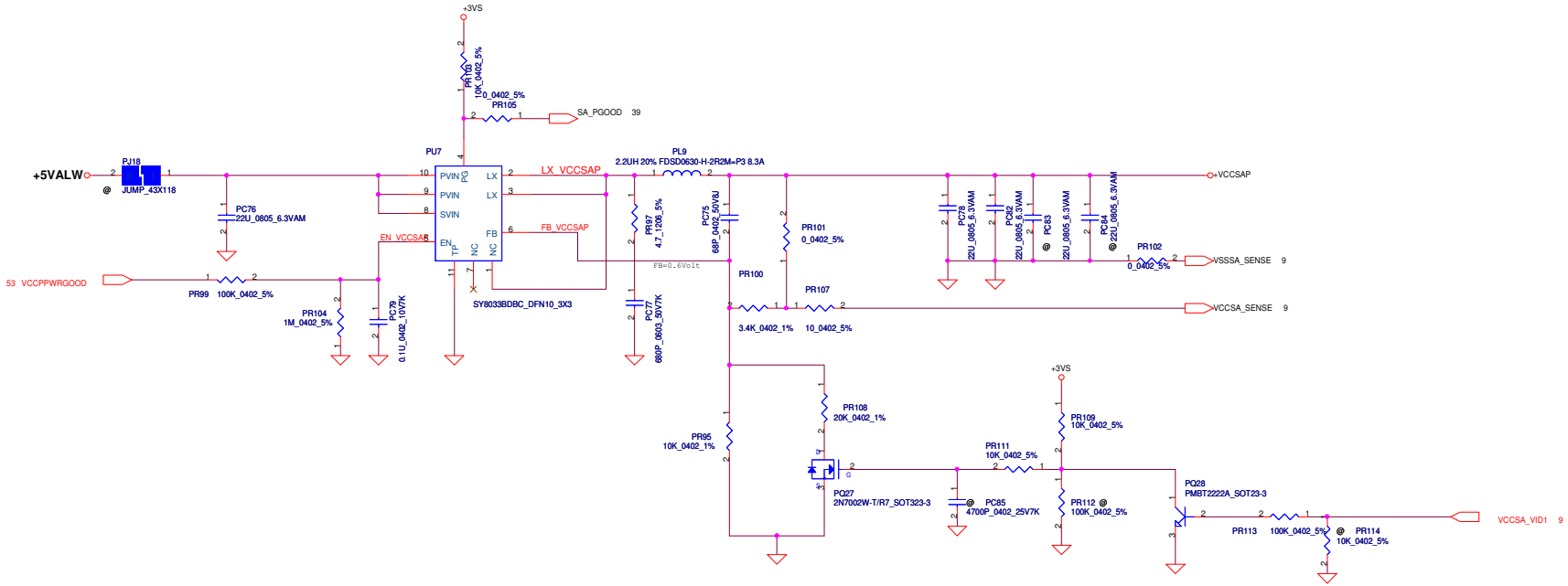
Size	Document Number	Rev
Custom	LA-7221P	0.1

Date: Wednesday, February 16, 2011 | Sheet 51 of 59

1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V





VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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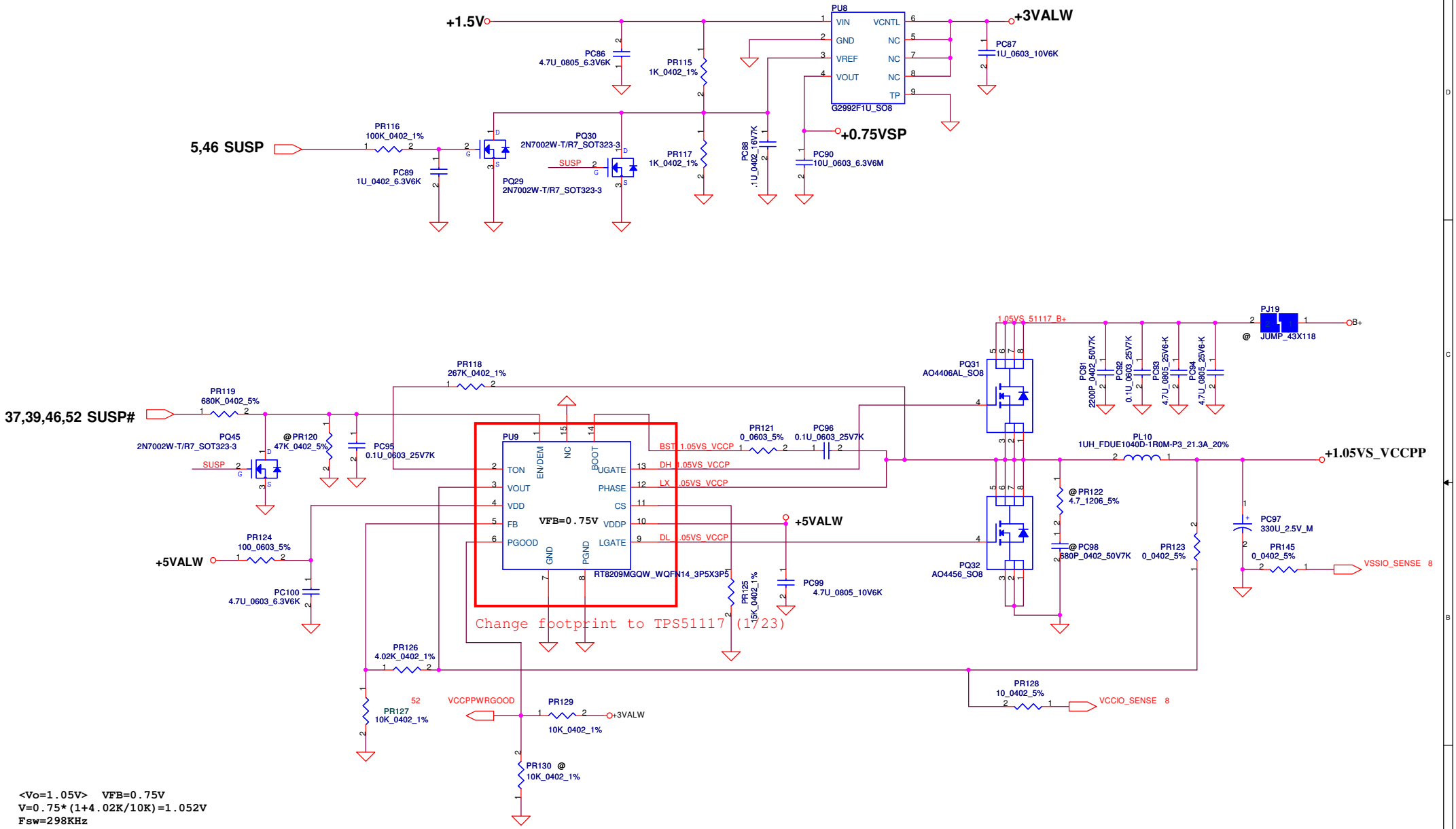
Compal Electronics, Inc.

Title: PWR +VCCSAP

Size: C | Document Number: LA-7221P | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 52 of 59



<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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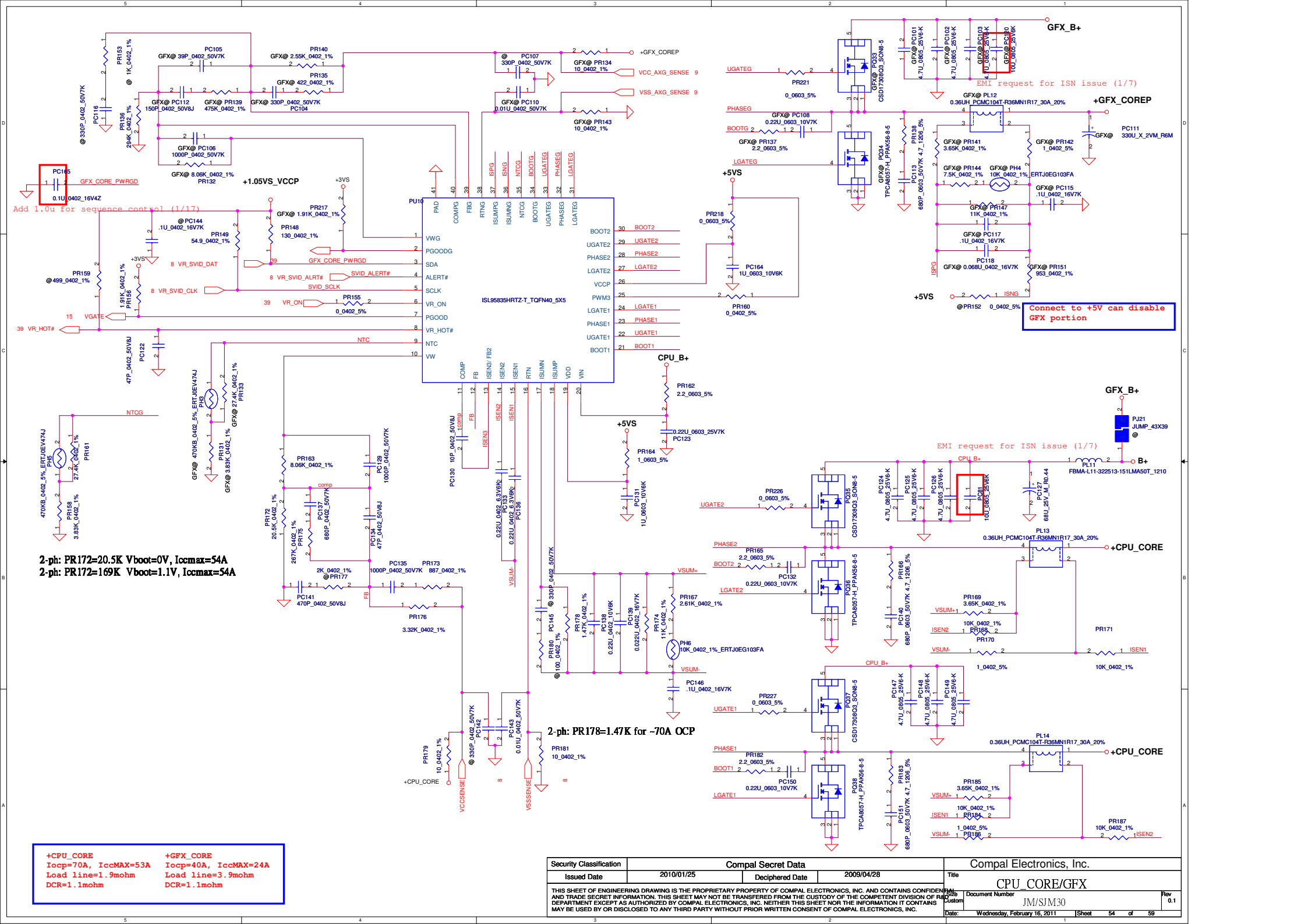
Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size: Custom | Document Number: LA-7221P | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 53 of 59



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/01/25	Deciphered Date	2009/04/28	Title: CPU_CORE/GFX
Size: Custom	Document Number: JM/SJM30			Rev: 0.1
Date: Wednesday, February 16, 2011	Sheet 54 of 59			

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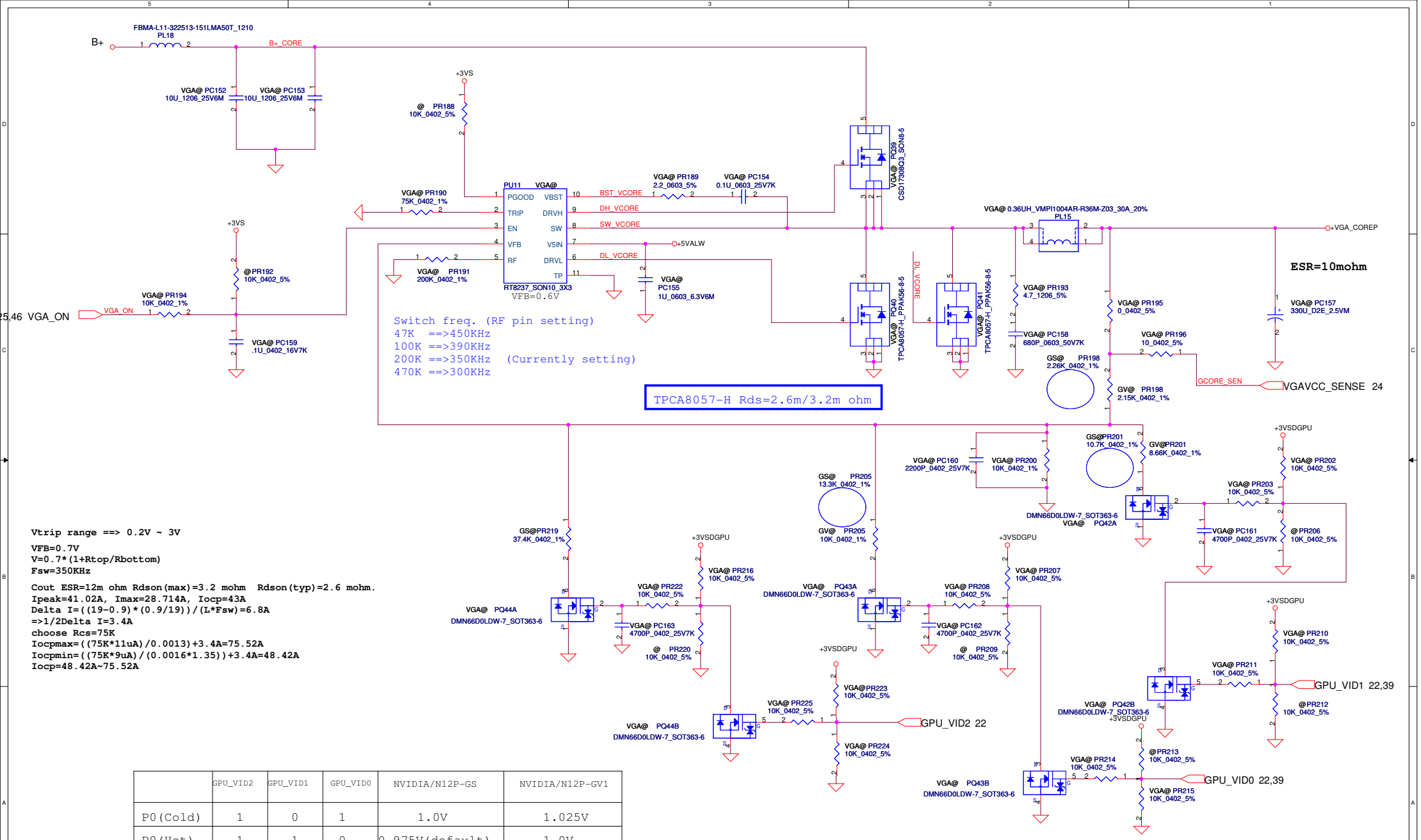


```
Vtrip range ==> 0.2V ~ 3V
VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz
Cout ESR=12m ohm Rdson(max)=3.2 mohm  Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A
```

	GPU_VID2	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P0(Cold)	1	0	1	1.0V	1.025V
P0(Hot)	1	1	0	0.975V(default)	1.0V
P8/P12	1	1	1	0.860V	0.85V(default)
SJM only ==> VPS	0	1	1	0.900V	----

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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Compal Electronics, Inc.

Title: +VGA_COREP

Size: Custom | Document Number: JM/SJM30 | Rev: 0.1

Date: Wednesday, February 16, 2011 | Sheet 55 of 59

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW/Edward request	Meet Turn off sequence		53	Add PQ45	2010 11/24	DVT
2	HW/Edward request	Meet Turn on sequence		53	Change PR119 to 680KΩ, PC95 to 0.1uF	2010 11/27	DVT
3	HW/Edward request	Meet new VGA table		55	Change PR201, PR205, PR219	2010 12/03	DVT
4	Battery Turn on time too long	Change enable 3/5V path				2010 12/04	DVT
5	HW/Edward request	For USB 3.0 charger function		47	Add PJ26	2010 12/04	DVT
6	HW/Edward request	Don't need VGA_PW_OK net		55	Delete net	2010 12/04	DVT
7	NVedia request.	NVedia request.	0.2	55	change PR201 to SD034107280. change PR198 to SD034226180 chnage PR205 to SD034133280. Change PR219 to SD034374280	2010 12/10	DVT
8	HW request.	to adjust power sequence to modify.	0.2	52 53	Change PR92 to SD034510380, remove PR94 SD028100480 Change PR116 from SD034249280 to SD034100380.	2010 12/10	DVT
9	Sourcer request.	Change to a normal part.	0.2	54	Change PC138 from SE00000R700to SE095224K00	2010 12/10	DVT
10	EMI request	For ISN issue, add solution on charger and CORE power	0.3	48,54	Add PL16 PC19 PC109 PC80 PC51 PC120 PC81	2010 01/17	PVT
11	EMI request	For ISN issue, add solution on charger	0.3	48	Change PL2 to SH162100M10 (4.7U to 10U)	2010 01/17	PVT
12	TI concern charger IC will be lauch	Negative current reaches 110mV on low side Rdson Charger IC will be lauch	0.3	48	Change PC38 to SE026104K80 (2.2U to 0.1U)	2010 01/23	PVT
13	RT8209 footprint issue	The footprint pad is too short, It will happen SMT problem	0.3	51 53	Change PU5, PU9 footprint to TPS51117RGYR_QFN14_3P5X3P5	2010 01/23	PVT
14							
15							
16							
17							

Security Classification: Compal Secret Data
Issued Date: 2010/04/12 Deciphered Date: 2010/10/12

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Version Change List (P. I. R. List) Page 1

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	Memo	2010/11/25	Compal	Bom structure error.	Correct LED1,LED2,LED5 bom structure to JM@	Rev02
2	27~30	Memo	2010/11/25	Compal		Change X76289BOL05(VRAM P/N) from SA00003MQ60 to SA000047Q20 Change X76289BOL06(VRAM P/N) from SA00003VS10 to SA00003YO20	Rev02
3	42	Memo	2010/11/25	Compal	New Audio Codec IC	Change U29 from SA000034010 to SA000034020 Change R635 from 0.1ohm to 0 ohm	Rev02
4	41	LED	2010/11/25	Compal	Battery LED Color mistake	SWAP LED1,LED6,LED7,LED8,LED9 Pin 2 and Pin3 (Pin2-->BATT_AMB_LED#,Pin3-->BATT_BLUE_LED#)	Rev02
5	07	EDP	2010/12/08	Compal	Bom structure error.	Correct R70 bom structure to EDP@	Rev02
6	24	Rework instruction	2010/12/08	Compal	N12P-GV Strap sets up the mistake	a. Pop R382, Depop R388 (ROM_SO: pull up 10K ohm) b. Pop R380, Change R380 from 15k to 45k. Depop R386.(STRAP2: pull up 45K ohm.) c. Pop R760, Change R760 from 10k to 5k.(STRAP3: pull down 5K ohm.) d. Pop R756. (STRAP4: pull down 10K ohm.) e. Pop R578. (STRAP_REF2, need to stuff with 40K ohm 1%.) f. Pop R757. (PGOOD (pin E7) stuff 10K ohm.)	Rev02
7	05	XDP	2010/12/08	Compal		Depop XDP component	Rev02
8	07	EDP	2010/12/08	Compal	Bom structure error.	Correct R70 bom structure to EDP@	Rev02
9	15	PCH	2010/12/08	Compal		Change R244.1 net name from PCH_RSMRST# to PCH_RSMRST#_R Pop R223,Depop U5 Delete R231(0 ohm) between SUSACK#_R and SUSWARN#_R Add T90 test point for SUSACK#	Rev02
10	17	PCH	2010/12/08	Compal		Delete VGA_ON for PD only. Change PR3.2 to PCH_GPIO53 Delete R257 Change U6.U7 to SA00000OH00	Rev02
11	18	PCH	2010/12/08	Compal	Power sequence for DGPU_PWROK after 1.5VSDGPU	Add Q75,Q74,R841	Rev02
12	22	GPU	2010/12/08	Compal		Change R342.1 from R762.2 to R762.1(NV_PERFORMANCE_R)	Rev02
13	26	GPU	2010/12/08	Compal	Bom structure error.	Correct C381 & C857 bom structure to OPT@	Rev02
14	31	LVDS	2010/12/08	Compal	For LCDVDD rise time sequence issue	Change R468 from 1k to 100k Change C481 from 0.047u to 0.47u PCH_LCD_CLK & PCH_LCD_DATA,Pull high at PCH side. Add R832 between +3VS and JLVDS1.31.	Rev02
15	32,33	CRT.HDMI	2010/12/08	Compal		D8, D9 change material to SCS00003600	Rev02
16	33	HDMI	2010/12/08	Compal		Pop R502.Depop D9 SDVO_CTRL.DATA strap pull high at PCH side	Rev02
17	34.44	ODD.USB3.0	2010/12/08	Compal		Change Q31.Q63.Q71 to SB000008J10	Rev02
18	35	LAN	2010/12/08	Compal	Auto power on issue	Change R541.2 net name from PCH_PCIE_WAKE# to LAN_WAKE#. Pop R541	Rev02
19	35	LAN	2010/12/08	Compal		Change C583 from 27 to 15P Change C582 from 27to 18P Change Y4 from CL(20P)to CL(12P) Add Q76 and Depop R555	Rev02
20	36	Transformer	2010/12/08	Compal		Change T63 from SP050003T10 to SP050003T20	Rev02

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
21	36	LAN	2010/12/08	Compal		L31 update CIS Symbol and PCB footprint	Rev02
22	37	3G	2010/12/08	Compal	3G Power noise	Delete L49.L50.R764.R765.R766.R767.U43.C852.C853.CR781.Q69.C856.C854. C855.C851.R572.R782 Change J3G1 Pin 2.4.6.8.10 to +3VS Change R572.3 to +3VS Change J3G1.30 to +VSB Change J3G1.17 to EC_SIM_DETECT#	Rev02
23	37	D_Door switch	2010/12/08	Compal		Add R838,R839 Depop R838 Pop R839	Rev02
24	38	Card Reader	2010/12/08	Compal		Change R590,R591 to 22ohm Change C635,C636 to 10P Add R833 between +3VS and +3VS_CARD	Rev02
25	39	EC	2010/12/08	Compal		Change R621 from 0ohm to 8.2k(Board ID) Add C863	Rev02
26	40	TP	2010/12/08	Compal	TP Pin define issue	Change JTP1 Pin define (Pin-->GND,Pin2-->RIGHT_BTN#,Pin3-->LEFT_BTN#,Pin4-->TP_DATA, Pin5-->TP_CLK,Pin6-->+5VS) Change JTP2 Pin define (Pin-->NC,Pin2-->GND,Pin3-->TP_CLK,Pin4-->TP_DATA,Pin5-->PWM,Pin6-->+5VS) Add C864	Rev02
27	40	Power Button	2010/12/08	Compal		Change R622.2 from +3VALW to +3VALW_EC	Rev02
28	40	Reset Button	2010/12/08	Compal	Reset system by mainpower and BI	Add R844,R836.R837.Q72.Q77 Change R836 to 1K Change R837 to 10K	Rev02
29	41	Power board	2010/12/08	Compal		Change JPWR2.5 from NC pin to BI_R (SJM D_door) Change LID_SW# from LED board(JLED1.8) to Power board(JPWR1.2)	Rev02
30	42	HD Audio Codec	2010/12/08	Compal	Fix HP/MIC Detect issue	Change R649 from 39.2k to 10k Change R650 from 10k to 39.2k	Rev02
31	42	HD Audio Codec	2010/12/08	Compal		Change C704.C705 to SE107225K80 Delete R637.R638.Q39.Q38.R634. R636.R639.R640.J2 Change power from +3VS to +3VS_CODEC. Add R834	Rev02
32	43	Headphone Out/SPDIF	2010/12/08	Compal	HP right and left channel inverse issue	Change R735.1 to HP_RIGHT Change R734.1 to HP_LEFT SWAP JHP1.3 and JHP1.8 (Pin8-->SPDIF_OUT and Pin3-->+5VSPDIF)	Rev02
33	43	Digital MIC	2010/12/08	Compal		Delete R666.R668 Add L50,L51 300ohm bead(SM010017710)	Rev02
34	44	USB3.0	2010/12/08	Compal	Modify SMI circuit for leakage issue	Delete R797,R830 Add R840,Q73.Q71	Rev02
35	44	USB3.0	2010/12/08	Compal		Change c792.c793 from 12P to 15P	Rev02
36	45	USB3.0	2010/12/08	Compal		Delete D46 Change C780 from SGA19151410(D size) to SGA00002N80(B2 size) Depop U41,C204,R754 Add R842,R843	Rev02
37	45	Screw Hole	2010/12/08	Compal		Change H4 from H_3P0 to H_3P3 Change H8 from H_3P0 to H_3P0x5P0 Delete H25	Rev02

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38	46	DC Interface	2010/12/08	Compal		a.+5VS (Change R679 from 20K to 100K) b.+3VS (Change R685 from 47K to 200K) c. +1.5VS (Change R692 from 200K to 750K)	Rev02
39	13~21	PCH	2010/12/08	Compal		Change U3 from SA00004EE10 to SA00004EE40	Rev02
40	38	Caed Reader	2010/12/08	Compal		Change R587 from SD028330A00 to SD028330A80	Rev02
41	20.34. 35.36.42	Capacitor	2010/12/08	Compal		C226, C540, C549, C566, C573, C576, C580, C590, C712 change material to SE000000K80	Rev02
42	24	GPU	2010/12/10	Compal	Update N12P-GV QS DevID: 0x1050	1. ROM_SCLK: pull up 5K ohm. 2. STRAP2: pull down 5K ohm. 3. ROM_SO: pull up 10K ohm.	Rev02
43	44	USB3.0	2010/12/20	Compal	USB driver can't install issue	Change Q73.2 from +3V_USB3.0 to +3V_USB3 Pop R840	Rev03
44	31	CMOS Camera	2010/12/29	Compal		Add R845,Delete R832	Rev03
45	39	BI	2011/01/03	Compal	TI charger short protection prevent	Add R848	Rev03
46	40	TP	2011/01/03	Compal		Change SW2.SW3 from SN111002700 to SN100000K00	Rev03
47	41	LED	2011/01/12	Compal		Change R625 from 3.9K to 680 ohm Change R626 from 2.2K to 390 ohm Change R739 from 3.9K to 390 ohm Change R740 from 100 to 3.3K ohm	Rev03
48	46	VGA_ON	2011/01/13	Compal	Restart dGPU loss issue.	Change R703 from 22K to 100K Add R849 (10K)	Rev04
49	19	CRT	2011/01/22	Compal	water ripple issue	Change L1 from SM01000AX00 to SHI00003Y00	Rev04
50	39	EC	2011/01/25	Compal		Delete U27	Rev0.5
51	41	BTN	2011/01/25	Compal		Change SW6 from SN100001C00 to SN100001D10	Rev0.5
52	39	Board ID	2011/01/27	Compal	Board ID version	Change R621 to 33K	Rev0.5
53	5	CPU XDP	2011/01/27	Compal		Delete C34.C35.Q1.R21.R24.JXDP1.R3~R16.R18~R22.R39~R41.R43.R45~R47.R53~R60 Add T94~T98	Rev0.5
54	40	TP	2011/01/27	Compal		Delete net name TP_PWM	Rev0.5
55	18	DGPU_PWROK	2011/01/27	Compal		Pop C872	Rev0.5
56	44	USB3.0	2011/01/27	Compal	For EEPROM (EON).	Pop R720	Rev0.5

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