

Compal Confidential

NAT02 M/B Schematics Document

Intel Clarkfield Processor with DDRIII + Ibex Peak-M + Madison Pro

2009-08-20

REV:0.1

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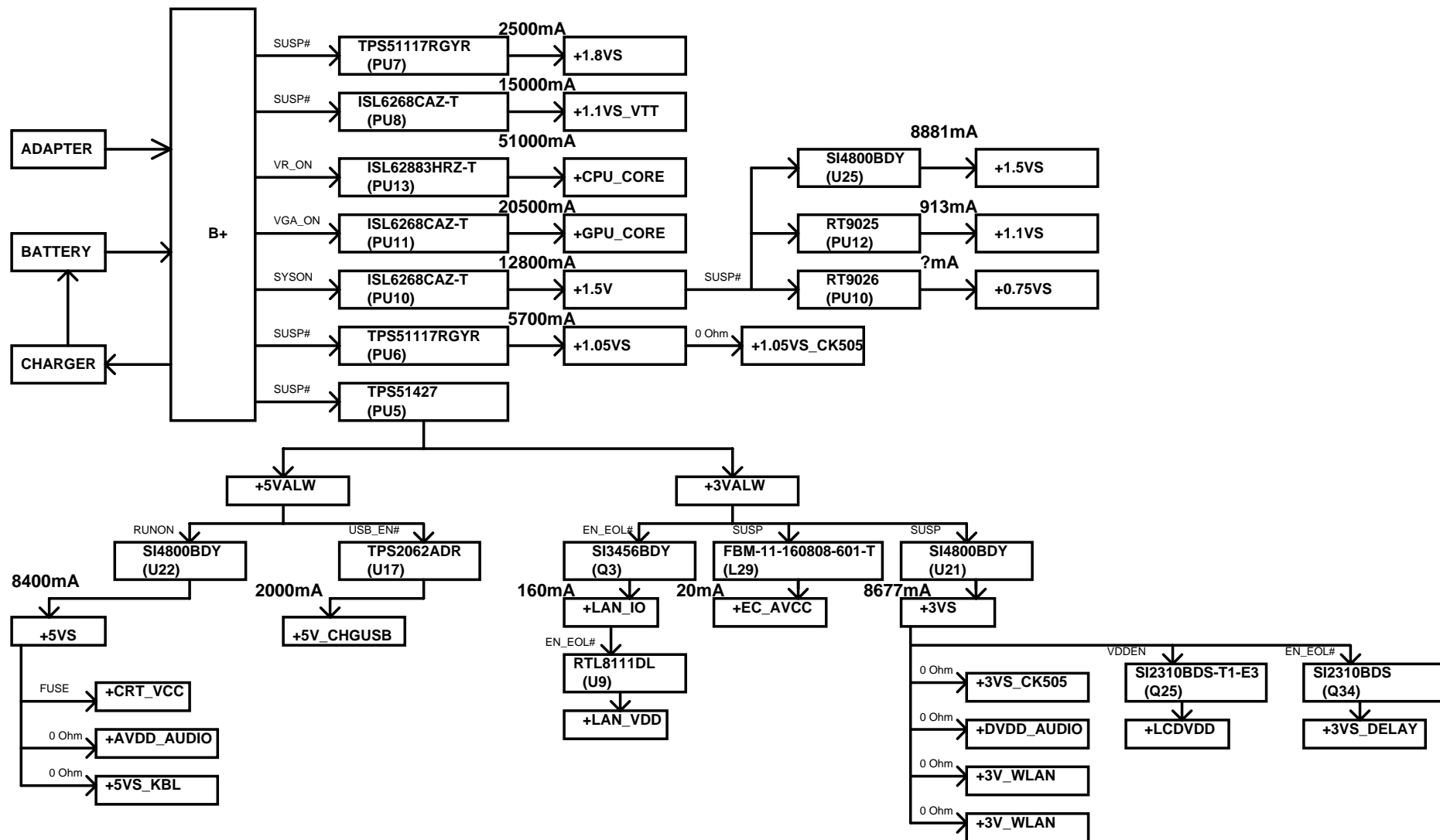
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Device	IDSEL#	REQ#/GNT#	Interrupts
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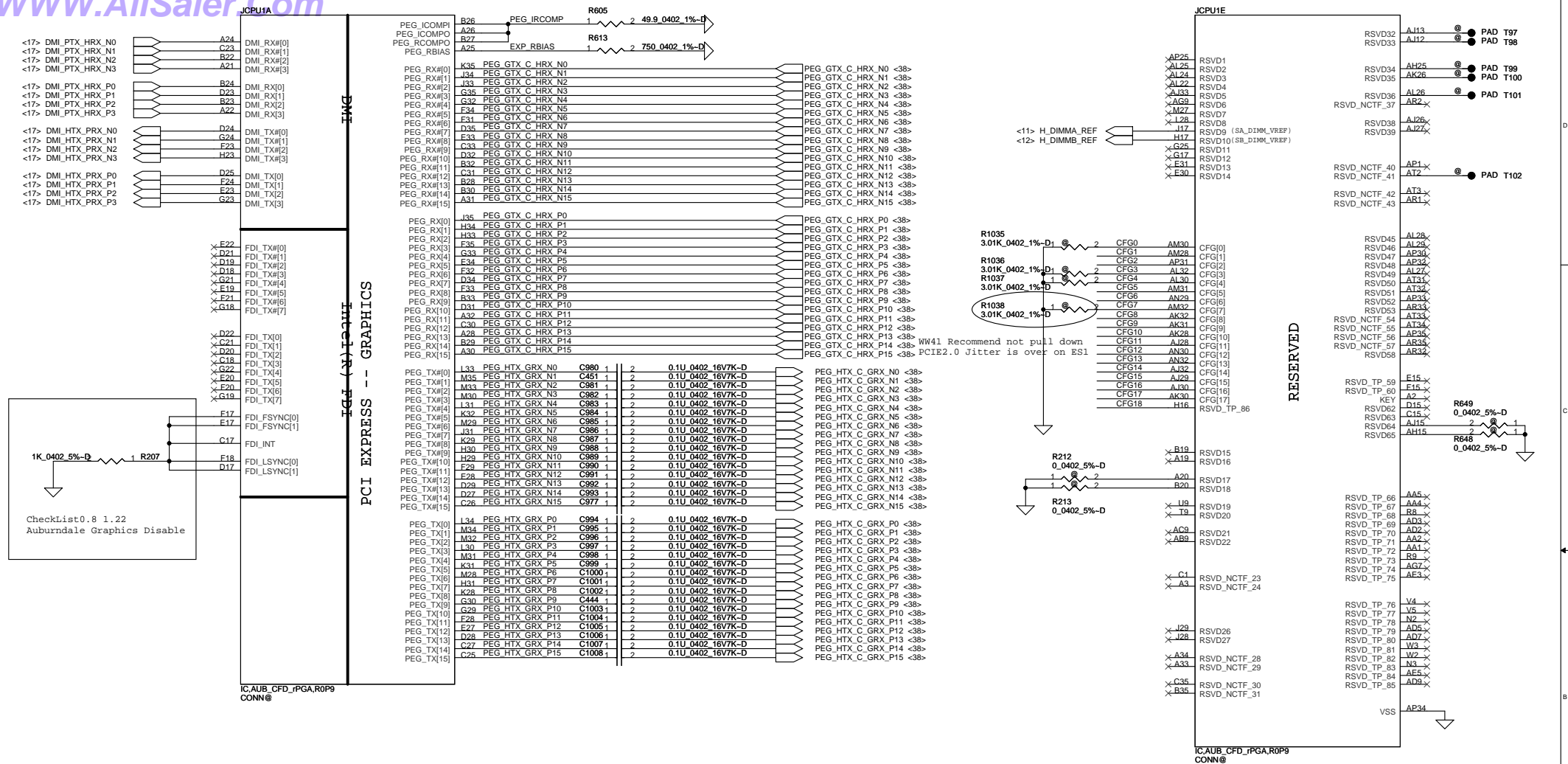
Board ID / SKU ID Table for AD channel

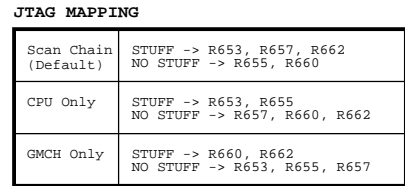
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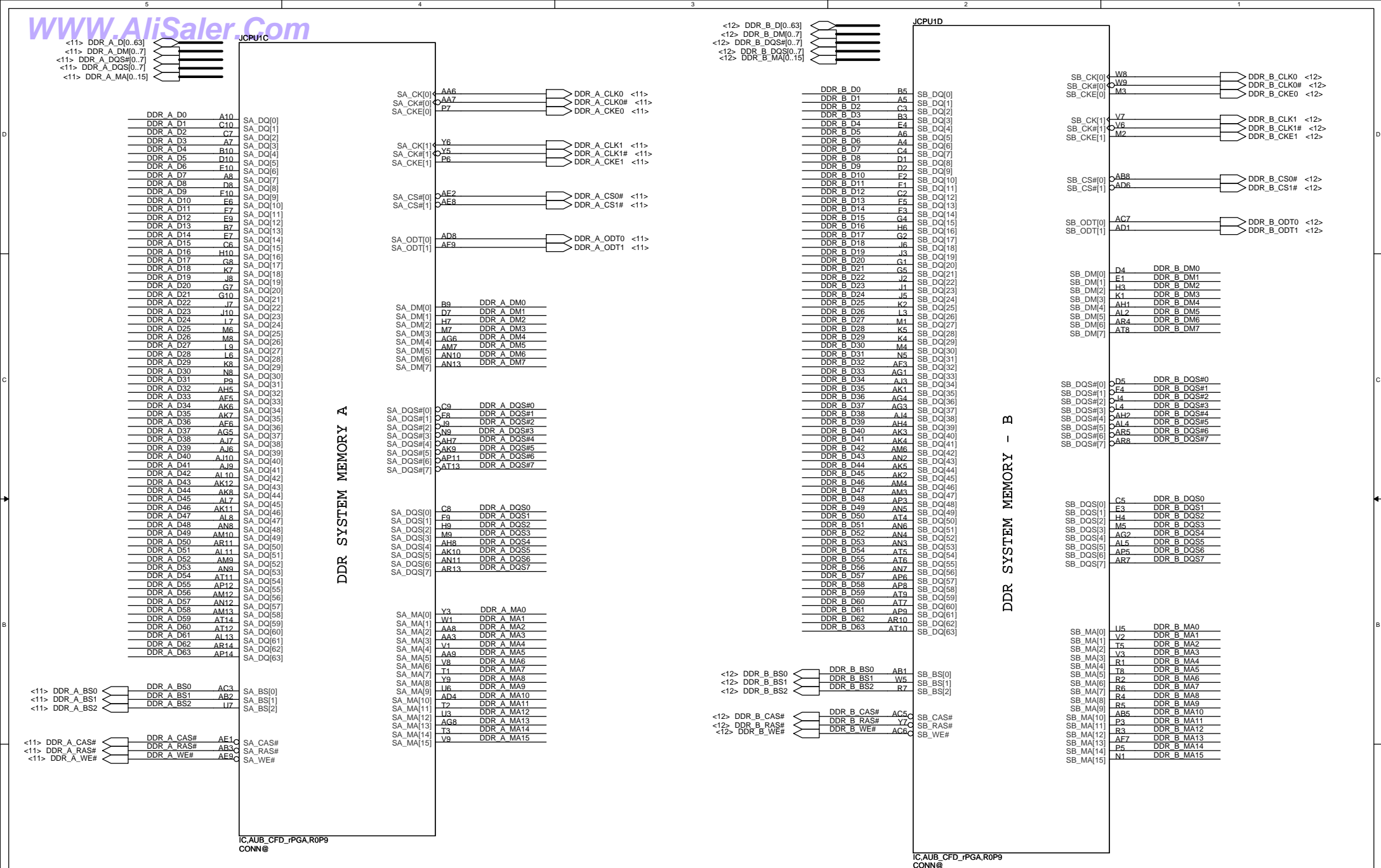
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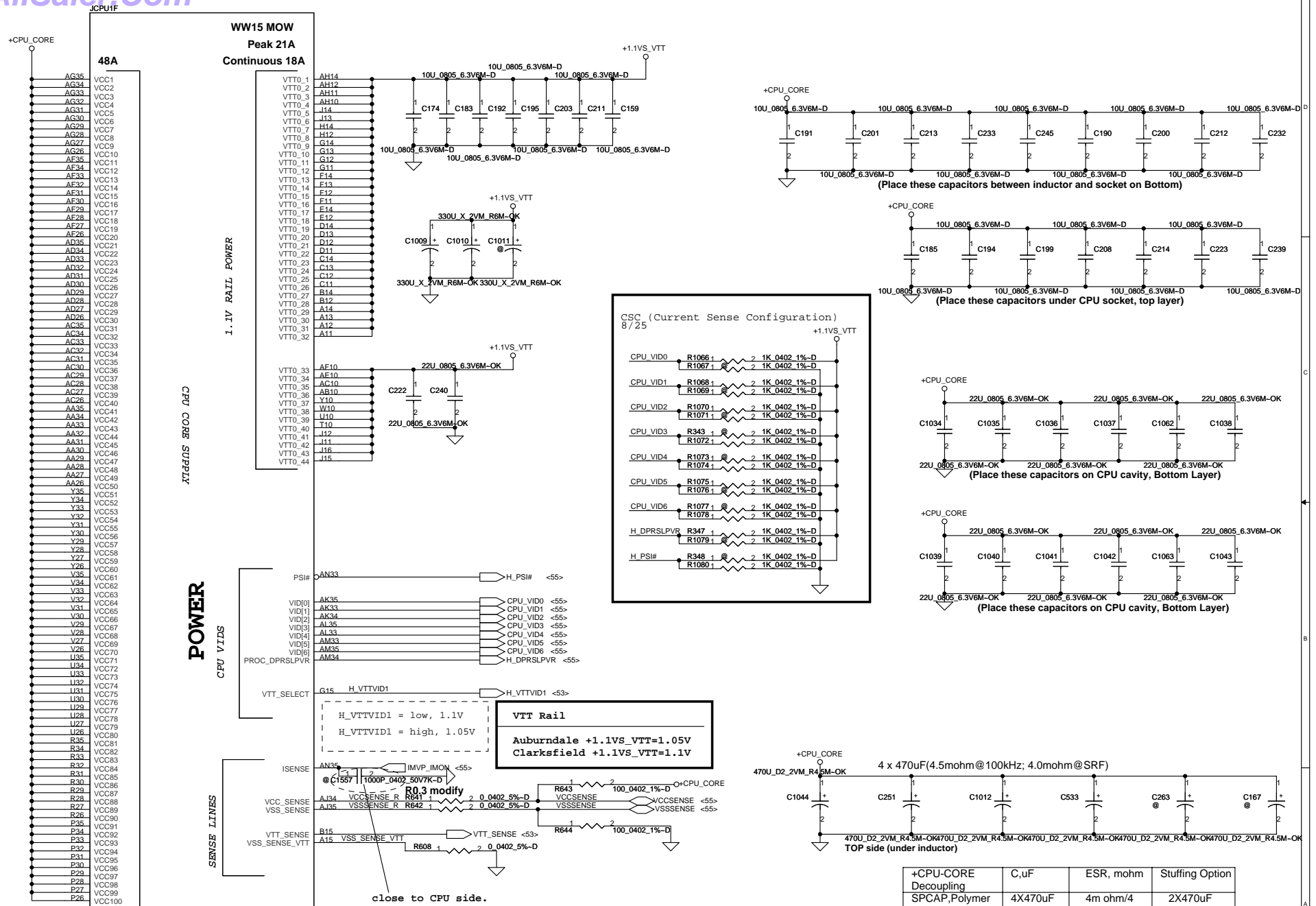
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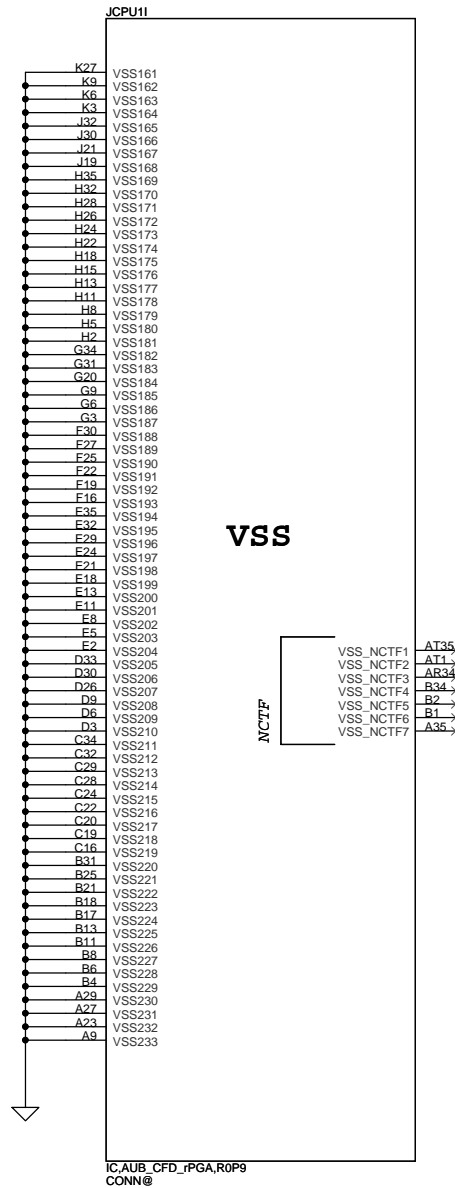
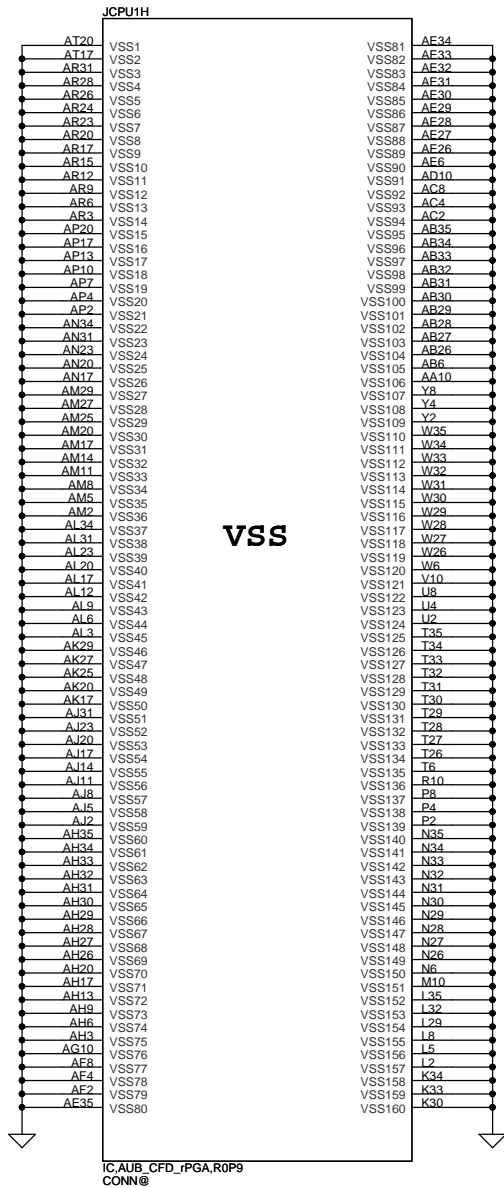


IC_AUB_CFD_PGA_R0P9
CONN@

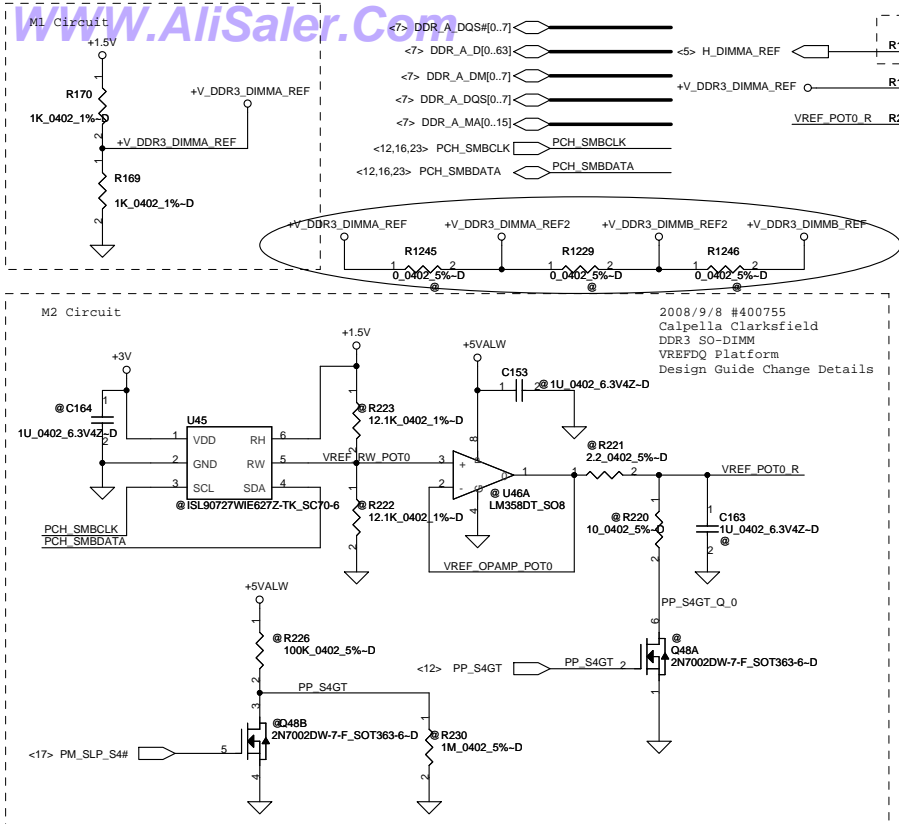
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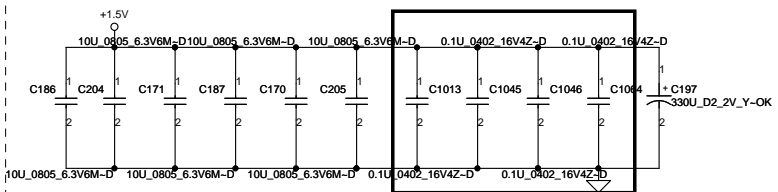


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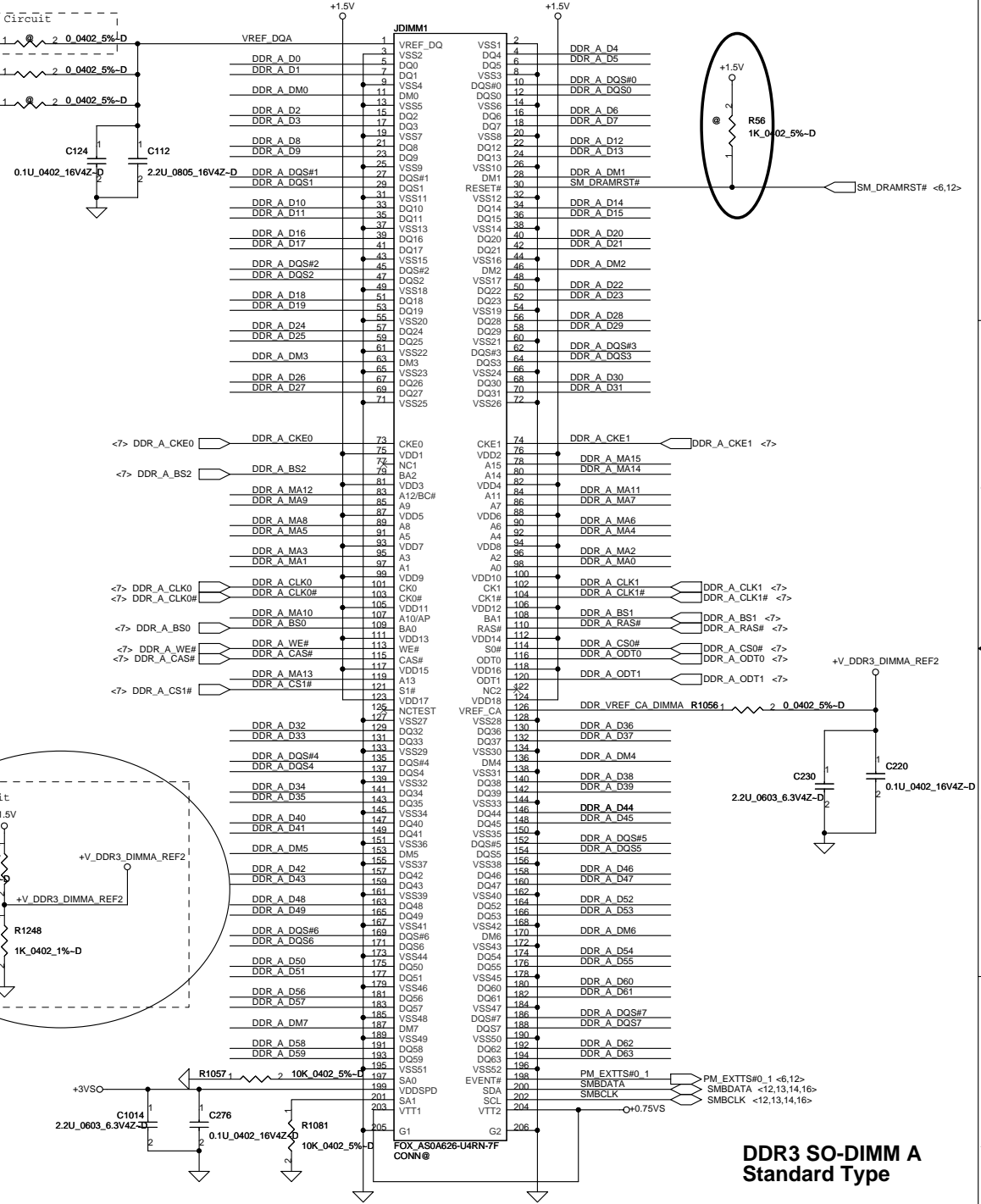
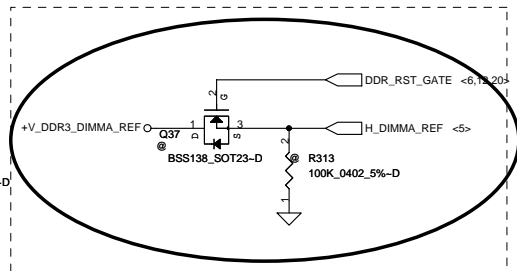
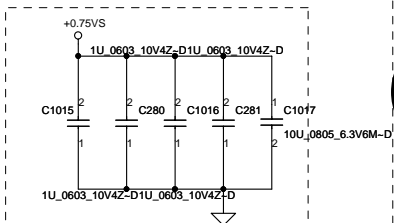


Layout Note:
Place near JDIMM1

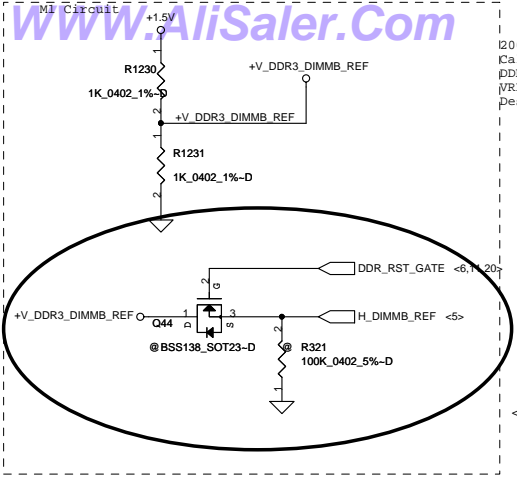
Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



Layout Note:
Place near JDIMM1.203 & JDIMM1.204

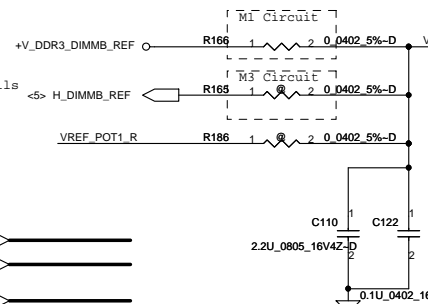


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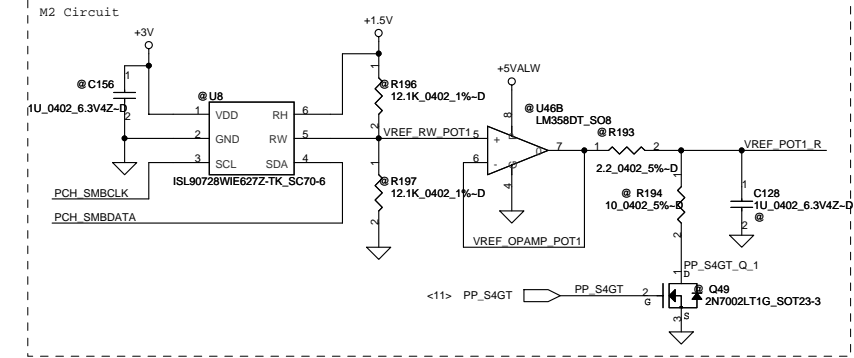
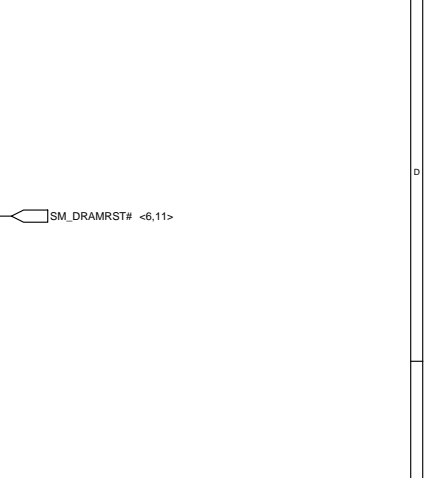
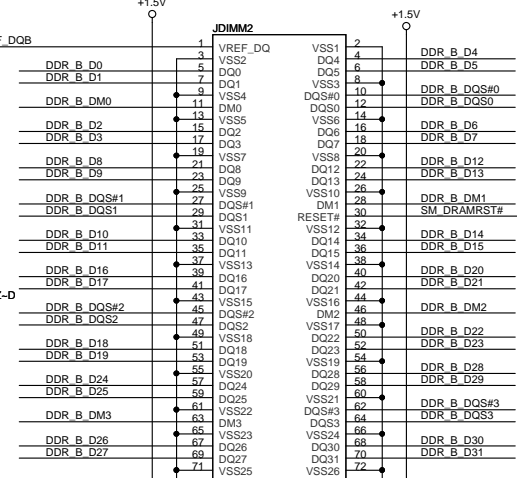


2008/9/8 #400755
Calpella Clarkfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

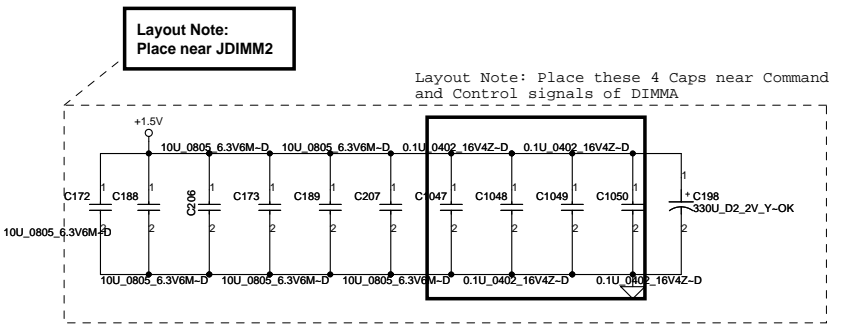
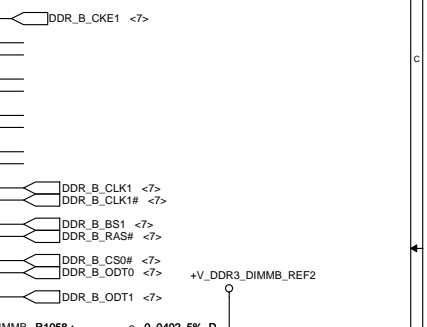
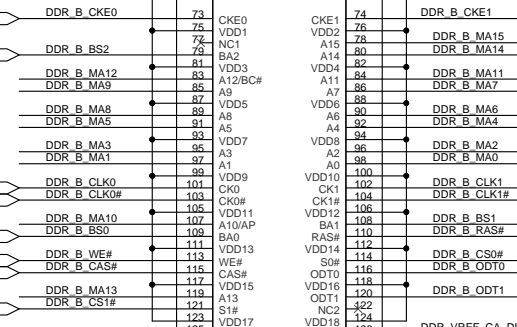
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- <7> DDR_B_DQ[0..63]
- <7> DDR_B_DM[0..7]
- <7> DDR_B_DQS#1[0..7]
- <7> DDR_B_MA[0..15]
- <11,16,23> PCH_SMBCLK
- <11,16,23> PCH_SMBDATA



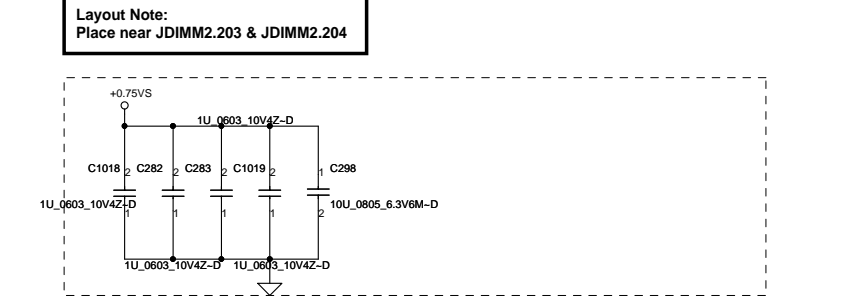
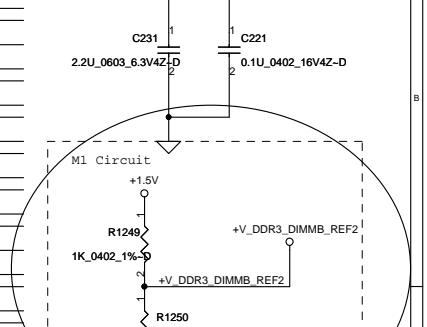
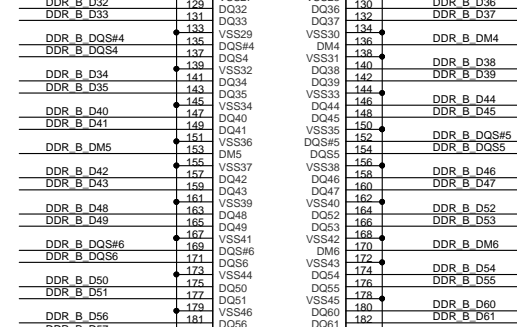
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- <7> DDR_B_CAS#
- <7> DDR_B_CS#



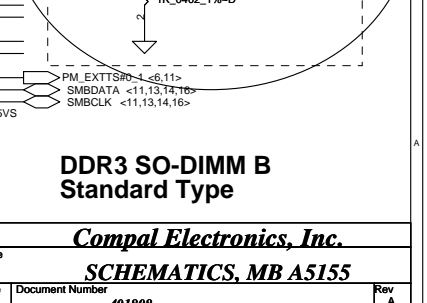
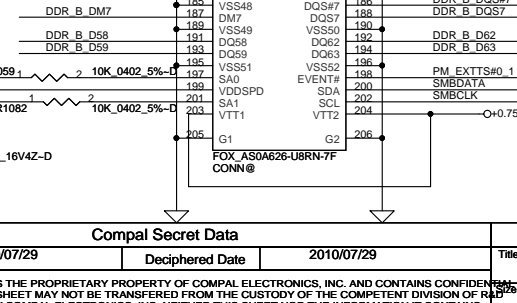
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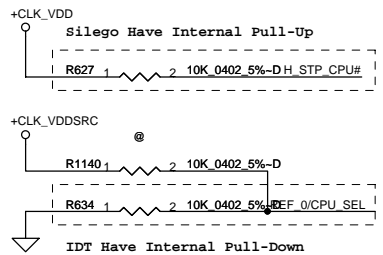
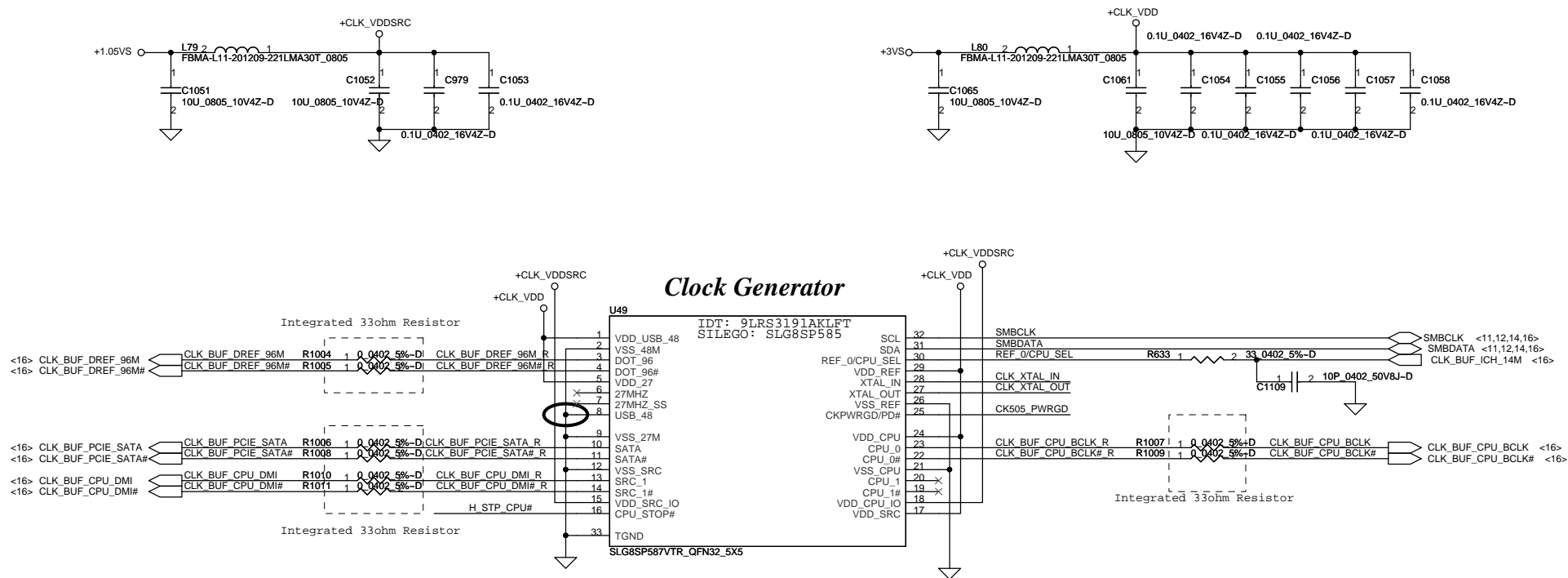


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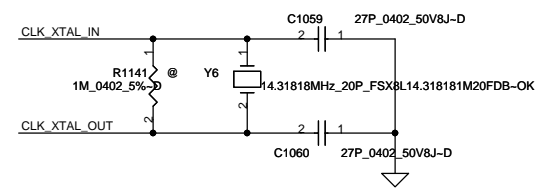
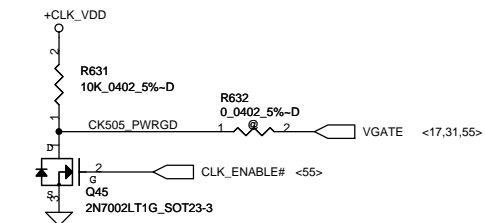


DDR3 SO-DIMM B
Standard Type

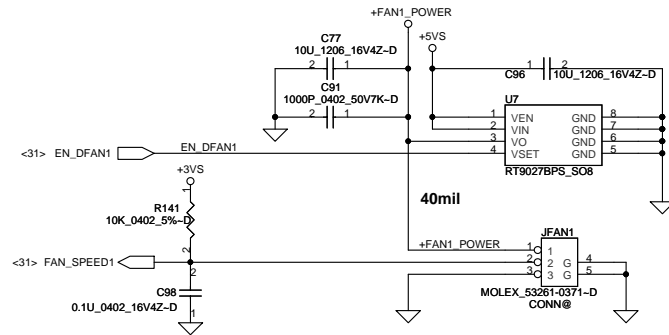
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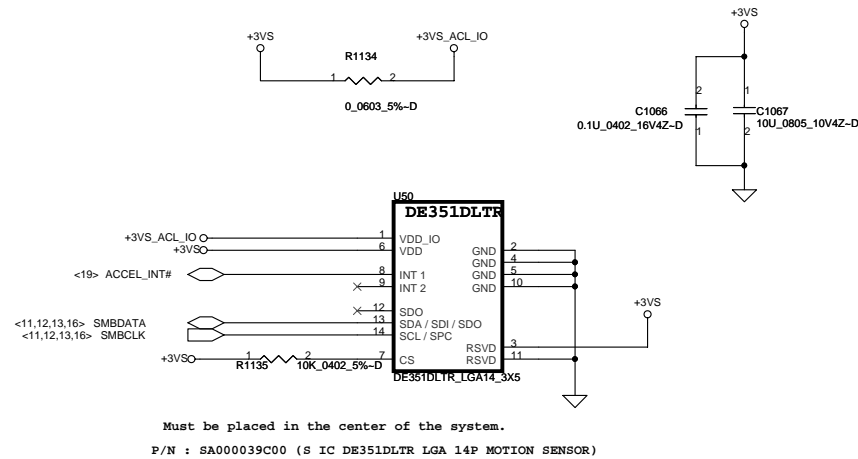
PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



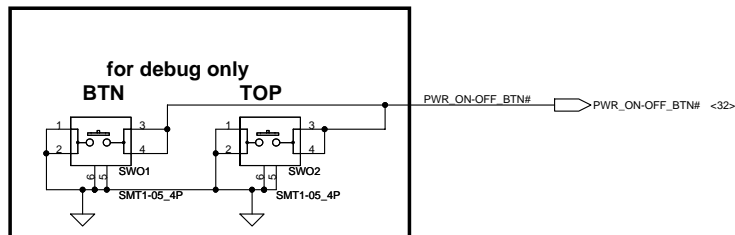
FAN Control circuit



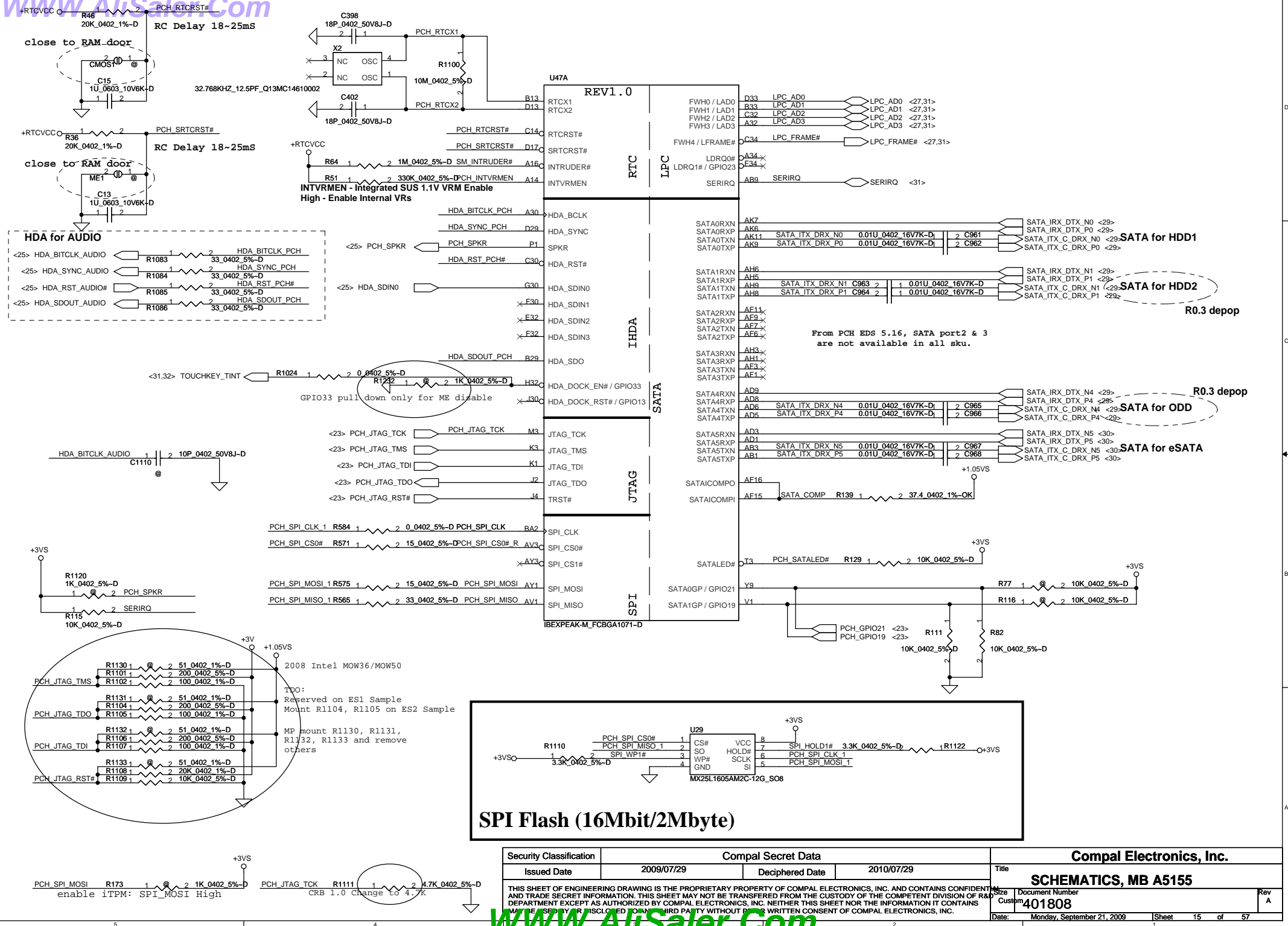
Free Fall Sensor



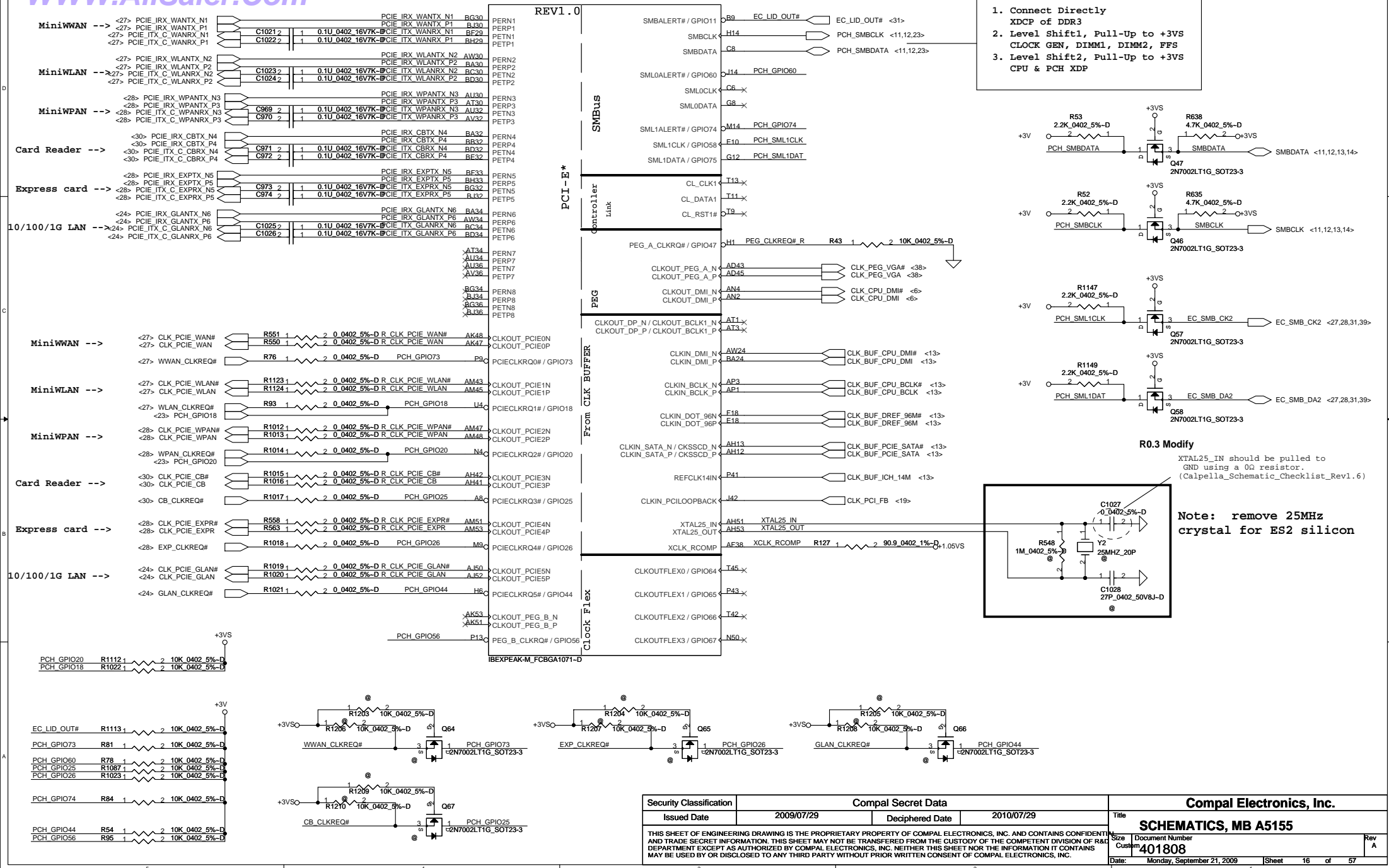
Power Button



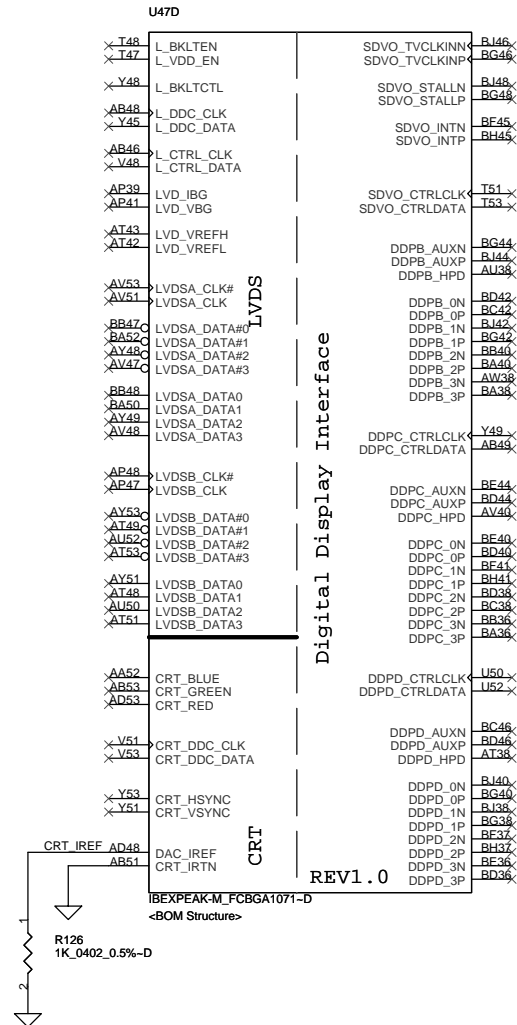
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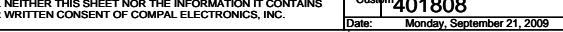
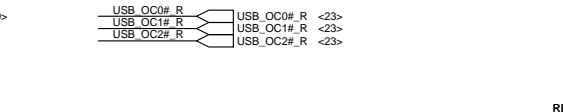
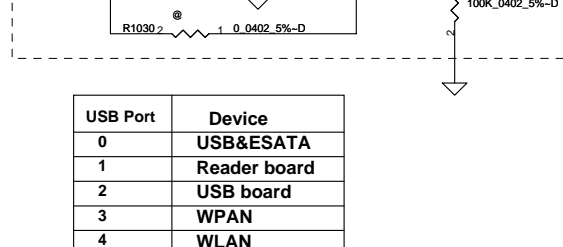
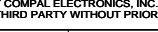
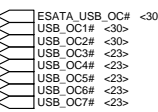
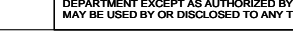
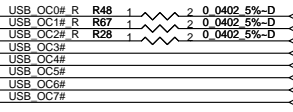
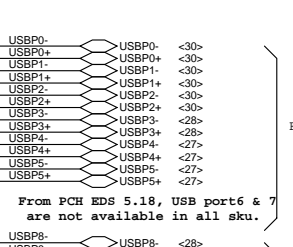
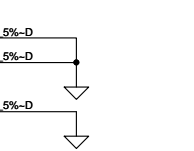
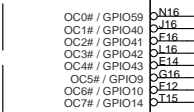
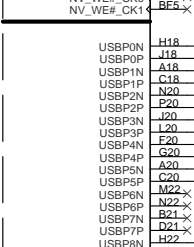
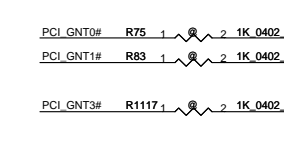
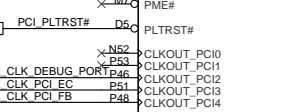
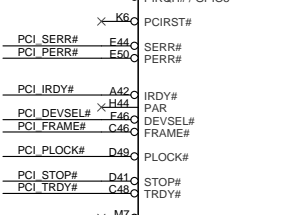
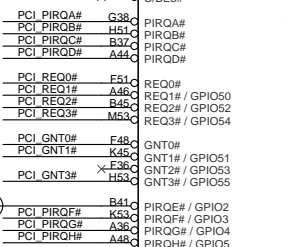
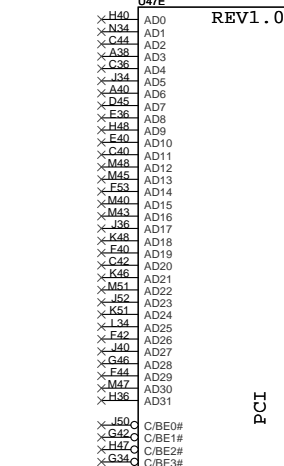
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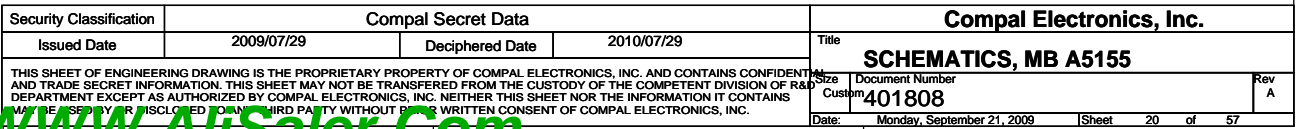


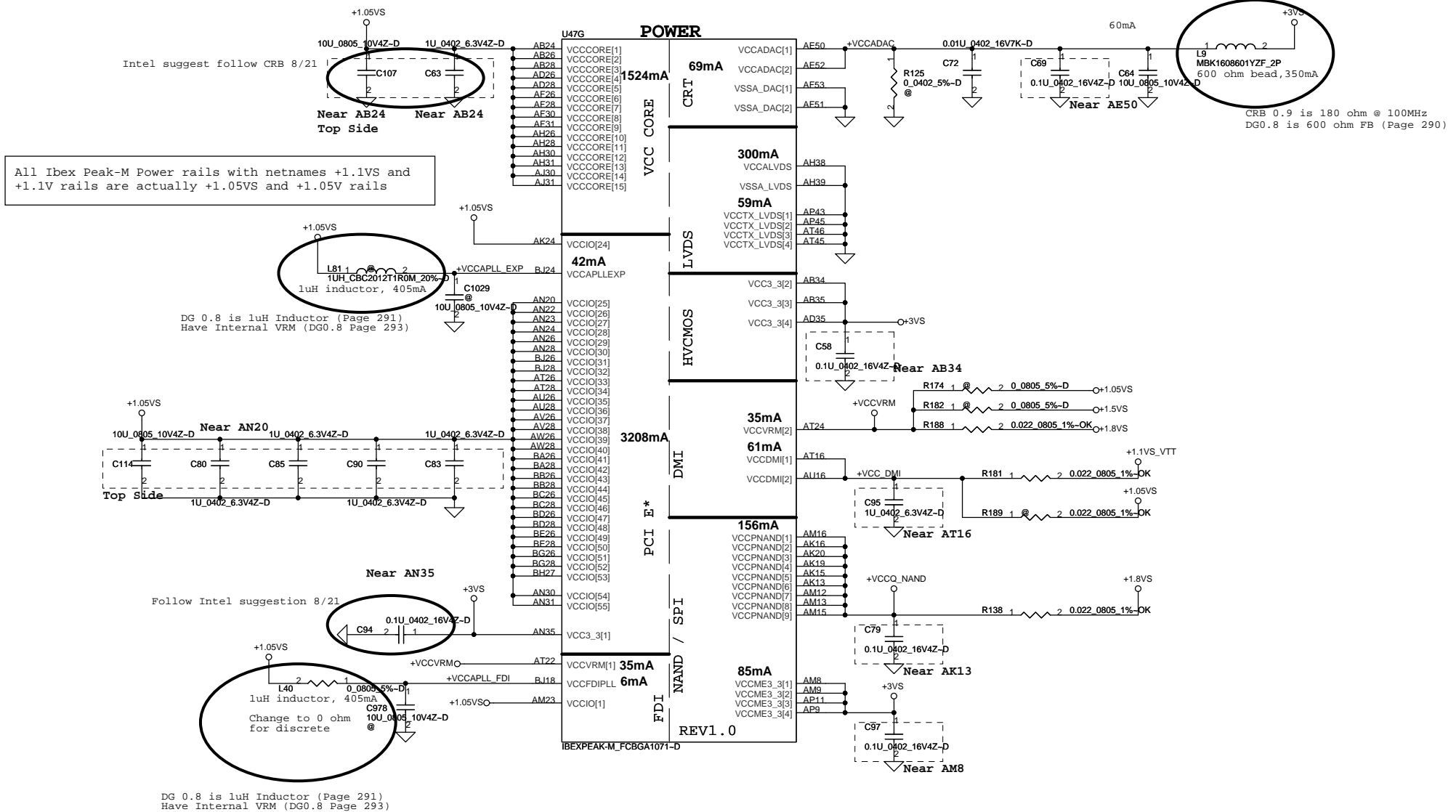
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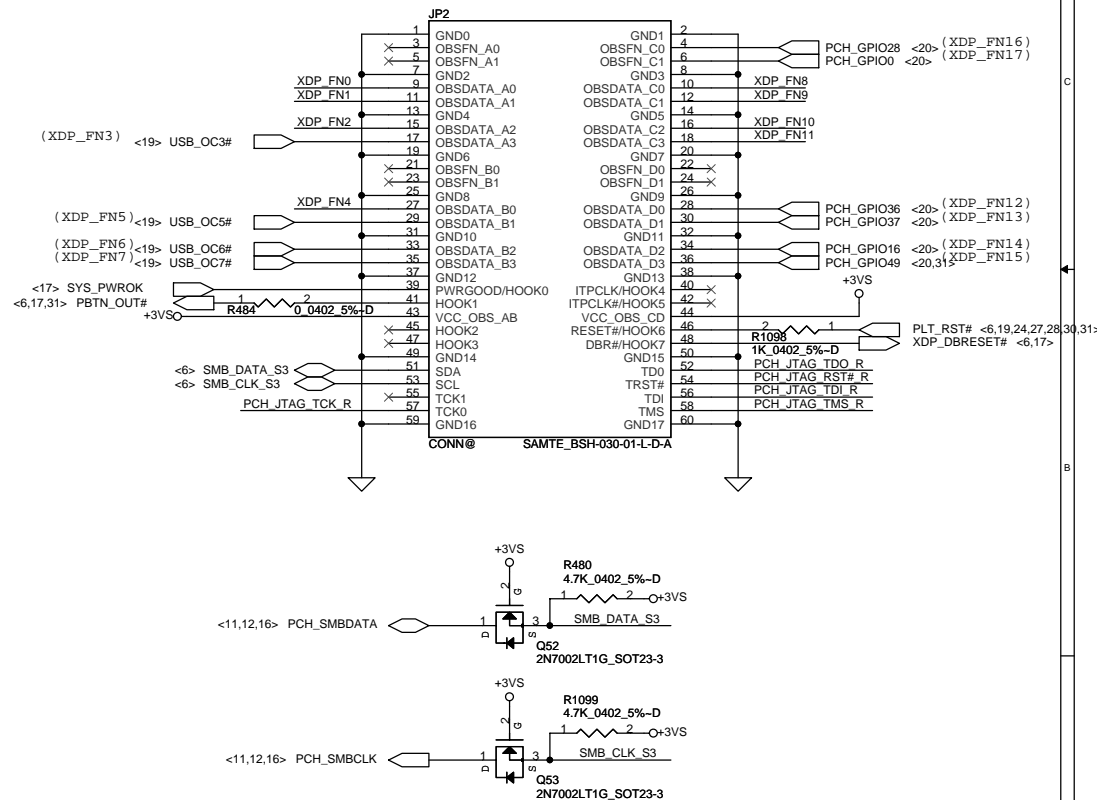
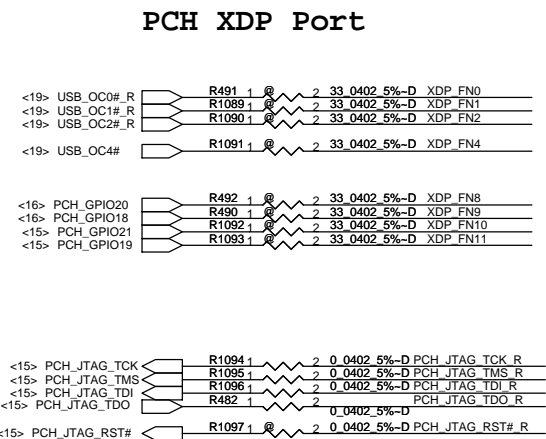
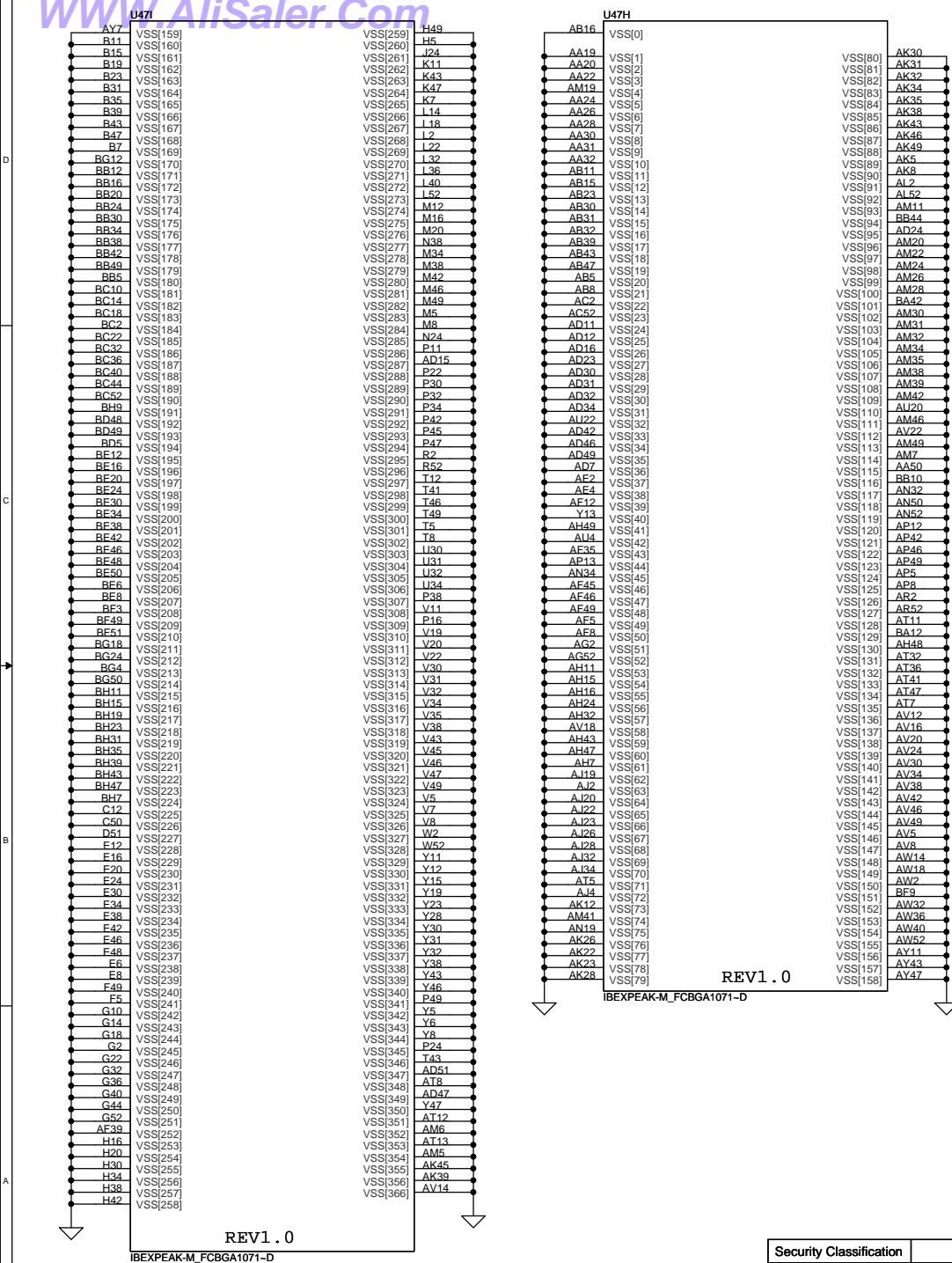




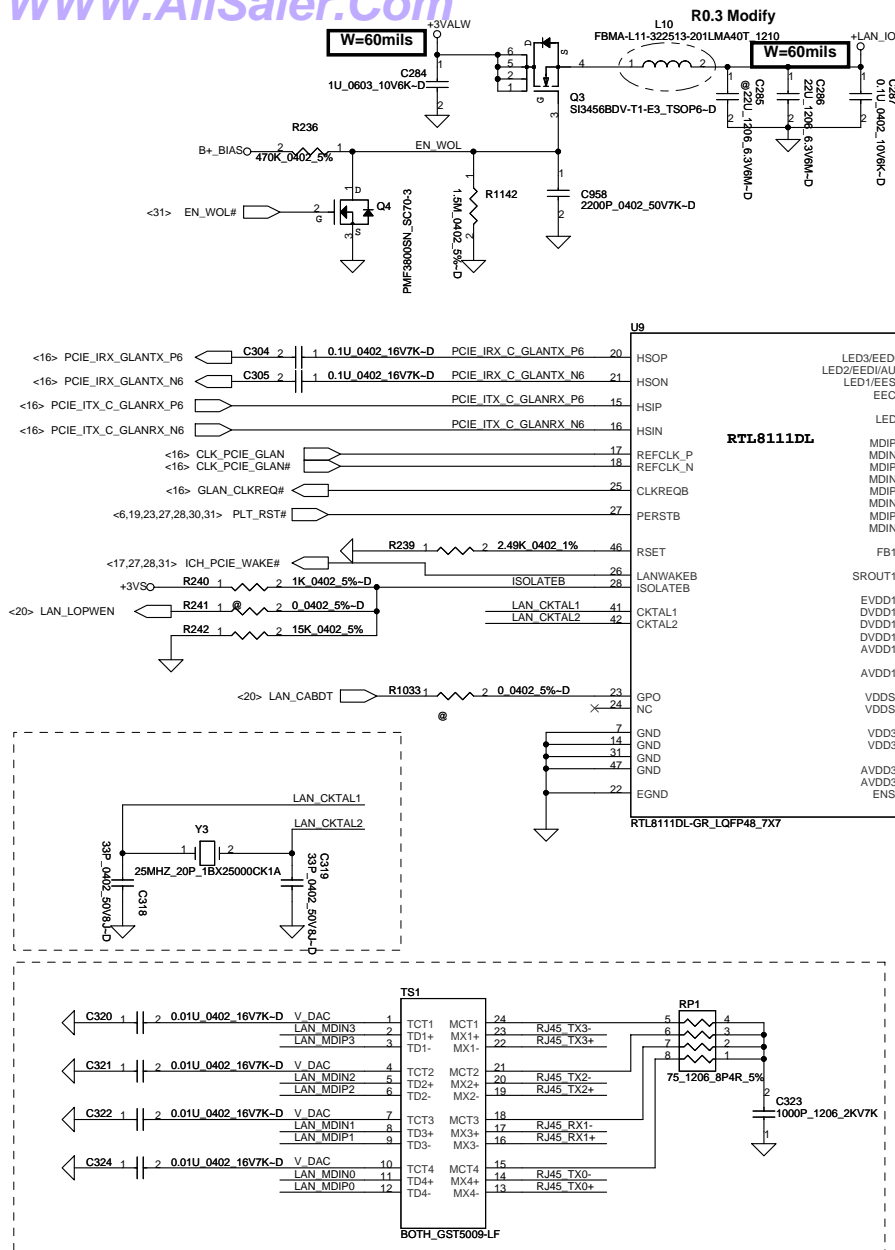
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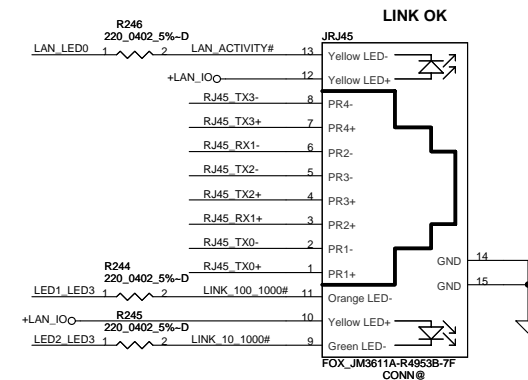
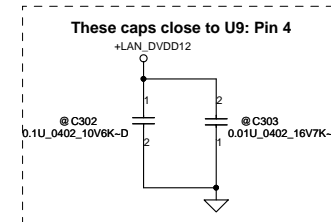
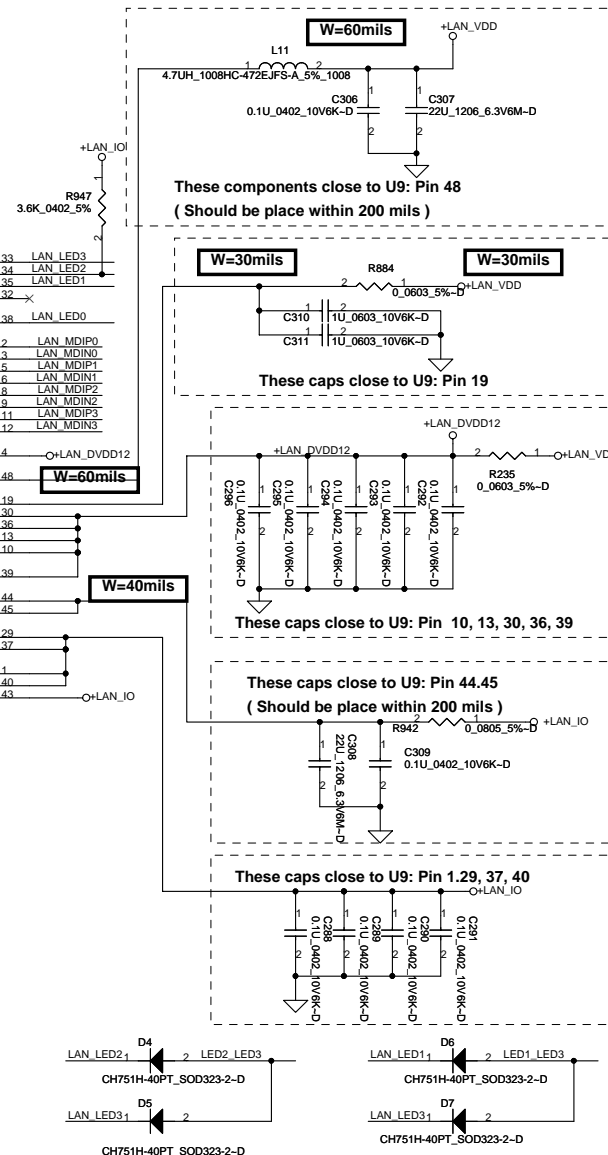
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				Size Custom 401808		
				Date: Monday, September 21, 2009 Sheet 23 of 57		

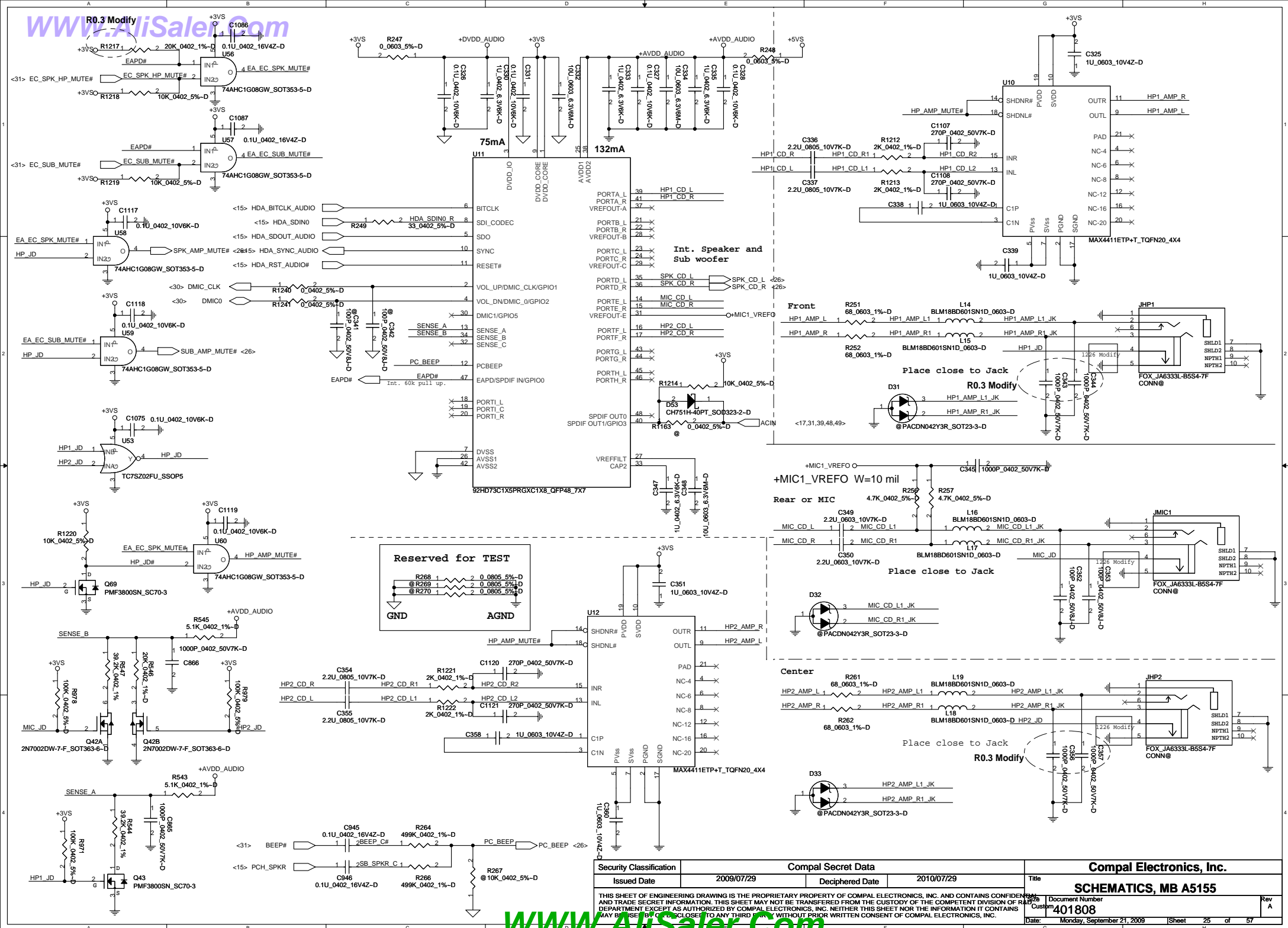


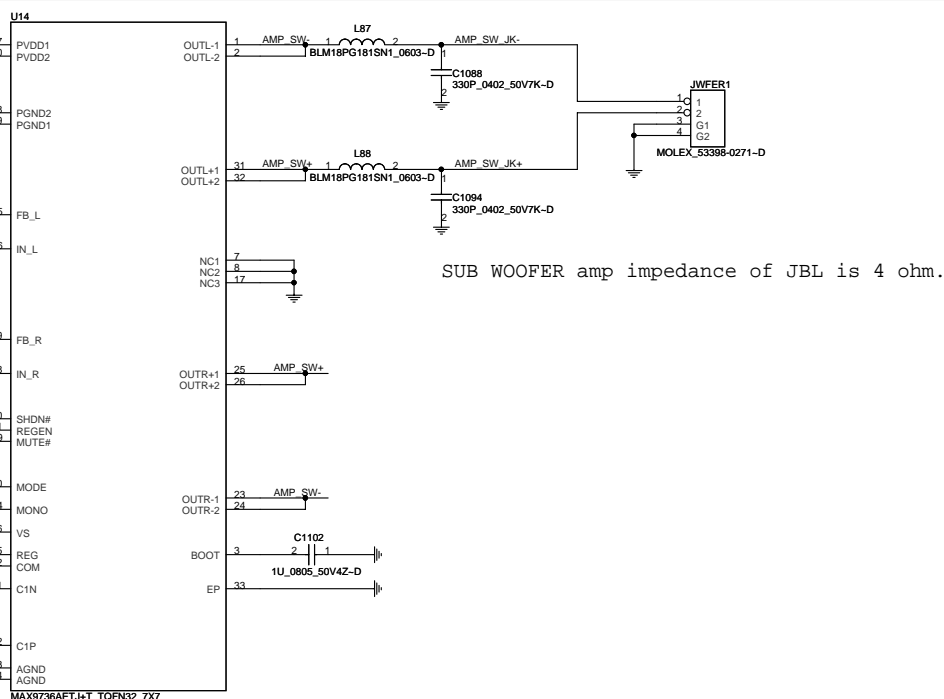
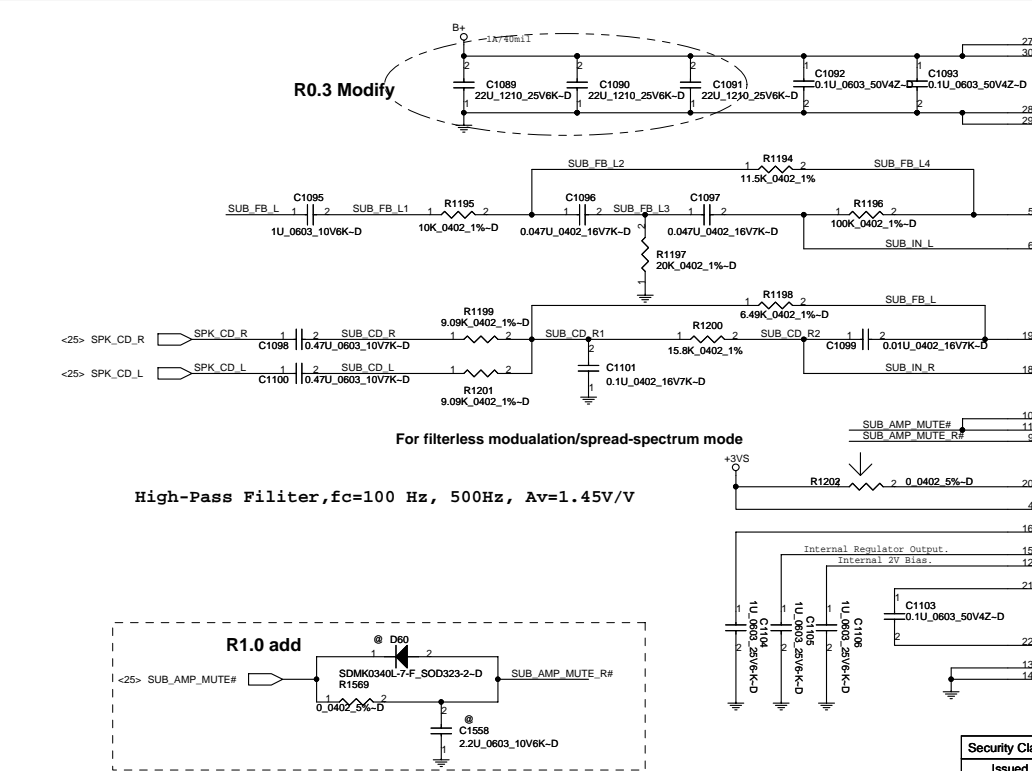
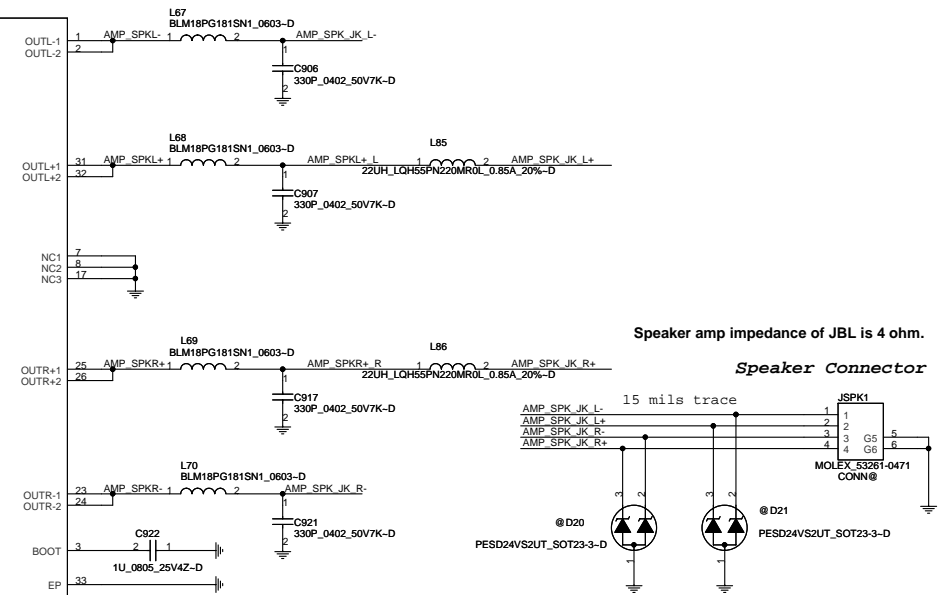
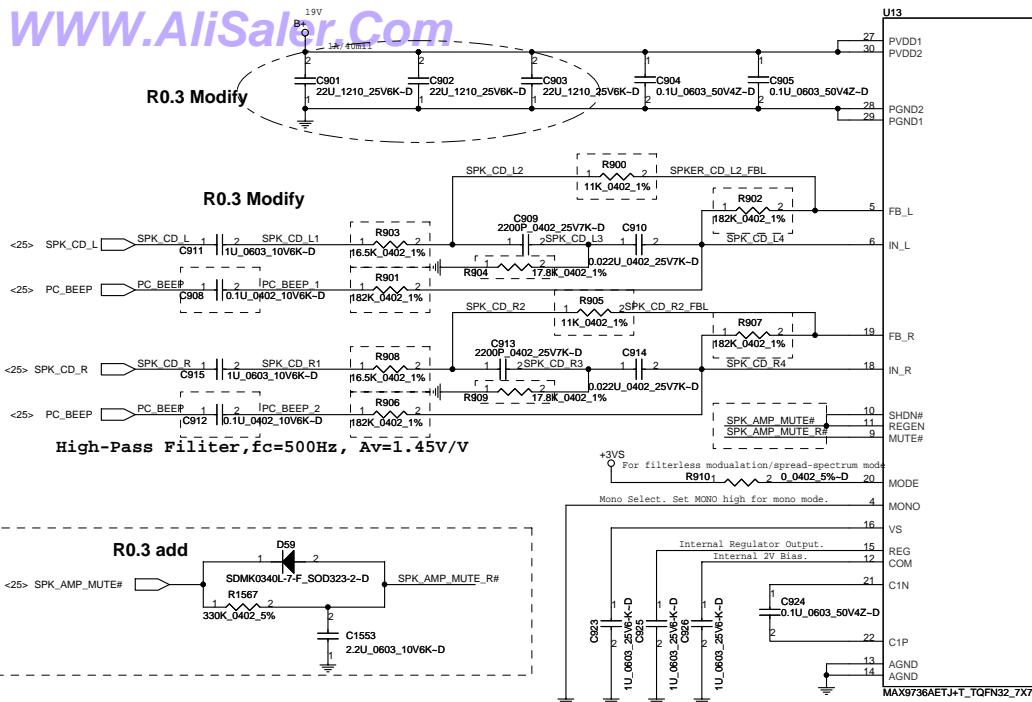
LEDS1-0	0 0	0 1	1 0	1 1
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 / 100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT



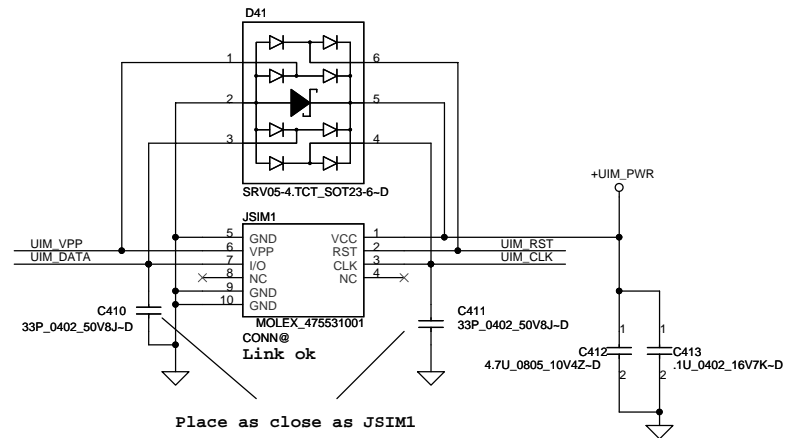
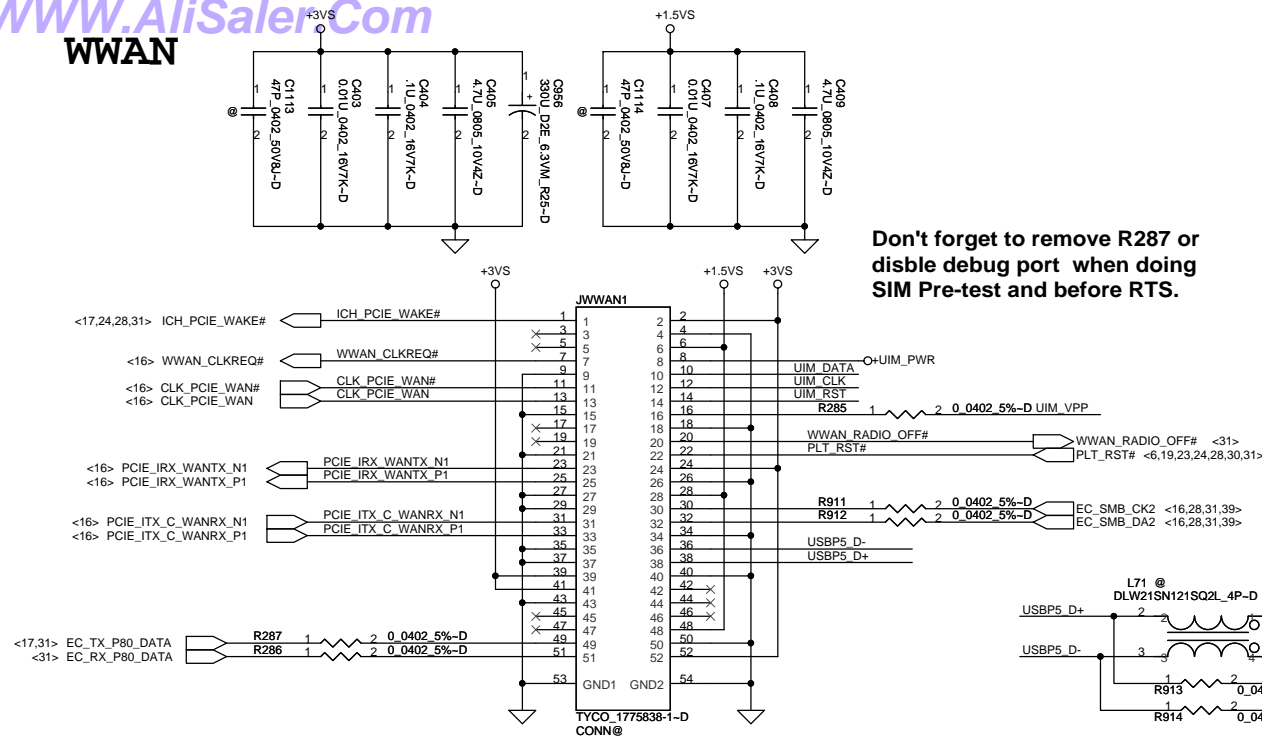
12/11 reserve for EMI as Dell Tony request

LAN MDIN3	C873	1	2	6.8PF	0402	50V9-D	
LAN MDIP3	C874	1	2	6.8PF	0402	50V9-D	
LAN MDIN1	C875	1	2	6.8PF	0402	50V9-D	
LAN MDIN2	C876	1	2	6.8PF	0402	50V9-D	
LAN MDIP2	C877	1	2	6.8PF	0402	50V9-D	
LAN MDIP1	C878	1	2	6.8PF	0402	50V9-D	
LAN MDIN0	C879	1	2	6.8PF	0402	50V9-D	
LAN MDIP0	C880	1	2	6.8PF	0402	50V9-D	

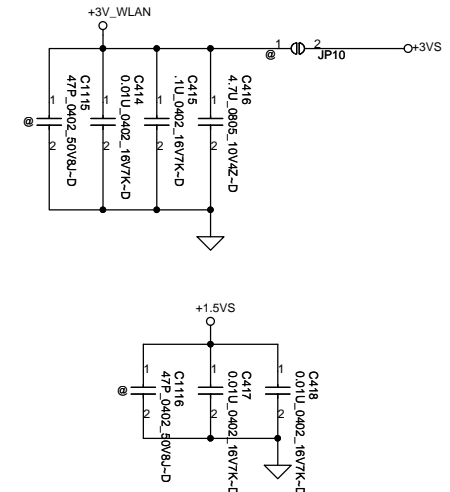
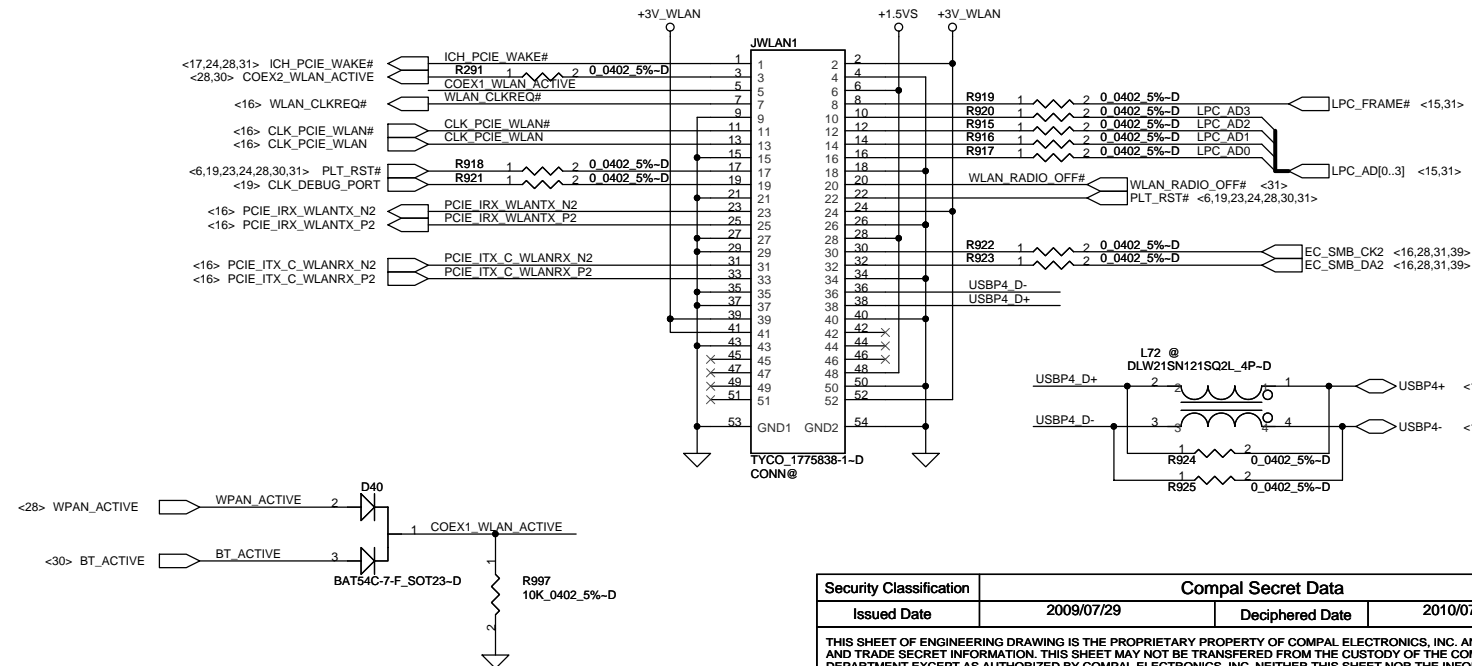




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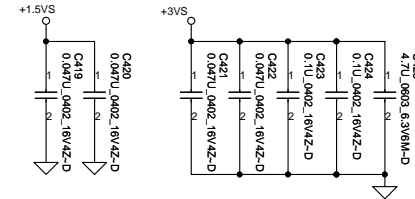
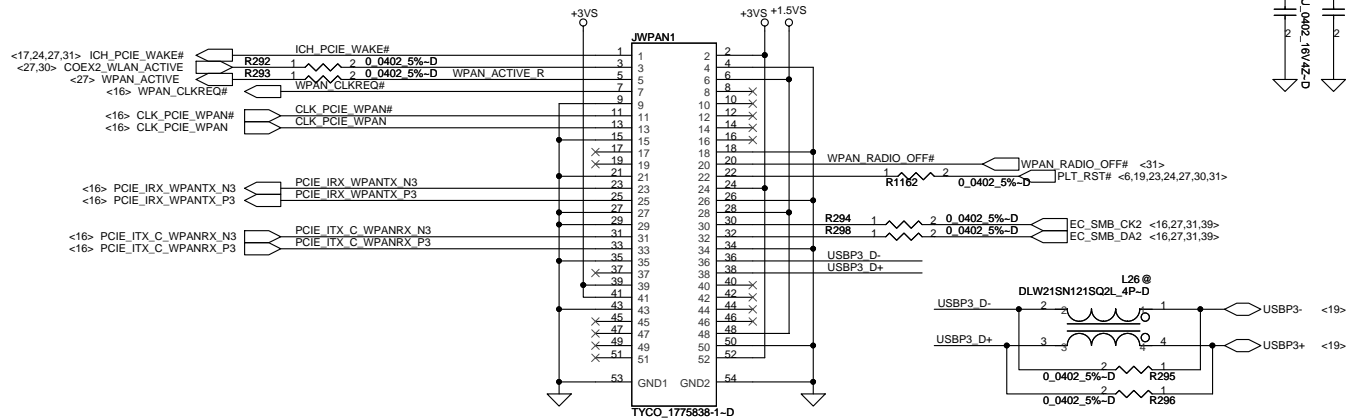


WLAN

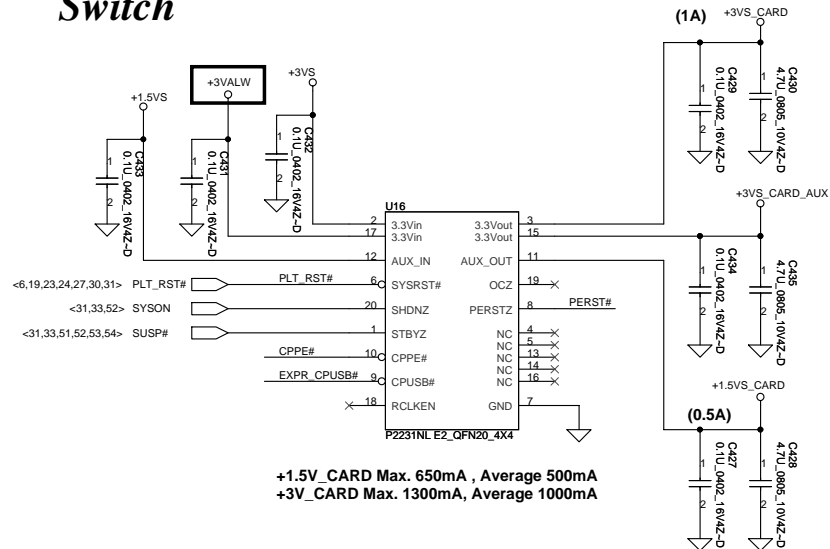


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WPAN Card

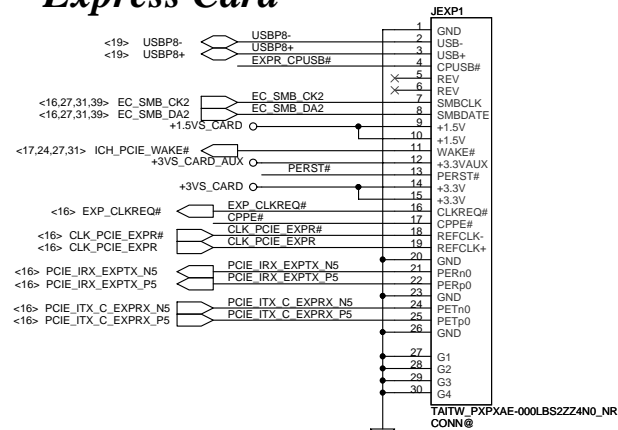


Express Card Power Switch



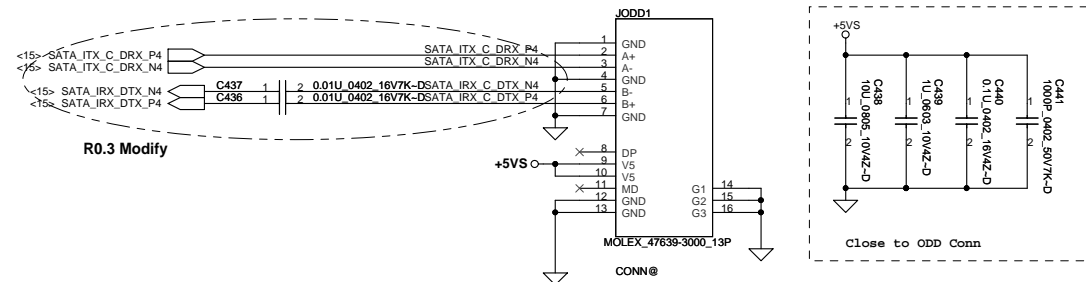
+1.5V_CARD Max. 650mA , Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

Express Card

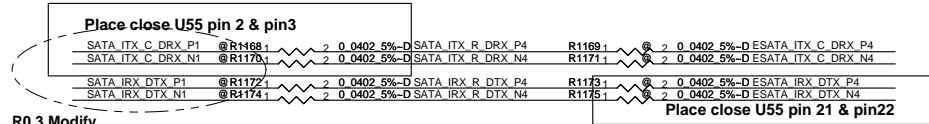
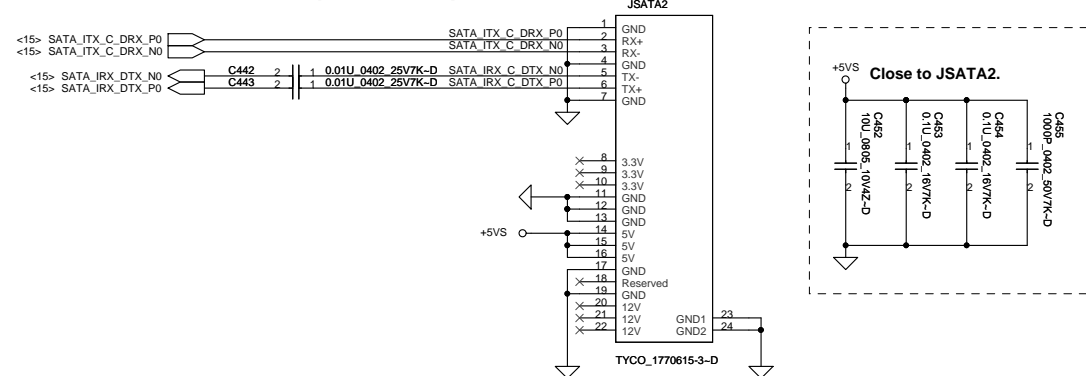


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				Customer	401808
				Date:	Monday, September 21, 2009

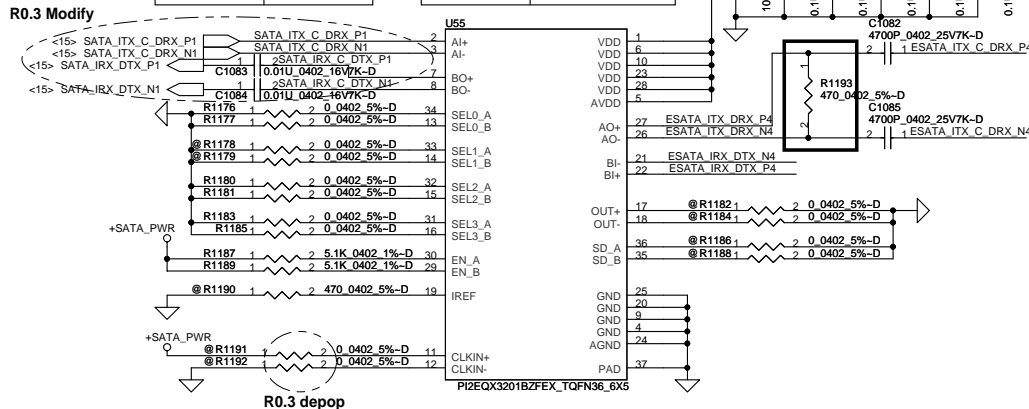
SATA ODD CONN



SATA HDD (On board)



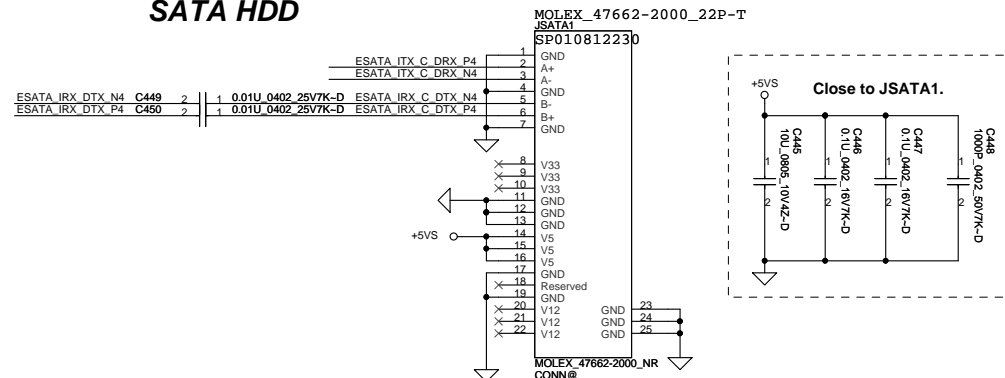
SEL2_ [A:B]	Swing	SEL3_ [A:B]	De-emphasis
0	1x	0	0dB
1	1.2x	1	-3.5dB



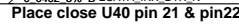
R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)

SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

SATA HDD

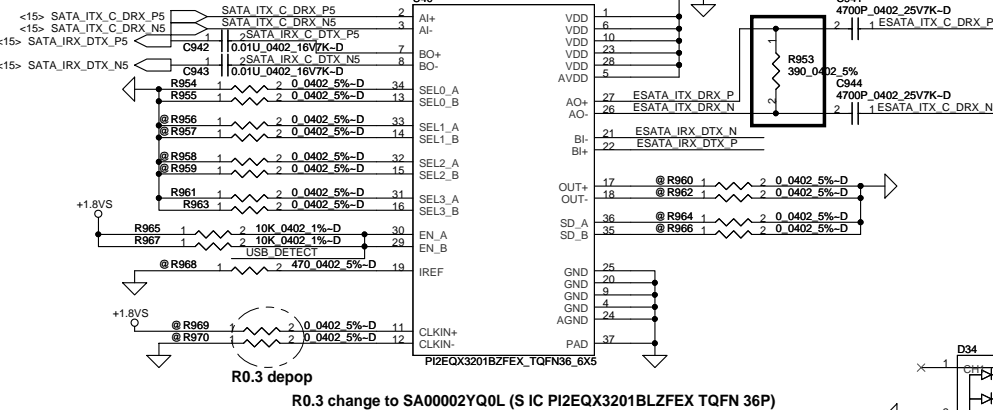


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Date: Monday, September 21, 2009		Sheet	29 of 57

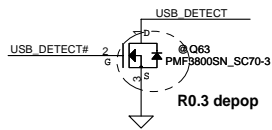


SEL2_ [A:B]	Swing
0	1x
1	1.2x

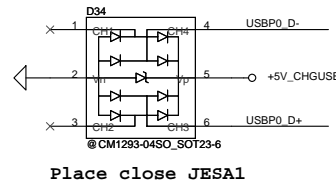
	SEL3_ [A:B]	De-emphasis
*	0	0dB
	1	-3.5dB



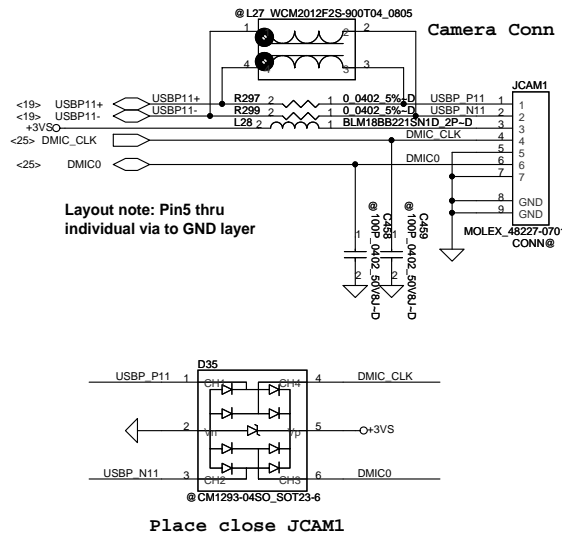
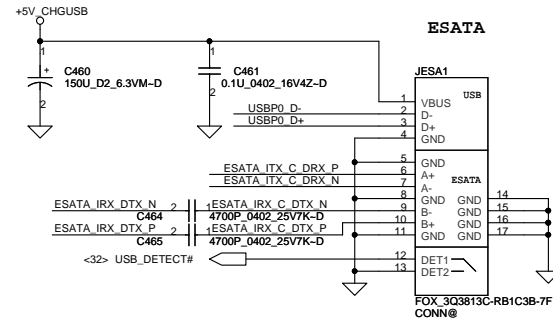
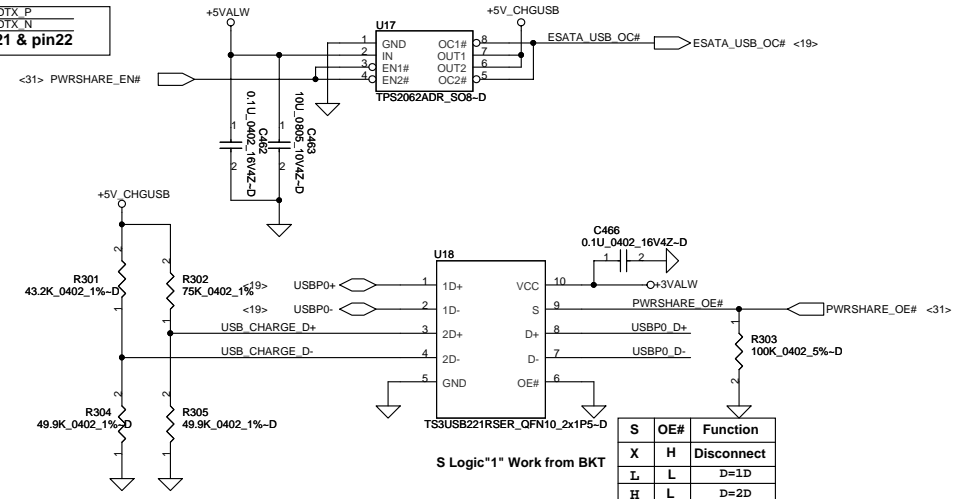
R0.3 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)



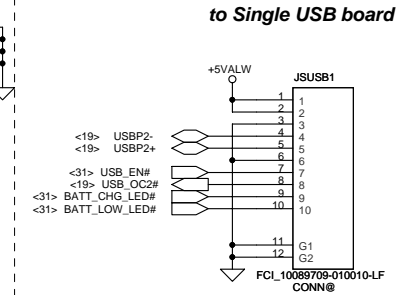
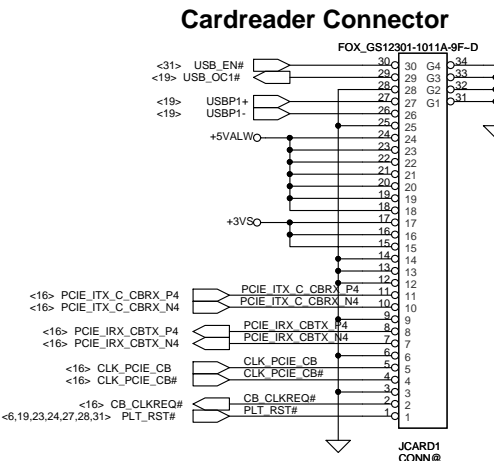
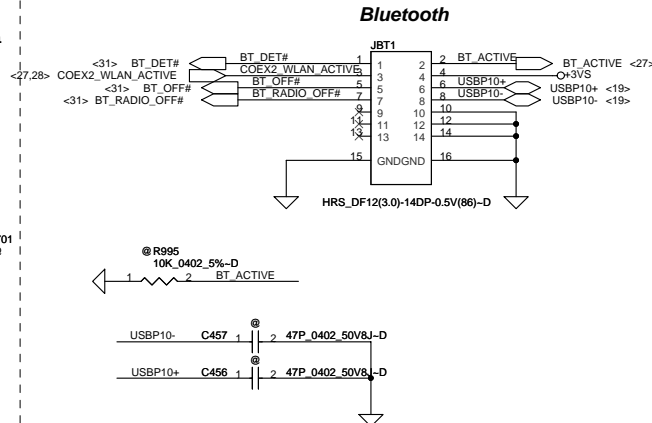
SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz



Place close JESA1

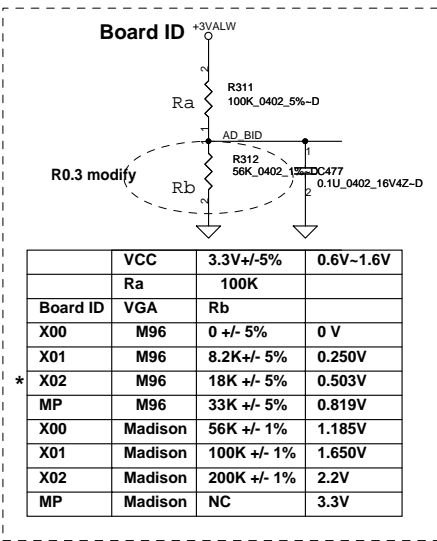


Place close JCAM1



to Single USB board

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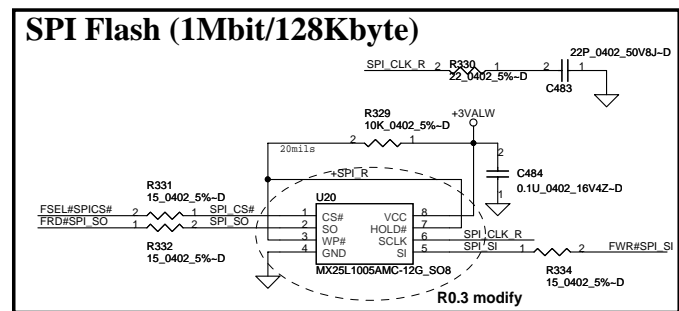
Place under u20

JP1

1 2 3 4 5 6 7 8

SPI CS# +3V SPI SO +SPI R SPI CLK R SPI SI E&T CONN

2941-G08N-00E-D

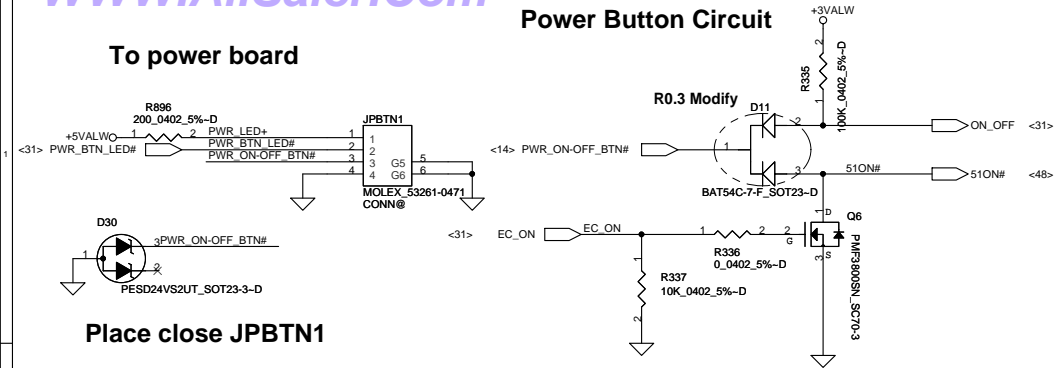


	VCC	3.3V+/-5%	0.6V~1.6V
	Ra	100K	
Board ID	VGA	Rb	
X00	M96	0 +/- 5%	0 V
X01	M96	8.2k+/- 5%	0.250V
X02	M96	18K +/- 5%	0.503V
MP	M96	33K +/- 5%	0.819V
X00	Madison	56K +/- 1%	1.185V
X01	Madison	100K +/- 1%	1.650V
X02	Madison	200K +/- 1%	2.2V
MP	Madison	NC	3.3V

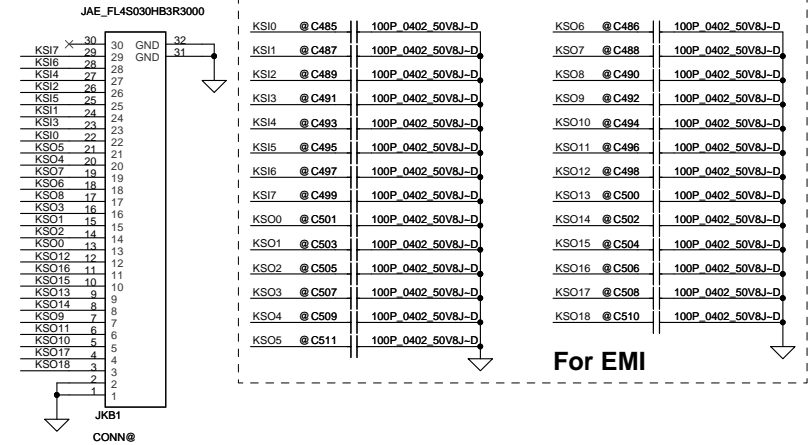
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Power Button Circuit

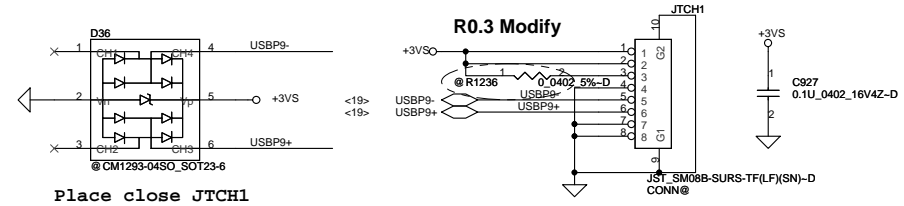
To power board



INT_KB_Conn.1

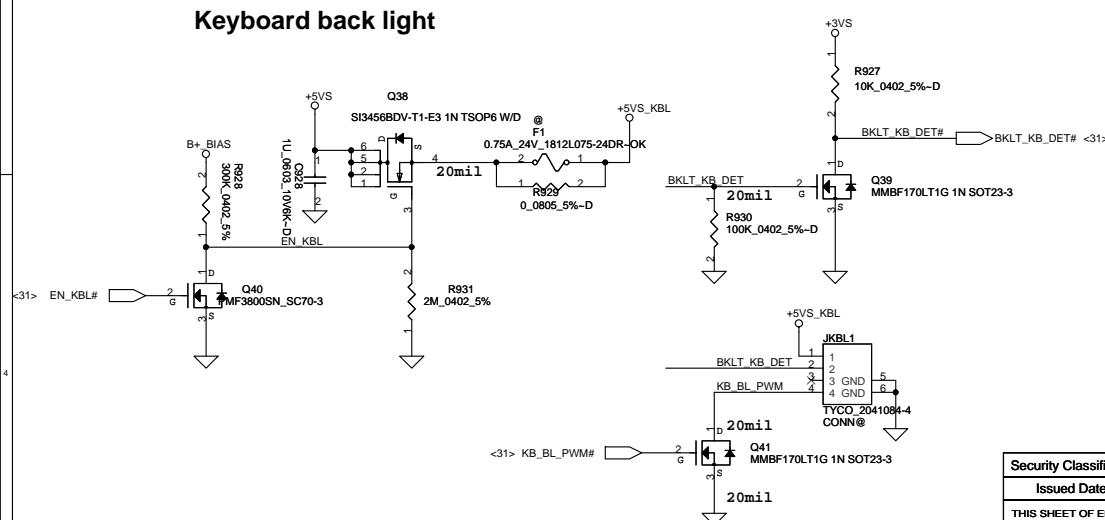


Touch Screen Connector

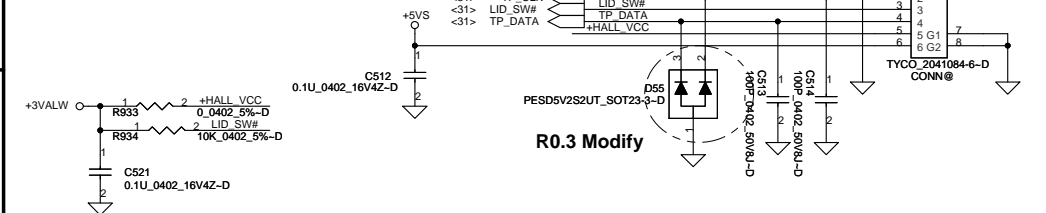


Power share

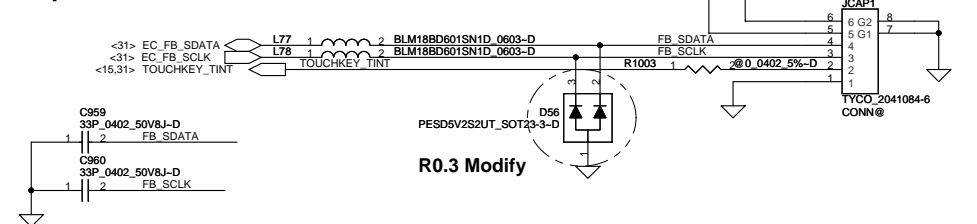
Keyboard back light



Touch PAD/B Conn.

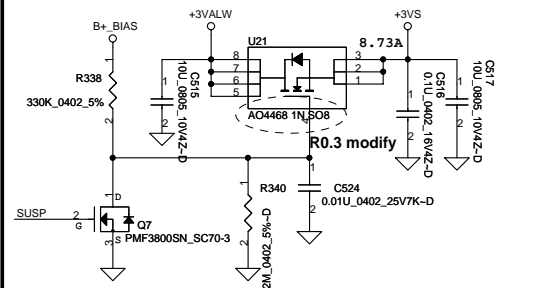


Cap Sensor

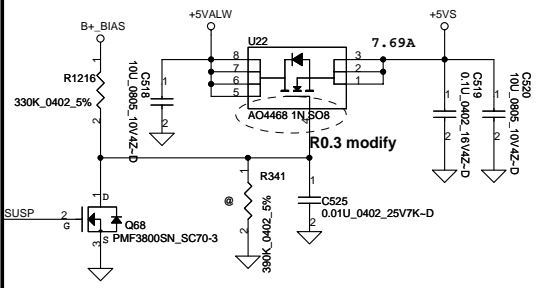


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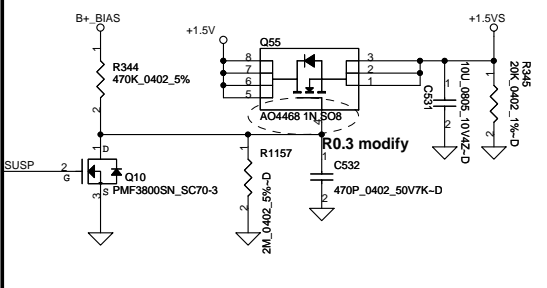
+3VALW to +3VS Transfer



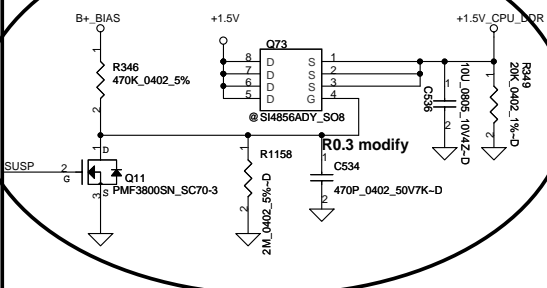
+5VALW to +5VS Transfer



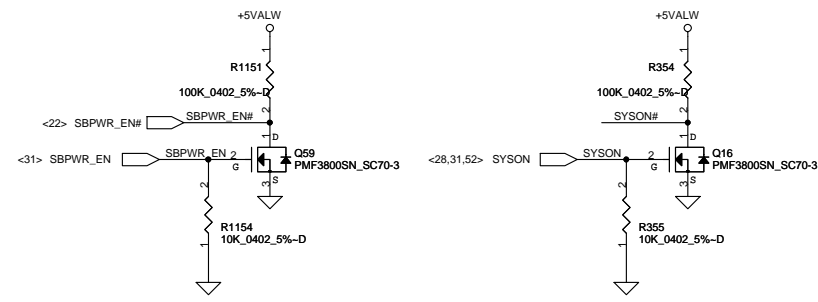
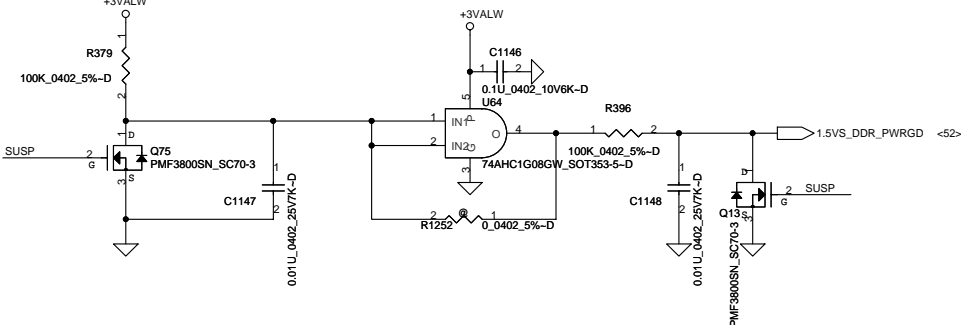
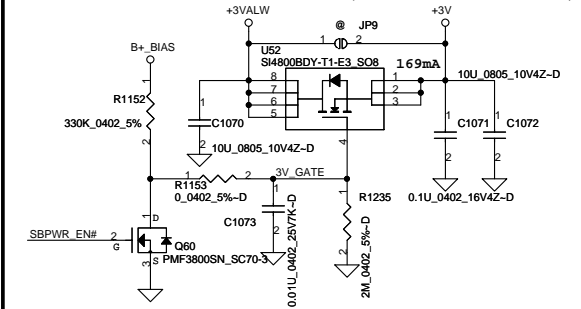
+1.5V to +1.5VS Transfer



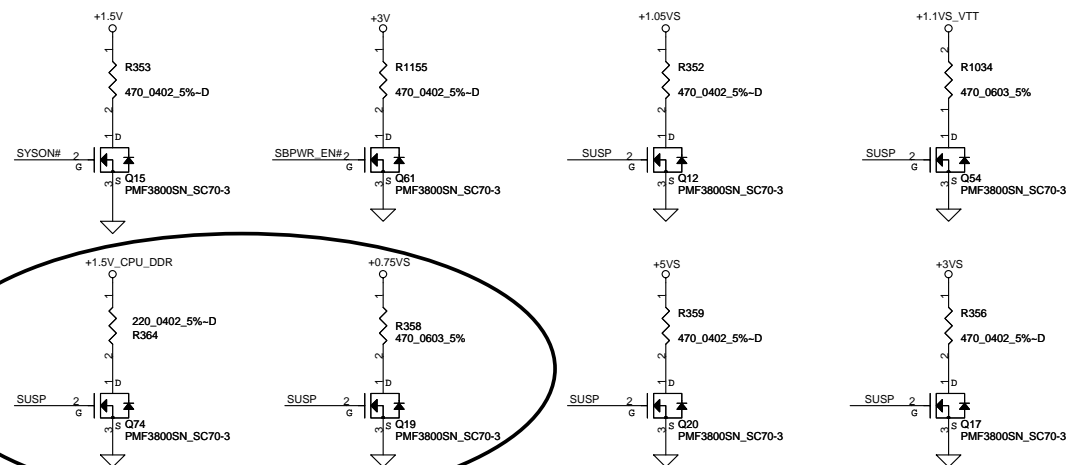
~~+1.5V~~ to +1.5VS_DDR Transfer



+3VALW to +3V Transfer (PCH AUX Power)



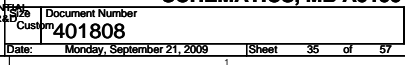
Discharge Circuit

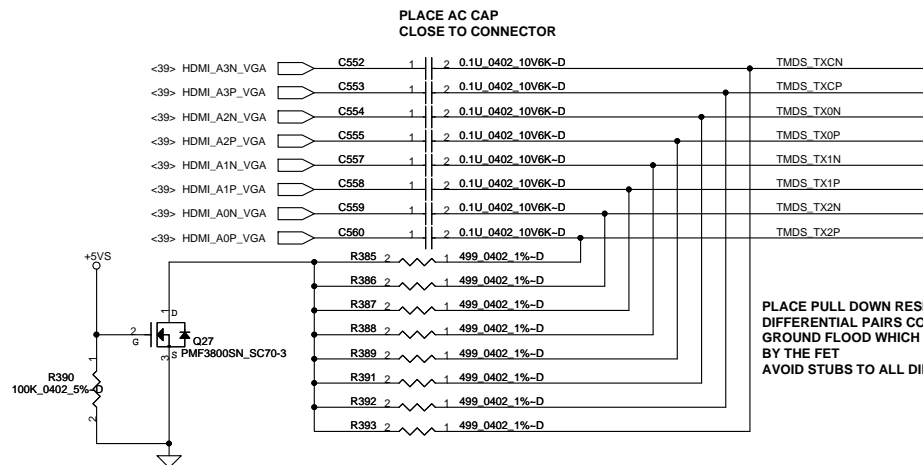


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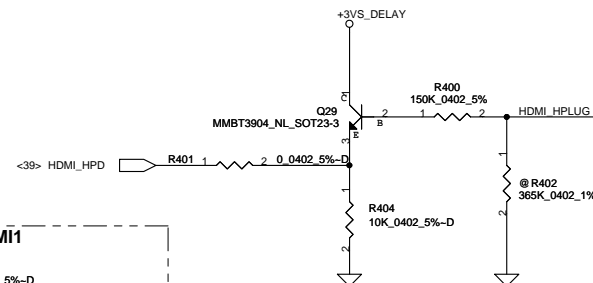


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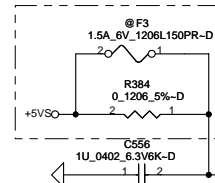
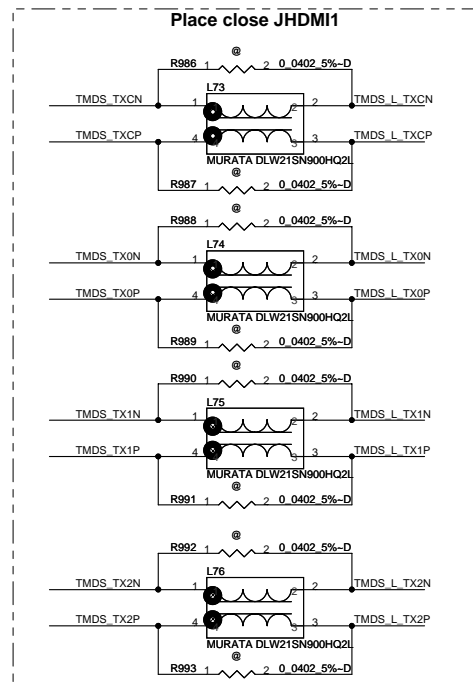
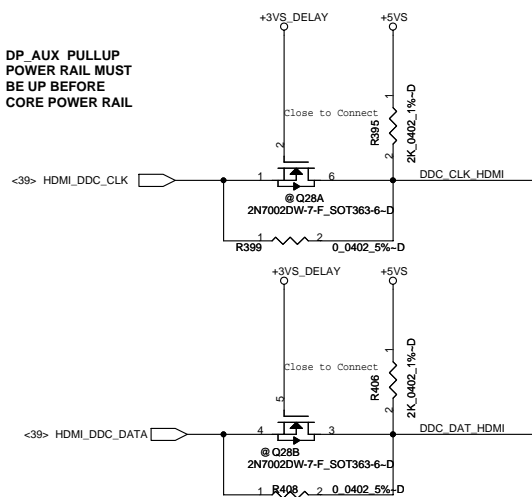




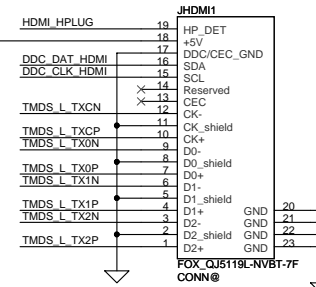
PLACE PULL DOWN RESISTORS CLOSE TO
DIFFERENTIAL PAIRS CONNECTED TO SOLID
GROUND FLOOD WHICH IS CONTROLLED
BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES



DP_AUX PULLUP
POWER RAIL MUST
BE UP BEFORE
CORE POWER RAIL

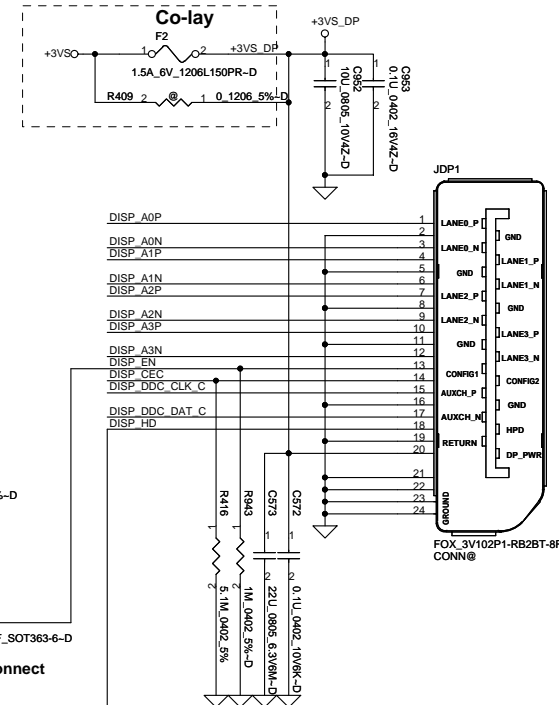
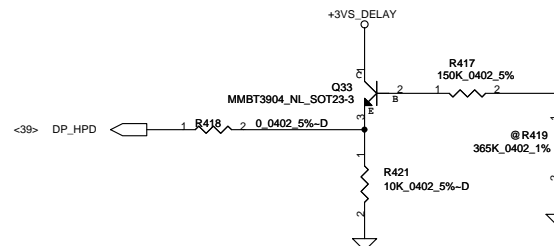
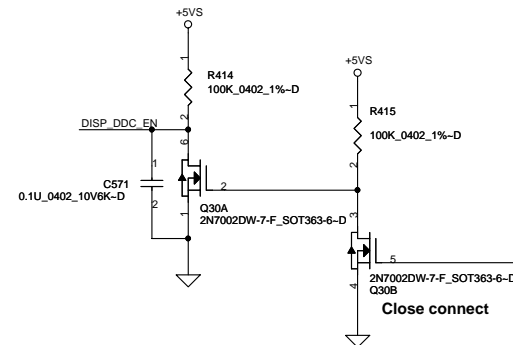
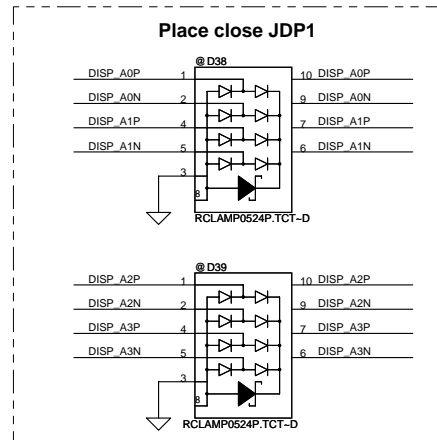
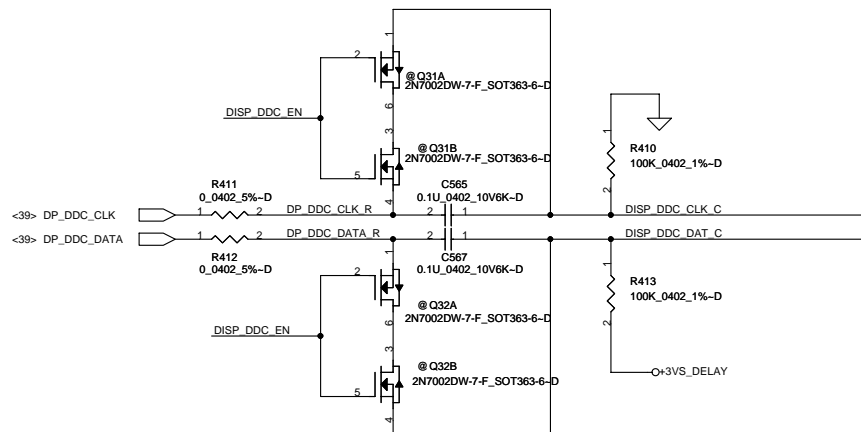


Co-lay

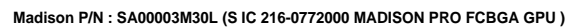


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<39> DISP_A0N_VGA	C561	2	1	0.1U_0402_10V6K-D	DISP_A0N
<39> DISP_A0P_VGA	C562	2	1	0.1U_0402_10V6K-D	DISP_A0P
<39> DISP_A1N_VGA	C563	2	1	0.1U_0402_10V6K-D	DISP_A1N
<39> DISP_A1P_VGA	C564	2	1	0.1U_0402_10V6K-D	DISP_A1P
<39> DISP_A2N_VGA	C565	2	1	0.1U_0402_10V6K-D	DISP_A2N
<39> DISP_A2P_VGA	C566	2	1	0.1U_0402_10V6K-D	DISP_A2P
<39> DISP_A3N_VGA	C569	2	1	0.1U_0402_10V6K-D	DISP_A3N
<39> DISP_A3P_VGA	C570	2	1	0.1U_0402_10V6K-D	DISP_A3P



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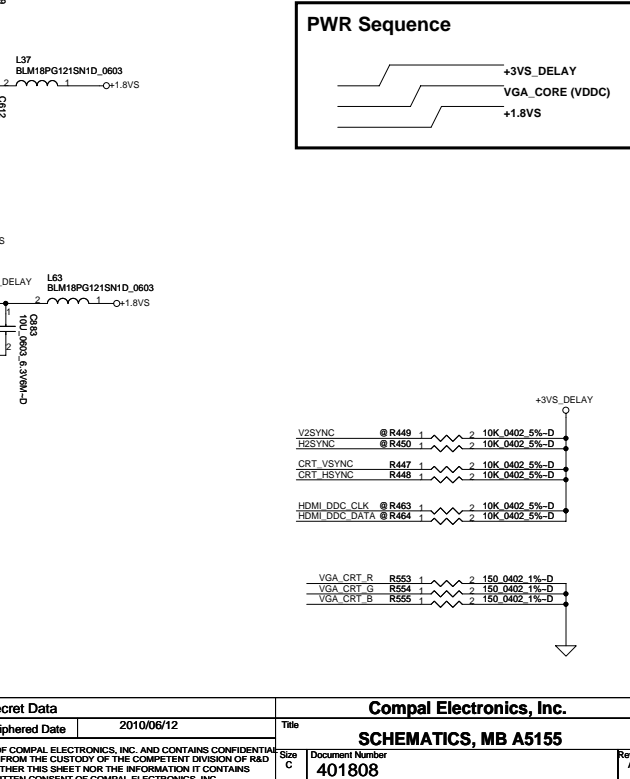
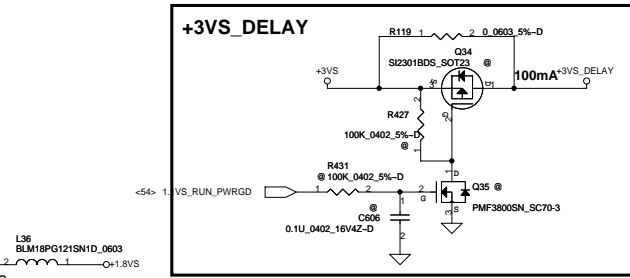
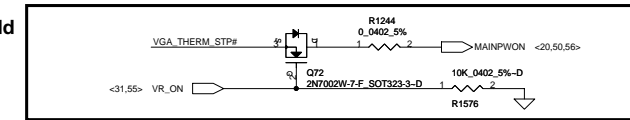
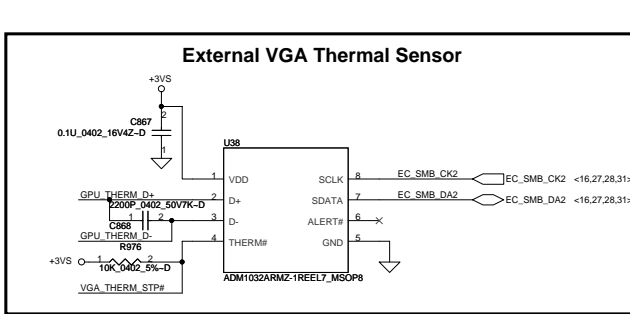
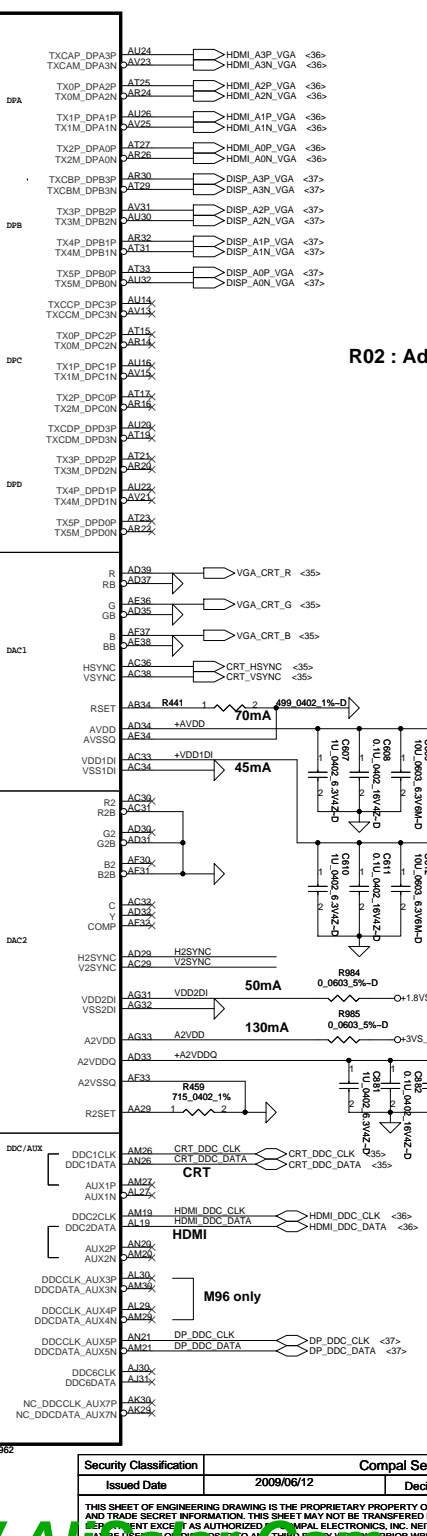
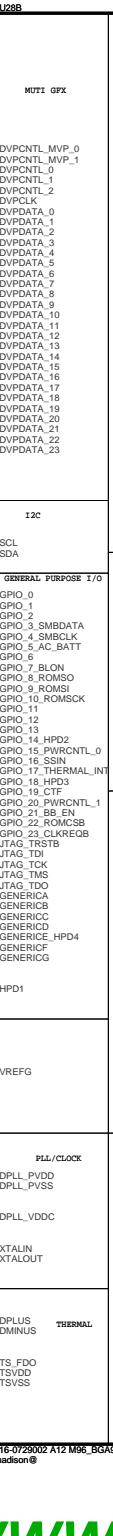
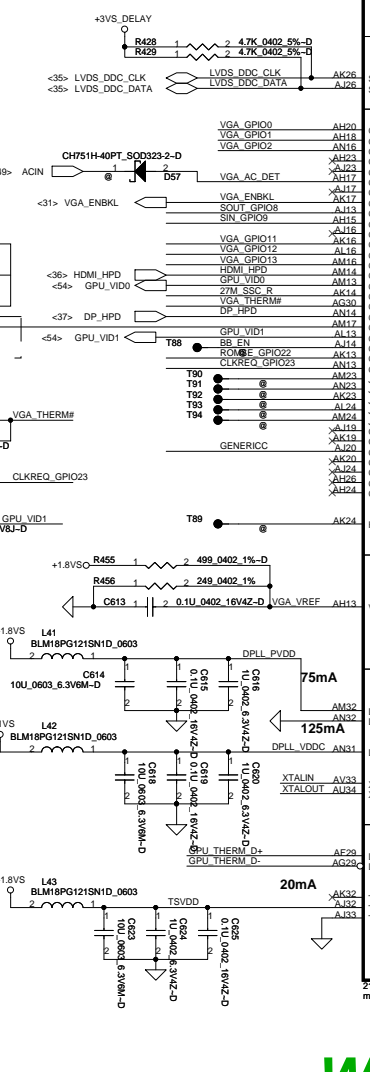
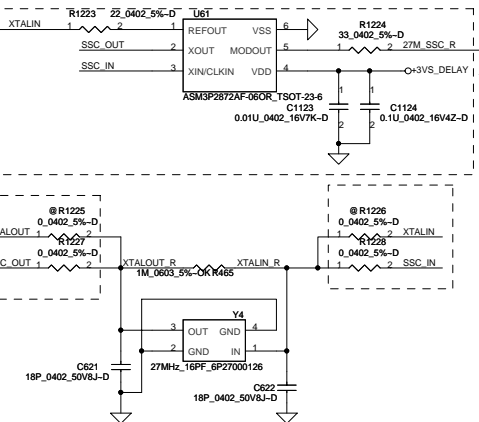
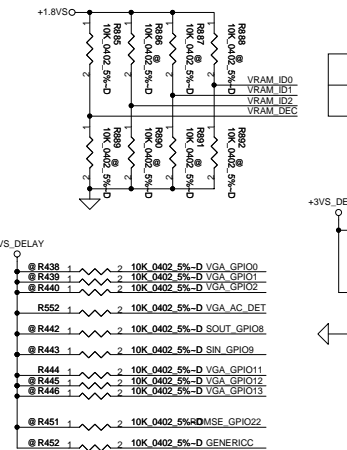


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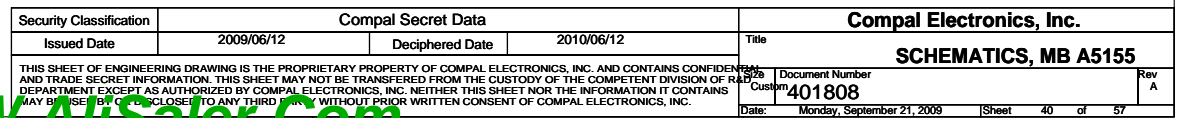
Strap Name	Pin	Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF_CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE_STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location	MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3
VRAM				
Samsung	0	0	0	0
HYNIX	1	0	0	0

Location	MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3
VRAM				
Samsung	0	0	0	0
HYNIX	1	0	0	0

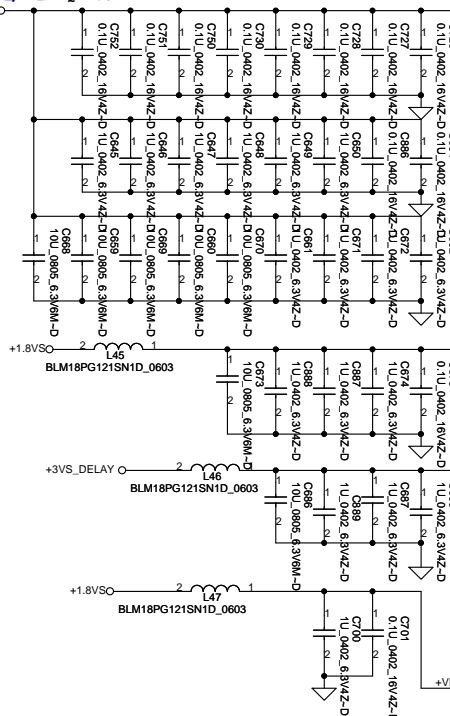


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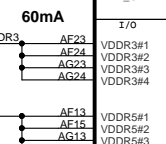
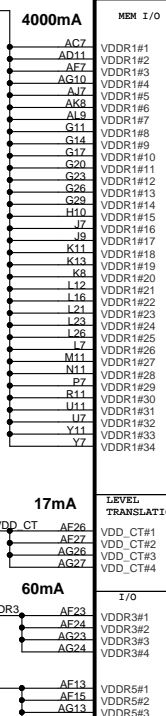


For DDR3, MVDDQ=1.5V

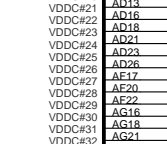
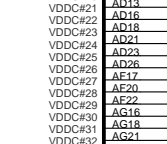
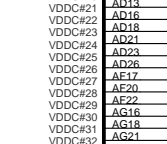
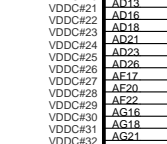
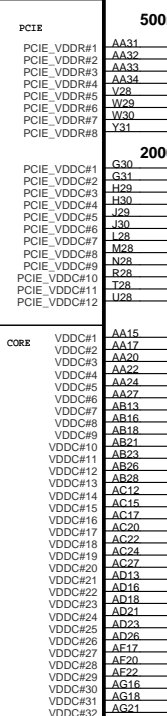
+1.5VSO



U28E

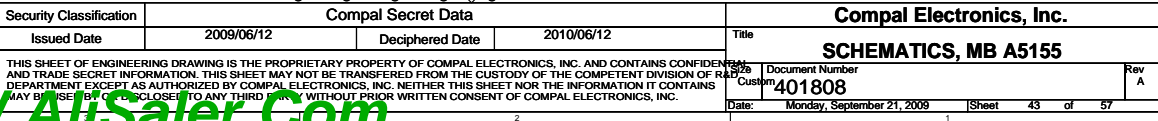


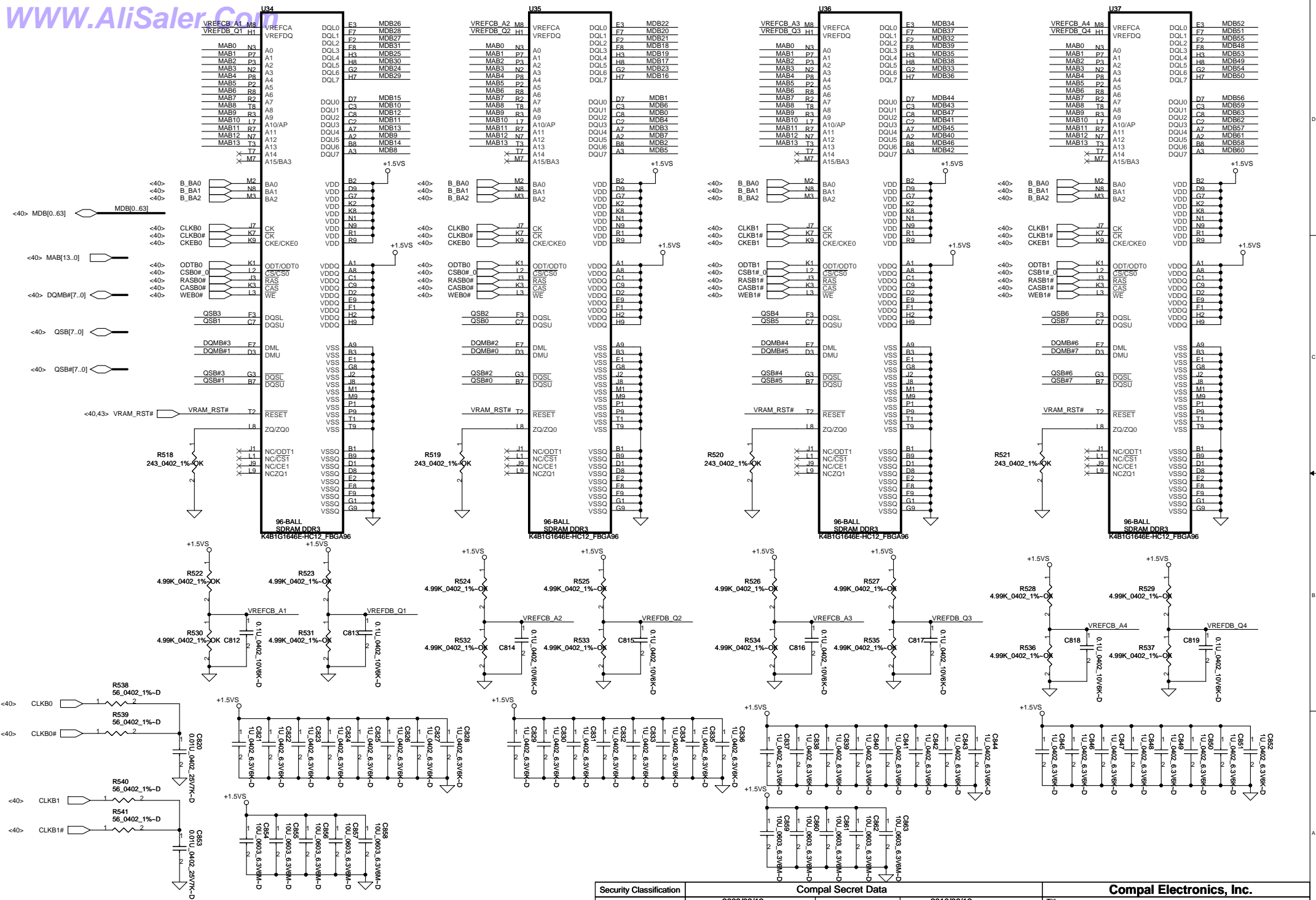
POWER



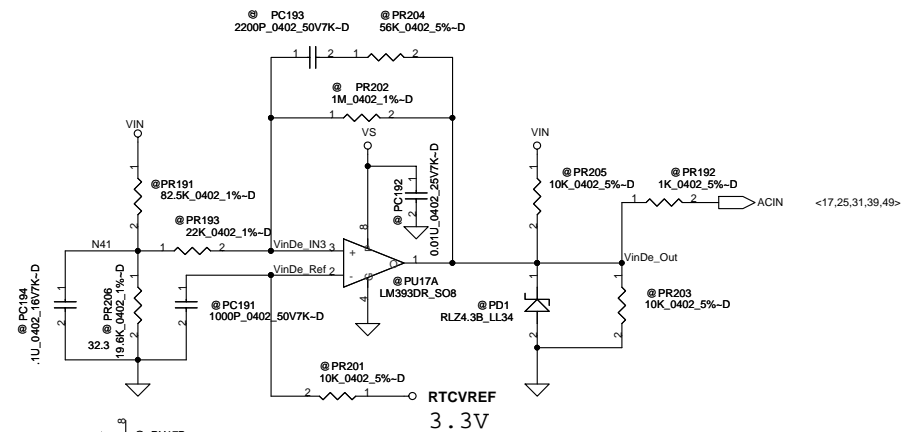
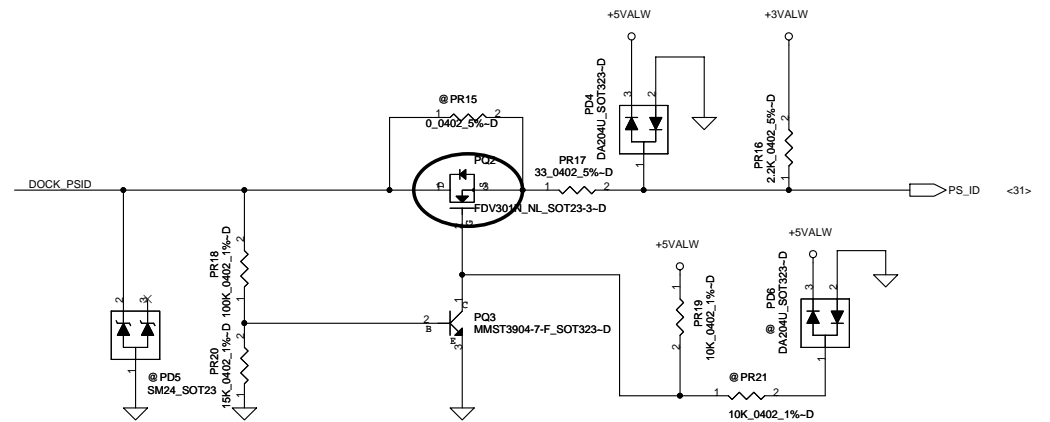


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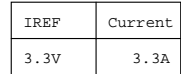




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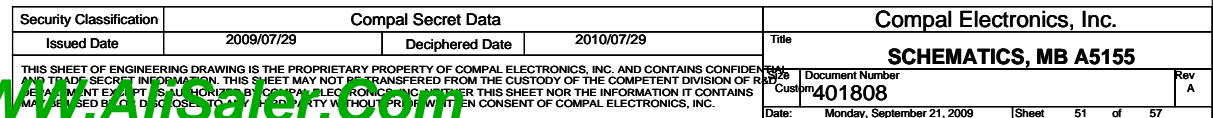


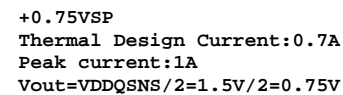
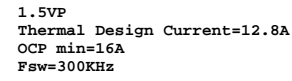
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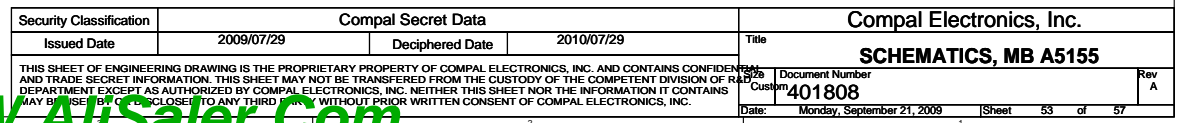
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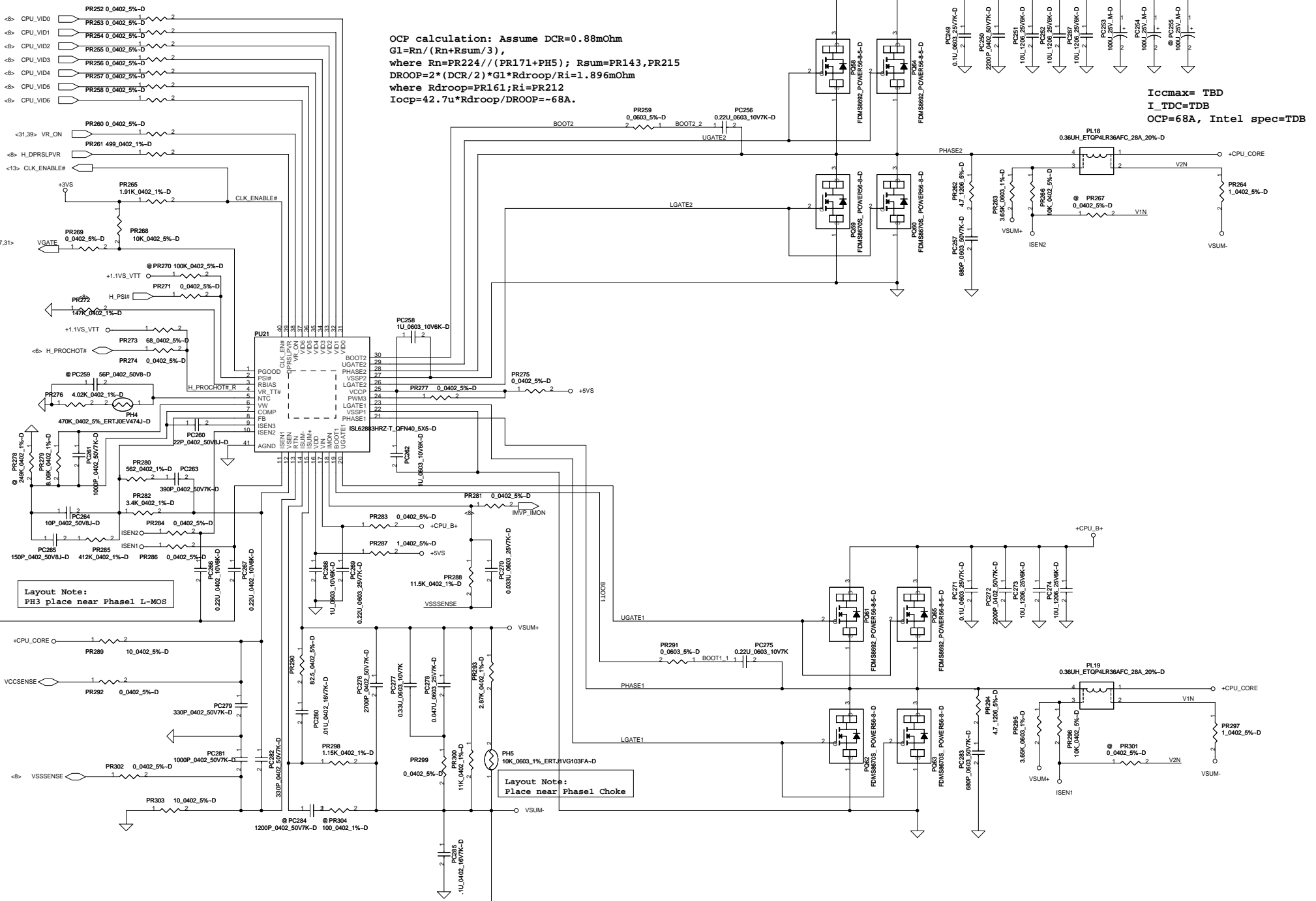


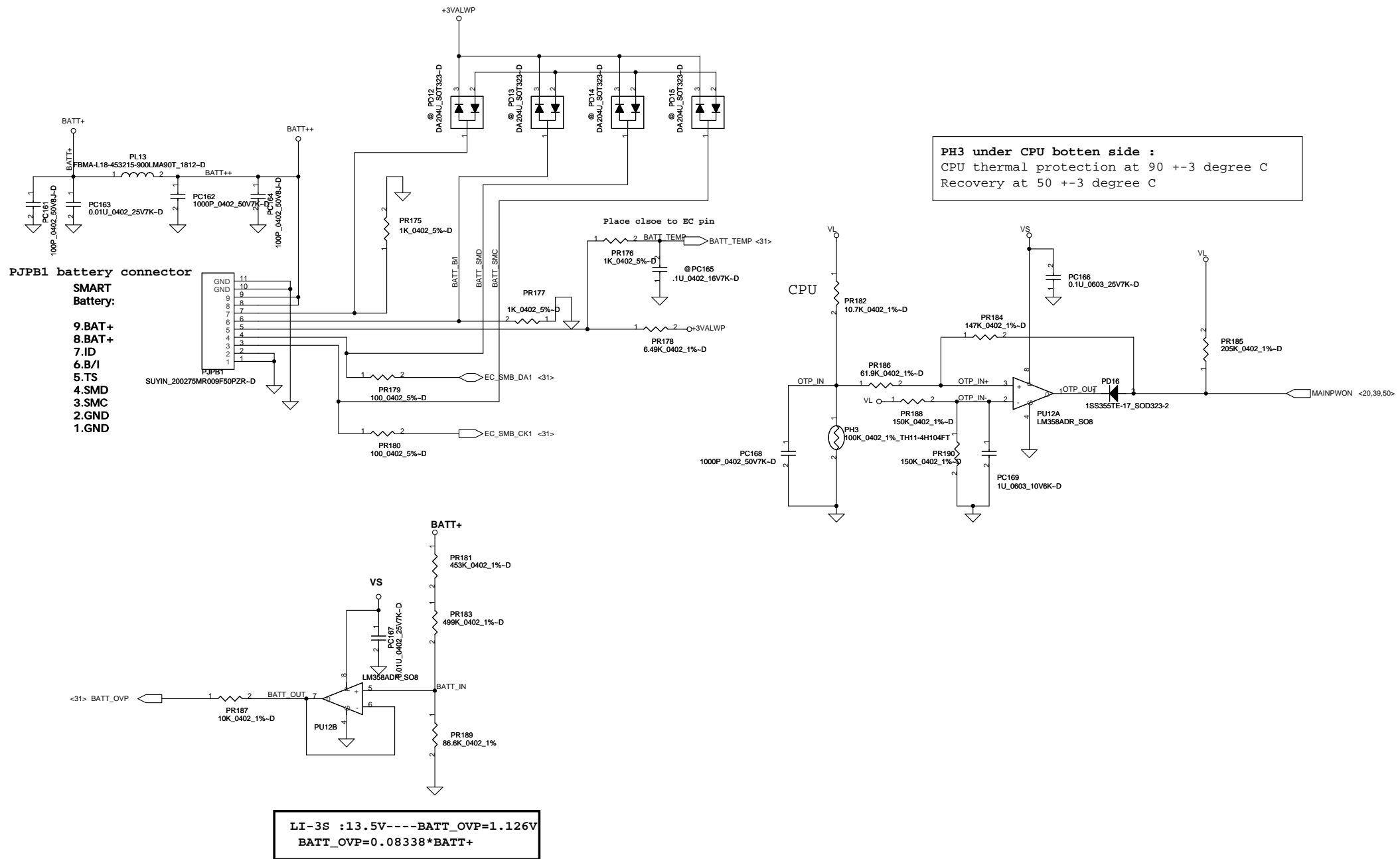


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