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Model Name: KAT00 DIS

PCB NO: LA-5151P

PCB P/N: DA80000E400

BOM P/N: 43169531L01 (M92)

43169531L02 (M96)

Compal Confidential

Schematic Document

POITIER Montevina M96/M92

2009 / 06/ 12 Rev:1.0 (A00)

@ : Nopop component

92@ : Use ATI M92 Graphic solution
96@ : Use ATI M96 Graphic solution

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Title: Cover Sheet		
Size	Document Number: LA-5151P	Rev: R10 (A00)
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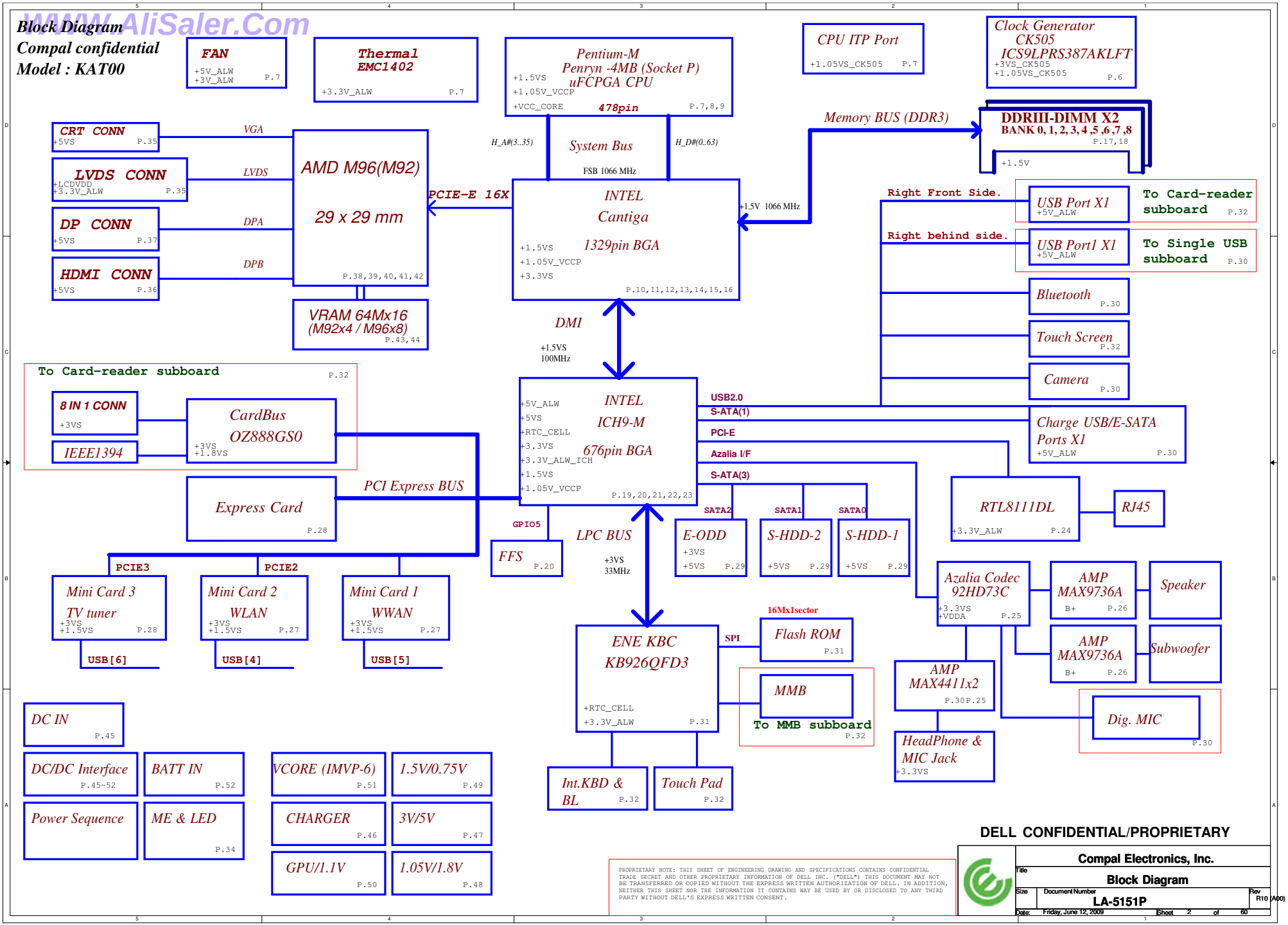
Block Diagram
Compal confidential
Model : KAT00



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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.1VS +VCCP +0.75VS +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

USB Port	Device
0	USB&ESATA
1	Reader/BD
2	USB board
3	NC
4	WLAN
5	WWAN
6	WPAN
7	Express
8	NC
9	Touch screen
10	Bluetooth
11	Camera

SATA Port	Device
0	JSATA1
1	JSATA2
4	JESA1
5	JODD

PCIE Port	Device
1	JWWAN1
2	JWLAN1
3	JWPAN1
4	Reader/BD (OZ888)
5	JEXP1
6	RTL8111DL

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X

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Title: Note List

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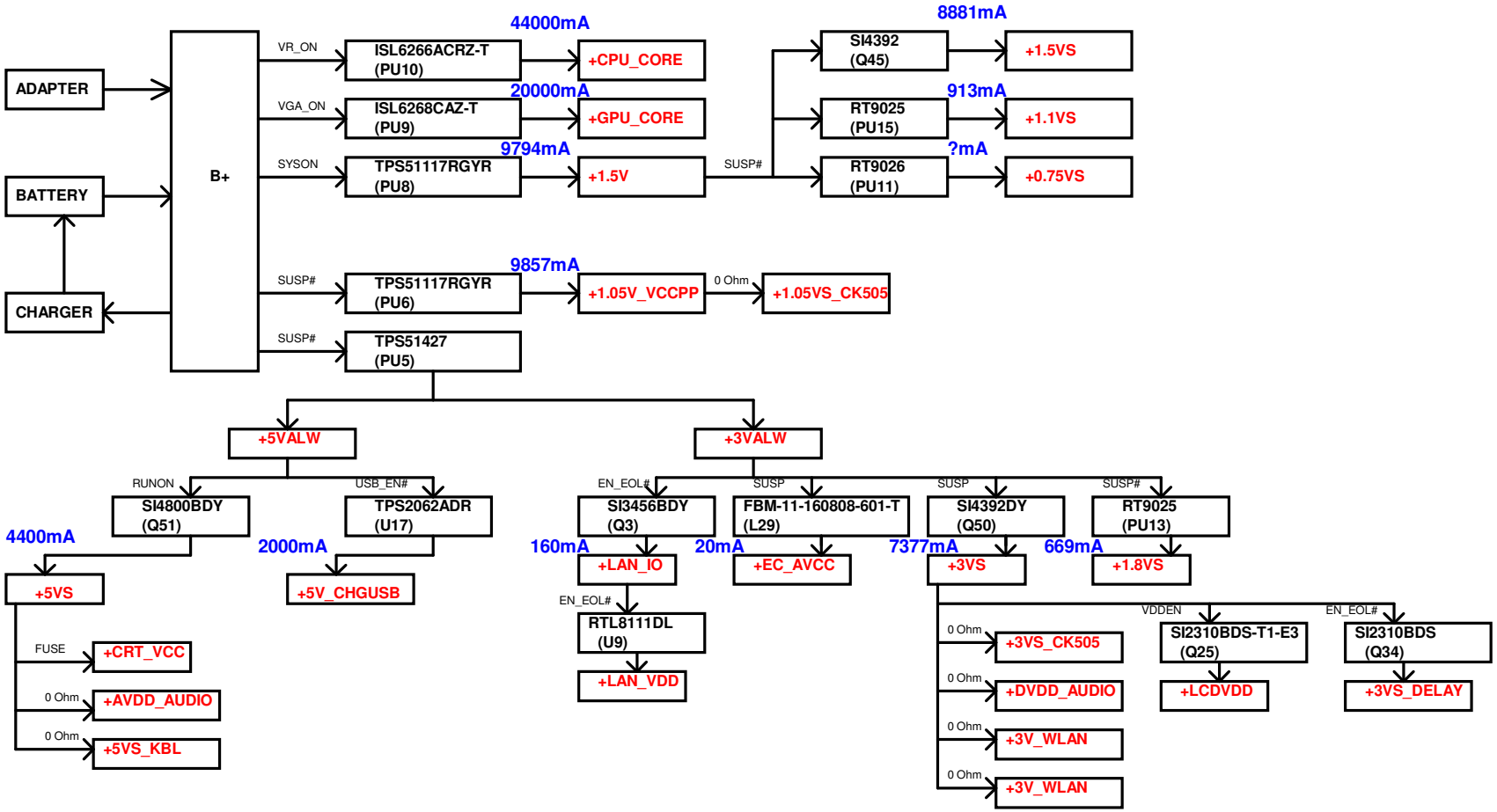

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Title: Power Rail	
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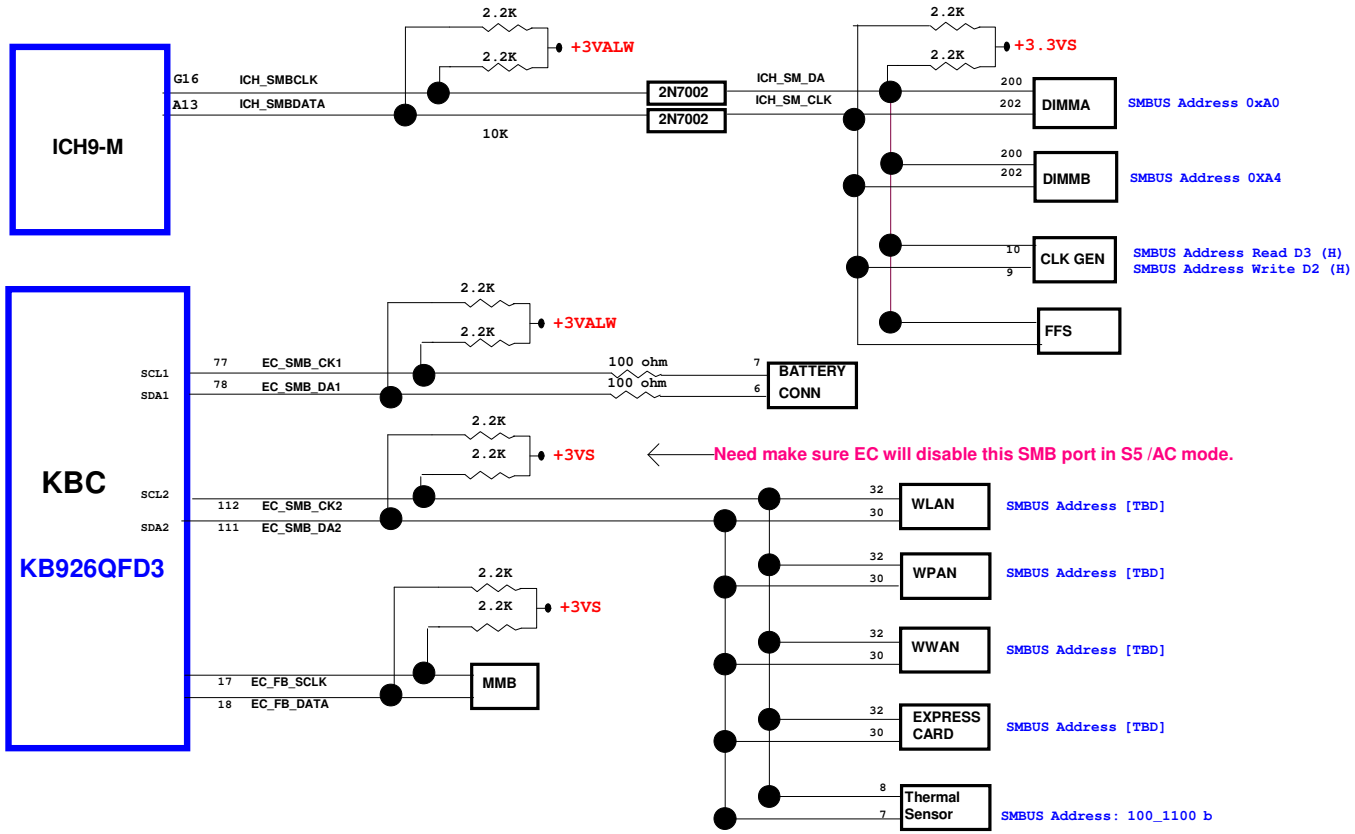

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

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Title: SMBUS TOPOLOGY

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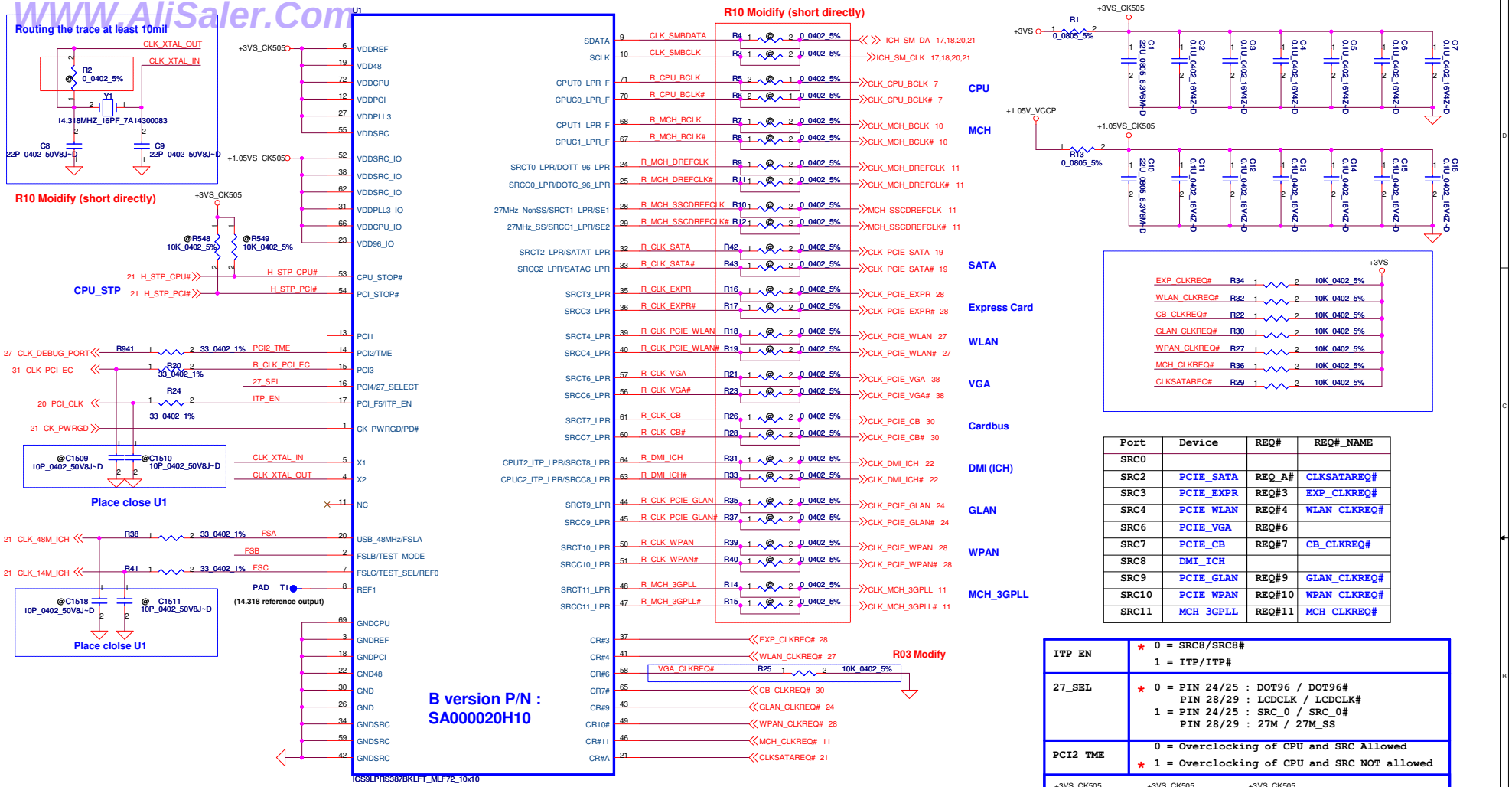

Port	Device	REQ#	REQ#_NAME
SRC0			
SRC2	PCIE_SATA	REQ_A#	CLKSATAREQ#
SRC3	PCIE_EXPR	REQ#3	EXP_CLKREQ#
SRC4	PCIE_WLAN	REQ#4	WLAN_CLKREQ#
SRC6	PCIE_VGA	REQ#6	
SRC7	PCIE_CB	REQ#7	CB_CLKREQ#
SRC8	DMI_ICH		
SRC9	PCIE_GLAN	REQ#9	GLAN_CLKREQ#
SRC10	PCIE_WPAN	REQ#10	WPAN_CLKREQ#
SRC11	MCH_3GPLL	REQ#11	MCH_CLKREQ#

ITP_EN	* 0 = SRC8/SRC8# 1 = ITP/ITP#
27_SEL	* 0 = PIN 24/25 : DOT96 / DOT96# PIN 28/29 : LCDCLK / LCDCLK# 1 = PIN 24/25 : SRC_0 / SRC_0# PIN 28/29 : 27M / 27M_SS
PCI2_TME	0 = Overclocking of CPU and SRC Allowed * 1 = Overclocking of CPU and SRC NOT allowed

	FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
*	0	0	0	266	100	33.3	14.318	96.0	48.0
	0	0	1	133	100	33.3	14.318	96.0	48.0
	0	1	0	200	100	33.3	14.318	96.0	48.0
	0	1	1	166	100	33.3	14.318	96.0	48.0
	1	0	0	333	100	33.3	14.318	96.0	48.0
	1	0	1	100	100	33.3	14.318	96.0	48.0
	1	1	0	400	100	33.3	14.318	96.0	48.0
	1	1	1	Reserved					

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Title: Clock Generator CK505

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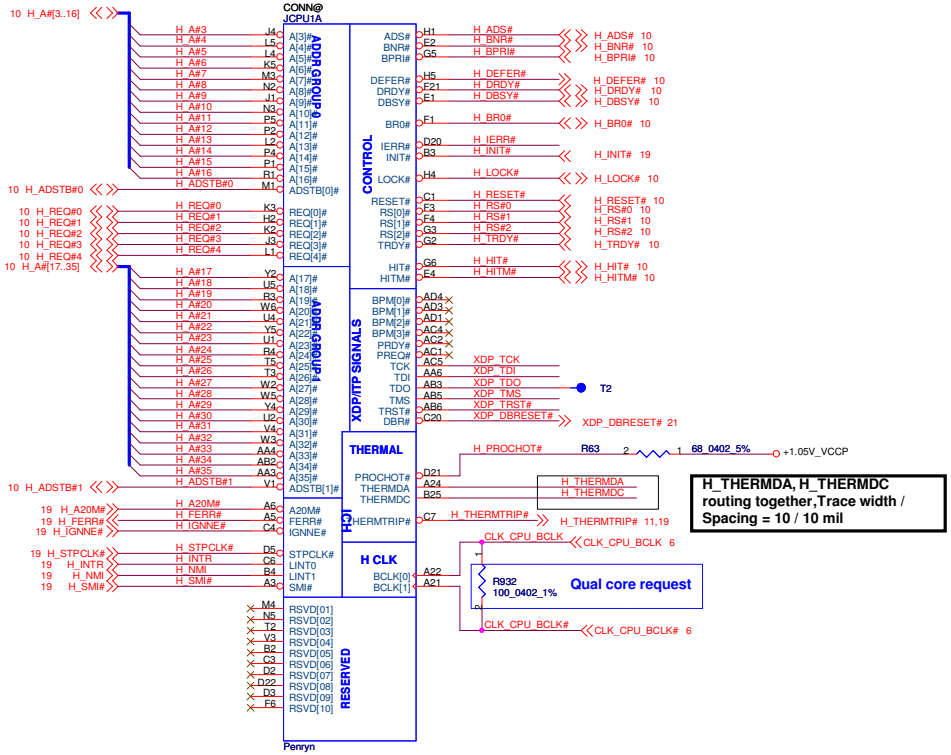
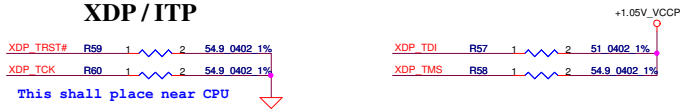
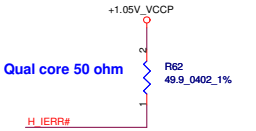


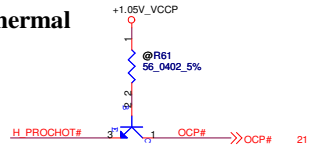
XDP / ITP



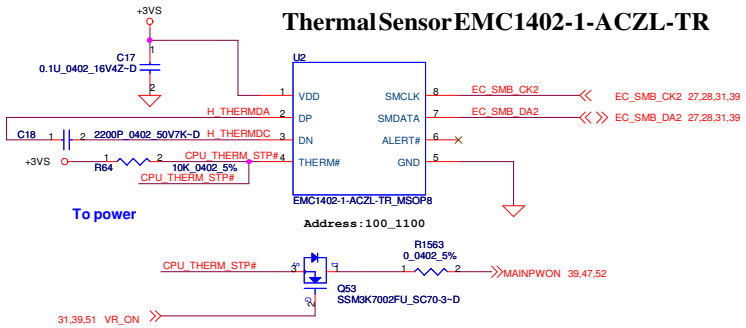
Control



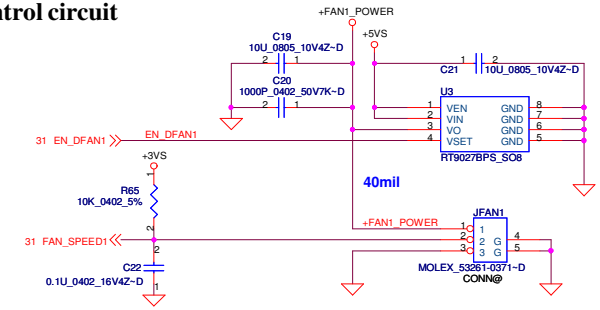
Thermal



Thermal Sensor EMC1402-1-ACZL-TR



FAN Control circuit



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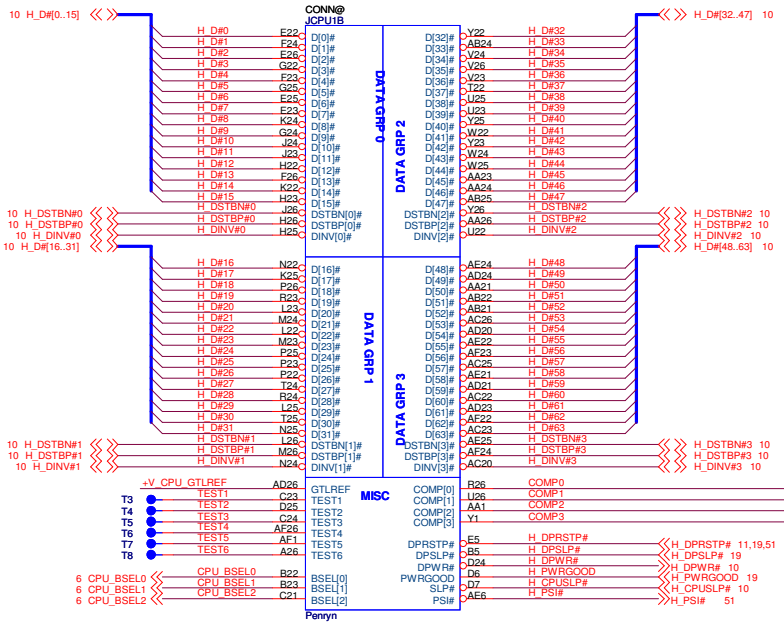
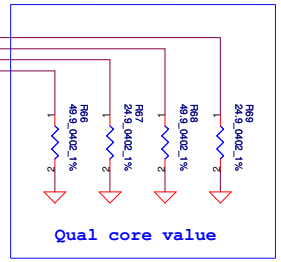
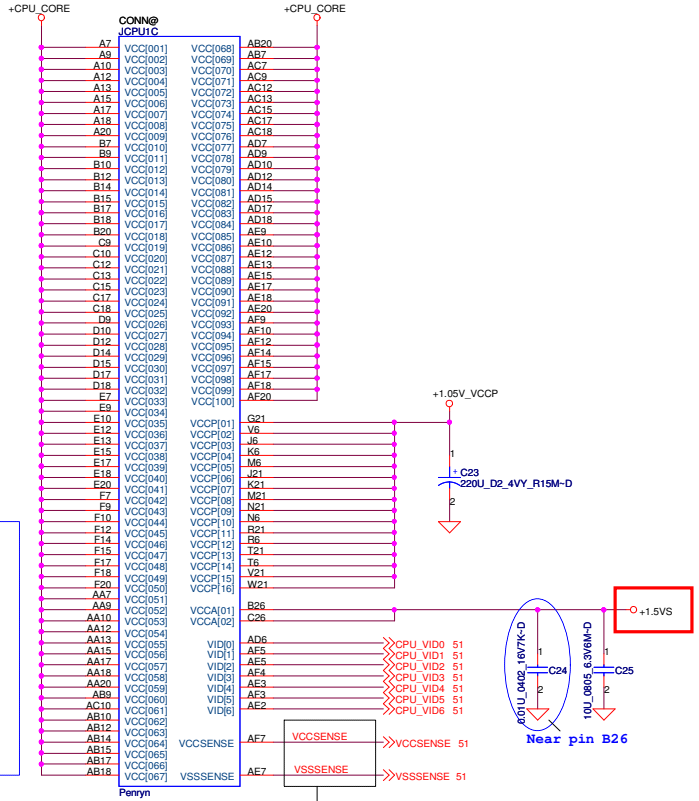


layout note: Rout H_DPRSTP# from ICH9 to IMVP6 then to GMCH & CPU

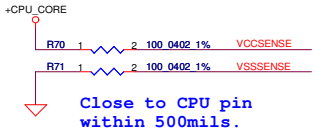
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs



Qual core value

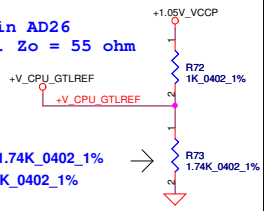


For 8 layer condition.
Length match within 25 mils.
The trace width/space/other
is 20/7/25. Zo = 27.4 ohm.



Close to CPU pin
within 500mils.

Close to CPU pin AD26
within 500mils. Zo = 55 ohm



Cpu Quad Core, R=1.74K_0402_1%
Cpu Dual Core, R=2K_0402_1%

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

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Title: Penryn(2/3)-AGTL+/ITP-XDP

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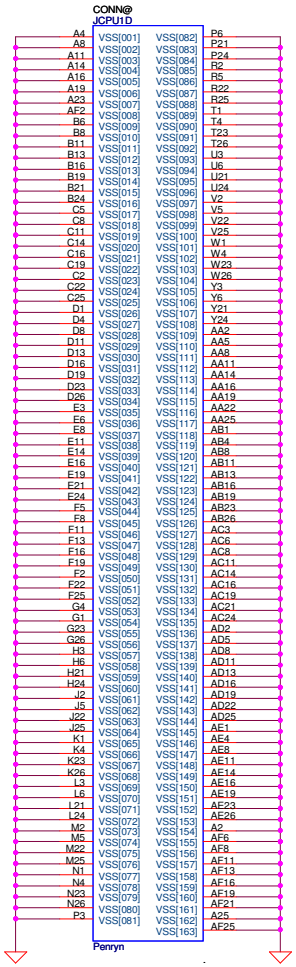
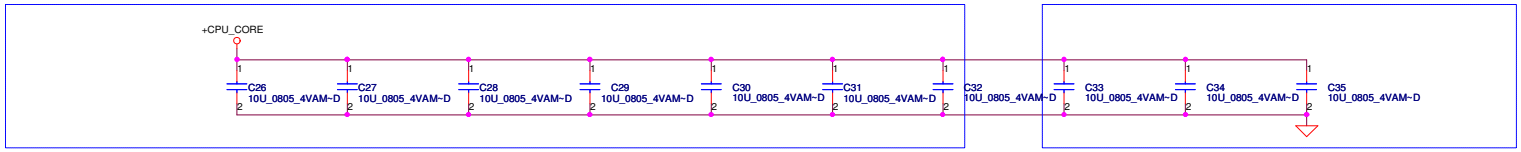
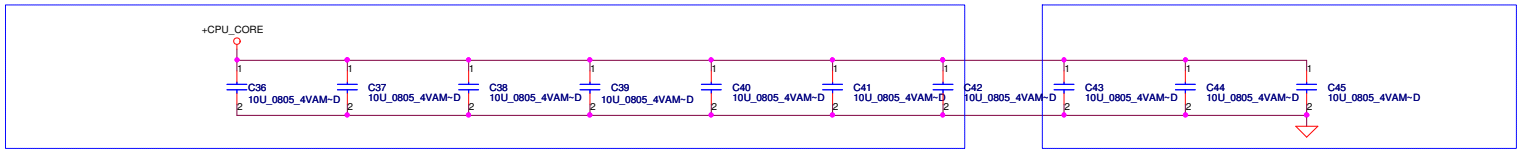
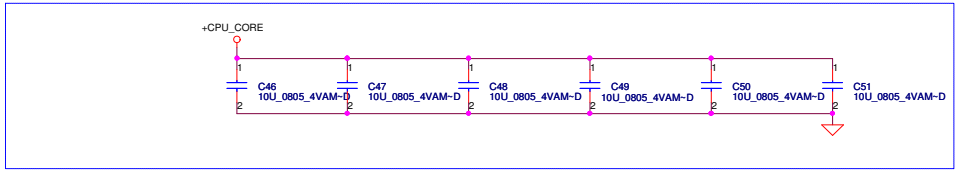
High Frequence Decoupling

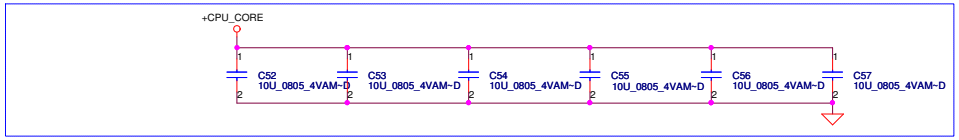
10uF 0805 X5R -> 85 degree.

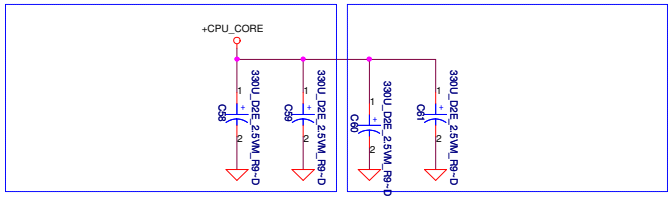






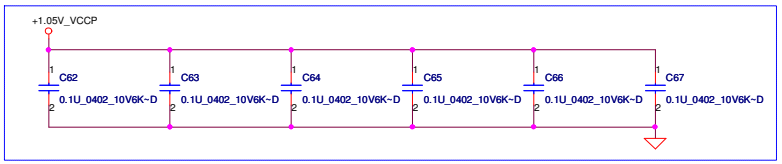






ESR <= 1.5m ohm

Capacitor > 880 uF



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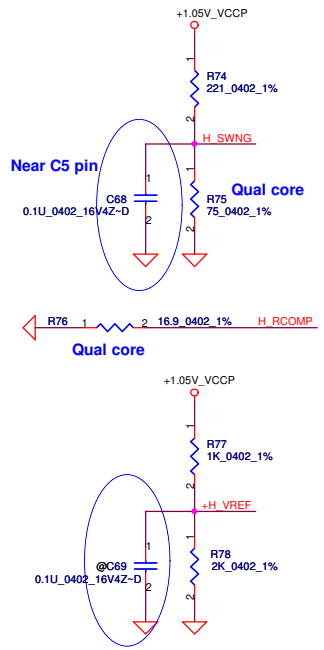
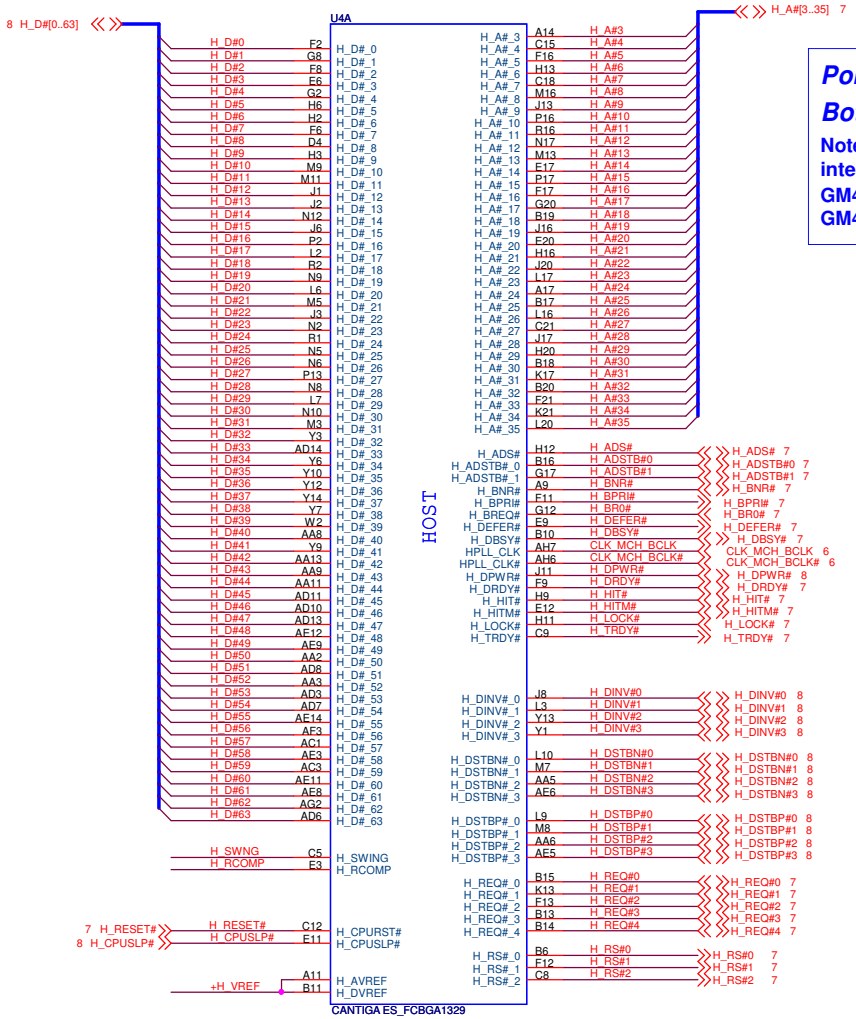
Layout Note :
H_RCOMP / H_VREF / H_SWNG
Trace width and spacing is 10 / 20



H_RCOMP Dual core 24.9 ohm_1% pull down
Qual core 16.9 ohm_1% pull down
H_SWNG Dual core 100 ohm_1% pull down
Qual core 75 ohm_1% pull down



Poitier

Both DIS & UMA use Cantiga GM45

Note : The difference between GM45 & GM47 is integrated graphic core freq @ Core voltage
GM45 : 533mHZ@1.05V
GM47 : 640mHZ@1.05V

P/N : SA00002JT3L (S IC AC82GM45 SLB94 B3 FCBGA1329 GM)

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Title	Cantiga(1 of 7)
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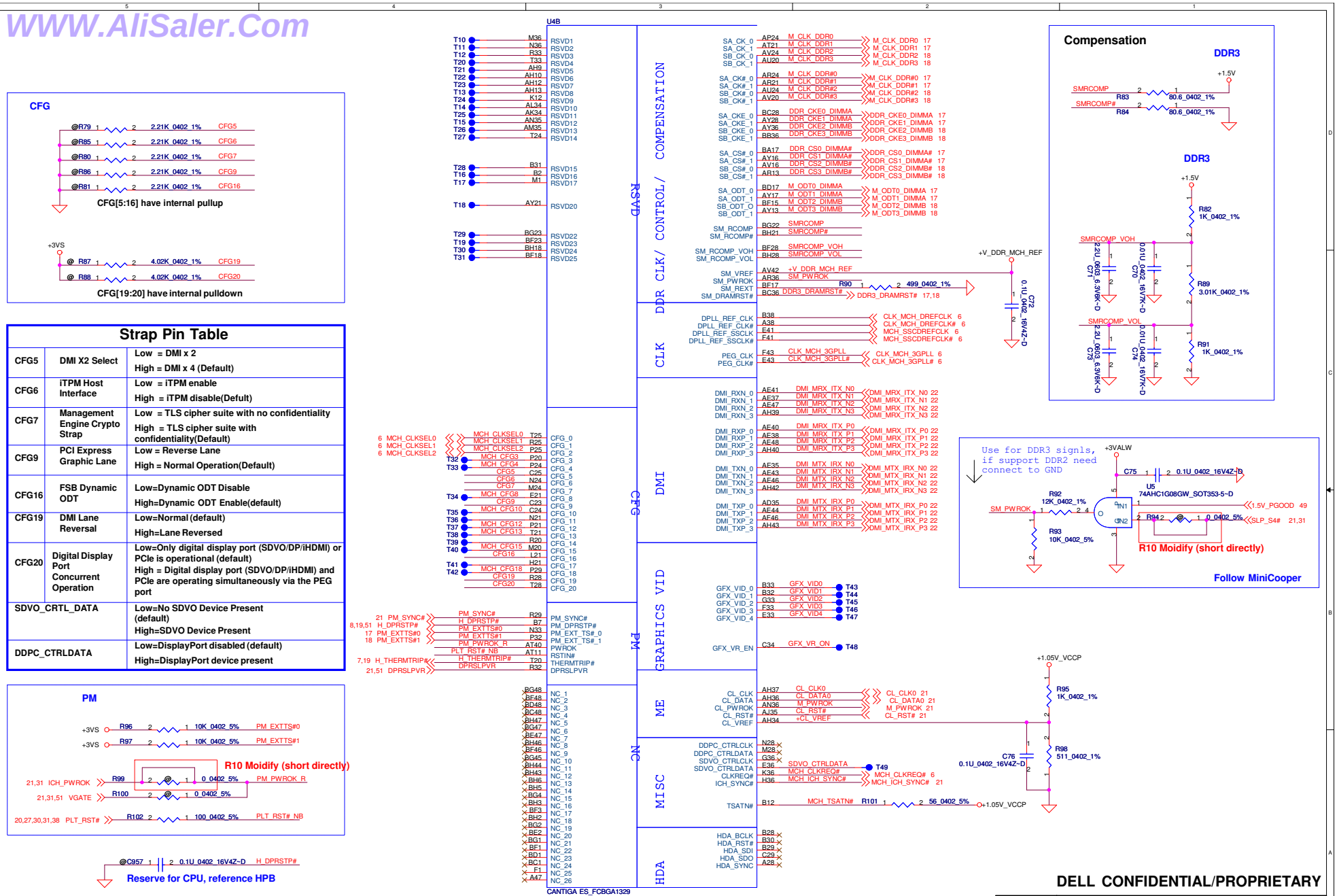

Strap Pin Table

CFG5	DMI X2 Select	Low = DMI x 2 High = DMI x 4 (Default)
CFG6	iTPM Host Interface	Low = iTPM enable High = iTPM disable(Defult)
CFG7	Management Engine Crypto Strap	Low = TLS cipher suite with no confidentiality High = TLS cipher suite with confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low = Reverse Lane High = Normal Operation(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	Digital Display Port Concurrent Operation	Low=Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CRTL_DATA		Low=No SDVO Device Present (default) High=SDVO Device Present
DDPC_CTRLDATA		Low=DisplayPort disabled (default) High=DisplayPort device present

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Title: Cantiga(2 of 7)

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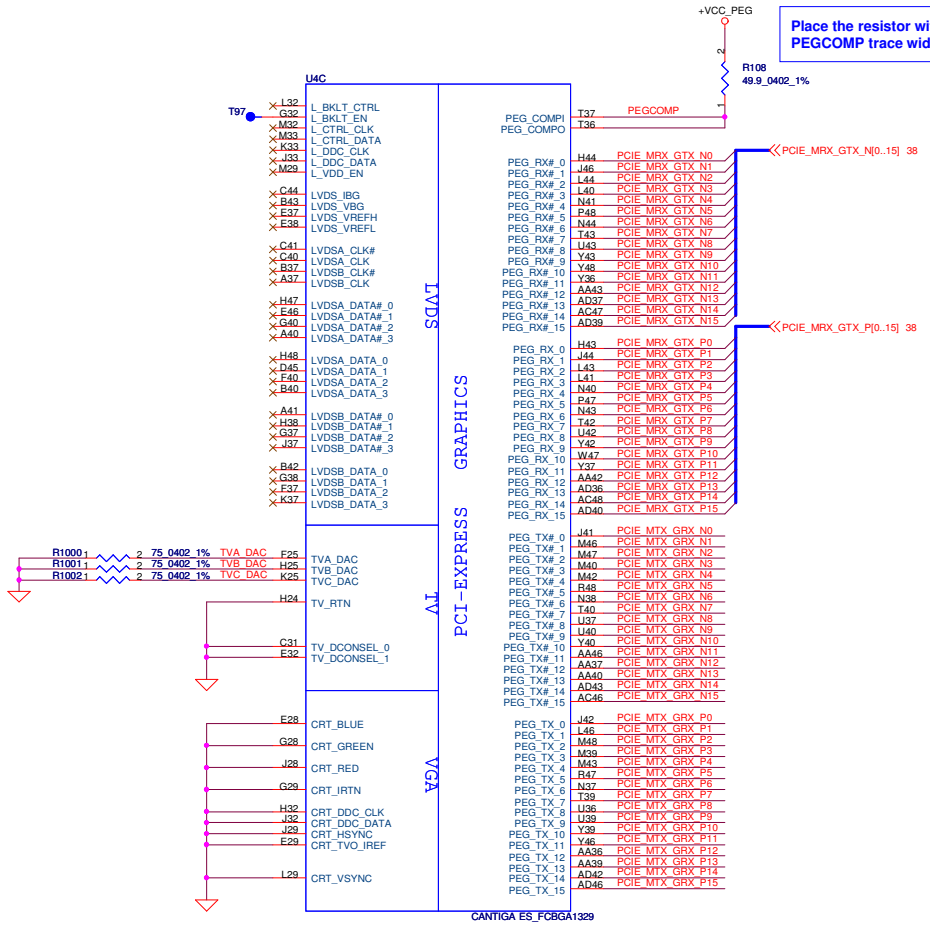

Place the resistor within 500mils of the GMCH PEGCOMP trace widht and spacing is 20/25 mils.

PCE-Express Graphics

PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15] 38
PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] 38

PCIE_MTX_GRX_P0	C77	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P0
PCIE_MTX_GRX_N0	C78	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N0
PCIE_MTX_GRX_P1	C79	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P1
PCIE_MTX_GRX_N1	C80	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N1
PCIE_MTX_GRX_P2	C81	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P2
PCIE_MTX_GRX_N2	C82	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N2
PCIE_MTX_GRX_P3	C83	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P3
PCIE_MTX_GRX_N3	C84	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N3
PCIE_MTX_GRX_P4	C85	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P4
PCIE_MTX_GRX_N4	C86	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N4
PCIE_MTX_GRX_P5	C87	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P5
PCIE_MTX_GRX_N5	C88	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N5
PCIE_MTX_GRX_P6	C89	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P6
PCIE_MTX_GRX_N6	C90	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N6
PCIE_MTX_GRX_P7	C91	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P7
PCIE_MTX_GRX_N7	C92	2	1	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N7
PCIE_MTX_GRX_P8	C93	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P8
PCIE_MTX_GRX_N8	C94	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N8
PCIE_MTX_GRX_P9	C95	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P9
PCIE_MTX_GRX_N9	C96	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N9
PCIE_MTX_GRX_P10	C97	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P10
PCIE_MTX_GRX_N10	C98	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N10
PCIE_MTX_GRX_P11	C99	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P11
PCIE_MTX_GRX_N11	C100	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N11
PCIE_MTX_GRX_P12	C101	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P12
PCIE_MTX_GRX_N12	C102	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N12
PCIE_MTX_GRX_P13	C103	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P13
PCIE_MTX_GRX_N13	C104	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N13
PCIE_MTX_GRX_P14	C105	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P14
PCIE_MTX_GRX_N14	C106	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N14
PCIE_MTX_GRX_P15	C107	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_P15
PCIE_MTX_GRX_N15	C108	1	2	0.1U 0402 10V7K-D	PCIE_MTX_C_GRX_N15

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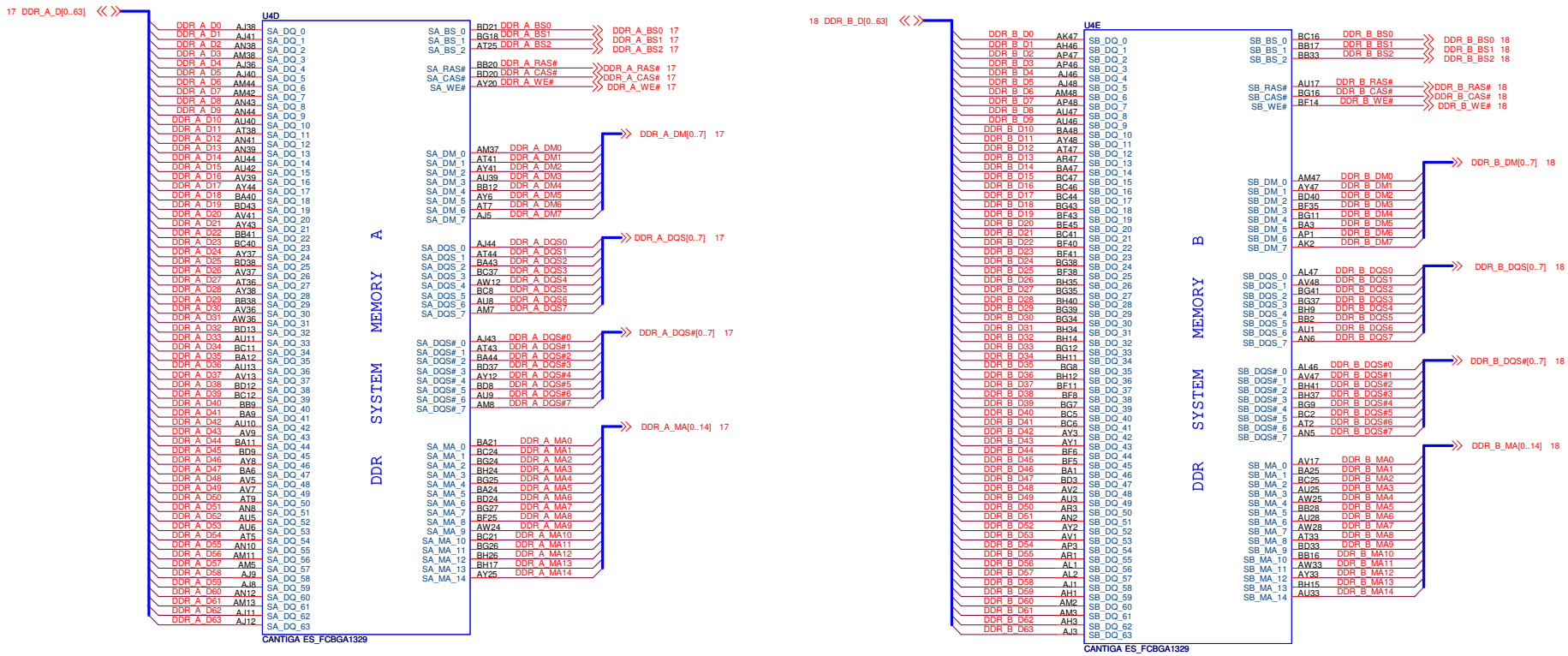

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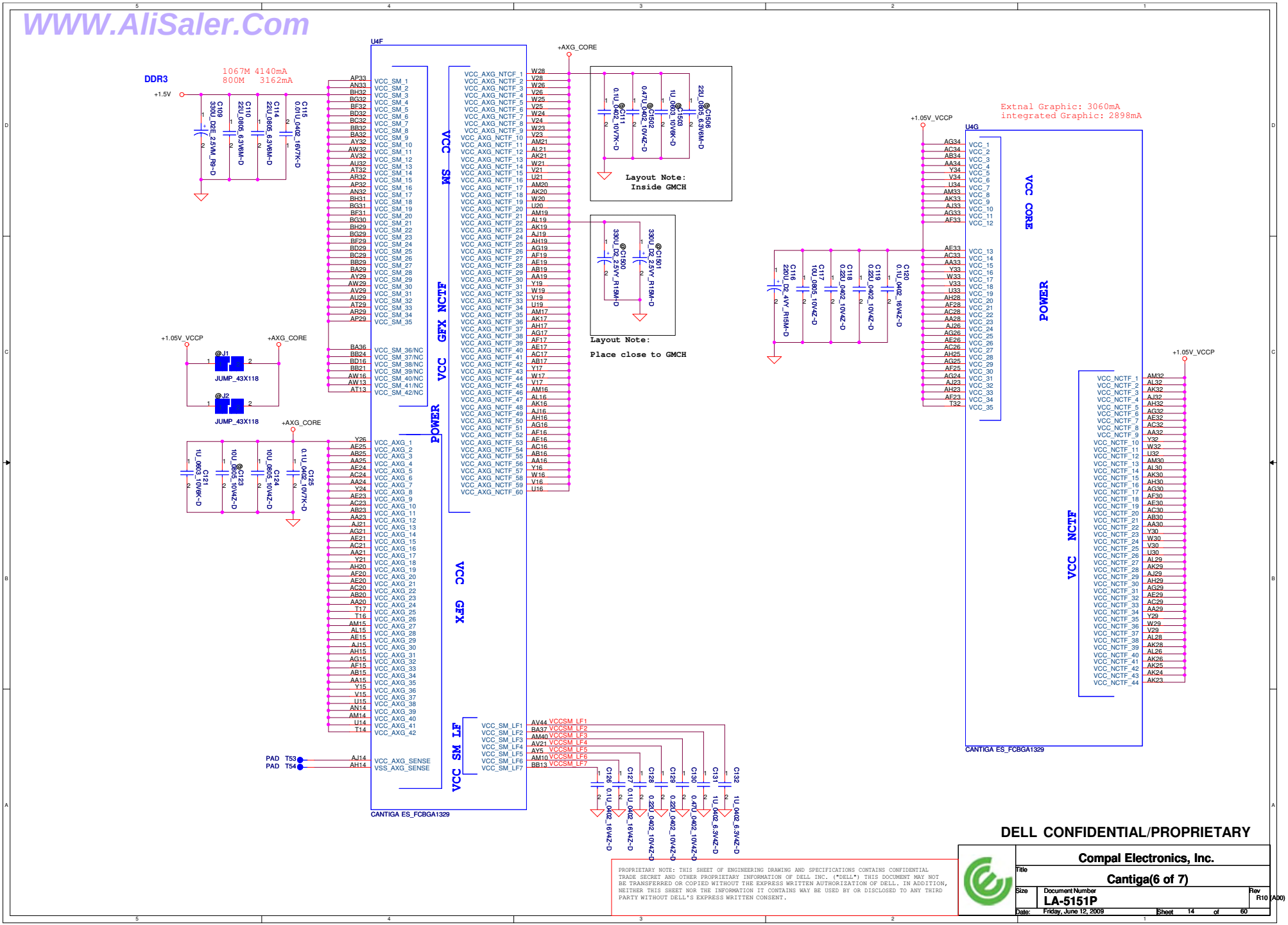

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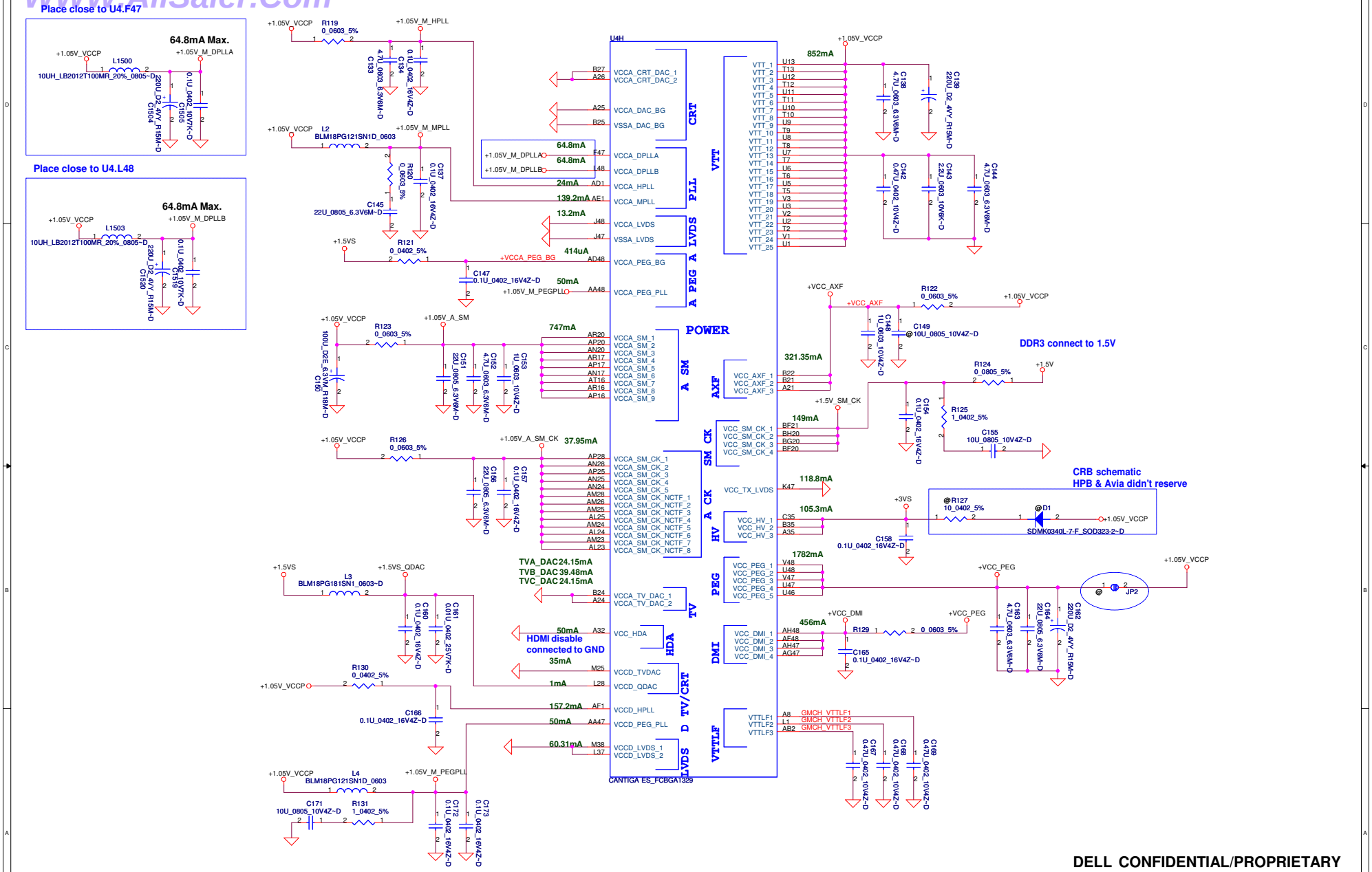

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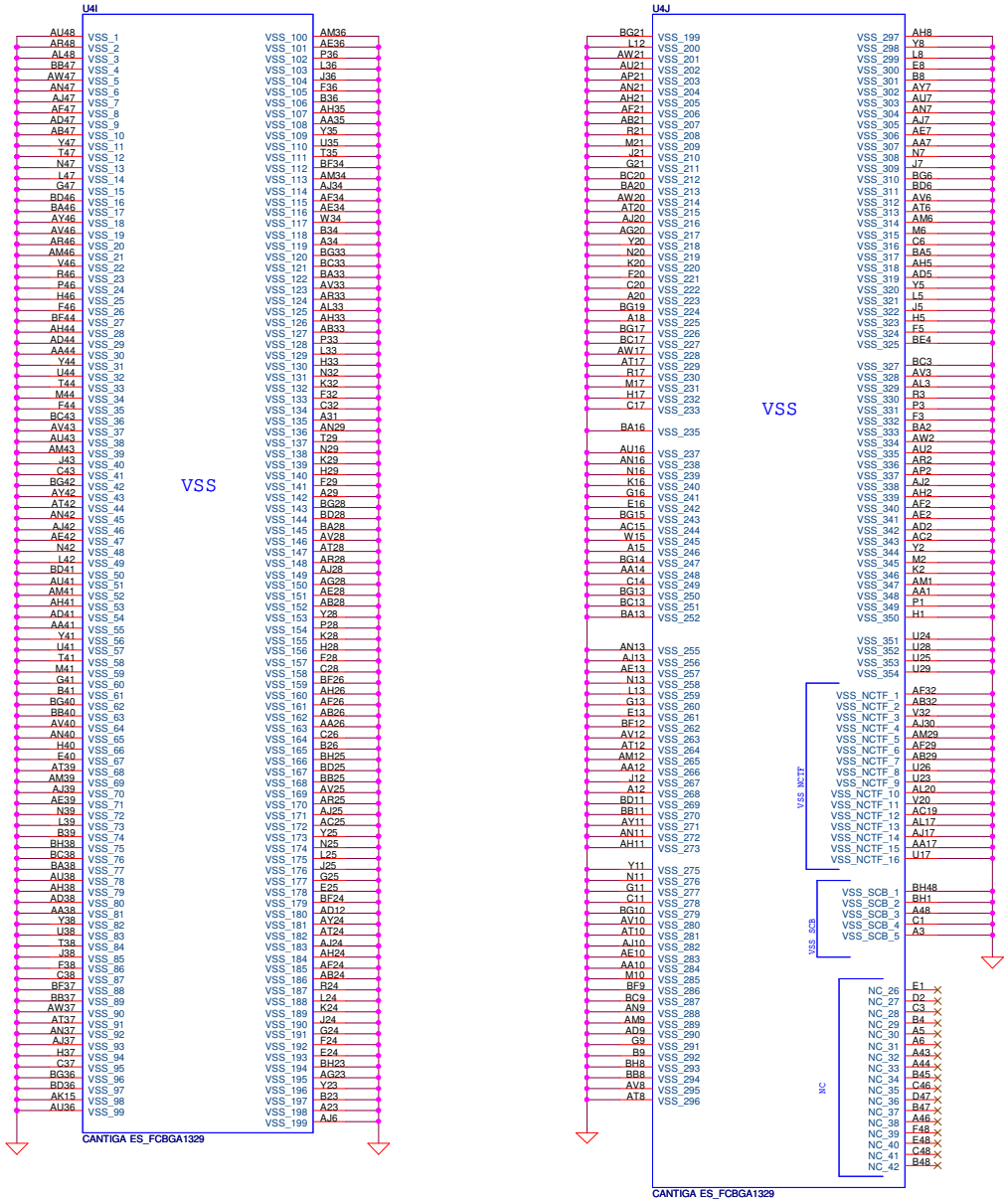

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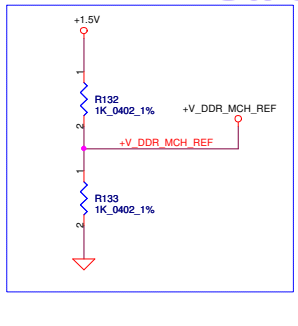
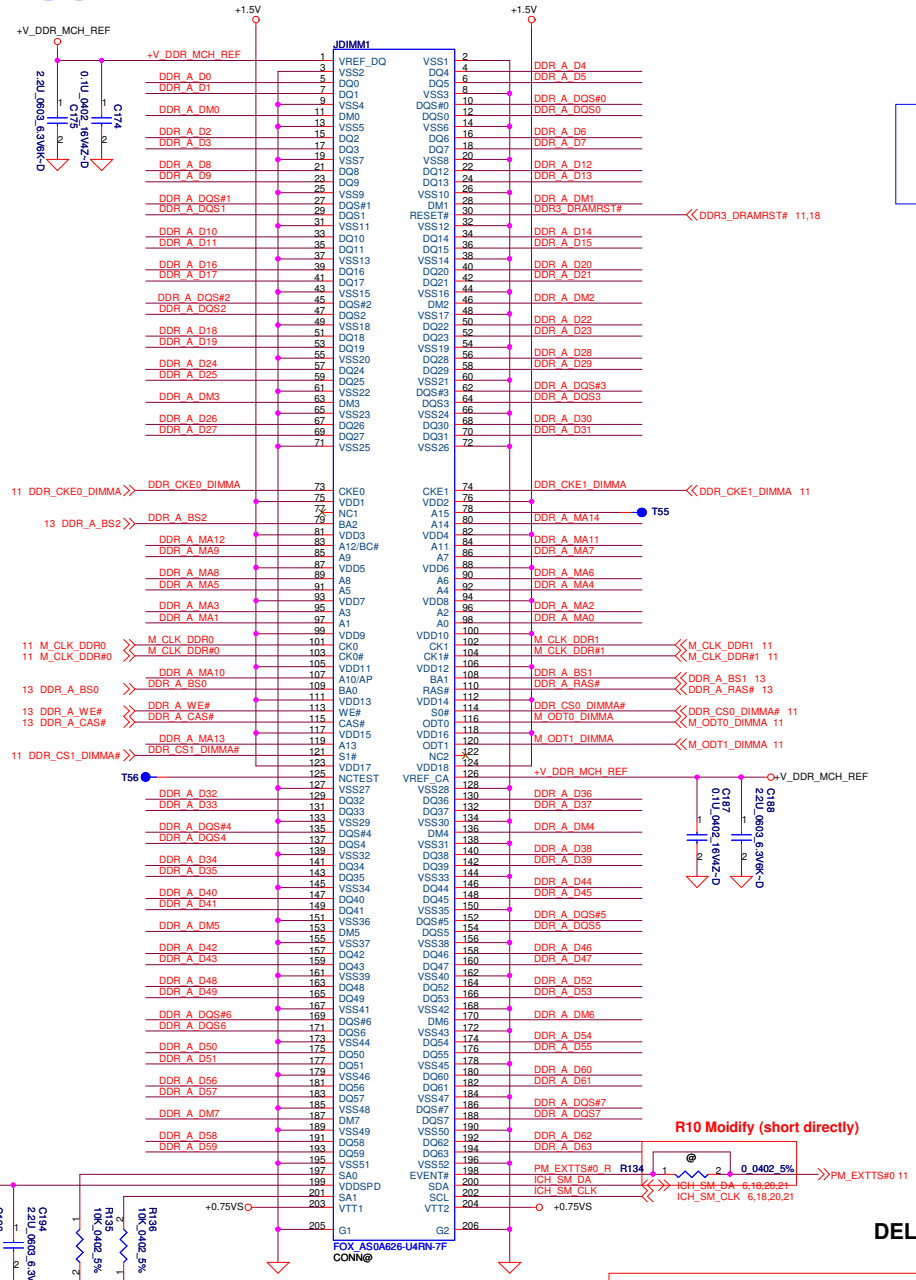
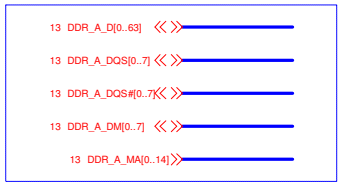
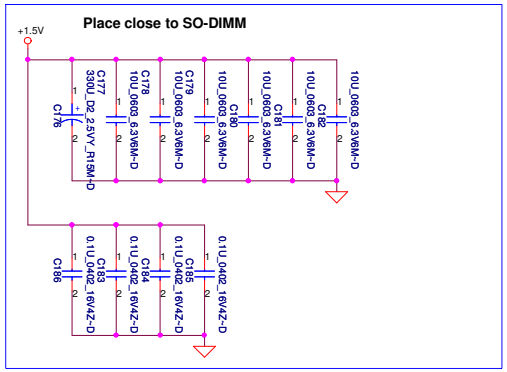


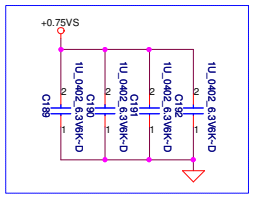


DDR3 SO-DIMM/Standard Type

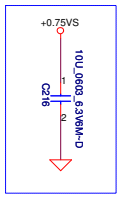
Note :
DDR3 command & contorl signals need no termination.
DDR2 command & command signals 56 ohm pull up to VccSus0_9







Place close to JDIMM pin 203 and 204



Place between 2 DIMMs

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Title: DDRIII SO-DIMM A SLOT			
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Date: Friday, June 12, 2009	Sheet 17 of 60		

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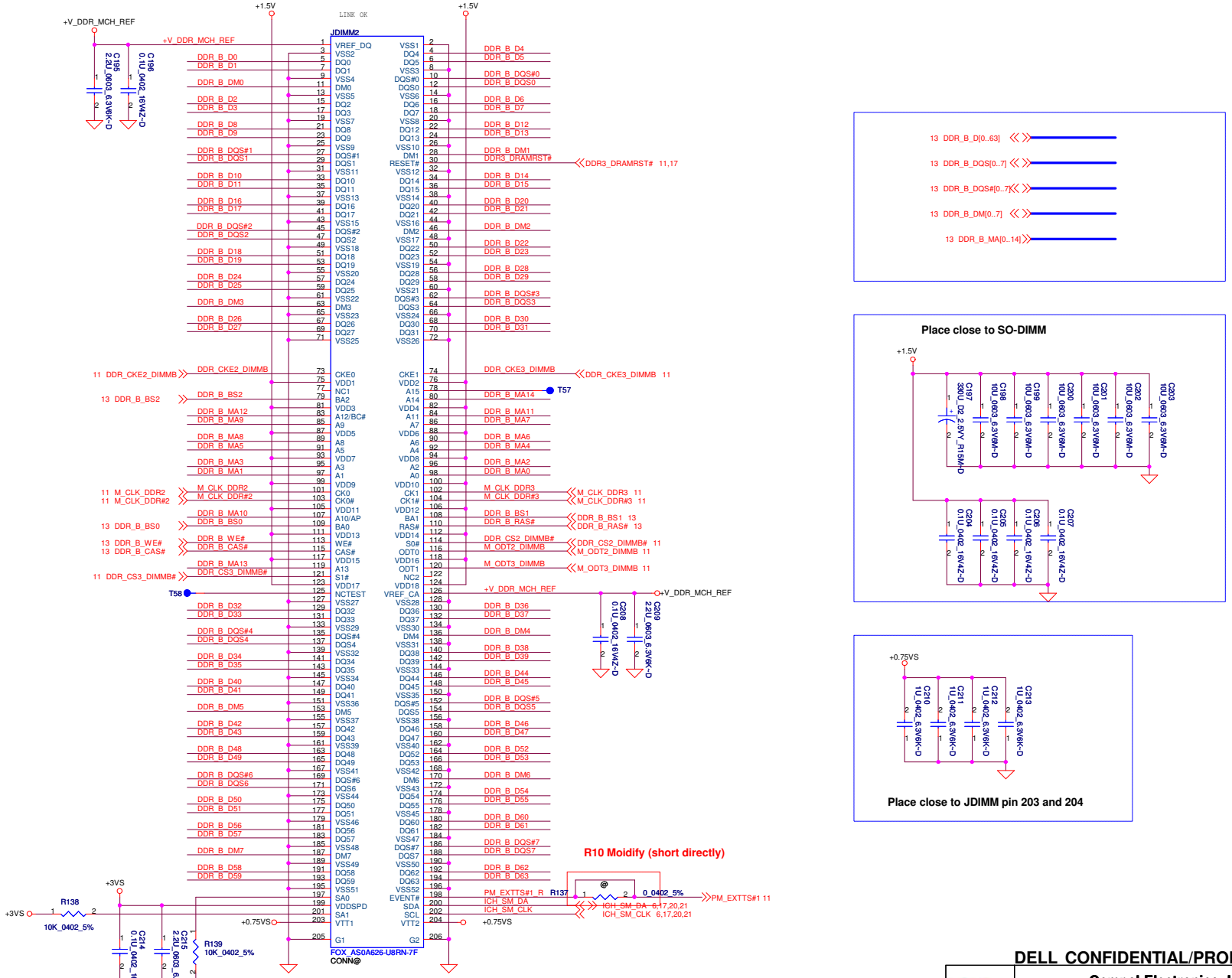

DDR3 SO-DIMM/Standard Type

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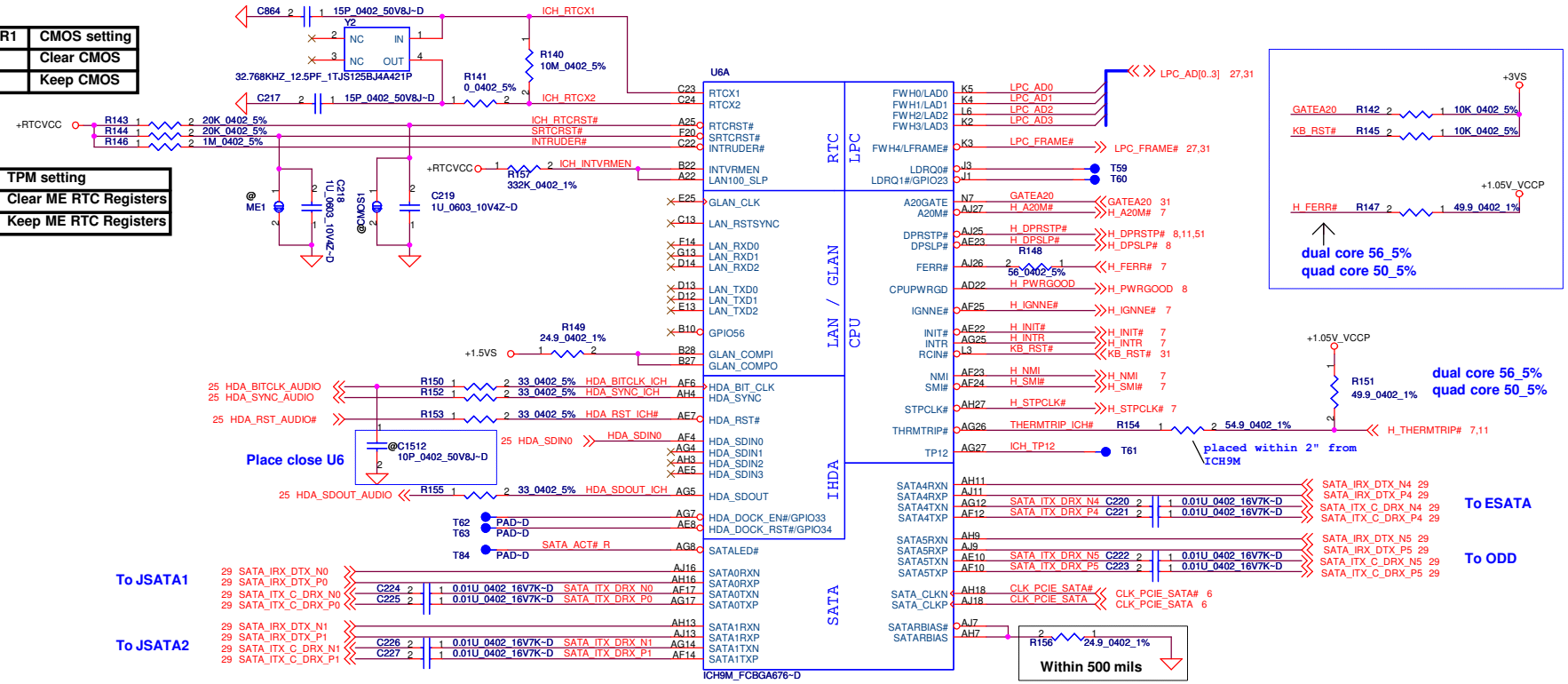
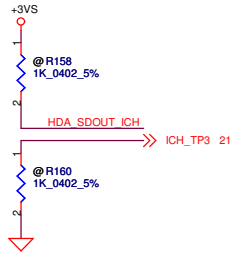
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



P/N : SA00002G12L (S IC AF82801IEM SLB8P A3 PBGA676P ICH9ME)

XOR Chain Entrance Strap		
ICH TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



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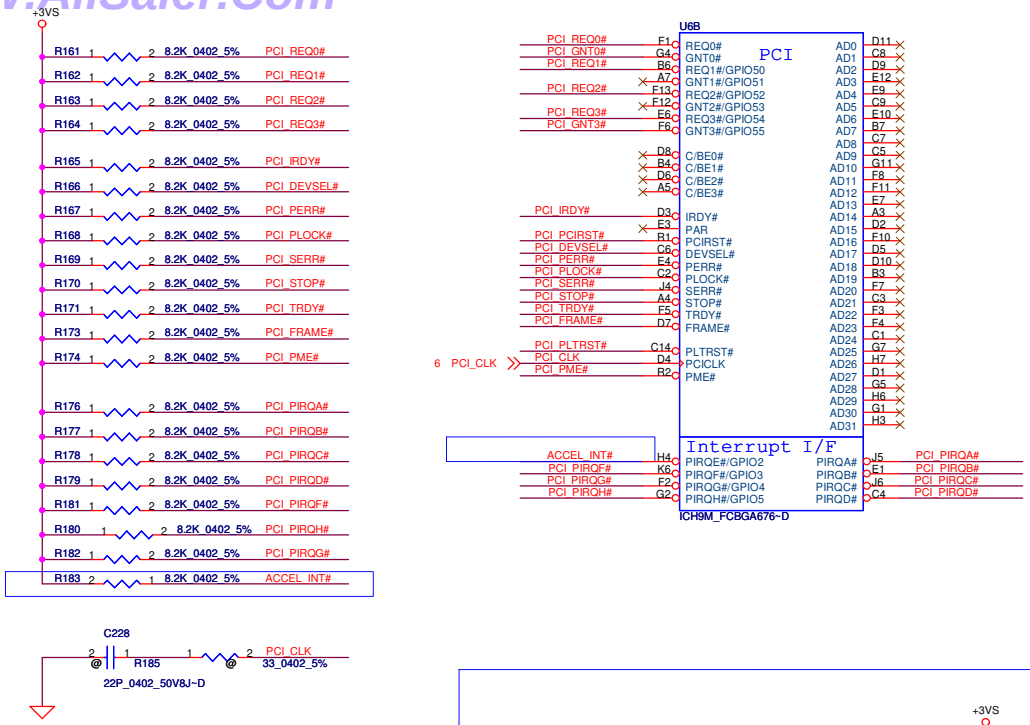
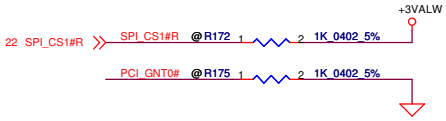
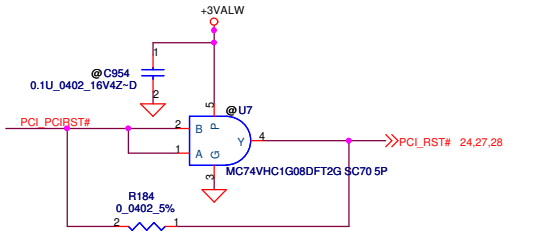


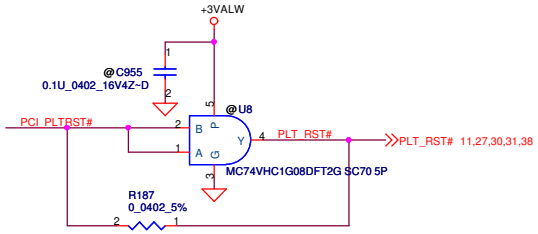
Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

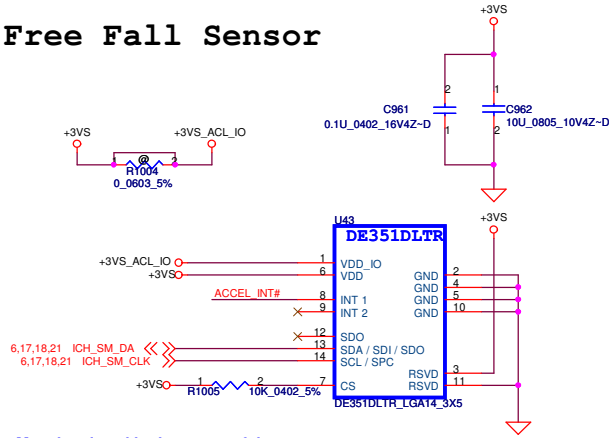


GNT0 & SPI_CS#1 have a weak internal pull up





Free Fall Sensor

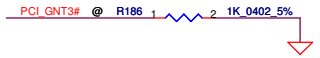


Must be placed in the center of the system.

P/N : SA000039C00 (S IC DE351DLTR LGA 14P MOTION SENSOR)

A16 swap override Strap

PCI_GNT3#	Low= A16 swap override Enble High= Default *



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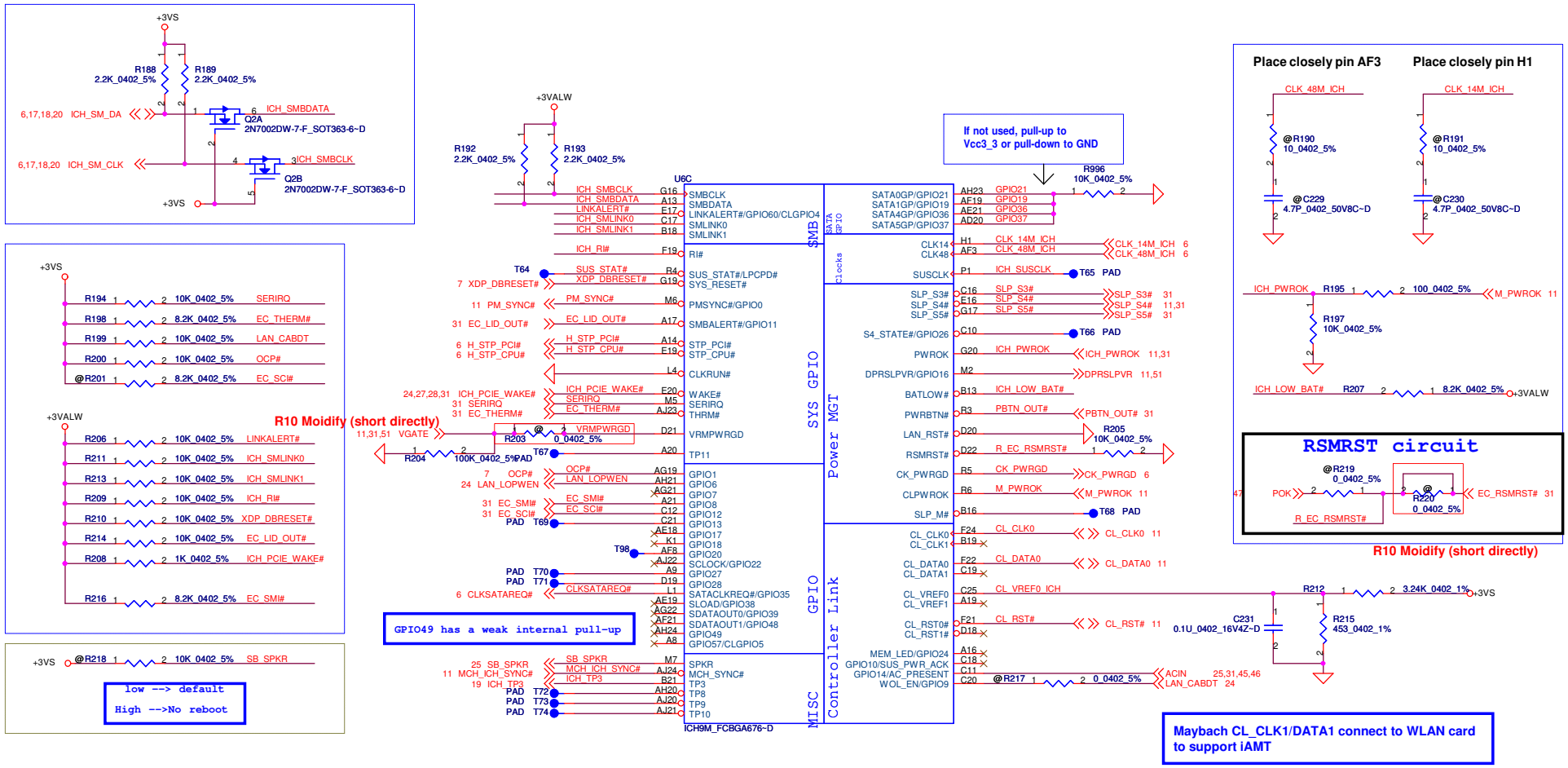

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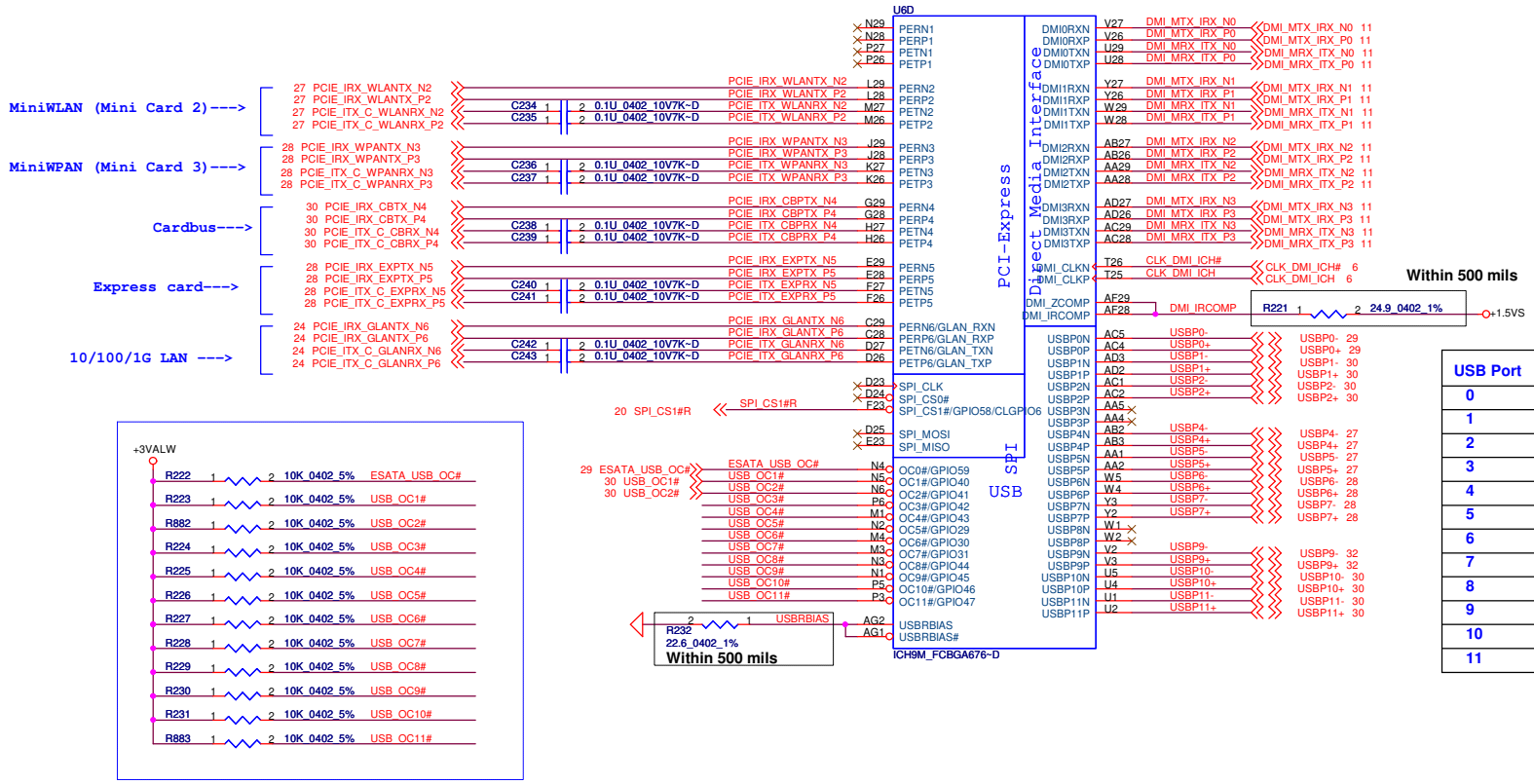

USB Port	Device
0	USB&ESATA
1	Reader board
2	USB board
3	NC
4	WLAN
5	WWAN
6	WPAN
7	Express
8	NC
9	Touch screen
10	Bluetooth
11	Camera

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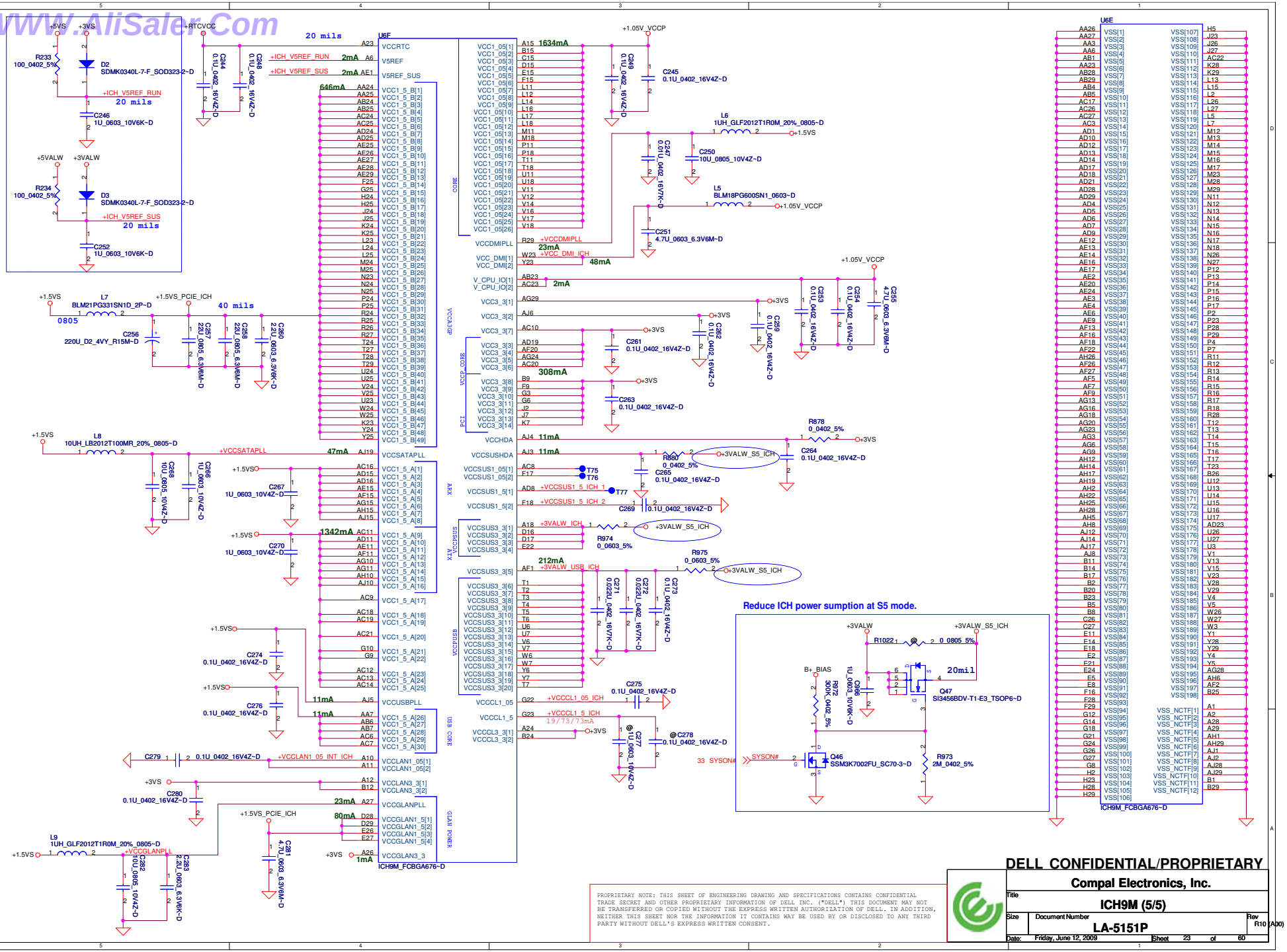

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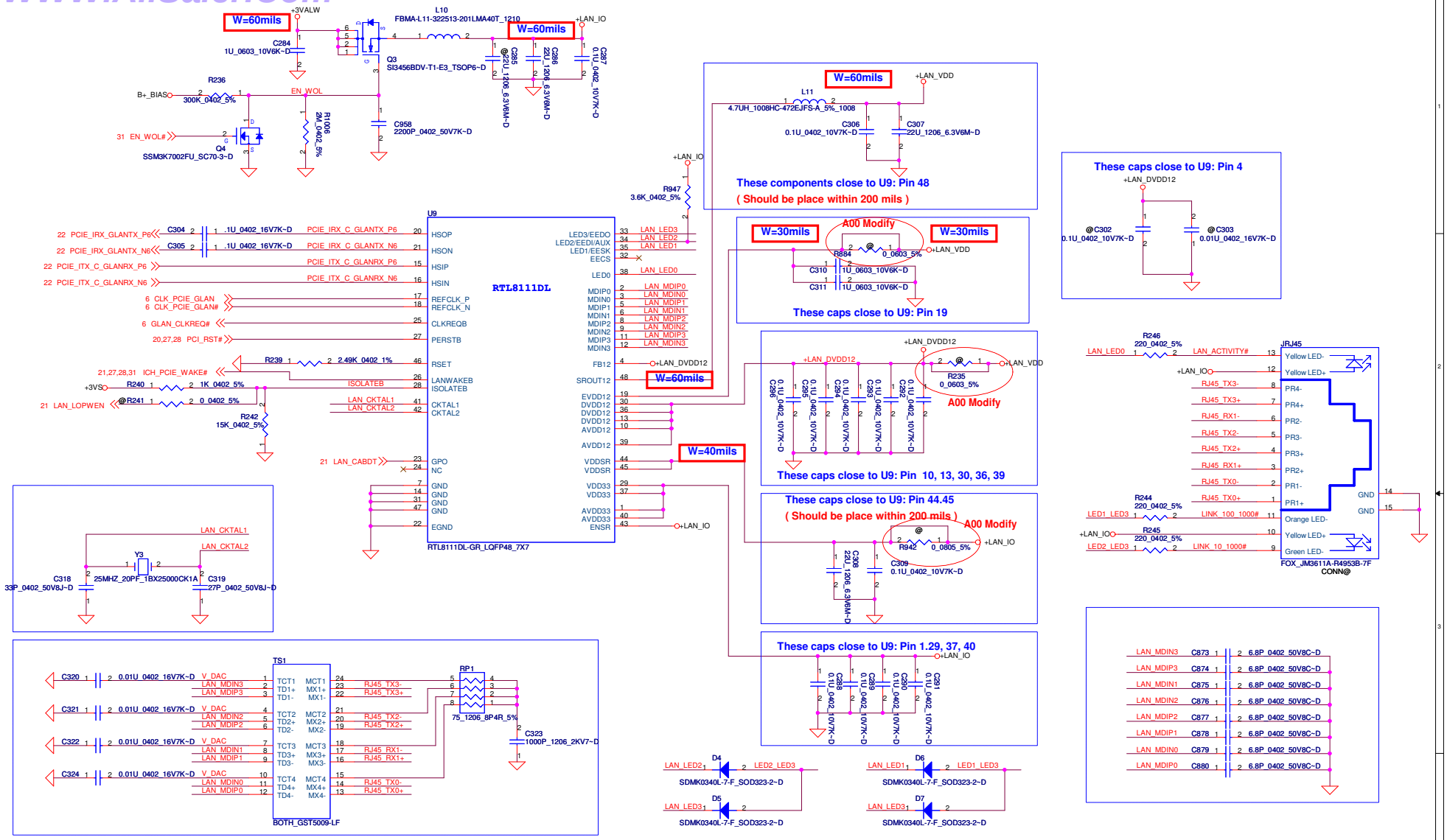

LEDS1-0	0 0	0 1	1 0	1 1
LED0	Tx / Rx	Tx / Rx	Tx	LINK10 / ACT
LED1	LINK100	LINK10 /100 / 1000	LINK	LINK100 / ACT
LED2	LINK10	LINK10 / 100	Rx	FULL
LED3	LINK1000	LINK1000	FULL	LINK1000 / ACT

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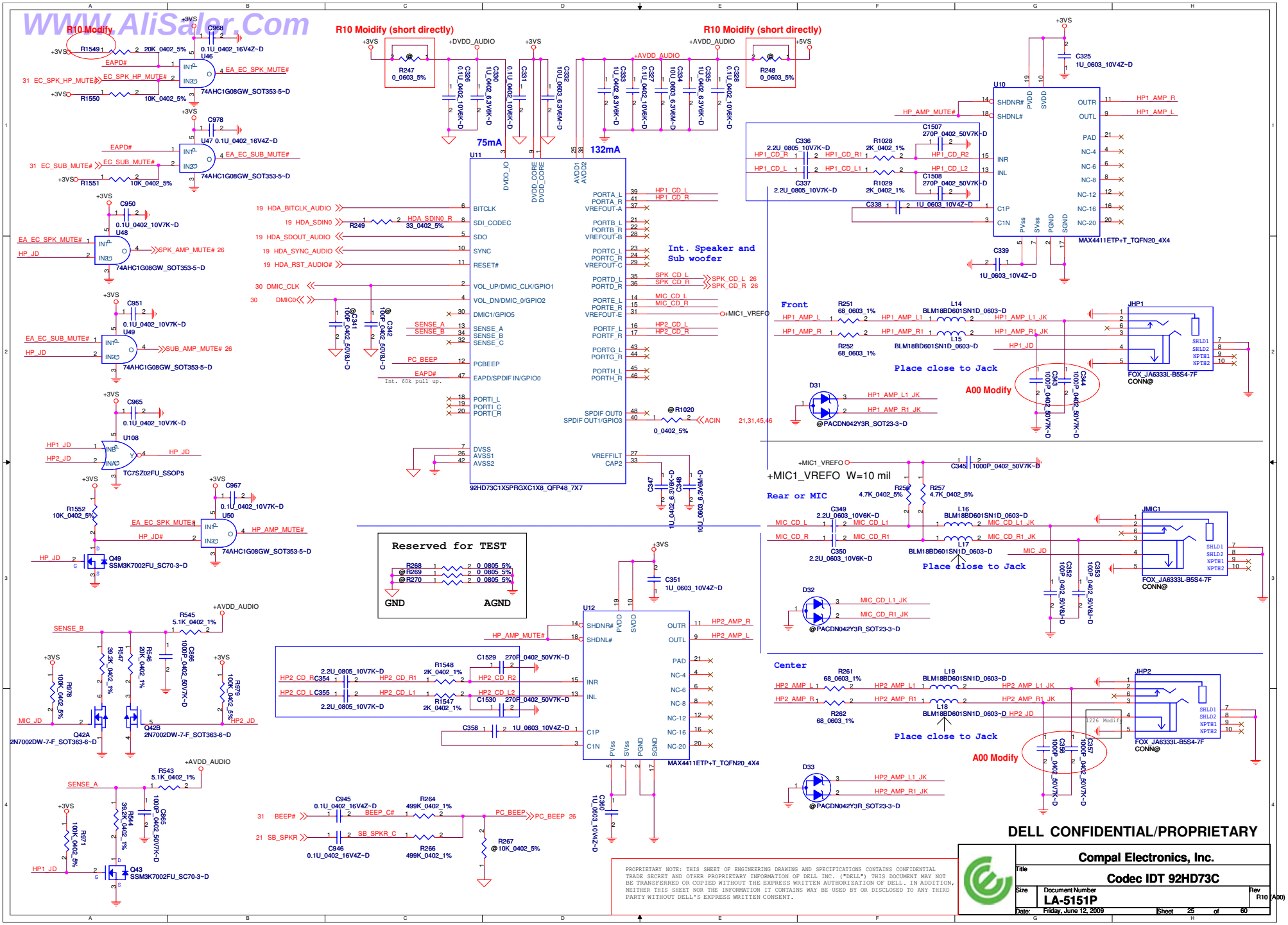

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Size	Document Number: LA-5151P
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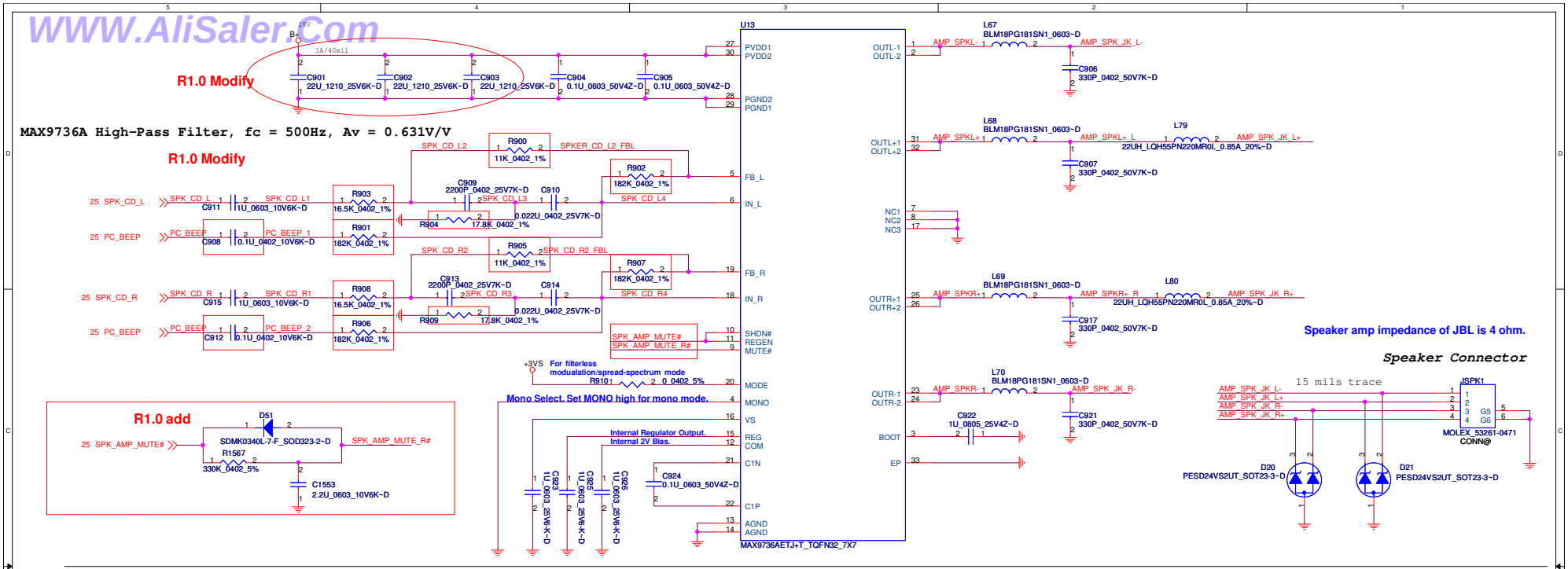

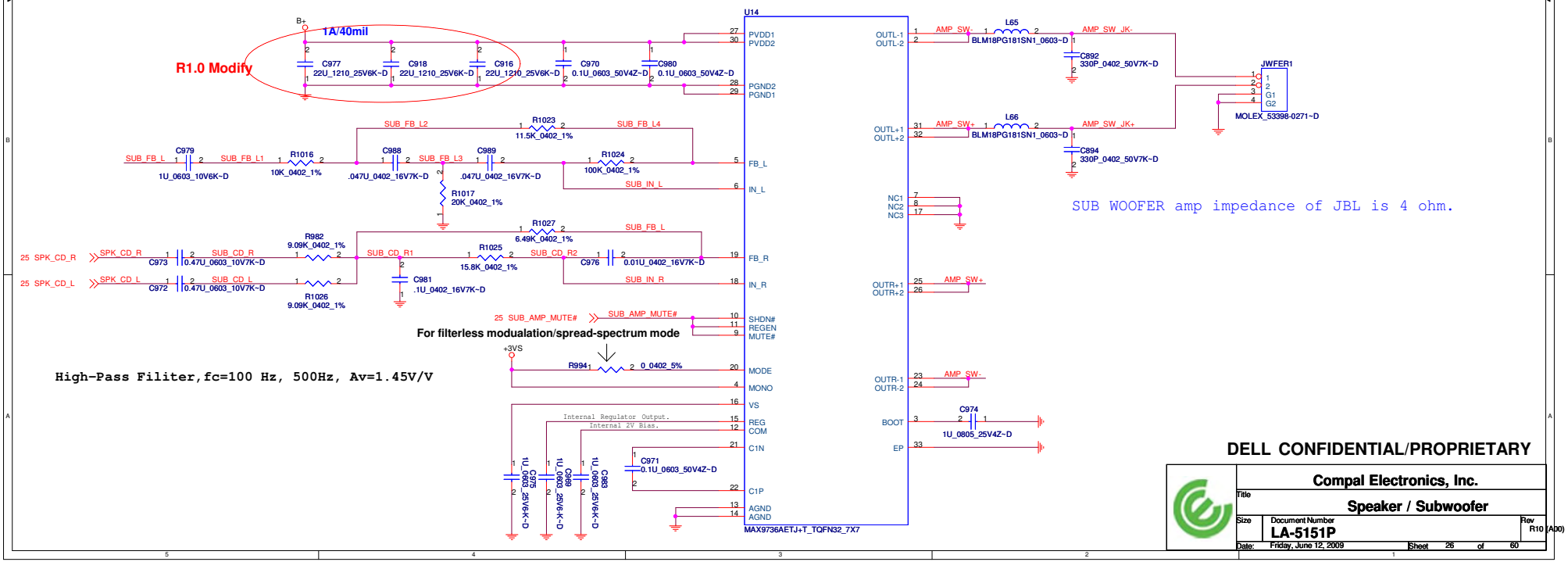

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Compal Electronics, Inc.		
Title: Speaker / Subwoofer		
Size	Document Number: LA-5151P	Rev: R10 (A00)
Date: Friday, June 12, 2009	Sheet 26 of 60	

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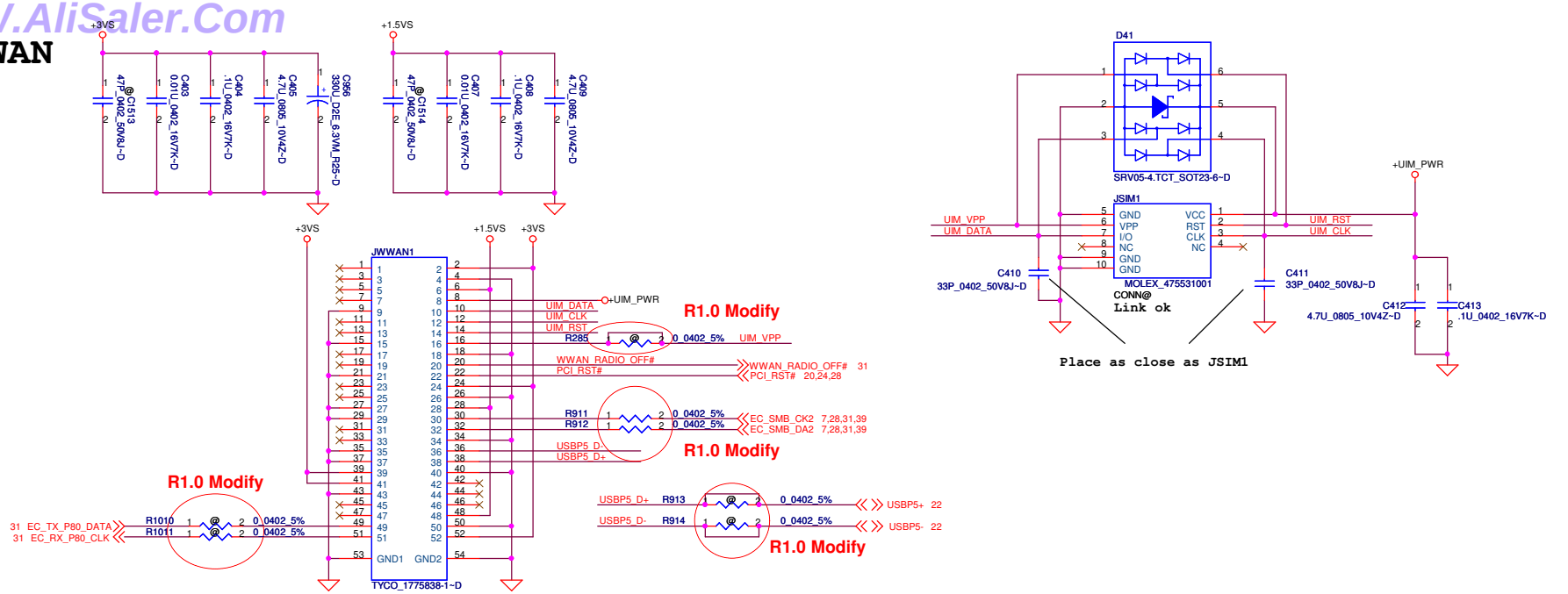
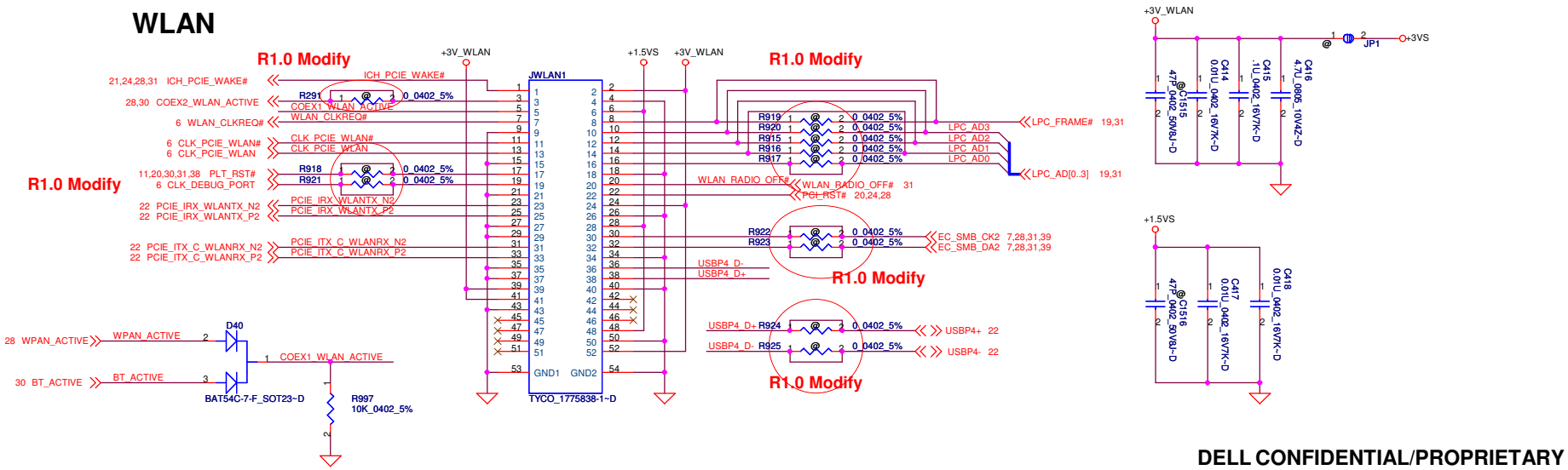
WWAN



WLAN



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Compal Electronics, Inc.	
Title	Mini Card_WLAN/WWAN
Size	Document Number: LA-5151P
Rev	R10 (A00)
Date: Friday, June 12, 2009	Sheet 27 of 60

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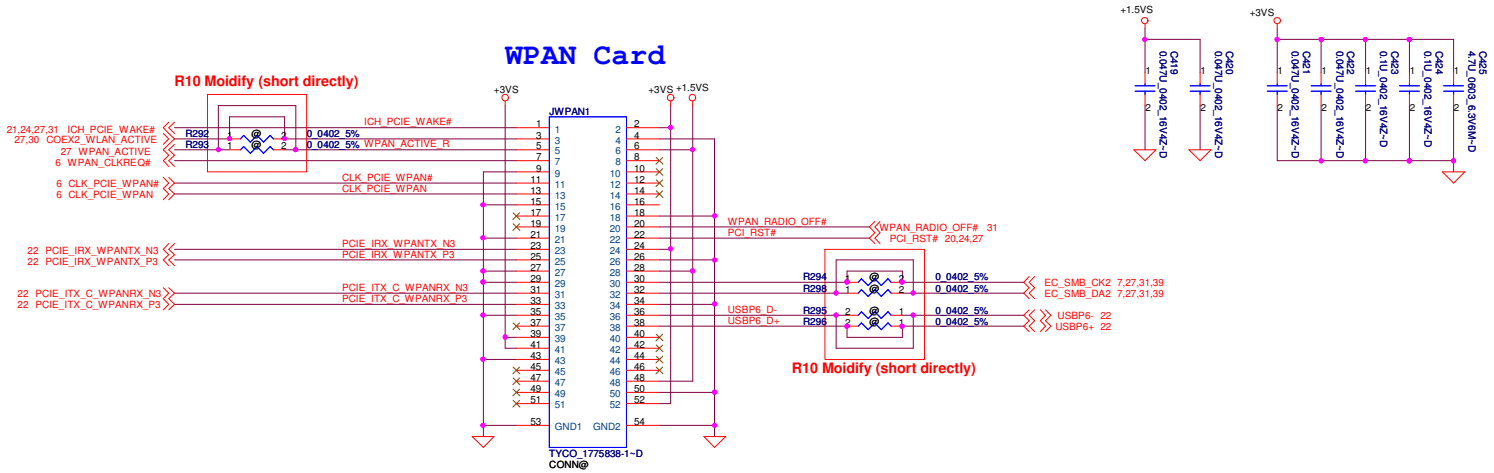
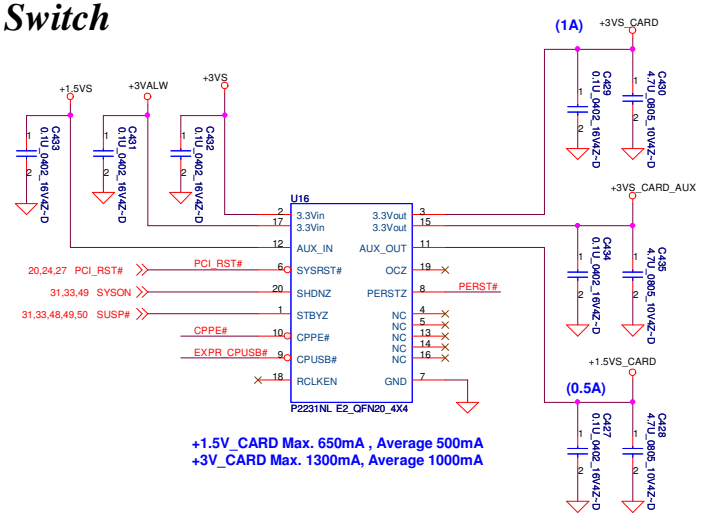
WPAN Card

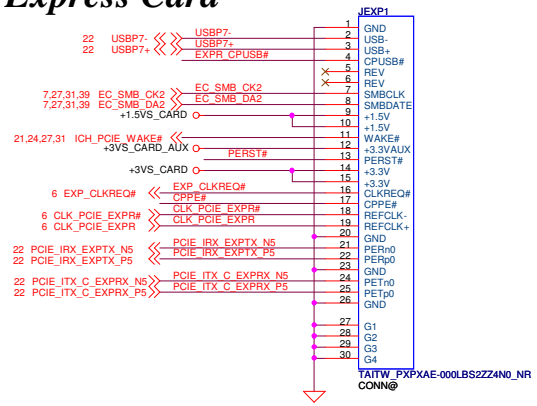


Express Card Power Switch



+1.5V_CARD Max. 650mA , Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA

Express Card



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Compal Electronics, Inc.	
Title	WPAN / Express Card
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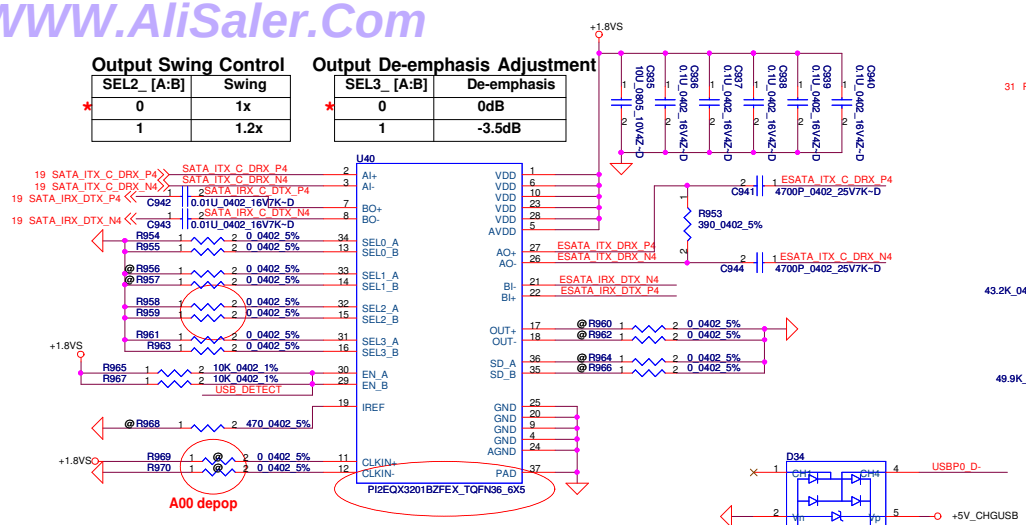
Output Swing Control

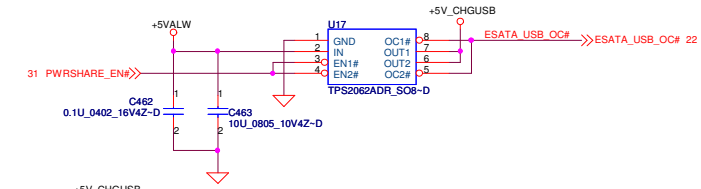
SEL2_ [A:B]	Swing
* 0	1x
1	1.2x

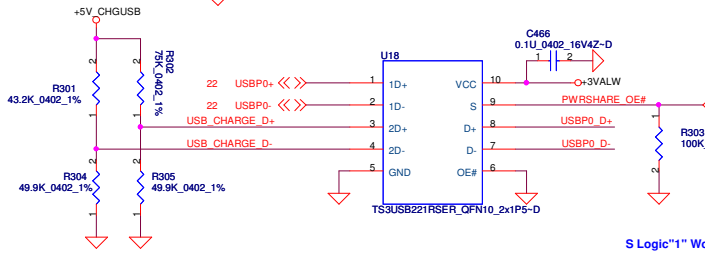
Output De-emphasis Adjustment

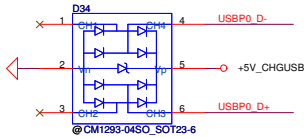
SEL3_ [A:B]	De-emphasis
* 0	0dB
1	-3.5dB



A00 change to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P)



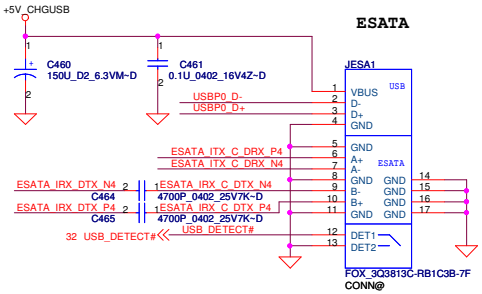


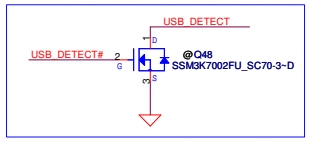


Place close JESA1

S Logic"1" Work from BKT

S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

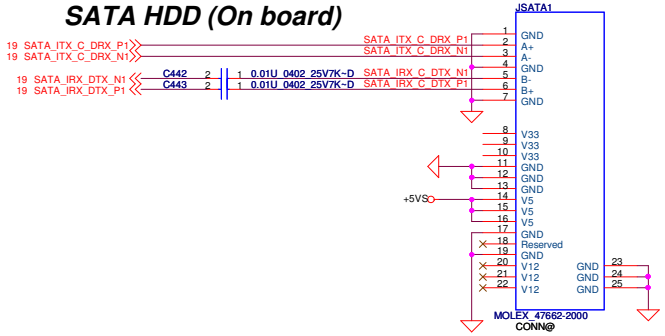


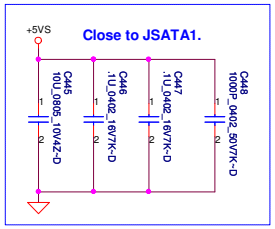


Equalizer Selection

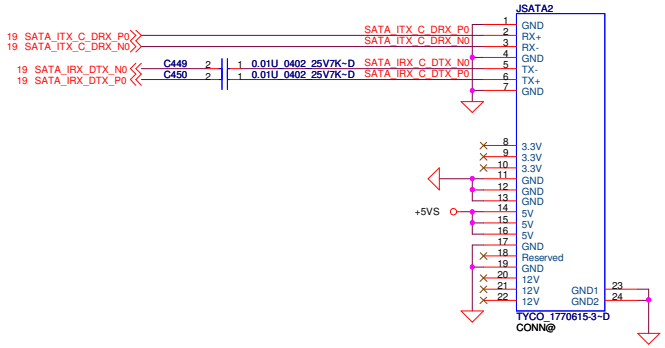
SEL0_ [A:B]	SEL1_ [A:B]	Compliance Channel
0	0	no equalization
* 0	1	[0:2.5dB] @ 1.6 GHz
1	0	[2.5:4.5dB] @ 1.6 GHz
1	1	[4.5:6.5dB] @ 1.6 GHz

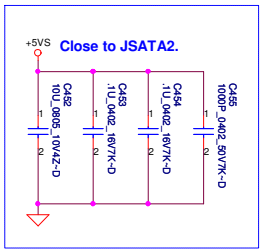
SATA HDD (On board)



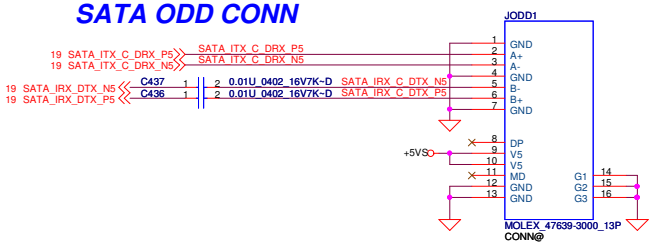


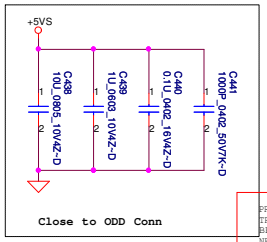
SATA HDD





SATA ODD CONN





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Title: ODD / SATA CONN			
Size	Document Number: LA-5151P		Rev: R10 (A00)
Date: Friday, June 12, 2009	Sheet 29 of 60		

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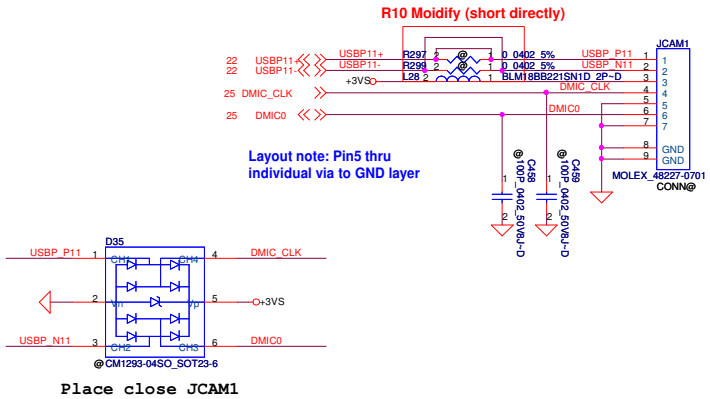

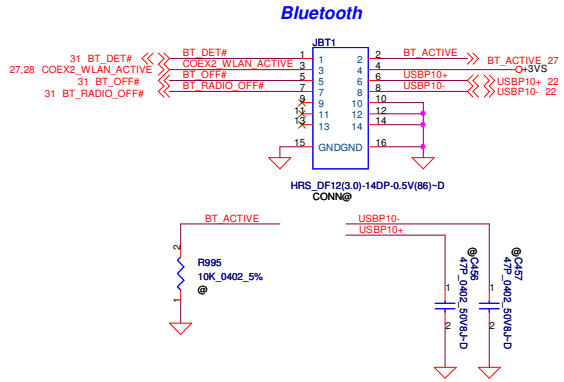

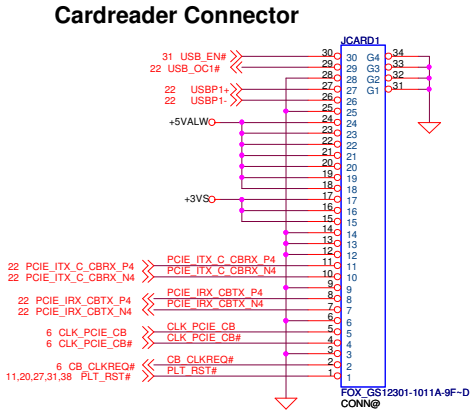

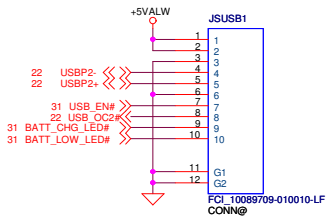

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Compal Electronics, Inc.			
Title: USB / ESATA / BT / CAMARA			
Size	Document Number: LA-5151P		Rev: R10 (A00)
Date: Friday, June 12, 2009	Sheet 30 of 60		

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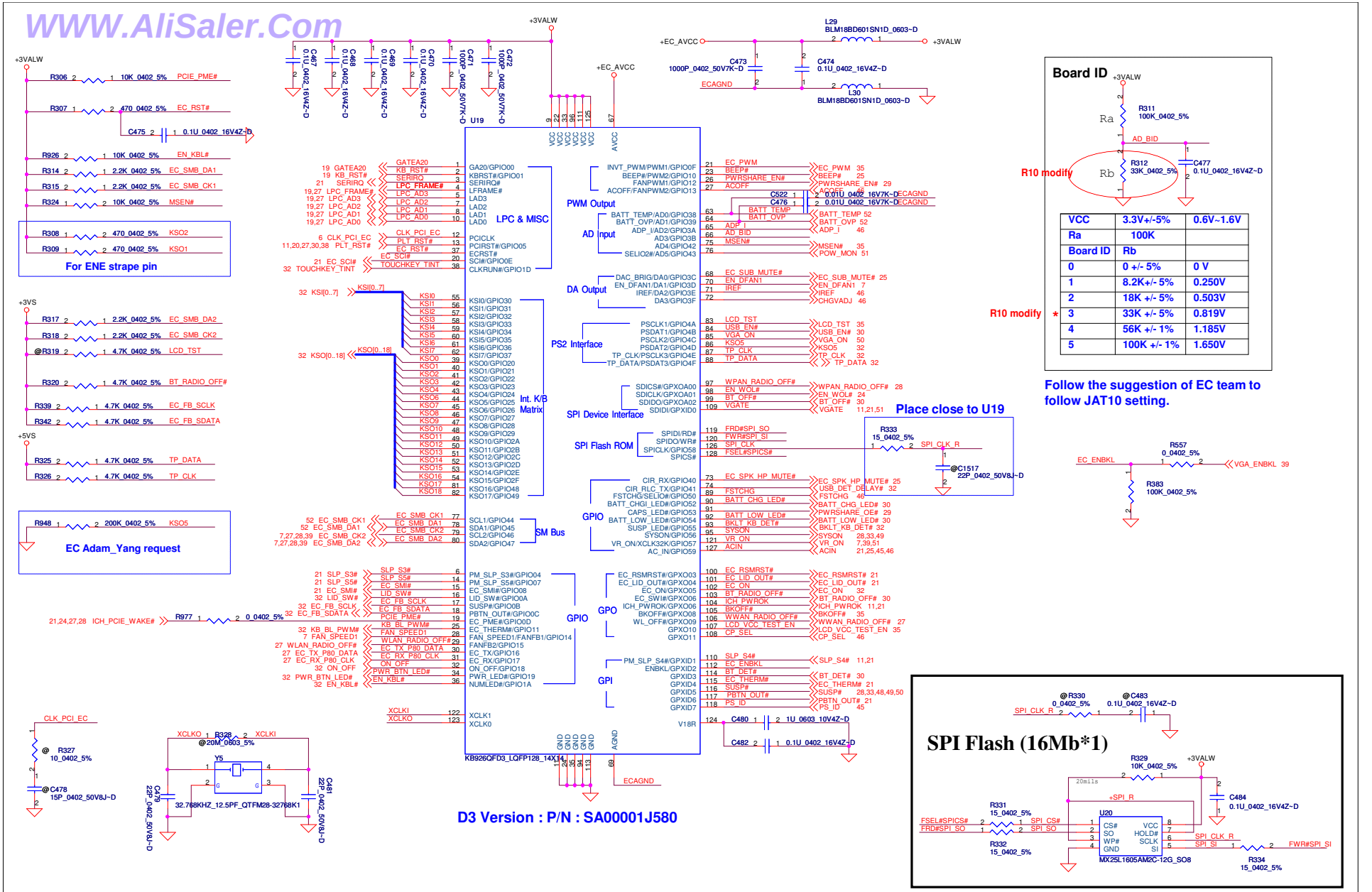

Board ID		
VCC	3.3V+/-5%	0.6V~1.6V
Ra	100K	
Board ID	Rb	
0	0 +/- 5%	0 V
1	8.2K+/- 5%	0.250V
2	18K +/- 5%	0.503V
* 3	33K +/- 5%	0.819V
4	56K +/- 1%	1.185V
5	100K +/- 1%	1.650V

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Compal Electronics, Inc.

Title: BIOS & EC I/O Port

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Date: Friday, June 12, 2009 | Sheet 31 of 60

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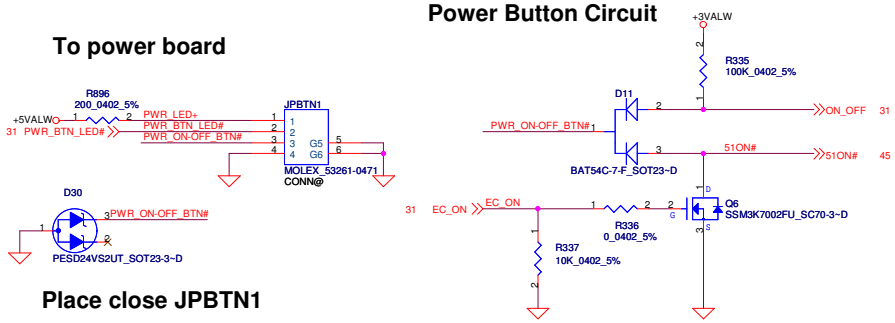
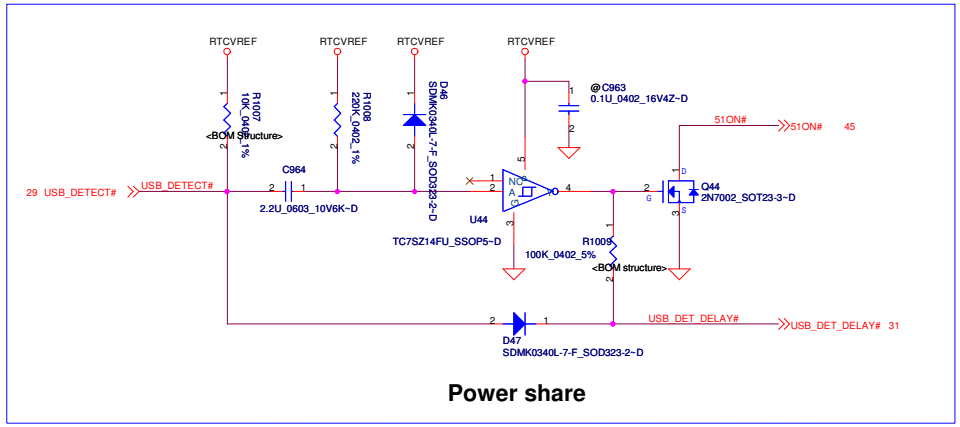
Power Button Circuit

To power board

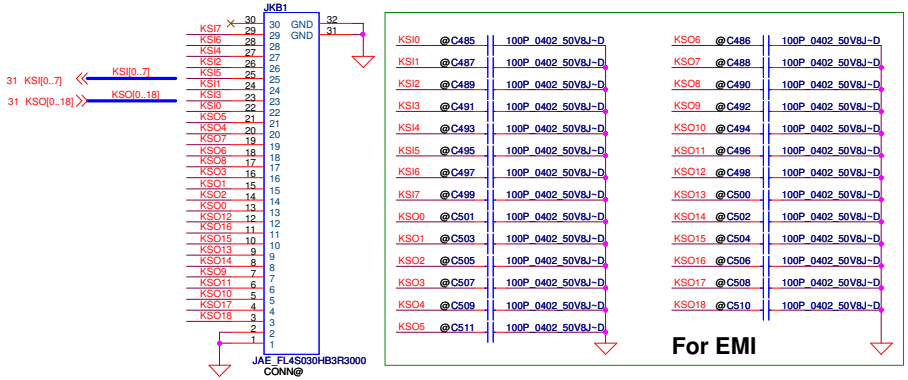


Place close JPBTN1



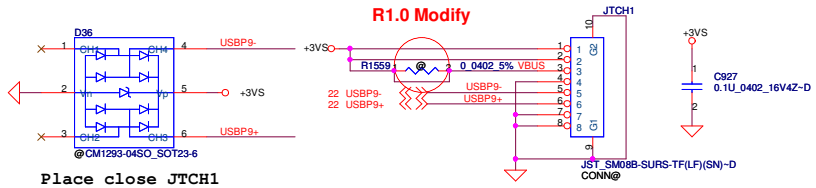
Power share

INT_KB_Conn.1



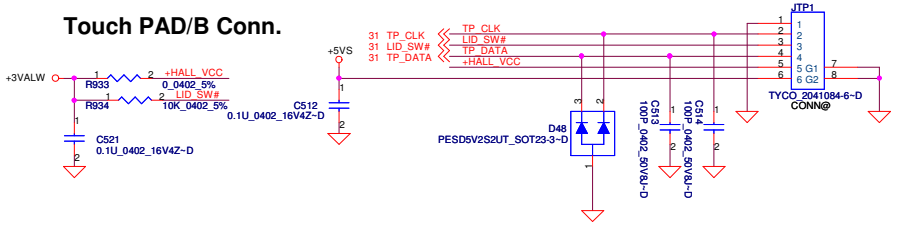
For EMI

Touch Screen Connector

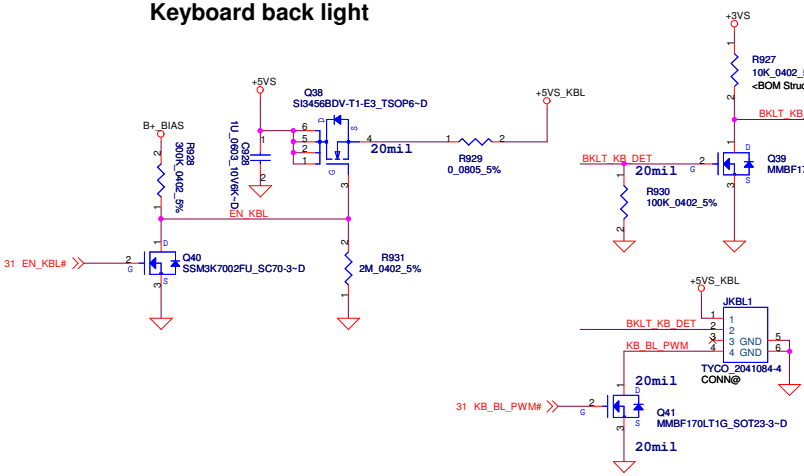


Place close JTCH1

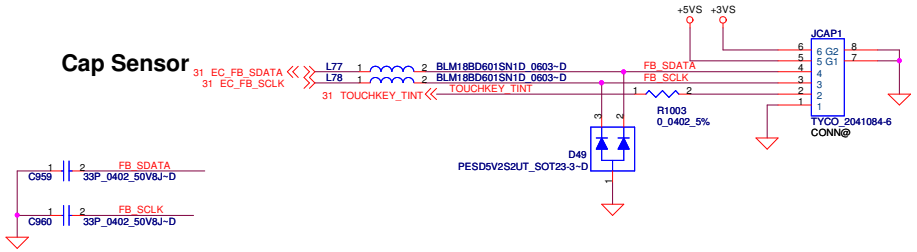
Touch PAD/B Conn.



Keyboard back light



Cap Sensor



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Compal Electronics, Inc.			
Title: PWROK/BTN/KB/Touch Pad			
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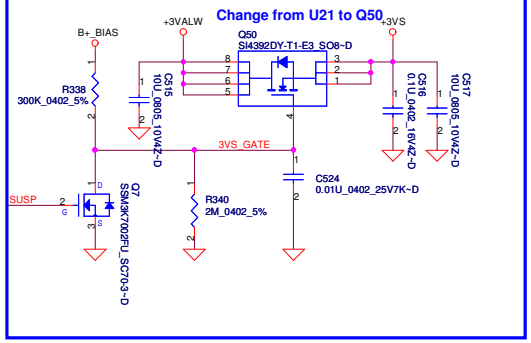
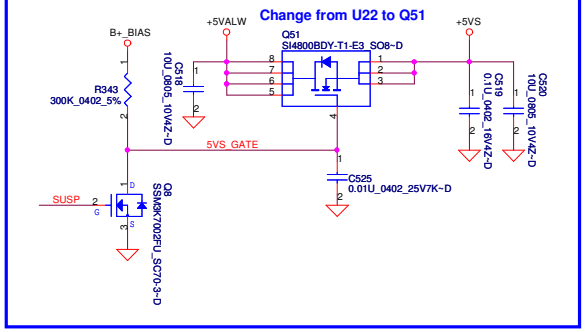
Voltage divider (7/8 VCC) on 3VS_gate

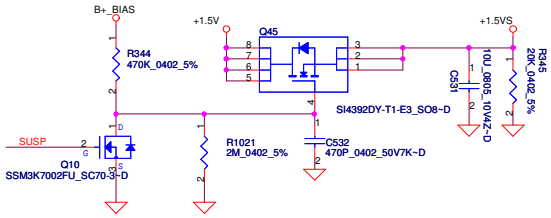
+3VALW to +3VS Transfer



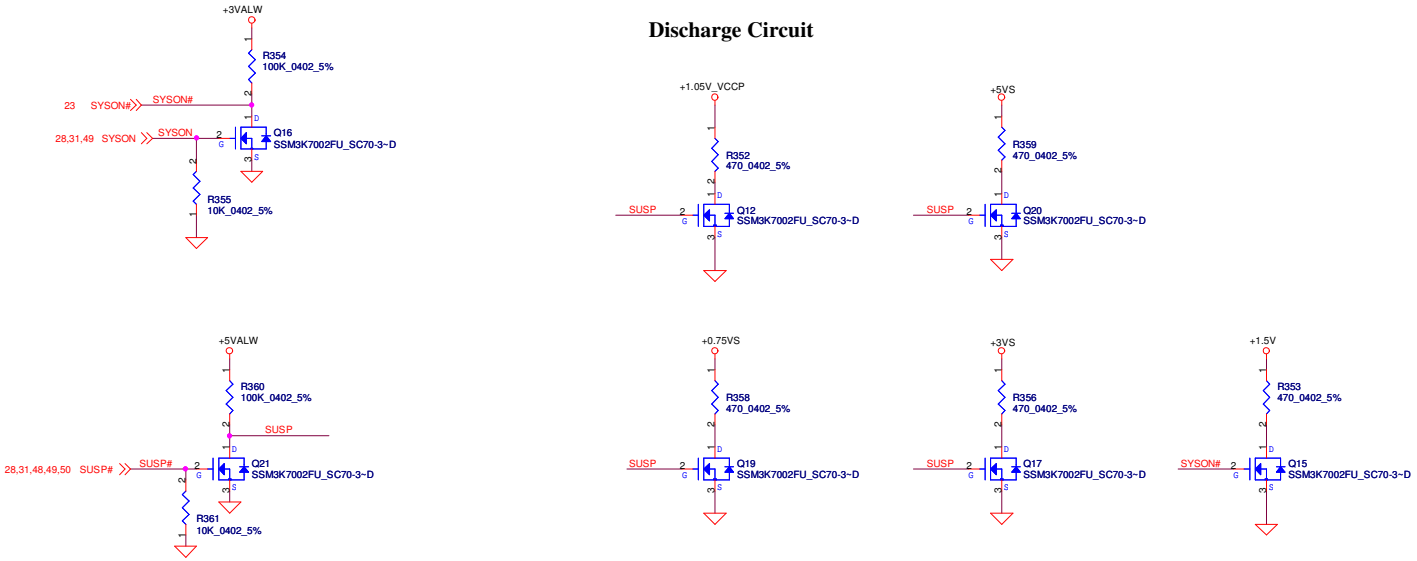
+5VALW to +5VS Transfer



+1.5V to +1.5VS Transfer



Discharge Circuit



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Compal Electronics, Inc.		
Title: DC/DC Circuits		
Size	Document Number: LA-5151P	Rev: R10 (A00)
Date: Friday, June 12, 2009	Sheet 33 of 60	

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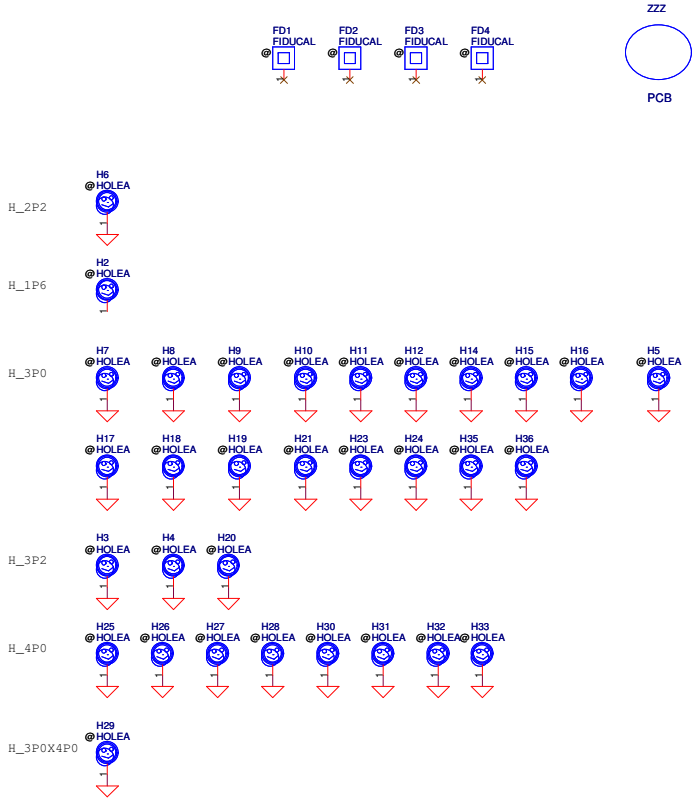

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Compal Electronics, Inc.		
Title: Screw		
Size	Document Number: LA-5151P	Rev: R10 (A00)
Date: Friday, June 12, 2009	Sheet 34 of 60	

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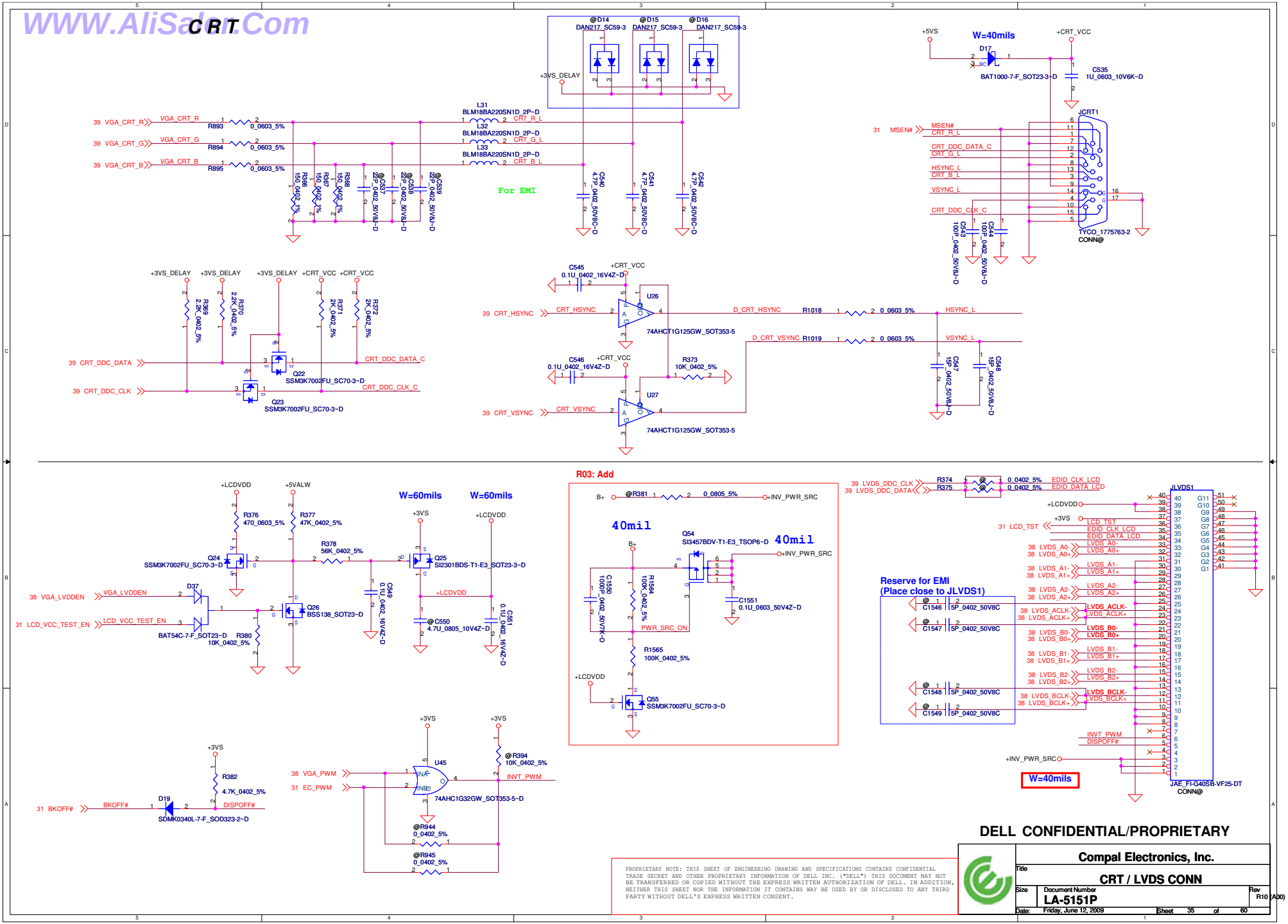
CRT



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Compal Electronics, Inc.	
Title: CRT / LVDS CONN	
Size	Document Number: LA-5151P
Rev	R10 (A00)
Date: Friday, June 12, 2009	Sheet 35 of 60

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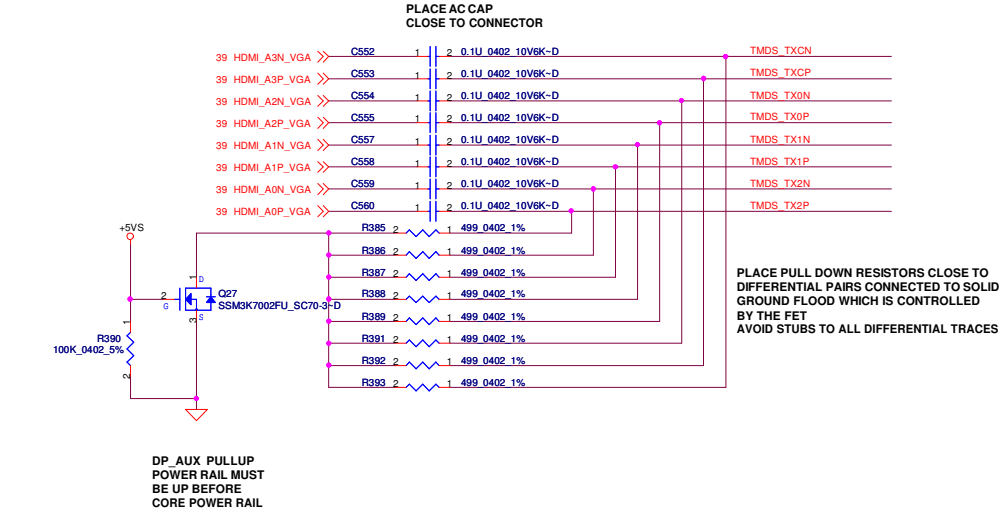
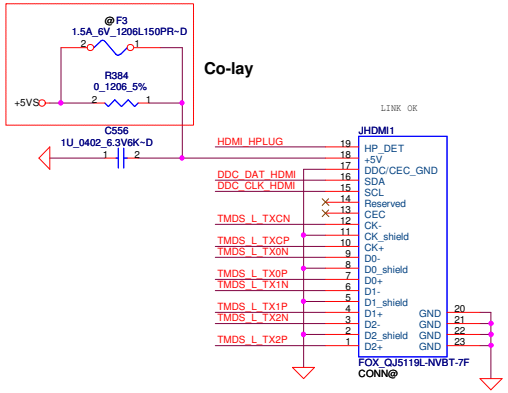
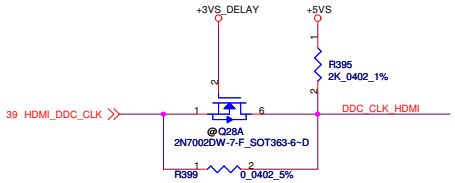
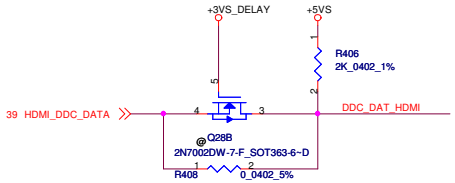
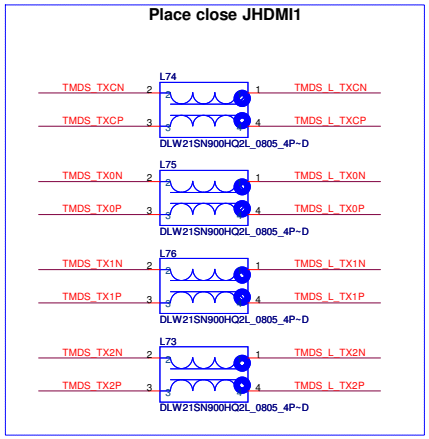


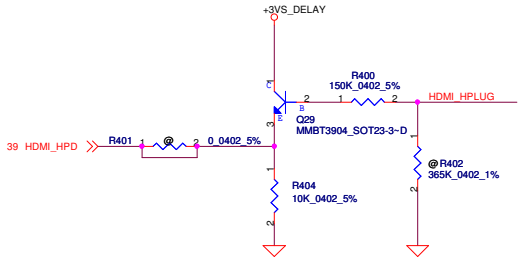


DP_AUX PULLUP
POWER RAIL MUST
BE UP BEFORE
CORE POWER RAIL









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Compal Electronics, Inc.			
Title: HDMI CONN			
Size	Document Number: LA-5151P		Rev: R10 (A00)
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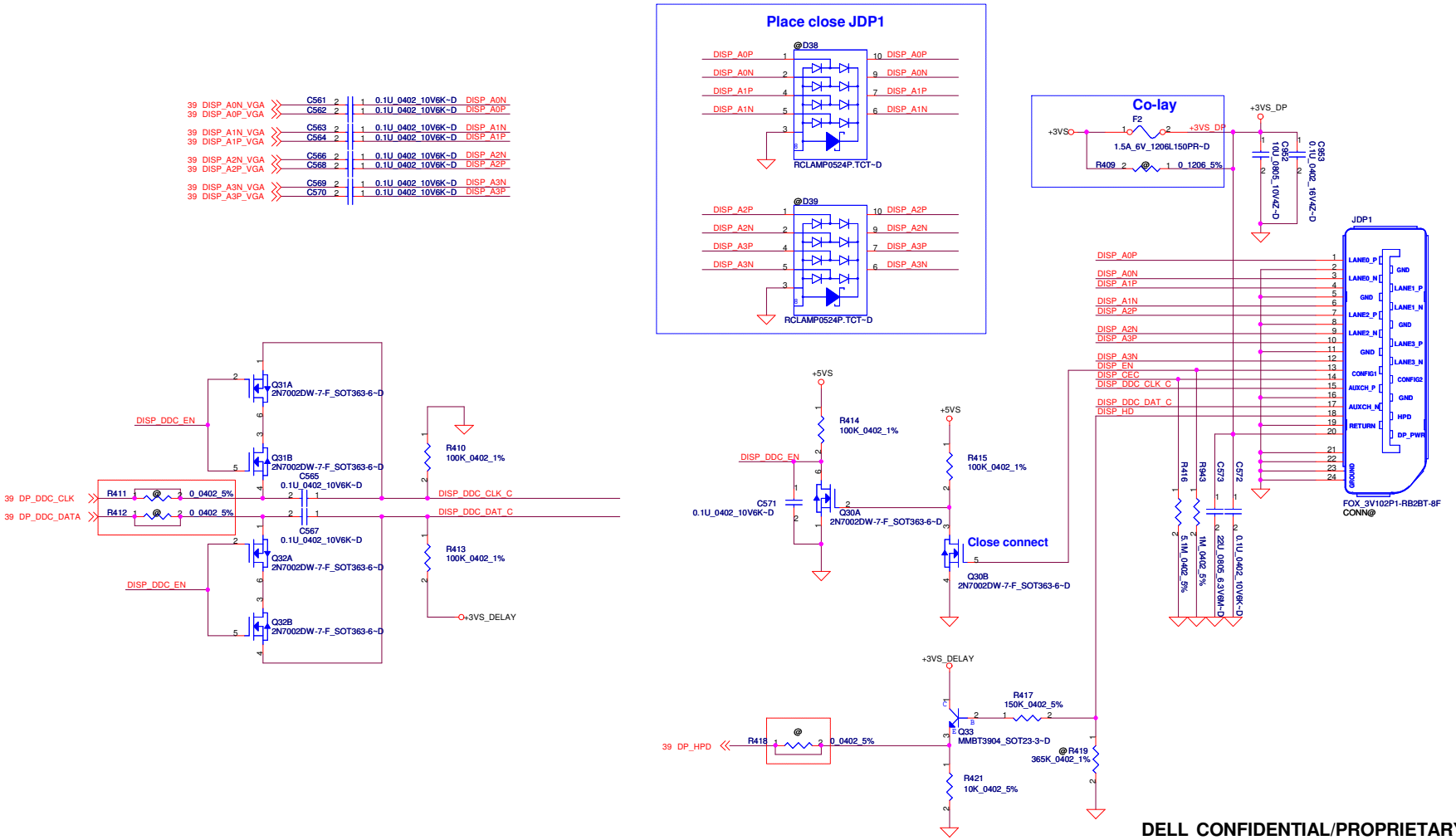

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Compal Electronics, Inc.

Title: Display Port

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Date: Friday, June 12, 2009 | Sheet 37 of 60

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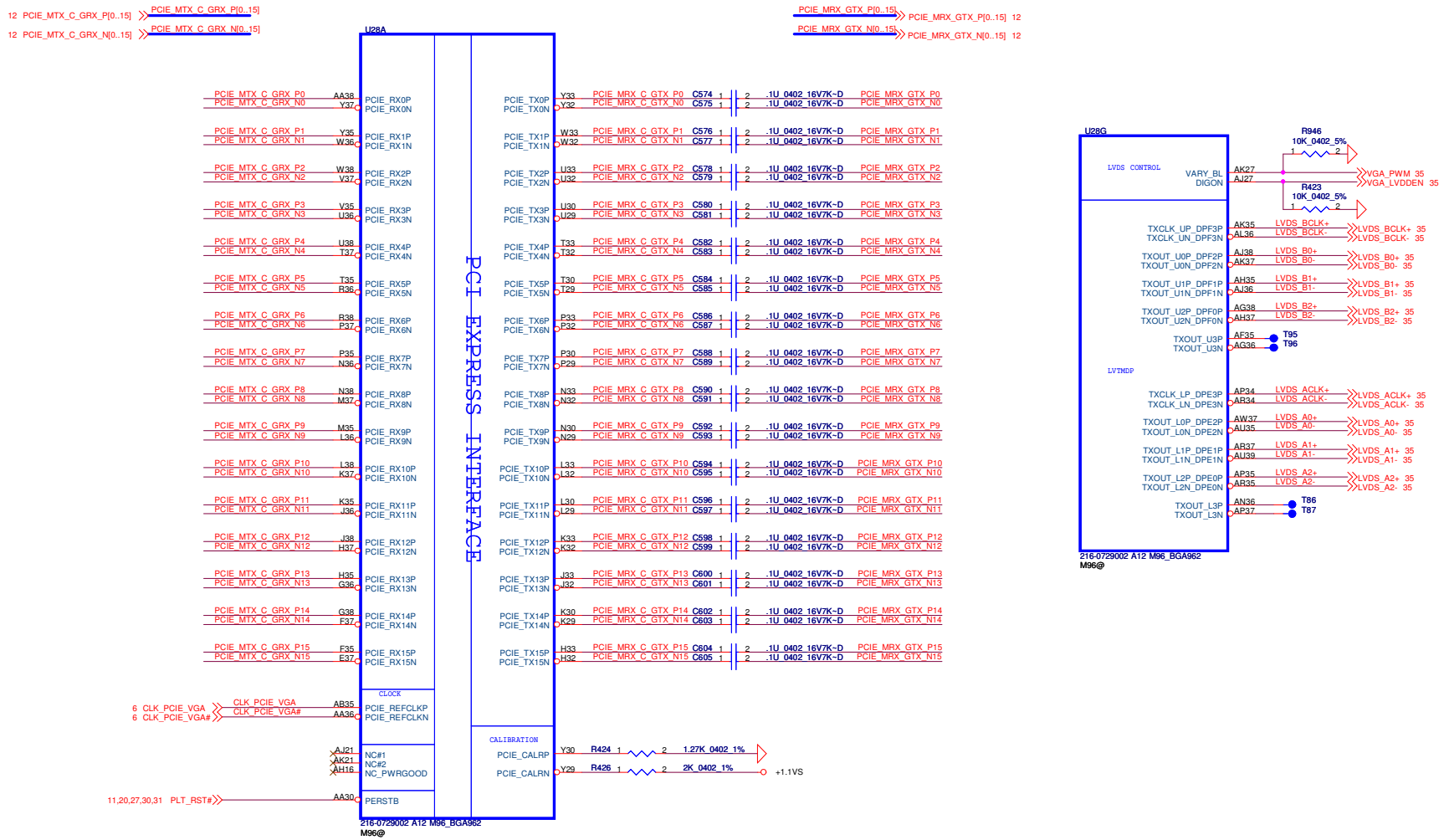

M96 P/N : SA00002UQ40 (S IC 216-0729042-00 A13 M96 FCBGA962 0FD)
M92 P/N : SA00002YX20 (S IC 216-0728014 A12 M92-M2 XT FCBGA 0FD)

M92/XT GPU
M92@

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Compal Electronics, Inc.			
Title: M96 PCIE/ LVDS			
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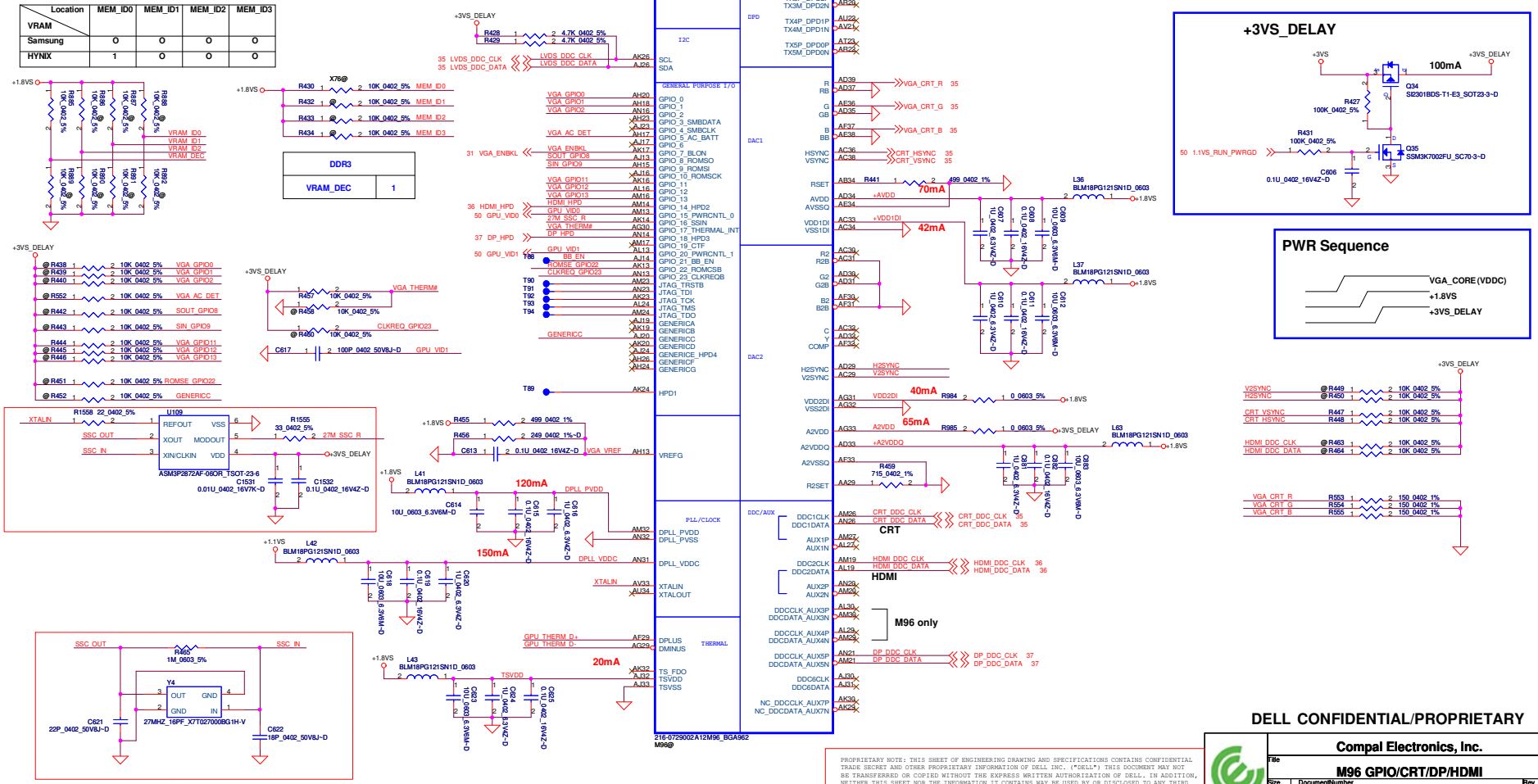
Strap Name	Pin Straps description		Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location / VRAM	MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3
Samsung	O	O	O	O
HYNIX	1	O	O	O

DDR3	
VRAM_DEC	1



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Compal Electronics, Inc.

Title: M96 GPIO/CRT/DP/HDMI

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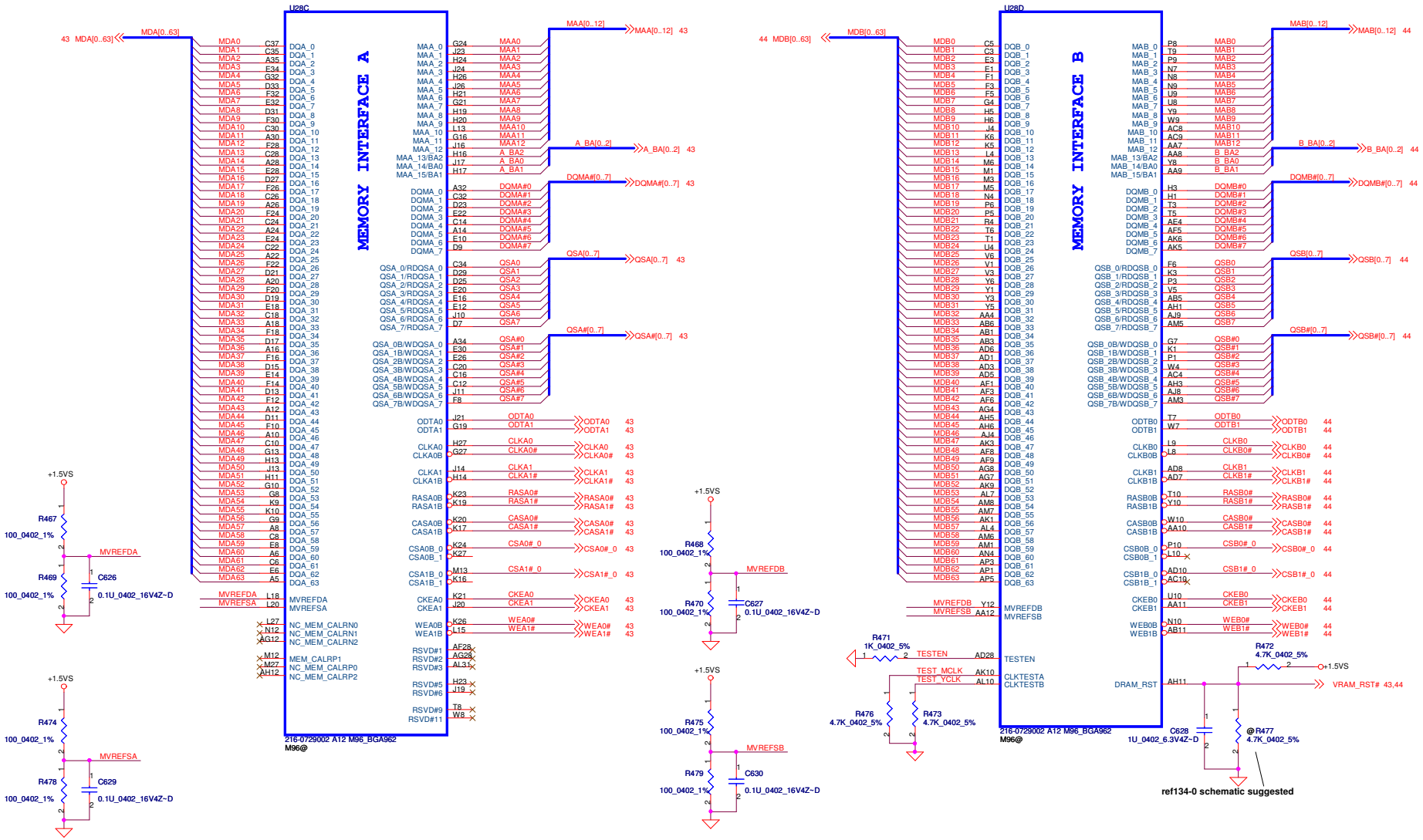
M92M Use Channel B memory interface only.



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Compal Electronics, Inc.	
Title: M96 MEMORY INTERFACE	
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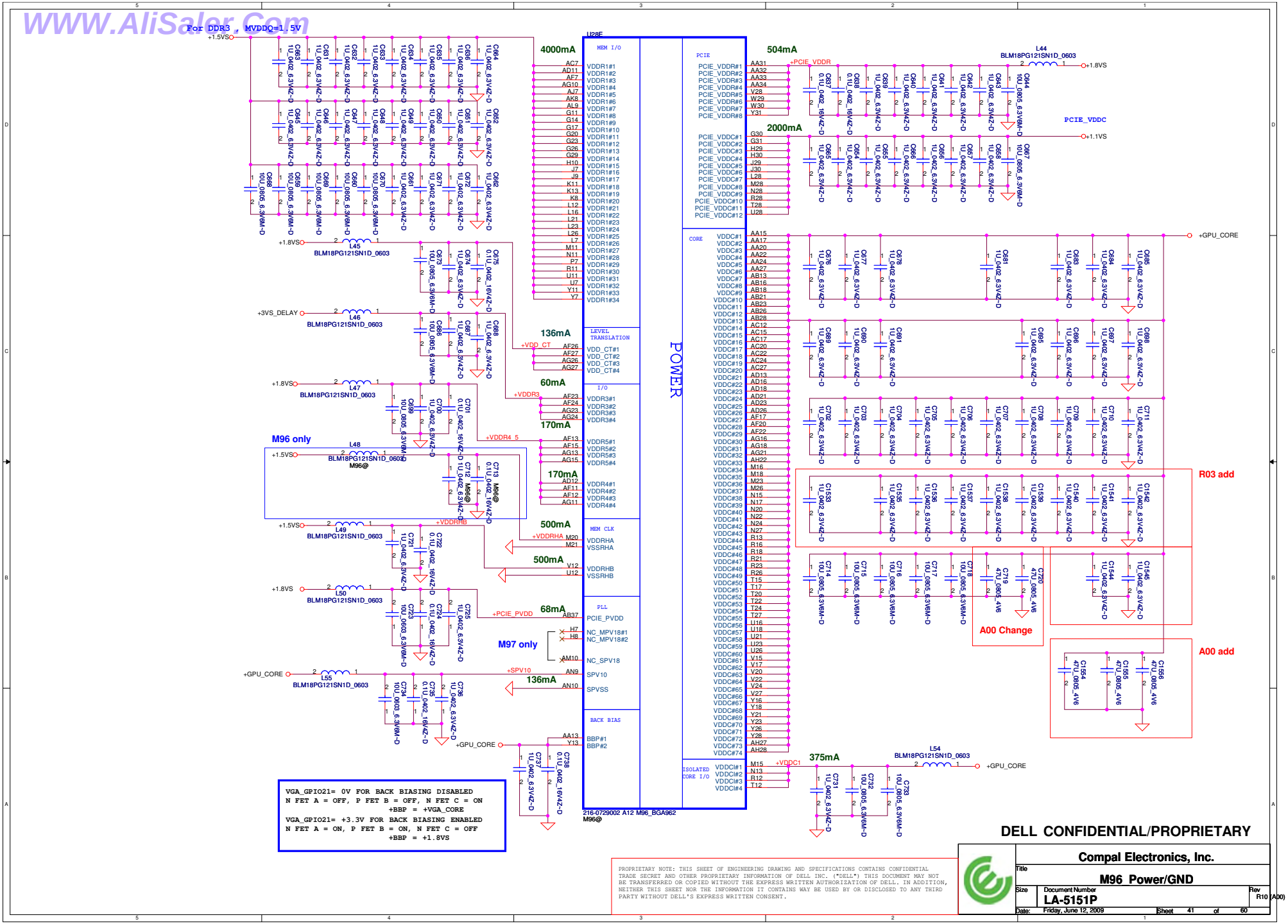

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Compal Electronics, Inc.

Title: M96_Power/GND

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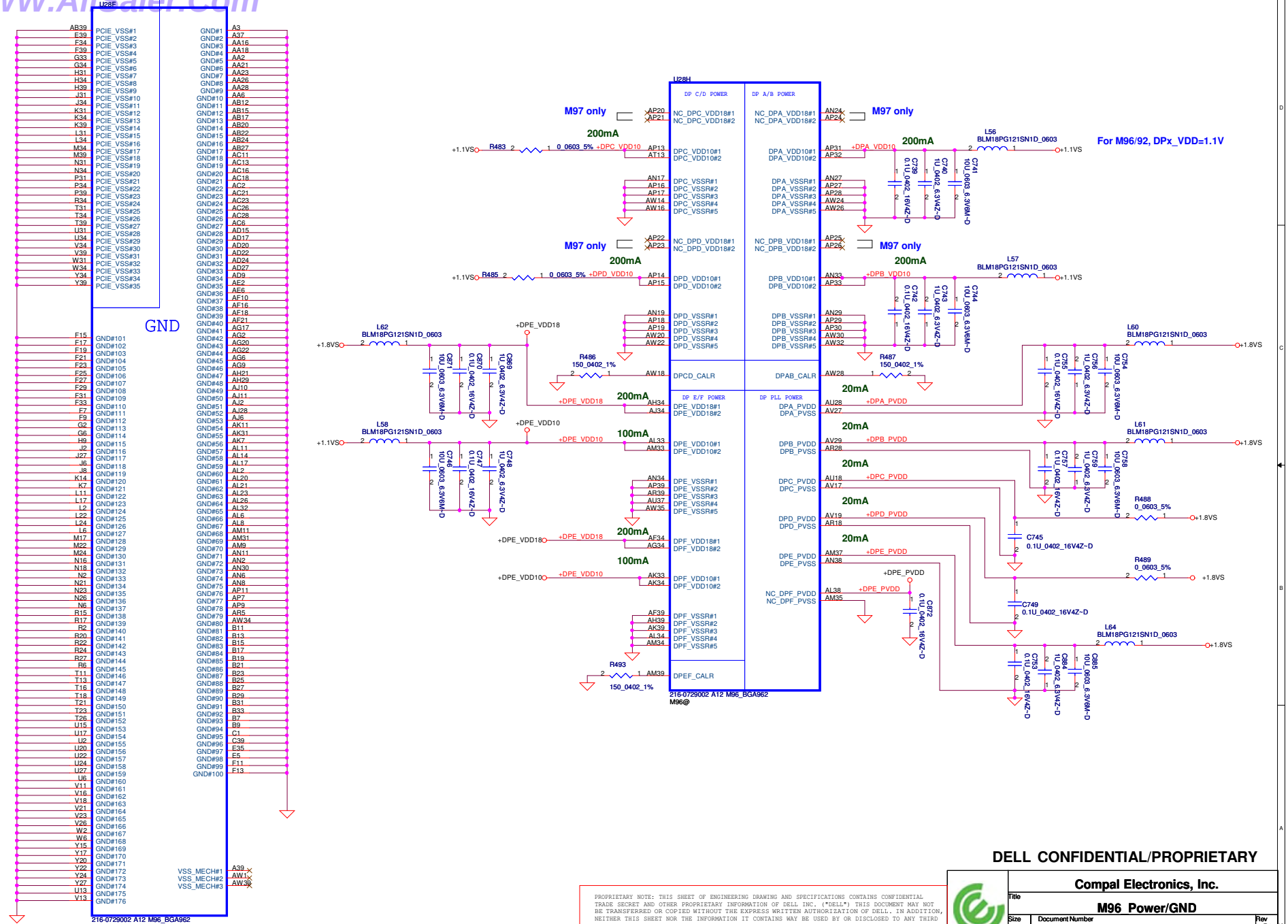

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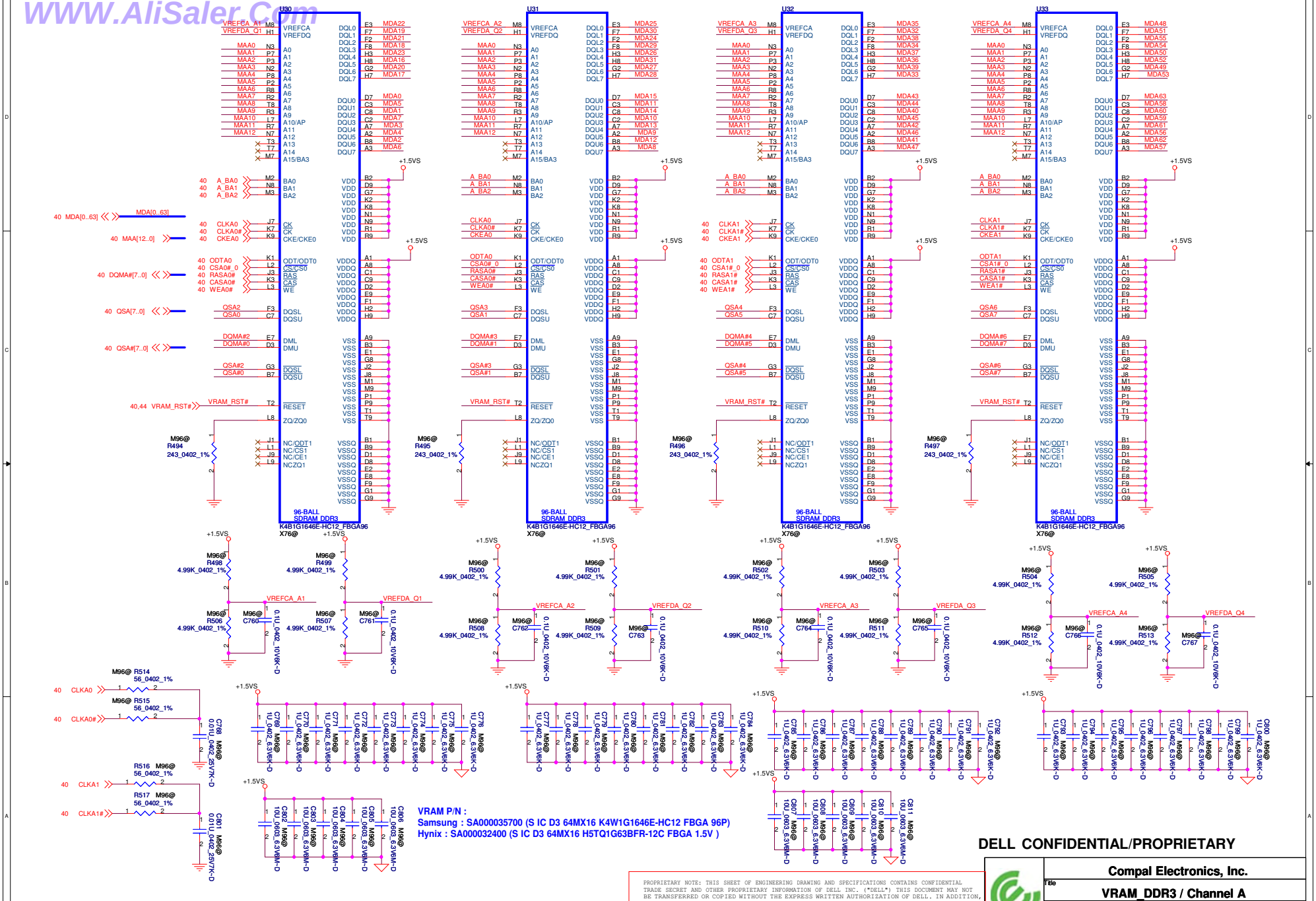

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

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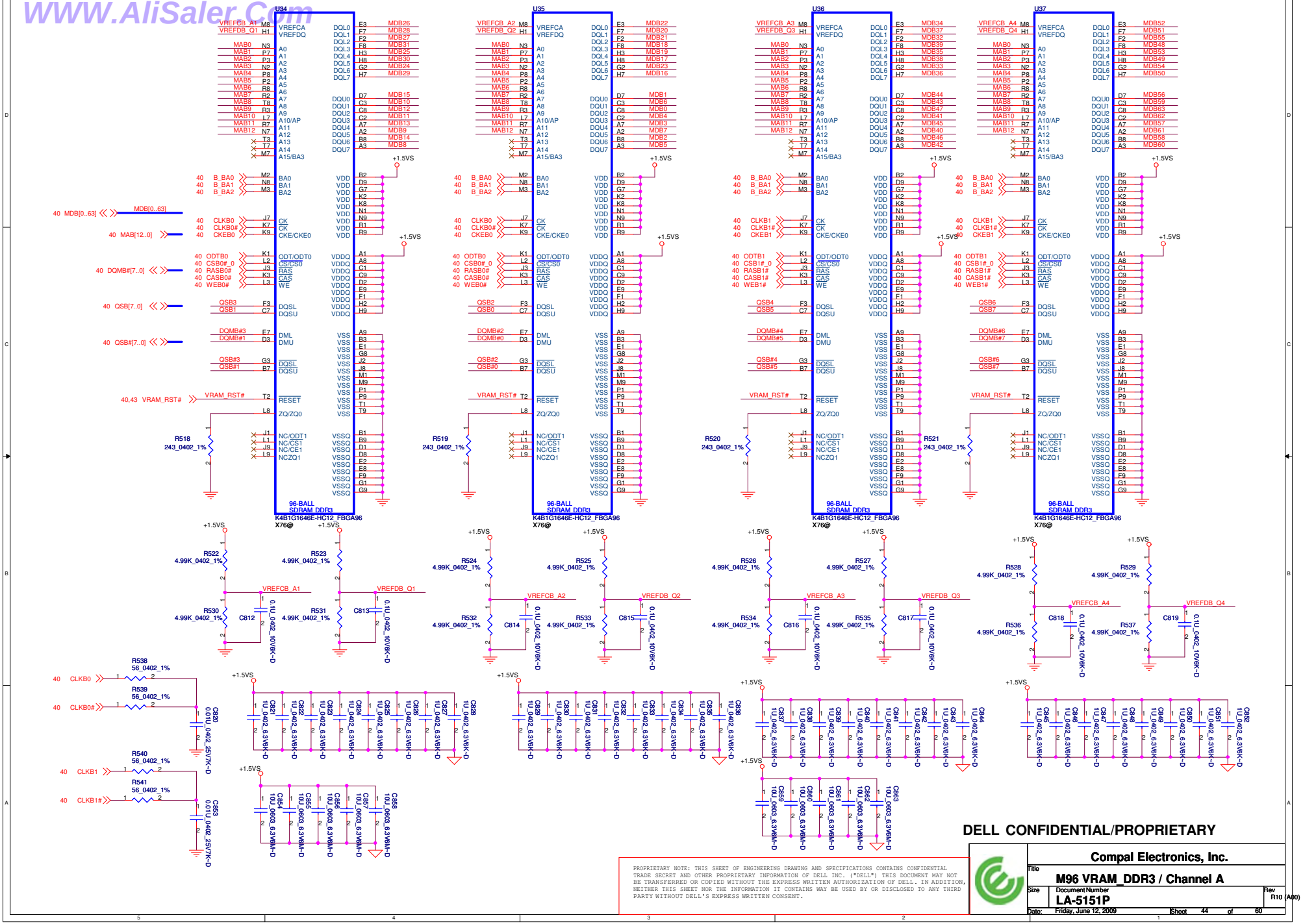

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Compal Electronics, Inc.

Title: **M96 VRAM_DDR3 / Channel A**

Size: | Document Number: **LA-5151P** | Rev: R10 (A00)

Date: Friday, June 12, 2009 | Sheet 44 of 60

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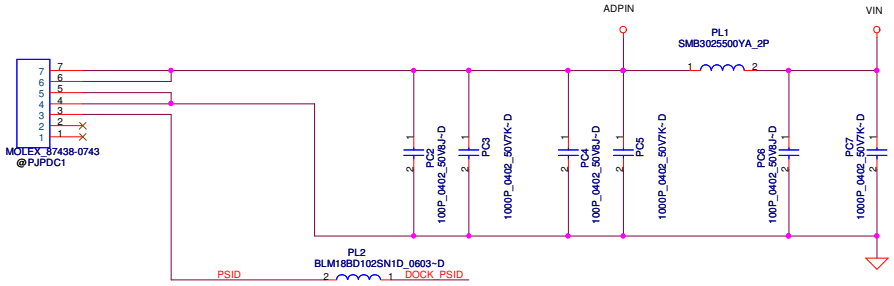

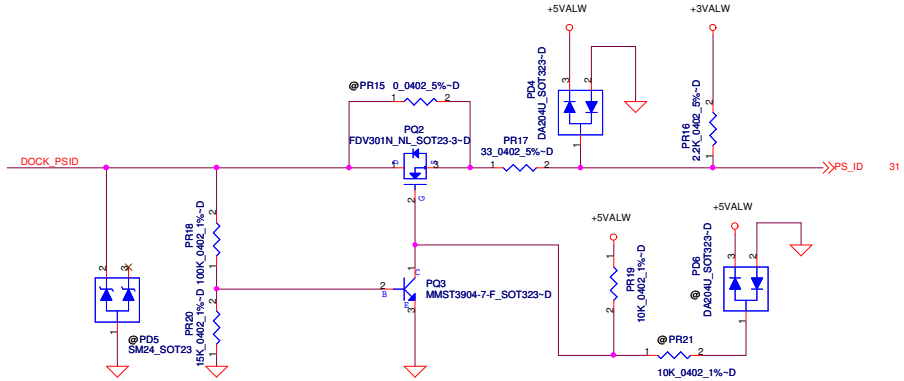

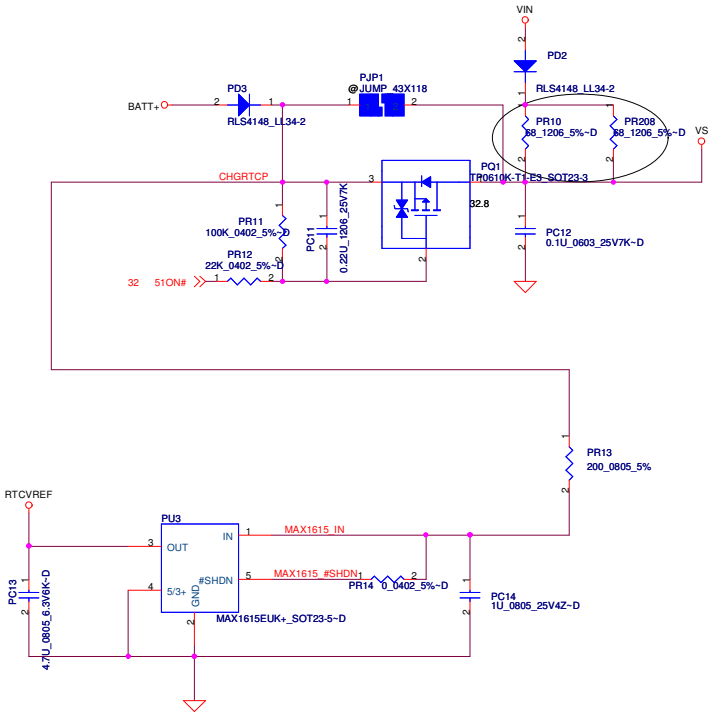

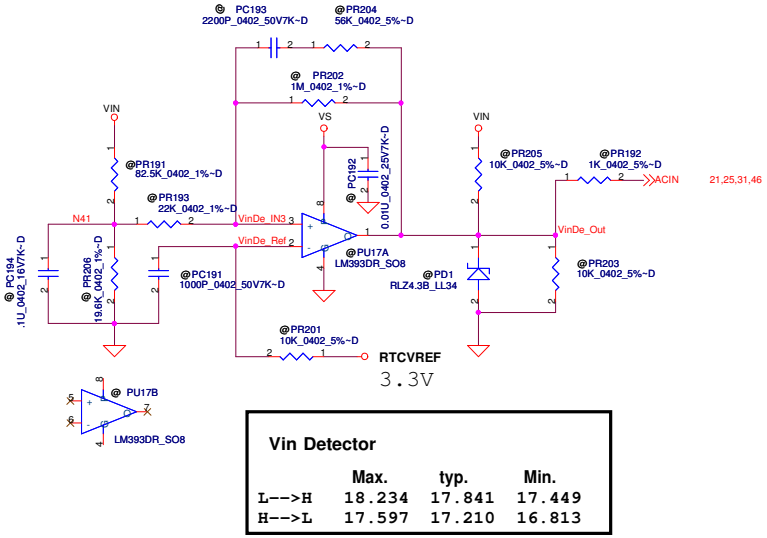

Vin Detector

	Max.	typ.	Min.
L-->H	18.234	17.841	17.449
H-->L	17.597	17.210	16.813

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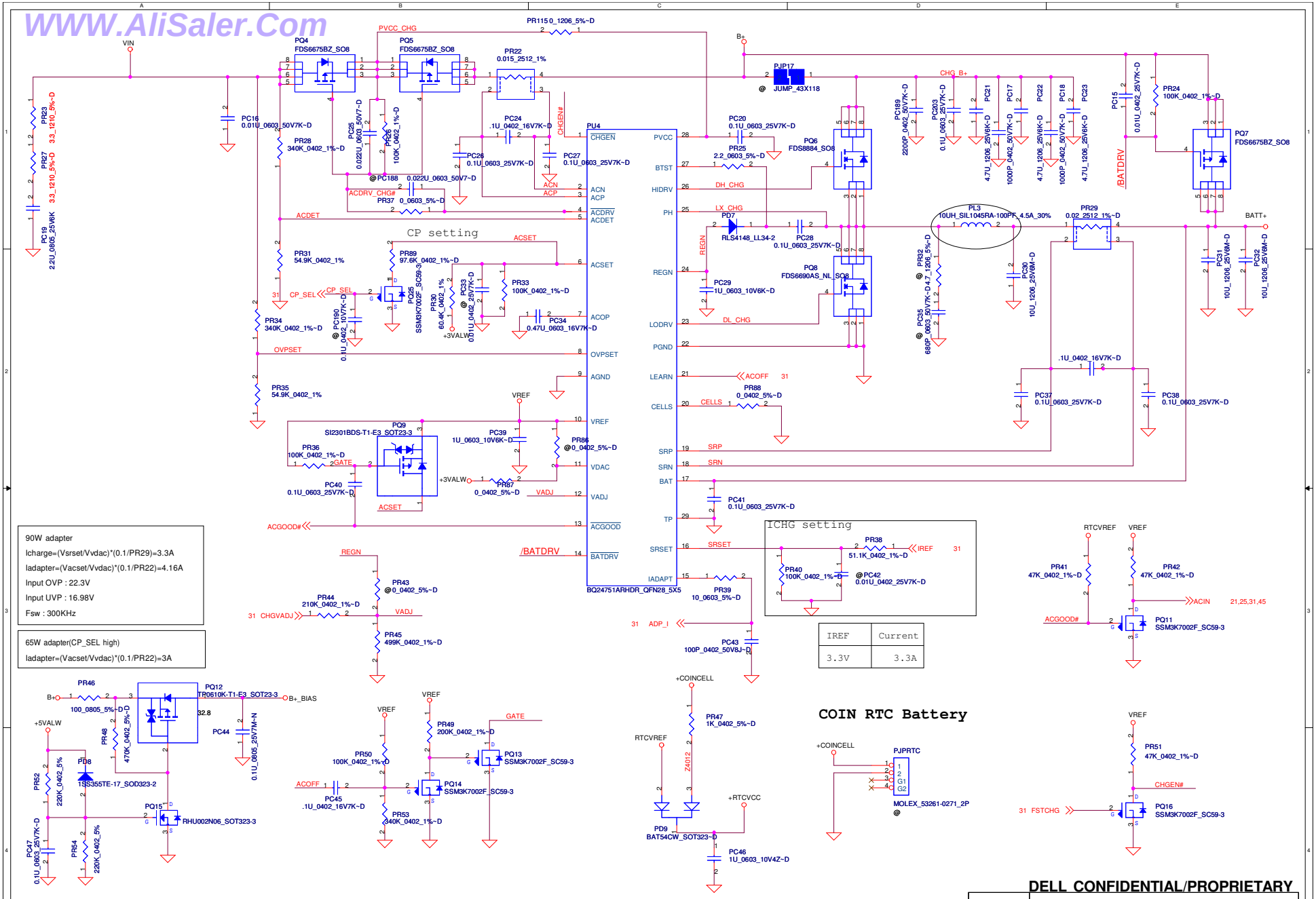

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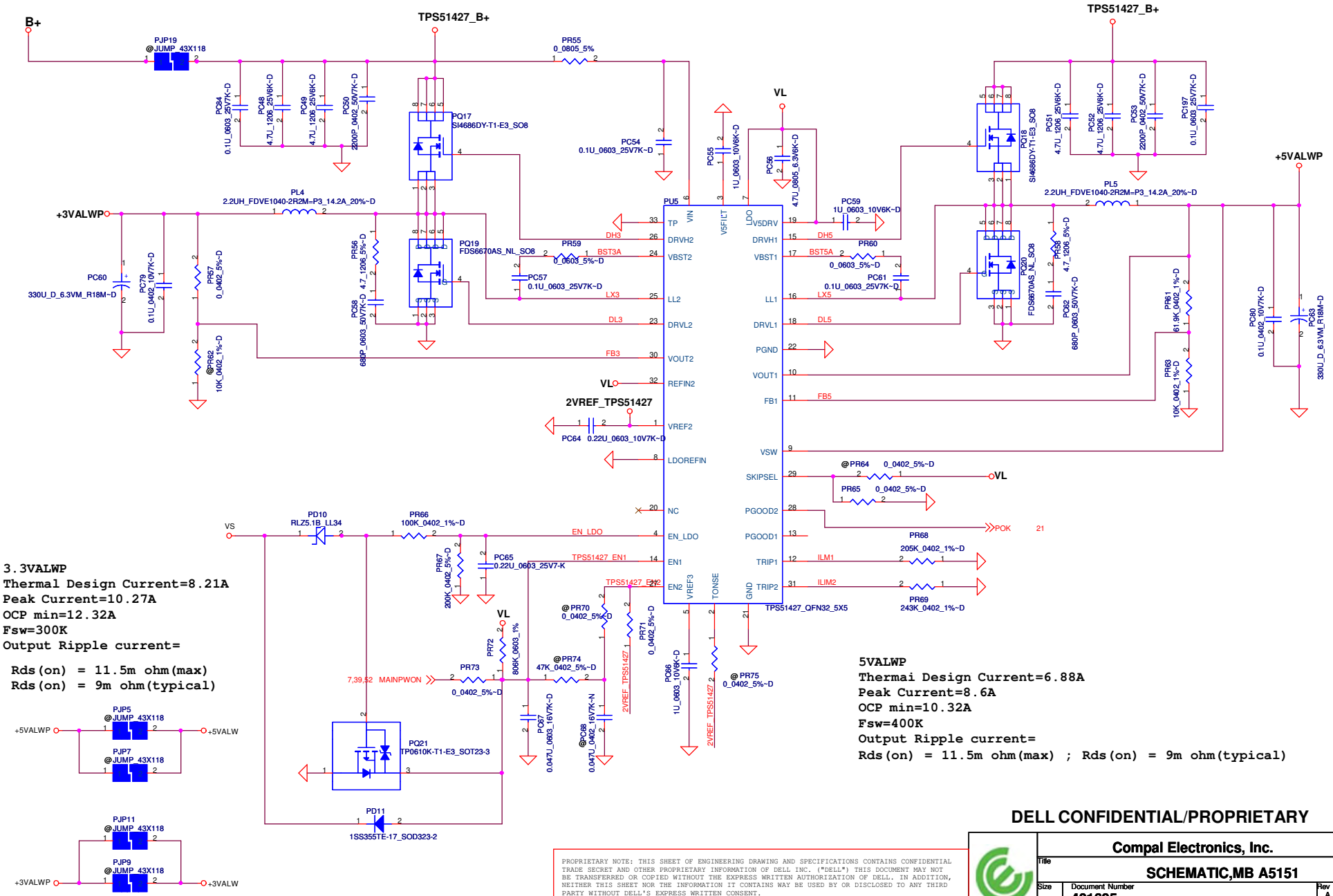

3.3VALWP
Thermal Design Current=8.21A
Peak Current=10.27A
OCP min=12.32A
Fsw=300K
Output Ripple current=

Rds(on) = 11.5m ohm(max)
Rds(on) = 9m ohm(typical)

5VALWP
Thermai Design Current=6.88A
Peak Current=8.6A
OCP min=10.32A
Fsw=400K
Output Ripple current=
Rds(on) = 11.5m ohm(max) ; Rds(on) = 9m ohm(typical)

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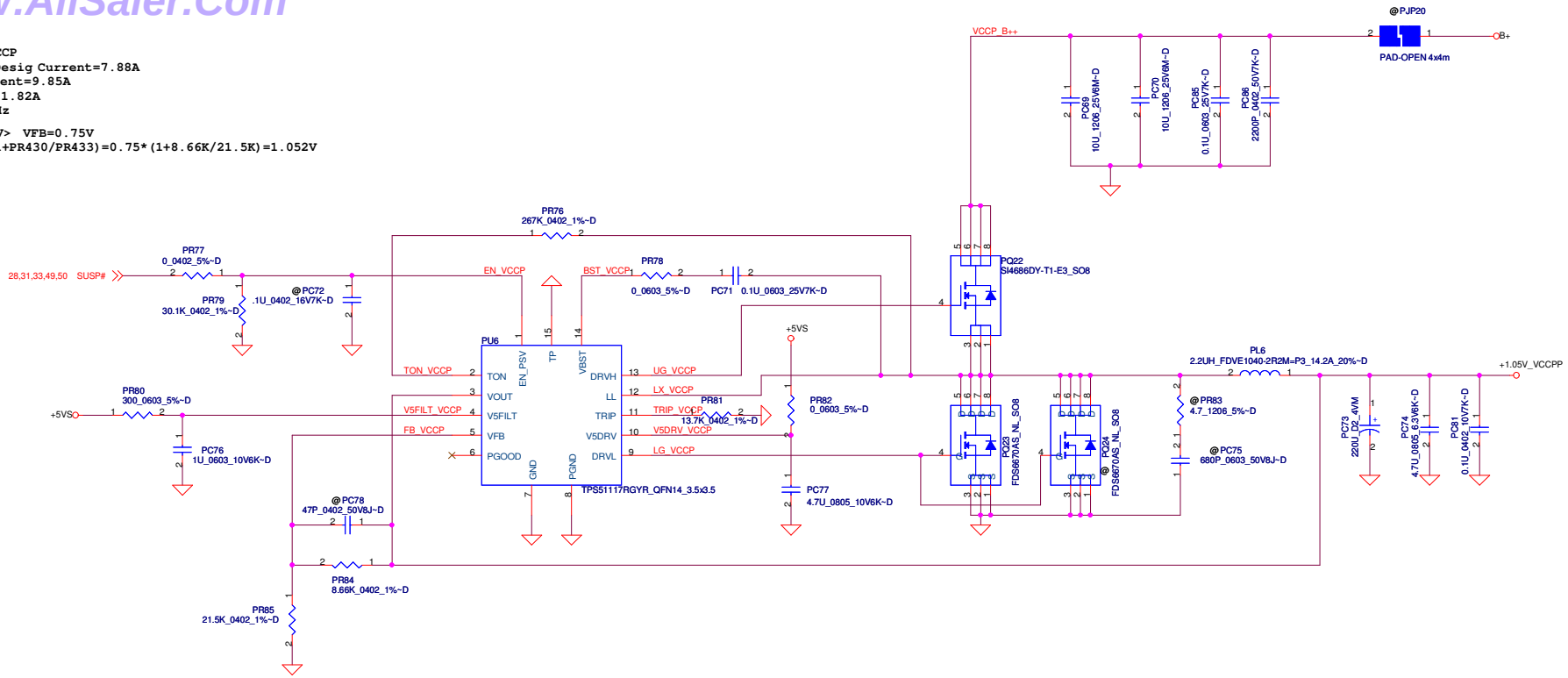
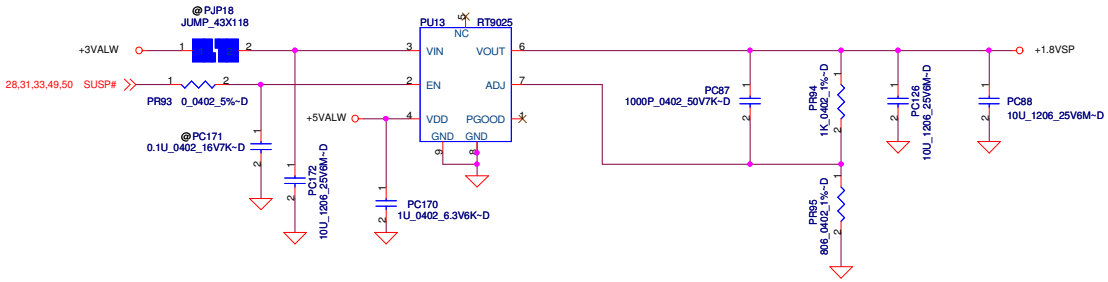
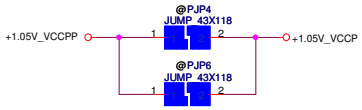
+1.05V_VCCP
Thermal Desig Current=7.88A
Peak Current=9.85A
OCP min=11.82A
Fsw=300KHz

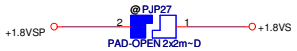
<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR430/PR433)=0.75*(1+8.66K/21.5K)=1.052V





+1.8VSP
Imax=0.67A
Vout=0.8*(PR94+PR95)/PR95=0.8*(1k+806)/806=1.79V





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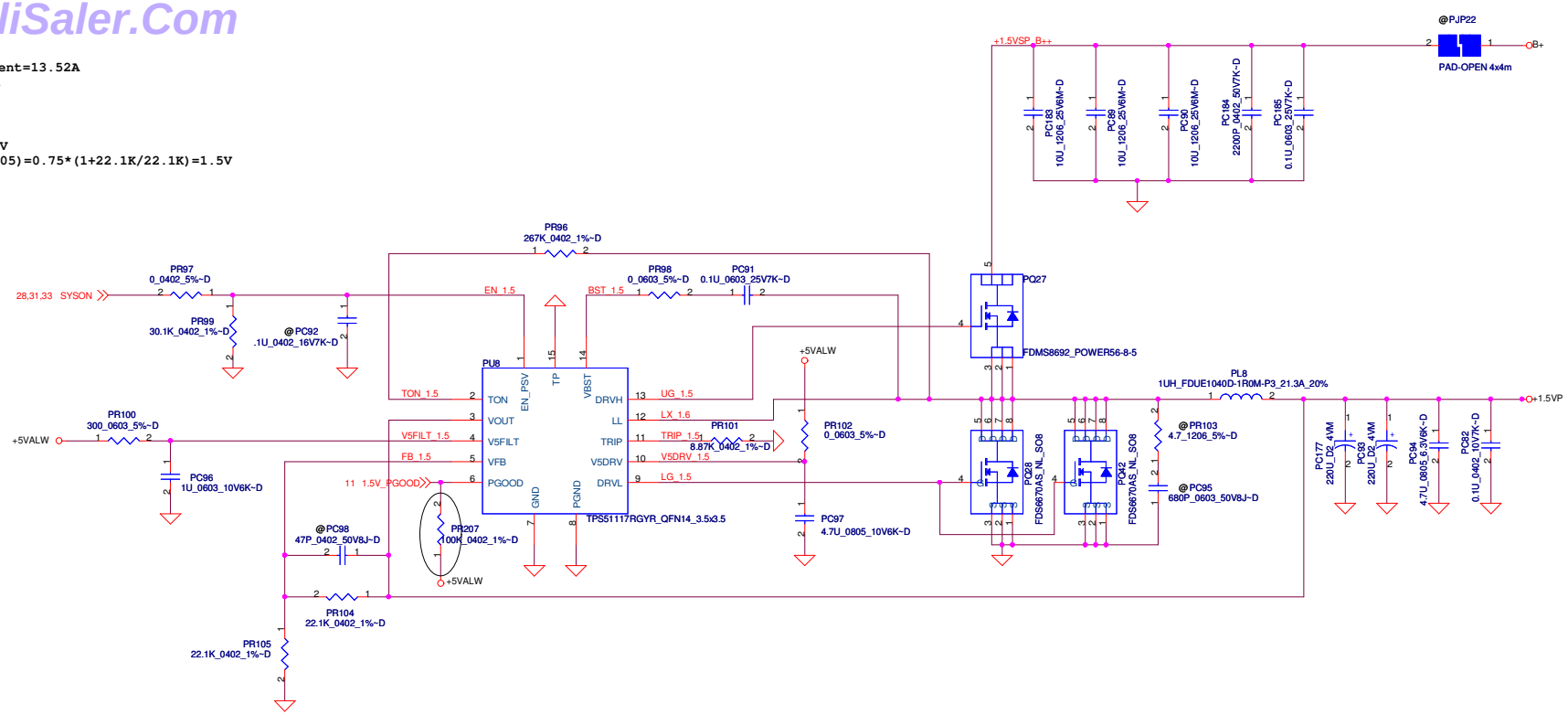
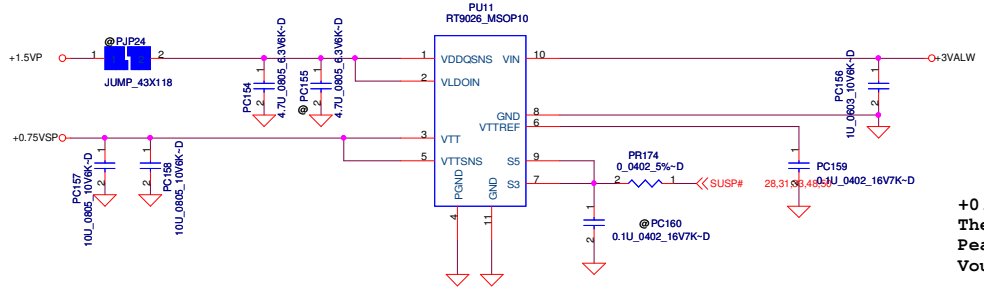
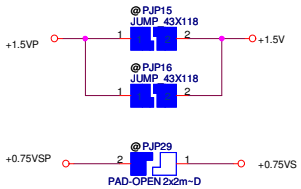
1.5V
Thermal Design Current=13.52A
Peak Current=16.91A
OCP min=20A
Fsw=298KHz

<Vo=1.5V> VFB=0.75V
Vo=VFB*(1+PR104/PR105)=0.75*(1+22.1K/22.1K)=1.5V





+0.75VSP
Thermal Design Current:0.7A
Peak current:1A
Vout=VDDQSNS/2=1.5V/2=0.75V



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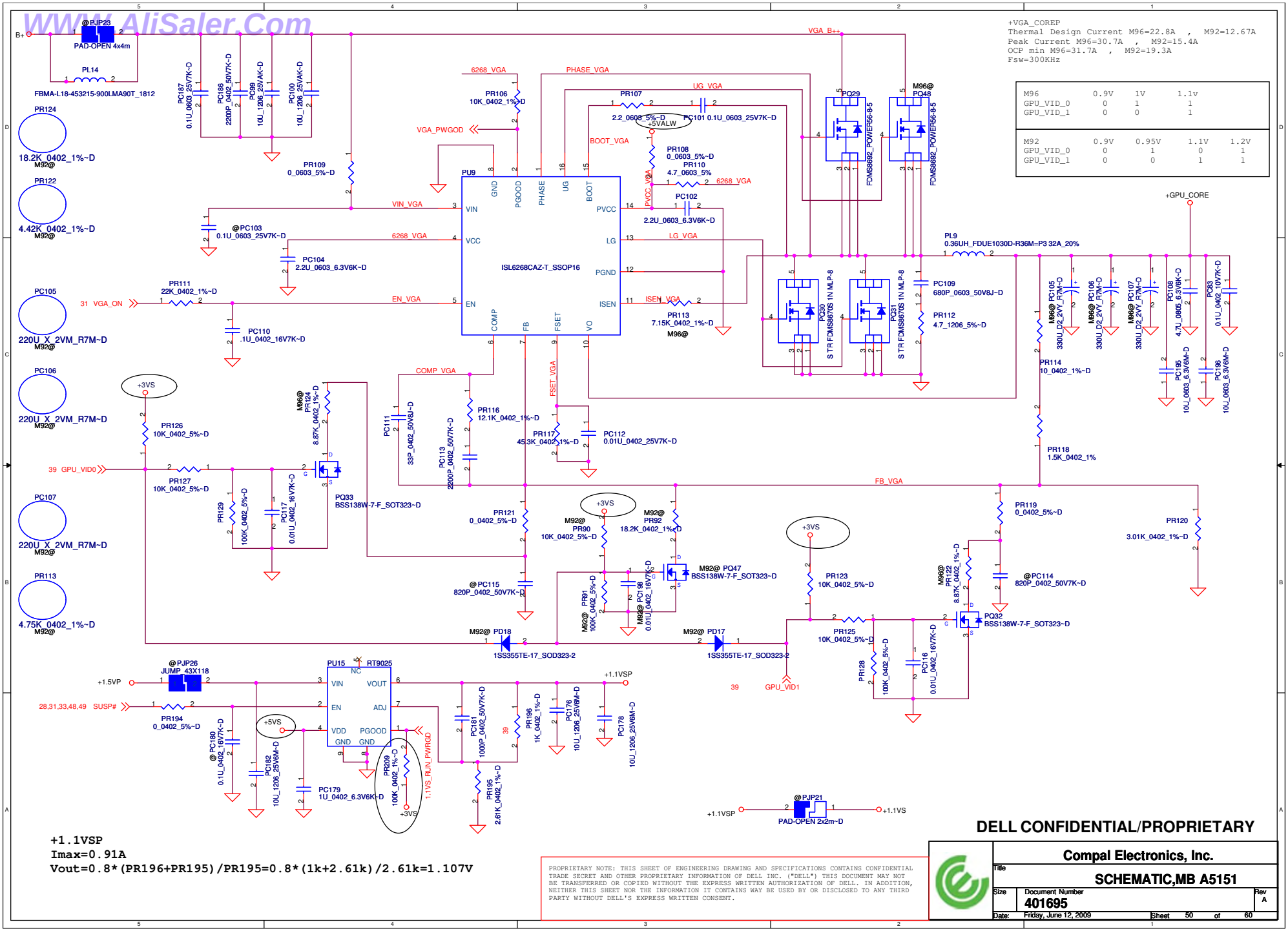

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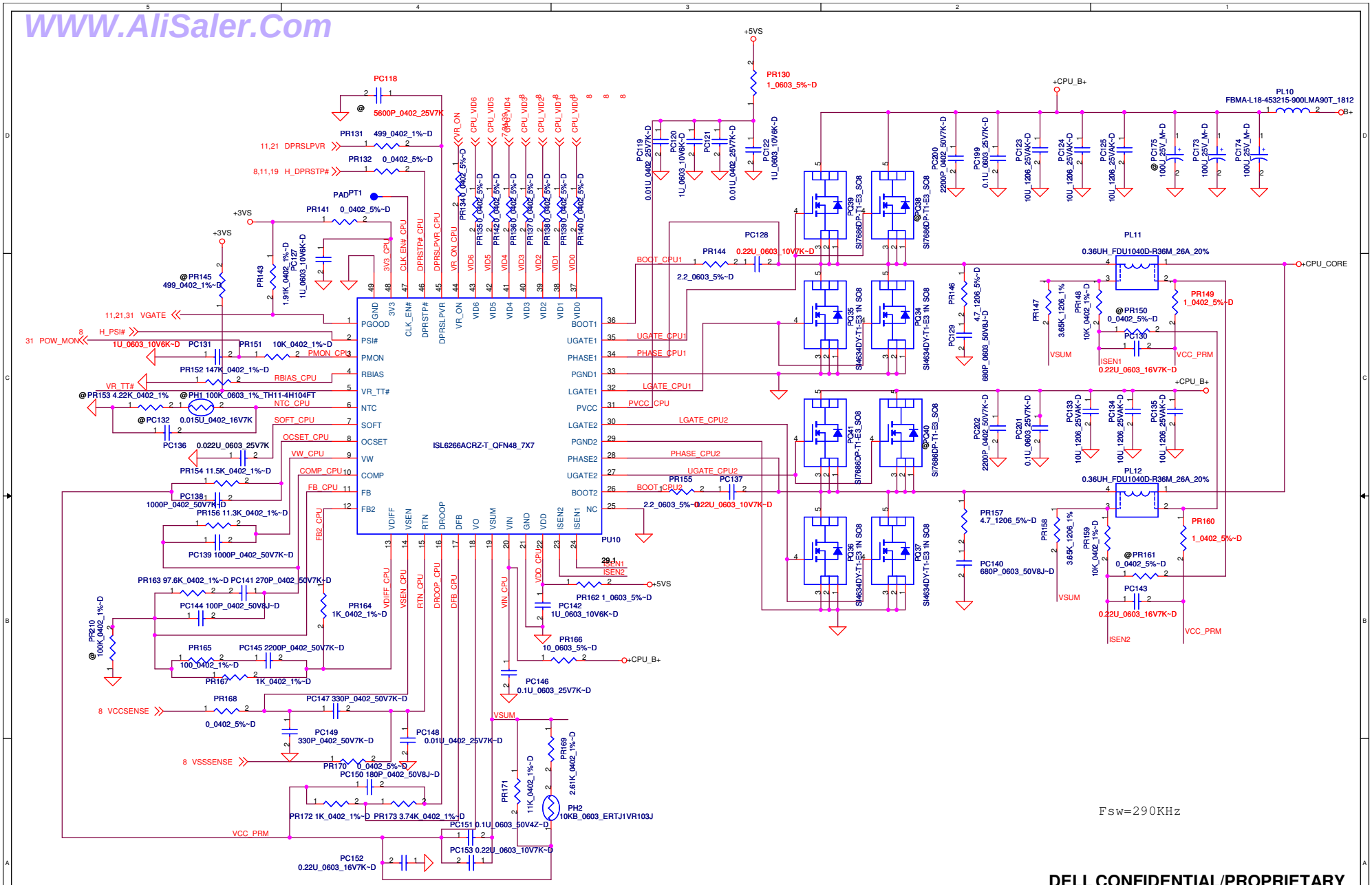

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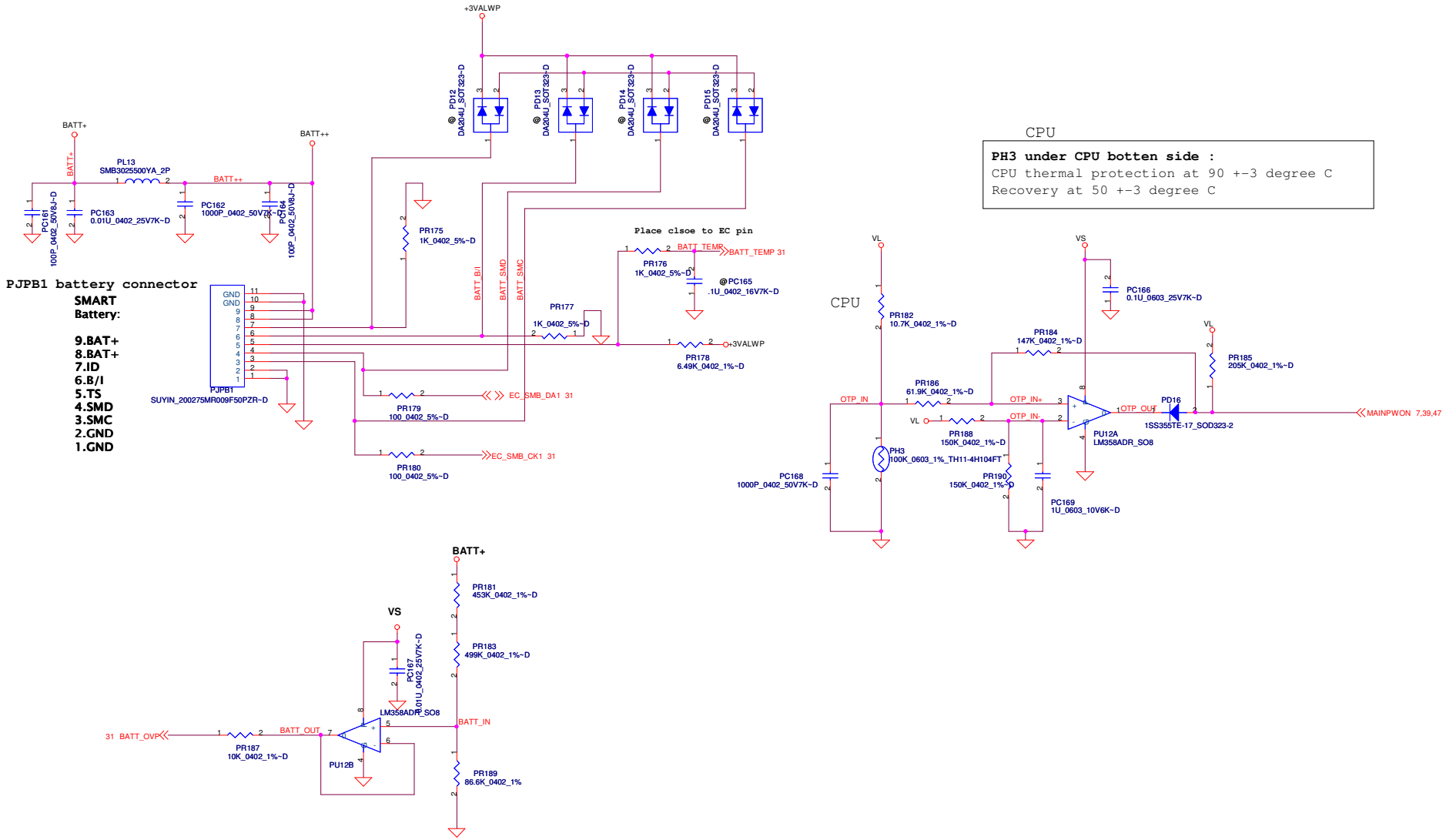
Battery Connect/OTP



LI-3S :13.5V----BATT_OVP=1.126V
BATT_OVP=0.08338*BATT+

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Title: SCHEMATIC,MB A5151

Size | Document Number: 401695 | Rev: A

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
01	47	+3VALWP/+5VALWP	01/22	Compal Mike	Setiing +5VALW OCP to 10.32A	Change PR68 from P/N:SD03429438L (294K +-1% 0402) to SD03424938L (249K +-1% 0402)	X01
02	47	+3VALWP/+5VALWP	01/22	Compal Mike	Setiing +3VALW OCP to 12.32A	Change PR69 from P/N: SD03424938L (249K +-1% 0402) to SD03429438L (294K +-1% 0402)	X01
03	48	+1.05V_VCCP/ +1.8VSP	01/22	Compal Mike	Setiing +1.05V_VCCP OCP to 11.82A	Change PR81 from P/N: SD03480618L (8.06K +-1% 0402) to SD03416228L (16.2K +-1% 0402)	X01
04	45	DCIN/Precharger	01/22	Compal Mike	Common circuit design modify	Change PR10 from P/N: SD00103308L (33 +-5% 1206) to SD011680A8L (68 +-5% 1206) Add PR208 SD011680A8L (68 +-5% 1206) parallel with PR10	X01
05	49	+1.5VSP/0.75VSP	01/22	Compal Mike	HW need to use +1.5VSP PGOOD signal,so need to add a pull high resister.	Add PR207 SD03410038L (100K +-1% 0402) between PU8 pin6 and PR97 pin 2.	X01
06	50	GPU_COREP/1.1VSP	01/22	Compal Mike	HW need to use +1.1VSP PGOOD signal,so need to add a pull high resister.	Add PR209 SD03410038L (100K +-1% 0402) between PU15 pin1 and +3VS.	X01
07	50	GPU_COREP/1.1VSP	02/09	Compal Mike	Change OCP setting from 20A to 25.6A	Change PR113 from P/N:SD03449910L(4.49K +-1% 0402) to SD03463418L(6.34K +-1% 0402)	X01
08	46	Charger	02/09	Compal Mike	Take off Cells selector function.	Populate PR88,take off PR37 and PQ10,change PR175 from 47K to SD02810018L(1K +-5% 0402)	X01
09	51	CPU_CORE	02/24	Compal Mike	Change CPU_CORE low-side MOSFET	Change PQ34,PQ35,PQ36,PQ37 from (SI4430BDY-T1-E3 1N SO-8) to SB00000DA00(SI4634DY-T1-E3 1N SO8)	X01
10	51	CPU_CORE	02/24	Compal Mike	HW don't need to use VR_TT# signal,so depopulate pull high resister.	Depopulate PR145 SD03449908L(499 +-1% 0402)	X01
11	51	CPU_CORE GPU_COREP	02/24	Compal Mike	Change input cap from X7R(85℃) to X6S(105℃)	Change PC99,PC100,PC123,PC124,PC125,PC133,PC134,PC135 from (10U 25V M X5R1206 H1.6) to SE153106K8L(10U 25V K X6S 1206 H1.6)	X01
12	47	+3VALWP/+5VALWP	02/24	Compal Mike	Take off Manufacturer:COMPOSTAR from PC64	Change PC64 from P/N: SE080224K8L (.22U 10V K X7R 0603) to SE080224M8L (.22U 10V K X7R 0603)	X01
13	52	BATTERY CONN	02/24	Compal Mike	Take off non-PSL Manufacturer:Panjit	Change PQ43,PQ44,PQ45,PQ46 from P/N: SB000006800 (2N7002W T/R7 1N SOT-323) to SB00000B30L (PMF3800SN 1N SC70-3)	X01
14	46	Charger	02/24	Compal Mike	Take off non-Lead Free material.	Change PR29 from P/N: SD021200D0L (S RES 1W .02 +-1% 2512) to SD000001F0L (S RES 1W .02 +-1% 2512 50PPM/C)	X01
15	50	GPU_COREP/1.1VSP	02/24	Compal Mike	Change frequence setting from 330KHz to 294KHz.	Change PR117 from SD03440228L (40.2K +-1% 0402) to SD03445328L (45.3K +-1% 0402)	X01
16	48	+3VALWP/+5VALWP +1.05V_VCCP	02/24	Compal Mike	Change choke reated current from 11A to 14.2A	Change PL4,PL5,PL6 from SH00000BQ0L (2.2UH +-20% MPLC1040L2R2 11A) to SH00000CG0L (2.2UH 20% FDVE1040-2R2M=P3 14.2A)	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	45	DCIN/Precharger	03/04	Compal Antony	Prevent diode breakdown from battery inrush current	Change PD3 from SCS00002G00 to SC11N414880	X01
18	45	DCIN/Precharger	03/04	Compal Antony	Change part number to L-end	Change PD4 part number from SC1A204U000 to SC1A204U00L	X01
19	47	+3VALWP/+5VALWP	03/04	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR68 from 249K ohm to 205K ohm	X01
20	47	+3VALWP/+5VALWP	03/04	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR69 from 294K ohm to 243K ohm	X01
21	48	+1.05V_VCCP/ +1.8VSP	03/04	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR81 from 16.2K ohm to 13.7K ohm	X01
22	49	+1.5VSP/0.75VSP	03/04	Compal Antony	Change Rtrip resistance to meet OCP setting	Change PR101 from 13.7K ohm to 8.87K ohm	X01
23	50	GPU_COREP/1.1VSP	03/04	Compal Antony	Change Rsen resistance to meet OCP setting	M96:Change PR113 from 6.35K ohm to 7.15K ohm M92:Change PR113 from 4.99K ohm to 4.75K ohm	X01
24	50	GPU_COREP/1.1VSP	03/04	Compal Antony	For better Bandwidth	Change PR116 from 13K ohm to 12.1K ohm	X01
25	50	GPU_COREP/1.1VSP	03/04	Compal Antony	Change part number to common part	Change PC113 part number from SE075222K8L to SE074222K8L	X01
26	50	GPU_COREP/1.1VSP	03/04	Compal Antony	Change output Capacitor	Change PC105、PC106、PC107 Capacitor from 220uF to 330uF	X01
27	50	GPU_COREP/1.1VSP	03/04	Compal Antony	Change VID resistance to meet setting	M92:Change PR122 from 4.53K ohm to 4.42K ohm	X01
28	50	GPU_COREP/1.1VSP	03/04	Compal Antony	Change VID resistance to meet setting	M92:Change PR124 from 17.4K ohm to 18.2K ohm	X01
29	51	CPU_CORE	03/04	Compal Antony	To avoid noise	Add PC199、PC201 0.1uF Cap to +CPU_B+	X01
30	51	CPU_CORE	03/04	Compal Antony	To avoid noise	Add PC200、PC202 2200pF Cap to +CPU_B+	X01
31	51	CPU_CORE	03/04	Compal Antony	Reserve space for load line shift control	Reserve PR194 space	X01
32	51	CPU_CORE	03/16	Compal Antony	To improve transient response	Change PC151 from 0.068uF to 0.1uF	X01

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Version Change List (P. I. R. List) Page 3

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
33	51	CPU_CORE	03/16	Compal Antony	Let difference of CPU Load Line and Spec smaller than 2mV	Change PR173 from 3.57K ohm to 3.74K ohm	X01
34	52	BATTERY CONN	03/16	Compal Antony	Disable Hardware CPU、GPU OTP circuit	Reserve PQ43、PQ44、PQ45、PQ46、PR197、PR198、PR199、PR200 space	X01
35	50	GPU_COREP/1.1VSP	03/16	Compal Antony	EMI solution	Add PL14 parallel PJP23	X01
36	50	GPU_COREP/1.1VSP	03/16	Compal Antony	EMI solution	Change PR107 from 0 ohm to 2.2 ohm	X01
37	50	GPU_COREP/1.1VSP	03/16	Compal Antony	EMI solution	Connect PC109 series PR112 from Phase node to GND	X01
38	50	GPU_COREP/1.1VSP	03/16	Compal Antony	Solve switching spike problem	Change L/S MOS PQ30、PQ31 from SO8 to power-PAK	X01
39	46	Charger	03/20	Compal Antony	Change 65W CP setting from 3.3A to 3A	Change PR89 from 143K ohm to 97.6K ohm	X01
40	48	1.05V_VCCP/ 1.8VSP	03/20	Compal Antony	For phase margin improved	Add PC87 1000pF between PU13 pin6 and PU13 pin7	X01
41	48	1.05V_VCCP/ 1.8VSP	03/20	Compal Antony	For phase margin improved	Add PC126 10uF between PU13 pin6 and PU13 GND	X01
42	50	GPU_COREP/1.1VSP	03/20	Compal Antony	For phase margin improved	Add PC181 1000pF between PU15 pin6 and PU15 pin7	X01
43	50	GPU_COREP/1.1VSP	03/20	Compal Antony	For phase margin improved	Add PC176 10uF between PU15 pin6 and GND	X01
44	50	GPU_COREP/1.1VSP	04/29	Compal Antony	To promote current sustain rating	M96:Add PQ48 for GPU buck circuit	X02
45	46	Charger	05/06	Compal Antony	TI FAE request	Add PR37 0 ohm resistor between PU4 pin4 and PR26	X02
46	46	Charger	05/06	Compal Antony	slove PQ5 design margin issue	Change PQ4,PQ5,PQ7 from FDS4435 to FDS6675 (SB966750080)	X02
47	51	CPU_CORE	05/06	Compal Antony	Montavina platform design	Change PC136 from 15nF to 22nF	X02
48	46	Charger	05/06	Compal Antony	TI FAE request	Add PQ26,PD19,PD20,PC203,PR115,PR133, reserve PC25 space	X02

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
49	46	Charger	06/04	Compal Antony	TI FAE request	Delete PQ26,PD19,PD20,PC203,PR115,PR133	X03
50	46	Charger	06/04	Compal Antony	TI request to reserve protection circuit	Reserve PR90 0ohm , PR37 0ohm , PC100 space ,PC25 0.022uF ,PC change to 0603 size	X03
51	46	Charger	06/04	Compal Antony	Recover a correct component	Recover correct component PR89 to 97.6K ohm	X03
52	45	DCIN/Precharge	06/04	Compal Antony	DELL command	Change PQ2 from SB502060000 (RHU002N06_SOT323-3) to SB50301008L (FDV301N 1N SOT23-3)	X03

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Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	06	Clock gen	2009/02/03	Adam_Lai	Error connection of clock gne I2C.	Correct CLK_SMBDATA connect to U1.9 , CLK_SMBCLK connect to U1.10.	Rev02 (X01)
2	26	Memo	2009/02/03	Adam_Lai	No need to using new part.	Change PN: SE020105Z8L (S CER CAP 1U 50V Z Y5V 0805 H1.25) [NA code) to SE033105Z8L (S CER CAP 1U 25V Z F(Y5V) 0805 H0.85) [AP code] Location: C889, C890, C891, C922	Rev02 (X01)
3	25	Codec	2009/02/03	Adam_Lai	Follow codec reference schematic	Correct C866 connect from R545 pin 2 to R545 pin1 Correct C865 connect from R543 pin 2 to R543 pin 1.	Rev02 (X01)
4	30	BT connector	2009/02/03	Adam_Lai		Update JBT1 conn SP01000SL0L (AP code) symbol.	Rev02 (X01)
5	30	CRT RGB EA	2009/02/09	Adam_Lai	CRT RGB signals EA failed on Rising / Falling time.	Change L31~L33 from SM01000AL00 (S SUPPRE_ CHENG-HANN MBK1608301YZF 0603) to SM01000DT0L (S SUPPRE_ MURATA BLM18BA220SN1D 0603)	Rev02 (X01)
6	35	CRT Diode	2009/02/23	Adam_Lai	CRT diode forward current is about 1Amp, need to change part to prevent damage.	Change D17 from SC1B411D010 (S DIO RB411DT146 SOT23) to SCS00002Y0L (S SCH DIO BAT1000-7-F SOT23-3)	Rev02 (X01)
7	37	Display Port (DF276959)	2009/02/23	Adam_Lai	Screen can't output to external monitor with DP under DOS mode	Update Q30B Pin3 & Pin4 connection.	Rev02 (X01)
8	32	Power share	2009/02/24	Adam_Lai	Power share didn't work.	Add power share schematic.	Rev02 (X01)
9	5	Clock gen	2009/02/24	Adam_Lai	Error connection of CLK_PCIE_WPAN & CLK_PCIE_WPAN#	Correct WPAN CLK +/- signal of U1.	
10	4	Power Rail	2009/02/25	Bill_Huang	Correct error item.	Correct +3VS, +5VS Power consumption.	Rev02 (X01)
11	10~16	MCH	2009/02/26	Dell	Follow Iris's mail on Feb25. Both DIS & UMA use GM45 MCH.	1. Change MCH from P/N: SA00002JJ2L (S IC AC82PM45 SLB97 B3 FCBGA1329 PM A31!) to SA00002JT3L (S IC AC82GM45 SLB94 B3 FCBGA1329 GM) 2. Change Connect U1 pin 24, 25 (CLK_MCH_DREFCLK) & pin 28, 29 (MCH_SSCDREFCLK) to MCH pin A38,B38 & E41,F41 3. Change U1 pin 56,57 (CLK_PCIE_VGA) to U28 [Delete CLK_PCIE_WAN signals.] 4. Change U1 pin 16 (27_SEL) from 10K pull down to 10K pull high to +3VS_CK505. 5. Change U4 VCC_AXG power plane from connect to GND to +1.05V_VCCP. 6. Change U4 pin F47 (VCCA_DPLLA) & pin L48 (VCCA_DPLLB) from connect to GND to +1.05V_VCCP power plane.	Rev02 (X01)
12	35	DPST	2009/03/06	Compal	1. LCD panel need to be turned backlight under this crisis recovery mode. 2. when FN+ D is pressed during POST, the LCD will perform the LCD BIST test and boot to PSA directly	add a gate to OR VGA_PWM and EC_PWM signals	Rev02 (X01)
13	19~23	ICH	2009/02/26	Compal	Change ICH to consign P/N.	Change ICH from P/N: SA00002JH50 (S IC AF82801IBM SLB8Q A3 PBGA 676P ICH9M) to SA00002G12L (S IC AF82801IEM SLB8P A3 PBGA 676P)	Rev02 (X01)
14	32	Keyboard	2009/02/26	Compal	Follow latest Keyboard pin define, change connector pin define.	modify keyboard connector pin definetion to fit keyboard module.	Rev02 (X01)
15	20	FFS	2009/02/26	Compal	Add FFS function	Add FFS parts in page 20	Rev02 (X01)
16	30	JCARD1	2009/02/26	Compal	1. Change JCARD1 pin 1 location to prevent cable twist. 2. Connect contact current rating is only 0.3 Ampere max.	Add +5VALW pin count from 2 to 7 pins.	Rev02 (X01)
17		Market / Capacitor	2009/03/02	Compal	Due to Janpan produce Y5V no more in the fucture.	change C133,C138,C144,C152,C163,C251,C255,C281,C425 from SE000009W0L to SE107475M0L	Rev02 (X01)
18	23	ICH	2009/03/06	Compal	ICH coneect to ALW power rail have power wastage at S5 mode	Add MOSFET control circuit to reduce ICH power wastage at S5 mode.	Rev02 (X01)
19	24	LAN	2009/03/06	Compal	1. Prevent B+_BIAS damage Q3 2. Correct +LAN_DVDD12 power name 3. To pass LAN EMI test.	1. Add R1006 (1.5M_0402) 2. Correct C302 & C303 power source from +LAN_VDD12 to +LAN_DVDD12 3. Pop C873 ~ C880 , SE07168AC8L(S CER CAP 6.8P 50V C NPO 0402)	Rev02 (X01)

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
20	25	Audio codec	2009/03/06	Compal	1. SPK_MUTE# change to controlled by HP1_JD or HP2_JD.	1. Add U108 OR gate. 2. Change C336, C337, C349, C350 , C354, C355 from 1U_0603 to 2.2U_0805.	Rev02 (X01)
21	27	WWAN	2009/03/06	Compal	To supprot EC TX/RX debug card.	Change EC_TX_P80_DATA & EC_RX_P80_CLK connect to JWWAN1 pin 49 & 51	Rev02 (X01)
22	30	E-SATA	2009/03/06	Compal	To prevent antenna effect at E-SATA re-driver.	Delete R949, R950, R951, R952 0 ohm reserve resistors.	Rev02 (X01)
23	32	Powershare	2009/03/06	Compal		Add powershare schematic.	Rev02 (X01)
24	33	DC/DC	2009/03/06	Compal	1. To fit power budget	1a. Change U21 & U22 from DMN3030LSS-13 to SI4800BDY 1b. Change U25 SI4800BDY to Q45 SI4329DY	Rev02 (X01)
25		EMI		Compal	For EMI concern	1. Reserve 10P_0402 cap for CLK_PCI_EC / PCI_CLK / CLK_48M_ICH / CLK_14M_ICH / HDA_BITCLK_AUDIO / 2. Reserve 22P_0402 cap for SPI_CLK and place close U19. 3. Reserve U109 spread spectrum circuit for U28 graphic.	Rev02 (X01)
26		Thermal Sensor		Compal	To save EC GPIO pin count.	1. Remove U2 pin 6 (CPU_THERM_ALERT#) connect to EC. 2. Remove U38 pin6 (VGA_THERM_ALERT#) to EC.	Rev02 (X01)
27		Crystal		Compal	After fine tune crystal by vendor	1. Change C217, C864 from 12P_0402 to 15P_0402. (Y2) 2. Change C318 from 27P_0402 to 33P_0402. (Y3) 3. Change C479 & C481 from 15P_0402 to 22P_0402 (Y5)	Rev02 (X01)
28		WWAN		Compal	Due to clock gne lack of SRC output & support WWAN for USB interface only.	Remove CLK singals from clock gen & PCIE signals from ICH.	Rev02 (X01)
29		SATA HDD		Compal	SATA port 0 & Port 1 change.	Chagne SATA port 0 connect from JSATA1 to JSATA2. Chagne SATA port 1 connect from JSATA2 to JSATA1.	Rev02 (X01)
30		Screw hole		Compal	ME drawing change	1. Change H1 from H_2P3 to H_3P1 , H2 from H_2P4 to H_1P6. H5 from H_2P2 to H_3P0, H24 from H_3P2 to H_3P0. 2. Delete H13	Rev02 (X01)
1	32	Digitizer	2009/04/27	Compal	Digitizer firmware circuit updare. (Set high=enable, low=disable)	1.JTCH1.3 change net name form GND to VBUS 2. VBUS pull high to +3VS via R1559.	Rev03 (X02)
2	36	HDMI	2009/04/27	Compal	HDMI EMI issue.	L73~L76 parts change to DLW21SN900HQ2L	Rev03 (X02)
3	28	Express card	2009/04/27	Compal	Express card socket type error, change to normail type, not reverse type.	JEXP1 change to TAITW_PXPXAE-000LBS2ZZ4N0_NR part.	Rev03 (X02)
4	6	Clock gen	2009/04/27	Compal	VGA_CLKREQ# need to pull down	Change VGA_CLKREQ# from pull high to +3VS to GND.	Rev03 (X02)
5	31	MSEN#	2009/04/27	Compal	Support S5 Power on when CRT insert	MSEN# change from pull high to +3VS to pull high to +3VALW via R324	Rev03 (X02)
6	31	Sourcer	2009/04/27	Compal	Soucer suggest	Change C19, C21, C463, C936 fromm 10U_1206_16V4Z to 10U_0805_10V4Z.	Rev03 (X02)
7	33	DC / DC	2009/04/30	Compal	Voltage divider (7/8 VCC) on 3VS_gate	1. Change R338 to 300K ohm, Change Q50 to SI4392DY. 2. Add R340 2M_0402 connect to GND.	Rev03 (X02)
8	33	DC / DC	2009/04/30	Compal	Modify +5VALW to +5VS transfer circuit.	1. Change R338 to 300K ohm, Change Q50 to SI4392DY. 2. Add R340 2M_0402 connect to GND.	Rev03 (X02)
9	29	DFx	2009/04/30	Compal	DFx issue.	Update JESA1 footprint to FOX_3Q3813C-RB1C3B-7F_13P-T	Rev03 (X02)
10		Audio	2009/04/30	Compal	Audio EA result	Change C1507, C1508, C1529, C1530 from 270P_0603_50V8J to SE074271K8L (S CER CAP 270P 50V +-10% X7R 0402)	Rev03 (X02)
11	33	Power share	2009/04/30	Compal	USB Power share schematic for setting resistors to +3.0V and contact to GPI42, but voltage will drop to 0.5V, change GPIO pin from GPI42 to GPIO40 or system power ready (+3VALW is ready), Rb voltage will be pass for +3.0V.	exchange MSEN# & USB_DET_DELAY# GPIO pin	Rev03 (X02)
12	20	FFS	2009/05/04	Compal	original PIRQH is by USB controller used	FFS change int to PIRQ setting from PIRQH to PIRQE	Rev03 (X02)
13	41	VGA power	2009/05/04	Compal	VGA Power Transient EA test fail	Add C1533~C1545 for +CPU_CORE	Rev03 (X02)

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14	7 39	OTP	2009/05/04	Compal	It may unbootable due to OTP sequence error.	Modify CPU_THERM_STP & VGA_THERM_STP# circuit.	Rev03 (X02)
15	35	LVDS	2009/05/04	Compal	Noise band on 850M & 900MHz.	Reserve C1546~C1549 5P_0402 for LVDS clock	Rev03 (X02)
16	26	Speak ESD diode	2009/05/04	Compal	Reverse ESD diode for Speaker connector. (it need high voltage rating to prevent burning)	Reserve D20, D21, change from PACDN042Y34_SOT23 to PESD24VS2UT_SOT23	Rev03 (X02)
17	29	E-SATA conn	2009/05/04	Compal	ME change	Update JESA1 Footprint to FOX_313813C-RB1C3B-7F	Rev03 (X02)
18	32	EMI for Cap sensor	2009/05/04	Compal	cap sensor EMI test result	Change L76, L77 from BLM18AG121SN1D_0603 to BLM18AG601SN1D_0603	Rev03 (X02)
19	33	Discharge circuit	2009/05/04	Compal	double discharge for +3VS (+3V_WLAN)	Delete R357, Q18 +3V_WLAN discharge circuit.	Rev03 (X02)
20	35	LVDS timing	2009/05/04	Compal	to meet LVDS +LCDVDD T1 timing in spec.	1. Change R378 from 1K to 56K 2. Change C549 from 0.047U_0402 to 0.1U_0402.	Rev03 (X02)
21	39	EMC for VGA	2009/05/04	Compal	Follow EMC team's test result	Pop U109 SS circuit on	Rev03 (X02)
22	41	VGA Power Transient	2009/05/04	Compal	VGA Power Transient EA test fail	Follow CRB, more add 13pcs 1U_0402 cap on.	Rev03 (X02)
~~23~~	~~25~~	~~Audio Codec~~	~~2009/05/05~~	~~Compal~~	~~Change EAPD# pull up to +3VALW~~	~~Change R1549, U46.5. U47.5 connect to +3VALW~~	~~Rev03 (X02)~~
24	25	E-SATA	2009/05/05	Compal	Change E-SATA output swing control to 1.2X	1.Depop R958, R959, 2. Change R953 from 470 ohm to 390 ohm	Rev03 (X02)
25	35	LVDS	2009/05/05	Compal	To prevent flash light when AC or Battery in.	Add a MOSFET control circuit for LVDS converter power.	Rev03 (X02)
26	39	VGA thermal	2009/05/05	Compal	Gfx thermal sensor should be ADM1032ARMZ-1(108 degree C)	Change U38 from ADM1032ARMZ-2REEL to ADM1032ARMZ-1	Rev03 (X02)
27	23	ICH9M(5/5)_POWER&GND	2009/05/06	COMPAL	Modify +3VALW_S5_ICH circuit.	R972 form 470Kohm change to 300Kohm. R973 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
28	35	VGA / LVDS	2009/05/06	COMPAL	Modify Keyboard back light circuit.	R928 form 470Kohm change to 300Kohm. R931 form 1.5Mohm change to 2M ohm.	Rev03 (X02)
1	39	VGA spread spectrum	2009/06/03	COMPAL	Schemaitc design mistake	Chagne R1558 from SD028220280 (S RES 1/16W 22K +-5% 0402) to SD028220A80 (S RES 1/16W 22 +-5% 0402)	Rev1.0 (A00)
2	32	ESD diode	2009/06/03	COMPAL	Be use PSL ESD diode.	Chagne D48, D49 from SCA00000A00 (S ZEN ROW PJDLC05 3P C/A SOT23) to SCA00000J0L (S ZEN ROW PESD5V2S2UT 3P C/A SOT23 ESD)	Rev1.0 (A00)
3	26	Cap ship schedule	2009/06/03	COMPAL	SE00000NZ0L , current shipping schedule is still very bad, will be ETA in July	Chagne C901, C902, C903, C916, C918, C977 from SE00000NZ0L (S CER CAP 22U 25V K X7R 1210 H2.5) to SE00000GF8L (S CER CAP 22U 25V K X5R 1210 H2.5)	Rev1.0 (A00)
4	26	Gain setting	2009/06/03	COMPAL	gain setting, Is Sat: 13dB, (Sub:20dB)the final suggestion from JBL	1. Change R901,R902,R906,R907 from 280K_0402 to 182K_0402 2. Change R900 & R905 from 43.2K_0402 to 11K_0402 3. Change R904 & R909 from 16.9K_0402 to 17.8K_0402 4. Change R903 & R908 from 25.5K_0402 to 16.5K_0402 5. Change C908 & C912 from 0.22U_0402_106K to 0.1U_0402_10V6K.	Rev1.0 (A00)
5	29	E-SATA re-driver	2009/06/03	COMPAL	E-SATA connector not support detect pin.	Depop Q48 for E-SATA re-driver power saving.	Rev1.0 (A00)
6	25	TV turner	2009/06/03	COMPAL	in order to pass AVerMedia TV turner S2a testing	Change C343, C344, C356, C357 from 100P_0402_50V8J to 1000P_0402_50V7K	Rev1.0 (A00)
7	29	E-SATA re-driver	2009/06/03	COMPAL	1. They are P2P part with exactly same setting and function 2. PI2EQX3201BLZFE remove some redundant circuit in PI2EQX3201BLZFE that will not be used in NB application 3. The OOB signal margin of PI2EQX3201BLZFE is little bit higher than PI2EQX3201BZFE against different kinds of HD and design 4. 3201B and 3201BL) are qualified on Dell commercial model (Roush, Roush-refresh) in Compal, and now Roush-refresh project already made transition to 3201BL.	1. Chagne U40 from SA00002D80L (S IC PI2EQX3201BZFEX TQFN 36P) to SA00002YQ0L (S IC PI2EQX3201BLZFEX TQFN 36P) 2. Depop R969, R970	Rev1.0 (A00)

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8		0 ohm resisotrs	2009/06/08	Compal	Schematic confirm ready, save 0 ohm resistors and then short the signals directly.	"short parts of 1.(Page06)R2, R3, R4, R5, R6, R7 ,R8 ,R9 ,R10 ,R11 ,R12 ,R42 ,R43 ,R16 ,R17 ,R18, R19, R21, R23, R26, R28, R31, R33, R35, R37, R39, R40, R14, R15, 2. (Page11) R99, R94, 3. (Page17) R134, 4. (Page18) R137, 5. (Page21) R203, R220 6. (Page20) R1004 6. (Page24) R884,R235,R942, 7. (Page25) R247, R248 8. (Page27) R285, R911, R912, R913, R914, R1010, R1011, , R919, R920, R915, R916, R917, R922, R923, R924, R925, R291, R918, R921, 9. (Page28) R294, R298, R295, R296, R292, R293, 10. (Page30) R297, R299, 11. (Page32) R1559, 12. (Page35) R374, R375 13, (Page36) R401 14. (Page37) R411, R412, R418	Rev10 (A00)
9	25	Beep sound	2009/06/08	Compal	To support unboot beep sound, need add back EAPD# pull high resistor.	Pop R1549.	Rev10 (A00)
10	26	po sound noise	2009/06/08	Compal	to reduce po sound noise of speaker.	Add D51, R1567, and C1553 circuit.	Rev10 (A00)
11	39	VGA thermal sensor	2009/06/08	Compal	Both ADM1032ARMZ-1 to ADM1032ARMZ-2REEL could work between 0~120 degree C, the only difference is the default THERM# temperature. (ADM1032ARMZ-1 default 108 degree, ADM1032ARMZ-2REEL default 85) , but Poitier has programming the thermal table.	Change U38 back from ADM1032ARMZ-1 to ADM1032ARMZ-2REEL	Rev10 (A00)
12	41	VGA power transient	2009/06/10	Compal	M96 VGA Power Transient over -8% spec.	1. Add C1554, C1555, C1556 47U_0805 caps. 2. Modify C719, C720 fiom 10U_0805 to 47U_0805 3. Delete C1543, C1534, C694, C693, C692, C679, C680, C682 1u_0402 caps.	Rev10 (A00)

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