

Selek 15" Schematic

CFL-H refresh

2019/04/03

REV : A00

DY : None Installed
UMA: UMA only installed
OPB: DISCRETE OPTIMUS installed

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Selek CFLH N17P



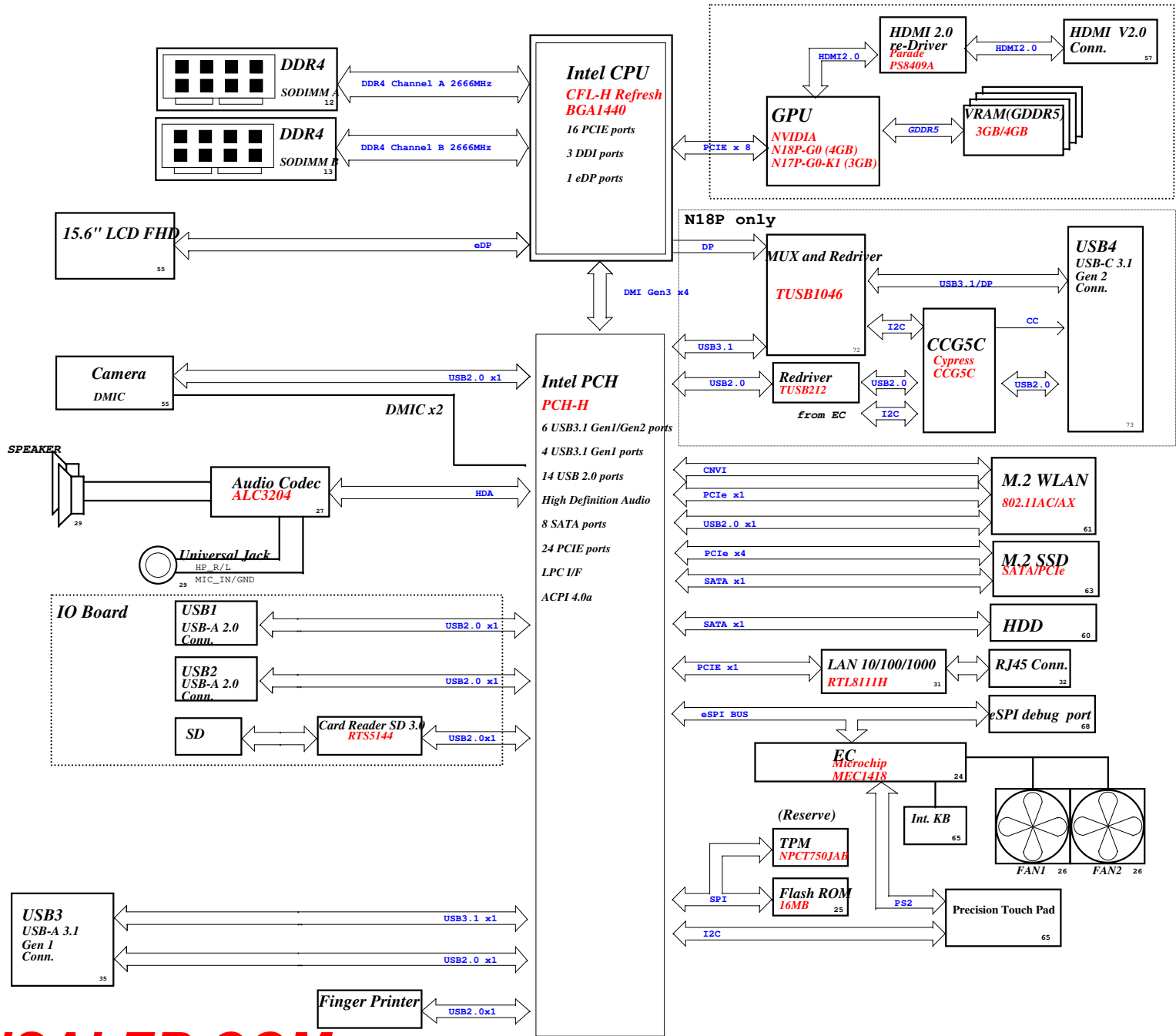
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Title Cover Page		
Size A4	Document Number Selek CFL-H	Rev A00
Date: Wednesday, April 03, 2019	Sheet 1 of	105

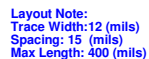
Project Code : 4PD0H7010001
PCB P/N : 18825-1
Revision : A00

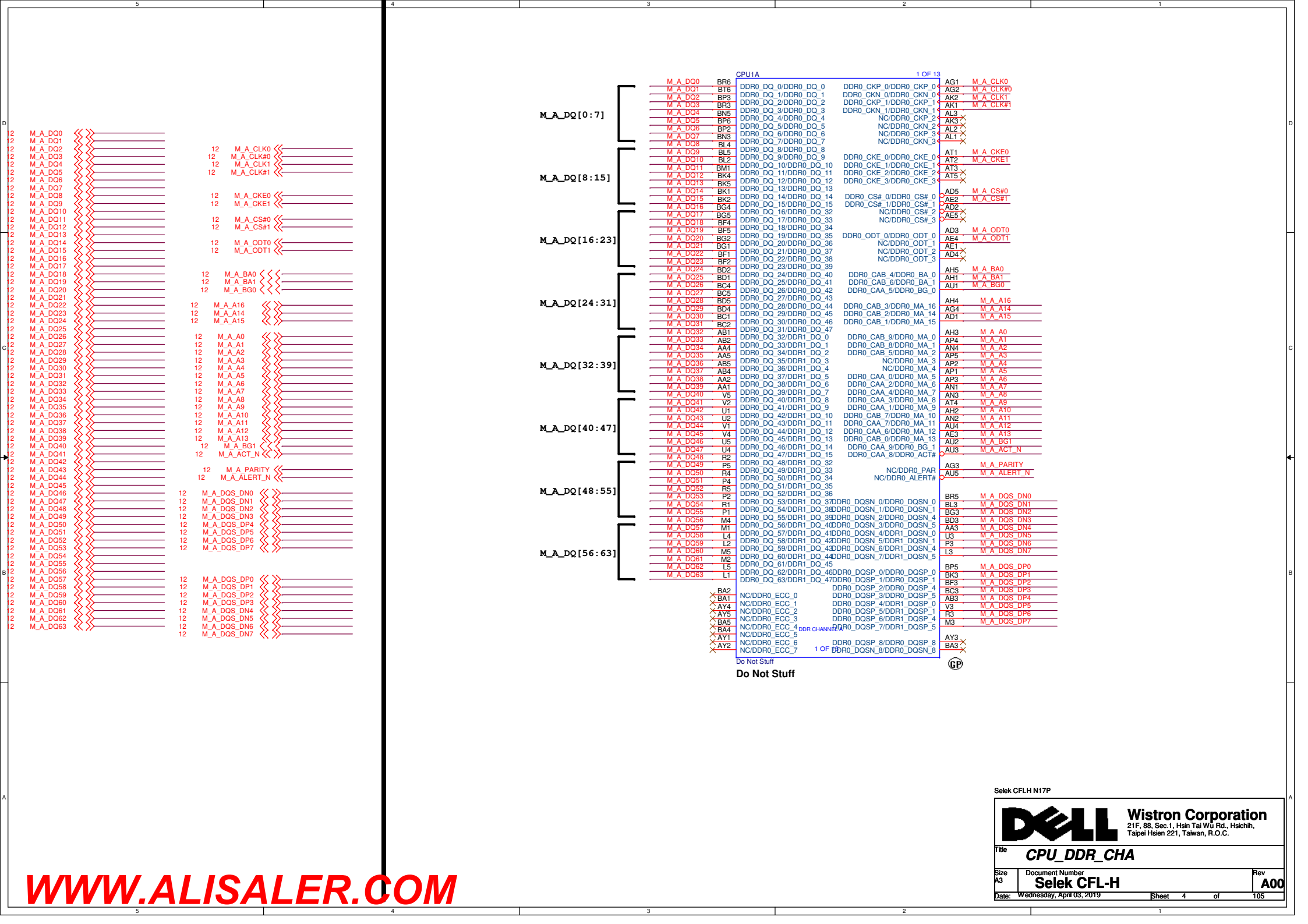
Selek CFL-H refresh Block Diagram

GPU

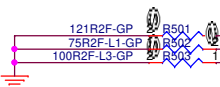


CHARGER	
ISL88739	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
3D3V PWR	3D3V S5
5V PWR	5V S5
DCBATOUT	
CPU Core Power	
NCPS1208MNTXG	46-50
NCPS1382MNTXG x 2	
NCPS1382MNTXG (23e)	
NCPS1253MNTBG	
INPUTS	OUTPUTS
DCBATOUT	VCC CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA
DDR4 SUS	
RT8231AGQW-GP	
AP15930KAI-TRG	51
INPUTS	OUTPUTS
3D3V S5	1D2V S3
	0D6V S0
DCBATOUT	2D5V S3
CPU VCCPRIM_CORE 1V	
	11
INPUTS	OUTPUTS
1D0V S5	+VCCPRIM CORE
CPU DCDC-V1D00A	
AO22262QI-10-GP-U	53
INPUTS	OUTPUTS
DCBATOUT	1D0V S5
LDO-V1D8V	
APL5930KAI-TRG	54
INPUTS	OUTPUTS
3D3V S5	1D8V S5
5V/3V S0	
TPS22966DUPR-GP	40
INPUTS	OUTPUTS
5V_S0	5V_S0
3D3V_S5	3D3V_S0
EOP10/EDRAM (23e)	
TPS22961DNYT	40
INPUTS	OUTPUTS
1D0V_S5	+V_EDRAM_VR
1D0V_S5	+V_EOP10_VR
3D3V VGA	
AO3419L	86
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
VGA CORE	
ISL62771HRTZ-GP-U	85
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
1D5V_VGA_S0	
Y8288RAC-GP	86
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0





SSID = CPU



CPU1B

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M_B_DQ00	BT11	DDR1_DQ_0/DDR0_DQ_16	DDR1_CK_P_0/DDR1_CK_P_0	AM9	M_B_CLK0
M_B_DQ01	BR11	DDR1_DQ_1/DDR0_DQ_17	DDR1_CK_N_0/DDR1_CK_N_0	AN9	M_B_CLK#0
M_B_DQ02	BT9	DDR1_DQ_2/DDR0_DQ_18	DDR1_CK_P_1/DDR1_CK_P_1	AM7	M_B_CLK1
M_B_DQ03	BR8	DDR1_DQ_3/DDR0_DQ_19	DDR1_CK_N_1/DDR1_CK_N_1	AN6	M_B_CLK#1
M_B_DQ04	BP11	DDR1_DQ_4/DDR0_DQ_20	NC/DDR1_CK_P_2	AM11	
M_B_DQ05	BN11	DDR1_DQ_5/DDR0_DQ_21	NC/DDR1_CK_N_2	AM10	
M_B_DQ06	BP8	DDR1_DQ_6/DDR0_DQ_22	NC/DDR1_CK_P_3	AJ10	
M_B_DQ07	BN8	DDR1_DQ_7/DDR0_DQ_23	NC/DDR1_CK_N_3	AJ11	
M_B_DQ08	BL12	DDR1_DQ_8/DDR0_DQ_24	DDR1_CKE_0/DDR1_CKE_0	AT8	M_B_CKE0
M_B_DQ09	BL11	DDR1_DQ_9/DDR0_DQ_25	DDR1_CKE_1/DDR1_CKE_1	AT10	M_B_CKE1
M_B_DQ10	BL8	DDR1_DQ_10/DDR0_DQ_26	DDR1_CKE_2/DDR1_CKE_2	AT7	
M_B_DQ11	BJ8	DDR1_DQ_11/DDR0_DQ_27	DDR1_CKE_3/DDR1_CKE_3	AT11	
M_B_DQ12	BJ11	DDR1_DQ_12/DDR0_DQ_28	DDR1_CS#_0/DDR1_CS#_0	AF11	M_B_CS#0
M_B_DQ13	BJ10	DDR1_DQ_13/DDR0_DQ_29	DDR1_CS#_1/DDR1_CS#_1	AE7	M_B_CS#1
M_B_DQ14	BL7	DDR1_DQ_14/DDR0_DQ_30	NC/DDR1_CS#_2	AF10	
M_B_DQ15	BJ7	DDR1_DQ_15/DDR0_DQ_31	NC/DDR1_CS#_3	AE10	
M_B_DQ16	BG11	DDR1_DQ_16/DDR0_DQ_48	DDR1_ODT_0/DDR1_ODT_0	AF7	M_B_ODT0
M_B_DQ17	BG10	DDR1_DQ_17/DDR0_DQ_49	NC/DDR1_ODT_1	AE8	M_B_ODT1
M_B_DQ18	BG8	DDR1_DQ_18/DDR0_DQ_50	NC/DDR1_ODT_2	AE9	
M_B_DQ19	BF8	DDR1_DQ_19/DDR0_DQ_51	NC/DDR1_ODT_3	AE11	
M_B_DQ20	BF11	DDR1_DQ_20/DDR0_DQ_52	DDR1_CAB_3/DDR1_MA_16	AH10	M_B_A16
M_B_DQ21	BF10	DDR1_DQ_21/DDR0_DQ_53	DDR1_CAB_2/DDR1_MA_14	AH11	M_B_A14
M_B_DQ22	BG7	DDR1_DQ_22/DDR0_DQ_54	DDR1_CAB_1/DDR1_MA_15	AF8	M_B_A15
M_B_DQ23	BF7	DDR1_DQ_23/DDR0_DQ_55	DDR1_CAB_4/DDR1_BA_0	AH8	M_B_BA0
M_B_DQ24	BB11	DDR1_DQ_24/DDR0_DQ_56	DDR1_CAB_6/DDR1_BA_1	AH9	M_B_BA1
M_B_DQ25	BC11	DDR1_DQ_25/DDR0_DQ_57	DDR1_CAA_5/DDR1_BG_0	AR9	M_B_BG0
M_B_DQ26	BB8	DDR1_DQ_26/DDR0_DQ_58	DDR1_CAB_9/DDR1_MA_0	AJ9	M_B_A0
M_B_DQ27	BC8	DDR1_DQ_27/DDR0_DQ_59	DDR1_CAB_3/DDR1_MA_1	AK6	M_B_A1
M_B_DQ28	BC10	DDR1_DQ_28/DDR0_DQ_60	DDR1_CAB_5/DDR1_MA_2	AK5	M_B_A2
M_B_DQ29	BC7	DDR1_DQ_29/DDR0_DQ_61	DDR1_CAB_7/DDR1_MA_10	AL5	M_B_A3
M_B_DQ30	BB7	DDR1_DQ_30/DDR0_DQ_62	DDR1_CAB_9/DDR1_MA_11	AL6	M_B_A4
M_B_DQ31	AA11	DDR1_DQ_31/DDR0_DQ_63	DDR1_CAB_6/DDR1_MA_12	AM6	M_B_A5
M_B_DQ32	AA10	DDR1_DQ_32/DDR1_DQ_16	DDR1_CAB_8/DDR1_MA_13	AN7	M_B_A6
M_B_DQ33	AC11	DDR1_DQ_33/DDR1_DQ_17	DDR1_CAB_9/DDR1_MA_7	AN10	M_B_A7
M_B_DQ34	AC10	DDR1_DQ_34/DDR1_DQ_18	DDR1_CAA_3/DDR1_MA_8	AN8	M_B_A8
M_B_DQ35	AA7	DDR1_DQ_35/DDR1_DQ_19	DDR1_CAA_1/DDR1_MA_9	AR11	M_B_A9
M_B_DQ36	AA8	DDR1_DQ_36/DDR1_DQ_20	DDR1_CAA_7/DDR1_MA_10	AH7	M_B_A10
M_B_DQ37	AC8	DDR1_DQ_37/DDR1_DQ_21	DDR1_CAA_9/DDR1_MA_11	AN11	M_B_A11
M_B_DQ38	AC7	DDR1_DQ_38/DDR1_DQ_22	DDR1_CAA_6/DDR1_MA_12	AR10	M_B_A12
M_B_DQ39	AC7	DDR1_DQ_39/DDR1_DQ_23	DDR1_CAB_0/DDR1_MA_13	AF9	M_B_A13
M_B_DQ40	W8	DDR1_DQ_40/DDR1_DQ_24	DDR1_CAA_9/DDR1_BG_1	AR7	M_B_BG1
M_B_DQ41	W7	DDR1_DQ_41/DDR1_DQ_25	DDR1_CAA_8/DDR1_ACT#	AT9	M_B_ACT_N
M_B_DQ42	V10	DDR1_DQ_42/DDR1_DQ_26	NC/DDR1_PAR	AJ7	M_B_PARITY
M_B_DQ43	V11	DDR1_DQ_43/DDR1_DQ_27	NC/DDR1_ALERT#	AP8	M_B_ALERT_N
M_B_DQ44	W11	DDR1_DQ_44/DDR1_DQ_28			
M_B_DQ45	W10	DDR1_DQ_45/DDR1_DQ_29			
M_B_DQ46	V7	DDR1_DQ_46/DDR1_DQ_30			
M_B_DQ47	V8	DDR1_DQ_47/DDR1_DQ_31			
M_B_DQ48	R11	DDR1_DQ_48/DDR1_DQ_48			
M_B_DQ49	P11	DDR1_DQ_49/DDR1_DQ_49			
M_B_DQ50	P7	DDR1_DQ_50/DDR1_DQ_50			
M_B_DQ51	R8	DDR1_DQ_51/DDR1_DQ_51			
M_B_DQ52	R10	DDR1_DQ_52/DDR1_DQ_52			
M_B_DQ53	P10	DDR1_DQ_53/DDR1_DQ_53			
M_B_DQ54	R7	DDR1_DQ_54/DDR1_DQ_54			
M_B_DQ55	P8	DDR1_DQ_55/DDR1_DQ_55			
M_B_DQ56	L11	DDR1_DQ_56/DDR1_DQ_56			
M_B_DQ57	M11	DDR1_DQ_57/DDR1_DQ_57			
M_B_DQ58	L7	DDR1_DQ_58/DDR1_DQ_58			
M_B_DQ59	M8	DDR1_DQ_59/DDR1_DQ_59			
M_B_DQ60	L10	DDR1_DQ_60/DDR1_DQ_60			
M_B_DQ61	M10	DDR1_DQ_61/DDR1_DQ_61			
M_B_DQ62	M7	DDR1_DQ_62/DDR1_DQ_62			
M_B_DQ63	L8	DDR1_DQ_63/DDR1_DQ_63			
AW11		NC/DDR1_ECC_0			
AY11		NC/DDR1_ECC_1			
AW8		NC/DDR1_ECC_2			
AY10		NC/DDR1_ECC_3			
AW10		NC/DDR1_ECC_4			
AY7		NC/DDR1_ECC_5			
AW7		NC/DDR1_ECC_6			
		NC/DDR1_ECC_7			


DDR CHANNEL B

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Do Not Stuff

Do Not Stuff

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CPU_DDR_CHB

Size A3 Document Number **Selek CFL-H** Rev **A00**

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AROUND_CPU

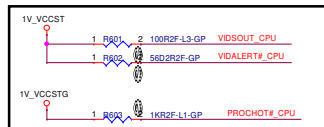
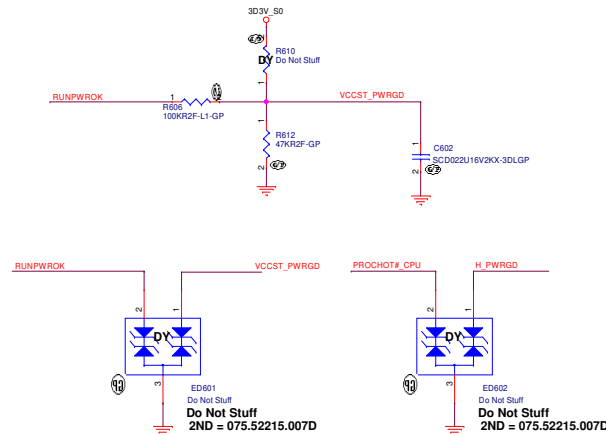


Table 13-14. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R _{PULL} [Ω]	R _{OUT} [Ω]	R _L [Ω]	R _S [Ω]	V _{CCST} [V]
VIDOUT							100	100	0	10	
VIDSCX	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT#							56	Empty	220	0	

Note: For additional information regarding SVID and power management refer to "Power Architecture Guide".



GPD11 pull high by Intel PDG1.3 request

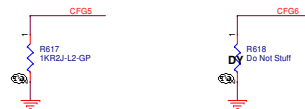
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

eDP Enable	
CFG4	1: Disable 0: Enable

PEG Training	
CFG7	1: (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.

Physical_Debug_Enabled (DPX privacy)	
CFG4	1: Disable 0: Enable (Set DPX enables bit in debug)

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled, function 2 disabled 01: Reserved - (Device 1 function 1 disabled, function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



Processor Internal Pull-Up / Pull-Down Terminations

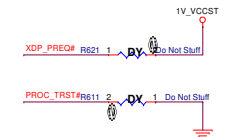
Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC _{IO}	16-60 Ω
PREQ#	Pull Up	VCC _{ST}	3 kΩ
PROC_TDI	Pull Up	VCC _{STG} ¹	3 kΩ
PROC_TMS	Pull Up	VCC _{STG} ¹	3 kΩ
CFG[19:0]	Pull Up	VCC _{IO}	3 kΩ

Note:
1. For SKL-S it should be VCC_{ST}

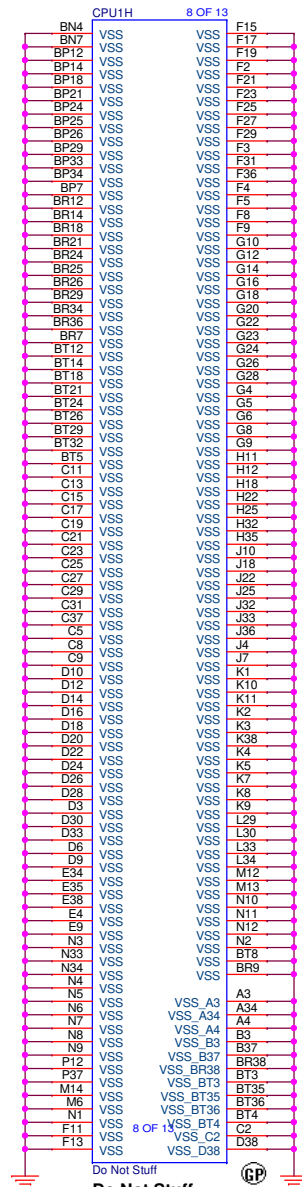
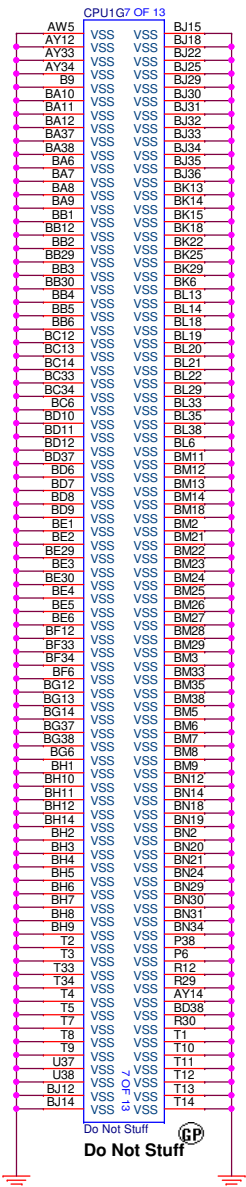
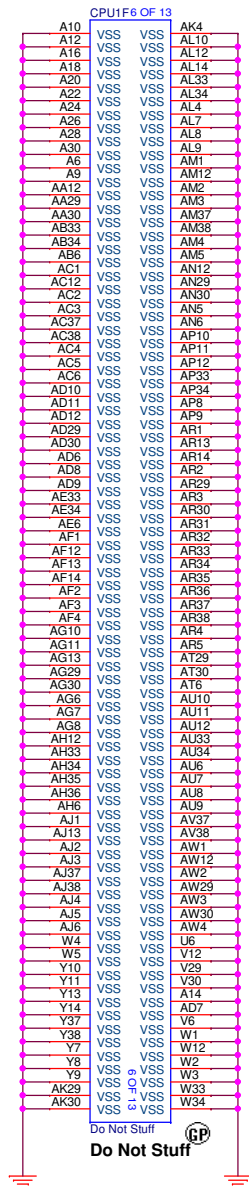
Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Shall reset sequence after PCU PLL lock until de-asserted. <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP enable. <ul style="list-style-type: none"> 1 = Enabled. 0 = Disabled. CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training. <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes. 	I/O	GTL		All processor lanes. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.




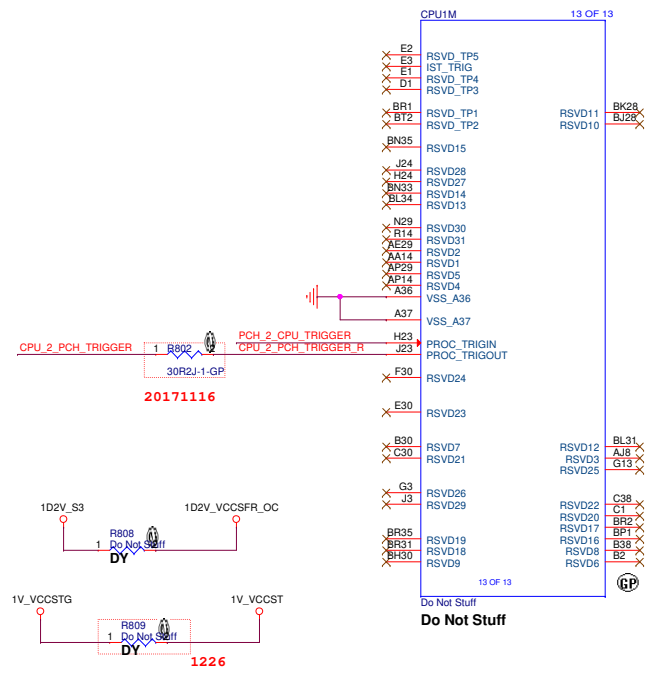
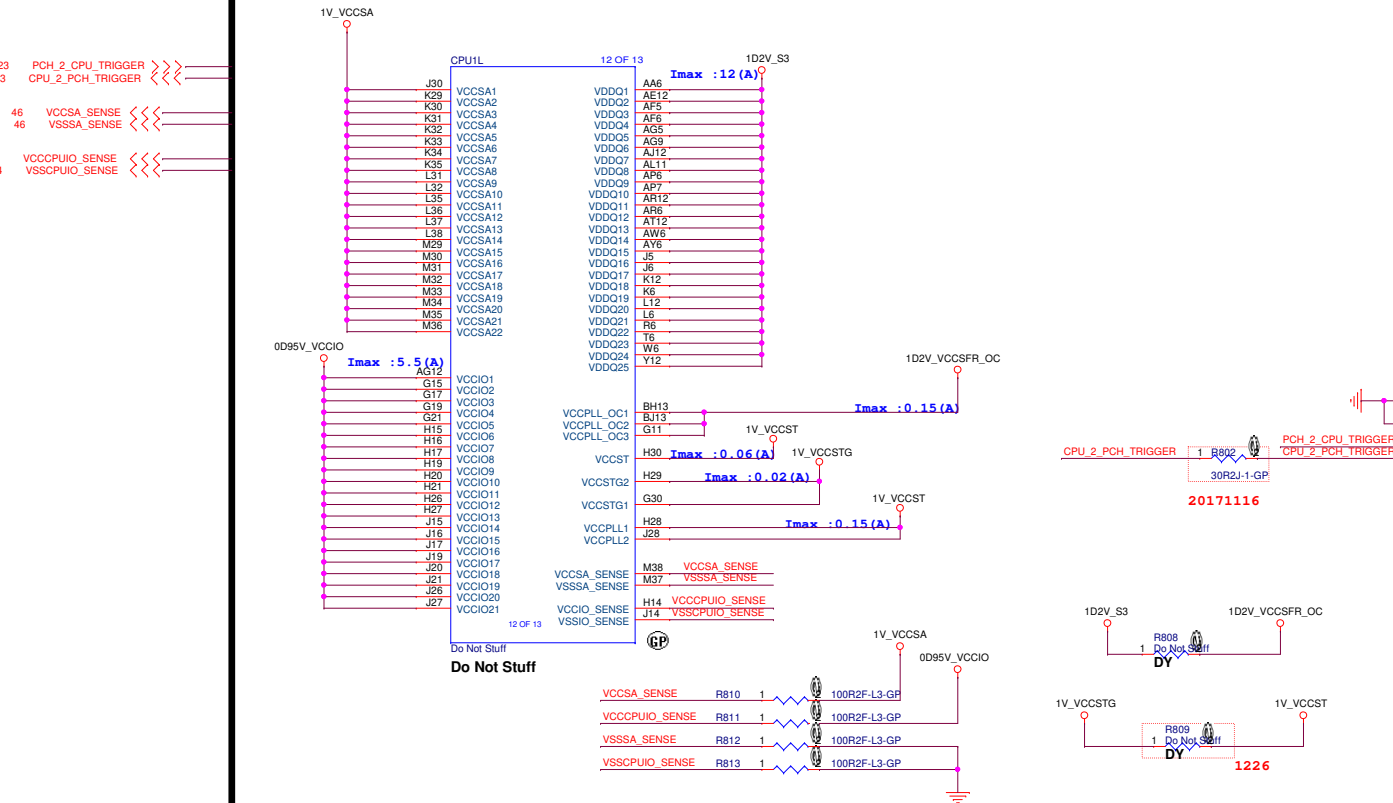
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Selek CFLH N17P



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Title CPU_GND			
Size A3	Document Number Selek CFL-H	Rev A00	
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Selek CFLH N17P

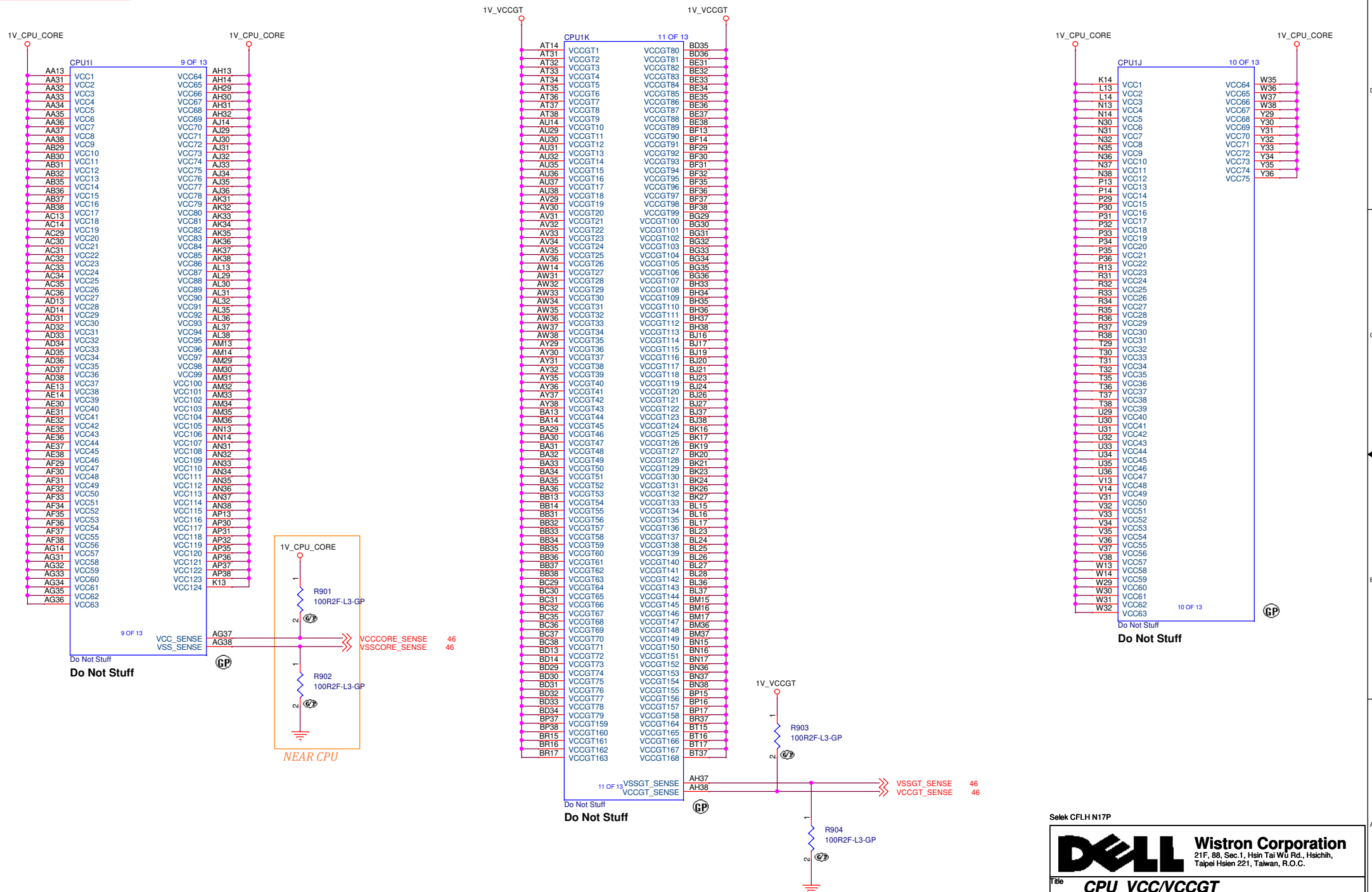
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File **CPU_POWER(VCCSA/VCCIO/VDD)**


Size Document Number Rev
Custom **Selek CFL-H** **A00**

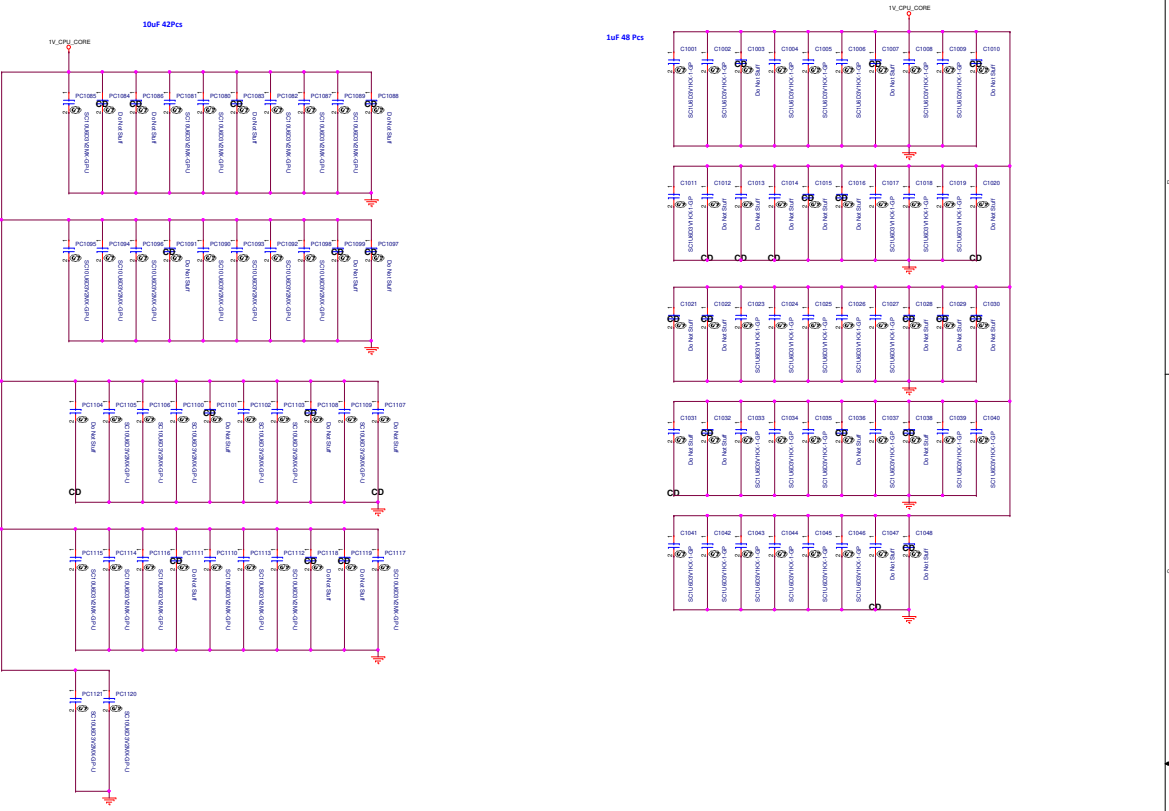
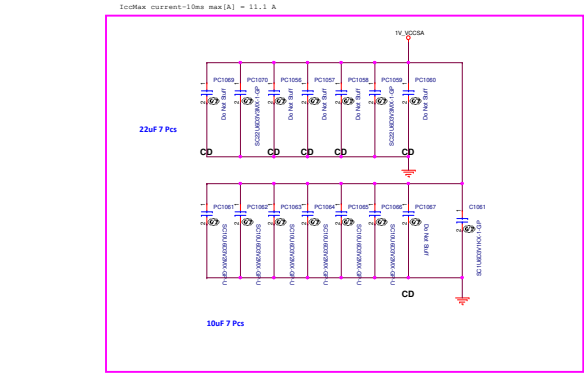
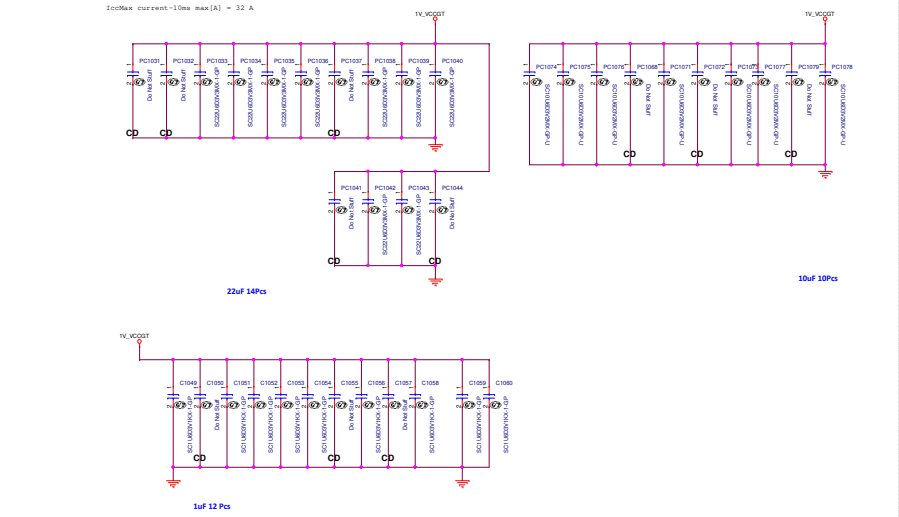
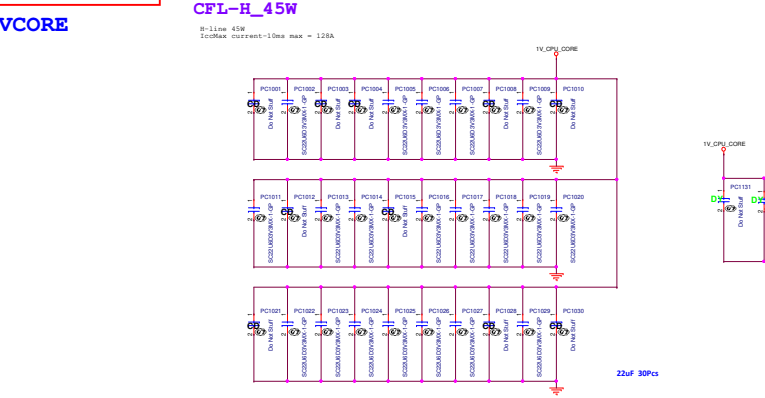
Date: Wednesday, April 03, 2019 Sheet 6 of 105

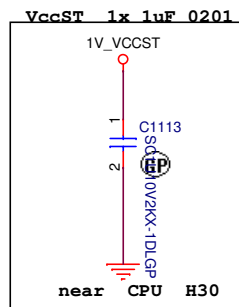
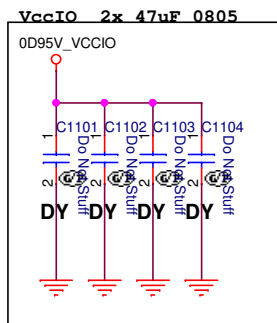
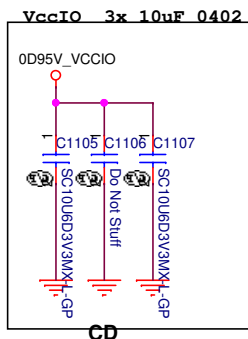
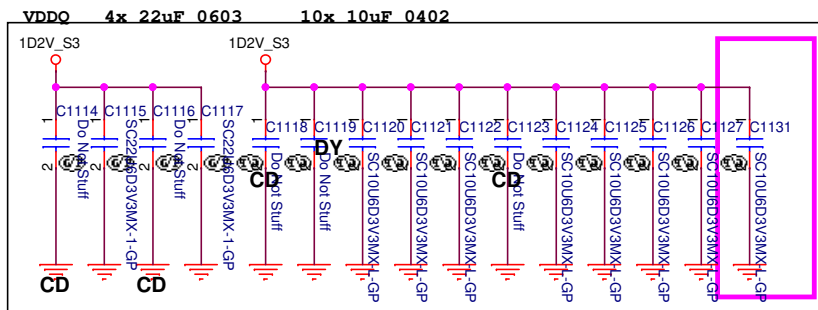
SSID = CPU



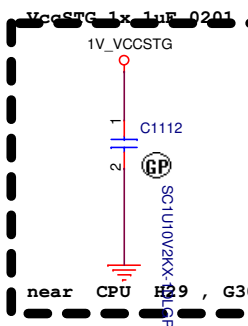
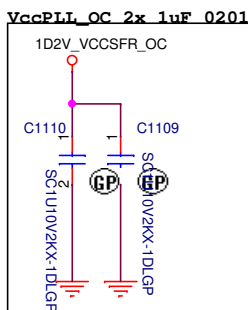
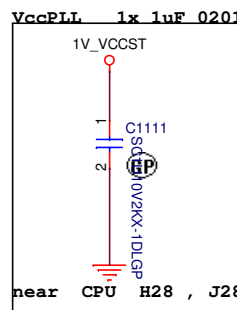
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU_VCC/VCCGT			
Size A3	Document Number Selek CFL-H	Rev A00	
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VR: +/-5% or +/-50mV
Place close to VR output



JJ 20150130

Table 50-5. Decoupling Requirements for CFL H 8+2 Processor (Sheet 1 of 2)

Domain	Board Edge cap	Backside cap	Notes
Vcc	2x 22uF 0603		
	8x 47uF 0805		
		48x 1uF 0201	
		42x 10uF 0402	
		10x 22uF 0603	
VccGT	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	
VccSA	2x 47uF 0805		
	2x 22uF 0603		
		7x 10uF 0402	
VDDQ		1x 1uF 0201	
		4x 22uF 0603	
		11x 10uF 0402	
VccIO		3x 10uF 0402	
		3x 0402 (placeholder)	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
VccST		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route VccST closest adjacent layer over any power net other than ground.
VccSTG		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail.
VccPLL		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
		1x 22uF/47uF 0805 (placeholder)	*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
Domain	Board Edge cap	Backside cap	Notes
VccPLL_OC		2x 1uF 0201	Must be Ground referenced. Share with VDDQ. Board resistance from BGA to Power gate should be less than 86mOhm.

Note: High Current Rail assuming 600KHz for VR bandwidth. Higher VR bandwidth assumptions results in lower quantity of MLCC (0805/0603) to meet the same AC loadline.
Note: It is important to make sure that the noise on VCCPLL rail must be limited to the +/-5% VR specification below 150KHz - as this will potentially impact the PLL failing to phase lock. Where necessary, the 0805 placeholder can be stuffed with a 22uF or 47uF to assist noise reduction. While stuffing the 0805 cap may reduce noise coupling, one should still route the PLL rail carefully (i.e. to avoid noisy and high current rail) to mitigate any potential issue.

Selek CFLH N17P

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CPU (Power CAP2)			
Size	Document Number	Rev	
Custom	Selek CFL-H		A00
Date:	Wednesday, April 03, 2019	Sheet	11 of 105





5

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2

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D

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C

B


B

A

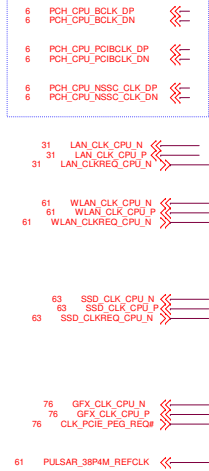
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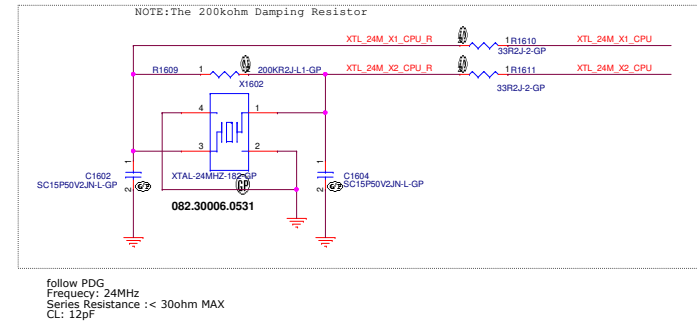
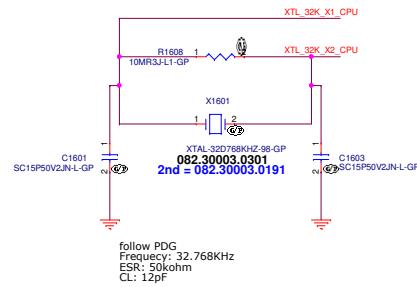
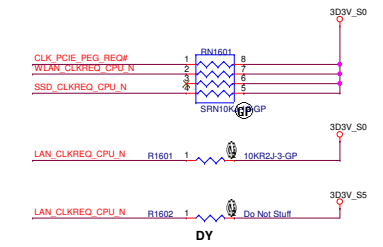
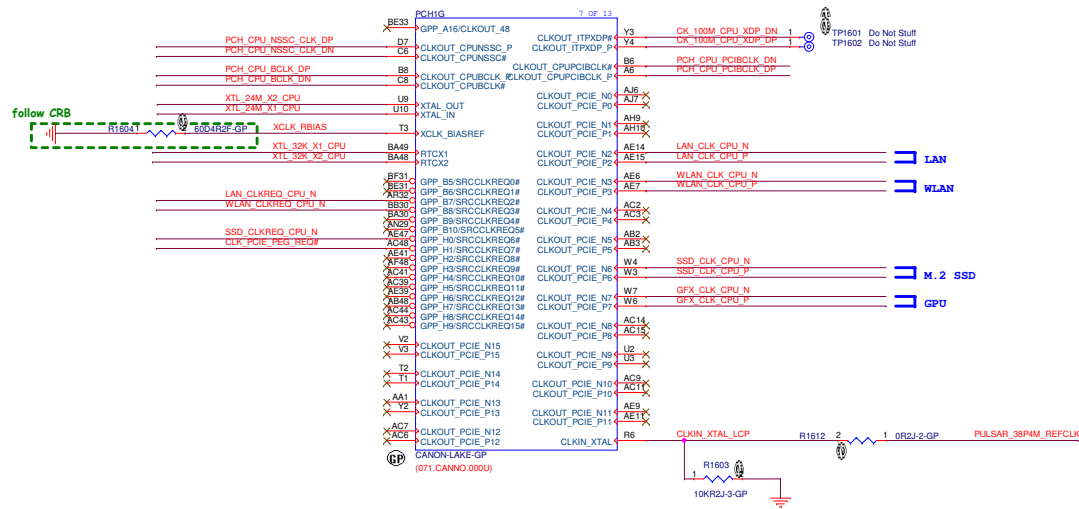
Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RESERVED			
Size A4	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 14	of 105

TO CPU CLOCK



- The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express® Root Ports
- SRCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
- SRCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
- SRCLKREQ#[15:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:0] differential clock pairs



24 MHz Crystal Specifications (Sheet 1 of 2)

Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	≤ 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk jitter	≤ 150	pS	Includes cycle to cycle and period
Operating Temperature	-40 to 85	°C	

Parameter	Values	Units	Max/Min Range
Series Resistance	≤ 30	Ω	
Aging	±3	PPM	

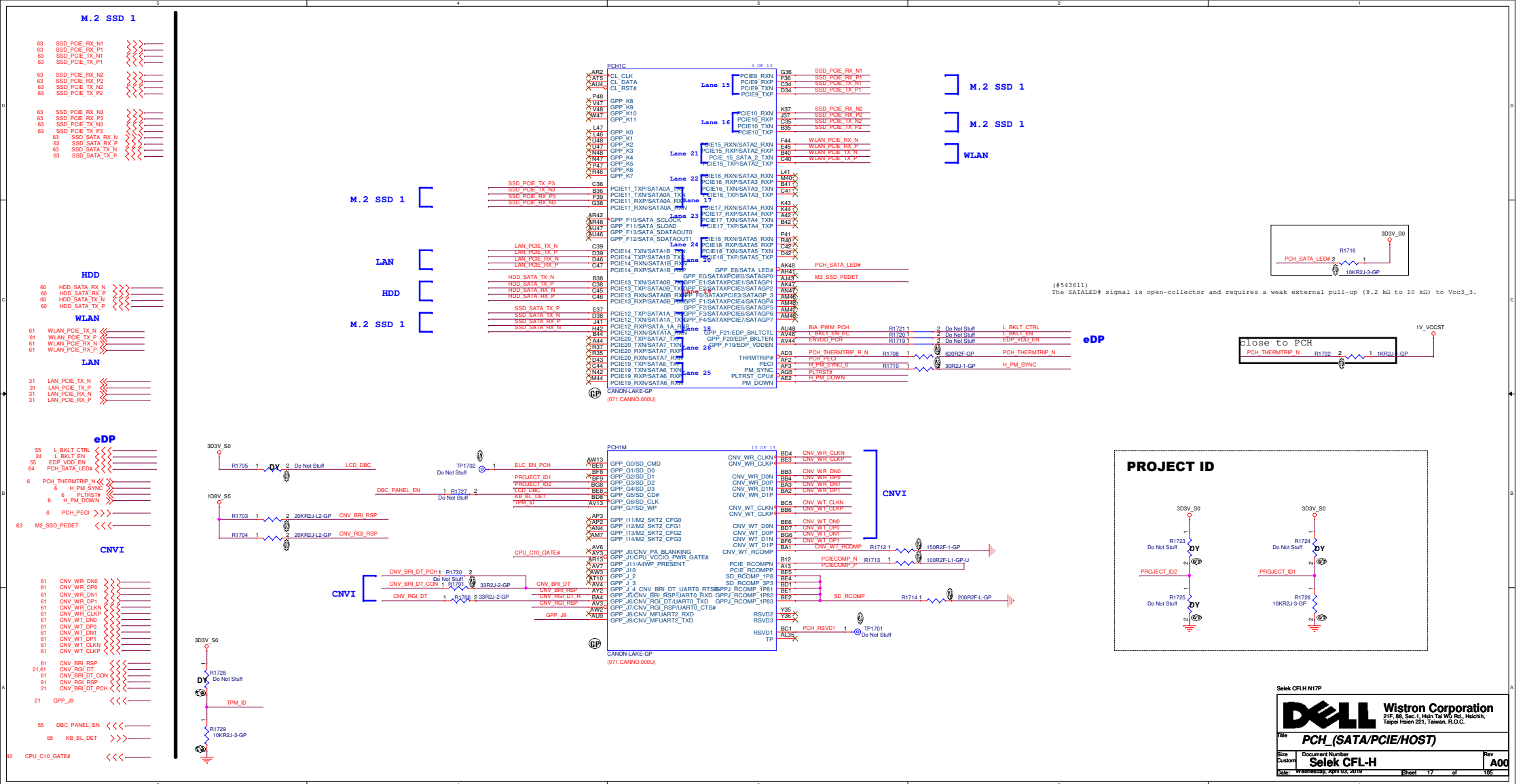
Selek CFLH N17P

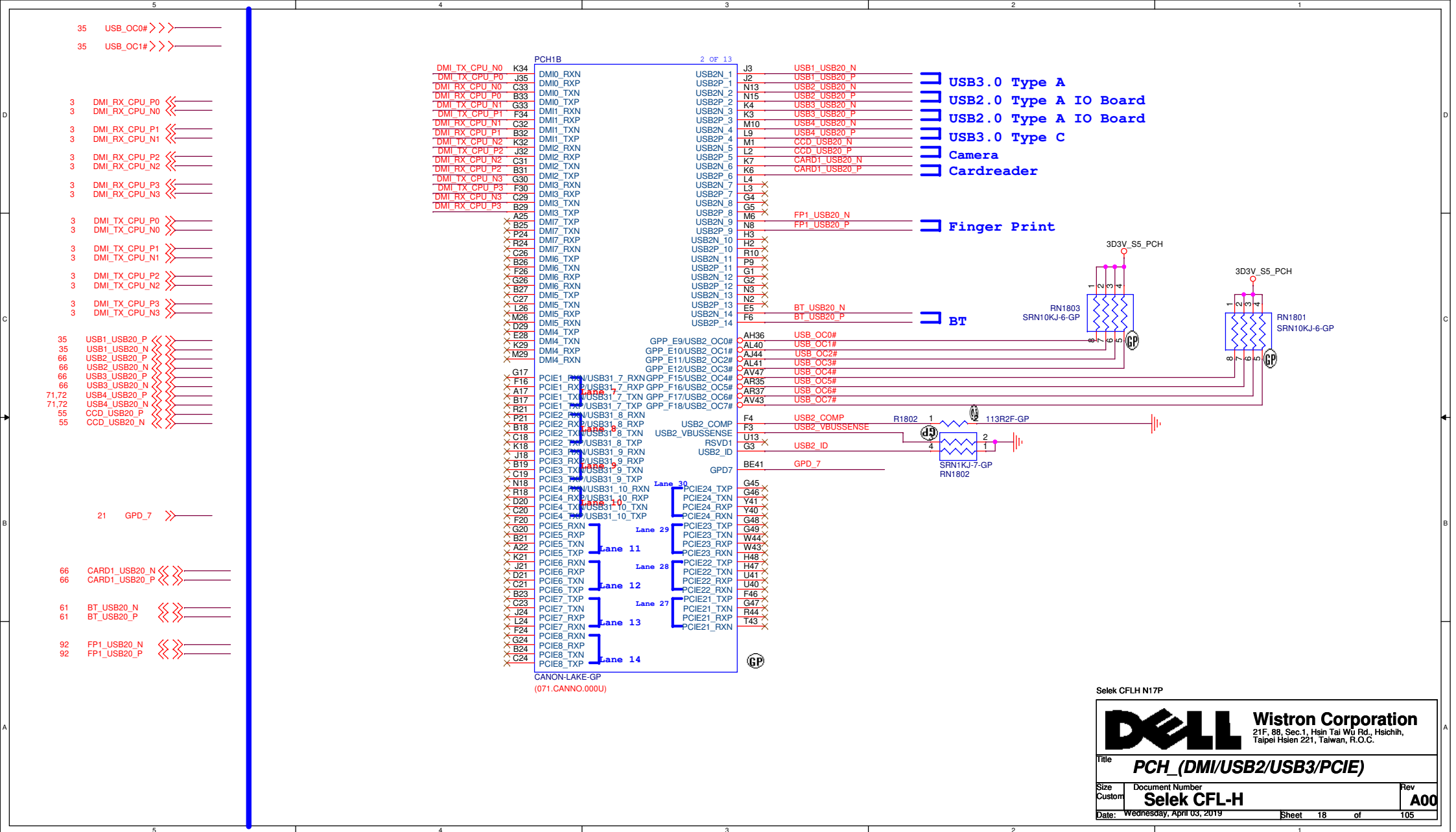
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

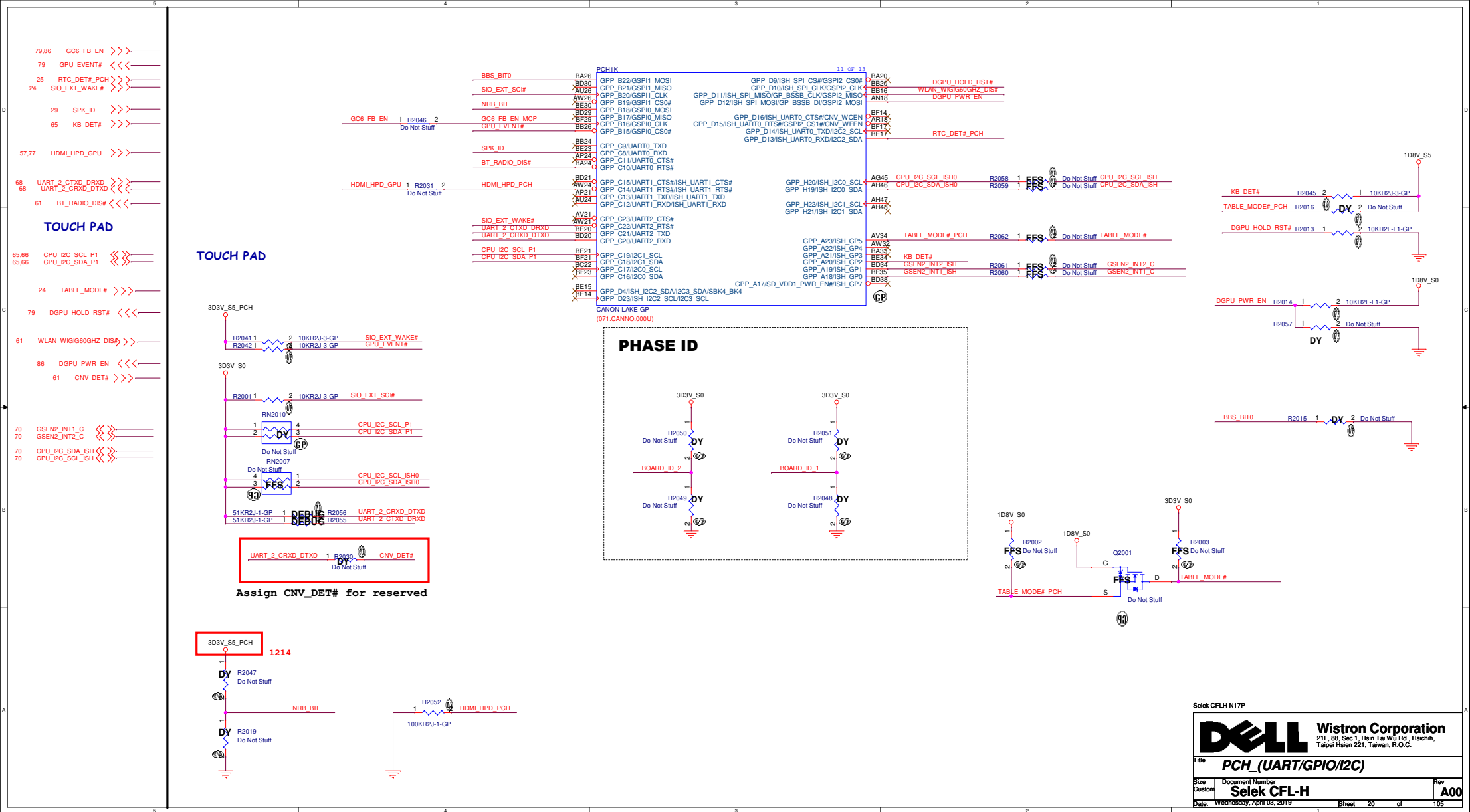
Title **PCH (CLK)**

Size Custom Document Number **Selek CFL-H** Rev **A00**

Date: Wednesday, April 10, 2019 Sheet 16 of 106







Selek CFLH N17P

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichah, Taipei Hsien 221, Taiwan, R.O.C.			
File PCH (UART/GPIO/I2C)			
Size	Document Number	Rev	
Custom	Selek CFL-H	A00	
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GPIO	GPP_B14 SPKR	GPP_B18 GSPIO_MOSI	GPP_C2 SMBALERT#	GPP_B22 GSPII_MOSI	GPP_C5 SMBALERT#	SPIO_MOSI SPIO_MISO	GPP_H15 SML3ALERT#
Schematic		default is internal pull down add TP at PCH side		default is internal pull down add TP at PCH side			

GPIO	GPP_B23 SML1ALERT# PCHHOT#	SPIO_IO2	SPIO_IO3	HDA_SDO/ I2S0_TXD	GPP_H12 SML2ALERT#	GPP_I6 DDPB_CTRLDATA	GPP_I8 DDPC_CTRLDATA
Schematic					internal pull down	Pull high at page 19	internal pull down

need check the latest CRB,PDG

GPIO	GPP_I10	GPP_F23/ DPPF_CTRLDATA	GPP_J4 CNV_BRI_DT UART0_RTS#	GPP_J6 CNV_RGI_DT UART0_TXD	GPP_J9	GPD7
Schematic		internal pull down				

Table 9-1. Pin Straps (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
GPP_B14 / SPCR	Top level Overclock	Rising edge of PCH_PWRON	This signal has a weak internal pull-down. 1 = Disable "Top level" mode. (Default) 0 = Enable "Top level" mode. This enables an address on-chip buffer and allows the chip to access the back channel of the original host block. PCH will report A00 (Address 0) to the master going to the master address (A00, A01, or A02) as indicated in the master block and will stop. Notes: 1. The internal pull-down is disabled after PCH_PWRON is high. 2. This signal is in the primary well. 3. The signal is in the primary well. 4. This signal is in the primary well.
GPP_B18 / GSPIO_MOSI	No device	Rising edge of PCH_PWRON	This signal has a weak internal pull-down. 1 = Disable "No device" mode. (Default) 0 = Enable "No device" mode. This enables the 100 MHz system clock output. This function is valid after entering VDDIO.
GPP_C2 / SMBALERT#	TLS Core activity	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 1 = Disable "No device" mode. (Default) 0 = Enable "No device" mode. This enables the 100 MHz system clock output. This function is valid after entering VDDIO.

Signal	Usage	When Sampled	Comment
GPP_B14 / SPCR	Top level Overclock	Rising edge of PCH_PWRON	This signal has a weak internal pull-down. 1 = Disable "Top level" mode. (Default) 0 = Enable "Top level" mode. This enables an address on-chip buffer and allows the chip to access the back channel of the original host block. PCH will report A00 (Address 0) to the master going to the master address (A00, A01, or A02) as indicated in the master block and will stop. Notes: 1. The internal pull-down is disabled after PCH_PWRON is high. 2. This signal is in the primary well. 3. The signal is in the primary well. 4. This signal is in the primary well.
GPP_B18 / GSPIO_MOSI	No device	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 1 = Disable "No device" mode. (Default) 0 = Enable "No device" mode. This enables the 100 MHz system clock output. This function is valid after entering VDDIO.
GPP_C2 / SMBALERT#	TLS Core activity	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 1 = Disable "No device" mode. (Default) 0 = Enable "No device" mode. This enables the 100 MHz system clock output. This function is valid after entering VDDIO.

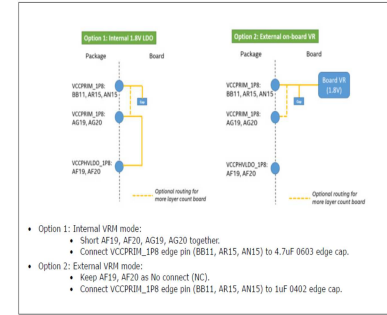
Signal	Usage	When Sampled	Comment
GPP_B14 / SPCR	Top level Overclock	Rising edge of PCH_PWRON	This signal has a weak internal pull-down. 1 = Disable "Top level" mode. (Default) 0 = Enable "Top level" mode. This enables an address on-chip buffer and allows the chip to access the back channel of the original host block. PCH will report A00 (Address 0) to the master going to the master address (A00, A01, or A02) as indicated in the master block and will stop. Notes: 1. The internal pull-down is disabled after PCH_PWRON is high. 2. This signal is in the primary well. 3. The signal is in the primary well. 4. This signal is in the primary well.
GPP_B18 / GSPIO_MOSI	No device	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 1 = Disable "No device" mode. (Default) 0 = Enable "No device" mode. This enables the 100 MHz system clock output. This function is valid after entering VDDIO.
GPP_C2 / SMBALERT#	TLS Core activity	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 1 = Disable "No device" mode. (Default) 0 = Enable "No device" mode. This enables the 100 MHz system clock output. This function is valid after entering VDDIO.

Signal	Usage	When Sampled	Comment
GPP_F23 / DPPF_CTRLDATA	Display Port 7 Detected	Rising edge of PCH_PWRON	This signal has a weak internal pull-down. 0 = Port 7 is not detected. (Default) 1 = Port 7 is detected. Notes: 1. The internal pull-down is disabled after PCH_PWRON is high. 2. This signal is in the primary well. 3. This signal is in the primary well.
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 0 = 38.4 MHz XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. Notes: 1. The internal pull-down is disabled after GSPII_MOSI is high. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	PL2 CNV Mode Select	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 0 = VCCSPI is connected to 1.8V rail. 1 = VCCSPI is connected to 1.1V rail. Notes: 1. The internal pull-down is disabled after GSPII_MOSI is high. 2. This signal is in the primary well.
GPP_J9	1.8V VCCSPI	Rising edge of GSPII_MOSI	This signal has a weak internal pull-down. 0 = VCCSPI is connected to 1.8V rail. 1 = VCCSPI is connected to 1.1V rail. Notes: 1. The internal pull-down is disabled after GSPII_MOSI is high. 2. This signal is in the primary well.
GPD7	Reserved	Rising edge of GSPII_MOSI	External pull-up is required. Recommend 100 kOhm. The strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

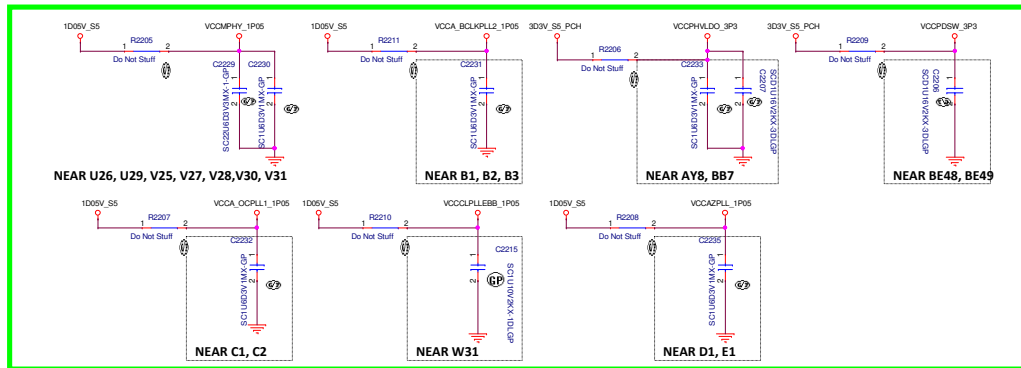
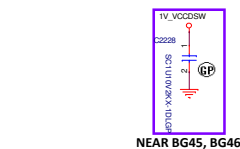
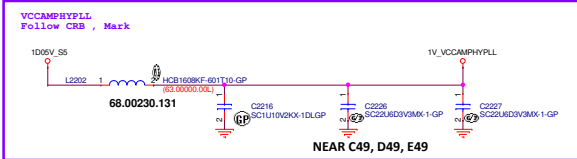
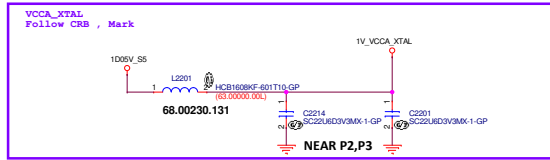
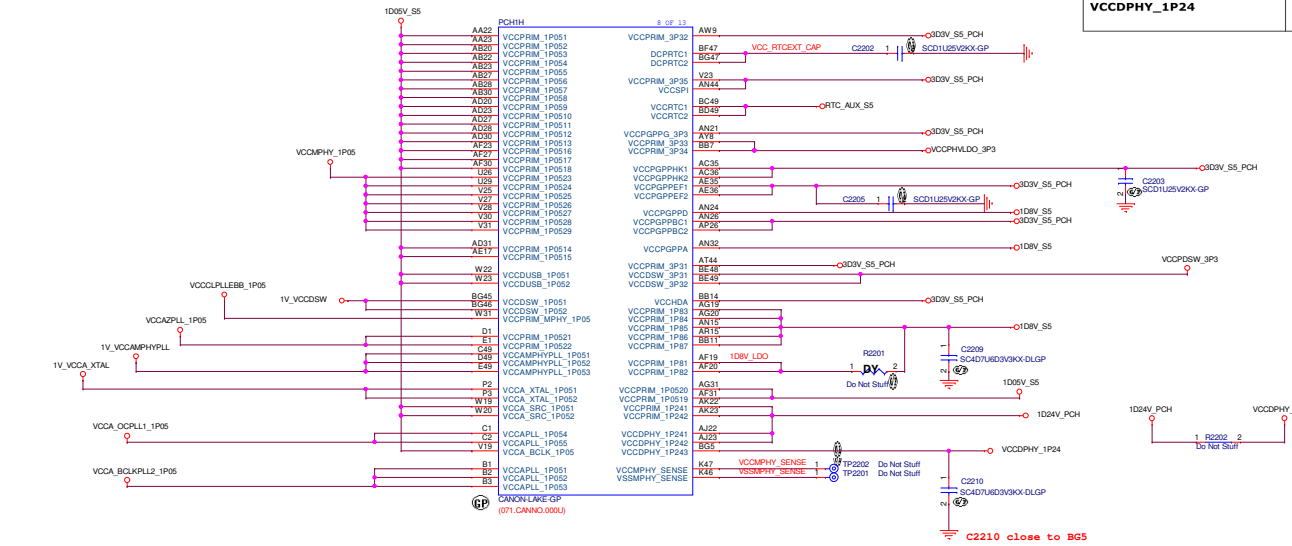
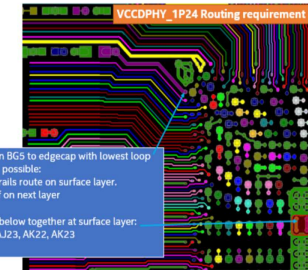
VCCDPHY_1P24

1.24V for CNVI logic. This rail can be supplied internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.

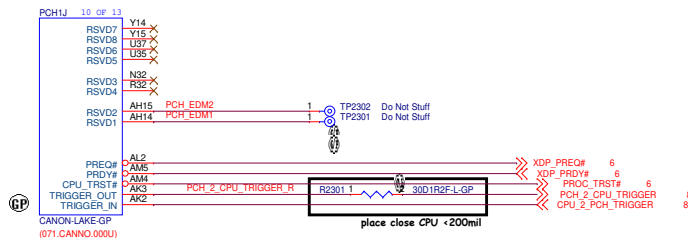
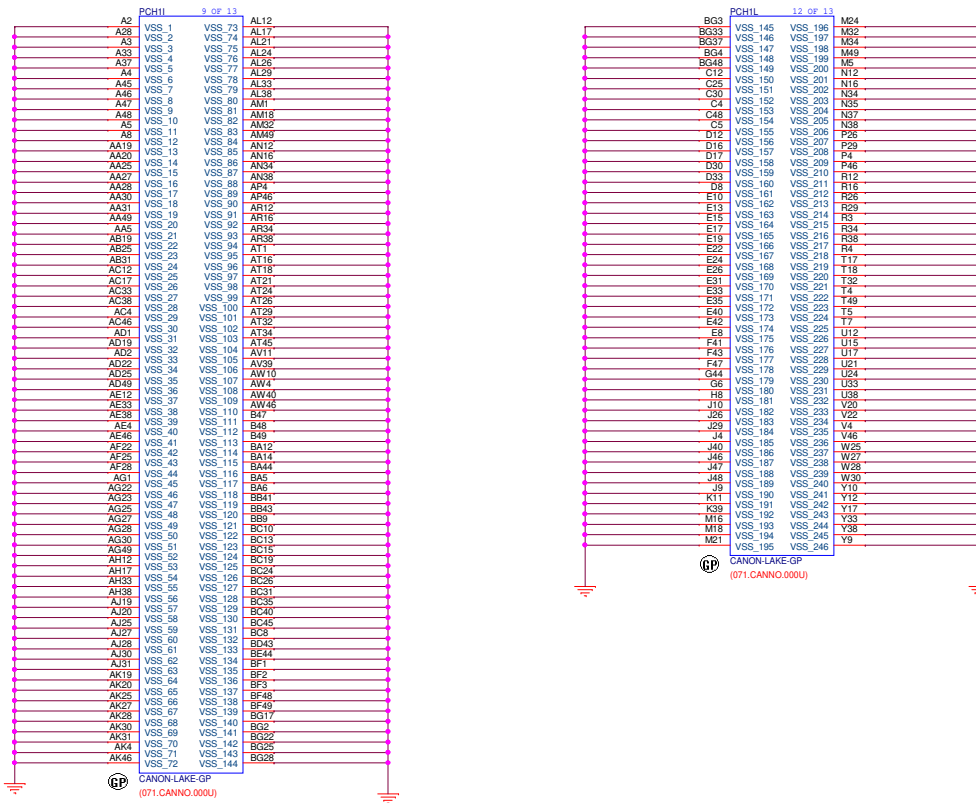
Figure 50-9: CFL PCH-H Power Rail VRM Recommendations



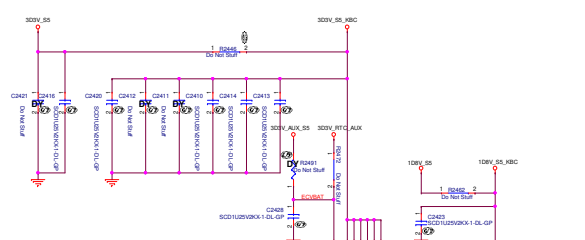
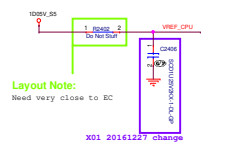
CFL PCH-H VCCDPHY_1P24 Routing



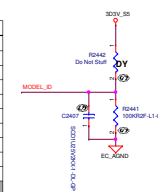
Selek CFLH N17P



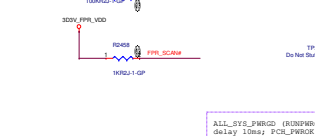
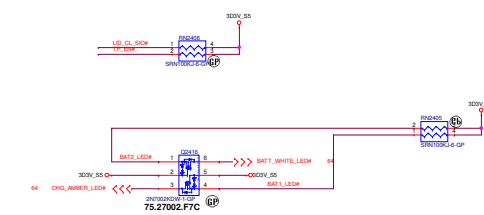
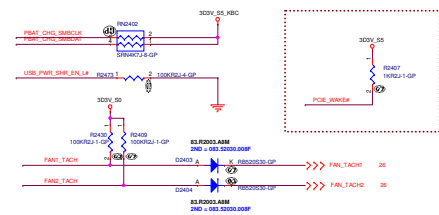
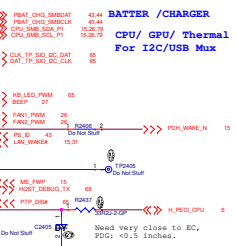
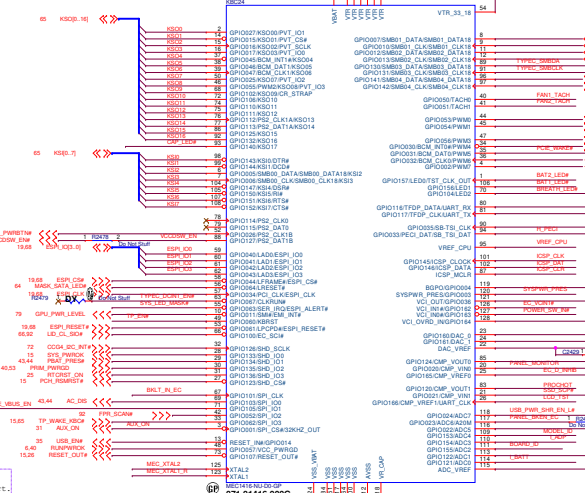
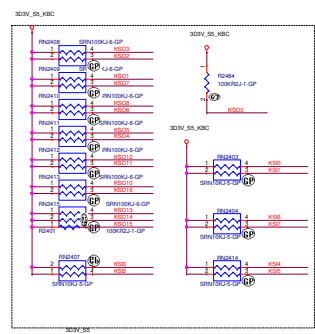
Main Func = KBC



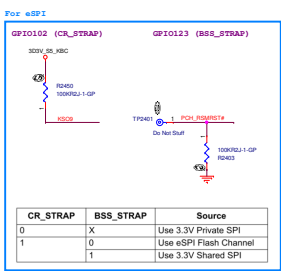
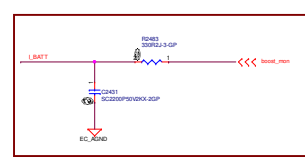
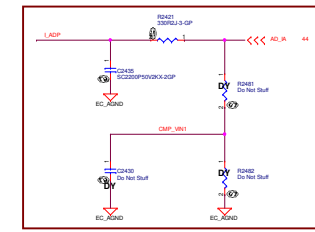
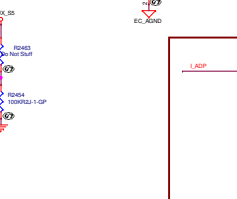
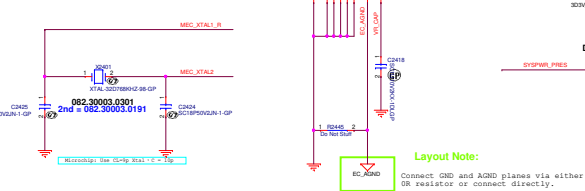
#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.0K	2.801
3	X02	100.0K	27.0K	2.506
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3



#	MODEL (DIPCH0153)	PULL-UP RESISTOR	PULL-DOWN RESISTOR	VOLTAGE
1	Nivada-N1 IP-G0-K1	100.0K	10.0K	
2		100.0K	17.8K	2.801
3	Nivada-N1 SP-G0	100.0K	27.0K	2.598
4		100.0K	37.4K	2.402
5	Nivada-N1 SE-G0	100.0K	49.9K	2.201
6		100.0K	64.9K	2.001
7	Nivada-N1 SE-G1	100.0K	82.5K	1.808
8		100.0K	107K	1.594
9		100.0K	154K	1.399
10		100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

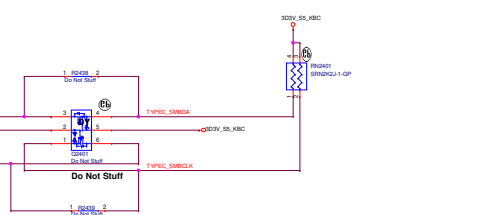
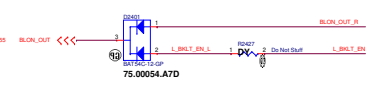


```
ALL_SYS_PWRGD (RUNPWROK)assert,  
delay 10ms; PCH_PWROK( RESET_OUT# )assert.
```



CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

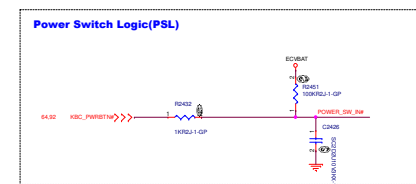
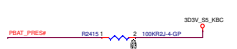
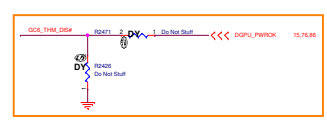
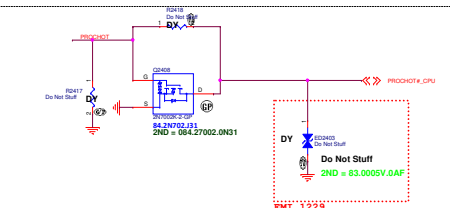


For USB TypeC

For CCG5

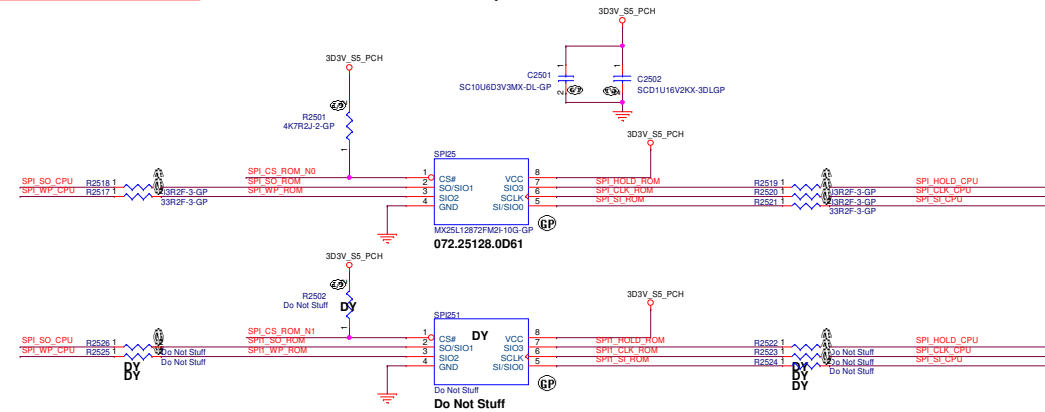
Need check

Follow EV project circuit DY Q2417 (R013_20171026)



SSID = Flash.ROM SPI FLASH ROM (32M byte) for PCH

15 SPI_CS_ROM_N0 >>>
15,21,91 SPI_SO_CPU <<<
15,21 SPI_WP_CPU <<<
15,21 SPI_HOLD_CPU <<<
15,91 SPI_CLK_CPU >>>
15,21,91 SPI_SI_CPU >>>
15 SPI_CS_ROM_N1 >>>



Main Func = RTC

BTY RTC CR2016_30MM KTS 2PIN
1st= 23.25212.011
-1 20161118

20 RTC_DET#_PCH <<<
24 RTCRST_ON >>>
24 VCCDSW_EN# >>>
15,40,45 3V_5V_POK >>>
52,53 3V_5V_DSW_OK <<<

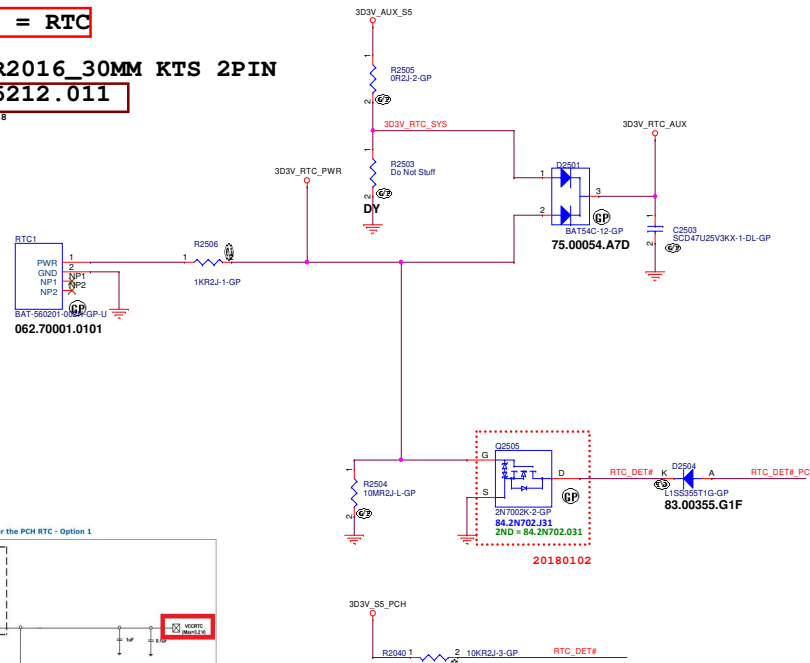
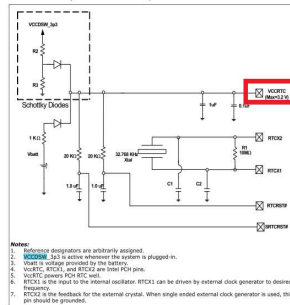
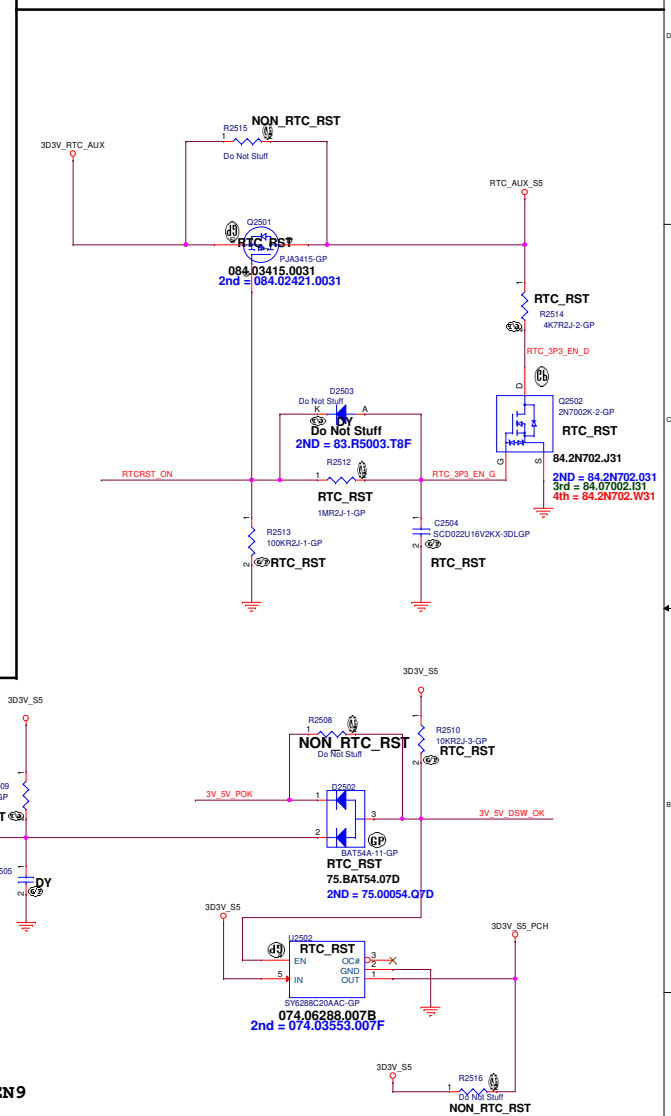


Figure 28-2: External Circuitry for the PCH RTC - Option 1



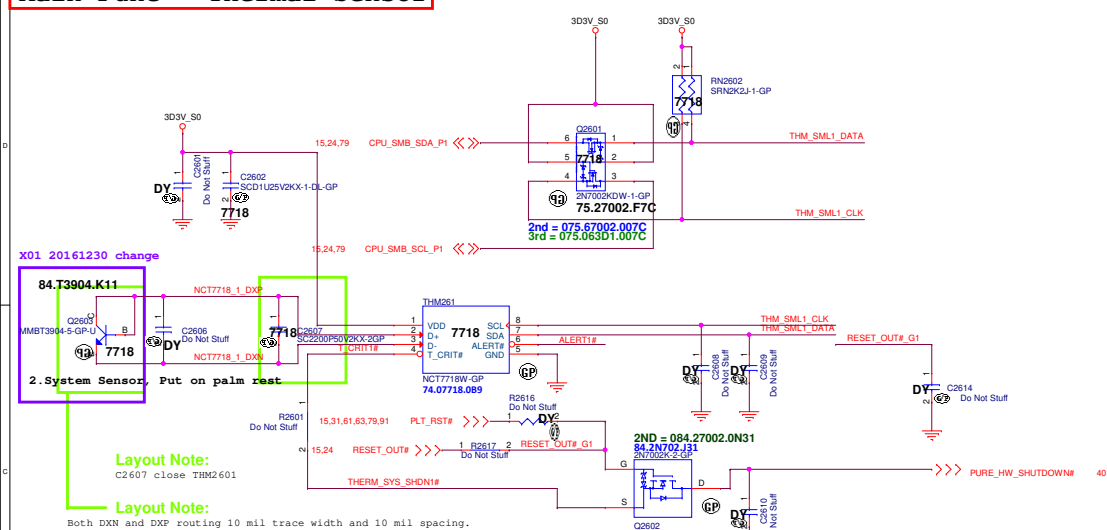
Notes:
1. Resistor designations are arbitrarily assigned.
2. R2508EN is active whenever the system is plugged in.
3. VCCDSW_EN# is active whenever the system is plugged in.
4. VCCDSW_EN# and VCCDSW_EN# are active-low signals.
5. VCCDSW_EN# is active-low.
6. RTC is the input to the internal oscillator. RTC can be driven by external clock generator to desired frequency.
7. RTC is a free feedback for the external crystal. When single ended external clock generator is used, this pin should be grounded.



RTC GEN9

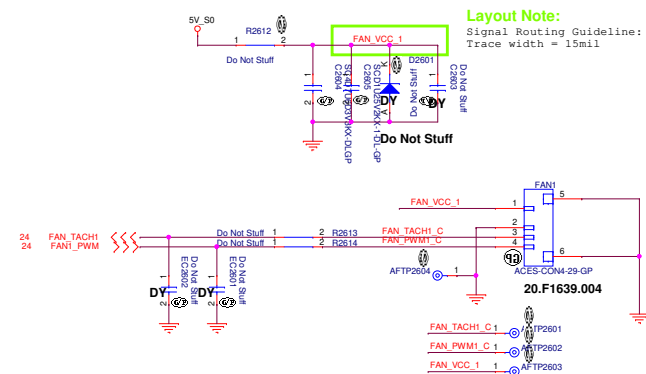
Selek CFLH N17P

Main Func = Thermal Sensor

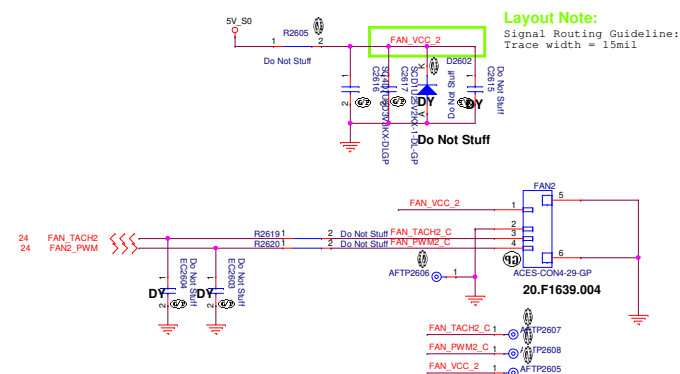


TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PWM FAN1

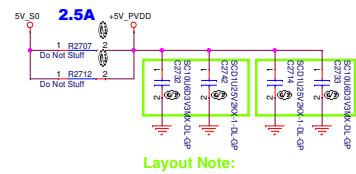
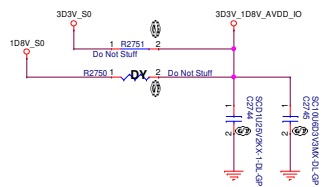
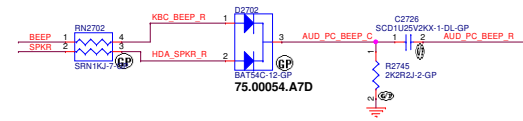
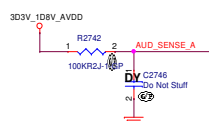
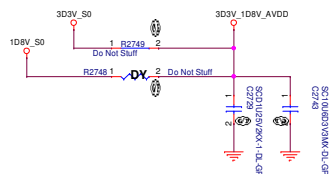
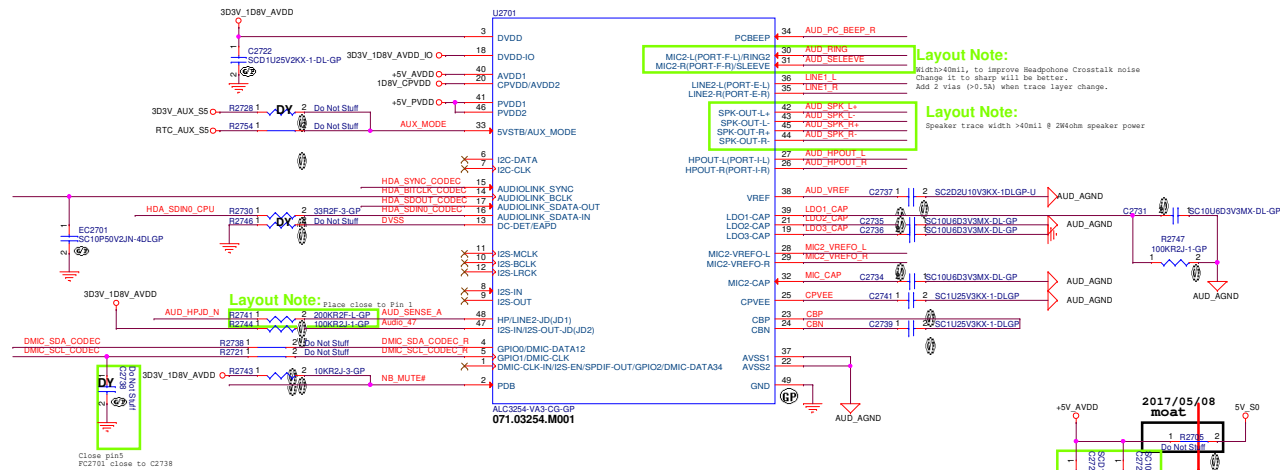
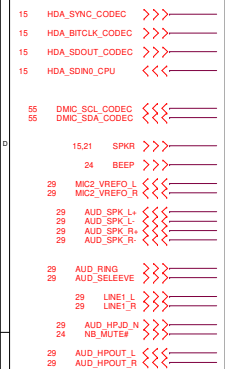


PWM FAN2



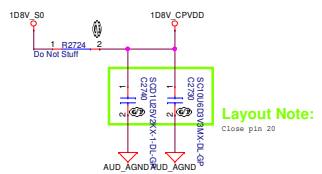
Selek CFLH N17P

DELL		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title THERMAL NCT7718W/Fan			
Size	Document Number	Rev	
Custom	Selek CFL-H	A00	
Date	Wednesday, April 03, 2019	Sheet	28 of 106



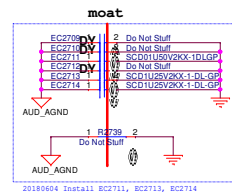
Layout Note:

Close pin46



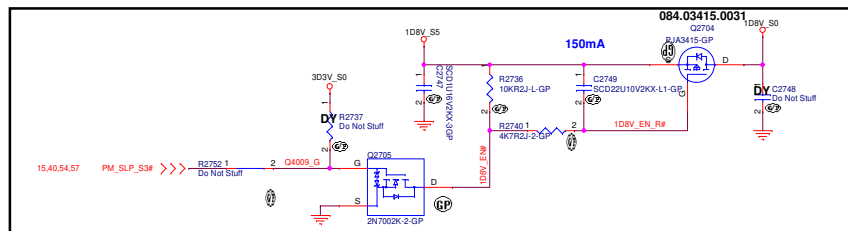
Layout Note:

Close pin 20



Layout Note:

R2739 should place nearby codec IC.



Selek CFLH N17P

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Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RESERVED			
Size A4	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 28	of 105

Main Func = Audio

20 SPK_ID <<>>

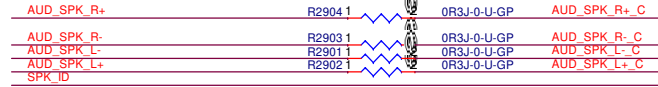
27 AUD_SPK_L+ >>>>
 27 AUD_SPK_L- >>>>
 27 AUD_SPK_R+ >>>>
 27 AUD_SPK_R- >>>>

27 MIC2_VREFO_R >>>>
 27 MIC2_VREFO_L >>>>

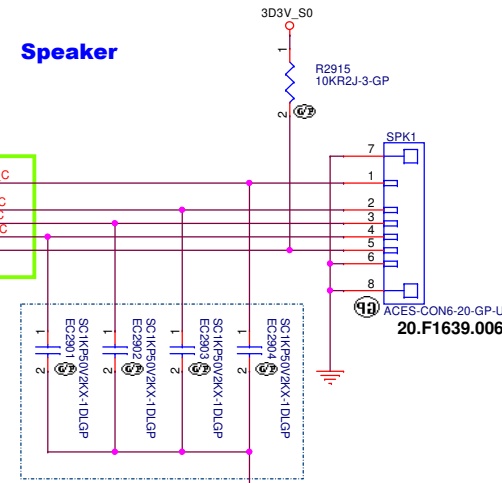
27 AUD_RING <<<<
 27 AUD_HPOUT_L >>>>
 27 LINE1_L >>>>
 27 AUD_HPOUT_R >>>>
 27 LINE1_R >>>>
 27 AUD_SELEEVE <<<<
 27 AUD_HPJD_N <<<<

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

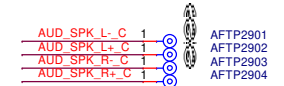


Speaker

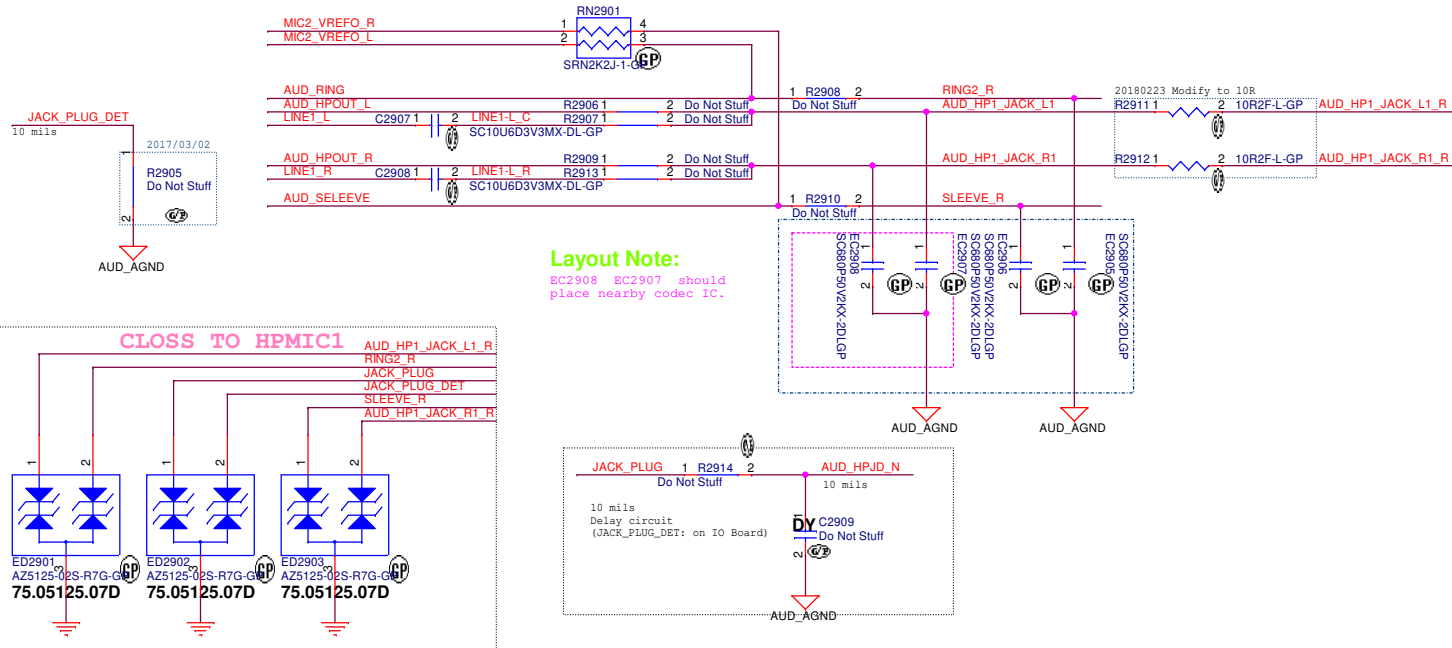


12/17 Clark move close to connector

CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

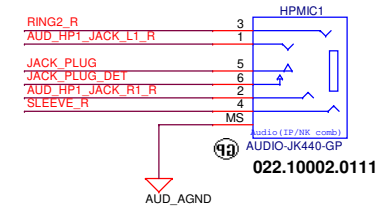


Universal Jack (Moved to I/O Board)




Layout Note:

EC2908 EC2907 should place nearby codec IC.



Selek CFLH N17P

Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 30 of	105

16 LAN_CLK_CPU_P
16 LAN_CLK_CPU_N
16 LAN_CLKREQ_CPU_N

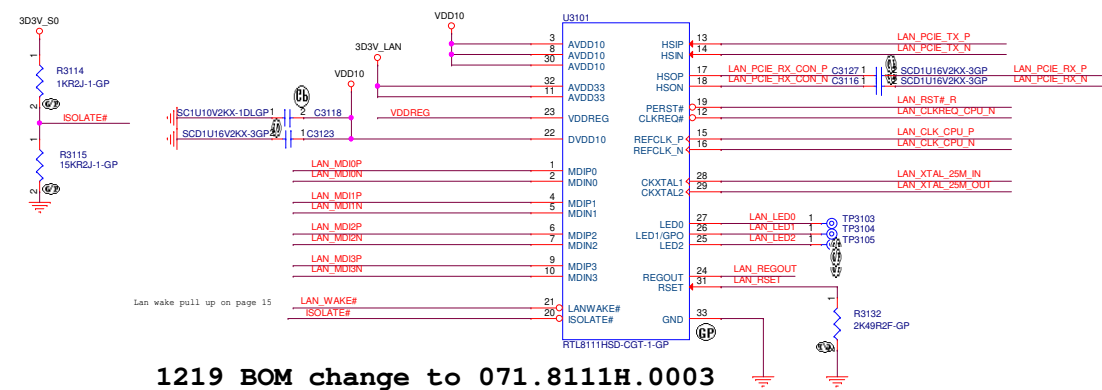
17 LAN_PCIE_TX_P
17 LAN_PCIE_TX_N
17 LAN_PCIE_RX_N
17 LAN_PCIE_RX_P

15,26,61,63,79,91 PLT_RST# >>>

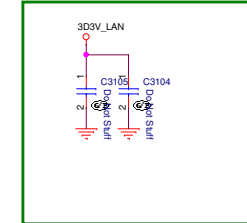
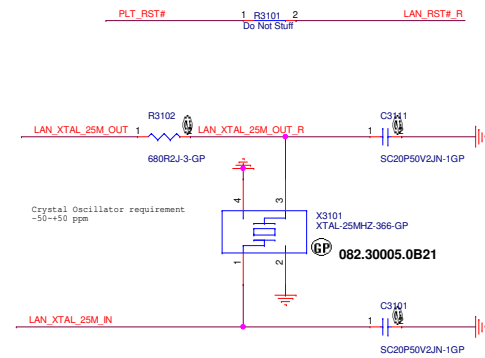
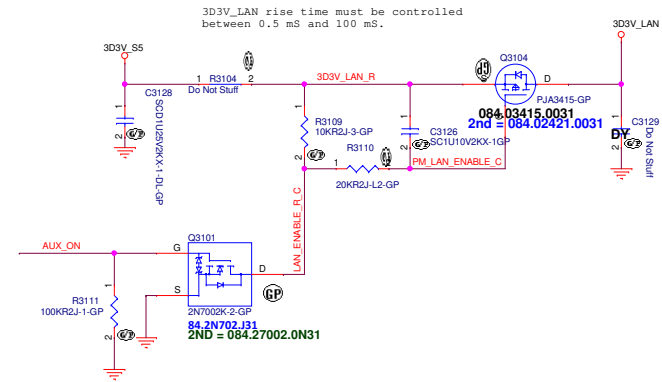
15,24 LAN_WAKE# <<<

32 LAN_MDIO_P
32 LAN_MDIO_N
32 LAN_MDIO_P
32 LAN_MDIO_N
32 LAN_MDIO_P
32 LAN_MDIO_N
32 LAN_MDIO_P
32 LAN_MDIO_N

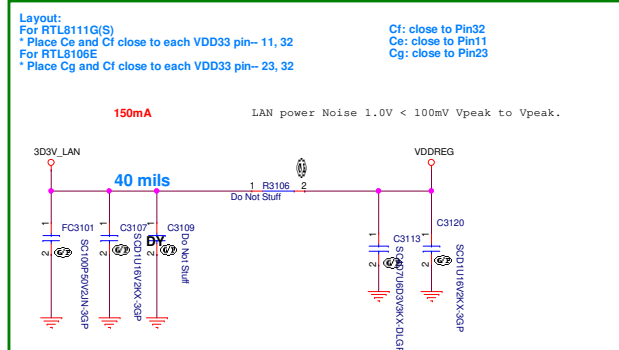
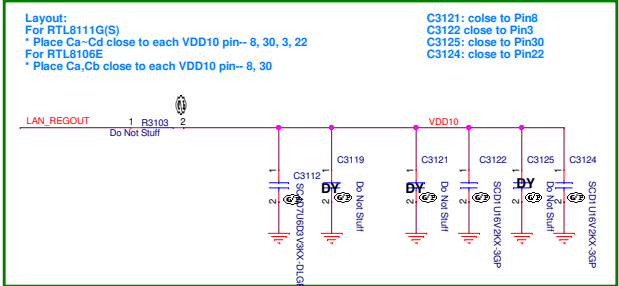
24 AUX_ON >>>



1219 BOM change to 071.8111H.0003



RTL8111HSD-CGT
071.8111H.M001
SWR mode
10/100/1000M



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Selek CFLH N17P

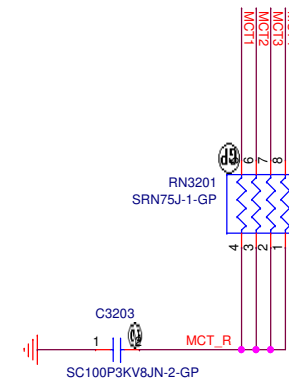
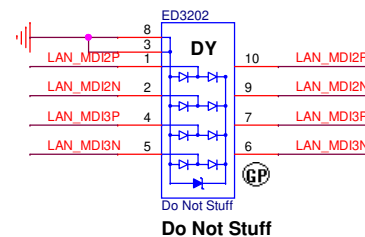
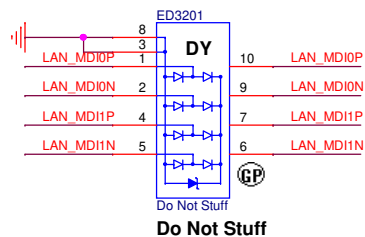
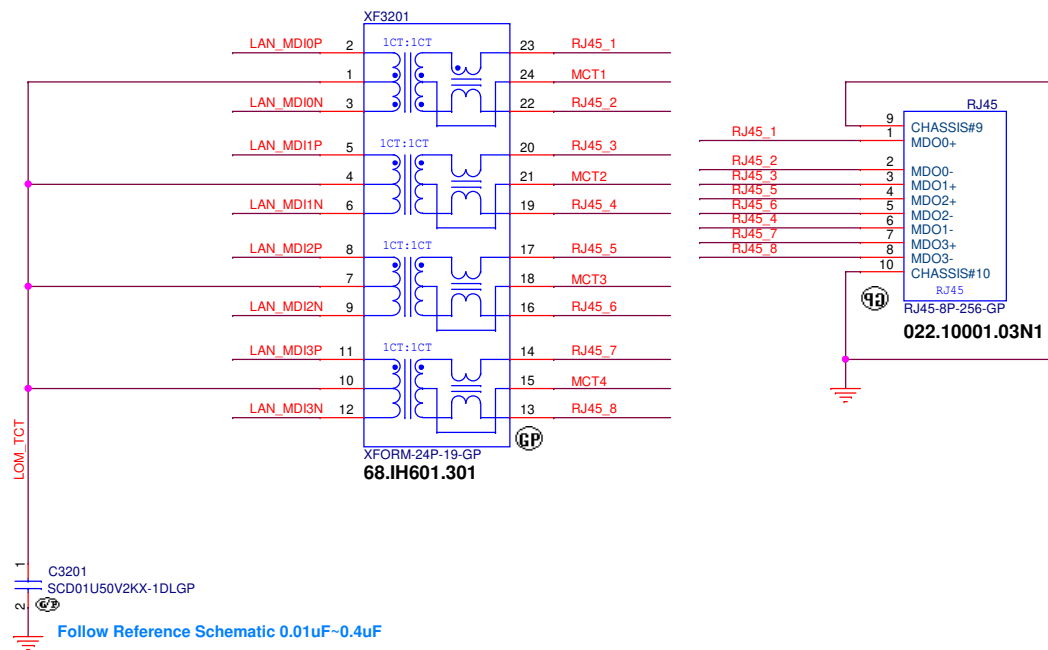
DELL Wistron Corporation
21F, 88, Sec.1, Hei Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File **LAN RTL8111H**

Size	Document Number	Rev
Custom	Selek CFL-H	A00
Date: Wednesday, April 03, 2019	Sheet 31	of 105

SSID = LAN

31 LAN_MDI0P
31 LAN_MDI0N
31 LAN_MDI1P
31 LAN_MDI1N
31 LAN_MDI2P
31 LAN_MDI2N
31 LAN_MDI3P
31 LAN_MDI3N



Selek CFLH N17P

DELL		Wistron Corporation	
		21 F, 88, Sec.1, Hsin Tai Wu Rd., Hsieh, Taipei Hsien 221, Taiwan, R.O.C.	
Title RJ45+Transformer			
Size B	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 32	of 105


SSID = Card Reader

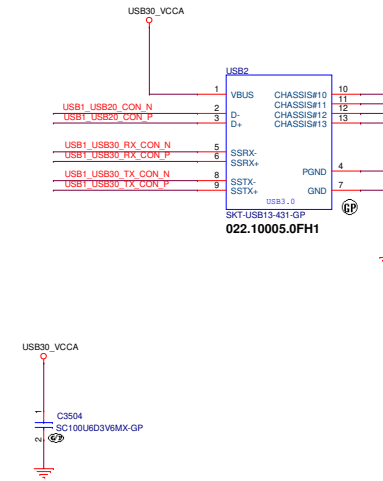
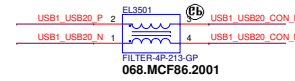
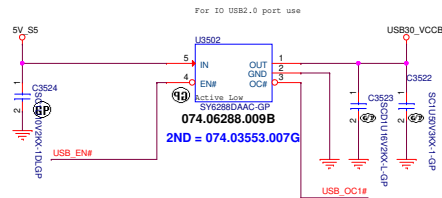
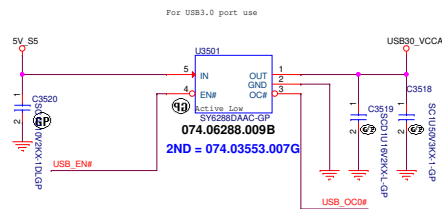
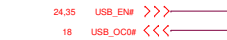
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Selek CFLH N17P

		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A2	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 33 of	105

Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A	Document Number Selek CFLH-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 34 of	105



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

Selek CFLH N17P			
		Wistron Corporation 21F, 86, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB3.0*2 CONN			
Size Custom	Document Number	Rev	
Selek CFL-H		A00	
Date:	Wednesday, April 03, 2019	Sheet	36 of 105

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2		

Selek CFLH N17P



Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wuj Rd., Hsiohih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title Charger		
Size B	Document Number Selek CFL-H	Rev A00
Date: Wednesday, April 03, 2019	Sheet 36	of 105

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Selek CFLH N17P



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title (Reserved)

Size A	Document Number Selek CFL-H	Rev A00
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Date: Wednesday, April 03, 2019	Sheet 37 of 105
---------------------------------	-----------------

SSID = USB3.0 Redrivere

USB 3.0 Re-driver Pull High / Low

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Selek CFLH N17P



Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsuehshien,
Taipei Hsien 221, Taiwan, R.O.C.

TitleUSB 3.0 Redriver

SizeA2

Document NumberSelek CFL-H

RevA00

DateWednesday, April 03, 2019Sheet36 of106

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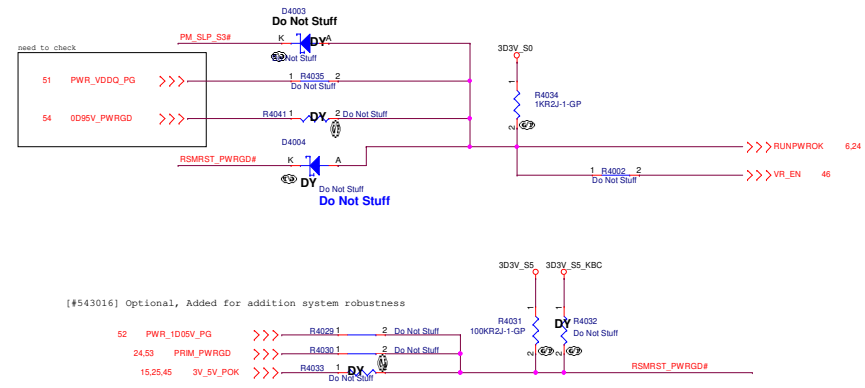
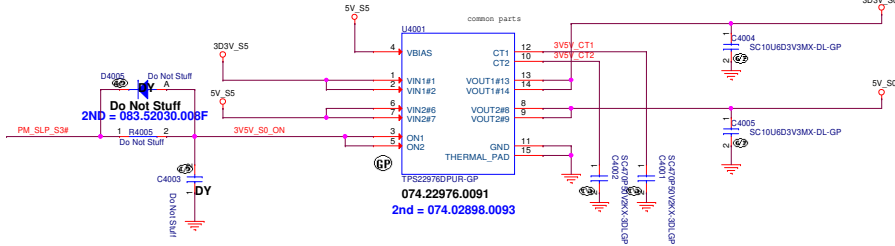
Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 39 of	105

15,27,54,57 PM_SLP_S3# >>>_____

5V_S0 Consumption	3D3V_S0 Consumption
Peak current 5A	Peak current 2.5A


5V_S5



Main Func = Power & Sequence

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Selek CFLH N17P



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Title

Connected_Standby(1/2)+DS3

Size
A3

Document Number
Selek CFL-H

Rev
A00

Date: Wednesday, April 03, 2019

Sheet 41 of 105

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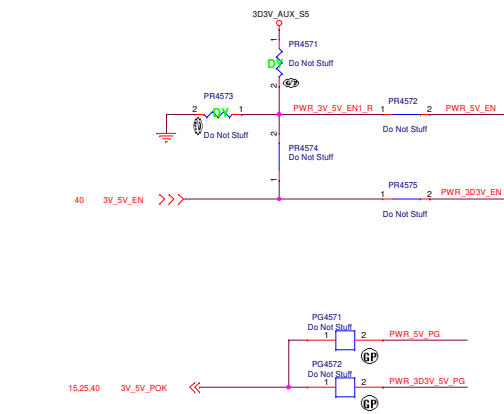
Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A	Document Number Selek CFL-H		Rev A00
Date: Wednesday, April 03, 2019		Sheet 42 of	105

		Wistron Corporation 21F, 88, Sec.3, Hsiao Tai Hsu Rd., Hsuehshih, Taipei Hsien 221, Taiwan, R.O.C.	
File			
<h1>Charger</h1>			
Size	Document Number		Rev
A3			A
<h2>Selek CFL-H</h2>			

SSID = PWR.Plane.Regulator_5V

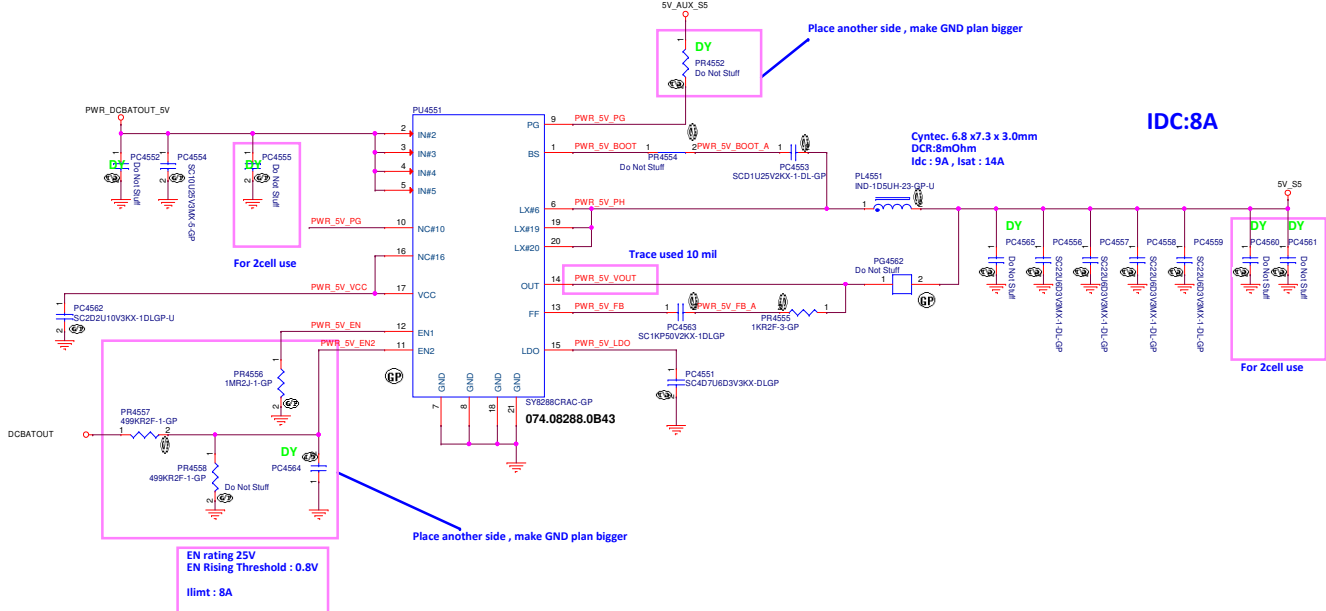
OFFPAGE-Signal



OFFPAGE-GAP



SY8288C For 5V

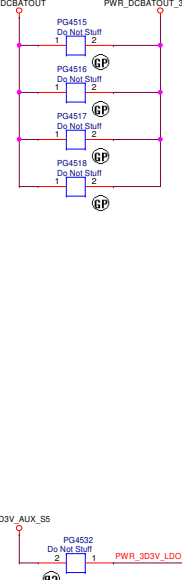


SSID = PWR.Plane.Regulator_3D3V

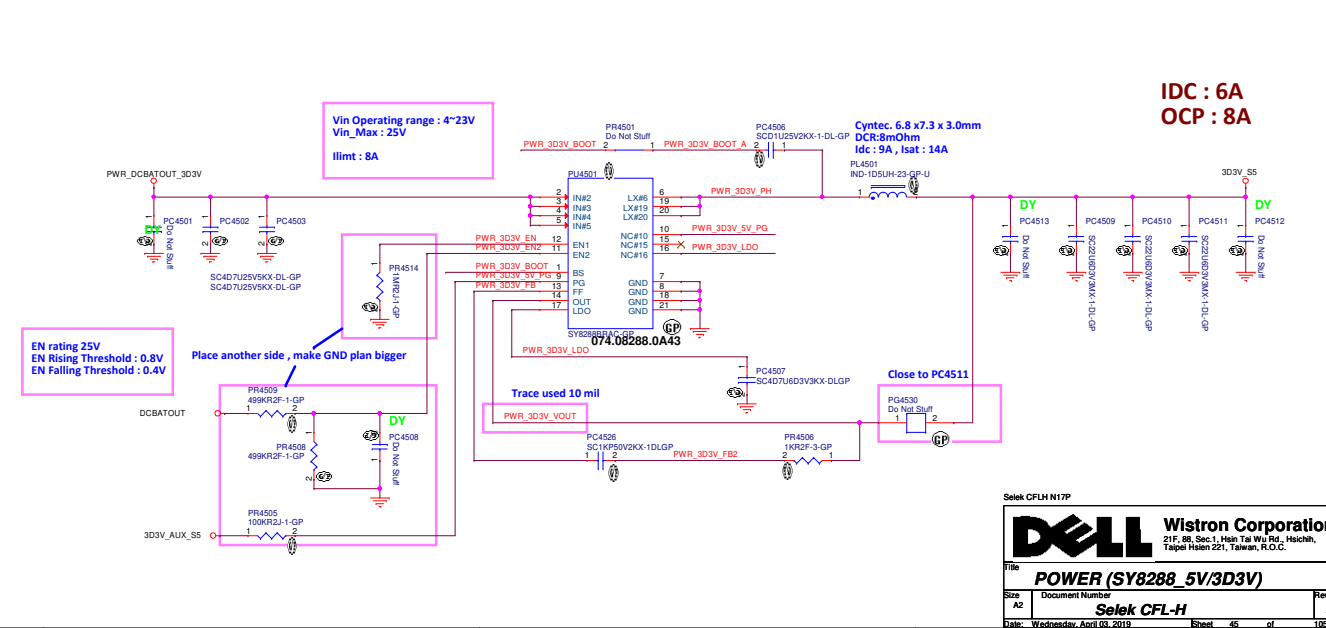
OFFPAGE-Signal



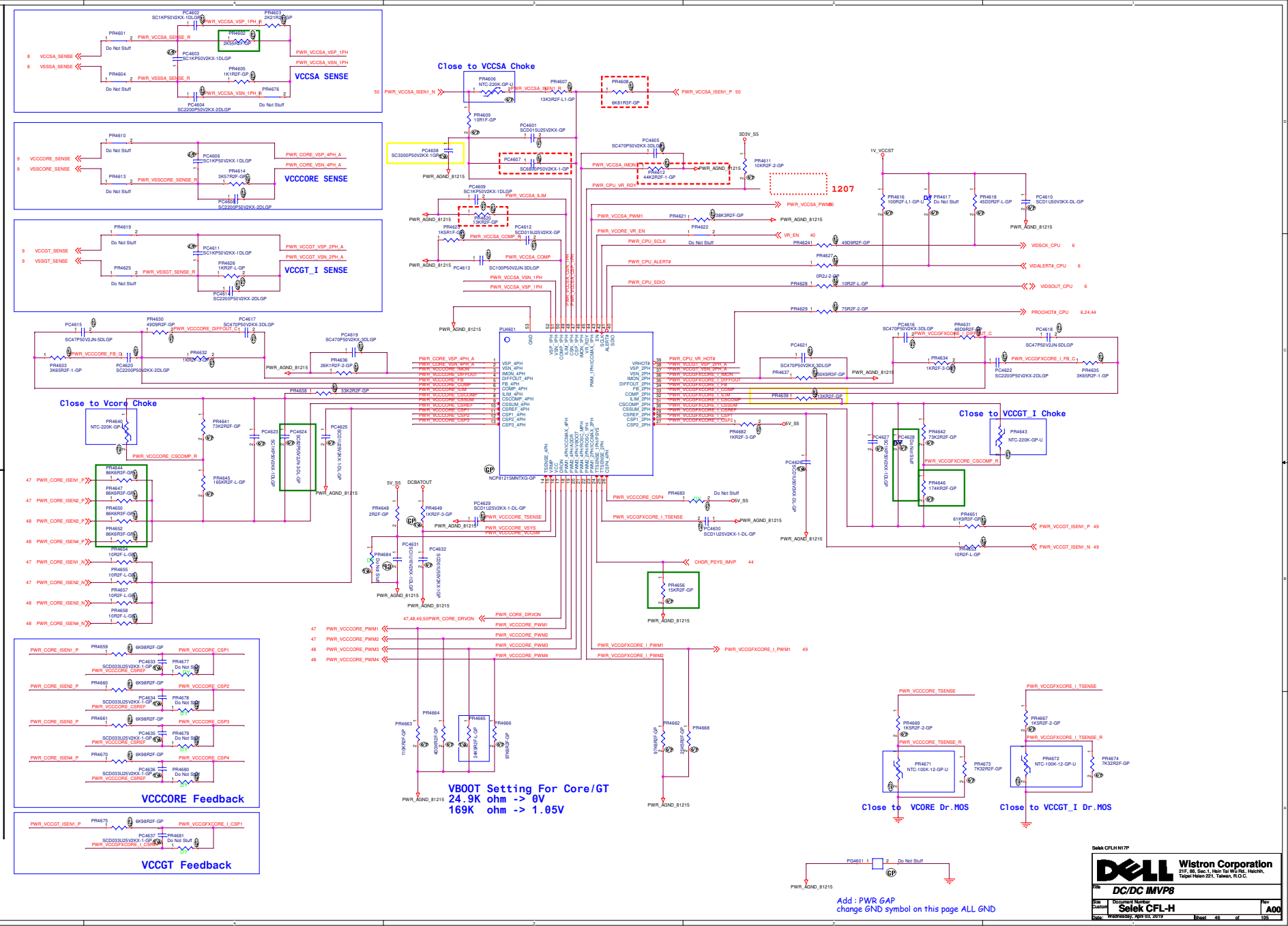
OFFPAGE-GAP



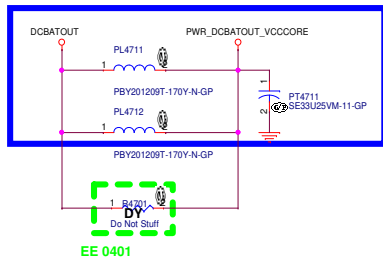
SY8286B For 3D3V



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For acousaic noise 1228



Max Current = 3.50(A)

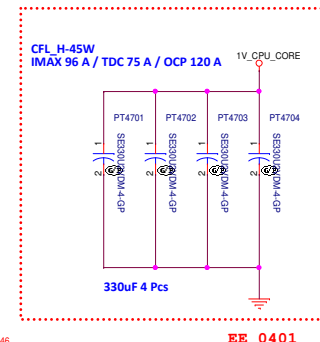
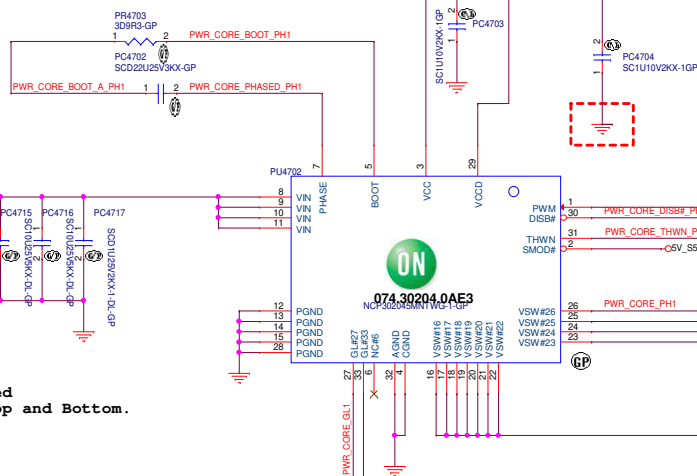
PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.



Selek CFLH N17P

DELL Wistron Corporation
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Taippei Hsien 221, Taiwan, R.O.C.

Title DC/DC VCCCPUCORE (1/2)

Size C Document Number SeleK CFL-H Rev A00
Date: Wednesday, April 03, 2019 Sheet 47 of 105

Max Current = 3.50(A)

PWR_DCBATOUT_VCCORE

MLCCs must be placed
symmetrically on Top and Bottom.

Max Current = 3.50(A)

PWR_DCBATOUT_VCCORE

MLCCs must be placed
symmetrically on Top and Bottom.

This circuit is for Hexa core.
Please refer to the table in next page.

Selek CFLH N17P

DELL Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taippei Hsien 221, Taiwan, R.O.C.

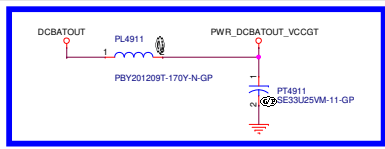
Title
DC/DC VCCCPUCORE (2/2)

Size
C Document Number
Selek CFL-H

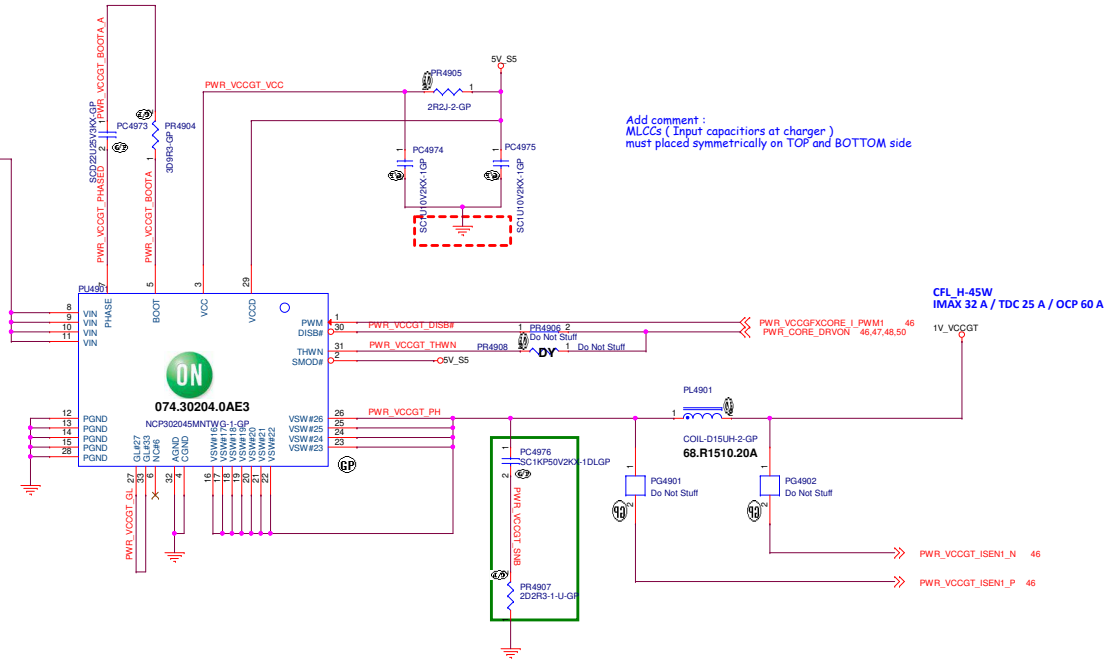
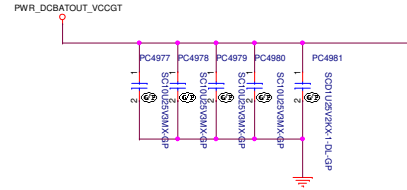
Rev
A00

Date: Wednesday, April 03, 2019

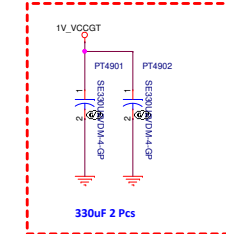
Sheet 48 of 105



For acousaic noise 1228



CFL_H-45W
IMAX 32 A / TDC 25 A / OCP 60 A

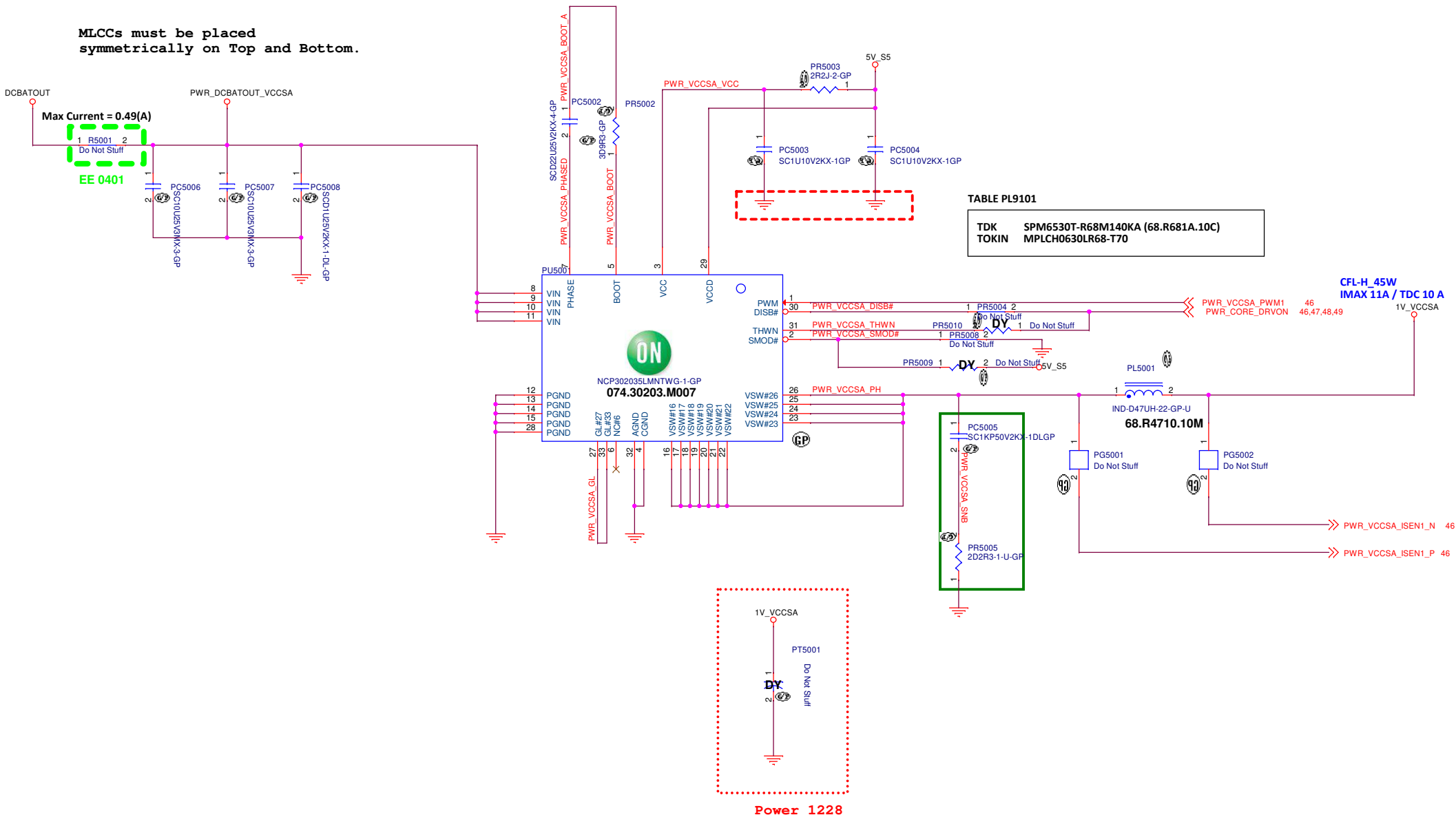


330uF 2 Pcs
Power 0401

Selek CFLH N17P

DELL		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DC/DC VCCGFXCORE_I(NCP302045)			
Size	Document Number	Rev	
Custom	Selek CFL-H	A00	
Date:	Wednesday, April 03, 2019	Sheet 49	of 105

MLCCs must be placed
symmetrically on Top and Bottom.



OFFPAGE-Signal

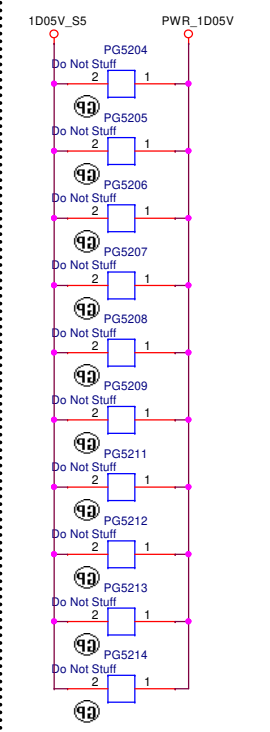
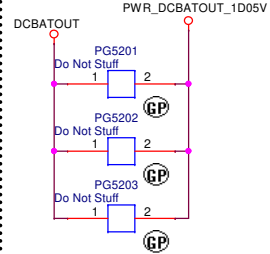
PH on EE Side

PWR_1D05V_PG

3V_5V_DSW_OK

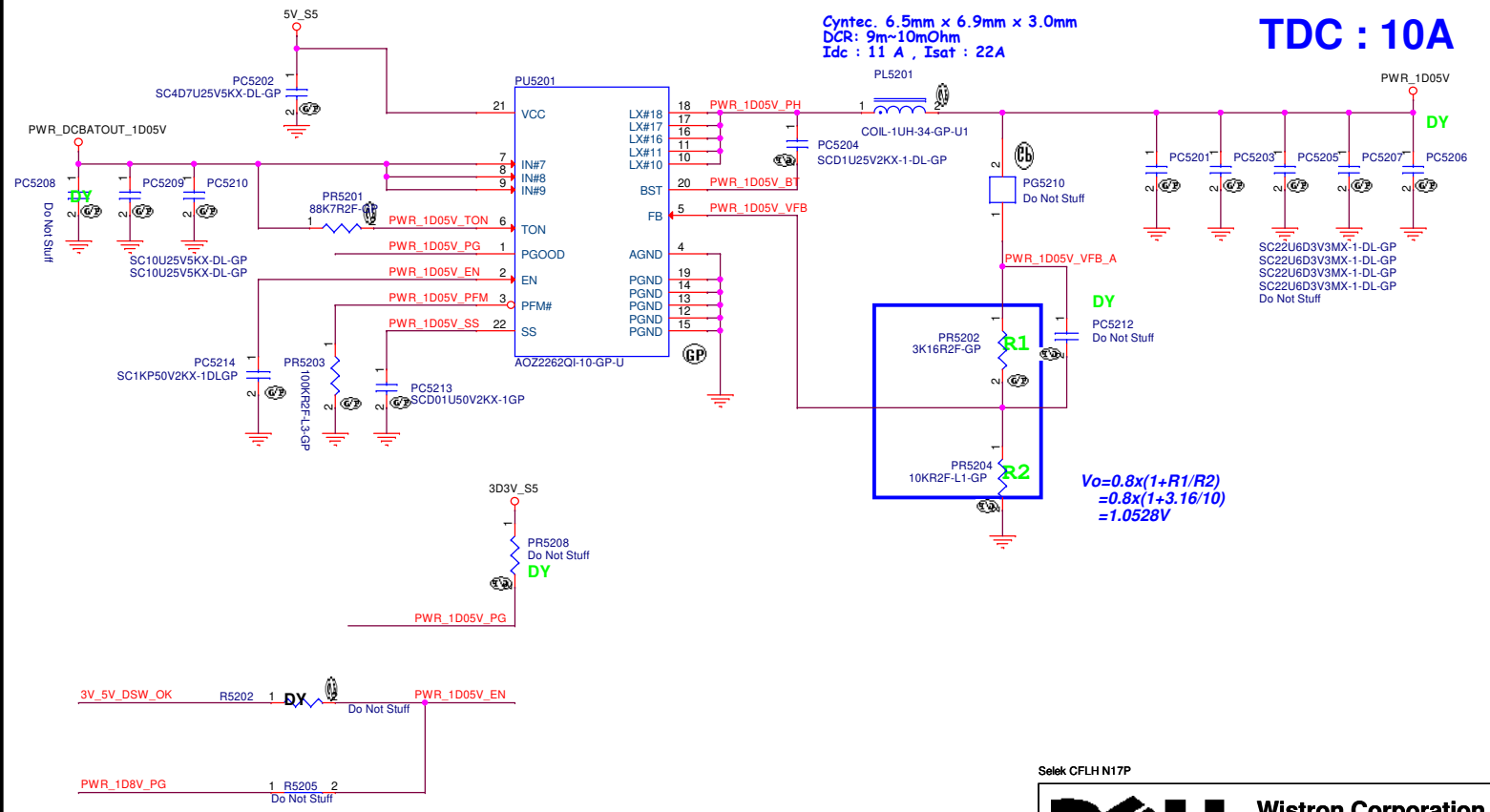
PWR_1D8V_PG

OFFPAGE-GAP



AOZ2262 For 1D05V

COM	IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
		074.02262.0043	074.02261.0A73	074.02260.0043
Chock		68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP		22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1



Cyntec. 6.5mm x 6.9mm x 3.0mm
DCR: 9m~10mOhm
Idc : 11 A , Isat : 22A

TDC : 10A

$$Vo = 0.8x(1+R1/R2) = 0.8x(1+3.16/10) = 1.0528V$$

Main Func = 1D8V

OFFPAGE

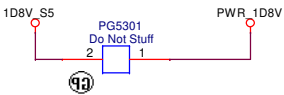
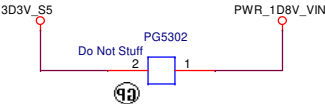
25,52 3V_5V_DSW_OK >>

PH on EE Side



52 PWR_1D8V_PG <<

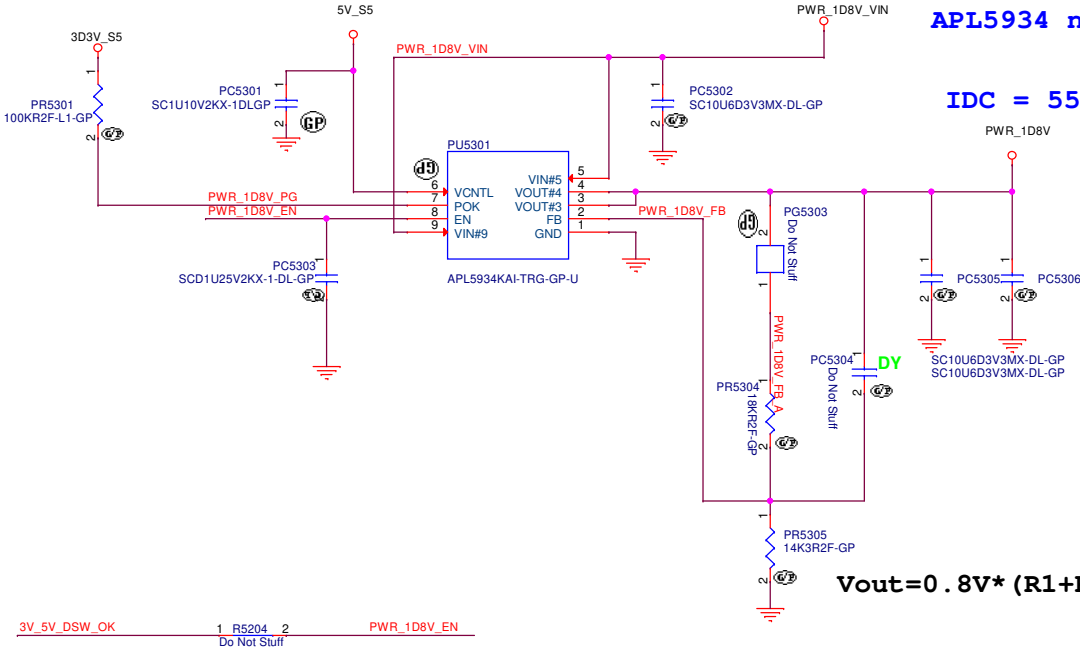
OFFPAGE_GAP



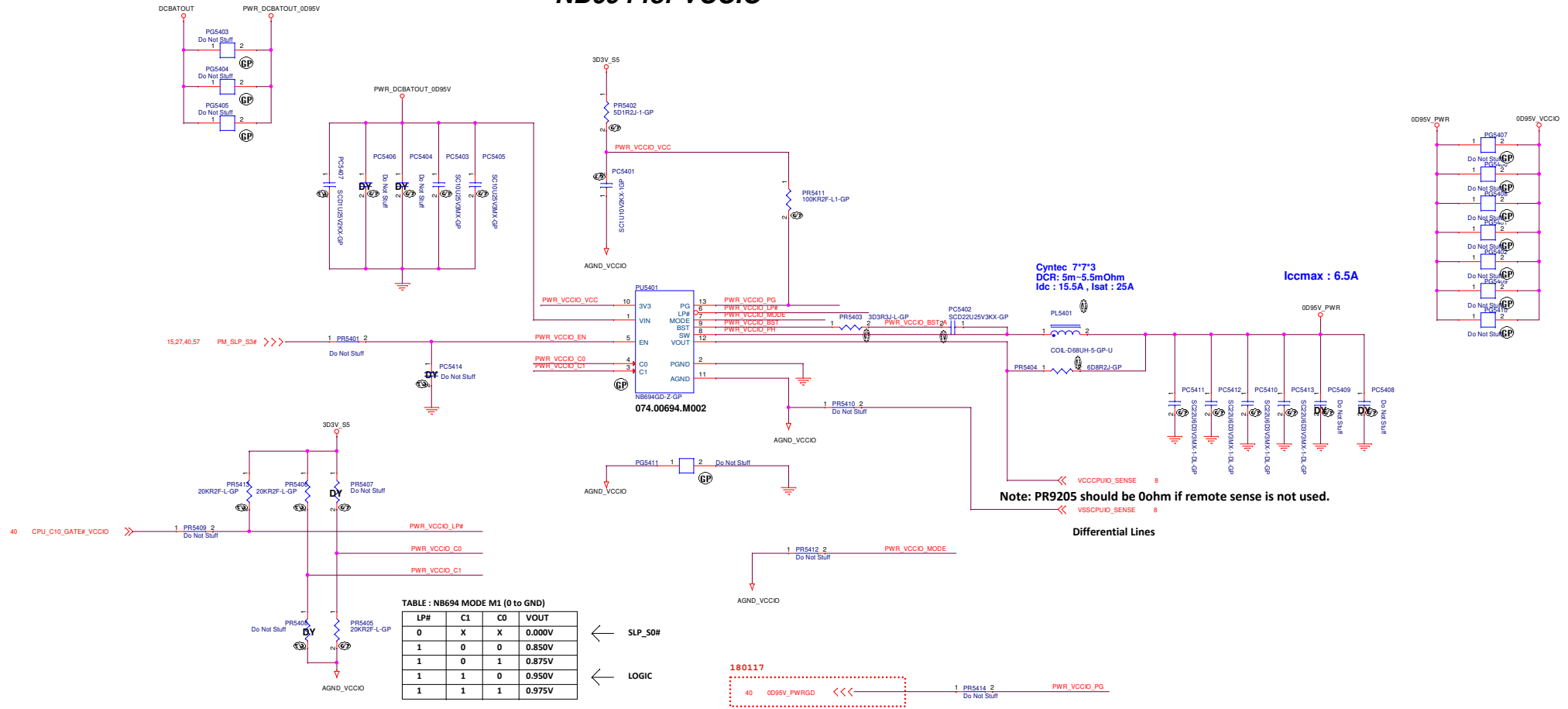
APL5934 for 1D8V

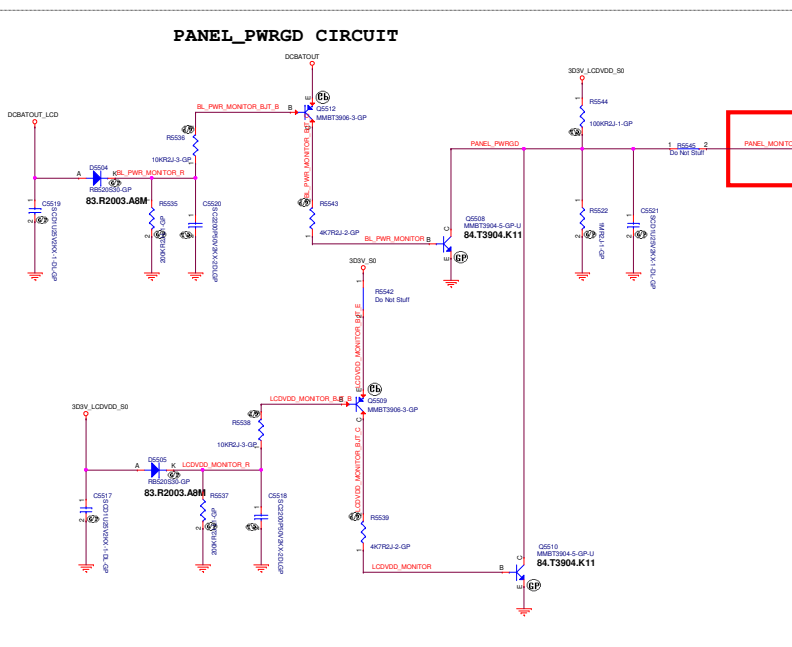
APL5934 need <1.8W

IDC = 550mA

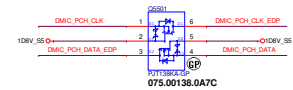


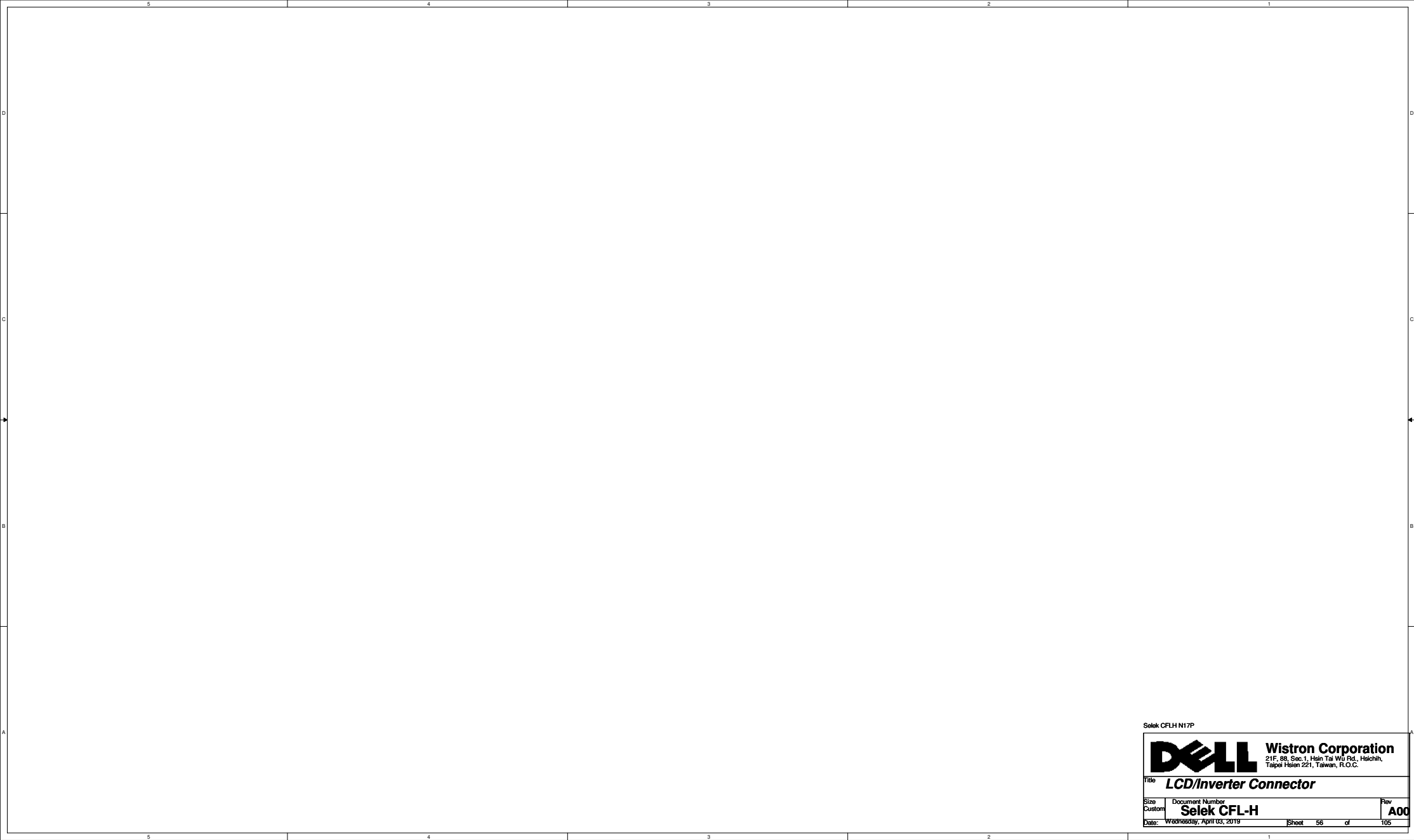
NB694 for VCCIO






3D3V_S0

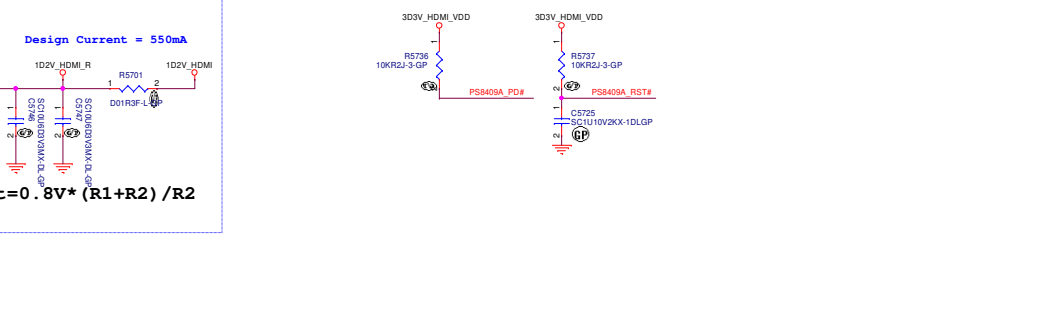
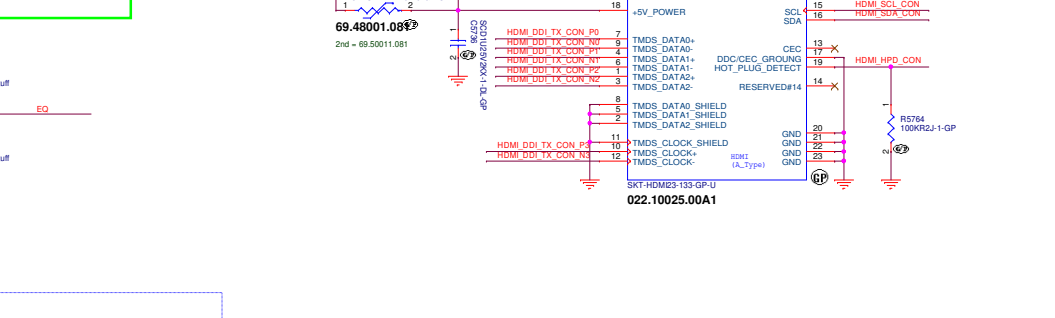
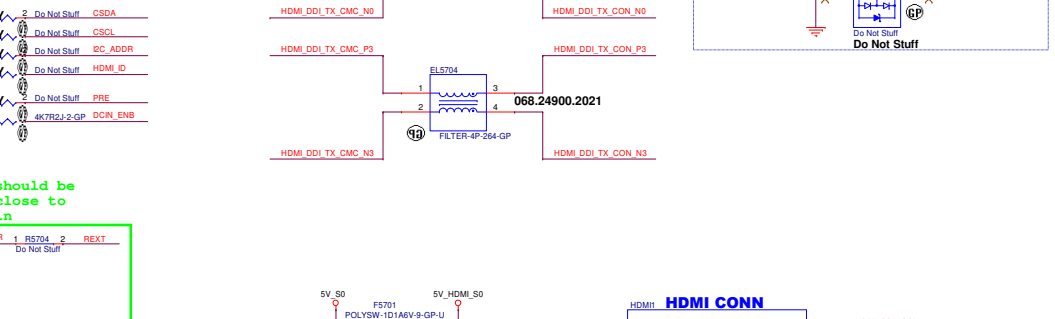
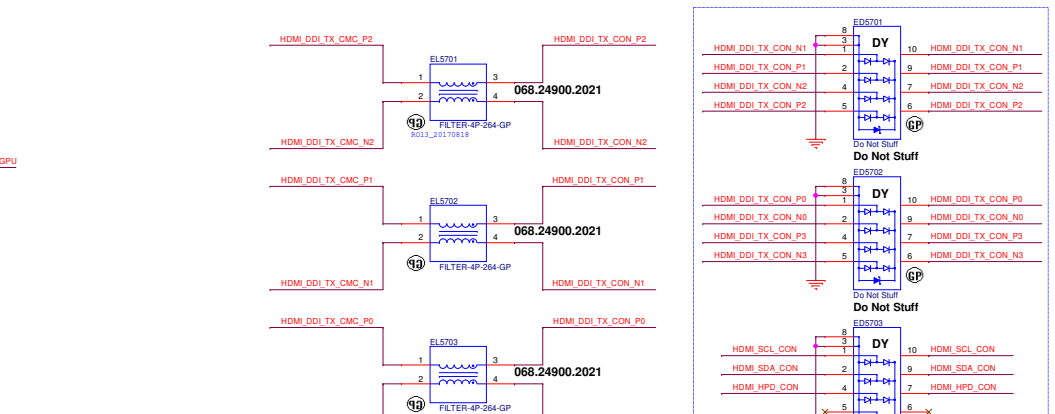
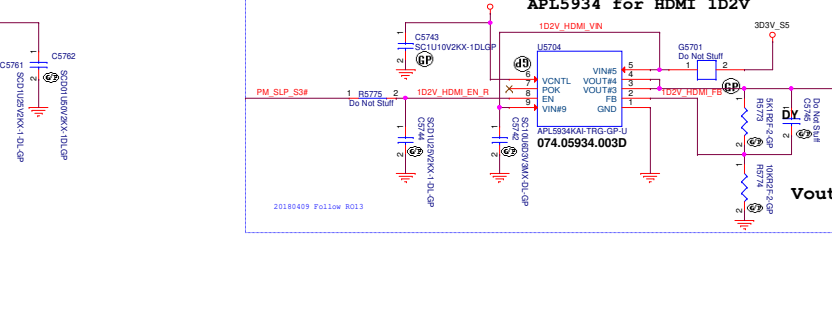
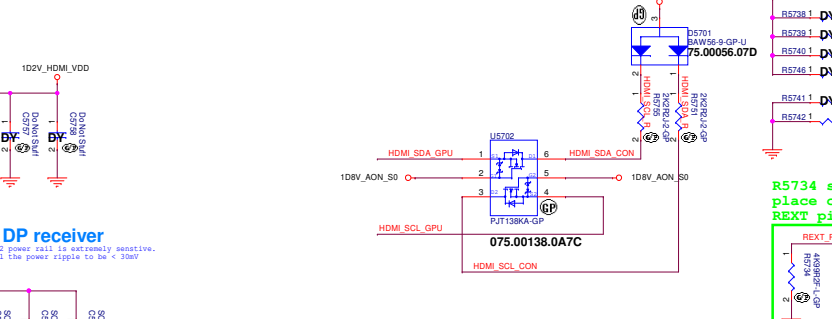
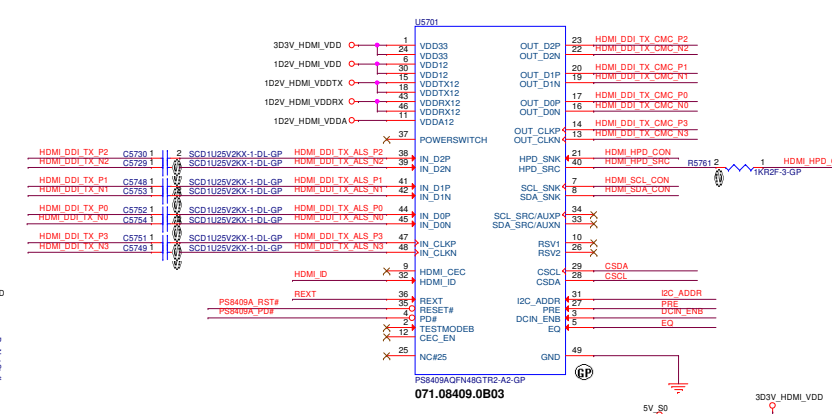
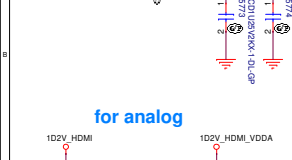
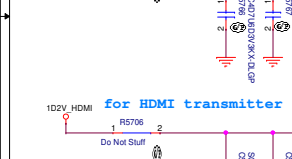
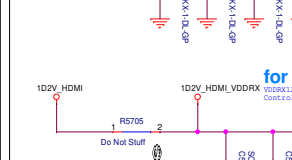
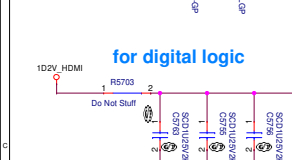
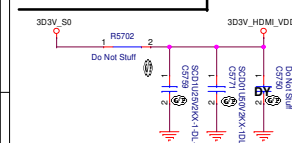
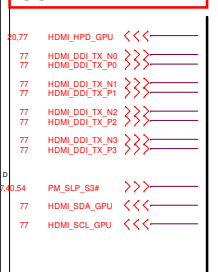




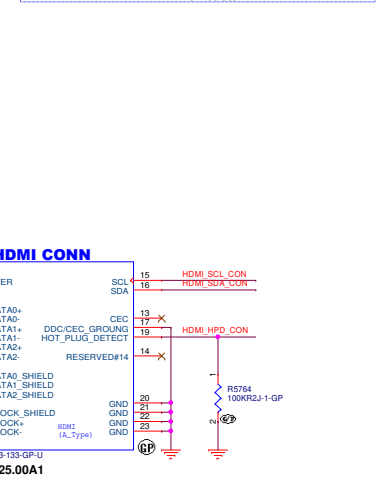
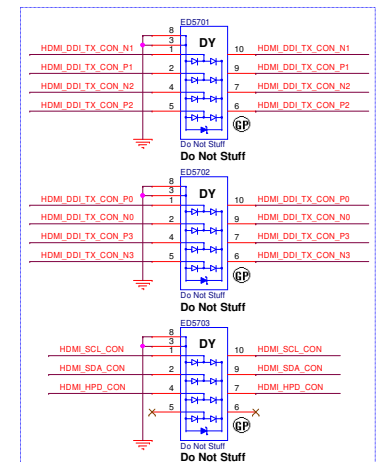
Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wü Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title LCD/Inverter Connector			
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SSID = HDMI



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Title (Reserved)			
Size A	Document Number Selek CFL-H		Rev A00
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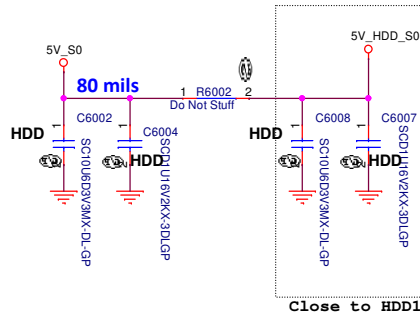
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Selek CFLH N17P

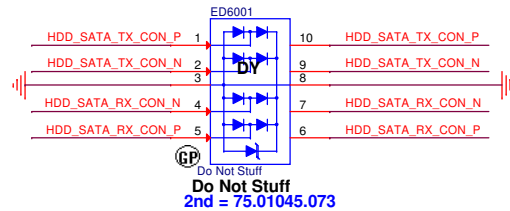
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
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Main Func = HDD

17 HDD_SATA_TX_P >>>
17 HDD_SATA_TX_N <<<
17 HDD_SATA_RX_N <<<
17 HDD_SATA_RX_P >>>
19 HDD_DEVSLP >>>
70 FFS_INT2_Q >>>
24.63 SSD_SCP# >>>



Layout Note:
Place near HDD1



SATA HDD Connector

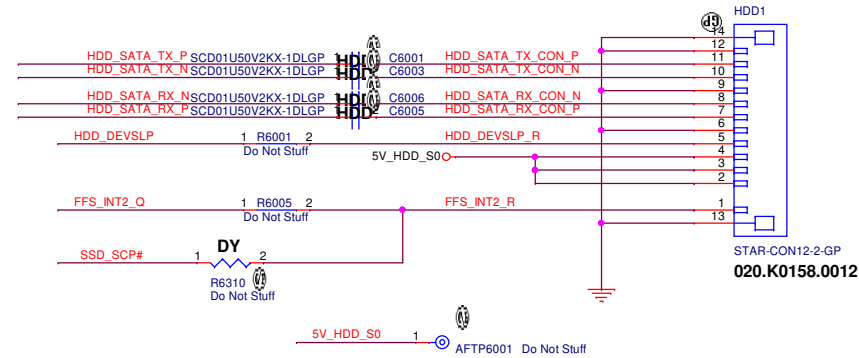


Table 16-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ¹	None ²	None ³

Notes:

- This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
- For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* lane that needs to support either PCIe* Gen2 devices or PCIe* Gen3 devices, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Use a non-interleaved breakout to isolate Tx and Rx.

SSID = Wireless

Selek CFLH N17P



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Title (Reserved)WWAN

Size A	Document Number Selek CFL-H	Rev A00
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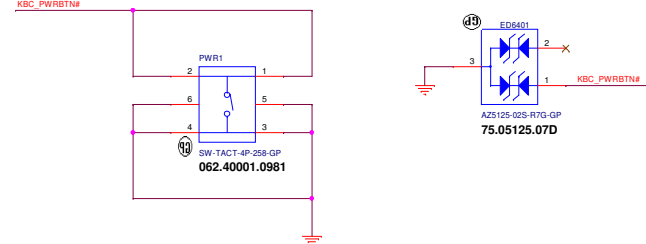
Mini Card Connector (NGFF m-SATA)



SSID = User.Interface

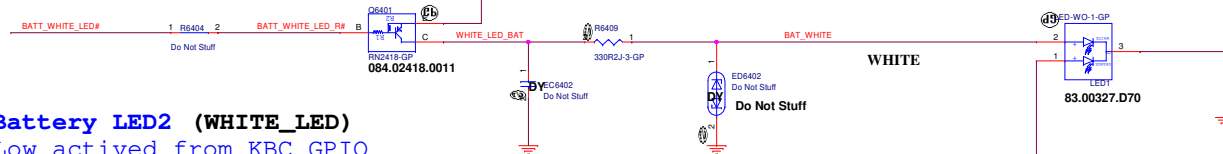
Power button

NONE FINGER PRINT 才會上件



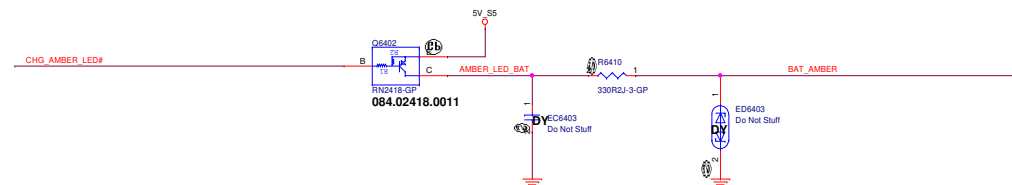
Battery LED1 (AMBER_LED)

Low activated from KBC GPIO

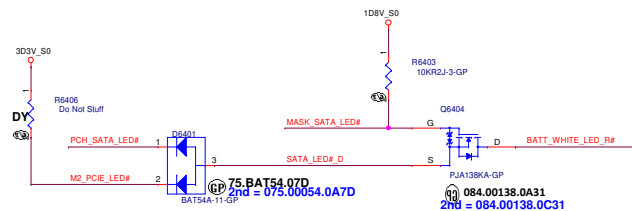


Battery LED2 (WHITE_LED)

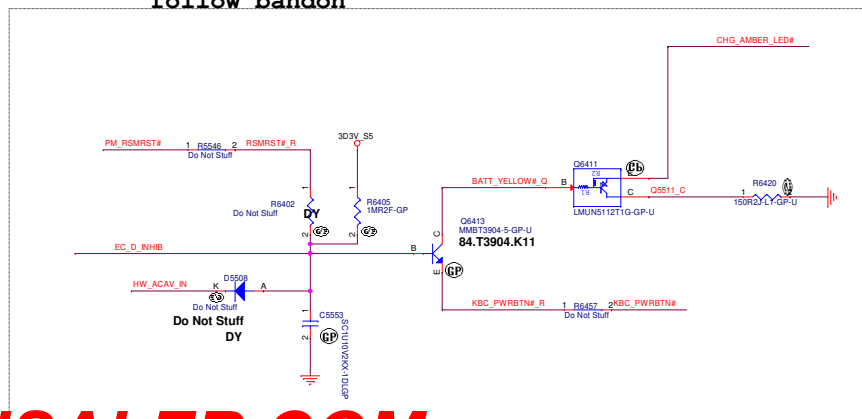
Low activated from KBC GPIO



SATA LED



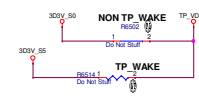
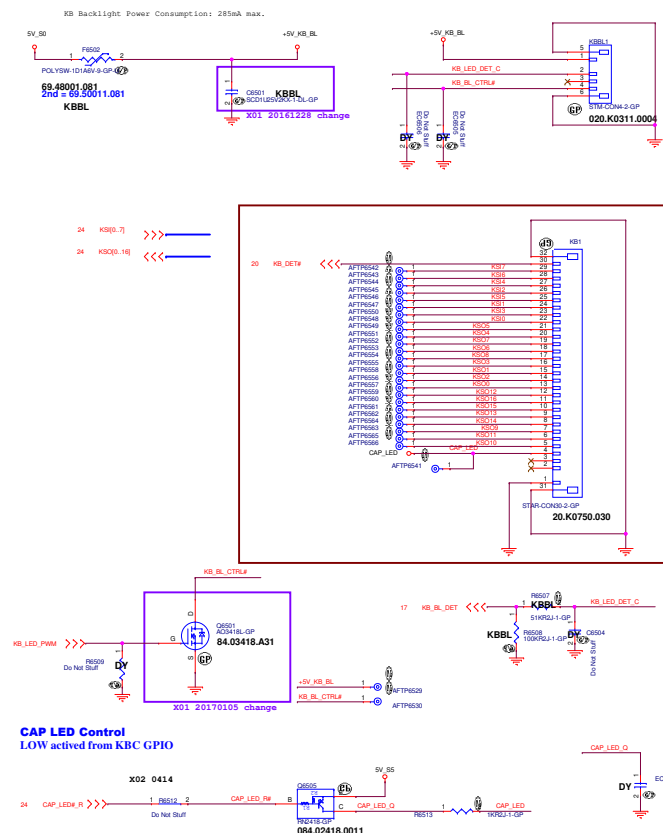
M-BIST for G10 (Proposed schematic)
follow bandon



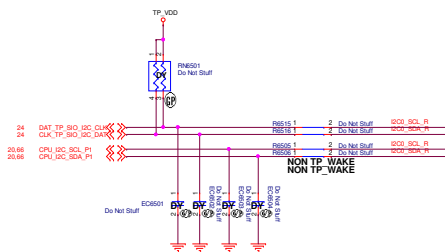
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Main Func = TPAD

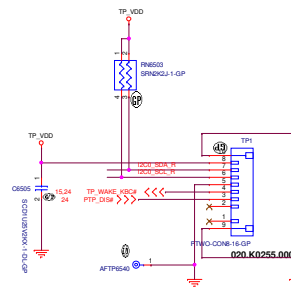


GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)



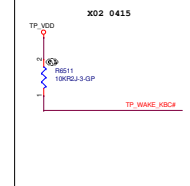
EC I2C

I2C



Change pindefine DWT1 0210 1330

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)

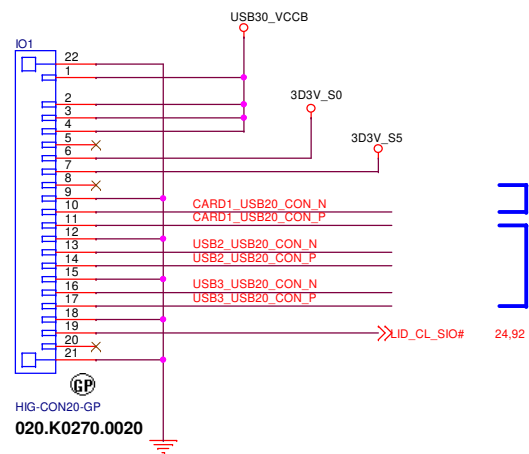
Module Pin	Signal	Target Pin
TP_VDD	1	AFTP65
I2C0_SCL_R	1	AFTP65
I2C0_SDA_R	1	AFTP65
TP_WARE_KBCIF	1	AFTP65
TP_PCSIF	1	AFTP65

18 USB3_USB20_P
18 USB3_USB20_N
18 USB2_USB20_P
18 USB2_USB20_N

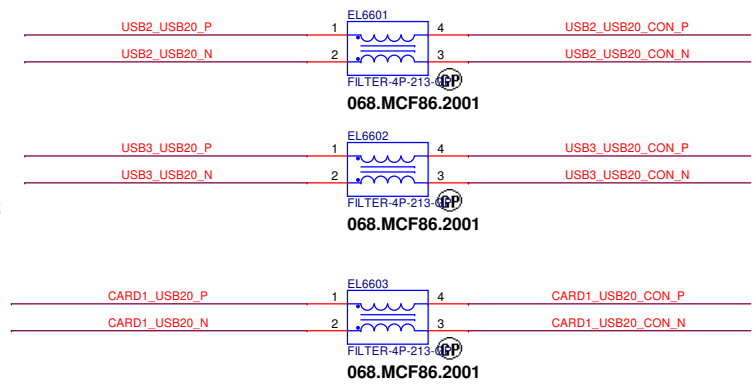
18 CARD1_USB20_N
18 CARD1_USB20_P

20.65 CPU_I2C_SCL_P1
20.65 CPU_I2C_SDA_P1

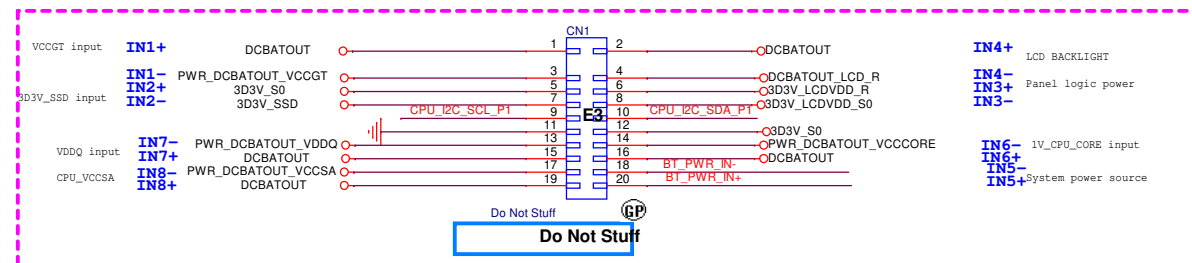
44 BT_PWR_IN-
44 BT_PWR_IN+



Cardreader
USB 2.0 Gen1 *2



E3 reserve



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Title **IO Board Connector**

Size A3 Document Number **Selek CFL-H** Rev **A00**

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Main Func = Hall Sensor

Selek CFLH N17P



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Title **Hall Sensor**

Size
A

Document Number

Selek CFL-H

Rev

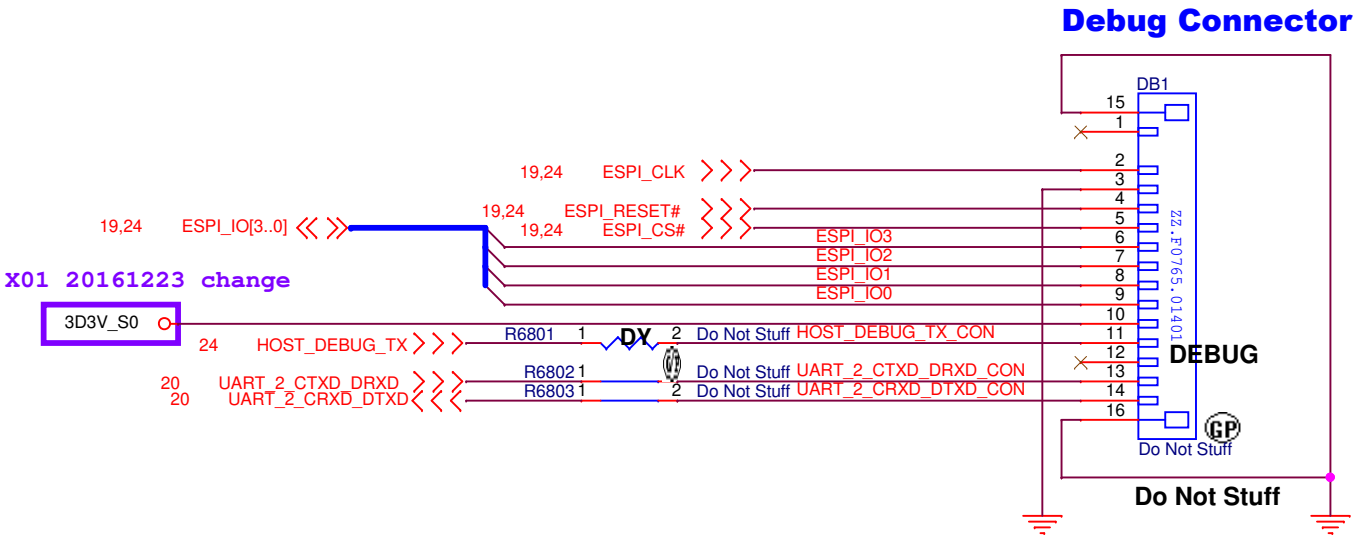
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Main Func = Debug



Selek CFLH N17P

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Dubug connector			
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Selek CFLH N17P



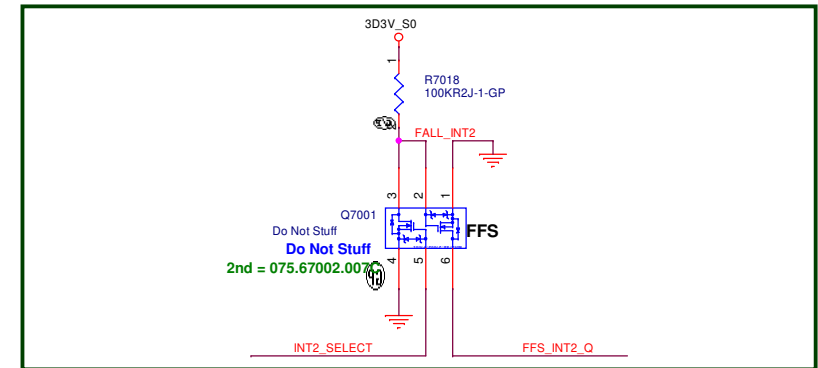
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

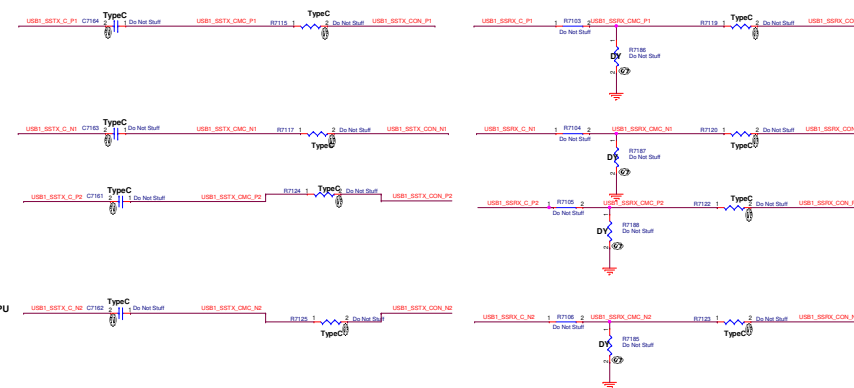
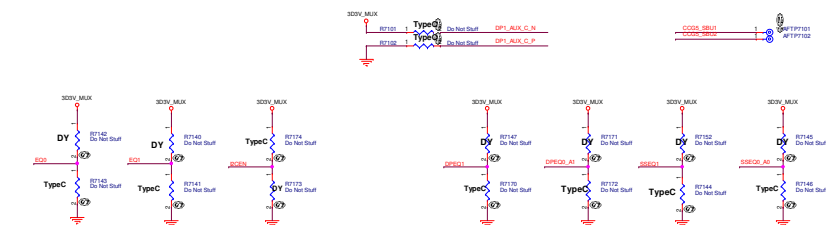
Title **Reserved**

Size A4	Document Number Selek CFLH-H	Rev A00
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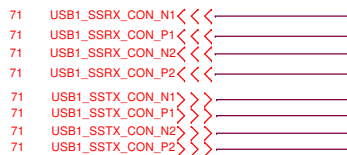
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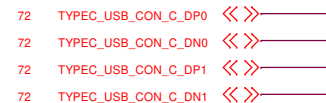




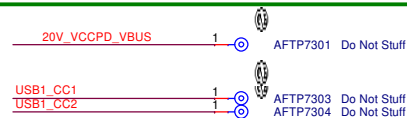
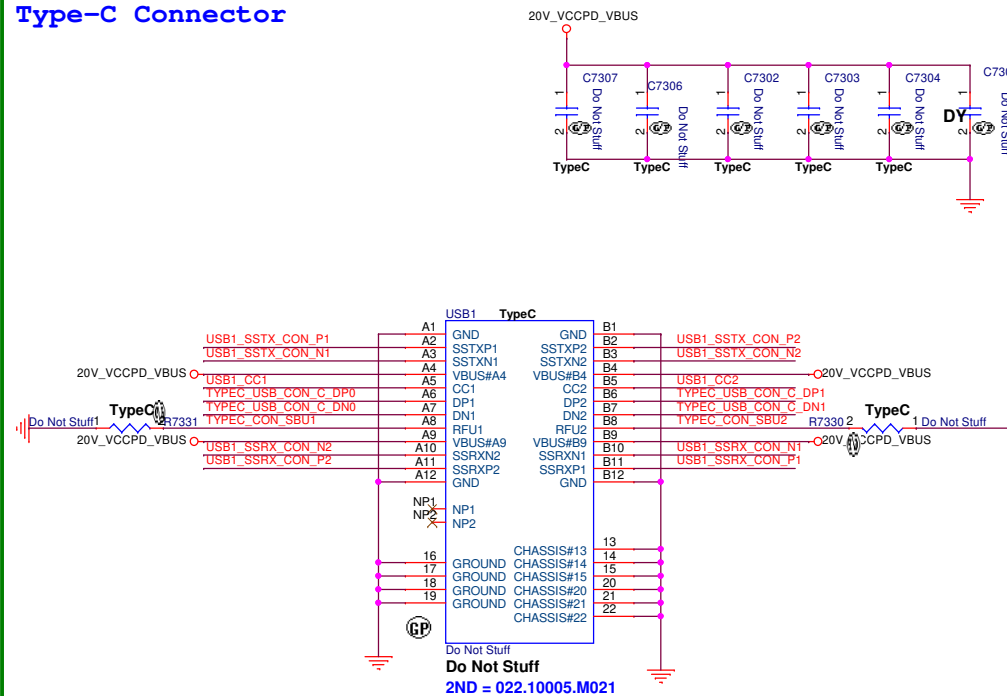
Main Func = TYPEC CONNECTOR



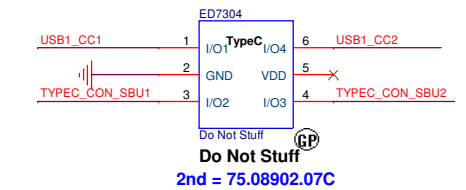
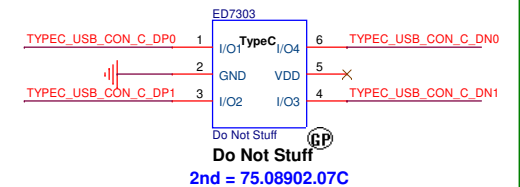
From USB2.0/ I2C Mux



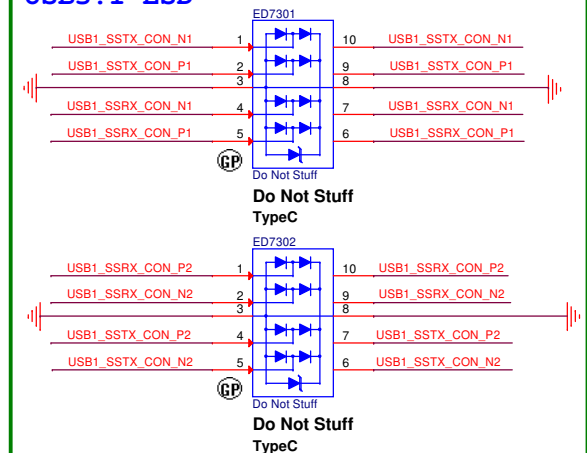
Type-C Connector



EMI



USB3.1 ESD

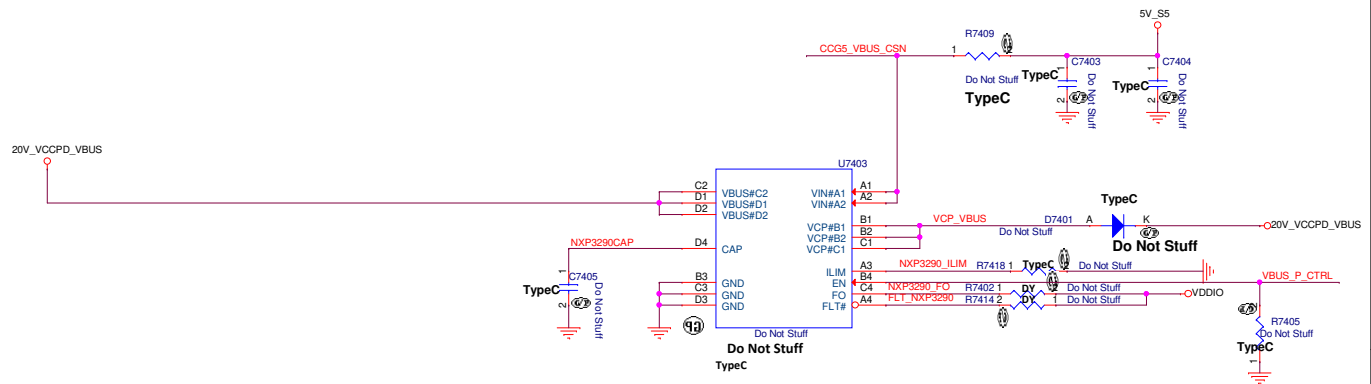


Main Func = LPS

72 VBUS_P_CTRL >>>—

72 NXP3290_FO <<<—

72 CCG5_VBUS_CSN <<<—



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Title

LPS

Size	Custom
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Selek CFL-H

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Selek CFLH N17P

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Title (Reserved)Thunderbolt (5/5)			
Size A	Document Number Selek CFL-H		Rev A00
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• PEX_HVDD and PEX_PLL_HVDD rails must be shared with 1V8_AON for GC6 2.1

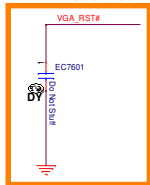
GPU	Capacitor Type	Footprint	N18	N17	Location
PEX_DVDD Supply Rail					
GB4C-128, GB4D-128	1.0 μ F	X65	0402	0201W	0 Under GPU
	0.47 μ F	X65	0201W	0201W	0 Under GPU
	4.7 μ F	X65	0603	0603	0 2 Near GPU
	4.7 μ F	X65	0603	0603	0 Under GPU
	10 μ F	X5R	0805	0805	0 2 Midway between GPU and power supply
	10 μ F	X65	0805	0805	3 0 Near GPU
	22 μ F	X5R	0805	0805	0 1 Midway between GPU and power supply
	22 μ F	X65	0805	0805	2 0 Near GPU

PEX_HVDD Supply Rail	GB4C-128, GB4D-128	1.0 μ F	X65	0402	0201W	0	4	Under GPU
		0.47 μ F	X65	0201W	0201W	13	0	Under GPU
		4.7 μ F	X65	0603	0603	0	2	Near GPU
		4.7 μ F	X65	0603	0603	3	0	Under GPU
		10 μ F	X5R	0805	0805	0	2	Midway between GPU and power supply
		10 μ F	X65	0805	0805	3	0	Near GPU
		22 μ F	X5R	0805	0805	0	1	Midway between GPU and power supply
		22 μ F	X65	0805	0805	2	0	Near GPU

Note:

1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

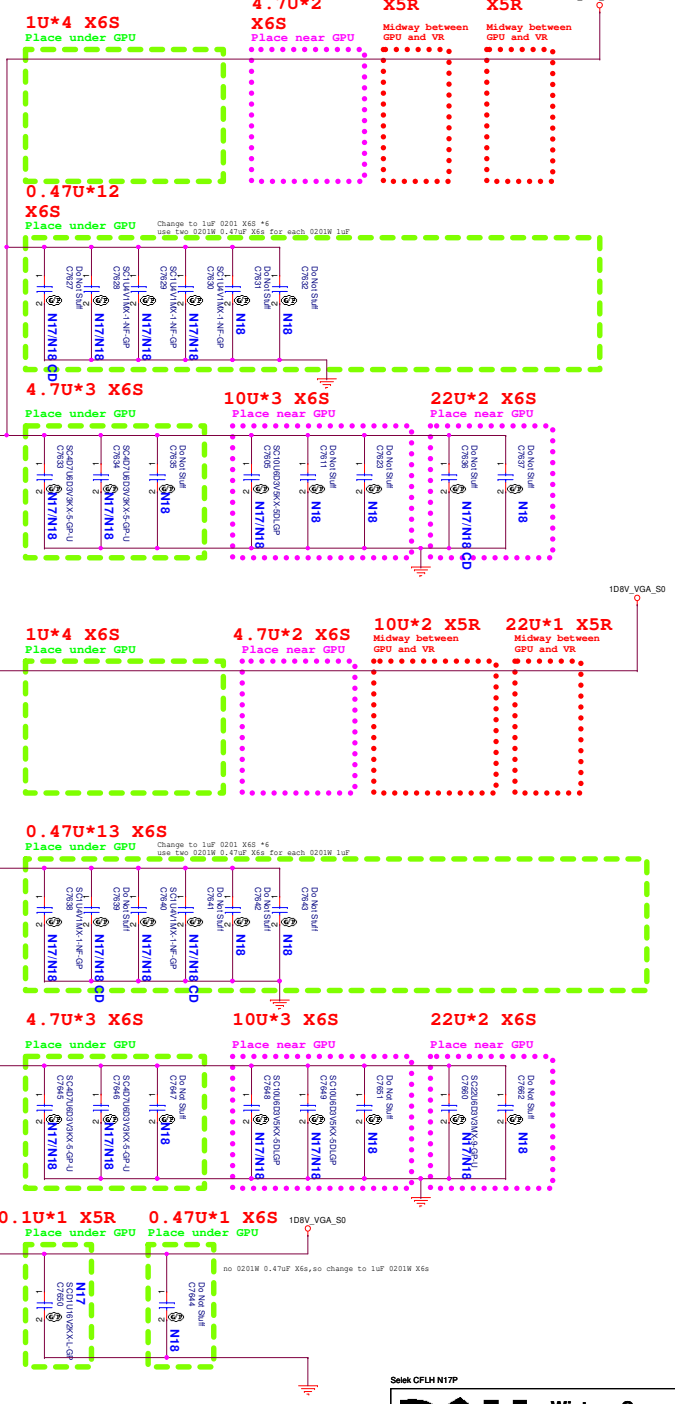
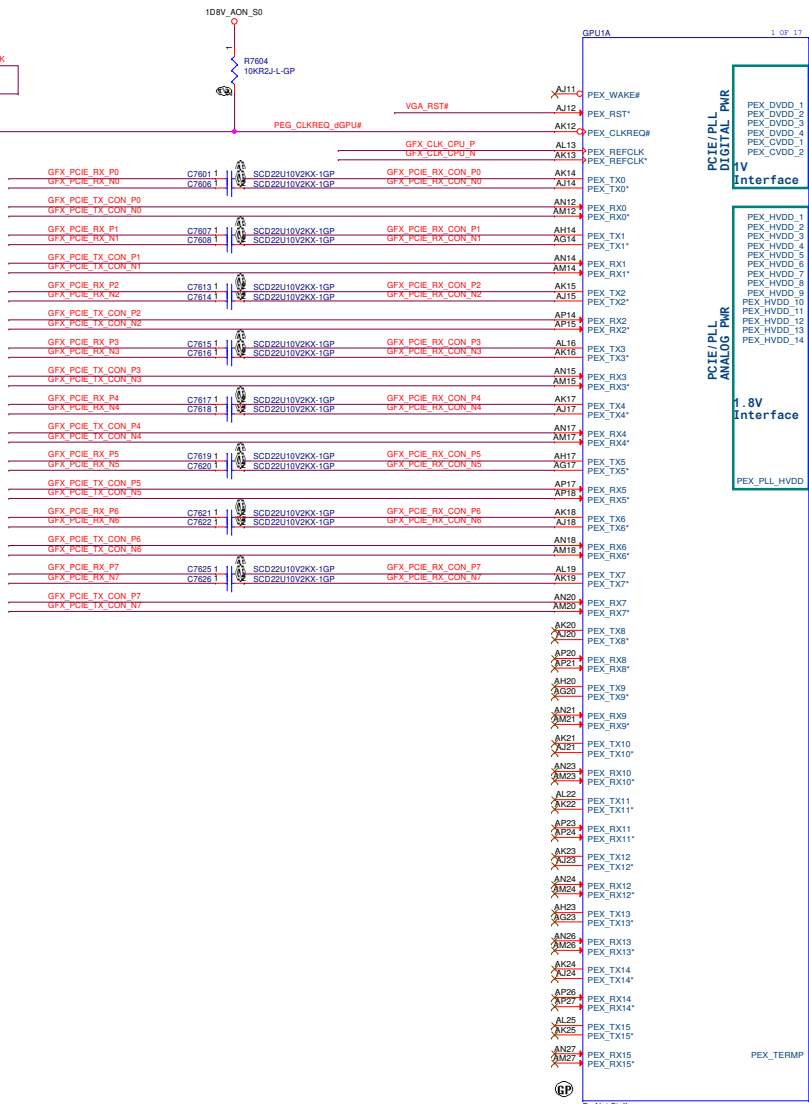
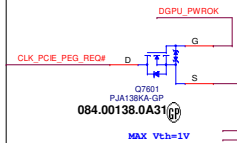
EMI Reserved

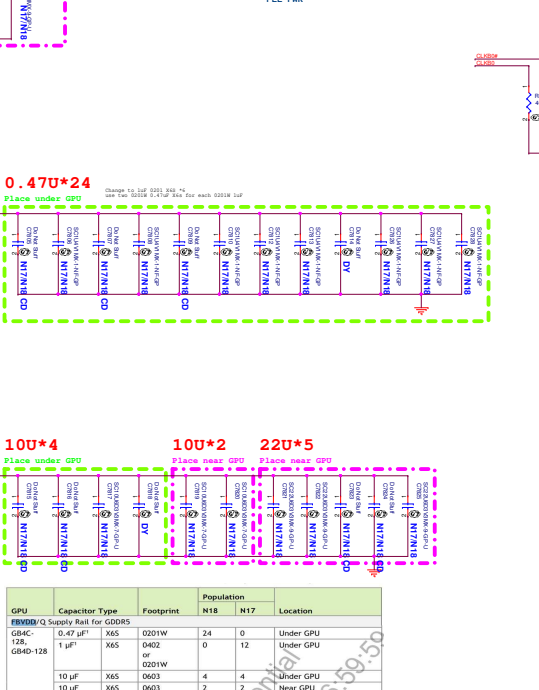
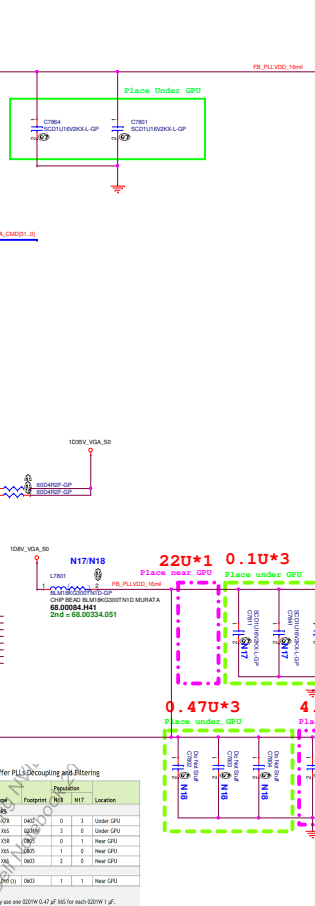
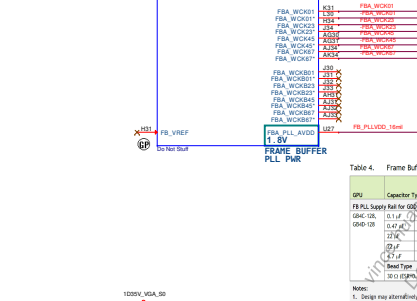
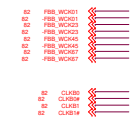


15,24,86 DGPU_PWROK
16 CLK_PCIE_PEG_REQ#
79 VGA_RST#
16 GFX_CLK_CPU_P
16 GFX_CLK_CPU_N

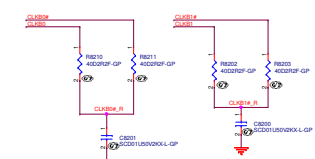
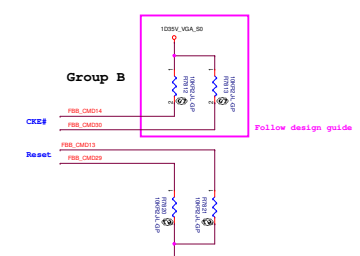
3 GFX_PCIE_RX_P7
3 GFX_PCIE_RX_N7
3 GFX_PCIE_RX_P8
3 GFX_PCIE_RX_N8
3 GFX_PCIE_RX_P9
3 GFX_PCIE_RX_N9
3 GFX_PCIE_RX_P10
3 GFX_PCIE_RX_N10
3 GFX_PCIE_RX_P11
3 GFX_PCIE_RX_N11
3 GFX_PCIE_RX_P12
3 GFX_PCIE_RX_N12
3 GFX_PCIE_RX_P13
3 GFX_PCIE_RX_N13
3 GFX_PCIE_RX_P14
3 GFX_PCIE_RX_N14
3 GFX_PCIE_RX_P15
3 GFX_PCIE_RX_N15
3 GFX_PCIE_RX_P16
3 GFX_PCIE_RX_N16
3 GFX_PCIE_RX_P17
3 GFX_PCIE_RX_N17

3 GFX_PCIE_TX_CON_P7
3 GFX_PCIE_TX_CON_N7
3 GFX_PCIE_TX_CON_P8
3 GFX_PCIE_TX_CON_N8
3 GFX_PCIE_TX_CON_P9
3 GFX_PCIE_TX_CON_N9
3 GFX_PCIE_TX_CON_P10
3 GFX_PCIE_TX_CON_N10
3 GFX_PCIE_TX_CON_P11
3 GFX_PCIE_TX_CON_N11
3 GFX_PCIE_TX_CON_P12
3 GFX_PCIE_TX_CON_N12
3 GFX_PCIE_TX_CON_P13
3 GFX_PCIE_TX_CON_N13
3 GFX_PCIE_TX_CON_P14
3 GFX_PCIE_TX_CON_N14
3 GFX_PCIE_TX_CON_P15
3 GFX_PCIE_TX_CON_N15
3 GFX_PCIE_TX_CON_P16
3 GFX_PCIE_TX_CON_N16
3 GFX_PCIE_TX_CON_P17
3 GFX_PCIE_TX_CON_N17





FBCLK Termination place on VRAM side



GPU	Capacitor Type	Footprint	Population N/B	NIT	Location	
FE PLL Supply Rail for G005						
G042-126	0.1 μ F	X58	D432	0	3	Under GPU
G042-126	0.47 μ F	X85	Q0305	3	0	Under GPU
	22 μ F	X58	D0305	0	1	Near GPU
	22 μ F	X85	D0305	1	0	Near GPU
	4.7 μ F	X85	D0321	2	0	Near GPU
Bond Type						
	30 (C) (ESD/ESD2)	C1	D0321	1	1	Near GPU

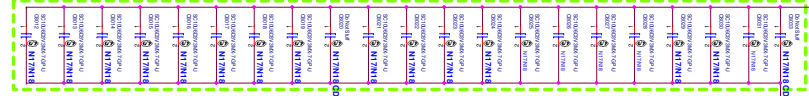
Notes:

1. Design may alternatively use one 0201W 0.47 μ F X85 for each 0201W 1 μ F.

GPU	Capacitor Type	Footprint	Population		Location
			N18	N17	
VB000/Q Supply Rail for GD0A5			24	0	Under GPU
GB4-128,	0.47 μ F X65	0201W	0	12	Under GPU
GB4-128	1 μ F ¹ X65	0402 or 0201W	0	0	Under GPU
	10 μ F X65	0603	4	4	Under GPU
	10 μ F X65	0603	2	2	Near GPU
	22 μ F X65	0603	5	5	Near GPU

Notes:

10U*21
Place under GPU



10U*13
Place under GPU



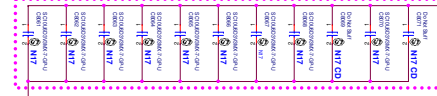
1U*13
Place under GPU



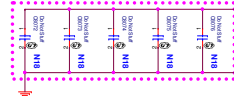
0.47U*26
Place under GPU



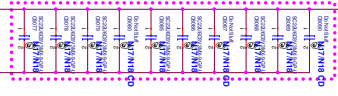
10U*11
Place near GPU



22U*5
Place near GPU



22U*10
Place near GPU



330U*1 4.7U*2
Place near GPU

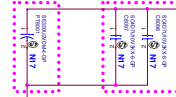


Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
NVVDD Supply Net						
GB4C-128, GB4D-128	10 μ F	X65	0603	34	21	Under GPU
	1 μ F ¹	X65	0402 or 0201W	0	13	Under GPU
	0.47 μ F ¹	X65	0402 or 0201W	26	0	Under GPU
	10 μ F	X65	0603	0	11	Near GPU
	22 μ F	X65	0805	15	10	Near GPU
	4.7 μ F	X65	0603	0	2	Near GPU
	330 μ F	POS	7343	0	1	Near GPU

Note:

1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

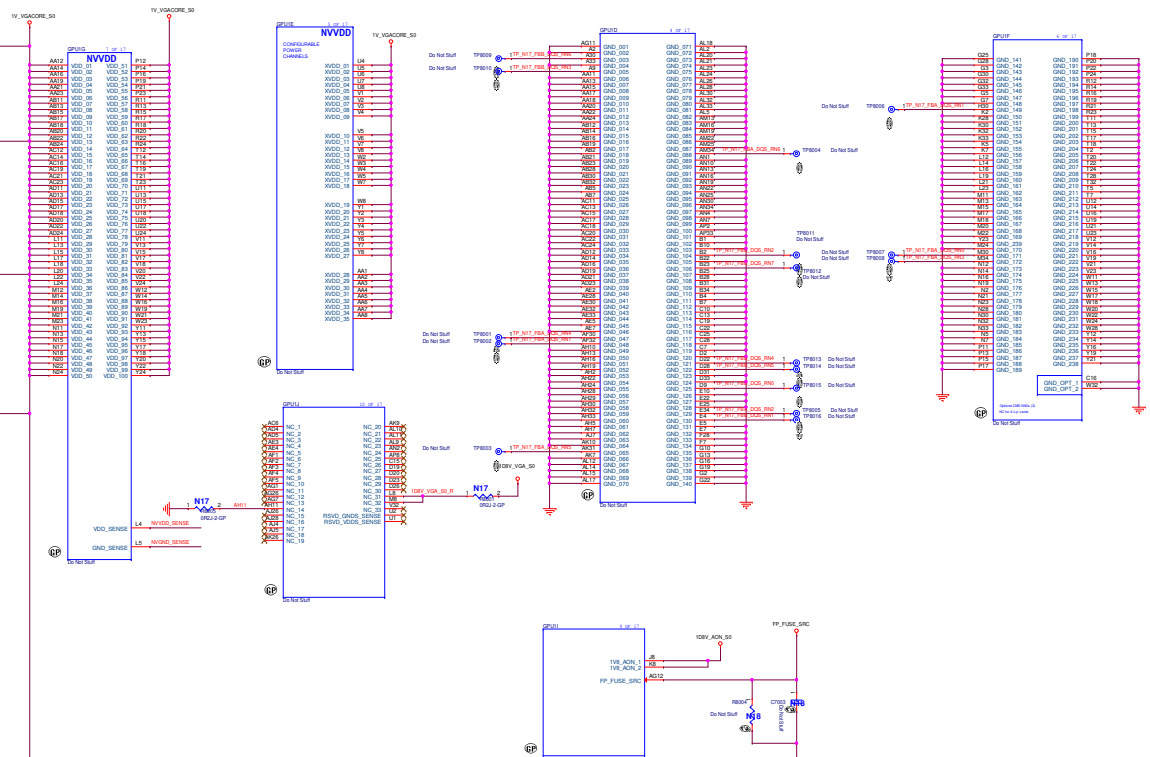
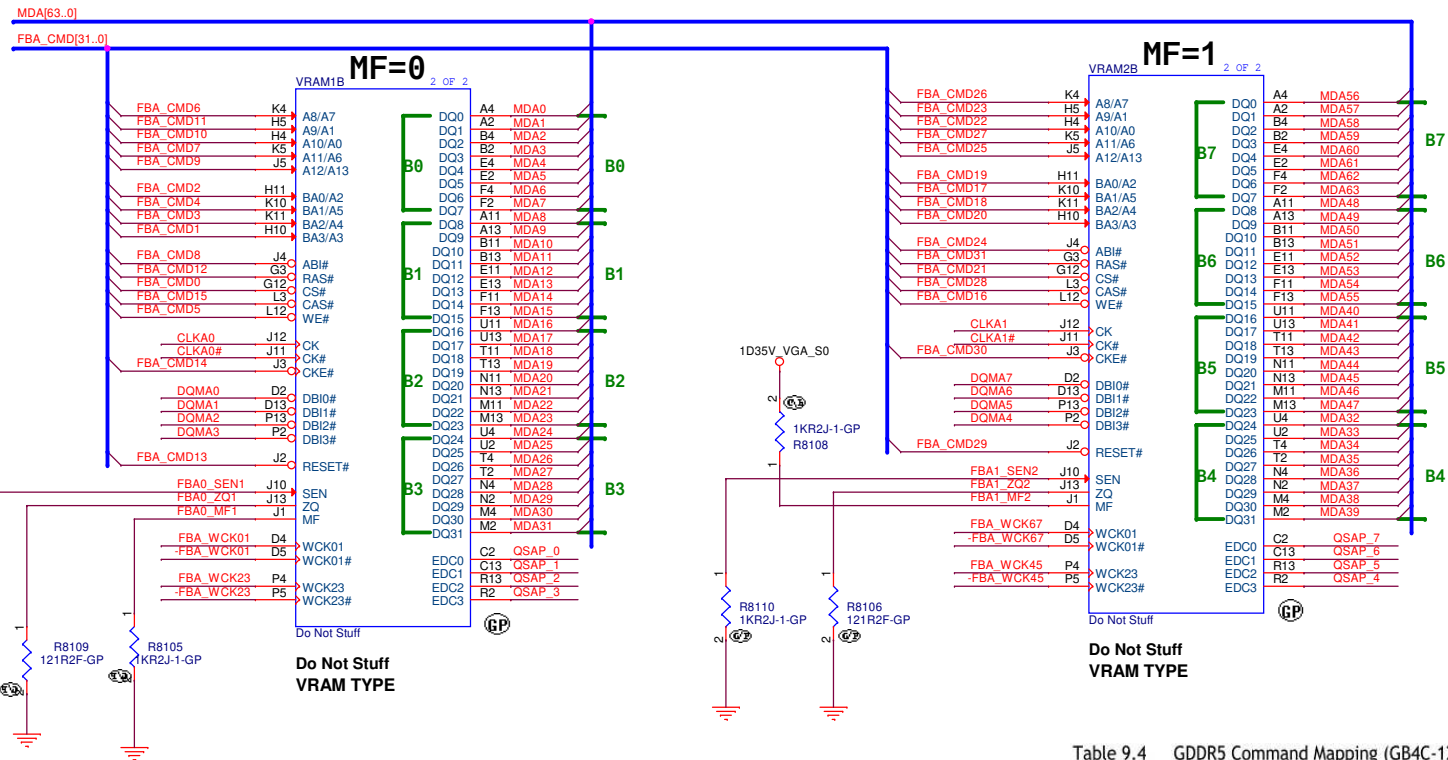
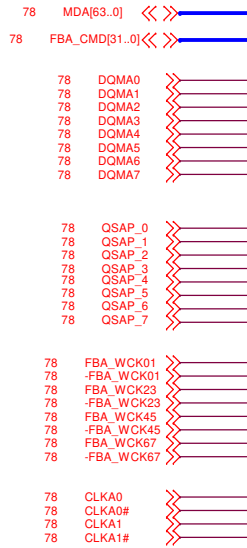


Table 9. VDD_AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
N17 VDD18 (N18 NC) Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X7R	0402	N/A	2	Under GPU
	1.0 μ F	X65	0603	N/A	1	Near GPU
	4.7 μ F	X65	0603	N/A	1	Near GPU
1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X7R	0402	0	2	Under GPU
	0.47 μ F ¹	X65	0201W	4	0	Under GPU
	1.0 μ F ¹	X65	0402 or 0201W	0	1	Near GPU
	0.47 μ F ¹	X65	0201W	6	0	Near GPU
	4.7 μ F	X65	0603	3	1	Near GPU

Note:

1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.



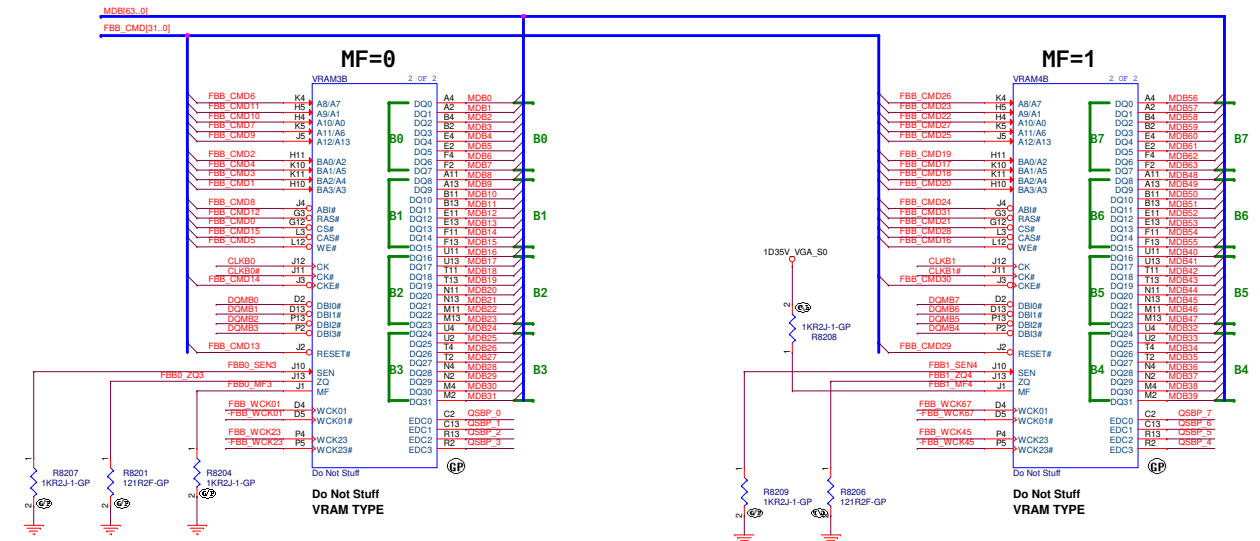
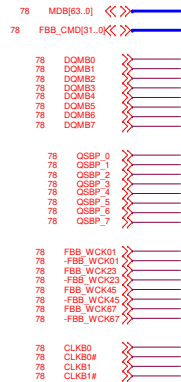
GDDR5 Data Mapping							
BYTE0 (BYTE4)		BYTE1 (BYTE5)		BYTE2 (BYTE6)		BYTE3 (BYTE7)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ32)	DQ8	DQ16 (DQ40)	DQ16	DQ8 (DQ48)	DQ24	DQ0 (DQ56)
DQ1	DQ25 (DQ33)	DQ9	DQ17 (DQ41)	DQ17	DQ9 (DQ49)	DQ25	DQ1 (DQ57)
DQ2	DQ26 (DQ34)	DQ10	DQ18 (DQ42)	DQ18	DQ10 (DQ50)	DQ26	DQ2 (DQ58)
DQ3	DQ27 (DQ35)	DQ11	DQ19 (DQ43)	DQ19	DQ11 (DQ51)	DQ27	DQ3 (DQ59)
DQ4	DQ28 (DQ36)	DQ12	DQ20 (DQ44)	DQ20	DQ12 (DQ52)	DQ28	DQ4 (DQ60)
DQ5	DQ29 (DQ37)	DQ13	DQ21 (DQ45)	DQ21	DQ13 (DQ53)	DQ29	DQ5 (DQ61)
DQ6	DQ30 (DQ38)	DQ14	DQ22 (DQ46)	DQ22	DQ14 (DQ54)	DQ30	DQ6 (DQ62)
DQ7	DQ31 (DQ39)	DQ15	DQ23 (DQ47)	DQ23	DQ15 (DQ55)	DQ31	DQ7 (DQ63)
DBI0	DBI3 (DBI4)	DBI1	DBI2 (DBI5)	DBI2	DBI1 (DBI6)	DBI3	DBI0 (DBI7)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC6)	EDC3	EDC0 (EDC7)
GDDR5 CLK Mapping							
WCK01	WCK23 (WCK45)			WCK23	WCK01 (WCK67)		
WCK01#	WCK23# (WCK45#)			WCK23#	WCK01# (WCK67#)		
CK	CK						
CK#	CK#						
Others							
MF	MF	SEN	SEN				
ZQ	ZQ	RESET#	RESET#				

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

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GDDR5 Data Mapping							
BYTE0 (BYTEA)		BYTE1 (BYTEB)		BYTE2 (BYTEC)		BYTE3 (BYTER)	
MF=0	MF=1	MF=0	MF=1	MF=0	MF=1	MF=0	MF=1
DQ0	DQ24 (DQ02)	DQ8	DQ16 (DQ04)	DQ16	DQ8 (DQ04)	DQ24	DQ0 (DQ06)
DQ1	DQ25 (DQ03)	DQ9	DQ17 (DQ05)	DQ17	DQ9 (DQ05)	DQ25	DQ1 (DQ07)
DQ2	DQ26 (DQ04)	DQ10	DQ18 (DQ06)	DQ18	DQ10 (DQ06)	DQ26	DQ2 (DQ08)
DQ3	DQ27 (DQ05)	DQ11	DQ19 (DQ07)	DQ19	DQ11 (DQ07)	DQ27	DQ3 (DQ09)
DQ4	DQ28 (DQ06)	DQ12	DQ20 (DQ08)	DQ20	DQ12 (DQ08)	DQ28	DQ4 (DQ10)
DQ5	DQ29 (DQ07)	DQ13	DQ21 (DQ09)	DQ21	DQ13 (DQ09)	DQ29	DQ5 (DQ11)
DQ6	DQ30 (DQ08)	DQ14	DQ22 (DQ10)	DQ22	DQ14 (DQ10)	DQ30	DQ6 (DQ12)
DQ7	DQ31 (DQ09)	DQ15	DQ23 (DQ11)	DQ23	DQ15 (DQ11)	DQ31	DQ7 (DQ13)
DBI0	DBI3 (DB04)	DBI1	DBI2 (DB05)	DBI2	DBI1 (DB05)	DBI3	DBI0 (DB07)
EDC0	EDC3 (EDC4)	EDC1	EDC2 (EDC5)	EDC2	EDC1 (EDC5)	EDC3	EDC0 (EDC7)
GDDR5 CLK Mapping							
WCK01	WCK23 (WCK45)	WCK23 WCK01# (WCK67)					
WCK01#	WCK23# (WCK46)	WCK23# WCK01# (WCK67#)					
CK	CK						
CK#	CK#						
Others							
MF	MF	SEN	SEN				
ZQ	ZQ	RESET#	RESET#				

Table 9.4 GDDR5 Command Mapping (GB4C-128 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

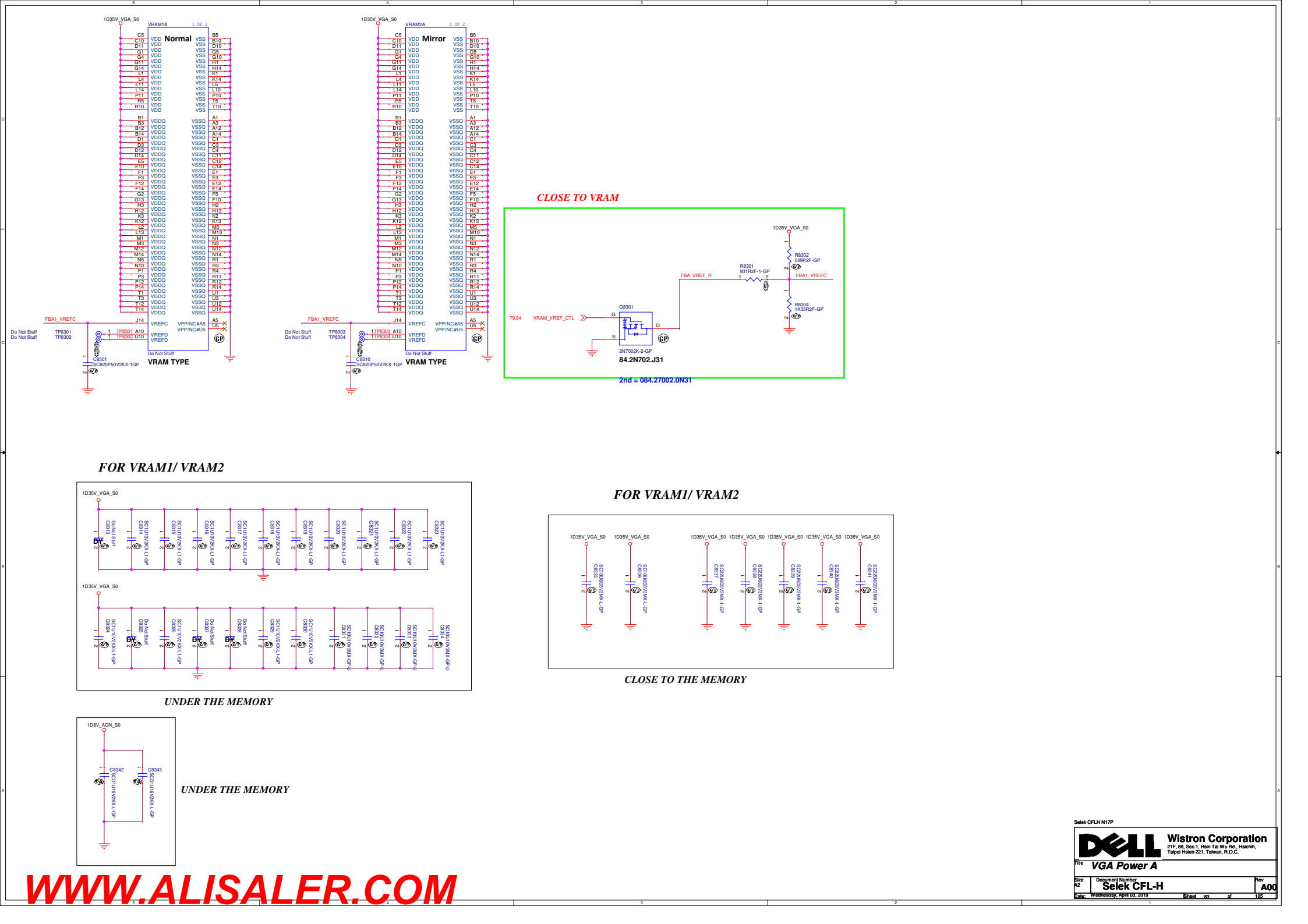
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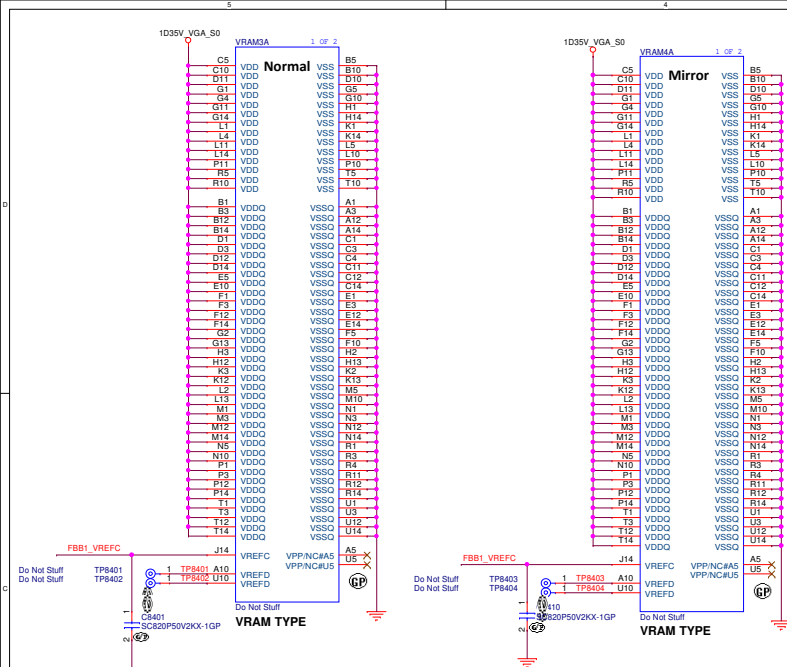
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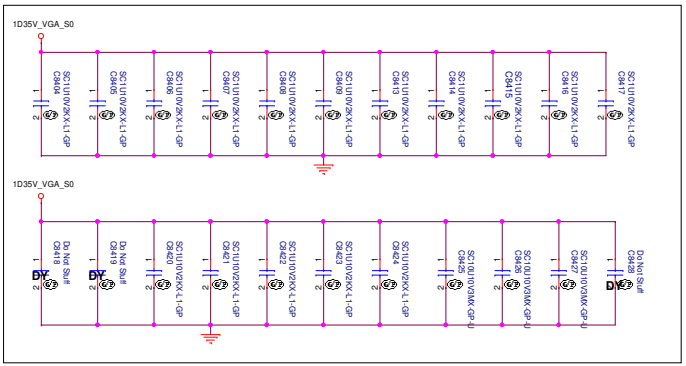
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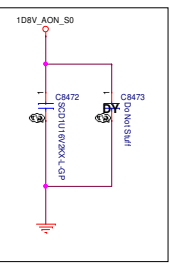
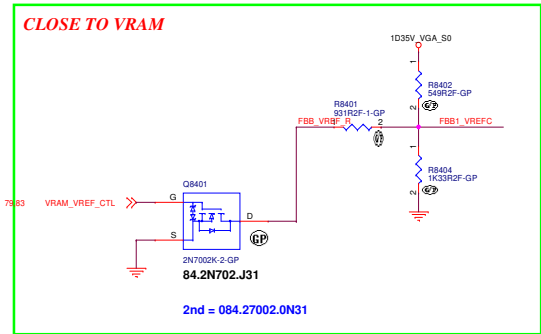




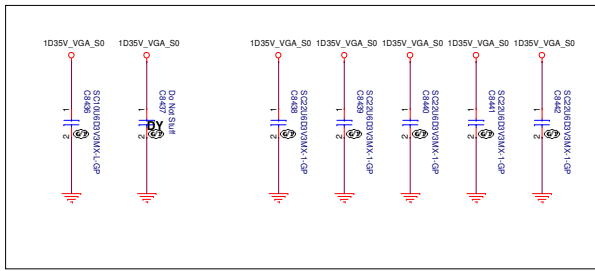
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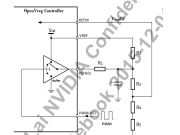
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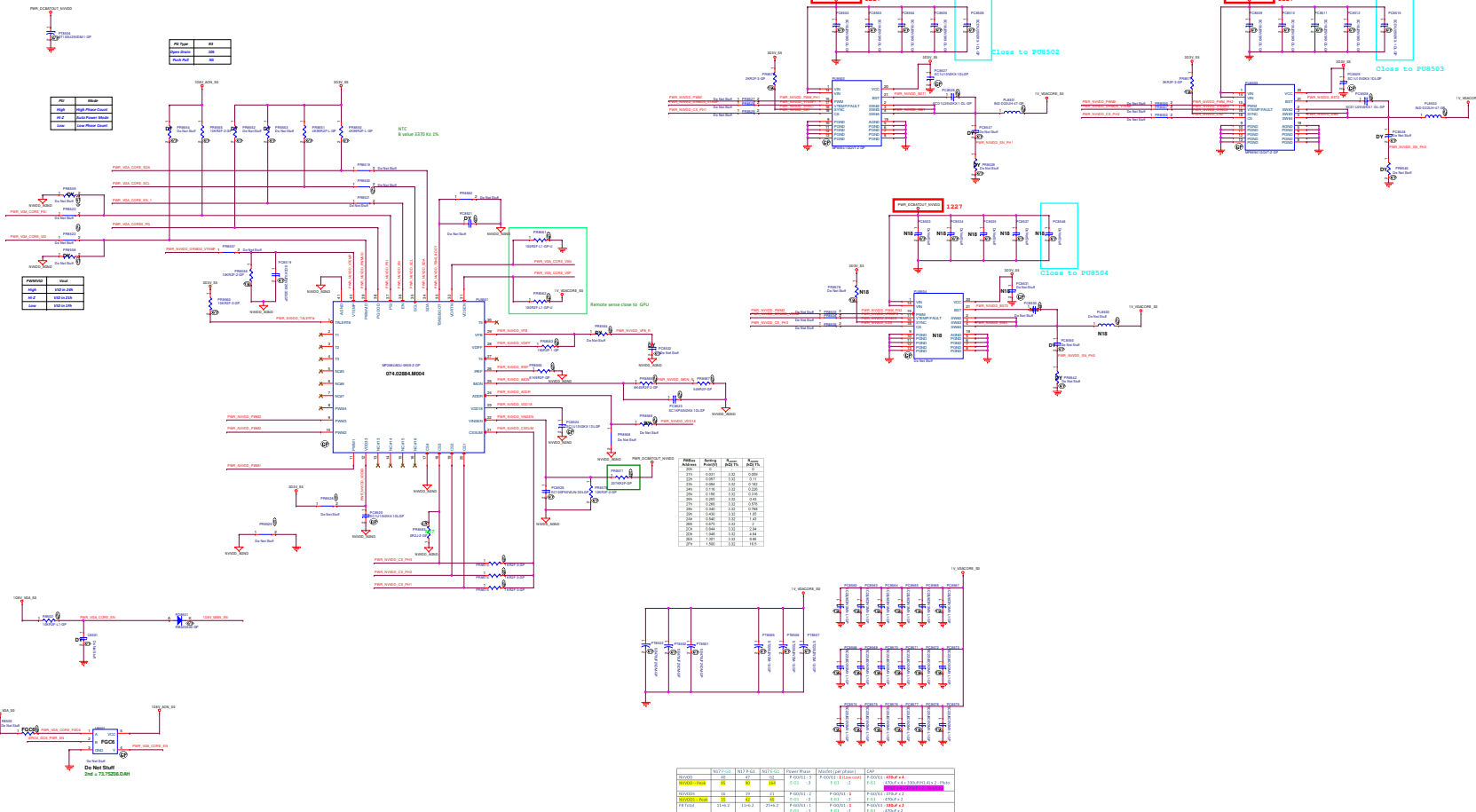
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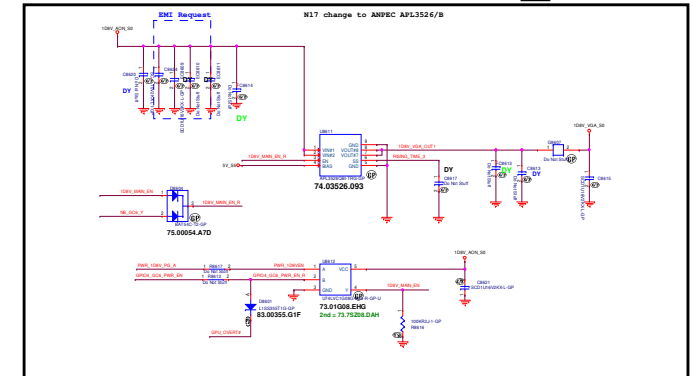


CLOSE TO THE MEMORY



PWM-VID Specification		Config
V _{min}	V	0.3
V _{max}	V	1.3
V _{boot}	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
Pulse Width Frequency F _{PWM}	kHz	8.75
PWM Minimum Pulse Width T _{PWM}	ns	9.25
VID Transient Time T	us	100
Component Value		
R1 (1%)	kΩ	6.19
R2 (1%)	kΩ	20.5
R3 (1%)	kΩ	4.32
R4 (5%)	kΩ	16.5
R5 (1%)	kΩ	0.299
C	nF	5.5





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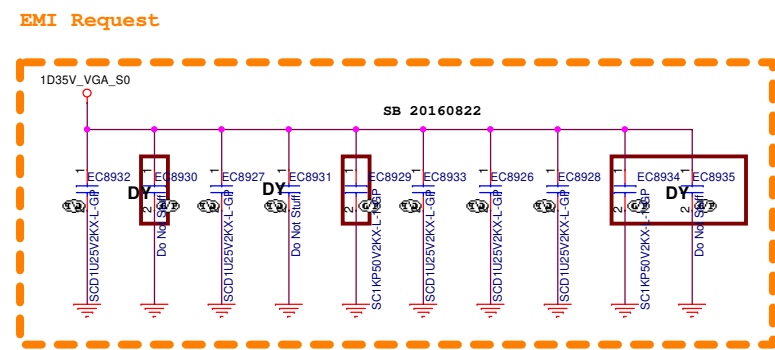
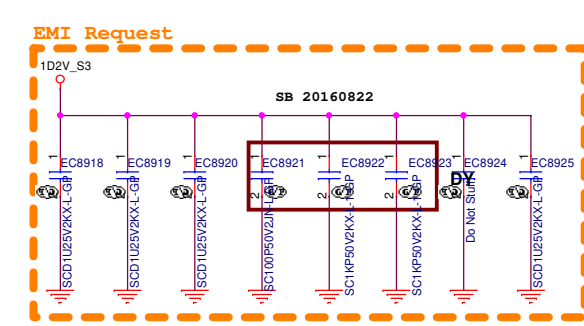
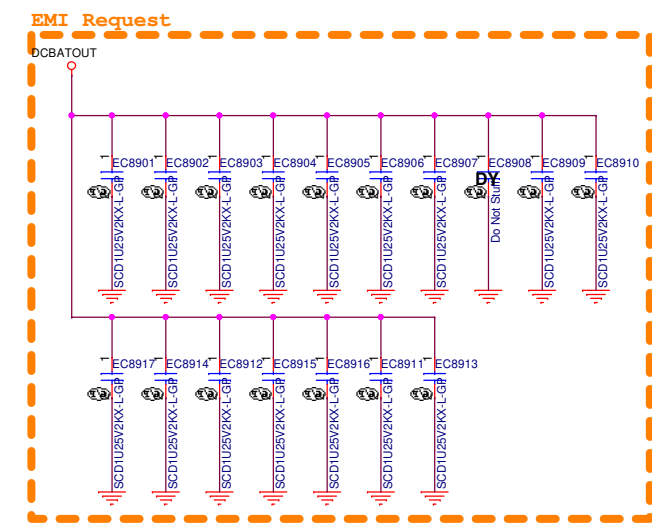
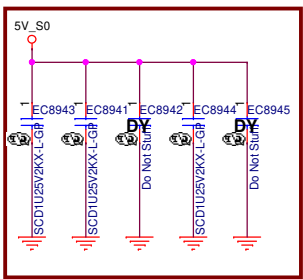
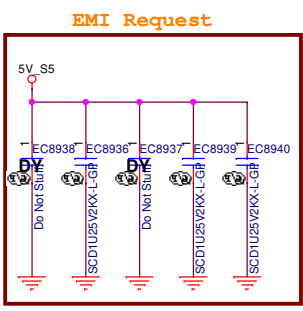
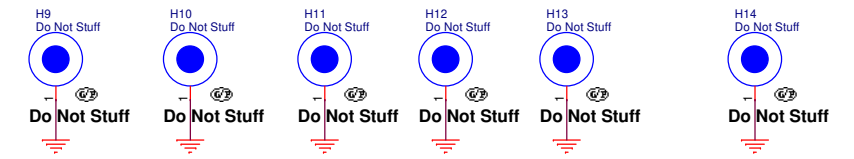
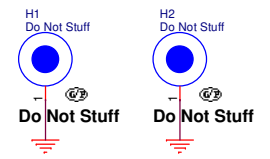
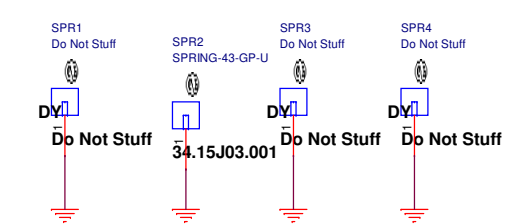
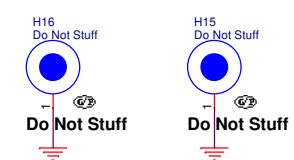
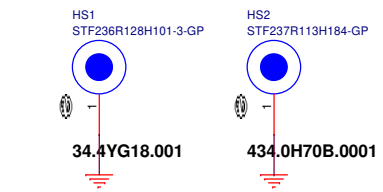
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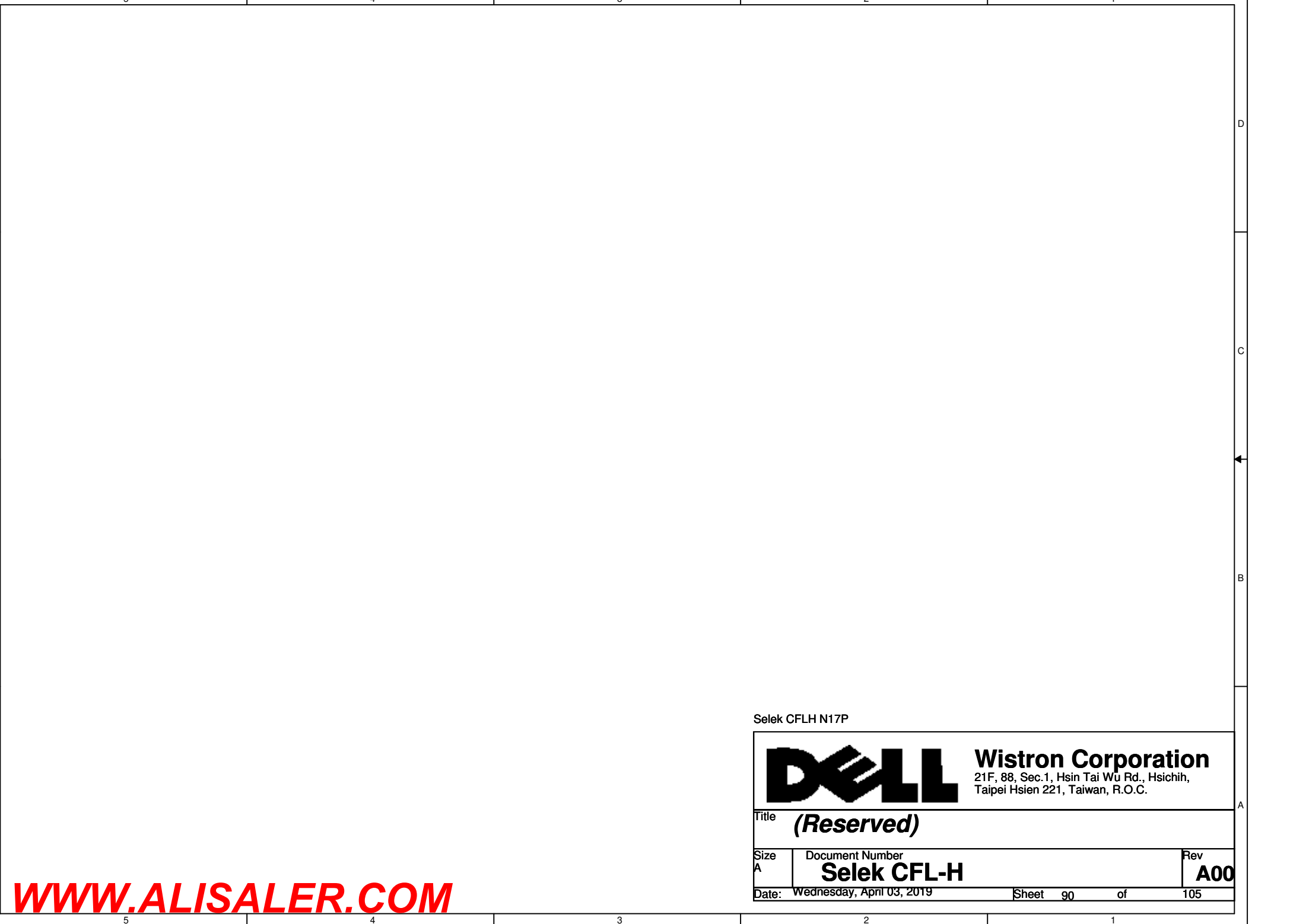
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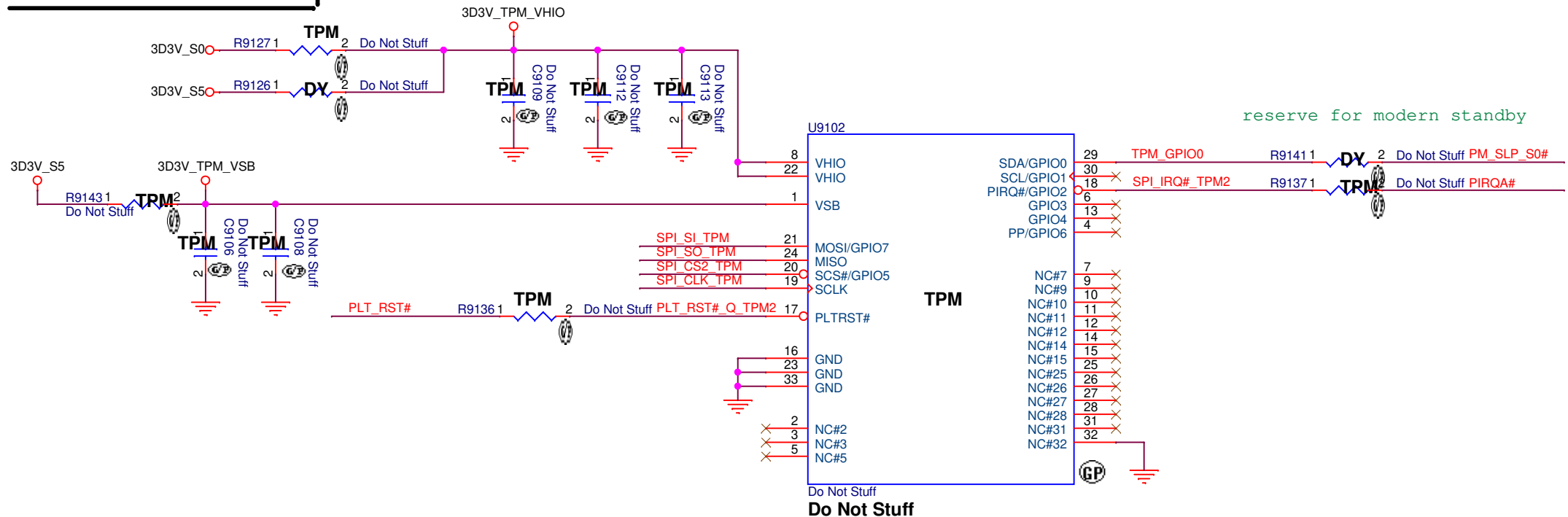
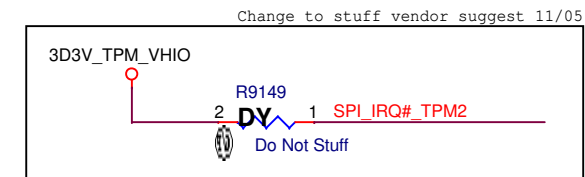
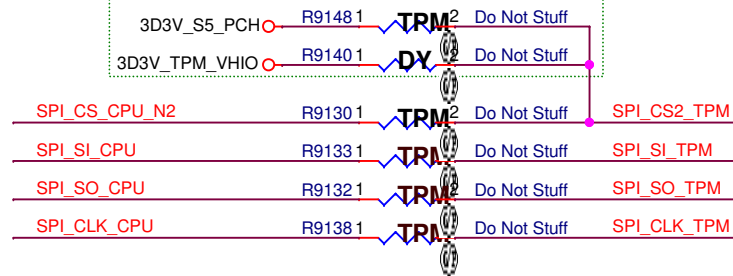
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15	TPM_SPI_IRQ#	>>>	_____
31,61,63,79	PLT_RST#	>>>	_____
15,40	PM_SLP_S0#	>>>	_____
15	SPI_CS_CPU_N2	>>>	_____
15,21,25	SPI_SO_CPU	<<<	_____
15,21,25	SPI_SI_CPU	>>>	_____
15,25	SPI_CLK_CPU	>>>	_____

reserve RTC Gen 9 reset circuit_20170814
leakage issue



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Title

TPM2.0

Size
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Document Number

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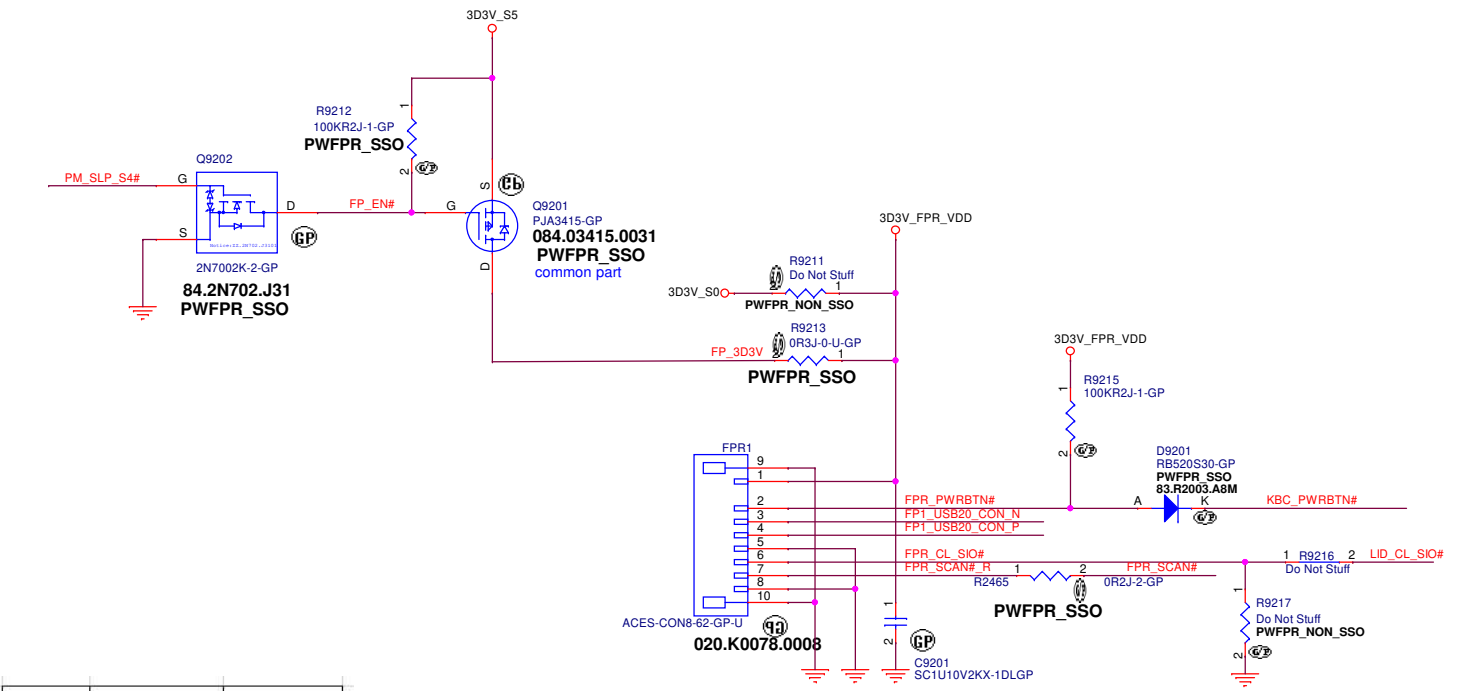
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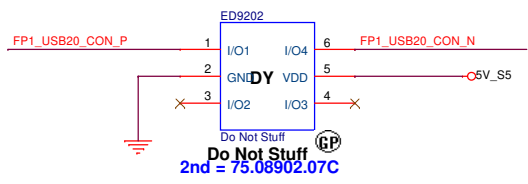
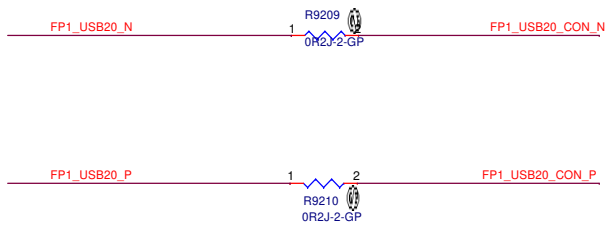
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24 FPR_SCAN# >>> _____
15,40,44,51 PM_SLP_S4# >>> _____
24,64 KBC_PWRBTN# <<< _____
24,66 LID_CL_SIO# >>> _____

18 FP1_USB20_N <<< _____
18 FP1_USB20_P <<< _____



	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0



FBR(Bottom side finger Print Sensor)

PWFPR_SSO: GOODIX module
PWFPR_NON_SSO: ELAN module(R9211 R9214 R9217)

GF5288WN1+GF128A+GM168 Module design

Pin Definition

CN PIN MAP	
PIN NO.	INFO
1	VCC-3.3V
2	Power button
3	USB_N
4	USB_P
5	GND
6	LID closed
7	GPIO_key shielding
8	GND(ID pin)

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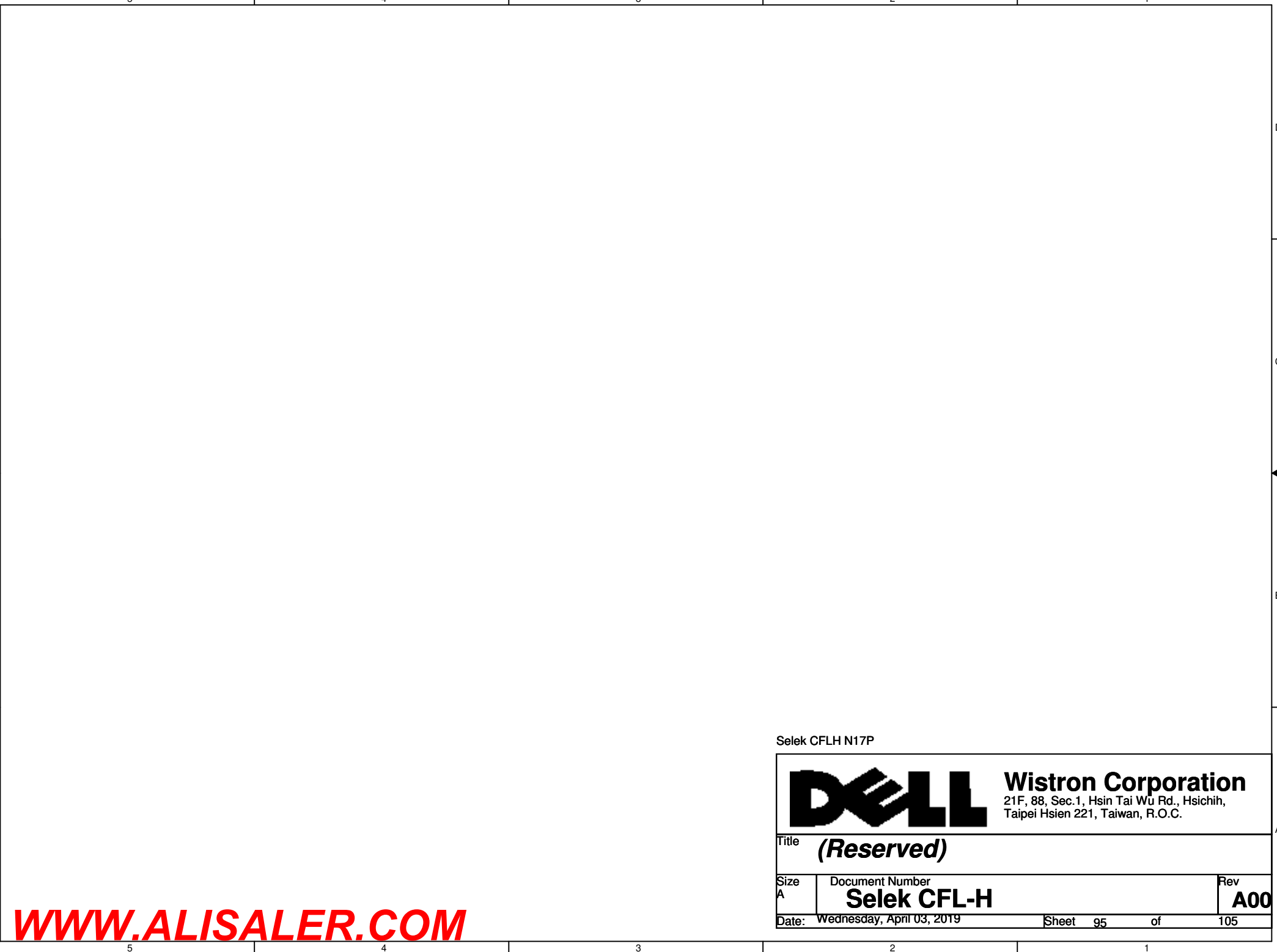
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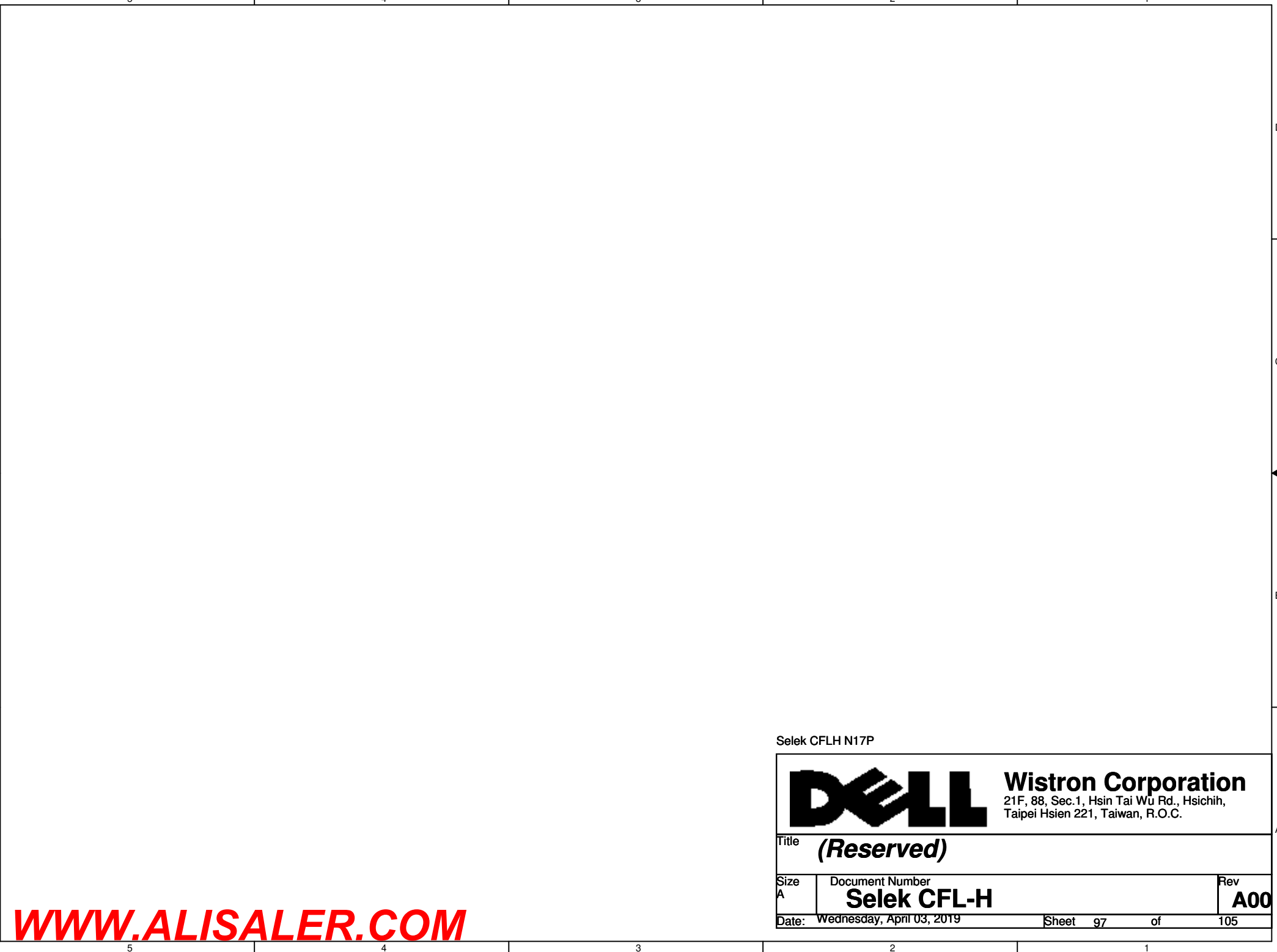
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Main Func = XDP

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TitleCPU_XDP;PCH_XDP

SizeA3


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C				C
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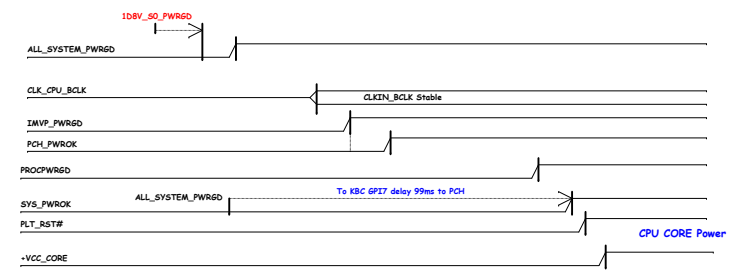
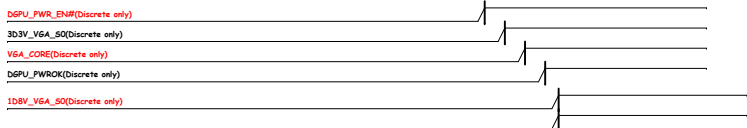
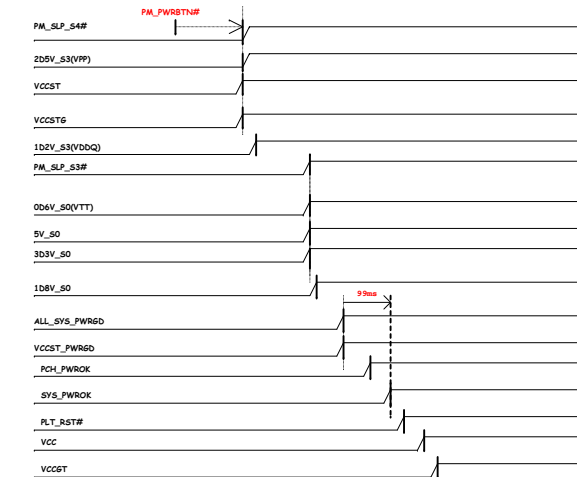
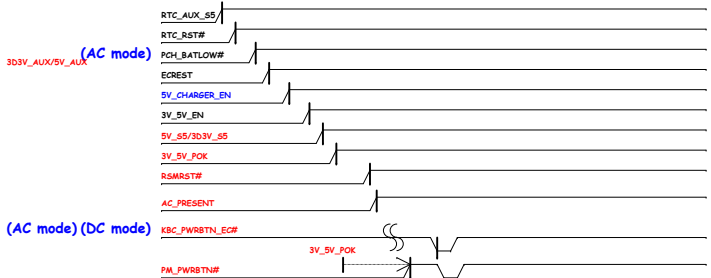
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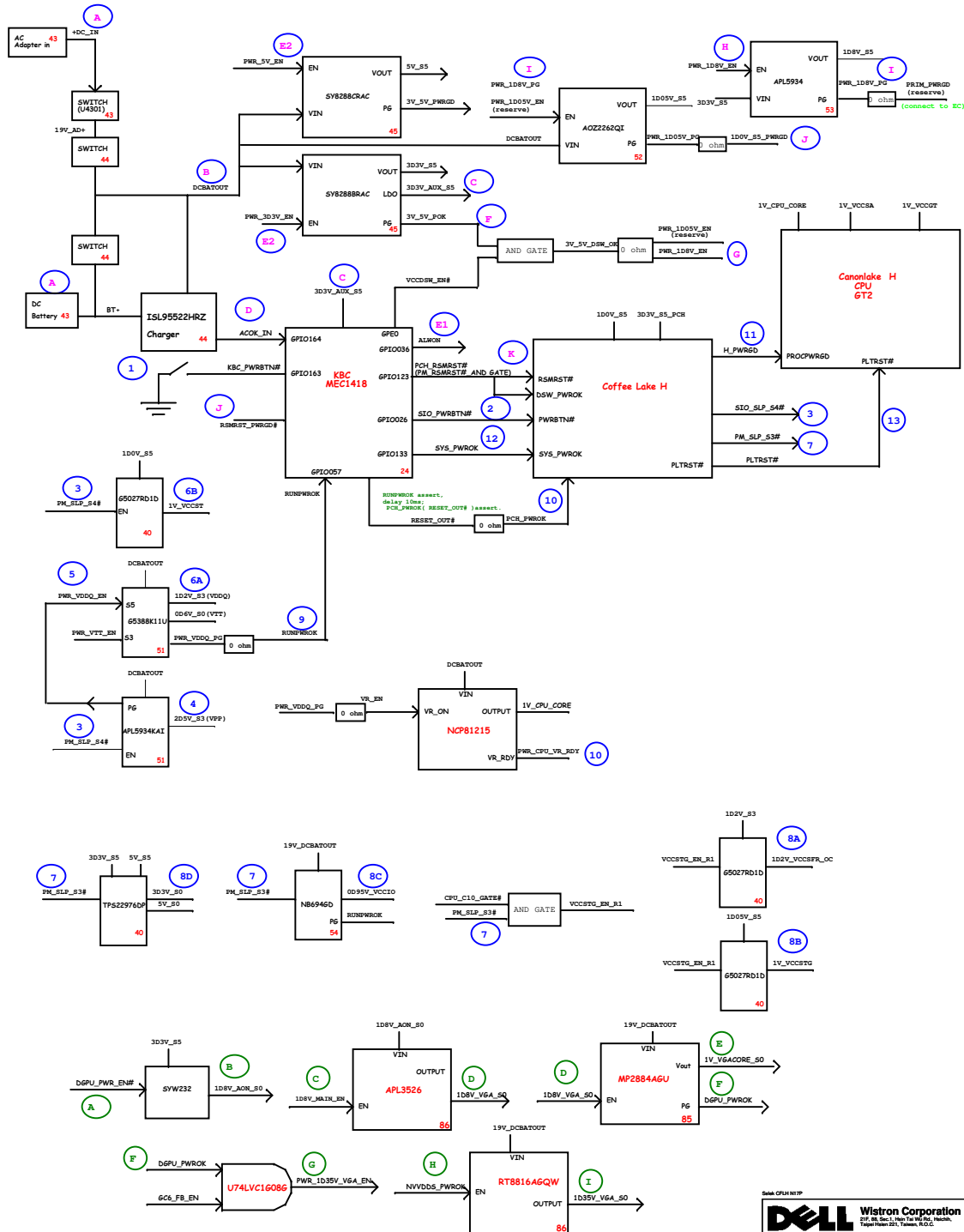
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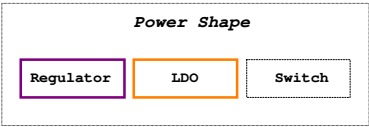
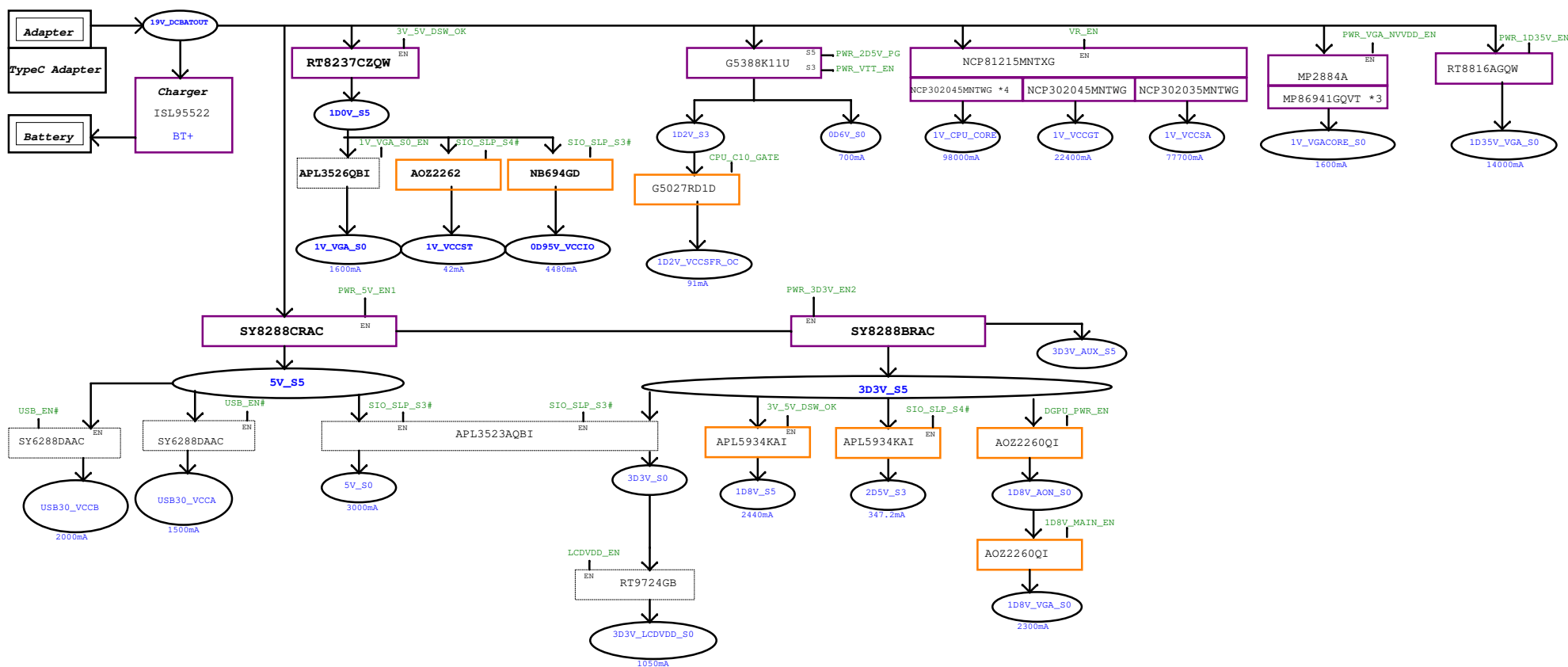
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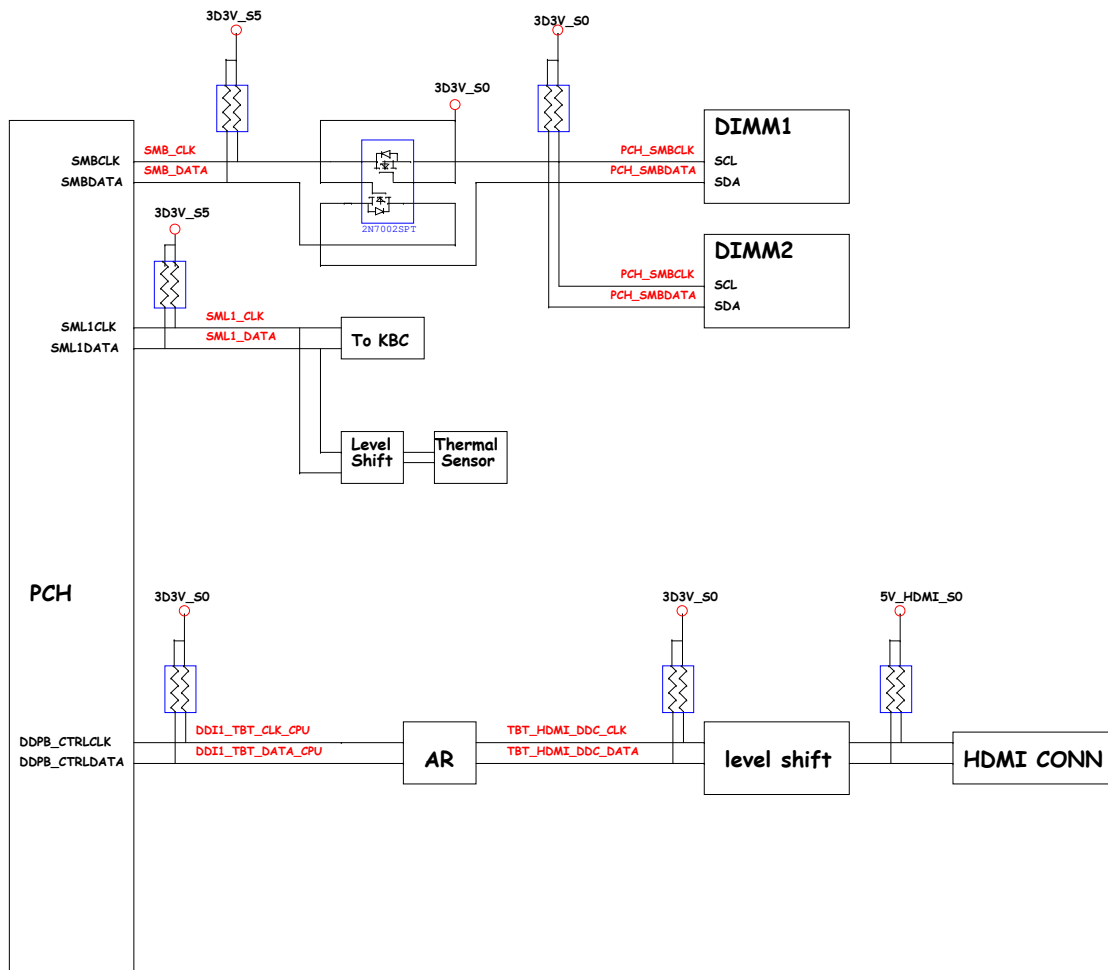


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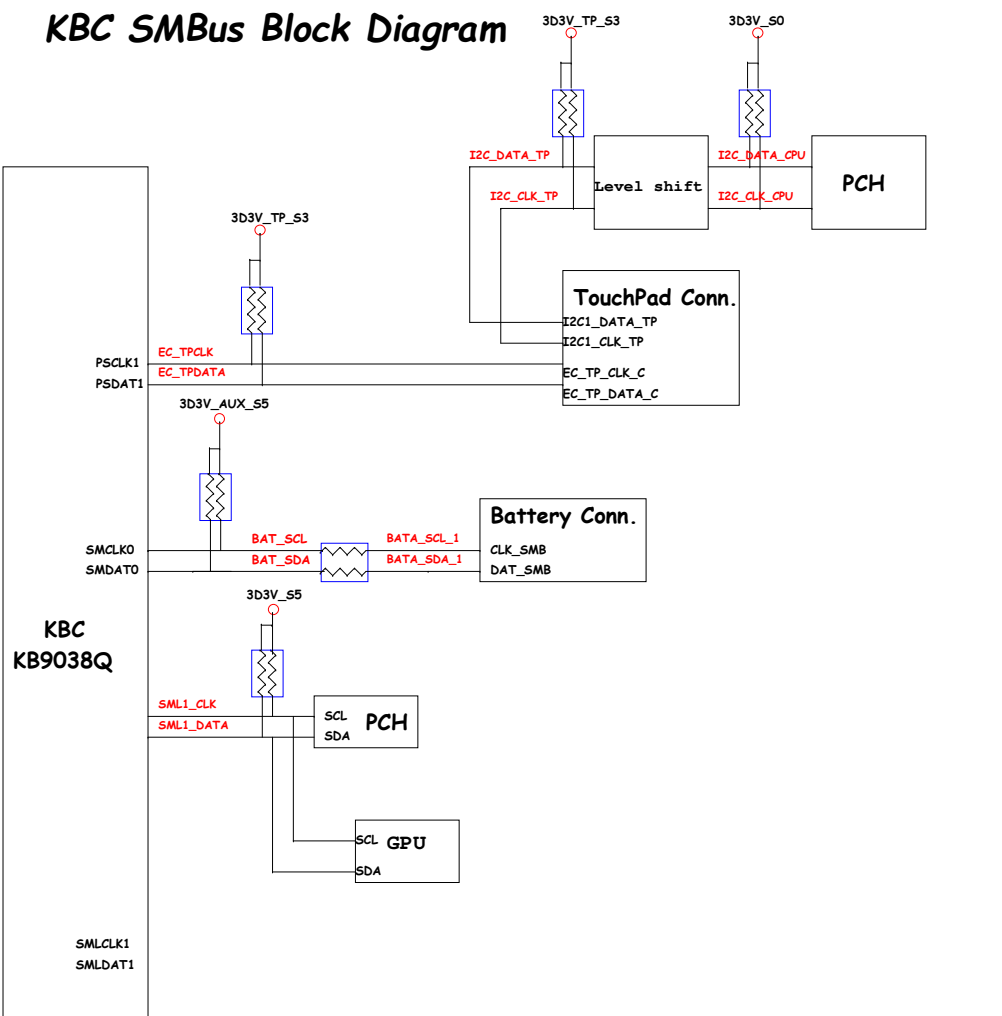




PCH SMBus Block Diagram



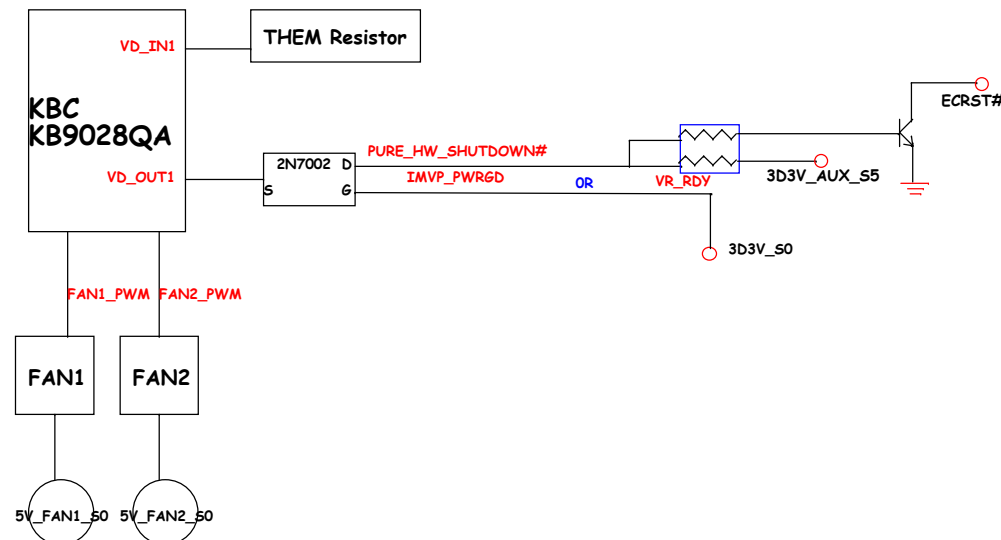
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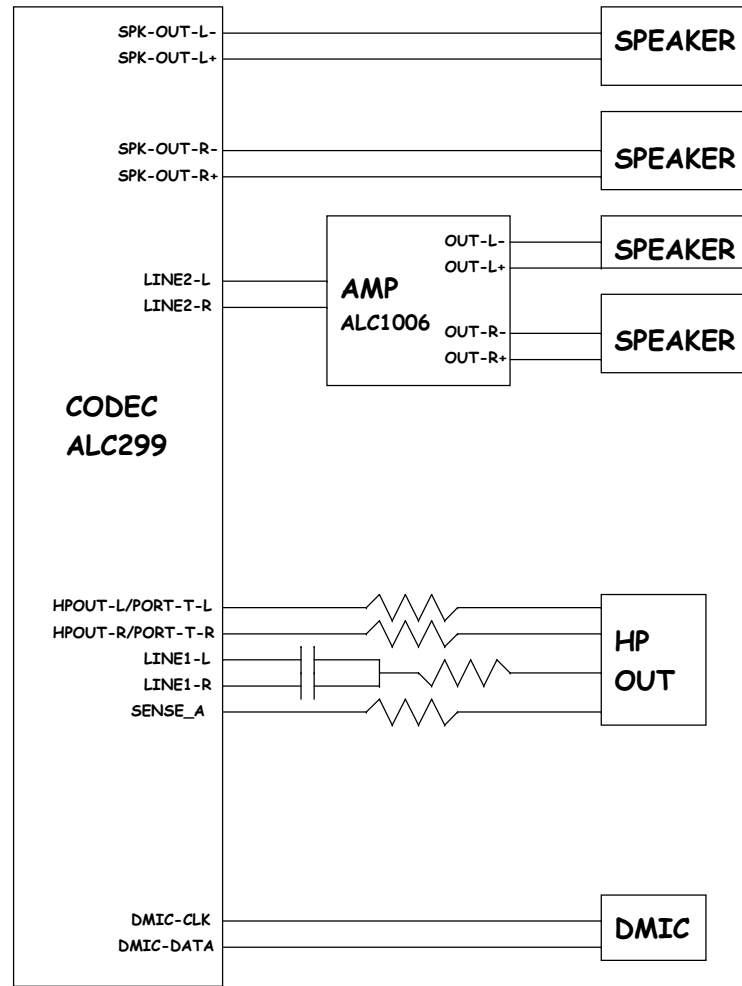
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Thermal Block Diagram



Audio Block Diagram



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