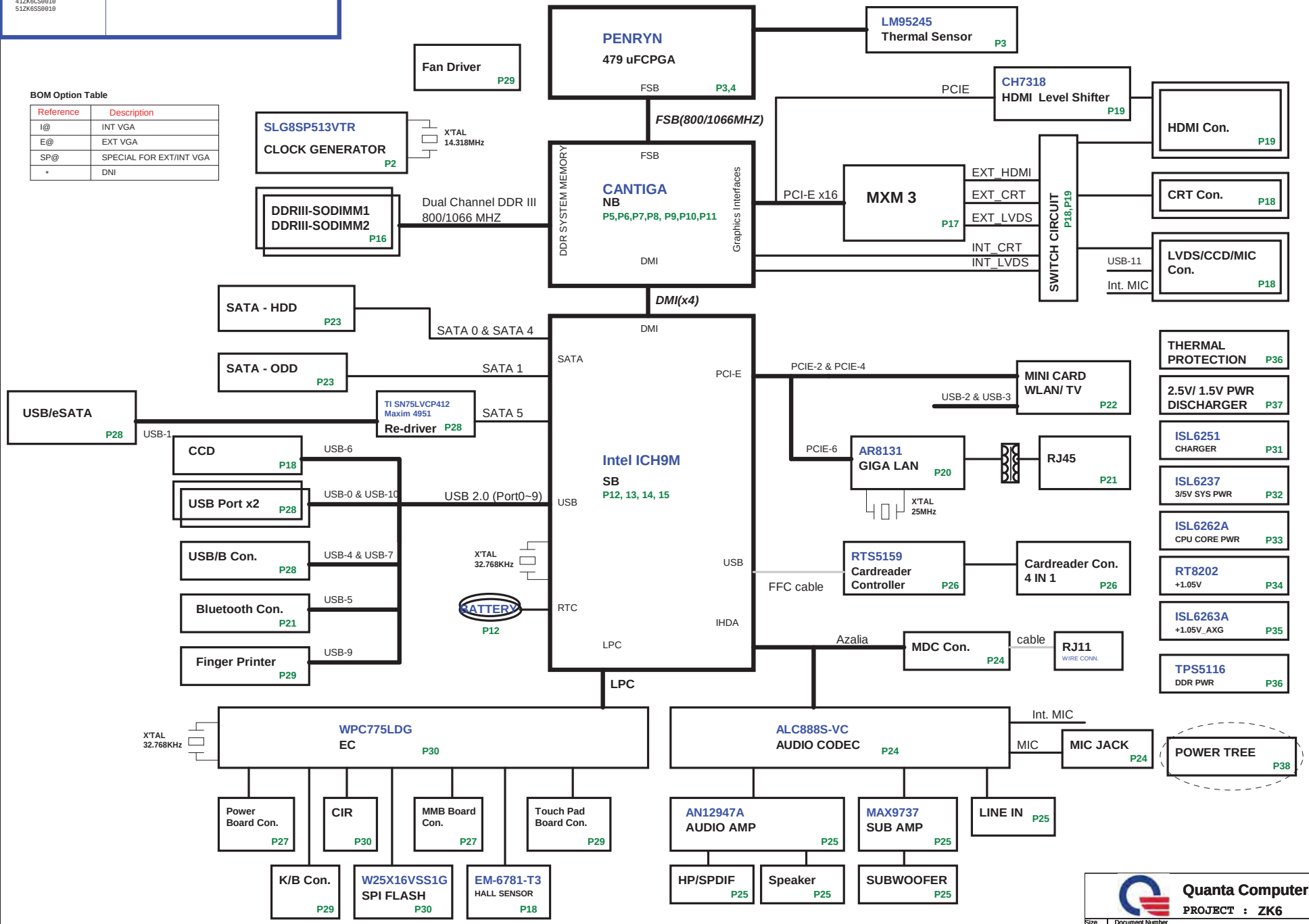
VER : 1A

BOM P/N	Description
31ZK6MB0000 41ZK6CS0000 51ZK6SS0000 31ZK6MB0010 41ZK6CS0010 51ZK6SS0010	uma / mxm 00 / 10

ZK6 MB Block Diagram

BOM Option Table

Reference	Description
I@	INT VGA
E@	EXT VGA
SP@	SPECIAL FOR EXT/INT VGA
*	DNI



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PROJECT : ZK6

Size	Document Number	Rev
	Block Diagram	1A

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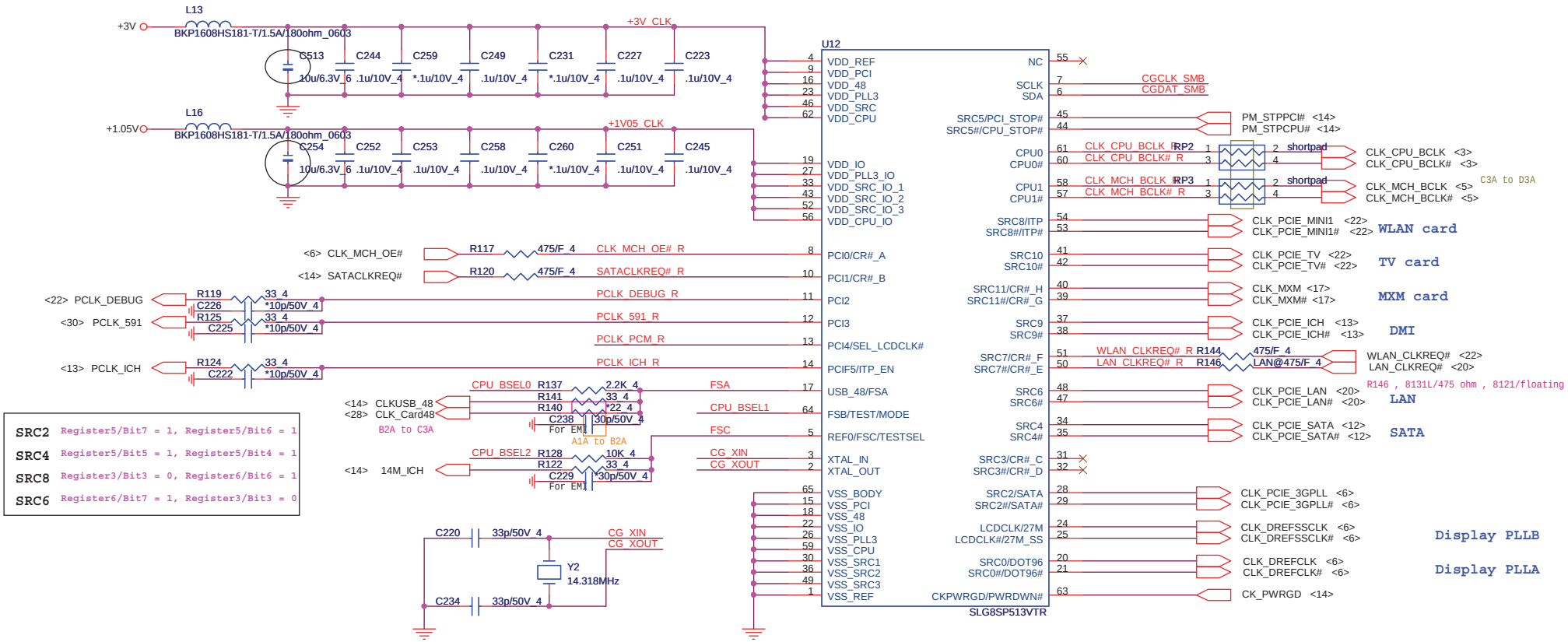
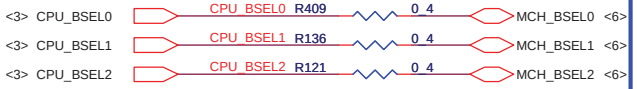
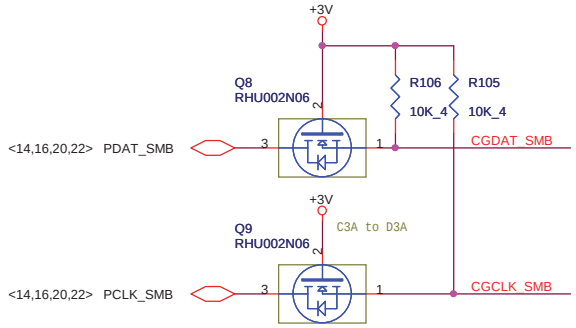
Clock Generator



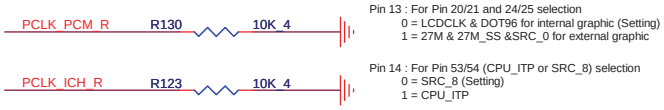
CPU Clock select



FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Generator Strap table



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PROJECT : ZK6

Size	Document Number	Rev
	CLOCK GENERATOR	1A

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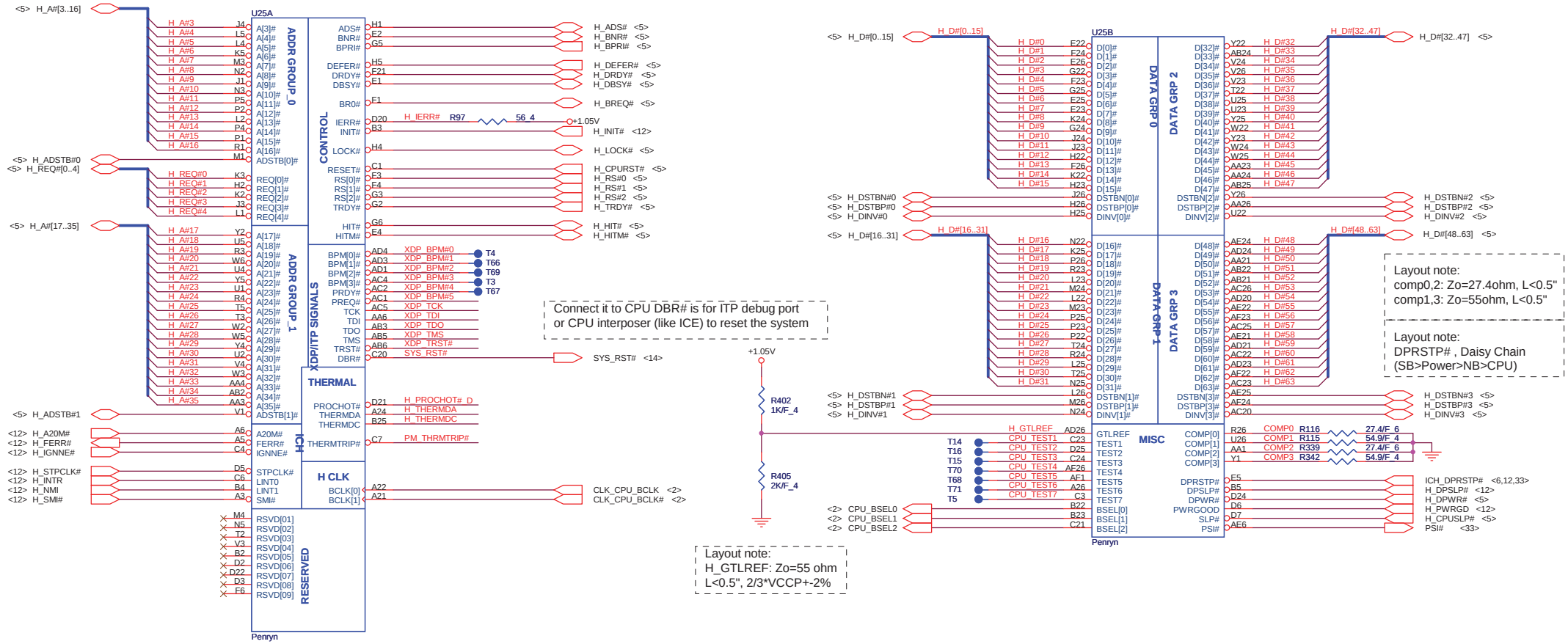
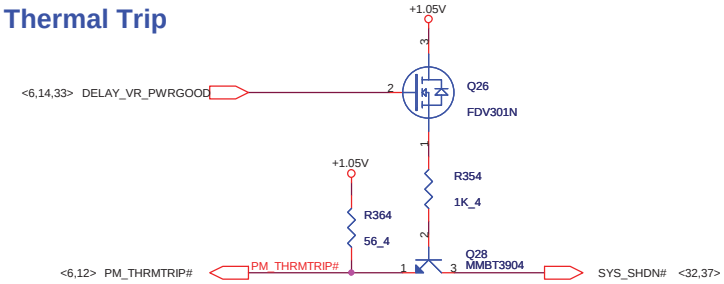


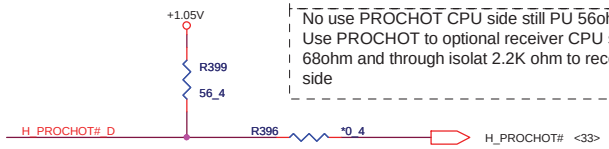
Thermal Trip



Processor hot

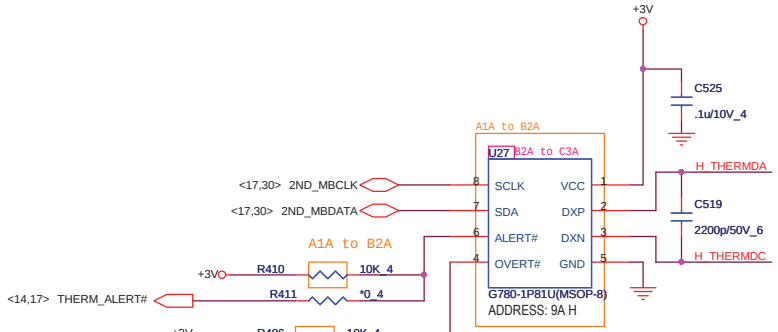
No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side



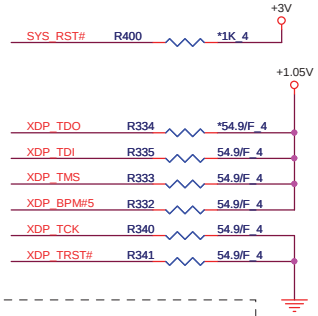
CPU 1/2

CPU Thermal monitor



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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PROJECT : ZK6

Size	Document Number	Rev
	CPU Host Bus	1A

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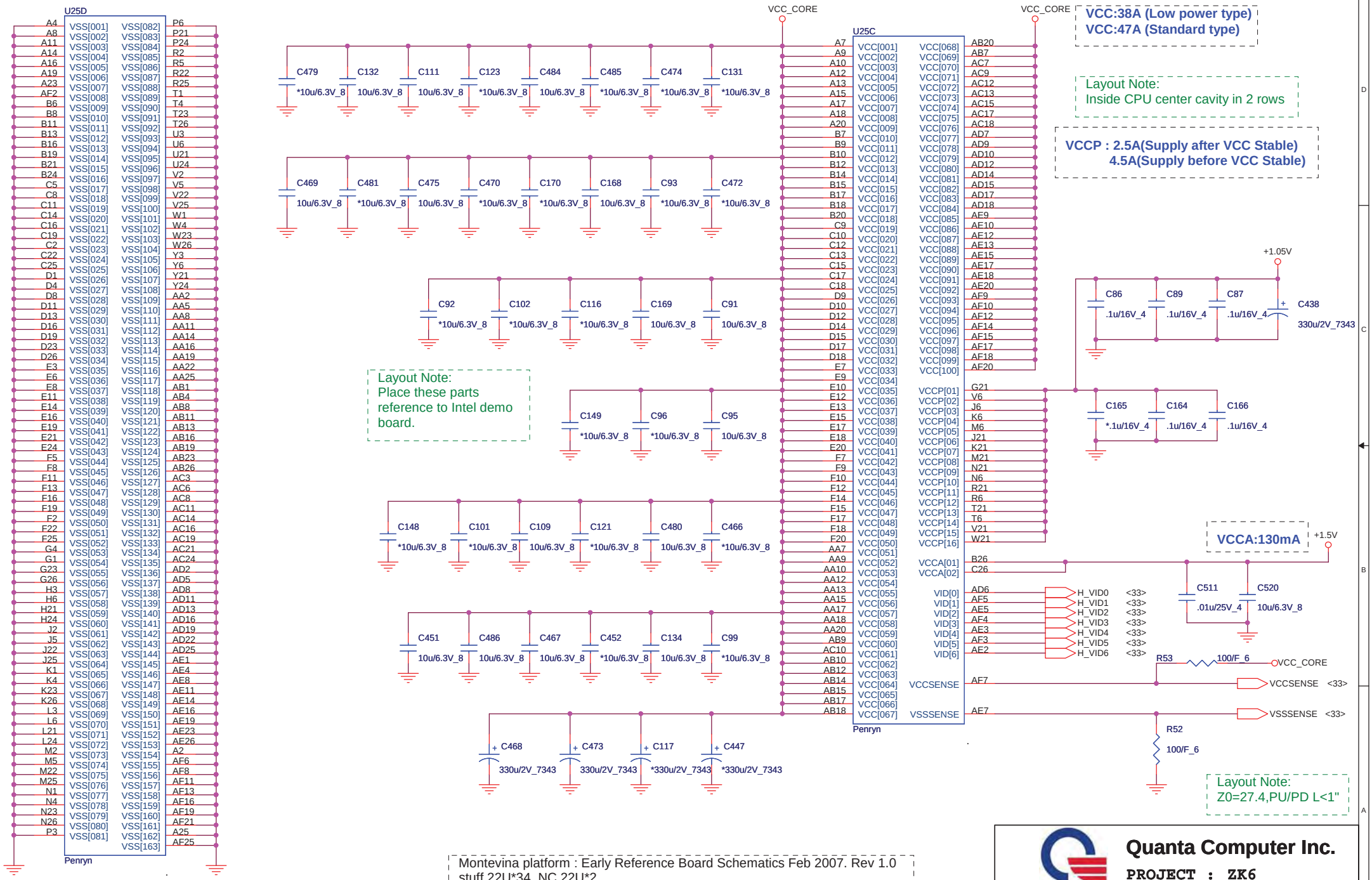

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	CPU Power	1A

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CPU 2/2

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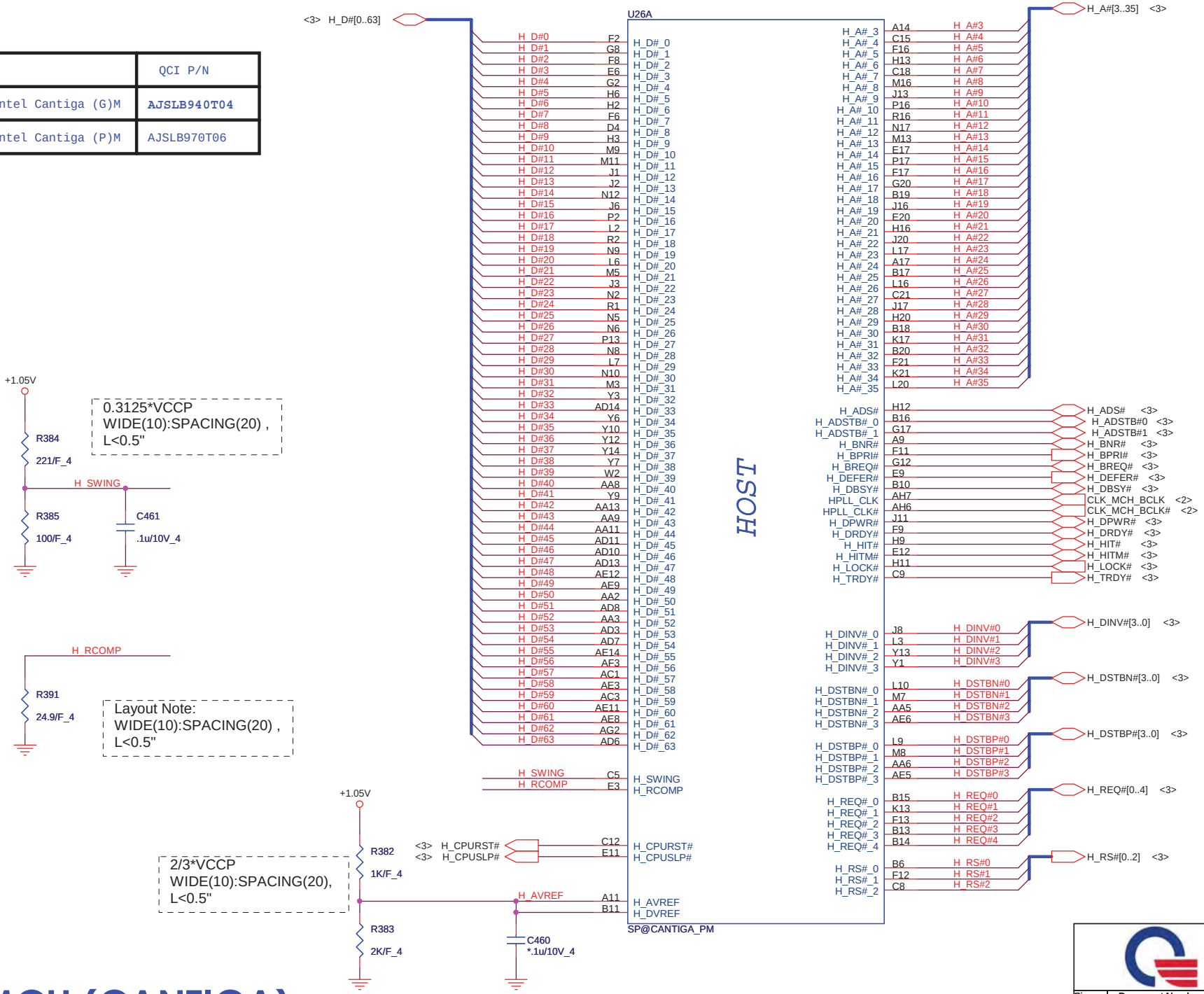
	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH HOST	1A

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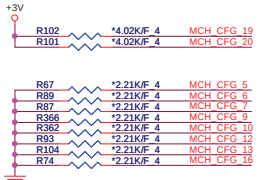
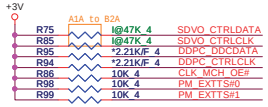
IV@
EV@

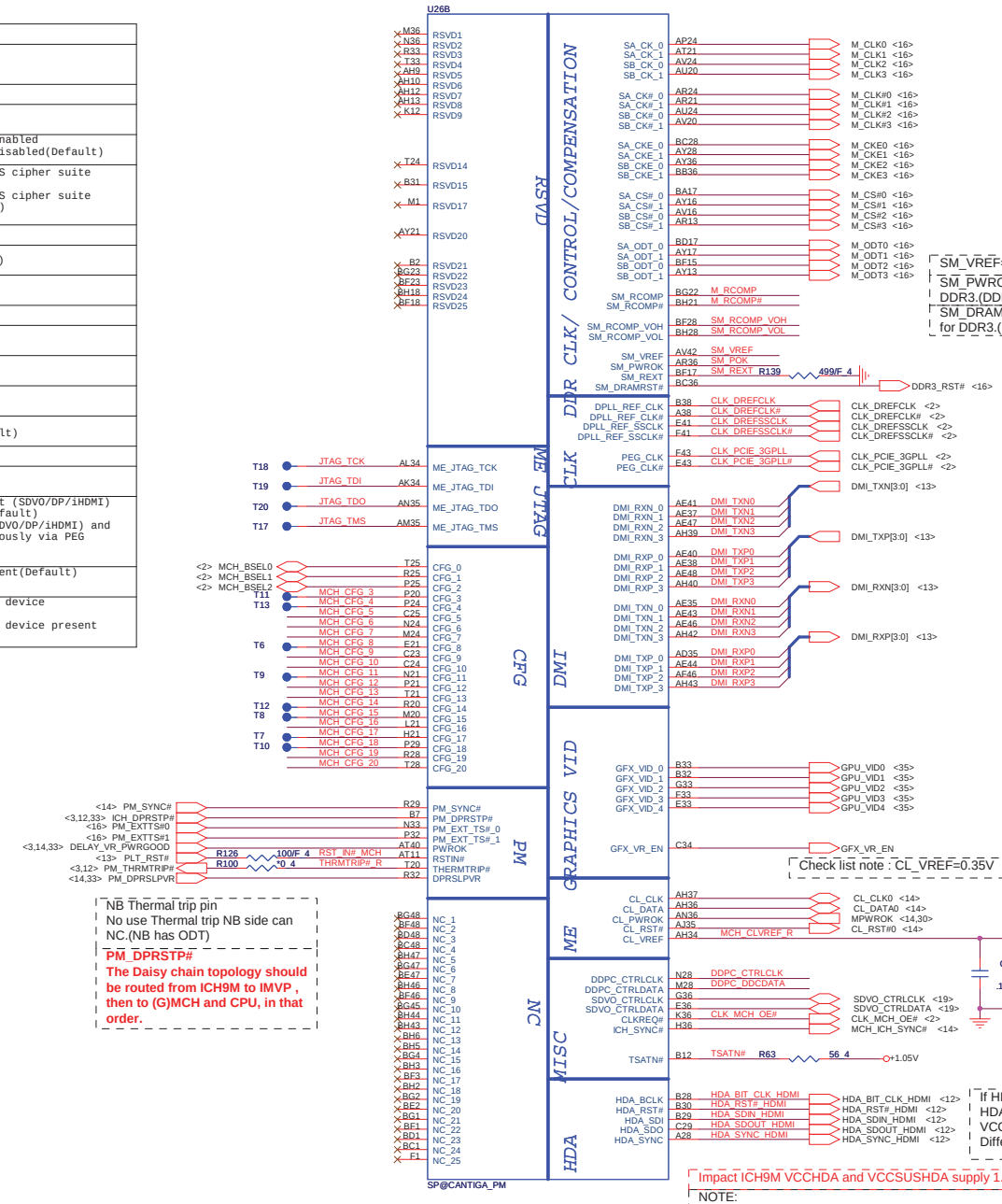
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

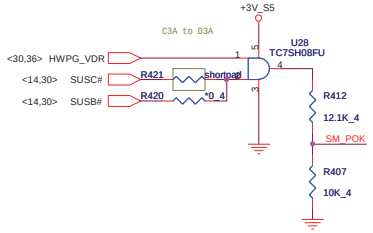
Strap pin

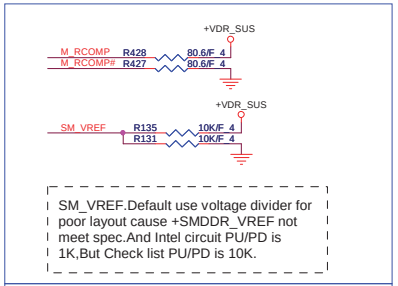


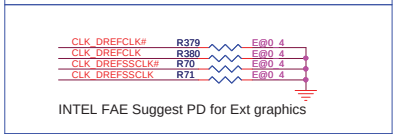


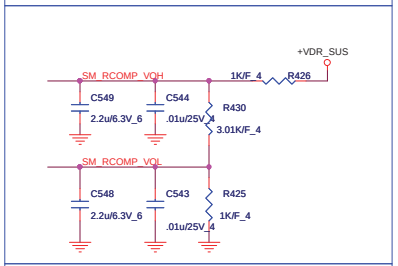


DDR3 PWROK

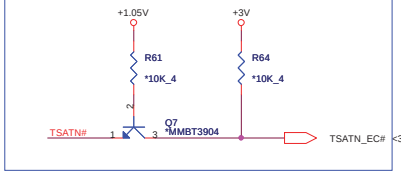








NB Thermaltrip



GMCH (CANTIGA)
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PROJECT : ZK6

Size	Document Number	Rev
	GMCH DMI	1A

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IV@

EV@

SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U26C

<18> L_BKLT_CTRL — L32 L_BKLT_CTRL
<18> INT_LVDS_BLON — G32 L_BKLT_EN
R92 I@10K_4 L_CTRL_CLK — M32 L_CTRL_CLK
+3V — R91 I@10K_4 L_CTRL_DATA — M33 L_CTRL_DATA
<18> INT_LVDS_EDIDCLK — K33 L_DDC_CLK
<18> INT_LVDS_EDIDDATA — J33 L_DDC_DATA
<18> INT_LVDS_DIGON — M29 L_VDD_EN
R65 I@2.37K/F_4 — C44 LVDS_IBG
B43 LVDS_VBG
E37 LVDS_VREFH
E38 LVDS_VREFL
<17> INT_TXLCLKOUT- — INT_TXLCLKOUT- — C41 LVDSA_CLK#
<17> INT_TXLCLKOUT+ — INT_TXLCLKOUT+ — C40 LVDSA_CLK
<17> INT_TXUCLKOUT- — INT_TXUCLKOUT- — B37 LVDSB_CLK#
<17> INT_TXUCLKOUT+ — INT_TXUCLKOUT+ — A37 LVDSB_CLK
<17> INT_TXLOUT0- — INT_TXLOUT0- — H47 LVDSA_DATA#_0
<17> INT_TXLOUT1- — INT_TXLOUT1- — E46 LVDSA_DATA#_1
<17> INT_TXLOUT2- — INT_TXLOUT2- — G40 LVDSA_DATA#_2
A40 LVDSA_DATA#_3
<17> INT_TXLOUT0+ — INT_TXLOUT0+ — H48 LVDSA_DATA_0
<17> INT_TXLOUT1+ — INT_TXLOUT1+ — D45 LVDSA_DATA_1
<17> INT_TXLOUT2+ — INT_TXLOUT2+ — F40 LVDSA_DATA_2
B40 LVDSA_DATA_3
<17> INT_TXUOUT0- — INT_TXUOUT0- — A41 LVDSB_DATA#_0
<17> INT_TXUOUT1- — INT_TXUOUT1- — H38 LVDSB_DATA#_1
<17> INT_TXUOUT2- — INT_TXUOUT2- — G37 LVDSB_DATA#_2
J37 LVDSB_DATA#_3
<17> INT_TXUOUT0+ — INT_TXUOUT0+ — B42 LVDSB_DATA_0
<17> INT_TXUOUT1+ — INT_TXUOUT1+ — G38 LVDSB_DATA_1
<17> INT_TXUOUT2+ — INT_TXUOUT2+ — F37 LVDSB_DATA_2
K37 LVDSB_DATA_3

LVDS

R68 75_4 INT_TV_COMP — F25 TVA_DAC
R69 75_4 INT_TV_Y/G — H25 TVB_DAC
R84 75_4 INT_TV_C/R — K25 TVC_DAC
H24 TV_RTN
C31 TV_DCONSEL_0
E32 TV_DCONSEL_1

TVOUT

<17> INT_CRT_BLU — INT_CRT_BLU — E28 CRT_BLUE
<17> INT_CRT_GRN — INT_CRT_GRN — G28 CRT_GREEN
<17> INT_CRT_RED — INT_CRT_RED — J28 CRT_RED
G29 CRT_IRTN
<17> INT_CRT_DDCCLK — H32 CRT_DDC_CLK
<17> INT_CRT_DDCDAT — J32 CRT_DDC_DATA
<17> INT_HSYNC — INT_HSYNC — J29 CRT_HSYNC
CRTIREF — E29 CRT_TVO_IREF
<17> INT_VSYNC — INT_VSYNC — L29 CRT_VSYNC

SP@CANTIGA_PM

PCI-EXPRESS GRAPHICS

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

PEG_COMPI — T37 EXP_A_COMPX — R103 49.9/F_4
PEG_COMPO — T36

PEG_RXN[15:0] <17>

PEG_RX#_0 — H44 PEG_RXN0
PEG_RX#_1 — J46 PEG_RXN1
PEG_RX#_2 — L44 PEG_RXN2
PEG_RX#_3 — L40 PEG_RXN3
PEG_RX#_4 — N41 PEG_RXN4
PEG_RX#_5 — P48 PEG_RXN5
PEG_RX#_6 — N44 PEG_RXN6
PEG_RX#_7 — T43 PEG_RXN7
PEG_RX#_8 — U43 PEG_RXN8
PEG_RX#_9 — Y43 PEG_RXN9
PEG_RX#_10 — Y48 PEG_RXN10
PEG_RX#_11 — Y36 PEG_RXN11
PEG_RX#_12 — AA43 PEG_RXN12
PEG_RX#_13 — AD37 PEG_RXN13
PEG_RX#_14 — AC47 PEG_RXN14
PEG_RX#_15 — AD39 PEG_RXN15

PEG_RXP[15:0] <17>

PEG_RX_0 — H43 PEG_RXP0
PEG_RX_1 — J44 PEG_RXP1
PEG_RX_2 — L43 PEG_RXP2
PEG_RX_3 — L41 PEG_RXP3
PEG_RX_4 — N40 PEG_RXP4
PEG_RX_5 — P47 PEG_RXP5
PEG_RX_6 — N43 PEG_RXP6
PEG_RX_7 — T42 PEG_RXP7
PEG_RX_8 — U42 PEG_RXP8
PEG_RX_9 — Y42 PEG_RXP9
PEG_RX_10 — W47 PEG_RXP10
PEG_RX_11 — Y37 PEG_RXP11
PEG_RX_12 — AA42 PEG_RXP12
PEG_RX_13 — AD36 PEG_RXP13
PEG_RX_14 — AC48 PEG_RXP14
PEG_RX_15 — AD40 PEG_RXP15

PEG_TXN[15:0] <17>

PEG_TX#_0	J41	C_PEG_TXN0	C103	.1u/10V_4	PEG_TXN0
PEG_TX#_1	M46	C_PEG_TXN1	C119	.1u/10V_4	PEG_TXN1
PEG_TX#_2	M47	C_PEG_TXN2	C125	.1u/10V_4	PEG_TXN2
PEG_TX#_3	M40	C_PEG_TXN3	C133	.1u/10V_4	PEG_TXN3
PEG_TX#_4	M42	C_PEG_TXN4	C105	E@.1u/10V_4	PEG_TXN4
PEG_TX#_5	R48	C_PEG_TXN5	C141	E@.1u/10V_4	PEG_TXN5
PEG_TX#_6	N38	C_PEG_TXN6	C154	E@.1u/10V_4	PEG_TXN6
PEG_TX#_7	T40	C_PEG_TXN7	C186	E@.1u/10V_4	PEG_TXN7
PEG_TX#_8	U37	C_PEG_TXN8	C197	E@.1u/10V_4	PEG_TXN8
PEG_TX#_9	U40	C_PEG_TXN9	C201	E@.1u/10V_4	PEG_TXN9
PEG_TX#_10	Y40	C_PEG_TXN10	C211	E@.1u/10V_4	PEG_TXN10
PEG_TX#_11	AA46	C_PEG_TXN11	C215	E@.1u/10V_4	PEG_TXN11
PEG_TX#_12	AA37	C_PEG_TXN12	C208	E@.1u/10V_4	PEG_TXN12
PEG_TX#_13	AA40	C_PEG_TXN13	C230	E@.1u/10V_4	PEG_TXN13
PEG_TX#_14	AD43	C_PEG_TXN14	C237	E@.1u/10V_4	PEG_TXN14
PEG_TX#_15	AC46	C_PEG_TXN15	C239	E@.1u/10V_4	PEG_TXN15

PEG_TXP[15:0] <17>

PEG_TX_0	J42	C_PEG_TXP0	C100	.1u/10V_4	PEG_TXP0
PEG_TX_1	L46	C_PEG_TXP1	C113	.1u/10V_4	PEG_TXP1
PEG_TX_2	M48	C_PEG_TXP2	C122	.1u/10V_4	PEG_TXP2
PEG_TX_3	M39	C_PEG_TXP3	C130	.1u/10V_4	PEG_TXP3
PEG_TX_4	M43	C_PEG_TXP4	C112	E@.1u/10V_4	PEG_TXP4
PEG_TX_5	R47	C_PEG_TXP5	C147	E@.1u/10V_4	PEG_TXP5
PEG_TX_6	N37	C_PEG_TXP6	C151	E@.1u/10V_4	PEG_TXP6
PEG_TX_7	T39	C_PEG_TXP7	C184	E@.1u/10V_4	PEG_TXP7
PEG_TX_8	U36	C_PEG_TXP8	C194	E@.1u/10V_4	PEG_TXP8
PEG_TX_9	U39	C_PEG_TXP9	C199	E@.1u/10V_4	PEG_TXP9
PEG_TX_10	Y39	C_PEG_TXP10	C202	E@.1u/10V_4	PEG_TXP10
PEG_TX_11	Y46	C_PEG_TXP11	C213	E@.1u/10V_4	PEG_TXP11
PEG_TX_12	AA36	C_PEG_TXP12	C207	E@.1u/10V_4	PEG_TXP12
PEG_TX_13	AA39	C_PEG_TXP13	C221	E@.1u/10V_4	PEG_TXP13
PEG_TX_14	AD42	C_PEG_TXP14	C232	E@.1u/10V_4	PEG_TXP14
PEG_TX_15	AD46	C_PEG_TXP15	C243	E@.1u/10V_4	PEG_TXP15

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 976 ohm to GND (>12")

CRTIREF
For IV: 1.02Kohm
For EV:0ohm

R72 SP@1K/F_4 CRTIREF

SP@

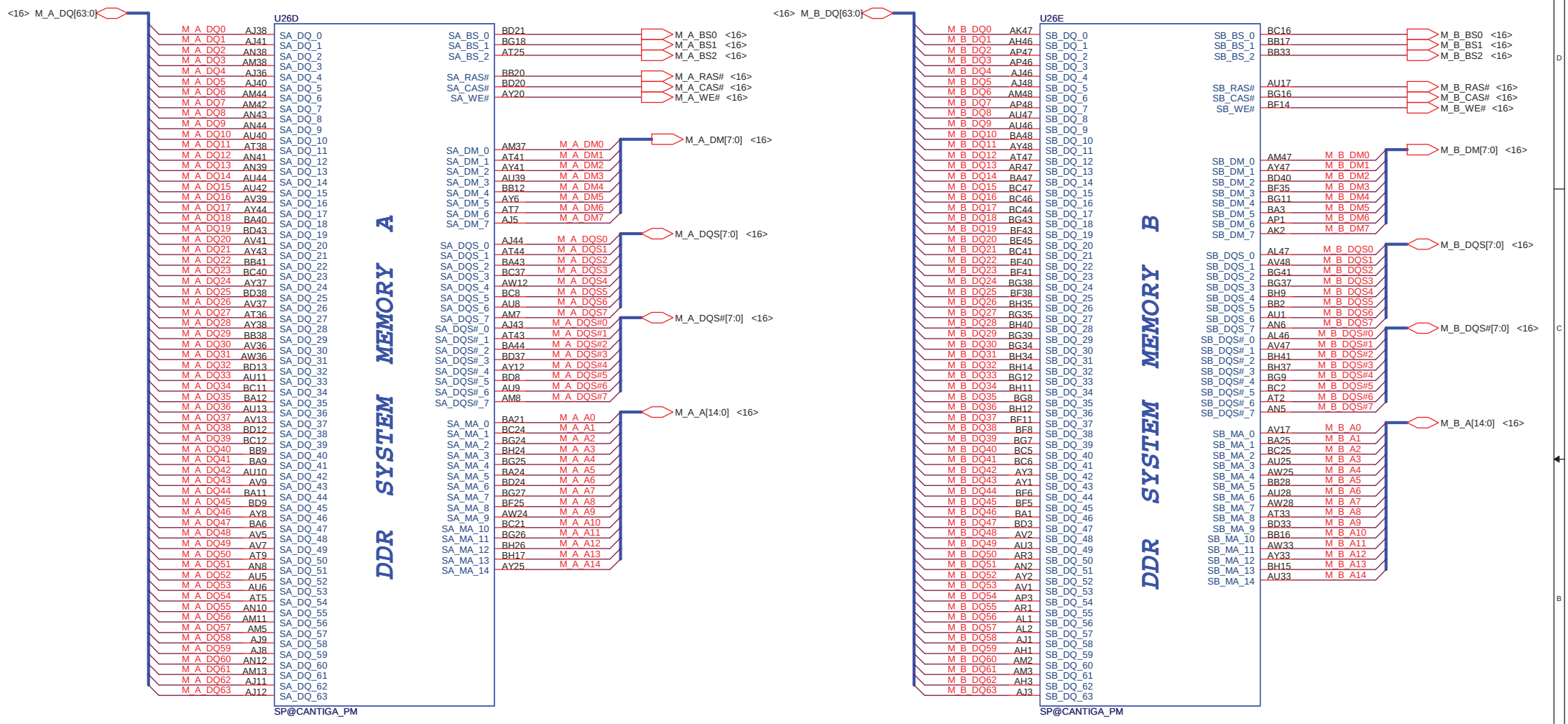
CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R73 SP@150_4 INT_CRT_BLU
R83 SP@150_4 INT_CRT_GRN
R88 SP@150_4 INT_CRT_RED

MXM STUFFED.

INT_HSYNC — R82 E@0_4
INT_VSYNC — R80 E@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F



GMCH (CANTIGA)

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PROJECT : ZK6

Size	Document Number	Rev
	GMCH DDRIII	1A

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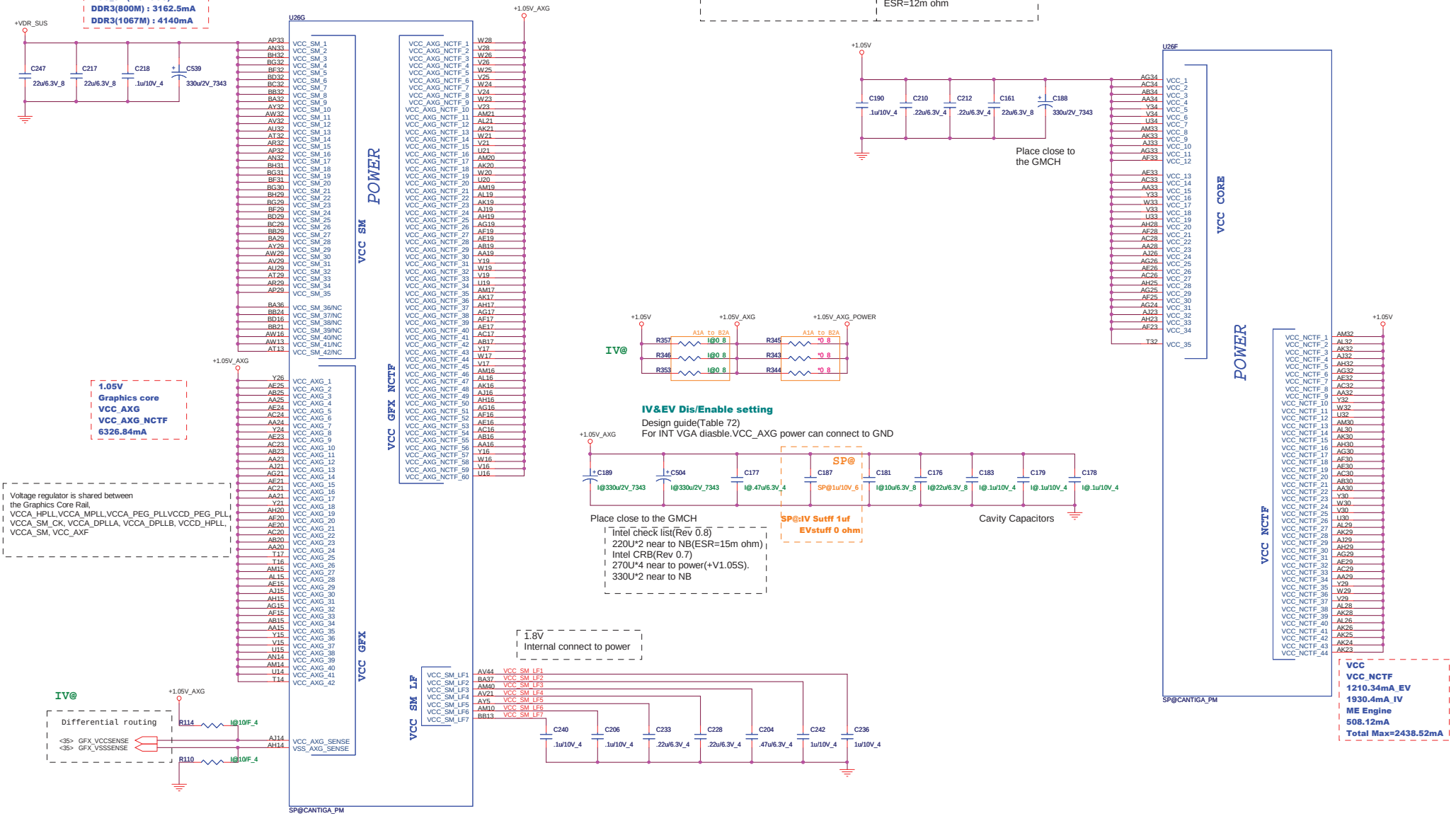
IV@

SP@

VCC_SM(1.5VSUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm



1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

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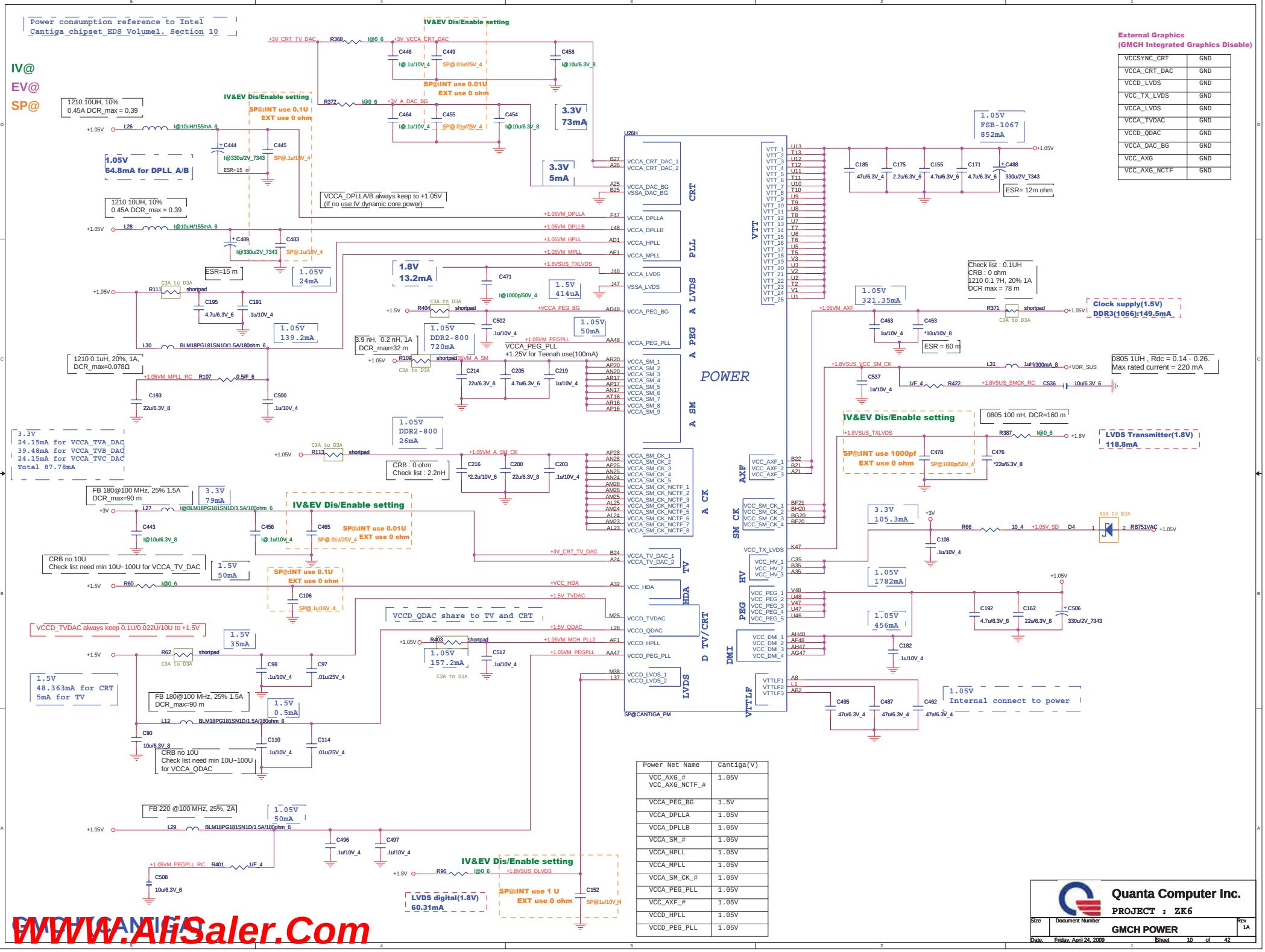

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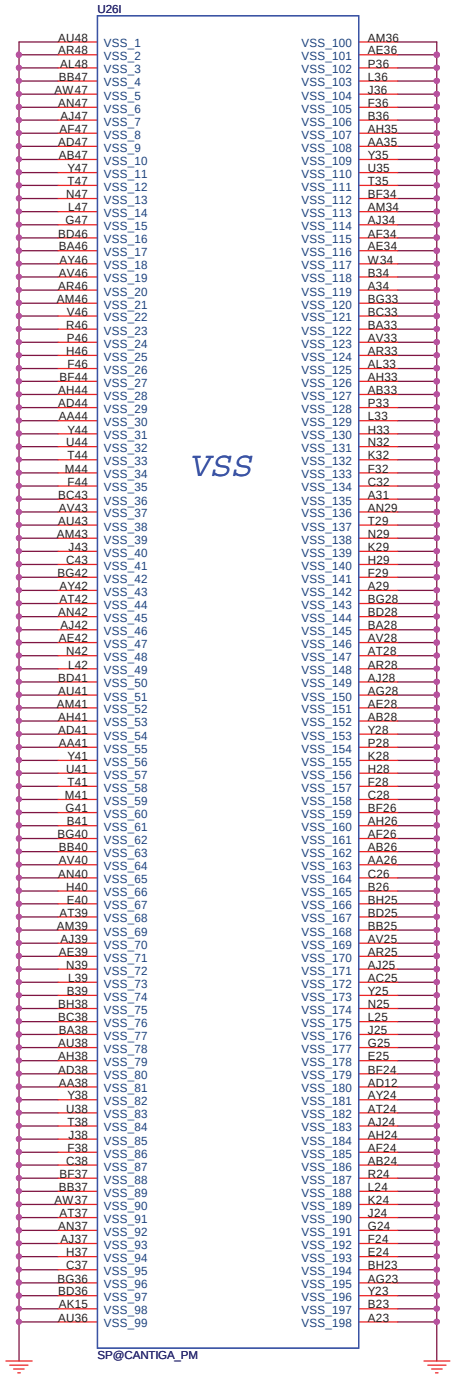
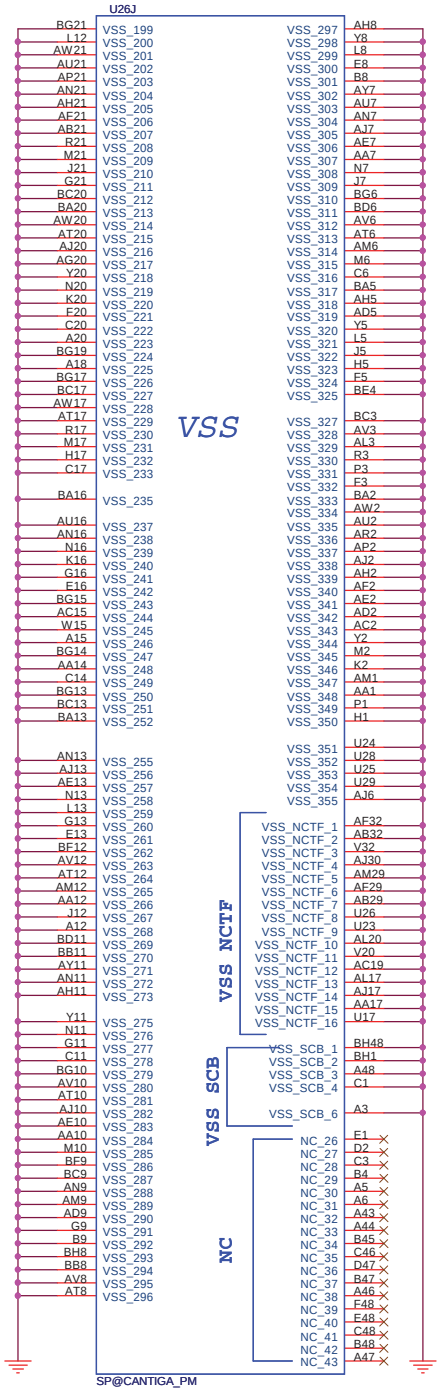




GMCH (CANTIGA)

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	GMCH VSS	1A

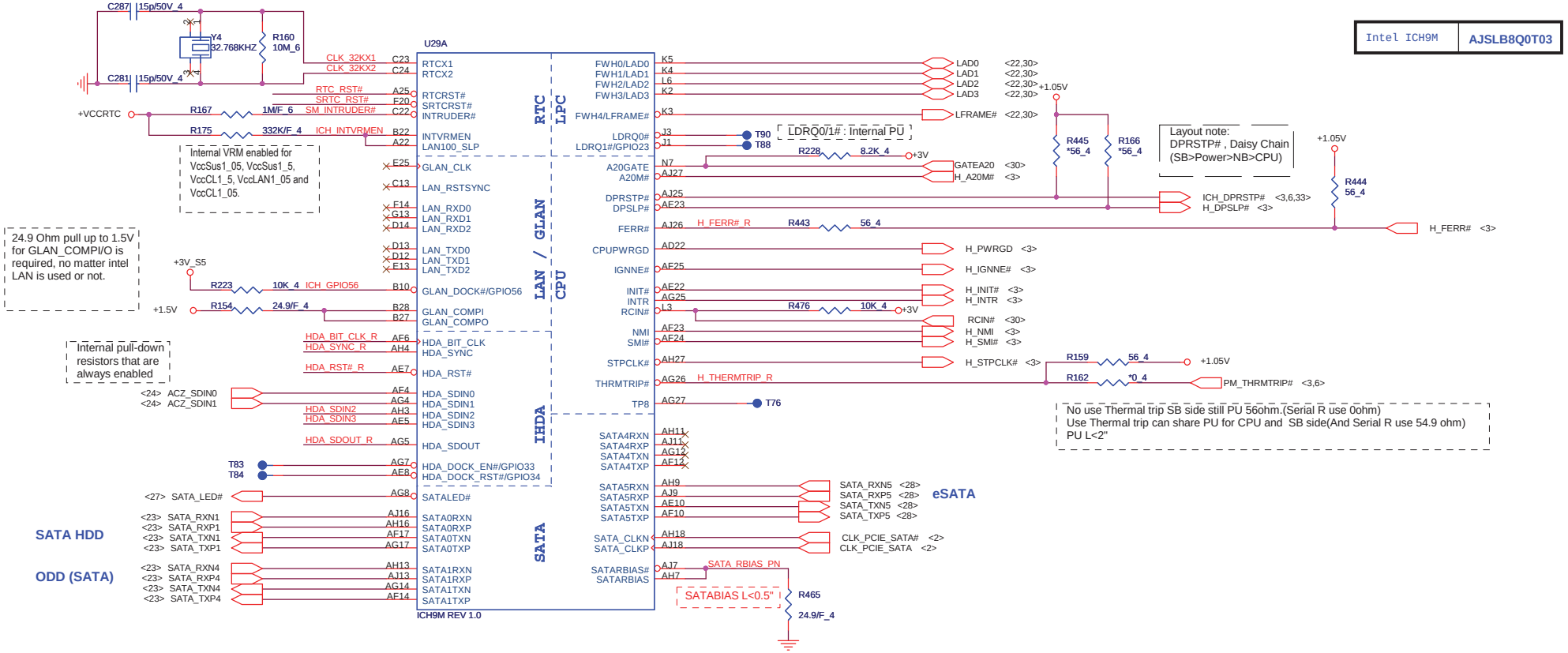
Date: Friday, April 24, 2009 Sheet 11 of 42

ICH9M

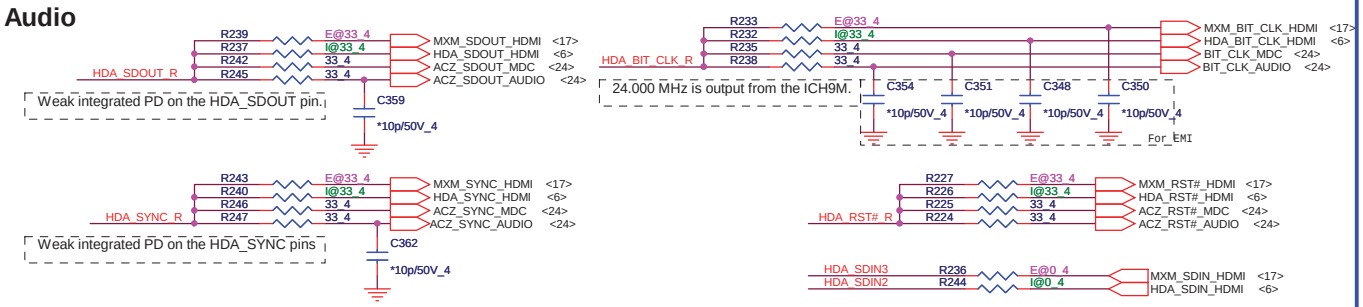
IV@

EV@

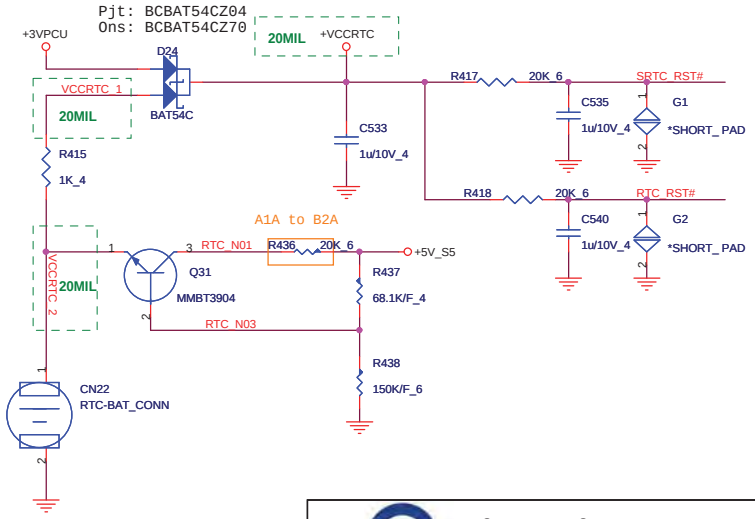
Intel ICH9M	AJSLB8Q0T03



HD Audio



RTC



South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT / Description 0 / 0 / RSVD 0 / 1 / Enter XOR Chain 1 / 0 / Normal opration(Default) 1 / 1 / Set PCIE port config bit 1	<14> ICH_TP3 ICH_TP3 R182 *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R R234 *1K_4 +3V

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PROJECT : ZK6

Size	Document Number	Rev
	ICH9M HOST	1A

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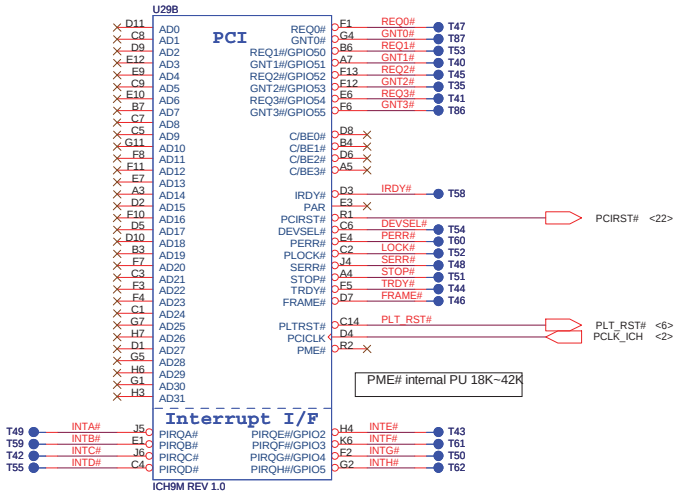
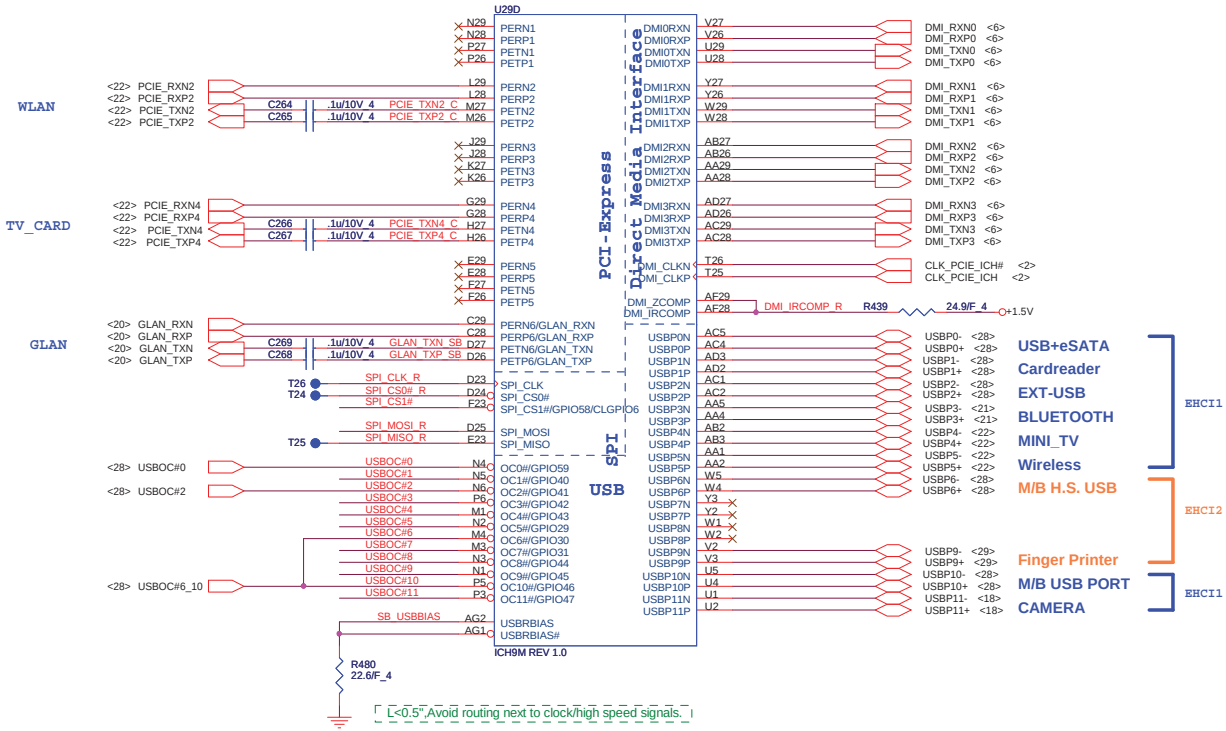
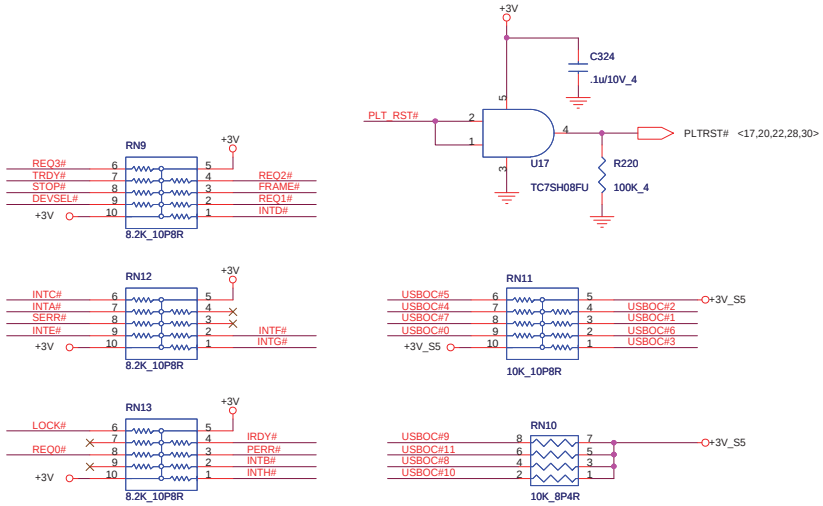
ICH9M







South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R485 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI_R R156 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI	GNT0# R486 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 1 / 0 / PCI 1 / 1 / **LPC(Default)**	SPI_CS1# R177 *1K_4

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	ICH9M PCIE / PCI / USB	1A

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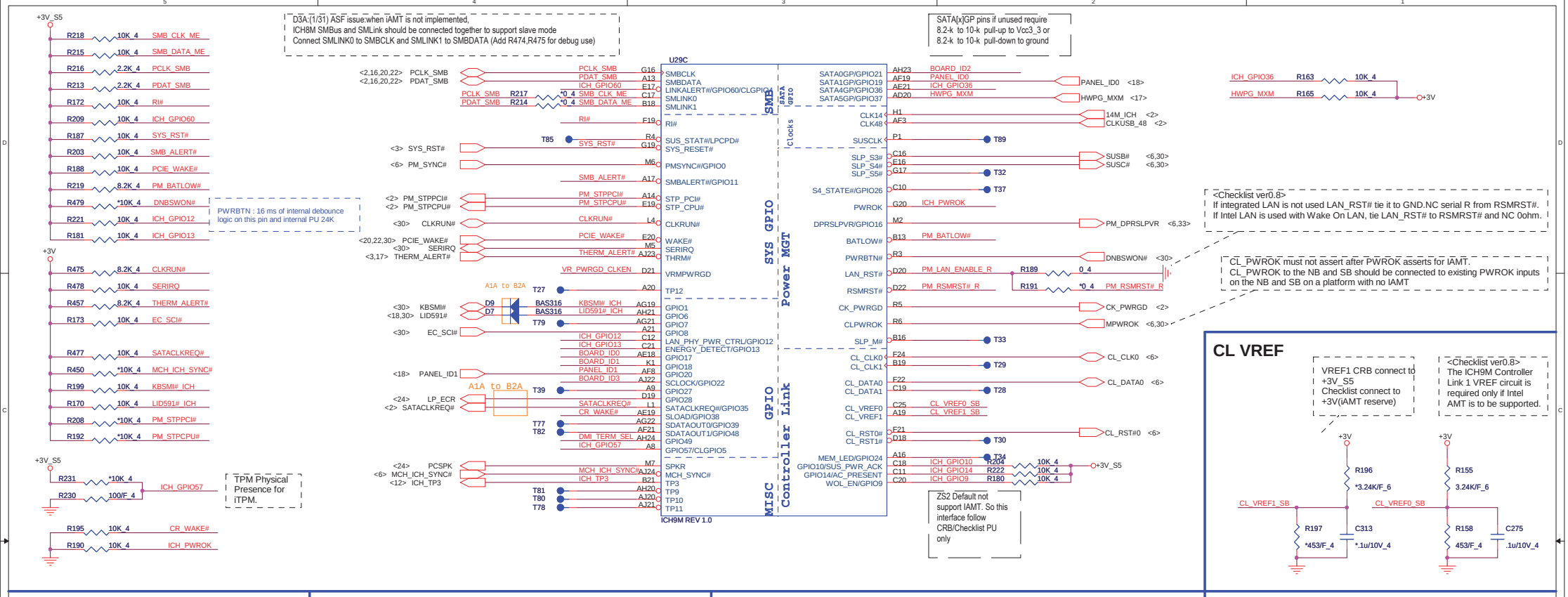
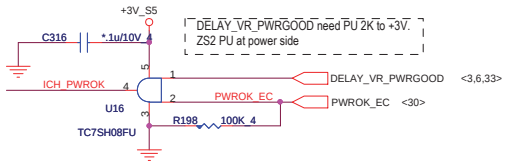
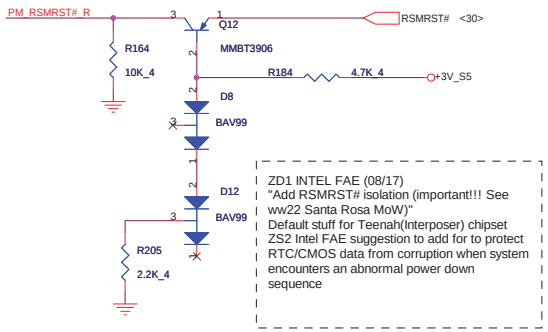


ICH PWROK

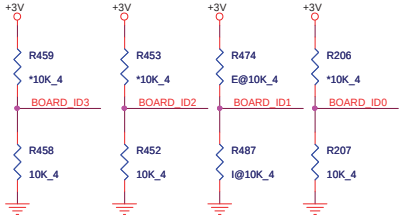


Resume RST



M/B ID

ID0 :: ZK=0 , ZR=1
ID1 :: UMA=0 , MXM=1

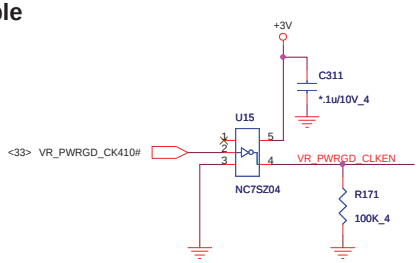


Board ID	ID3	ID2	ID1	ID0
default	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R229 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R446 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	ICH9M GPIO	1A

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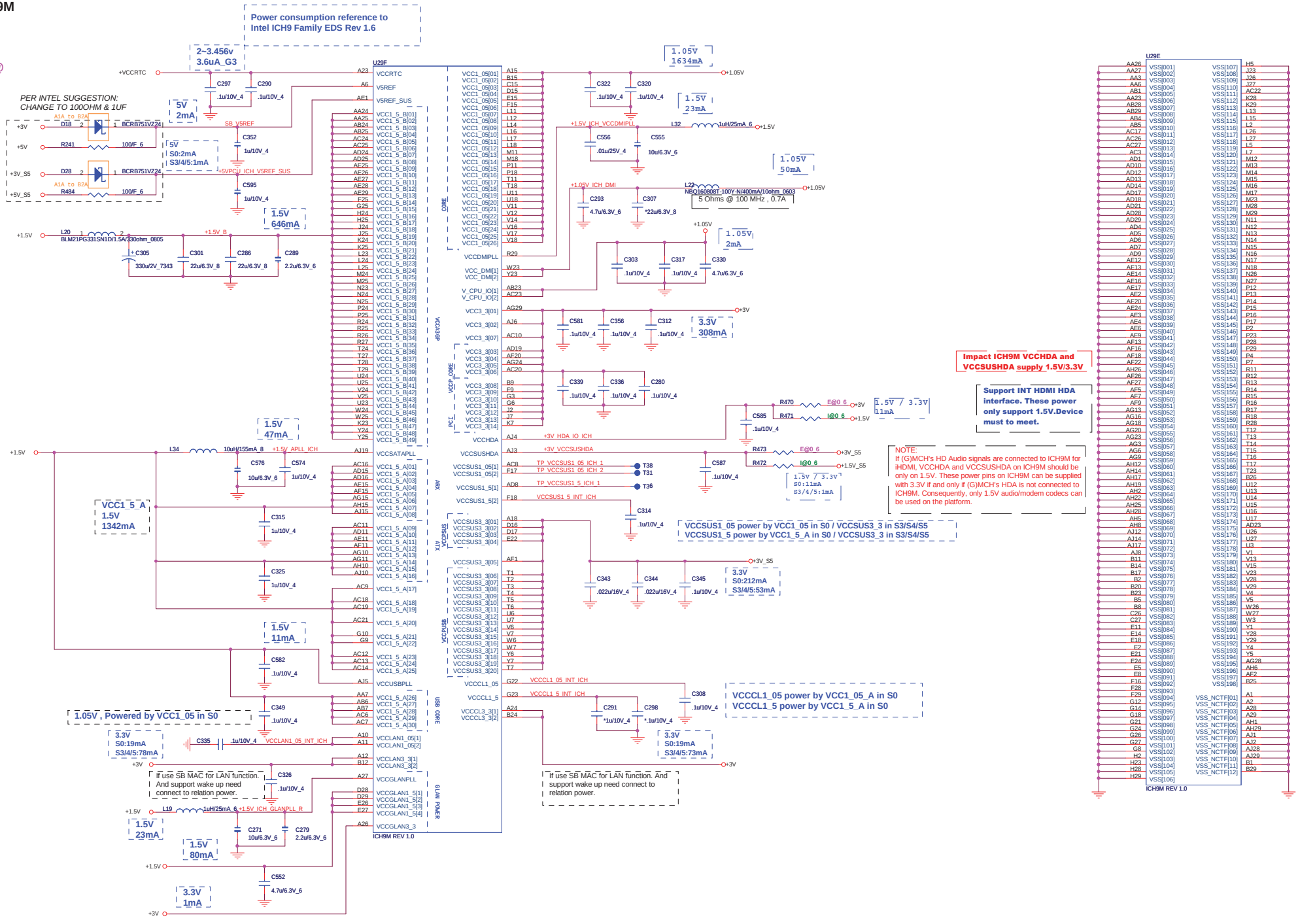
ICH9M

IV@

EV@



Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	ICH9 POWER	1A

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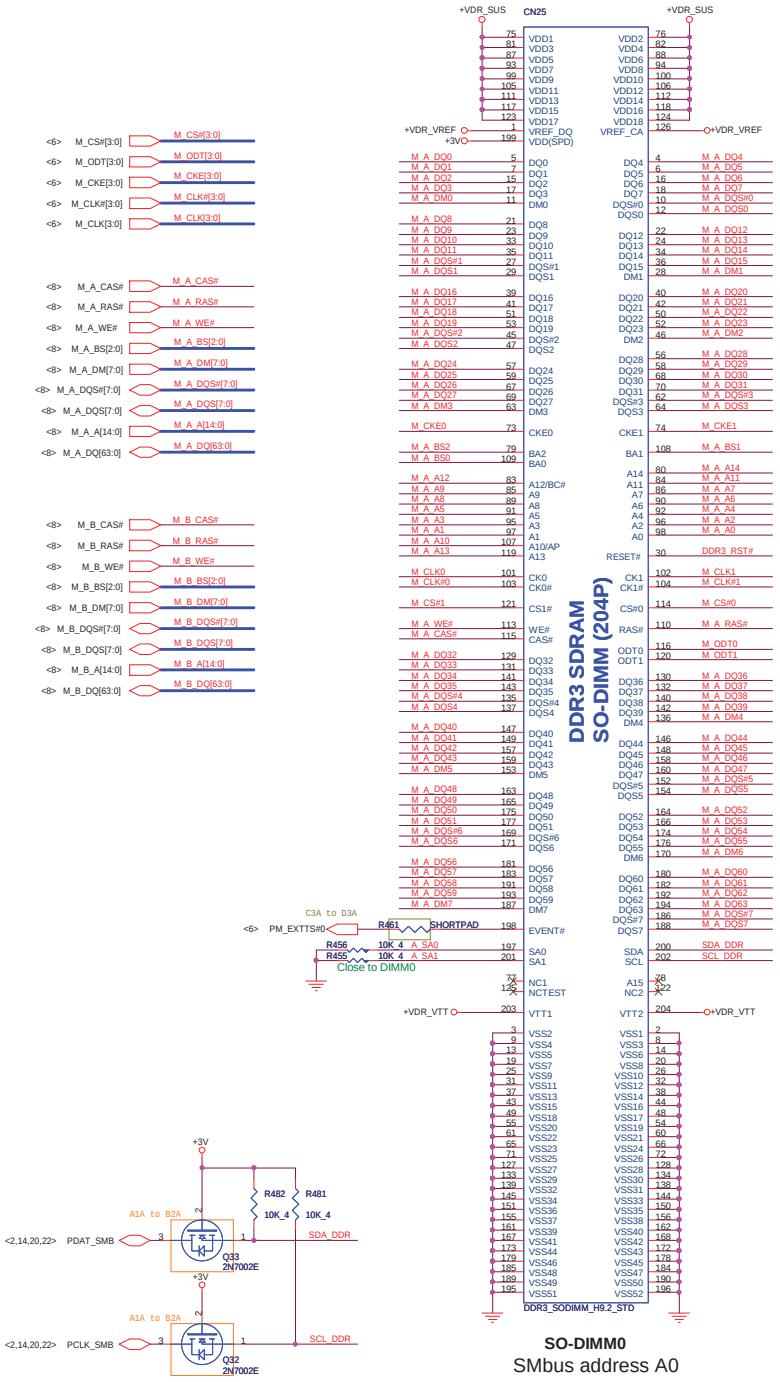
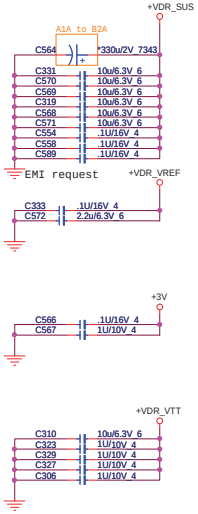
H=9.2mm / DGMK4000058



Decoupling capacitor

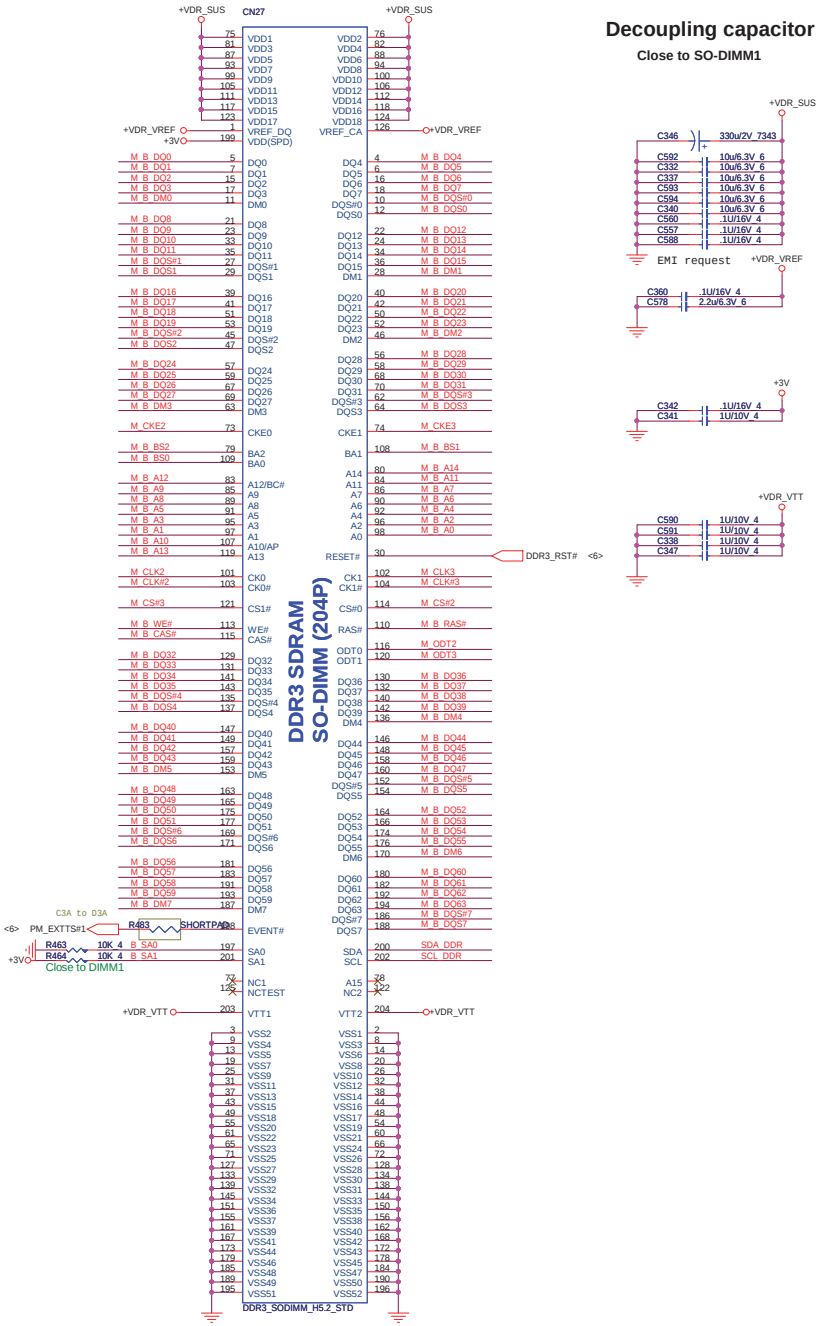
Close to SO-DIMM0



SO-DIMM0

SMbus address A0

H=5.2mm / DGMK4000059



Decoupling capacitor

Close to SO-DIMM1

SO-DIMM1

SMbus address A2

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	DDRIII SO-DIMM	1A

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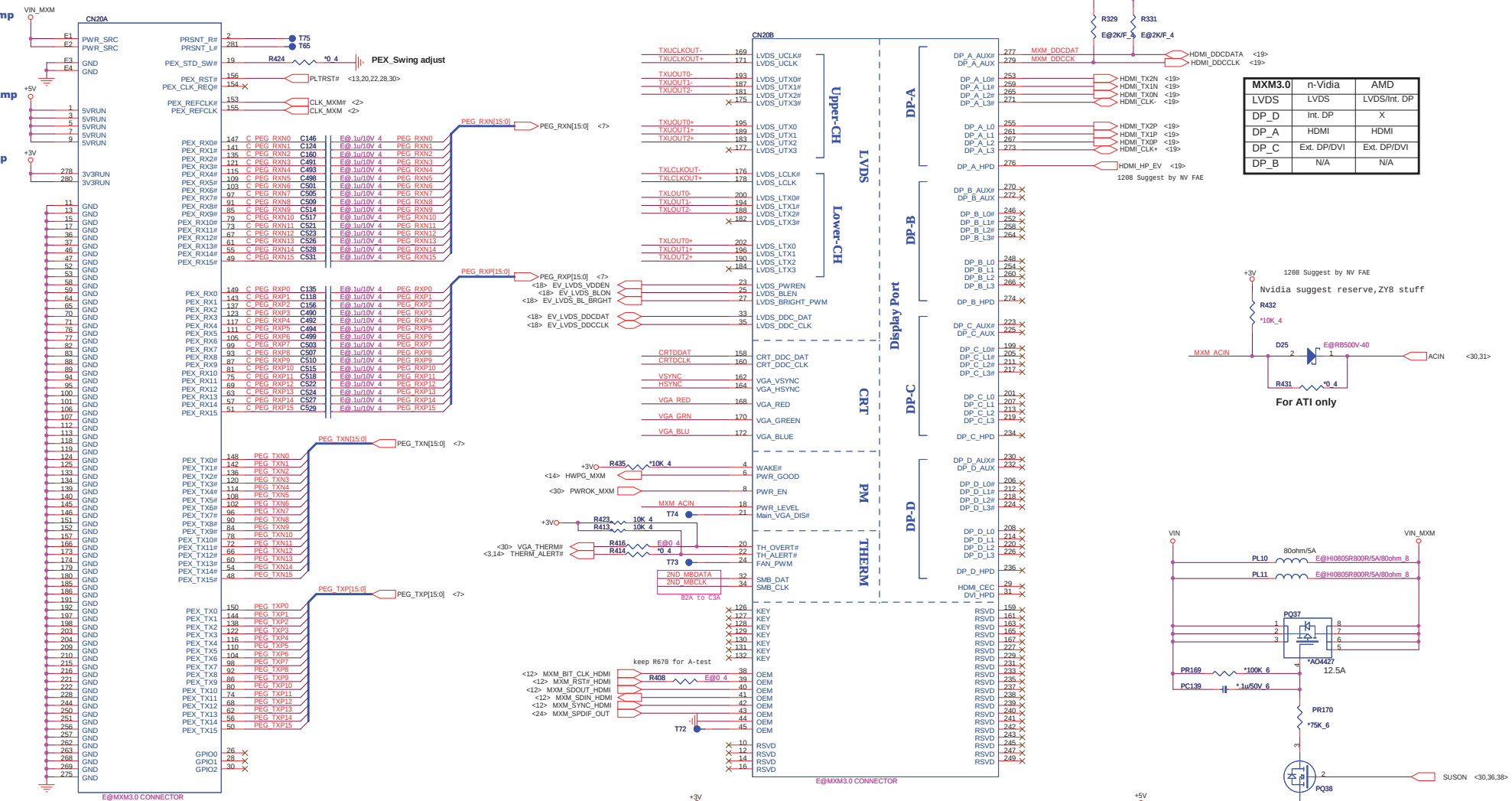
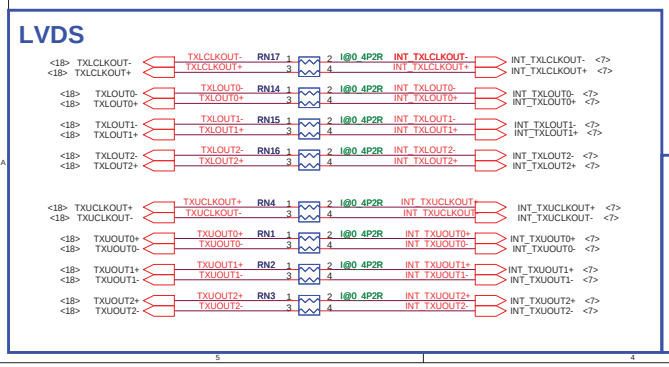
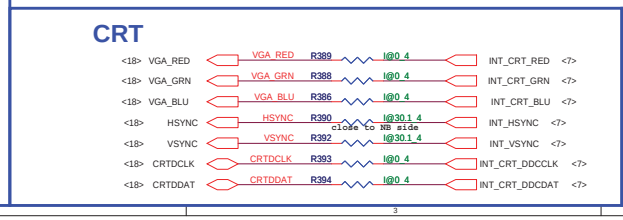
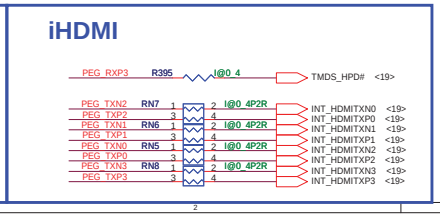
MXM Module



MXM3.0	n-Vidia	AMD
LVDS	LVDS	LVDS/Int. DP
DP_D	Int. DP	X
DP_A	HDMI	HDMI
DP_C	Ext. DP/DVI	Ext. DP/DVI
DP_B	N/A	N/A







Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	MXM3.0	1A

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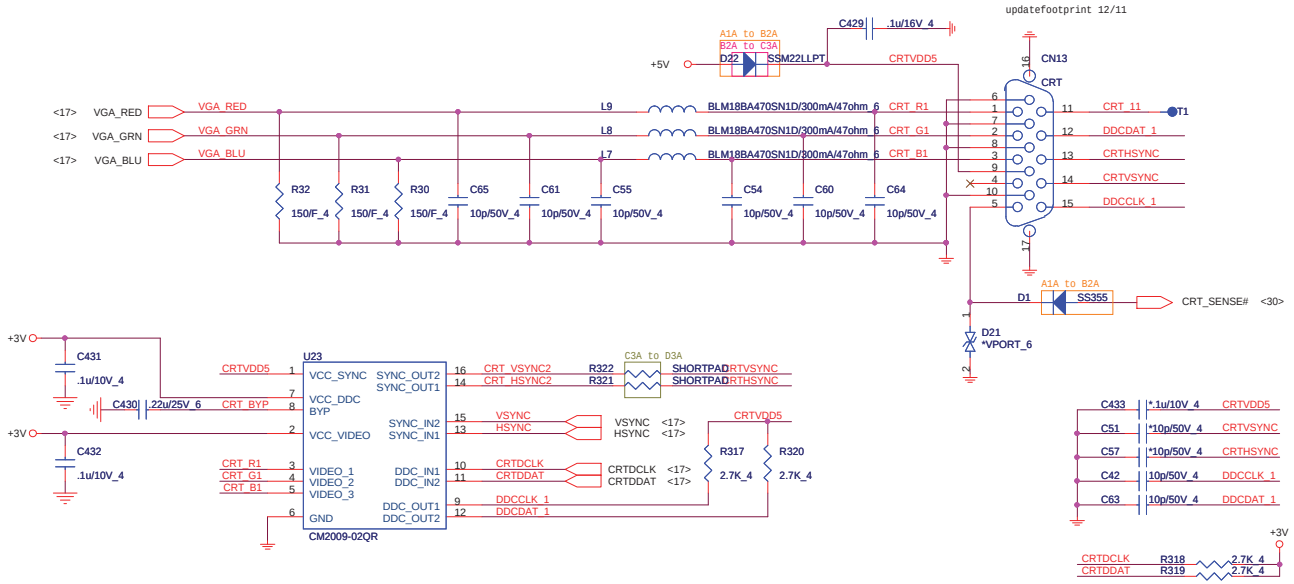
CRT

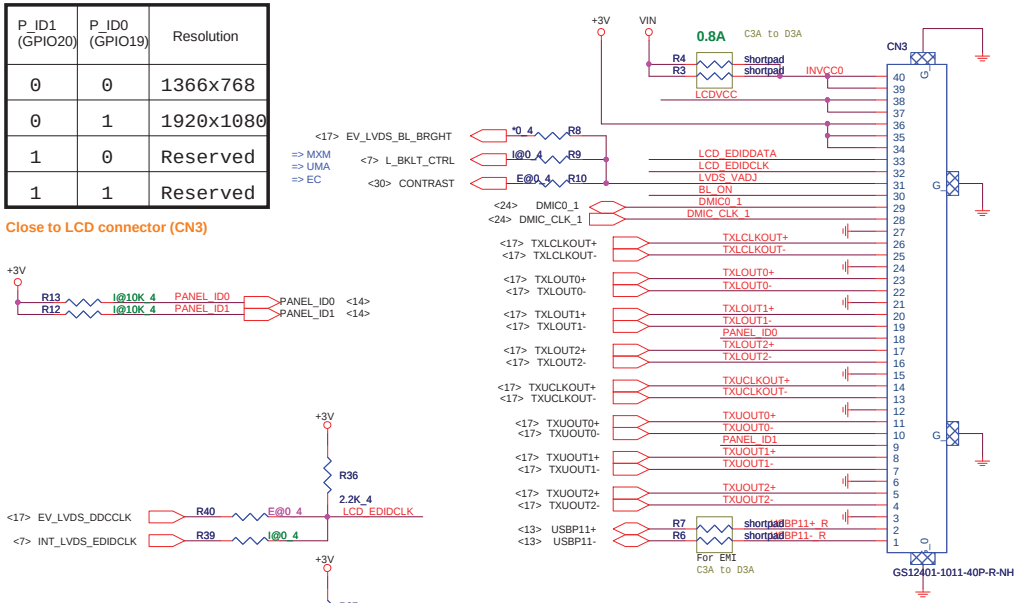
IV@
EV@



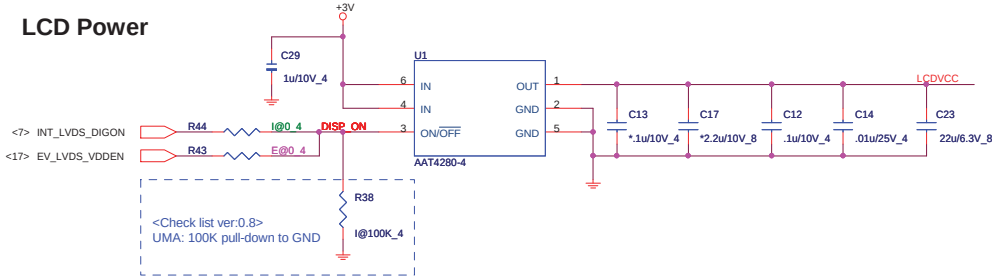
LVDS Panel ID (UMA only)

P_ID1 (GPIO20)	P_ID0 (GPIO19)	Resolution
0	0	1366x768
0	1	1920x1080
1	0	Reserved
1	1	Reserved

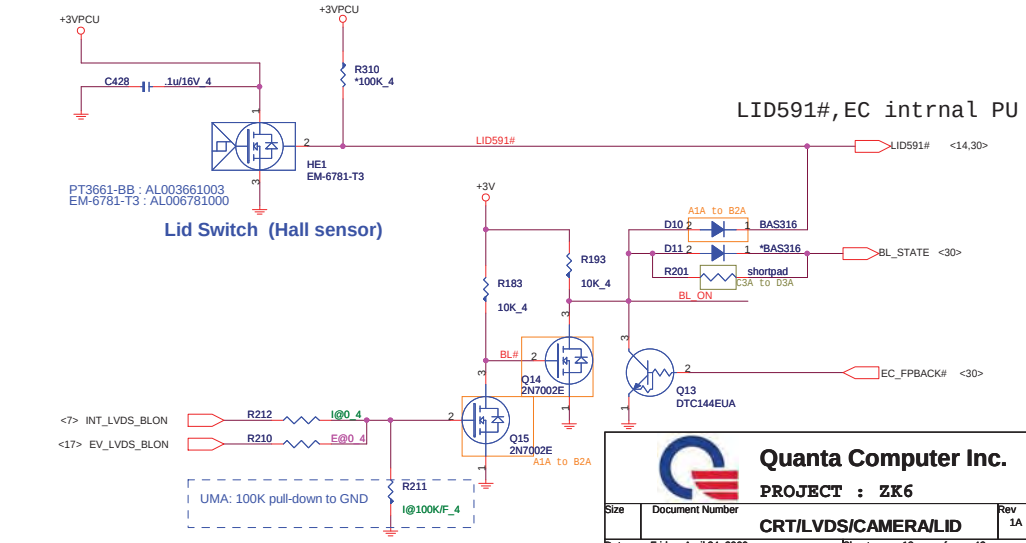
Close to LCD connector (CN3)



LCD Power



Backlight Control & LID



Quanta Computer Inc.
PROJECT : ZK6

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

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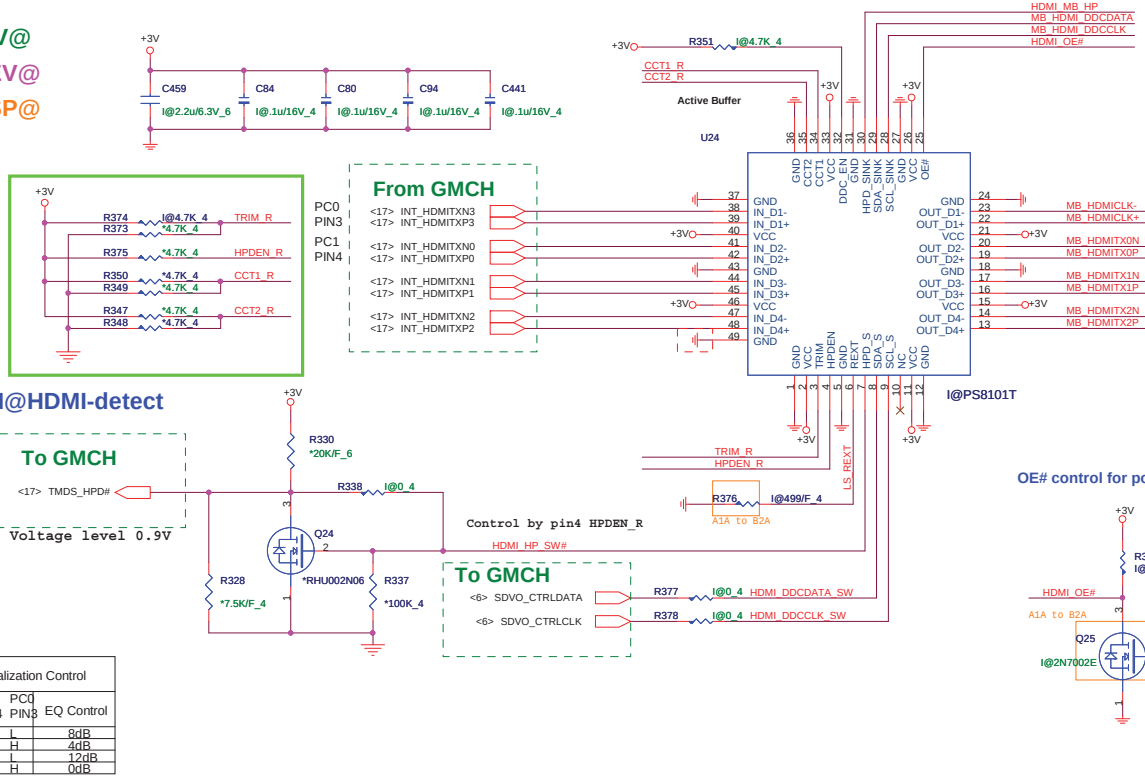
CH7318C :: AL007318002
PS8101T :: AL008101001

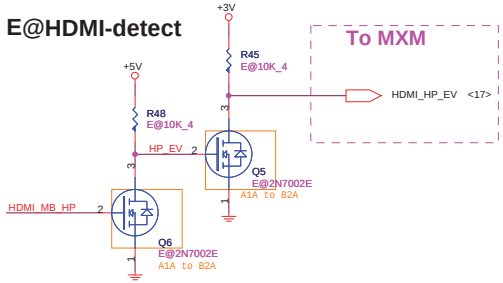
I@ HDMI LEVEL SHIFTER

IV@
EV@
SP@

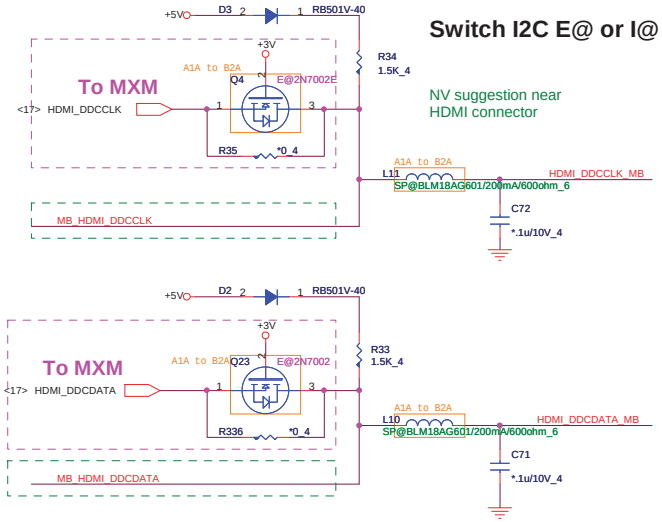


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

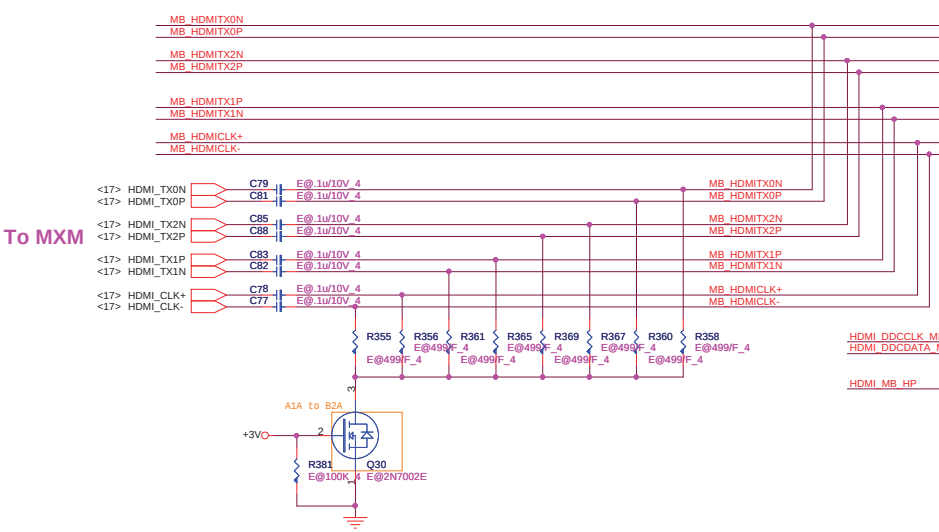
E@HDMI-detect



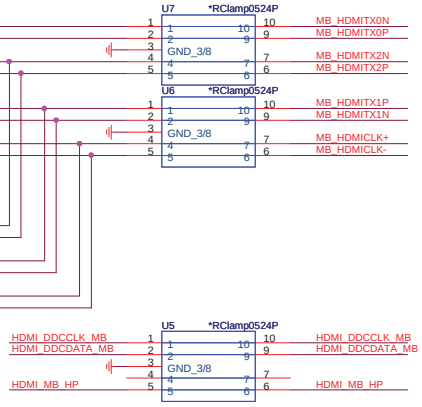
Switch I2C E@ or I@



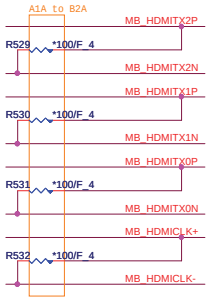
Switch E@ or I@



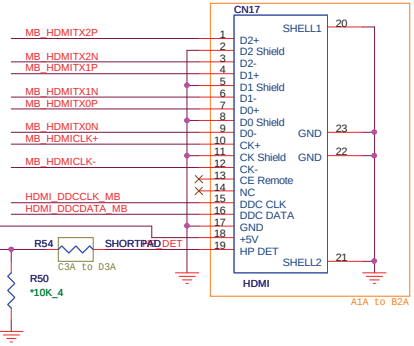
ESD Protect



EMI



HDMI connector



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	HDMI (CH7318C)	1A

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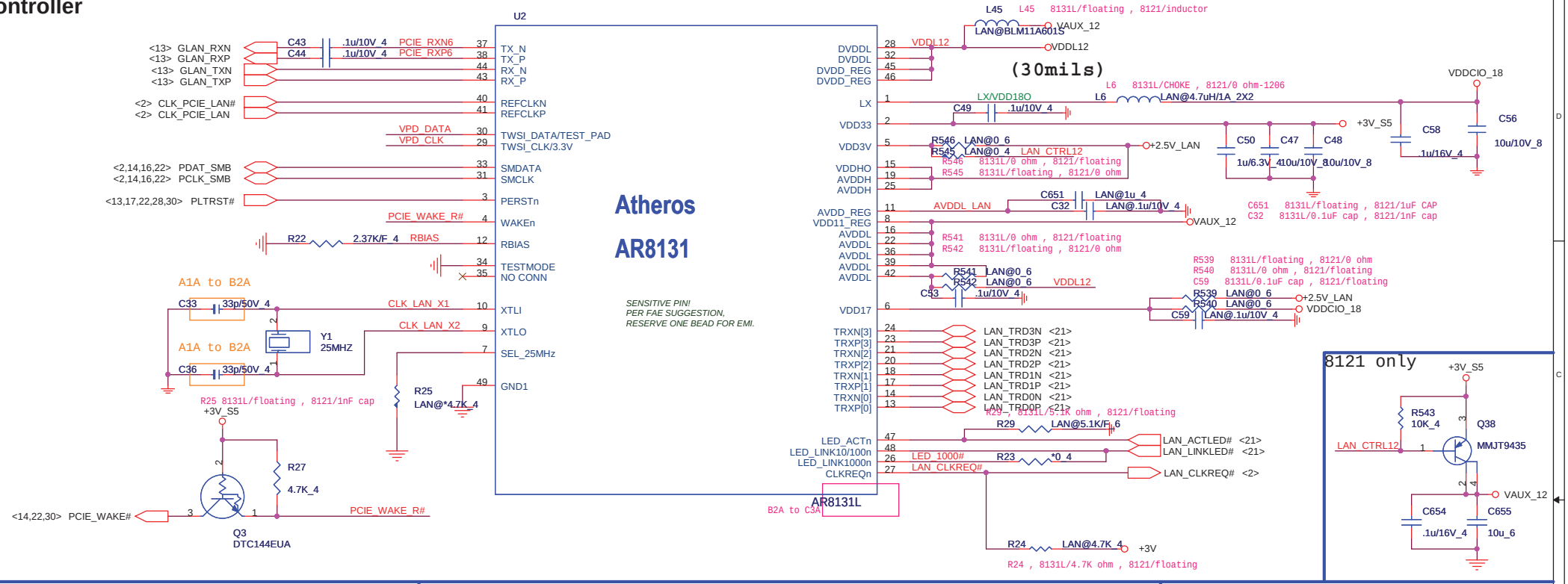
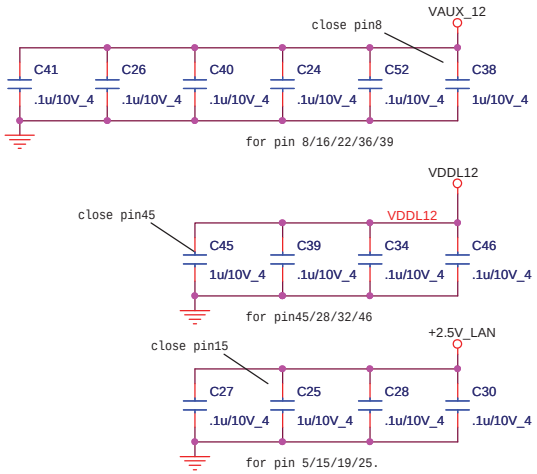
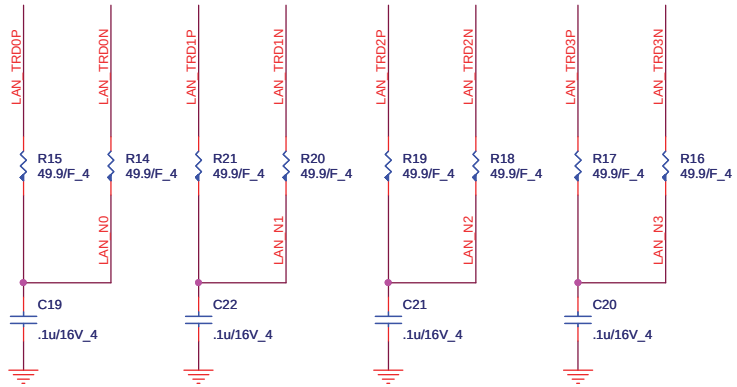
LAN Controller



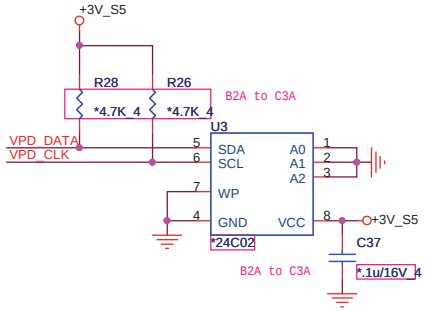
Decoupling CAP



PLACE NEAR IC SIDE



EEPROM



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	AR8131 GLAN	1A

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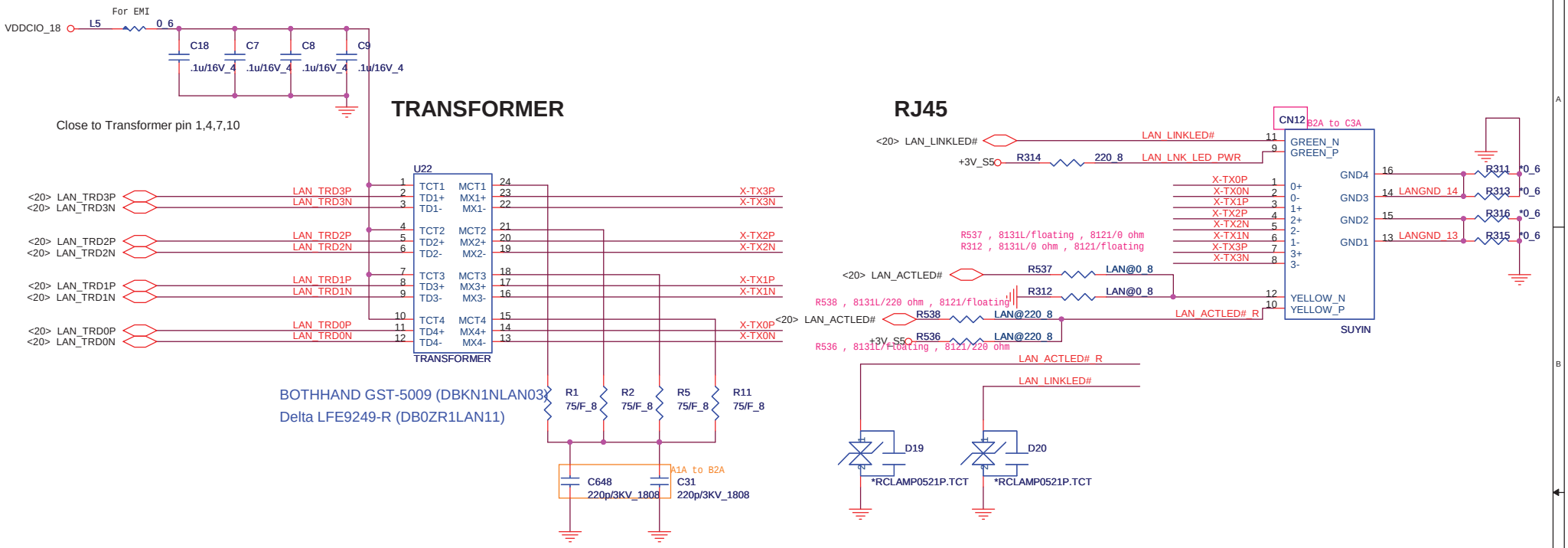
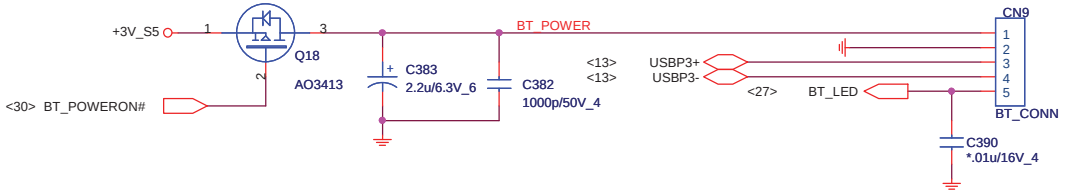


BLUETOOTH CONNECTOR



Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number LAN Transformer and RJ45/BT	Rev 1A
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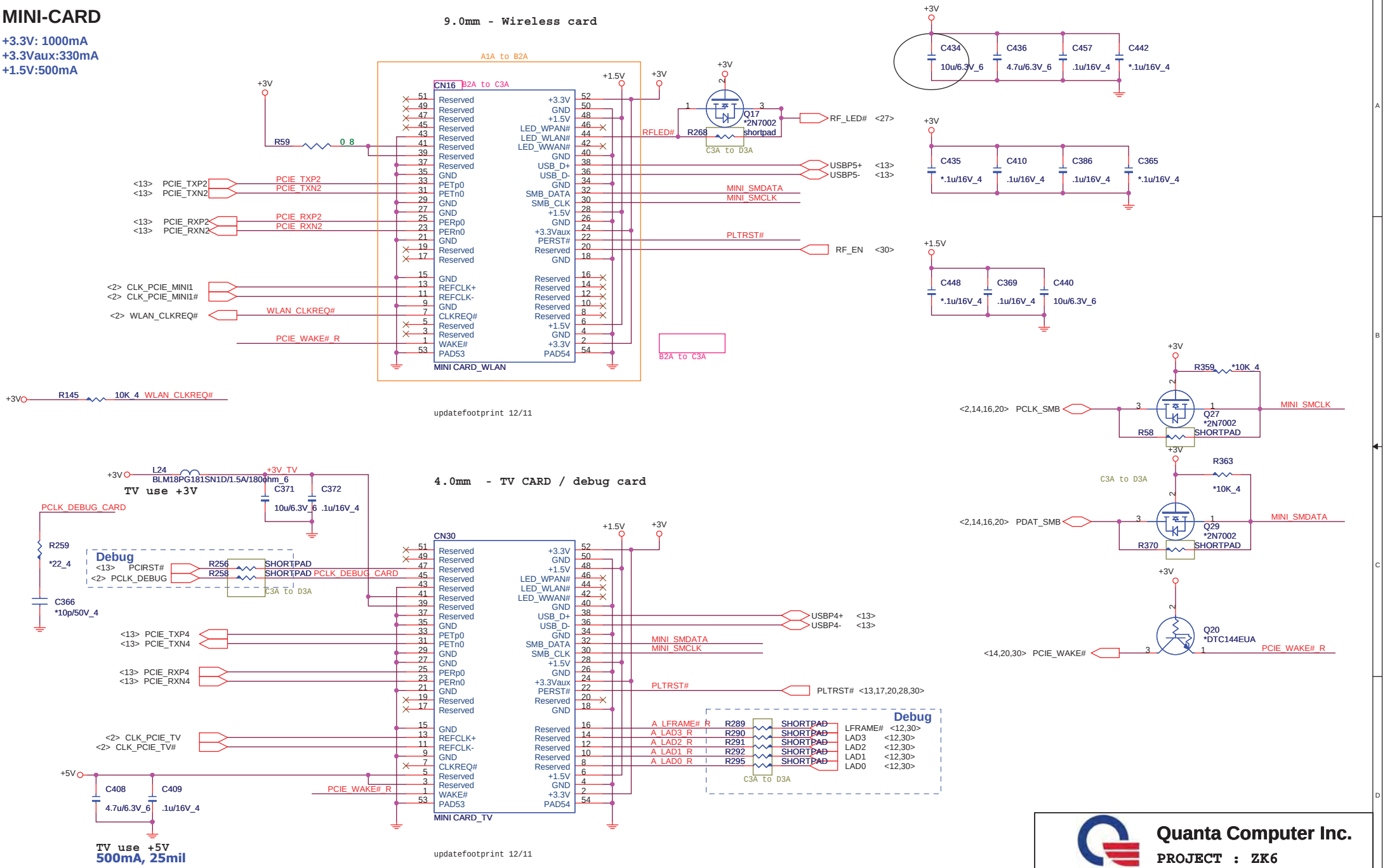
MINI-CARD

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

9.0mm - Wireless card



4.0mm - TV CARD / debug card

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PROJECT : ZK6

Size	Document Number	Rev
	MINI PCI-E card/TV	1A

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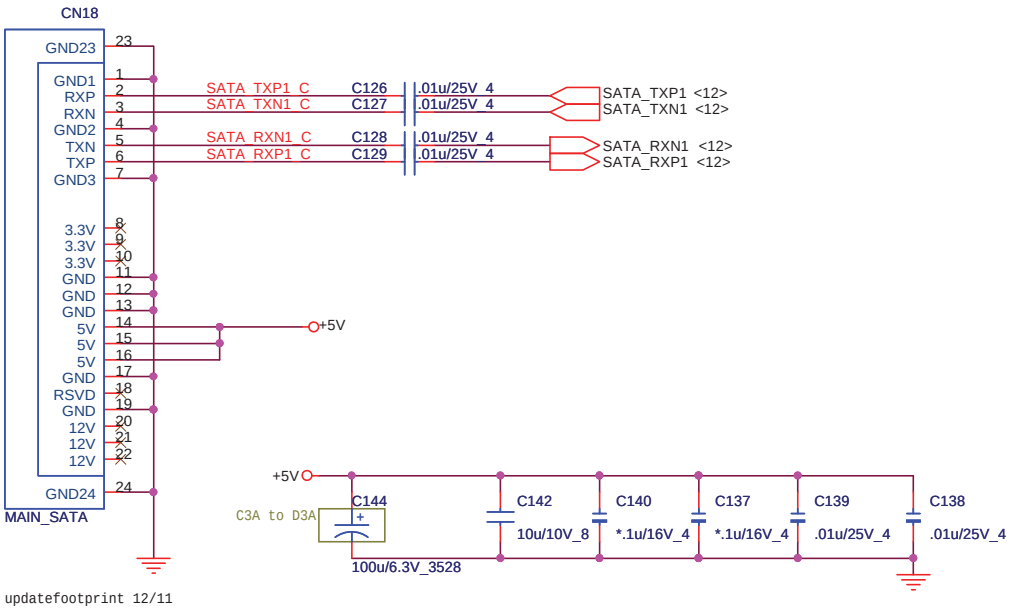
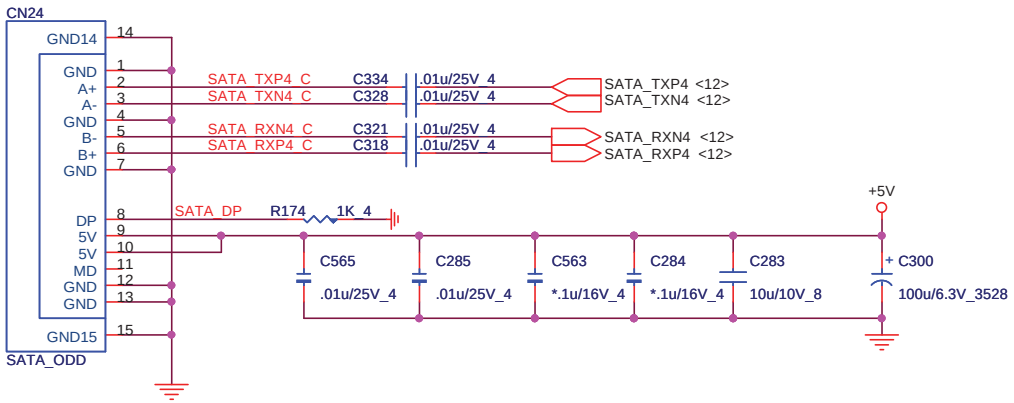
MAIN SATA HDD



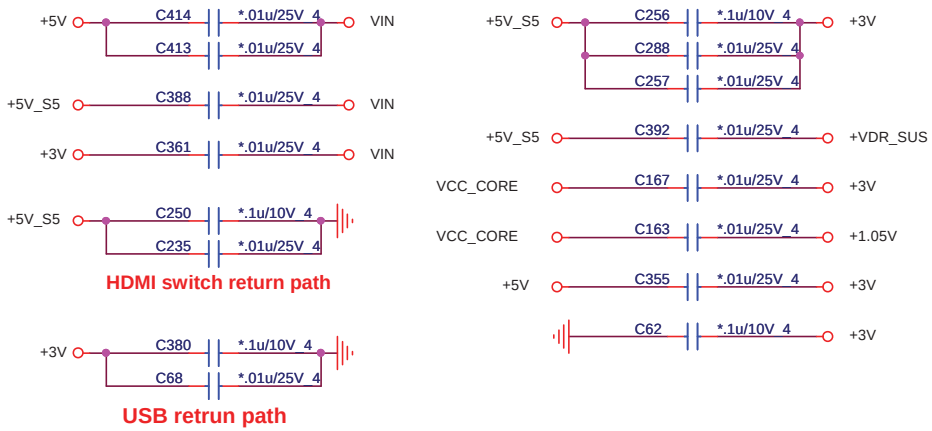
updatefootprint 12/11

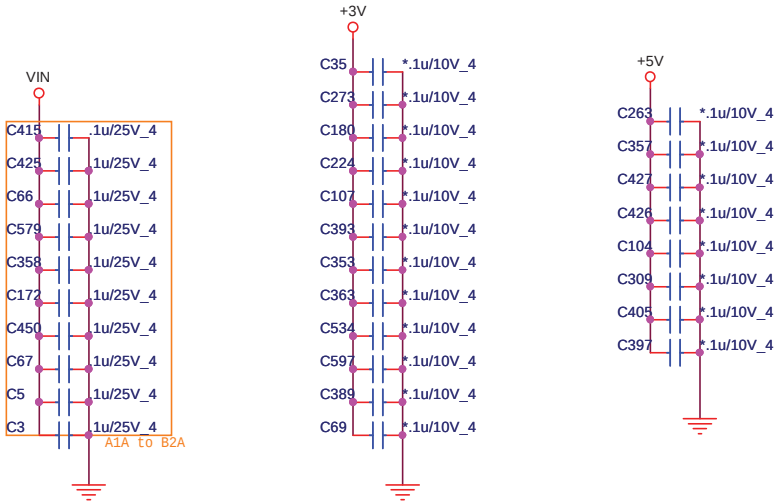
ODD (SATA)



updatefootprint 12/11

EE RETURN-PATH CAPACITORS





Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

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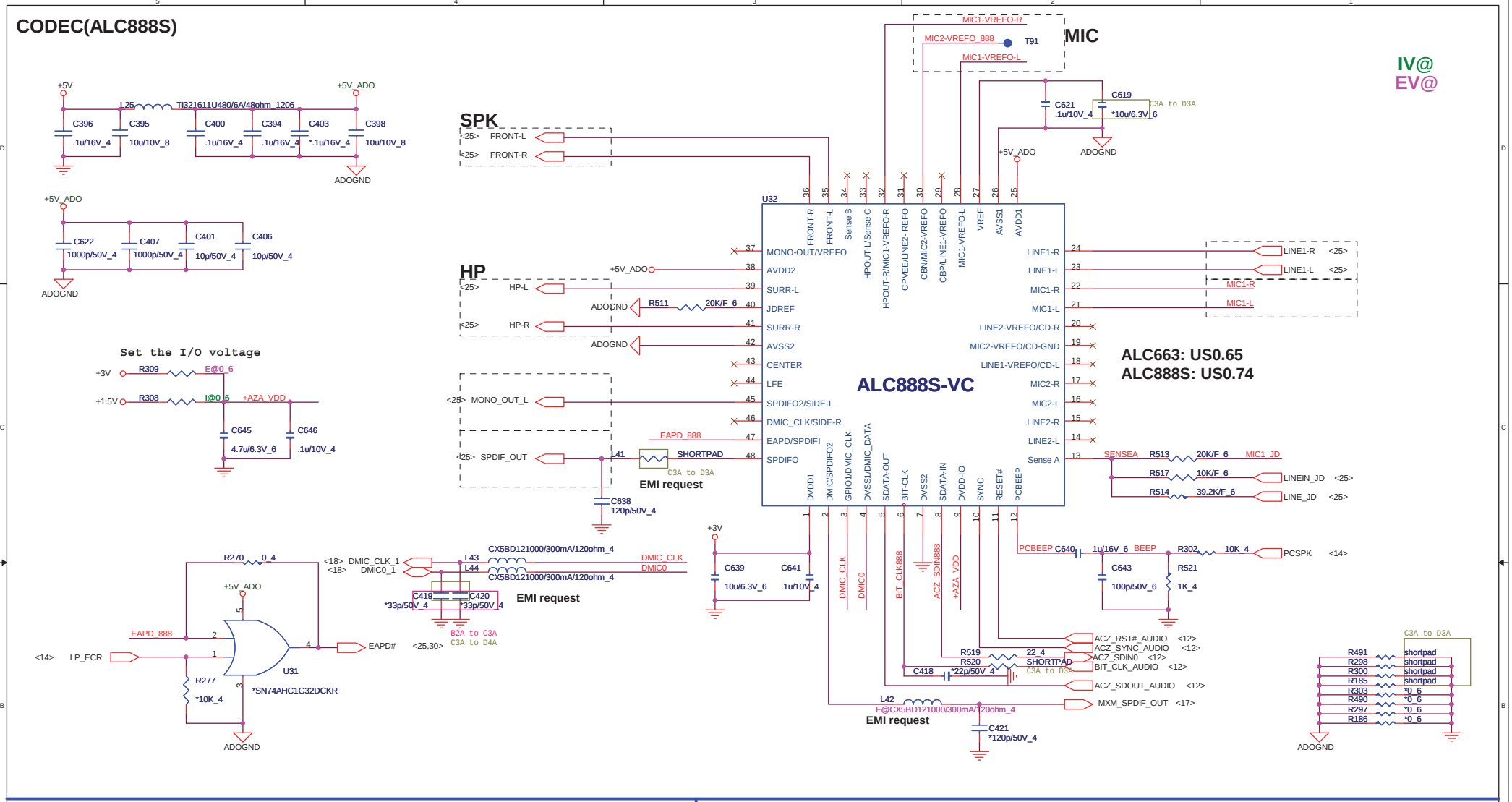
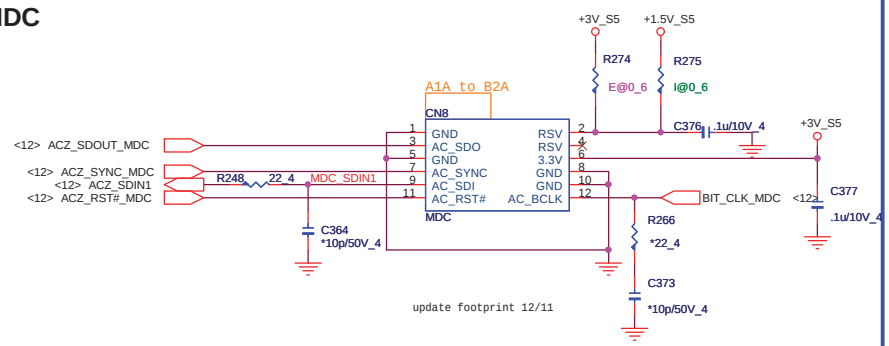
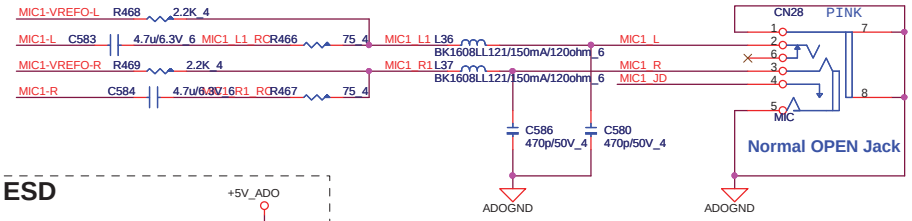
CODEC(ALC888S)



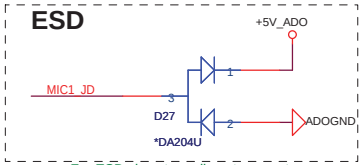
MDC



MIC



ESD



For ESD close to audio out connecter

CODEC & MDC

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PROJECT : ZK6

Size	Document Number	Rev
	REALTEK ALC663&888/MDC	1A

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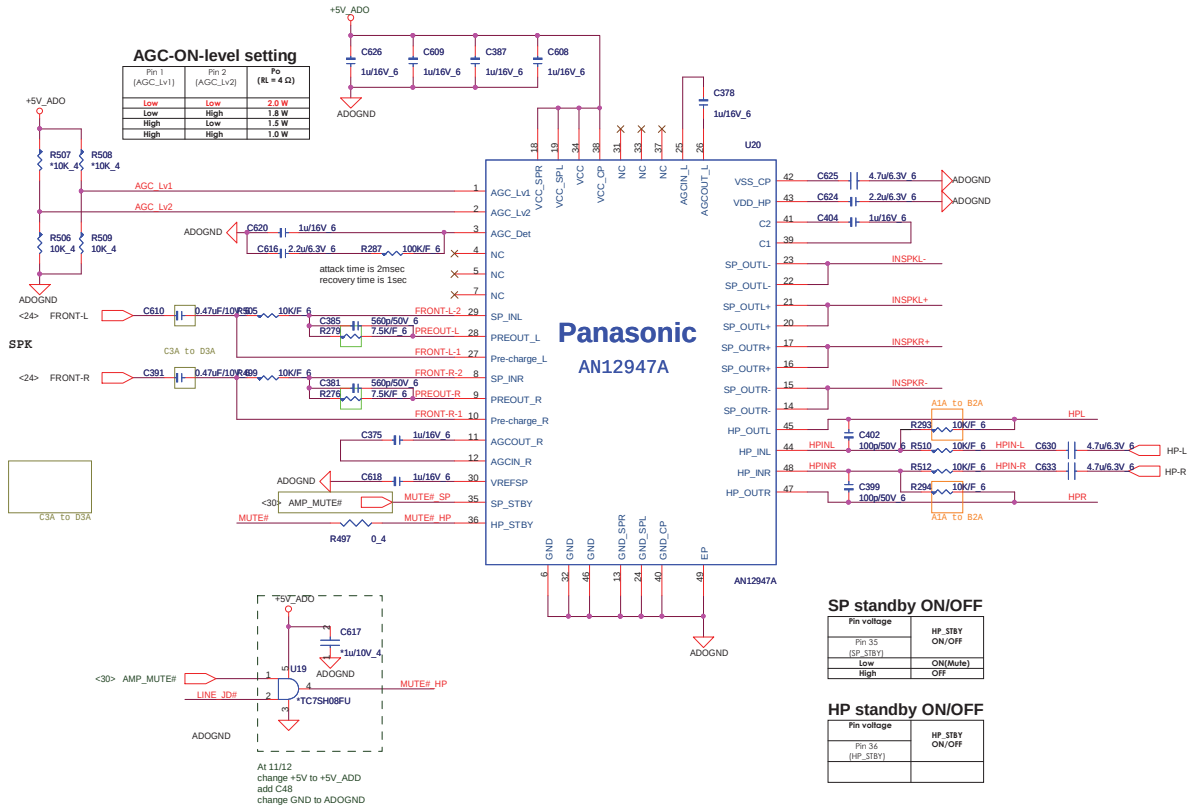
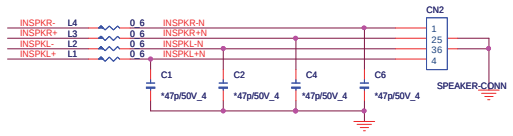
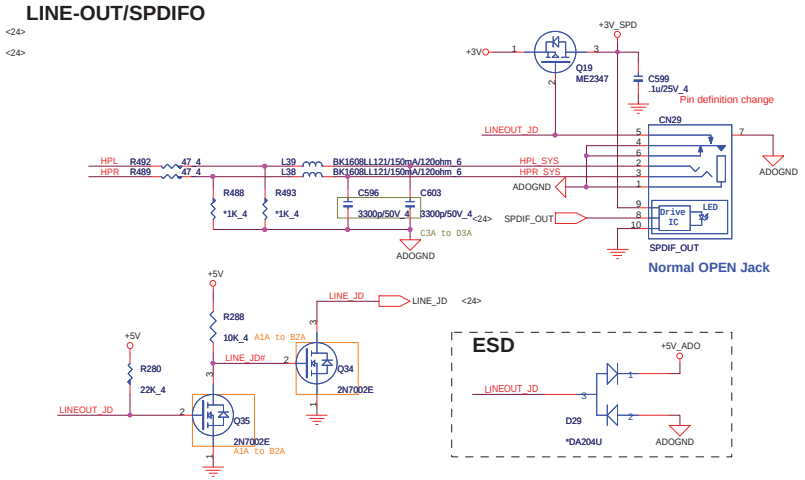
SPEAKER/HP AMP.



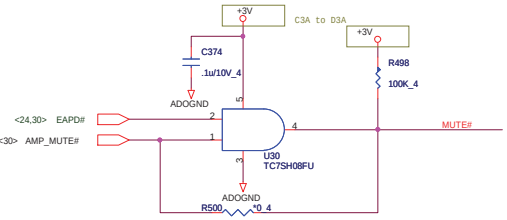
SPEAKER



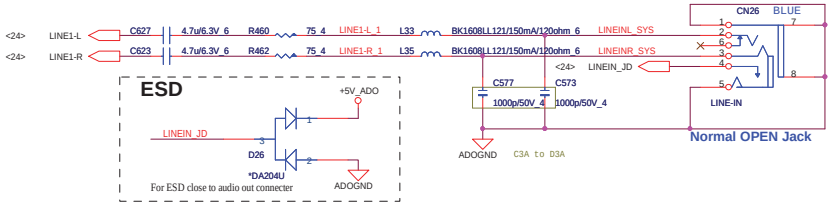
LINE-OUT/SPDIFO



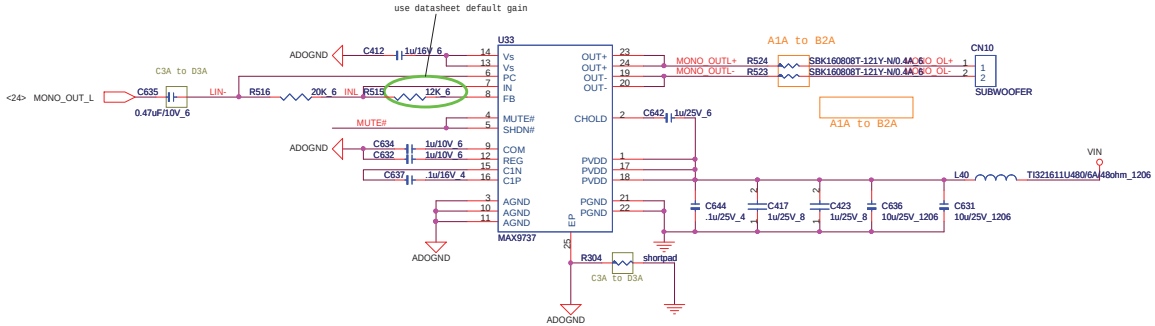
MUTE



LINE IN



SUBWOOFER



AMP& PHONE JACK & SUBWOOFER

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A

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Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	CARD READER RTS5159	1A

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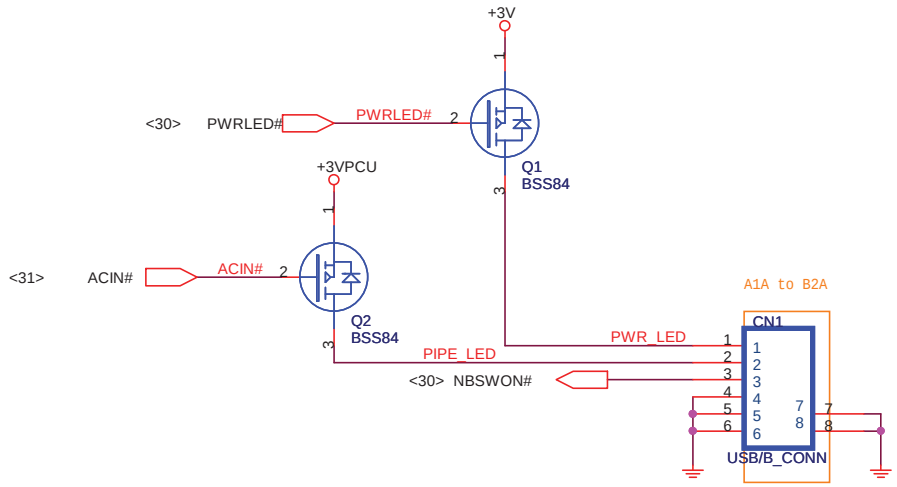
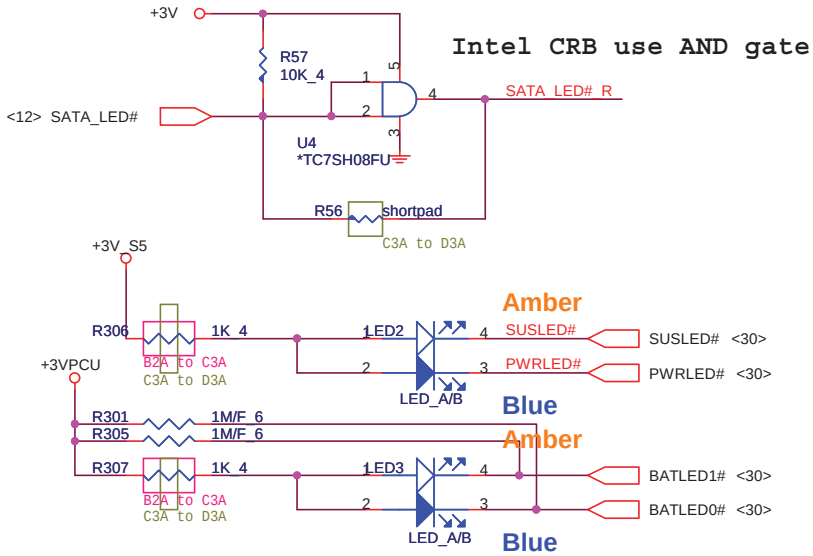
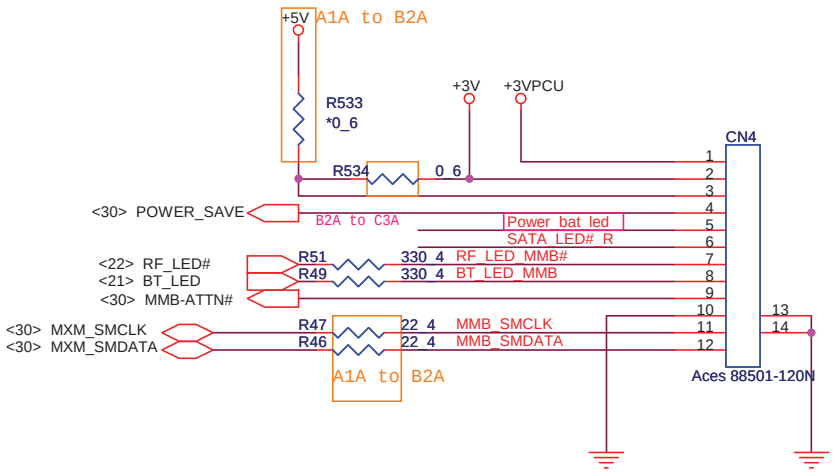
POWER BOARD



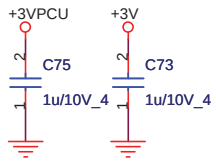
LED

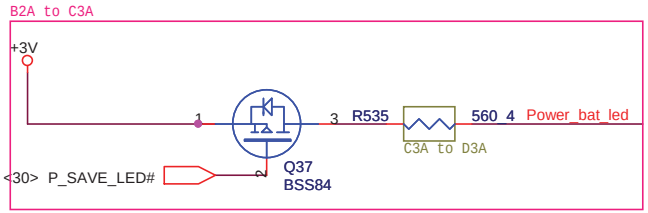


MMB



Close to MMB connector





Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A

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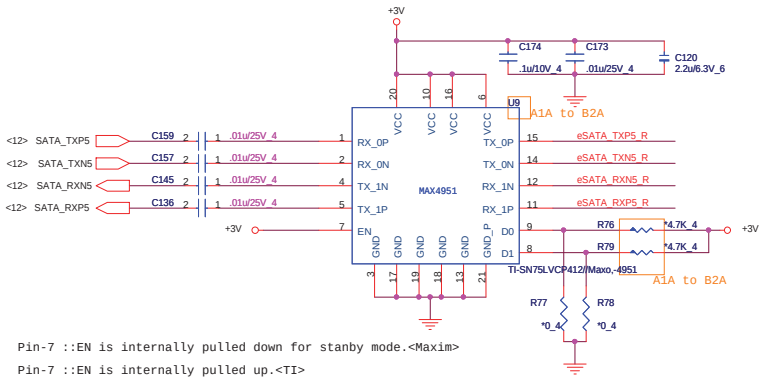
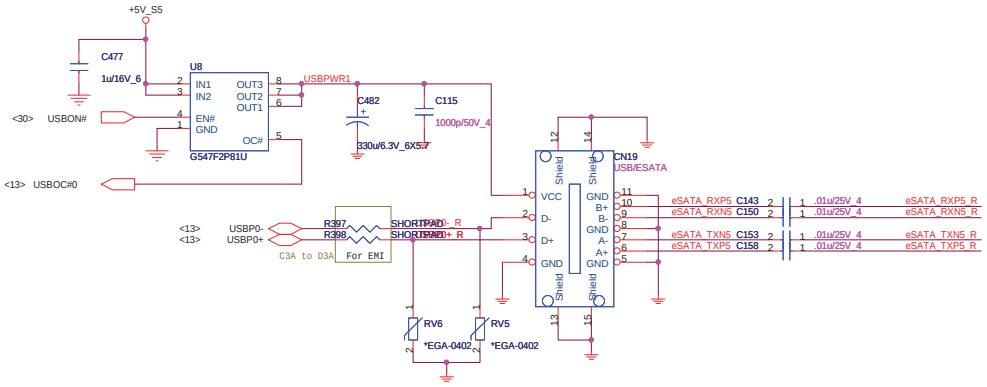
ESATA





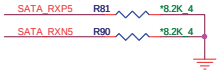

```
Pin-7 ::EN is internally pulled down for stanby mode.<Maxim>
Pin-7 ::EN is internally pulled up.<TI>
Pin-8 ::BB is internally pulled down.<TI/MAXIM>
Pin-9 ::BA is internally pulled down.<TI/MAXIM>
```

EN	BA/D0	BB/D1	CH-0/A	CH-1/B
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

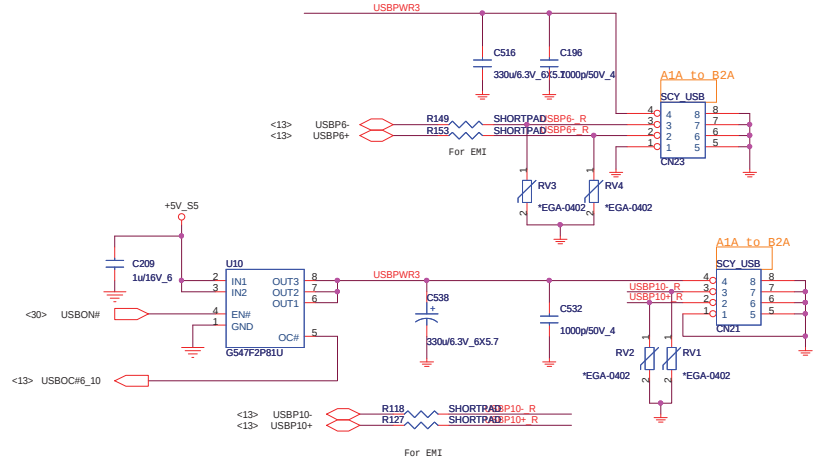
X=don't care

DG2.1 4.2.4 Terminating Unused SATA Interface

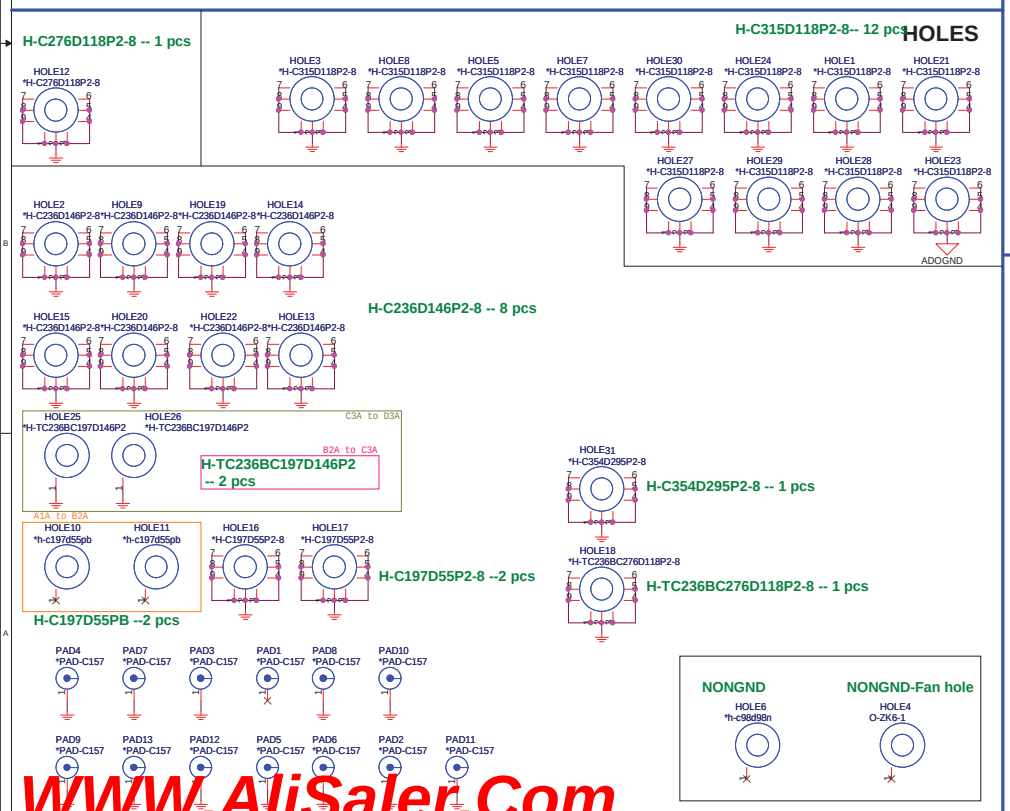
SATA[1:0]RXp/n, SATA[5:4]RXp/n connect to GND while SATA not be implemented



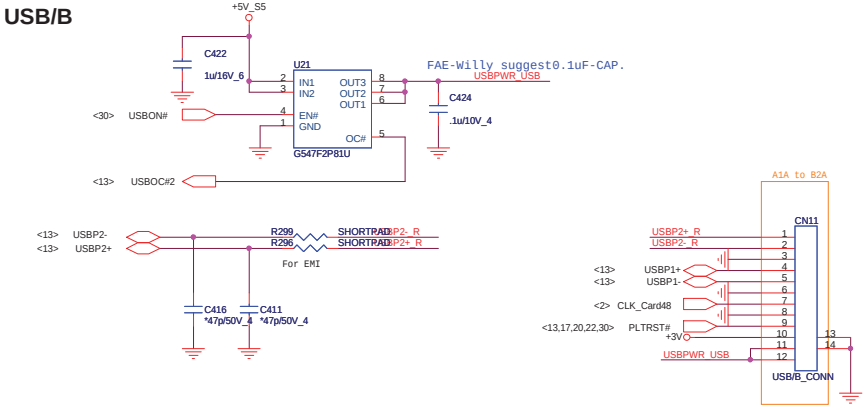
USB PORT



HOLES



USB/B



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PROJECT : ZK6

Size	Document Number	Rev
	USB	1A

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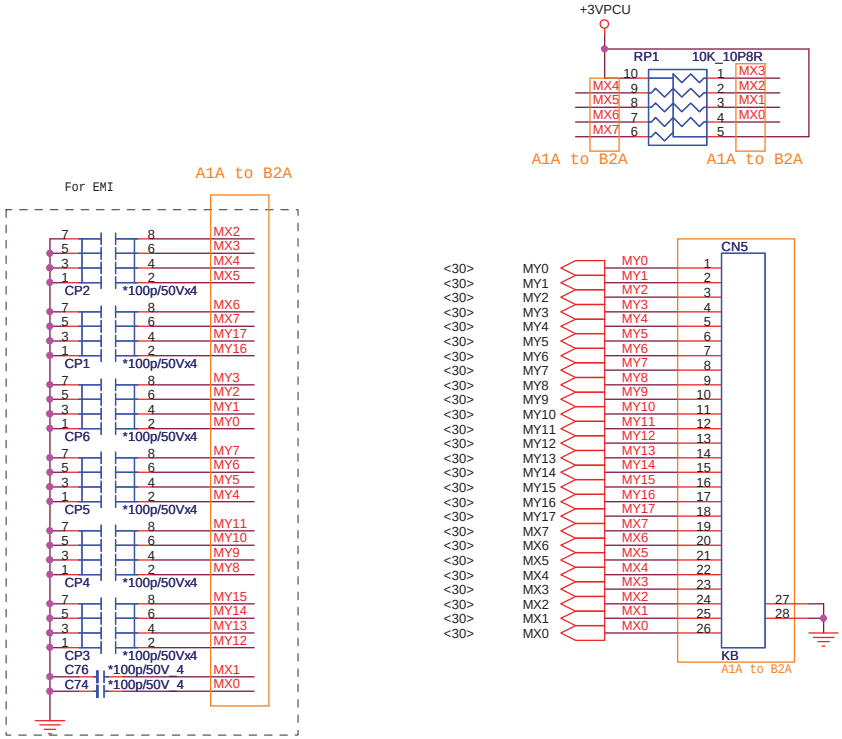
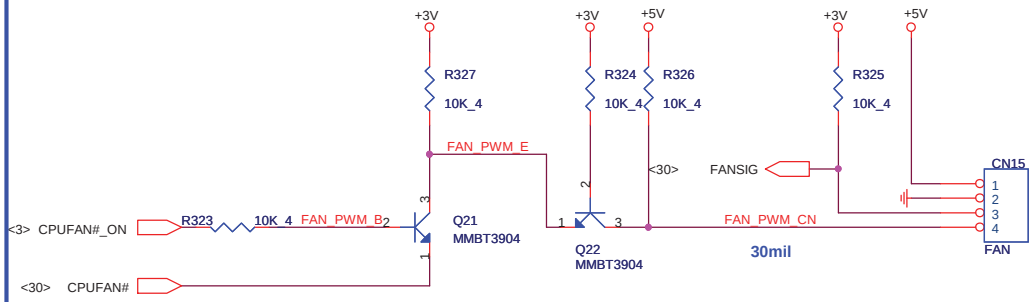
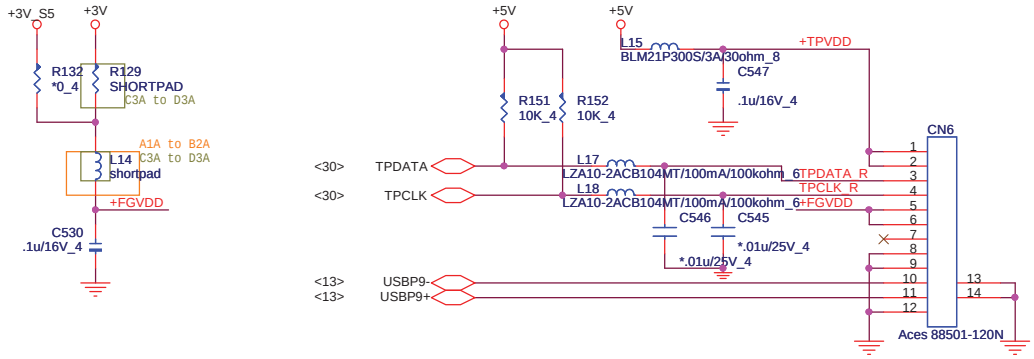
K/B



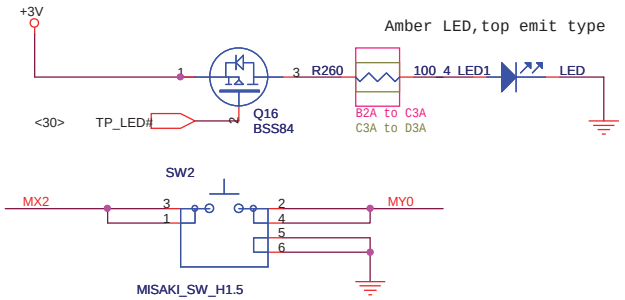
CPU FAN



TOUCHPAD & Finger-Printer CONN.

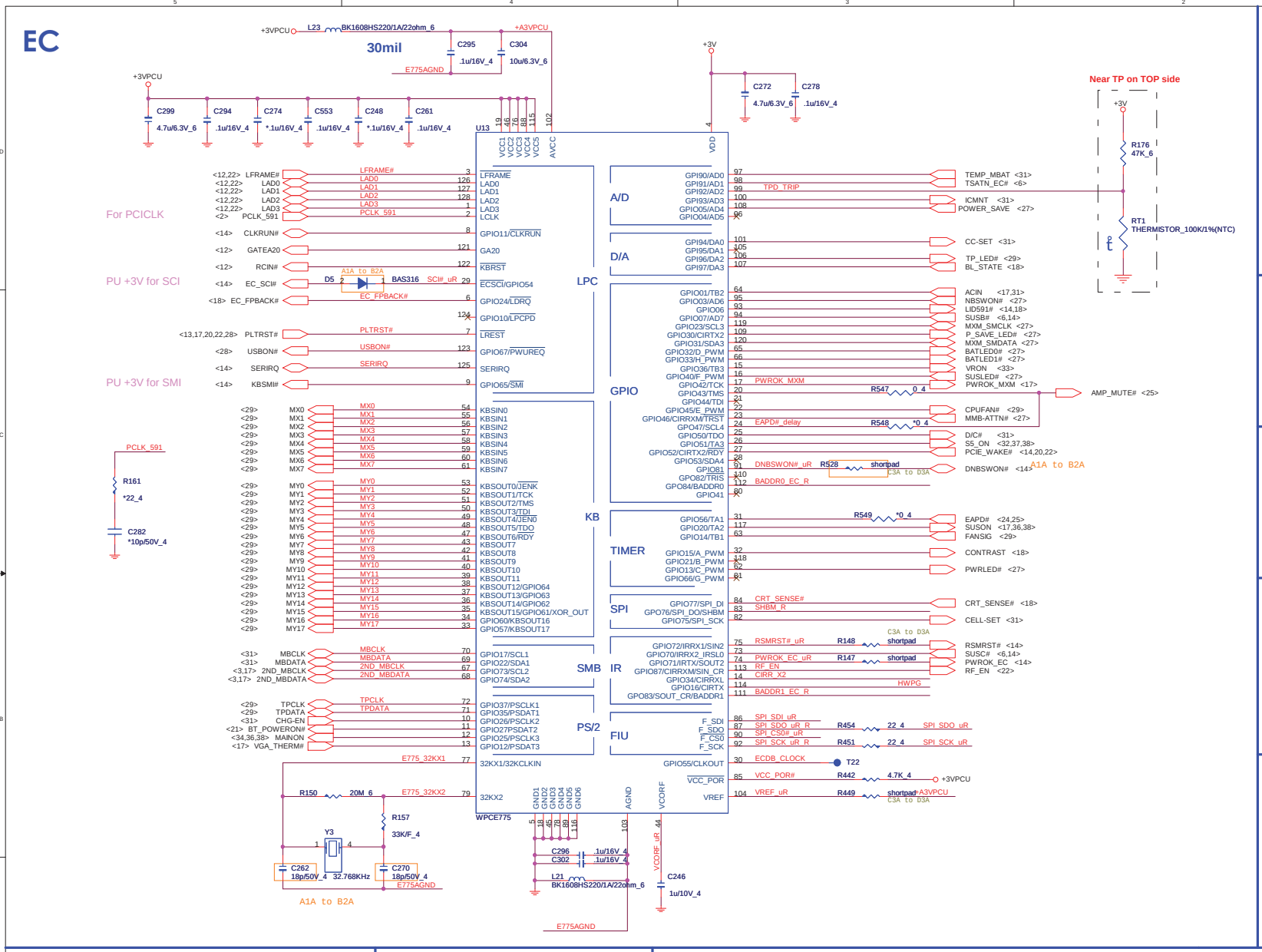


TP LOCK Button



Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: KB/FAN/TP+FP	Rev 1A
Date: Friday, April 24, 2009	Sheet 29 of 42	

EC



I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

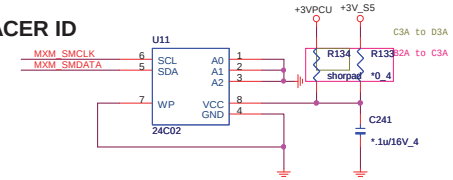
BADDR0 — BADDR0_EC_R — R179 — 10K_4
BADDR1 — BADDR1_EC_R — R178 — *10K_4
SHBM — SHBM_R — R440 — 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

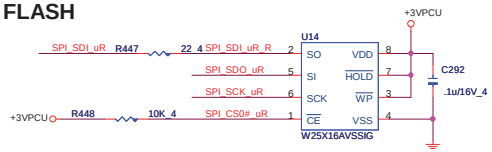
SM BUS PU

2ND_MBCLK — R419 — 10K_4
2ND_MBDATA — R429 — 10K_4
MBCLK — R434 — 10K_4
MBDATA — R433 — 10K_4
MXM_SMCLK — R168 — 10K_4
MXM_SMDATA — R169 — 10K_4
CRT_SENSE# — R441 — 4.7K_4

ACER ID

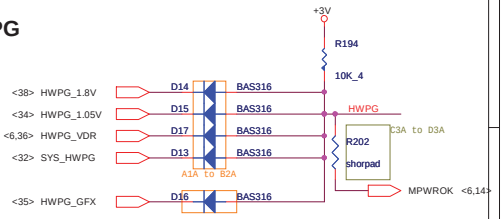


SPI FLASH



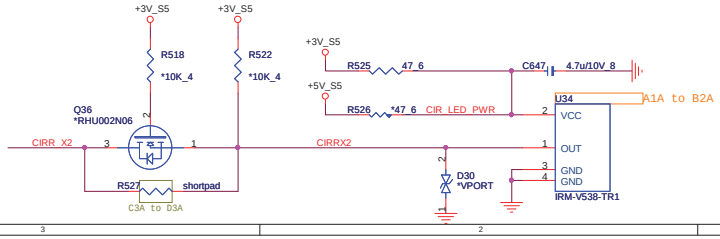
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG



INTERNAL KEYBOARD STRIP SET

CIR



Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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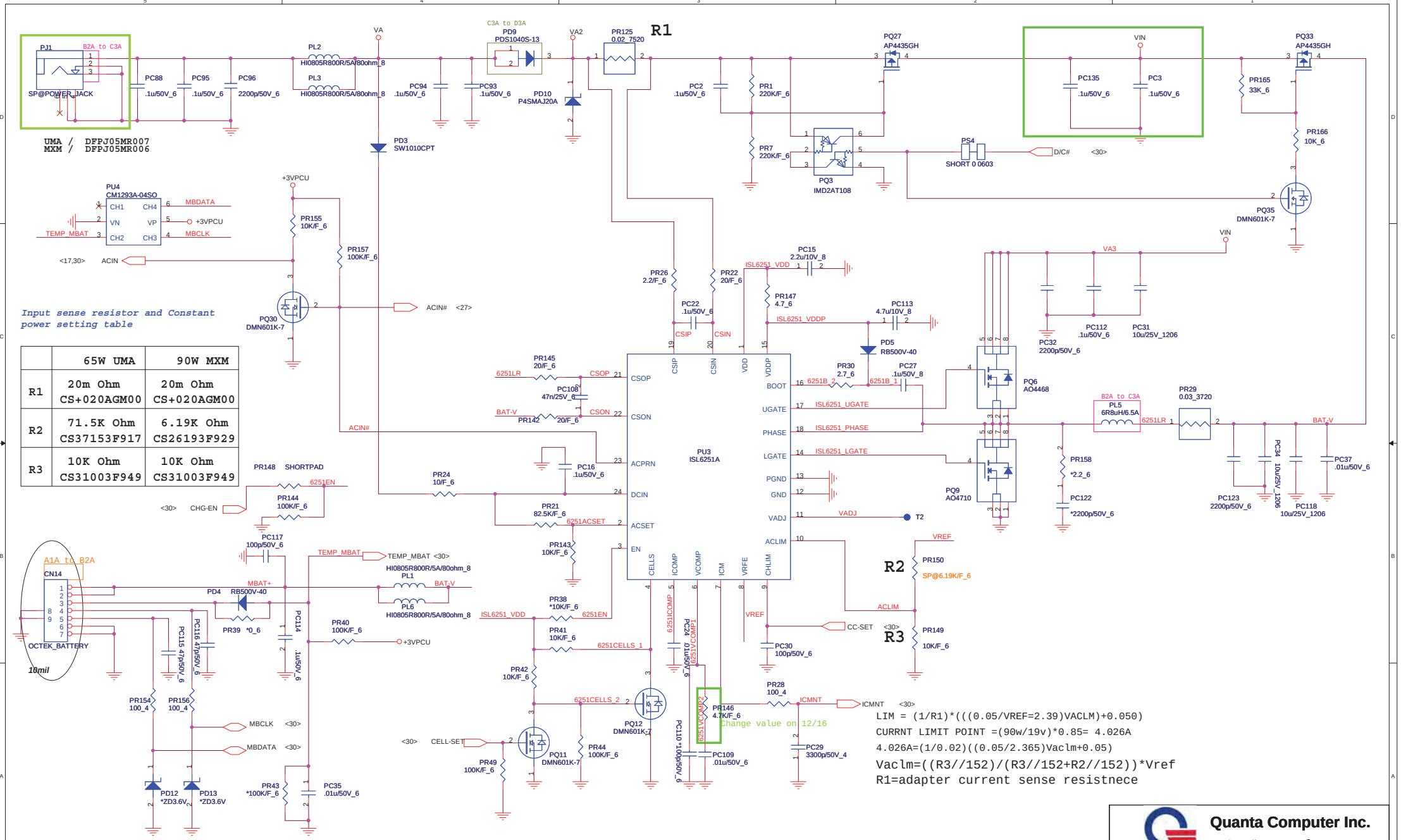
PJ1
B2A to C3A
SP@POWER_JACK
PC88 .1u/50V_6
PC95 .1u/50V_6
PC96 2200p/50V_6
PL2 HI0805R800R/5A/80ohm_8
PL3 HI0805R800R/5A/80ohm_8
VA
PC94 .1u/50V_6
PC93 .1u/50V_6
C3A to D3A
PD9 PDS1040S-13
PD10 P4SMAJ20A
VA2
PR125 0.02_7520
R1
PD3 SW1010CPT
PC2 .1u/50V_6
PR1 220K/F_6
PR7 220K/F_6
PQ27 AP4435GH
PQ3 IMD2AT108
PS4 SHORT 0 0603
D/C# <30>
VIN
PC135 .1u/50V_6
PC3 .1u/50V_6
PQ33 AP4435GH
PR165 33K_6
PR166 10K_6
PQ35 DMN601K-7
UMA / DFPJ05MR007
MXM / DFPJ05MR006
PU4 CM1293A-04SO
CH1 CH4 VN VP CH2 CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
<17,30> ACIN
PR155 10K/F_6
PR157 100K/F_6
PQ30 DMN601K-7
ACIN# <27>
Input sense resistor and Constant power setting table
PR26 2.2/F_6
PR22 20/F_6
PC22 .1u/50V_6
CSIP
CSIN
ISL6251_VDD
PC15 2.2u/10V_8
PR147 4.7_6
ISL6251_VDDP
PC113 4.7u/10V_8
PD5 RB500V-40
PC27 .1u/50V_8
PR30 2.7_6
6251B_2
6251B_1
VA3
PC32 2200p/50V_6
PC112 .1u/50V_6
PC31 10u/25V_1206
PR145 20/F_6
6251LR
CSOP
PC108 47n/25V_6
BAT-V
PR142 20/F_6
CSON
ACIN#
PR148 SHORTPAD
6251EN
PR144 100K/F_6
<30> CHG-EN
PR24 10/F_6
PC16 .1u/50V_6
PR21 82.5K/F_6
6251ACSET
PR143 10K/F_6
PU3 ISL6251A
CSOP CSON ACPRN DCIN ACSET EN
CSIP CSIN VDD VDDP
BOOT UGATE PHASE LGATE PGND GND VADJ ACLIM
CELLS ICOMP VCOMP ICM VREF CHLIM
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
VADJ
T2
PQ6 AO4468
PQ9 AO4710
B2A to C3A
PL5 6R8uH/6.5A
PR29 0.03_3720
PR158 *2.2_6
PC122 *2200p/50V_6
PC123 2200p/50V_6
PC34 10u/25V_1206
PC118 10u/25V_1206
PC37 .01u/50V_6
VREF
R2
PR150 SP@6.19K/F_6
ACLIM
CC-SET <30>
R3
PR149 10K/F_6
PC30 100p/50V_6
A1A to B2A
CN14
OCTEK_BATTERY
10mil
PC117 100p/50V_6
TEMP_MBAT
TEMP_MBAT <30>
HI0805R800R/5A/80ohm_8
PL1
BAT-V
MBAT+
PD4 RB500V-40
PL6 HI0805R800R/5A/80ohm_8
PR39 *0_6
PC114 .1u/50V_6
PC115 47p/50V_6
PC116 47p/50V_6
PR40 100K/F_6
+3VPCU
ISL6251_VDD
PR38 *10K/F_6
6251EN
PR41 10K/F_6
6251CELLS_1
6251ICOMP
PC24 .01u/50V_6
6251VCOMP1
PR42 10K/F_6
6251CELLS_2
PQ12 DMN601K-7
PR146 4.7K/F_6
Change value on 12/16
PR28 100_4
ICMNT
ICMNT <30>
PC110 *100p/50V_6
PC109 .01u/50V_6
PC29 3300p/50V_4
PR154 100_4
PR156 100_4
MBCLK <30>
MBDATA <30>
<30> CELL-SET
PQ11 DMN601K-7
PR49 100K/F_6
PR44 100K/F_6
PD12 *ZD3.6V
PD13 *ZD3.6V
PR43 *100K/F_6
PC35 .01u/50V_6
LIM = (1/R1)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((R3//152)/(R3//152+R2//152))*Vref
R1=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ---->4S
CELL-SET = Low ----> Cells = GND ---->3S
Quanta Computer Inc.
PROJECT : ZK6
Size
Document Number
CHARGER (ISL6251A)
Rev 1A
Date: Friday, April 24, 2009
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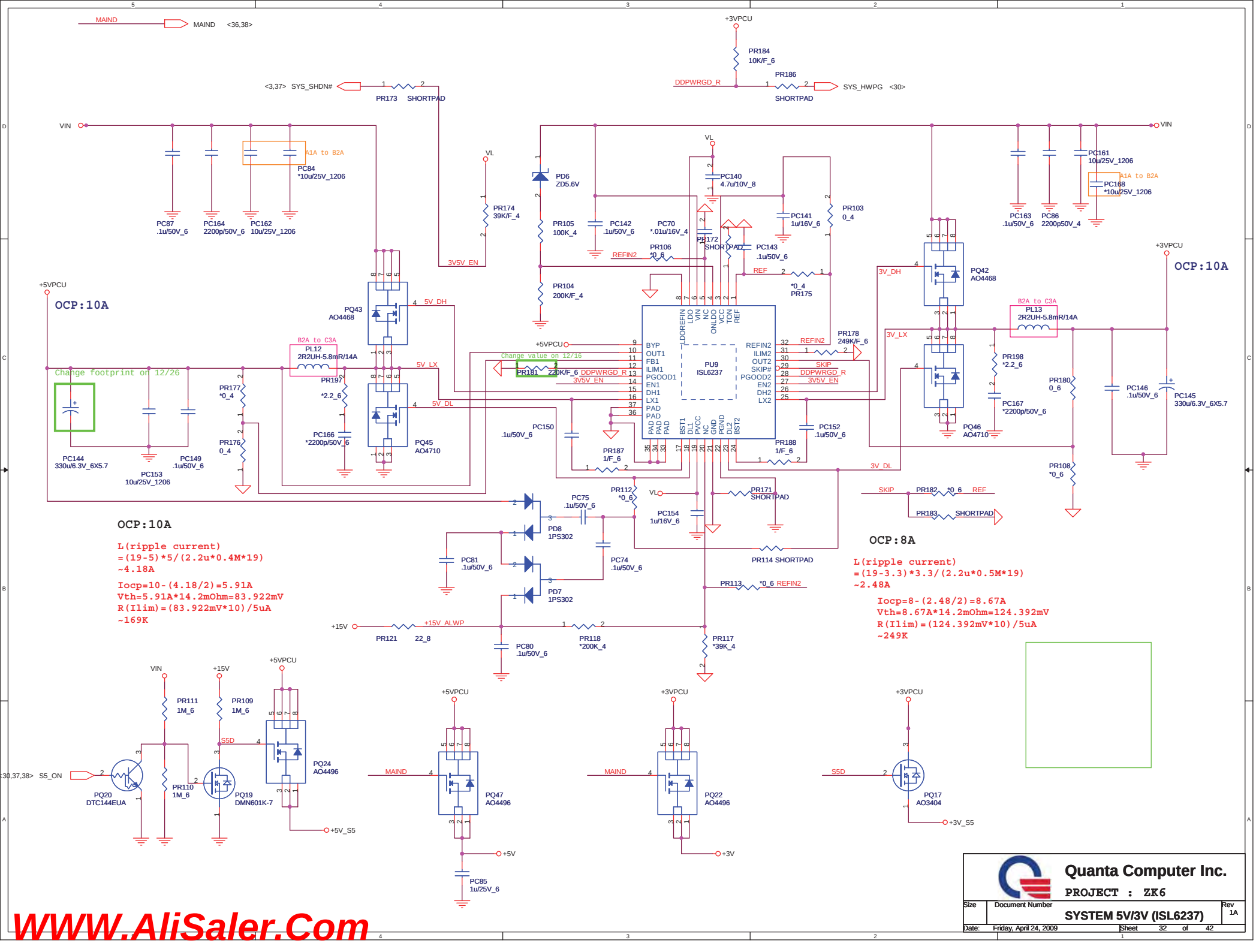

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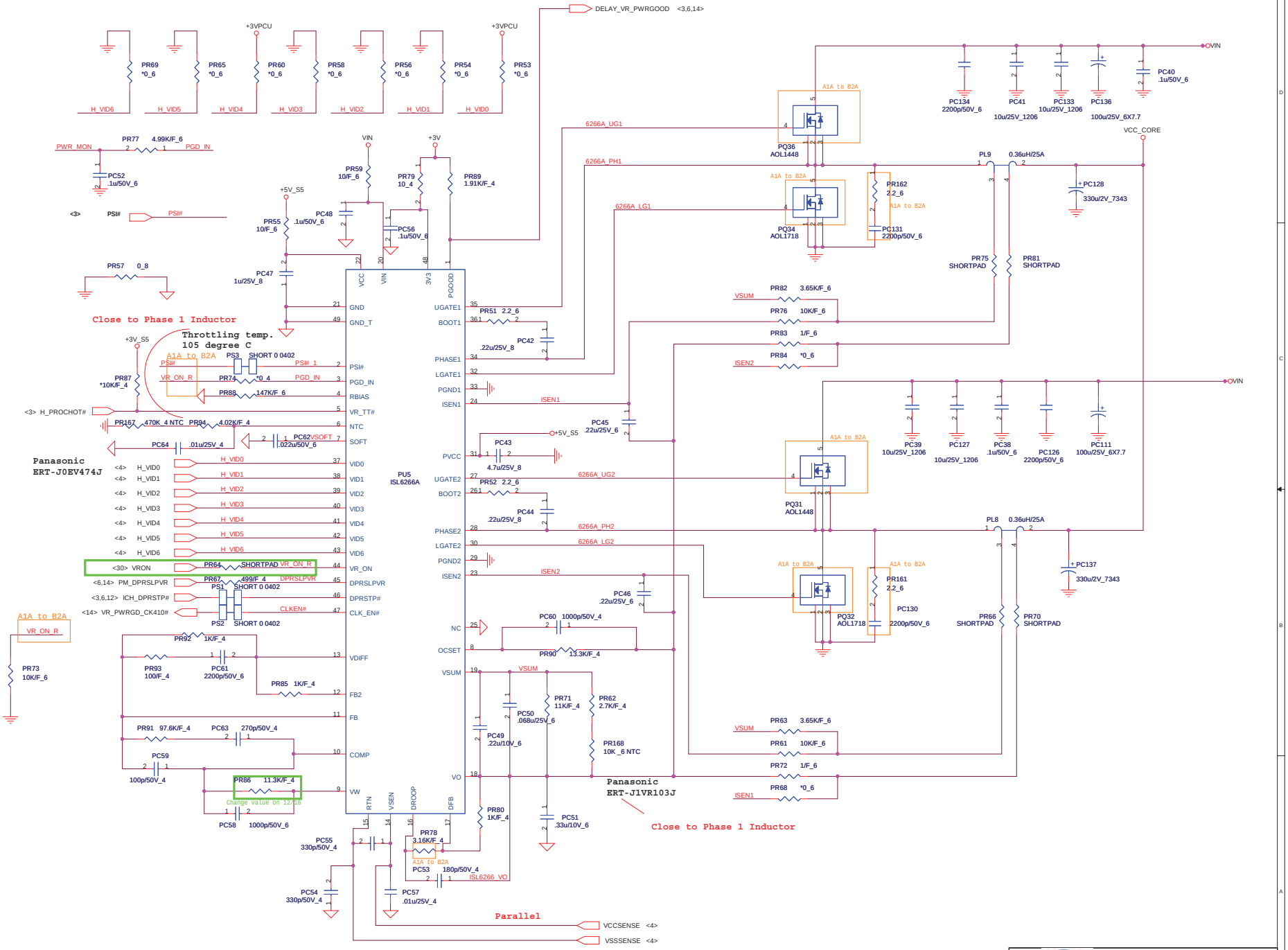

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	CPU CORE(ISL6266A)	1A

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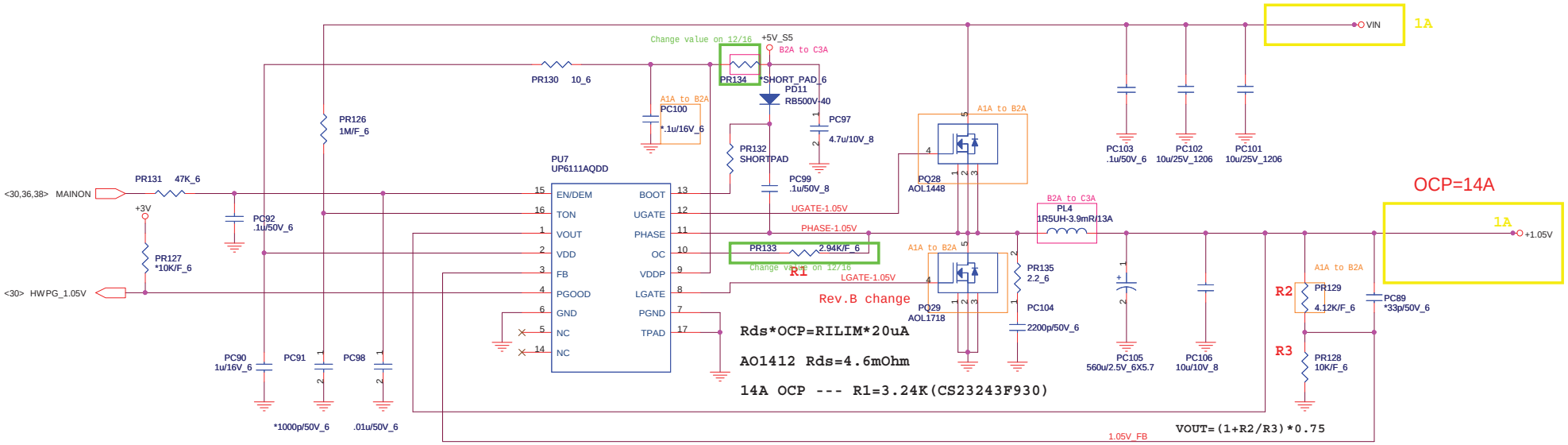

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number	Rev
	VTT 1.05V (RT8202)	1A
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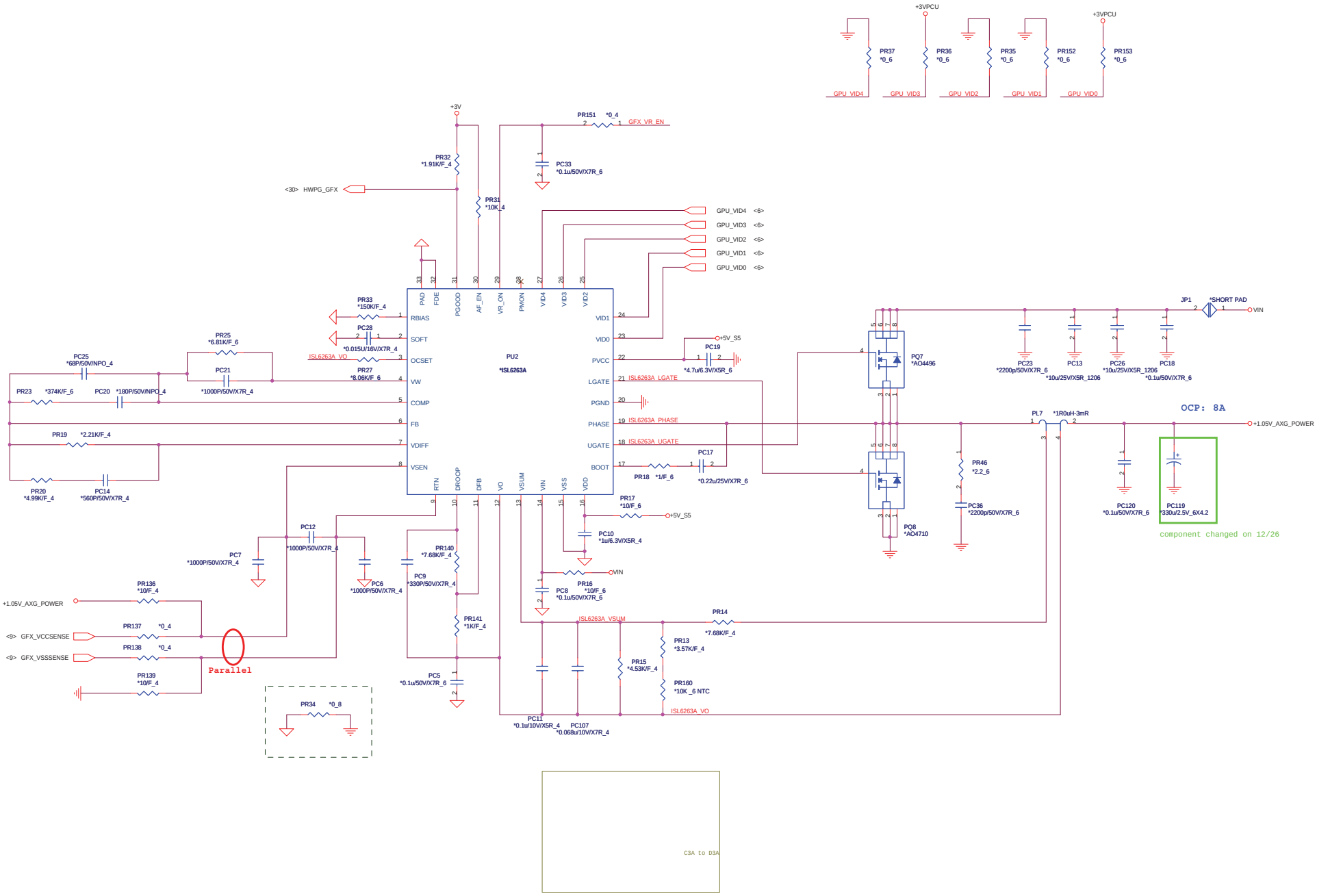
all component in this page would be stuff for UMA only



Quanta Computer Inc.

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Size	Document Number	Rev
	+1.05V_GFX-ISL6263A	1A

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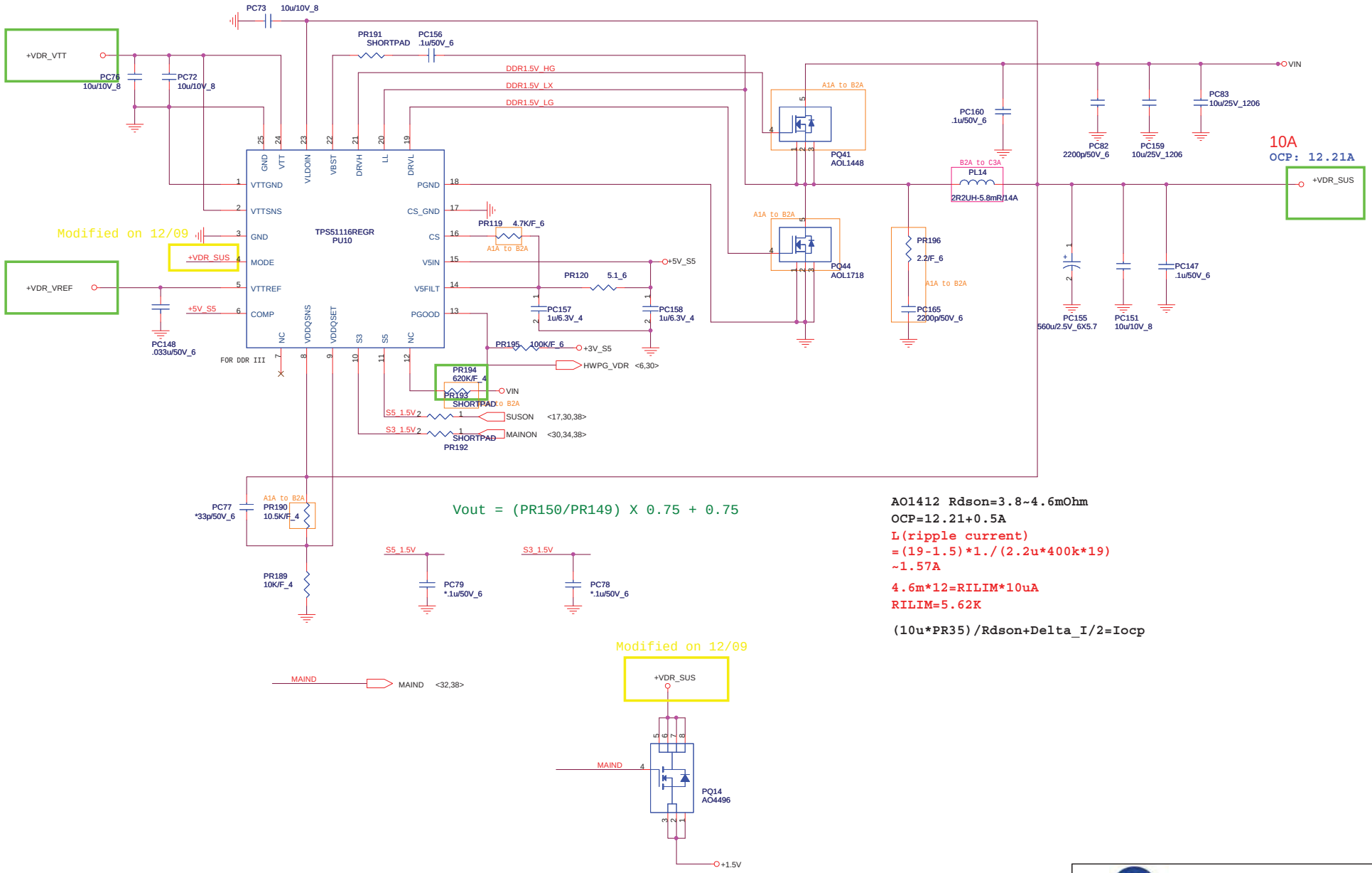

AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1./(2.2u*400k*19)
~1.57A

4.6m*12=RILIM*10uA
RILIM=5.62K

(10u*PR35)/Rdson+Delta_I/2=Iocp

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Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A

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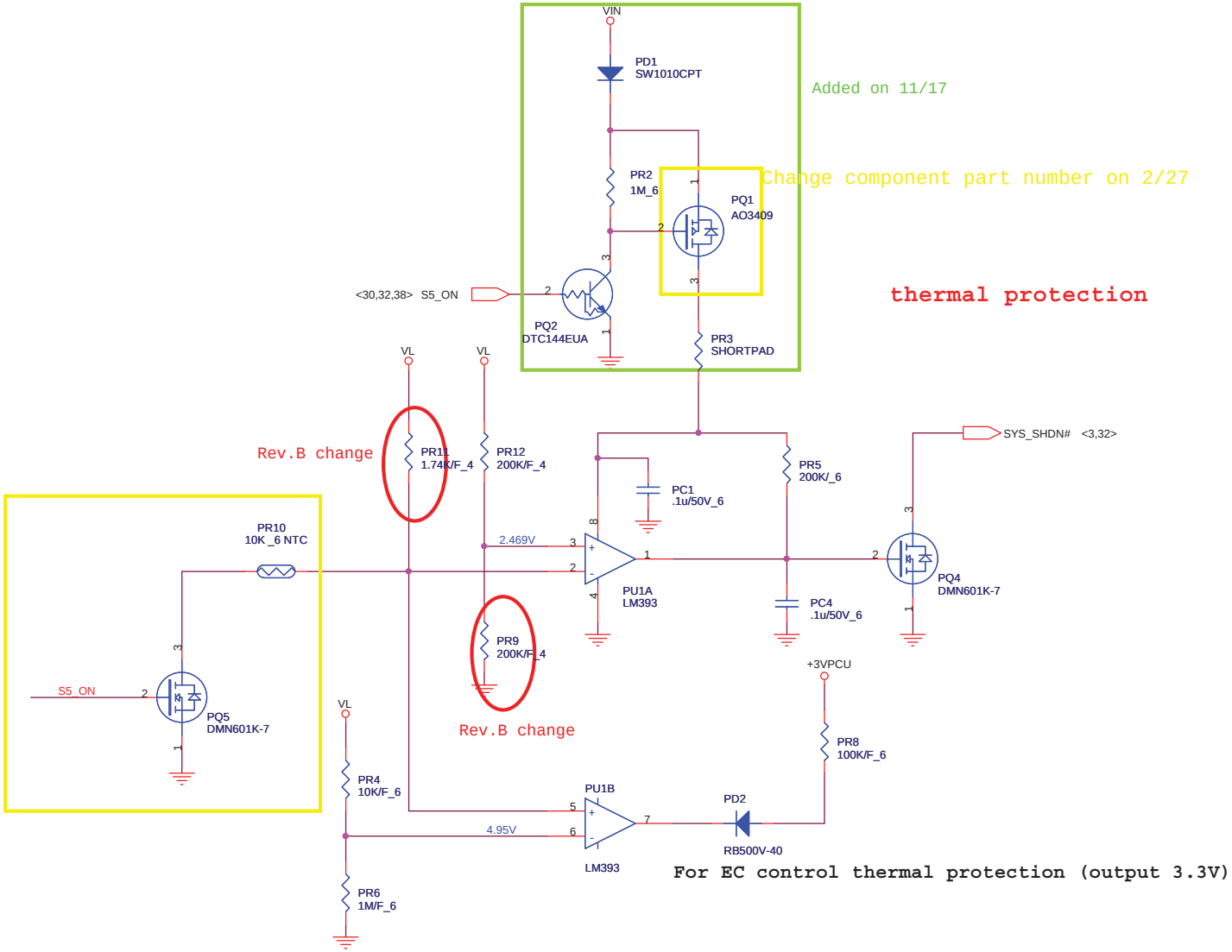

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZK6		
Size	Document Number: Thermal protect	Rev 1A
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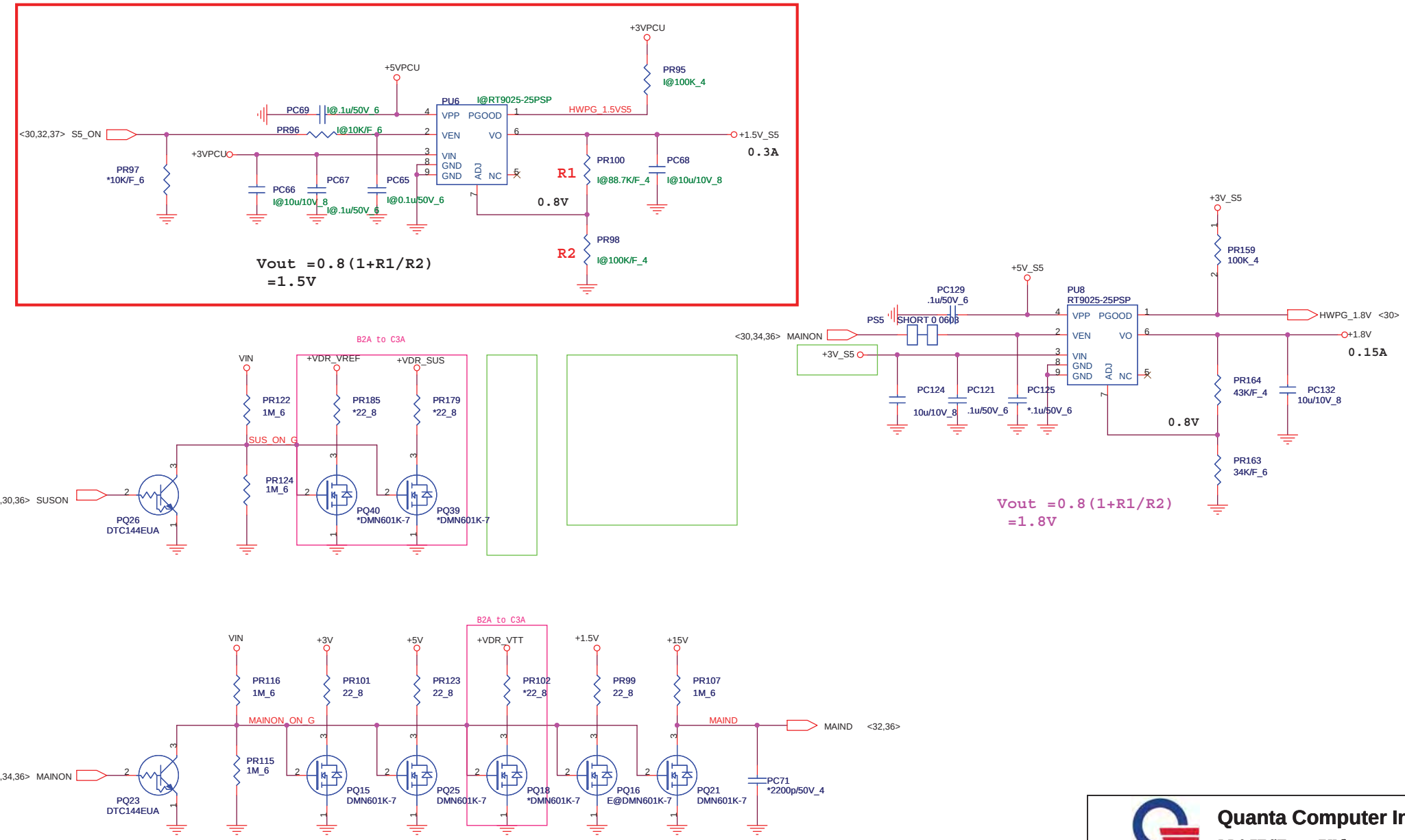

Quanta Computer Inc.

PROJECT : ZK6

Size	Document Number	Rev
	Discharge (2.5V/1.5V)	1A

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