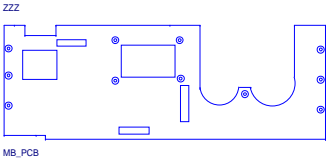


MODEL NAME : ZZZZZZ

PCB NO : LA-E672P

BOM P/N : 43xxxxx



Dell/Compal Confidential

Schematic Document

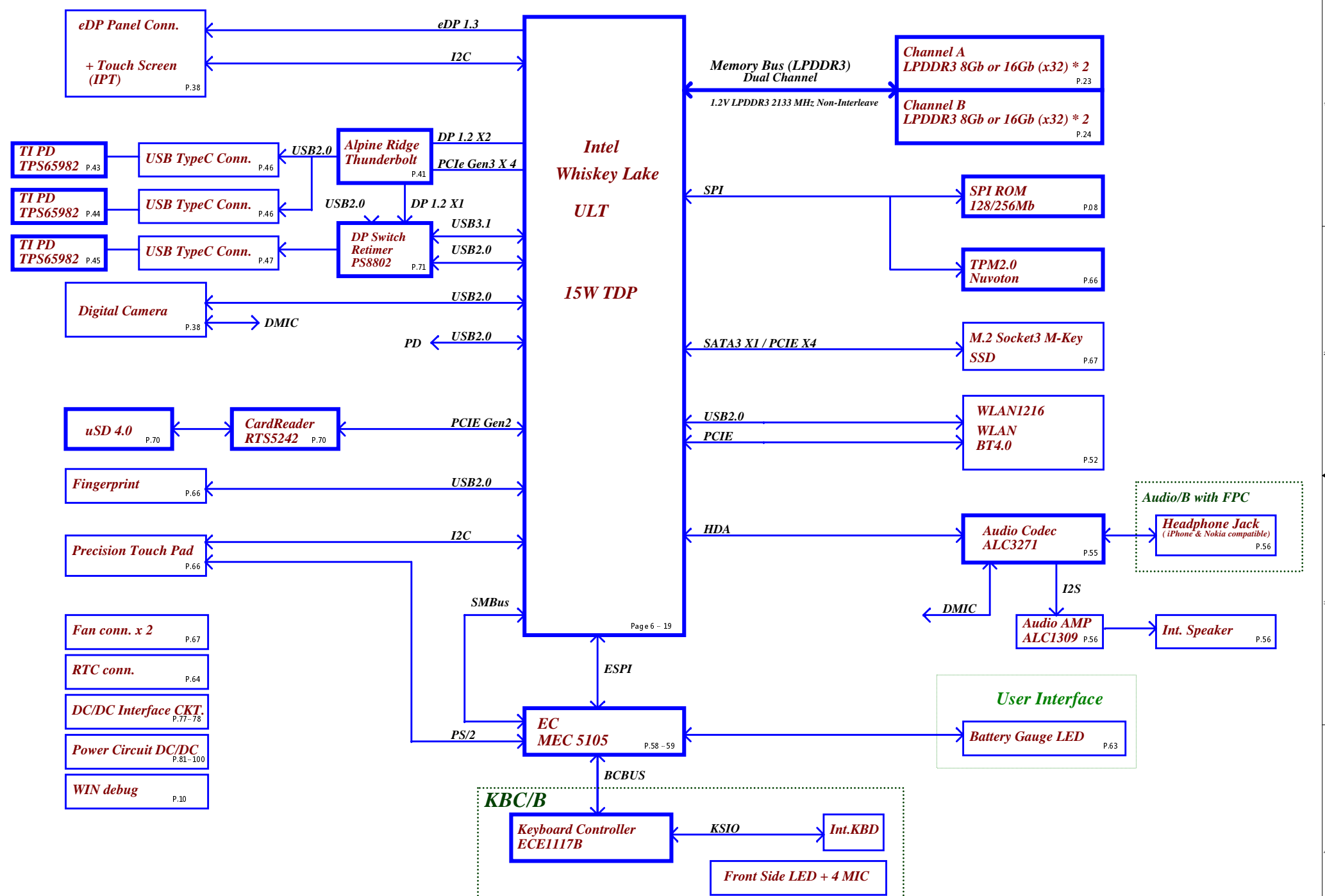
Italia WHL

2018-10-22

Rev: 1.0 (A00)

@ : Nopop Component
L@: Intel 8265
XPS@ : Killer1435-S
DCI@ : for DCI Debug
DEBUG@ : for Other Debug
@CONN@ : Reserve Connector Component
@EMC@ : Reserve EMC Component
CONN@ : Connector Component
EMC@ : EMC Component
RF@ : RF Solution Component
XDP@ : XDP Debug Component
RTD3@ : for TBT RTD3 and follow Merion
@RTD3@ : No TBT RTD3

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2016/12/16		2016/12/13		P01-Cover Page	
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				LA-E672	0.1
				Date: Tuesday, October 30, 2018	Sheet 1 of 100



Board ID Table for AD channel

RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	A00
4.3K	4700p	
2K	4700p	
1K	4700p	

CPU	4+2	2+2	VPro
Italia WHL EDO30			

BOARD_ID rise time is measured from 5%~68%.

SMBUS Control Table

	SOURCE	BATTERY Charger	PD1	PD2	PWR_MON	5105	XDP	Audio AMP	eDP	Touch Pad	Touch S	IR_THER_S
SMB00_CLK SMB00_DATA	MEC5105			V								
SMB01_CLK SMB01_DATA	MEC5105											V
SMB02_CLK SMB02_DATA	MEC5105									V		
SMB04_CLK SMB04_DATA	MEC5105		V									
SMB05_CLK SMB05_DATA	MEC5105							V				
SMB07_CLK SMB07_DATA	MEC5105				V							
SMB10_CLK SMB10_DATA	MEC5105	V										
PCH_SML1CLK PCH_SML1DATA	PCH					V						
SMBCLK SMBDATA	PCH						V					
I2C0_CLK I2C0_DATA	PCH										V	
I2C1_CLK I2C1_DATA	PCH									V		
I2C2_CLK I2C2_DATA	PCH								V			

PCH USB 2.0 Port Mapping	USB PORT#	DESTINATION
	1	PD PORT3
	2	NC
	3	NC
	4	NC
	5	IR Camera & Cam
	6	USB PD PORT2
	7	NGFF WLAN BT
	8	NC
	9	USB PD PORT1
	10	Fingerprint
PCH USB 3.0 Port Mapping	1	DP MX (PS8743B)
	2	

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	1	Alpine Ridge
	2	Alpine Ridge

CLK	DIFFERENTIAL CLK#	DESTINATION	PCI EXPRESS PORT#	DESTINATION
	CLKOUT_PCIE0	Alpine Ridge	Lane 5	Card Reader
	CLKOUT_PCIE1	NGFF WLAN	Lane 6	NC
	CLKOUT_PCIE2	NC	Lane 7	NGFF WLAN
	CLKOUT_PCIE3	M.2 SSD	Lane 8	NC
	CLKOUT_PCIE4	NC	Lane 9	Alpine Ridge
	CLKOUT_PCIE5	Card Reader	Lane 10	Alpine Ridge
	FLEX CLK#	DESTINATION	Lane 11	Alpine Ridge
	CLKOUT_LPC_0	ESPI 5105	Lane 12	Alpine Ridge
	CLKOUT_LPC_1	NC	Lane 13	M.2 SSD
	CLKOUT_ITPXDP	XDP CONN	Lane 14	M.2 SSD
			Lane 15	M.2 SSD
			Lane 16 / SATA 2	M.2 SSD

SATA PORT#	DESTINATION
SATA-0	NC
SATA-1A	NC
SATA-1B	NC
SATA-2	M.2 SSD

Symbol Note :

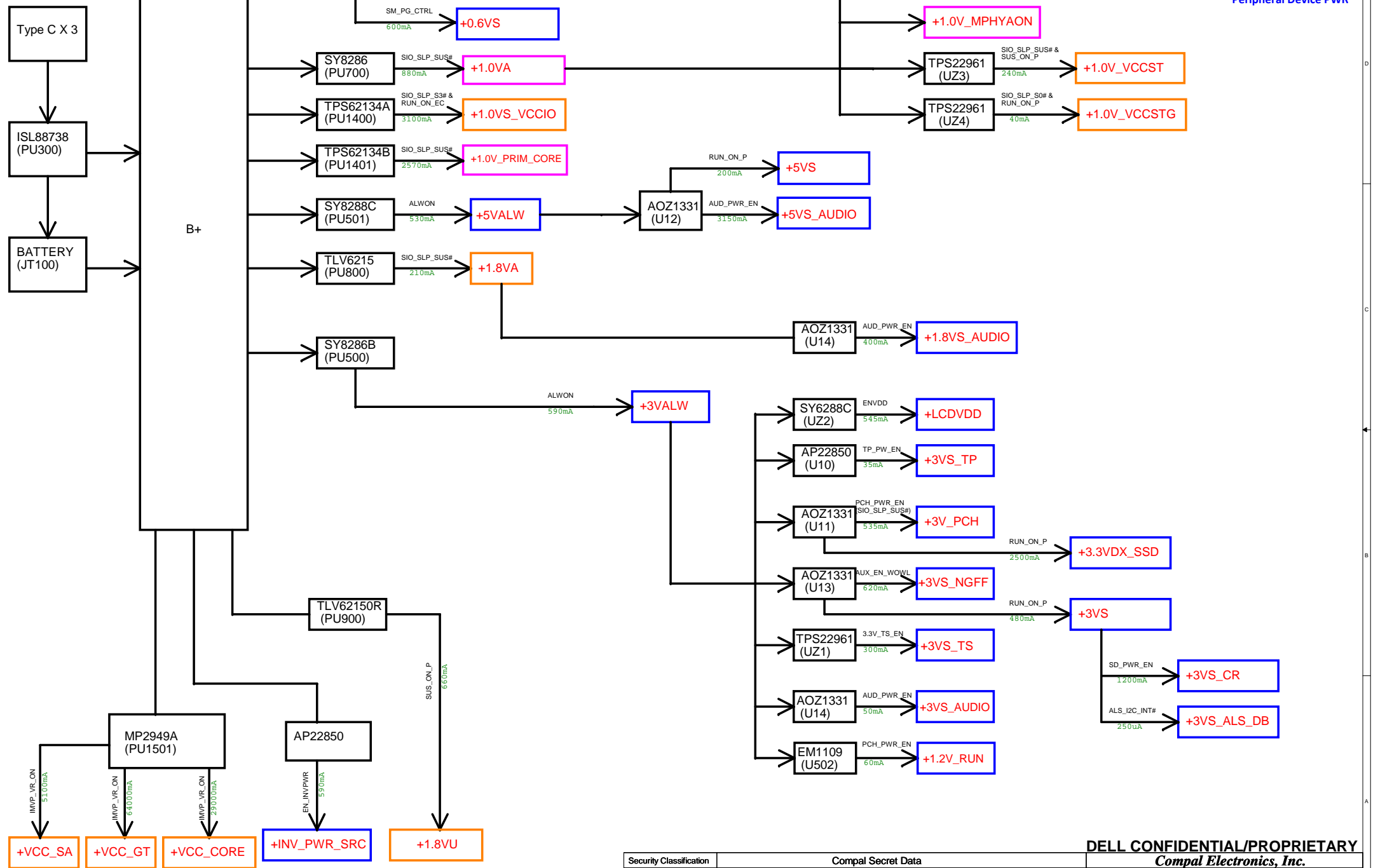


: means Digital Ground



: means Analog Ground

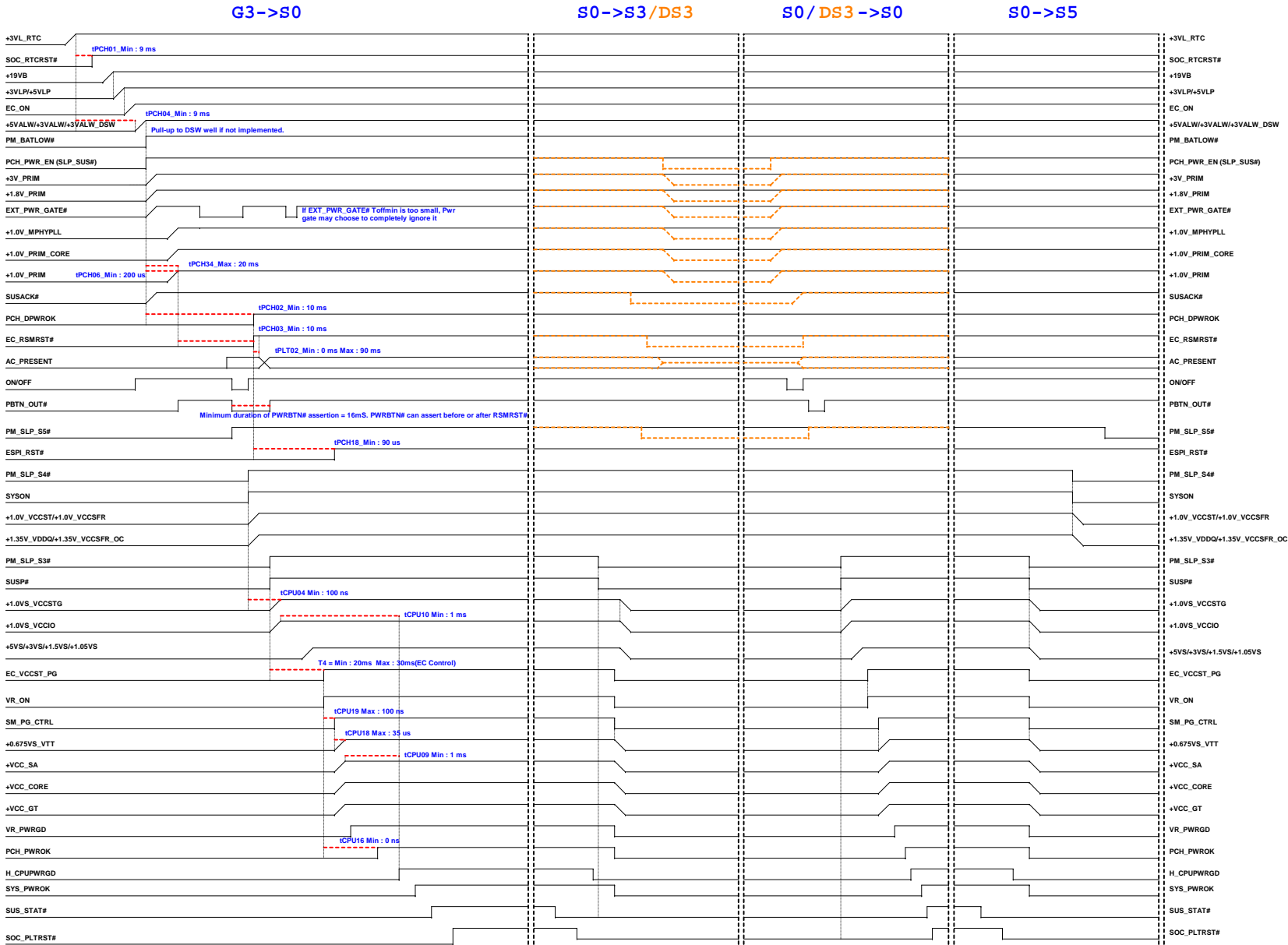
Security Classification				Compal Secret Data				DELL CONFIDENTIAL/PROPRIETARY			
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2015/12/16				2016/12/13				P03-Notes List			
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Date:				Monday, October 22, 2018				Sheet 3 of 100			



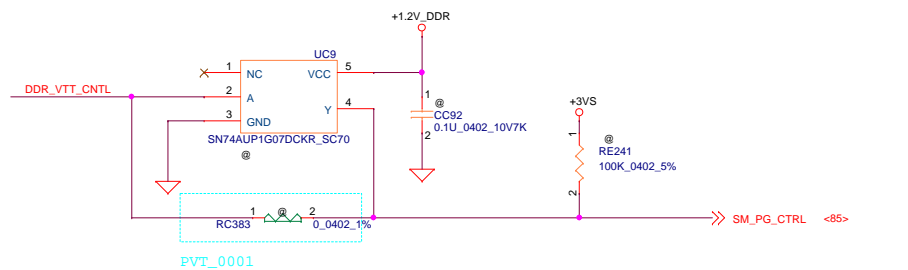
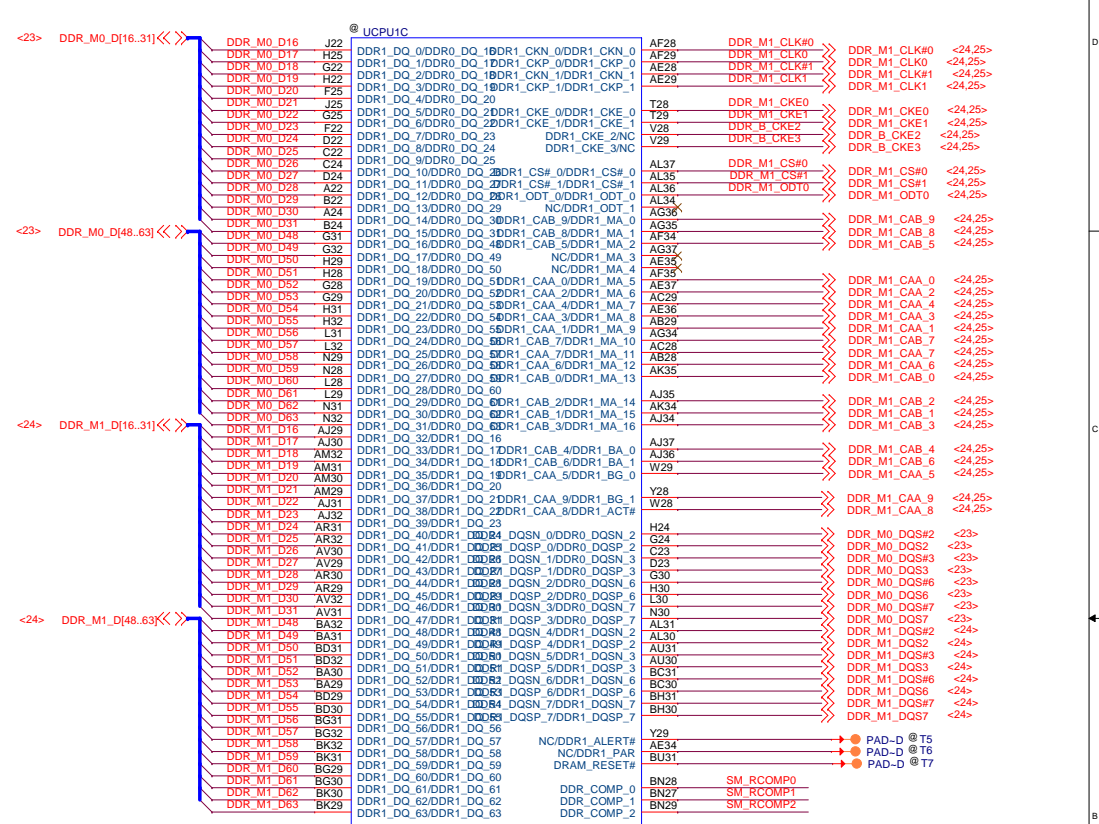
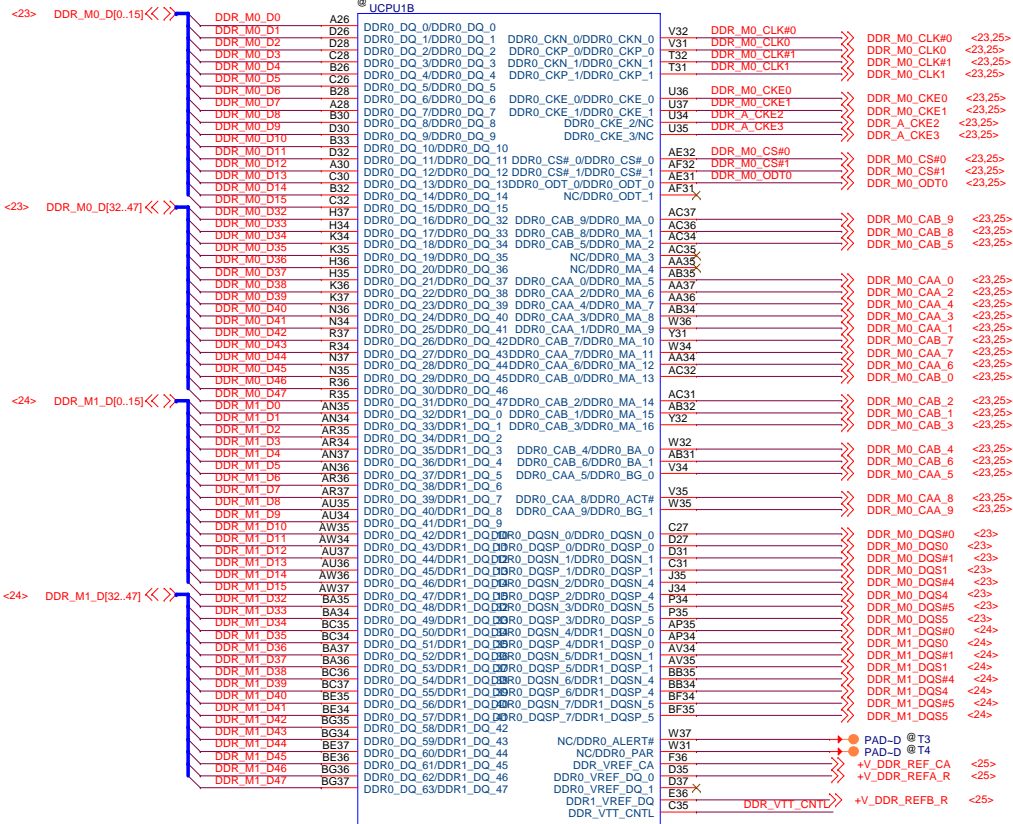
CPU PWR
PCH PWR
GPU PWR
Peripheral Device PWR

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		Date		Monday, October 22, 2018	
		Sheet		4 of 100	
		Rev		0.1	
		LA-E671P			



LPDDR3, Ballout for side by side(Non-Interleave)

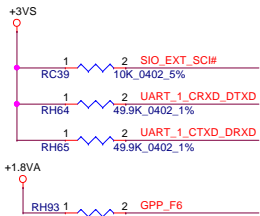


LPDDR3 COMPENSATION SIGNALS

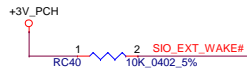


CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

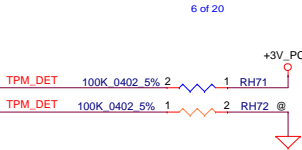
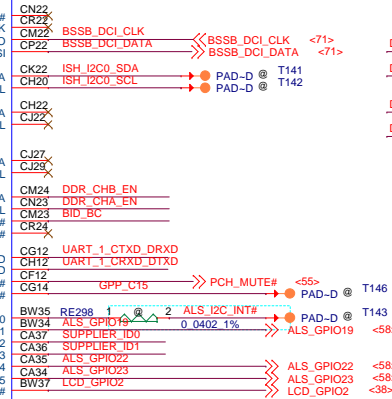
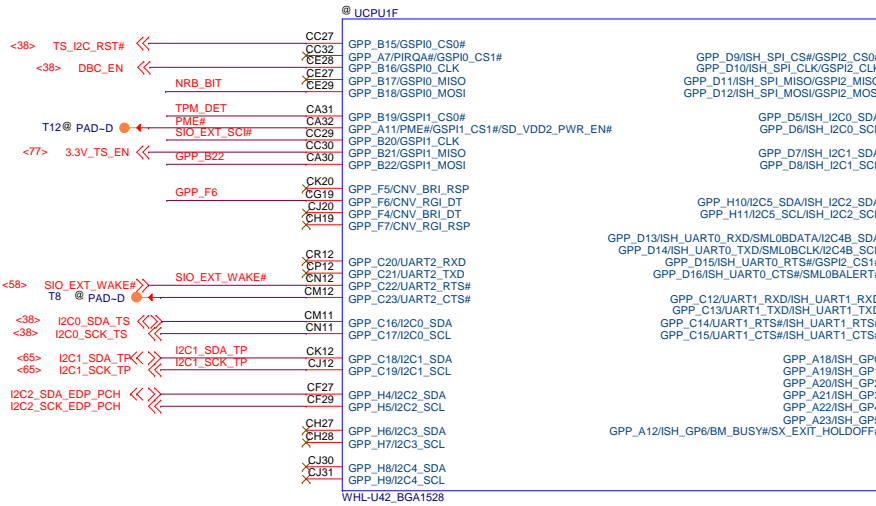
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				Document Number	
				LA-E671P	
				Rev	
				0.1	
Date:		Monday, October 22, 2018		Sheet 7 of 100	



0 = Integrated CNWi enable.
1 = Integrated CNWi disable.
(Disable CNWi for bring up).

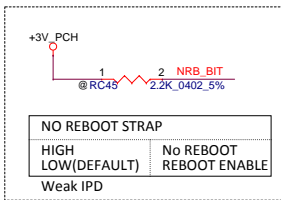


TS
TP
eDP
PWRMONITOR

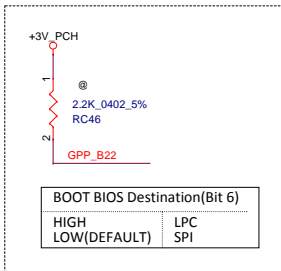


TPM BOM Optional

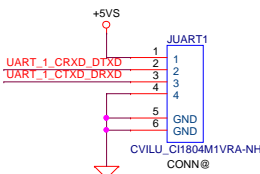
TPM_DET	
TPM	1 = W/TPM 0 = W/O TPM



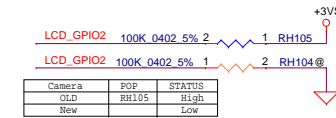
NO REBOOT STRAP	
HIGH LOW(DEFAULT)	No REBOOT REBOOT ENABLE
Weak IPD	



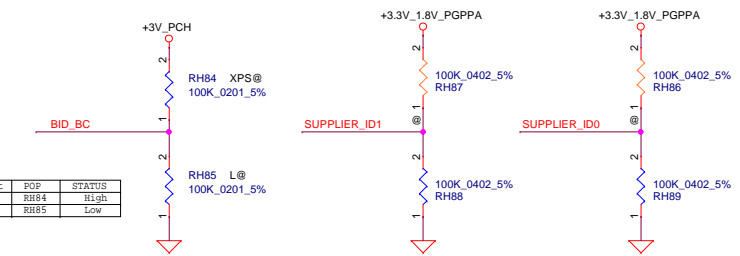
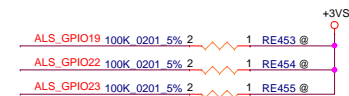
BOOT BIOS Destination(Bit 6)	
HIGH LOW(DEFAULT)	LPC SPI



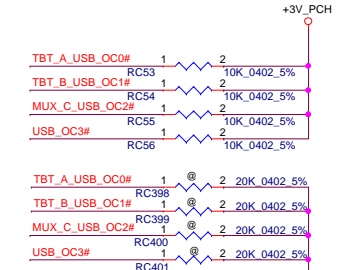
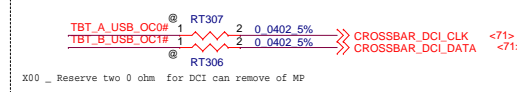
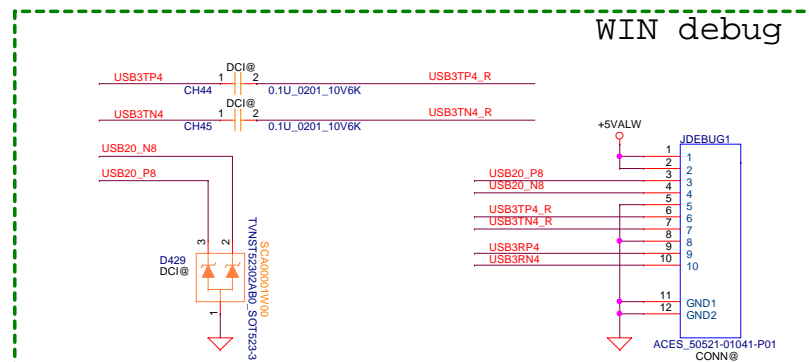
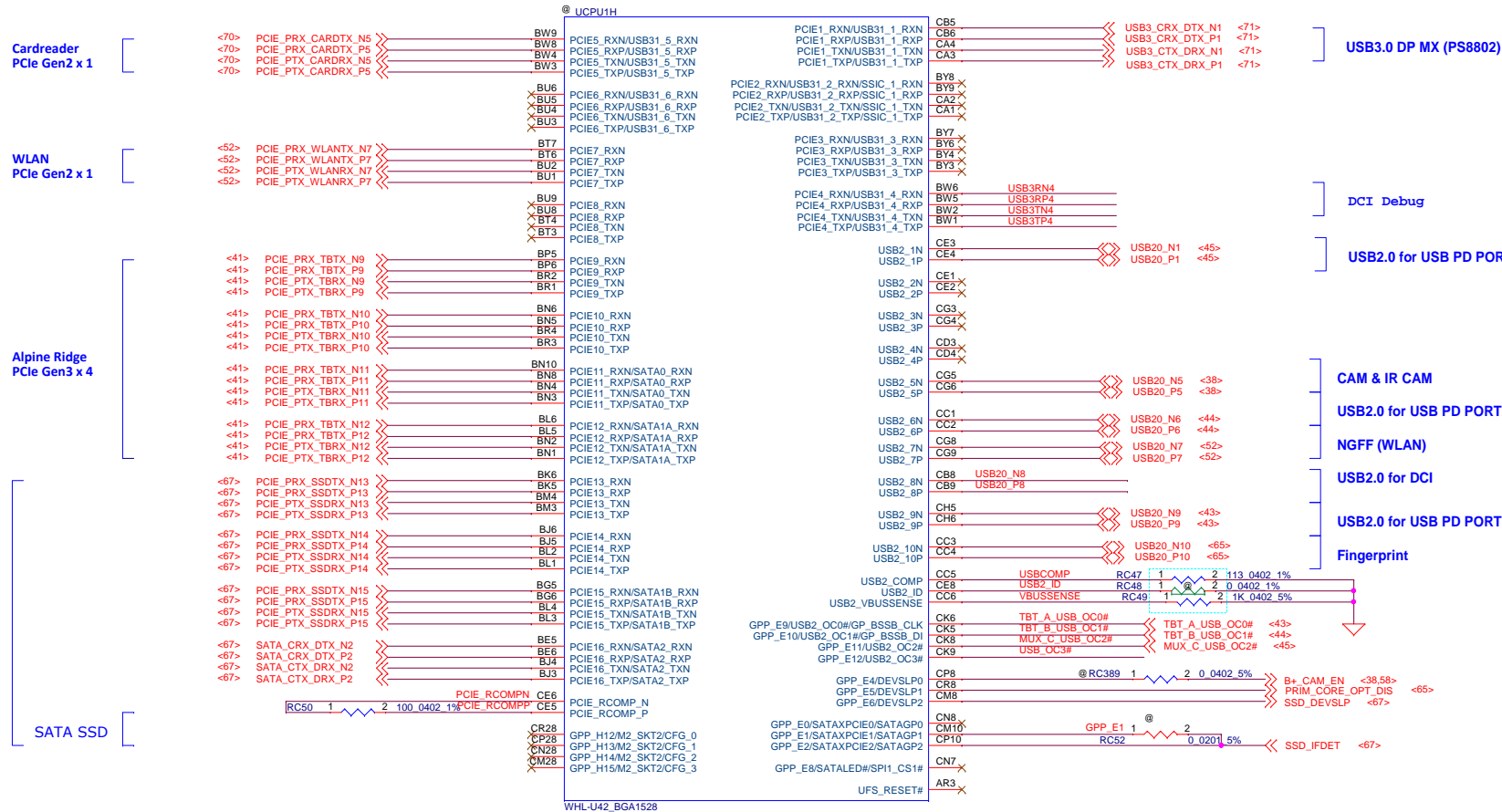
Product	POP	STATUS
XPS	RH84	High
L	RH85	Low



Camera	POP	STATUS
OLD	RH105	High
New	RH104	Low



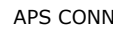
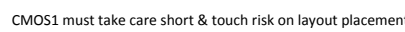
	RH87	RH88	RH86	RH89		REV
*		V		V	0 0	Supplier A
		V	V		0 1	Supplier B
	V			V	1 0	Supplier C
	V		V		1 1	Supplier D



Note : JDEBUG1 place to BOT side and need check footprint

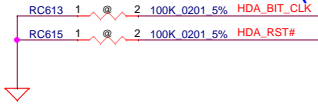
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				LA-E671P	1.0
				Date: Monday, October 22, 2018	Sheet 10 of 100

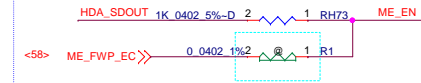
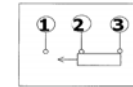


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Issued Date	2015/12/16	Deciphered Date	2016/12/13	Title	<div style="text-align: center;"> P11-MCP(6/14)CLK.PM.RTC LA-E671P </div>
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<div style="display: flex; justify-content: space-between;"> 3 2 </div>				Date: Tuesday, October 23, 2018	Sheet 11 of 100

PCH GLITCH ISSUE MITIGATION(PDG p.130)



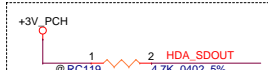
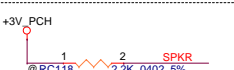
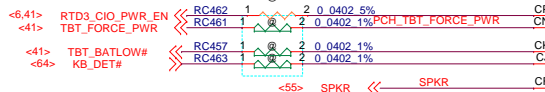
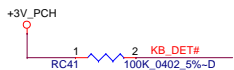
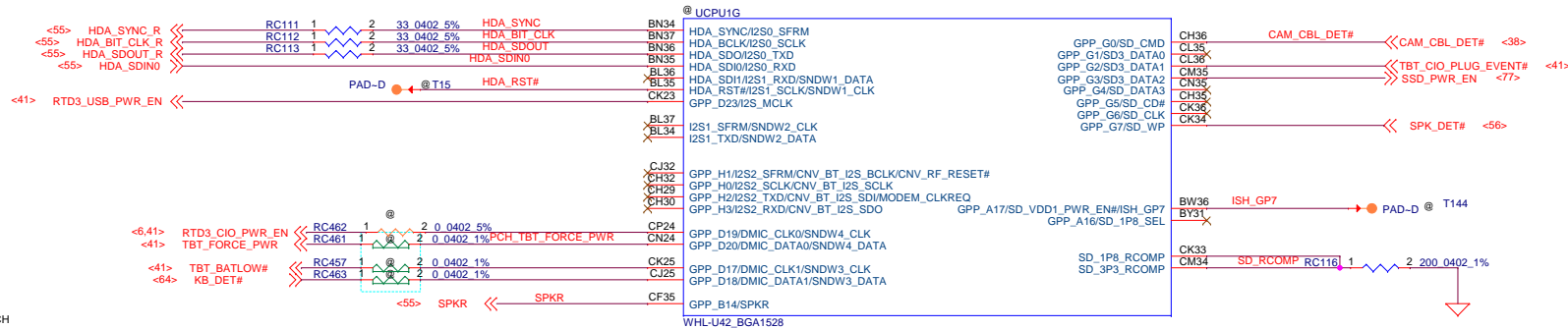
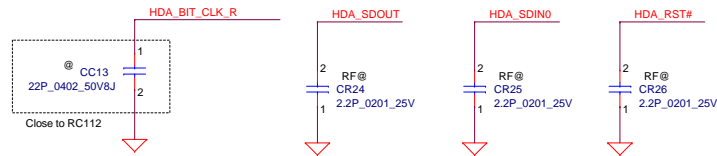
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.



ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE

Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

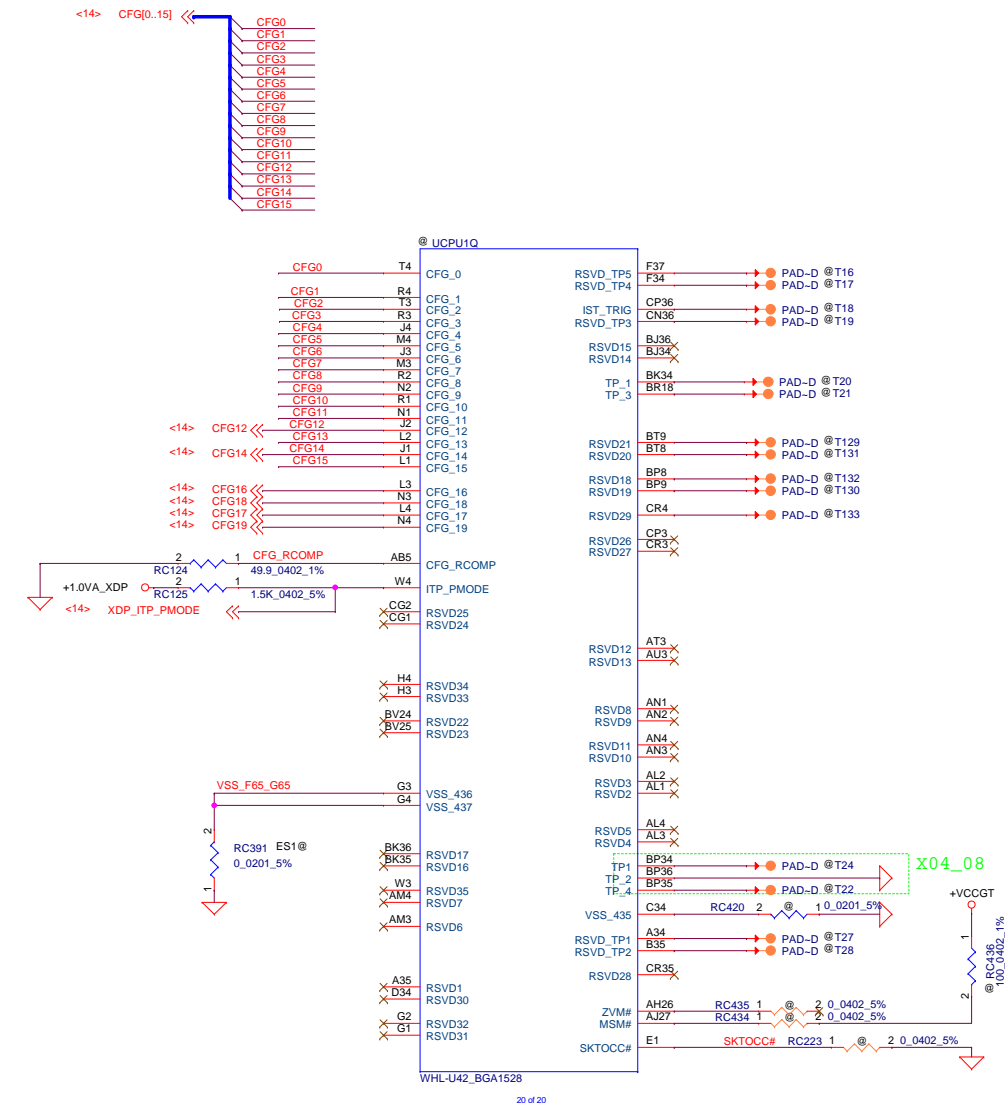
Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

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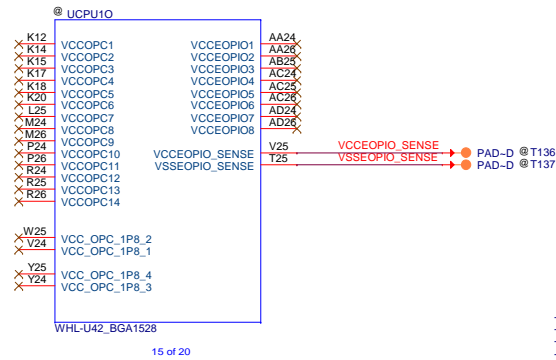
Title	P12-MCP(7/14)MISC,JTAG,HDA,SDIO	
Document Number	LA-E671P	
Date	Monday, October 22, 2018	Rev 1.0
Sheet	12	of 100



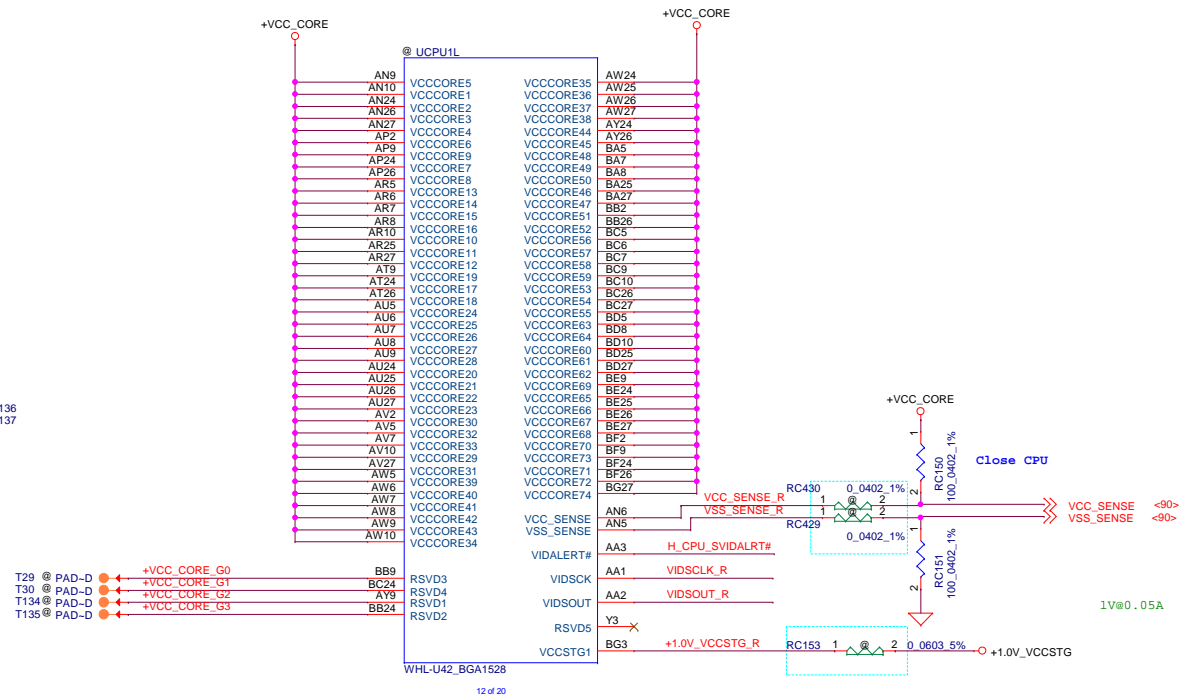


+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A

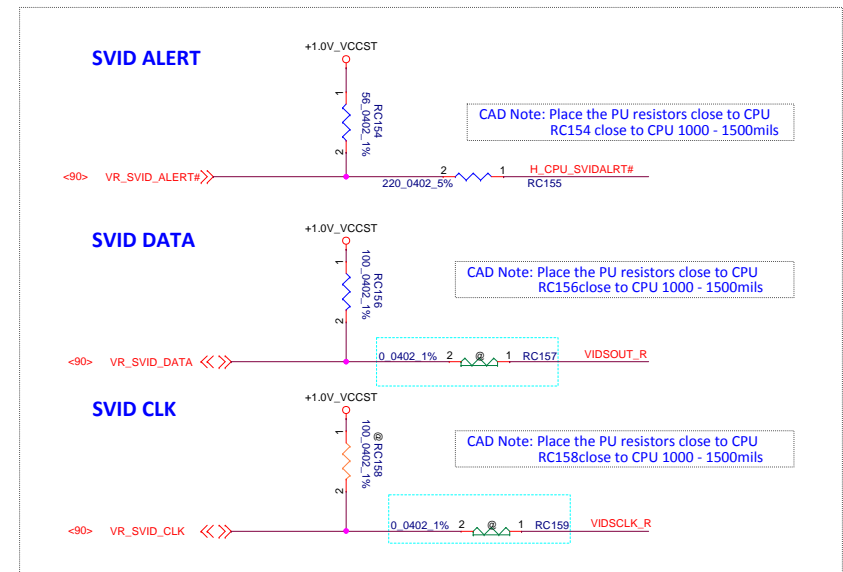
Pin Number	CPLD Use	WHL U42 CS/Production	CNL U22/WHL-U42 ES01
AH26	ZVMH	RSVD	RSVD
T25	VSSOEOP10_SENSE	RSVD	RSVD
V25	VCCOEOP10_SENSE	RSVD	RSVD
AA24	VCCOEOP10	RSVD	RSVD
AA26	VCCOEOP10	RSVD	RSVD
AB25	VCCOEOP10	RSVD	RSVD
AC24	VCCOEOP10	RSVD	RSVD
AC25	VCCOEOP10	RSVD	RSVD
AC26	VCCOEOP10	RSVD	RSVD
AD24	VCCOEOP10	RSVD	RSVD
AD26	VCCOEOP10	RSVD	RSVD
K12	VCCOPC	RSVD	RSVD
K14	VCCOPC	RSVD	RSVD
K15	VCCOPC	RSVD	RSVD
K17	VCCOPC	RSVD	RSVD
K18	VCCOPC	RSVD	RSVD
K20	VCCOPC	RSVD	RSVD
L25	VCCOPC	RSVD	RSVD
M24	VCCOPC	RSVD	RSVD
M26	VCCOPC	RSVD	RSVD
P24	VCCOPC	RSVD	RSVD
P26	VCCOPC	RSVD	RSVD
R24	VCCOPC	RSVD	RSVD
R25	VCCOPC	RSVD	RSVD
R26	VCCOPC	RSVD	RSVD
Y24	VCC_OPC_1P8	RSVD	RSVD
Y25	VCC_OPC_1P8	RSVD	RSVD
V24	VCC_OPC_1P8	RSVD	RSVD
W25	VCC_OPC_1P8	RSVD	RSVD
A127	MSMH	RSVD	RSVD
G4	VSS	RSVD	RSVD
G3	VSS	RSVD	RSVD
G24	VSS	RSVD	RSVD



+V1.8S_EDRAM: 1.8V, 50mA - REMOVE
+VCC_EOPIO: 0.8~1V, 2A - REMOVE

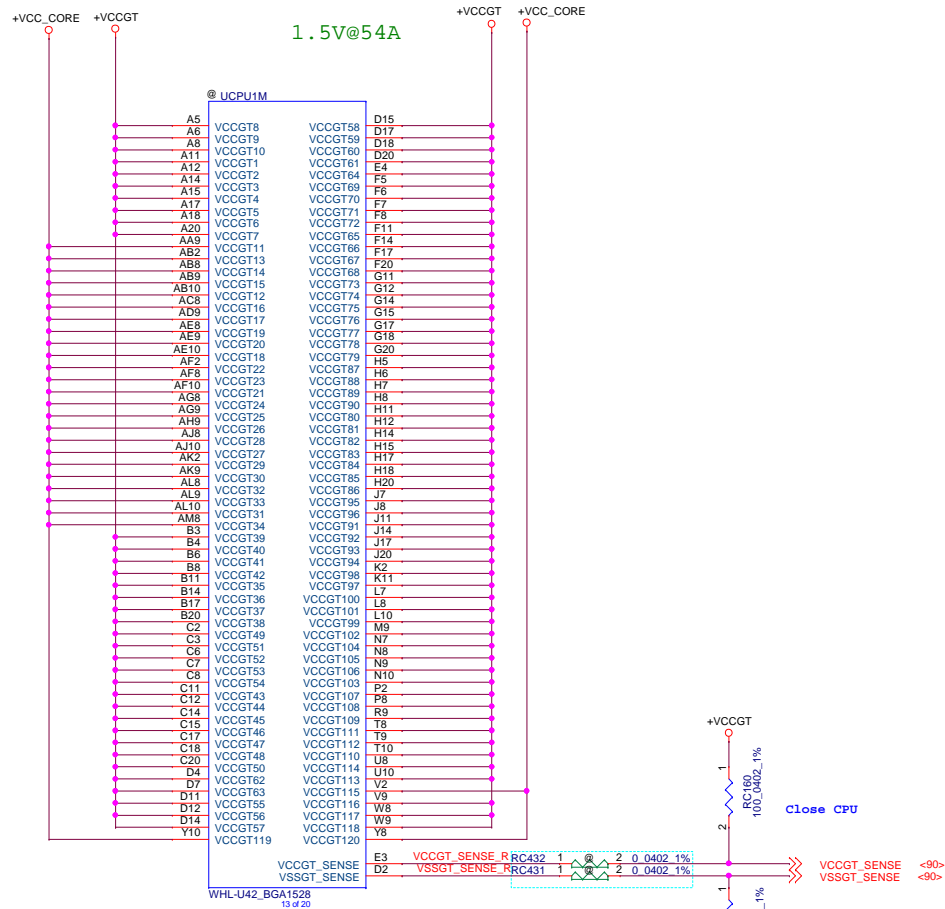


VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



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Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
AM9	VCCGT	VCCGT	VCCCORE
AM10	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE



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Title: **P16-MCP(11/14)PWR-VCCGT**

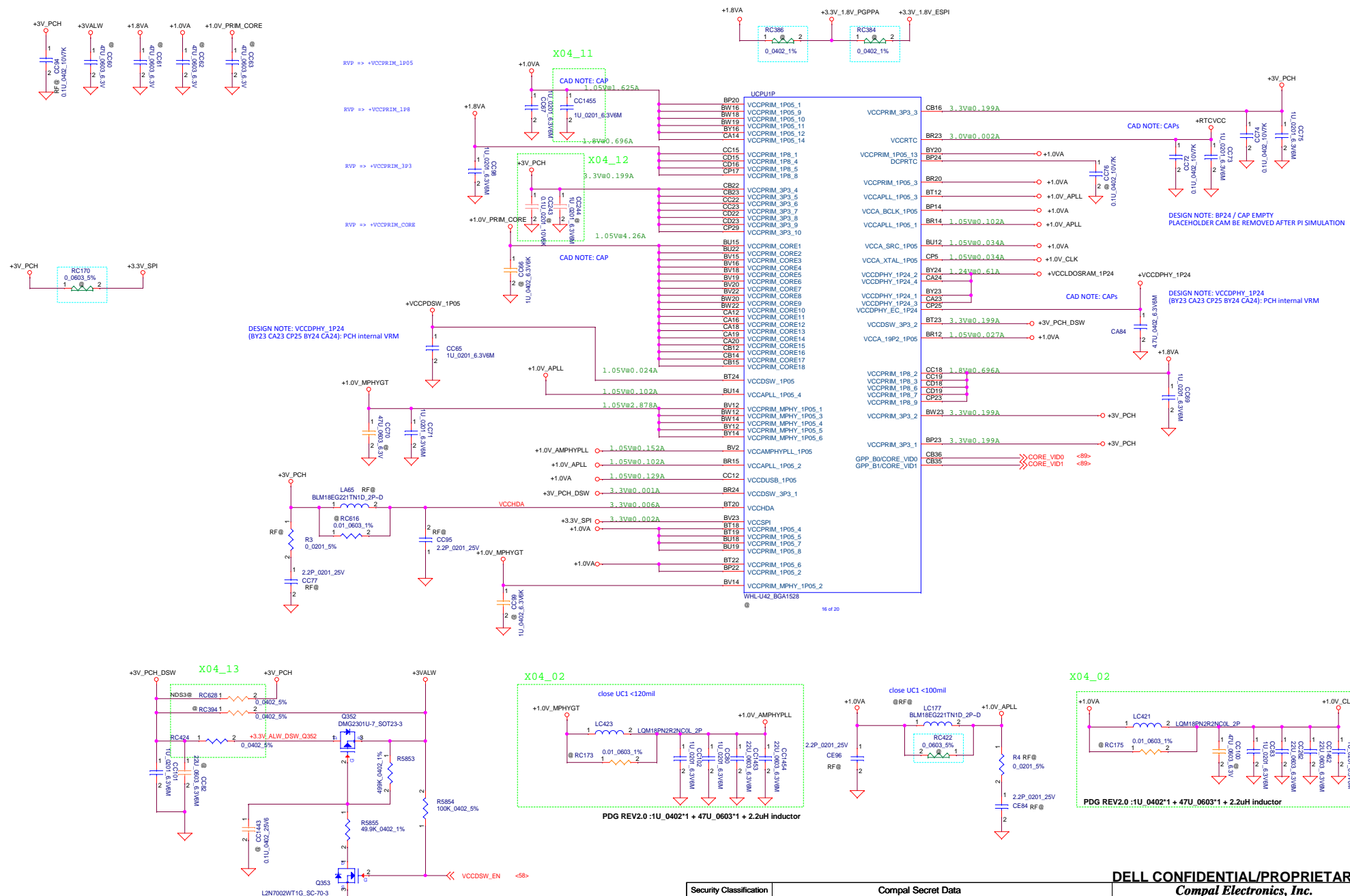
Document Number: **LA-E671P**

Date: Monday, October 22, 2018 Sheet 16 of 100

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PCH PWR

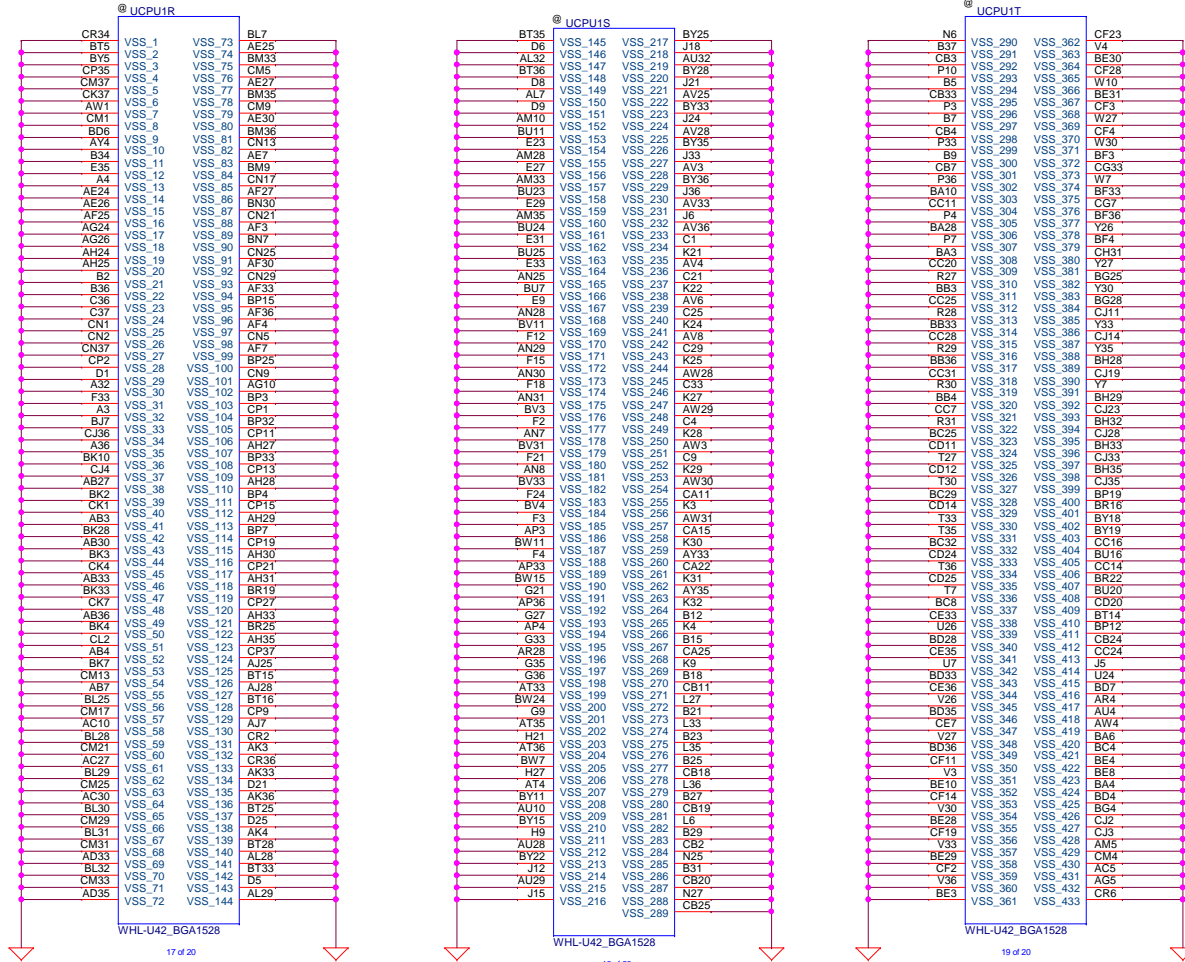


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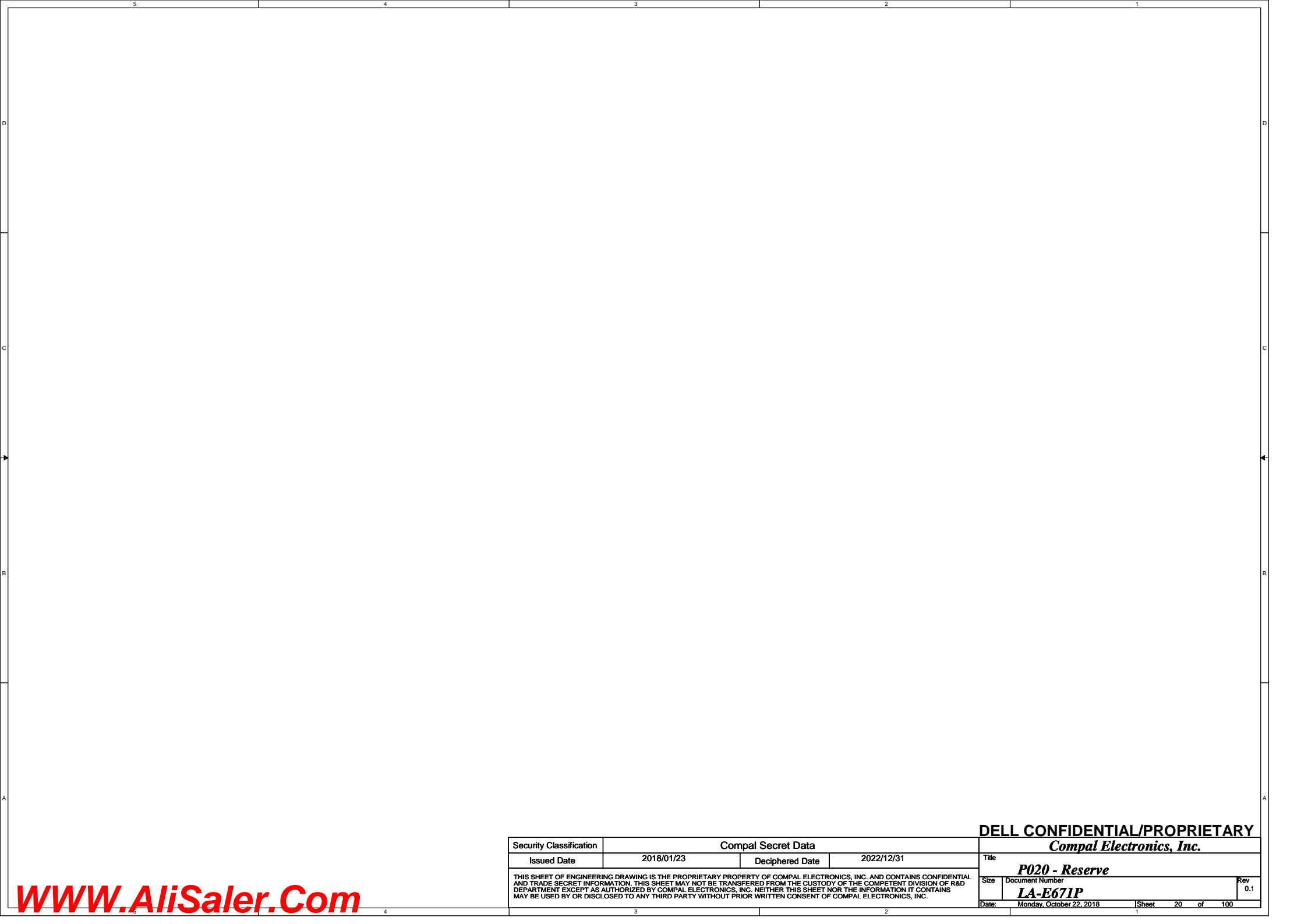
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Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation



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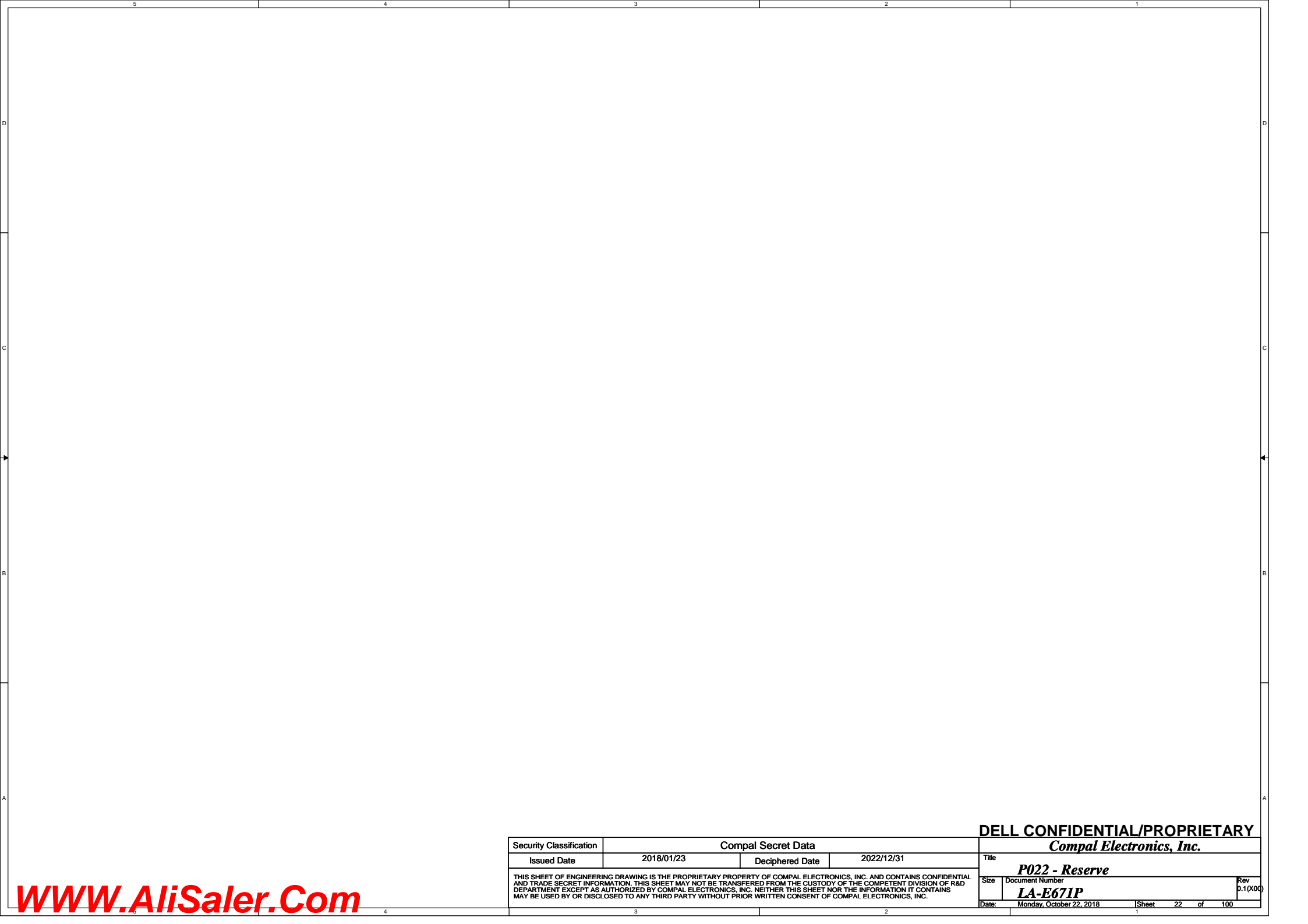
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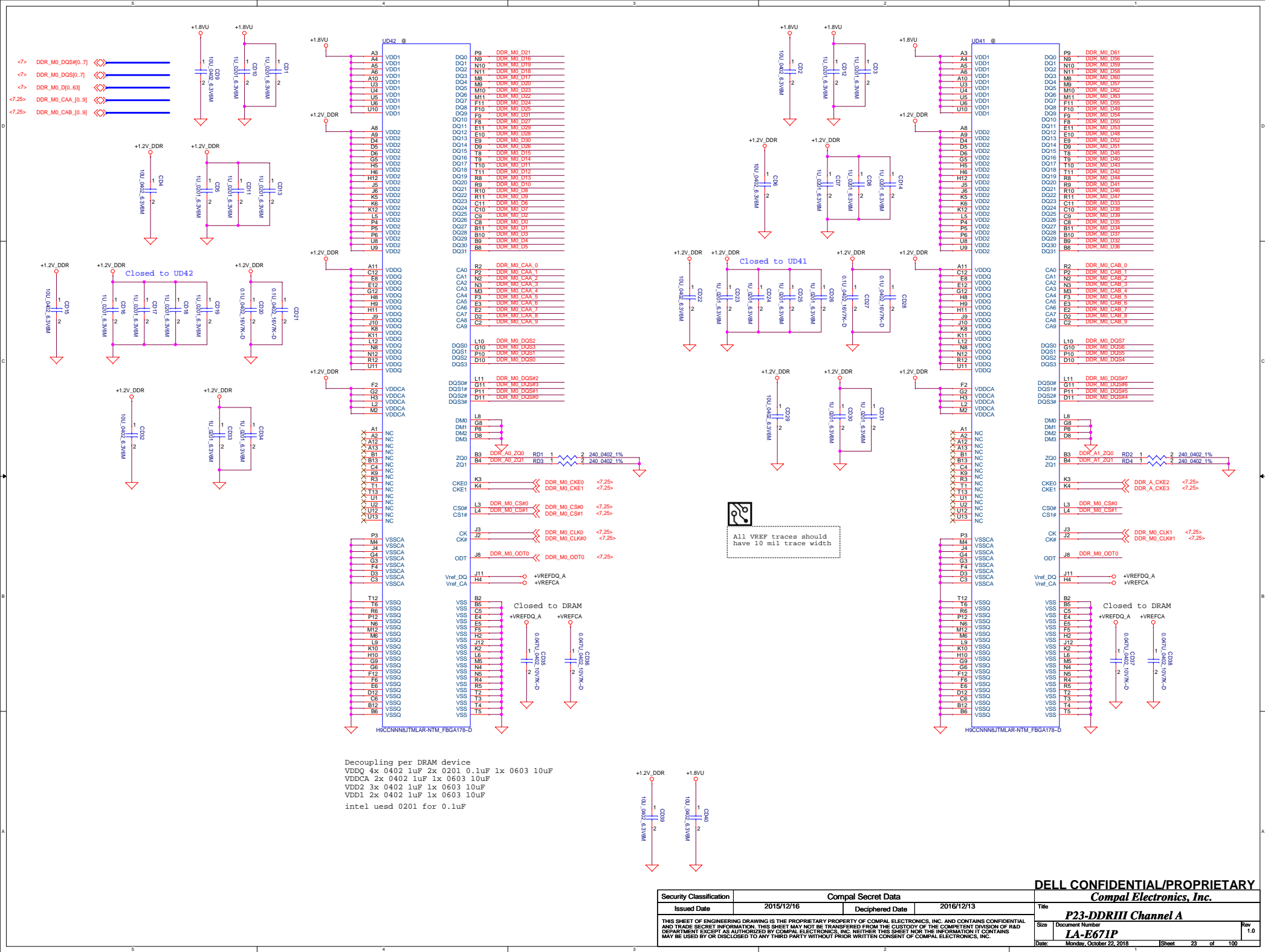


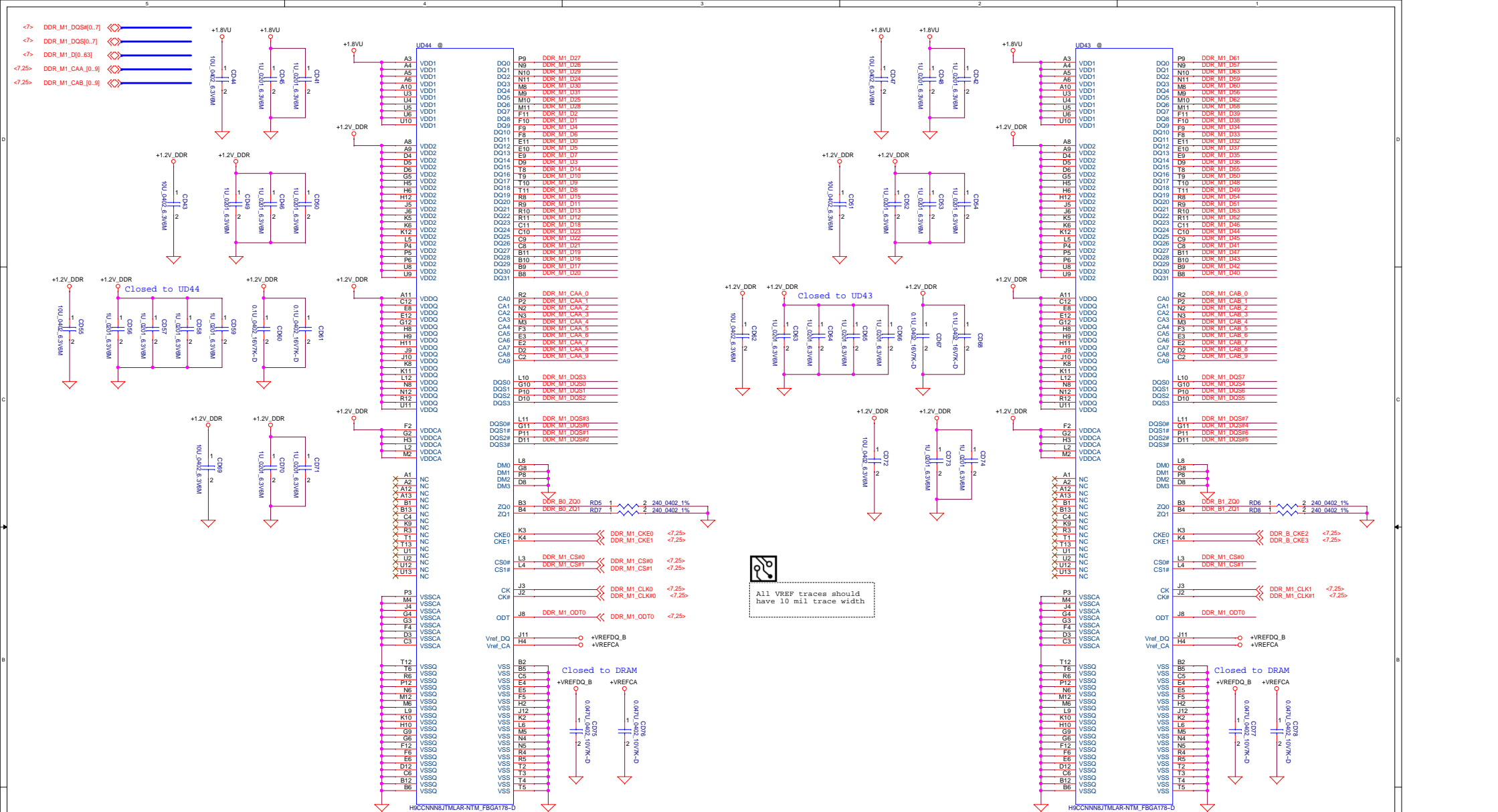
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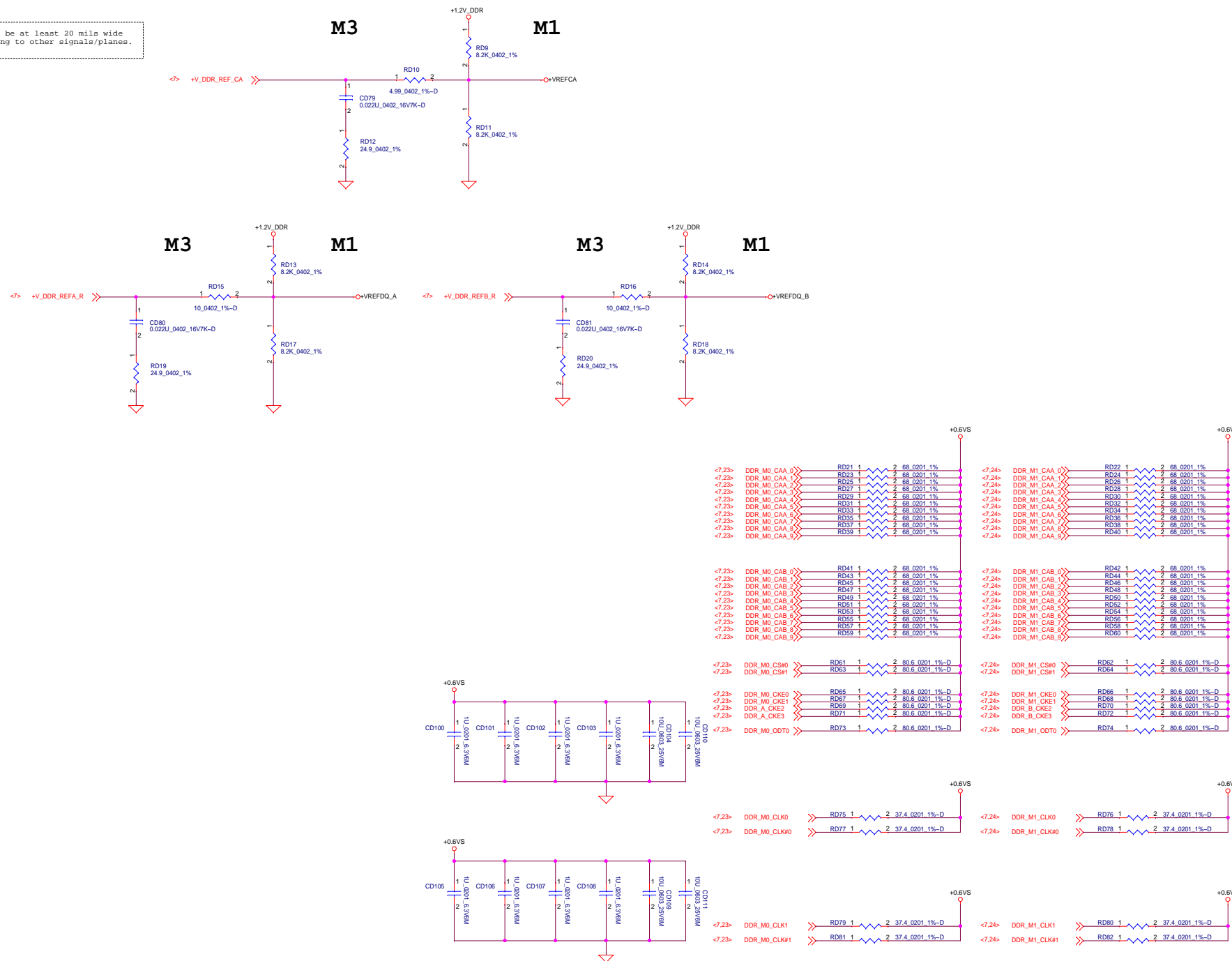




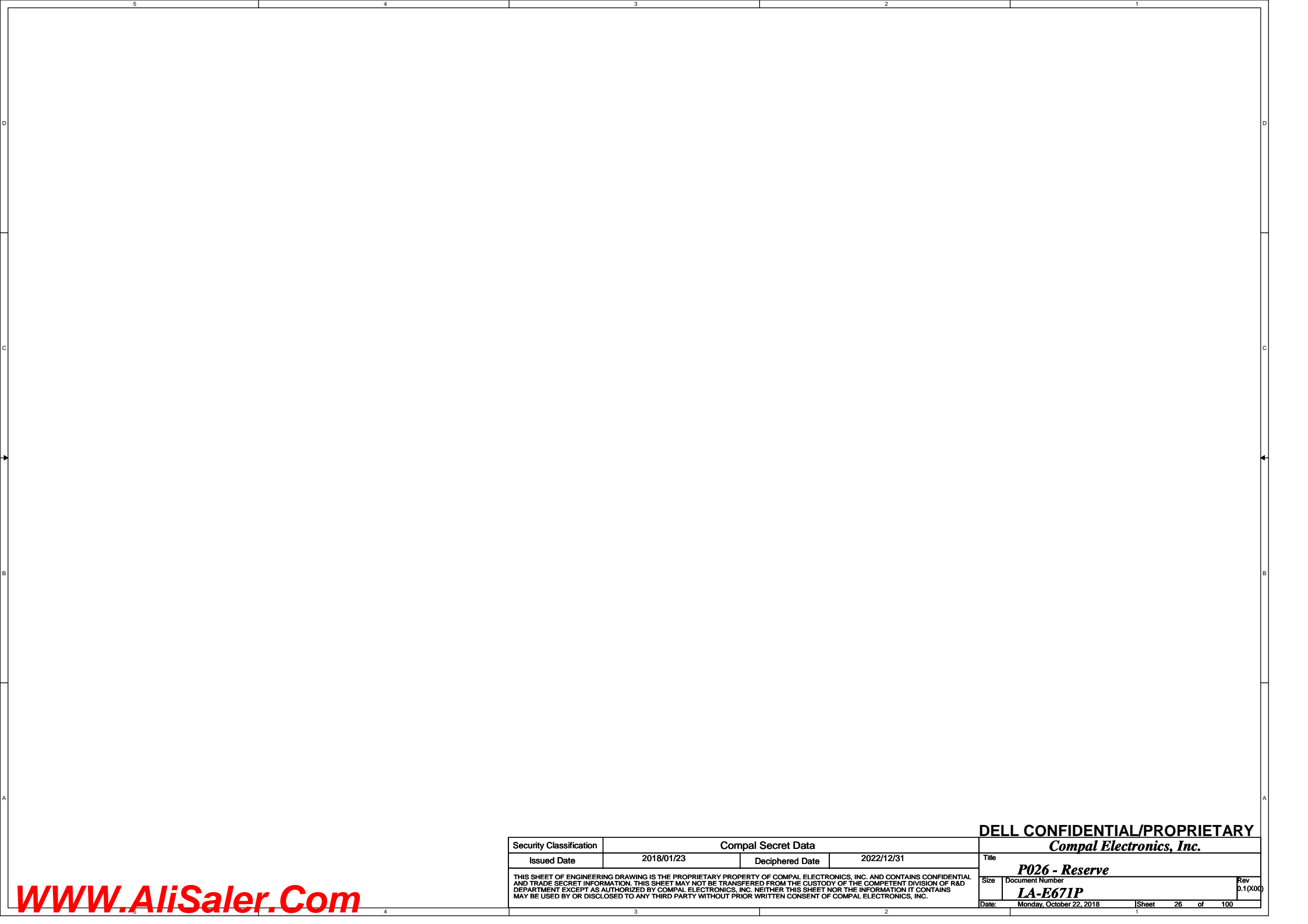
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VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.



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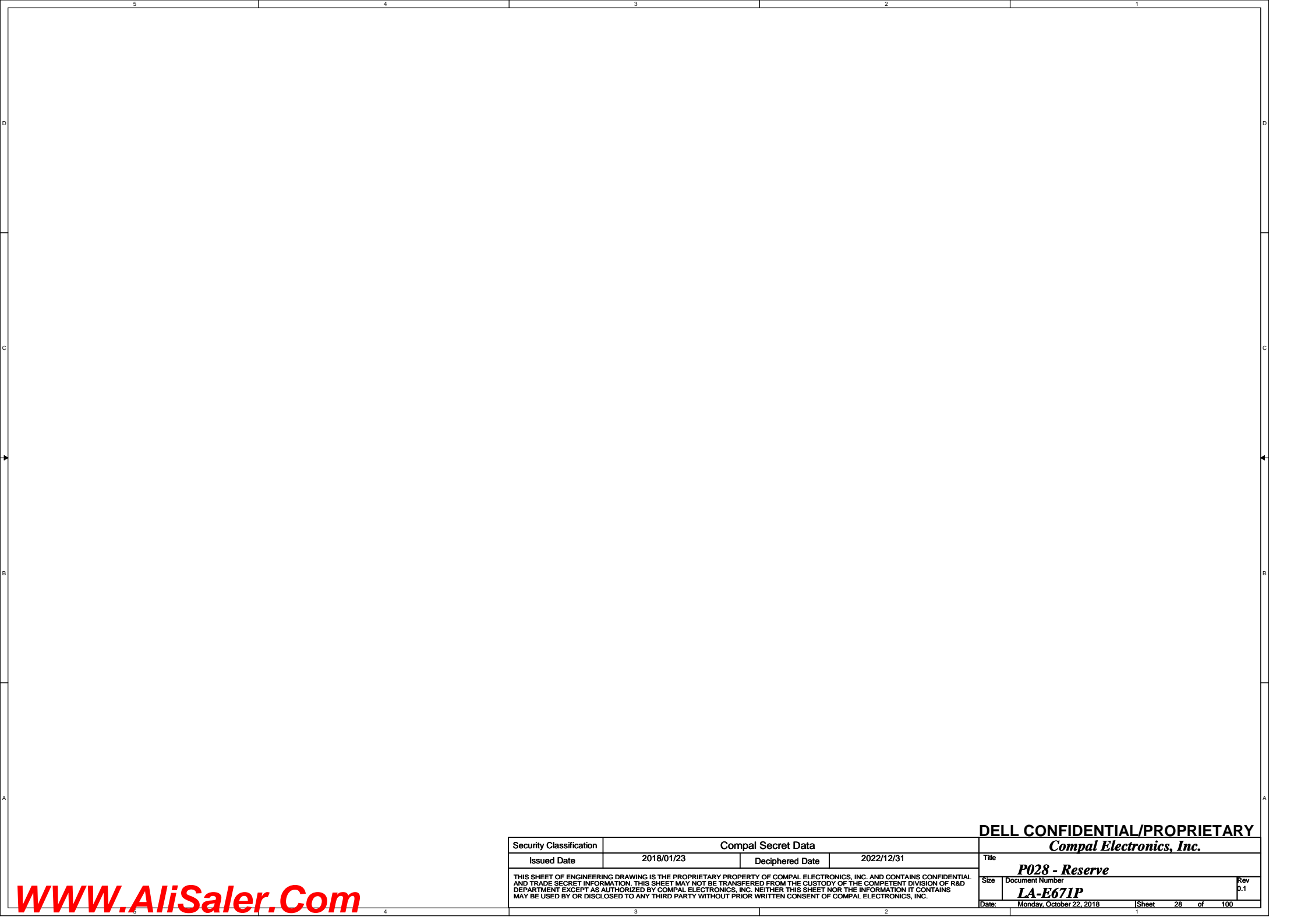


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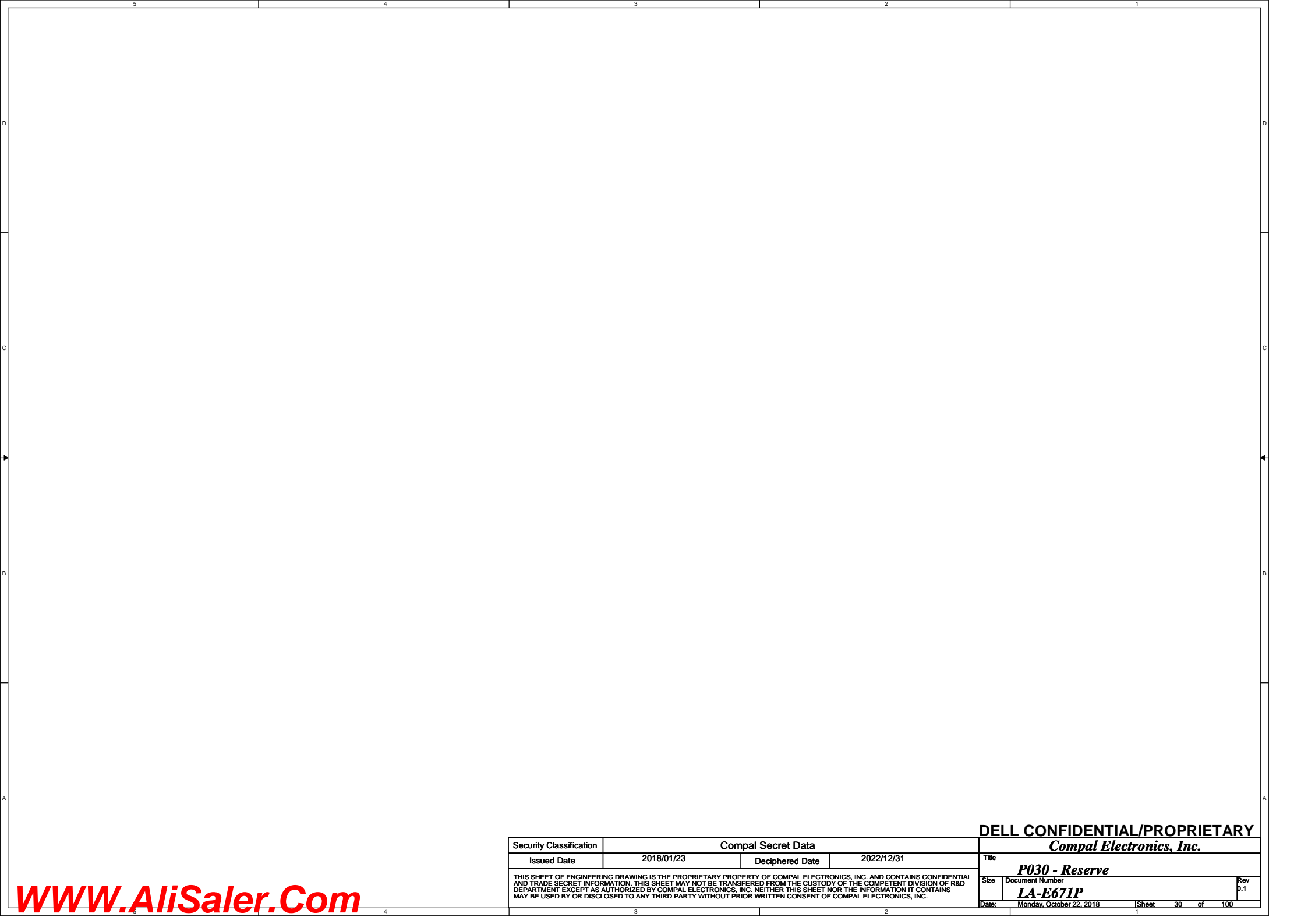


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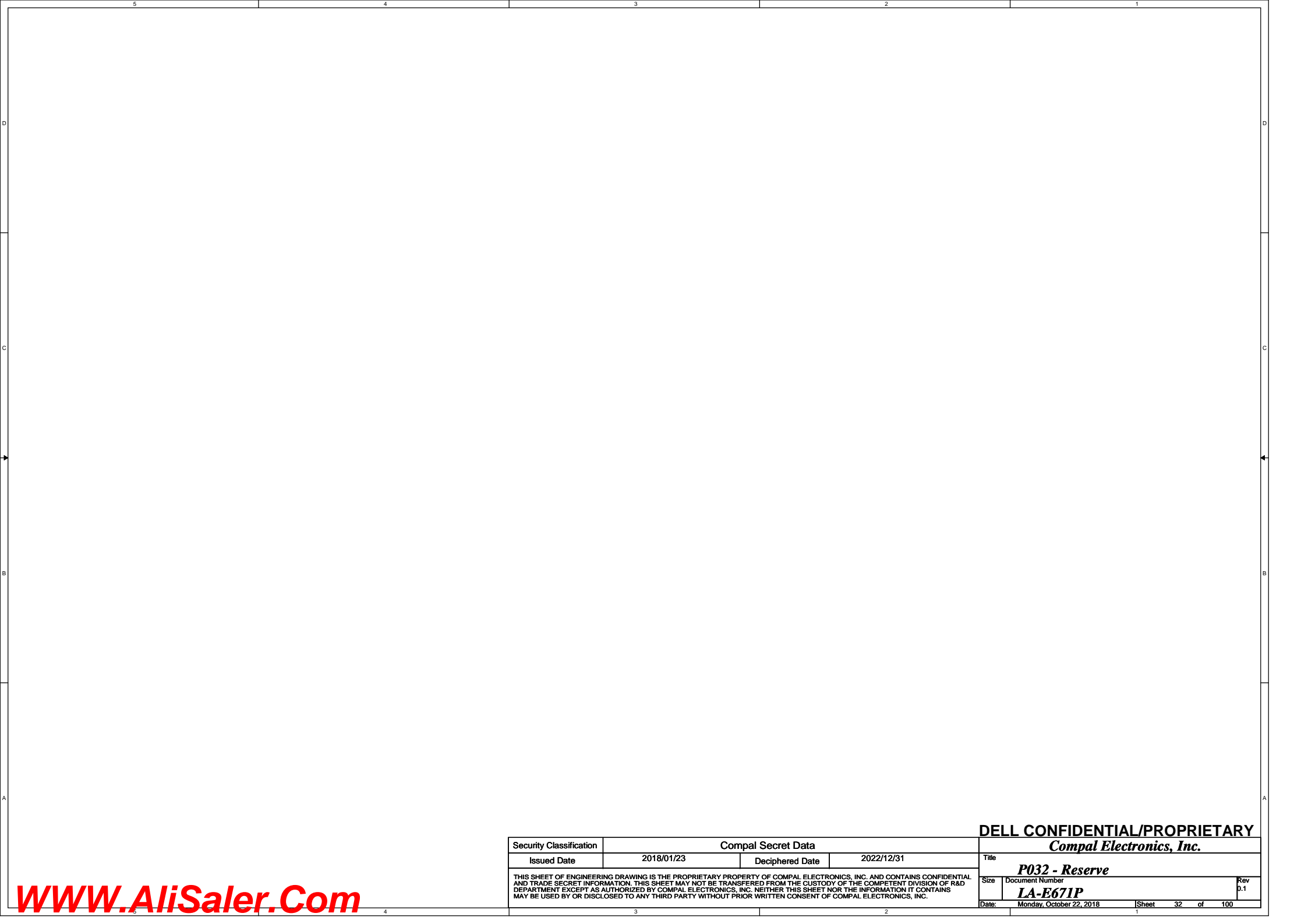


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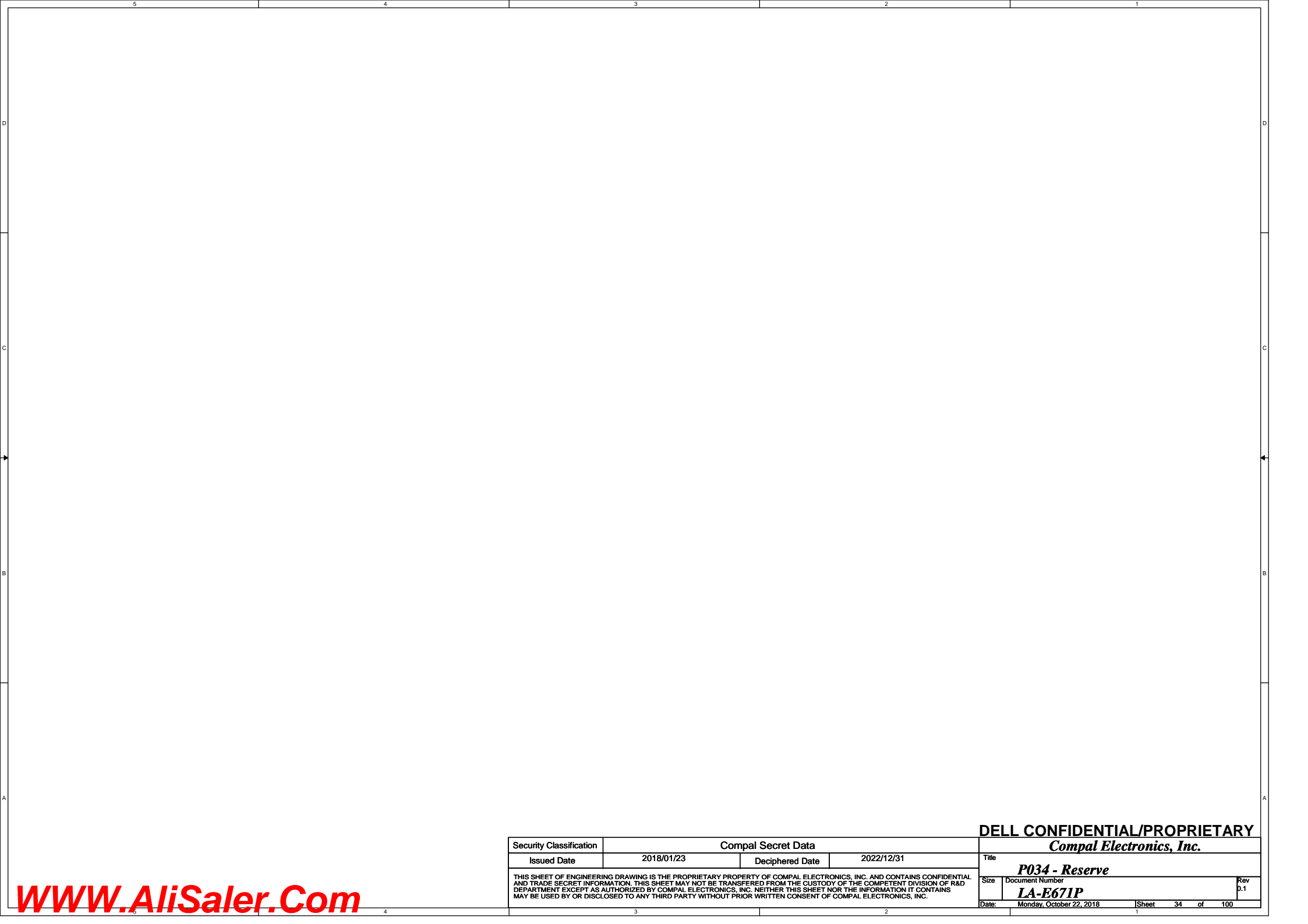


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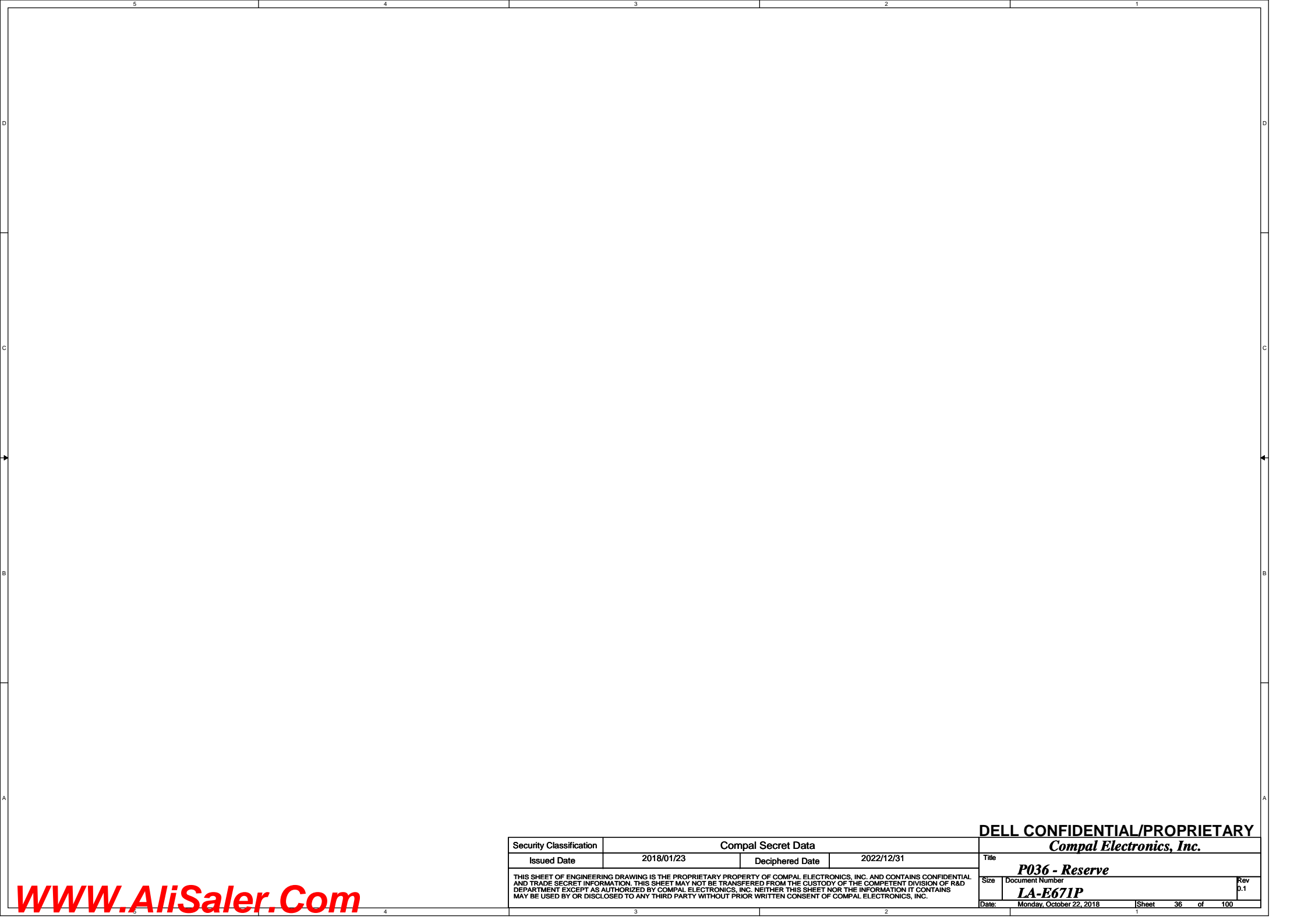
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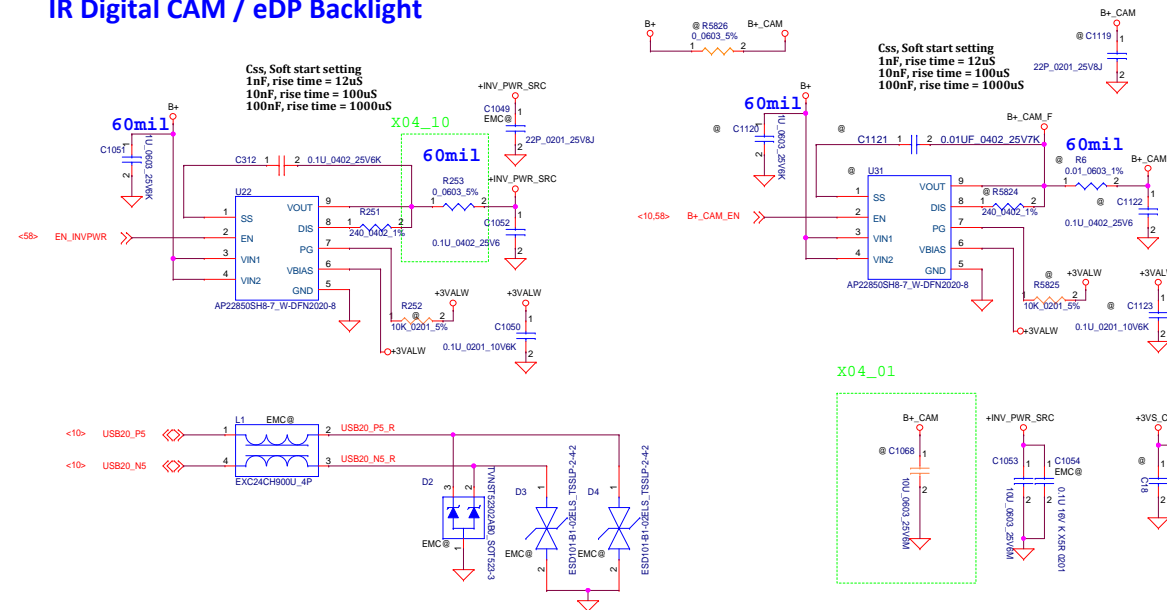
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IR Digital CAM / eDP Backlight

Css, Soft start setting
1nF, rise time = 12uS
10nF, rise time = 100uS
100nF, rise time = 1000uS

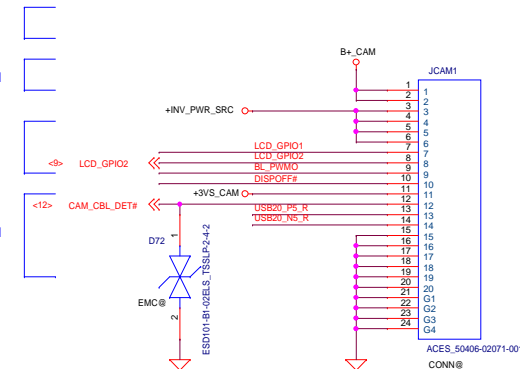


ALS

CAM & IR CAM

LCD BL Power

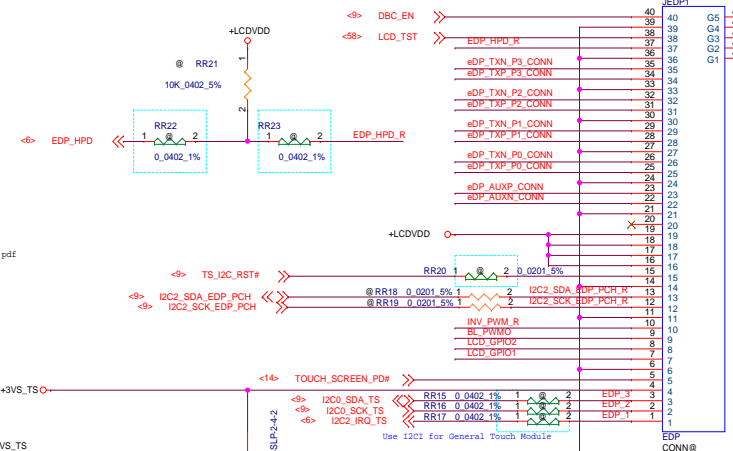
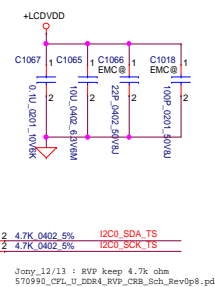
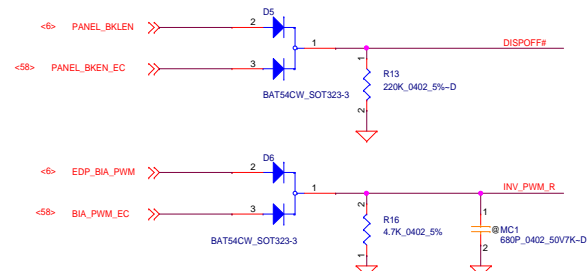
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eDP Conn



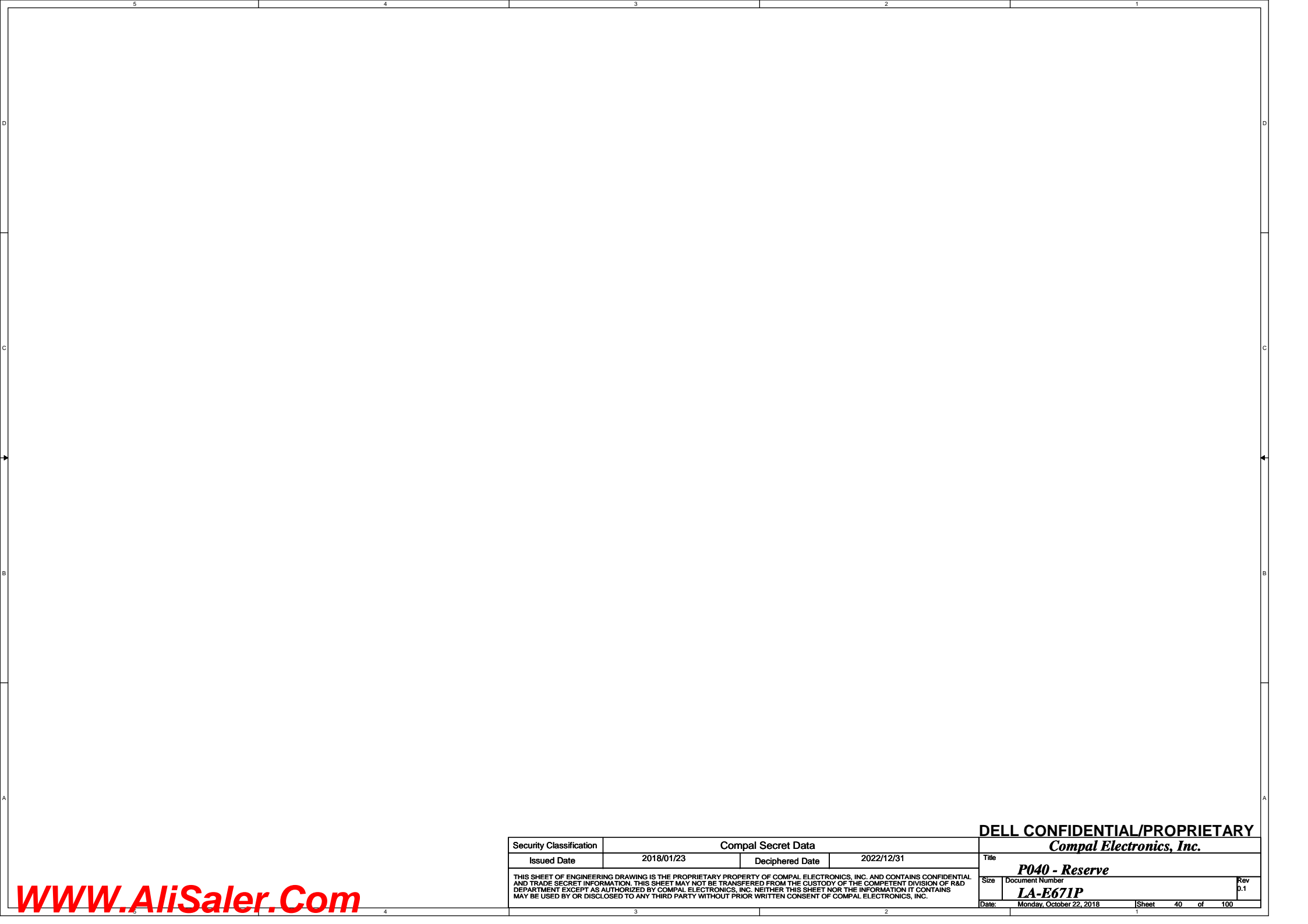
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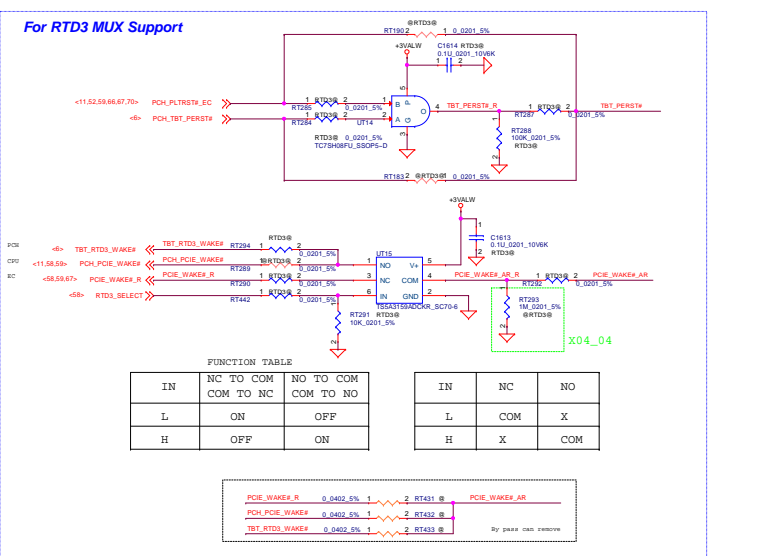
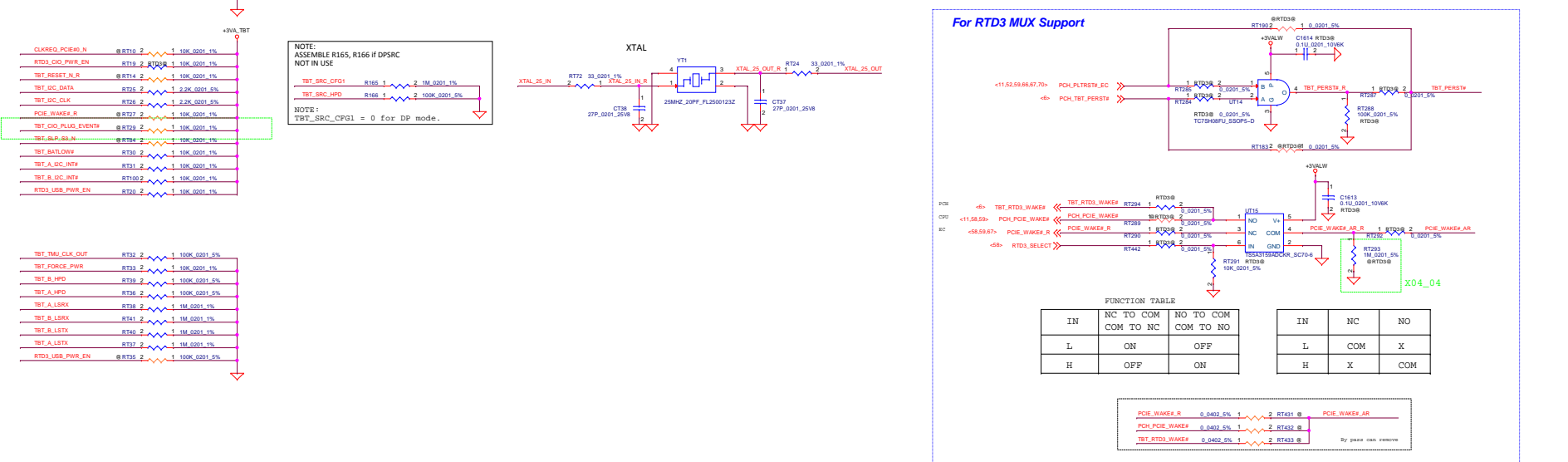
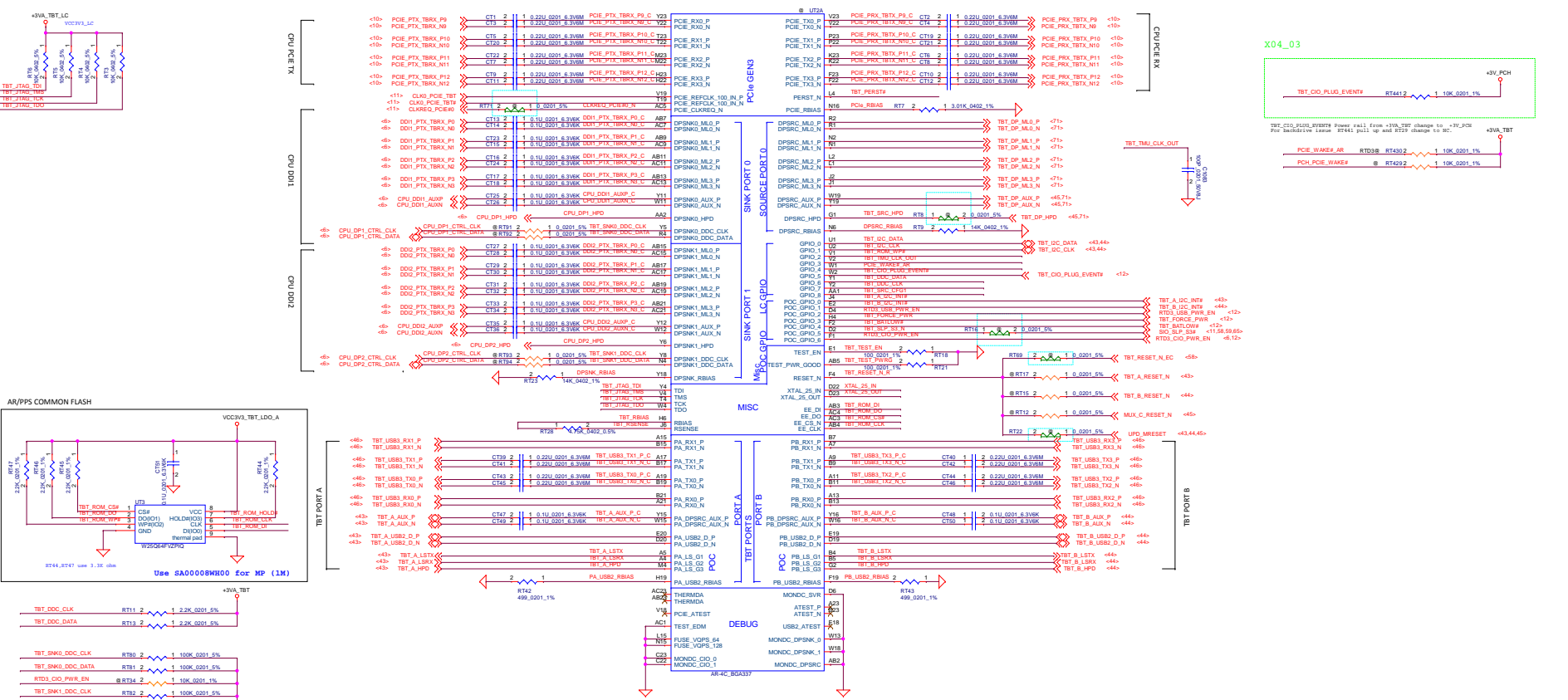
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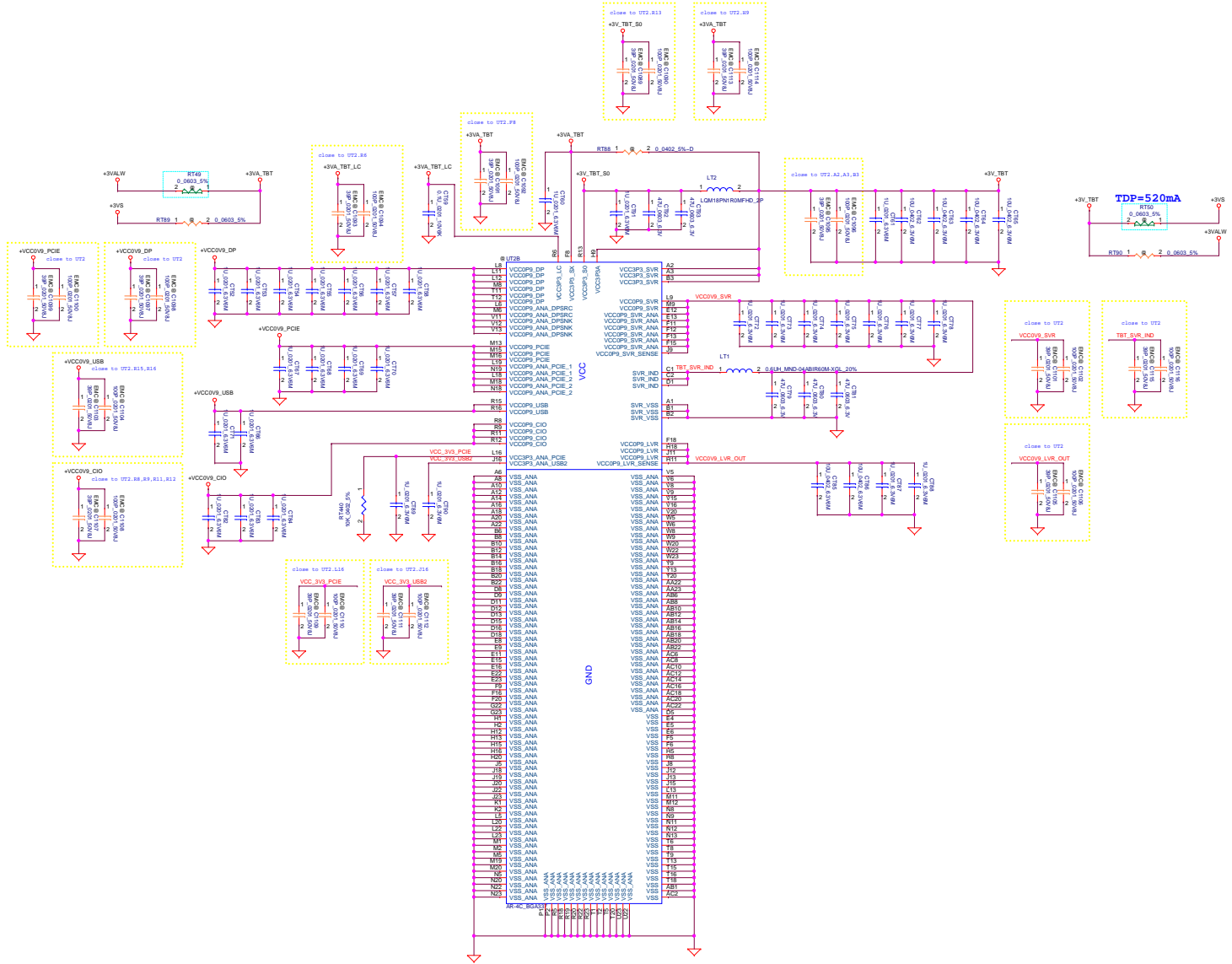
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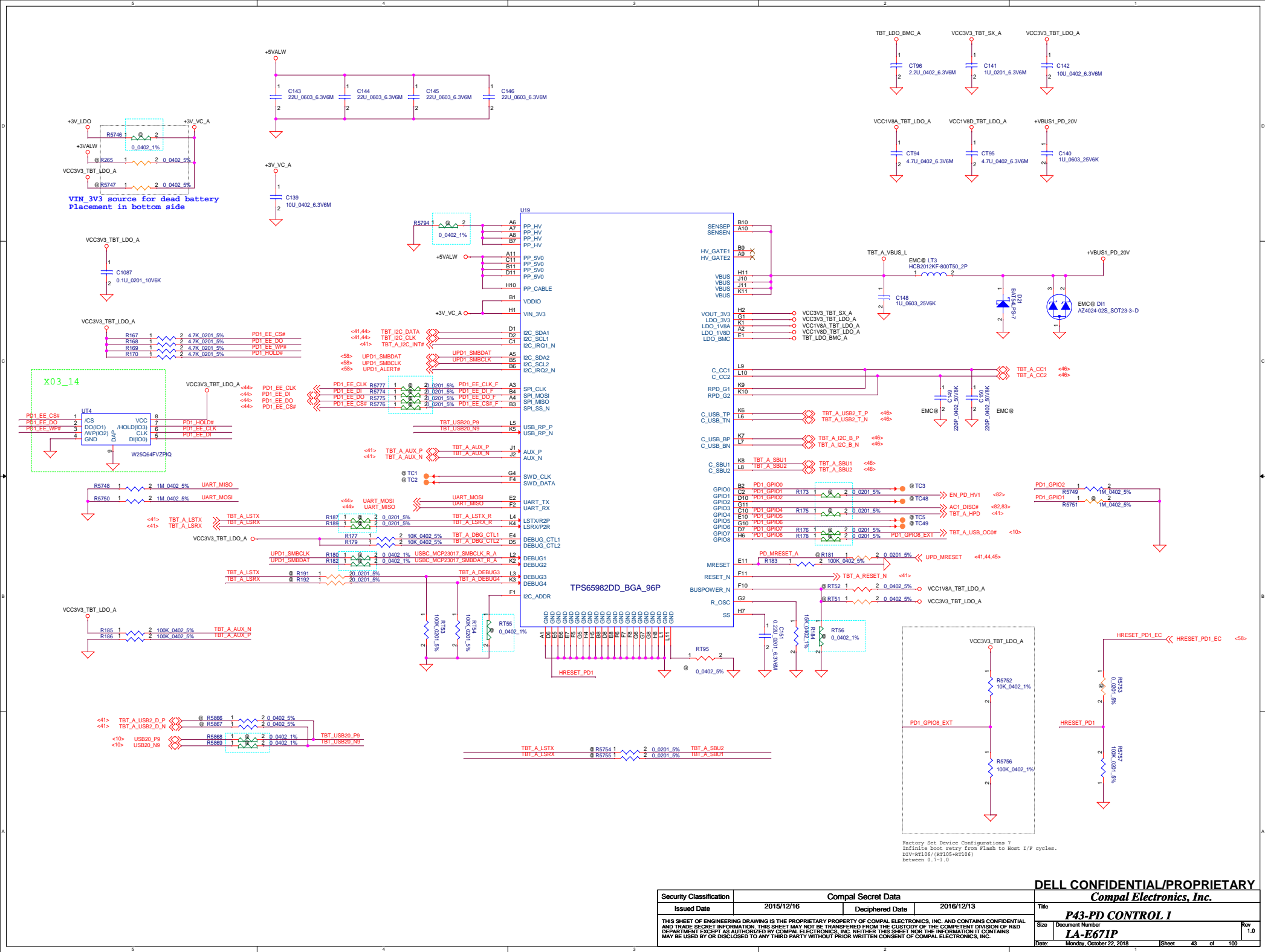
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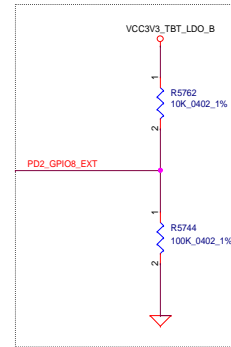
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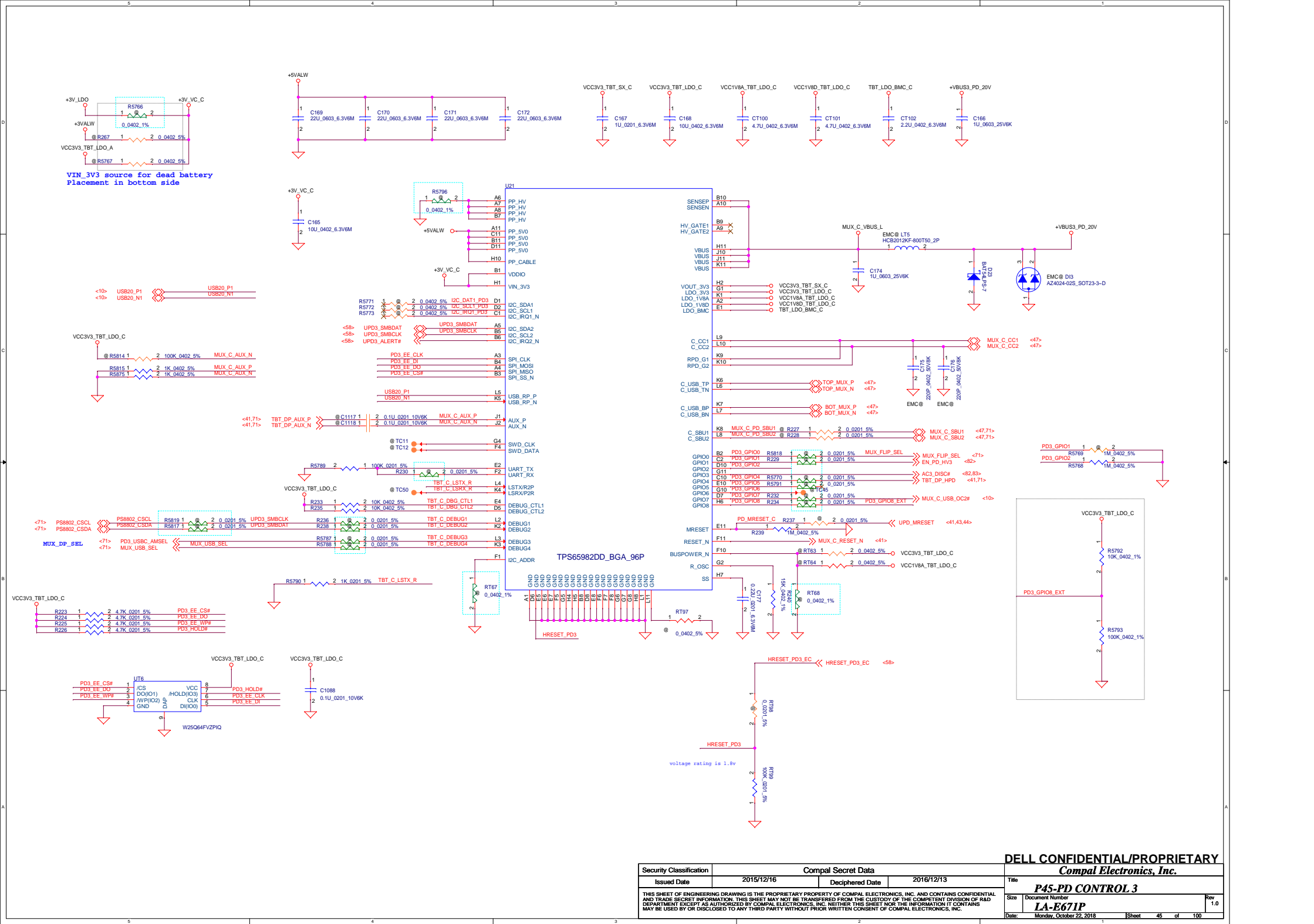
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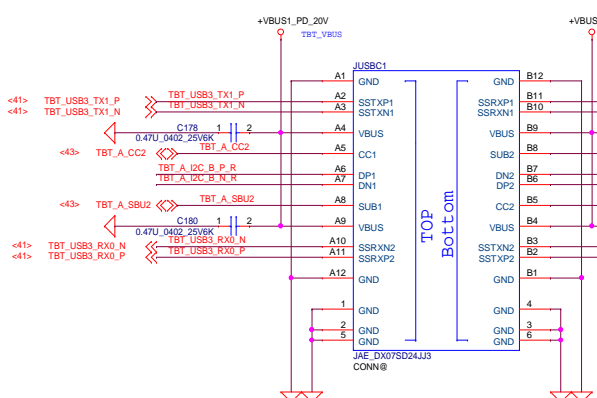
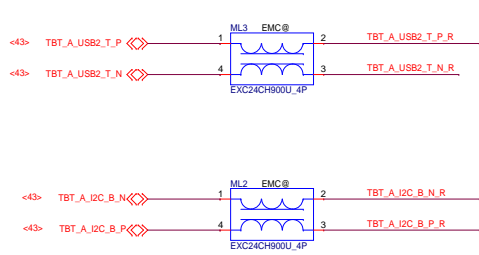




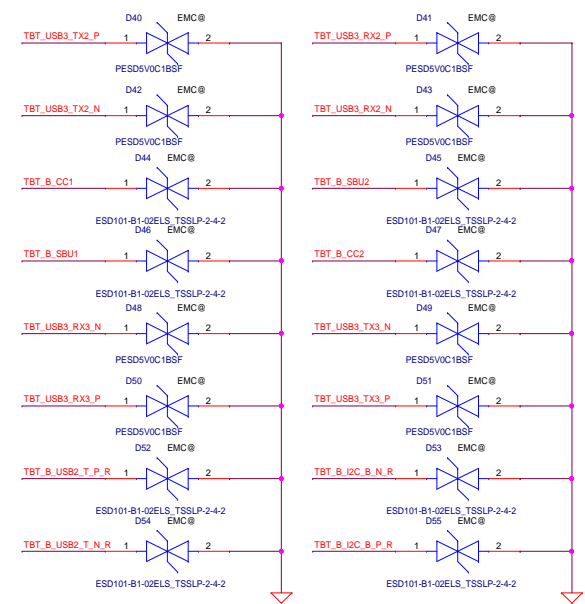
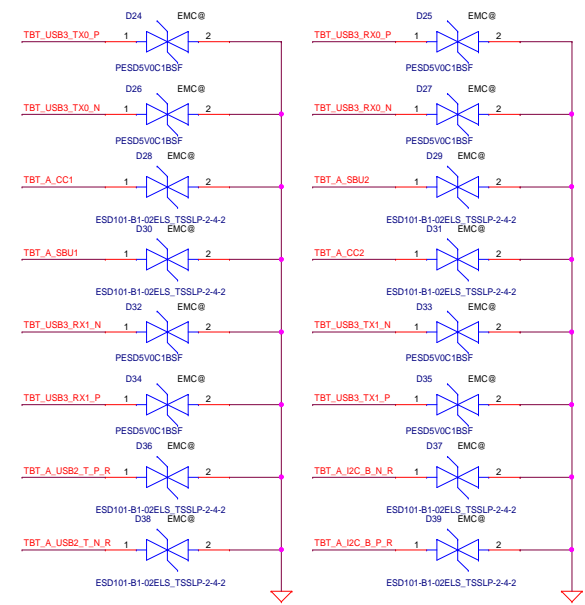
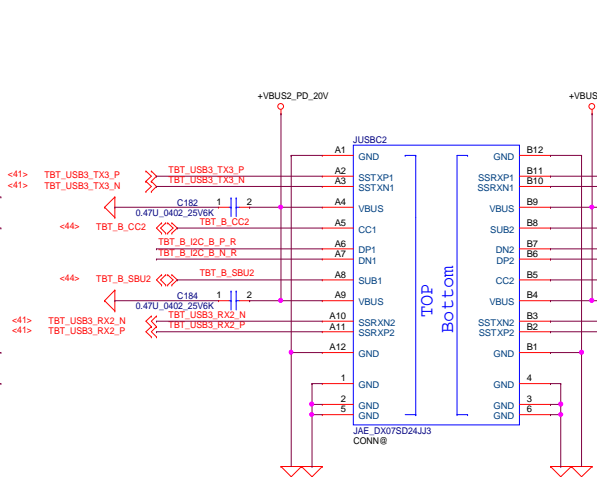
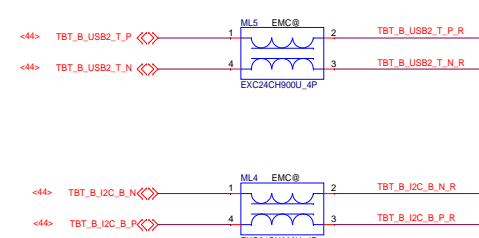


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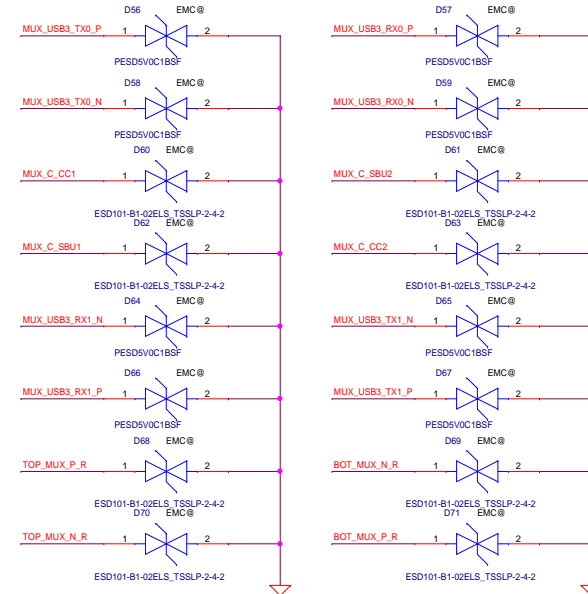
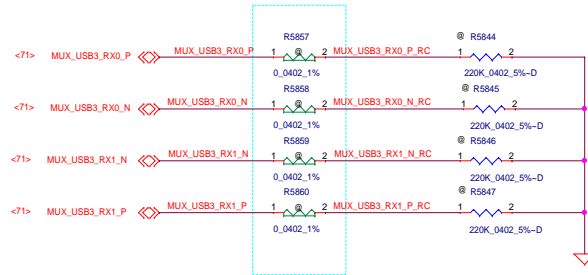
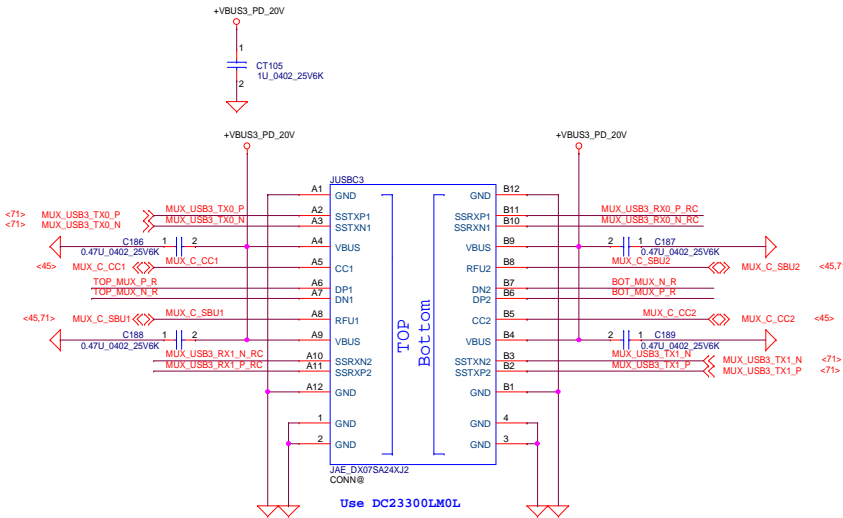
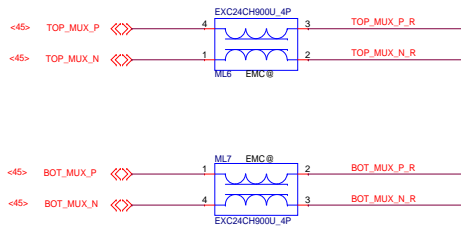


JUSBC1 and JUSBC2 use SP060009R0L

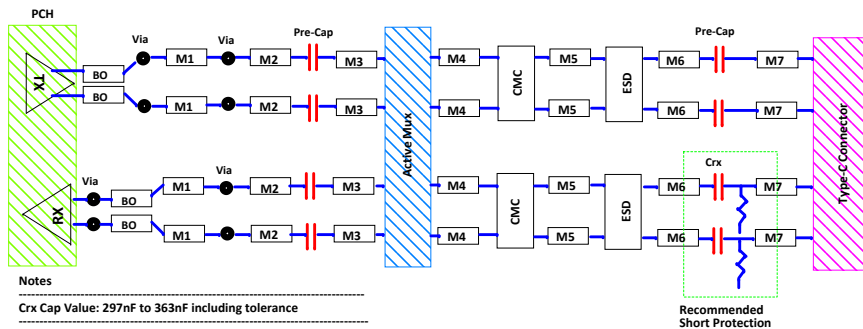


Security Classification				Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date				2015/12/16		2016/12/13	
Deciphered Date				2016/12/13		2016/12/13	
Title				P46-PD USB TYPE-C TBT 1 & 2		LA-E671P	
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Date				Monday, October 22, 2018		Sheet 46 of 100	

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CNL/CFL Type-C External (Back Panel) Topology with Active Mux



Notes

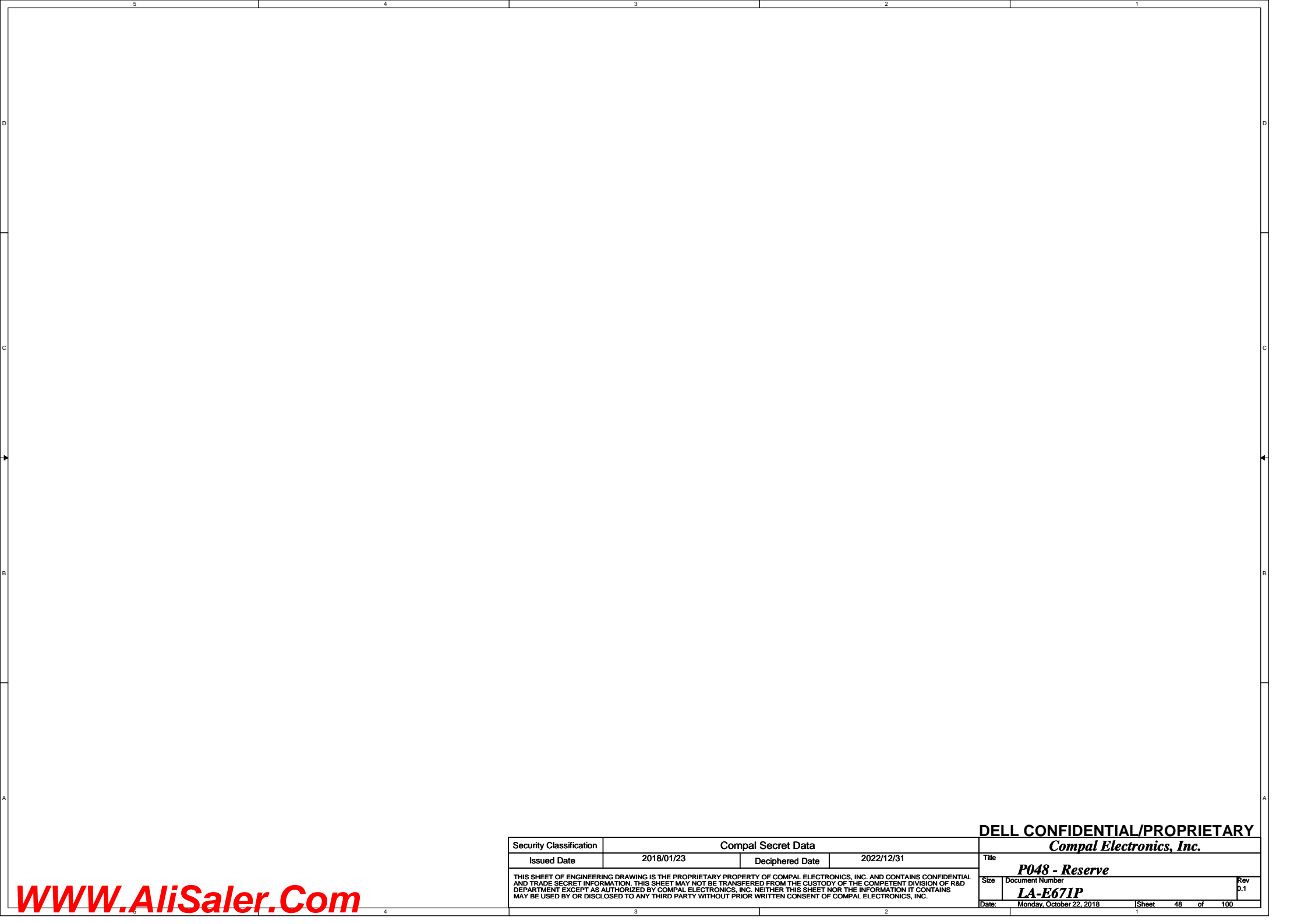
Crx Cap Value: 297nF to 363nF including tolerance

Rb Resistor Value: 220kΩ ±5%

USB3p1_Type_C_CNUpdate_CNUpdate_CNUpdate_CNUpdate_CNUpdate .pdf

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Compal Electronics, Inc.			
Title			
P47-PD USB TYPE-C 3			
Size	Document Number	Rev	1.0
C	LA-E671P		
Date:	Monday, October 22, 2018	Sheet	47 of 100

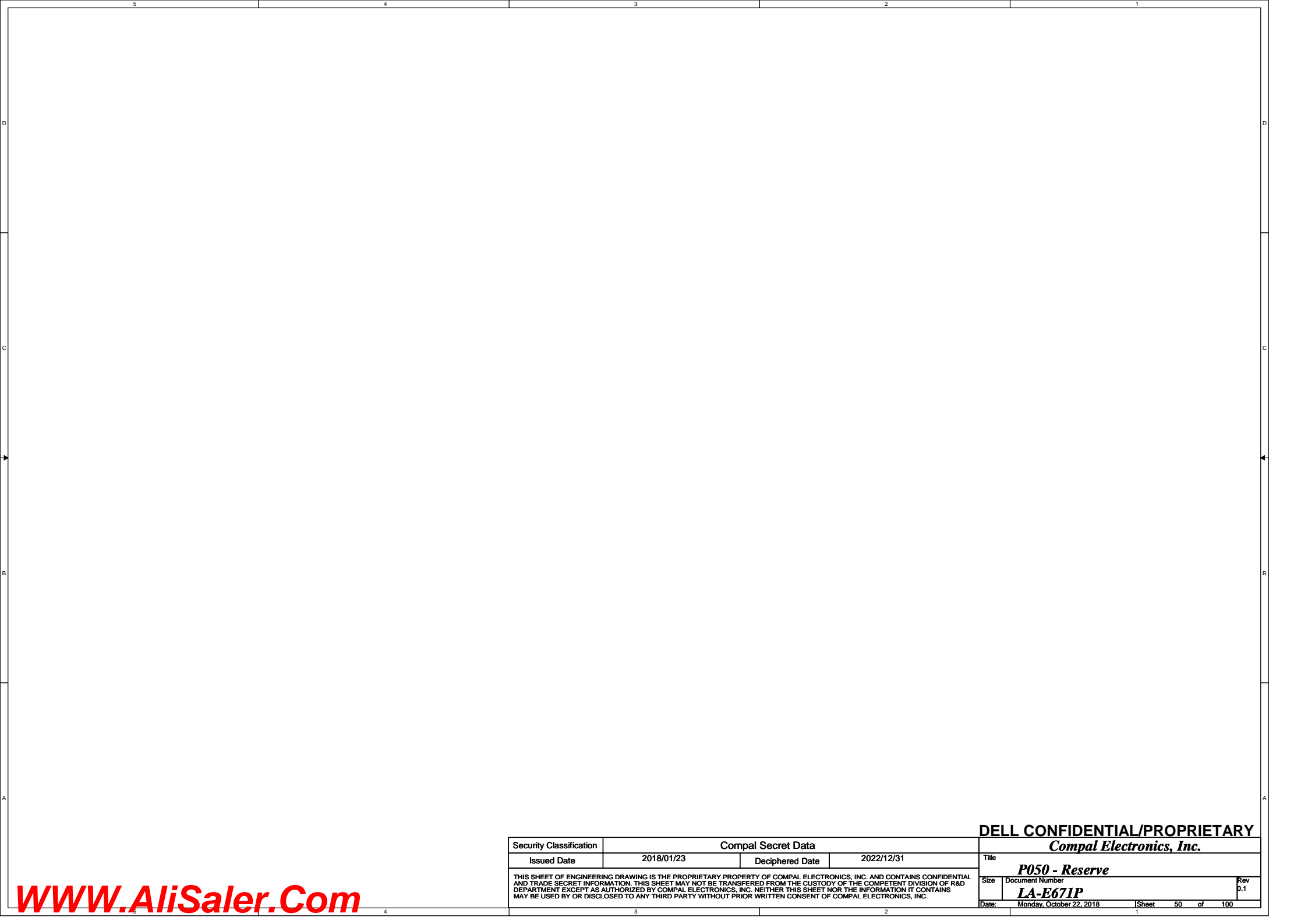


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				Size	Document Number	Rev 0.1	
				LA-E671P			
				Date:			Monday, October 22, 2018
				Sheet	48		of 100



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Issued Date		Deciphered Date		Title	
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				LA-E671P	
				Rev 0.1	
				Date: Monday, October 22, 2018	
				Sheet 49 of 100	



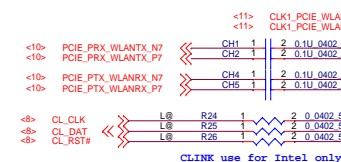
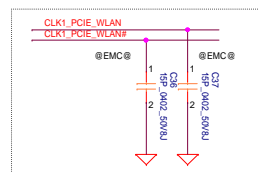
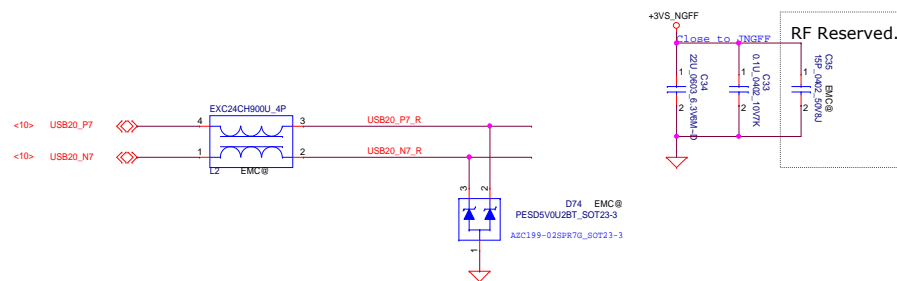
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				Size	Document Number		Rev 0.1
				LA-E671P			
				Date:		Monday, October 22, 2018	
				Sheet		50 of 100	

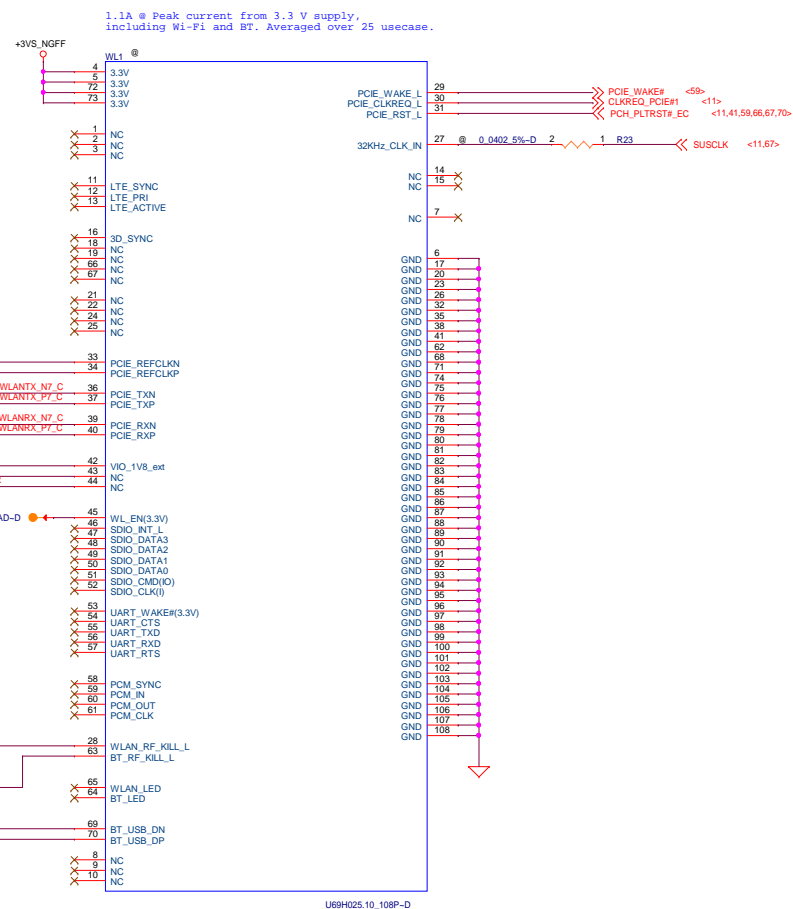
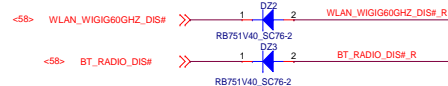


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M.2 Slot-A Key-A (WLAN)



Commodity	WLAN	CPN - R1	
Italia XPS	Killer1435-S	PK29S006810	R24-R26 de-pop
Italia-L	Intel 8265	PK29S00980L	R24-R26 pop



CIS footprint change to Killer1435-S
U69H025.10_108P~D



D

D

C

C

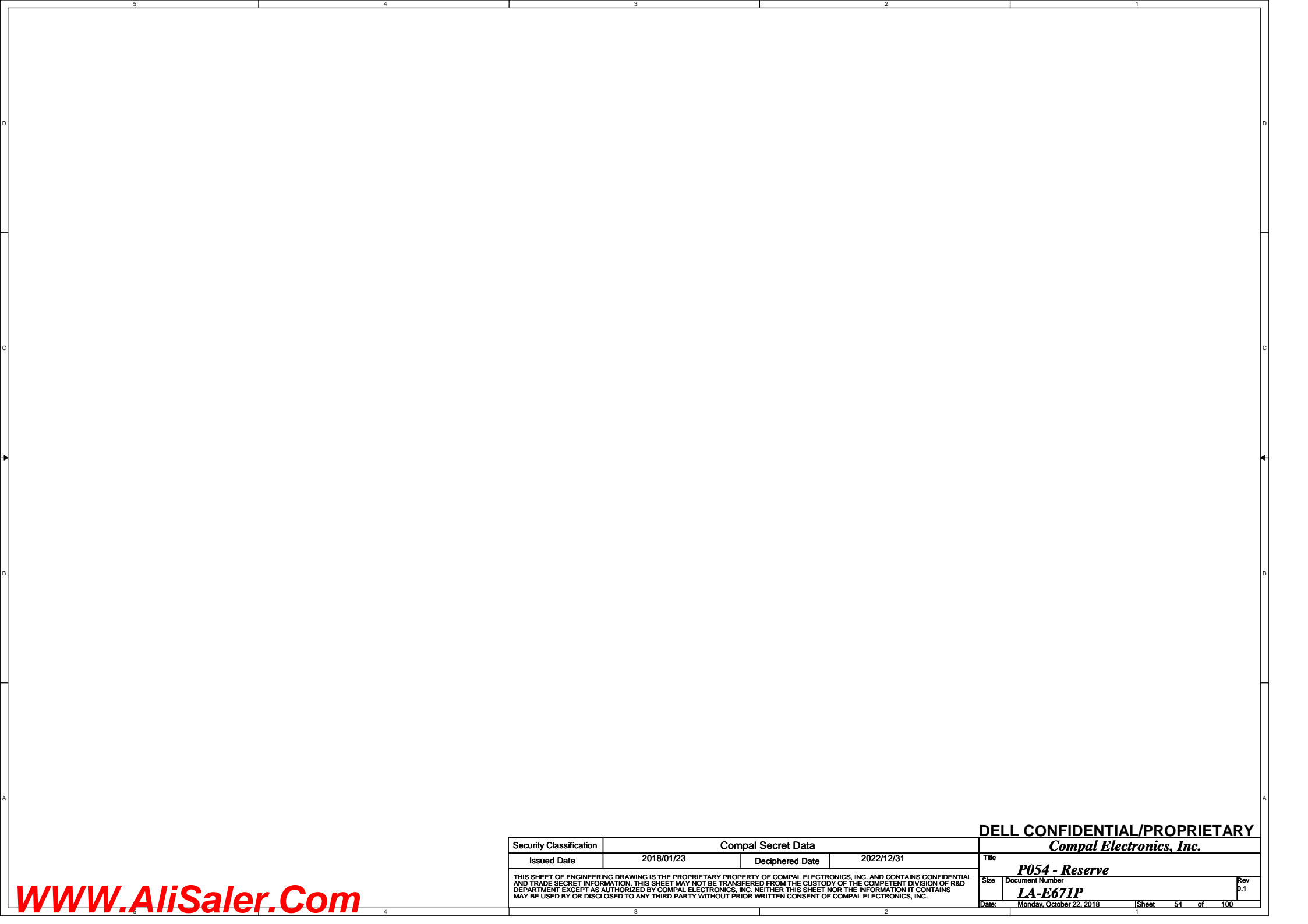
B

B

A

A

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					Size	Document Number	Rev
					LA-E671P		0.1
					Date:	Monday, October 22, 2018	Sheet 53 of 100

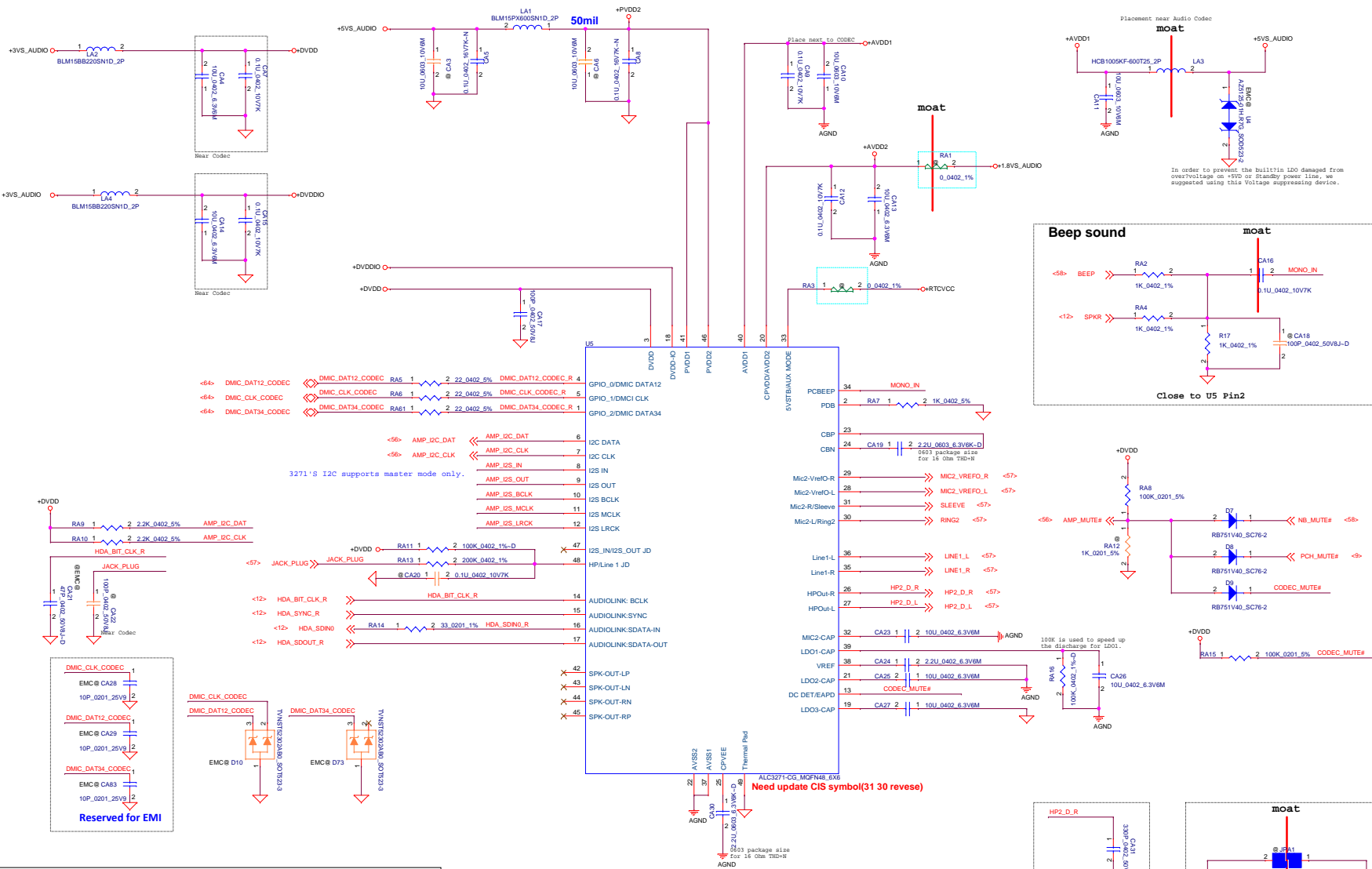


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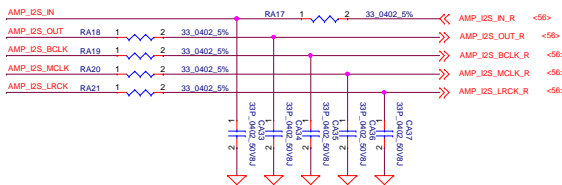
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Issued Date		2018/01/23	Deciphered Date	Compal Electronics, Inc.	
			2022/12/31	Title	
				P054 - Reserve	
				Size	Document Number
				LA-E671P	
				Date	Monday, October 22, 2018
				Sheet	54 of 100
				Rev	0.1

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HD Audio Codec

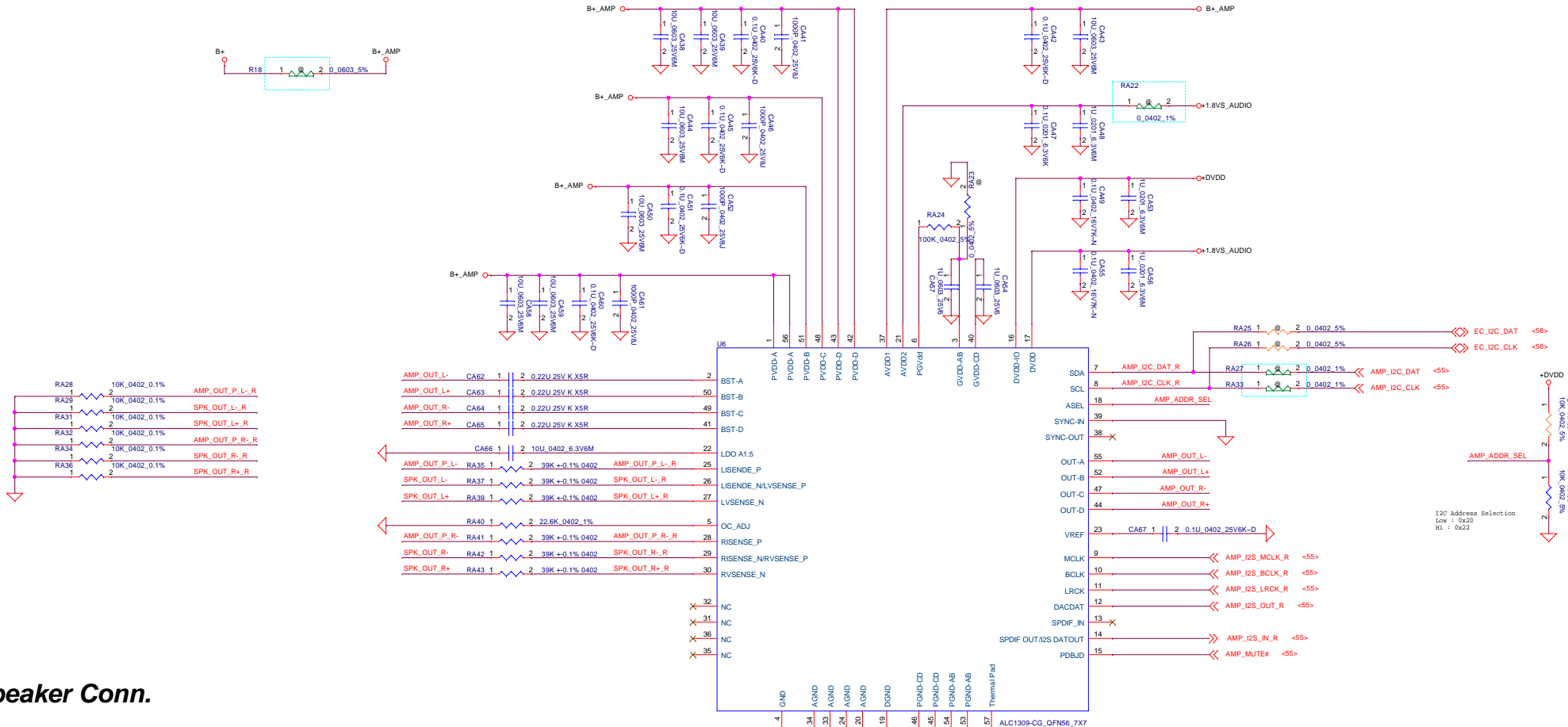


POST I2S interface



Security Classification		Compel Secret Data		<div style="text-align: right;"> ALL INFORMATION CONTAINED HEREIN IS UNCLASSIFIED DATE 01-09-2018 BY 60322 </div>	
Issued Date	2013/07/04	Deciphered Date	2013/10/28	Compel Electronics, Inc. CONFIDENTIAL	
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				Sheet <u>Document Number</u> Rev LA-E671P Monday, October 22, 2018 Sheet 55 of 100 Rev 1.0	

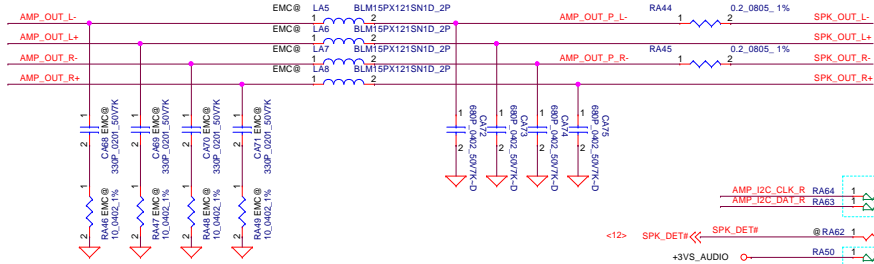
SMART AMP



Int. Speaker Conn.

Use 120 ohm bead
(SMD1000L300, MURATA BLM15PX121SN1D)

40mil = For 4ohm 3W Speaker



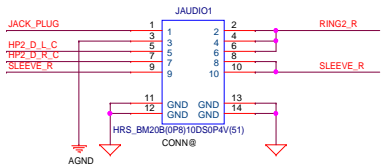
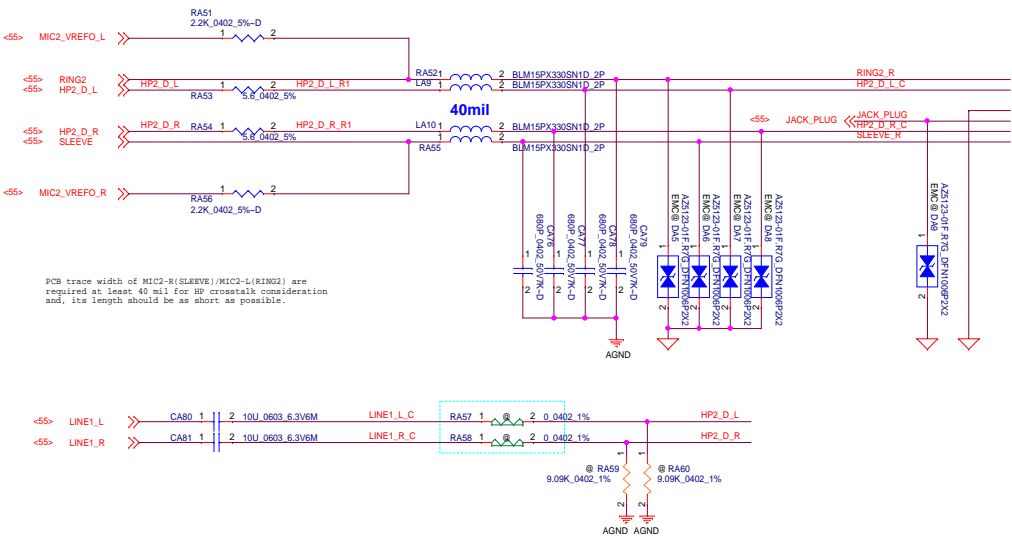
SPK_DET+ SPK_DET-

Function	RA50	RA62
EEPROM Speaker	0 ohm	NC
Speaker Detection	10K	0 ohm

EVT1.1 use SA00009JZ10

Security Classification		Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date		Deciphered Date		Compal Electronics, Inc.	
2014/09/08		2013/10/28		P56-Smart AMP / Speaker	
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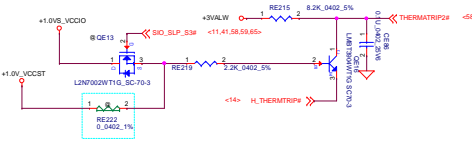
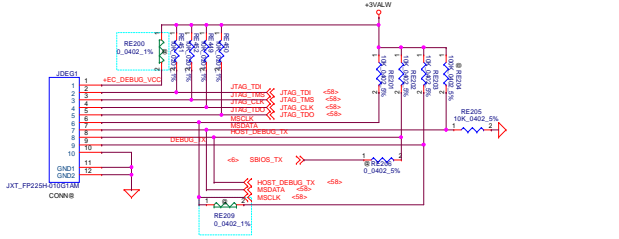
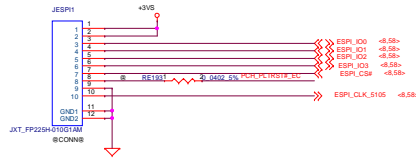
Universal Audio Jack



Security Classification				Compal Secret Data		DELL CONFIDENTIAL/PROPRIETARY	
Issued Date				2041/09/08		Compal Electronics, Inc.	
Deciphered Date				2013/10/28		Title	
						P57-Audio CONN	
						Size	
						LA-E671P	
						Rev	
						1.0	
						Date: Monday, October 22, 2018	
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QFN Pinout (Top)	QFN	QFN
1	VDD	VDD
2	VDD	VDD
3	VDD	VDD
4	VDD	VDD
5	VDD	VDD
6	VDD	VDD
7	VDD	VDD
8	VDD	VDD
9	VDD	VDD
10	VDD	VDD

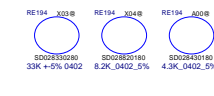


RE249	RE250	REV
@	@	Italia XPS
		Italia-L

RE196	CE78	REV
240K	4700p	ES1
130K	4700p	ES2
62K	4700p	QS
33K	4700p	U22
8.2K	4700p	V-PRO
4.3K	4700p	.
2K	4700p	.
1K	4700p	.



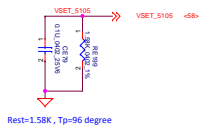
RE194	CE75	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	X03
8.2K	4700p	X04
4.3K	4700p	A00
2K	4700p	.
1K	4700p	.



RE195	CE76	PANEL SIZE
240K	4700p	
130K	4700p	
33K	4700p	
4.3K	4700p	Italia 13 WHL

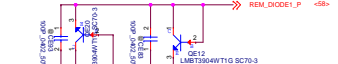
PANEL_ID rise time is measured from 5%~68%

BOARD_ID rise time is measured from 5%~68%

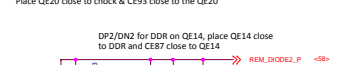


5105 Channel	Location
DP1/DN1	OTP (QE12)
SEN4	DN1a/DP1a Charger (QE20)
SEN1	DP2/DN2 DDR (QE14)
SEN5	DN2a/DP2a SKIN (QE21)
SEN6	DP3/DN3 SKIN (QE22)
SEN2	DN3a/DP3a SSD (QE15)
SEN3	DP4/DN4 WLAN (QE19)
	DN4a/DP4a

DP1/DN1 for CPU
Place CE83 close to the QE12 as possible



DN1a/DP1a for VR
Place QE20 close to chock & CE93 close to the QE20



DP2/DN2 for DDR on QE14, place QE14 close to DDR and CE87 close to QE14



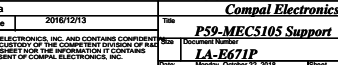
DN2a/DP2a for SKIN.
Place CE84 close to QE21



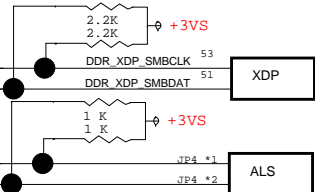
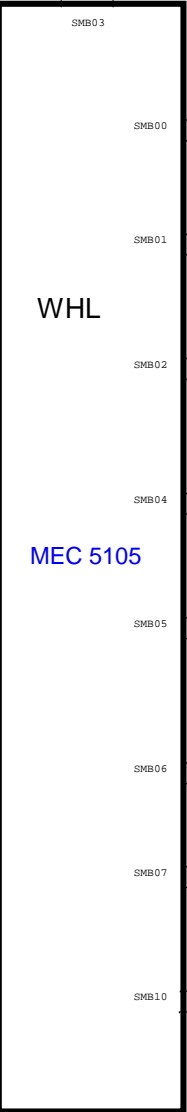
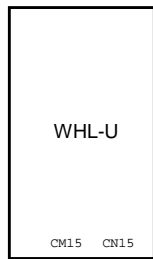
DP3/DN3 for SSD
Place CE91 close to the QE15 as possible



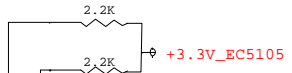
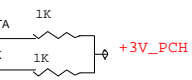
DN3a/DP3a for SSD.
Place CE95 close to QE22



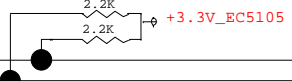
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2018/01/23		2022/12/31		Compal Electronics, Inc.	
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Document Number		Date		Sheet	
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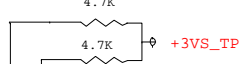
ALS address selection 0x52_TBD
Sensor address selection 0x6C_TBD



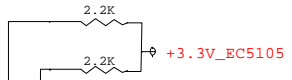
TI PD2
TI PD address selection 0x70_TBD
PD_Debug
PD_Debug address selection 0xEC_TBD



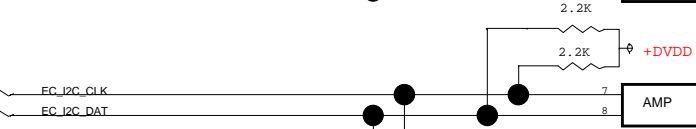
R_THER_S



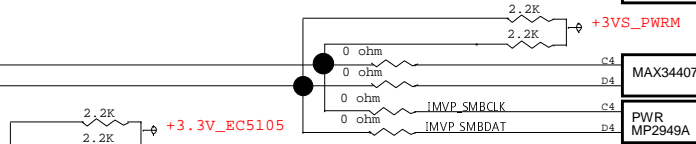
TP
TP address :0x42_TBD



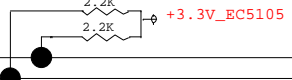
PD1_Debug
PD_Debug address selection 0xEC_TBD
TI PD1
TI PD address selection 0x70_TBD



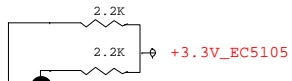
AMP
I2C address selection L= 0x20H (L= 0x20H ; H= 0x22H)_TBD
Audio



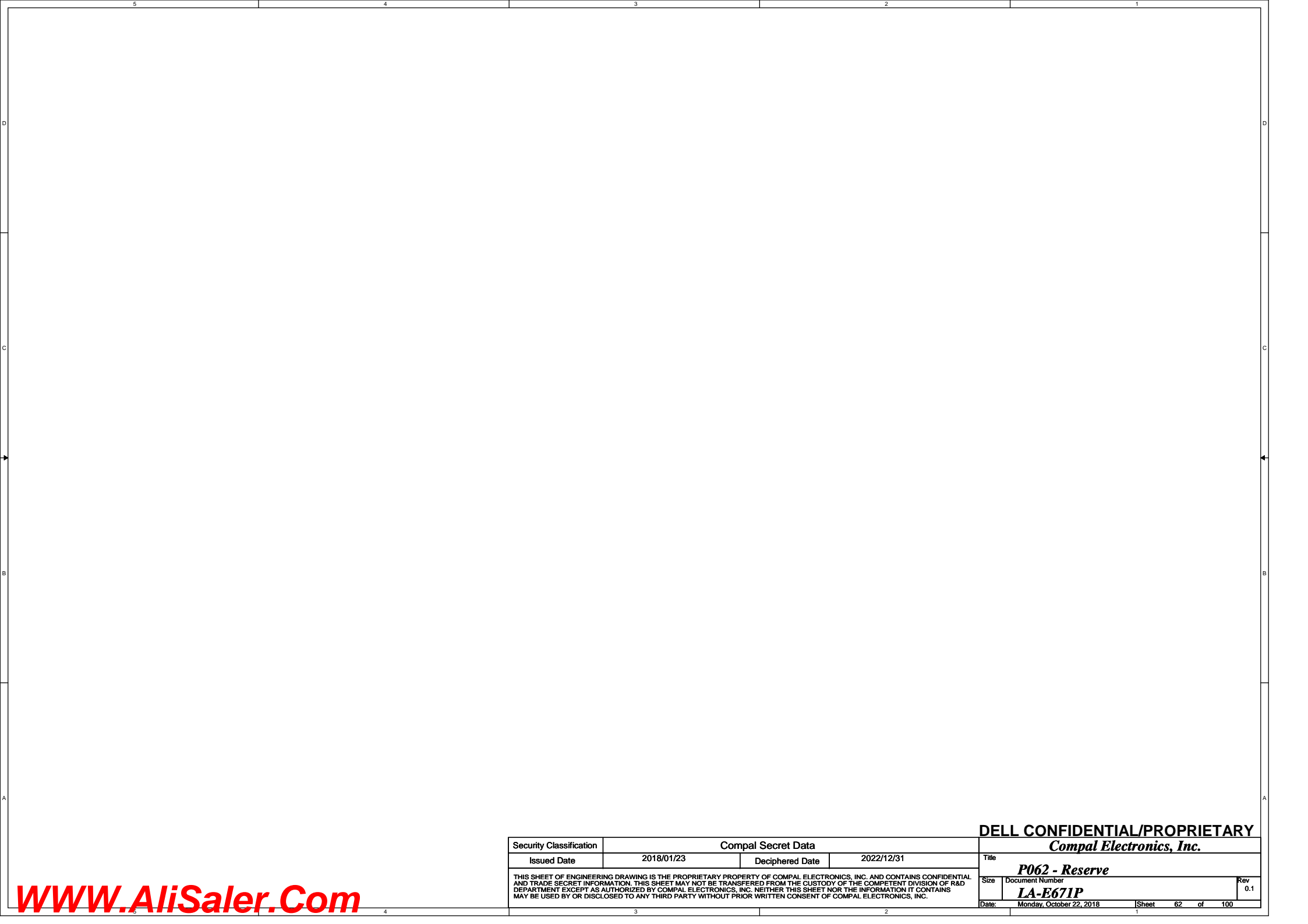
MAX34407
PWR MP2949A



TI PD3



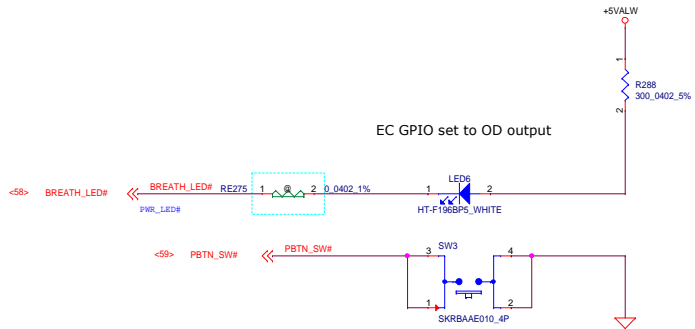
BATTERY CONN
Battery address selection 0x16_TBD
Charger
Charger address selection 0x12_TBD



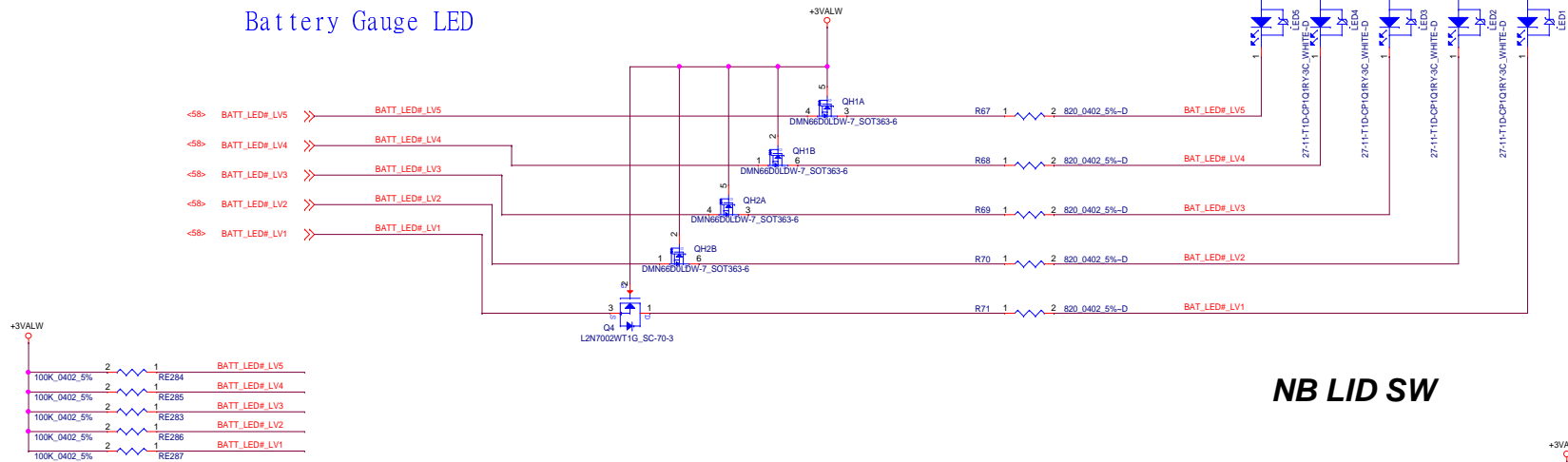
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				P062 - Reserve	
				Size	
				Document Number	
				LA-E671P	
				Date	
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				62 of 100	
				Rev	
				0.1	

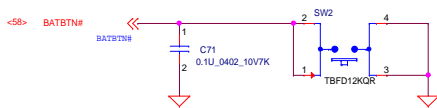
Power Button +LED



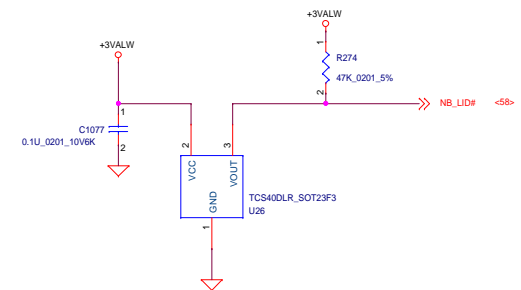
Battery Gauge LED



Battery Gauge Button



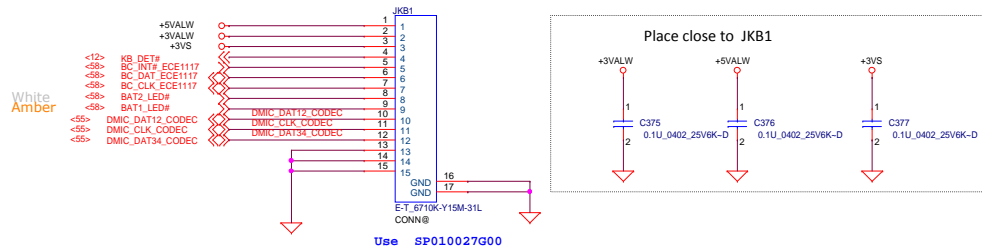
NB LID SW



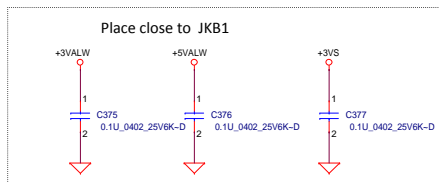
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.

Security Classification	Compal Secret Data			<div style="text-align: center;"> DO NOT CONFIDENTIALIZE DO NOT CONFIDENTIALIZE </div>	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	<div style="text-align: center;"> Compal Electronics, Inc. P63-Battery LED / LID </div>	
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				Date:	Monday, October 22, 2018
				Sheet	63 of 100

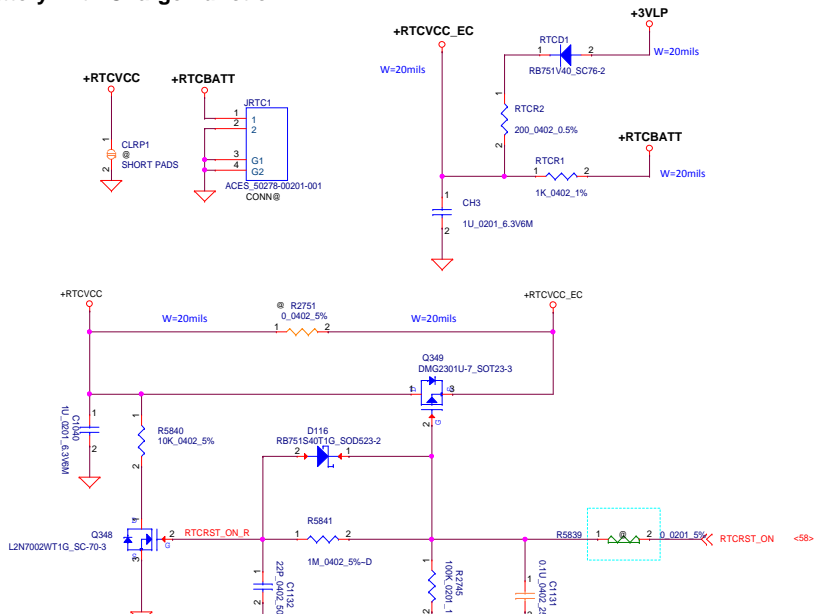
Keyboard Controller board + DMIC



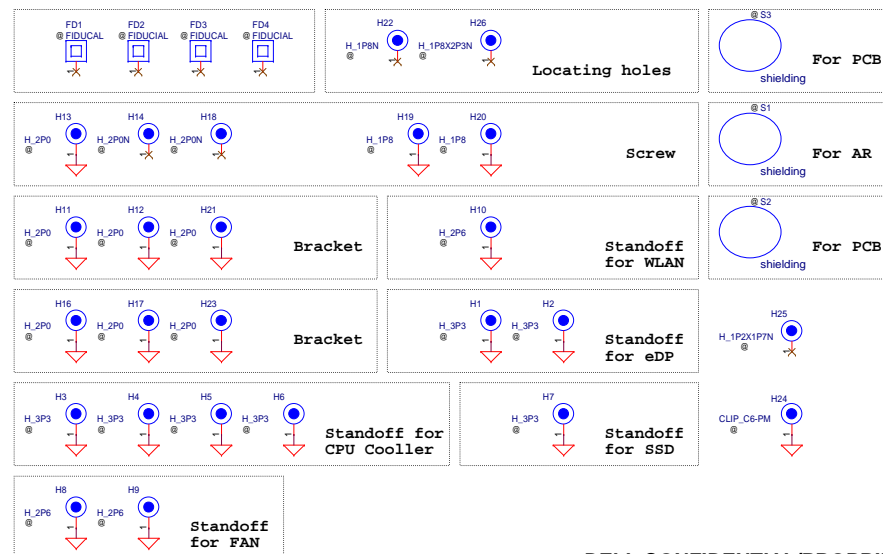
Power Monitor



RTC Battery With Charge Function



SCREW Hole



DELL CONFIDENTIAL/PROPRIETARY

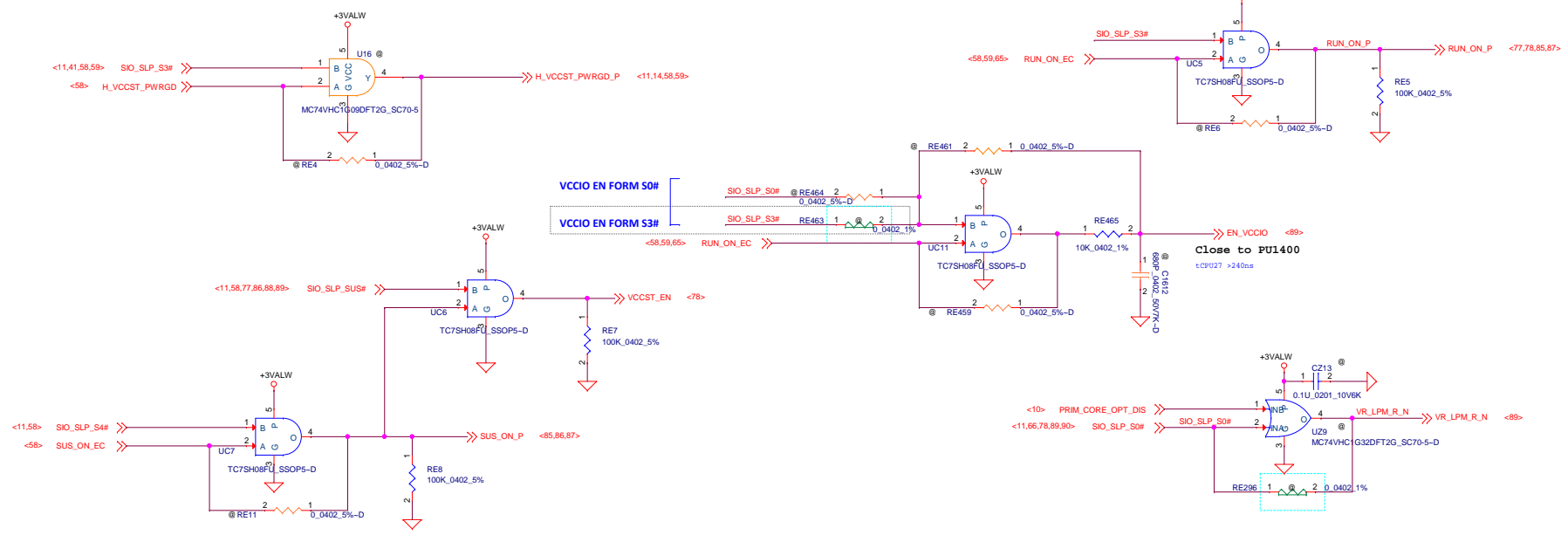
Compal Electronics, Inc.

Title **P64-SCREWH/KR/PTC/IP T/PWPM**

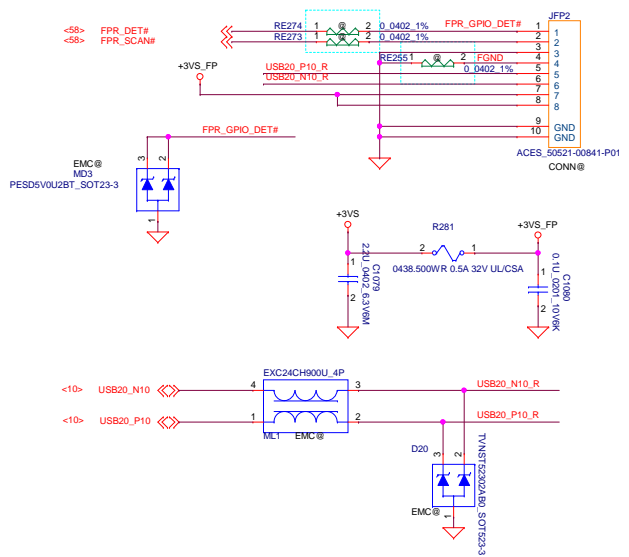
Size	Document Number	Rev
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	LA-E671P	1.0
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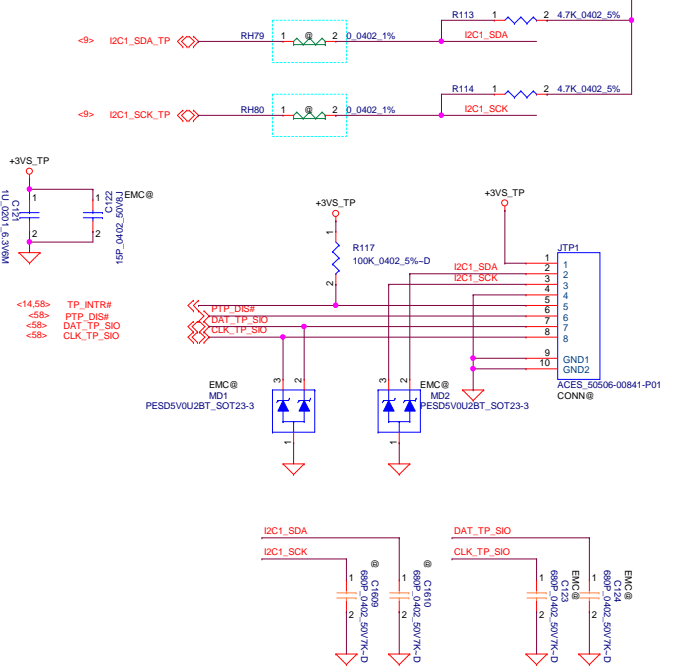
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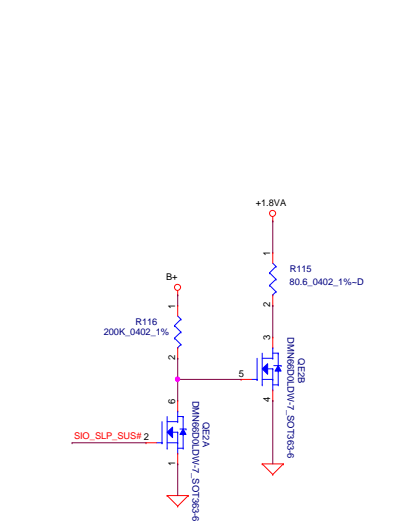
Fingerprint CONN



Touchpad CONN



+1.8VA Discharge

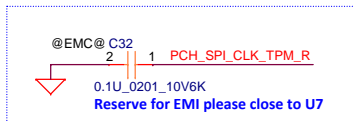
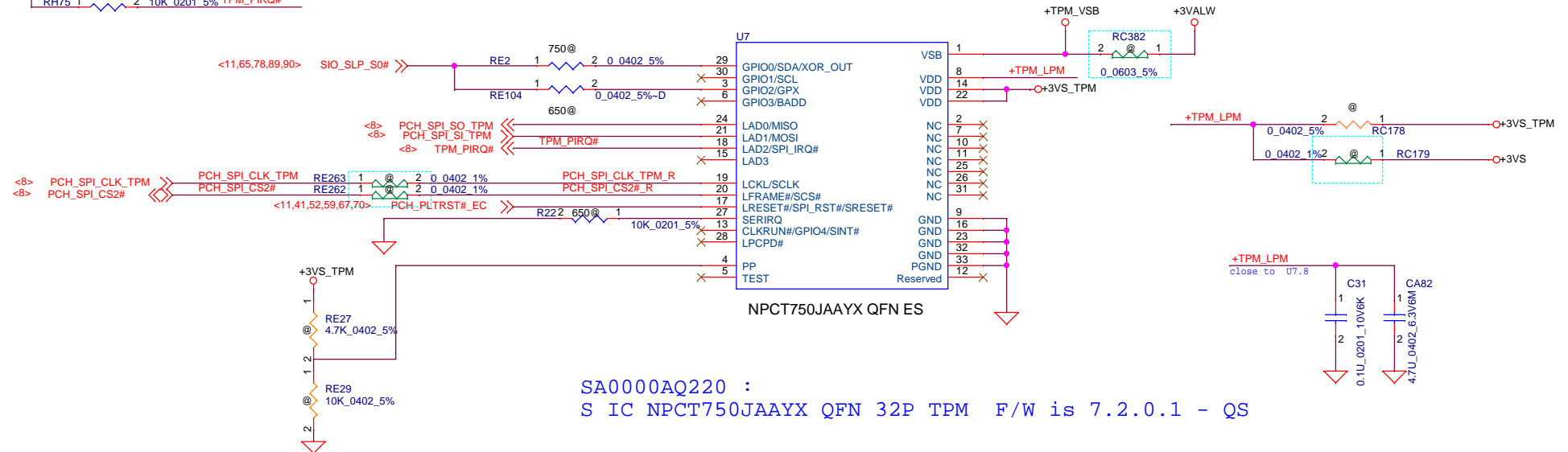
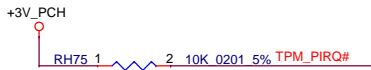
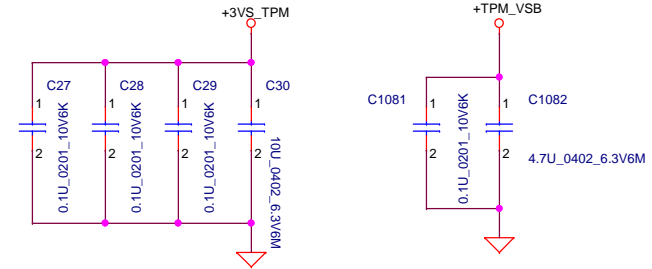
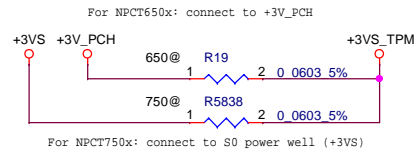


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Title		Document Number	
P65-TP/FP/PWGRGD		LA-E671P	
Date		Sheet	
Monday, October 22, 2018		65 of 100	

NOTE:
Follow the SPI topology layout guidelines
in the relevant Intel Platform Design Guide

TPM

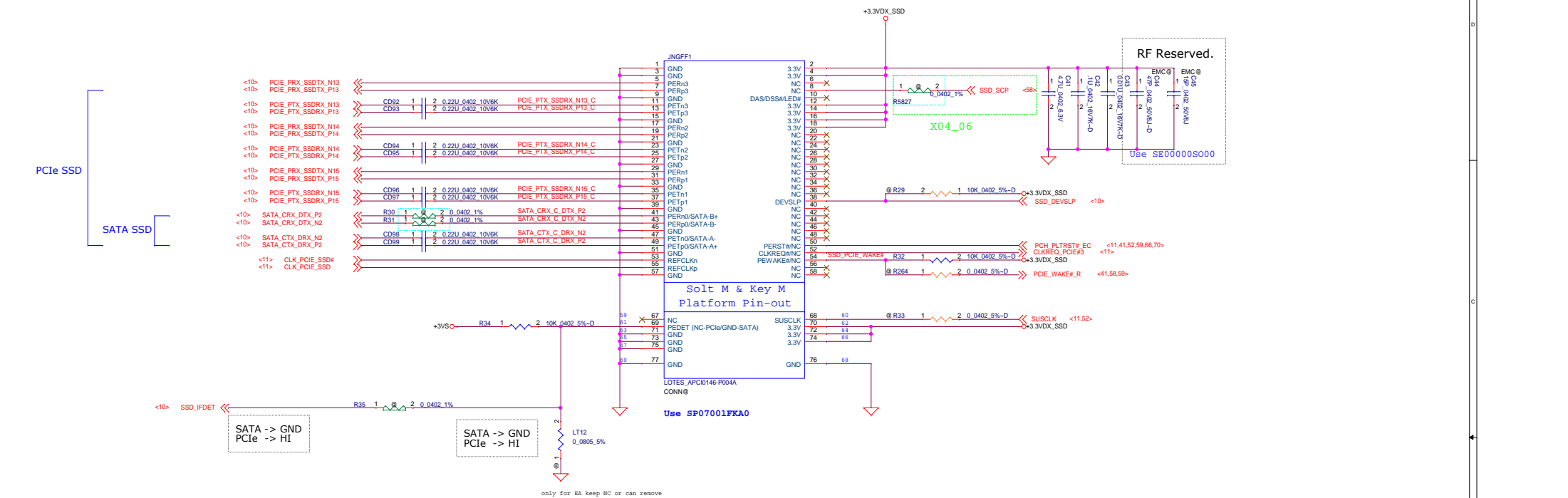
NOTE:
Place 0.1 uF capacitors as close as
possible to the device power pins



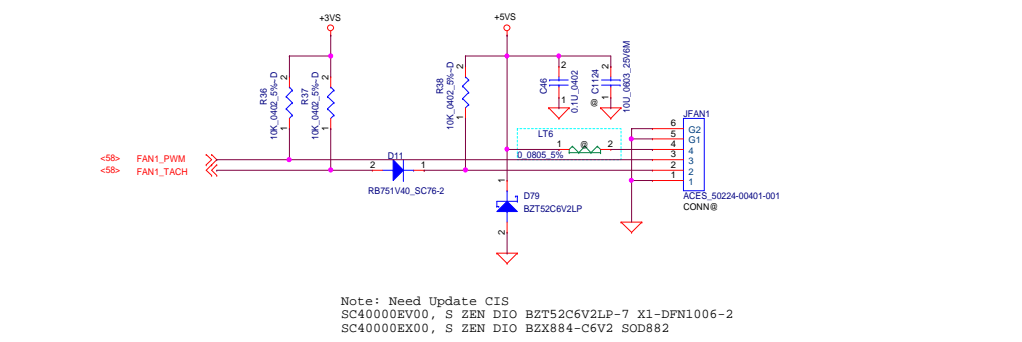
- 1.Pin14&Pin22 (+3VS_TPM):
For NPCT650x: connect to same power well with host SPI interface (it should be +3V_PCH)
For NPCT750x: connect to S0 power well (+3VS)
- 2.Pin27:
For NPCT650x: pop R22
For NPCT750x: de-pop R22
- 3.SLP_S0# connection:
For NPCT650x: pop RE104, de-pop RE2
For NPCT750x: pop RE2, de-pop RE104
- 4.RC180 can be just deleted for both NPCT650x and NPCT750x
- 5.TPM_PIRQ# is recommended that pull-up to same GPIO power well at host side

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				LA-E671P			
				1.0			
				Date:	Monday, October 22, 2018	Sheet	66 of 100

M.2 Slot-C Key-M (SSD)

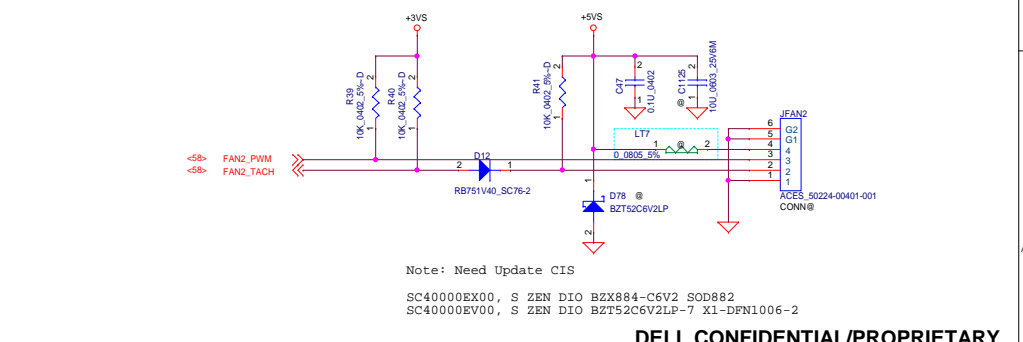


FAN 1



Note: Need Update CIS
SC40000EV00, S ZEN DIO B2T52C6V2LP-7 X1-DFN1006-2
SC40000EV00, S ZEN DIO BZX884-C6V2 SOD882

FAN 2



Note: Need Update CIS
SC40000EX00, S ZEN DIO BZX884-C6V2 SOD882
SC40000EV00, S ZEN DIO B2T52C6V2LP-7 X1-DFN1006-2

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Title				P67-SSD(M.2) / FAN			
Size				Document Number			
C				LA-E671P			
Date				Rev			
Monday, October 22, 2018				1.0			
Sheet				67 of 100			



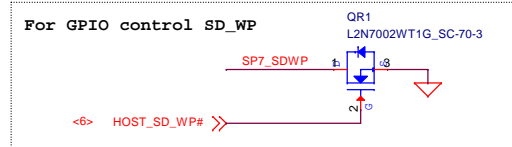
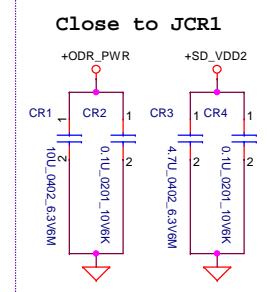
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				LA-E671P	

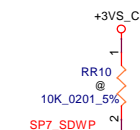


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				Sheet	69 of 100
				Rev	0.1
				LA-E671P	

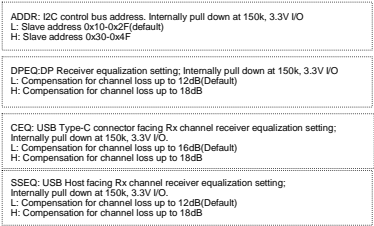
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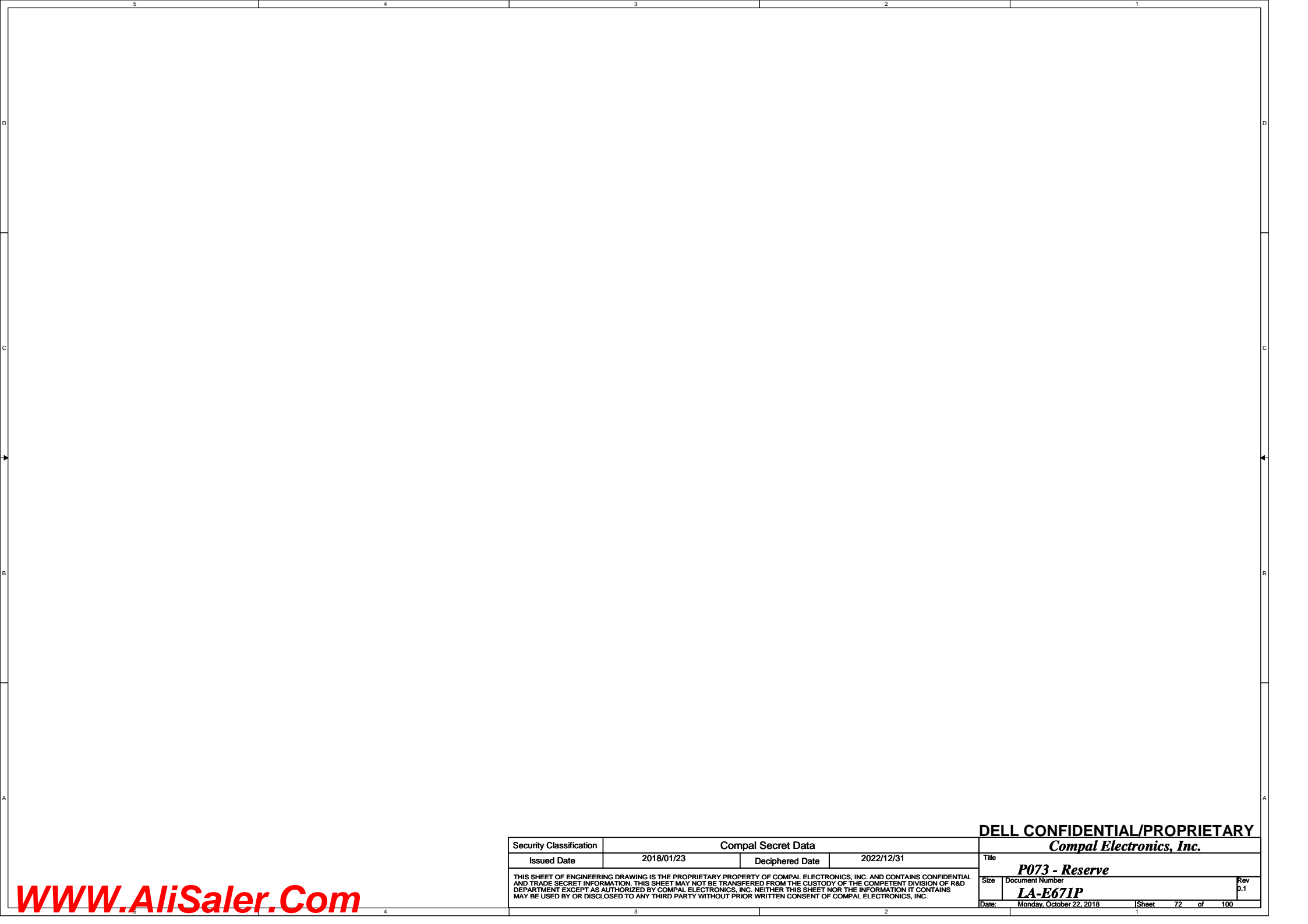
- If GPIO not use for LED function,
must be pull-high (Layout guide)



Title			
<i>P70-Card Reader - RT5242</i>			
Size	Document Number		Rev
	<i>LA-E671P</i>		1.0
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<i>Compal Electronics, Inc.</i>			
Title	<i>P071-DP/USB3 Repeater SW2 PS8802</i>		
Size B	Document Number <i>LA-E671P</i>	Rev 0.2	
Date:	Monday, October 22, 2018	Sheet	71 of 100



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2018/01/23		2022/12/31		Title	
				P073 - Reserve	
				Size	Rev
				Document Number	0.1
				LA-E671P	
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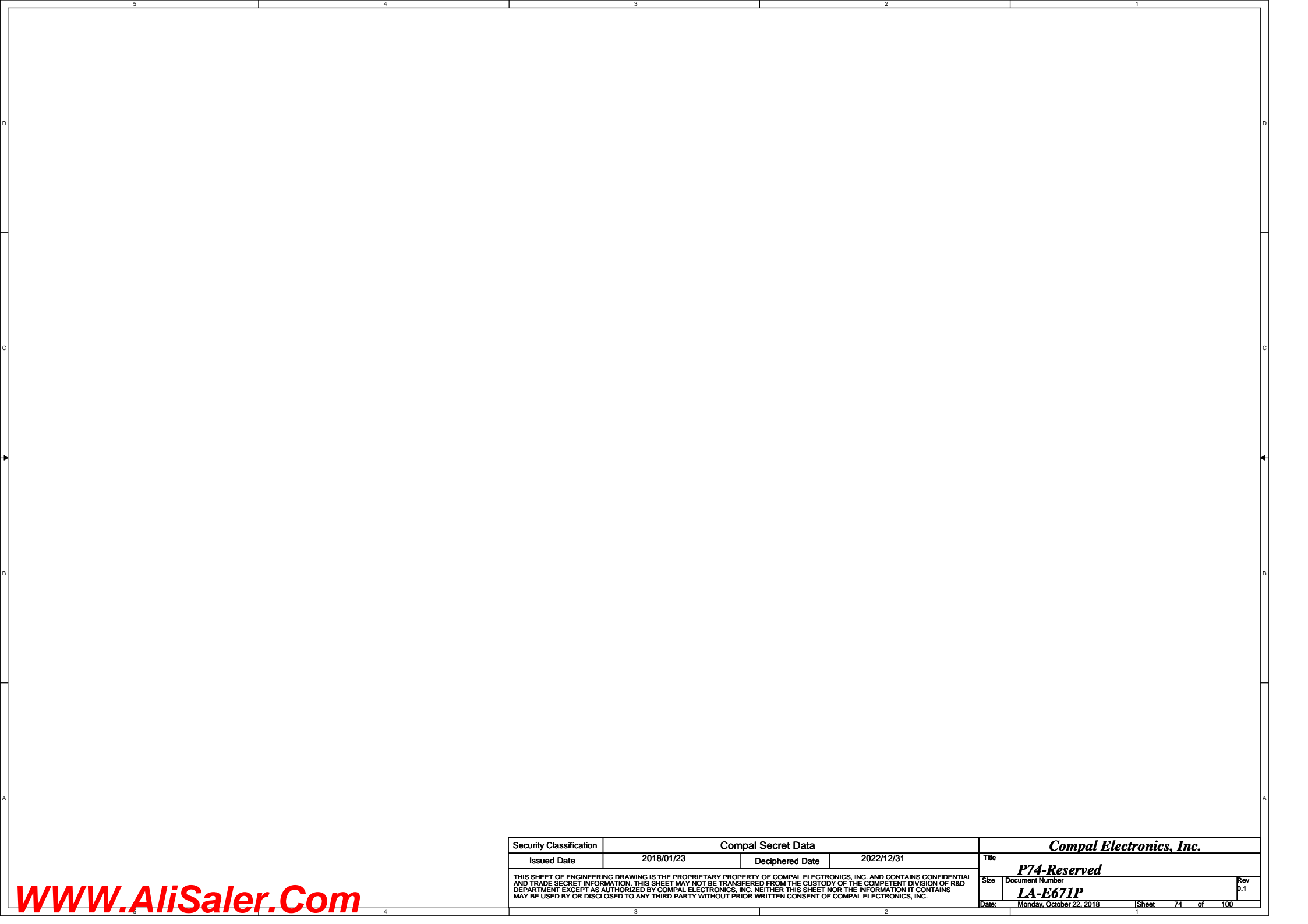
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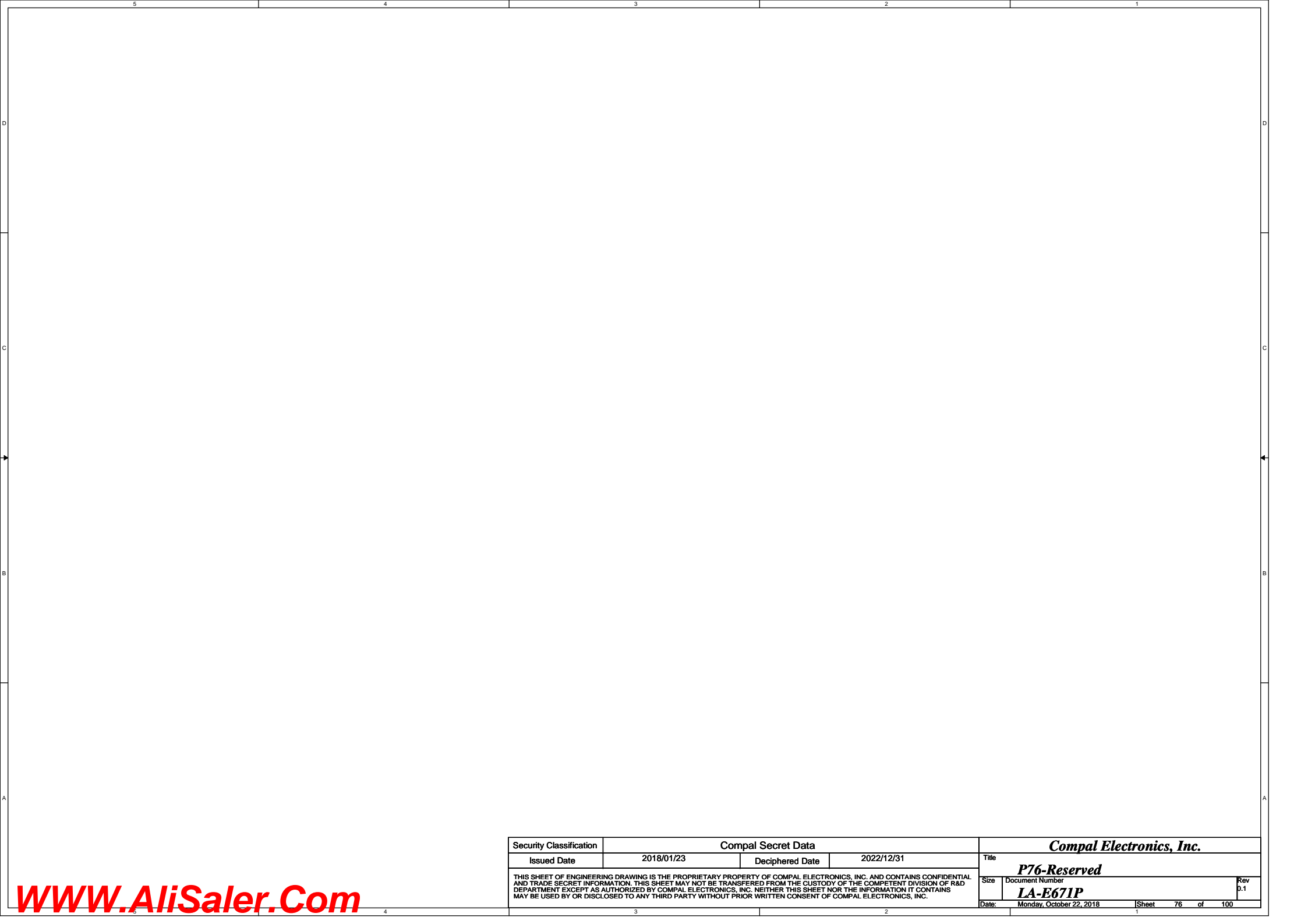
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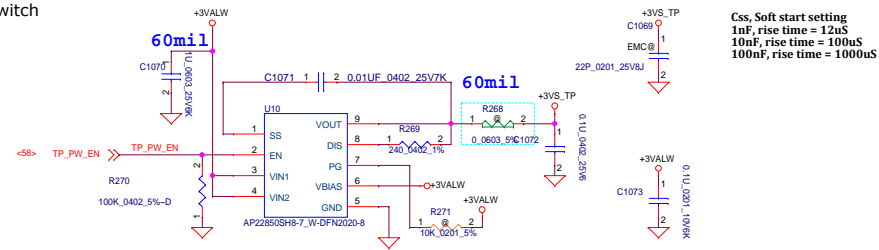
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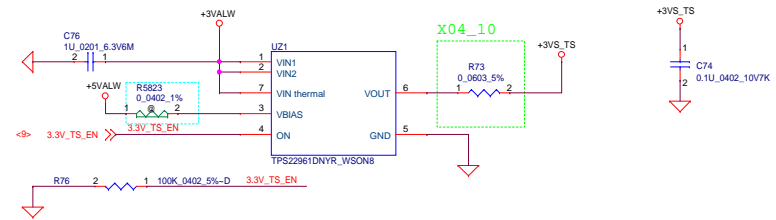
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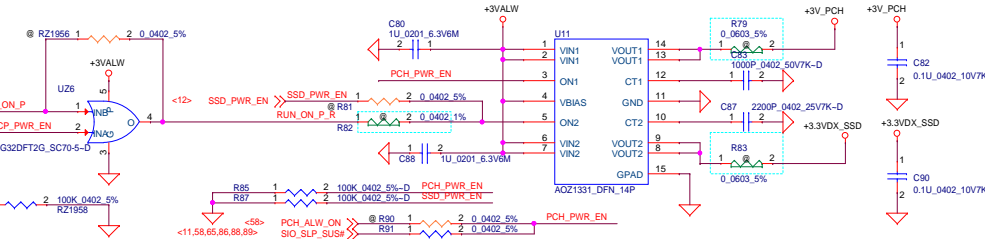
Touch Pad Load Switch



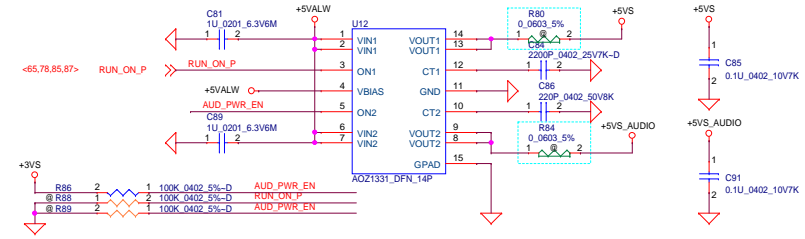
Touch Screen Load Switch



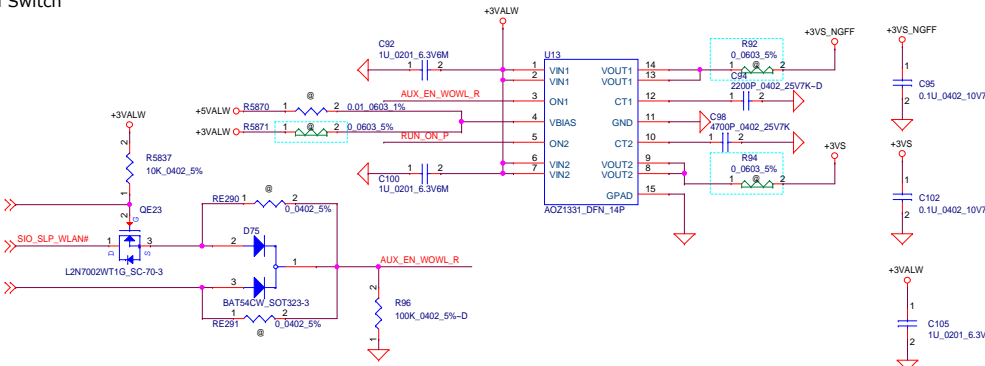
Deeper Sleep, SSD Load Switch



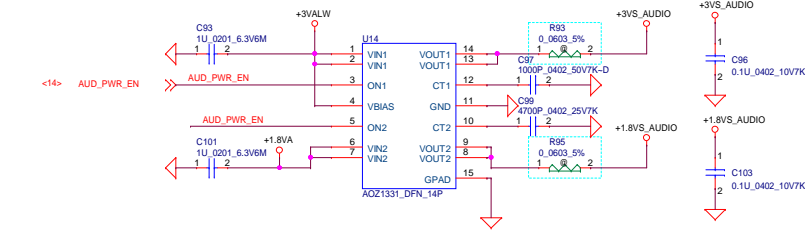
5V_Run, 5V_Audio Load Switch



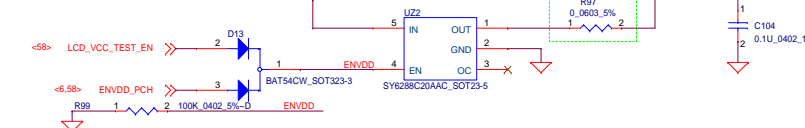
WiFi, 3V_RUN Load Switch



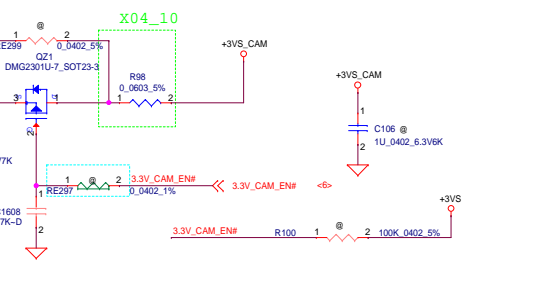
3V_Audio, 1.8V_Audio Load Switch



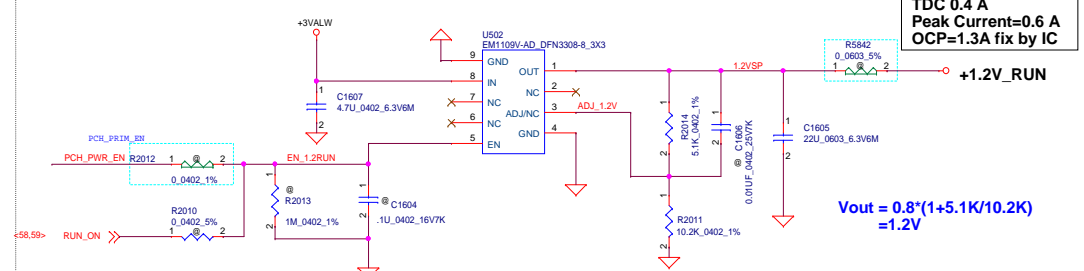
LCD Load Switch



Camera

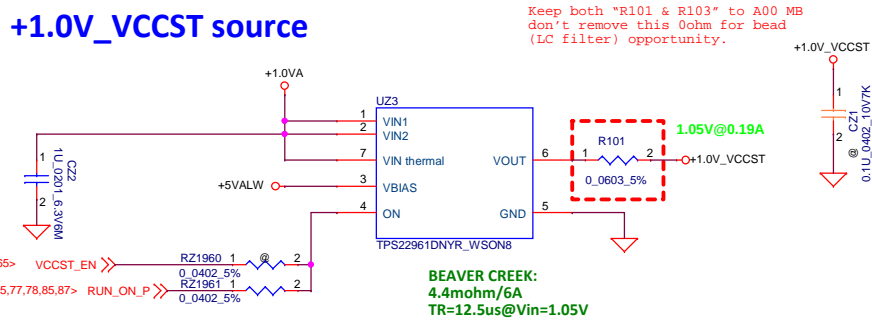


TypeC-SW MUX Load Switch

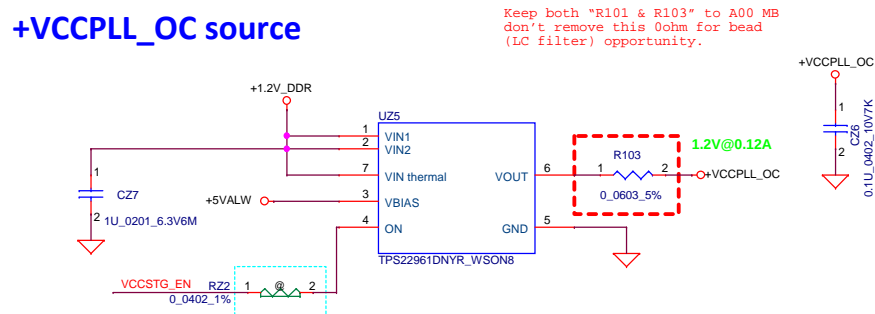


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+1.0V_VCCST source

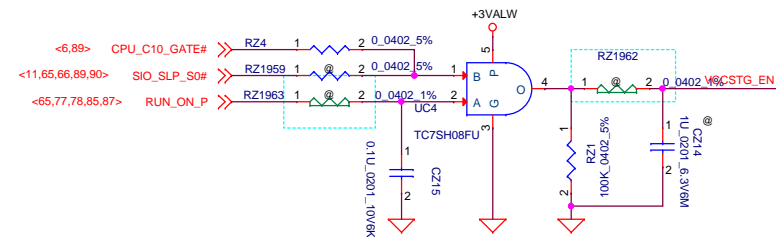
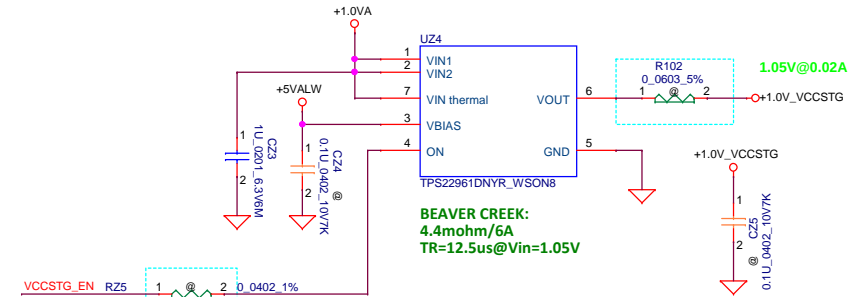


+VCCPLL_OC source



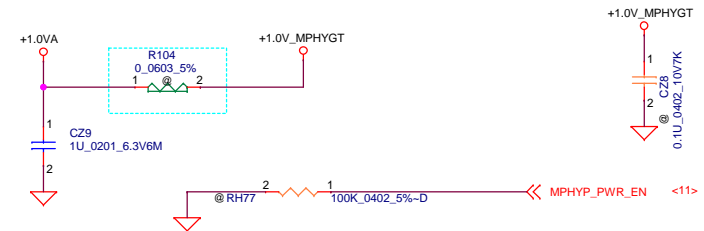
+1.8VU Load Switch

+1.0V_VCCSTG source



	S0	S0Ix	S3
SIO_SLP_S0#	high	low	low
RUN_ON_EC	high	high	low

+1.0V_MPHYGT source












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4+2 CPU Option

UCPU1 ES1_4+2@  SA0000BX10L SA0000BX10L_ES1	UCPU1 QS@  SA0000C6R1L I3-8145U_2.1G	UCPU1 QS@  SA0000C6Q1L I5-8265U_1.6G	UCPU1 VPRO@  SA0000CF10L I7-8565U_1.8G	UCPU1 VPRO@  SA0000C161L I5-8265U_1.6G
UCPU1 ES2_4+2@  BBBBBB ZZZZZZZZ	UCPU1 QS@  SA0000C6P2L I7-8565U_1.8G	UCPU1 QS@  SA0000C6Q3L I5-8265U_1.6G	UCPU1 QS@  SA0000C6Q3L I3-8145U_2.1G	

AR Option

UT2 AR_SLL42@  SA0000ZV3L DSL6340 SLL42 B2
--

TPM Option

U7 TPM750@  SA0000AQ220 TPM750 - QS FW is 7.2.0.1

DRAM Option

UD1 M4G_2133@  SA0000XZUOL SA0000AZUOL	UD2 M4G_2133@  SA0000AZUOL SA0000AZUOL	UD3 M4G_2133@  SA0000AZUOL SA0000AZUOL	UD4 M4G_2133@  SA0000AZUOL SA0000AZUOL
Micron 4G/2133 SA00009XUOL MT52L256M32D1PF-093 WT:B MT52L256M32D1PF-093 WT:B MT52L256M32D1PF-093 WT:B MT52L256M32D1PF-093 WT:B			

UD1 M8G_2133@  SA00009U7OL SA0000AM4OL	UD2 M8G_2133@  SA0000AM4OL SA0000AM4OL	UD3 M8G_2133@  SA0000AM4OL SA0000AM4OL	UD4 M8G_2133@  SA0000AM4OL SA0000AM4OL
Micron 8G/2133 SA00009U7OL MT52L512M32D2PF-093 WT:B MT52L512M32D2PF-093 WT:B MT52L512M32D2PF-093 WT:B MT52L512M32D2PF-093 WT:B			

UD1 M16G_2133@  SA00009ZNUOL SA00009ZNUOL	UD2 M16G_2133@  SA00009ZNUOL SA00009ZNUOL	UD3 M16G_2133@  SA00009ZNUOL SA00009ZNUOL	UD4 M16G_2133@  SA00009ZNUOL SA00009ZNUOL
Mircon 16G/2133 SA00009ZNUOL MT52L1G32D4PG-093WT:B MT52L1G32D4PG-093WT:B MT52L1G32D4PG-093WT:B MT52L1G32D4PG-093WT:B			

UD1 S4G_2133@  SA0000BTEOL SA0000BTEOL	UD2 S4G_2133@  SA0000BTEOL SA0000BTEOL	UD3 S4G_2133@  SA0000BTEOL SA0000BTEOL	UD4 S4G_2133@  SA0000BTEOL SA0000BTEOL
Samsung 4G/2133 SA0000BTEOL K4E8E324EB-EGCG K4E8E324EB-EGCG K4E8E324EB-EGCG K4E8E324EB-EGCG			

UD1 S8G_2133@  SA0000AZT1L SA0000AZT1L	UD2 S8G_2133@  SA0000AZT1L SA0000AZT1L	UD3 S8G_2133@  SA0000AZT1L SA0000AZT1L	UD4 S8G_2133@  SA0000AZT1L SA0000AZT1L
Samsung 8G/1866 SA0000AZT1L K4E6E304EC-EGCG K4E6E304EC-EGCG K4E6E304EC-EGCG K4E6E304EC-EGCG			














































UD1 S16G_2133@  SA00008VV2L SA00008VV2L	UD2 S16G_2133@  SA00008VV2L SA00008VV2L	UD3 S16G_2133@  SA00008VV2L SA00008VV2L	UD4 S16G_2133@  SA00008VV2L SA00008VV2L
Samsung 16G/2133 SA00008VV2L K4EBE304EC-EGCG K4EBE304EC-EGCG K4EBE304EC-EGCG K4EBE304EC-EGCG			

UD1 H4G_2133@  SA0000AZR0L SA0000AZR0L	UD2 H4G_2133@  SA0000AZR0L SA0000AZR0L	UD3 H4G_2133@  SA0000AZR0L SA0000AZR0L	UD4 H4G_2133@  SA0000AZR0L SA0000AZR0L
Hynix 4G/2133 SA0000AZR0L H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD			

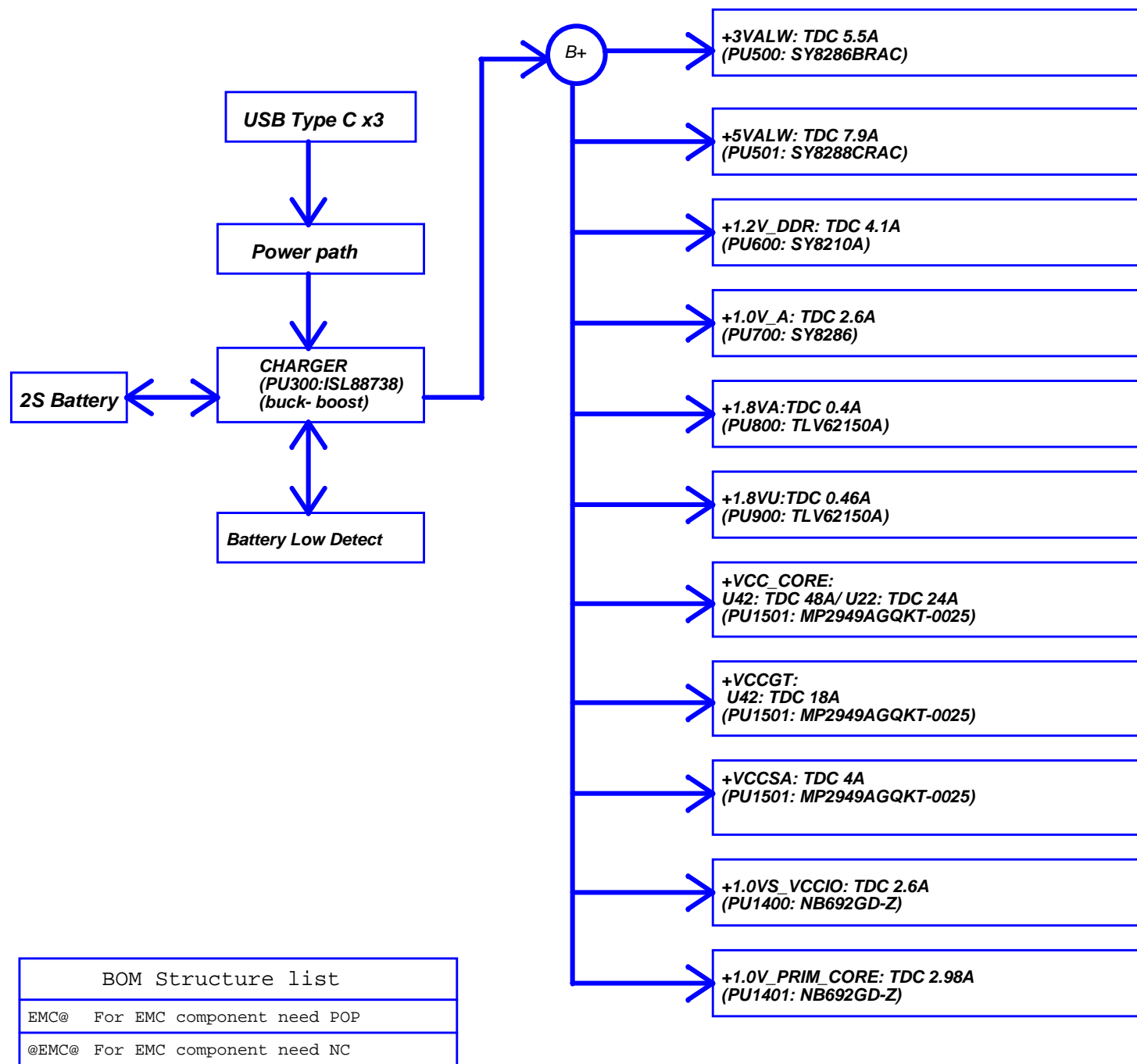
UD1 H8G_2133@  SA0000ALP0L SA0000ALP0L	UD2 H8G_2133@  SA0000ALP0L SA0000ALP0L	UD3 H8G_2133@  SA0000ALP0L SA0000ALP0L	UD4 H8G_2133@  SA0000ALP0L SA0000ALP0L
Hynix 8G/2133 SA0000ALP0L H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD			

UD1 H16G_2133@  SA00009ZL0L SA00009ZL0L	UD2 H16G_2133@  SA00009ZL0L SA00009ZL0L	UD3 H16G_2133@  SA00009ZL0L SA00009ZL0L	UD4 H16G_2133@  SA00009ZL0L SA00009ZL0L
Hynix 16G/2133 SA00009ZL0L H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD H9CCNN8GTALAR-NVD			

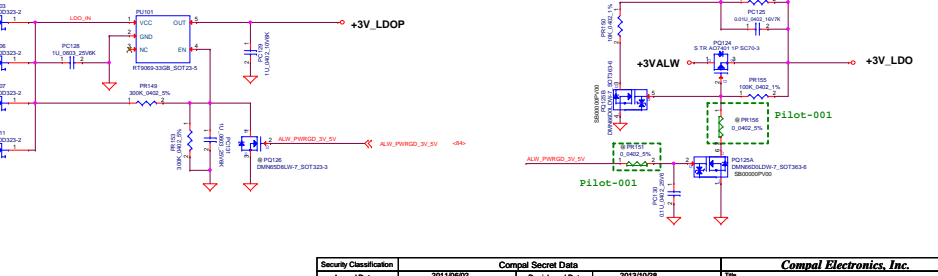
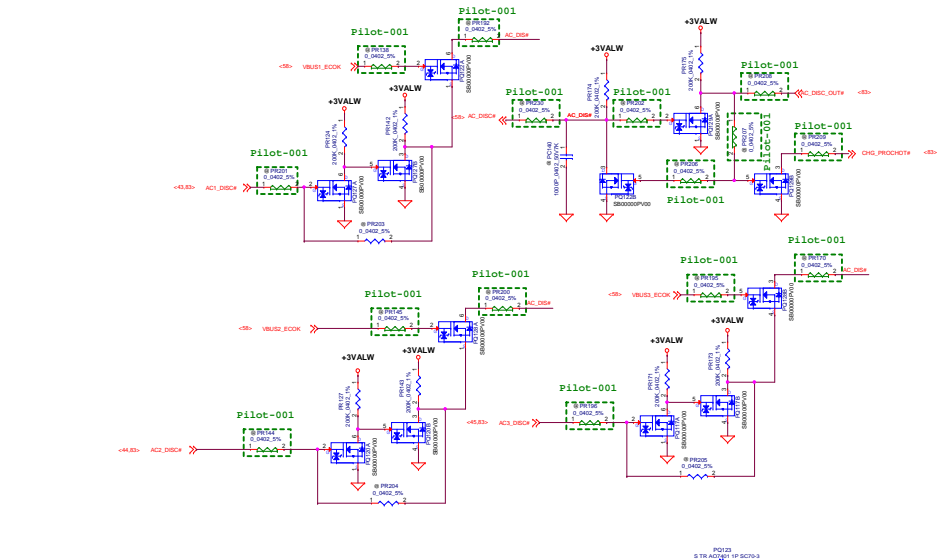
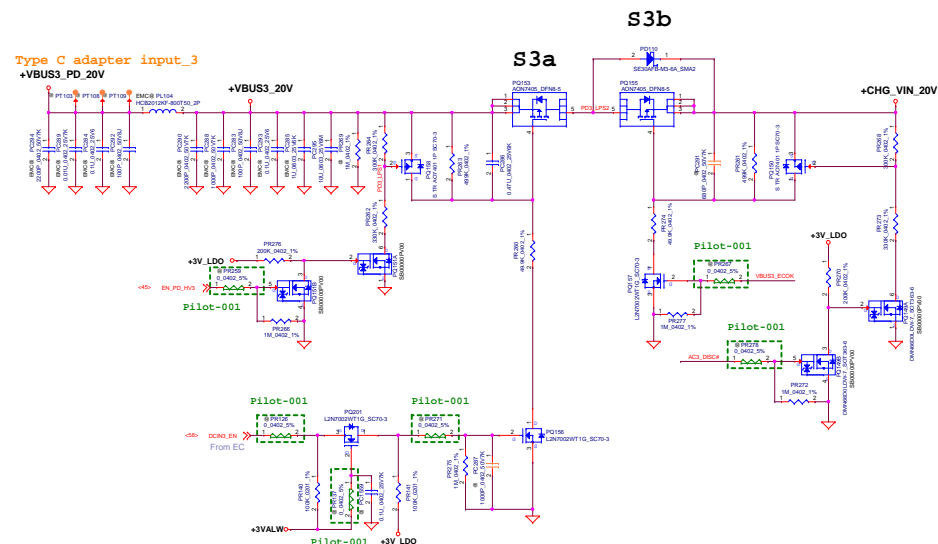
DRAM Config Option

MEM_CONFIG0 RH51 M4G_2133@  SD028100280 10K_0402_5%	MEM_CONFIG1 RH51 M4G_2133@  SD028100280 10K_0402_5%	MEM_CONFIG2 RH56 M4G_2133@  SD028100280 10K_0402_5%	MEM_CONFIG3 RH57 M4G_2133@  SD028100280 10K_0402_5%	MEM_CONFIG4 RH60 M4G_2133@  SD028100280 10K_0402_5%
RH52 M8G_2133@  SD028100280 10K_0402_5%	RH53 M8G_2133@  SD028100280 10K_0402_5%	RH56 M8G_2133@  SD028100280 10K_0402_5%	RH57 M8G_2133@  SD028100280 10K_0402_5%	RH60 M8G_2133@  SD028100280 10K_0402_5%
RH52 M16G_2133@  SD028100280 10K_0402_5%-D	RH54 M16G_2133@  SD028100280 10K_0402_5%-D	RH55 M16G_2133@  SD028100280 10K_0402_5%-D	RH58 M16G_2133@  SD028100280 10K_0402_5%-D	RH59 M16G_2133@  SD028100280 10K_0402_5%-D
RH51 S4G_2133@  SD028100280 10K_0402_5%-D	RH53 S4G_2133@  SD028100280 10K_0402_5%-D	RH55 S4G_2133@  SD028100280 10K_0402_5%-D	RH57 S4G_2133@  SD028100280 10K_0402_5%-D	RH60 S4G_2133@  SD028100280 10K_0402_5%-D
RH52 S8G_2133@  SD028100280 10K_0402_5%-D	RH54 S8G_2133@  SD028100280 10K_0402_5%-D	RH56 S8G_2133@  SD028100280 10K_0402_5%-D	RH58 S8G_2133@  SD028100280 10K_0402_5%-D	RH59 S8G_2133@  SD028100280 10K_0402_5%-D
RH52 S16G_2133@  SD028100280 10K_0402_5%-D	RH53 S16G_2133@  SD028100280 10K_0402_5%-D	RH56 S16G_2133@  SD028100280 10K_0402_5%-D	RH57 S16G_2133@  SD028100280 10K_0402_5%-D	RH59 S16G_2133@  SD028100280 10K_0402_5%-D
RH52 H4G_2133@  SD028100280 10K_0402_5%-D	RH54 H4G_2133@  SD028100280 10K_0402_5%-D	RH55 H4G_2133@  SD028100280 10K_0402_5%-D	RH57 H4G_2133@  SD028100280 10K_0402_5%-D	RH60 H4G_2133@  SD028100280 10K_0402_5%-D
RH51 H8G_2133@  SD028100280 10K_0402_5%-D	RH54 H8G_2133@  SD028100280 10K_0402_5%-D	RH55 H8G_2133@  SD028100280 10K_0402_5%-D	RH57 H8G_2133@  SD028100280 10K_0402_5%-D	RH60 H8G_2133@  SD028100280 10K_0402_5%-D
RH51 H16G_2133@  SD028100280 10K_0402_5%-D	RH53 H16G_2133@  SD028100280 10K_0402_5%-D	RH55 H16G_2133@  SD028100280 10K_0402_5%-D	RH58 H16G_2133@  SD028100280 10K_0402_5%-D	RH59 H16G_2133@  SD028100280 10K_0402_5%-D

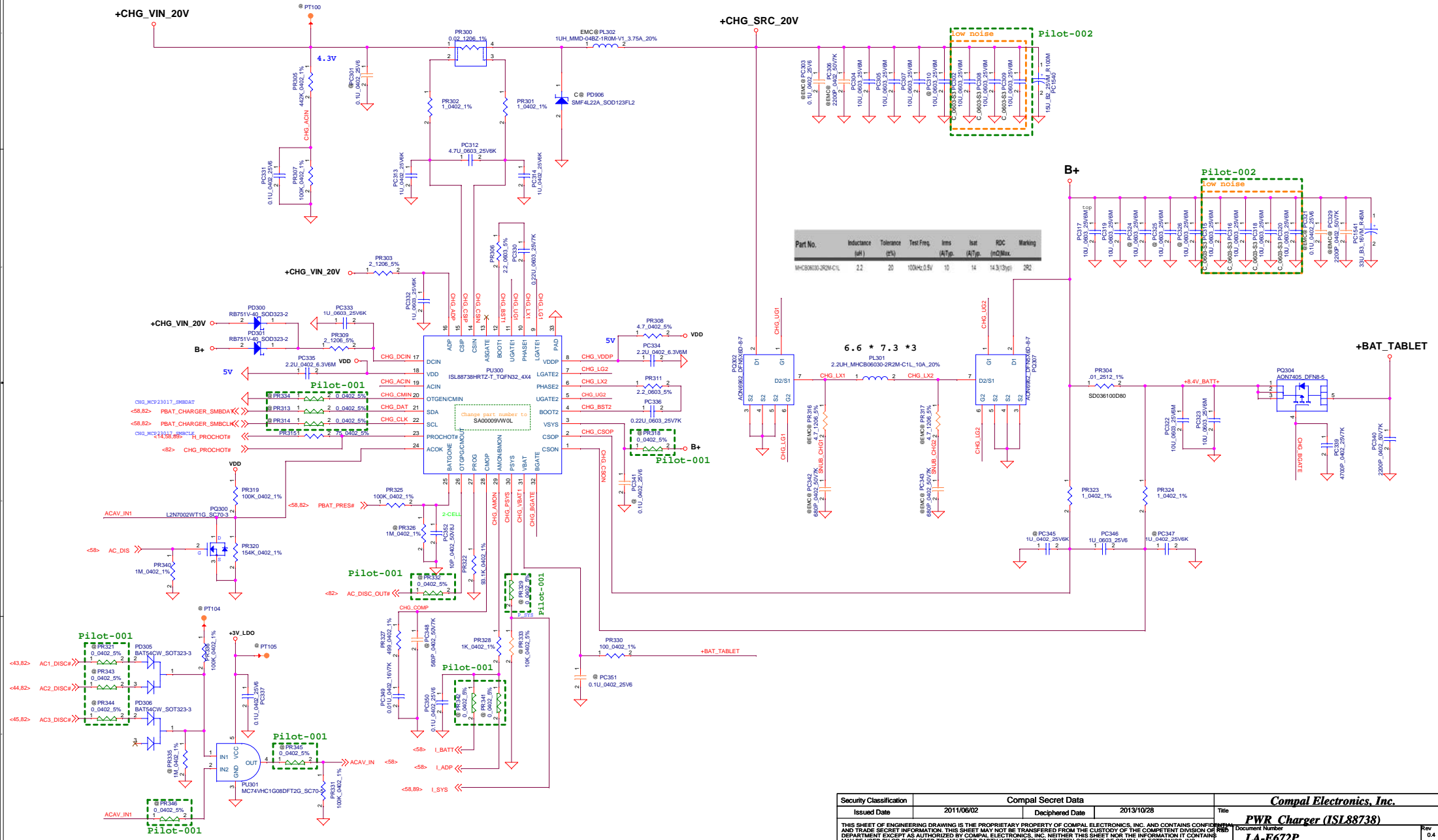
LA-E671P Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/16	Deciphered Date	2016/12/13	Title
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Size	Document Number	LA-E671P	Rev	0.1
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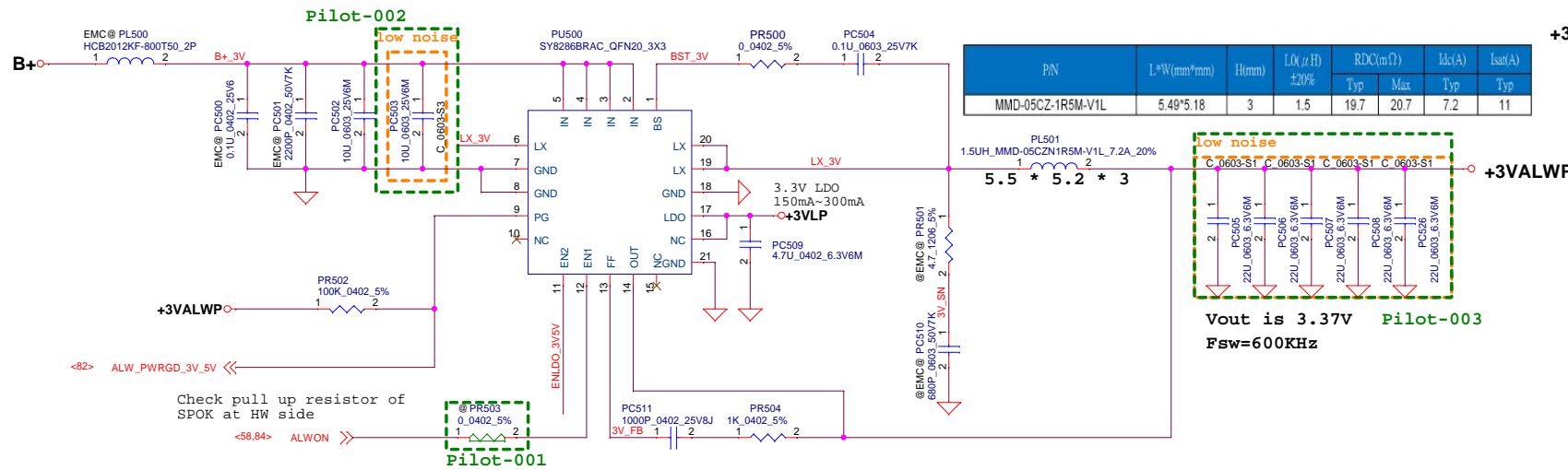


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Title	DCIN/Power Path	
	Size	Document Number
		LA-E672P





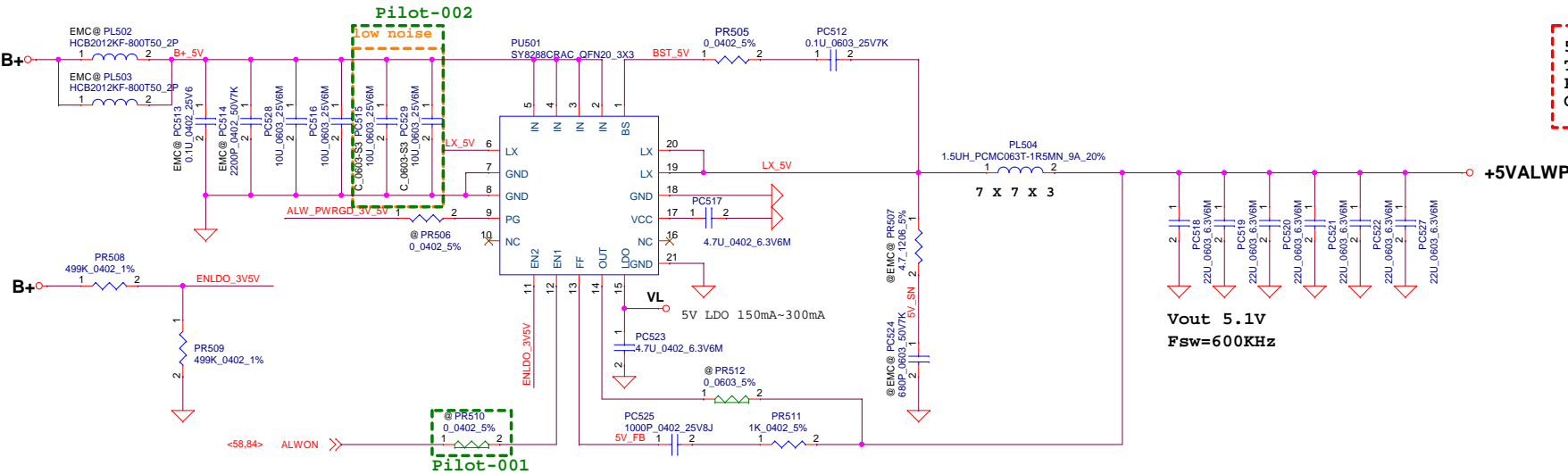
+3VALWP @ PJP500 JUMP 43X118 2 +3VALW

3VALWP
TDC 5.2A
Peak Current 7.5A
OCP Current 8.0A (fix)

Non AR
3VALWP
TDC 5.5A
Peak Current 7.5A
OCP Current 8.0A (fix)

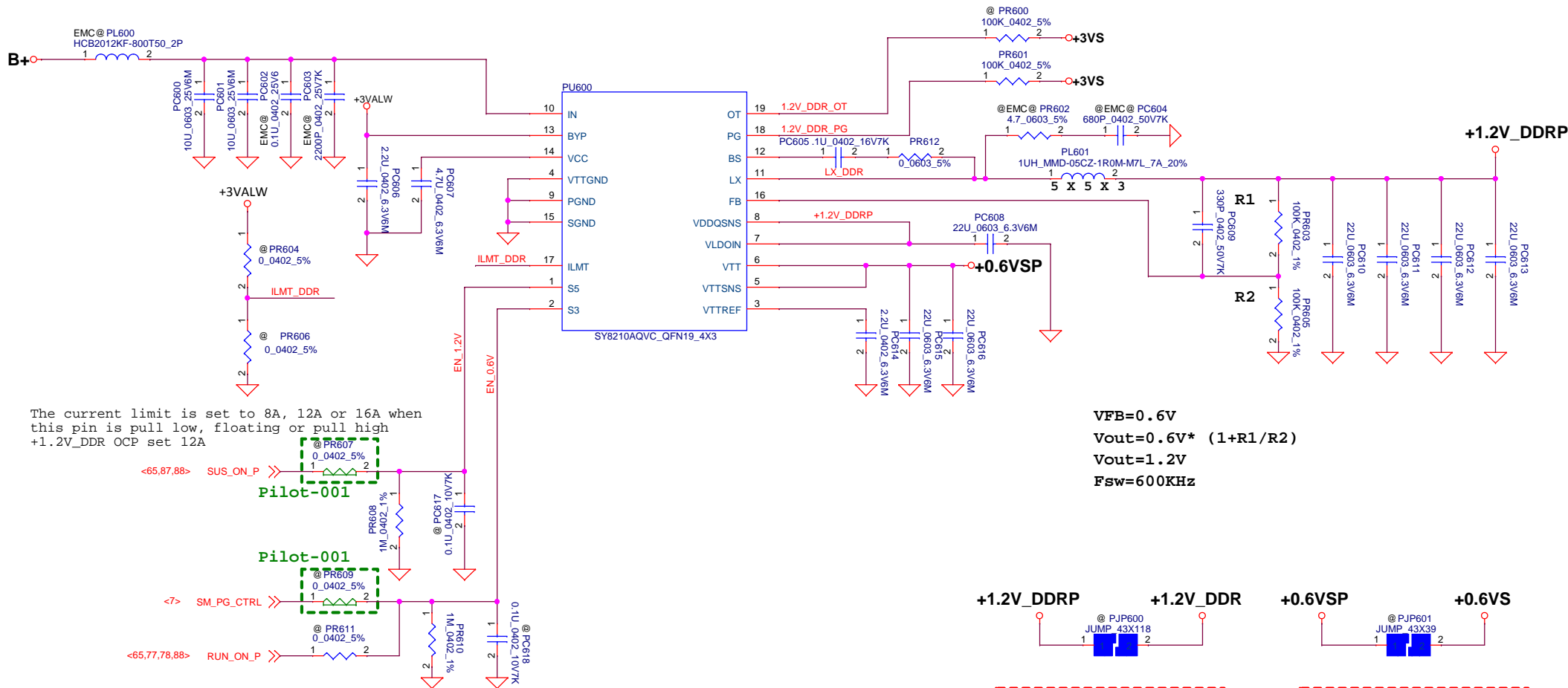
+5VALWP @ PJP501 JUMP 43X118 2 +5VALW

5VALWP
TDC 7.9A
Peak Current 11.0A
OCP Current 13.0A



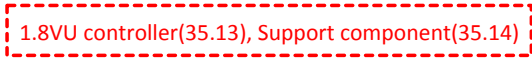
3V/5V controller(35.1), Support component(35.2)

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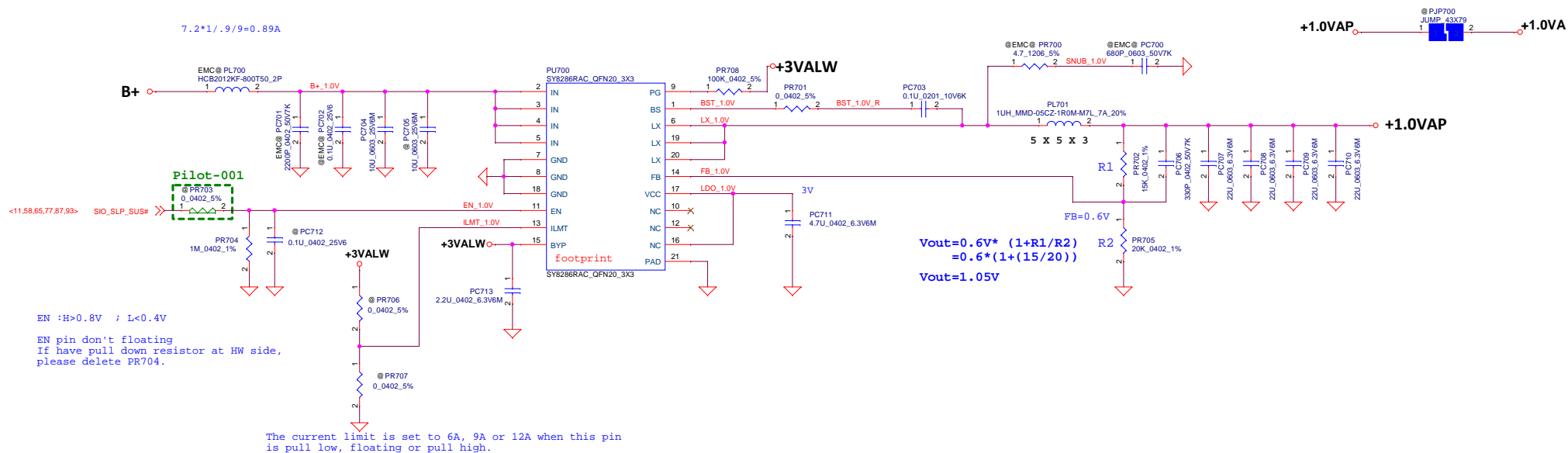
DDR controller(35.3), Support component(35.4)

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Title			
+1.8VU			
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+1.0VA
TDC 3.5A
Peak Current 5A
OCP current 9A



1.05V controller(35.5), Support component(35.6)

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	LPM	VID1	VID0	Vout
	0	X	X	0 (LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

VCCIO
TDC 2.6A
Peak Current 3.7 A
OCP Current 7.6 A Fix by IC
MIN:7A
MAX:8.5A
Frequency:750KHz

PJP1400 JUMP 43X79

+1.0VS_VCCIO

PRIM_CORE
TDC 2.98A
Peak Current 4.26 A
OCP Current 7.6 A Fix by IC
MIN:7A
MAX:8.5A
Choke DCR 34.0mohm

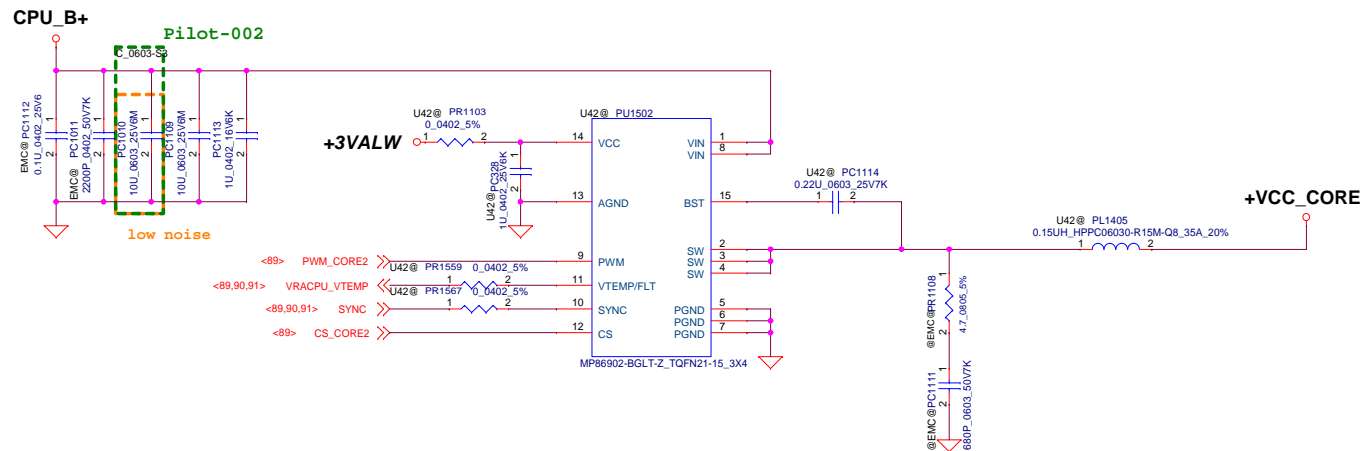
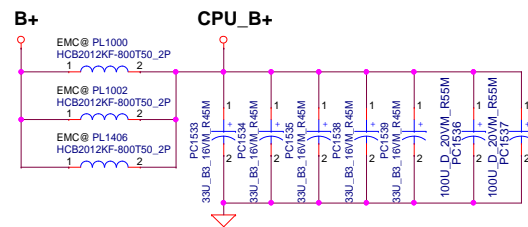
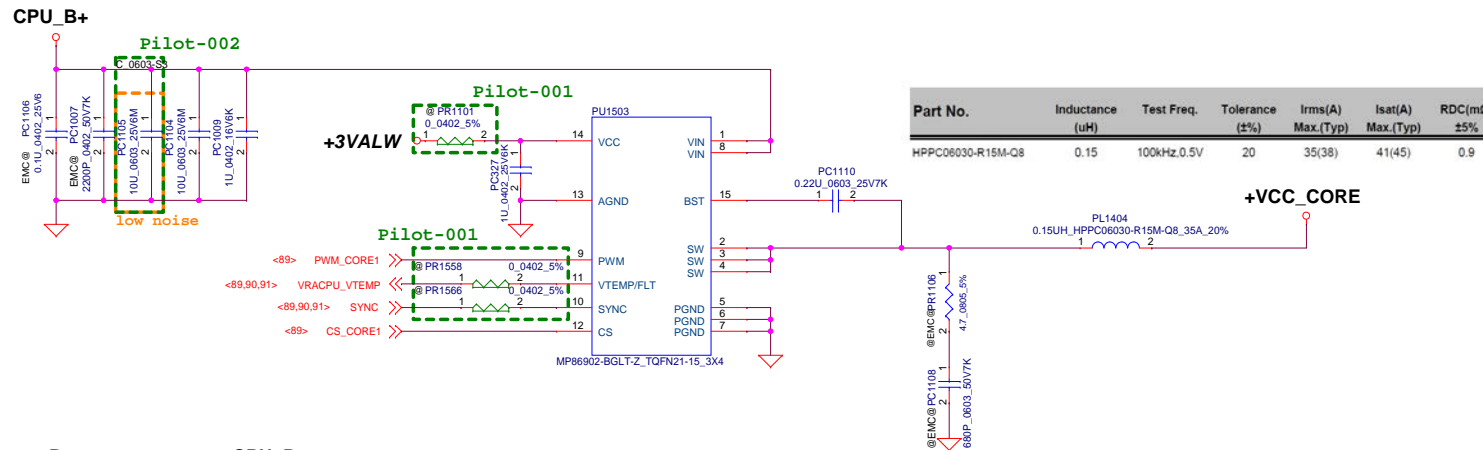
PJP1401 JUMP 43X79

+1.0V_PRIM_CORE

	LPM	VID1	VID0	Vout
	0	X	X	0.75 (LPM)
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

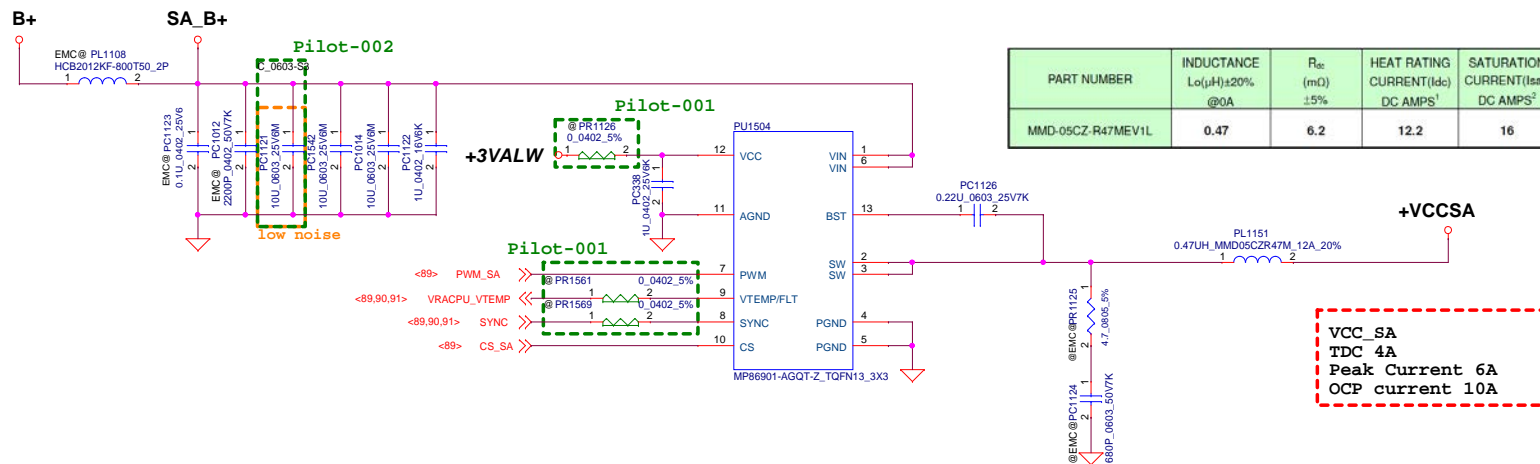
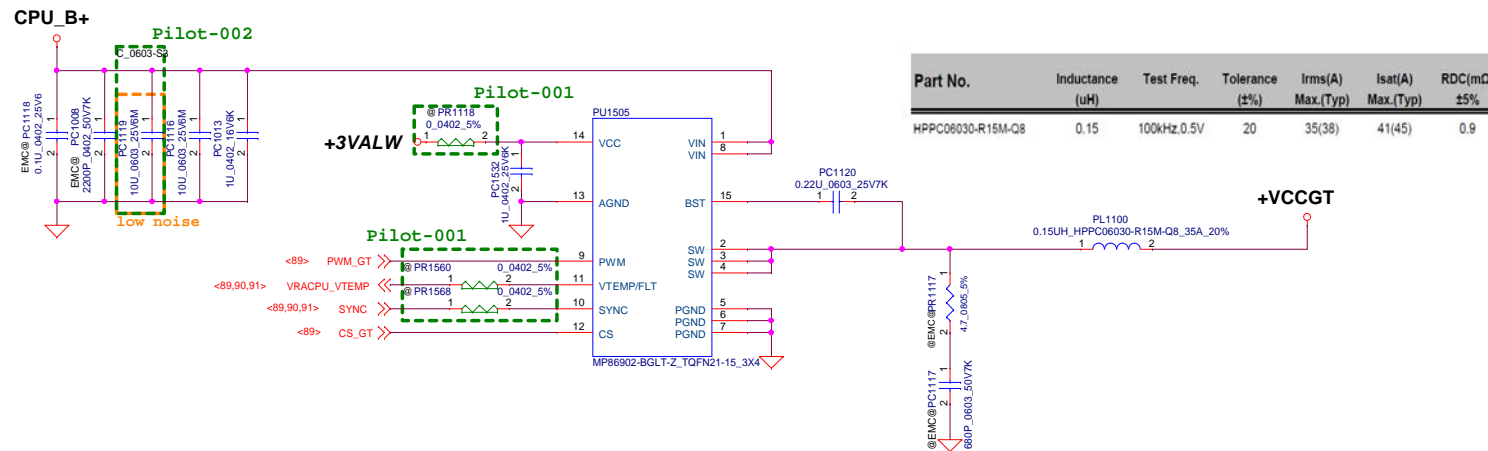
+1.0VS_VCCIO controller(35.37), Support component(35.38)
+1.0V_PRIM_CORE controller(35.39), Support component(35.40)

VCC_CORE Dr. MOS (36.2), Support component(36.3)



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								PWR_+VCORE	
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VCC_GT/SA Dr. MOS (36.2), Support component(36.3)



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+VCC_CORE

U22 Normal cap

VCC_CORE

U42:22U_0603*23 pcs
U42:22U_0603*27 pcs
U42:330u_B2*4 pcs
U22:330u_B2*2 pcs
U42:1U_0201*54 pcs
U22:1U_0201*54 pcs

+VCCGT

VCCGT

22U_0603*18 pcs
330u_B2*2 pcs
1U_0201*14 pcs

low noise

+VCC_CORE

U22 Normal cap

VCCSA

22U_0603*9 pcs
1U_0201*7 pcs

VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

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Security Classification					Compal Secret Data										Compal Electronics, Inc.														
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Security Classification					Compal Secret Data										Compal Electronics, Inc.																			
Issued Date					2014/10/17					Deciphered Date					2014/12/05					Title														
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