DW70 CALPELLA N11P-GE1 Schematics

uFCPGA Mobile Arrandale/Clarksfield

Intel Ibex Peak-M

2009-09-03

REV : SA

DY : Nopop Component
UMA : Pop when schematic is UMA
DIS : Pop when schematic is DIS
ARD : Pop when schematic is Arrandale
CFD : Pop when schematic is Clarksfield

UMA

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Title: *Cover Page*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

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Winery CALPELLA Block Diagram

PCB LAYER
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom

Project code : 91.4RU01.001
Part Number : 48.4RU06.0SA
PCB P/N : 09290
Revision : SA

Clock Generator
SLG8SP585 7

VRAM(gDDR3)
64Mbx16x8 (1GB)
84,85,89,90

VRAM

Nvidia
N11P-GE1(40nm)
80,81,82,83

100MHz/
2.5Gbps
PCIe x 16
Bandwidth
:8GB

Intel CPU
Arrandale
Clarksfield
8,9,10,11,12,13,14

DDRIII Channel A
Arrandale 800/1066MHz
Clarksfield 1066/1333MHz

DDRIII DM1 18
Arrandale 1066MHz
Clarksfield 1333MHz

DDRIII Channel B
Arrandale 800/1066MHz
Clarksfield 1066/1333MHz

DDRIII DM2 19
Arrandale 1066MHz
Clarksfield 1333MHz

HDMI 57
CRT 55
LCD 54

HDMI
RGB CRT
LVDS

Switchable

(Dual Channel)

DMIx4
FDI

Intel
PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

PCIE x 1
10/100/1000LOM
RTL8111DL
RJ45 CONN
(On LAN board)

Power SW
TPS2231R
New Card
(On I/O board)

PCIE x 1 USB 2.0 x 1

PCIE
100MHz
2.5Gbps

Mini-Card
802.11a/b/g/n 64

Touch Panel
(On LAN board)

Left Side:
USB x 2
63

Right Side:
USB x 2
(On LAN board)

CAMERA
(Option) 73

Bluetooth
(On Audio board)

Biometric 78

USB 2.0
480Mbps

SM Bus
400KHz

Free fall sensor 40

LPC Bus
33MHz

TPM CONN 76

DEBUG BOARD
GOLDEN FINGER 70

KBC
NUVOTON
NPCE781BA0DX 37

SPI
SM Bus

1394 Connector
(8 in 1)SD/MMC
MS/MS Pro/xD
(On I/O board)

CardReader
1394
RICOH
R5U230

PCIE
100MHz
2.5Gbps

Digital Mic Array
(Option)
MIC IN
HP OUT
(On Audio board)

HD AUDIO
CODEC
OP AMP
IDT
92HD81-UA

HD AUDIO

2CH SPEAKER

SATA, USB
SATA
SPI

USB,ESATA
Multi-Port x1 63

ODD
HDD 59

Flash ROM
4MB

Flash ROM
256kB 62

Touch
PAD 68

Int.
KB 68

Thermal
& Fan
EMC2102 39,58

Capacity Board

CPU DC/DC ISL62883 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51125 46	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC TPS51218 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC TPS51117 52	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_PCH

LDO APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO RT9025 87	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

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Title: Block Diagram

Size: Custom | Document Number: Vostro Calpella | Rev: SA

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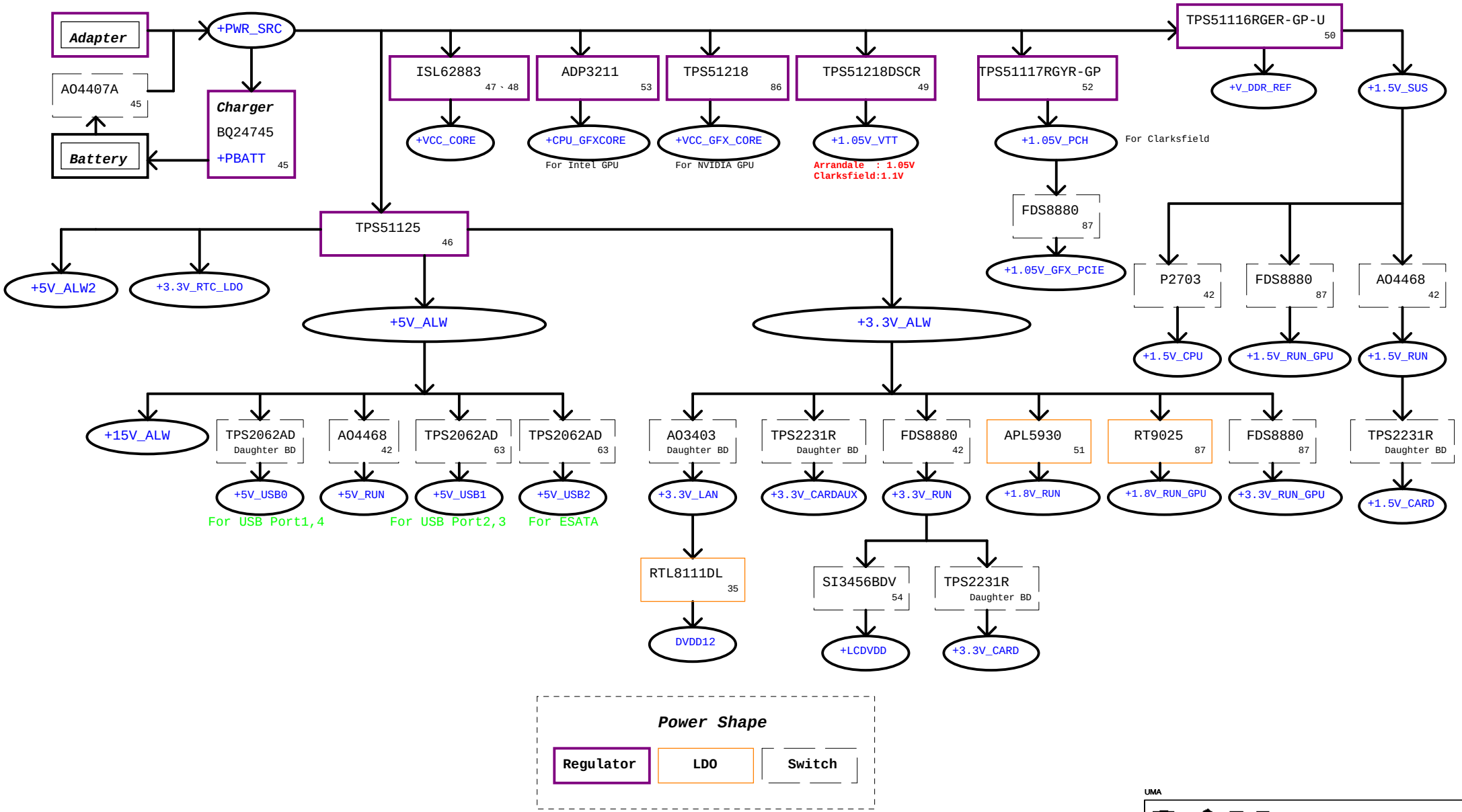

Power Shape

Regulator	LDO	Switch

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Title: ***Power Block Diagram***

Size	Document Number	Rev
Custom	***Vostro Calpella***	***SA***

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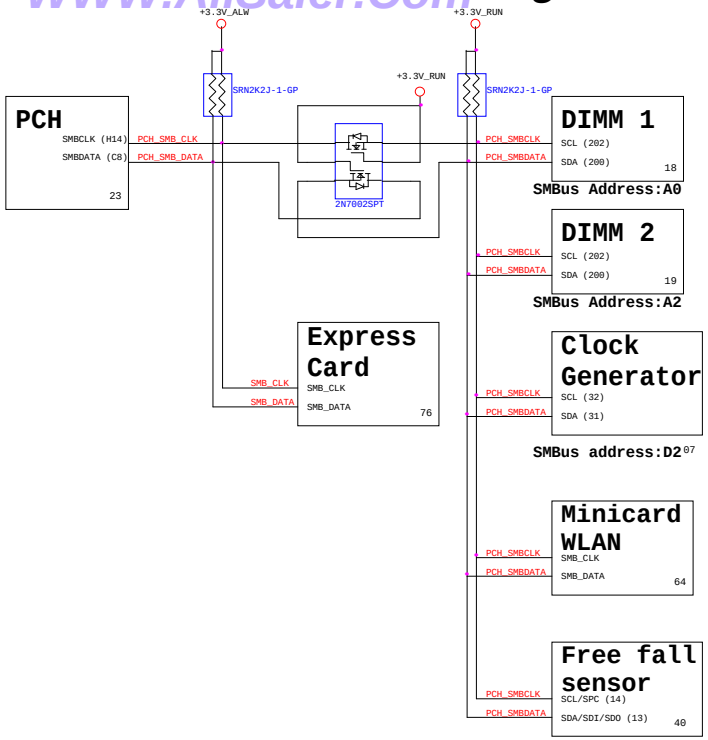
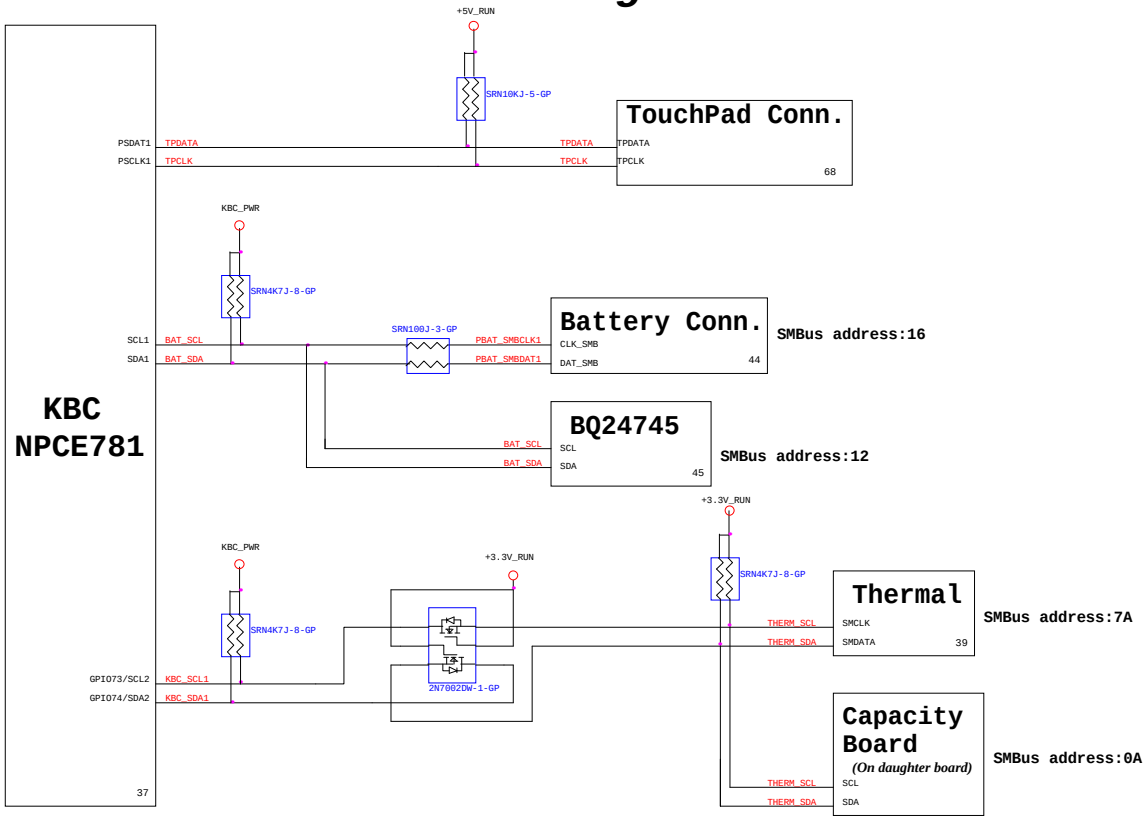
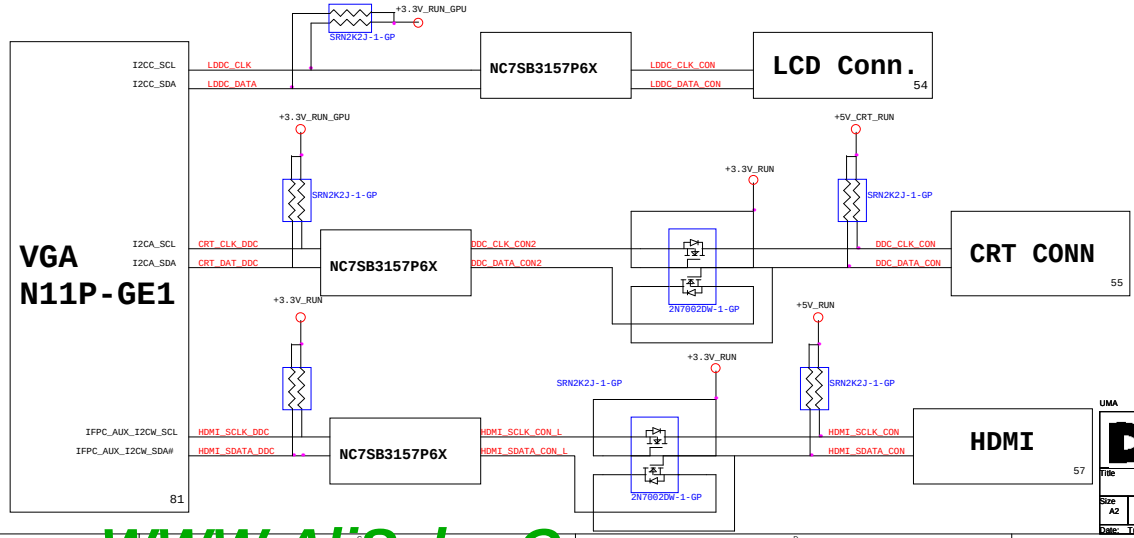
PCH SMBus Block Diagram



KBC SMBus Block Diagram



VGA SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	Vostro Calpella	SA

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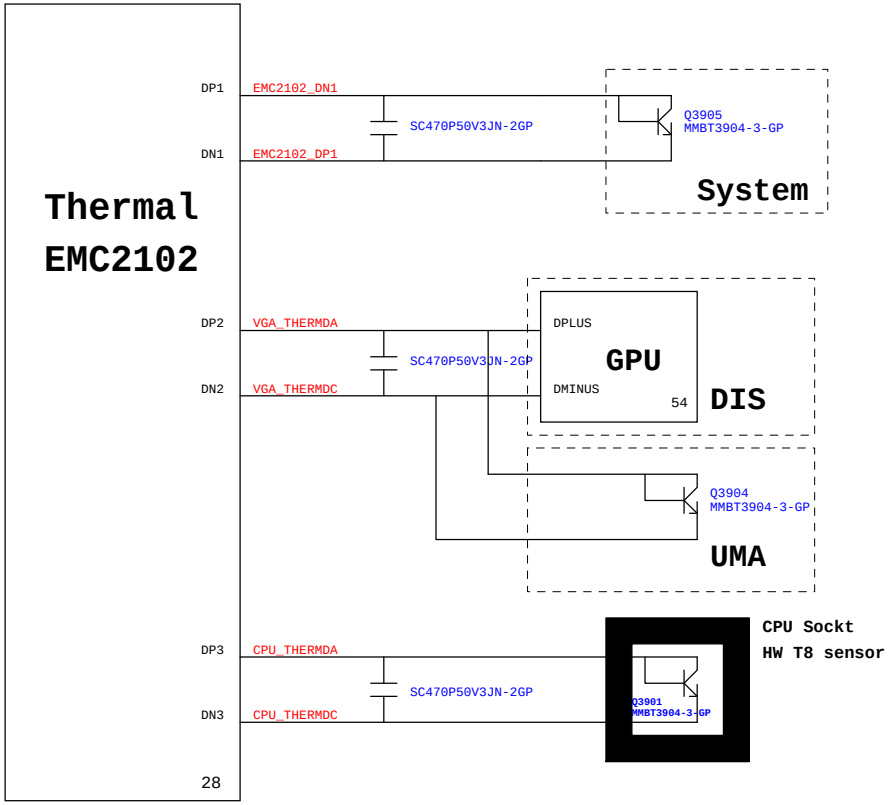
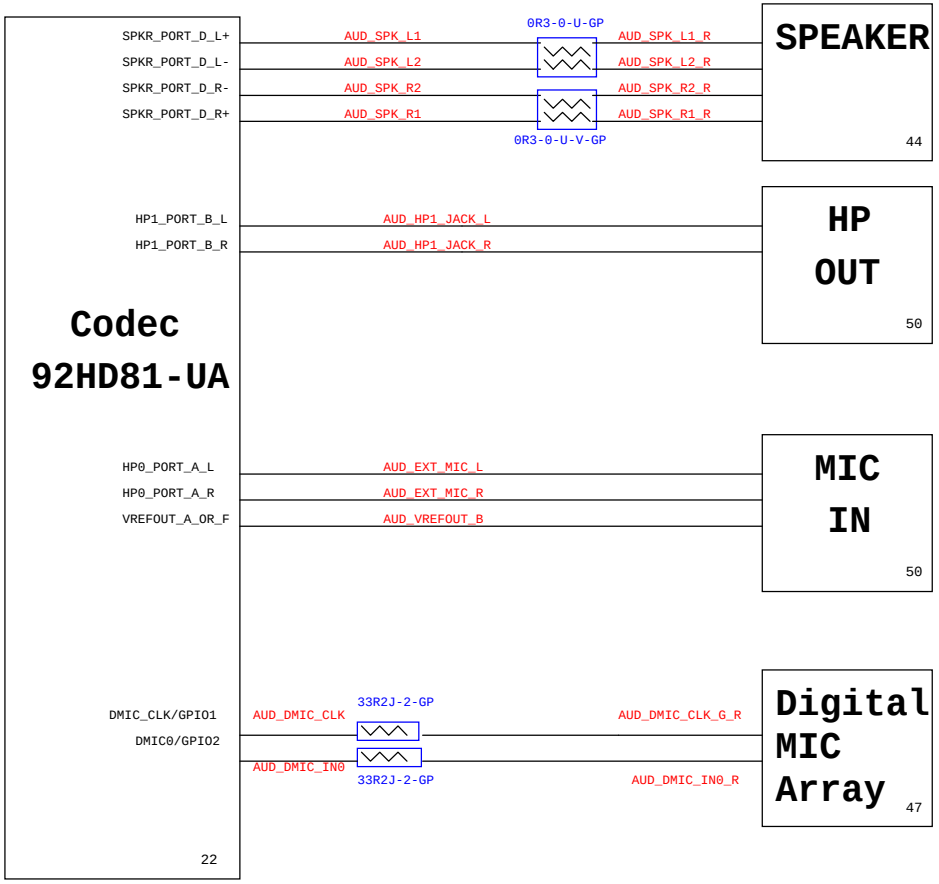
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:**Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:**Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:**Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:**Leave floating. (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)-** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)--**Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. CRB recommends 1-kΩ pull-down for FD Override. **Note:** There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)-**Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)--**Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	NC
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1 > LAN BOARD
1	USB4 > LAN BOARD
2	USB2 > M/B
3	USB3 > M/B
4	USB for ESATA
5	RESERVED
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Touch Panel
10	Biometric
11	CAMERA
12	New Card
13	WLAN

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Title: Table of Content

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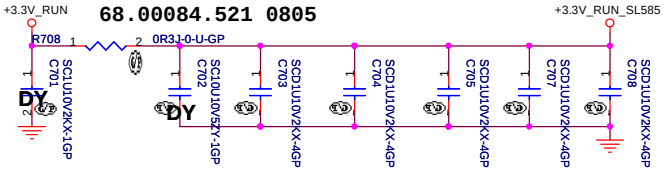
68.00119.131 0603
68.00084.521 0805



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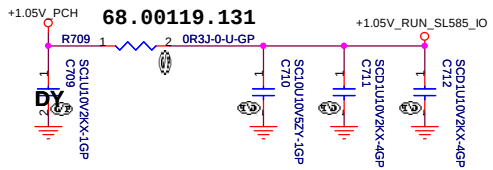
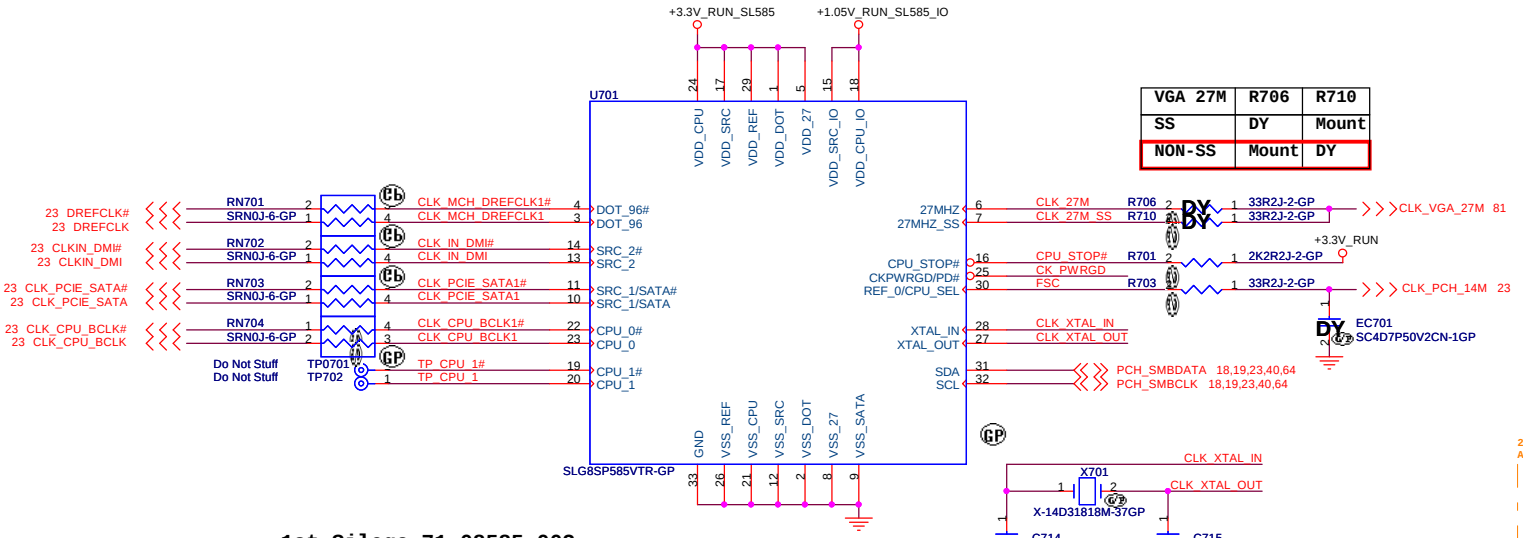
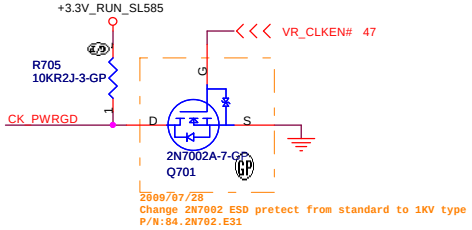
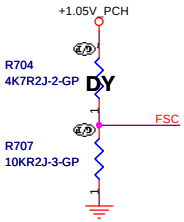




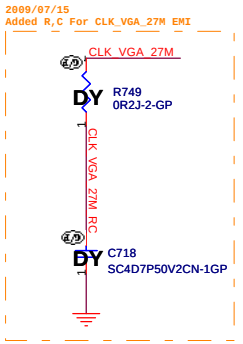
VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY



1st Silego 71.08585.003
2nd ICS 71.93197.003



FSC	0	1
SPEED	133MHz (Default)	100MHz



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Title: Clock Generator SLG8SP585

Size	Document Number	Rev
	Vostro Calpella	SA

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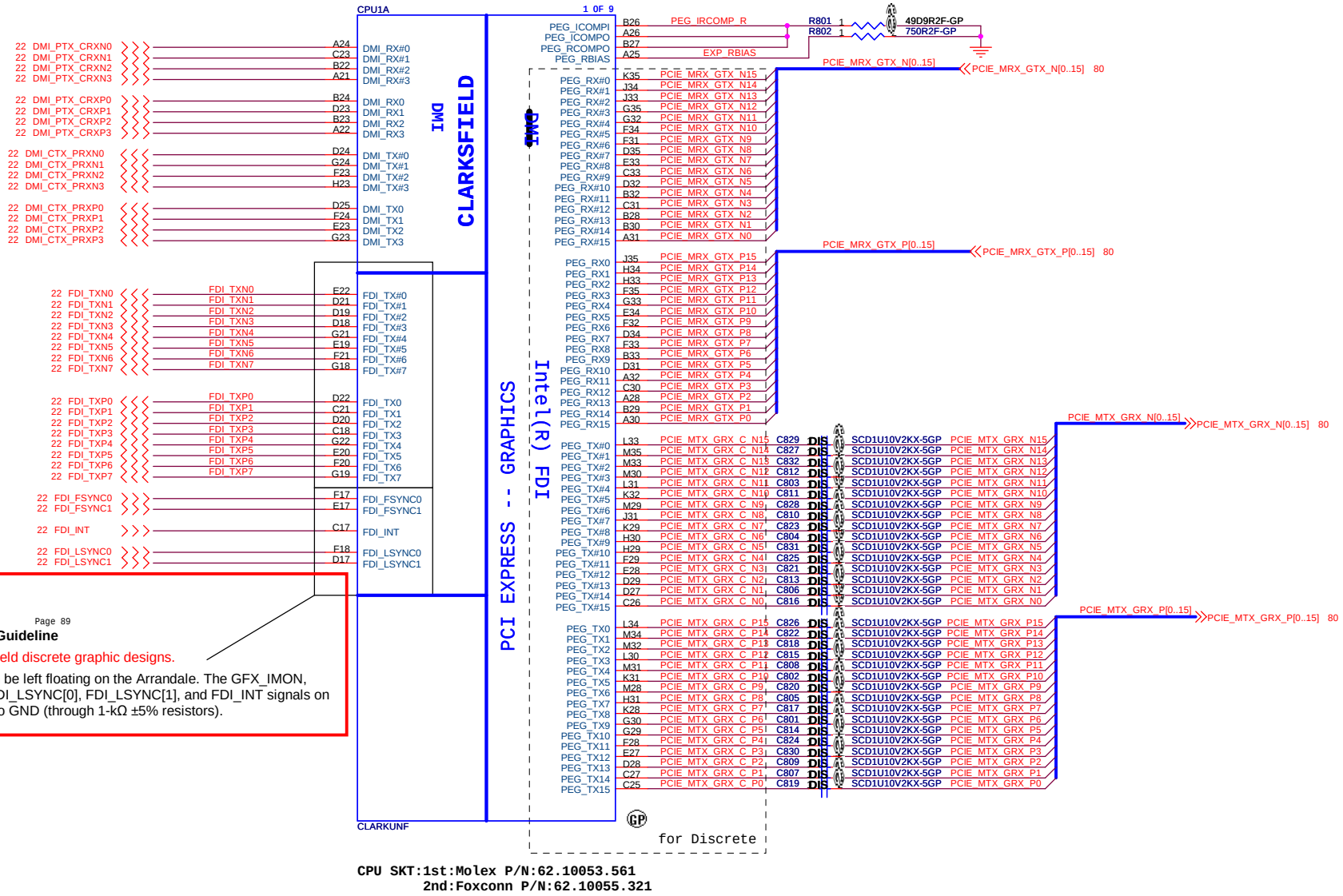

Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

CPU SKT:1st:Molex P/N:62.10053.561
2nd:Foxconn P/N:62.10055.321

UMA

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Title: **CPU (PCIE/DMI/FDI)**

Size	Document Number	Rev
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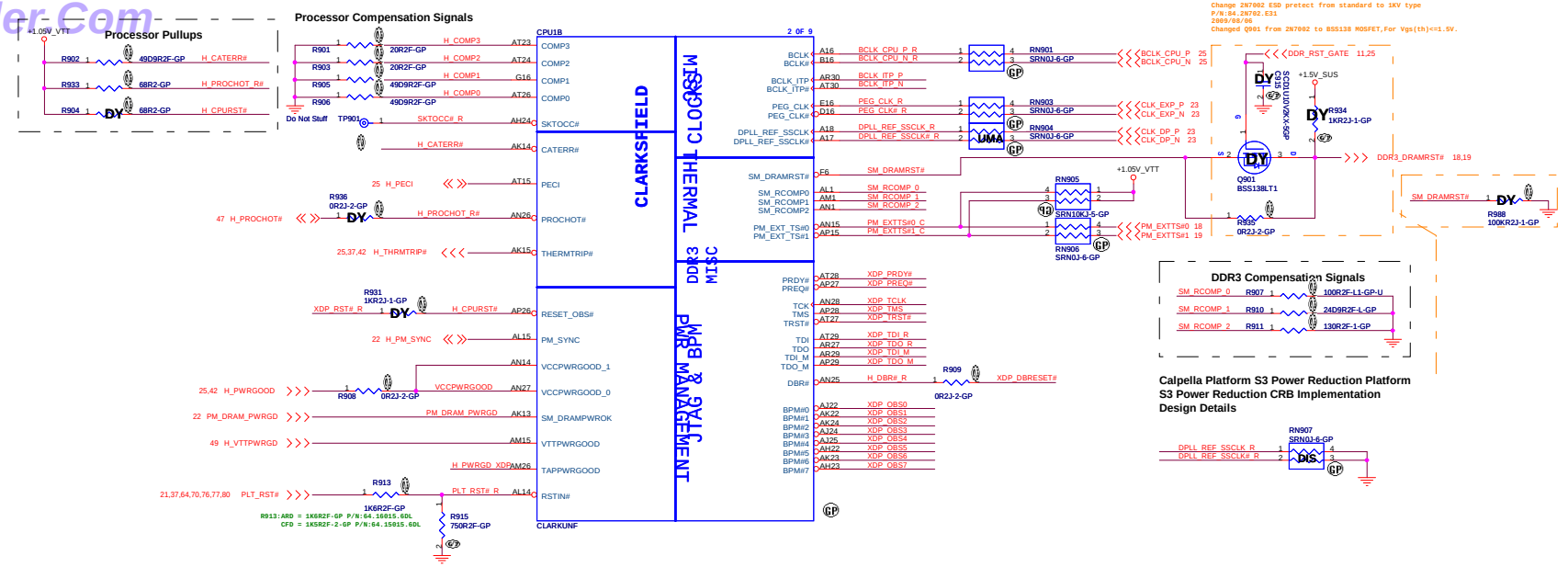
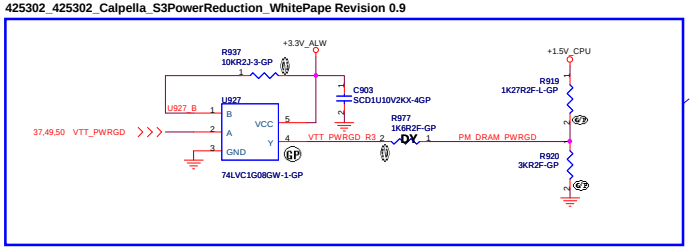


425302_425302_Calpella_S3PowerReduction_WhitePape Revision 0.9



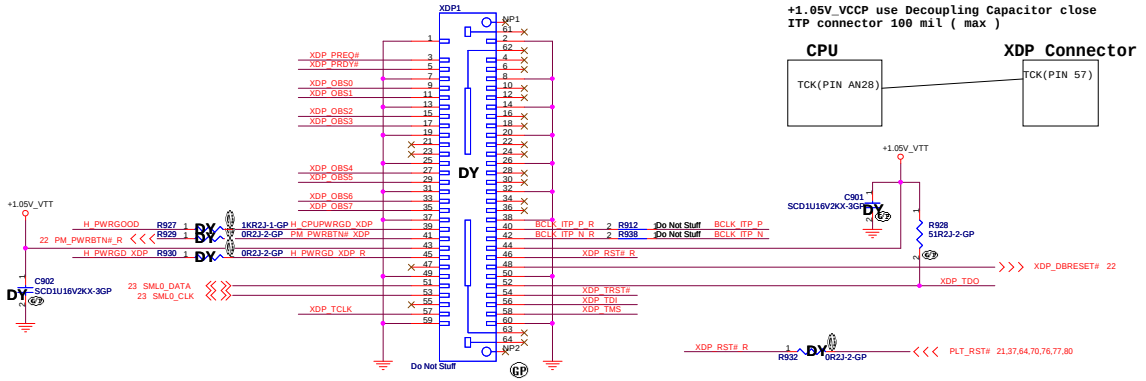
Normal

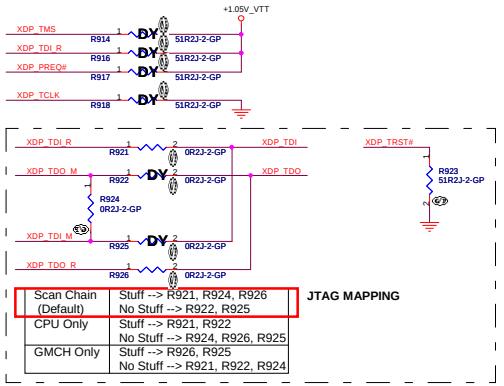
	R919	R920	R977
AUB	1.27k	3k	1.6k(DY)
CFD	1.1k	3k	1.5k(DY)

S3 Power Reduction circuit

	R919	R920	R977
AUB	1.1k(DY)	0.75k	1.6k
CFD	1.1k(DY)	0.75k	1.5k

XDP Connector





Scan Chain (Default)	Stuff --> R921, R924, R926 No Stuff --> R922, R925
CPU Only	Stuff --> R921, R922 No Stuff --> R924, R926, R925
GMCH Only	Stuff --> R926, R925 No Stuff --> R921, R922, R924

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
	Vostro Calpella	SA

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CLARKSFIELD

DDR SYSTEM MEMORY A

18 M_A_DQ[63..0] ⟷ M_A_DQ[63..0]

M_A_DQ0	A10	SA_DQ0
M_A_DQ1	C10	SA_DQ1
M_A_DQ2	C7	SA_DQ2
M_A_DQ3	A7	SA_DQ3
M_A_DQ4	B10	SA_DQ4
M_A_DQ5	D10	SA_DQ5
M_A_DQ6	E10	SA_DQ6
M_A_DQ7	A8	SA_DQ7
M_A_DQ8	D8	SA_DQ8
M_A_DQ9	F10	SA_DQ9
M_A_DQ10	E6	SA_DQ10
M_A_DQ11	F7	SA_DQ11
M_A_DQ12	E9	SA_DQ12
M_A_DQ13	B7	SA_DQ13
M_A_DQ14	F7	SA_DQ14
M_A_DQ15	C6	SA_DQ15
M_A_DQ16	H10	SA_DQ16
M_A_DQ17	G8	SA_DQ17
M_A_DQ18	K7	SA_DQ18
M_A_DQ19	J8	SA_DQ19
M_A_DQ20	G7	SA_DQ20
M_A_DQ21	G10	SA_DQ21
M_A_DQ22	J7	SA_DQ22
M_A_DQ23	J10	SA_DQ23
M_A_DQ24	L7	SA_DQ24
M_A_DQ25	M6	SA_DQ25
M_A_DQ26	M8	SA_DQ26
M_A_DQ27	L9	SA_DQ27
M_A_DQ28	L6	SA_DQ28
M_A_DQ29	K8	SA_DQ29
M_A_DQ30	N8	SA_DQ30
M_A_DQ31	P9	SA_DQ31
M_A_DQ32	AH5	SA_DQ32
M_A_DQ33	AF5	SA_DQ33
M_A_DQ34	AK6	SA_DQ34
M_A_DQ35	AK7	SA_DQ35
M_A_DQ36	AF6	SA_DQ36
M_A_DQ37	AG5	SA_DQ37
M_A_DQ38	AJ7	SA_DQ38
M_A_DQ39	AJ6	SA_DQ39
M_A_DQ40	AJ10	SA_DQ40
M_A_DQ41	AJ9	SA_DQ41
M_A_DQ42	AL10	SA_DQ42
M_A_DQ43	AK12	SA_DQ43
M_A_DQ44	AK8	SA_DQ44
M_A_DQ45	AL7	SA_DQ45
M_A_DQ46	AK11	SA_DQ46
M_A_DQ47	AL8	SA_DQ47
M_A_DQ48	AN8	SA_DQ48
M_A_DQ49	AM10	SA_DQ49
M_A_DQ50	AR11	SA_DQ50
M_A_DQ51	AL11	SA_DQ51
M_A_DQ52	AM9	SA_DQ52
M_A_DQ53	AN9	SA_DQ53
M_A_DQ54	AT11	SA_DQ54
M_A_DQ55	AP12	SA_DQ55
M_A_DQ56	AM12	SA_DQ56
M_A_DQ57	AN12	SA_DQ57
M_A_DQ58	AM13	SA_DQ58
M_A_DQ59	AT14	SA_DQ59
M_A_DQ60	AT12	SA_DQ60
M_A_DQ61	AL13	SA_DQ61
M_A_DQ62	AR14	SA_DQ62
M_A_DQ63	AP14	SA_DQ63

18 M_A_BS0	AC3	SA_BS0
18 M_A_BS1	AB2	SA_BS1
18 M_A_BS2	U7	SA_BS2

18 M_A_CAS#	AE1	SA_CAS#
18 M_A_RAS#	AB3	SA_RAS#
18 M_A_WE#	AE9	SA_WE#

SA_CK0	AA6	M_CLK_DDR0 18
SA_CK#0	AA7	M_CLK_DDR#0 18
SA_CKE0	P7	M_CKE0 18
SA_CK1	Y6	M_CLK_DDR1 18
SA_CK#1	Y5	M_CLK_DDR#1 18
SA_CKE1	P6	M_CKE1 18
SA_CS#0	AE2	M_CS0# 18
SA_CS#1	AE8	M_CS1# 18
SA_ODT0	AD8	M_ODT0 18
SA_ODT1	AF9	M_ODT1 18

SA_DM0	B9	M_A_DM0
SA_DM1	D7	M_A_DM1
SA_DM2	H7	M_A_DM2
SA_DM3	M7	M_A_DM3
SA_DM4	AG6	M_A_DM4
SA_DM5	AM7	M_A_DM5
SA_DM6	AN10	M_A_DM6
SA_DM7	AN13	M_A_DM7

M_A_DM[7..0] 18
M_A_DQS#[7..0] 18
M_A_DQS[7..0] 18
M_A_A[15..0] 18

SA_DQS#0	C9	M_A_DQS#0
SA_DQS#1	F8	M_A_DQS#1
SA_DQS#2	J9	M_A_DQS#2
SA_DQS#3	N9	M_A_DQS#3
SA_DQS#4	AH7	M_A_DQS#4
SA_DQS#5	AK9	M_A_DQS#5
SA_DQS#6	AP11	M_A_DQS#6
SA_DQS#7	AT13	M_A_DQS#7

SA_DQS0	C8	M_A_DQS0
SA_DQS1	F9	M_A_DQS1
SA_DQS2	H9	M_A_DQS2
SA_DQS3	M9	M_A_DQS3
SA_DQS4	AH8	M_A_DQS4
SA_DQS5	AK10	M_A_DQS5
SA_DQS6	AN11	M_A_DQS6
SA_DQS7	AR13	M_A_DQS7

SA_MA0	Y3	M_A_A0
SA_MA1	W1	M_A_A1
SA_MA2	AA8	M_A_A2
SA_MA3	AA3	M_A_A3
SA_MA4	V1	M_A_A4
SA_MA5	AA9	M_A_A5
SA_MA6	V8	M_A_A6
SA_MA7	T1	M_A_A7
SA_MA8	Y9	M_A_A8
SA_MA9	U6	M_A_A9
SA_MA10	AD4	M_A_A10
SA_MA11	T2	M_A_A11
SA_MA12	U3	M_A_A12
SA_MA13	AG8	M_A_A13
SA_MA14	T3	M_A_A14
SA_MA15	V9	M_A_A15

CLARKUNF

19 M_B_DQ[63..0] ⟷ M_B_DQ[63..0]

CPU1D — 4 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY - B

M_B_DQ0	B5	SB_DQ0
M_B_DQ1	A5	SB_DQ1
M_B_DQ2	C3	SB_DQ2
M_B_DQ3	B3	SB_DQ3
M_B_DQ4	E4	SB_DQ4
M_B_DQ5	A6	SB_DQ5
M_B_DQ6	A4	SB_DQ6
M_B_DQ7	C4	SB_DQ7
M_B_DQ8	D1	SB_DQ8
M_B_DQ9	D2	SB_DQ9
M_B_DQ10	F2	SB_DQ10
M_B_DQ11	F1	SB_DQ11
M_B_DQ12	C2	SB_DQ12
M_B_DQ13	E5	SB_DQ13
M_B_DQ14	F3	SB_DQ14
M_B_DQ15	G4	SB_DQ15
M_B_DQ16	H6	SB_DQ16
M_B_DQ17	G2	SB_DQ17
M_B_DQ18	J6	SB_DQ18
M_B_DQ19	J3	SB_DQ19
M_B_DQ20	G1	SB_DQ20
M_B_DQ21	G5	SB_DQ21
M_B_DQ22	J2	SB_DQ22
M_B_DQ23	J1	SB_DQ23
M_B_DQ24	J5	SB_DQ24
M_B_DQ25	K2	SB_DQ25
M_B_DQ26	L3	SB_DQ26
M_B_DQ27	M1	SB_DQ27
M_B_DQ28	K5	SB_DQ28
M_B_DQ29	K4	SB_DQ29
M_B_DQ30	M4	SB_DQ30
M_B_DQ31	N5	SB_DQ31
M_B_DQ32	AF3	SB_DQ32
M_B_DQ33	AG1	SB_DQ33
M_B_DQ34	AJ3	SB_DQ34
M_B_DQ35	AK1	SB_DQ35
M_B_DQ36	AG4	SB_DQ36
M_B_DQ37	AG3	SB_DQ37
M_B_DQ38	AJ4	SB_DQ38
M_B_DQ39	AH4	SB_DQ39
M_B_DQ40	AK3	SB_DQ40
M_B_DQ41	AK4	SB_DQ41
M_B_DQ42	AM6	SB_DQ42
M_B_DQ43	AN2	SB_DQ43
M_B_DQ44	AK5	SB_DQ44
M_B_DQ45	AK2	SB_DQ45
M_B_DQ46	AM4	SB_DQ46
M_B_DQ47	AM3	SB_DQ47
M_B_DQ48	AP3	SB_DQ48
M_B_DQ49	AN5	SB_DQ49
M_B_DQ50	AT4	SB_DQ50
M_B_DQ51	AN6	SB_DQ51
M_B_DQ52	AN4	SB_DQ52
M_B_DQ53	AN3	SB_DQ53
M_B_DQ54	AT5	SB_DQ54
M_B_DQ55	AT6	SB_DQ55
M_B_DQ56	AN7	SB_DQ56
M_B_DQ57	AP6	SB_DQ57
M_B_DQ58	AP8	SB_DQ58
M_B_DQ59	AT9	SB_DQ59
M_B_DQ60	AT7	SB_DQ60
M_B_DQ61	AP9	SB_DQ61
M_B_DQ62	AR10	SB_DQ62
M_B_DQ63	AT10	SB_DQ63

19 M_B_BS0	AB1	SB_BS0
19 M_B_BS1	W5	SB_BS1
19 M_B_BS2	R7	SB_BS2

19 M_B_CAS#	AC5	SB_CAS#
19 M_B_RAS#	Y7	SB_RAS#
19 M_B_WE#	AC6	SB_WE#

SB_CK0	W8	M_CLK_DDR2 19
SB_CK#0	W9	M_CLK_DDR#2 19
SB_CKE0	M3	M_CKE2 19
SB_CK1	V7	M_CLK_DDR3 19
SB_CK#1	V6	M_CLK_DDR#3 19
SB_CKE1	M2	M_CKE3 19
SB_CS#0	AB8	M_CS2# 19
SB_CS#1	AD6	M_CS3# 19
SB_ODT0	AC7	M_ODT2 19
SB_ODT1	AD1	M_ODT3 19

SB_DM0	D4	M_B_DM0
SB_DM1	E1	M_B_DM1
SB_DM2	H3	M_B_DM2
SB_DM3	K1	M_B_DM3
SB_DM4	AH1	M_B_DM4
SB_DM5	AL2	M_B_DM5
SB_DM6	AR4	M_B_DM6
SB_DM7	AT8	M_B_DM7

M_B_DM[7..0] 19
M_B_DQS#[7..0] 19
M_B_DQS[7..0] 19
M_B_A[15..0] 19

SB_DQS#0	D5	M_B_DQS#0
SB_DQS#1	F4	M_B_DQS#1
SB_DQS#2	J4	M_B_DQS#2
SB_DQS#3	L4	M_B_DQS#3
SB_DQS#4	AH2	M_B_DQS#4
SB_DQS#5	AL4	M_B_DQS#5
SB_DQS#6	AR5	M_B_DQS#6
SB_DQS#7	AR8	M_B_DQS#7

SB_DQS0	C5	M_B_DQS0
SB_DQS1	E3	M_B_DQS1
SB_DQS2	H4	M_B_DQS2
SB_DQS3	M5	M_B_DQS3
SB_DQS4	AG2	M_B_DQS4
SB_DQS5	AL5	M_B_DQS5
SB_DQS6	AP5	M_B_DQS6
SB_DQS7	AR7	M_B_DQS7

SB_MA0	U5	M_B_A0
SB_MA1	V2	M_B_A1
SB_MA2	T5	M_B_A2
SB_MA3	V3	M_B_A3
SB_MA4	R1	M_B_A4
SB_MA5	T8	M_B_A5
SB_MA6	R2	M_B_A6
SB_MA7	R6	M_B_A7
SB_MA8	R4	M_B_A8
SB_MA9	R5	M_B_A9
SB_MA10	AB5	M_B_A10
SB_MA11	P3	M_B_A11
SB_MA12	R3	M_B_A12
SB_MA13	AF7	M_B_A13
SB_MA14	P5	M_B_A14
SB_MA15	N1	M_B_A15

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size | Document Number: Vostro Calpella | Rev: SA

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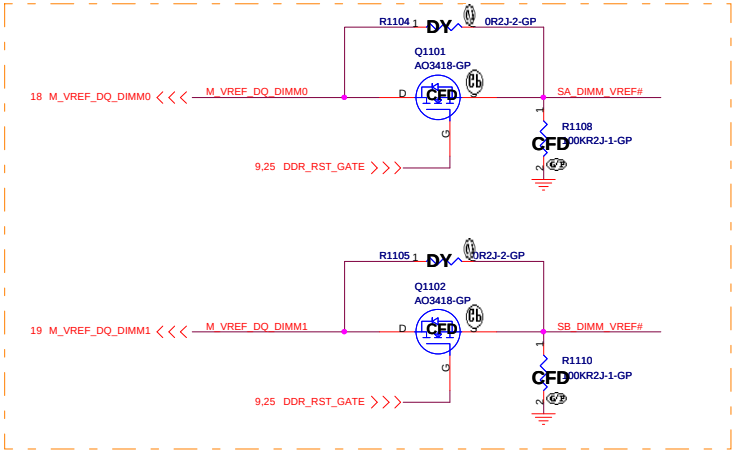
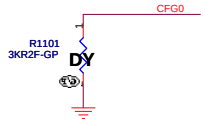
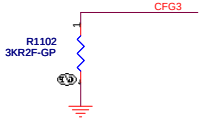


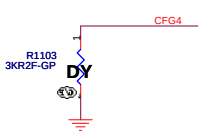


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

DIS改5%



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

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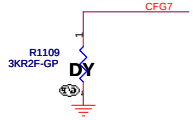
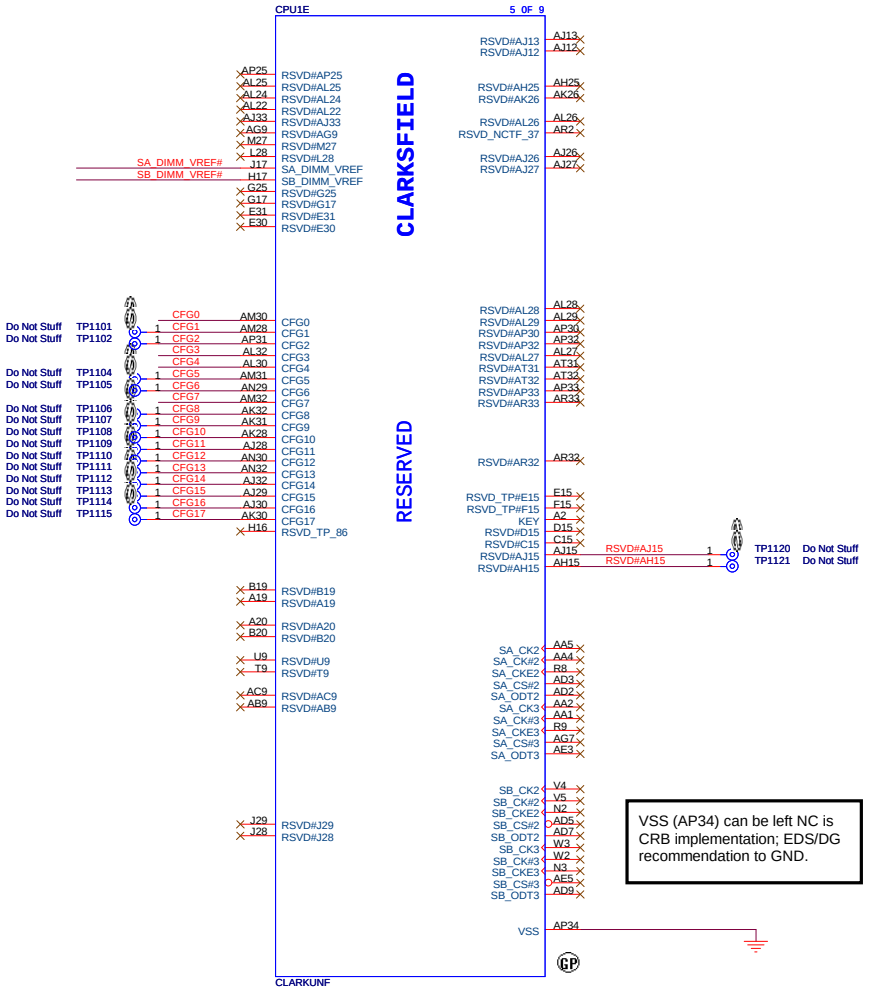


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

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Title: CPU (RESERVED)

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PROCESSOR CORE POWER

Clarksfield = 52A

Arrandale = 48A

+VCC_CORE

C1206 C1207 C1208 C1209 C1220 C1210 — SC10U6D3V5MX-3GP

C1212 C1213 C1214 C1215 C1223 C1224 — SC10U6D3V5MX-3GP

C1225 C1226 C1227 C1228 C1229 C1230 C1231 C1232 — SC22U6D3V5MX-2GP / SC10U6D3V5MX-3GP

C1235 C1236 C1237 C1238 C1239 C1240 C1241 C1242 — SC10U6D3V5MX-3GP / SC22U6D3V5MX-2GP

C1243 DY SC10U6D3V5MX-3GP

CPU1F 6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

CLARKUNF

VCC: AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VTT0: AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

VTT0: AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05V_VTT

C1201 C1202 C1217 C1218 C1204 C1205 — SC10U10V5ZY-1GP

C1234 — SC10U6D3V5MX-3GP

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V

DIS(Clarksfield +1.05V_VTT) = 14.4A

DIS(Arrandale +1.05V_VTT) = 20.95A

UMA(Arrandale +1.05V_VTT) = 19.84A

POWER

CPU VIDS

PSI# AN33 — PSI# 47

VID AK35 CPU_VID0
VID AK33 CPU_VID1
VID AK34 CPU_VID2
VID AL35 CPU_VID3
VID AL33 CPU_VID4
VID AM33 CPU_VID5
VID AM35 CPU_VID6
PROC_DPRSLPVR AM34 — PM_DPRSLPVR 47

CPU_VID[6..0] 47

VTT_SELECT G15 — TP_VTT_SELECT 1 — TP1203 Do Not Stuff

VTT_SELECT = Low, 1.1V
VTT_SELECT = High, 1.05V

SENSE LINES

ISENSE AN35 — IMVP_IMON 47

VCC_SENSE AJ34 VCC_SENSE
VSS_SENSE AJ35 VSS_SENSE

VCC_SENSE 47
VSS_SENSE 47

VTT_SENSE B15
VSS_SENSE_VTT A15 — TP_VSS_SENSE_VTT 1 — TP1202 Do Not Stuff

VTT_SENSE 49

+VCC_CORE

R1201 100R2F-L1-GP-U

R1204 100R2F-L1-GP-U

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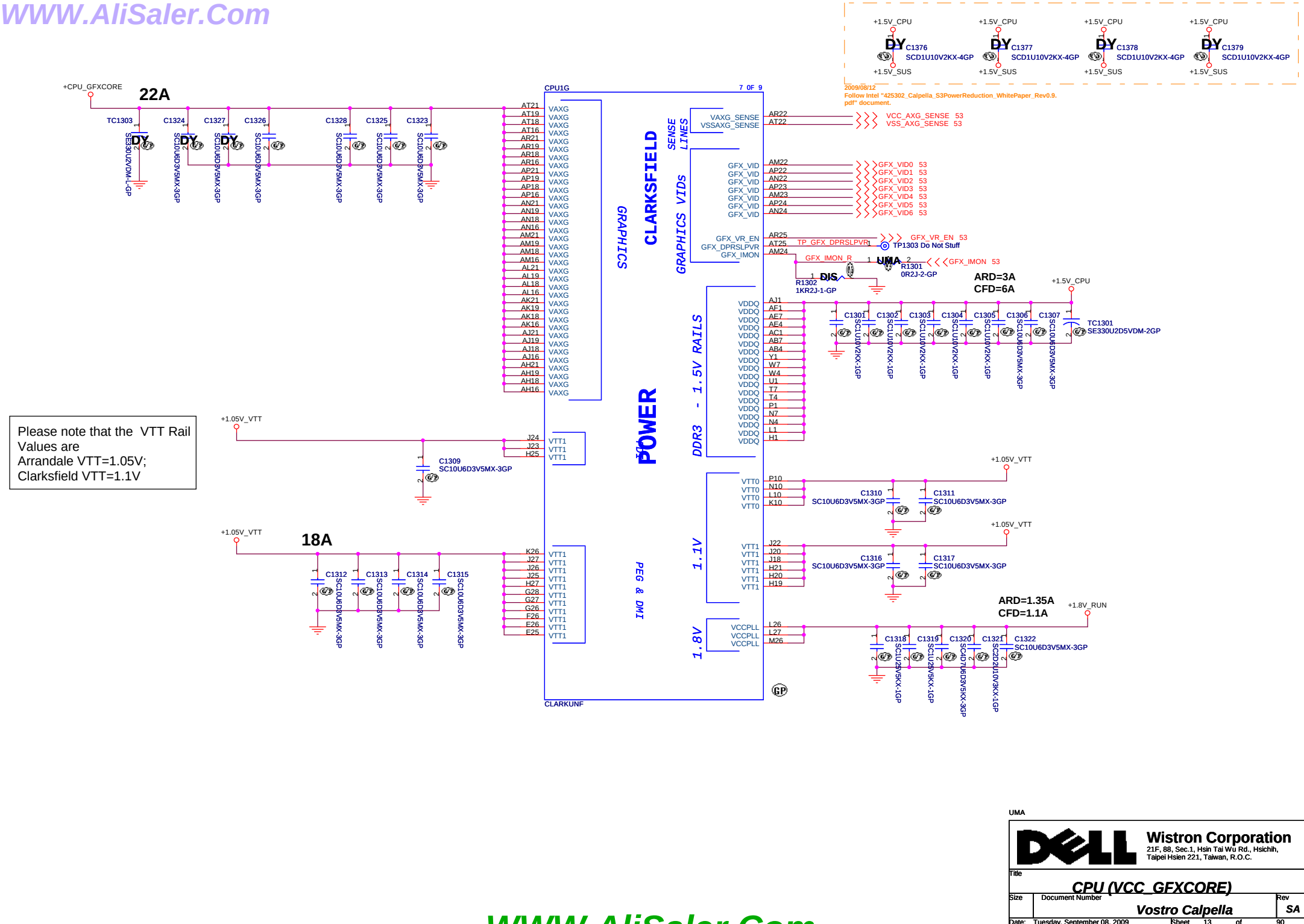
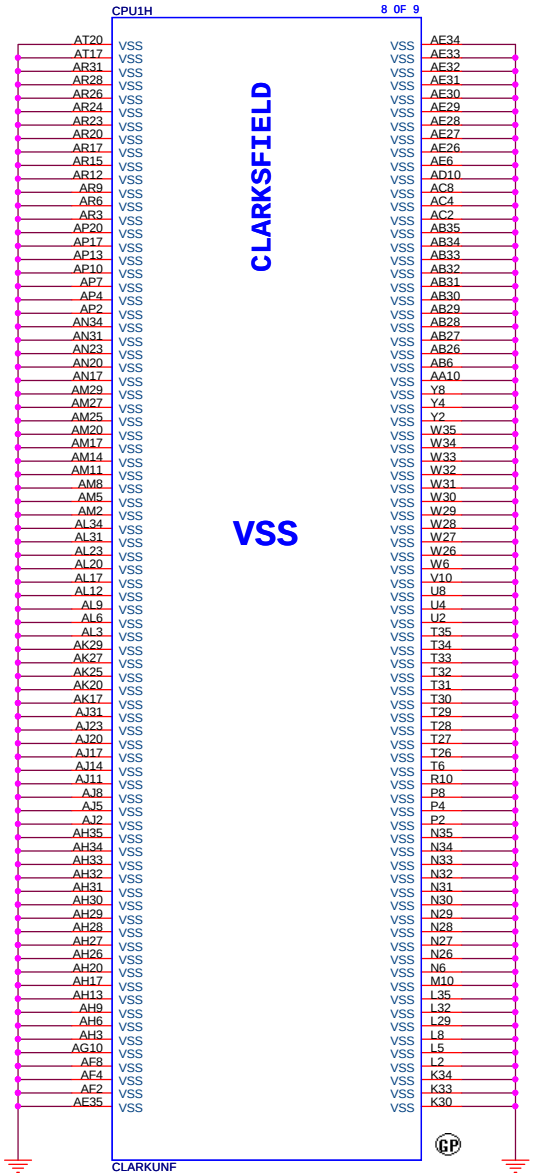
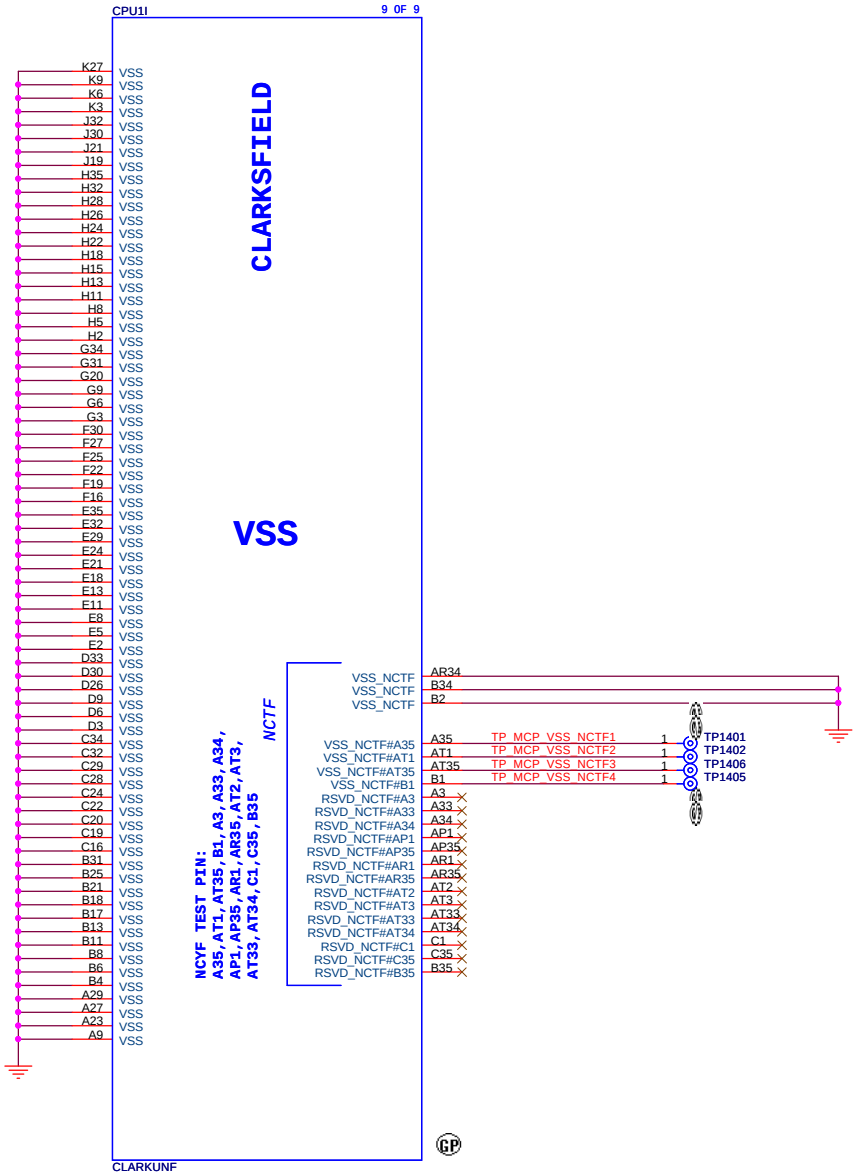
Title: CPU (VCC_CORE)

Size | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 12 of 90







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Title	***CPU (VSS)***	
Size	Document Number: ***Vostro Calpella***	Rev: ***SA***
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Title: *Reserved*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 15 of 90

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Title: *Reserved*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 16 of 90

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Title: (Reserve)

Size: A3 | Document Number: Vostro Calpella | Rev: SA

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SSID = MEMORY

10 M_A_DQS#[7..0]
10 M_A_DQ[63..0]
10 M_A_DM[7..0]
10 M_A_DQS[7..0]
10 M_A_A[15..0]

Layout Note:
Place near DM1

+1.5V_SUS
C1803 SC10U6D3V5MX-3GP
C1804 SC10U6D3V5MX-3GP
C1812 SC10U6D3V5MX-3GP
C1802 SC10U6D3V5MX-3GP
C1811 SC10U6D3V5MX-3GP
C1816 SC10U6D3V5MX-3GP
TC1803 ST330U2D5VBM-1-GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT
C1814 SC1U10V2KX-1GP
C1813 SC1U10V2KX-1GP
C1815 SC1U10V2KX-1GP
C1801 SC1U10V2KX-1GP
C1823 SC10U6D3V5MX-3GP

+1.5V_SUS
C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875 SCD1U10V2KX-4GP

2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

DM1

M_A_A0	98	A0	
M_A_A1	97	A1	
M_A_A2	96	A2	
M_A_A3	95	A3	
M_A_A4	92	A4	
M_A_A5	91	A5	
M_A_A6	90	A6	
M_A_A7	86	A7	
M_A_A8	89	A8	
M_A_A9	85	A9	
M_A_A10	107	A10/AP	
M_A_A11	84	A11	
M_A_A12	83	A12	
M_A_A13	119	A13	
M_A_A14	80	A14	
M_A_A15	78	A15	
M_A_BS2	79	A16/BA2	10 M_A_BS2
M_A_BS0	109	BA0	10 M_A_BS0
M_A_BS1	108	BA1	10 M_A_BS1
M_A_DQ0	5	DQ0	
M_A_DQ1	7	DQ1	
M_A_DQ2	15	DQ2	
M_A_DQ3	17	DQ3	
M_A_DQ4	4	DQ4	
M_A_DQ5	6	DQ5	
M_A_DQ6	16	DQ6	
M_A_DQ7	18	DQ7	
M_A_DQ8	21	DQ8	
M_A_DQ9	23	DQ9	
M_A_DQ10	33	DQ10	
M_A_DQ11	35	DQ11	
M_A_DQ12	22	DQ12	
M_A_DQ13	24	DQ13	
M_A_DQ14	34	DQ14	
M_A_DQ15	36	DQ15	
M_A_DQ16	39	DQ16	
M_A_DQ17	41	DQ17	
M_A_DQ18	51	DQ18	
M_A_DQ19	53	DQ19	
M_A_DQ20	40	DQ20	
M_A_DQ21	42	DQ21	
M_A_DQ22	50	DQ22	
M_A_DQ23	52	DQ23	
M_A_DQ24	57	DQ24	
M_A_DQ25	59	DQ25	
M_A_DQ26	67	DQ26	
M_A_DQ27	69	DQ27	
M_A_DQ28	56	DQ28	
M_A_DQ29	58	DQ29	
M_A_DQ30	68	DQ30	
M_A_DQ31	70	DQ31	
M_A_DQ32	129	DQ32	
M_A_DQ33	131	DQ33	
M_A_DQ34	141	DQ34	
M_A_DQ35	143	DQ35	
M_A_DQ36	130	DQ36	
M_A_DQ37	132	DQ37	
M_A_DQ38	140	DQ38	
M_A_DQ39	142	DQ39	
M_A_DQ40	147	DQ40	
M_A_DQ41	149	DQ41	
M_A_DQ42	157	DQ42	
M_A_DQ43	159	DQ43	
M_A_DQ44	146	DQ44	
M_A_DQ45	148	DQ45	
M_A_DQ46	158	DQ46	
M_A_DQ47	160	DQ47	
M_A_DQ48	163	DQ48	
M_A_DQ49	165	DQ49	
M_A_DQ50	175	DQ50	
M_A_DQ51	177	DQ51	
M_A_DQ52	164	DQ52	
M_A_DQ53	166	DQ53	
M_A_DQ54	174	DQ54	
M_A_DQ55	176	DQ55	
M_A_DQ56	181	DQ56	
M_A_DQ57	183	DQ57	
M_A_DQ58	191	DQ58	
M_A_DQ59	193	DQ59	
M_A_DQ60	180	DQ60	
M_A_DQ61	182	DQ61	
M_A_DQ62	192	DQ62	
M_A_DQ63	194	DQ63	
M_A_DQS#0	10	DQS0#	
M_A_DQS#1	27	DQS1#	
M_A_DQS#2	45	DQS2#	
M_A_DQS#3	62	DQS3#	
M_A_DQS#4	135	DQS4#	
M_A_DQS#5	152	DQS5#	
M_A_DQS#6	169	DQS6#	
M_A_DQS#7	186	DQS7#	
M_A_DQS0	12	DQS0	
M_A_DQS1	29	DQS1	
M_A_DQS2	47	DQS2	
M_A_DQS3	64	DQS3	
M_A_DQS4	137	DQS4	
M_A_DQS5	154	DQS5	
M_A_DQS6	171	DQS6	
M_A_DQS7	188	DQS7	
M_ODT0	116	ODT0	10 M_ODT0
M_ODT1	120	ODT1	10 M_ODT1
	126	VREF_CA	
M_VREF_DQ_DIMM0	1	VREF_DQ	
9,19 DDR3_DRAMRST#	30	RESET#	
	203	VTT1	
	204	VTT2	

NP1	NP1		
NP2	NP2		
RAS#	110	M_A_RAS# 10	
WE#	113	M_A_WE# 10	
CAS#	115	M_A_CAS# 10	
CS0#	114	M_CS0# 10	
CS1#	121	M_CS1# 10	
CKE0	73	M_CKE0 10	
CKE1	74	M_CKE1 10	
CK0	101	M_CLK_DDR0	M_CLK_DDR0 10
CK0#	103	M_CLK_DDR#0	M_CLK_DDR#0 10
CK1	102	M_CLK_DDR1	M_CLK_DDR1 10
CK1#	104	M_CLK_DDR#1	M_CLK_DDR#1 10
DM0	11	M_A_DM0	
DM1	28	M_A_DM1	
DM2	46	M_A_DM2	
DM3	63	M_A_DM3	
DM4	136	M_A_DM4	
DM5	153	M_A_DM5	
DM6	170	M_A_DM6	
DM7	187	M_A_DM7	
SDA	200	PCH_SMBDATA	PCH_SMBDATA 7,19,23,40,64
SCL	202	PCH_SMBCLK	PCH_SMBCLK 7,19,23,40,64
EVENT#	198		PM_EXTTS#0 9
VDDSPD	199		
SA0	197	SA0_DM1	
SA1	201	SA1_DM1	
NC#1	77		
NC#2	122		
NC#/TEST	125		
VDD1	75		
VDD2	76		
VDD3	81		
VDD4	82		
VDD5	87		
VDD6	88		
VDD7	93		
VDD8	94		
VDD9	99		
VDD10	100		
VDD11	105		
VDD12	106		
VDD13	111		
VDD14	112		
VDD15	117		
VDD16	118		
VDD17	123		
VDD18	124		
VSS	2		
VSS	3		
VSS	8		
VSS	9		
VSS	13		
VSS	14		
VSS	19		
VSS	20		
VSS	25		
VSS	26		
VSS	31		
VSS	32		
VSS	37		
VSS	38		
VSS	43		
VSS	44		
VSS	48		
VSS	49		
VSS	54		
VSS	55		
VSS	60		
VSS	61		
VSS	65		
VSS	66		
VSS	71		
VSS	72		
VSS	127		
VSS	128		
VSS	133		
VSS	134		
VSS	138		
VSS	139		
VSS	144		
VSS	145		
VSS	150		
VSS	151		
VSS	155		
VSS	156		
VSS	161		
VSS	162		
VSS	167		
VSS	168		
VSS	172		
VSS	173		
VSS	178		
VSS	179		
VSS	184		
VSS	185		
VSS	189		
VSS	190		
VSS	195		
VSS	196		
VSS	205		
VSS	206		

Height 5.2mm

DDR3-204P-25-GP
62.10017.K11

2009/07/30
Change connector to 62.10017.K11

+1.5V_SUS
+3.3V_RUN
C1806 SCD1U16V2KX-3GP
C1807 SC2D2U10V3KX-1GP
DY

SA0_DM1
SA1_DM1
R1802 10KR2J-3-GP
R1801 10KR2J-3-GP

SMBUS address:A0

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

put near connector

M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
C1821 Do Not Stuff
C1819 Do Not Stuff
C1820 Do Not Stuff
C1818 Do Not Stuff

+V_DDR_REF
R1803 ARDDR2J-2-GP
M_VREF_DQ_DIMM0 11
C1817 SCD1U16V2KX-3GP
C1805 SC2D2U10V3KX-1GP

+V_DDR_REF
C1810 SCD1U16V2KX-3GP
C1809 SC2D2U10V3KX-1GP
M_VREF_DQ_DIMM0

+0.75V_DDR_VTT

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT1
Size: Custom
Document Number: Vostro Calpella
Rev: SA
Date: Tuesday, September 08, 2009
Sheet 18 of 90

SSID = MEMORY

10 M_B_DQS#[7..0]
10 M_B_DQ[63..0]
10 M_B_DM[7..0]
10 M_B_DQS[7..0]
10 M_B_A[15..0]

Layout Note:
Place near DM2

+1.5V_SUS
TC1903 ST330U2D5VBM-1-GP
C1919 SC10U6D3V5MX-3GP
C1905 SC10U6D3V5MX-3GP
C1911 SC10U6D3V5MX-3GP
C1916 SC10U6D3V5MX-3GP
C1913 SC10U6D3V5MX-3GP
C1920 SC10U6D3V5MX-3GP

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT
C1908 SC1U10V2KX-1GP
C1917 SC1U10V2KX-1GP
C1909 SC1U10V2KX-1GP
C1918 SC1U10V2KX-1GP

+1.5V_SUS
C1976 SCD1U10V2KX-4GP
C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

2009/08/12
Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9. pdf" document.

+V_DDR_REF
R1905 ARD 0R2J-2-GP
C1910 SCD1U16V2KX-3GP
C1912 SC2D2U10V3KX-1GP
C1907 SCD1U16V2KX-3GP
C1914 SC2D2U10V3KX-1GP
M_VREF_DQ_DIMM1 11

DM2
DDR3-204P-24-GP
62.10017.K01

Height 9.2mm

10 M_B_BS2
10 M_B_BS0
10 M_B_BS1
10 M_ODT2
10 M_ODT3
9,18 DDR3_DRAMRST#
M_VREF_DQ_DIMM1
+0.75V_DDR_VTT

M_B_RAS# 10
M_B_WE# 10
M_B_CAS# 10
M_CS2# 10
M_CS3# 10
M_CKE2 10
M_CKE3 10
M_CLK_DDR2 10
M_CLK_DDR#2 10
M_CLK_DDR3 10
M_CLK_DDR#3 10
PCH_SMBDATA 7,18,23,40,64
PCH_SMBCLK 7,18,23,40,64
PM_EXTTS#1 9
SA0_DM2
SA1_DM2
+1.5V_SUS

+3.3V_RUN
R1903 10KR2J-3-GP DY
R1904 10KR2J-3-GP
R1901 10KR2J-3-GP
R1902 10KR2J-3-GP DY
SA1_DM2
SA0_DM2

SMBUS address:A4

+3.3V_RUN
C1906 SCD1U16V2KX-3GP DY
C1921 SC2D2U10V3KX-1GP

put near connector
M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
C1901 Do Not Stuff
C1904 Do Not Stuff
C1902 Do Not Stuff
C1903 Do Not Stuff

2009/07/30
Change connector to 62.10017.K01

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII-SODIMM SLOT2
Size: Custom
Document Number: Vostro Calpella
Rev: SA
Date: Tuesday, September 08, 2009
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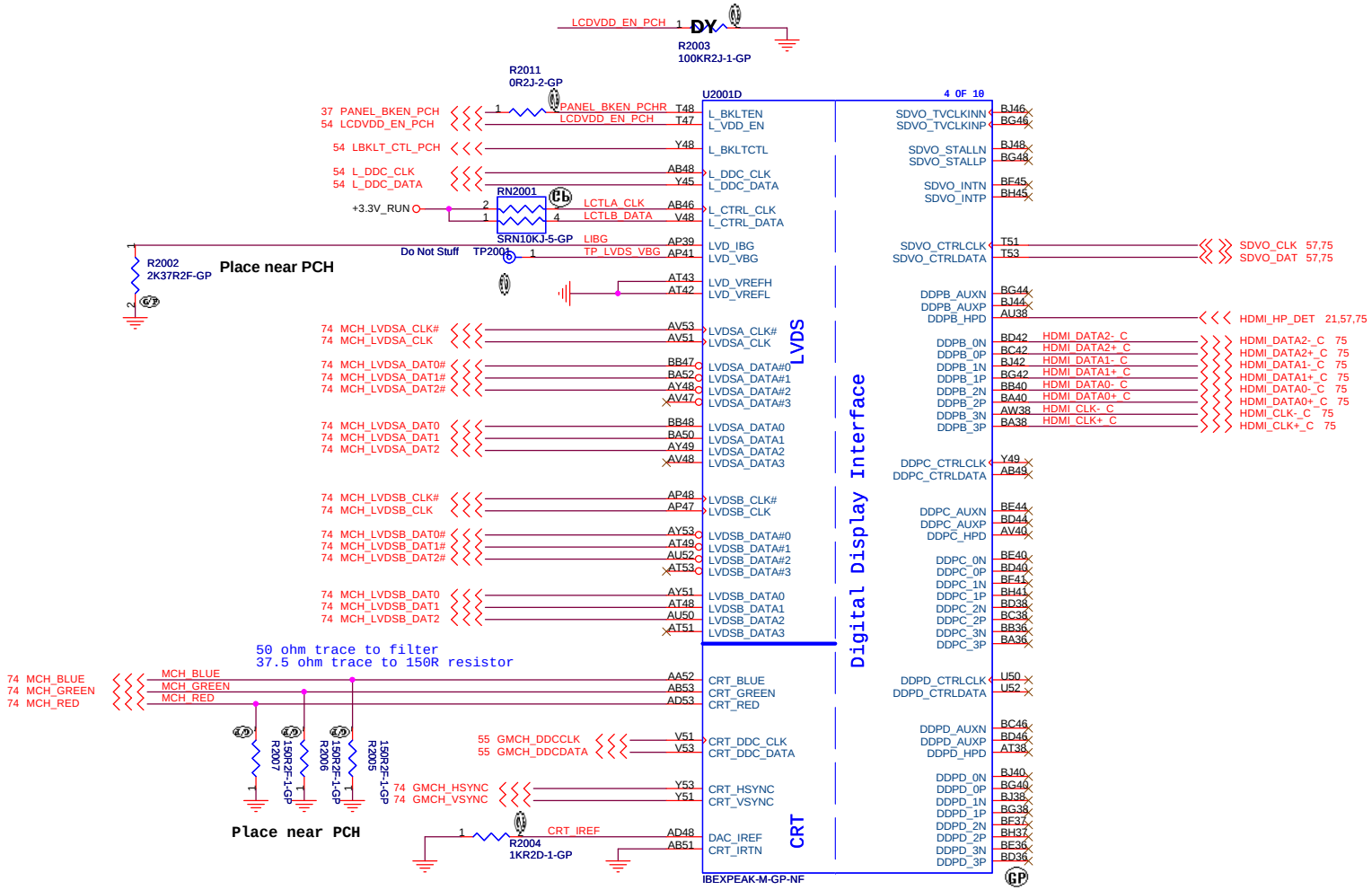


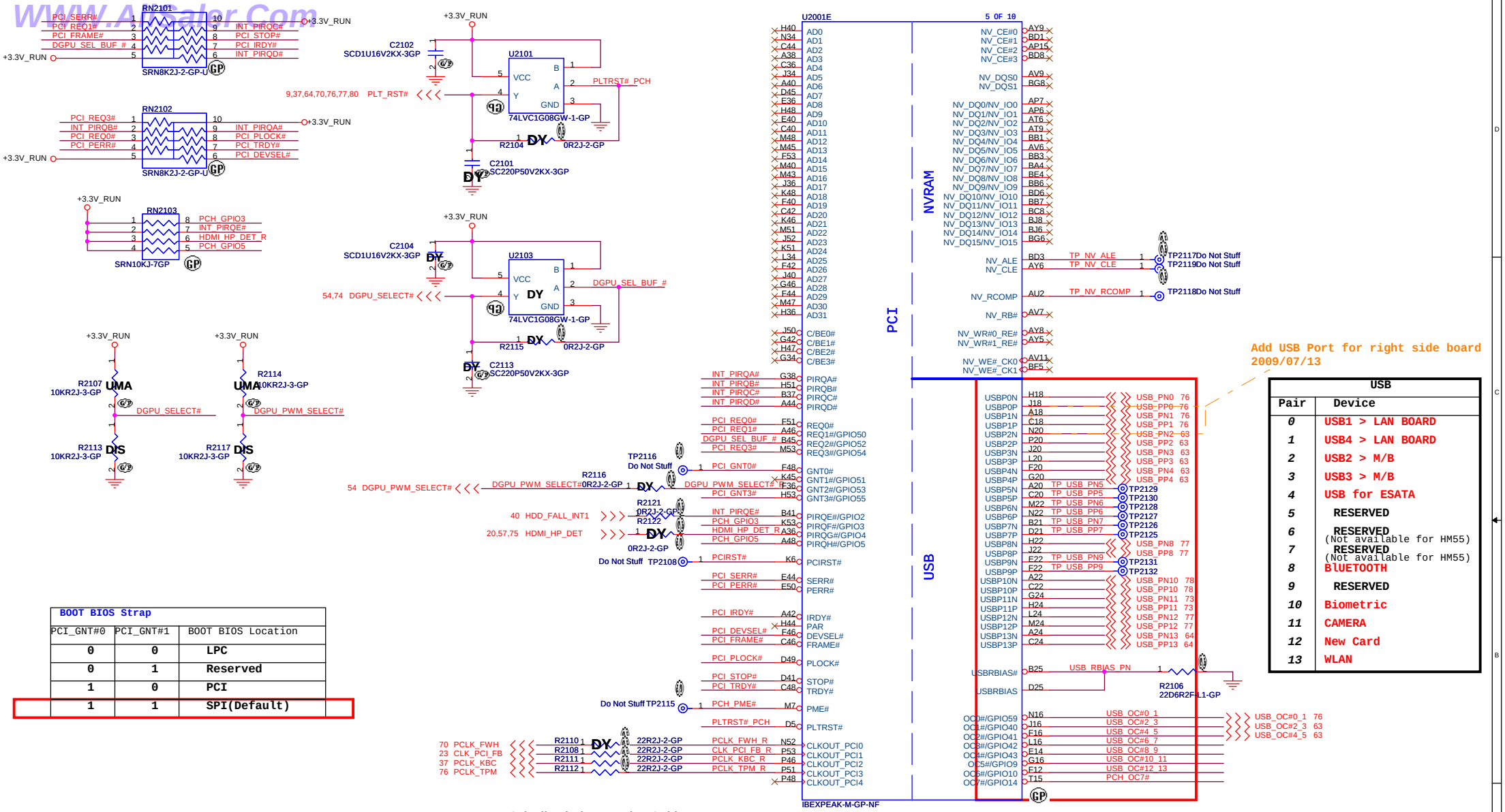
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 20 of 90

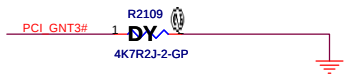


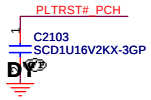
Add USB Port for right side board 2009/07/13

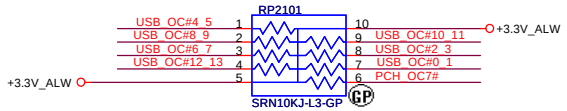
USB	
Pair	Device
0	USB1 > LAN BOARD
1	USB4 > LAN BOARD
2	USB2 > M/B
3	USB3 > M/B
4	USB for ESATA
5	RESERVED
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	RESERVED
10	Biometric
11	CAMERA
12	New Card
13	WLAN

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default







Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

UMA

Wistron Corporation
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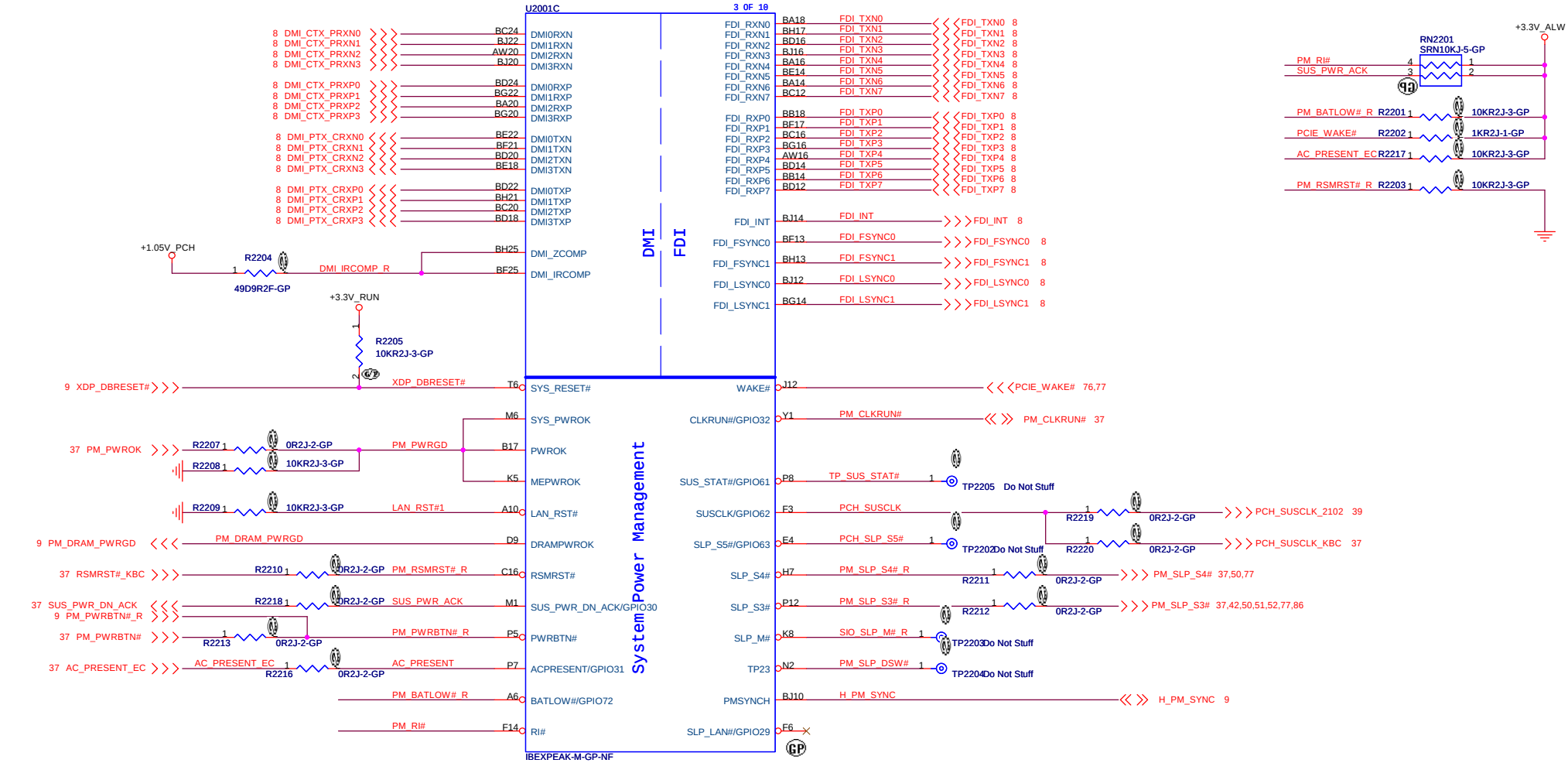
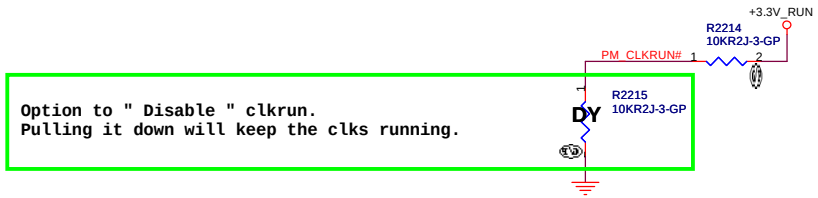
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)

Size	Document Number	Rev
	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 21 of 90





UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 22 of 90

U2001B 2 OF 10

PCI-E*
Card Reader
WLAN
LAN
New Card
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex

(Not available for HM55)

(Not available for HM55)

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

IBEXPEAK-M-GP-NF

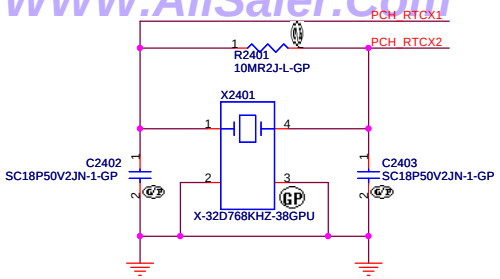
2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31

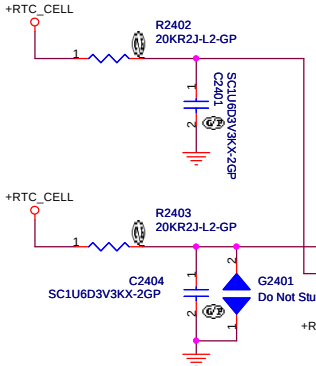
2009/08/10
Modify 25MHz crystal schematic
for Intel design guideline on PCH

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: Document Number: Vostro Calpella Rev: SA
Date: Tuesday, September 08, 2009 Sheet 23 of 90



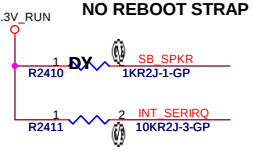


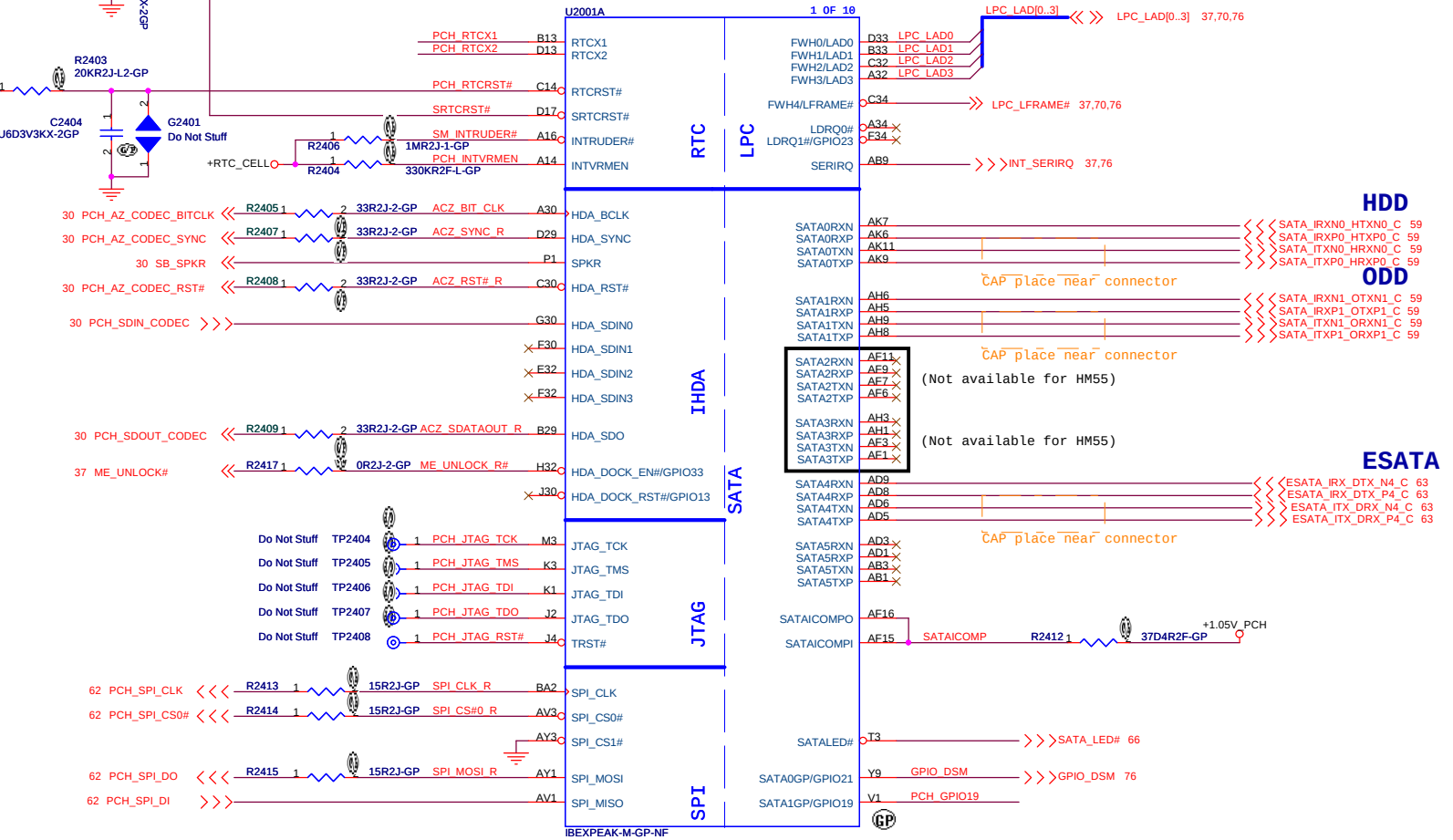
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

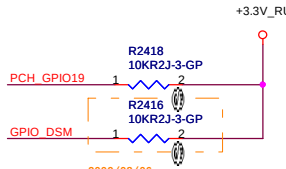
Flash Descriptor Security Override/ ME Debug Mode	
ME_UNLOCK#	This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot







2009/08/06
R2416 made STUFF ,For Lan chip connecter senser Pin.

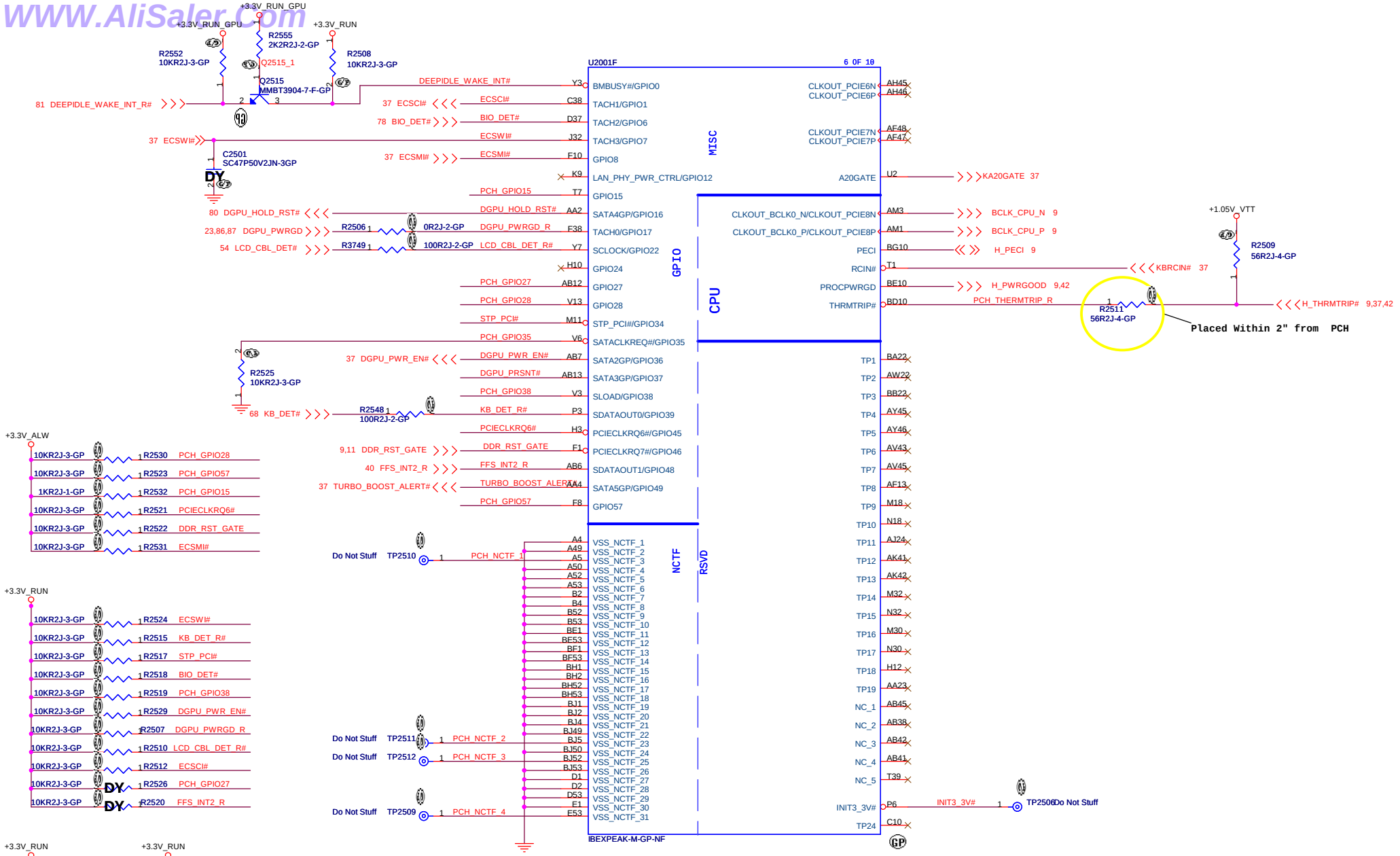
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 24 of 90



UMA

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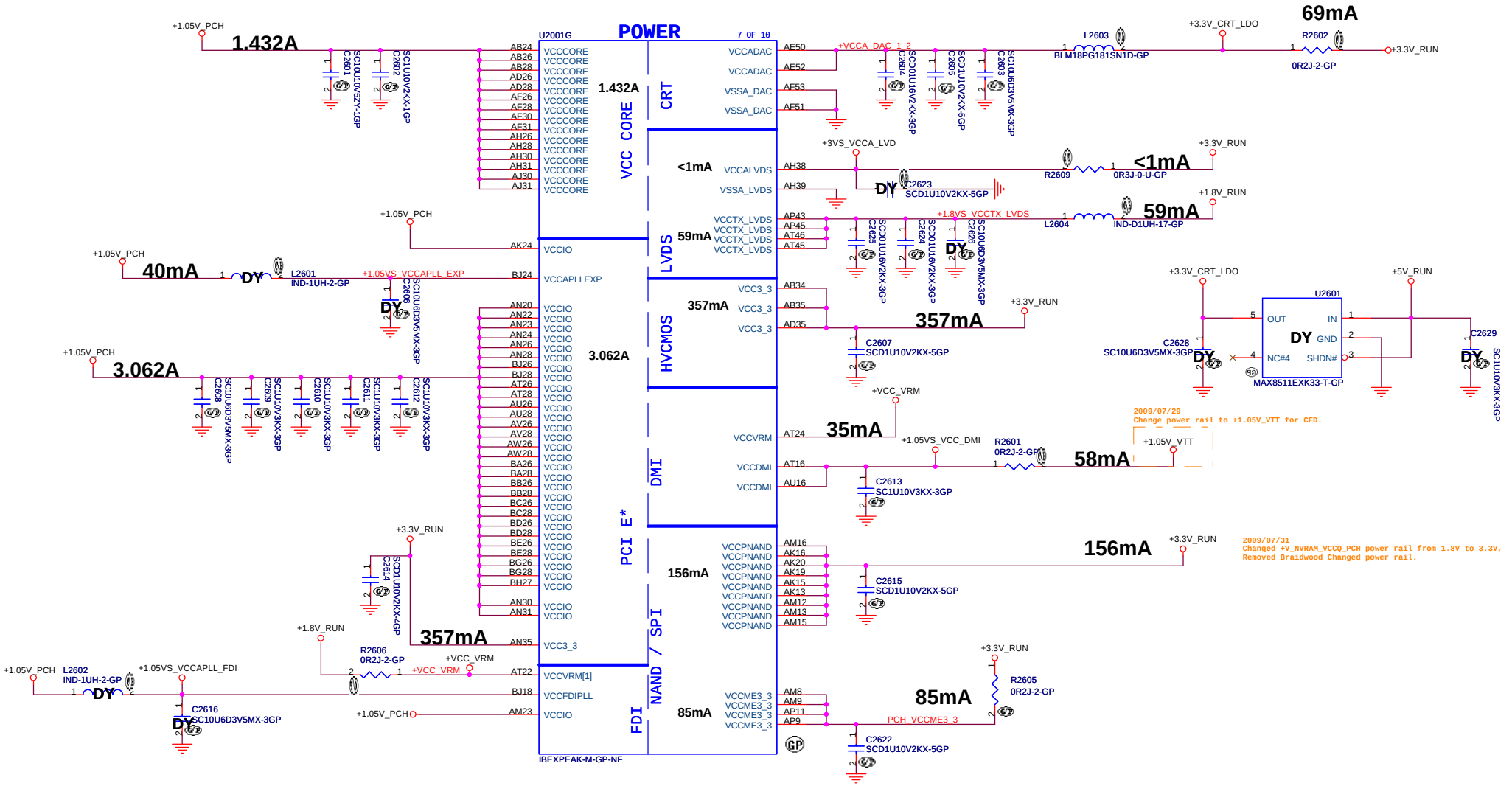
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 25 of 90



UMA

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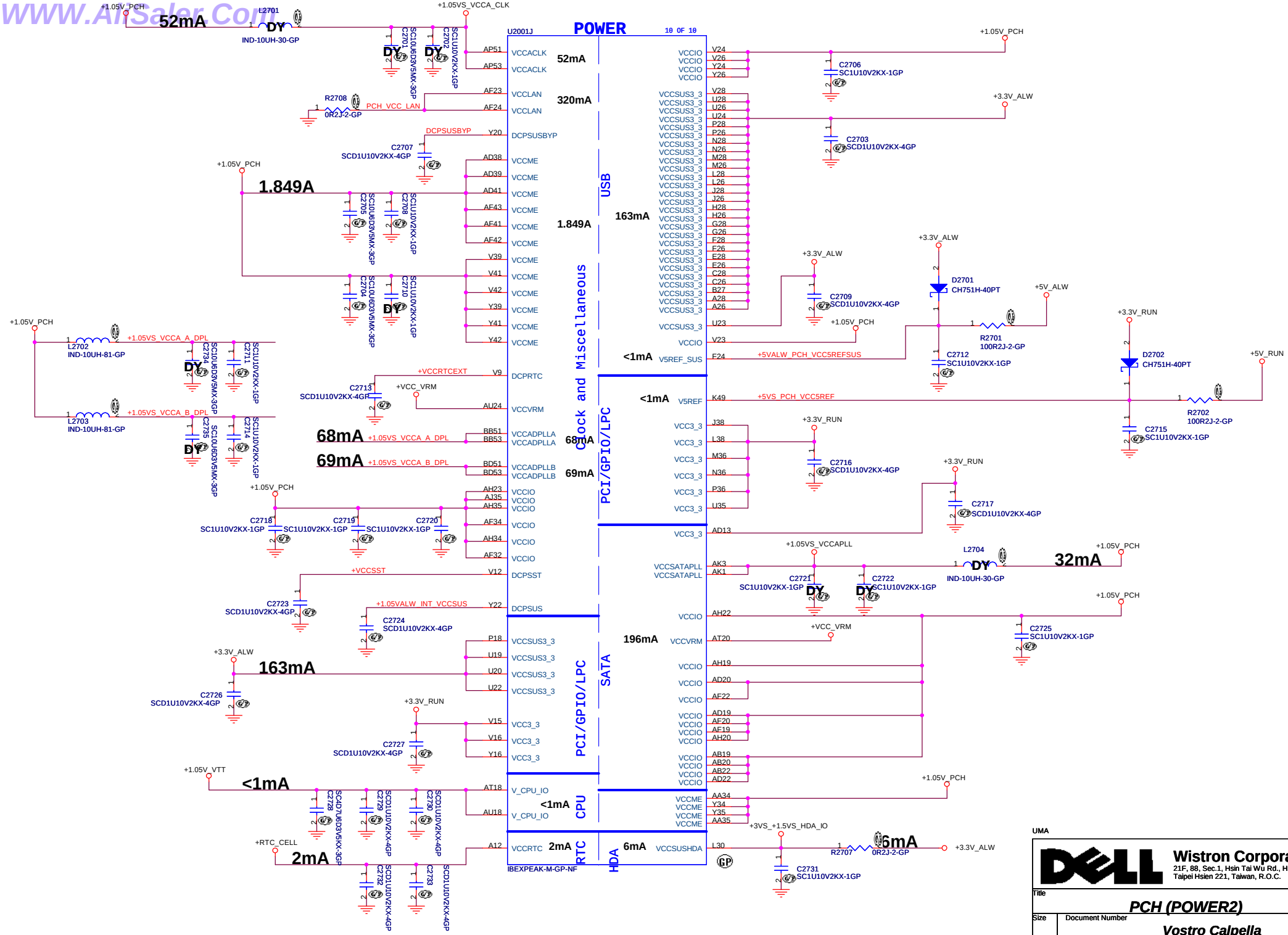
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 26 of 90



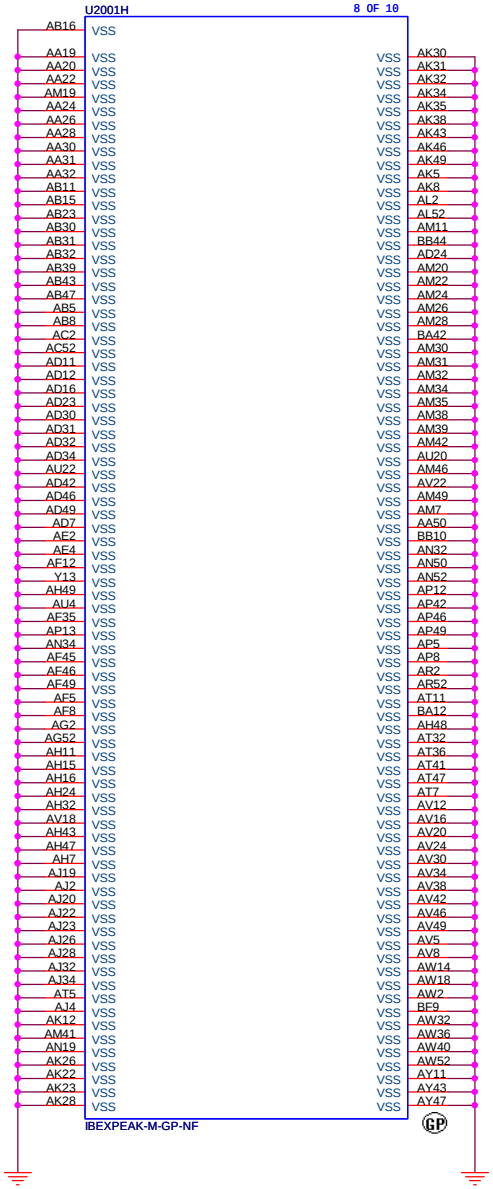
UMA

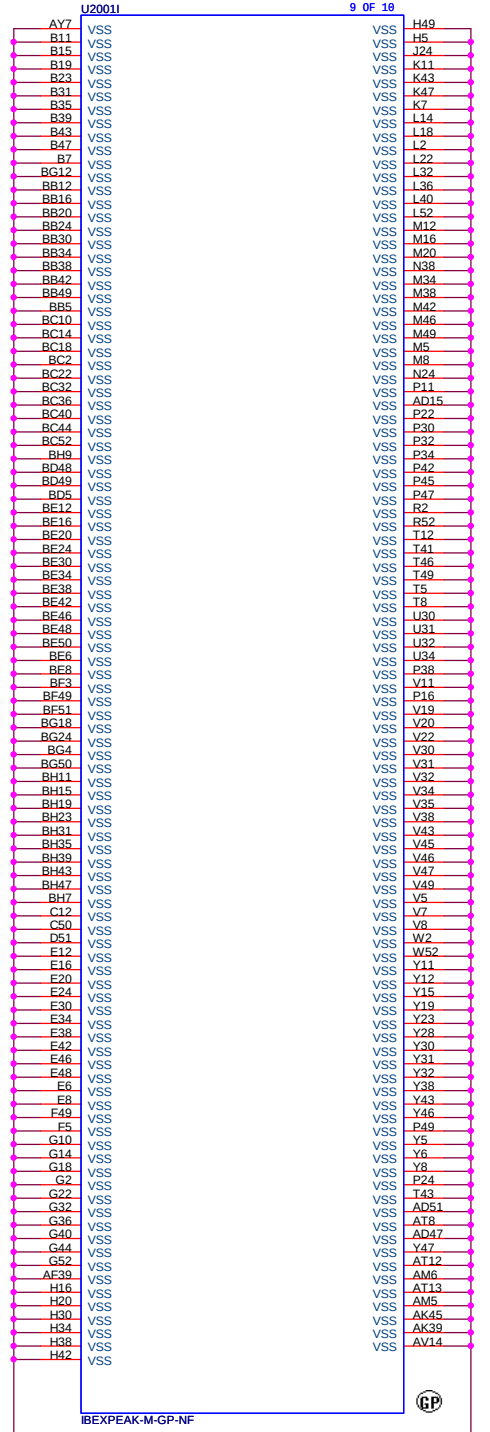
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER2)**

Size	Document Number	Rev
	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 27 of 90





UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size	Document Number	Rev
	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 28 of 90

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UMA

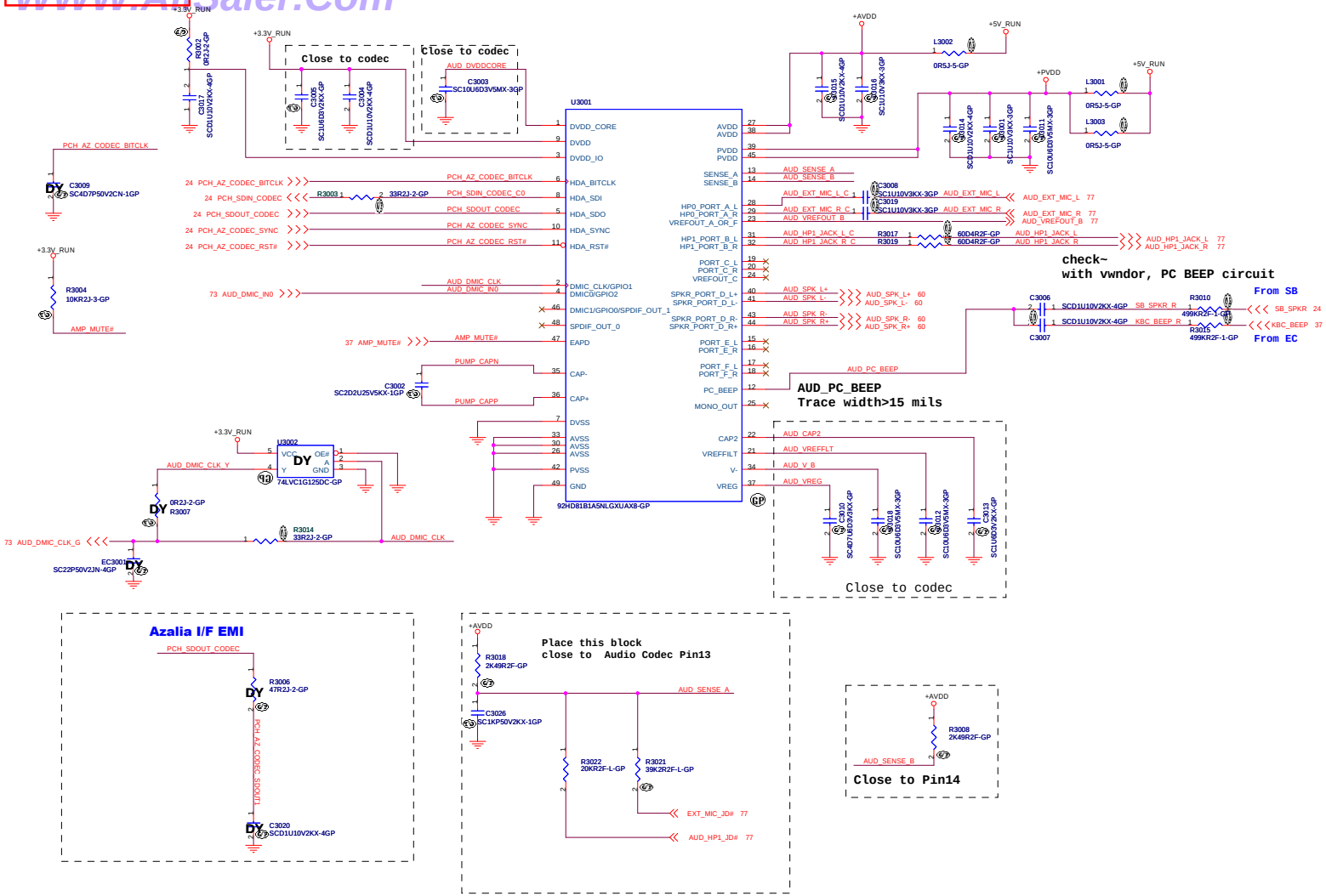
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserve)*

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 29 of 90

SSID = AUDIO



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CODEC 92HD81

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 30 of 90

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 31 of 90

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserve

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 32 of 90

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 33 of 90

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 34 of 90

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserve)

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 35 of 90

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 36 of 90

SSID = KBC

Added 10mW circuit
2009/06/04

Check~

Put 0.1uf close to VCC-GND pin pair.

Pull High : Discrete
internal Pull Low for UMA

Remove
HDD_FALL_INT1

MB VERSION		
ID	VER1	VER0
SA	0	0
SB	0	1
SC	1	0
-1	1	1

KBC CLK
EMI

2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31
2009/0806
Changed Q3714 from N-MOS to BJT Gate,For cost down.

2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31

2009/08/05
added Q3709

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 37 of 90

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 38 of 90

SSID = Thermal

1. CPU System Sensor

Q3905 must be near CPU
C3912 must be near Q3905
C3914 must be near EMC2102

Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. GPU Sensor (DIS)

C3906 must be near EMC2102

Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

C3901 must be near Q3901
C3913 must be near Q3904
C3903 must be near EMC2102

3.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

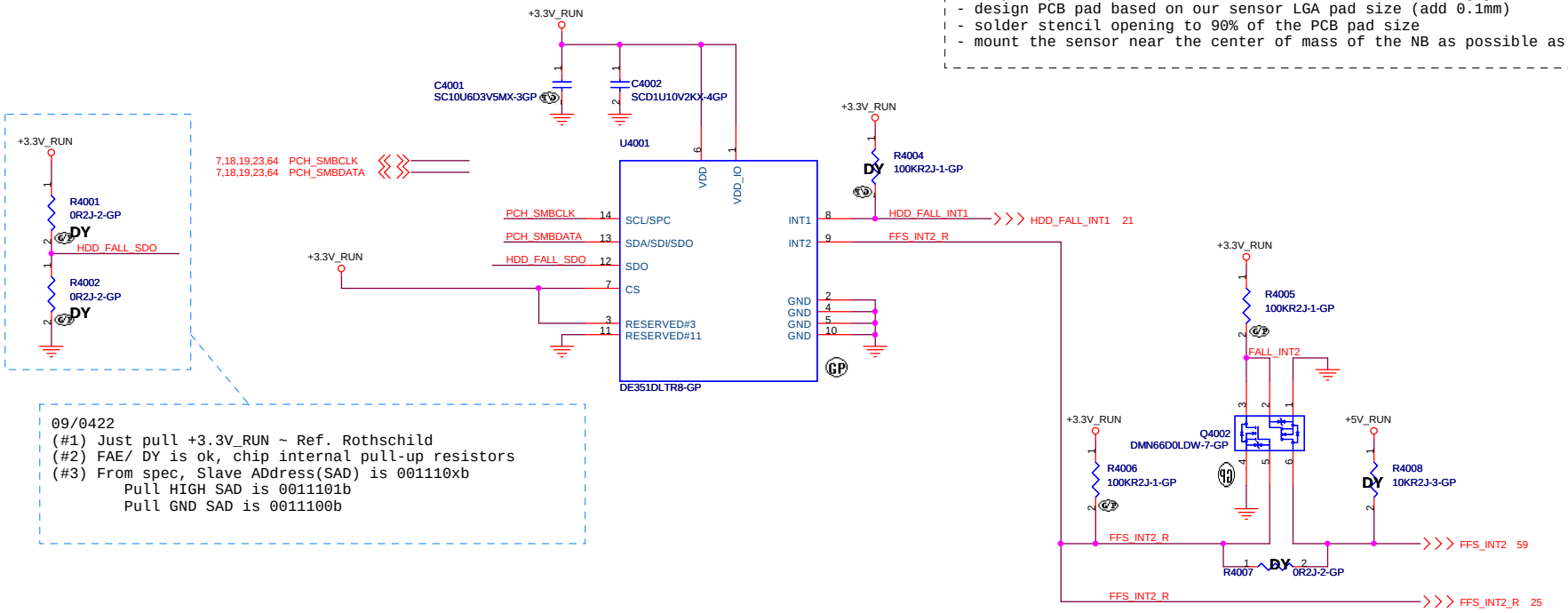
TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 88 deg-C.

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thermal/Fan Controllor EMC2102
Size	Custom
Document Number	Vostro Calpella
Rev	SA
Date:	Tuesday, September 08, 2009
Sheet	39 of 90

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Free Fall Sensor

Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 40 of 90

(Blank)

UMA

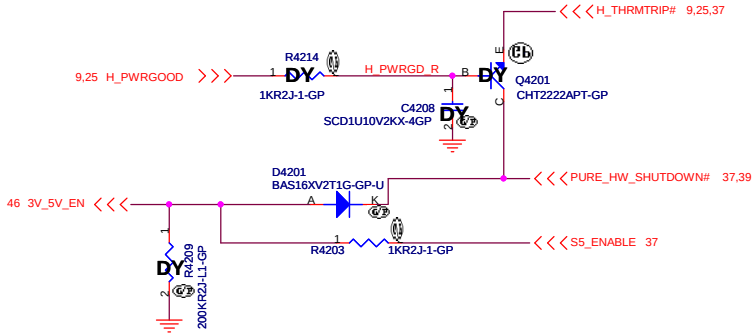
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserve)

Size: Custom | Document Number: Vostro Calpella | Rev: SA

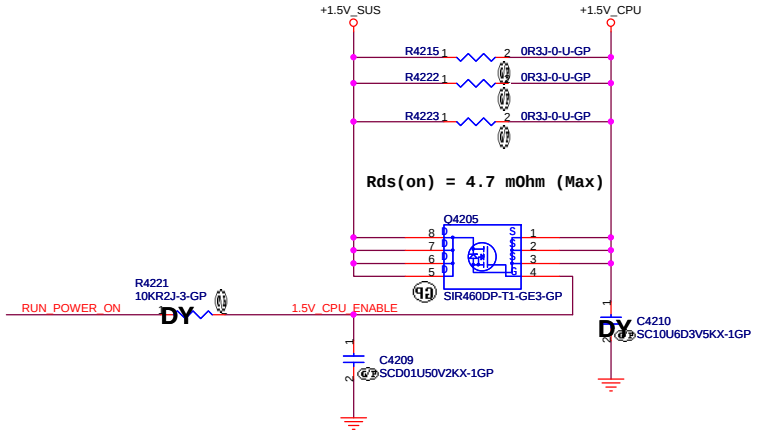
Date: Tuesday, September 08, 2009 | Sheet 41 of 90

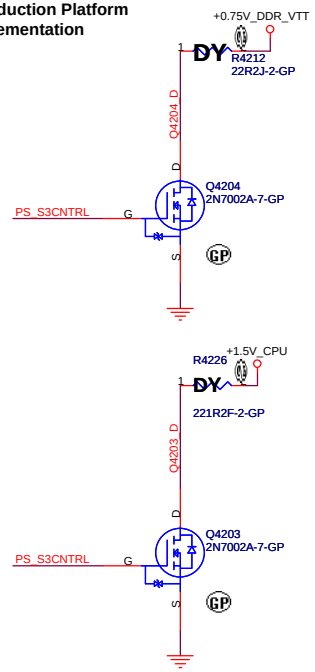
SSID = Reset.Suspend

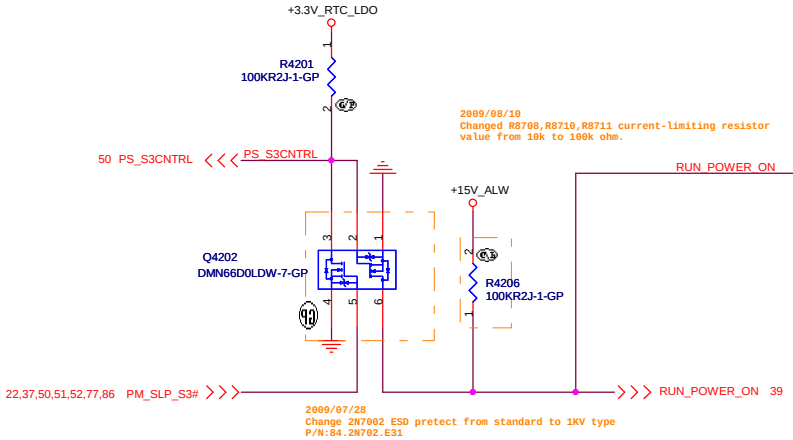


+1.5V_CPU:

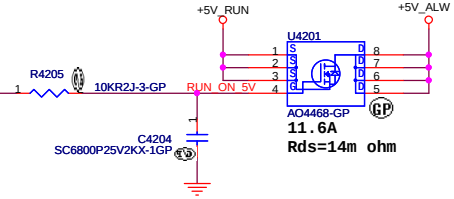
Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details



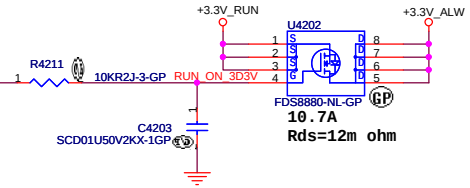




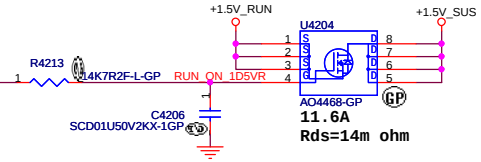
Design current: 4246.6mA



Design current: 6480.6mA



Design current: 2783.6mA



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

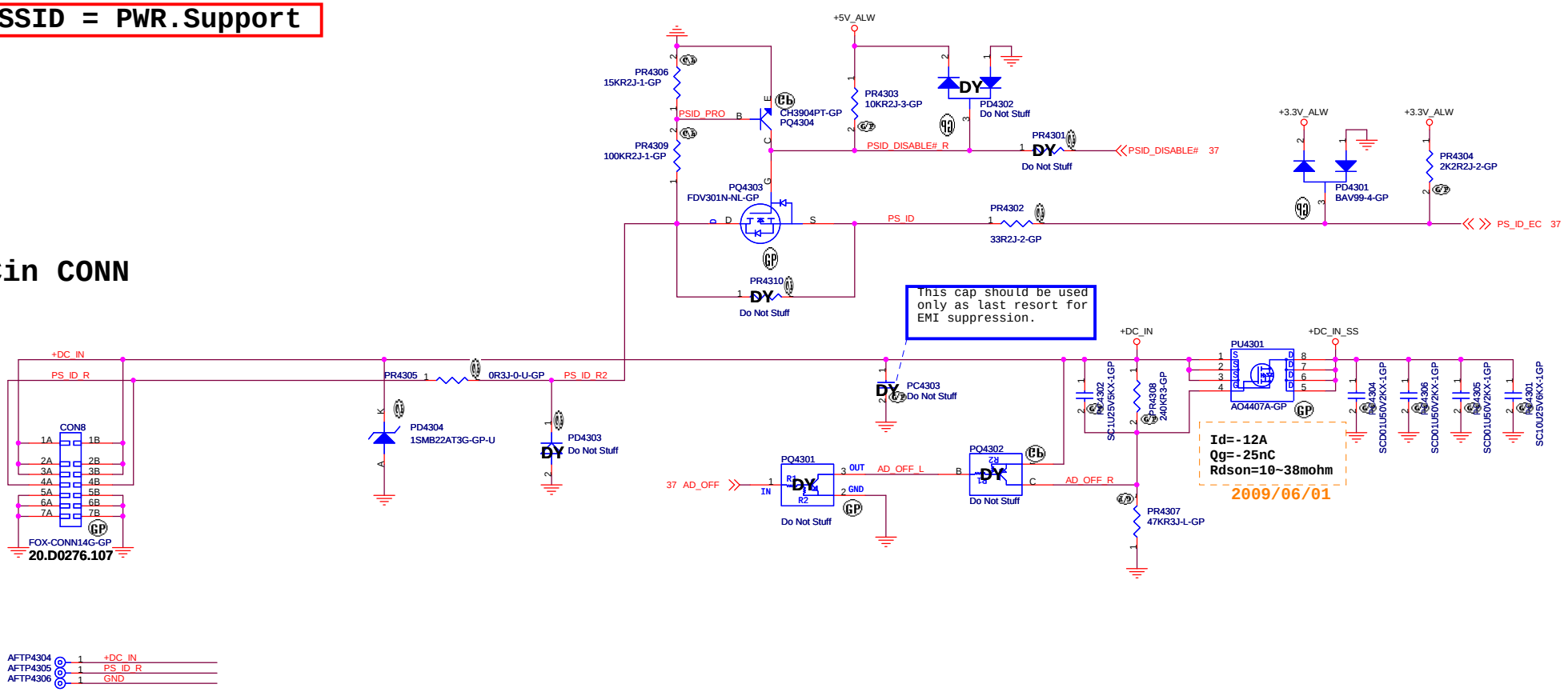
Title: **Power Plane Enable**

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 42 of 90

SSID = PWR.Support

DCin CONN

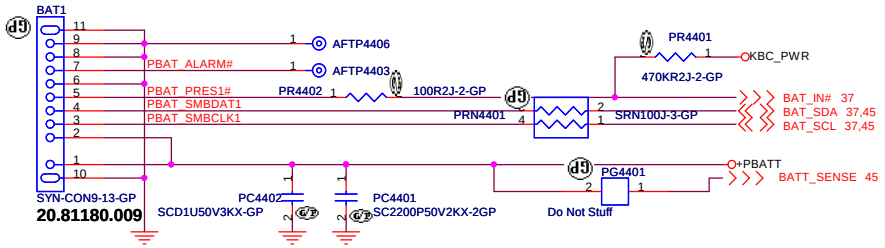


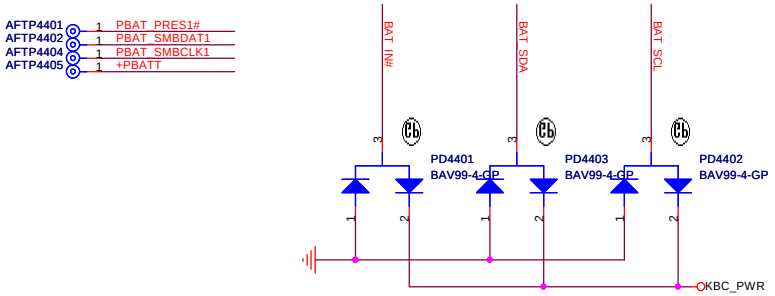
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
DC IN		
Size: Custom	Document Number: Vostro Montevina Discrete	Rev: SA
Date: Tuesday, September 08, 2009	Sheet 43 of 90	

Batt Connecter





UMA

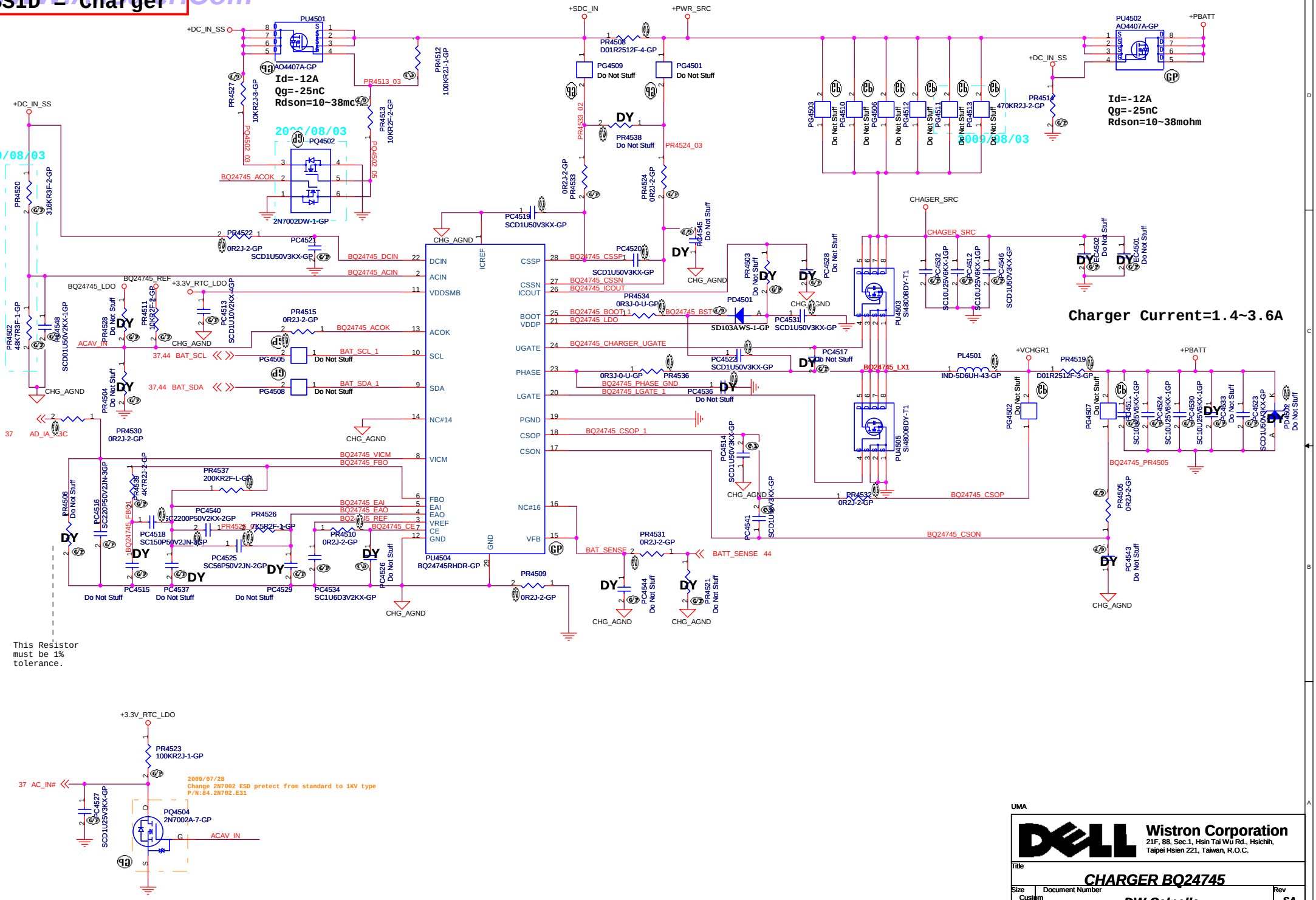
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	Vostro Montevina Discrete	SA

Date: Tuesday, September 08, 2009 Sheet 44 of 90

SSID = Charger



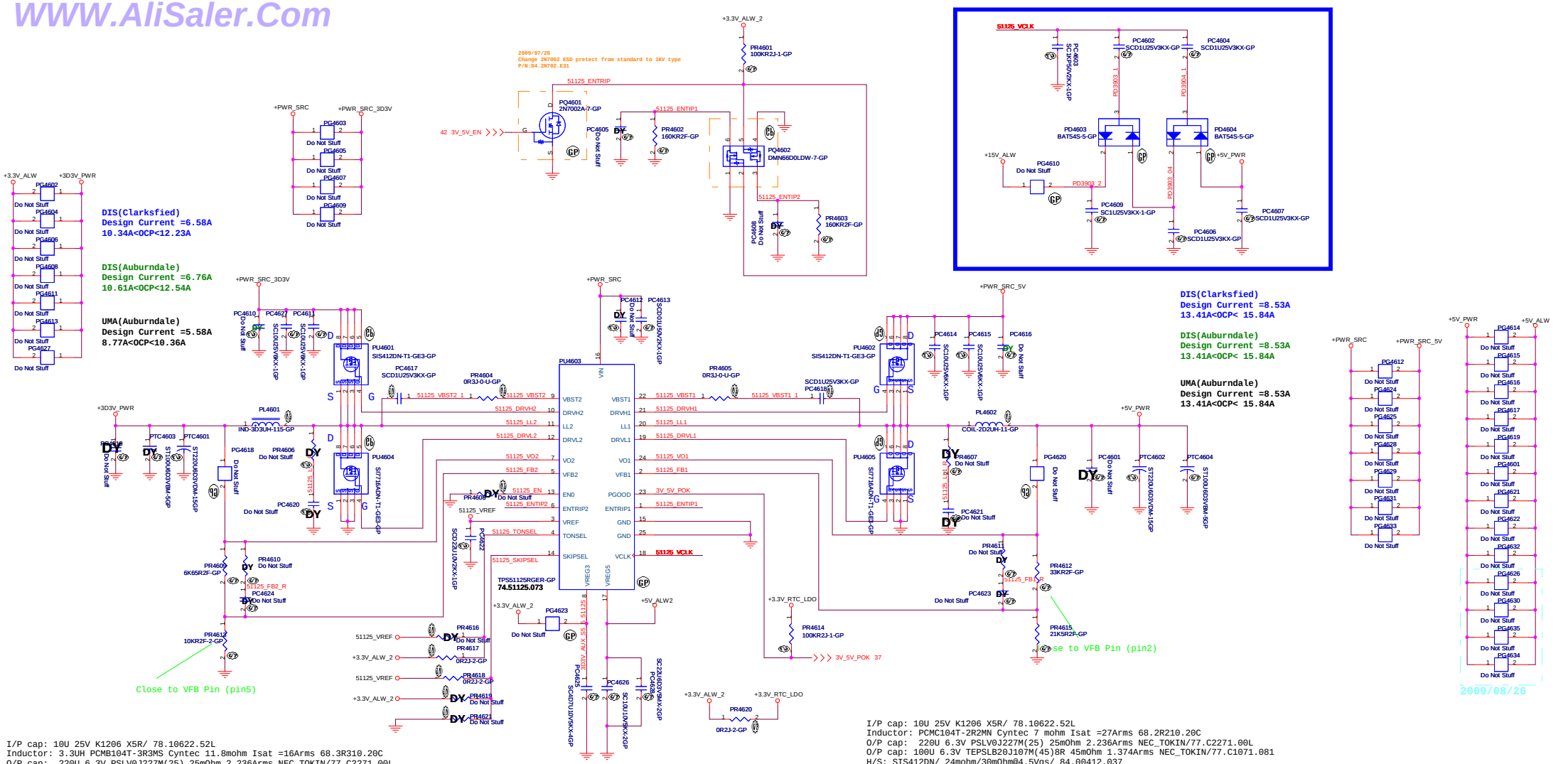
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: DW Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 45 of 90



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: PCMC104T-2R2MN Cyntec 7 mohm Isat =27Arms 68.2R210.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51125_5V/3D3V

Size	Document Number	Rev
Custom	DW Calpella	X00

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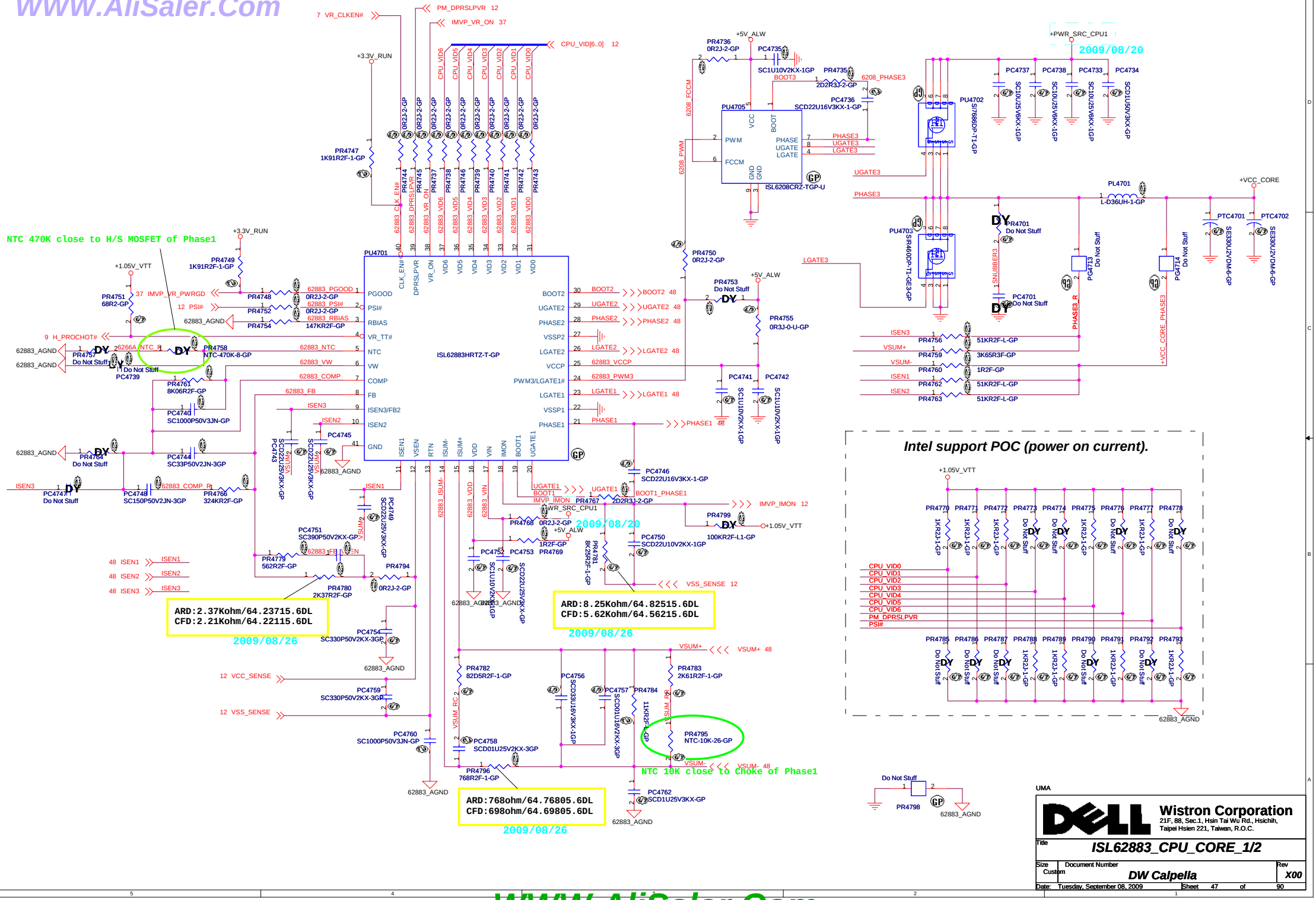
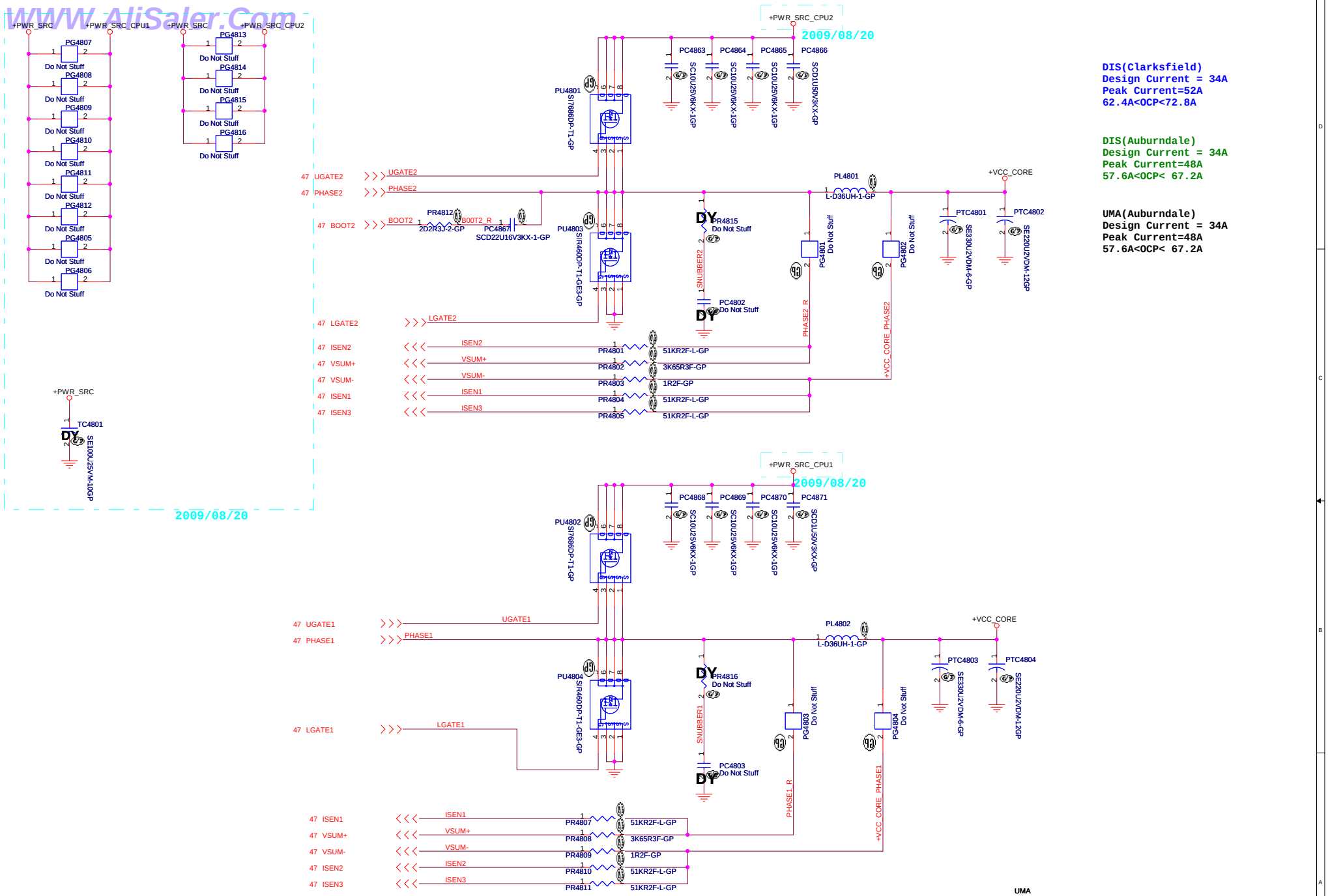




DIS(Clarksfield)
Design Current = 34A
Peak Current=52A
62.4A<OCP<72.8A

DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

UMA(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Freq=300KHz@PER PHASE

UMA

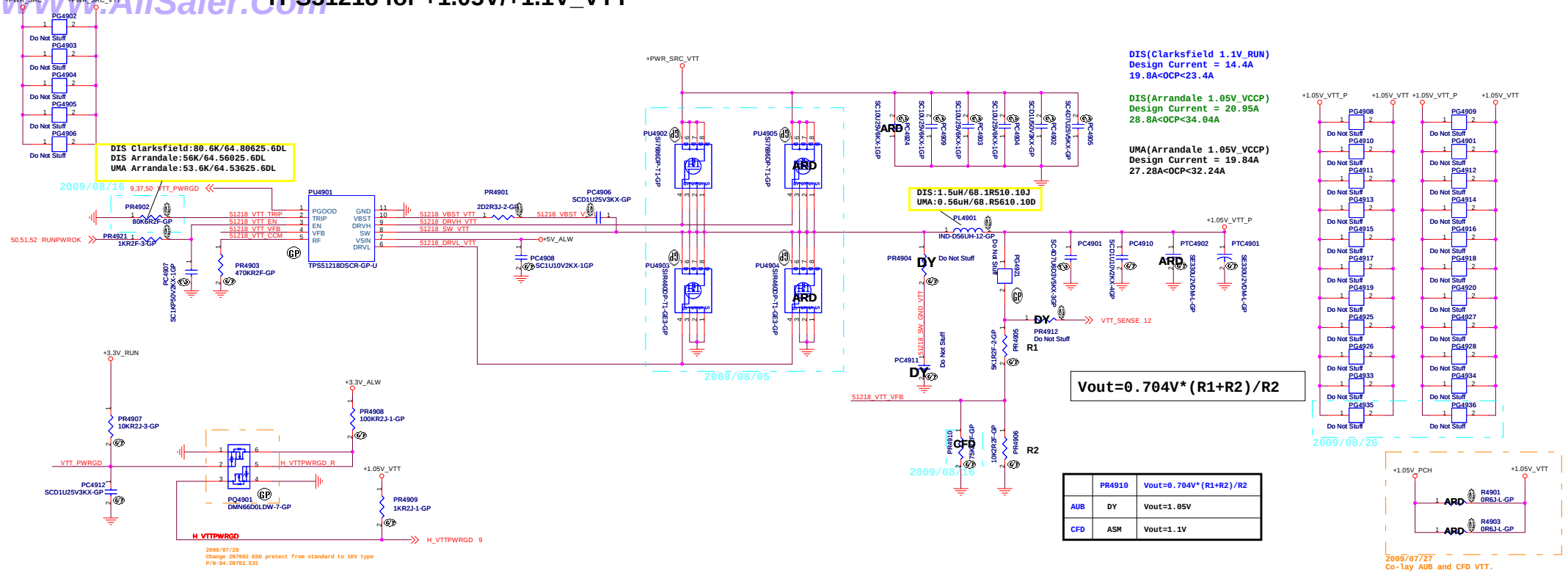
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE_2/2

Size: Custom | Document Number: DW Calpella | Rev: X00

Date: Tuesday, September 08, 2009 | Sheet 48 of 90

TPS51218 for +1.05V/+1.1V_VTT



	PR4910	Vout=0.704V*(R1+R2)/R2
AUB	DY	Vout=1.05V
CFD	ASM	Vout=1.1V

Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
Inductor: 1.5uH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat=33Arms 68.1R510.10J
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
Custom	DJ1 Discrete	X00

Date: Tuesday, September 08, 2009 Sheet 49 of 90

SSID = PWR.Plane.Regulator_1p5v0p75v

DIS Clarksfield:11.5K/64.11525.6DL
DIS Arrandale:9.76K/64.97615.6DL
UMA Arrandale:6.65K/64.66515.6DL

2009/08/16

2009/07/09
follow vostro 15 inch schematic

2009/07/29
Reserved R,C By PM_SLP_S4# ,for time delay

2009/08/05

TPS51116RGER-GP-U

Design Current = 0.7A

DIS(Clarksfied)
Design Current = 14.52A
22.82A<OCP<26.97A

DIS(Auburndale)
Design Current = 12.42A
19.52A<OCP<23.07A

UMA(Auburndale)
Design Current = 8.51A
13.37A<OCP<15.8A

DIS:1.0uH/68.1R01A.20A
UMA:1.5uH/68.1R510.10J

DIS:EEFSX0D331ER/79.33719.L01
UMA:EEFCX0D221R/79.22719.20L

Close to VFB Pin (pin5)

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.0uH PCMC104T-1R0MN Cyntec DCR:3.5mohm Isat=40Arms 68.1R01A.20A
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

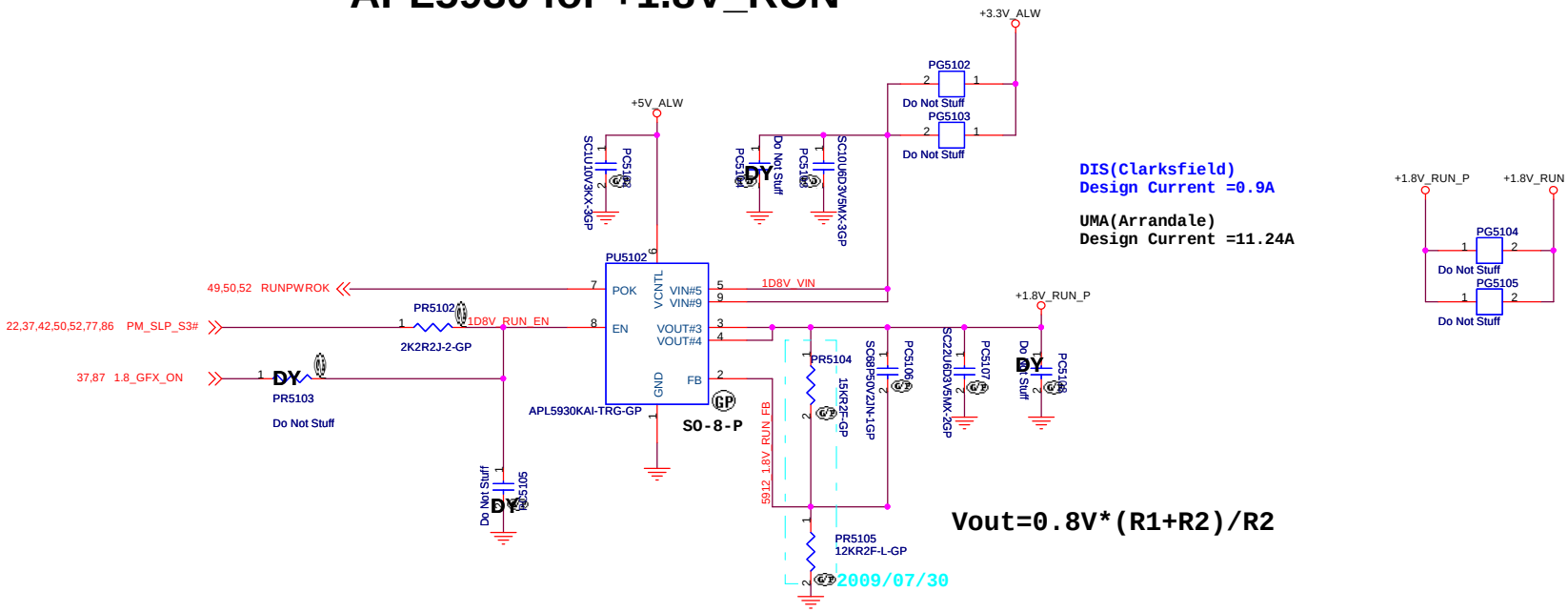
Title: TPS51116_+1.5V_SUS

Size	Document Number	Rev
Custom	DW Calpella	X00

Date: Tuesday, September 08, 2009 Sheet 50 of 90

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



DIS(Clarksfield)
Design Current =0.9A

UMA(Arrandale)
Design Current =11.24A

Vout=0.8V*(R1+R2)/R2

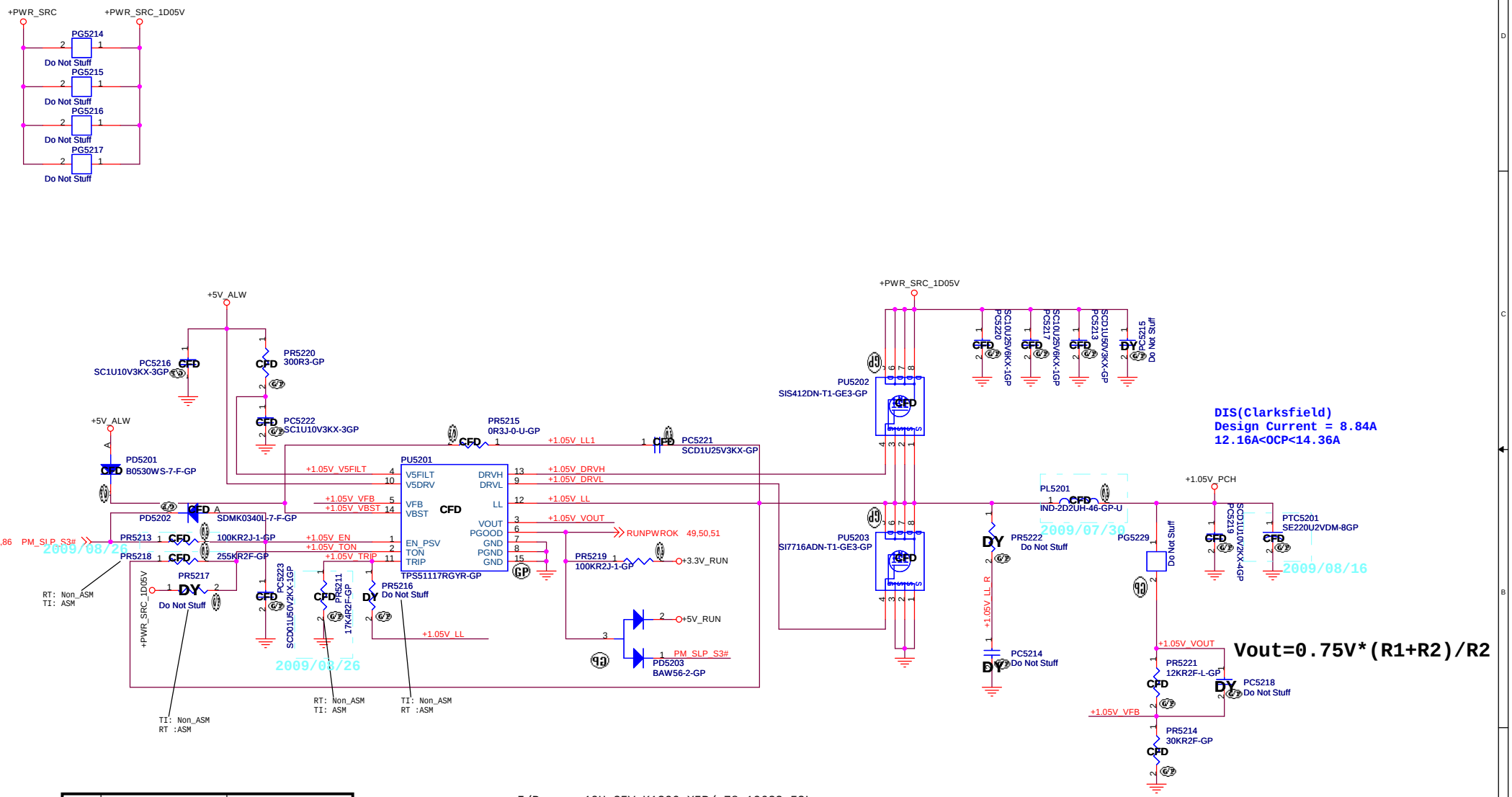
2009/07/30

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930 +1.8V RUN	
Size: A3	Document Number: DW Calpella	Rev: X00
Date: Tuesday, September 08, 2009	Sheet 51 of 90	

SSID = PWR.Plane.Regulator_1p05v



	ASM	Non_ASM
TI	PR5218, PR5211	PR5217, PR5216
RT	PR5217, PR5216	PR5218, PR5211

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor:2.2UH PCMC063T-2R2MN Cyntec DCR:20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 2V EEFCX0D221R 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SIS412DN/ 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN/ 13.5mOhm/16.5mohm@4.5Vgs/ 84.07716.037
Switching freq-->320KHz

UMA

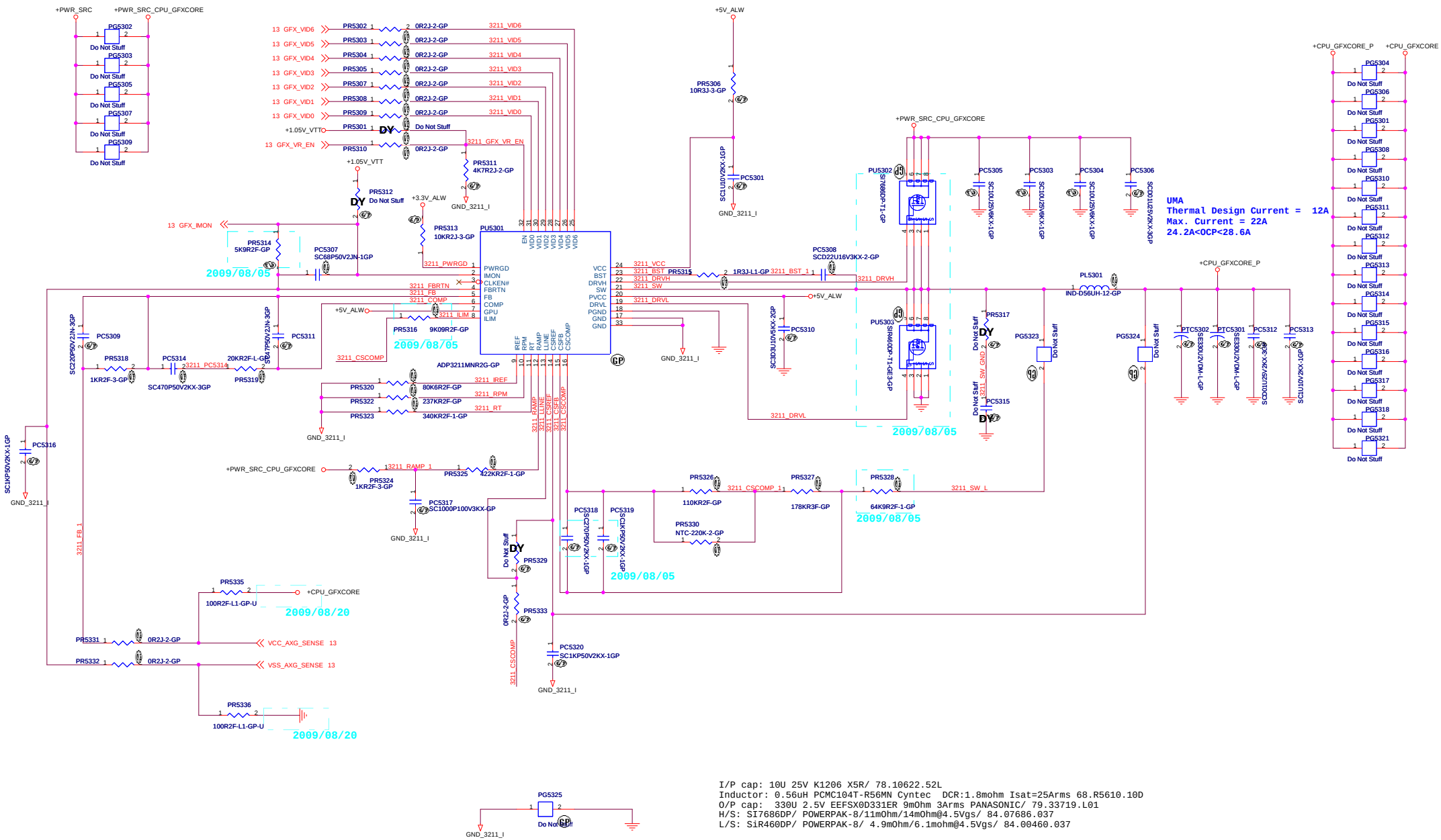
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.05V

Size	Document Number	Rev
A3	DW Calpella (Clarksfield)	SA

Date: Tuesday, September 08, 2009 Sheet 52 of 90

SSID = CPU.GFX.Regulator



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3211 CPU_GFXCORE

Size	Document Number	Rev
Custom	DW Calpella UMA	X00

Date: Tuesday, September 08, 2009 Sheet 53 of 90

SSID = VIDEO

Close PCH

+3.3V_RUN

RN5404 SRN2K2J-1-GP

20 L_DDC_DATA
20 L_DDC_CLK

Close GPU

+3.3V_RUN_GPU

RN5409 SRN2K2J-1-GP DIS

81 LDDC_DATA
81 LDDC_CLK

UMA/DIS LVDS DDC CLK/DAT select circuit

R5409 1 UMA 0R2J-2-GP

U5444

81 LDDC_DATA
20 L_DDC_DATA

B0 A
GND VCC
B1 S
DIS

LDDC_DATA_CON
EDID_SELECT#

NC7SB3157P6X-1GP
73.03157.C0H

+3.3V_RUN

C5407 SCD1U10V2KX-4GP DIS

23,55,57 EDID_SELECT# EDID_SELECT#

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

R5411 1 UMA 0R2J-2-GP

U5445

81 LDDC_CLK
20 L_DDC_CLK

LDDC_CLK_CON
EDID_SELECT#

NC7SB3157P6X-1GP
73.03157.C0H

+3.3V_RUN

LDDC_DATA_CON
LDDC_CLK_CON

DY DY

EV @ LVDS side

C5414 SC22P50V2JN-4GP
C5415 SC22P50V2JN-4GP

C5408 SCD1U10V2KX-4GP DIS

LVDS CONNECTOR

LCD1

+PWR_SRC_GFX
+LCDVDD

C5402 SCD1U10V2KX-4GP

+3.3V_RUN

R5410 10KR2J-3-GP DY

R5404 33R2J-2-GP

+3.3V_EEPROM
LCD_BRIGHTNESS

BLON_OUT_R R5406 100R2J-2-GP

LCD_TST
LDDC_CLK_CON
LDDC_DATA_CON
LCD_DET_G

R5408 100R2J-2-GP

VGA_TXBOUT0-
VGA_TXBOUT0+
VGA_TXBOUT1-
VGA_TXBOUT1+
VGA_TXBOUT2-
VGA_TXBOUT2+
VGA_TXBCLK-
VGA_TXBCLK+
VGA_TXAOUT0-
VGA_TXAOUT0+
VGA_TXAOUT1-
VGA_TXAOUT1+
VGA_TXAOUT2-
VGA_TXAOUT2+
VGA_TXACLK-
VGA_TXACLK+
LCD_CBL_DET#

IPEX-CONN40-2R-GP
20.F1093.040

UMA/DIS LVDS PWM select circuit

2009/07/27
Added LCD brightness control by EC.
2009/07/29
Removed LCD brightness control,Combine EC and GPU

37 LBKLT_CTL_EC
81 LBKLT_CTL_GPU
20 LBKLT_CTL_PCH

R5438 1 DY 0R2J-2-GP LCD_BRESS
R5439 1 DIS 0R2J-2-GP

U5448

B0 A
GND VCC
B1 S
DIS

LCD_BRIGHTNESS

NC7SB3157P6X-1GP
73.03157.C0H

+3.3V_RUN

C5409 SCD1U10V2KX-4GP DIS

DGPU_PWM_SELECT# 21

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

LBKLT_CTL_EC R5412 1 UMA 0R2J-2-GP
LBKLT_CTL_PCH R5413 1 UMA 0R2J-2-GP
LCD_BRIGHTNESS

LCD_BRIGHTNESS
LCD_TST

C5402 SC33P50V2JN-3GP DY
C5401 SC33P50V2JN-3GP DY

For EMI request

BLON_OUT_R

R5407 10KR2J-3-GP

SSID = Inverter

INVERTER POWER

+PWR_SRC_GFX
+PWR_SRC

F5401 POLYSW-1D1A24V-1-GP

C5401 SC1KP50V2KX-1GP
C5405 SCD1U50V3KX-GP

SSID = VIDEO

LCD POWER

+LCDVDD

C5403 SC10U6D3V5KX-1GP
C5406 SCD1U10V2KX-4GP

+3.3V_RUN

Q5401 SI3456BDV-T1-GP

+15V_ALW
R5402 330KR2J-L1-GP FPVCC_CTL1
C5404 SCD1U50V3KX-GP
R5403 DY Do Not Stuff

R5401 120R3J-2-GP

Q5402 DMN66D0LDW-7-GP

LCDVDD_1

2009/07/28
Change 2N7002 ESD pretect from standard to 1KV type
P/N:84.2N702.E31

+3.3V_ALW
R5405 47KR2J-2-GP

37 SHBM_LCDTST_EN
LVDVDD_EN
ENVDD_D
FPVCC_CTL3

D5402 BAT54C-7-F-GP

Q5403 DDTC144EUA-7-GP

R5414 1 UMA 0R2J-2-GP

U5446

81 LCDVDD_EN_GPU
20 LCDVDD_EN_PCH

B0 A
GND VCC
B1 S
DIS

LVDVDD_EN
DGPU_SELECT#

NC7SB3157P6X-1GP
73.03157.C0H

+3.3V_RUN

C5410 SCD1U10V2KX-4GP DIS

DGPU_SELECT# 21,74

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size: Custom | Document Number: Vostro Calpella | Rev: SA

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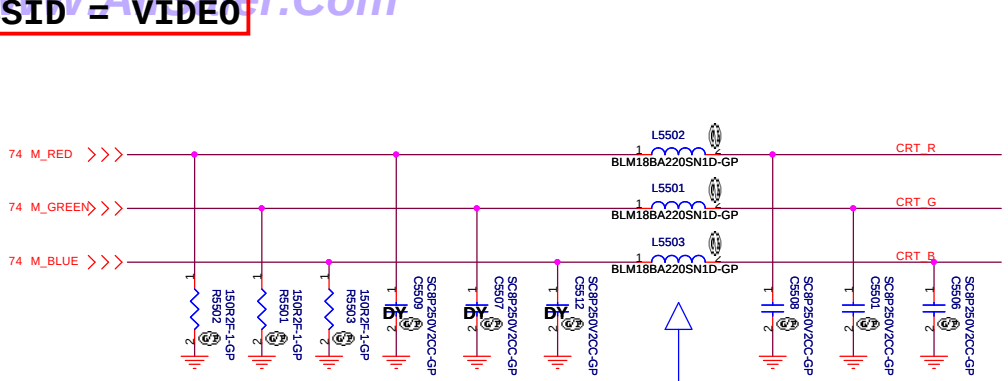
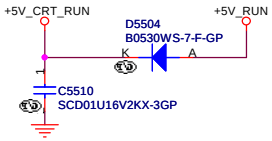
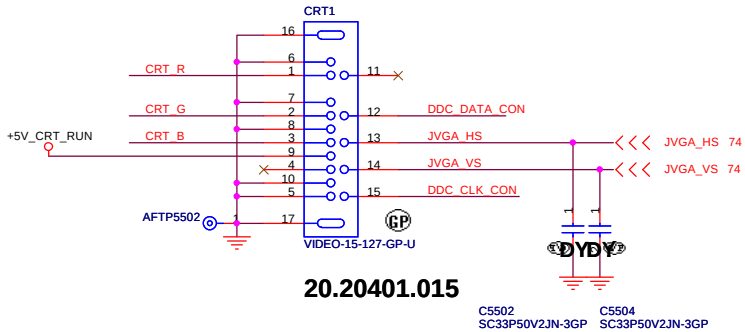
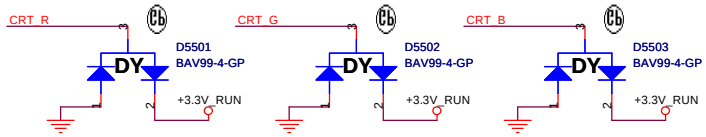
SSID = VIDEO





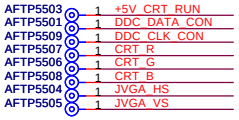


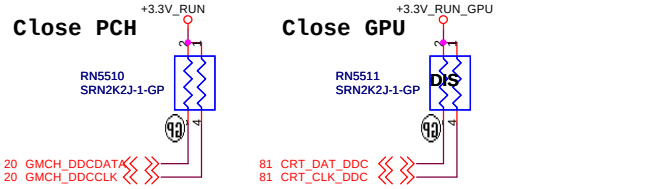
20.20401.015



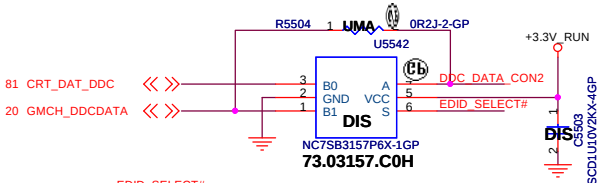
Layout Note:

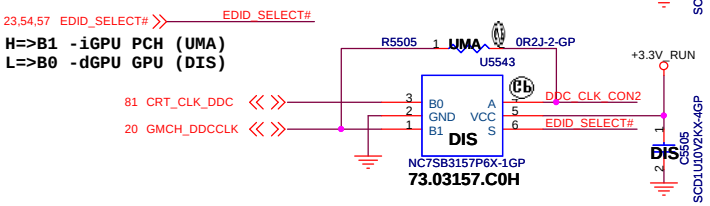
*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

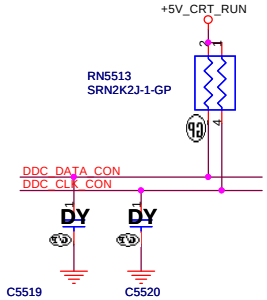


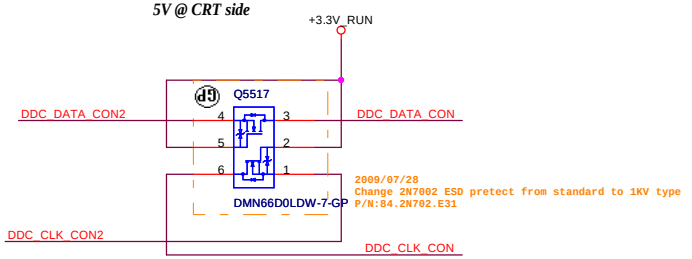


UMA/DIS CRT DDC CLK/DAT select circuit









UMA

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Title	***CRT Connector***	
Size A3	Document Number ***Vostro Calpella***	Rev ***SA***
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Title: *(Reserve)*

Size	Document Number	Rev
Custom	*Vostro Calpella*	*SA*

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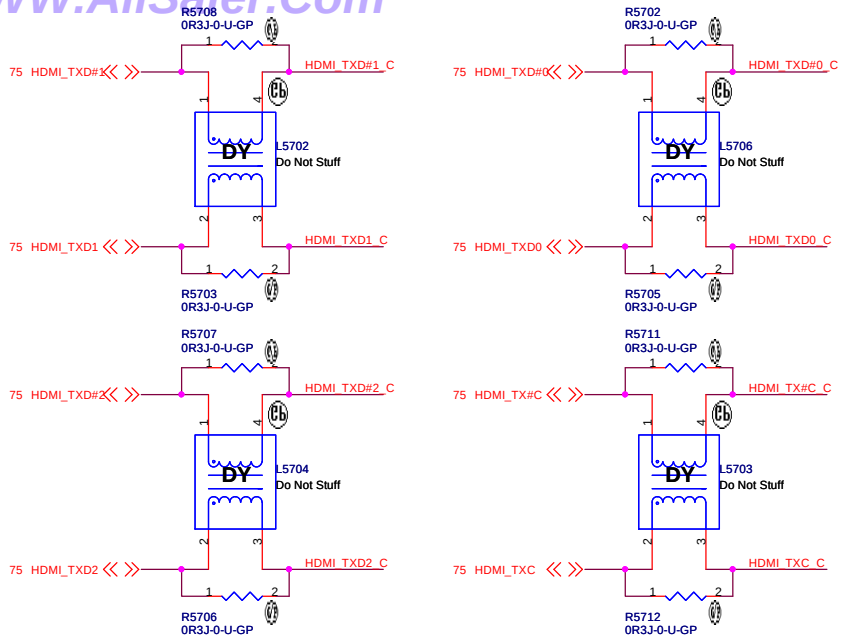
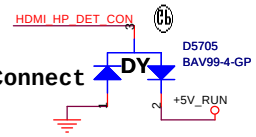
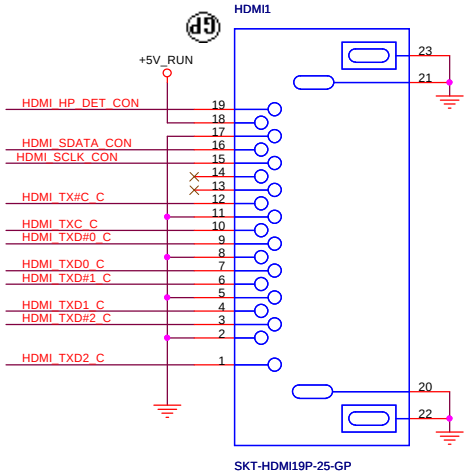
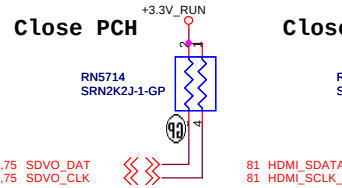




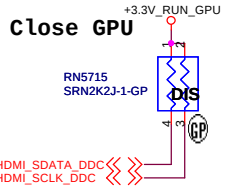
Close HDMI Connect



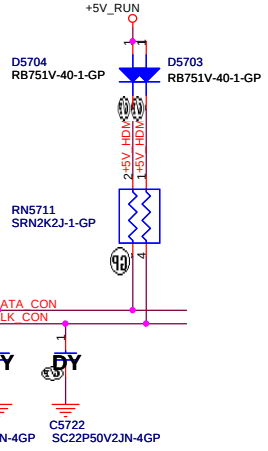
22.10296.061



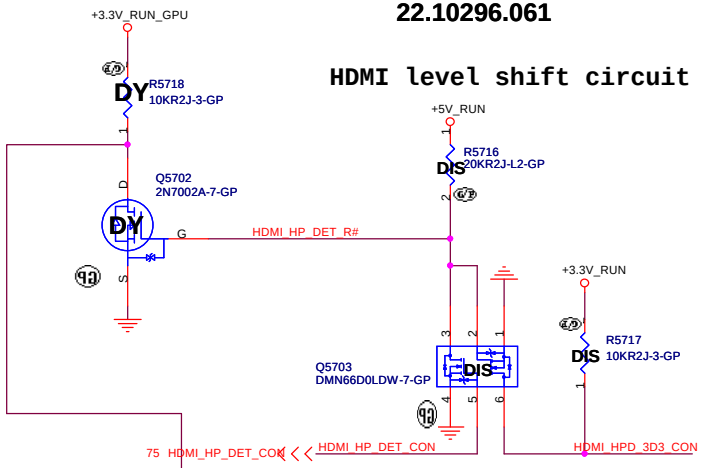
Close PCH



Close GPU

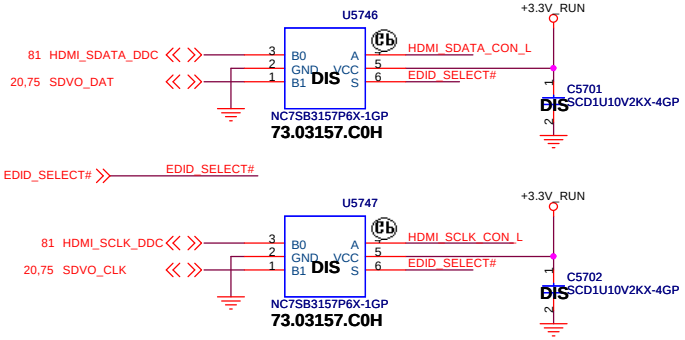


5V @ HDMI side

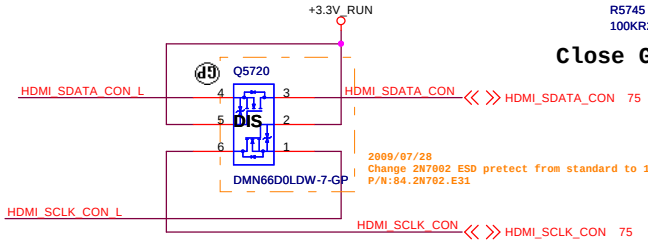


HDMI level shift circuit

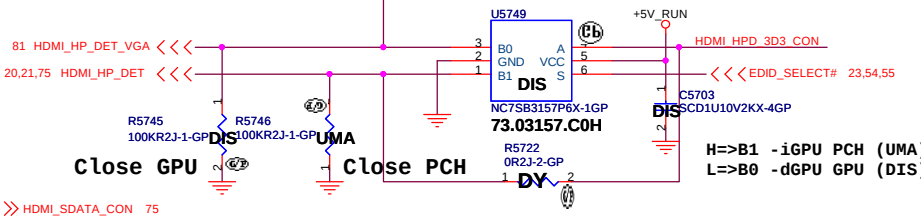
UMA/DIS HDMI DDC CLK/DAT select circuit



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



UMA/DIS HDMI Detection select circuit



Close GPU

Close PCH

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

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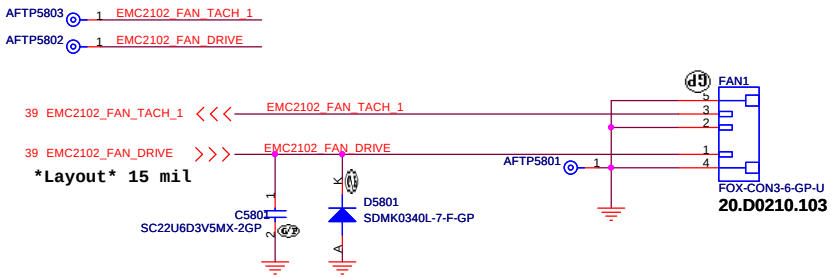
Title: HDMI Connector

Size	Document Number	Rev
A3	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 57 of 90

SSID = Thermal

Fan Connector



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Title		
58_FAN		
Size: A3	Document Number: Vostro Calpella	Rev: SA
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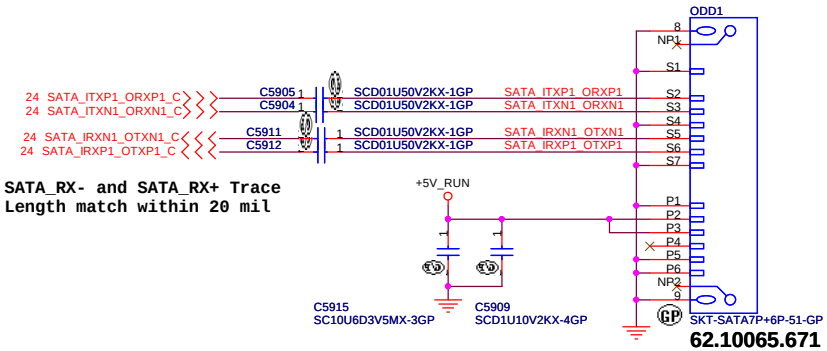
SSID = SATA

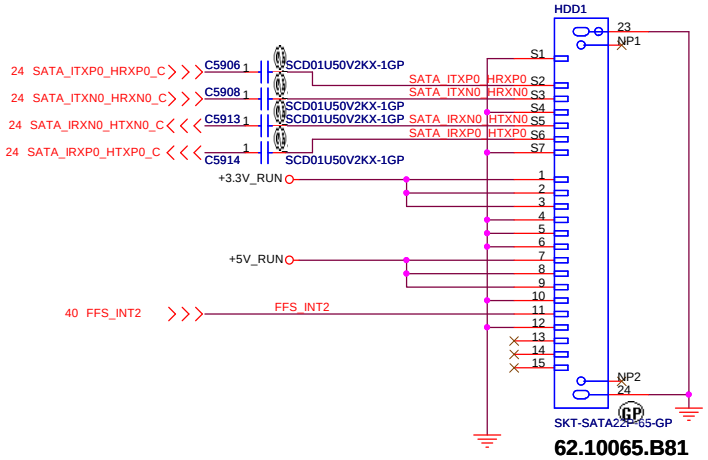
ODD Connector



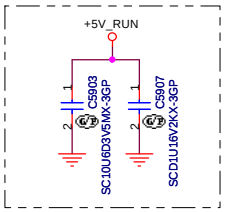
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

SSID = SATA

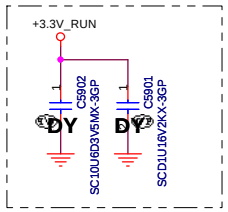
SATA HDD Connector



Close to CONN
5V power pin



Close to CONN
3.3V power pin




```
SATA HDD Interface comment
*******************************
--- GND
RX+
RX-
--- GND
TX-
TX+
--- GND
*******************************
------------ 3.3V
------------ 3.3V
------------ 3.3V
--- GND
--- GND / Dell Detected Pin
--- GND
------------ 5V
------------ 5V
------------ 5V
--- GND
(Dell: FFS_INT for supported HDD)
--- GND
------------ 12V
------------ 12V
------------ 12V
*******************************
```

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Title: HDD/ODD Connector

Size	Document Number	Rev
A3	Vostro Calpella	SA

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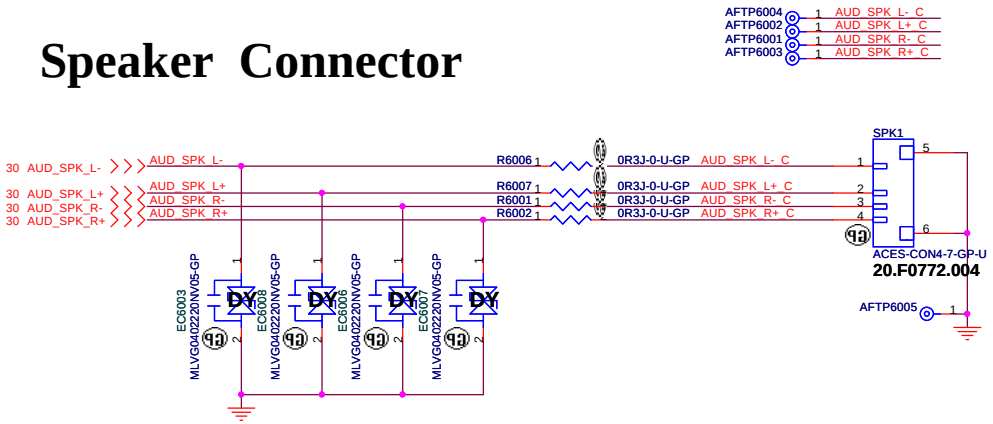
SSID = AUDIO

Speaker Connector



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Title: *Speaker/HP/MIC Jack*

Size	Document Number	Rev
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Title: *(Reserve)*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

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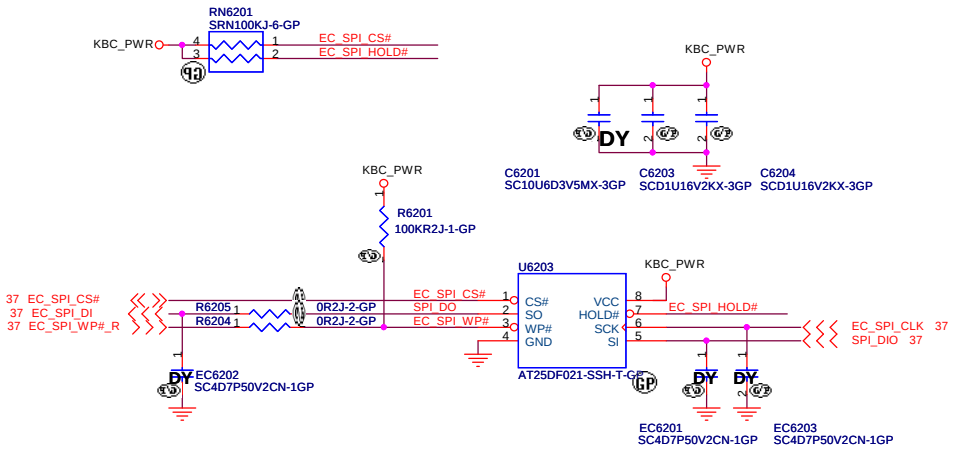
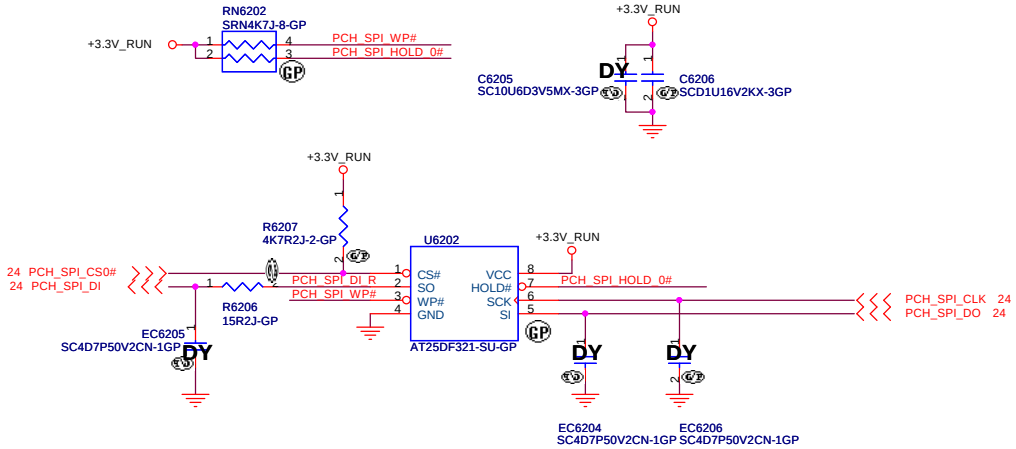
SSID = Flash.ROM

SPI FLASH ROM (256K Bytes) for KBC

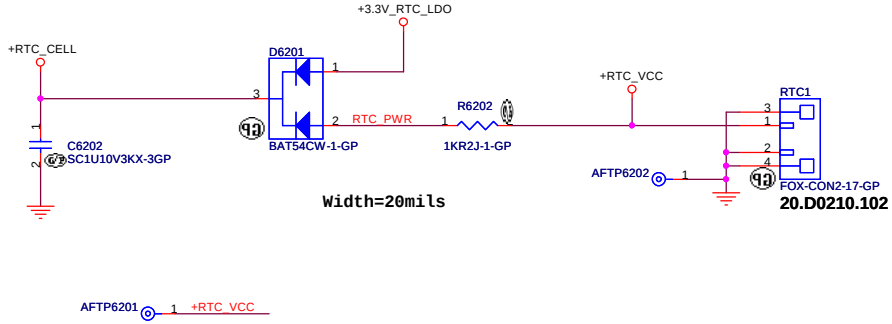


SPI FLASH ROM (4M Bytes) for PCH



SSID = RBATT

RTC Connector



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Title: EEPROM/RTC Connector

Size	Document Number	Rev
A3	Vostro Calpella	SA

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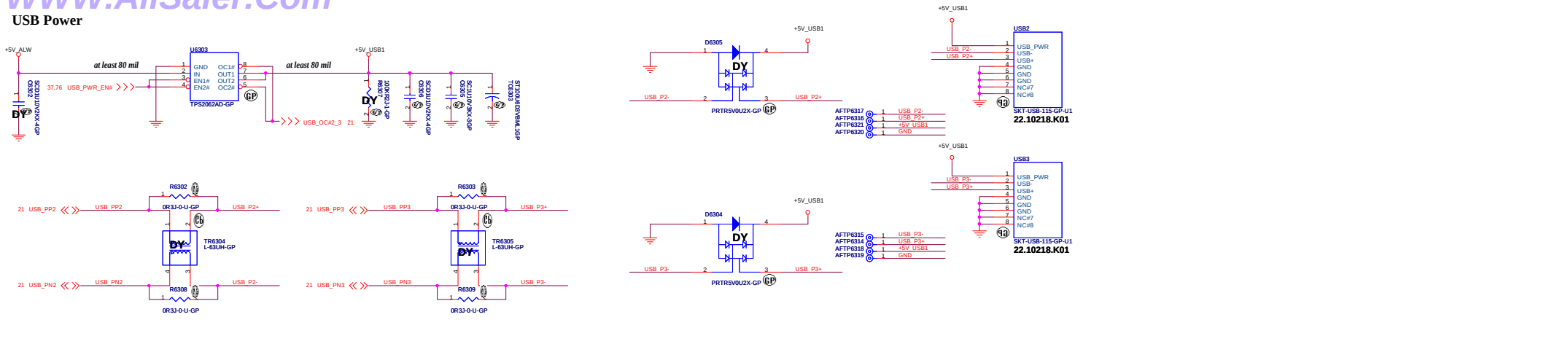
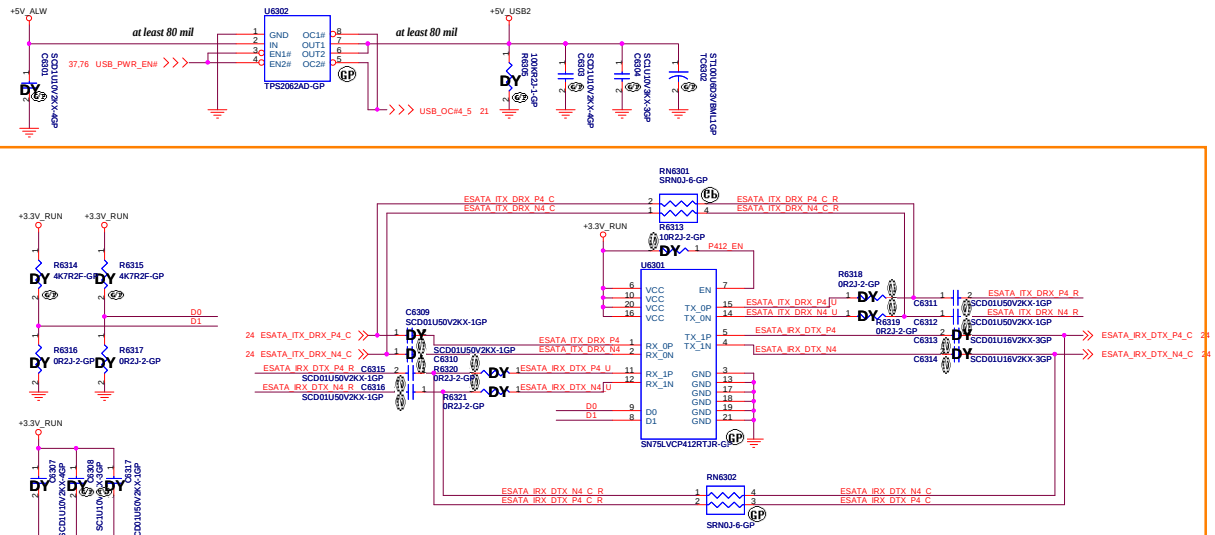
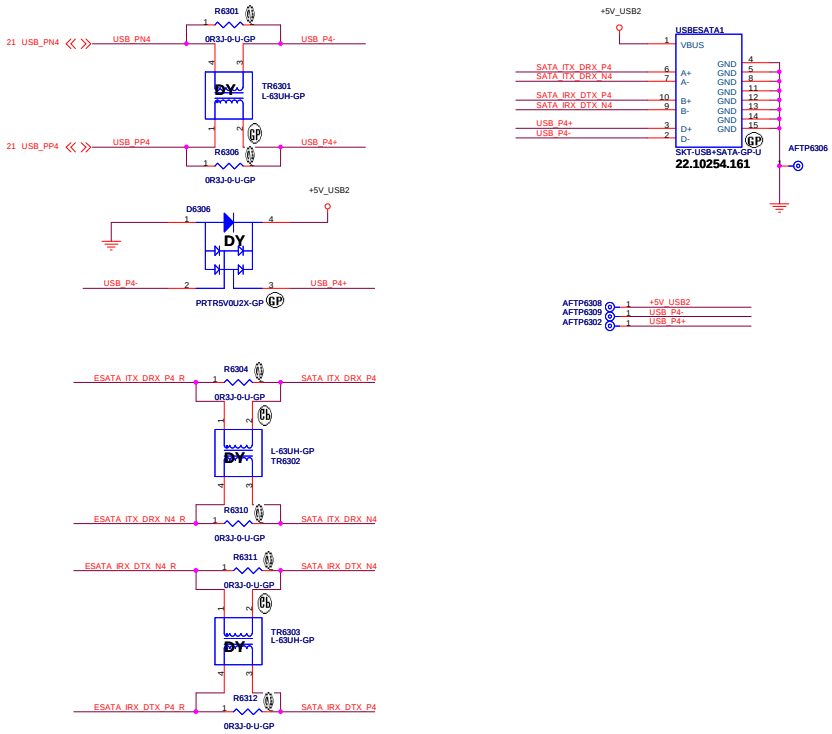
SSID = USB

USB Power



ESATA Power





	If you added U6301(SN75LVCP412RTJR-GP). You need to BOM change
ASM	R6313, R6314, R6315, R6318, R6319, R6320, R6321 C6309, C6310, C6313, C6314, C6307, C6308, C6317
DY	RN6301, RN6302

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Title: USB /ESATA Port

Size	Document Number	Rev
A2	Vostro Calpella	SA

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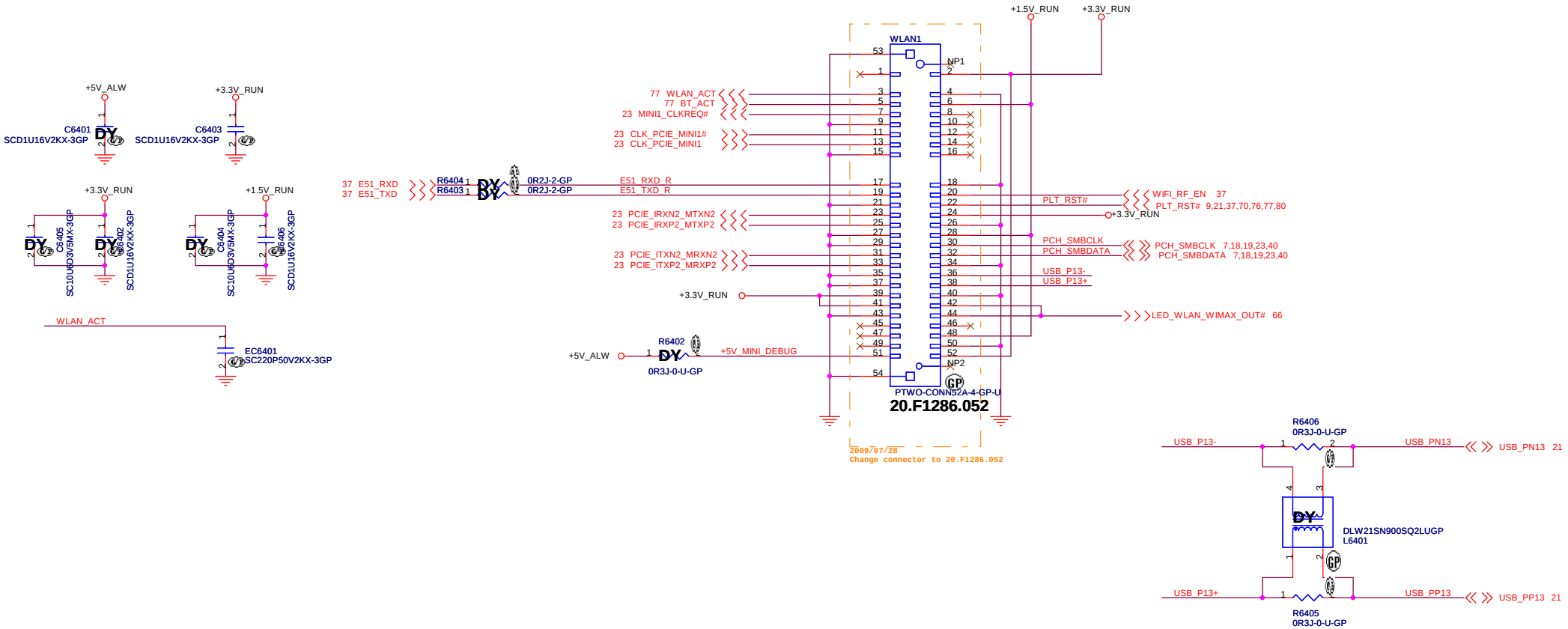
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title: ***MINICARD(WLAN)/ITP CONN***

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

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Title

WWAN Connector

Size	Document Number	Rev
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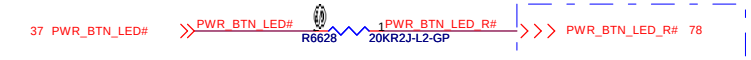
For LED & Capacity board:

LED Type	Color	Power rail
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN WIMAX LED	White	RUN

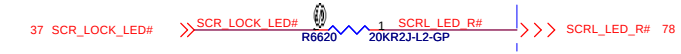
For IO board:

LED Type	Color	Power rail
PWR LED2	White(Multi-color)	ALW
BATTERY LED2	Amber(Multi-color)	ALW
	White(Multi-color)	ALW

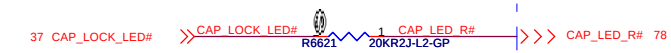
PWR BTN LED



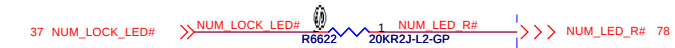
SCRLK LED



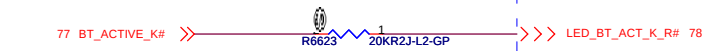
CAPS LED



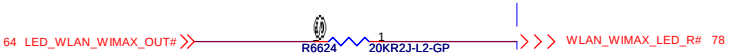
NUM LED



Bluetooth LED

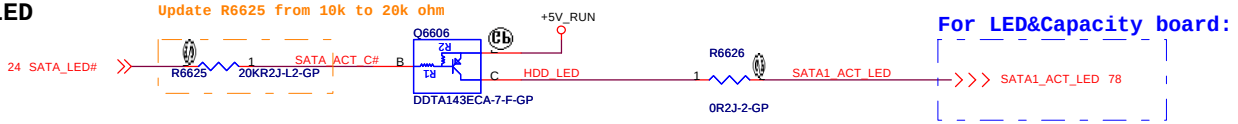


WLAN LED



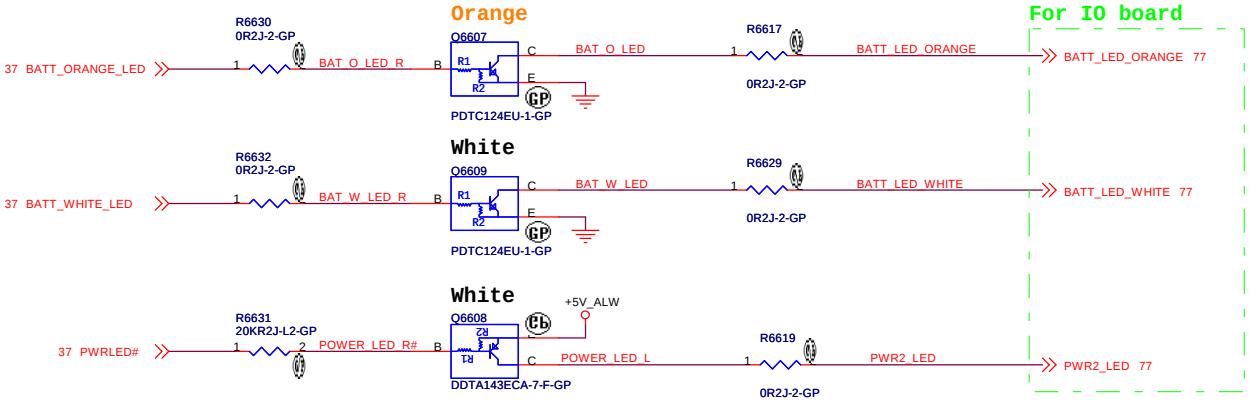
HD LED

2009/07/29
Update R6625 from 10k to 20k ohm



Power & Battery LED

2009/08/12
Changed battery LED be one LED with bi-color (white and amber). For I/O board. Update Spec.



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Title: LED

Size	Document Number	Rev
A3	Vostro Calpella	SA

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Title: (Reserve)

Size	Document Number	Rev
A2	Vostro Calpella	SA

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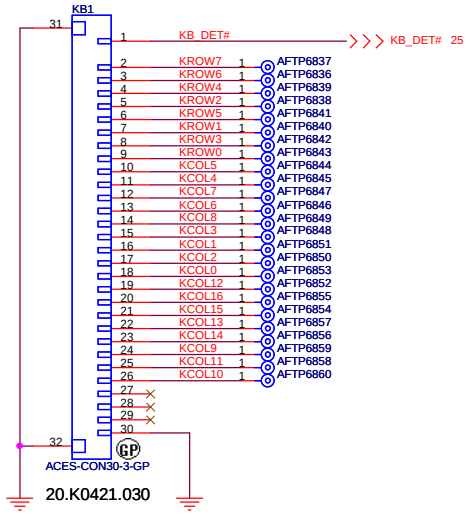
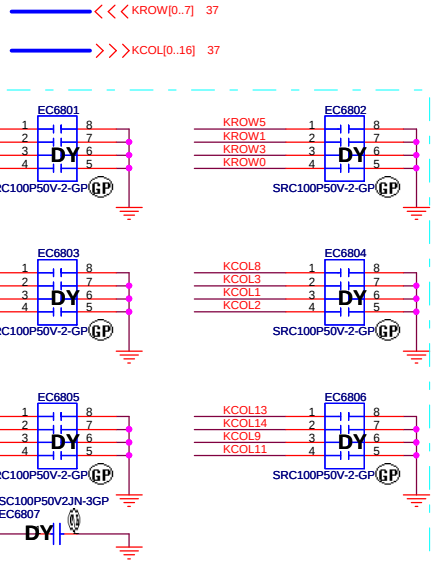
SSID = KBC

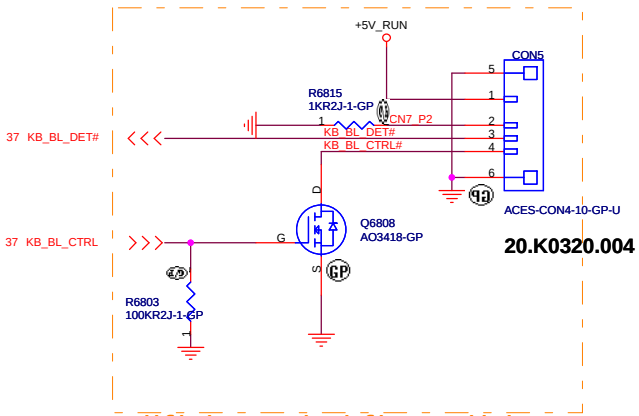
Internal KeyBoard Connector





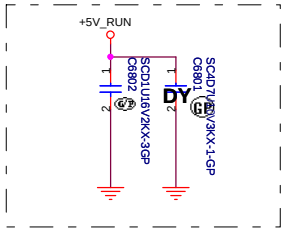
Added KB1 EMI Cap
2009/06/17

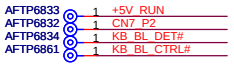
KB Backlight CONN



Modified CON5 pin define & added N-MOS
2009/07/17

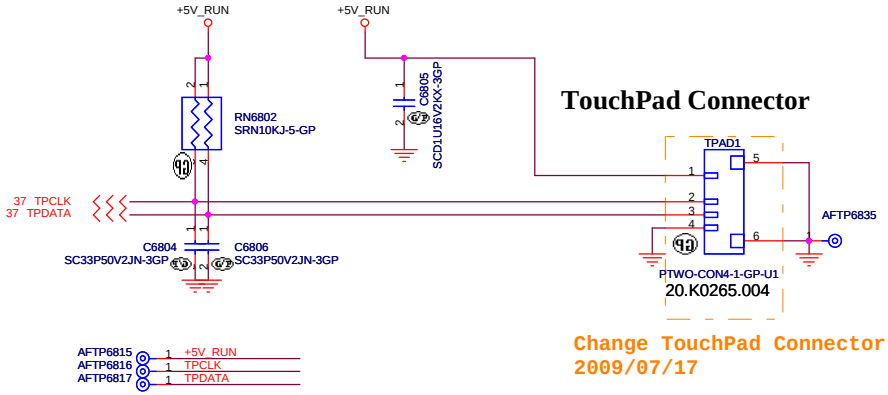
Place near CON5





SSID = Touch.Pad

TouchPad Connector



Change TouchPad Connector
2009/07/17

UMA

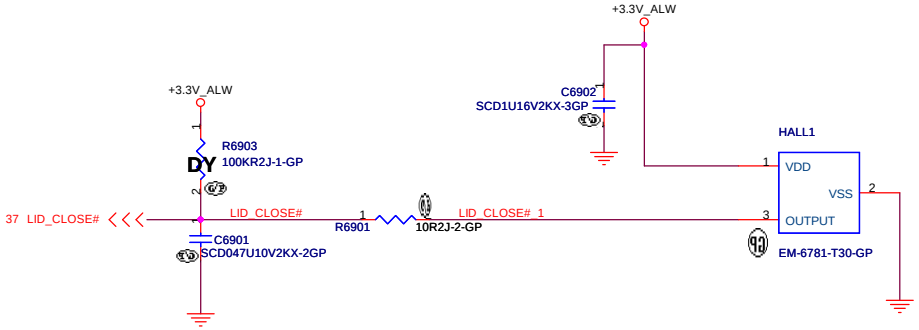
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard/Touch Pad

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 68 of 90

Hall Sensor Connector



UMA

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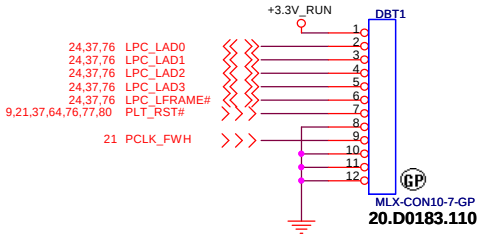
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Hall sensor*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 69 of 90

GOLDEN FINGER FOR DEBUG BOARD



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Debug port*

Size	Document Number	Rev
A3	*Vostro Calpella*	*SA*

Date: Tuesday, September 08, 2009 Sheet 70 of 88

(Blank)

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PX Swith-2

Size: A3 | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 71 of 90

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Braidwood

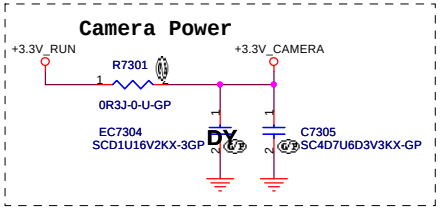
Size	Document Number	Rev
A3	***Vostro Calpella***	***SA***

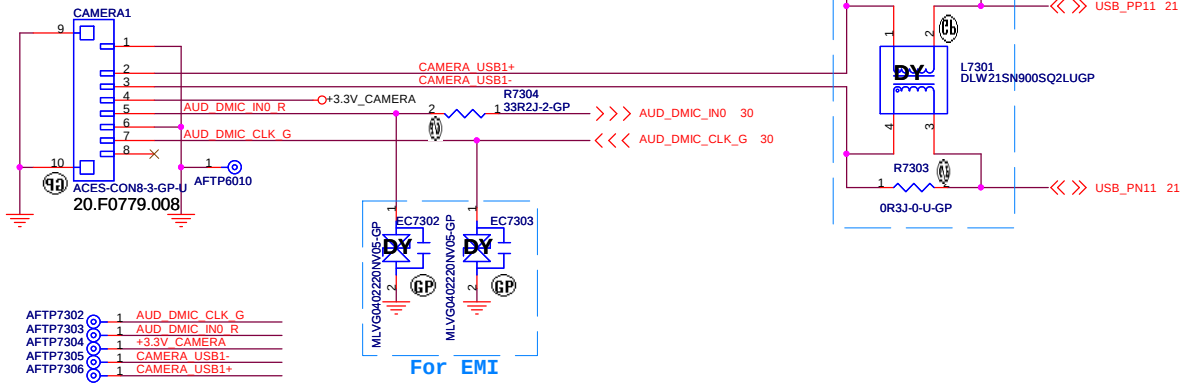
Date: Tuesday, September 08, 2009 Sheet 72 of 90

SSID = User.Interface

Camera Connector

2009/07/31
Change CAMERA1 connector pin define.
For cable is already to be finished





UMA

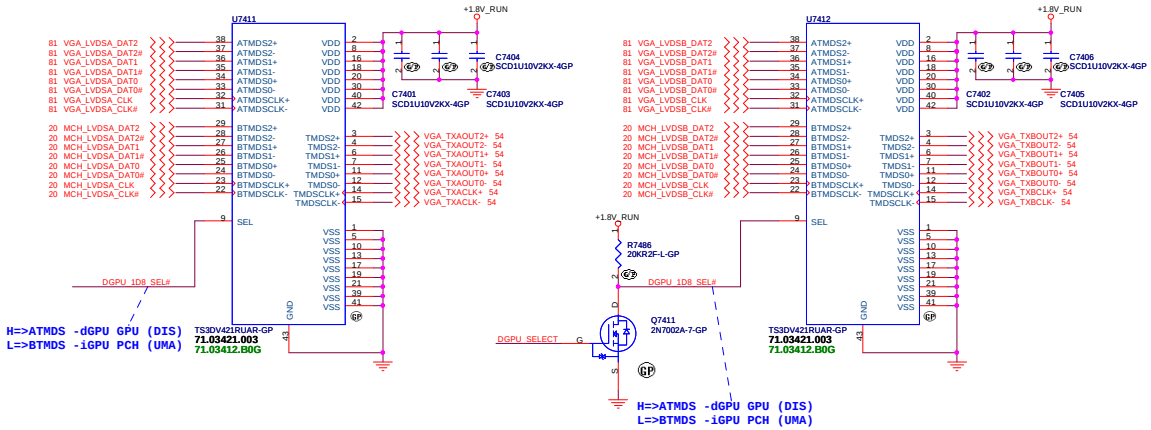
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Camera Connector

Size: A3 | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 73 of 90

UMA/DIS LVDS signal select circuit



FUNCTION TABLE

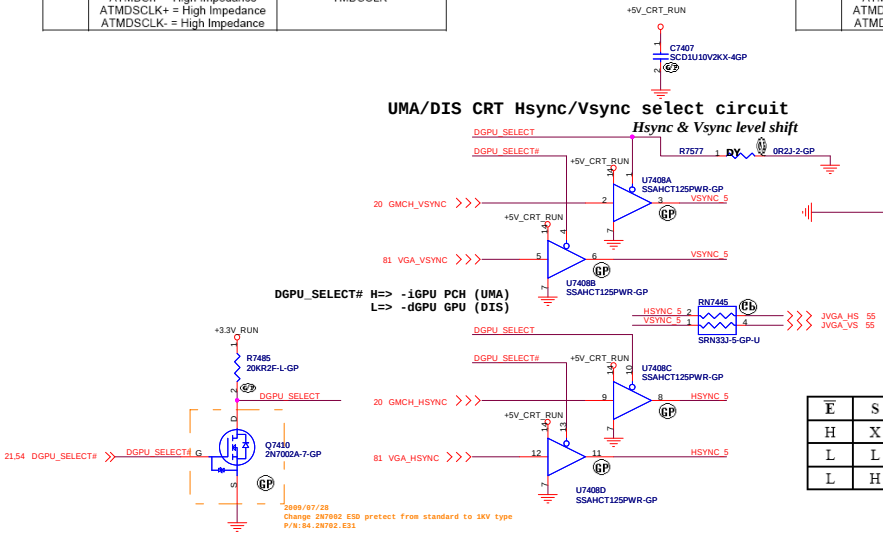
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

FUNCTION TABLE

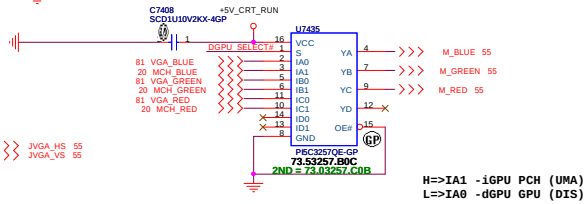
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



UMA/DIS CRT signal select circuit



$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

UMA

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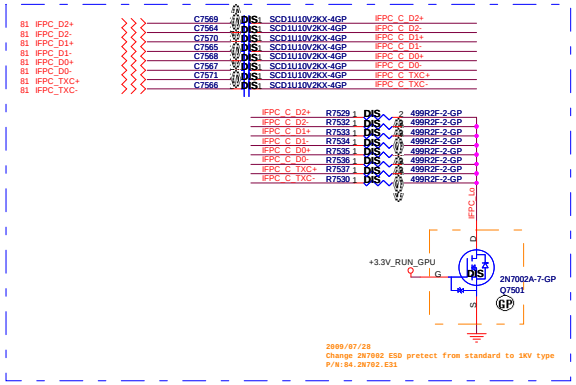
Title: PX Swith-1

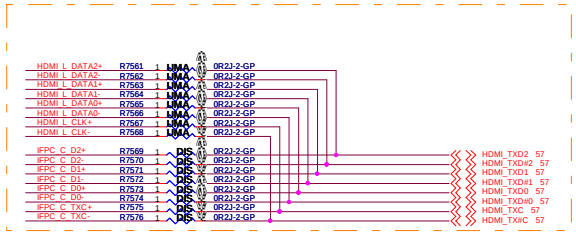
Size	Document Number	Rev
Custom	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 74 of 90

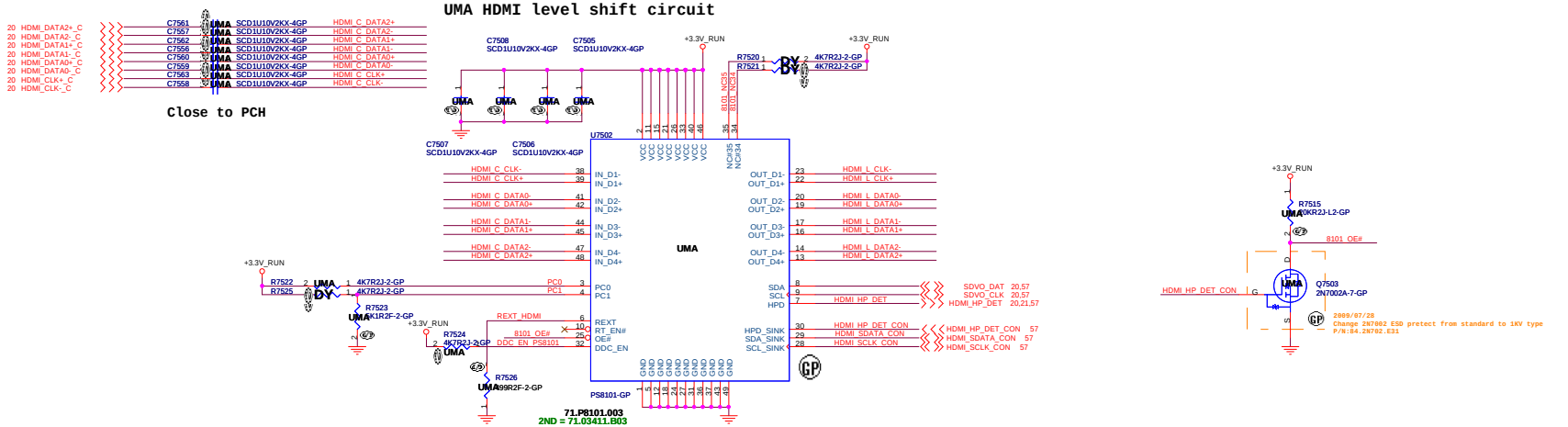
Close to connector



UMA/DIS HDMI signal select circuit



UMA HDMI level shift circuit



UMA

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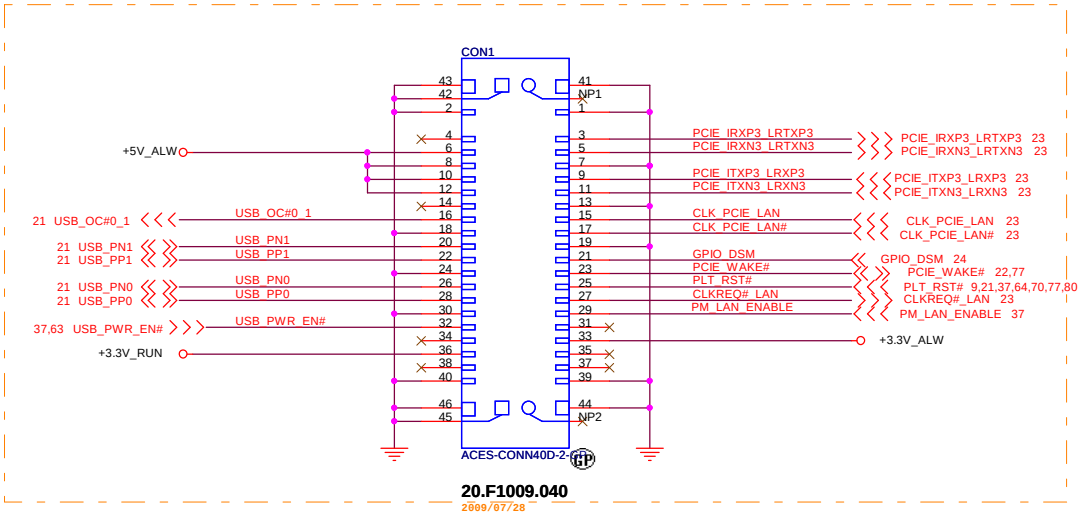
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserve)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 75 of 90

LAN baord CON

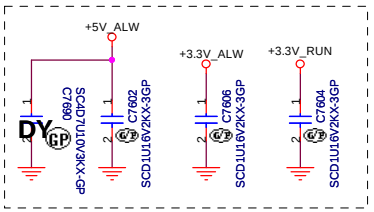


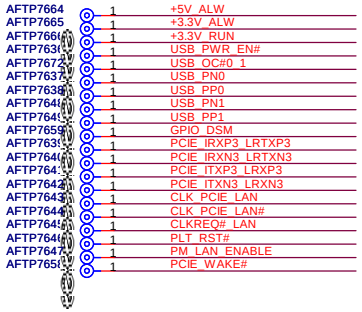
20.F1009.040

2009/07/28
Change connector to 20.F0692.060
2009/08/17
Change connector to 20.F1044.040
and chenge pin define
2009/08/25
Change connector to 20.F1009.040

2009/07/27
Change TPM to connector
2009/07/30
Change TPM1 connector to 20.K0238.010

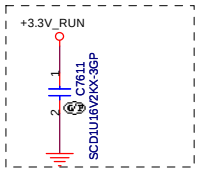
Place near CON1

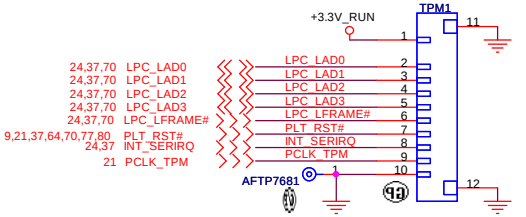




TPM board CON

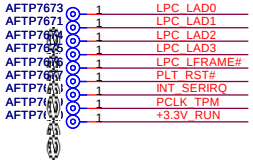
Place near TPM1





+3.3V_RUN : 30mA

20.K0238.010



UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

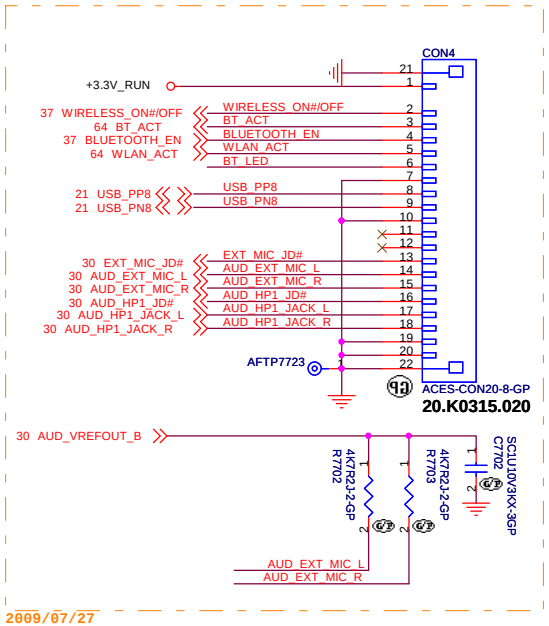
Title: **LAN Board Connector**

Size: A3 | Document Number: **Vostro Calpella** | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 76 of 88

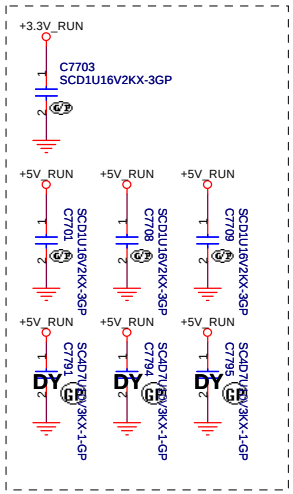
SSID = User.Interface

Audio board CON

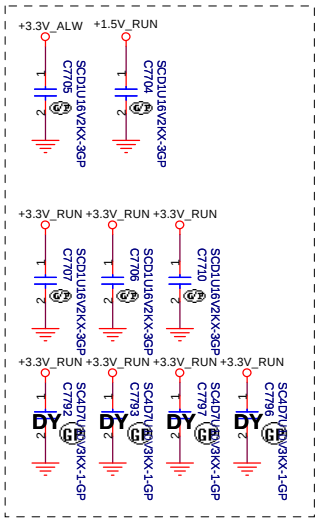


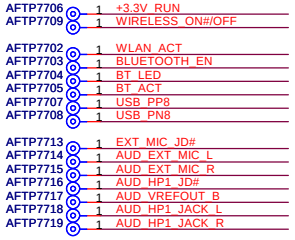
2009/07/27
Change CON4 PIN define
Remove +15V_ALW
2009/07/29
Change CON4 connector to 20.K0275.028
And change CON4 pin define
2009/08/03
Change CON4 pin define.
2009/08/18
Change CON4 connector P/N:20.K0315.020
2009/08/19
Remove AUD_VREFOUT_B from Audio board to main board.

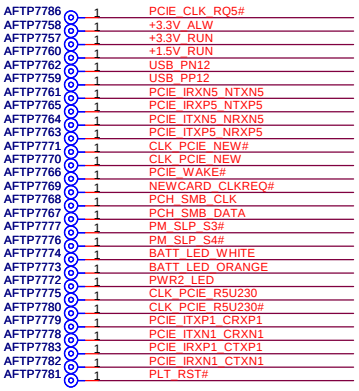
Place near CON4

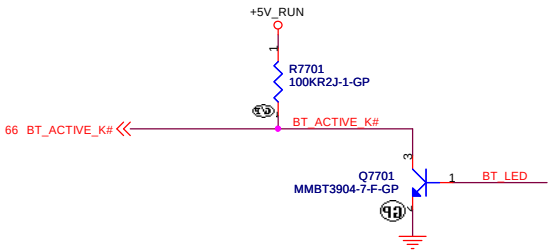


Place near CON6

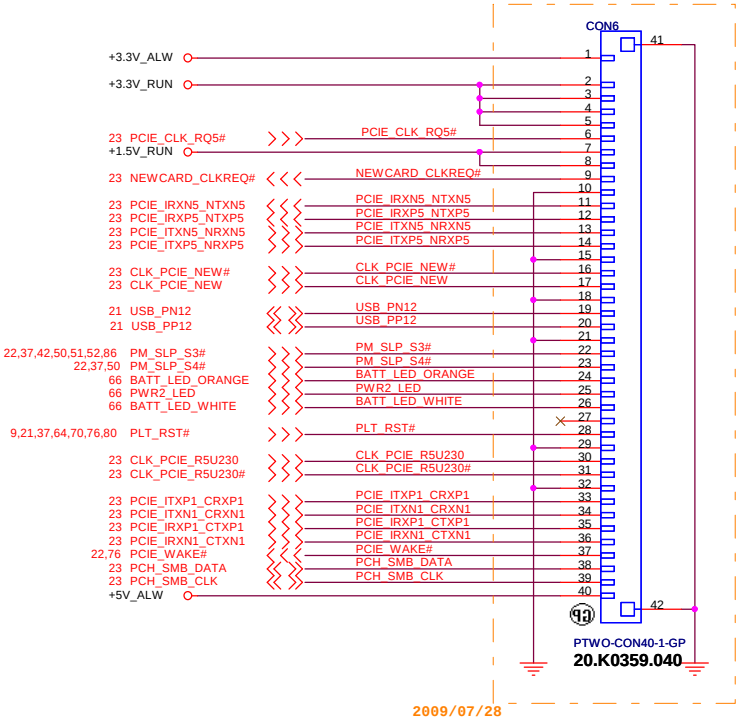








IO baord CON



2009/07/28
Change CON6 connector to 20.K0286.040
2009/08/05
Change CON6 pin define
2009/08/12
Change CON6 pin define

UMA

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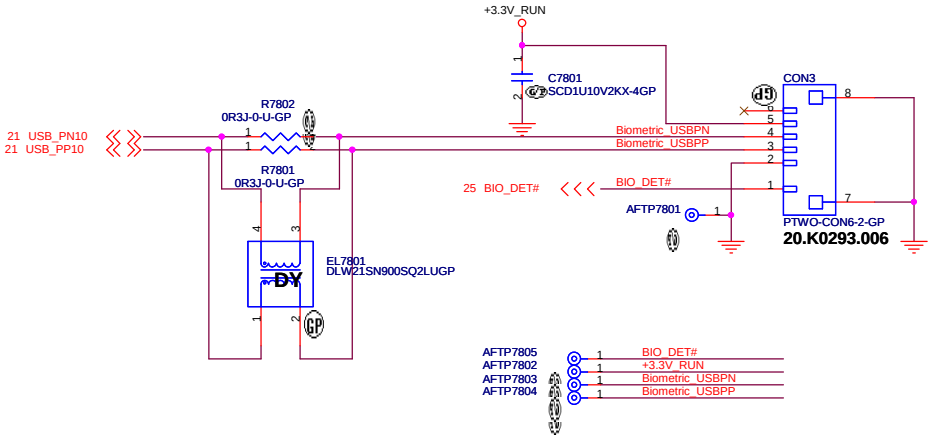
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board/Audio Board Connector

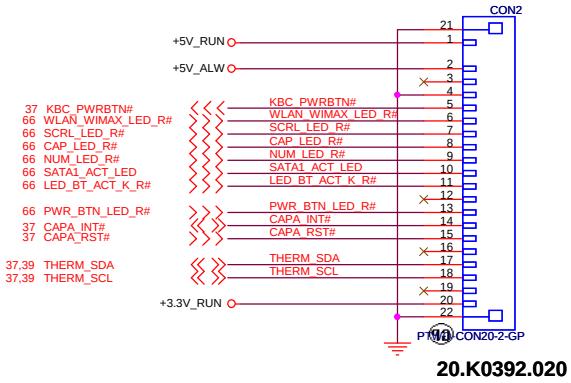
Size	Document Number	Rev
A3	Vostro Calpella	SA

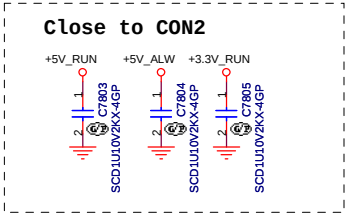
Date: Tuesday, September 08, 2009 Sheet 77 of 90

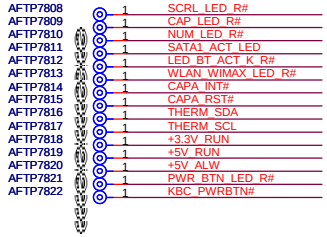
Finger Printer Connector



LED&Capacity board CONN







UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

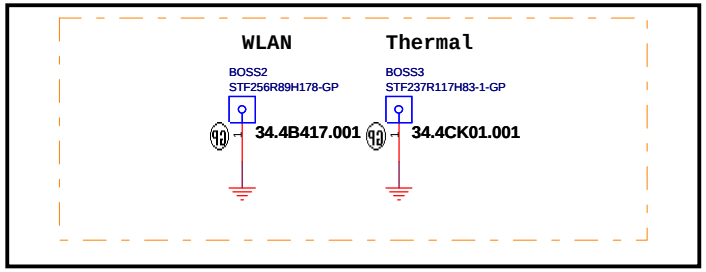
Title: Finger Printer

Size: Custom | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 78 of 90

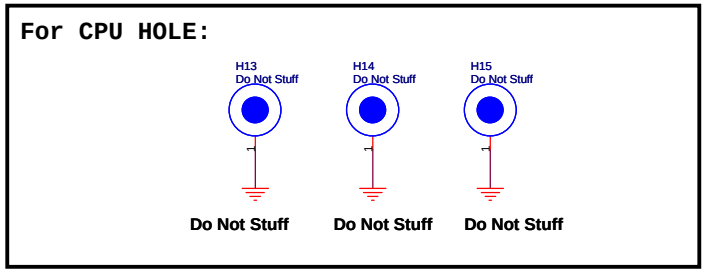
SSID = Mechanical

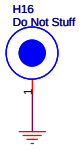
BOSS:



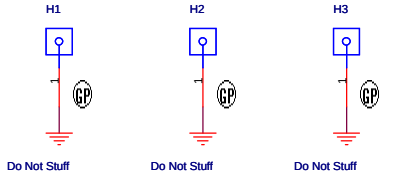
2009/07/30
Change connector

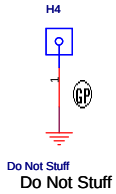
For CPU HOLE:

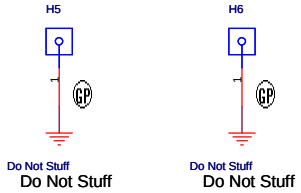


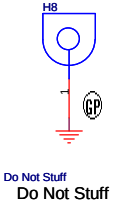


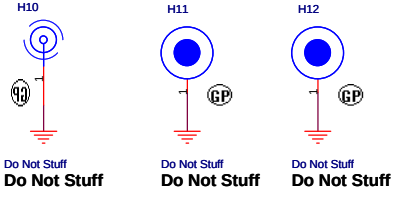
HOLE:

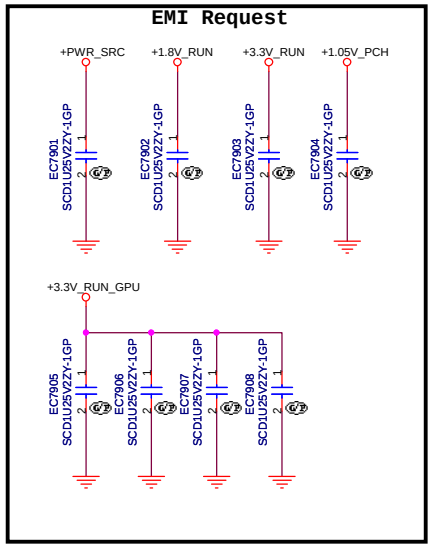












UMA

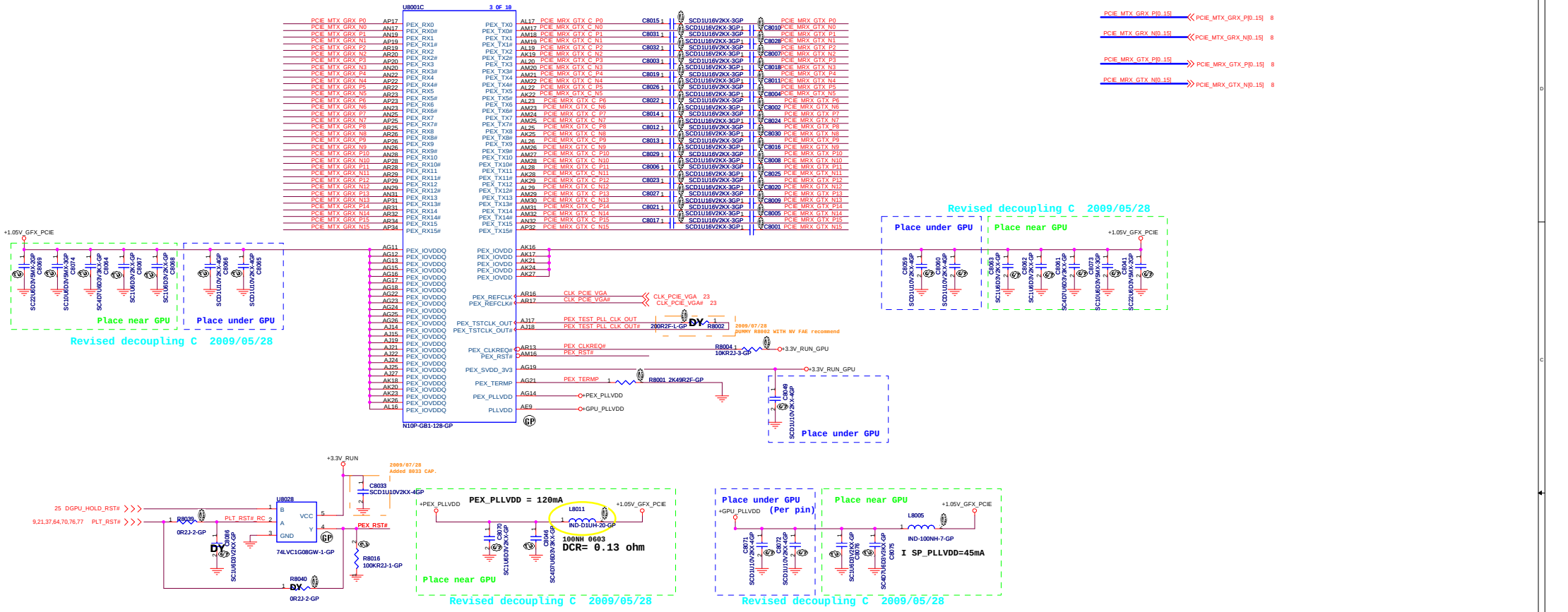
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Miscellaneous Components*

Size: Custom | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Tuesday, September 08, 2009 | Sheet 79 of 90

SSID = VIDEO



UMA

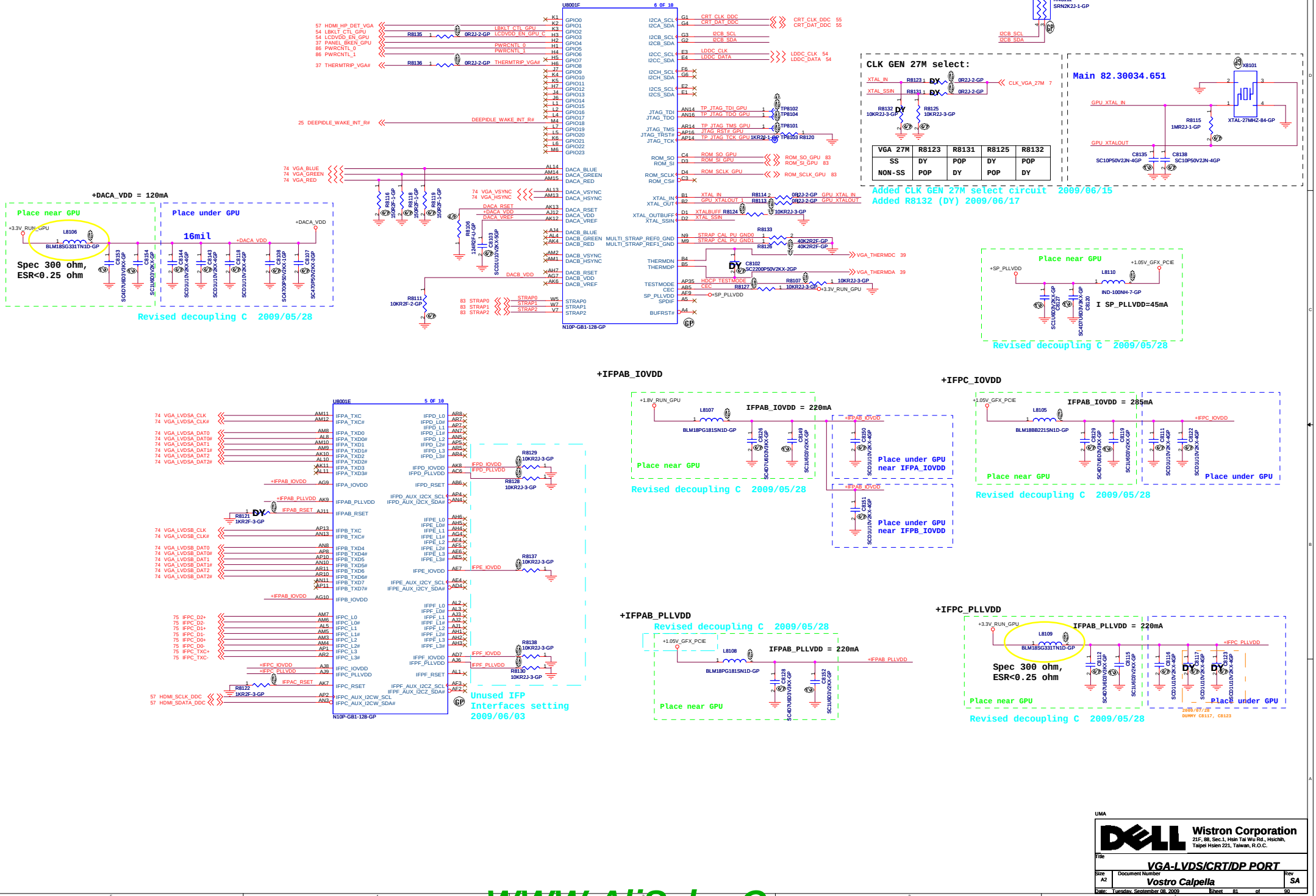
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 80 of 90

SSID = VIDEO



SSID = VIDEO

+VCC_GFX_CORE = 31.66A

FBVDD/Q = 2.24A

Revised decoupling C 2009/05/28

Revised decoupling C 2009/05/28

Layout notice:
VDD_SENSE need check layout SPEC.

UMA

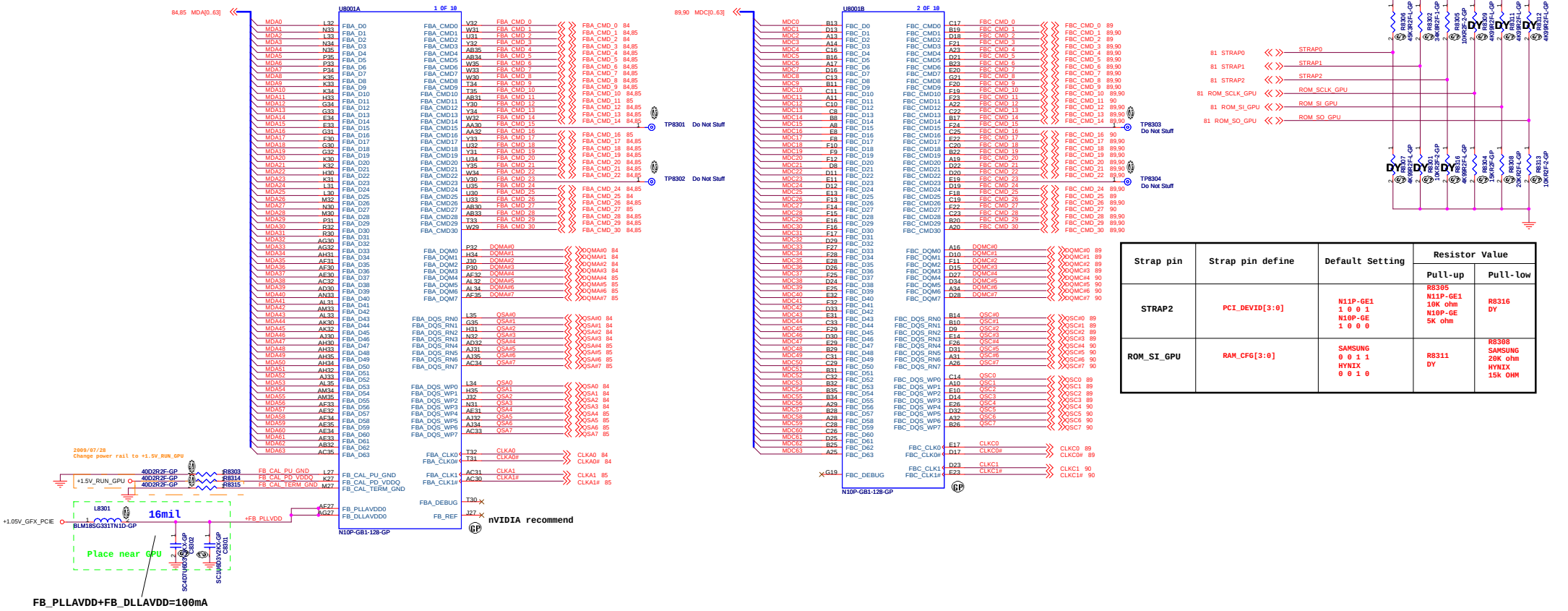
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-POWER/GND(3/4)

Size: A2 | Document Number: Vostro Calpella | Rev: SA

Date: Tuesday, September 08, 2009 | Sheet 82 of 90

SSID = VIDEO



Strap pin resistor need use 1% resistor (NV Design Guide)

Strap pin	Strap pin define	Default Setting	Resistor Value	
			Pull-up	Pull-low
STRAP2	PCI_DEVID[3:0]	N11P-GE1 1 0 0 1 N10P-GE 1 0 0 0	R8305 N11P-GE1 10K ohm N10P-GE 5K ohm	R8316 DY
ROM_SI_GPU	RAM_CFG[3:0]	SAMSUNG 0 0 1 1 HYNIX 0 0 1 0	R8311 DY	R8308 SAMSUNG 20K ohm HYNIX 15K OHM

UMA

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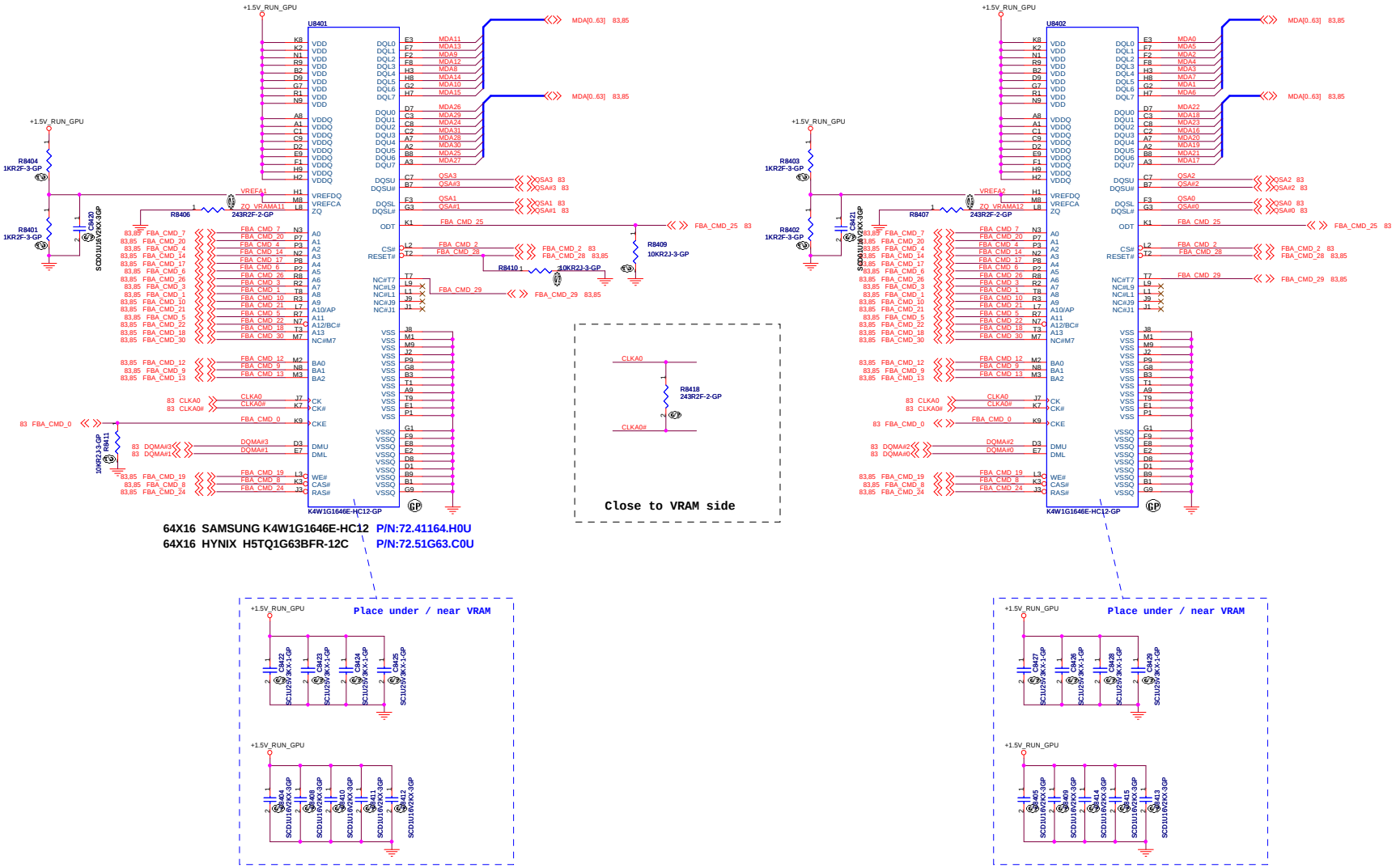
Title: VGA-MEMORY(5/5)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 83 of 90

SSID = VIDEO



UMA

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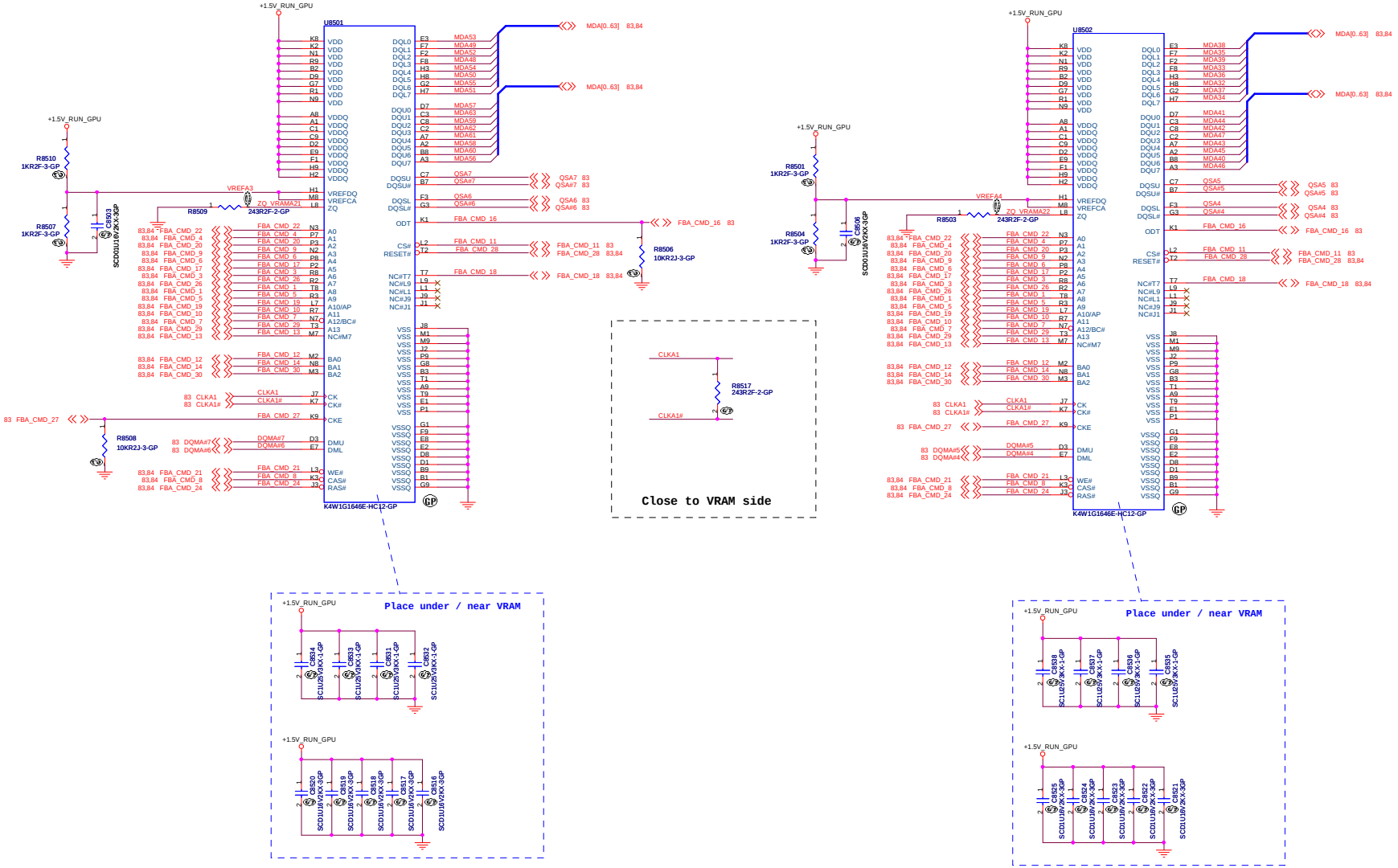
Title: VRAM(1/2)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 84 of 90

SSID = VIDEO



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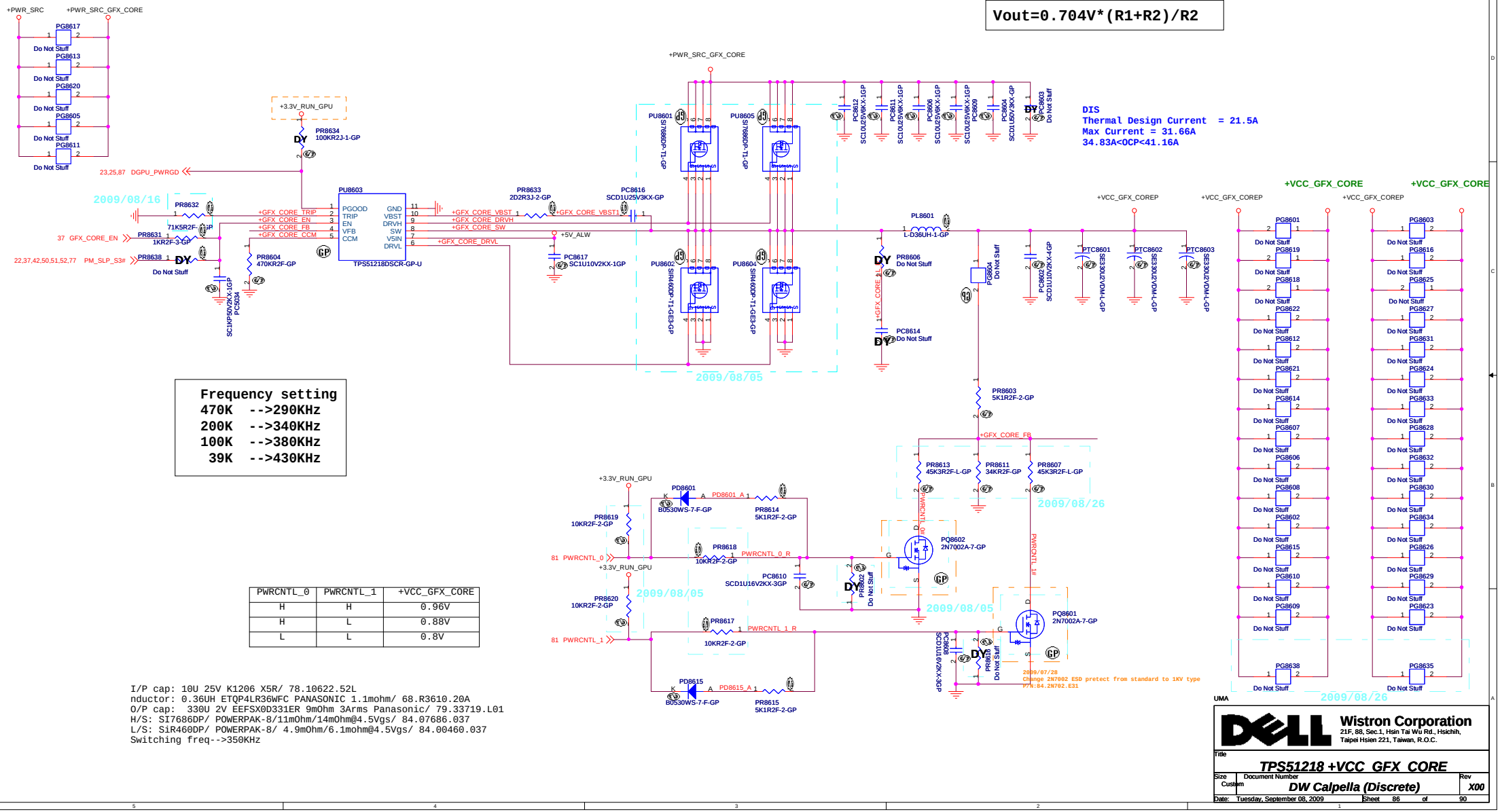
Title: VRAM

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 85 of 90

SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2



PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	0.96V
H	L	0.88V
L	L	0.8V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
nductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

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Title: TPS51218 +VCC_GFX_CORE

Size	Document Number	Rev
Custom	DW Calpella (Discrete)	X00

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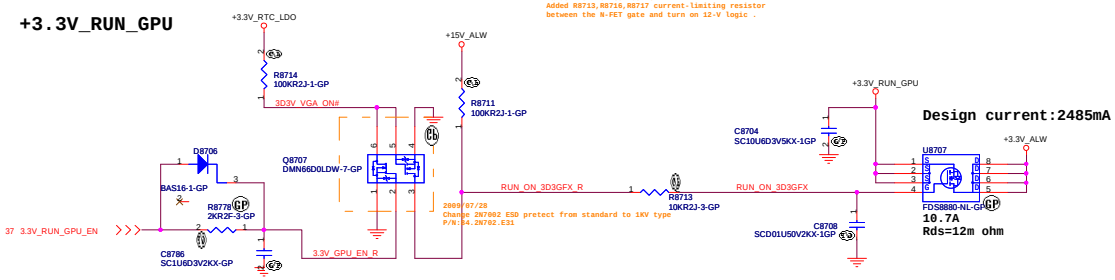
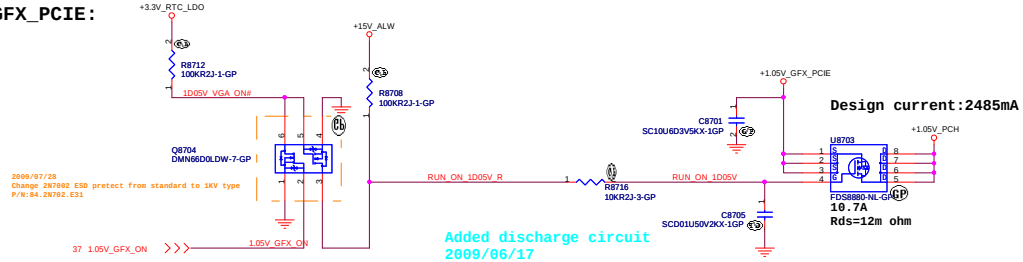
+3.3V_RUN_GPU



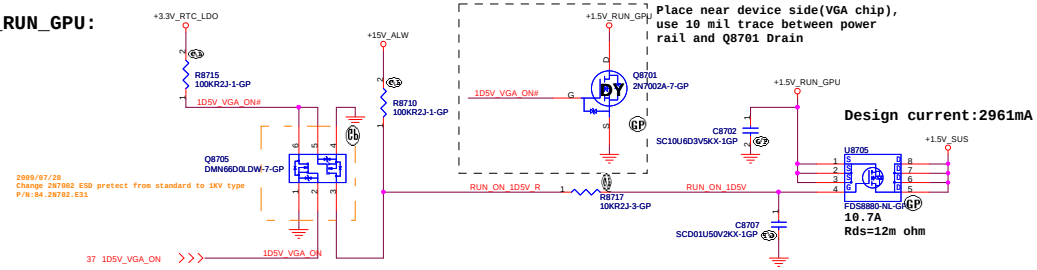
Added +1.05V_GFX_PCIE, +1.5V_RUN_GPU power switch 2009/05/25

+1.05V_GFX_PCIE:



Added discharge circuit
2009/06/17

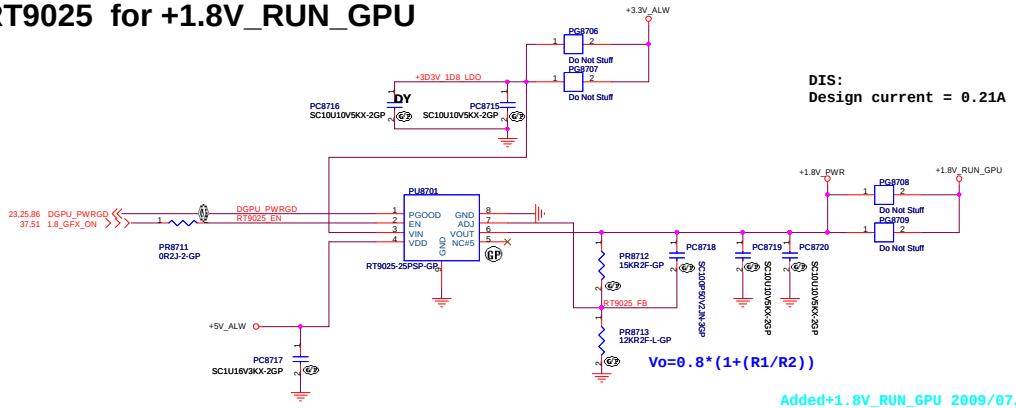
+1.5V_RUN_GPU:



Place near device side(VGA chip), use 10 mil trace between power rail and Q8701 Drain

+1.8V_RUN_GPU

RT9025 for +1.8V_RUN_GPU



DIS:
Design current = 0.21A

Vo=0.8*(1+(R1/R2))

Added+1.8V_RUN_GPU 2009/07/17

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Title: LDO 1.8V

Size: Custom | Document Number: Vostro Calpella | Rev: SA

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
1	12	2009/07/13		DW70 need support Clarksfield(Qual core)	Add VTT_SELECT pin to control VTT_CORE voltage level	SA
2	21	2009/07/13			Add USB port for right side board	SA
3	23	2009/07/13			Follow 15 inch PCI-E port	SA
4	65	2009/07/13			Add SIM card schematic	SA
5	76	2009/07/13			Add LAN board connector schematic	SA
6	77	2009/07/13			Change IO board connector and add Audio board connector	SA
7	78	2009/07/13			Add Finger Printer Connector schematic	SA
8	30,60	2009/07/14			Remove AUDIO Schematic and speaker connector	SA
9	35	2009/07/14			Remove LAN Schematic	SA
10	54	2009/07/14			LCD_BRIGHTNESS follow 15 inch schematic	SA

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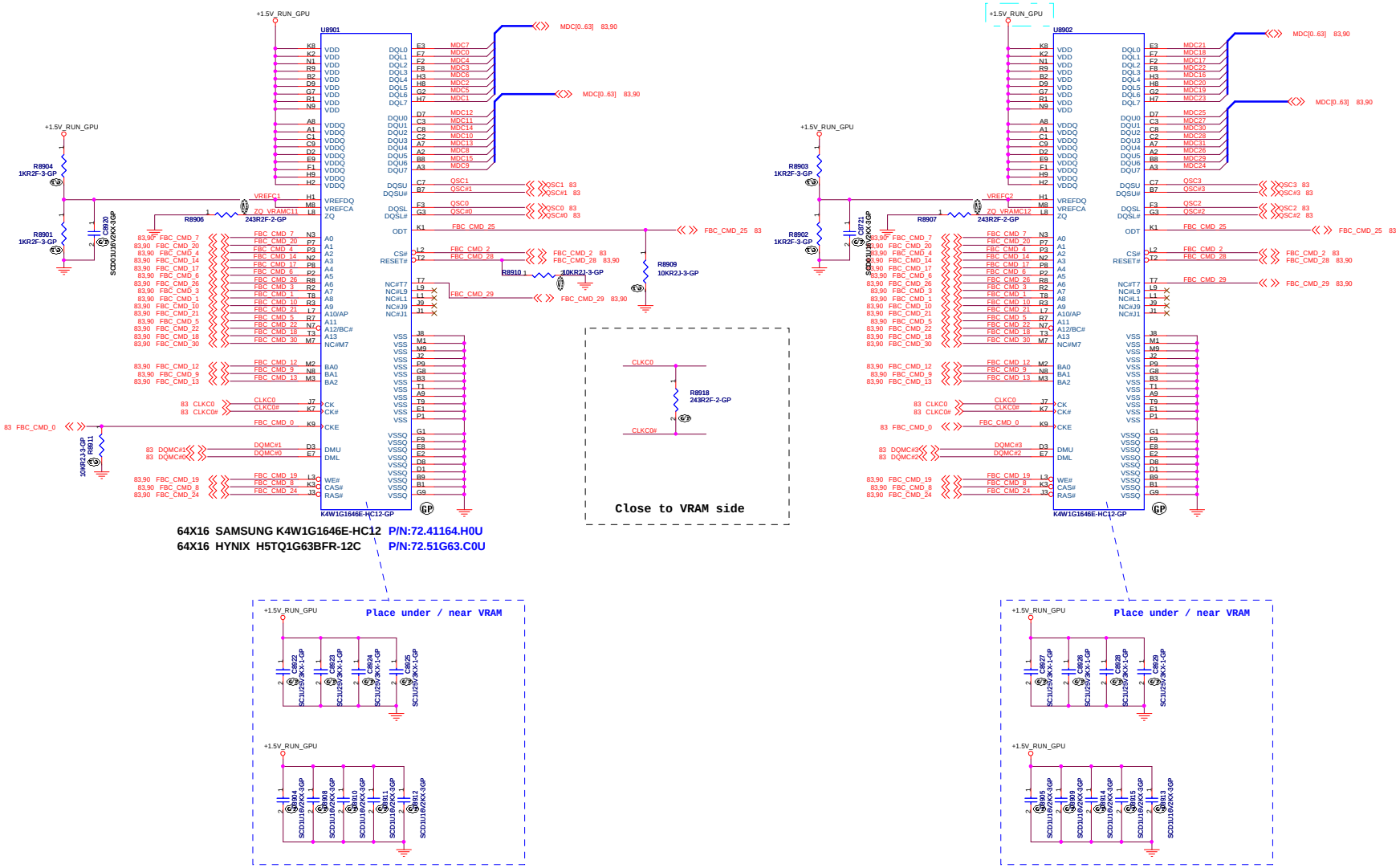
Title: *Change List(1/3)*

Size: A3 | Document Number: *Vostro Calpella* | Rev: *SA*

Date: Tuesday, September 08, 2009 | Sheet 88 of 90

SSID = VIDEO



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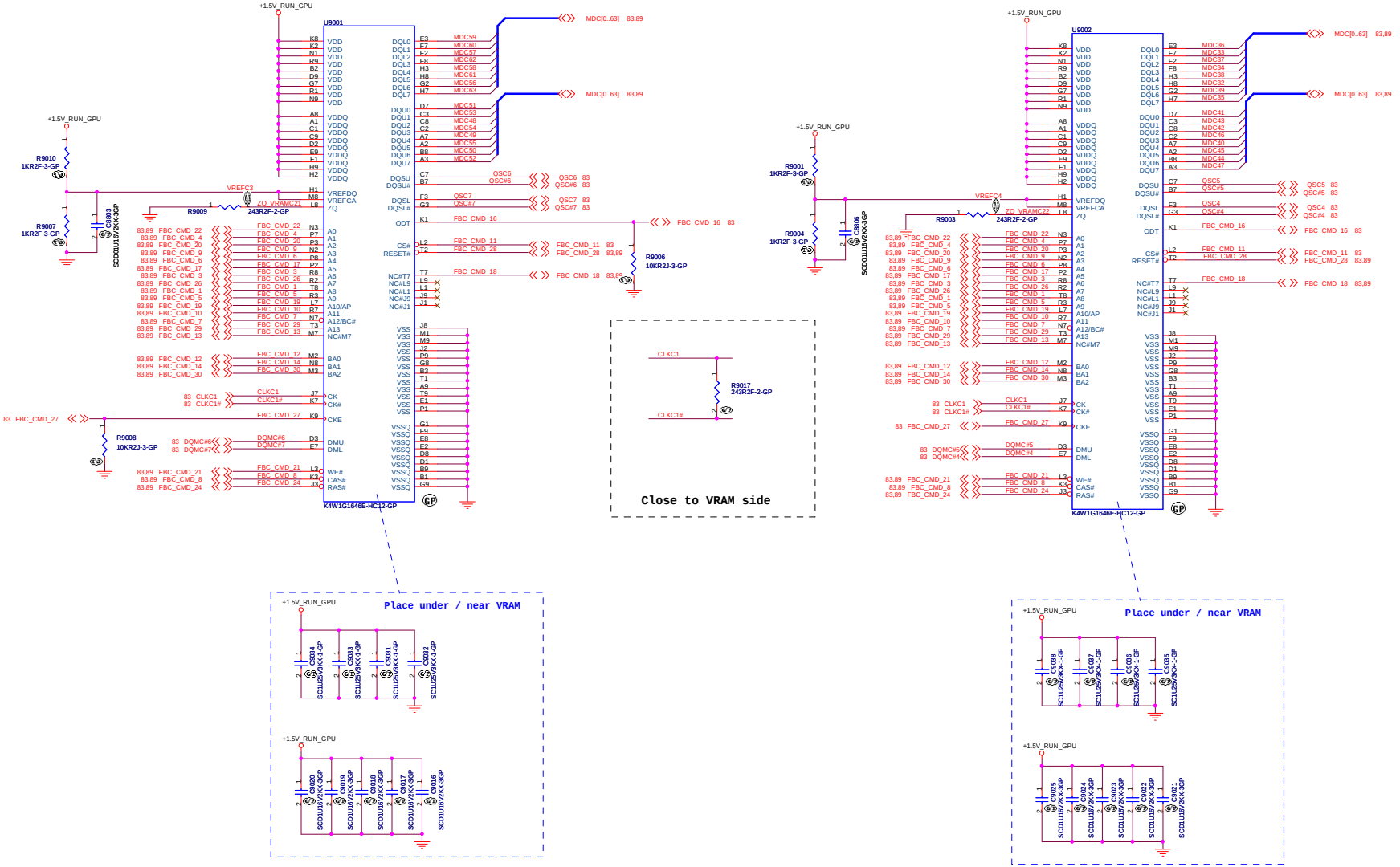
Title: VRAM(1/2)

Size	Document Number	Rev
A2	Vostro Calpella	SA

Date: Tuesday, September 08, 2009 Sheet 89 of 90

SSID = VIDEO



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Title: VRAM

Size	Document Number	Rev
A2	Vostro Calpella	SA

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