

ZZZ1

PCB
14*DAZ@

ZZZ2

LA-7011P
14*DA@

ZZZ3

LS-7011P
14*DA@

ZZZ4

LS-7013P
14*DA@

ZZZ5

LS-7014P
14*DA@

Compal Confidential

Schematics Document

PAW10

Montevina

with Intel Cantiga + ICH9 core logic

REV:1.0A

2010-12-24

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Clock Generator
SLG8SP556VTR

page16

Mobile Penryn

uPGA-478 CPU

page4, 5, 6

For 14"
LS-7011P 4PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

For 15"
LS-7012P 8PIN PWR/B
LS7013P Audio/B
LS7014P Touch/B

H_A#(3..35)
H_D#(0..63)



FSB
667/800MHz

CRT Connector

page21

LVDS
Connector

page22

Intel Cantiga GMCH

GM45

uFCBGA 1329

page 7, 8, 9, 10, 11, 12, 13

DDR3-SO-DIMM X2

BANK 0, 1, 2, 3

page 14,15

Dual Channel
DDR3-667/800(1.5V)

up to 4G

DMI *4

C-Link

**Wire Less Mini
card Slot 1**

page23

6*PCL-E BUS

Intel ICH9-M

page 17, 18, 19, 20

**SPI ROM
BIOS**

LPC BUS

EC

ENE KB926 E0

page27

AR8151/8152

10/100/Giga LAN

page24

RJ45 CONN

page25

AZALIA

Audio Codec
CONEXTAN

CX20671

page26

2Channel Speaker

page26

Analog MIC_Int

page26

CMOS Camera

page22

BlueTooth CONN

page30

USB CONN X1(Right)

page29

USB PORT X1(Left)

page29

USB PORT X1(Left)

page29

Audio Jack SB CONN
HP X 1+

MIC_Ext X1

page30

Card Reader RTS5139

SATA HDD CONN

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SATA ODD CONN

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Touch Pad

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Int.KBD

page32

**SPI ROM
BIOS**

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DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	ICH9	Thermal
EC_SMB_CK1 EC_SMB_DA1	KB926 +3VALW	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB926 +3VALW	X	X	X	X	X	X	V +3VS
ICH_SMBCLK ICH_SMBDATA	ICH +3VALW	X	X	V +3VS	V +3VS	V +3VALW	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM	A0	10100000
DDR SO-DIMM	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

Structure	Description	NON-USE
45@	45 BOM	
BT@	Blue Tooth function	
CMOS@	CMOS CAMERA function	

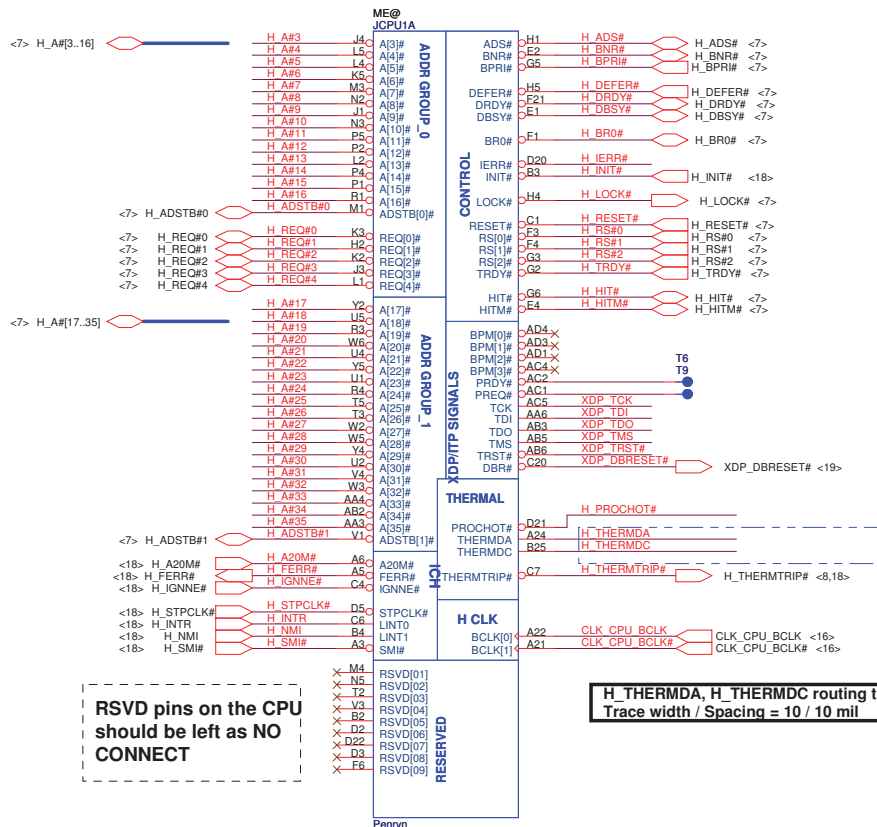
PCIe PORT LIST

PORT	DEVICE
1	LAN
2	
3	WLAN
4	
5	
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	
4	CARD READER
5	WIRELESS
6	BT
7	USB PORT (ESATA)
8	
9	
10	
11	
12	
13	

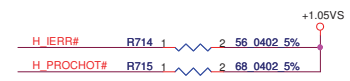
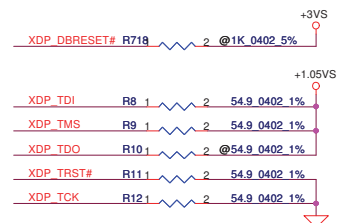
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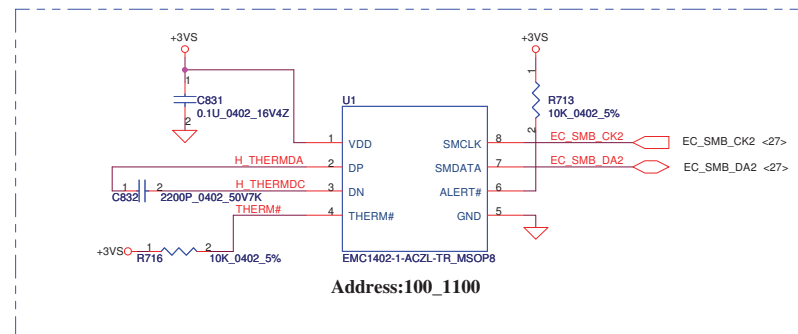
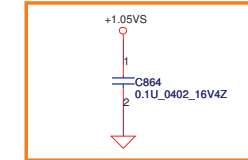
RSVD pins on the CPU should be left as NO CONNECT

H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil

XDP Reserve for debug , Please close to CPU side

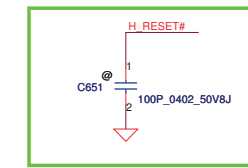


PVT ESD solution. Please close to R715



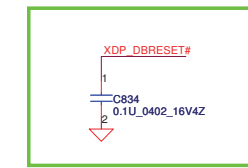
Address:100_1100

10/01 Add for reduce noise



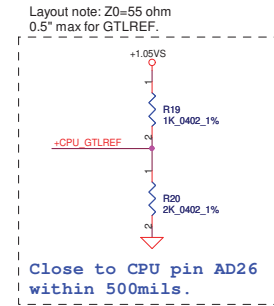
Place closely pin C1

09/16 Add C834 For ESD



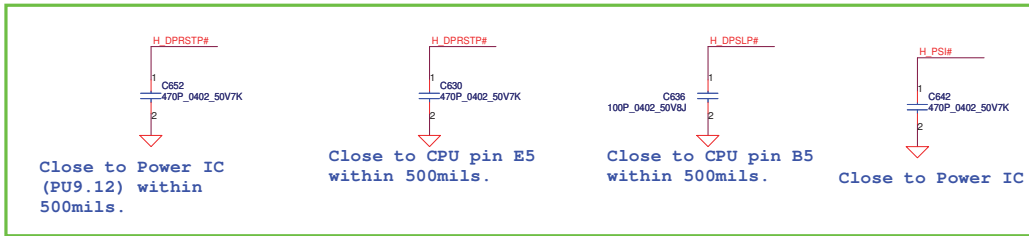
Place closely pin C20

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

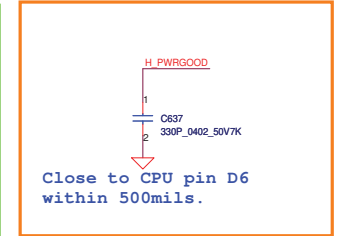


TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 5mils and Space 25mils (55Ohms)
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

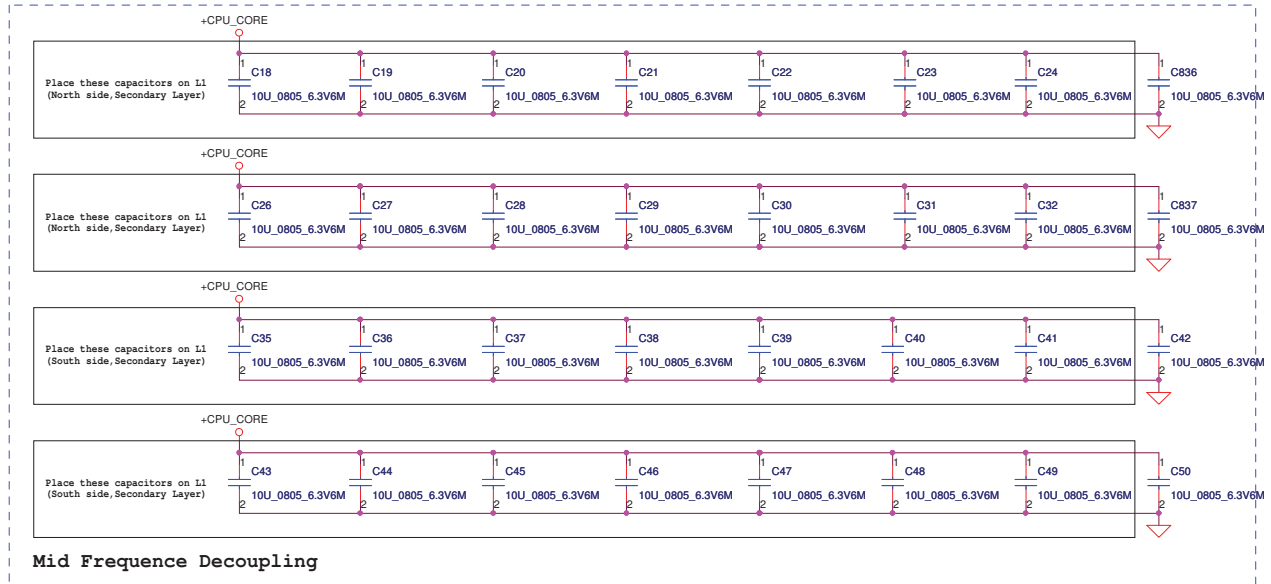
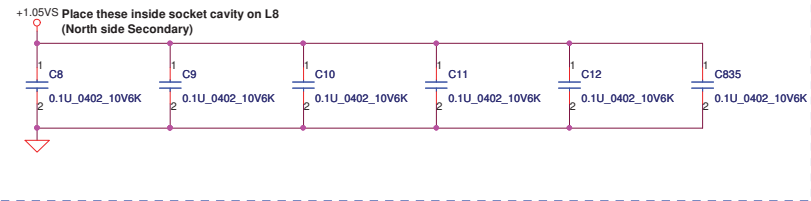
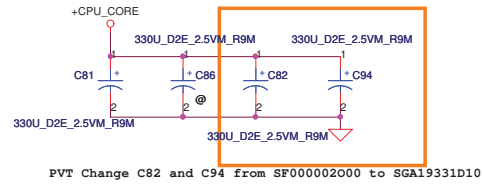
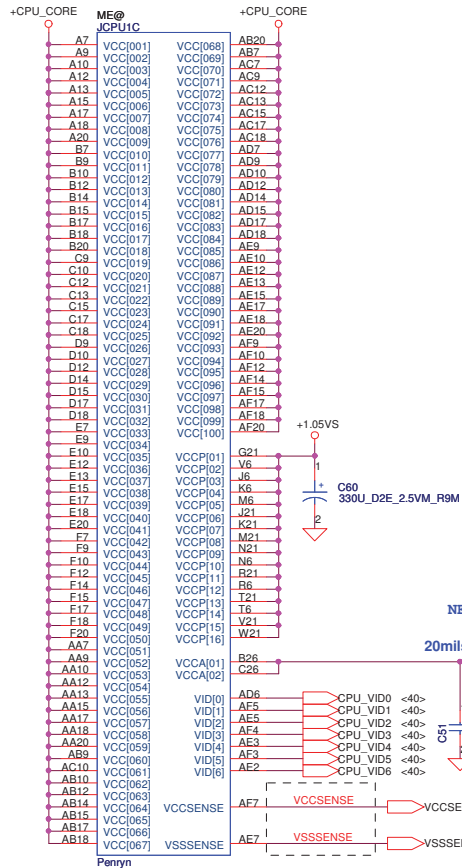
09/29 Add for power noise



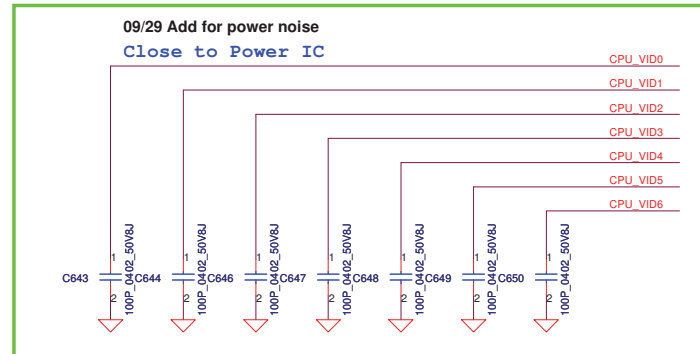
PVT for ESD solution



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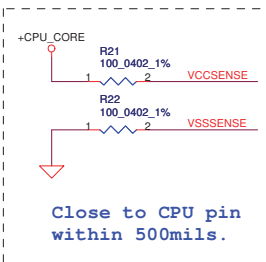


Mid Frequency Decoupling

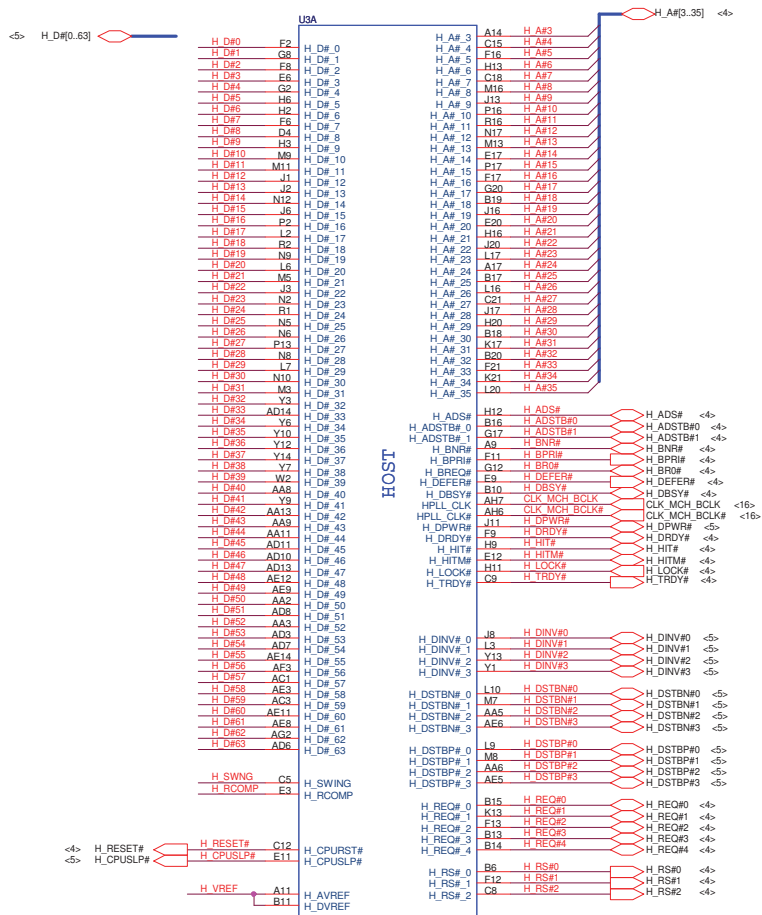


The trace width/space/other is 18/7/25.

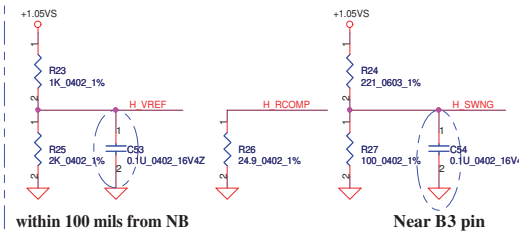
Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



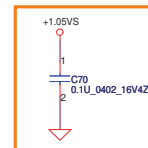
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Layout Note:
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20



PVT ESD solution.
Please close to R23



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<14> DDR_A_D[0..63]

U00
DDR A D0 AJ38 SA_DQ_0
DDR A D1 AJ41 SA_DQ_1
DDR A D2 AN38 SA_DQ_2
DDR A D3 AM38 SA_DQ_3
DDR A D4 AJ36 SA_DQ_4
DDR A D5 AJ40 SA_DQ_5
DDR A D6 AM44 SA_DQ_6
DDR A D7 AM42 SA_DQ_7
DDR A D8 AN43 SA_DQ_8
DDR A D9 AN44 SA_DQ_9
DDR A D10 AU40 SA_DQ_10
DDR A D11 AT38 SA_DQ_11
DDR A D12 AN41 SA_DQ_12
DDR A D13 AN39 SA_DQ_13
DDR A D14 AU44 SA_DQ_14
DDR A D15 AU42 SA_DQ_15
DDR A D16 AV39 SA_DQ_16
DDR A D17 AY44 SA_DQ_17
DDR A D18 BA40 SA_DQ_18
DDR A D19 BD43 SA_DQ_19
DDR A D20 AV41 SA_DQ_20
DDR A D21 AY43 SA_DQ_21
DDR A D22 BA41 SA_DQ_22
DDR A D23 BC40 SA_DQ_23
DDR A D24 AY37 SA_DQ_24
DDR A D25 BD38 SA_DQ_25
DDR A D26 AV37 SA_DQ_26
DDR A D27 AT36 SA_DQ_27
DDR A D28 AY38 SA_DQ_28
DDR A D29 BB38 SA_DQ_29
DDR A D30 AV36 SA_DQ_30
DDR A D31 AW36 SA_DQ_31
DDR A D32 BD13 SA_DQ_32
DDR A D33 AU11 SA_DQ_33
DDR A D34 BC11 SA_DQ_34
DDR A D35 BA12 SA_DQ_35
DDR A D36 AU13 SA_DQ_36
DDR A D37 AV13 SA_DQ_37
DDR A D38 BD12 SA_DQ_38
DDR A D39 BC12 SA_DQ_39
DDR A D40 BB9 SA_DQ_40
DDR A D41 BA9 SA_DQ_41
DDR A D42 AU10 SA_DQ_42
DDR A D43 AV9 SA_DQ_43
DDR A D44 BA11 SA_DQ_44
DDR A D45 BD9 SA_DQ_45
DDR A D46 AY8 SA_DQ_46
DDR A D47 BA6 SA_DQ_47
DDR A D48 AV9 SA_DQ_48
DDR A D49 AV7 SA_DQ_49
DDR A D50 AT9 SA_DQ_50
DDR A D51 AN8 SA_DQ_51
DDR A D52 AU5 SA_DQ_52
DDR A D53 AU6 SA_DQ_53
DDR A D54 AT5 SA_DQ_54
DDR A D55 AN10 SA_DQ_55
DDR A D56 AM11 SA_DQ_56
DDR A D57 AM6 SA_DQ_57
DDR A D58 AJ9 SA_DQ_58
DDR A D59 AJ8 SA_DQ_59
DDR A D60 AN12 SA_DQ_60
DDR A D61 AM13 SA_DQ_61
DDR A D62 AJ11 SA_DQ_62
DDR A D63 AJ12 SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0
SA_BS_1
SA_BS_2
SA_RAS#
SA_CAS#
SA_WE#
SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7
SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7
SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7
SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21 DDR A BS0
BG18 DDR A BS1
AT25 DDR A BS2
BB20 DDR A RAS#
BD20 DDR A CAS#
AY20 DDR A WE#

AM37 DDR A DM0
AT41 DDR A DM1
AY41 DDR A DM2
AU39 DDR A DM3
BD12 DDR A DM4
AY3 DDR A DM5
AT7 DDR A DM6
AJ5 DDR A DM7

AJ44 DDR A DQS0
AT44 DDR A DQS1
BA43 DDR A DQS2
BC37 DDR A DQS3
AW12 DDR A DQS4
BC8 DDR A DQS5
AJ8 DDR A DQS6
AM7 DDR A DQS7

AJ43 DDR A DQS#0
AT43 DDR A DQS#1
BA44 DDR A DQS#2
BD37 DDR A DQS#3
AY12 DDR A DQS#4
BD8 DDR A DQS#5
AJ9 DDR A DQS#6
AM8 DDR A DQS#7

BA21 DDR A MA0
BC24 DDR A MA1
BG24 DDR A MA2
BH24 DDR A MA3
BG35 DDR A MA4
BA24 DDR A MA5
BD24 DDR A MA6
BG27 DDR A MA7
BF25 DDR A MA8
AW24 DDR A MA9
BC21 DDR A MA10
BG26 DDR A MA11
BH26 DDR A MA12
BH17 DDR A MA13
AY25 DDR A MA14

CANTIGA ES_FCBGA1329
GM45@

<14x15> DDR_B_D[0..63]

U00
DDR B D0 AK47 SB_DQ_0
DDR B D1 AH46 SB_DQ_1
DDR B D2 AP47 SB_DQ_2
DDR B D3 AP46 SB_DQ_3
DDR B D4 AJ46 SB_DQ_4
DDR B D5 AJ48 SB_DQ_5
DDR B D6 AM48 SB_DQ_6
DDR B D7 AP46 SB_DQ_7
DDR B D8 AU47 SB_DQ_8
DDR B D9 AU46 SB_DQ_9
DDR B D10 BA48 SB_DQ_10
DDR B D11 AY48 SB_DQ_11
DDR B D12 AT47 SB_DQ_12
DDR B D13 BA47 SB_DQ_13
DDR B D14 SA47 SB_DQ_14
DDR B D15 BC47 SB_DQ_15
DDR B D16 BC46 SB_DQ_16
DDR B D17 BC44 SB_DQ_17
DDR B D18 BC43 SB_DQ_18
DDR B D19 BF43 SB_DQ_19
DDR B D20 BE45 SB_DQ_20
DDR B D21 BC41 SB_DQ_21
DDR B D22 BF40 SB_DQ_22
DDR B D23 BF41 SB_DQ_23
DDR B D24 BC38 SB_DQ_24
DDR B D25 BF38 SB_DQ_25
DDR B D26 BH35 SB_DQ_26
DDR B D27 BC35 SB_DQ_27
DDR B D28 BH40 SB_DQ_28
DDR B D29 BG39 SB_DQ_29
DDR B D30 BC34 SB_DQ_30
DDR B D31 BH34 SB_DQ_31
DDR B D32 BH14 SB_DQ_32
DDR B D33 BH12 SB_DQ_33
DDR B D34 BH11 SB_DQ_34
DDR B D35 BG8 SB_DQ_35
DDR B D36 BH12 SB_DQ_36
DDR B D37 BF11 SB_DQ_37
DDR B D38 BF8 SB_DQ_38
DDR B D39 BG7 SB_DQ_39
DDR B D40 BC5 SB_DQ_40
DDR B D41 BC6 SB_DQ_41
DDR B D42 AY3 SB_DQ_42
DDR B D43 AY1 SB_DQ_43
DDR B D44 BF6 SB_DQ_44
DDR B D45 BF5 SB_DQ_45
DDR B D46 BA1 SB_DQ_46
DDR B D47 BC3 SB_DQ_47
DDR B D48 AV2 SB_DQ_48
DDR B D49 AU3 SB_DQ_49
DDR B D50 AR3 SB_DQ_50
DDR B D51 AN2 SB_DQ_51
DDR B D52 AY2 SB_DQ_52
DDR B D53 AV1 SB_DQ_53
DDR B D54 AP2 SB_DQ_54
DDR B D55 AR1 SB_DQ_55
DDR B D56 AL1 SB_DQ_56
DDR B D57 AL2 SB_DQ_57
DDR B D58 AJ1 SB_DQ_58
DDR B D59 AH1 SB_DQ_59
DDR B D60 AM2 SB_DQ_60
DDR B D61 AM6 SB_DQ_61
DDR B D62 AH3 SB_DQ_62
DDR B D63 AJ3 SB_DQ_63

DDR SYSTEM MEMORY B

BC16 DDR B BS0
BB17 DDR B BS1
BB33 DDR B BS2
AU17 DDR B RAS#
BG16 DDR B CAS#
BF14 DDR B WE#

AM47 DDR B DM0
AY47 DDR B DM1
BD40 DDR B DM2
BF35 DDR B DM3
BG11 DDR B DM4
BA3 DDR B DM5
AP1 DDR B DM6
AK2 DDR B DM7

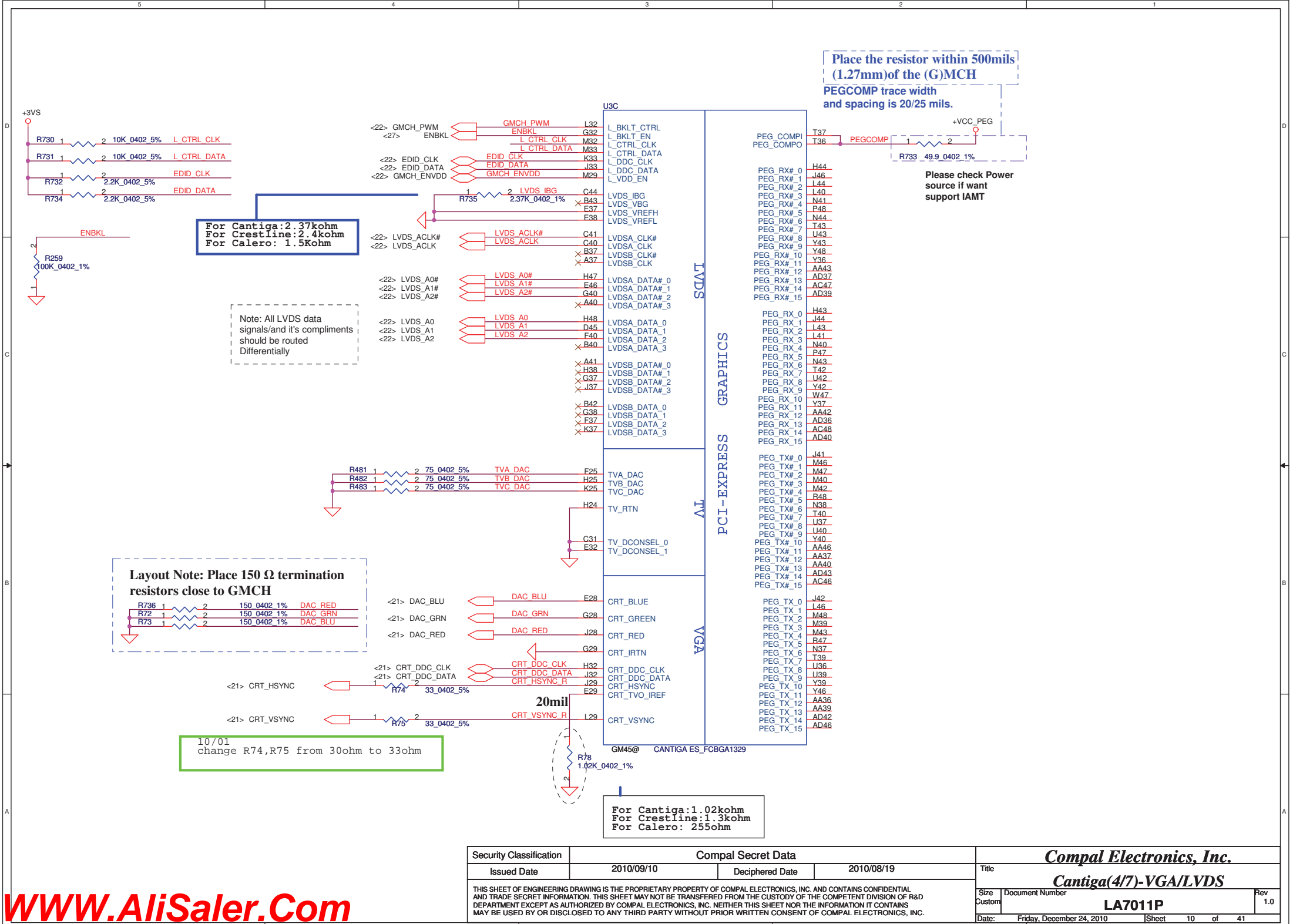
AL47 DDR B DQS0
AV48 DDR B DQS1
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BH9 DDR B DQS4
BB2 DDR B DQS5
AU11 DDR B DQS6
AN6 DDR B DQS7

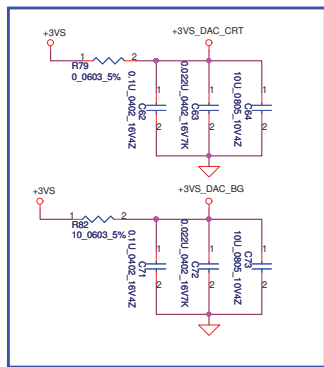
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AV47 DDR B DQS#1
BH4 DDR B DQS#2
BH7 DDR B DQS#3
BG9 DDR B DQS#4
BC2 DDR B DQS#5
AT2 DDR B DQS#6
AN5 DDR B DQS#7

AV17 DDR B MA0
BA25 DDR B MA1
BC25 DDR B MA2
AU25 DDR B MA3
AW25 DDR B MA4
BB28 DDR B MA5
AU28 DDR B MA6
AW28 DDR B MA7
AT33 DDR B MA8
BD33 DDR B MA9
BB16 DDR B MA10
AW33 DDR B MA11
AY33 DDR B MA12
BH15 DDR B MA13
AU33 DDR B MA14

CANTIGA ES_FCBGA1329
GM45@

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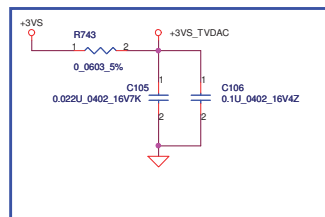




VCCA_CRT_DAC: 73mA (0.1UF*1, 0.01UF*1)
VCCA_DAC_BG: 2.68mA (0.1UF*1, 0.01UF*1)

VCCA_SM: 720mA (22UF*2, 4.7UF*1, 1UF*1)

VCCA_SM_CK: 220mA (22UF*1, 2.2UF*1, 0.1UF*1)



+3V5V_TV_DAC: 40mA (0.1UF*1, 0.01UF*1 for each DAC)

+3V5V_TV_DAC_2: 79mA

+1.5V5V_TV_DAC: 3.5mA

+1.5V5V_TV_DAC_2: 1mA

+1.5V5V_TV_DAC_3: 1.57, 2mA

+1.5V5V_TV_DAC_4: 0mA

+1.5V5V_TV_DAC_5: 0mA

+1.5V5V_TV_DAC_6: 0mA

+1.5V5V_TV_DAC_7: 0mA

+1.5V5V_TV_DAC_8: 0mA

+1.5V5V_TV_DAC_9: 0mA

+1.5V5V_TV_DAC_10: 0mA

+1.5V5V_TV_DAC_11: 0mA

+1.5V5V_TV_DAC_12: 0mA

+1.5V5V_TV_DAC_13: 0mA

+1.5V5V_TV_DAC_14: 0mA

+1.5V5V_TV_DAC_15: 0mA

+1.5V5V_TV_DAC_16: 0mA

+1.5V5V_TV_DAC_17: 0mA

+1.5V5V_TV_DAC_18: 0mA

+1.5V5V_TV_DAC_19: 0mA

+1.5V5V_TV_DAC_20: 0mA

+1.5V5V_TV_DAC_21: 0mA

+1.5V5V_TV_DAC_22: 0mA

+1.5V5V_TV_DAC_23: 0mA

+1.5V5V_TV_DAC_24: 0mA

+1.5V5V_TV_DAC_25: 0mA

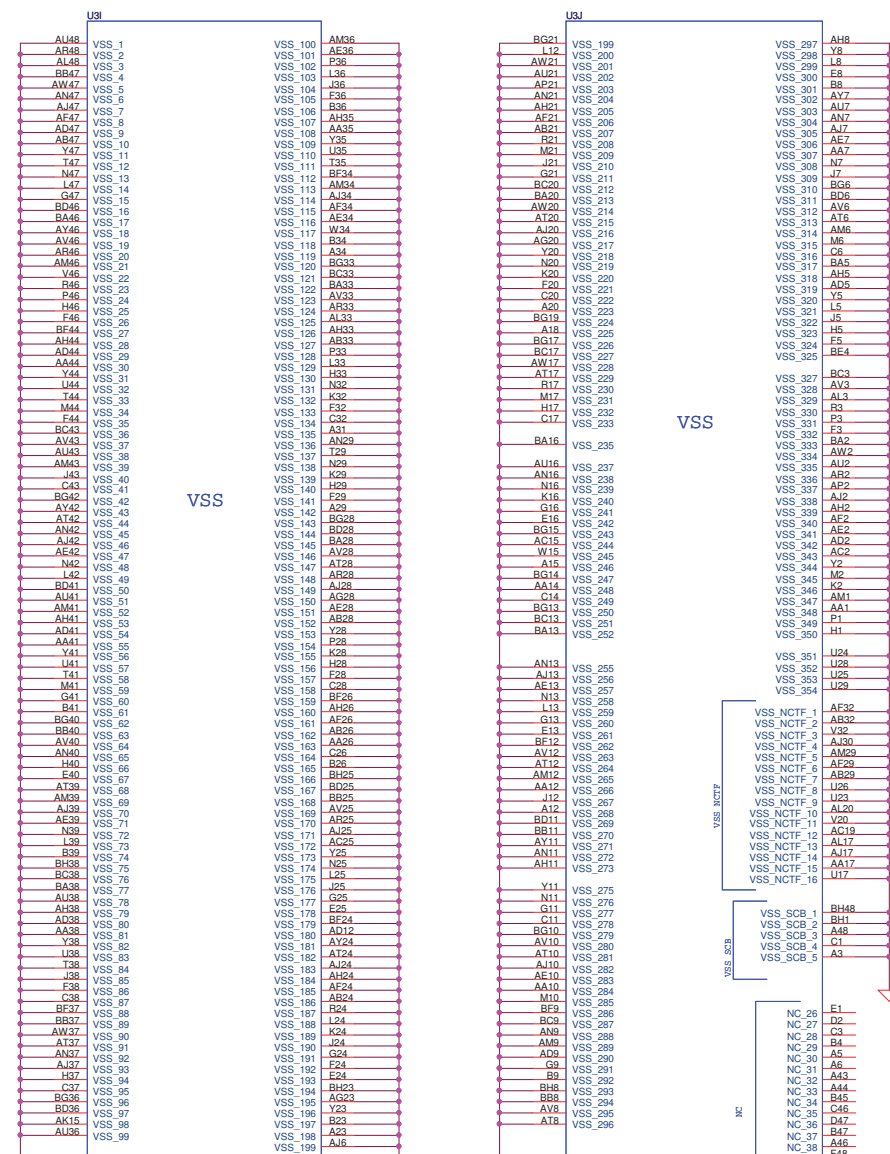
+1.5V5V_TV_DAC_26: 0mA

+1.5V5V_TV_DAC_27: 0mA

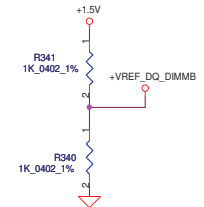
+1.5V5V_TV_DAC_28: 0mA

+1.5V5V_TV_DAC_29: 0mA

+1.5V5V_TV_DAC_30: 0mA



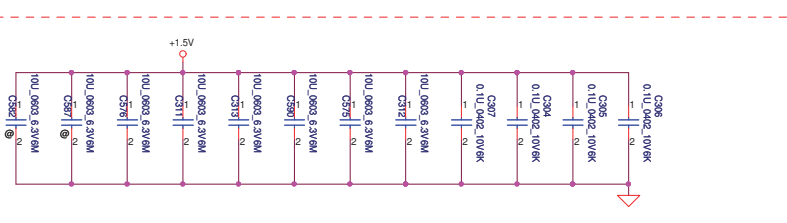
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2010/09/10		2010/08/19		Cantiga(7/7)-GND	
Size		Document Number		Rev	
Custom		LA7011P		1.0	
Date:		Friday, December 24, 2010		Sheet 13 of 41	



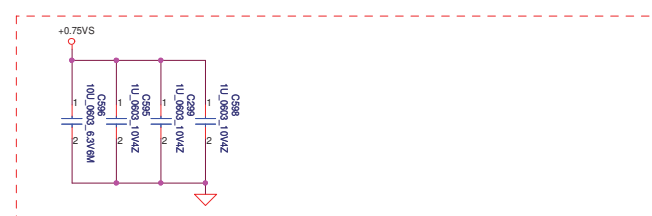
07/17/2009

A schematic diagram showing a capacitor labeled C640. The capacitor is represented by two parallel horizontal lines. The top terminal is labeled '1' and is connected to a red line labeled 'SM_DRAMRST#'. The bottom terminal is labeled '2' and is connected to a red triangle symbol representing ground. The capacitor value '100P_0402_50V8J' is written next to the capacitor symbol.

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



```
VDDQ(1.5V) =
    3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
    6*0603 10uf (PER CONNECTOR)

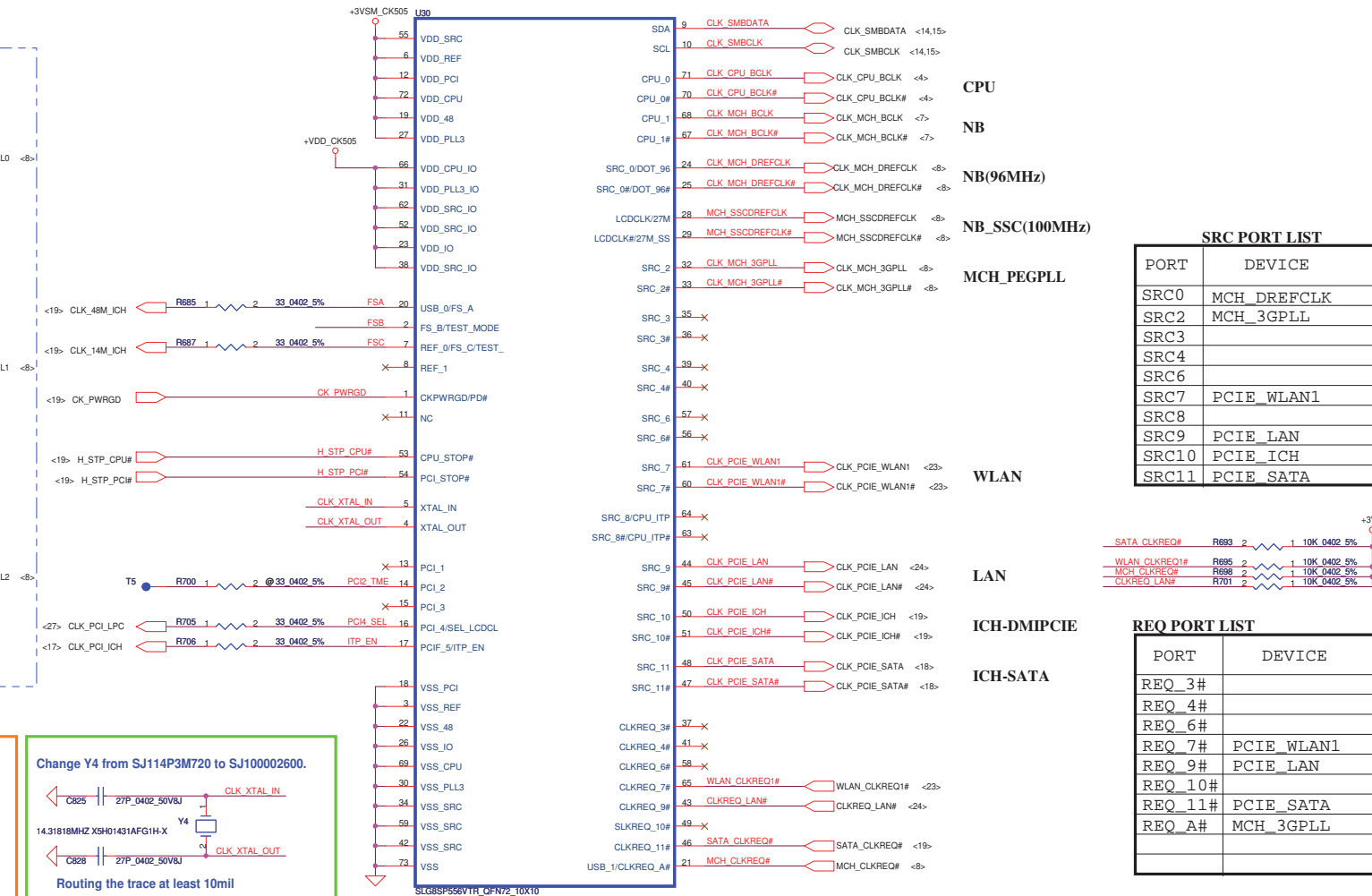
VTT(0.75V) =
    3*0805 10uf    4*0402 1uf

    1*0402 0.1uf    1*0402 2.2uf

VDDSPD (3.3V) =
    1*0402 0.1uf    1*0402 2.2uf
```

DDR3 SO-DIMM A H=8mm Reverse type

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PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST	
PORT	DEVICE
REQ_3#	
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

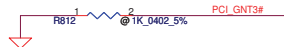
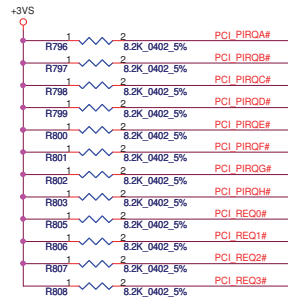
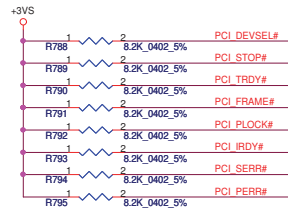
The diagram shows a vertical red line representing a signal trace. At the top, it is connected to a red circle labeled '+3VS'. The trace is labeled '1' at the top and '2' at the bottom. A horizontal blue line, representing a resistor, is connected to the trace between points 1 and 2. The resistor is labeled 'C657' and '470P_0402_50V7K'. The trace ends at a red triangle pointing downwards, representing ground.

Change Y4 from SJ114P3M720 to SJ100002600.

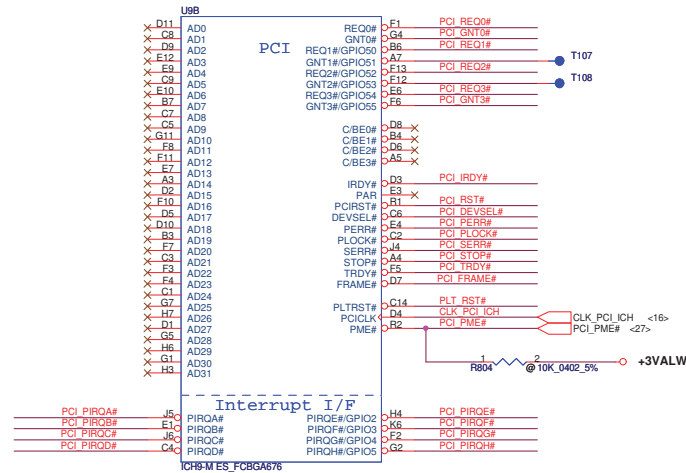
14.31818MHZ XSH01431AFG1H-X

Routing the trace at least 10mil

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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Clock Generator CK505 Title		
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A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

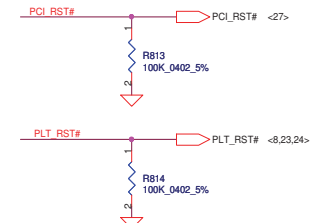
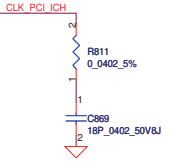


Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

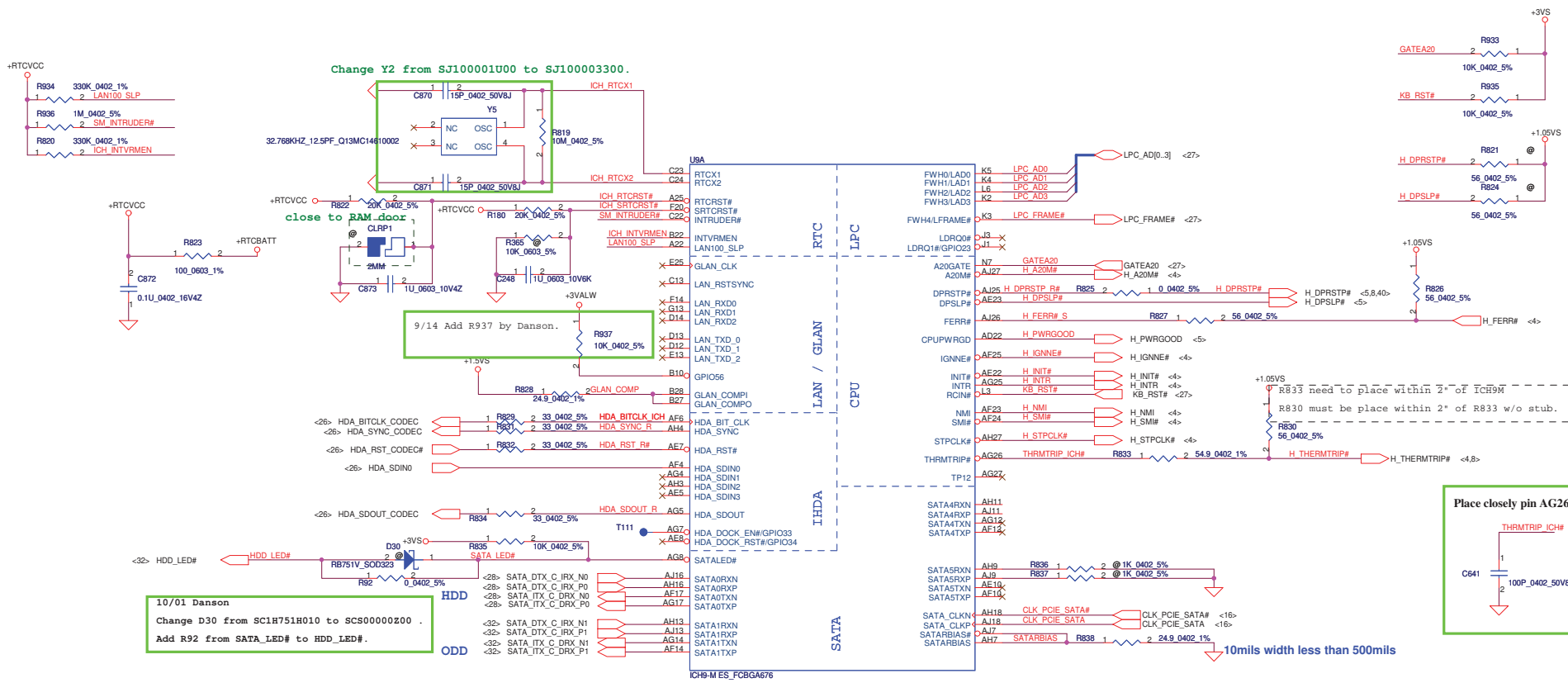
09/16 Add C858 For ESD
Place closely pin C14



Place closely pin D4



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Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	ICH9M(1/4)-PCI
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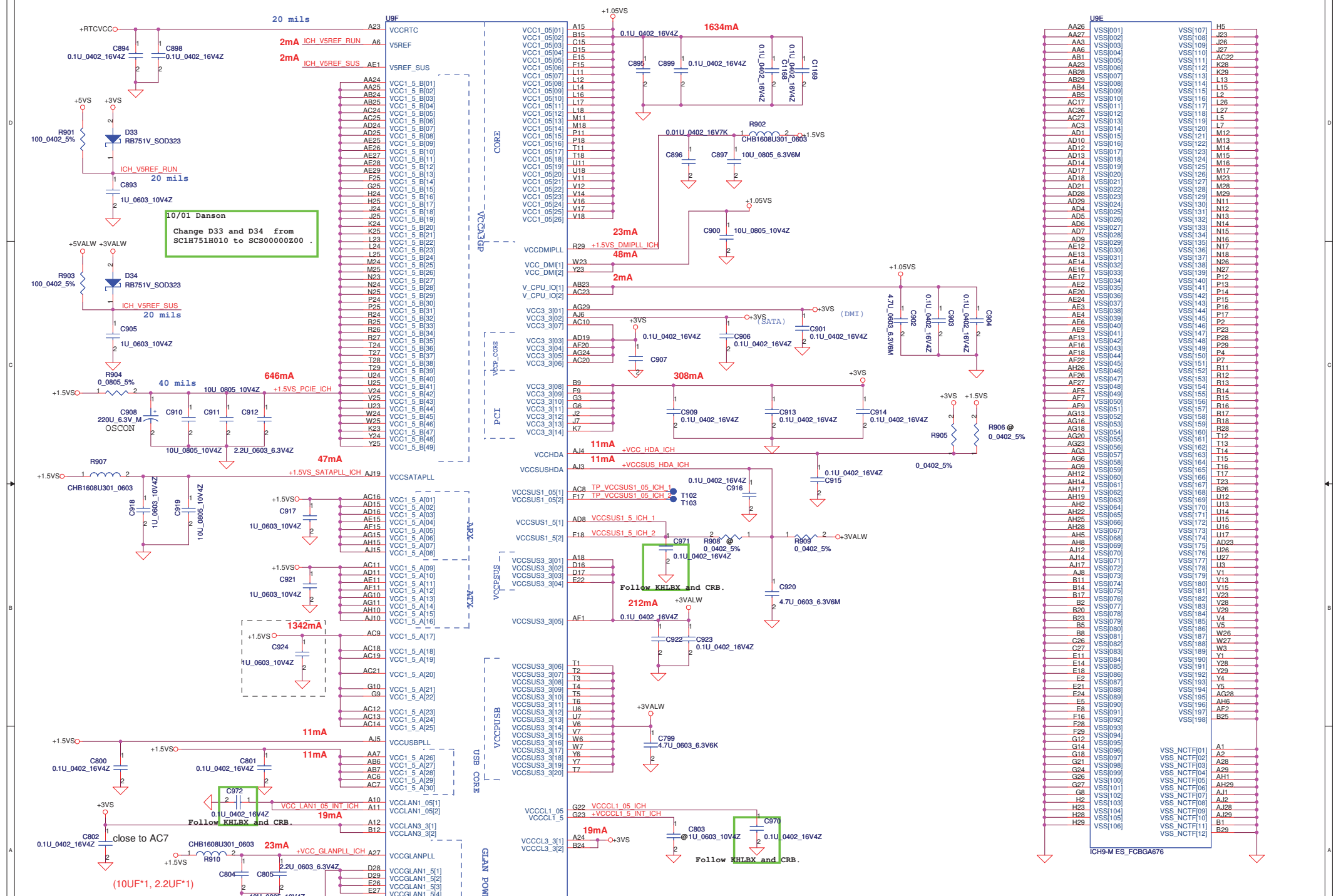


Flash Descriptor Security Override Strap	
GPIO33	Low= Descriptor Security override High= Default* (Internal pull-up)

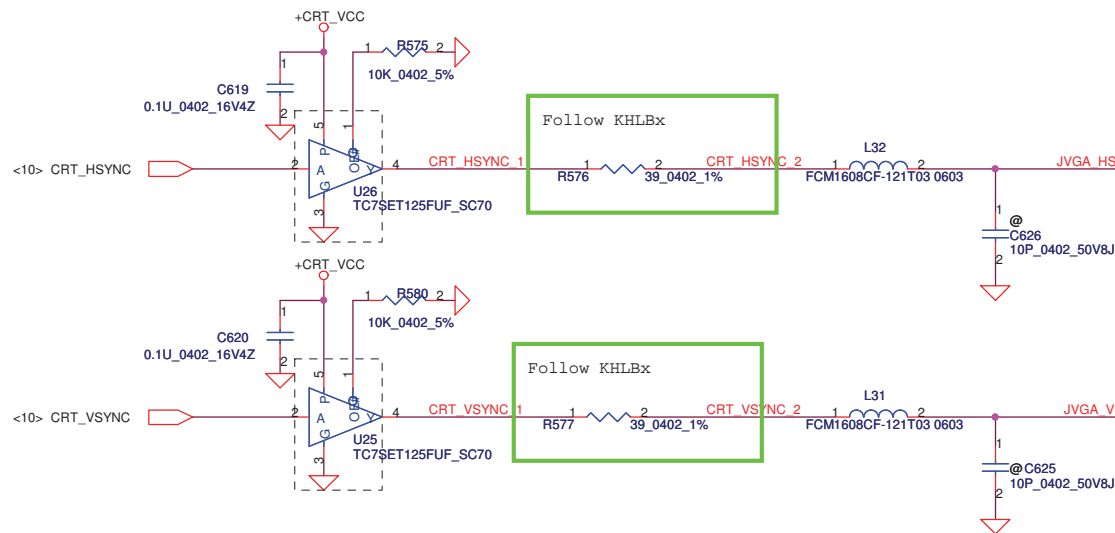
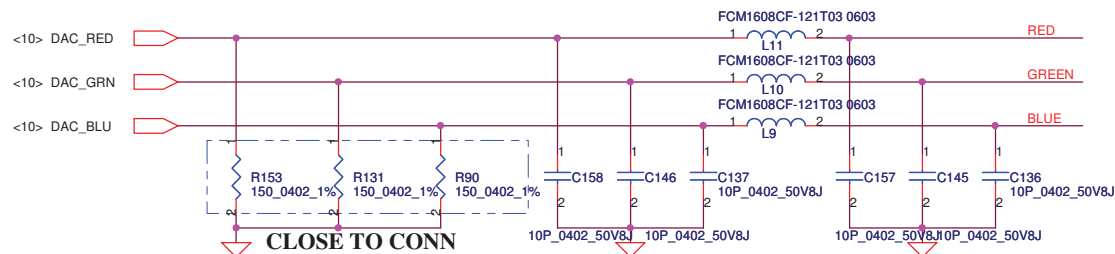
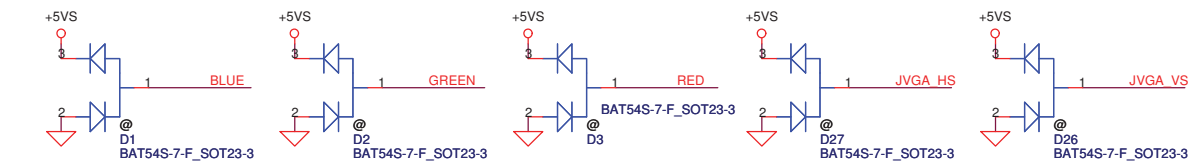
SATA PORT LIST	
PORT	DEVICE
0	HDD
1	ODD
4	
5	

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	Title	ICH9M(2/4)-LAN,ATA,LPC,RTC
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				LA7011P	
				Date	Friday, December 24, 2010
				Sheet	18 of 41

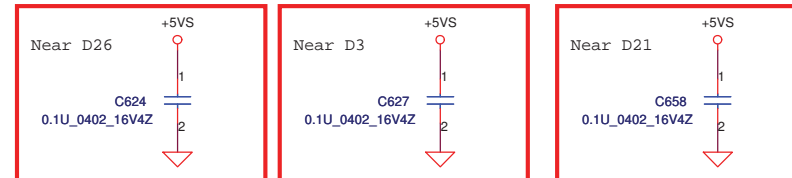




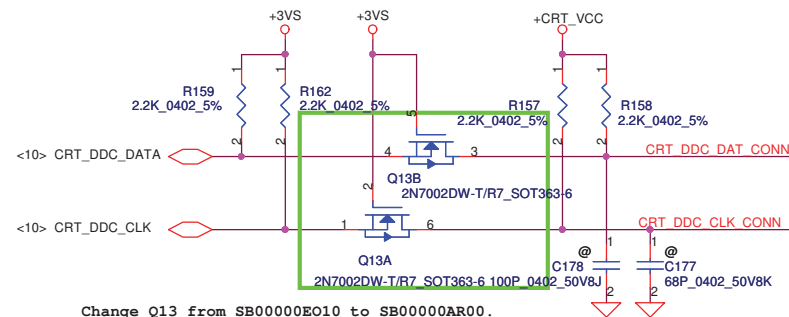
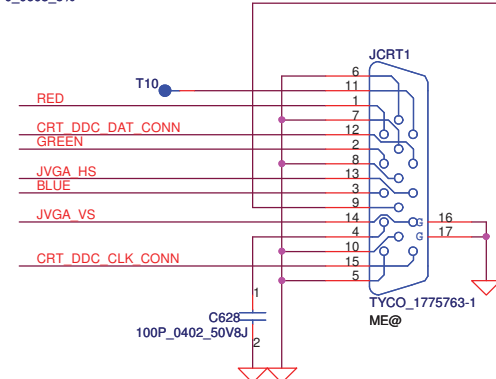
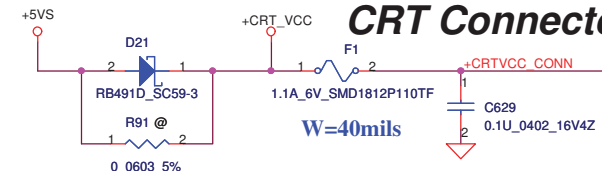
Security Classification		Compal Secret Data		Title	
Issued Date	2010/09/10	Deciphered Date	2010/08/19	ICH9M(4/4)-POWER&GND	
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Pre MP ADD for ESD solution

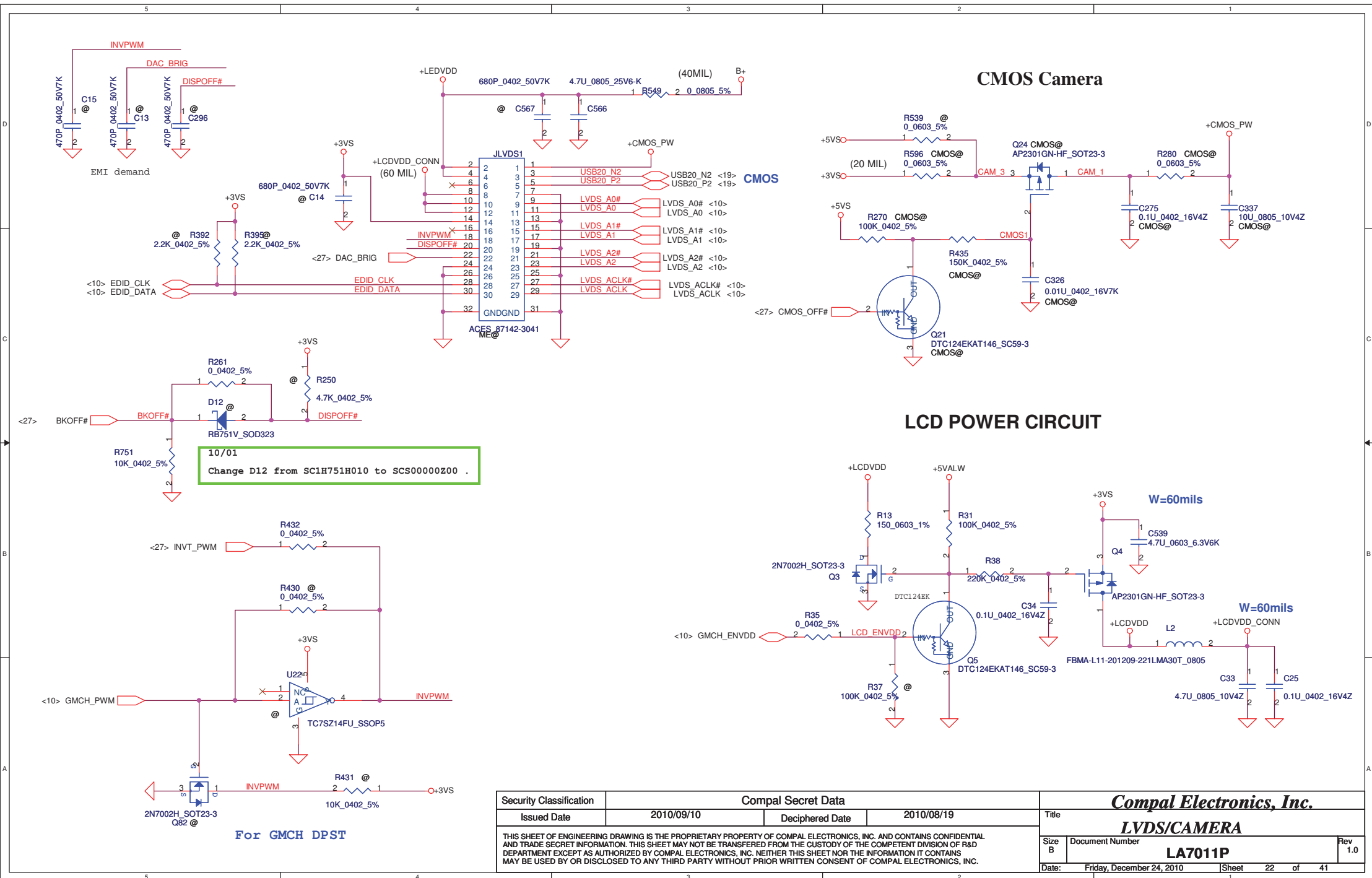


CRT Connector



Change Q13 from SB00000EO10 to SB00000AR00.

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						Size B	Document Number			LA7011P		Rev 1.0
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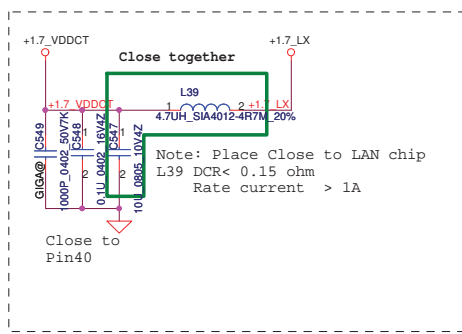
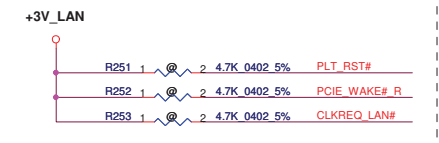
A	B	C	D	E
---	---	---	---	---

4



Atheros request can't disable LAN power

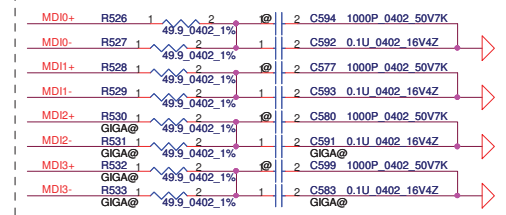
Atheros request reserve



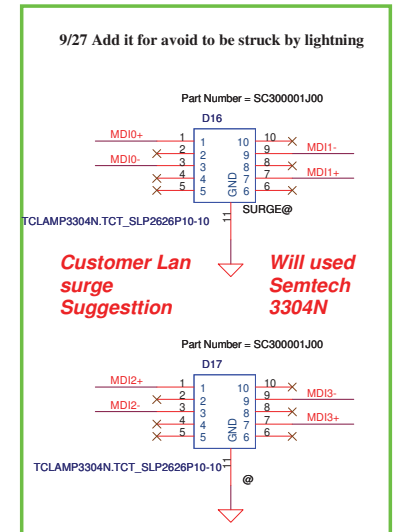
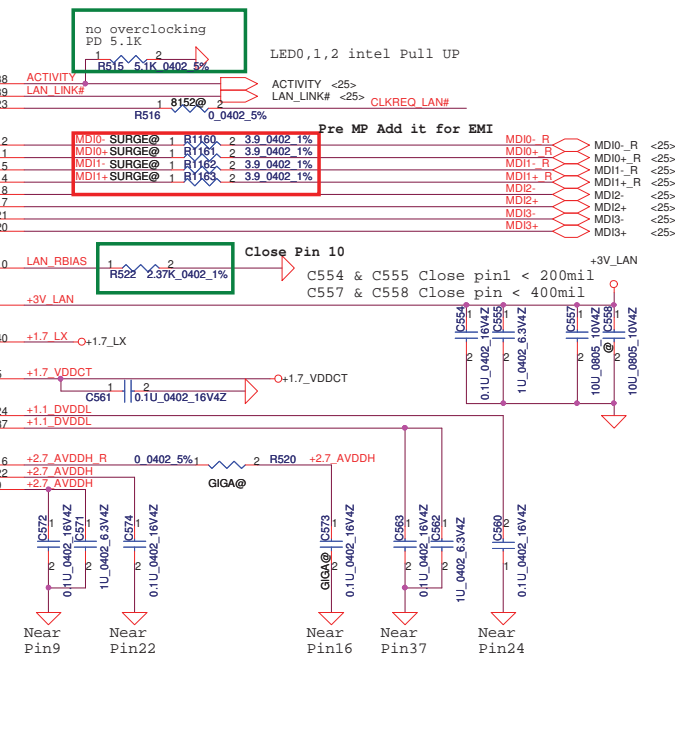
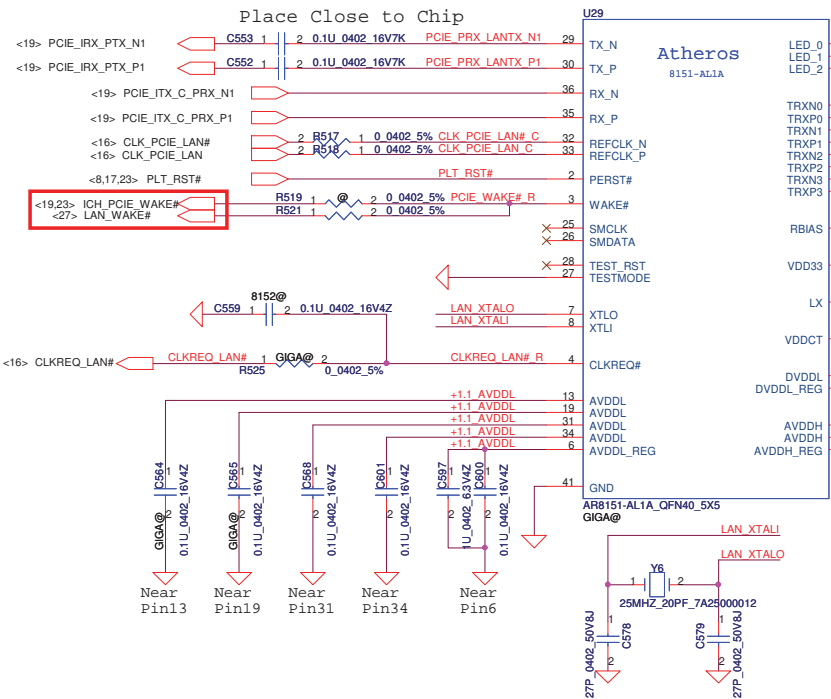
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED1	H:SWR Switch mode regulator Select AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	---

Place Close to LAN chip



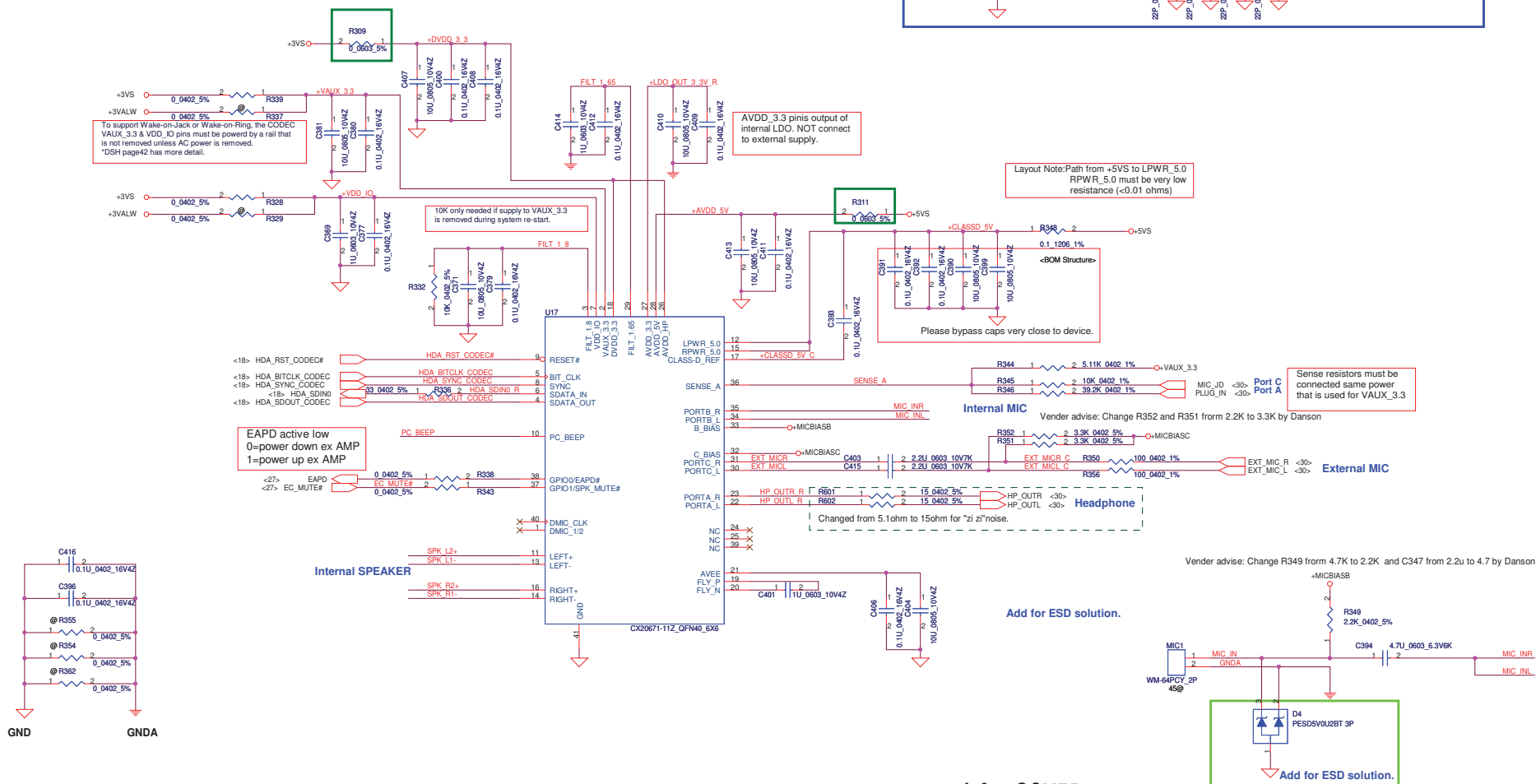
Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap
Note 2 : C594, C577, C580, C599, reserved for EMI.



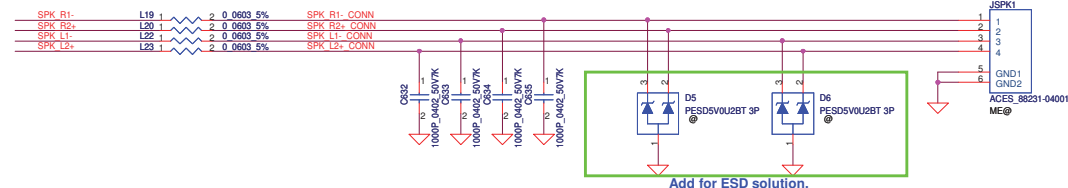
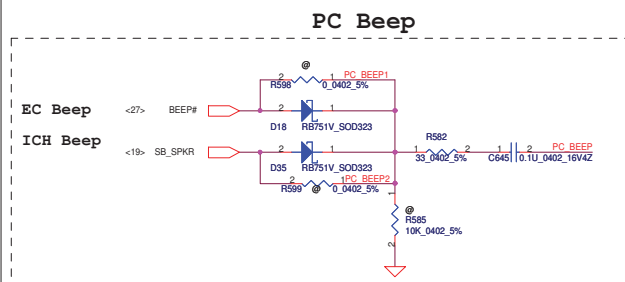
	Pin4	Configure	Pin23	Configure
AR8152	VDDCT_REG	*	CLKREQn	*
AR8151	CLKREQn	*	LED[2]	

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Issued Date	2010/09/10	Deciphered Date	2010/08/19	
Title				LAN-AR8151/8152
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CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



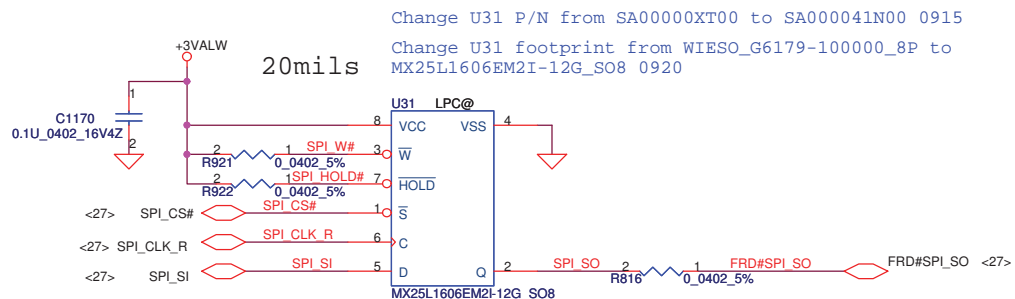
wide 20MIL



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					Size C	Document Number	New
					LA7011P		
Date: Friday, December 24, 2010					Sheet	26 of 41	

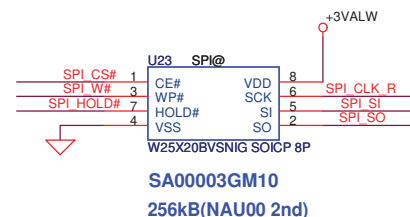
SPI Flash (16Mb*1)

FOR EC 16M SPI ROM

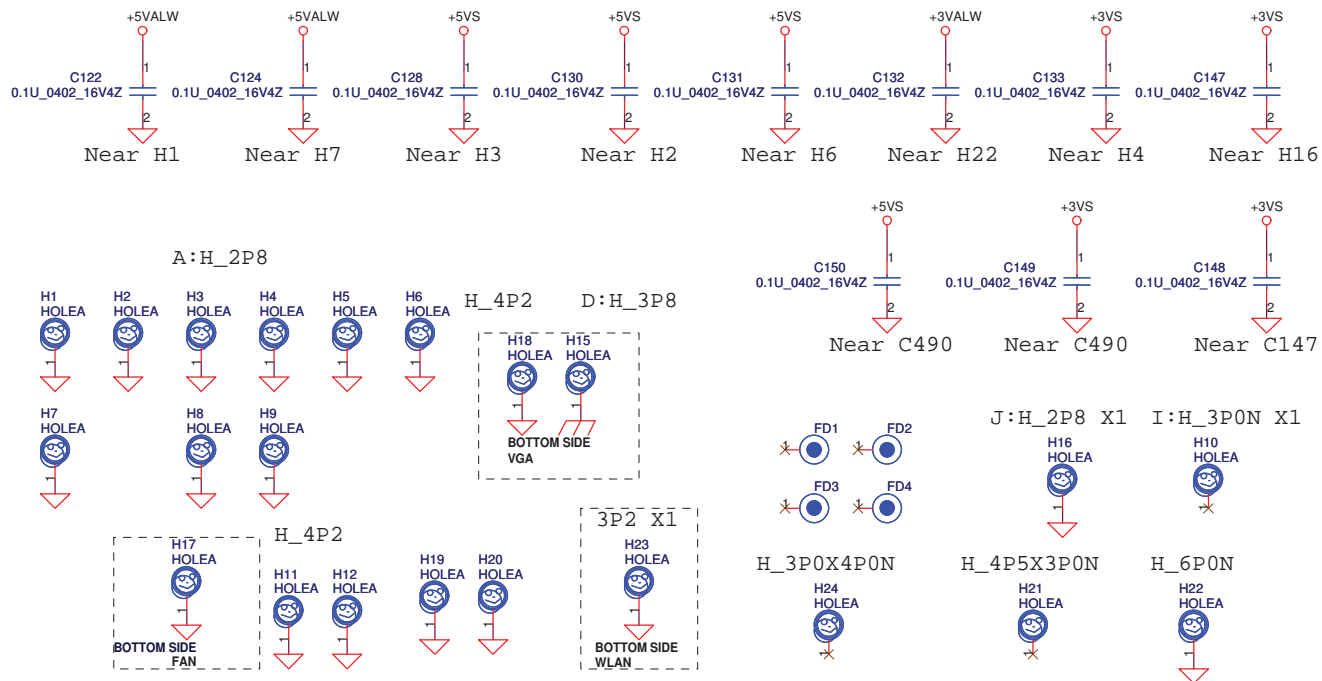
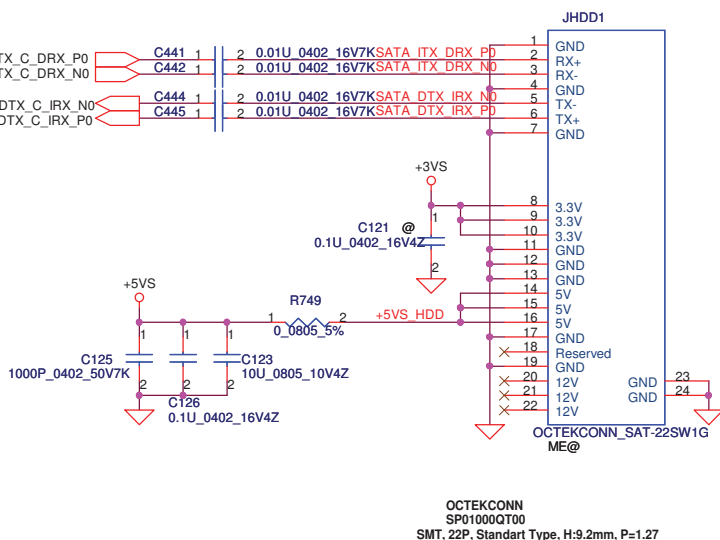


FOR EC 256K SPI ROM (NONShare ROM)

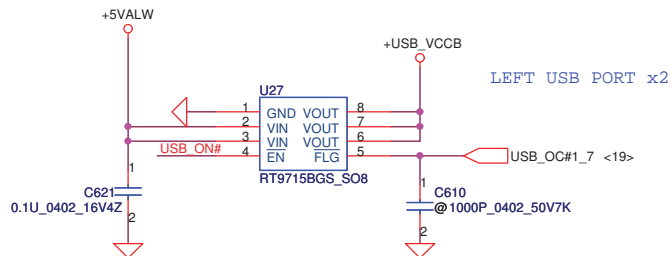
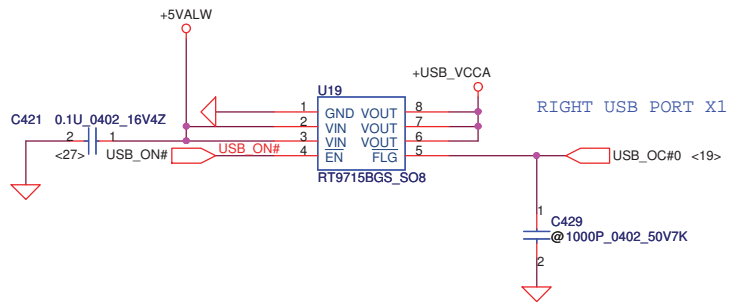
2010/09/24 Add U23 for NONShare SPI ROM.



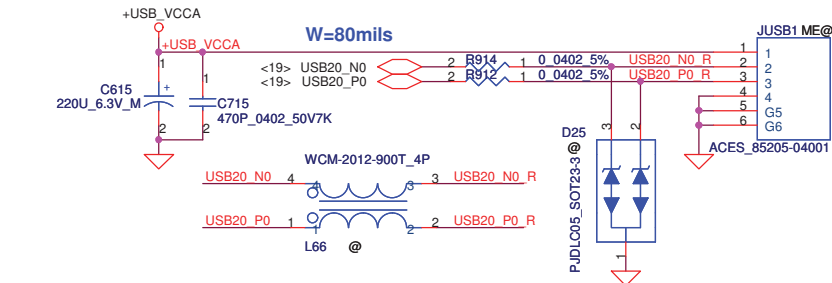
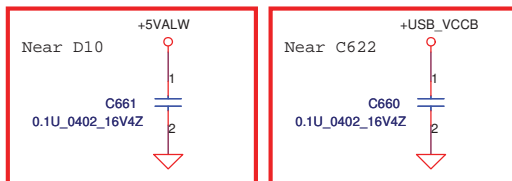
SATA HDD Conn.



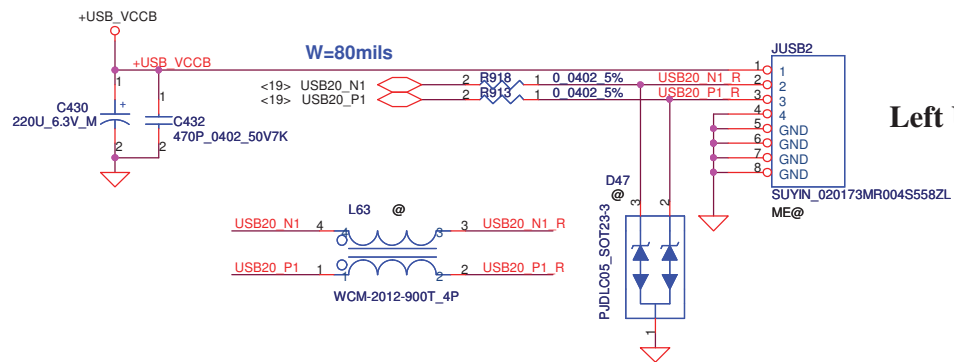
PVT Change U19 and U27 part number from SA000039E00 to SA00002XX00



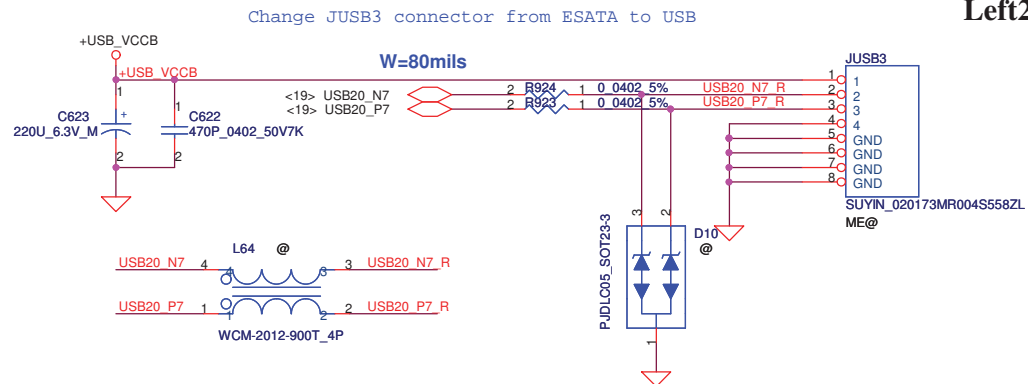
Pre MP ADD for ESD solution



Right USB Conn.



Left USB Conn.



Left2 USB Conn.

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Power Button

TOP Side

Bottom Side

SW1

SMT1-05_4P

+3VALW

R272
100K_0402_5%

J5

SHORT PADS

D14

DAN202UT106_SC70-3

ON/OFFBTN#

ON/OFF#

ON#

D15
RLZ20A_LL34

C356
1000P_0402_50V7K

Q28
2N7002H_SOT23-3

R302
10K_0402_5%

EC_ON

<27,37>

<27>

<34>

BT MODULE CONN

The schematic diagram illustrates the internal circuitry of the BT module and its connections. Key components include:

- Transistors:** Q31 (DTC124EKAT146_SC59-3) and Q32 (AP2301GN-HF_SOT23-3).
- Resistors:** R304 (100K_0402_5%), R616 (100K_0402_5%), R583 (0_0603_5%).
- Capacitors:** C353 (0.1U_0402_16V4Z), C354 (0.1U_0402_16V4Z).
- Power Supply:** +5VALV, +3VS, +3VS_BT.
- Control Signals:** BT_OFF# (pin 2), BT_LED# (pin 3).
- Data Signals:** USB20_P6 (pin 19), USB20_N6 (pin 19), BT_ACTIVE (pin 23).
- BT Module Pins:** 1 (+5VALV), 2 (BT_OFF#), 3 (BT_LED#), 4 (BT@), 5 (BT@), 6 (BT@), 7 (BT@), 8 (BT@), 9 (BT@), 10 (BT@), 11 (BT@), 12 (BT@), 13 (BT@), 14 (BT@), 15 (BT@), 16 (BT@), 17 (BT@), 18 (BT@), 19 (BT@), 20 (BT@), 21 (BT@), 22 (BT@), 23 (BT@), 24 (BT@), 25 (BT@), 26 (BT@), 27 (BT@), 28 (BT@), 29 (BT@), 30 (BT@), 31 (BT@), 32 (BT@), 33 (BT@), 34 (BT@), 35 (BT@), 36 (BT@), 37 (BT@), 38 (BT@), 39 (BT@), 40 (BT@), 41 (BT@), 42 (BT@), 43 (BT@), 44 (BT@), 45 (BT@), 46 (BT@), 47 (BT@), 48 (BT@), 49 (BT@), 50 (BT@), 51 (BT@), 52 (BT@), 53 (BT@), 54 (BT@), 55 (BT@), 56 (BT@), 57 (BT@), 58 (BT@), 59 (BT@), 60 (BT@), 61 (BT@), 62 (BT@), 63 (BT@), 64 (BT@), 65 (BT@), 66 (BT@), 67 (BT@), 68 (BT@), 69 (BT@), 70 (BT@), 71 (BT@), 72 (BT@), 73 (BT@), 74 (BT@), 75 (BT@), 76 (BT@), 77 (BT@), 78 (BT@), 79 (BT@), 80 (BT@), 81 (BT@), 82 (BT@), 83 (BT@), 84 (BT@), 85 (BT@), 86 (BT@), 87 (BT@), 88 (BT@), 89 (BT@), 90 (BT@), 91 (BT@), 92 (BT@), 93 (BT@), 94 (BT@), 95 (BT@), 96 (BT@), 97 (BT@), 98 (BT@), 99 (BT@), 100 (BT@).

Diagram illustrating the pin connections for JPWRB1:

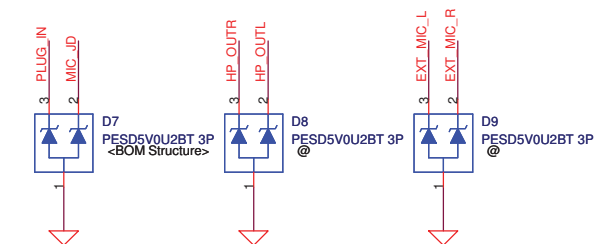
- Pin 1: +5VALW
- Pin 2: <27,32> PWR_LED#
- Pin 3: NOVO_BTN#
- Pin 4: ON/OFFBTN#
- Pin 5: GND
- Pin 6: GND
- Pin 7: GND
- Pin 8: GND

ACES_85201-0605N
ME@

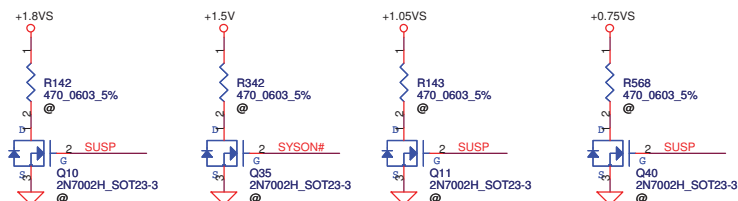
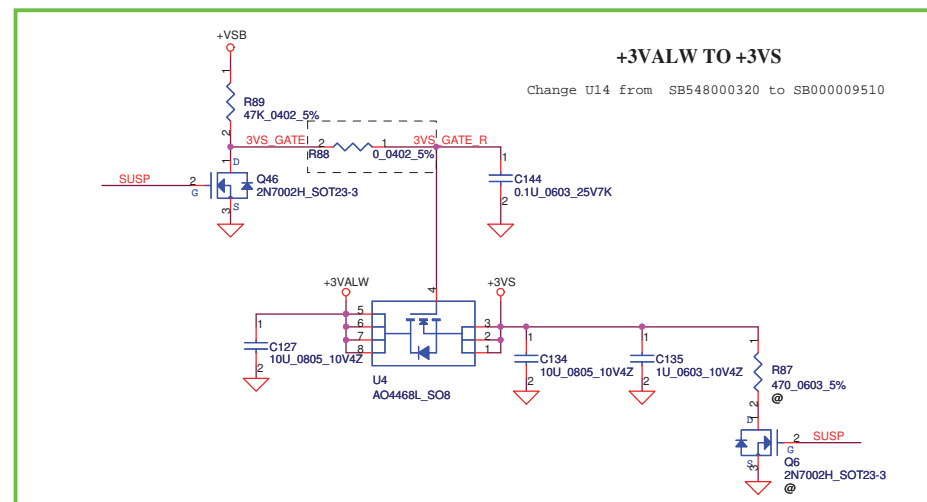
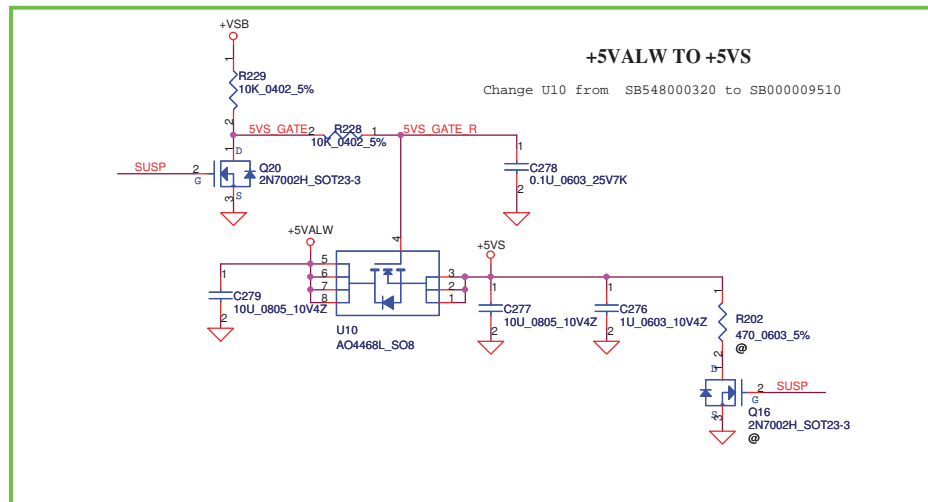
The schematic diagram illustrates the LED driver circuit. It features three 0.1uF capacitors (C360, C361, C365) connected to a +5VALW supply. The output of C360 is connected to the NOVO_BTN# pin. The output of C361 is connected to the ON/OFFBTN# pin. The output of C365 is connected to the PWR_LED# pin. The PWR_LED# pin is also connected to the D49 AZ5125-02S.R7G_SOT23-3 LED.

The diagram illustrates the electrical connections for the ACES_85201-1205N module. It features a central module with 14 pins. The connections are as follows:

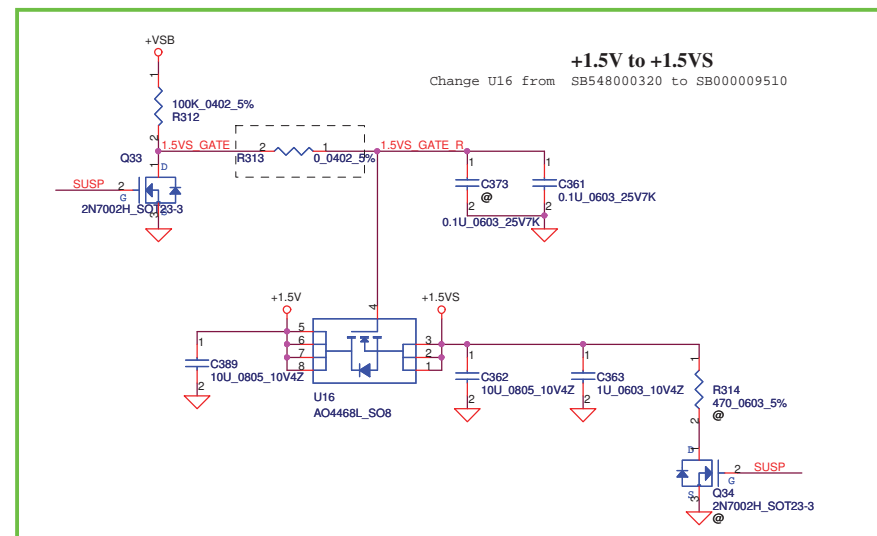
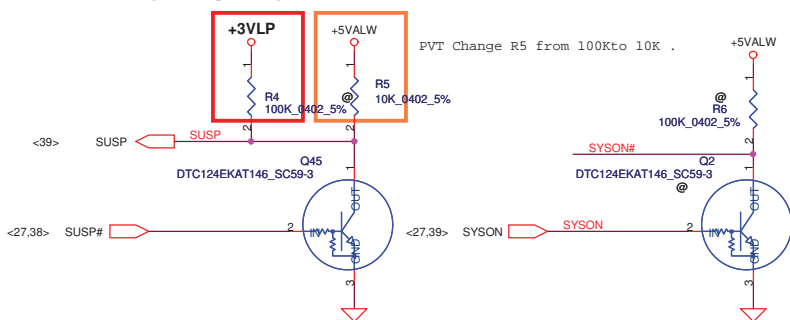
- CardReader Connections:**
 - Pins 1-3: PLUG_IN, HP_OUTL, HP_OUTR
 - Pins 4-6: MIC_JD, EXT_MIC_L, EXT_MIC_R
 - Pins 7-12: USB20_P4, USB20_N4, and associated control lines (R326, R325, 0, 1, 0402, 5%, USB20, P4 R, N4 R).
- WCM-2012-900T_4P Connections:**
 - Pins 13-14: USB20_P4, USB20_N4, and associated control lines (L65, @, 3, 2, USB20_P4 R, N4 R).
- Power and Ground Connections:**
 - +3VS: Connected to pin 1.
 - ME@: Connected to pin 14.
 - GND: Connected to pins 13 and 14.



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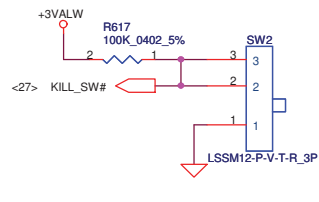
Pre MP Change SUSP pull high from +5VALW to +3VLP



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Schematic diagram of the LID SW circuit. The circuit includes a pull-up resistor R614 (100K_0402_5%) connected to +VCC_LID and a pull-down resistor R615 (100K_0402_5%) connected to ground. A capacitor C694 (0.1u_0402_16V4Z) is connected between the LID_SW pin and ground. The LID_SW pin is also connected to the output of a buffer U32 (S-5711ACDL-M3) and a capacitor C695 (10pF_0402_50V8J). The buffer U32 is powered by +VCC_LID and ground.

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON



The schematic diagram illustrates the LED connections for the Raspberry Pi 4 Model B. It shows four LEDs: LED1 (White), LED2 (Orange), LED3 (White), and LED4 (White). Each LED is connected to a specific GPIO pin, a resistor, and a power source. LED1 is connected to PWR_LED# (GPIO 27.30) and LED1_5V (300_0402_5%). LED2 is connected to CHARGE_LED1# (GPIO 27) and LED2_3V (300_0402_5%). LED3 is connected to WLAN_LED# (GPIO 23) and LED3_5V (300_0402_5%). LED4 is connected to HDD_LED# (GPIO 18) and LED4_5V (300_0402_5%).

11/05 Add this function.

The schematic shows the following components and connections:

- Inputs:** +5V_S, +5V_ODD, ODD_EN.
- Resistors:** R552 (10K_0402_5%), R677 (100K_0402_5%).
- Capacitors:** C612 (0.1U_0402_16V4Z), C611 (100U_0805_10V4Z), C613 (0.01U_0402_16V7K).
- MOSFETs:** Q99 (AP2301GN-HF_SOT23-3), Q100 (DTC124EKAT146_SC59-3).
- Other Components:** JUMP_43X79.

The circuit logic is as follows:

- The +5V_S input is connected to a network of resistors (R552, R677) and capacitors (C612, C611, C613).
- The output of this network is connected to the +5V_ODD input.
- A MOSFET (Q99) is connected to the +5V_ODD input and the ODD_EN signal.
- The MOSFET (Q100) is connected to the +5V_ODD input and the ODD_EN signal.

[illegible][illegible]

The schematic diagram illustrates the electrical connections for the OCTEK_SLS3SB1G_RV board. It shows the interface between a SATA controller and a DTX (Digital-to-Analog) converter. The SATA controller is connected to the DTX converter via a series of signal lines, including SATA_ITX_C_DRX_P1, SATA_ITX_C_DRX_N1, SATA_DTX_C_IRX_N1, and SATA_DTX_C_IRX_P1. The DTX converter is connected to the SATA controller via a series of signal lines, including SATA_DTX_C_IRX_P1, SATA_DTX_C_IRX_N1, SATA_ITX_C_DRX_N1, and SATA_ITX_C_DRX_P1. The diagram also shows the connection of power lines, including +5V_ODD, +5V, +3VOS, and GND. The board is identified as OCTEK_SLS3SB1G_RV and ME@.

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Title KB/TP/LID/KLL/ODD/LED FOR 14			
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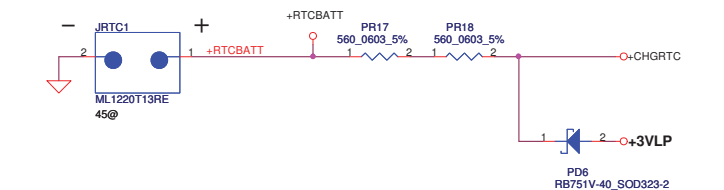
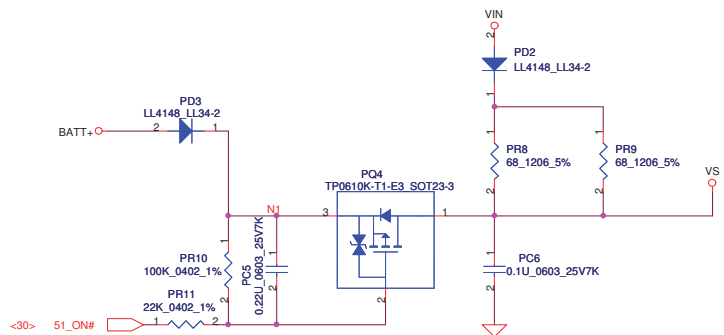
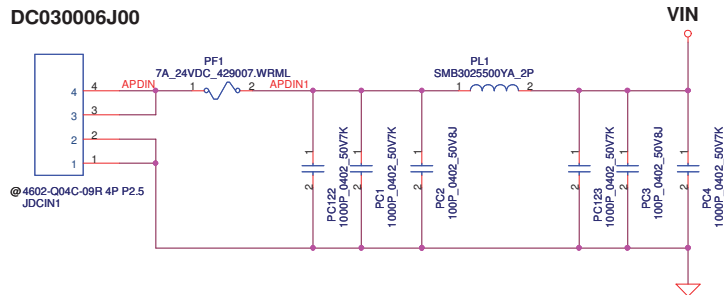
Version change list (P.I.R. List)

Page 1 of 1 for HW

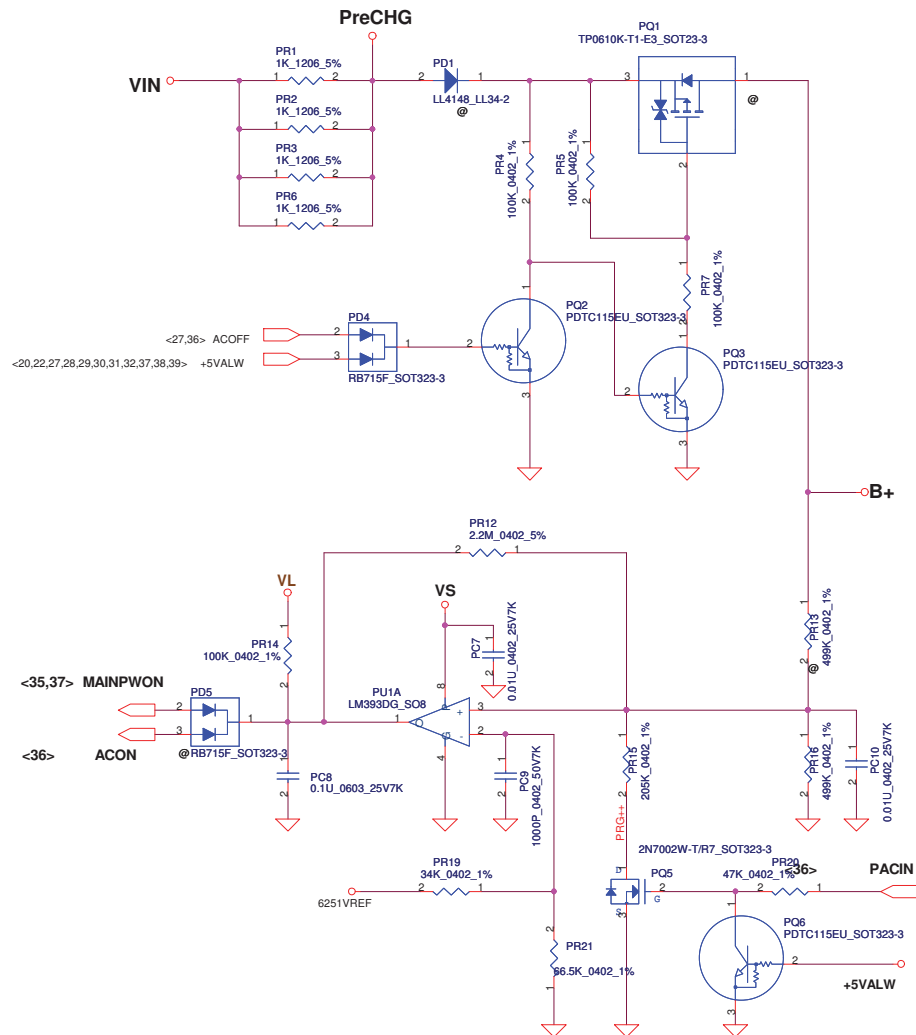
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DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

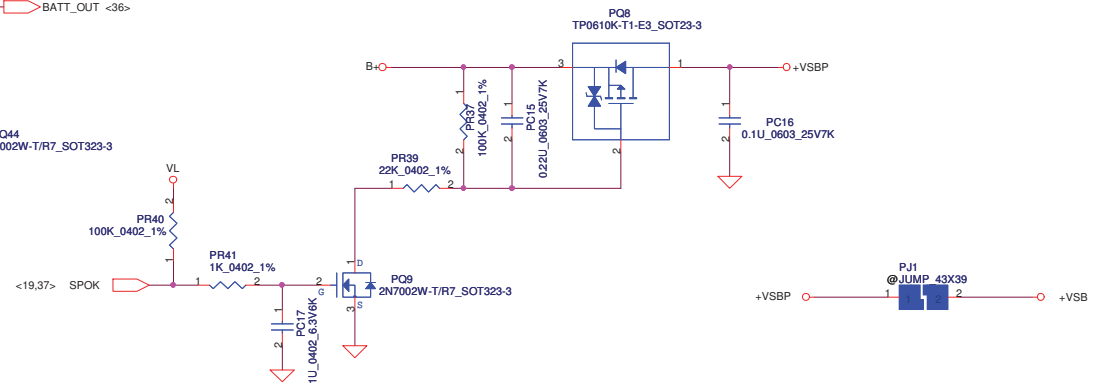
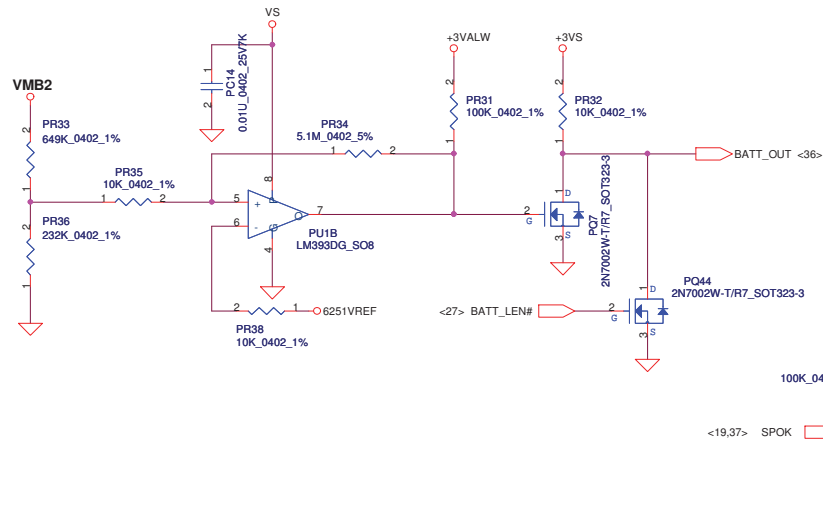
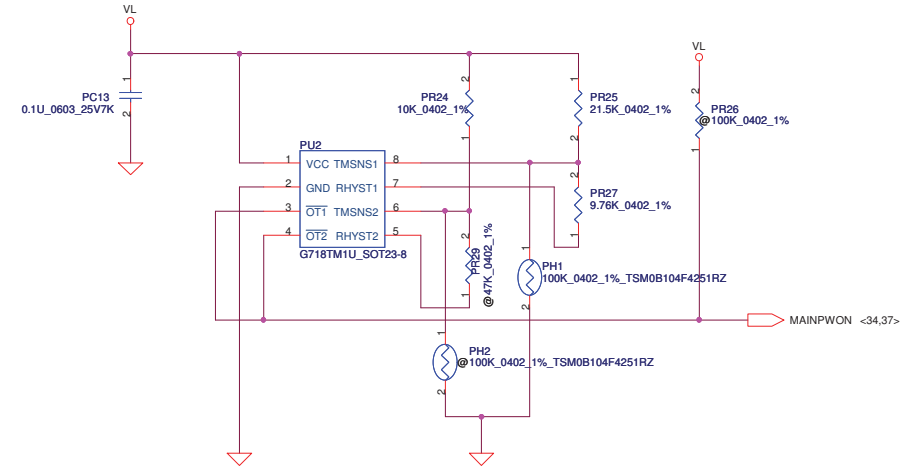
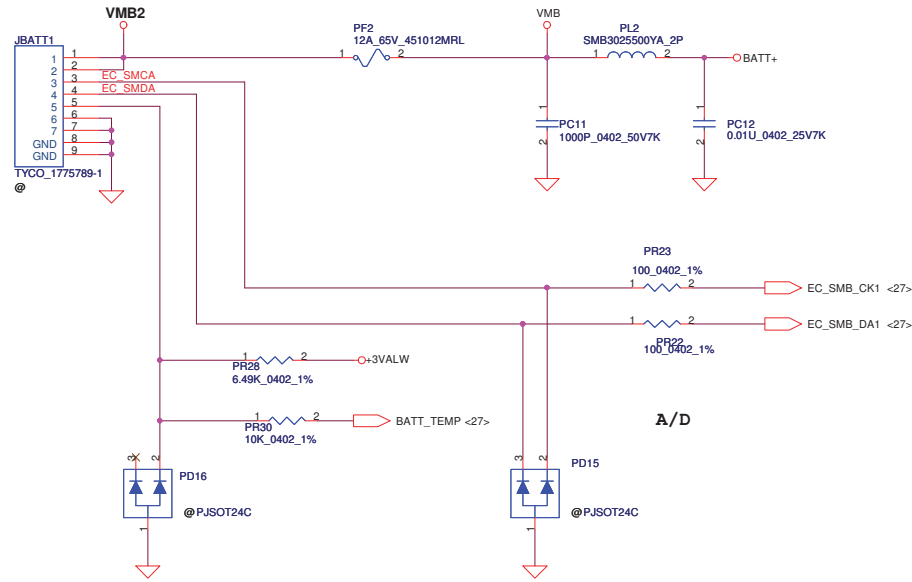
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

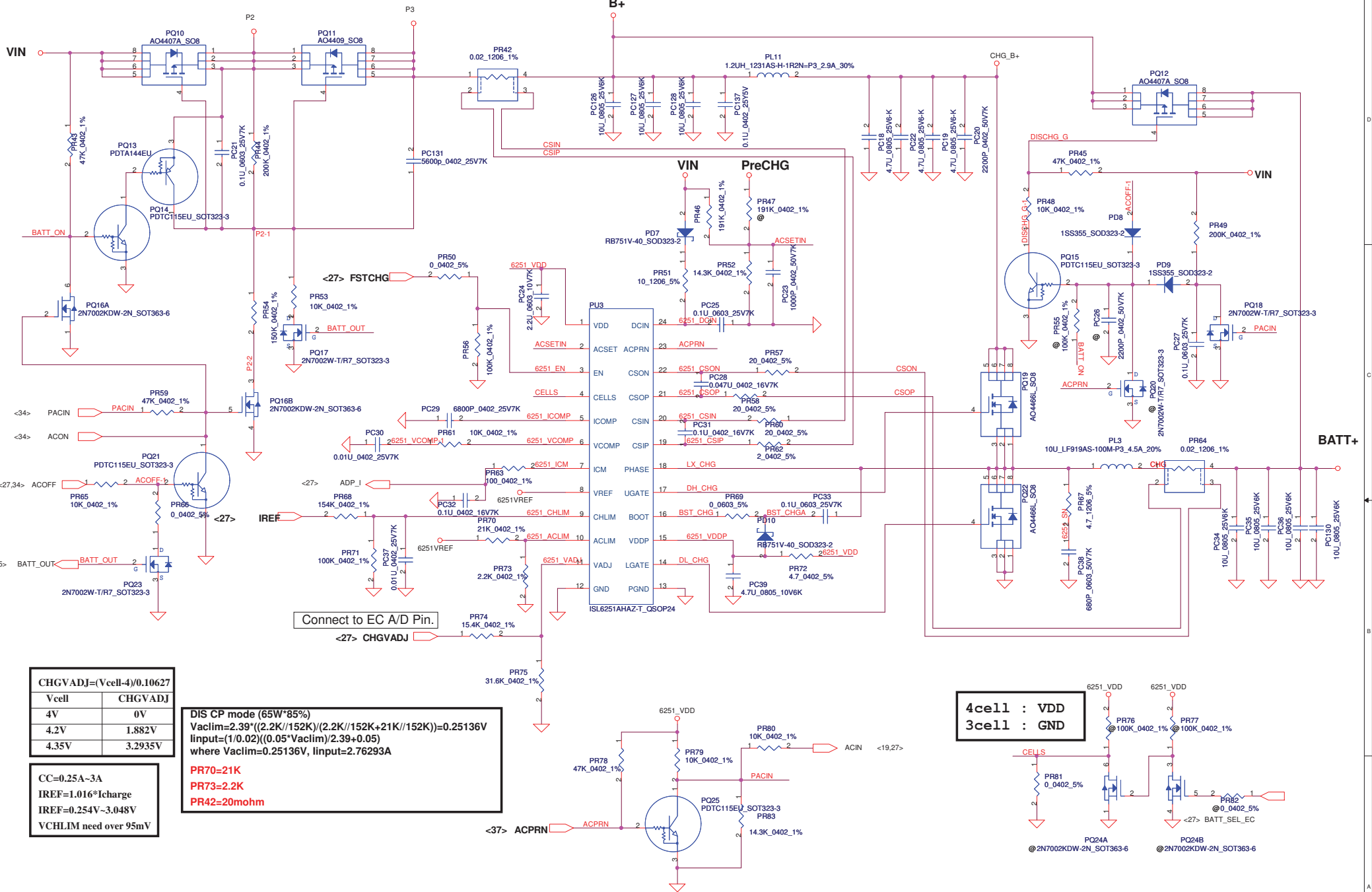
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

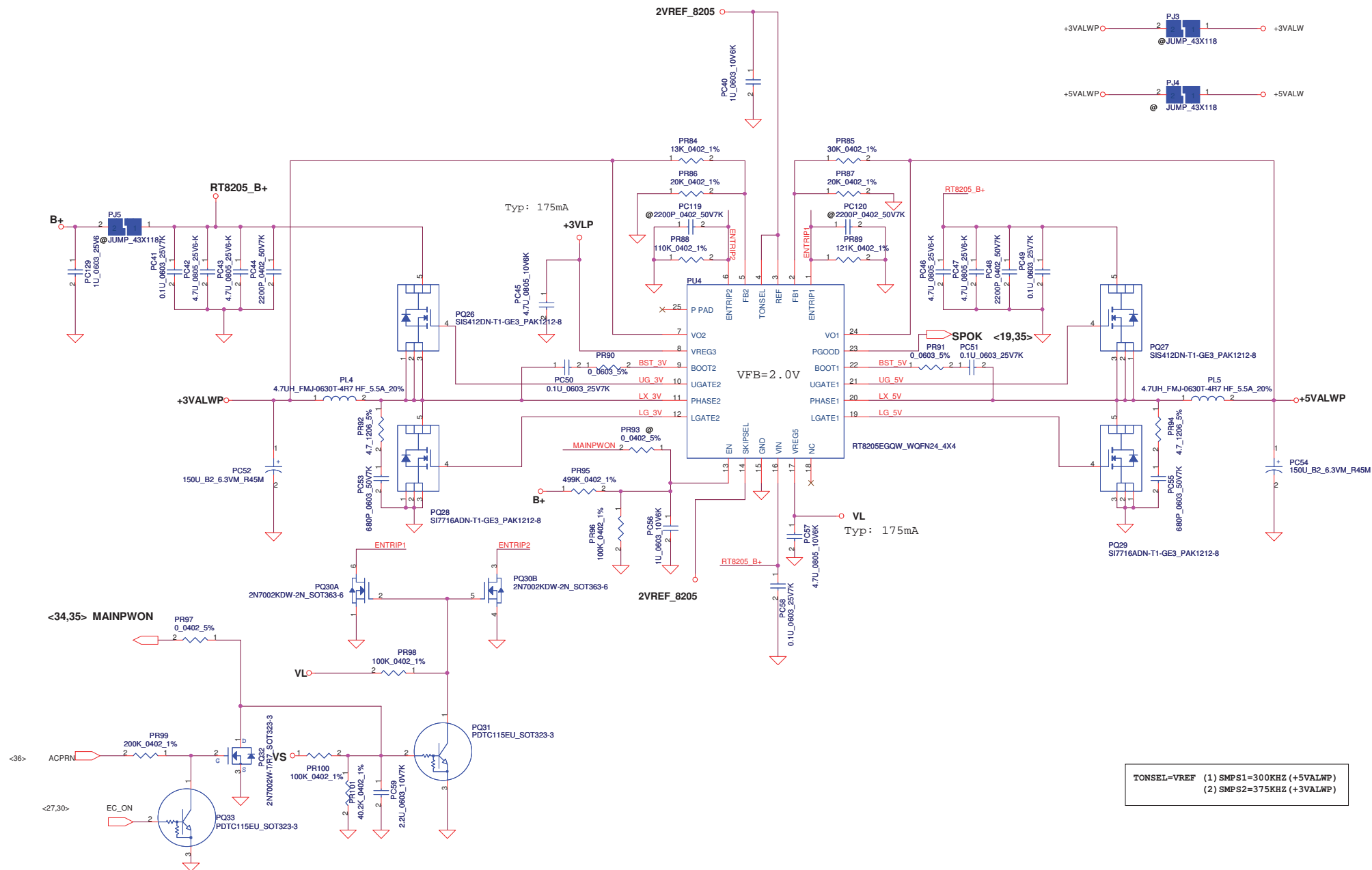


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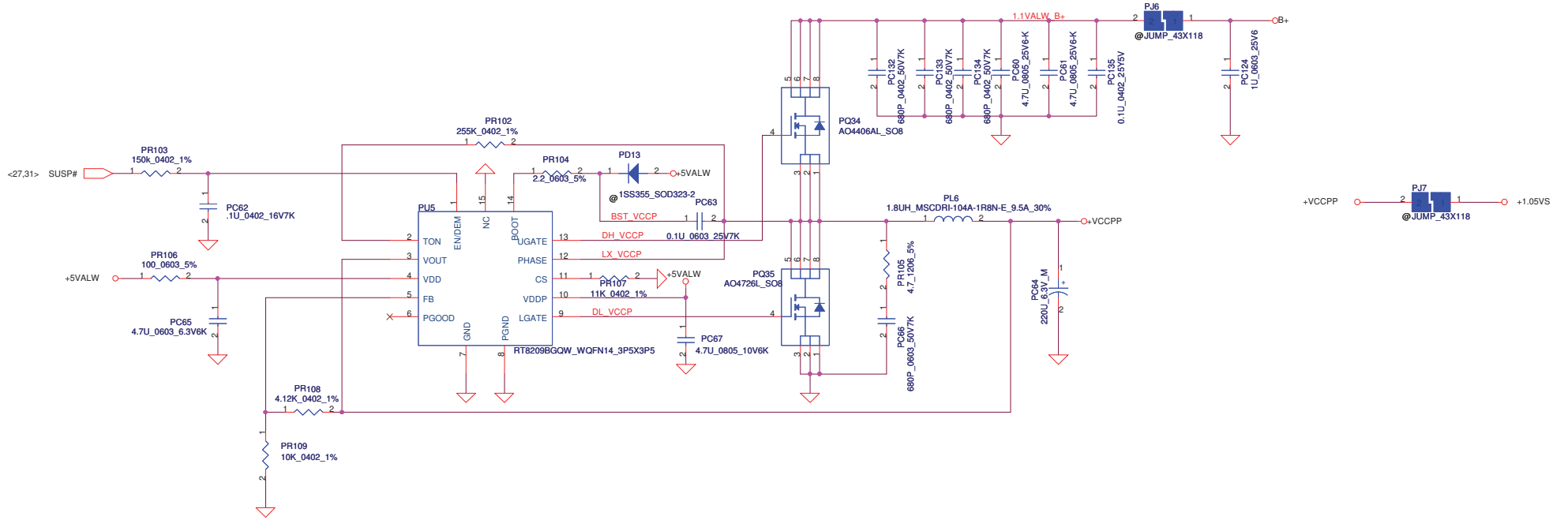


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Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P35,37,39	Add capacities for EMI request	2010.11.12	EMI	EMI test fail	Add PC132,PC133,PC134,PC135,PC136,PC137
P37	Change resistance for EMI request	2010.11.12	EMI	EMI test fail	Change PR104 from 0 ohm to 2.2ohm
P35	Add one capacitor for prevent inrush current too large	2010.11.12	PWR	If there isn't add capacity, the MOS of PQ11 have damaged risk.	Add PC131 which value is 5600PF
P34	Add one transistor for improve design margin	2010.11.12	PWR	If there isn't add transistor, the design margin of PQ11 is not enough.	Add PQ44
p39	Change resistance for CPU loadline fine tuning	2010.11.12	PWR	For meet the load line of intel spec	Change PR138 from 4.3k to 4.75k
P35	Add one capacitor for improve ripple current	2010.11.12	PWR	For meet the ripple current spec of Compal	Add PC130

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Size	Document Number	Rev			1.0
Custom	LA7011P				
Date:	Friday, December 24, 2010	Sheet	41	of	41