Compal Confidential

DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2013-02-27

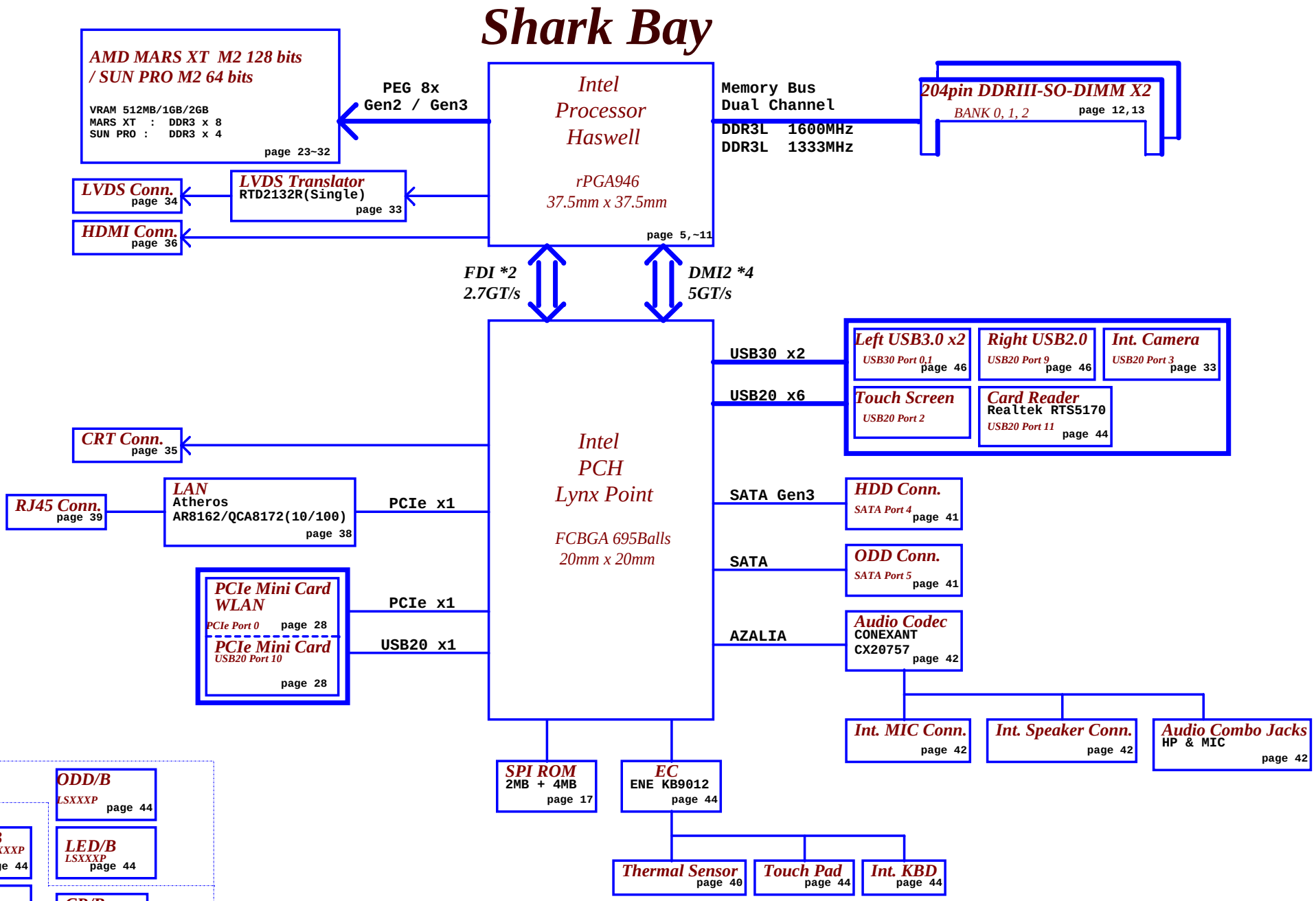
LA-9641P

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: LA-9641P	Rev: 0.3
Date: Wednesday, March 06, 2013	Sheet 1 of 61	

Shark Bay



Sub-borad

15"

14"

- ODD/B LSXXXP page 44
- Power/B LSXXXP page 44
- LED/B LSXXXP page 44
- USB/B LSXXXP page 44
- CR/B LSXXXP page 44

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Compal Electronics, Inc.

Title: Block Diagram

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 2 of 61

Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.35V	+5VS +3VS +VCC_CORE +VGA_CORE +1.5VS +0.675VS +1.05VS
S0	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID / SKU ID Table for AD channel

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	Left USB3.0
		1	Left USB3.0
	UHCI1	2	Touch screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	Right USB2.0
	UHCI5	10	WLAN
		11	Card reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Cameara	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
Righ side USB	RUSB@
Zero ODD circuit	ZODD@
Share ROM	SROM@
Non-share ROM	NOSROM@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

R_USB@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001_100xb

PCH SM Bus address

Device	Address
DDR DIMM1 ChannelA	0xA0
DDR DIMM2 ChannelB	0xA4

Device	Address
RTD2132R	1101 010Xb

AMD-GPU SM Bus address

Device	Address
Internal thermal sensor	1000_001xb

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	V +3VS

VRAM BOM STRUCTURE Refer P4. VGA NOTE

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Compal Electronics, Inc.			
Title: Notes List			
Size: B	Document Number: LA-9641P		Rev: 0.3
Date: Wednesday, March 06, 2013	Sheet 3 of 61		

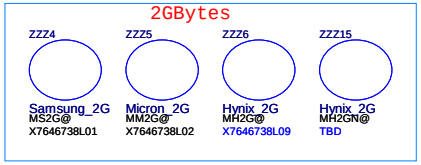
Mars XT VRAM STRAP

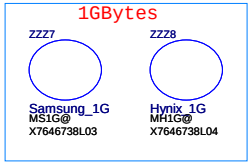
	X76@ Vendor (UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12)	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	R_pd RV27
ZZZ4 MS2G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
ZZZ5 MM2G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	0	1	0	4.53K	2K
ZZZ7 MS1G@	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
ZZZ8 MH1G@	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC
ZZZ15 MH2GN@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K

2GBytes

1GBytes

2GBytes





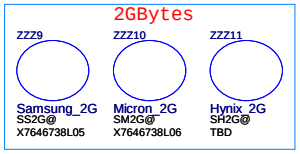
Sun PRO VRAM STRAP

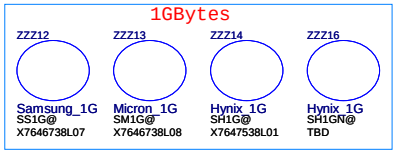
	X76@ Vendor (UV9, UV10, UV11, UV12)	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV20	R_pd RV27
ZZZ9 SS2G@	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
ZZZ10 SM2G@	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-107G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
ZZZ13 SM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@	Hynix 2048Mbits SA000065300 H5TQ2G63DFR-N0C	1	1	1	4.75K	NC
	Hynix 2048Mbits SA00006H400 H5TC2G63FFR-11C	1	0	0	4.53K	4.99K

2GBytes

1GBytes

1GBytes

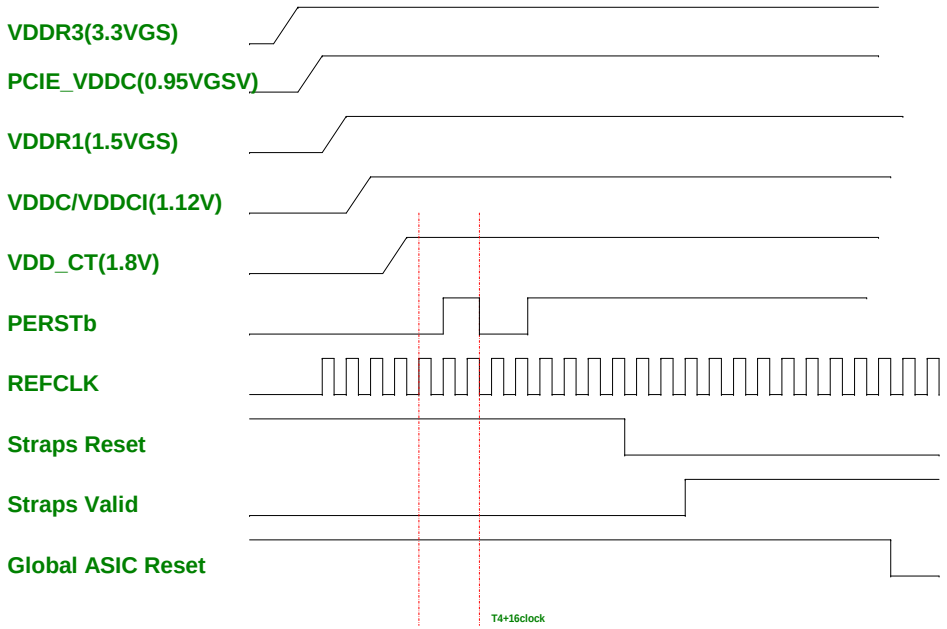




Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date 2012/07/11	Title: VGA Notes List
			Size: Custom; Document Number: LA-9641P; Rev: 0.3
			Date: Wednesday, March 06, 2013; Sheet 4 of 61

ZZZ1 14@

14" PCB LA9641

DA6000WQ000

ZZZ2 15@

15" PCB LA9641

DA6000WQ100

+VCOMP_OUT

PEG_RCOMP 2 — 24.9_0402_1% — 1 R1

Note:
Trace width=12 mils ,Spacing=15mils
Max length= 400 mils.

Haswell rPGA EDS

JCPU1A

DMI

<15> DMI_CRX_PTX_N0 — DMI_CRX_PTX_N0 D21 — DMI_RXN_0
<15> DMI_CRX_PTX_N1 — DMI_CRX_PTX_N1 C21 — DMI_RXN_1
<15> DMI_CRX_PTX_N2 — DMI_CRX_PTX_N2 B21 — DMI_RXN_2
<15> DMI_CRX_PTX_N3 — DMI_CRX_PTX_N3 A21 — DMI_RXN_3

<15> DMI_CRX_PTX_P0 — DMI_CRX_PTX_P0 D20 — DMI_RXP_0
<15> DMI_CRX_PTX_P1 — DMI_CRX_PTX_P1 C20 — DMI_RXP_1
<15> DMI_CRX_PTX_P2 — DMI_CRX_PTX_P2 B20 — DMI_RXP_2
<15> DMI_CRX_PTX_P3 — DMI_CRX_PTX_P3 A20 — DMI_RXP_3

<15> DMI_CTX_PRX_N0 — DMI_CTX_PRX_N0 D18 — DMI_TXN_0
<15> DMI_CTX_PRX_N1 — DMI_CTX_PRX_N1 C17 — DMI_TXN_1
<15> DMI_CTX_PRX_N2 — DMI_CTX_PRX_N2 B17 — DMI_TXN_2
<15> DMI_CTX_PRX_N3 — DMI_CTX_PRX_N3 A17 — DMI_TXN_3

<15> DMI_CTX_PRX_P0 — DMI_CTX_PRX_P0 D17 — DMI_TXP_0
<15> DMI_CTX_PRX_P1 — DMI_CTX_PRX_P1 C18 — DMI_TXP_1
<15> DMI_CTX_PRX_P2 — DMI_CTX_PRX_P2 B18 — DMI_TXP_2
<15> DMI_CTX_PRX_P3 — DMI_CTX_PRX_P3 A18 — DMI_TXP_3

FDI

<15> FDI_CSYNC — H29 — FDI_CSYNC
<15> FDI_INT — J29 — DISP_INT

Note:
Trace width=4 mils ,Spacing=5mil
Max length= 10000 mils.

PEG

PEG_RCOMP — E23 PEG_RCOMP

PEG_RXN_0 M29
PEG_RXN_1 M28
PEG_RXN_2 M31
PEG_RXN_3 L30
PEG_RXN_4 M33
PEG_RXN_5 L32
PEG_RXN_6 M35
PEG_RXN_7 L34
PEG_RXN_8 E29 PCIE_CRX_GTX_N7
PEG_RXN_9 D28 PCIE_CRX_GTX_N6
PEG_RXN_10 E31 PCIE_CRX_GTX_N5
PEG_RXN_11 D30 PCIE_CRX_GTX_N4
PEG_RXN_12 E35 PCIE_CRX_GTX_N3
PEG_RXN_13 D34 PCIE_CRX_GTX_N2
PEG_RXN_14 E33 PCIE_CRX_GTX_N1
PEG_RXN_15 E32 PCIE_CRX_GTX_N0

PCIE_CRX_GTX_N[0..7] <23>

PEG_RXP_0 L29
PEG_RXP_1 L28
PEG_RXP_2 L31
PEG_RXP_3 K30
PEG_RXP_4 L33
PEG_RXP_5 K32
PEG_RXP_6 L35
PEG_RXP_7 K34
PEG_RXP_8 F29 PCIE_CRX_GTX_P7
PEG_RXP_9 E28 PCIE_CRX_GTX_P6
PEG_RXP_10 F31 PCIE_CRX_GTX_P5
PEG_RXP_11 E30 PCIE_CRX_GTX_P4
PEG_RXP_12 F35 PCIE_CRX_GTX_P3
PEG_RXP_13 E34 PCIE_CRX_GTX_P2
PEG_RXP_14 F33 PCIE_CRX_GTX_P1
PEG_RXP_15 D32 PCIE_CRX_GTX_P0

PCIE_CRX_GTX_P[0..7] <23>

PEG_TXN_0 H35
PEG_TXN_1 H34
PEG_TXN_2 J33
PEG_TXN_3 H32
PEG_TXN_4 J31
PEG_TXN_5 G30
PEG_TXN_6 C33
PEG_TXN_7 B32
PEG_TXN_8 B31 PCIE_CTX_GRX_C_N7 — C9 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N7
PEG_TXN_9 A30 PCIE_CTX_GRX_C_N6 — C10 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N6
PEG_TXN_10 B29 PCIE_CTX_GRX_C_N5 — C11 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N5
PEG_TXN_11 A28 PCIE_CTX_GRX_C_N4 — C12 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N4
PEG_TXN_12 B27 PCIE_CTX_GRX_C_N3 — C13 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N3
PEG_TXN_13 A26 PCIE_CTX_GRX_C_N2 — C14 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N2
PEG_TXN_14 B25 PCIE_CTX_GRX_C_N1 — C15 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N1
PEG_TXN_15 A24 PCIE_CTX_GRX_C_N0 — C16 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_N0

PCIE_CTX_GRX_N[0..7] <23>

PEG_TXP_0 J35
PEG_TXP_1 G34
PEG_TXP_2 H33
PEG_TXP_3 G32
PEG_TXP_4 D31
PEG_TXP_5 D30
PEG_TXP_6 B33
PEG_TXP_7 A32
PEG_TXP_8 C31 PCIE_CTX_GRX_C_P7 — C25 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P7
PEG_TXP_9 B30 PCIE_CTX_GRX_C_P6 — C26 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P6
PEG_TXP_10 C29 PCIE_CTX_GRX_C_P5 — C27 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P5
PEG_TXP_11 B28 PCIE_CTX_GRX_C_P4 — C28 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P4
PEG_TXP_12 C27 PCIE_CTX_GRX_C_P3 — C29 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P3
PEG_TXP_13 B26 PCIE_CTX_GRX_C_P2 — C30 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P2
PEG_TXP_14 C25 PCIE_CTX_GRX_C_P1 — C31 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P1
PEG_TXP_15 B24 PCIE_CTX_GRX_C_P0 — C32 PX@ — 2 0.22U_0402_10V6K PCIE_CTX_GRX_P0

PCIE_CTX_GRX_P[0..7] <23>

INTEL_HASWELL_HASWELL 1 OF 9

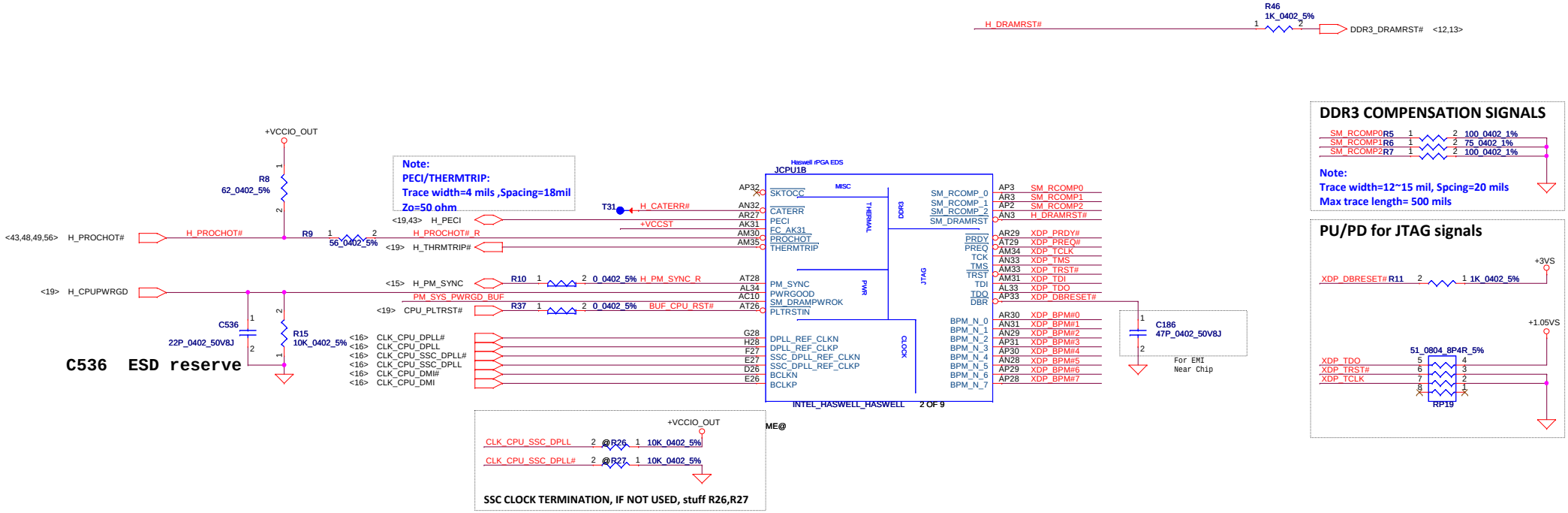
ME@

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

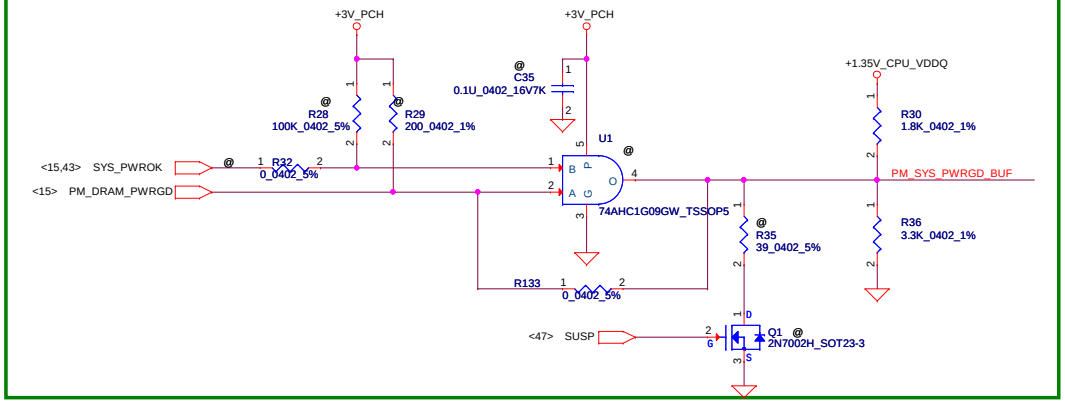
Title: **PROCESSOR(1/7) DMI,FDI,PEG**

Size: Custom | Document Number: **LA-9641P** | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 5 of 61



SM_DRAMPWROK with DDR Power Gating Topology



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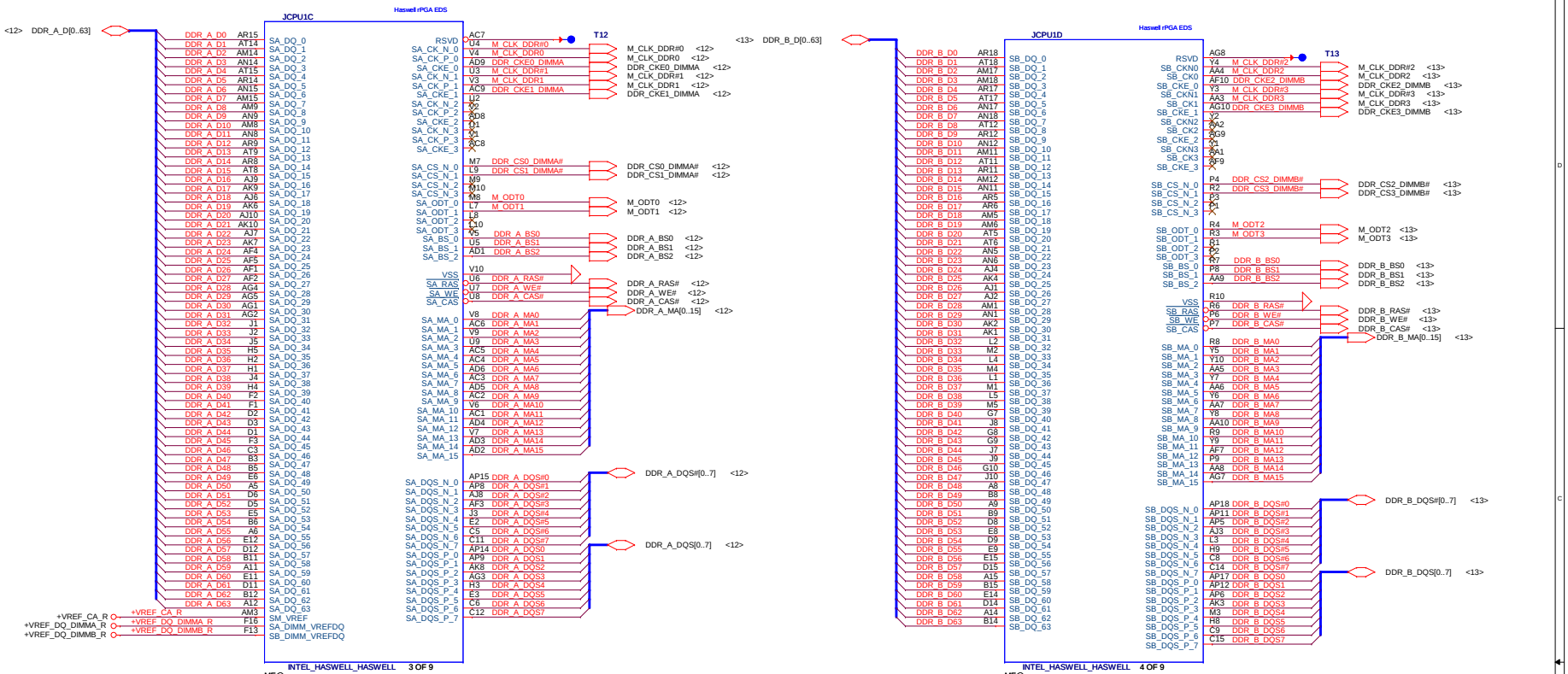
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 6 of 61



CPI DRIVER VREF PATH IS DEFAULT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-9641P	0.3

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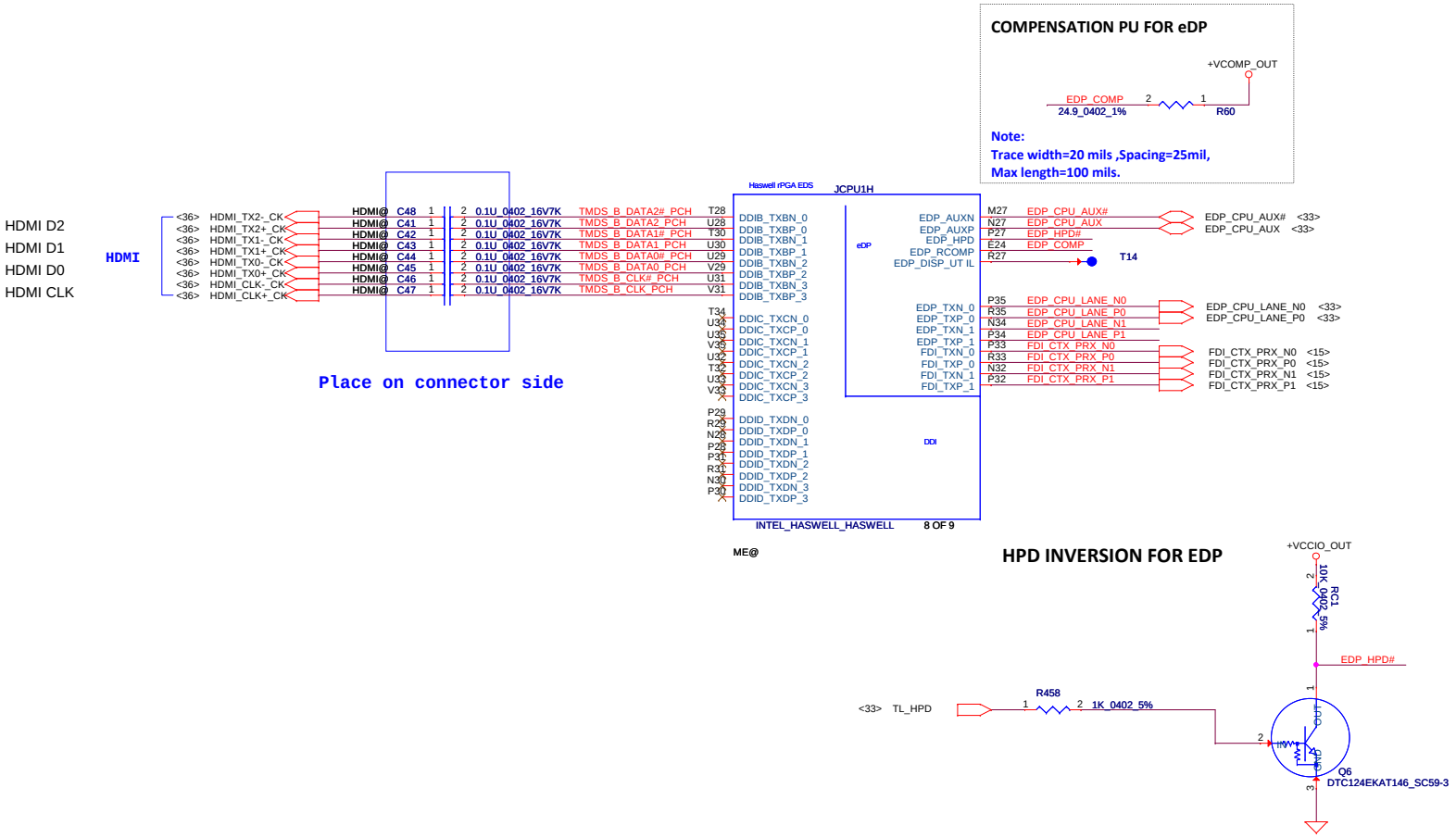

HPD is a active high signal from device. The HPD processor input is a low voltage active signal.

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Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: LA-9641P | Rev: 0.3

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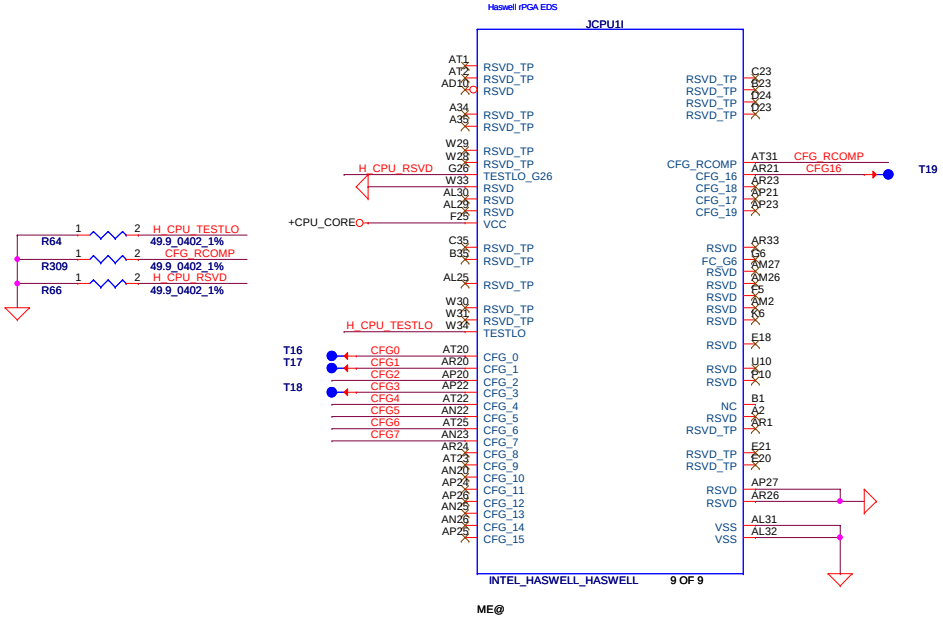
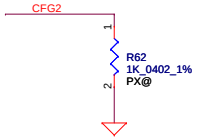
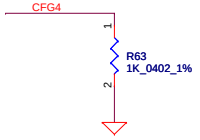
CFG Straps for Processor

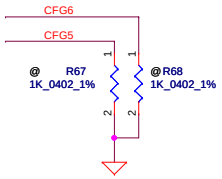




PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: LA-9641P | Rev: 0.3

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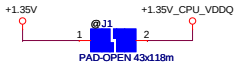
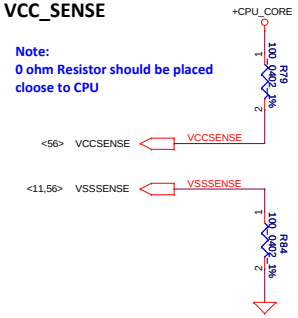
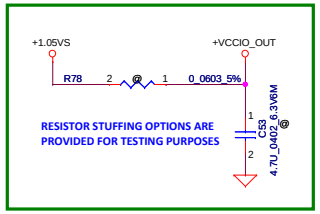
+1.35V_CPU_VDDQ Source

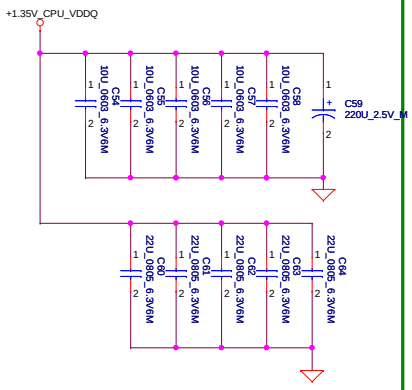


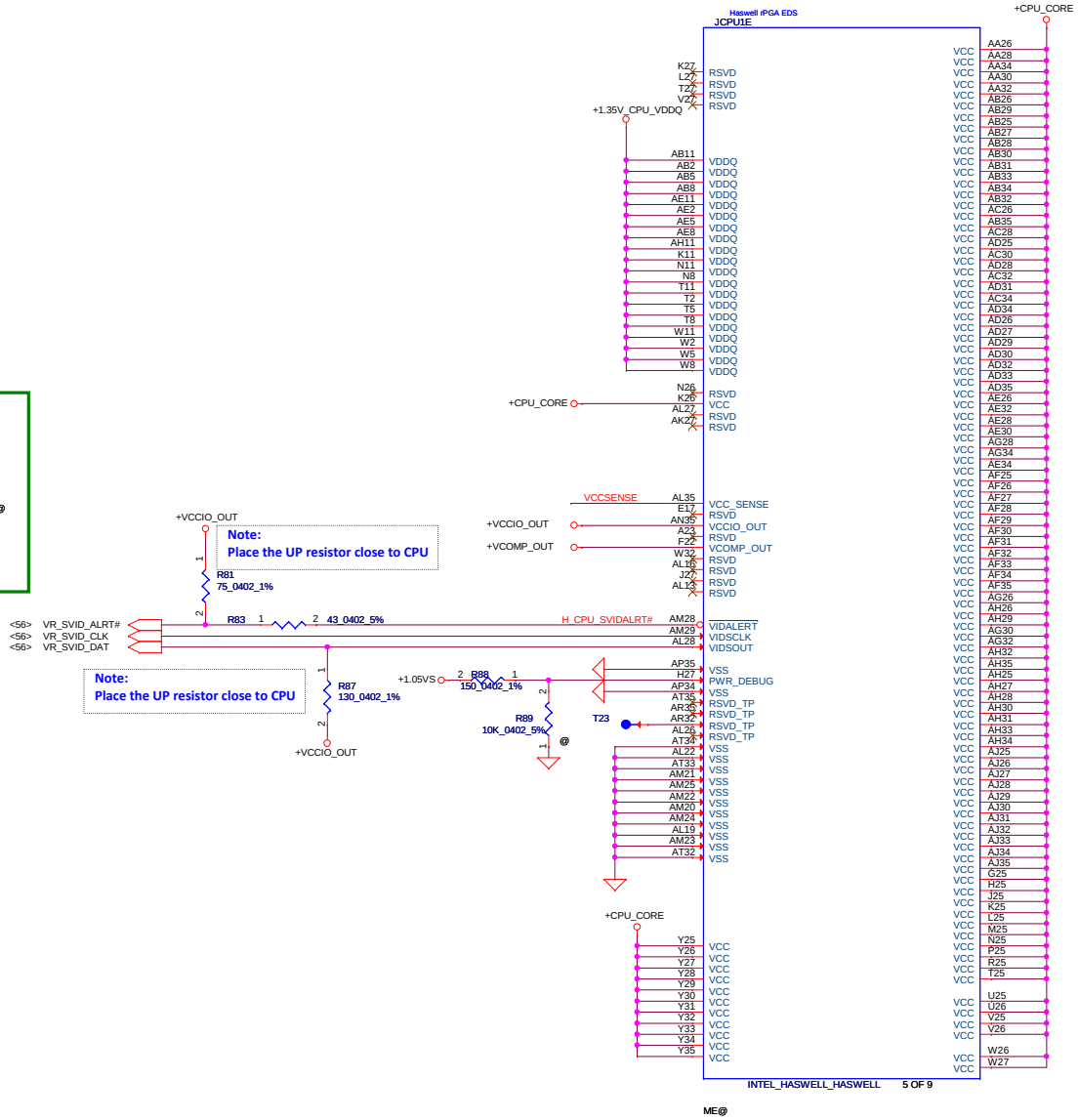
VCC_SENSE





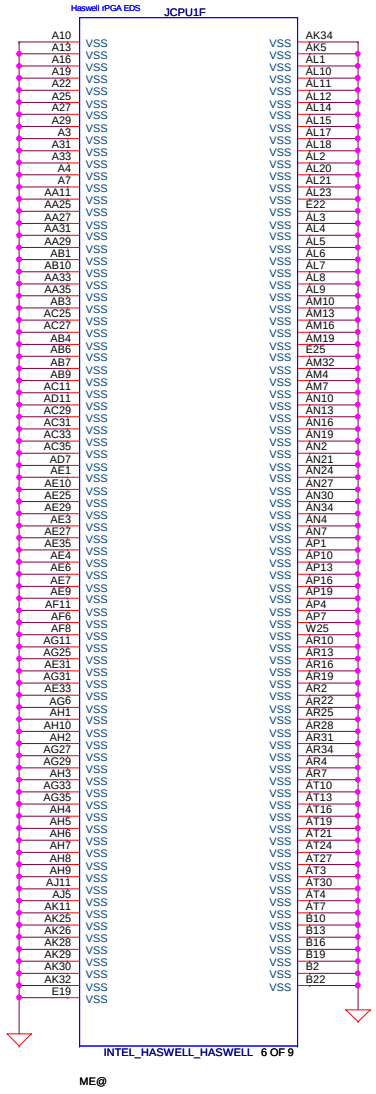
VDDQ DECOUPLING

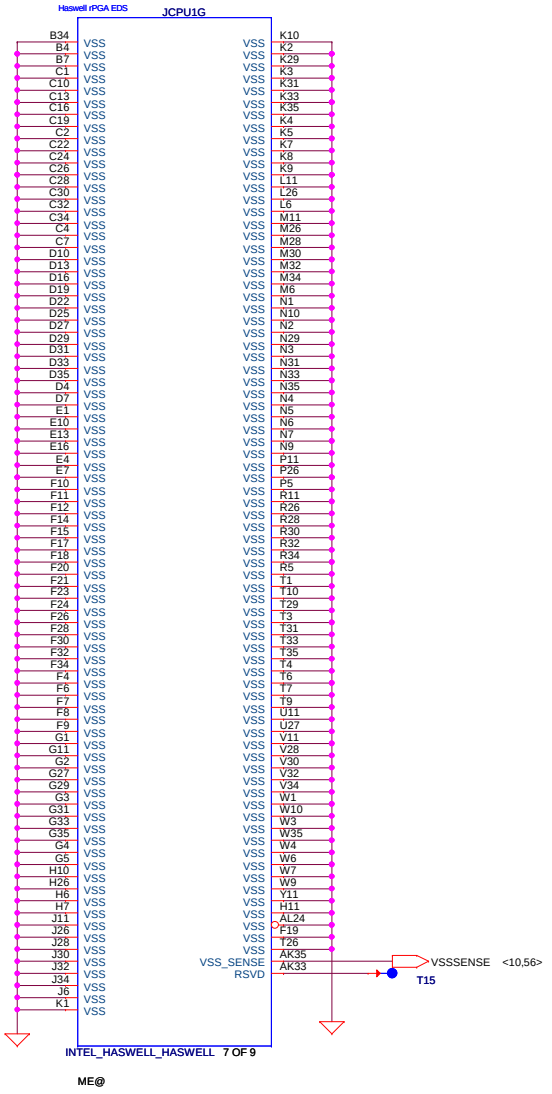




Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	PROCESSOR(6/7) PWR		
Size: Custom	Document Number: LA-9641P		Rev: 0.3
Date: Wednesday, March 06, 2013	Sheet 10 of 61		





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number: LA-9641P | Rev: 0.3

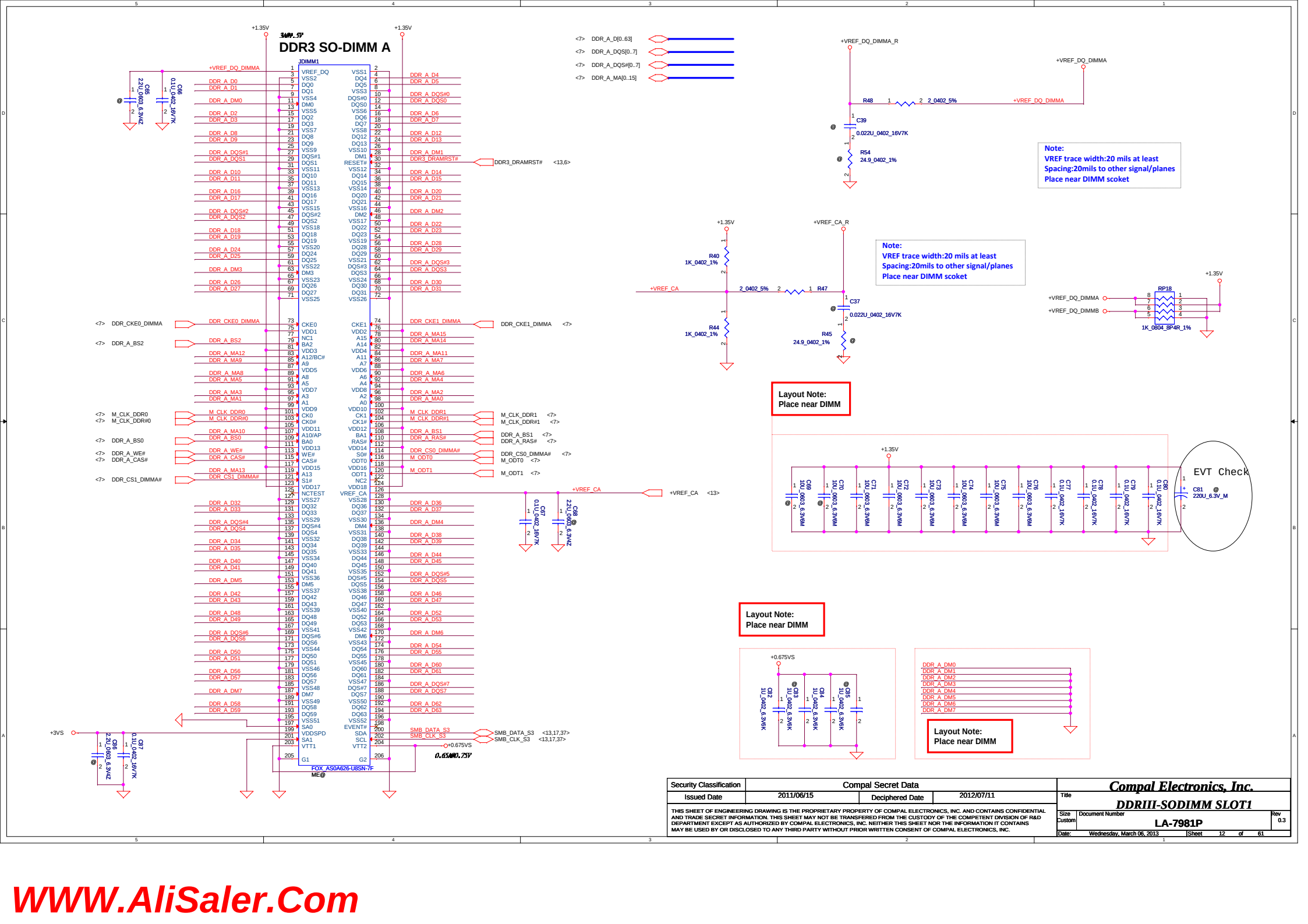
Date: Wednesday, March 06, 2013 | Sheet 11 of 61

DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U8SN-7F

ME@



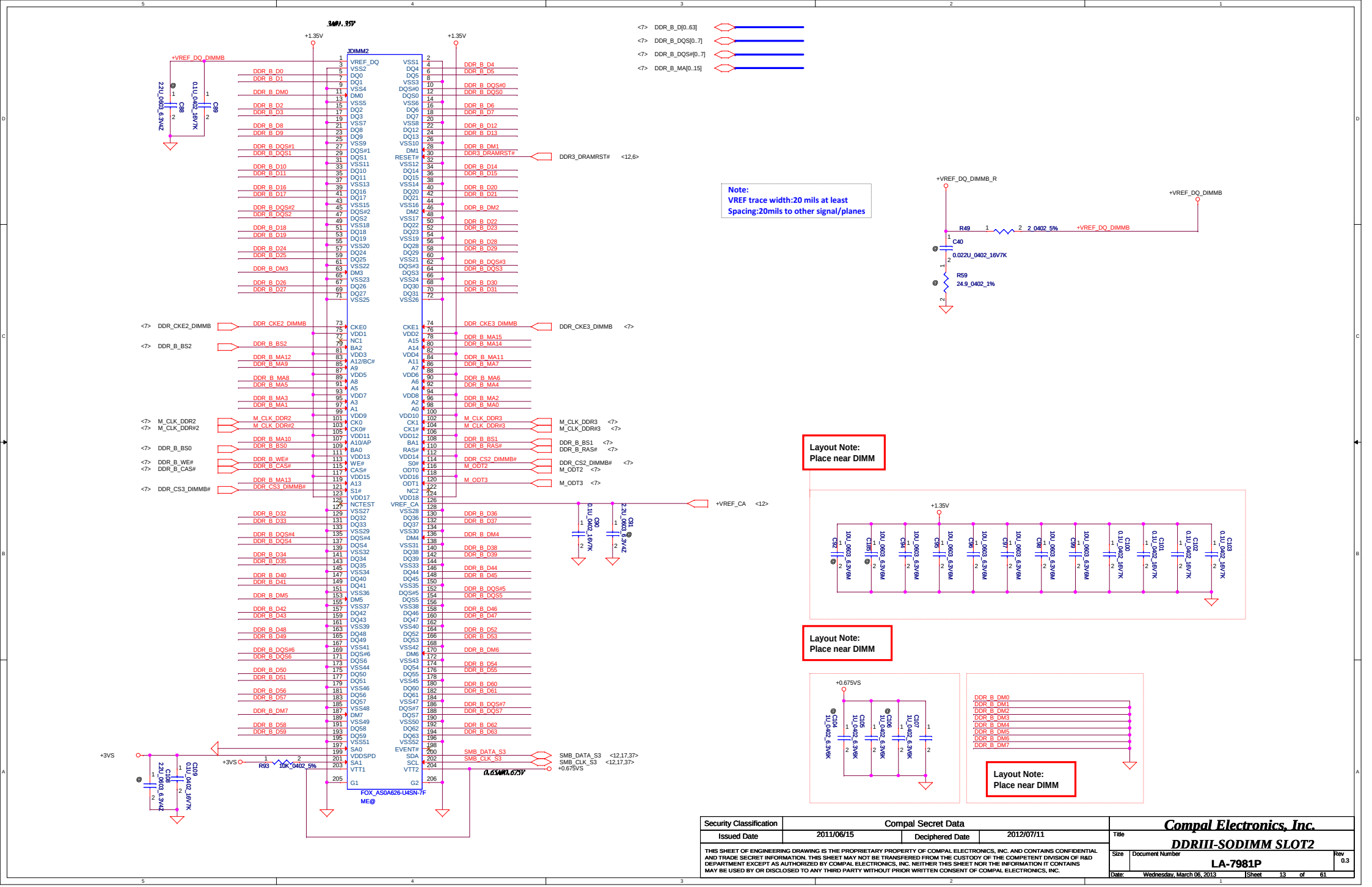
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **LA-7981P** | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 12 of 61



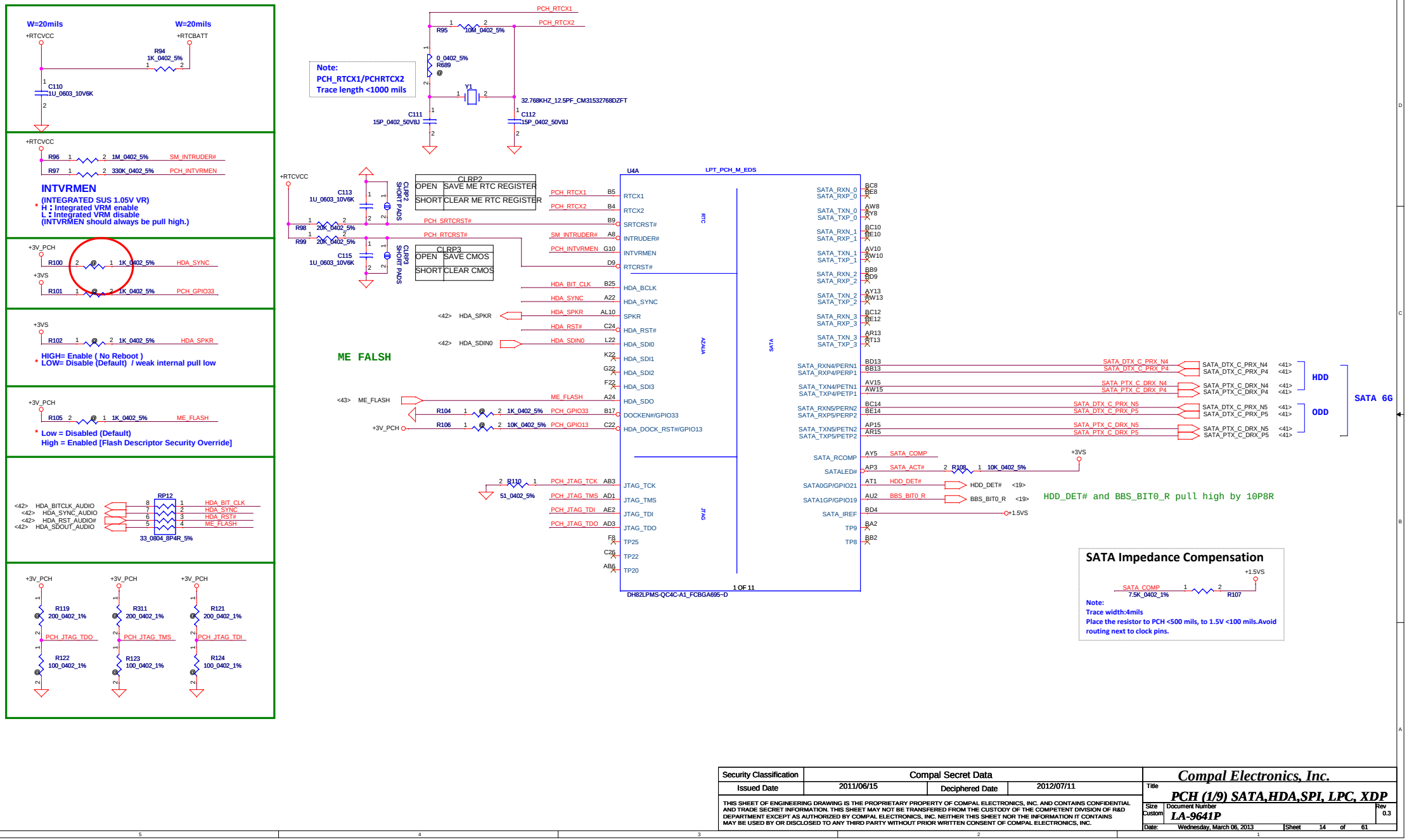
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-7981P	0.3

Date: Wednesday, March 06, 2013 | Sheet 13 of 61



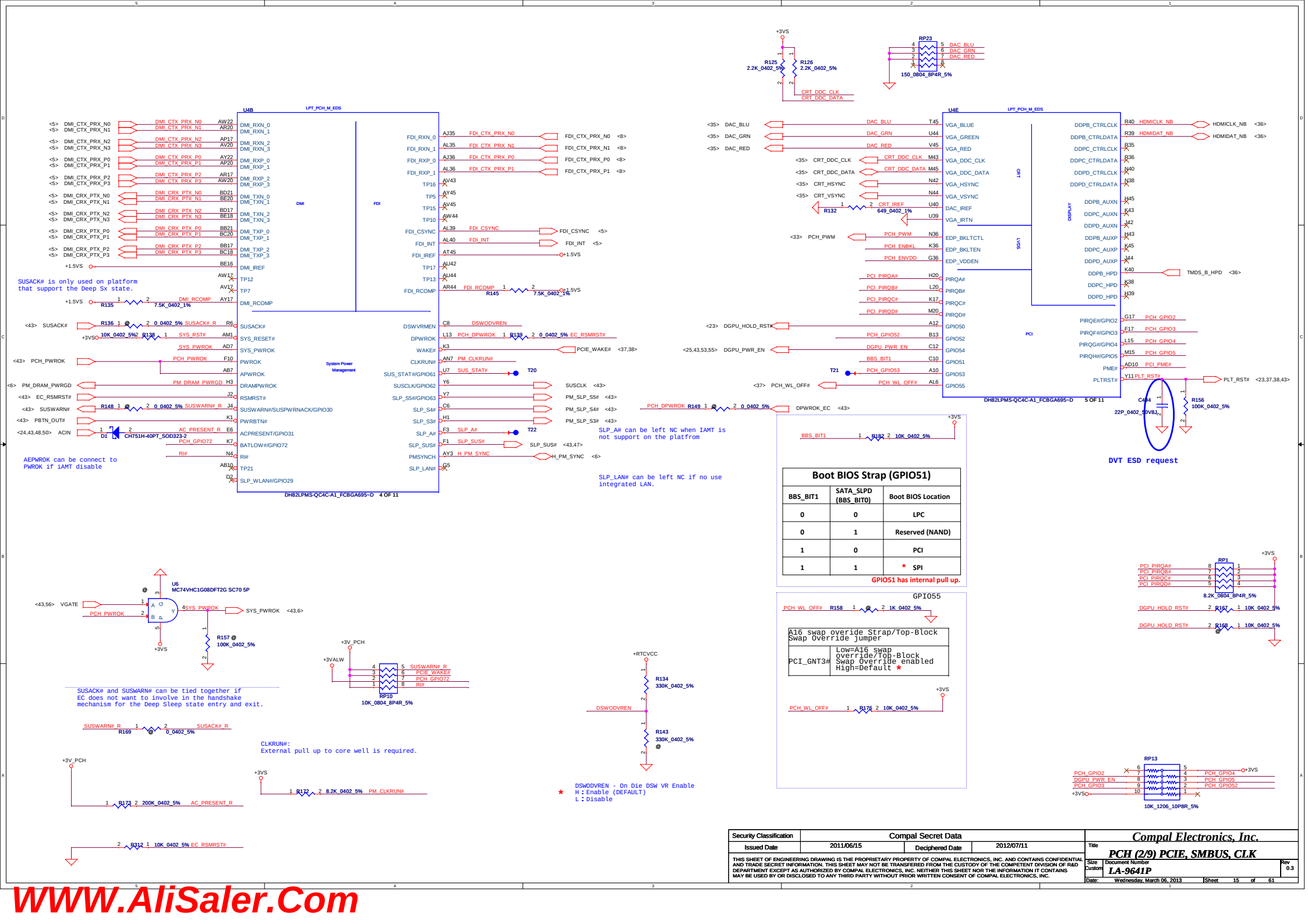
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

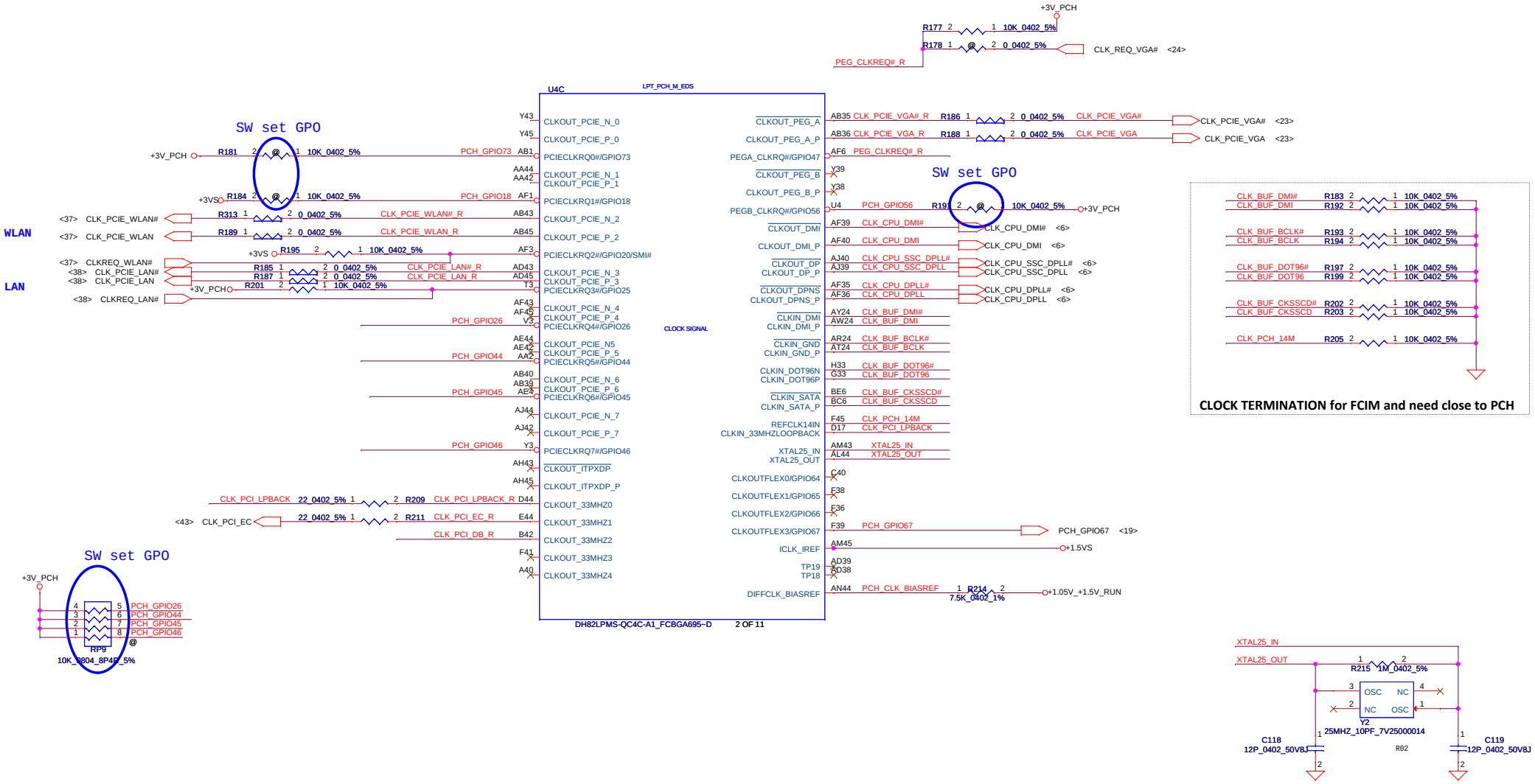
Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC, XDP

Size	Document Number	Rev
Custom	LA-9641P	0.3

Date: Wednesday, March 06, 2013 Sheet 14 of 61





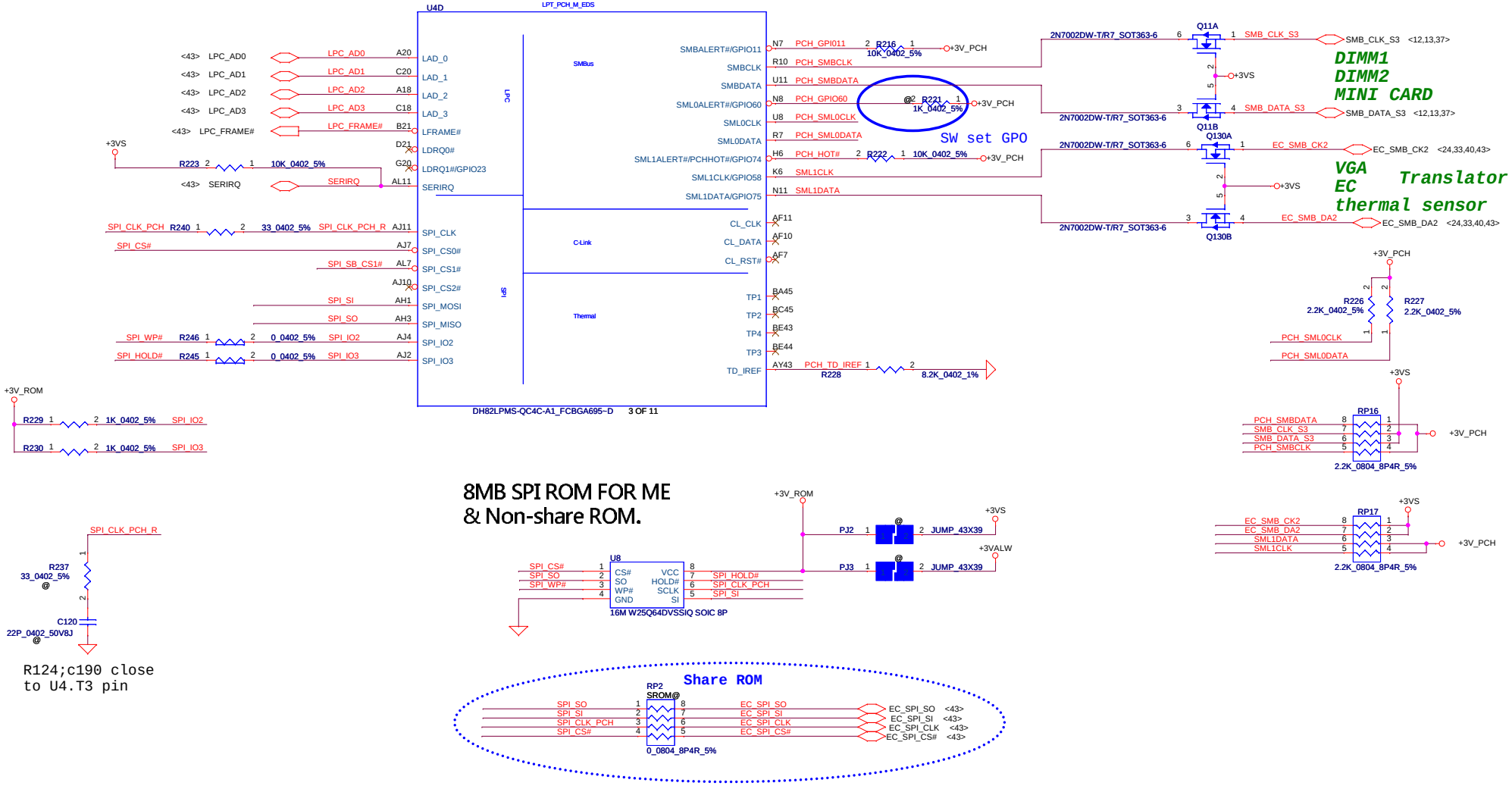
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-9641P	0.3

Date: Wednesday, March 06, 2013 Sheet 16 of 61



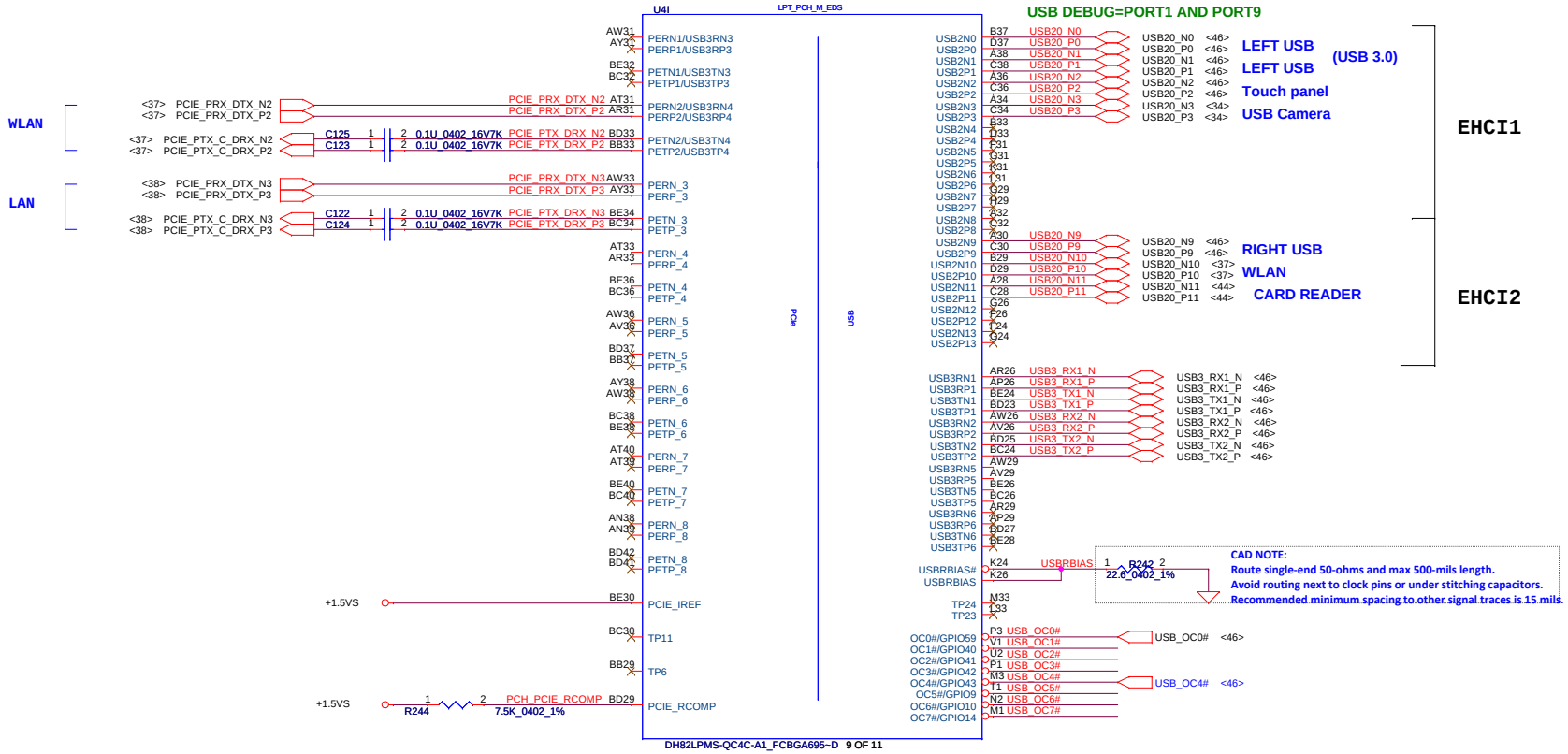
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

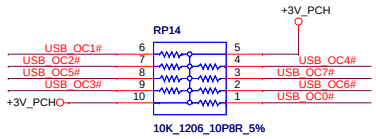
Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 17 of 61





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: LA-9641P | Rev: 0.3

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SW set GPO

GPIO8 Weak internal pull-high but requires an external pull down.

Remove strap description inform SW set GPO

PU on power side

SW set GPO

SW set GPO

Need Update

BIOS Request SKU ID

PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	DIS
1	1	UMA

PCH_GPIO69	Function
0	
1	

PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	SUN PRO
1	Mars XT

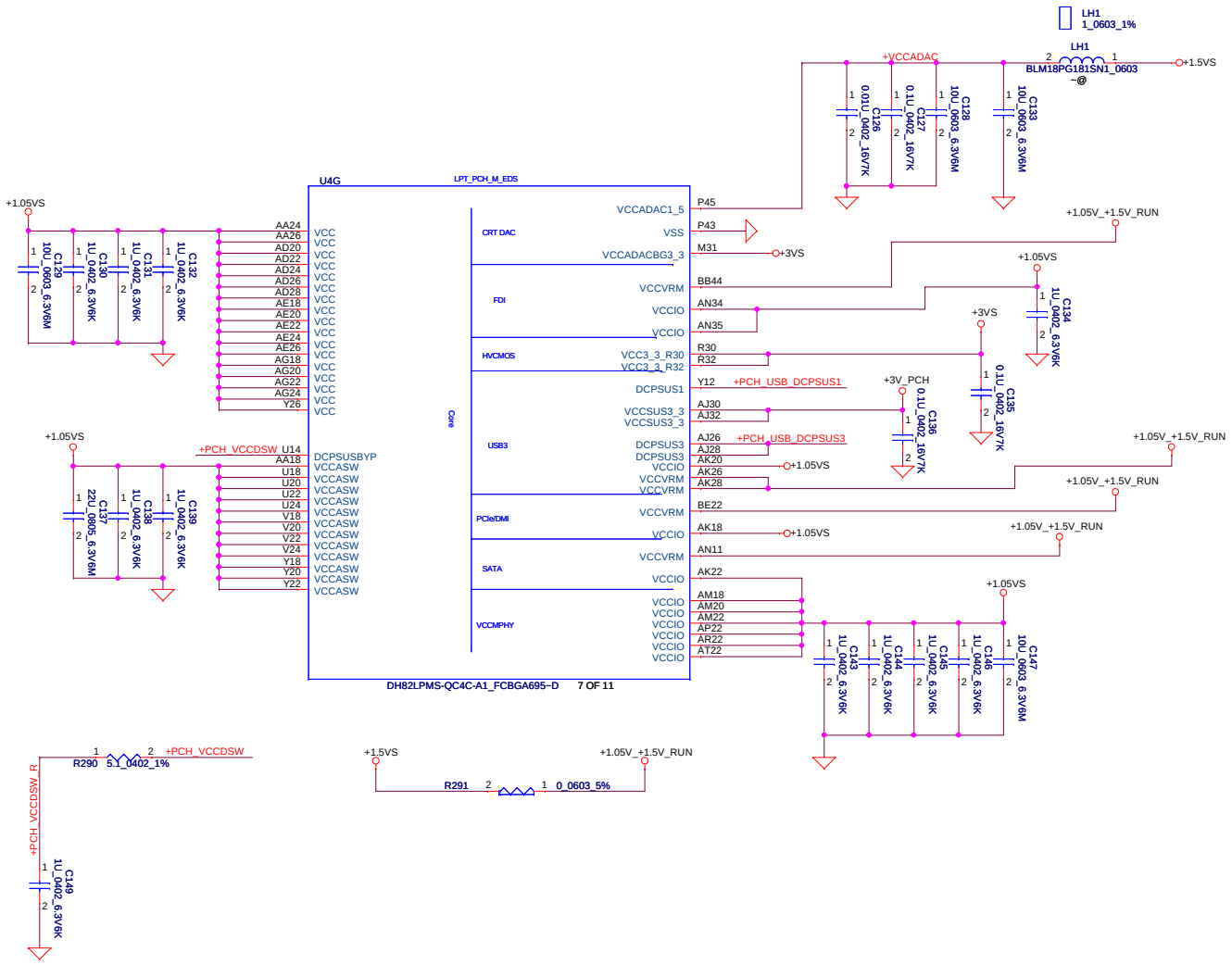
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 19 of 61



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

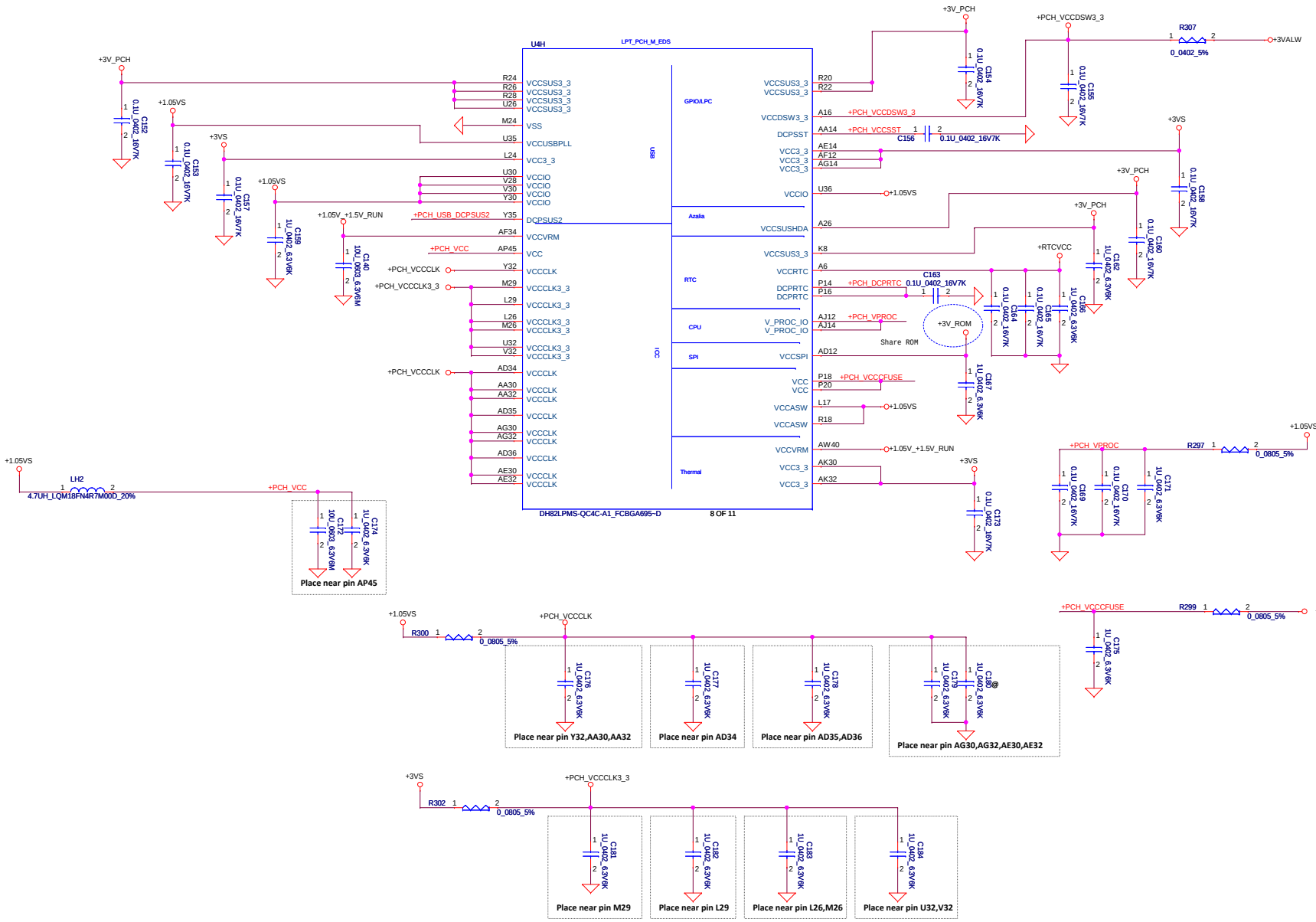
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 20 of 61



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCADAC1_5	1.5V	0.070 A
VCCADAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

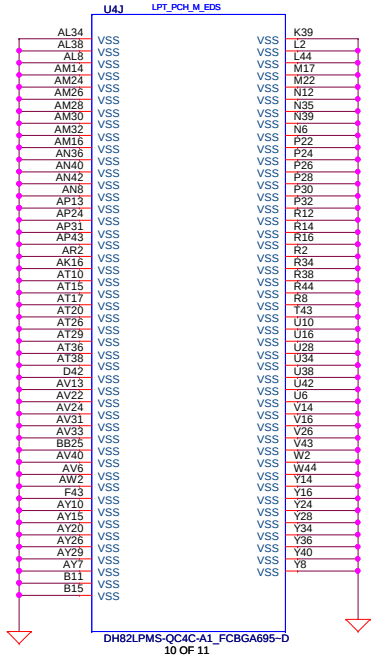
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

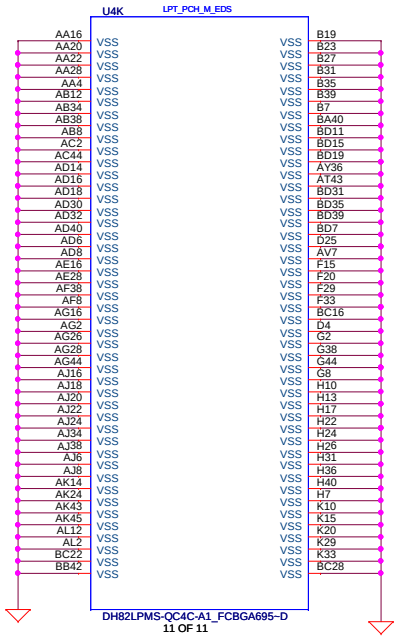
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 21 of 61





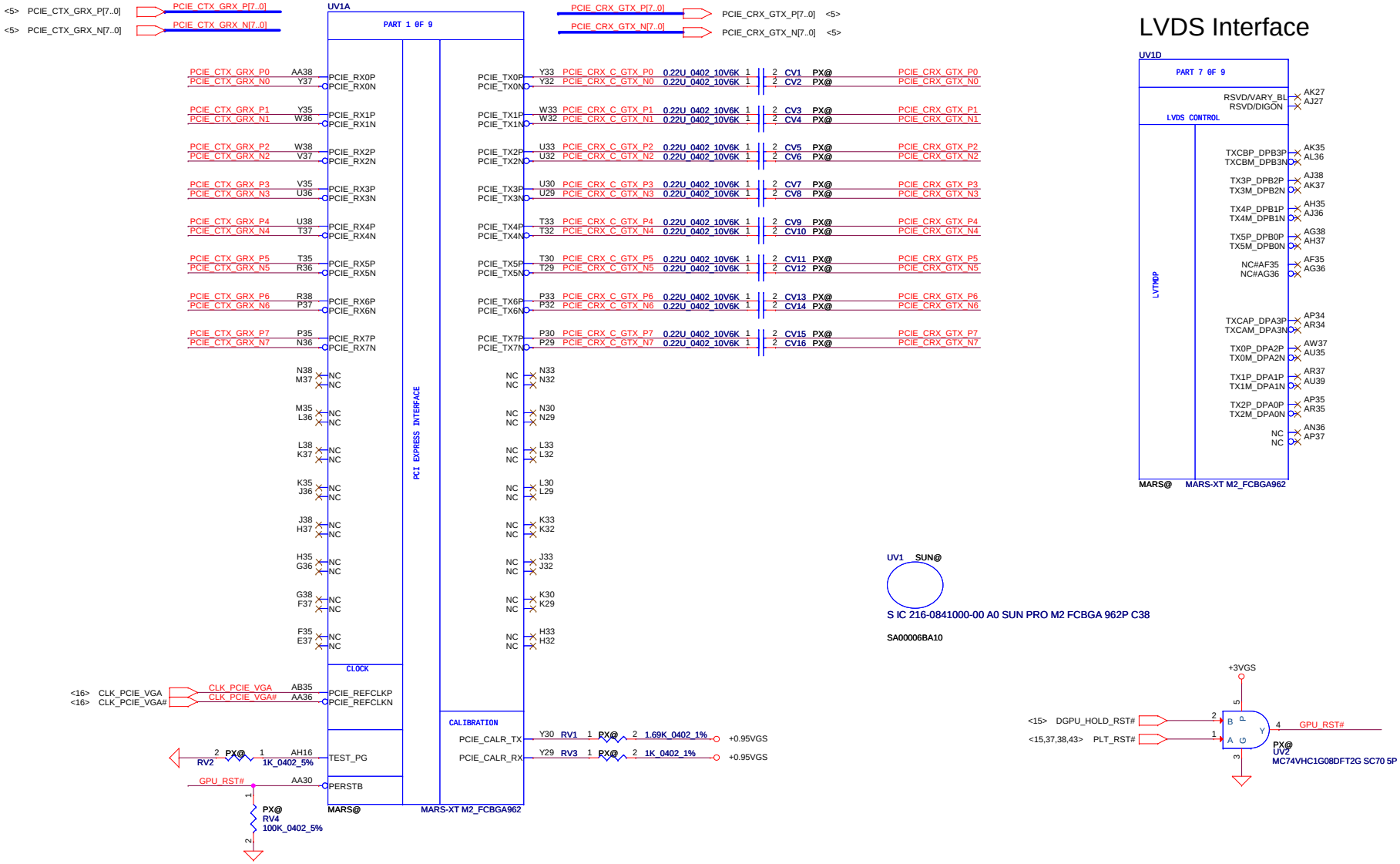
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 22 of 61



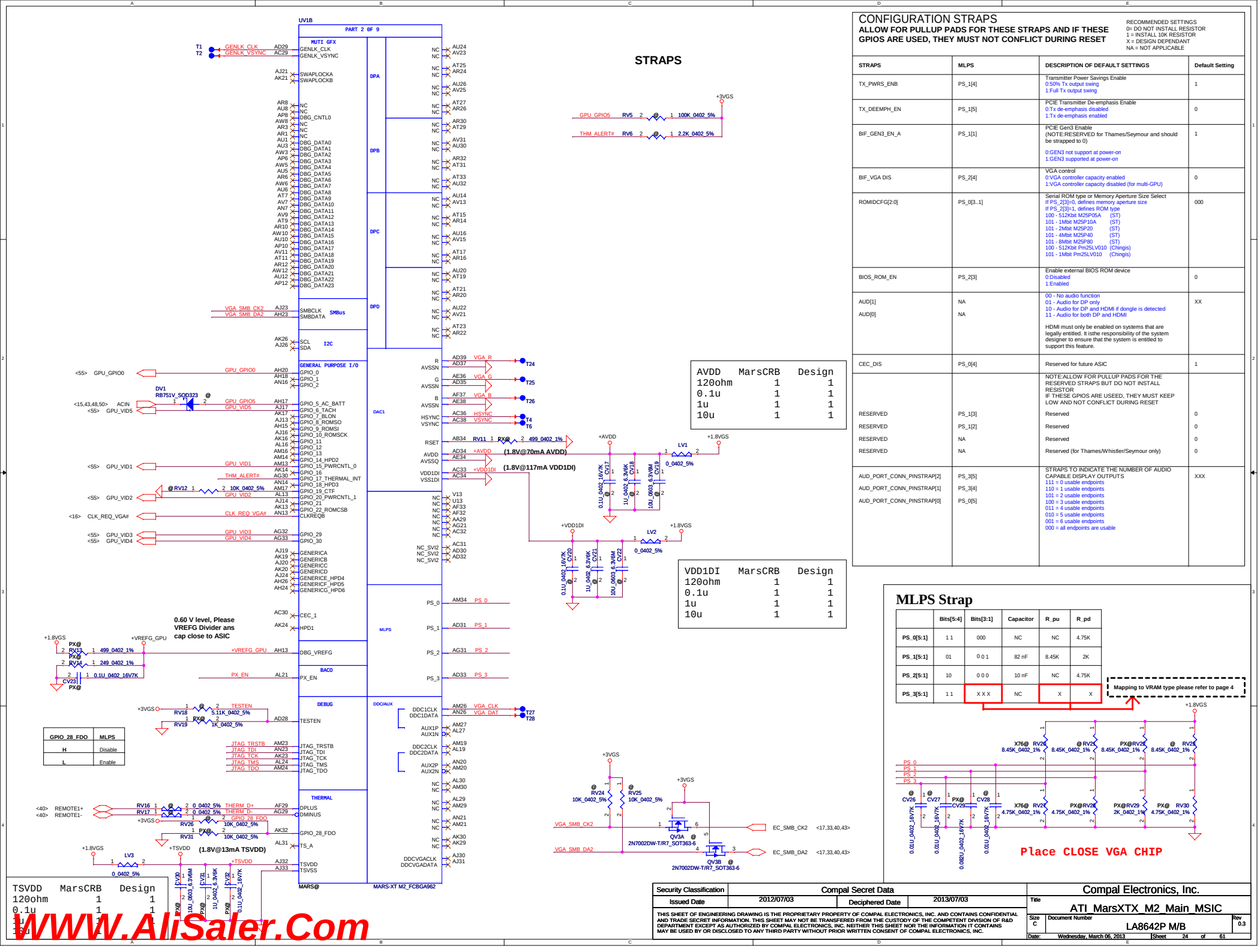
LVDS Interface

UV1 SUN@

S IC 216-0841000-00 A0 SUN PRO M2 FCBGA 962P C38

SA00006BA10

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2012/07/03	Deciphered Date 2013/07/03	Title: ATI_MarsXTX_M2_PCIE/LVDS
			Size: Custom; Document Number: LA8642P M/B; Rev: 0.3
			Date: Wednesday, March 06, 2013; Sheet 23 of 61


UV1B
PART 2 OF 9
MUTI GFX
GENERAL PURPOSE I/O
I2C
SMBus
DPA
DPB
DPC
DPD
DAC1
MLPS
BACO
DEBUG
THERMAL
DDC/AUX
MARS@
MARS-XT M2_FCBGA962
STRAPS
CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET
RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
STRAPS | MLPS | DESCRIPTION OF DEFAULT SETTINGS | Default Setting
TX_PWRS_ENB | PS_1[4] | Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing | 1
TX_DEEMPH_EN | PS_1[5] | PCIE Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled | 0
BIF_GEN3_EN_A | PS_1[1] | PCIE Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on | 1
BIF_VGA DIS | PS_2[4] | VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU) | 0
ROMIDCFG[2:0] | PS_0[3..1] | Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV010 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis) | 000
BIOS_ROM_EN | PS_2[3] | Enable external BIOS ROM device 0:Disabled 1:Enabled | 0
AUD[1] AUD[0] | NA NA | 00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It isthe responsibility of the system designer to ensure that the system is entitled to support this feature. | XX
CEC_DIS | PS_0[4] | Reserved for future ASIC | 1
RESERVED | PS_1[3] | NOTE:ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOS ARE USEED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved | 0
RESERVED | PS_1[2] | Reserved | 0
RESERVED | NA | Reserved | 0
RESERVED | NA | Reserved (for Thames/Whistler/Seymour only) | 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0] | PS_3[5] PS_3[4] PS_0[5] | STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable | XXX
AVDD MarsCRB Design
120ohm 1 1
0.1u 1 1
1u 1 1
10u 1 1
VDD1DI MarsCRB Design
120ohm 1 1
0.1u 1 1
1u 1 1
10u 1 1
MLPS Strap
Bits[5:4] Bits[3:1] Capacitor R_pu R_pd
PS_0[5:1] 1 1 000 NC NC 4.75K
PS_1[5:1] 01 0 0 1 82 nF 8.45K 2K
PS_2[5:1] 10 0 0 0 10 nF NC 4.75K
PS_3[5:1] 1 1 X X X NC X X
Mapping to VRAM type please refer to page 4
Place CLOSE VGA CHIP
GPIO_28_FDO MLPS
H Disable
L Enable
TSVDD MarsCRB Design
120ohm 1 1
0.1u 1 1
1u 1 1
10u 1 1
0.60 V level, Please VREFG Divider ans cap close to ASIC
(1.8V@70mA AVDD)
(1.8V@117mA VDD1DI)
(1.8V@13mA TSVDD)
Security Classification Compal Secret Data
Issued Date 2012/07/03 Deciphered Date 2013/07/03
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Compal Electronics, Inc.
Title ATI_MarsXTX_M2_Main_MSIC
Size C Document Number LA8642P M/B Rev 0.3
Date: Wednesday, March 06, 2013 Sheet 24 of 61
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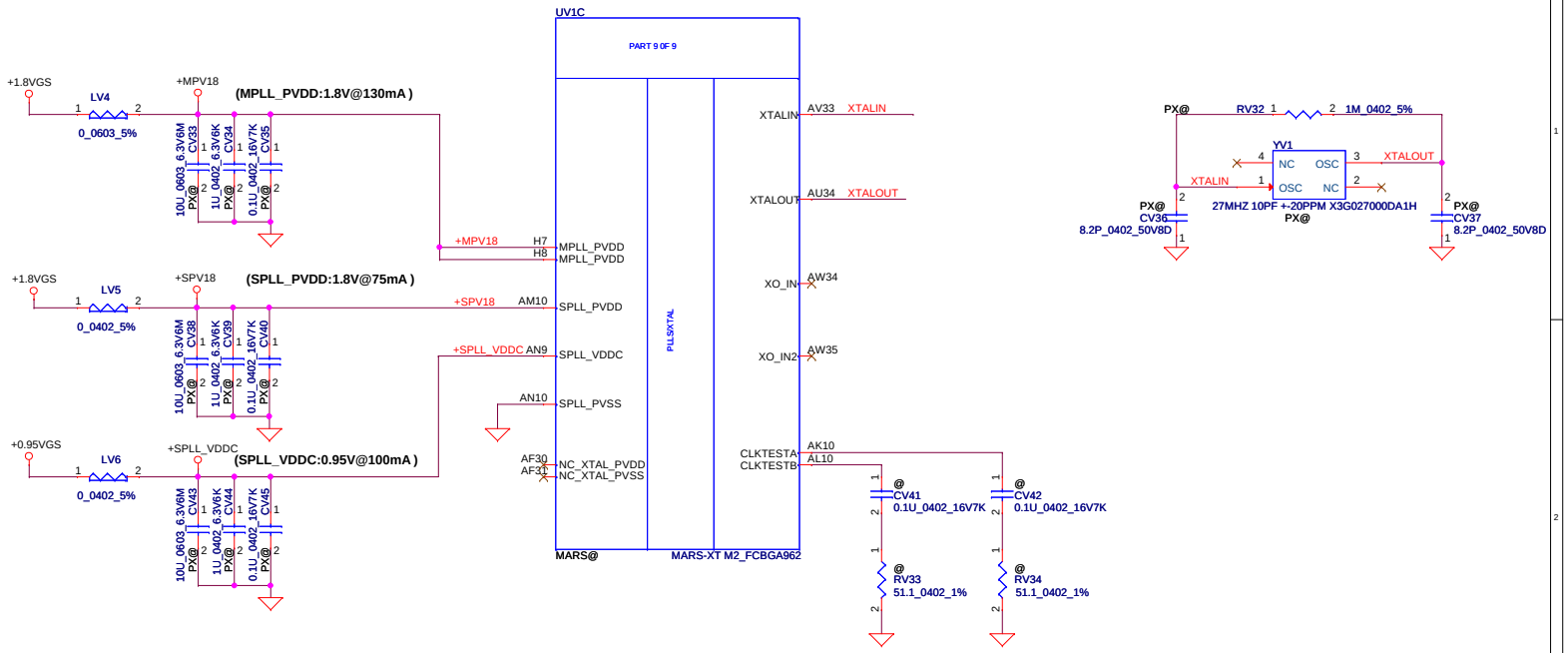
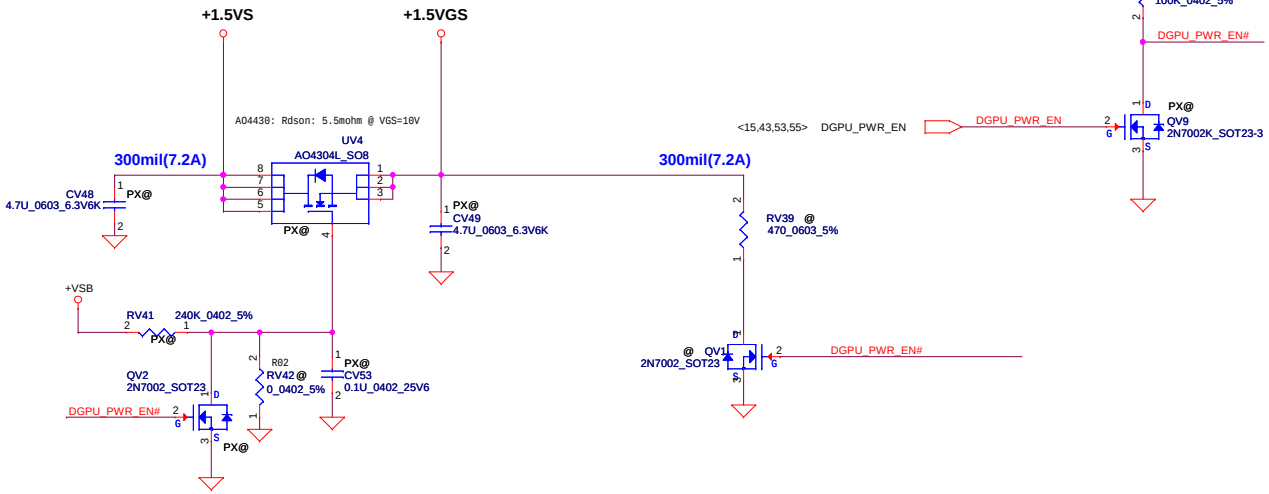
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

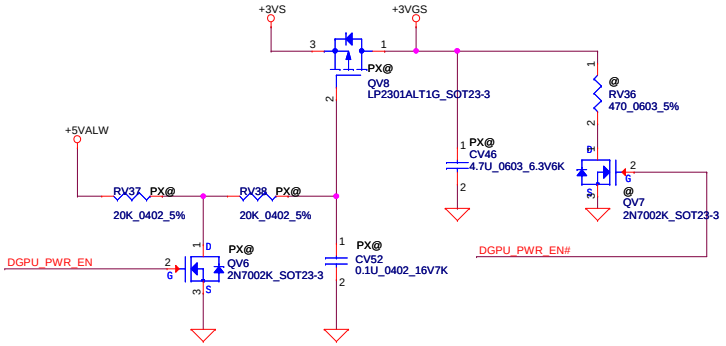
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



+1.5VS to +1.5VGS Transfer



<+3VS TO +3VGS>



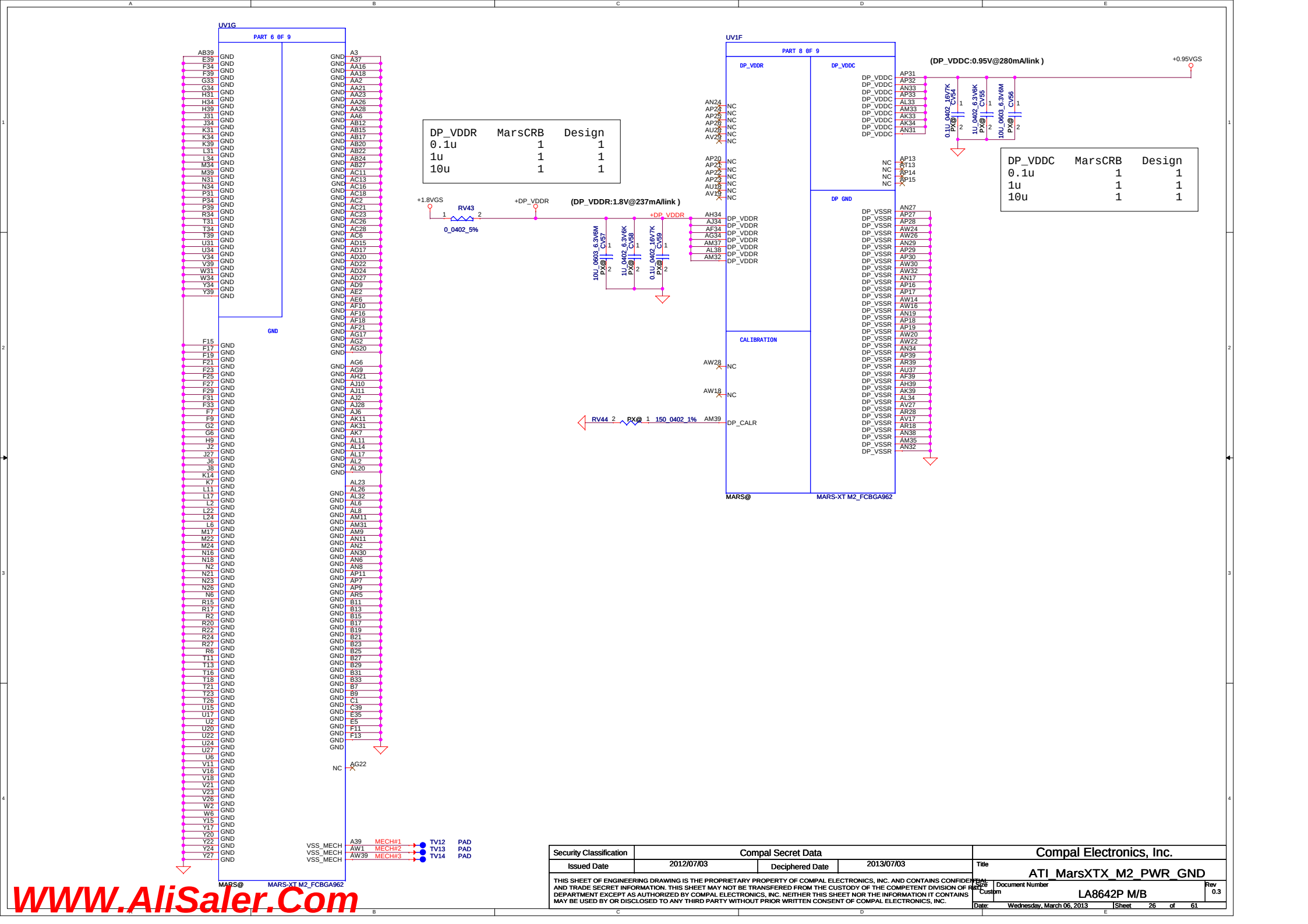
Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_BACO POWER

Size: Custom | Document Number: LA8642P M/B | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 25 of 61



Security Classification	Compal Secret Data		
Issued Date	2012/07/03	Deciphered Date	2013/07/03

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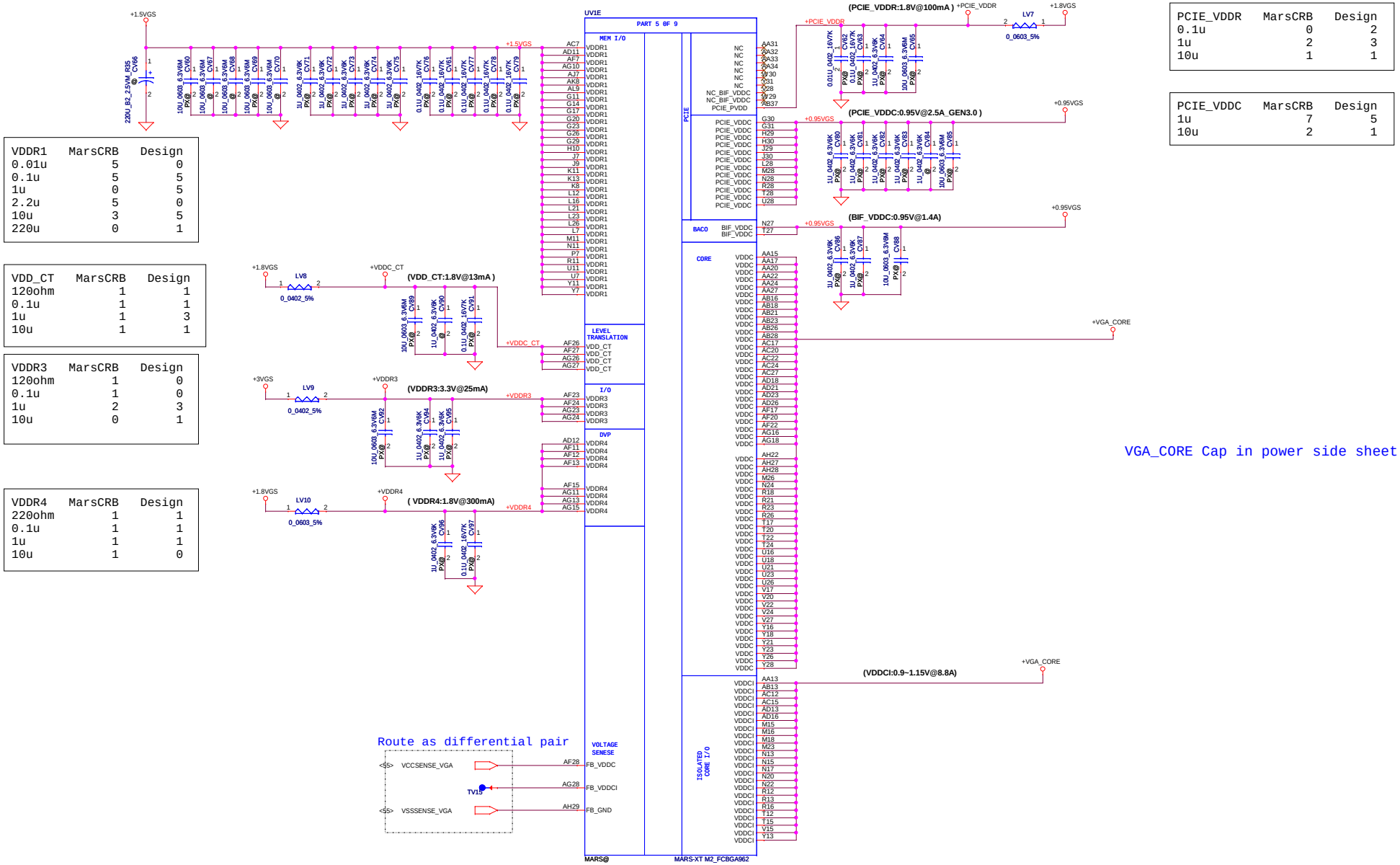
Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_PWR_GND

Size: Custom | Document Number: LA8642P M/B | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 26 of 61



Route as differential pair

VGA_CORE Cap in power side sheet

VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

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Issued Date	2012/07/03	Deciphered Date 2013/07/03	Title: ATI_MarsXTX_M2_Power

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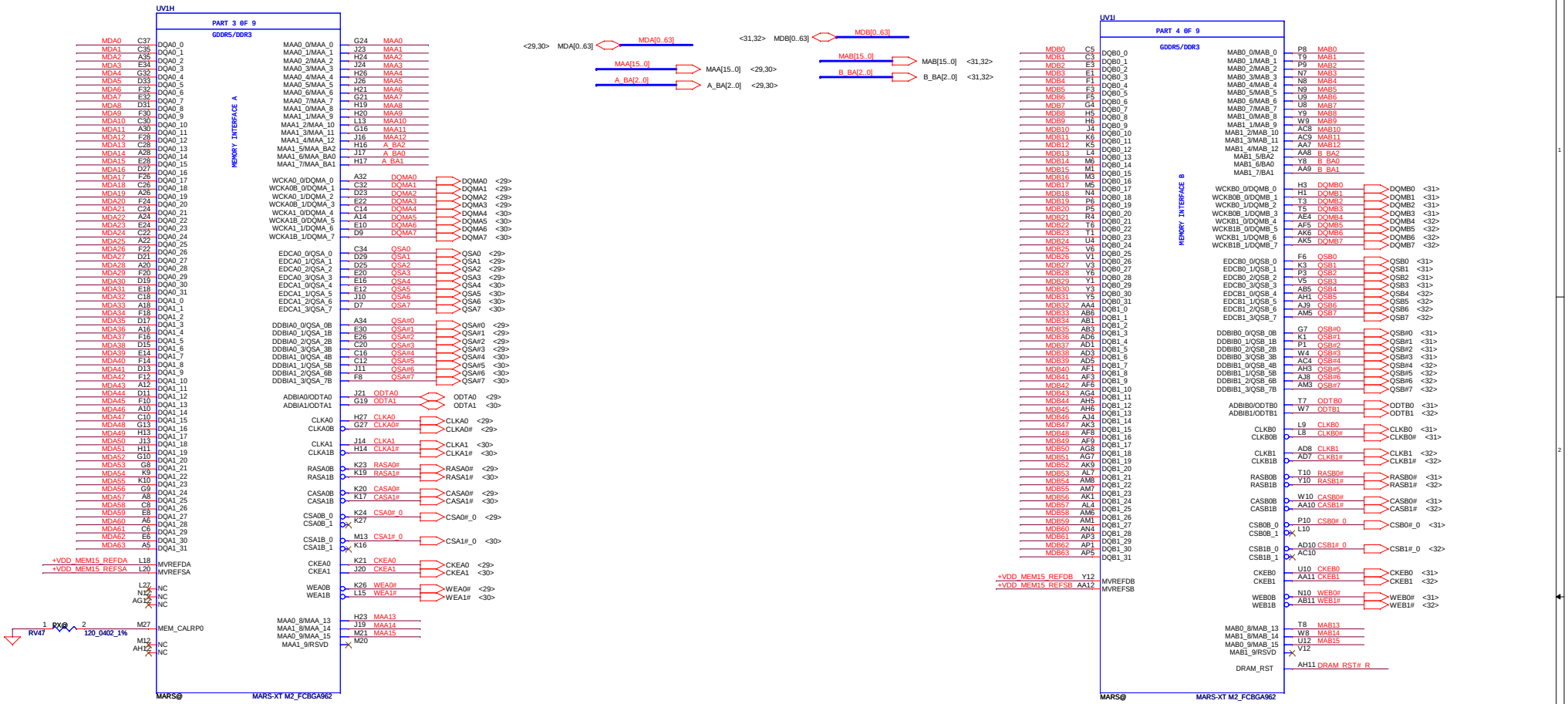
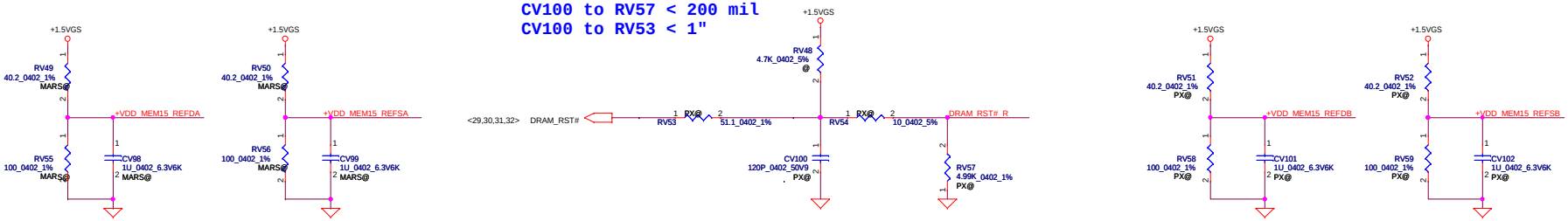
C	LA8642P M/B	0.3
Date: Wednesday, March 06, 2013	Sheet 27 of 61	



Ball to RV57 < 1"
CV100 to RV57 < 200 mil
CV100 to RV53 < 1"



DRAM_RST# is a daisy-chain net that connects to all VRAM

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: ATI_MarsXTX_M2_MEM IF

Size	Document Number	Rev
C	LA8642P M/B	0.3

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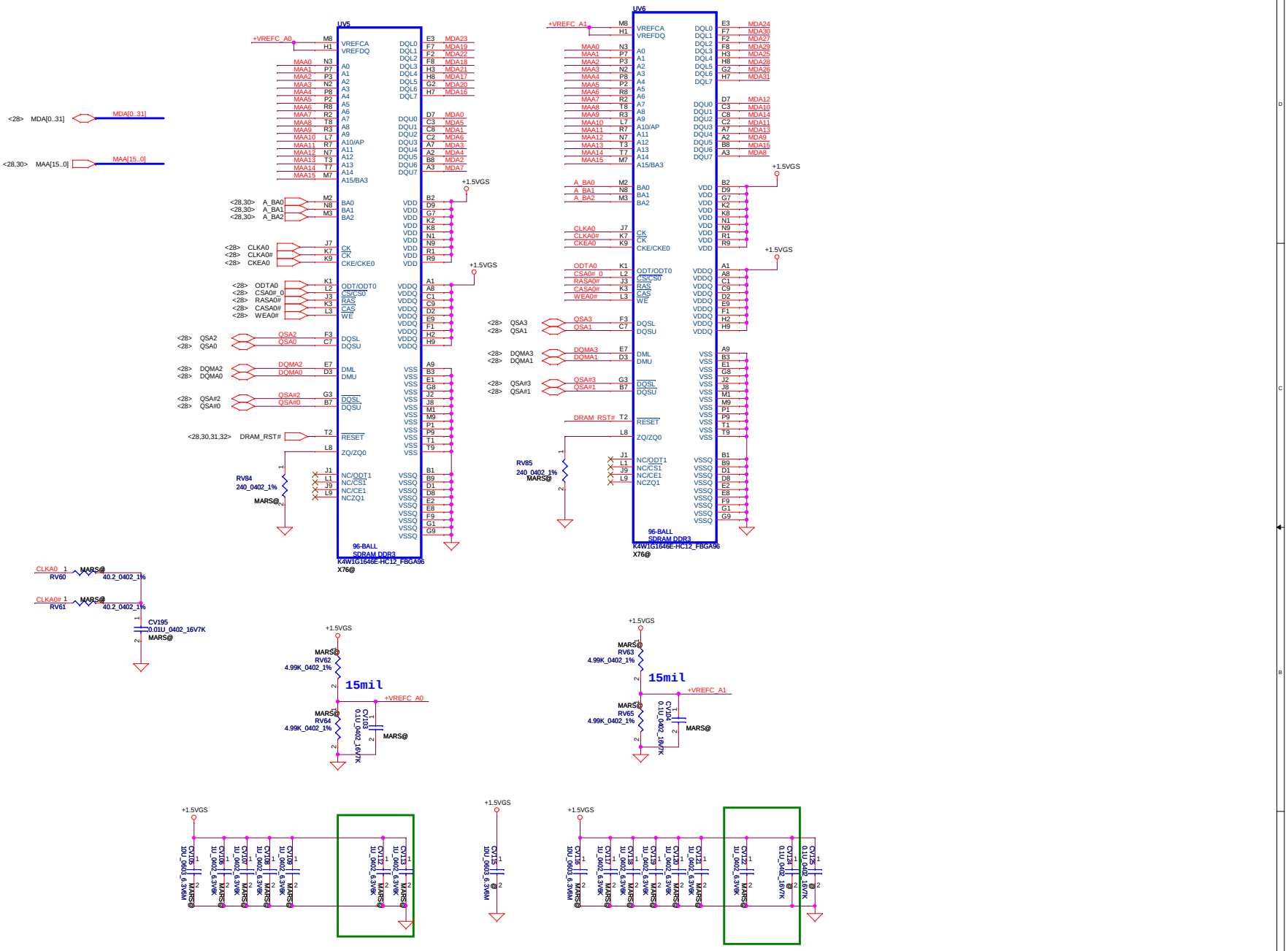


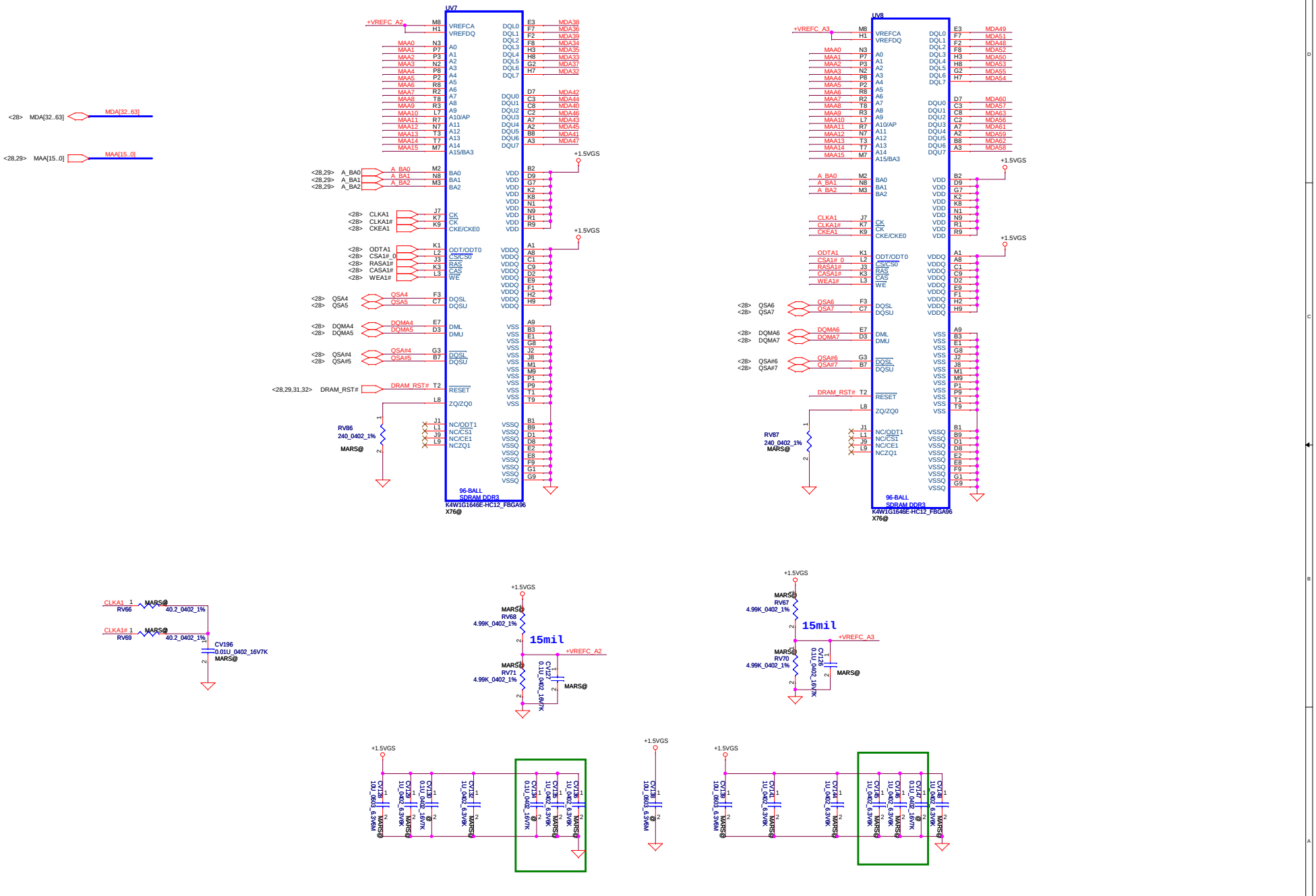
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	QIQY2 LA6884P	0.3

Date: Wednesday, March 06, 2013 | Sheet 29 of 61



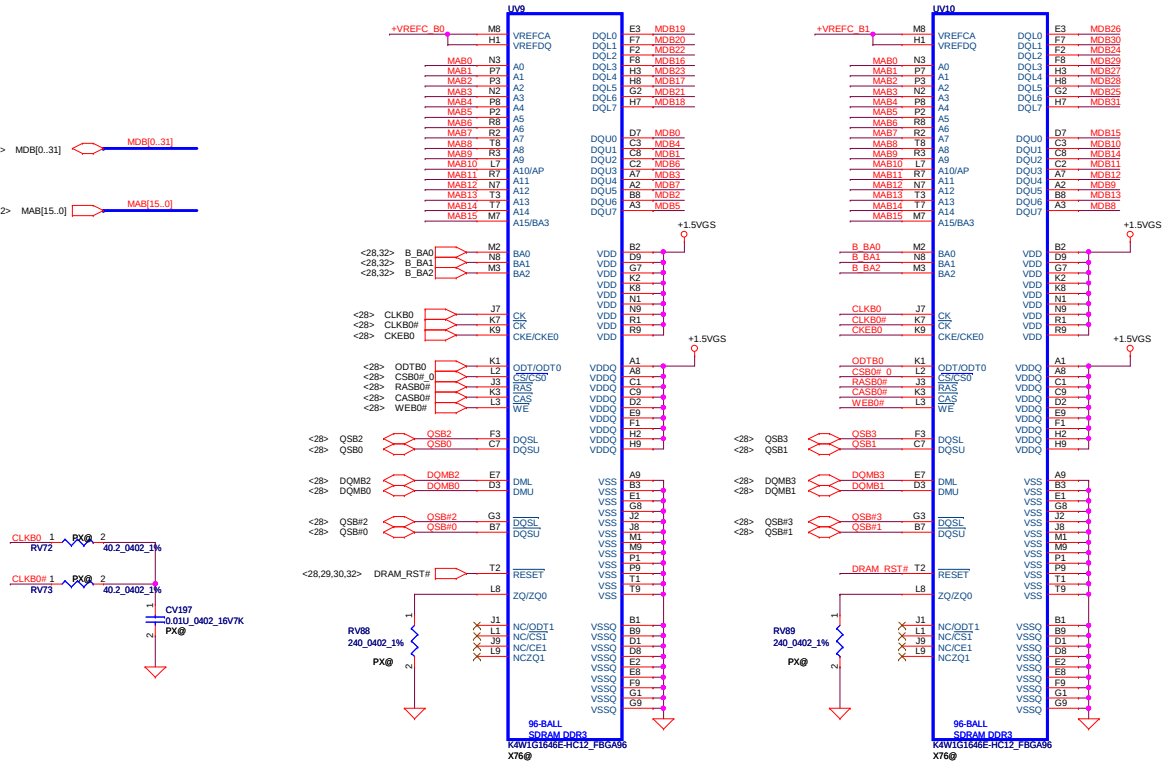
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

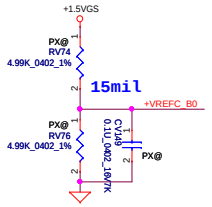
Compal Electronics, Inc.

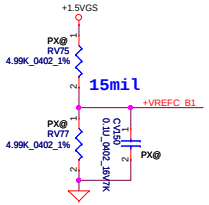
Title: ATI_Whistler_M2_VRAM_A

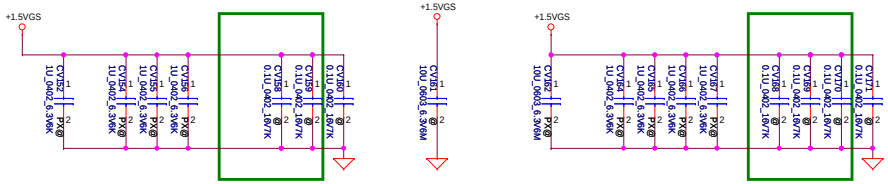
Size	Document Number	Rev
C	QIQY2 LA6884P	0.3

Date: Wednesday, March 06, 2013 | Sheet 30 of 61









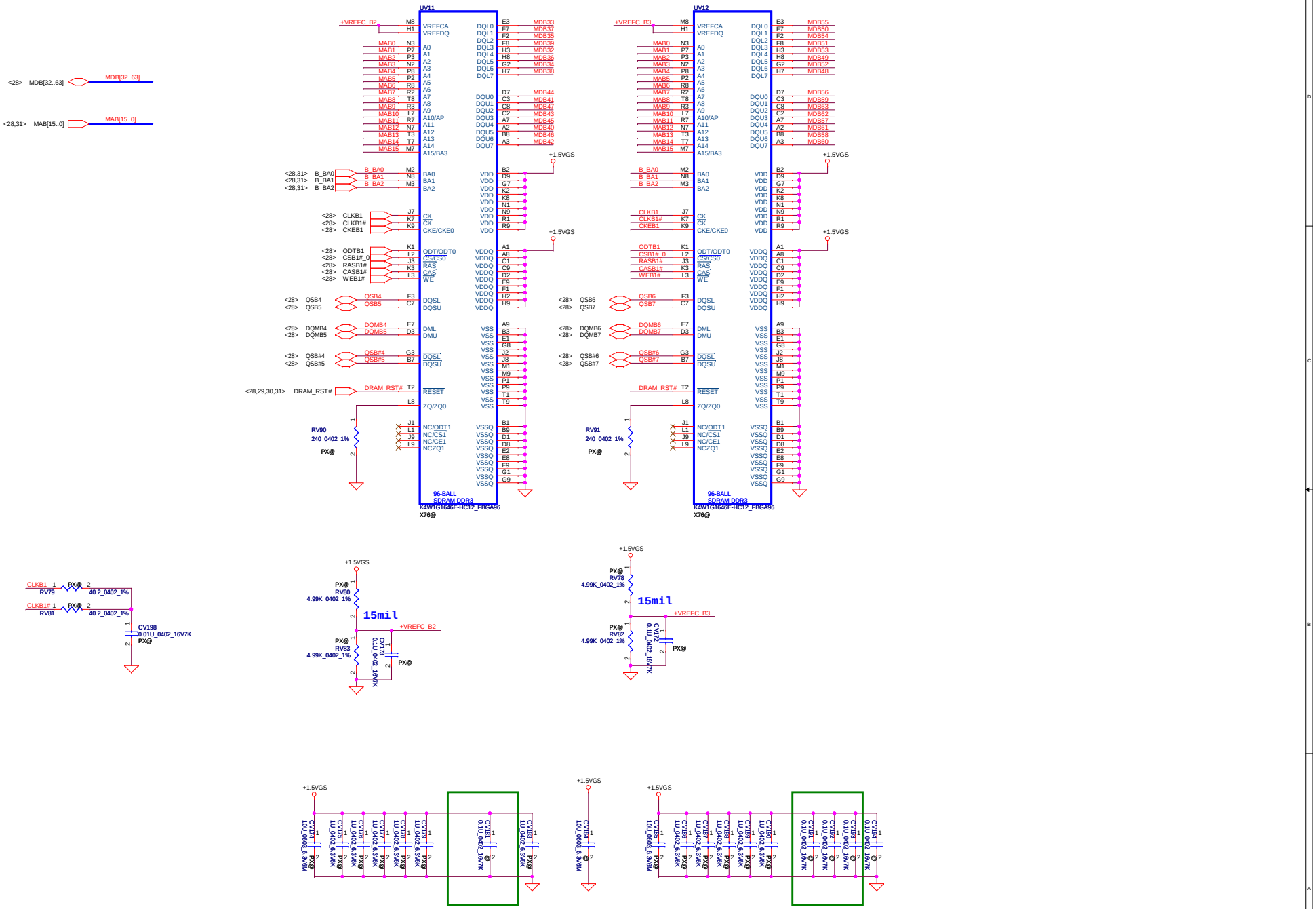
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_B

Size	Document Number	Rev
C	QIQY2 LA6884P	0.3

Date: Wednesday, March 06, 2013 | Sheet 31 of 61



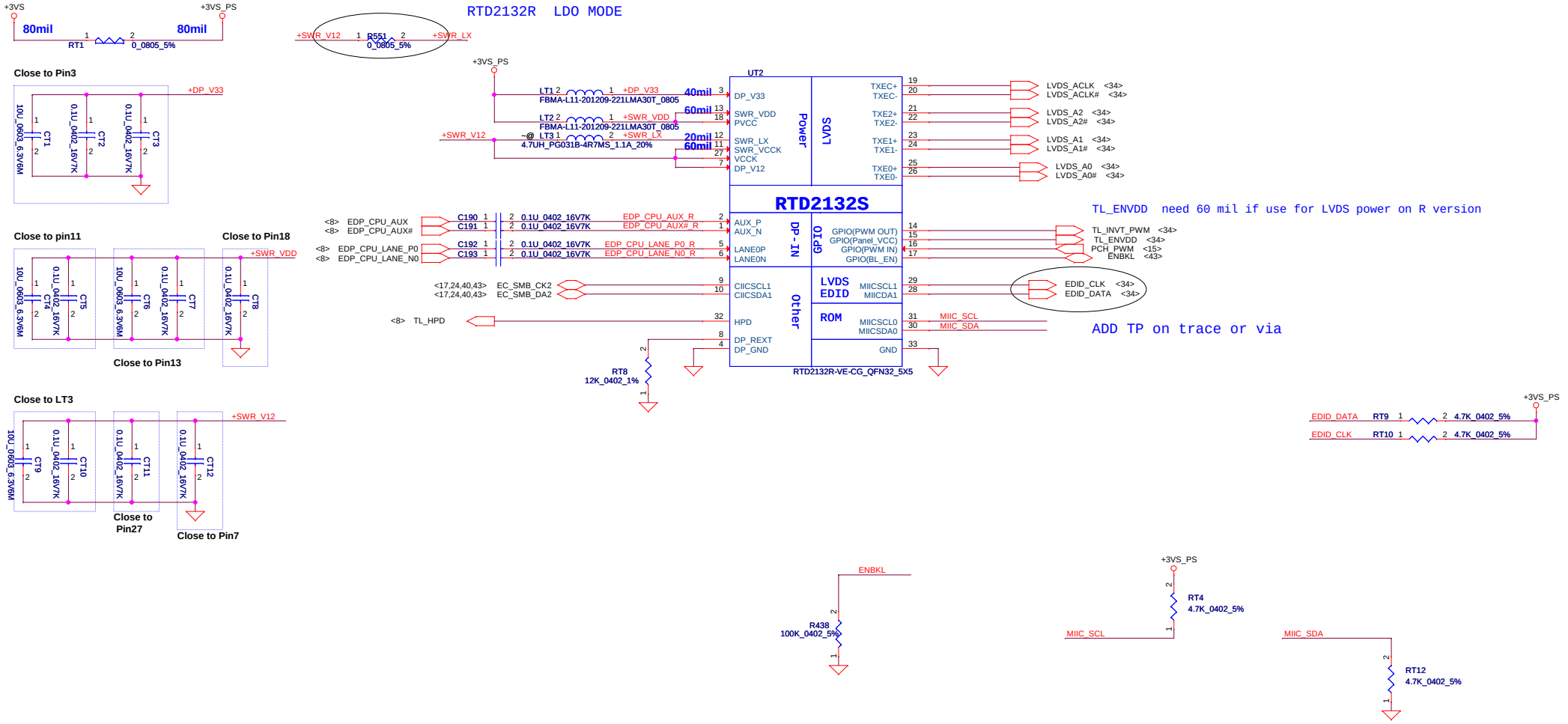
Security Classification	Compal Secret Data		
Issued Date	2010/08/25	Deciphered Date	2012/08/25

Compal Electronics, Inc.

Title: ATI_Whistler_M2_VRAM_A

Size	Document Number	Rev
C	QIQY2 LA6884P	0.3

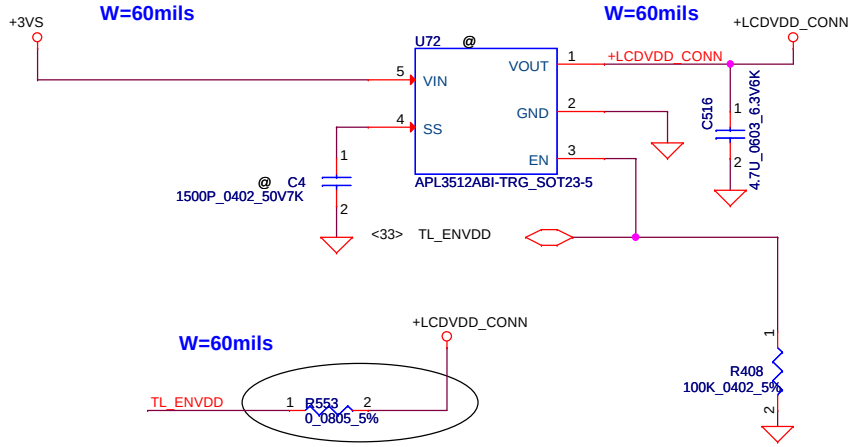
Date: Wednesday, March 06, 2013 | Sheet 32 of 61



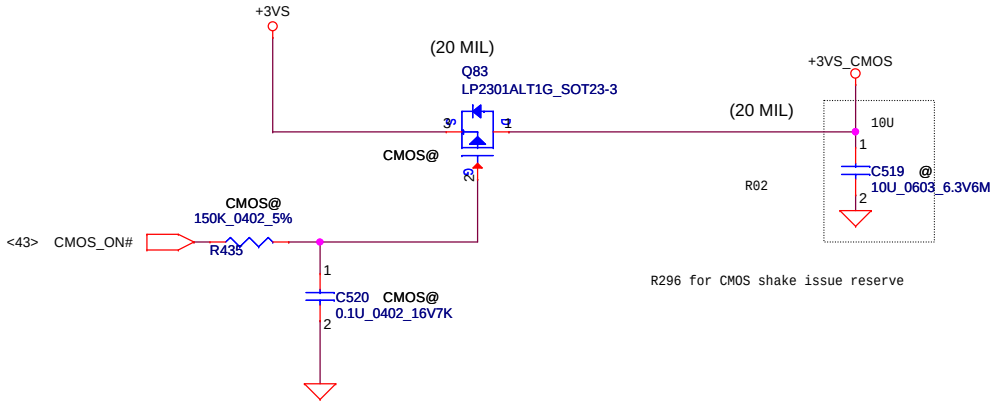
MIIC_SCL \ MIIC_SDA	0	1
0	X	EC CODE
1	Internal ROM	EEPROM

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/30	Deciphered Date 2013/06/30	Title: LVDS Translator - RTD2132S
			Size: Custom; Document Number: LA-9641P; Rev: 0.3
			Date: Wednesday, March 06, 2013; Sheet 33 of 61

LCD POWER CIRCUIT

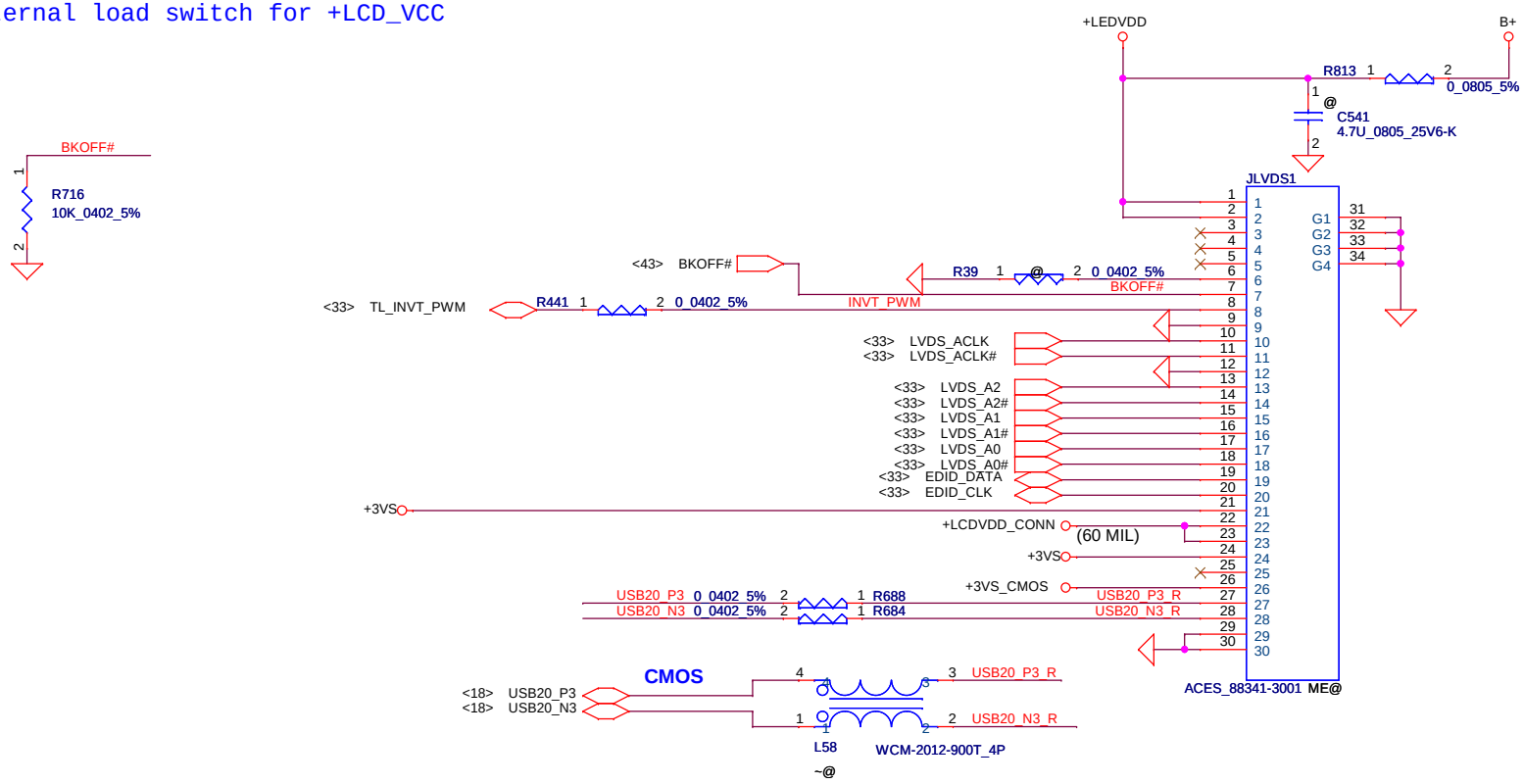


CMOS Camera



RTD2132R Internal load switch for +LCD_VCC

VGA LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

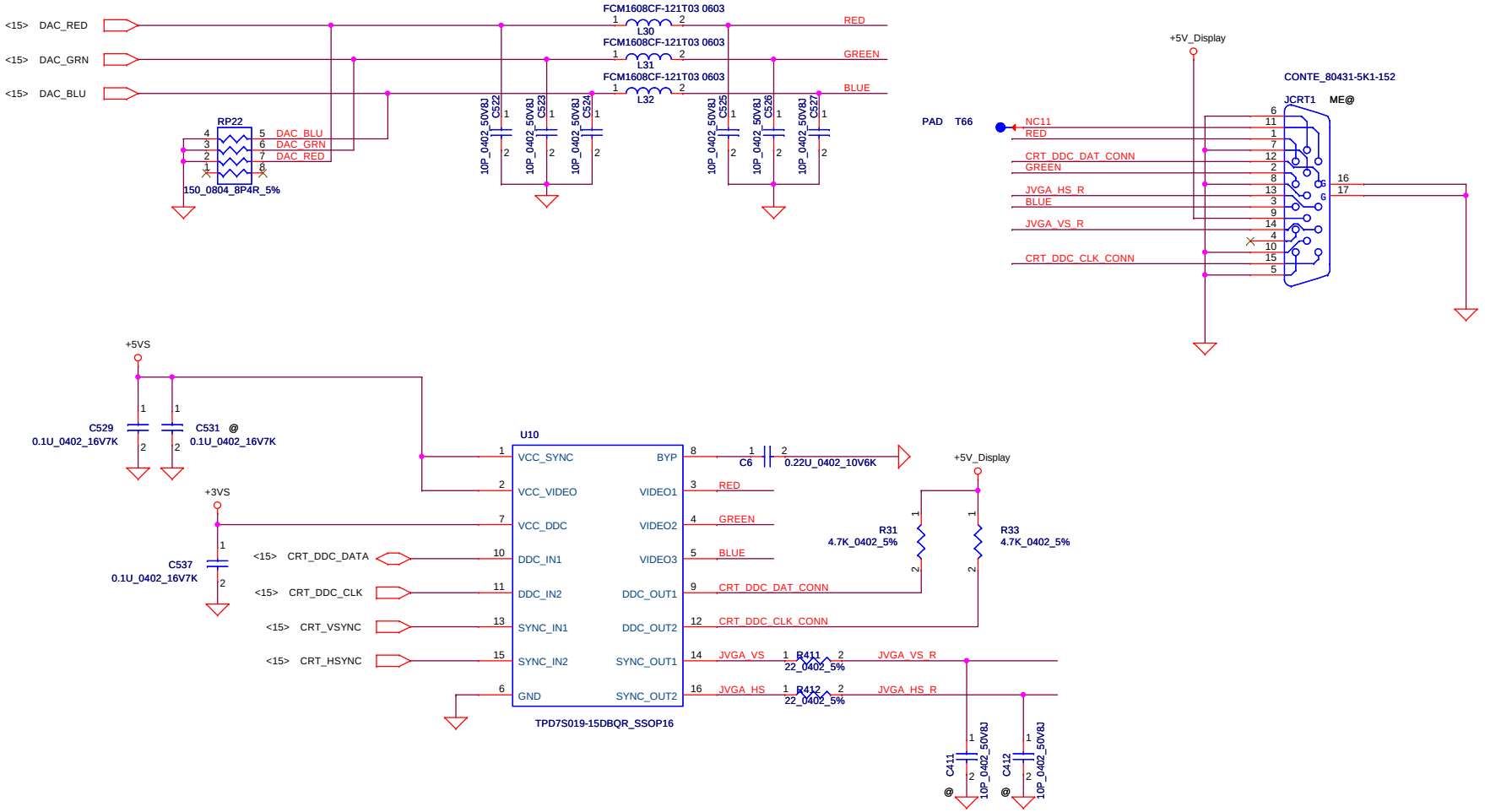
Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	LA-9641P	0.3

Date: Wednesday, March 06, 2013 Sheet 34 of 61

CRT Connector



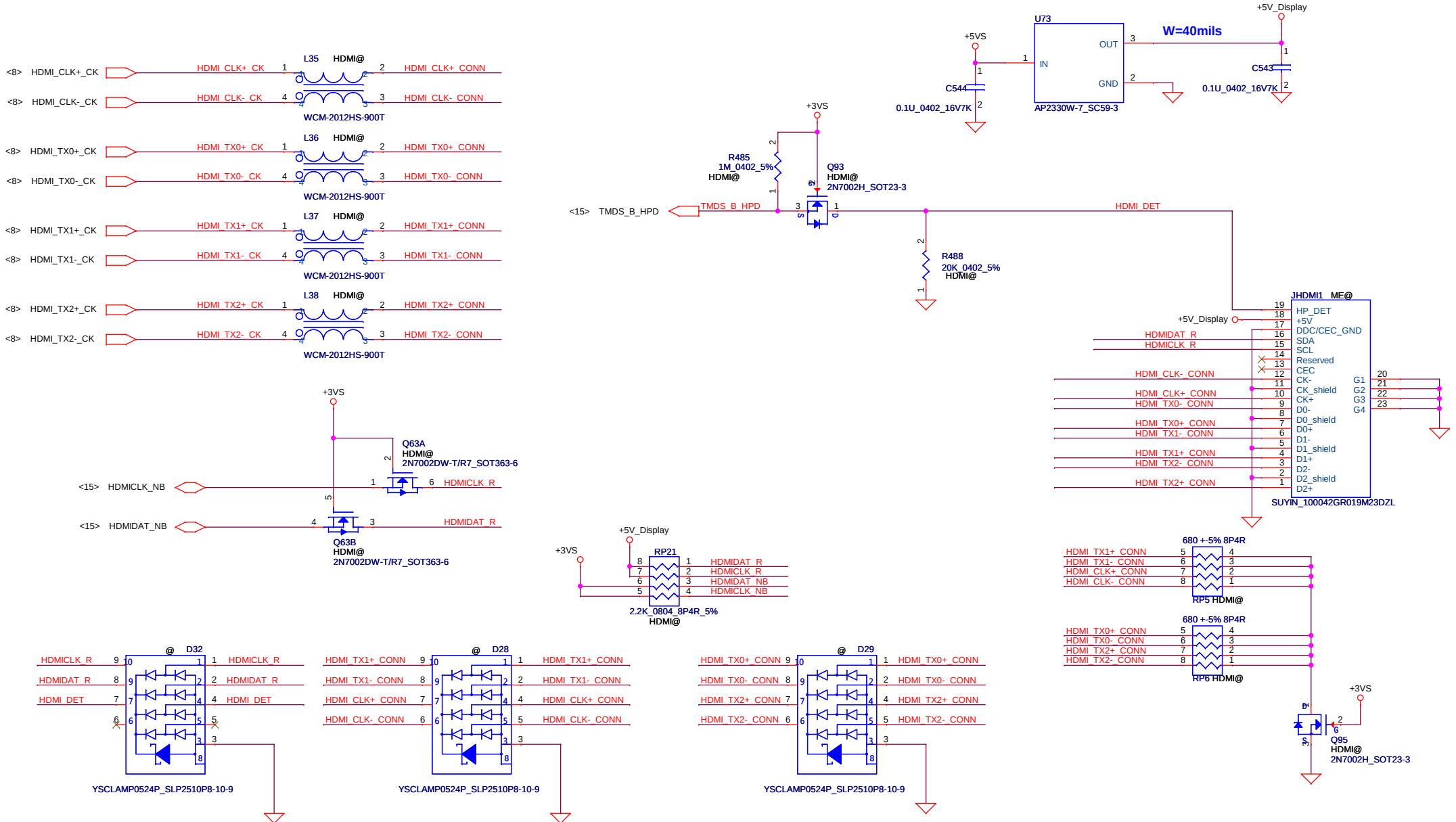
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 35 of 61



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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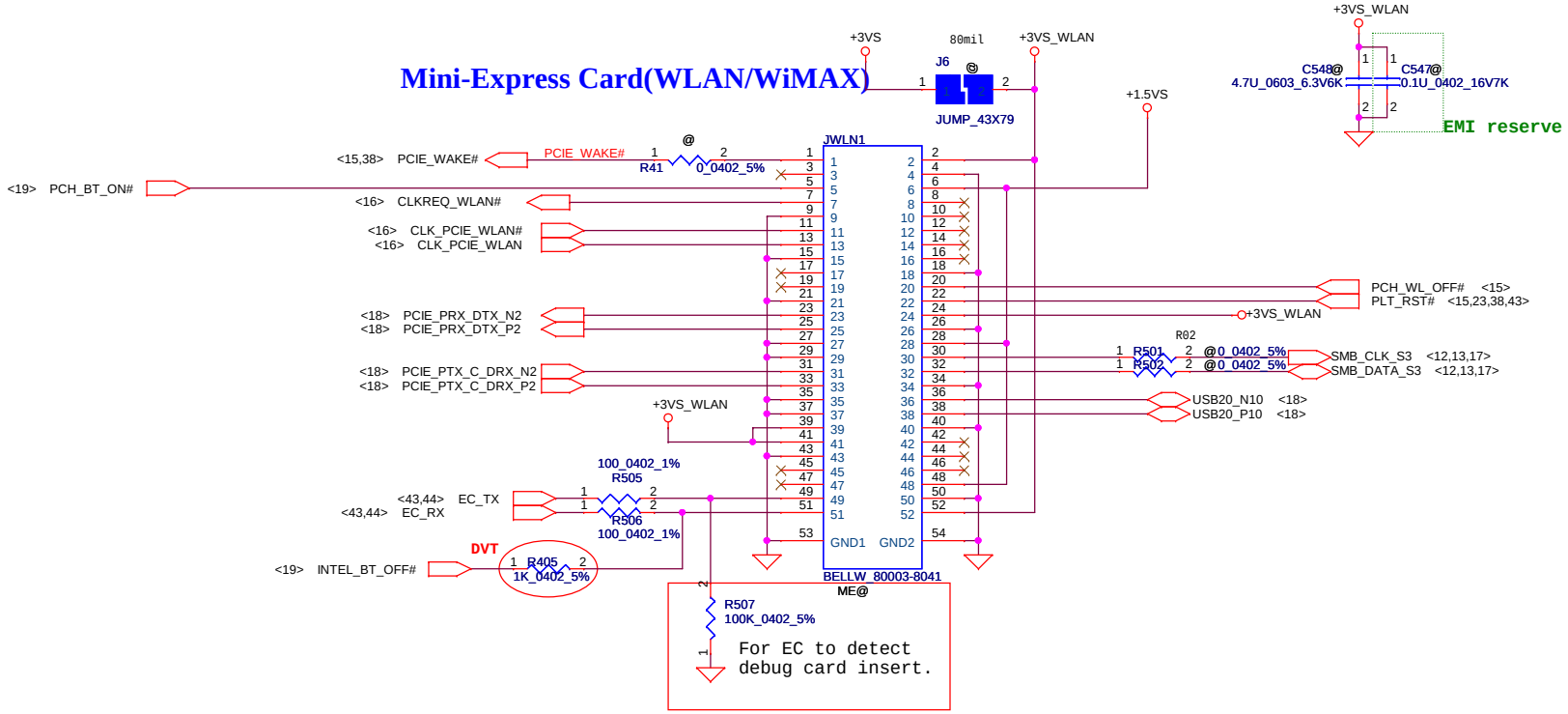
Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
B	LA-9641P	0.3

Date: Wednesday, March 06, 2013 Sheet 36 of 61

Mini-Express Card for WLAN/WiMAX(Half)



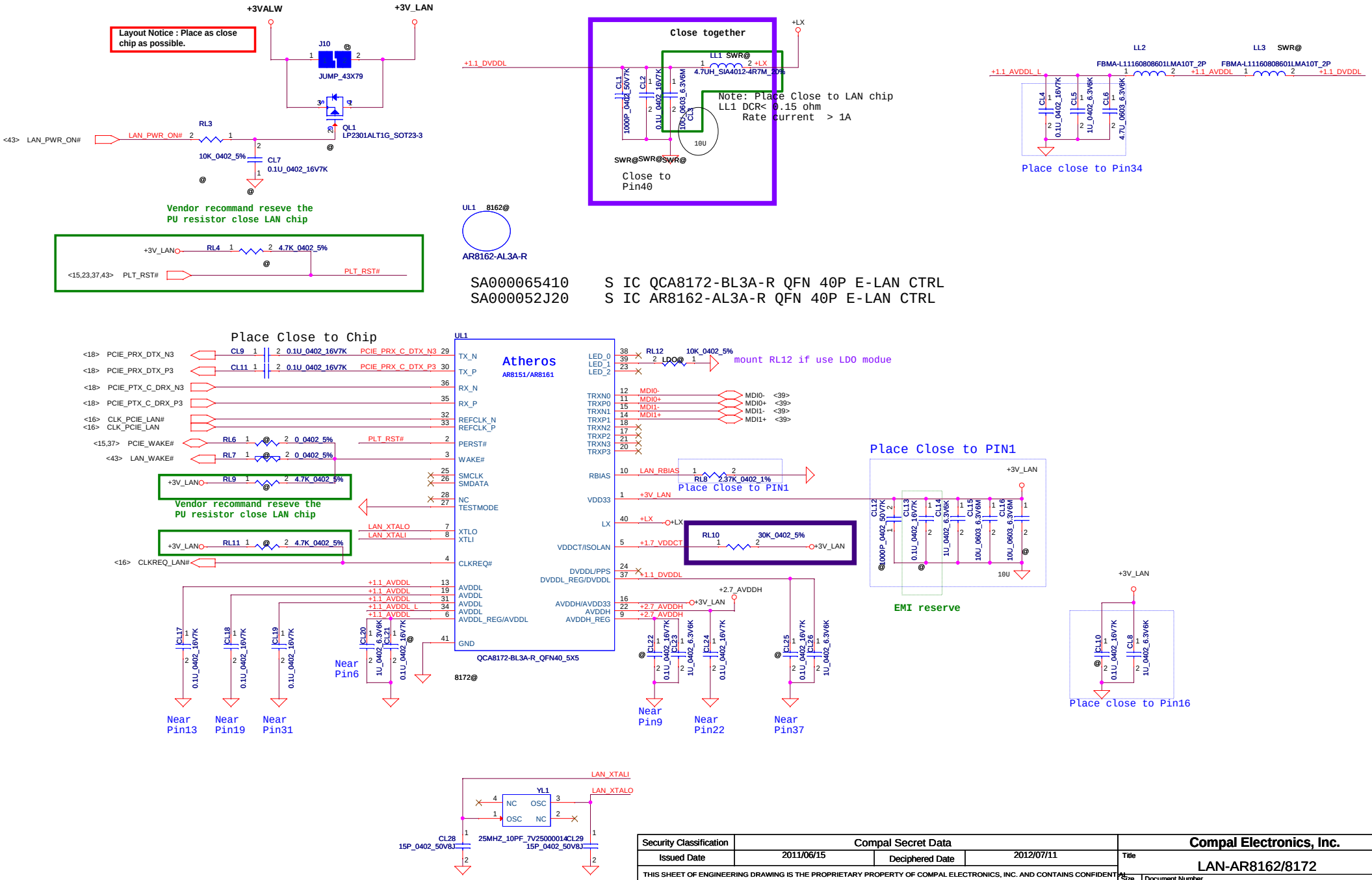
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: Mini-Card/NEW Card/SIM

Size | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 37 of 61

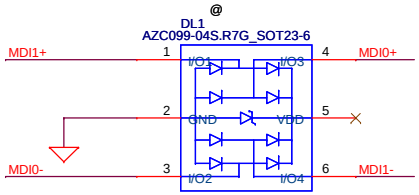


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

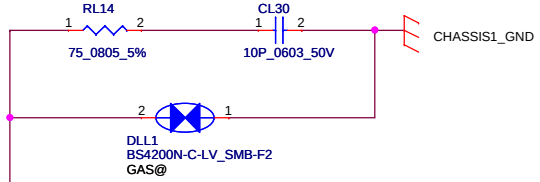
Compal Electronics, Inc.	
Title	LAN-AR8162/8172
Size: Custom	Document Number: LA-7982P
Rev	0.3
Date:	Wednesday, March 06, 2013
Sheet	38 of 61

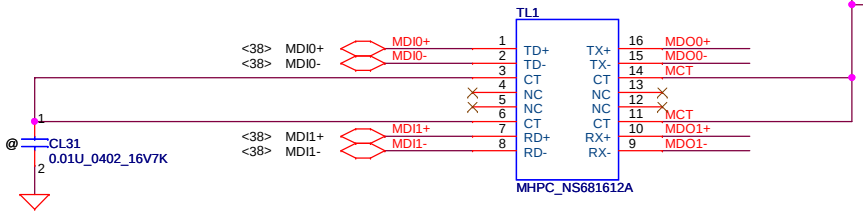
Place Close to TL1

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

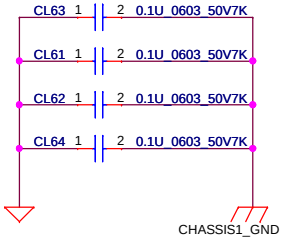


Reserve gas tube for EMI go rural solution

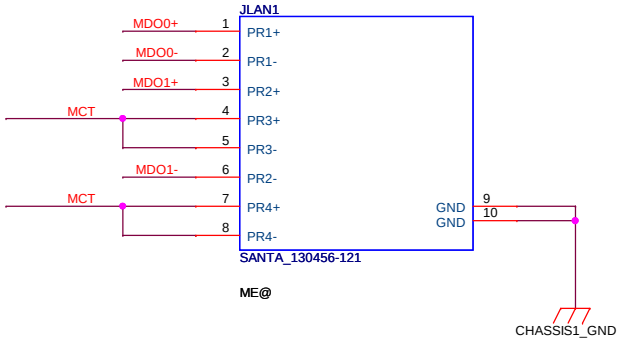




Place Close to TL1

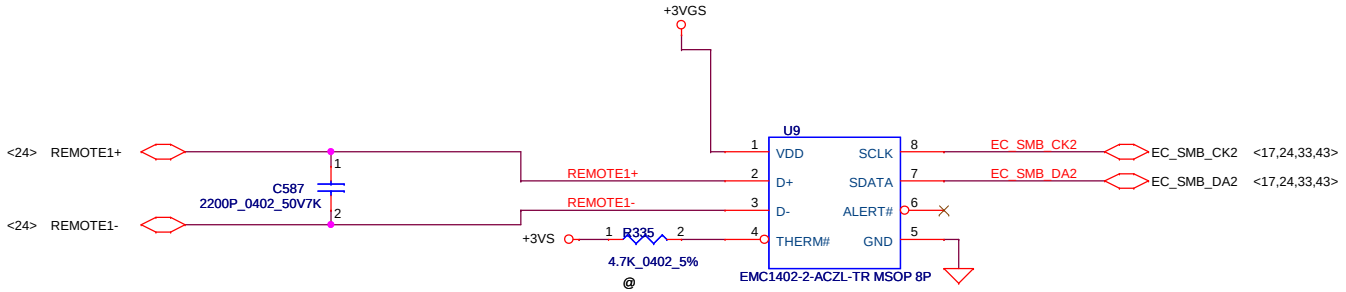


Need check Symbol



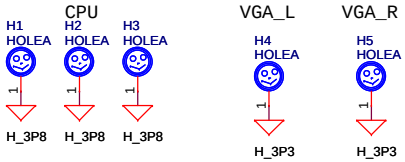
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	LAN_Transformer		
Size B	Document Number LA-7982P		Rev 0.3
Date: Wednesday, March 06, 2013	Sheet 39 of 61		



EMC1412-A (SA00003YA00)
Address 1111_100xb
S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

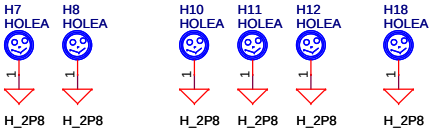


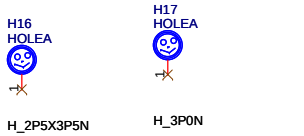
A

B

M/B 橢圓孔

M/B 圓孔



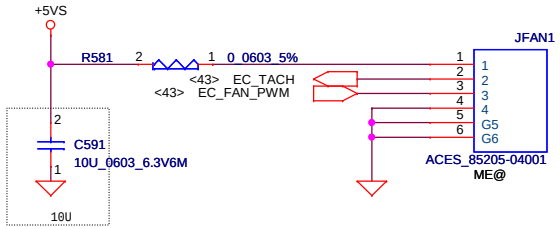


2P8 * 7 pcd

D

E

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

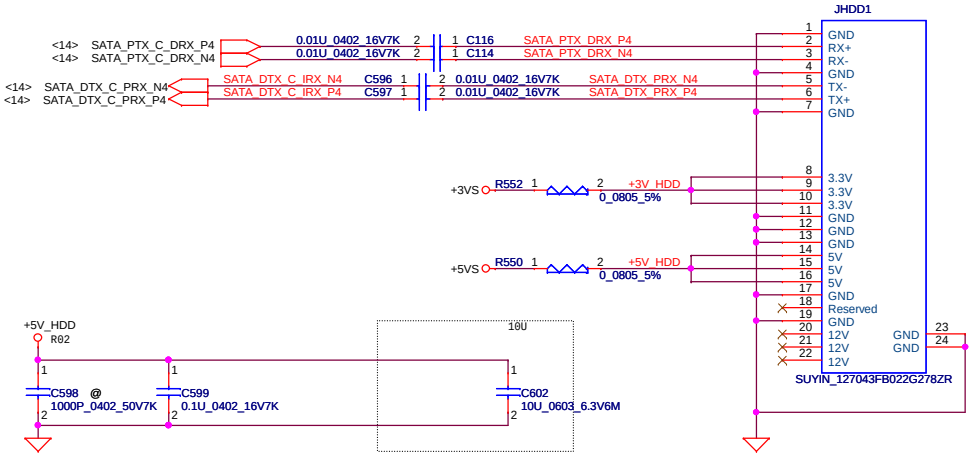
Compal Electronics,Ltd.

Title: Fintek-Thermal IC/FAN/screw

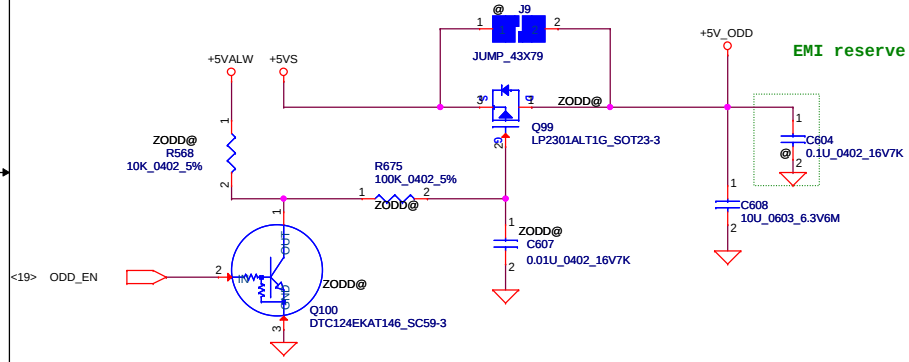
Size: B | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 40 of 61

SATA HDD Conn.

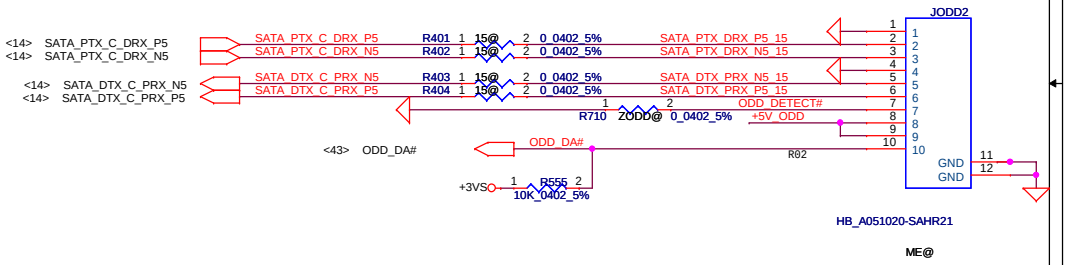


ODD Power Control



FOR 15"

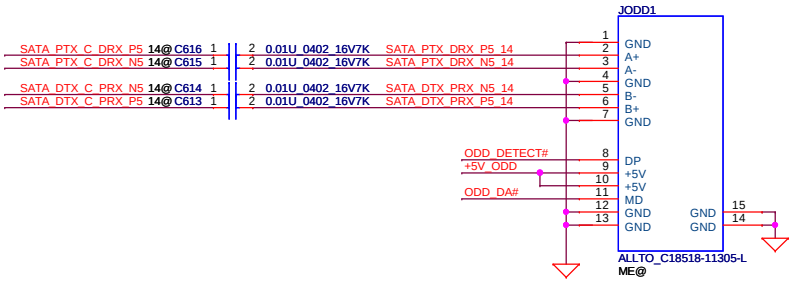
SATA ODD FFC Conn.



Co-lay

FOR 14"

SATA ODD Conn.



Compal Electronics, Inc.

Title: HDD/ODD/BT Connector

Size: Custom | Document Number: LA-9641P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 41 of 61

CX20751
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

Sense resistors must be connected same power that is used for VAUX_3.3

mount RA6 on the Jack Sense circuit to configure Port-C for mono MIC.

Don't support LINE_IN function RA7 could be @

CA3 vendor suggest change to 2.2U

AVDD_3.3 pinis output of internal LDO. NOT connect to external supply.

Should be same supply rail as used for PCH HDA bus controller section

Layout Note:Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

Please bypass caps very close to device.

Check footprint

HGNDA, HGNDB 80mils

10 mils

using wide copper bridge under codec (100 mils or more)

Universal Jack
External MIC

Internal analog MIC

Headphone

Internal SPEAKER

EMI request reserve RA21 & CA7

CA30 vendor suggest change to 2.2U

for Universal jack

follow vendor suggest & reserver default design

Place colose to Codec chip

CA41 vendor suggest change to 1U

LA1~LA4 vendor suggest mount 0 ohm first~ Bead reserve for EMI if needed

wide 20MIL

vendor suggest change to 1000p

PC Beep

EC Beep

ICH Beep

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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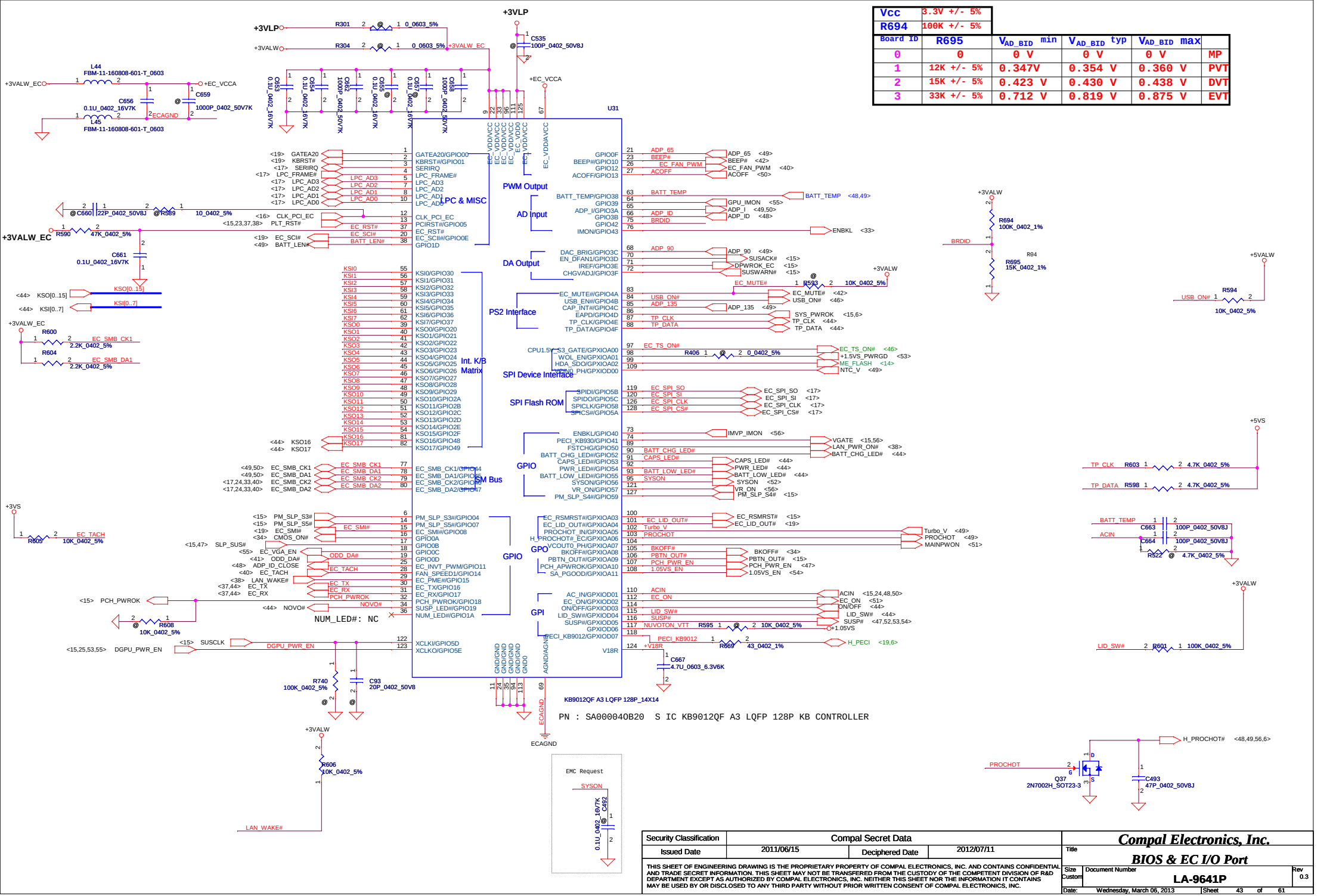
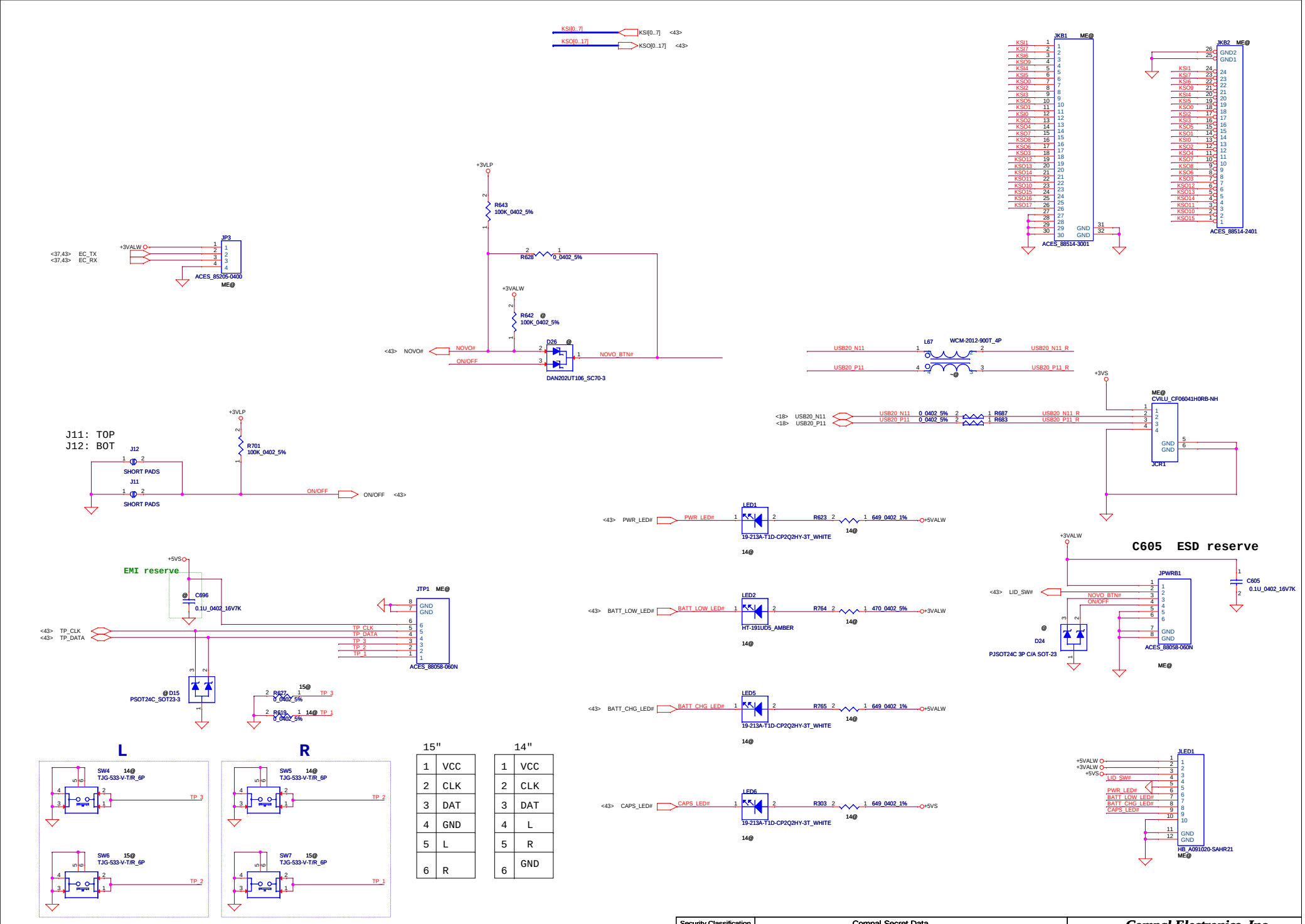
Compal Electronics, Inc.

Title: CX20751 Codec

Size: Custom | Document Number: LA-7982P | Rev: 0.3

Date: Wednesday, March 06, 2013 | Sheet 42 of 61





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: ROM/KBD/PWR/CR/LED/TP Conn.

Size	Document Number	Rev
C	LA-9641P	0.3

Date: Wednesday, March 06, 2013 Sheet 44 of 61

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

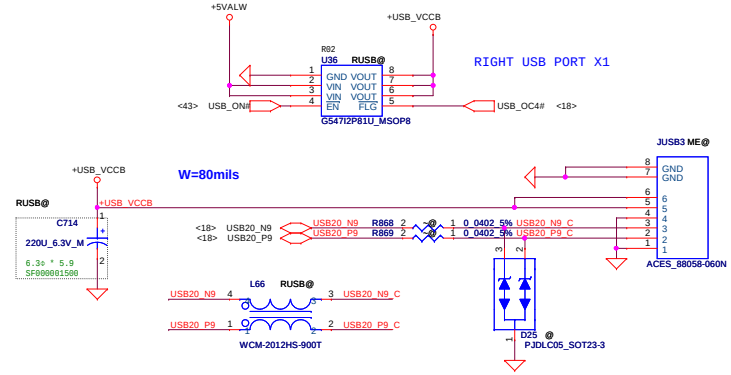
Compal Electronics, Inc.

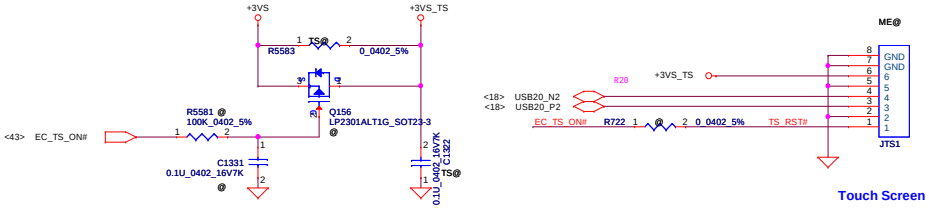
Title: USB ext. ports

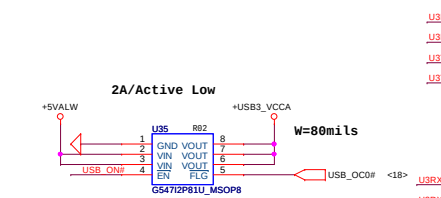
Size	Document Number	Rev
B	LA-9641P	0.3

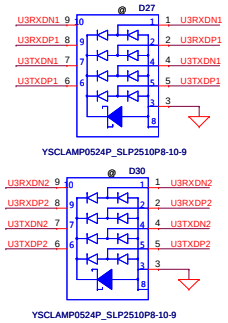
Date: Wednesday, March 06, 2013 Sheet 45 of 61

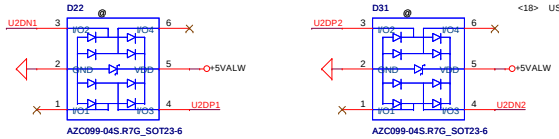
Right Ext.USB Conn.

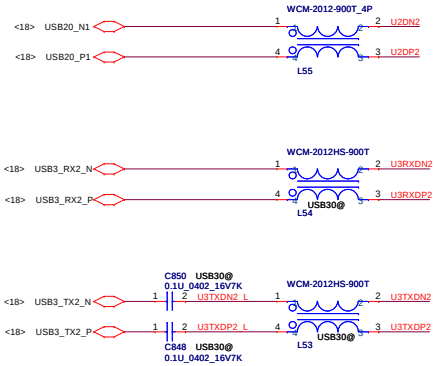


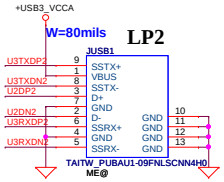


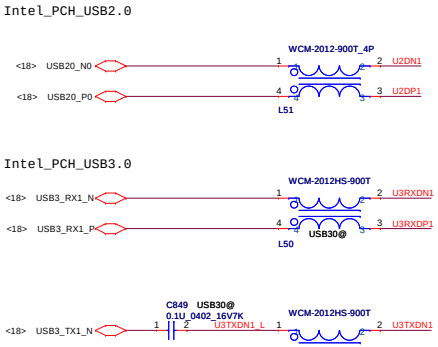


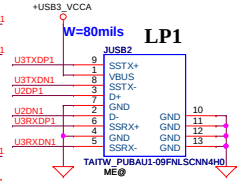












Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **USB3.0/Left USB Ports**

Size	Document Number	Rev
Custom		0.3

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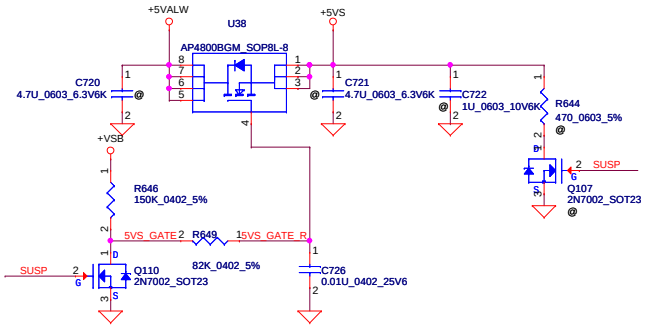
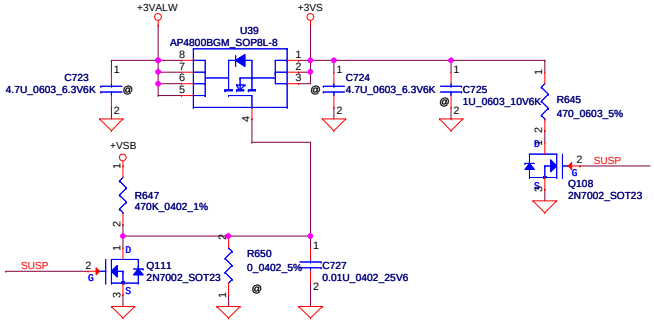
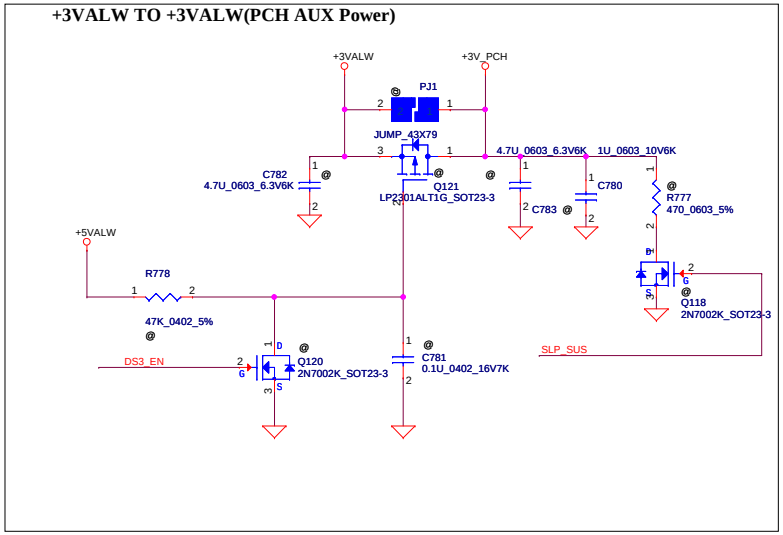
+5VALW TO +5VS

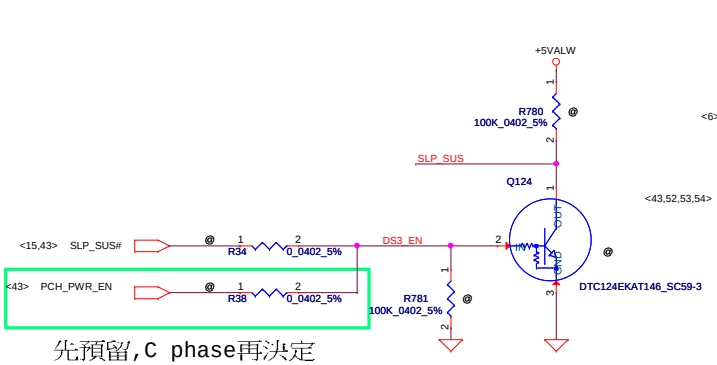


+3VALW TO +3VS

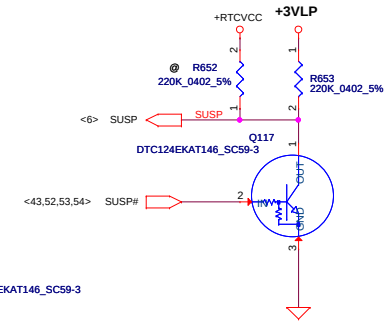


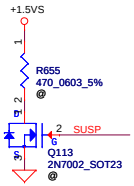
+3VALW TO +3VALW(PCH AUX Power)

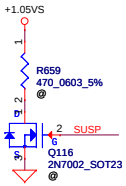




先預留,C phase再決定







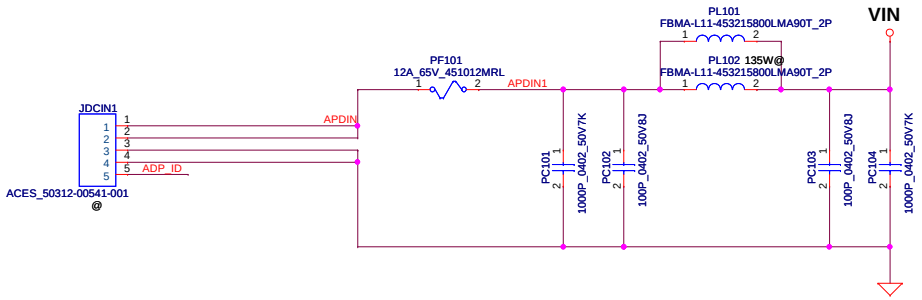
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

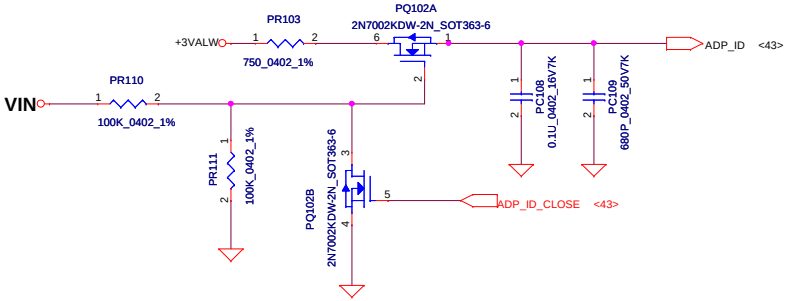
Compal Electronics, Inc.

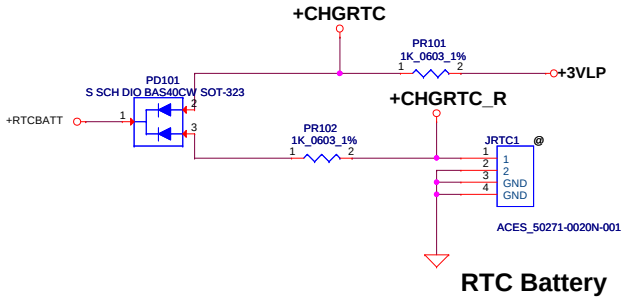
Title: DC Interface

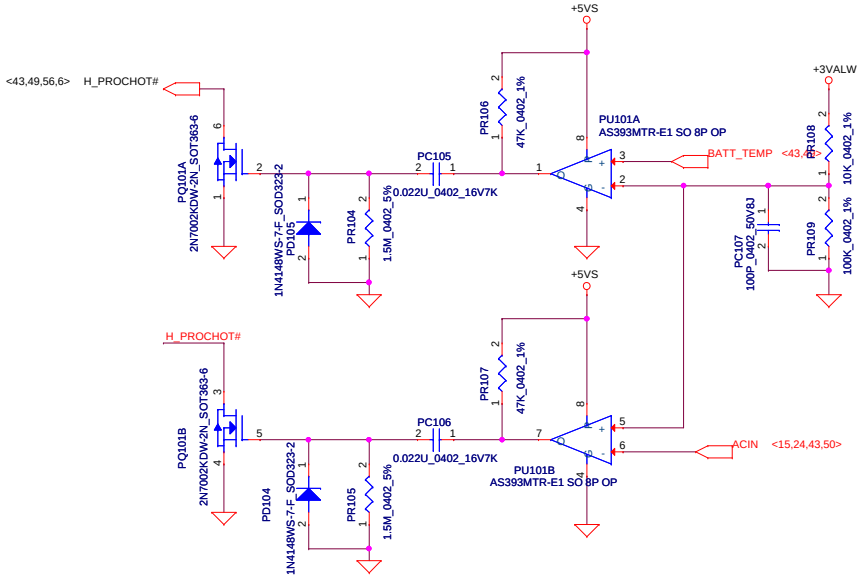
Size	Document Number	Rev
Custom	LA-9641P	0.3

Date: Wednesday, March 06, 2013 | Sheet 47 of 61









Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

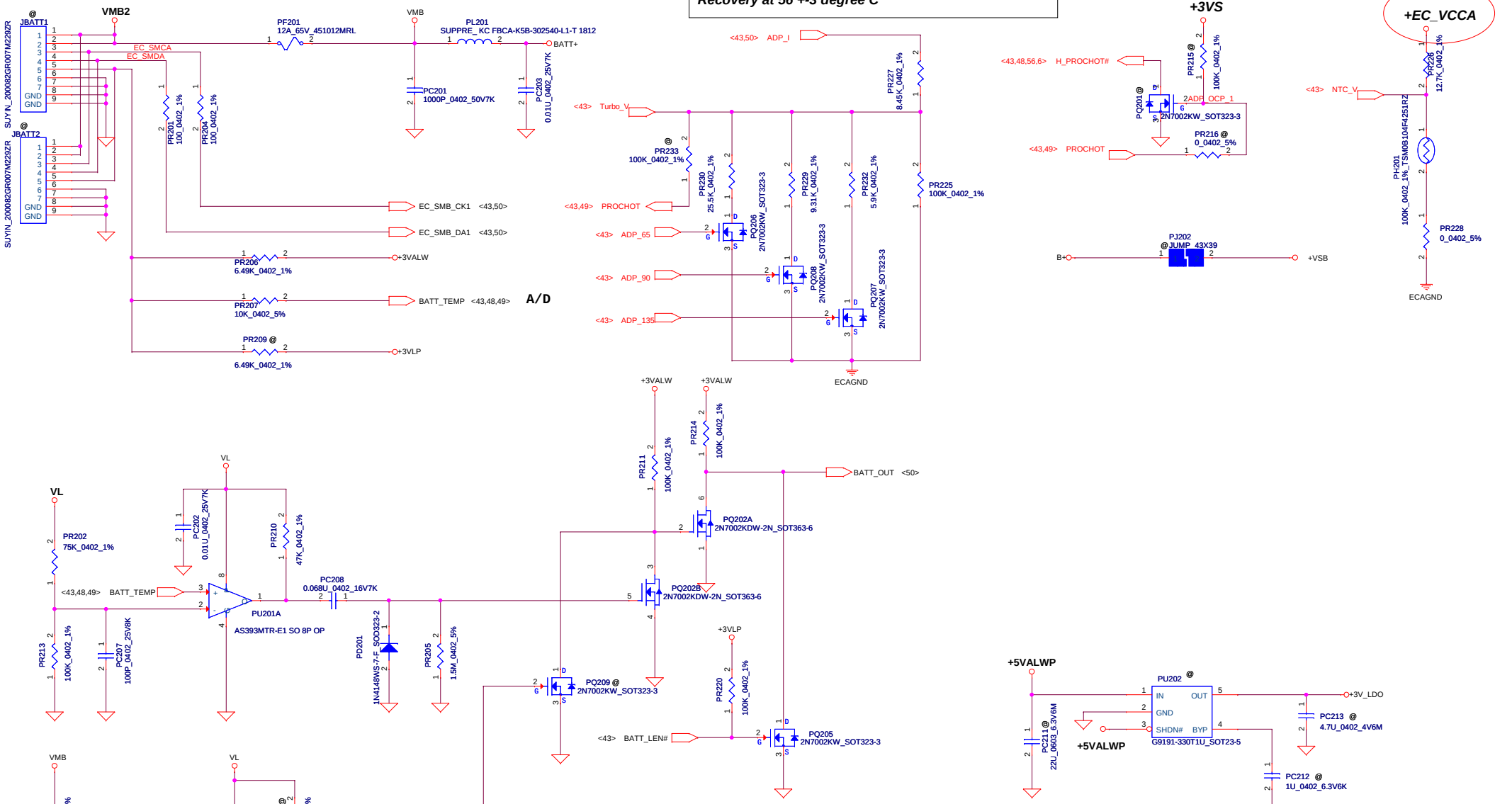
Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: LA-9641P | Rev: 0.2

Date: Wednesday, March 06, 2013 | Sheet 48 of 59

JBATT1 -15" JBATT2 -14"

PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



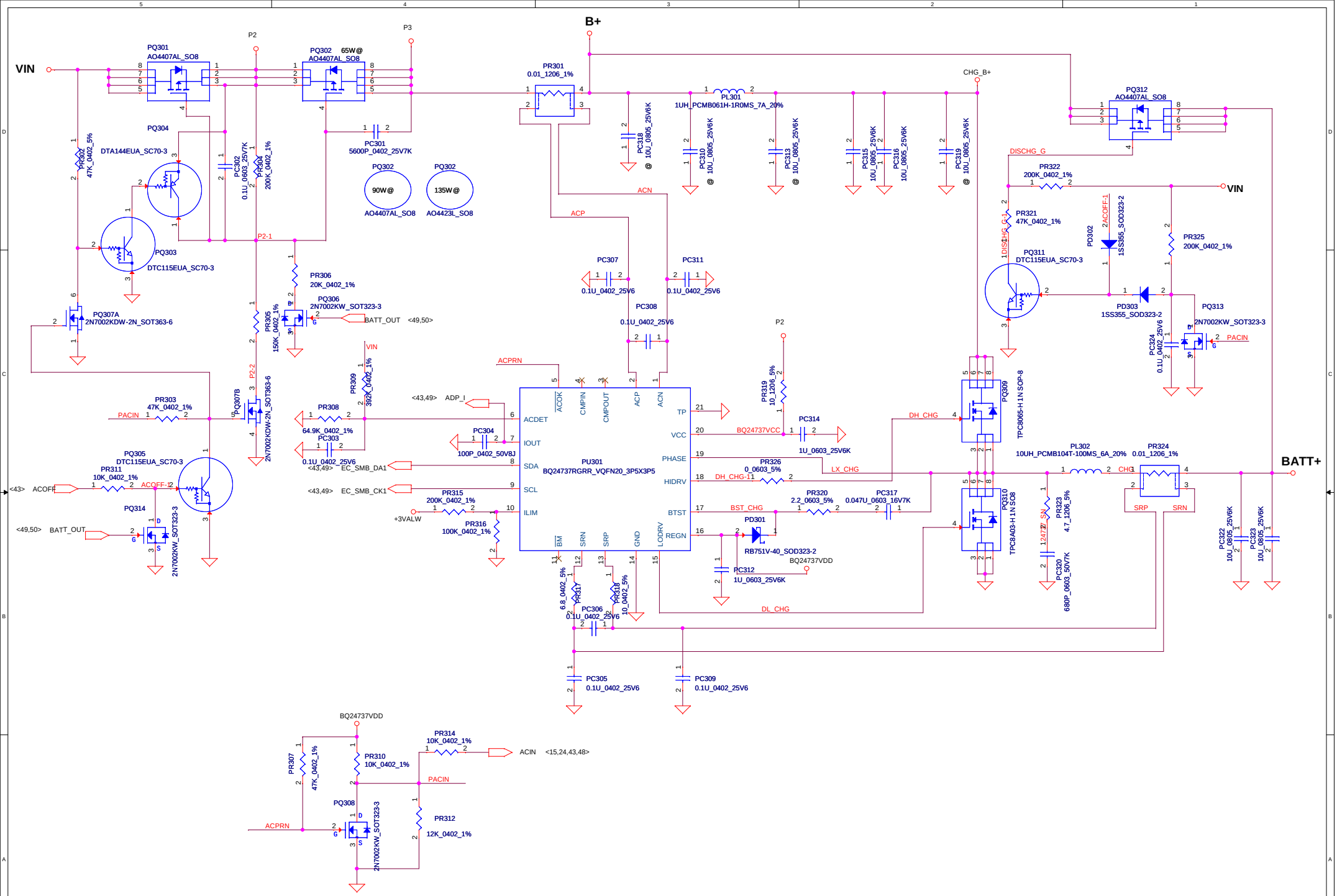
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

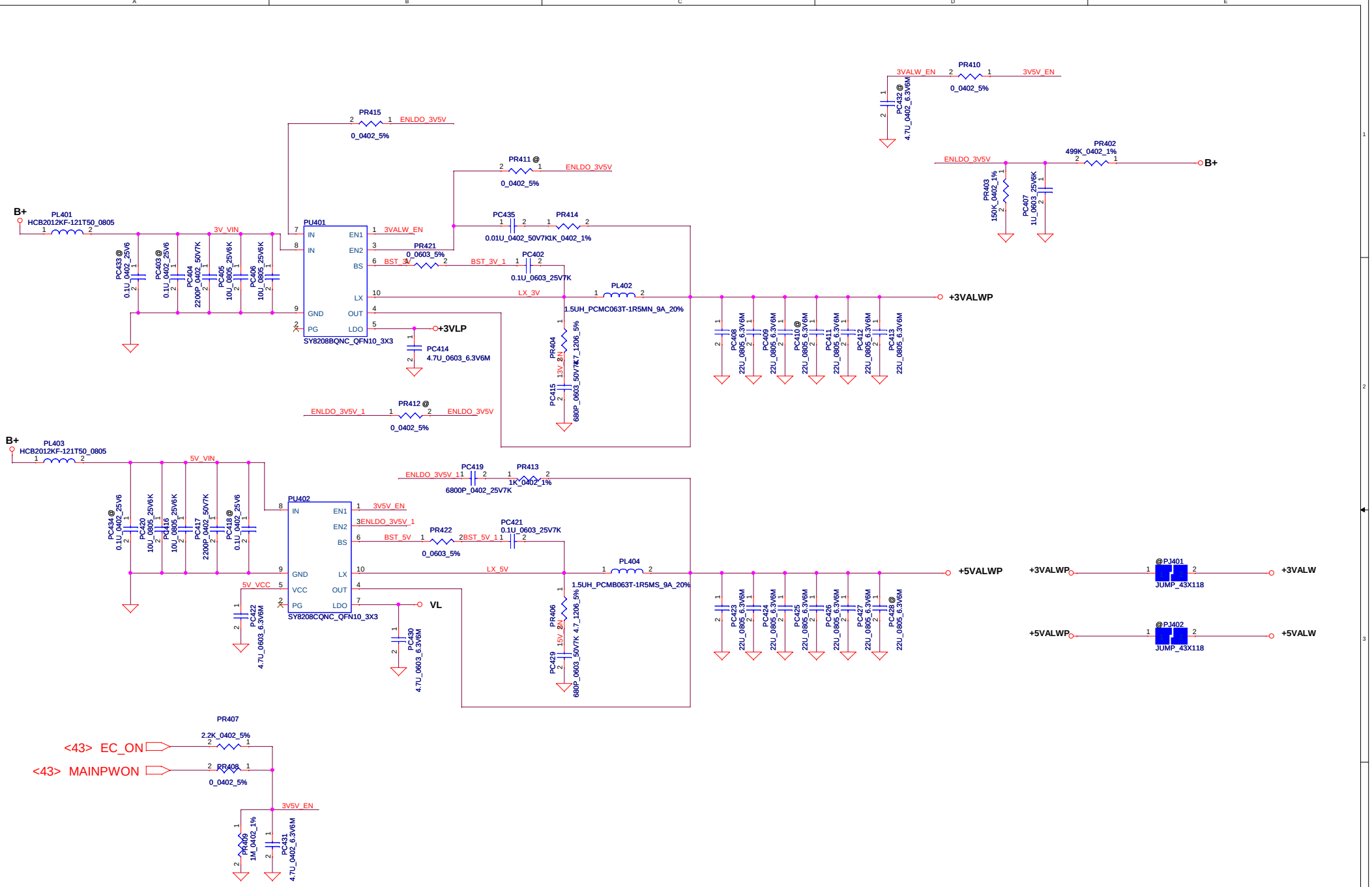
Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: LA-9641P | Rev: 0.2

Date: Wednesday, March 06, 2013 | Sheet 49 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/01/13	Deciphered Date	2012/07/11
Title	CHARGER-BQ24737		
Size	Document Number		Rev
	LA-9641P		0.2
Date:	Wednesday, March 06, 2013	Sheet	50 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

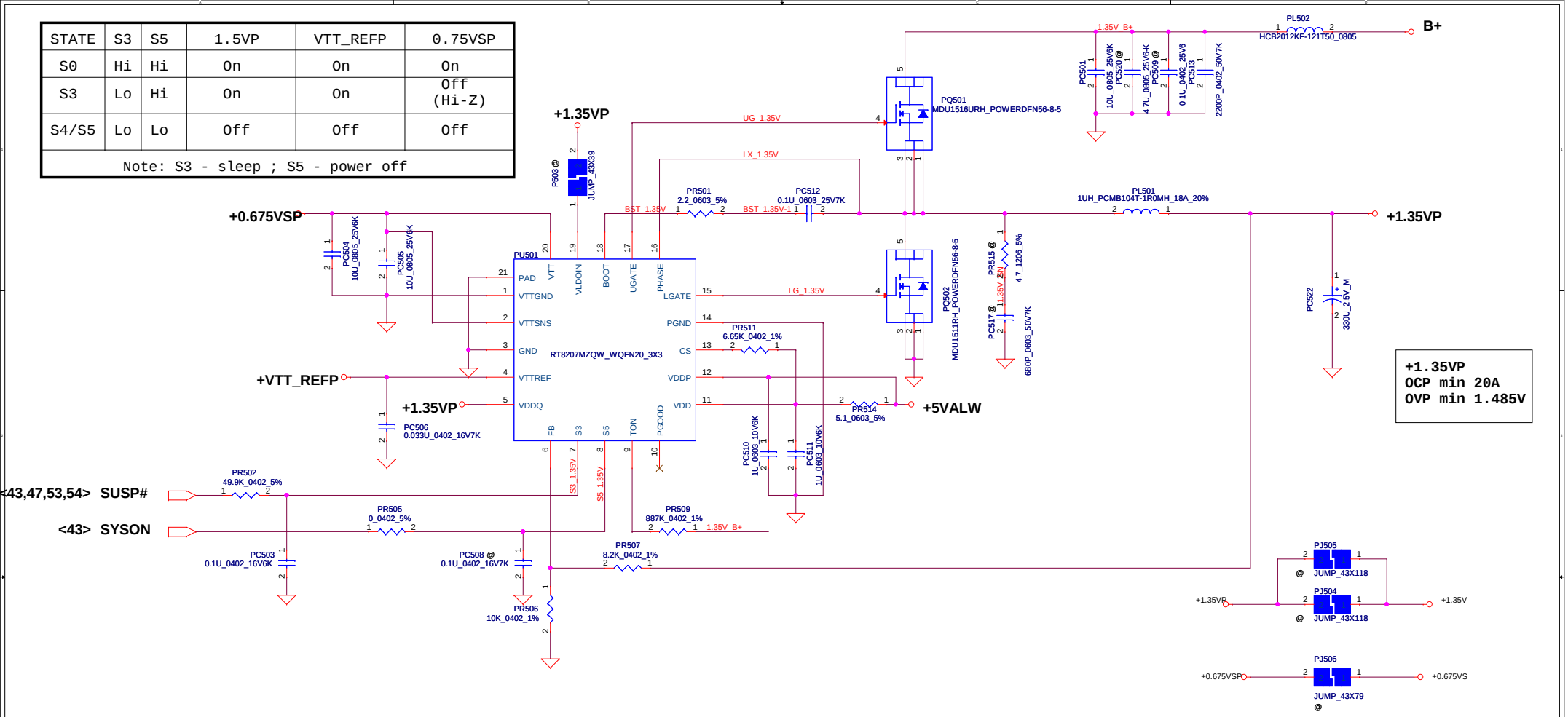
Compal Electronics, Inc.

Title: **PWR- 3VALWP/5VALWP**

Size	Document Number	Rev
Custom	LA-9641P	0.2

Date: Wednesday, March 06, 2013 Sheet 51 of 12

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



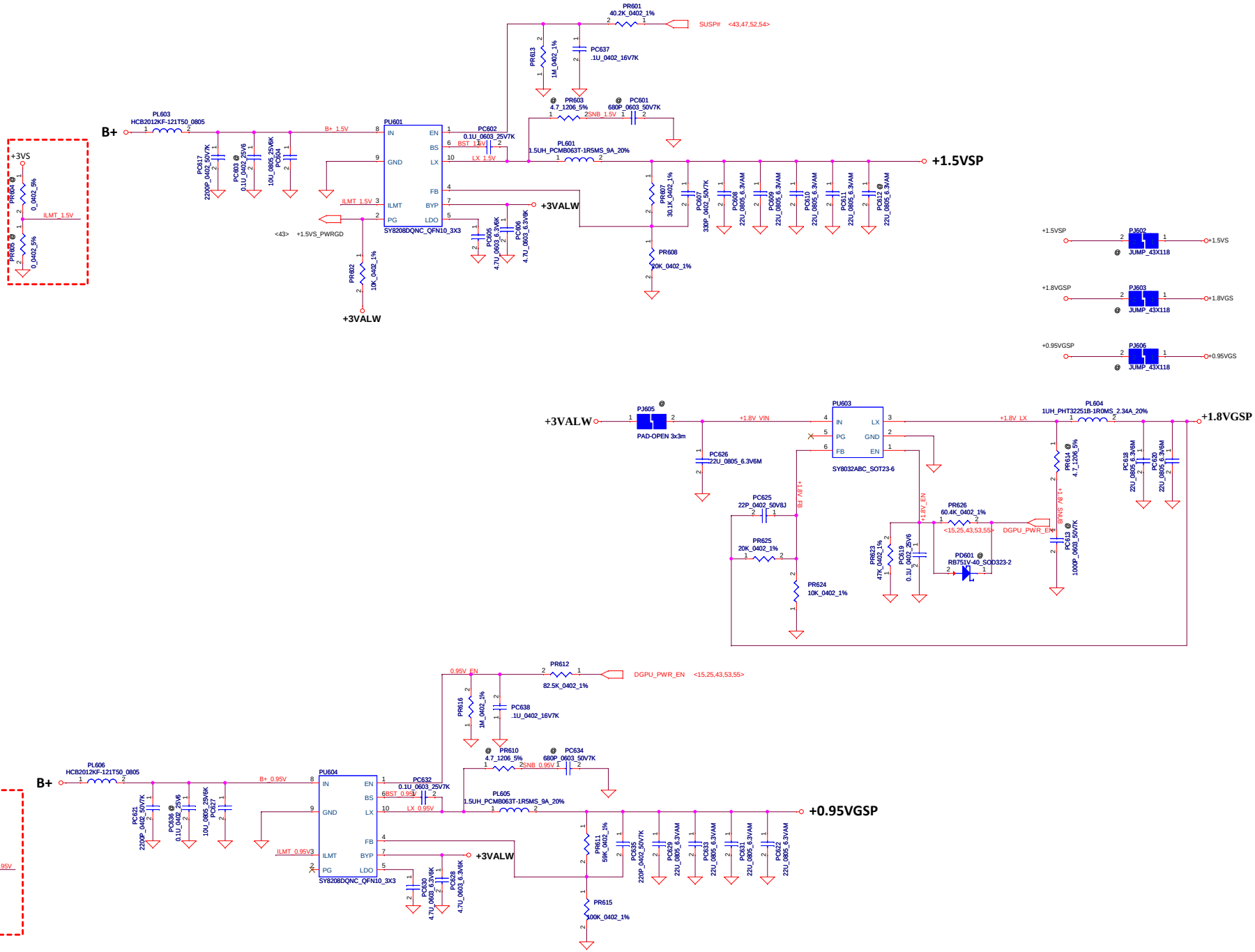
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.35V_DDR

Size: Custom | Document Number: LA-9641P | Rev: 0.2

Date: Wednesday, March 06, 2013 | Sheet 52 of 59



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

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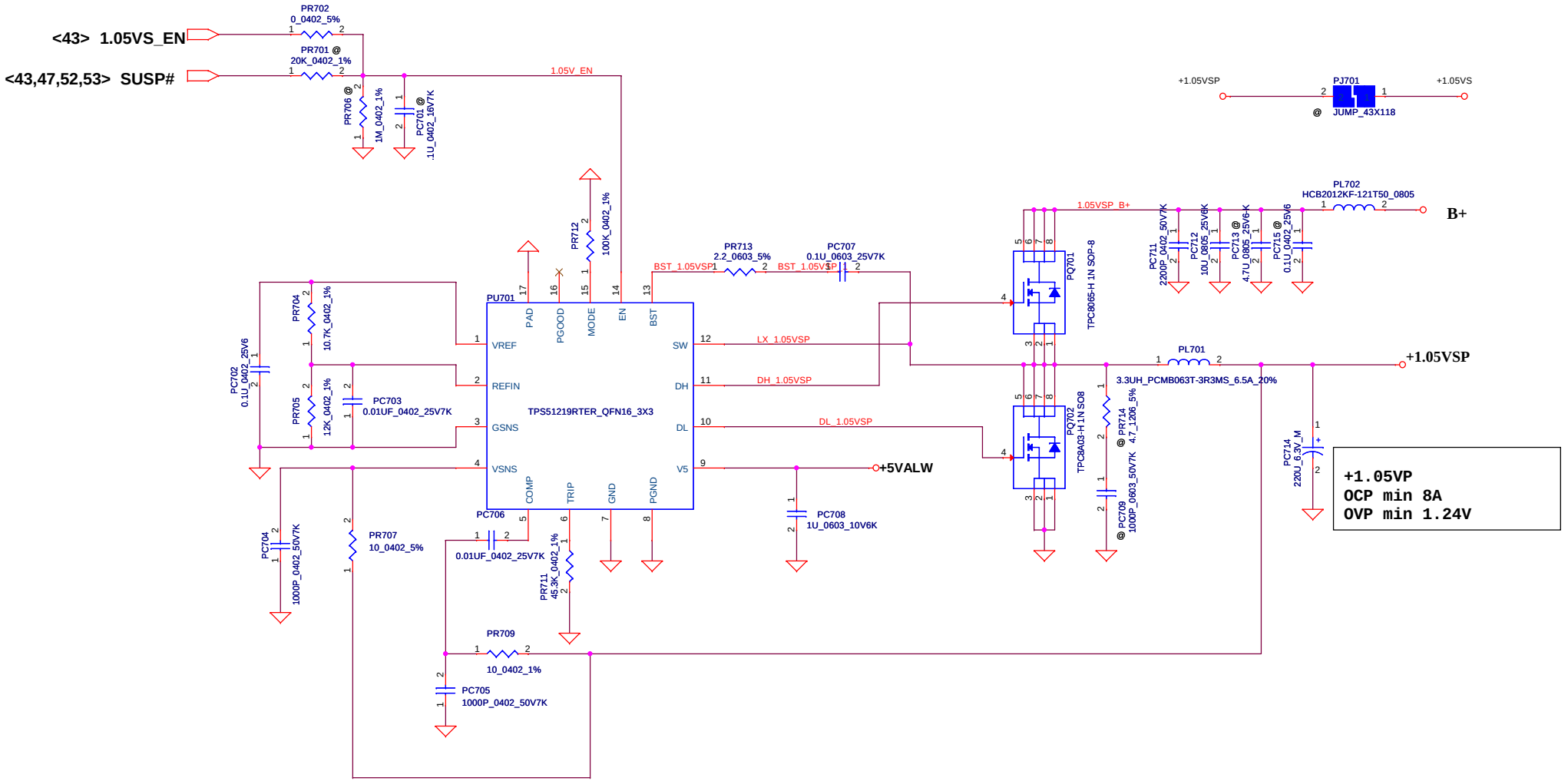
Compal Electronics, Inc.

Title: 1.5V_VRAM/1.8V/0.95V

Size	Document Number	Rev
C	LA-9641P	0.2

Date: Wednesday, March 06, 2013 Sheet 53 of 59



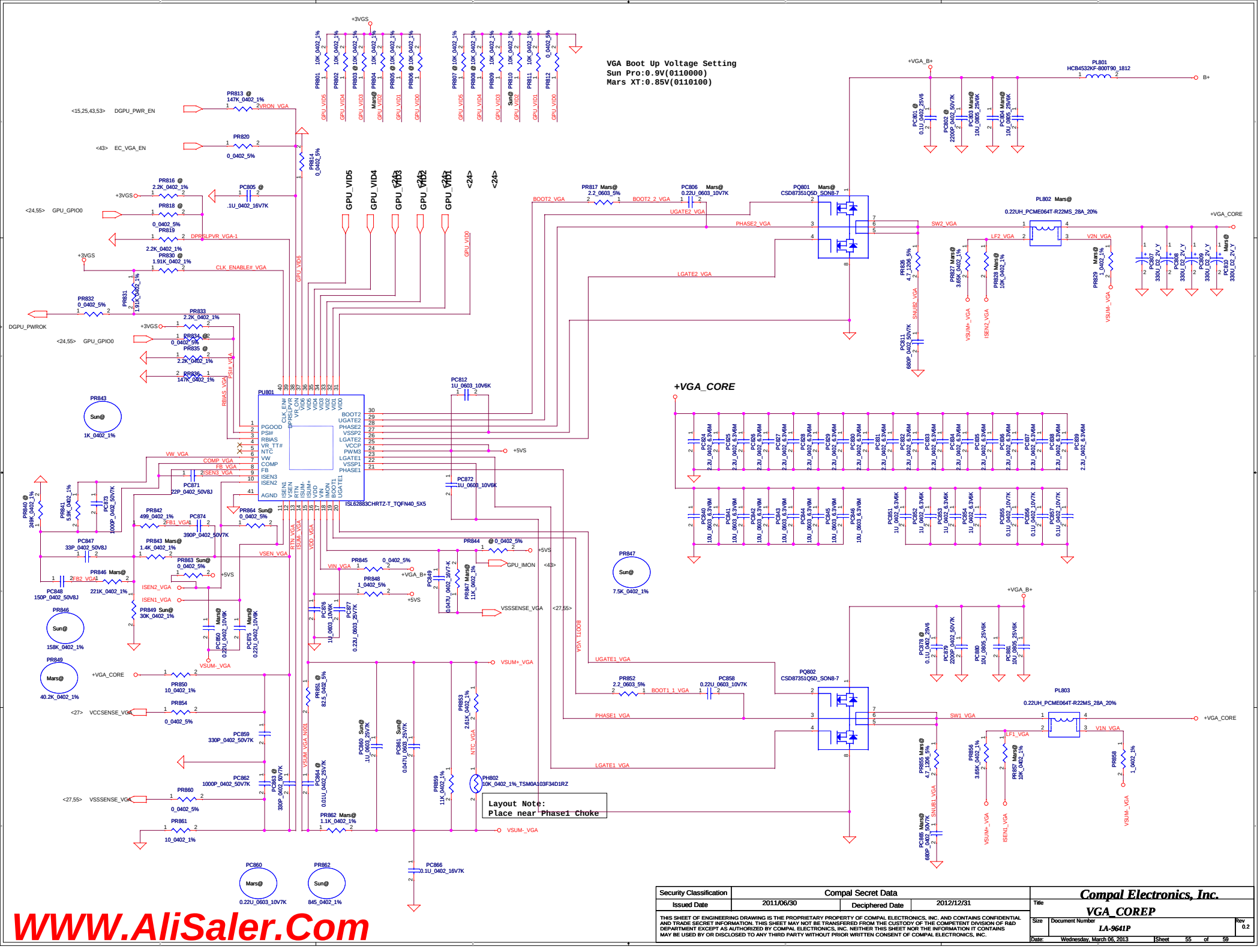
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: +1.05VS

Size	Document Number	Rev
Custom	LA-9641P	0.2

Date: Wednesday, March 06, 2013 Sheet 54 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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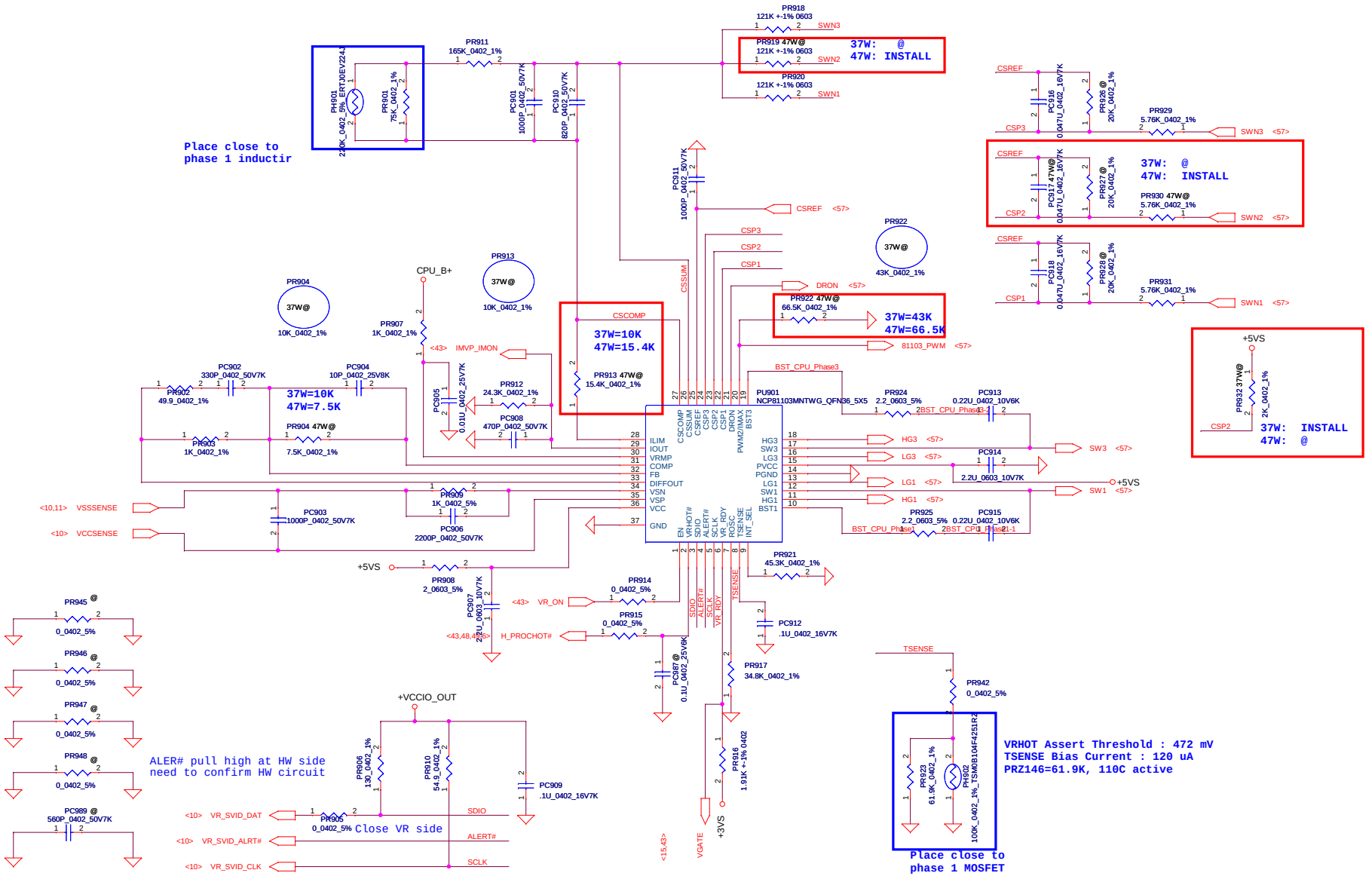
Compal Electronics, Inc.

Title: VGA_COREP

Size	Document Number	Rev
	LA-9641P	0.2

Date: Wednesday, March 06, 2013 | Sheet 55 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

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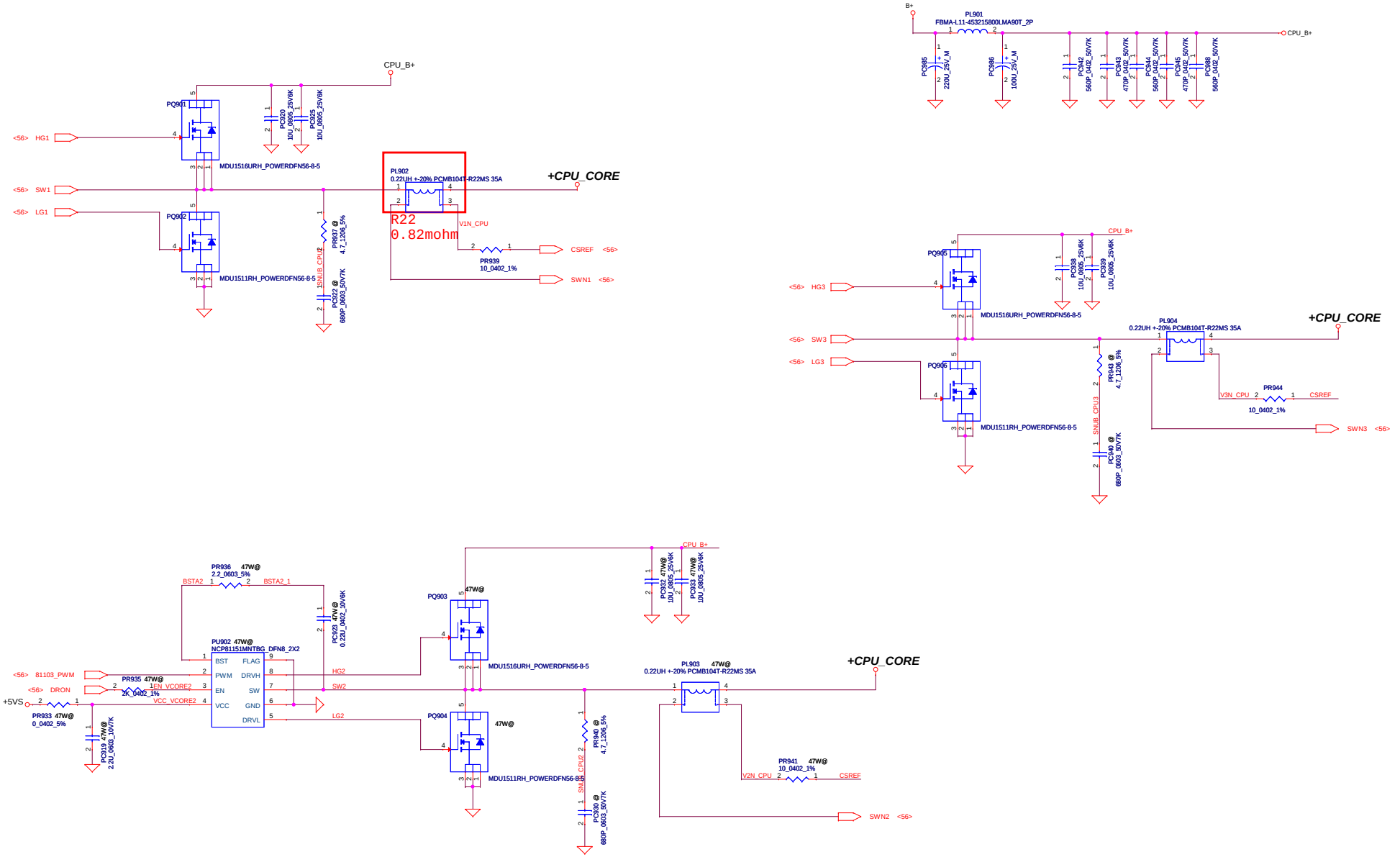
Compal Electronics, Inc.

Title: CPU_CORE1

Size: Custom | Document Number: LA-9641P | Rev: 0.2

Date: Wednesday, March 06, 2013 | Sheet 56 of 59



Security Classification	Compal Secret Data		
Issued Date	2011/12/14	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE2

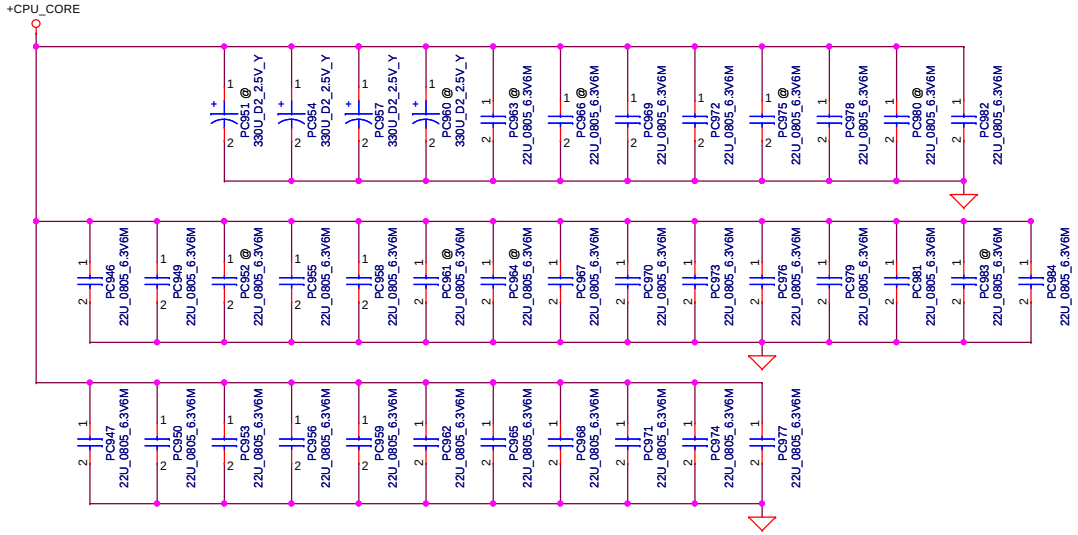
Size	Document Number	Rev
C	LA-9641P	0.2

Date: Wednesday, March 06, 2013 Sheet 57 of 59

+CPU_CORE

3 X 330u/9m(47W)
34 X 22u/0805

2X330u/9m(37W)
34 X 22u/0805



Security Classification	Compal Secret Data		
Issued Date	2012/04/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: ***PROCESSOR DECOUPLING***

Size | Document Number: **LA-9641P** | Rev: 0.2

Date: Wednesday, March 06, 2013 | Sheet 58 of 59

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Adapter ID selection circuit	48 49	Add PR103,PR110,PR111,PQ102,PC108,PC109 Add PR227,PR230,PR229,PR232,PR225,PQ206,PQ208,PQ207	2012.11.28	DVT
2	Delete reserve circuit B+ to VSB	49	Delete PR217,PR218,PR219,PC204,PQ203,PR223,PR224,PC205,PQ204,PC206	2012.11.28	DVT
3	Pop Snubber by EMI request	50	PR323,PC320	2012.11.28	DVT
4	To reduce Ripple	51	PC411,PC426 and change PL404 to 3.3uH	2012.11.28	DVT
5	Reserve enable signal by HW request	51	Add PR410,PC432	2012.11.28	DVT
6	Add boost resistor by EMI request	51	Add PR421,PR422	2012.11.28	DVT
7	Reserve feedback signal for IC application	51	Add PR413,PC419	2012.11.28	DVT
8	To reduce Ripple	53	Change PL601and PL605 to 1.5uH	2012.11.28	DVT
9	Delete reserve circuit	53	Delete PC623,PU602,PC624,PR619,PR620,PR622,PC614,PR627,PL602,PR613, PC612,PC615,PC616	2012.11.28	DVT
10	To reduce Ripple	54	Change PL601and PL701 to 3.3uH	2012.11.28	DVT
11	Reserve enable signal by HW request	54	Add PR702	2012.11.28	DVT
12	Pop Snubber by EMI request	55	PR826,PC811,PR855,PC865	2012.11.28	DVT
13	Add input MLCC by EMI request	57	Add PC943,PC944,PC945,PC988	2012.11.28	DVT
14	Reserve battery detective circuit	49 50	Add PR2003,PR217,PC209,PR212,PC210,PD203,PR208,PQ209,PC211,PU202,PC212,PC213 Add PQ314,PR311(Pop)	2013.03.03	PVT
15	Reserve capacitor by EMI request	50	Add PC318,PC319	2013.03.03	PVT
16	Reduce Component	51	Delete PD401	2013.03.03	PVT
17	Reserve 1.5VSP Power Good by HW request	53	Add PR602	2013.03.03	PVT
18	Reserve bridge resistor by EMI request	55	Add PR948,PC989		

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	PIR (PWR)		
Size: Custom	Document Number: LA-9641P		Rev: 0.2
Date: Wednesday, March 06, 2013	Sheet 59 of 59		

Item	Reason for change	PG#	Modify List	Date	Phase
1	USE singal 8M ROM for BIOS		Change U8 to SA000039A30 8MB ROM Del U7,R239,R234,R235,R233,R236	12/25	DVT
2	POWER NEW AC Connector		U31.21--> ADP_65 U31.68 change from EC_WL_OFF# to ADP_90 U31.85 change from EC_TS_ON#to ADP_135 U31.66 change from BRDID_1 to ADP_ID	12/25	DVT
3	Change XDP pull down Resistor to R pack		Del R18,R21,R23 / Add RP19	12/25	DVT
4	Update Lenovo BGA footprint		UV1,U4,UV5,UV6,UV7,UV8,UV9,UV10,UV11,UV12	12/25	DVT
5	Move 15" ODD CAP to Small Board		ChangeC605 to R401/ChangeC606 to R402/ ChangeC618 to R403/ChangeC617 to R404	12/25	DVT
6	WLAN Control change to PCH		PCH_GPIO55--> PCH_WL_OFF# PCH_GPIO22-->PCH_BT_ON# PCH_GPIO34-->INTEL_BT_OFF#	12/25	DVT
7	POP TL_ENVDD PULL DOWN		POP R408	12/25	DVT
8	Change HDMI LV from 10P8R to 8R4R X2		Del RP19 ADD RP5, RP6	12/25	DVT
9	Update EC GPIO		NOVO# change form pin 26 to 34 EC_FAN_PWM change form pin 34 to 26 ENBKL change form pin 73 to 76 IMVP_IMON change form pin 76 to 73 DGPU_PWR_EN change form pin 107 to 123	12/25	DVT
10	VGA sequence		+1.5VGS : RV41 --> 240K / CV53 --> 0.1U	12/25	DVT
11	EC Board ID		Change R695 to 15K	12/25	DVT
12	Change ODD connector symbol		JODD1->ALLTO_C18518-11305-L_13P-T	12/25	DVT
13	Update Crystal cap Value by vendor suggestion		C111/ C112 --> 15p CV36/CV37-->8.2p	12/25	DVT
14	Reserve for EMI		ADD R411,R412,C411,C412	12/25	DVT
15	Change PCIE port and clock connection by SW request		LAN-->Port 3 / WLAN--> Port2	12/25	DVT
16	Reserve R301		Reserve +3VLP power rail to EC	12/25	DVT
17	Change EC_RST# power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
18	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC		Using power rail which the same with EC.	12/25	DVT
19					
20					
21					
22					

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	PIR (HW)		
Size: Custom	Document Number: VIWGQ/GS		Rev: 0.3
Date: Wednesday, March 06, 2013	Sheet 60 of 61		

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add resistor to switch audio power from +3VS to +3VLP and +3VALW.		Add RA1,RA2	02/18	PVT
2	Reconnect HDD +3VS power rail.		Add R-short R552.	02/18	PVT
3	Modify LED current limiting resistor value.		Modify : R623,R765,R303	02/18	PVT
4	Add parallel resistor to separate BIOS and EC.		Add RP2	02/18	PVT
5	Add a Capacitor to connect CHASSIS_GND and GND by EMI request.		Add CL64	02/18	PVT
6					
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22					

Security Classification	Compal Secret Data		
Issued Date	2009/01/06	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PIR (HW)

Size	Document Number	Rev
Custom	VIWGQ/GS	0.3

Date: Wednesday, March 06, 2013 Sheet 61 of 61