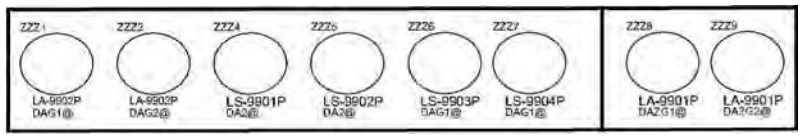


Compal Confidential

G400S/G500S UMA M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

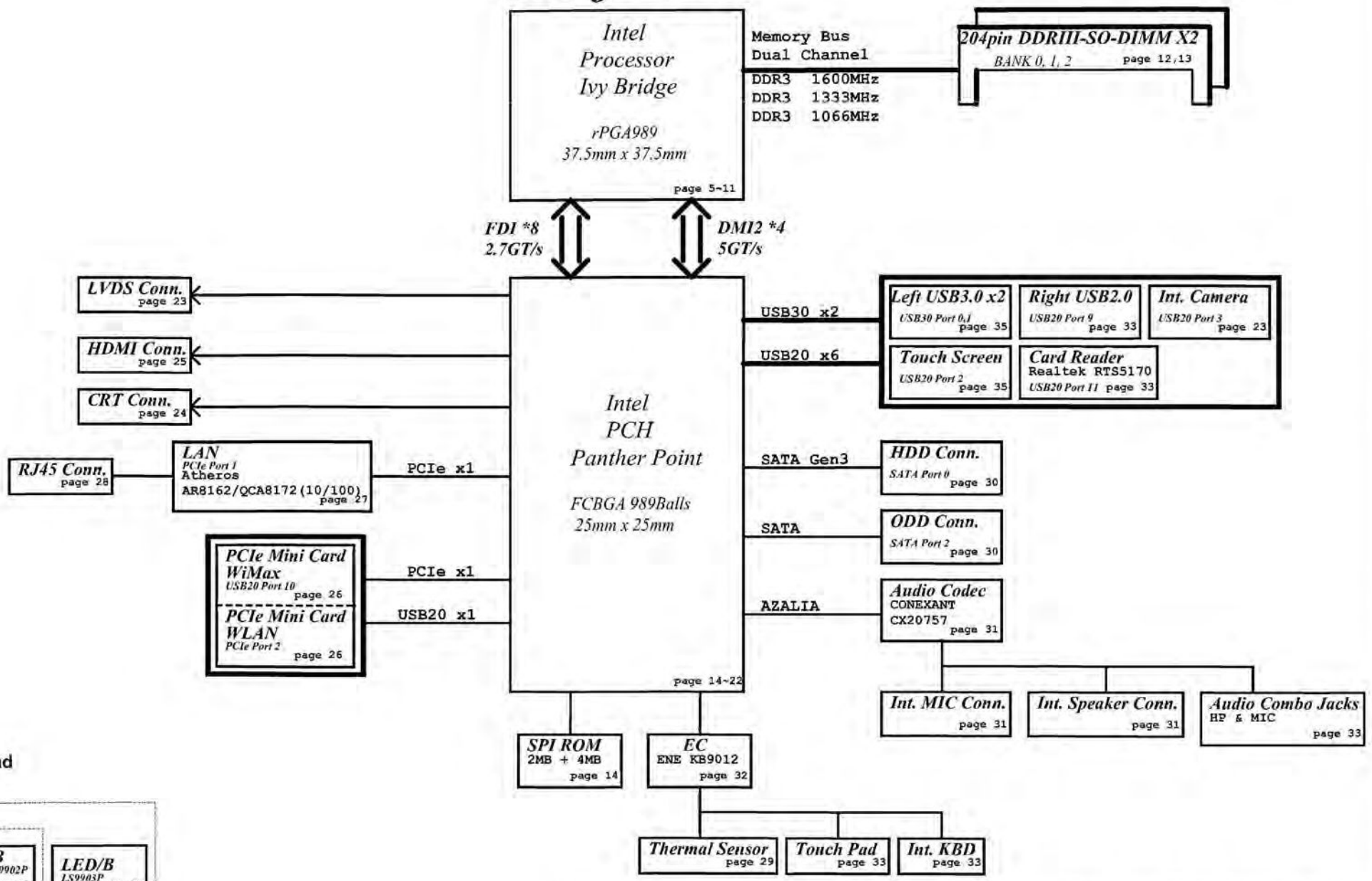
LA-9902P

2013-05-06

REV:1.0

	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	SCHEMATIC M/B LA-9902
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size: Custom	Document Number: 4019N1	Rev: B
				Date: Wednesday, May 08, 2013	Sheet 1 of 52

Chief River



Sub-borad

15"

14"

- Power/B LS9902P page 33
- LED/B LS9903P page 33
- IO/B LS9901P page 33
- ODD/B LS9904P page 30

Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

SCHEMATIC M/B LA-9902

Size: Custom	Document Number: 4019N1	Rev: B
Date: Wednesday, May 08, 2013	Sheet 2 of 52	

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID table for AD channel

Vcc	3.3V					
Ra	100K +/- 1%					
Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor	1001 100xb

PCH SM Bus address

Device	Address
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	USB Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB/B (Right Side USB2.0)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
45 LEVEL	45@
Connector	ME@
For VILG2 (14")	14@
For VILG1 (15")	15@
HDMI	HDMI@
Camera	CMOS@
LAN LDO Mode	LDO@
LAN Switch mode	SWR@
10/100 LAN(AR8162L)	8162@
10/100 LAN(QCA8172)	8172@
Green clock(DIS sku)	GCLK304@
Green clock(UMA sku)	GCLK244@
Green clk support	GCLK@
No Green clk support	NOGCLK@
Touch Screen SKU	TS@
Optimus SKU	OPT@
UMA SKU	UMA@
PCH(NM70 sku)	NM70@
PCH(HM70 sku)	HM70@
PCH(HM76 sku)	HM76@
VRAM(1000MHz)	1000M@
VRAM(900MHz)	900M@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	V +3VS_VGA	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS_VGA	X	V +3VS	X	X	V +3VS	X

Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: B | Document Number: 4019N1 | Rev: 3

Date: Wednesday, May 08, 2013 | Sheet 2 of 52

N14x GPIO Pin Definition Table

Pin Name	Normal Function	I/O	Functional Description	Default PU/PD
GPIO0	FB_CLAMP_MON	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID:Strap to boot FBVDDQ
GPIO2~4	Non-support for LCD	O	Panel	100k PD
GPIO5	Reserve			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100k PD
GPIO8	OVERT	IO	Active Low Thermal Catastrophic Over Temperature	100k PU
GPIO9	ALERT	IO	Active Low Thermal Alert	100k PU
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100k PD
GPIO11	PWM_VID	O	GPU Core VDD PWM control supply overdraw input	
GPIO12	PWR_LEVEL	I	AC power detact or control signal	100k PU
GPIO13	PSI	O	Phase Shedding	PSI 100k PU to enable two phase
GPIO14~19	Non-support for HDA	I	Hot Plug	
GPIO20~21	Reserve			

For N14P-GV2 strap table

X76

GPU	Frenc	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GV2	1 GHz	128M*16*4 1GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M*16*4 1GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PU 5K
N14P-GV2	1 GHz	128M*16*4 1GB	Hynix H5TQ2G63DFR-N0C	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 35K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M*16*4 2GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PU 5K
N14P-GV2	900 MHz	256M*16*4 2GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 45K	R PD 15K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PU 5K

For N14P-GS strap table

X75

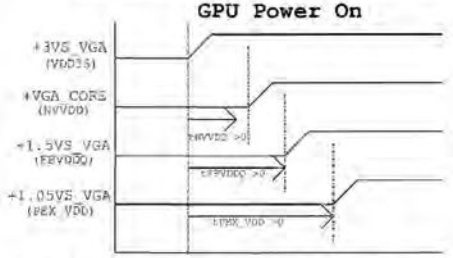
GPU	Frenc	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14P-GS	1 GHz	128M*16*8 2GB	Samsung K4W2G1646E-BC1A	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 45K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M*16*8 2GB	Micron MT41J128M16JT-093G:K	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 30K	R PU 5K	R PD 15K
N14P-GS	1 GHz	128M*16*8 2GB	Hynix H5TQ2G63DFR-N0C	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 35K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M*16*8 4GB	Samsung K4W4G1646B-HC11	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 20K	R PU 5K	R PD 15K
N14P-GS	900 MHz	256M*16*8 4GB	Micron MT41K256M16HA-107G:E	R PU 45K	R PD 5K	R PD 20K	R PD 5K	R PD 45K	R PD 10K	R PU 5K	R PD 15K

For N14M-GE strap table

X76

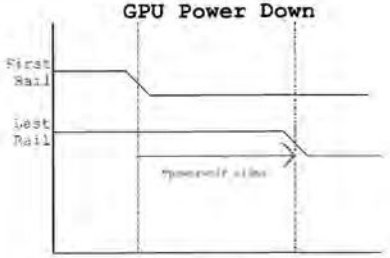
GPU	Frenc	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N14M-GE	1 GHz	128M*16*4 1GB	Samsung K4W2G1646E-BC1A	R PU 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M*16*4 1GB	Micron MT41J128M16JT-093G:K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	1 GHz	128M*16*4 1GB	Hynix H5TQ2G63DFR-N0C	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M*16*4 2GB	Samsung K4W4G1646B-HC11	R PU 10K	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K
N14M-GE	900 MHz	256M*16*4 2GB	Micron MT41K256M16HA-107G:E	R PU 10K	R PD 10K	R PD 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PD 10K

GPU Power On



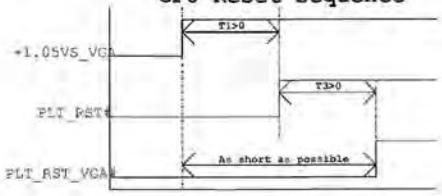
1. All power rail ramp up time should be larger than 400us
2. The total time for all rails to run should be within 5ms.
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up
4. No signal should be applied to the GPU before the power rail are fully ramped.

GPU Power Down

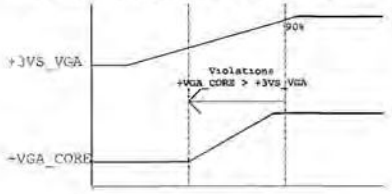


1.All GPU power rails should be turned off within 10ms

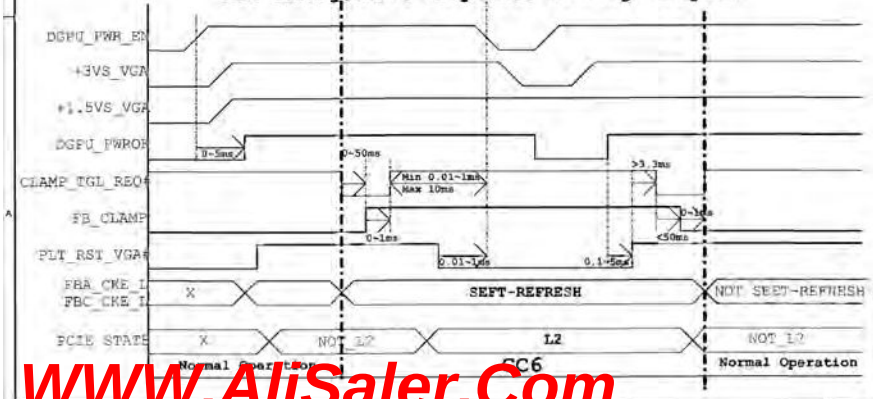
GPU Reset Sequence



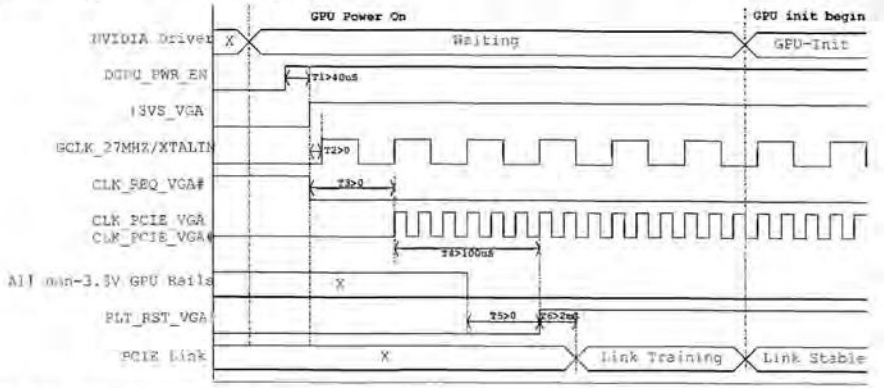
Power sequencing violations



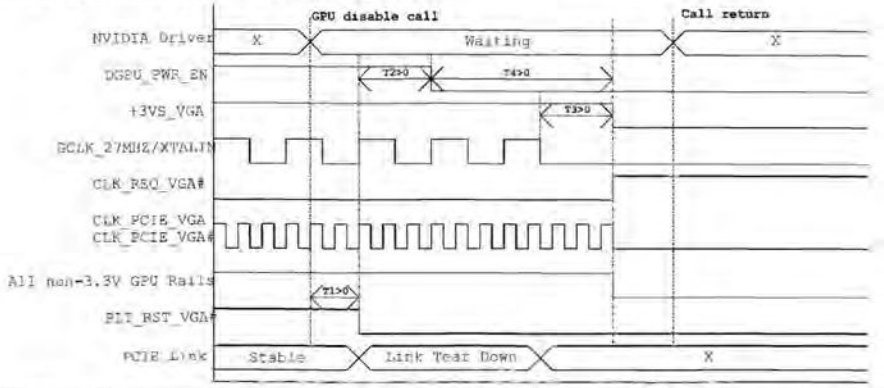
GC6 Entry/Exit Sequence Timing Diagram



Optimus Typical Power-Up Sequence



Optimus Typical Power-Down Sequence



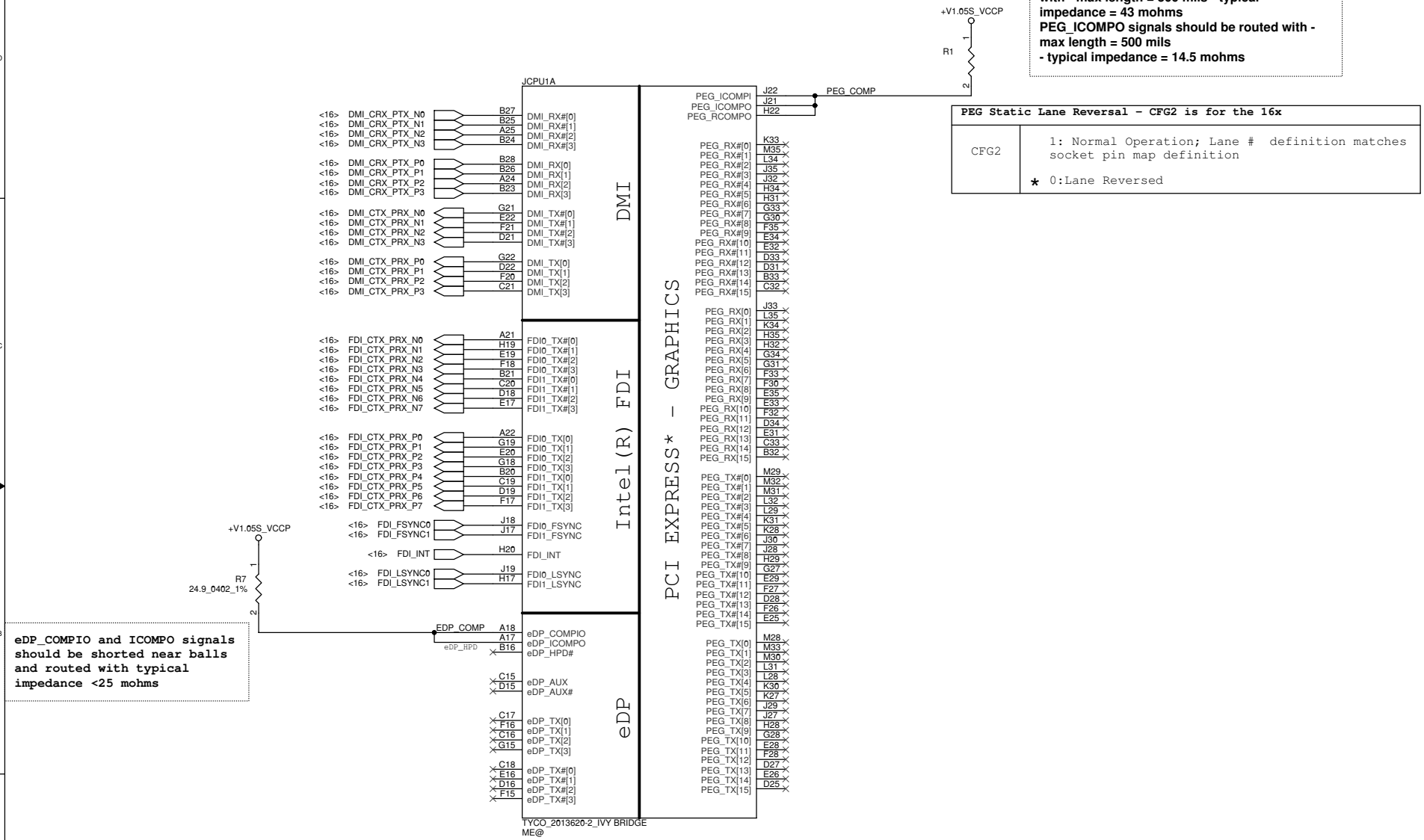
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 4 of 52



PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal – CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

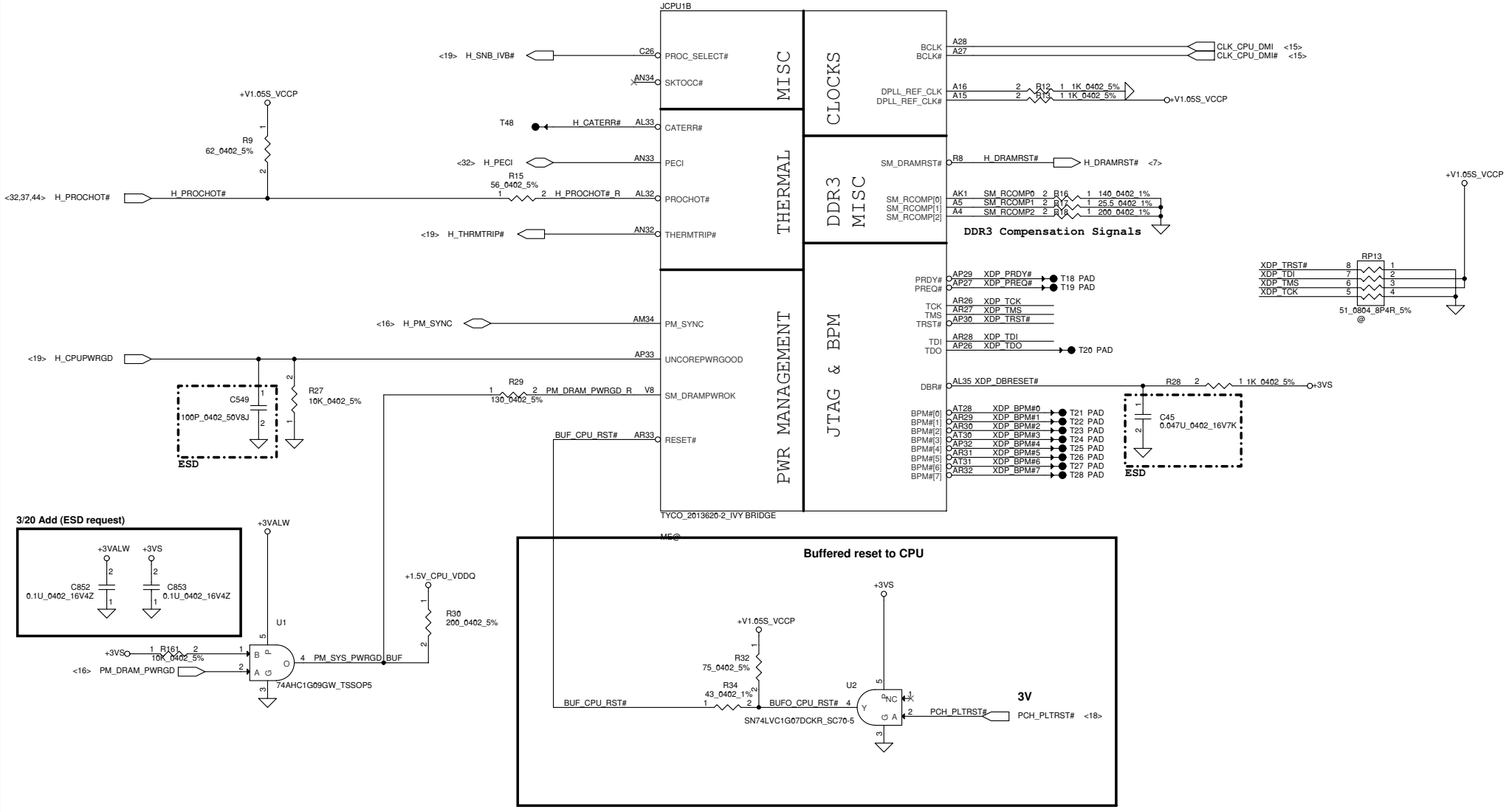
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 5 of 52



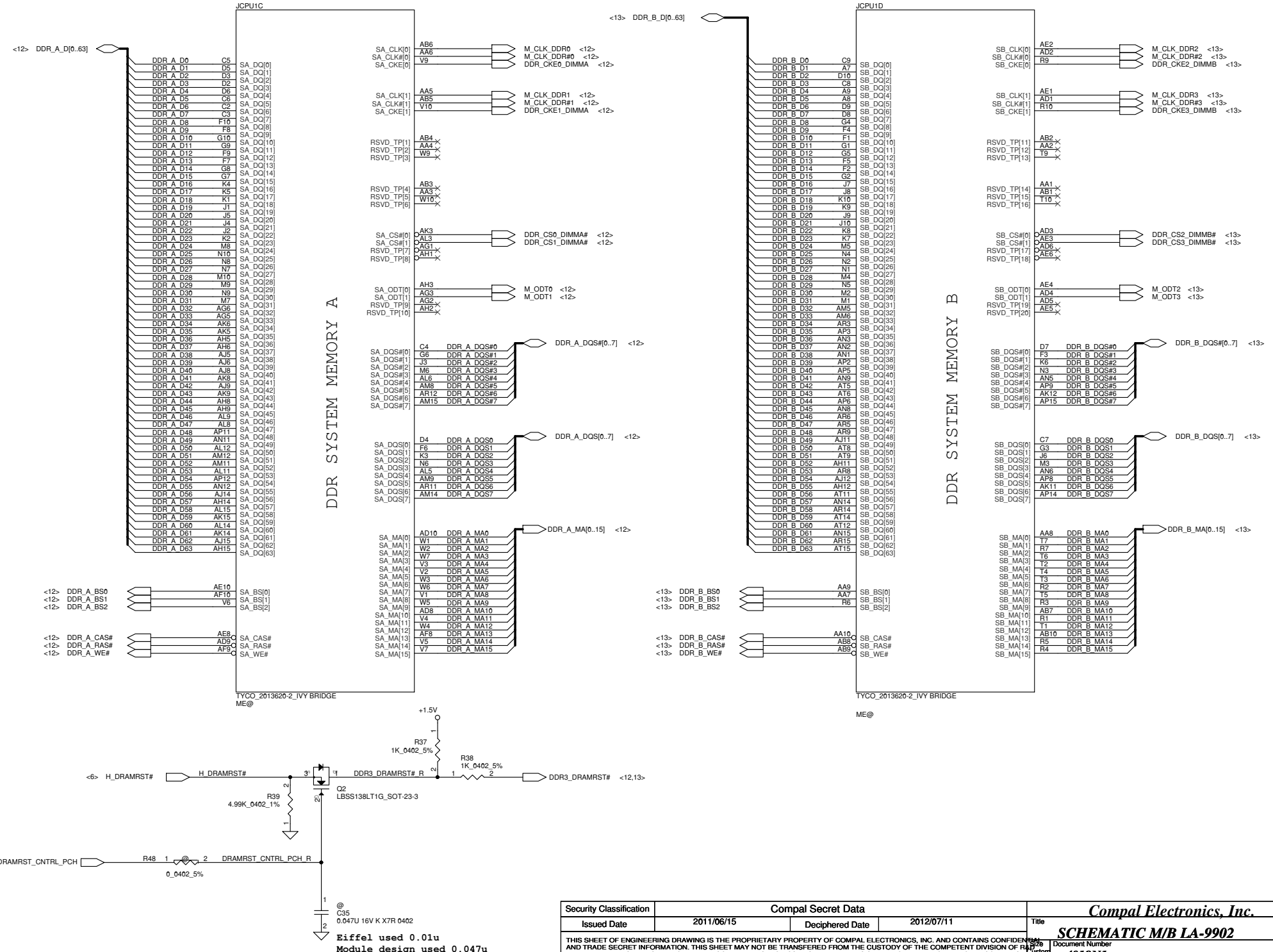
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 6 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

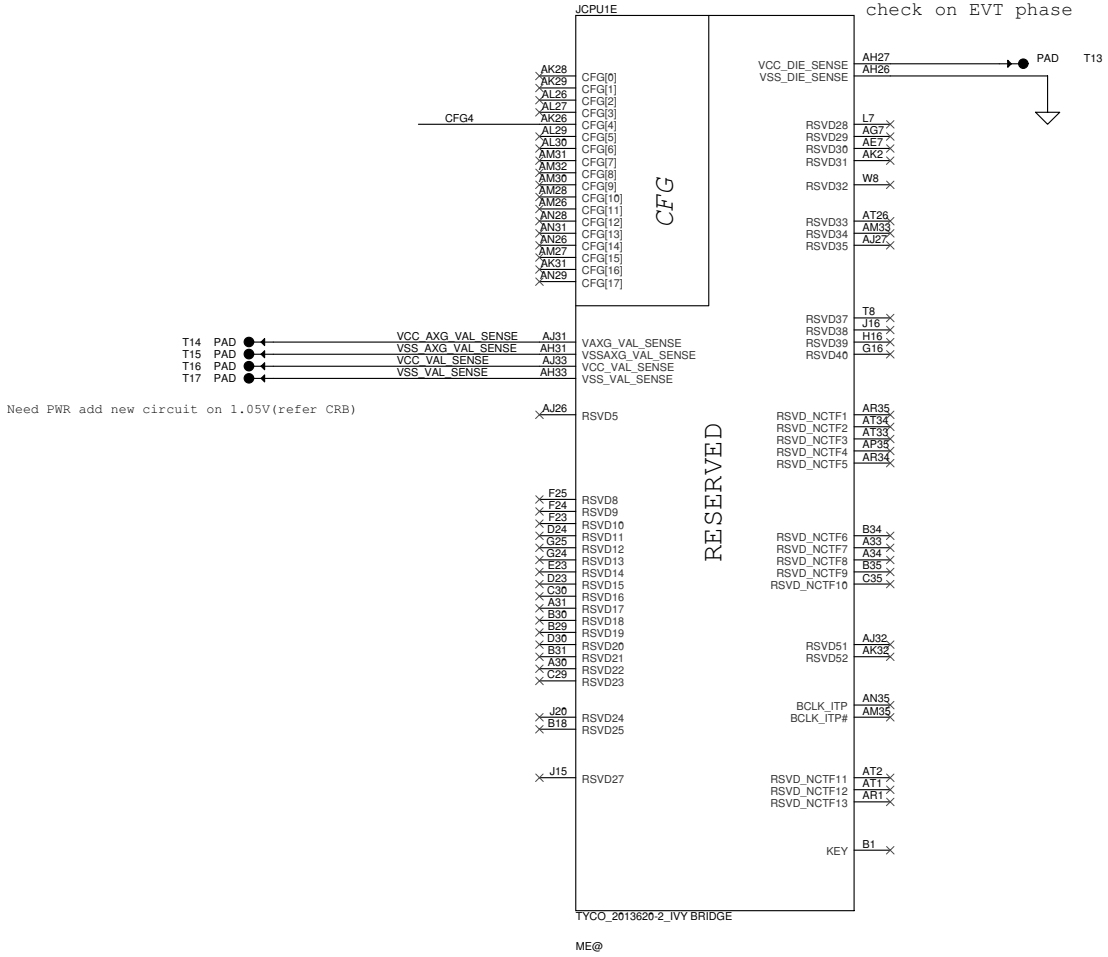
Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

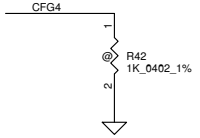
Date: Wednesday, May 08, 2013 | Sheet 7 of 52

CFG Straps for Processor

Interl request AH26 short GND
check on EVT phase



PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled *10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 8 of 52

POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

AG35	VCC1	VCCIO1	AH13
AG34	VCC2	VCCIO2	AH10
AG33	VCC3	VCCIO3	AG10
AG32	VCC4	VCCIO4	AC10
AG31	VCC5	VCCIO5	Y10
AG30	VCC6	VCCIO6	U10
AG29	VCC7	VCCIO7	P10
AG28	VCC8	VCCIO8	L10
AG27	VCC9	VCCIO9	J14
AG26	VCC10	VCCIO10	J13
AF35	VCC11	VCCIO11	J12
AF34	VCC12	VCCIO12	J11
AF33	VCC13	VCCIO13	H14
AF32	VCC14	VCCIO14	H12
AF31	VCC15	VCCIO15	H11
AF30	VCC16	VCCIO16	G14
AF29	VCC17	VCCIO17	G13
AF28	VCC18	VCCIO18	G12
AF27	VCC19	VCCIO19	F14
AF26	VCC20	VCCIO20	F13
AD35	VCC21	VCCIO21	F12
AD34	VCC22	VCCIO22	F11
AD33	VCC23	VCCIO23	E14
AD32	VCC24	VCCIO24	E12
AD31	VCC25	VCCIO25	E11
AD30	VCC26	VCCIO26	D14
AD29	VCC27	VCCIO27	D13
AD28	VCC28	VCCIO28	D12
AD27	VCC29	VCCIO29	D11
AD26	VCC30	VCCIO30	C14
AC35	VCC31	VCCIO31	C13
AC34	VCC32	VCCIO32	C12
AC33	VCC33	VCCIO33	C11
AC32	VCC34	VCCIO34	B14
AC31	VCC35	VCCIO35	B12
AC30	VCC36	VCCIO36	A14
AC29	VCC37	VCCIO37	A13
AC28	VCC38	VCCIO38	A12
AC27	VCC39	VCCIO39	A11
AC26	VCC40	VCCIO40	J23
AA35	VCC41		
AA34	VCC42		
AA33	VCC43		
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
V28	VCC68		
V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

TYCO_2013620-2_IVY BRIDGE

ME@

+V1.05S_VCCP

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# 1 R47 2 43_0402_5%
VIDSCLK AJ30
VIDSOUT AJ28

VR_SVID_ALRT# <44>
VR_SVID_CLK <44>
VR_SVID_DAT <44>

R50 2 1 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51
100_0402_1%

VCC_SENSE AJ35
VSS_SENSE AJ34

VCCSENSE <44>
VSSSENSE <44>

R54
100_0402_1%

VCCIO_SENSE B10
VSS_SENSE_VCCIO A10

VSSIO_SENSE_L 1 R74 2
10_0402_1%

VCCIO_SENSE <43>

R74 & R79 put together

+V1.05S_VCCP

R79
2 1
10_0402_1%

VSSIO_SENSE_L <43>

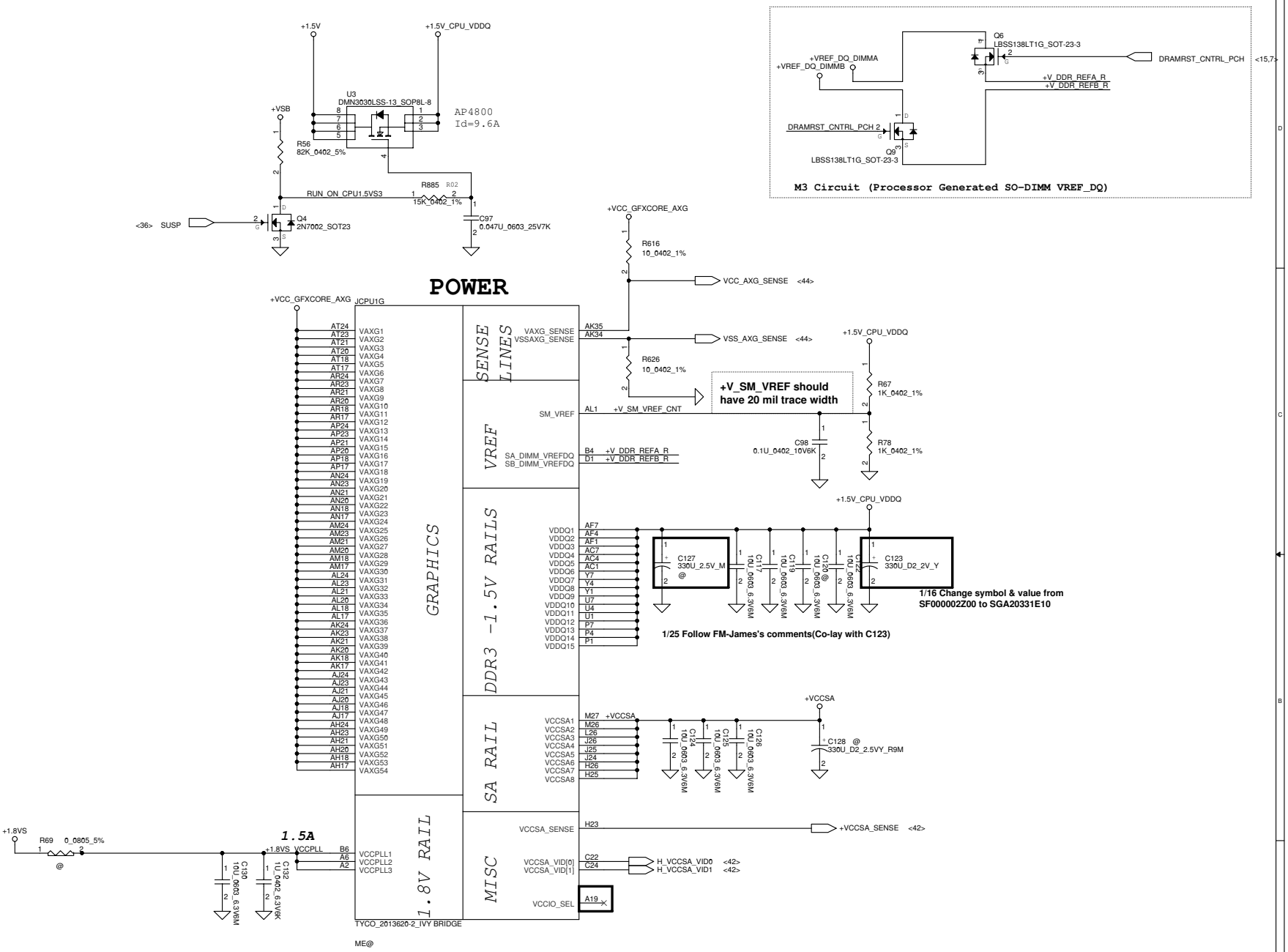
VSS_SENCE 100ohm +-1% pull-down to GND near processor

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: ***SCHEMATIC M/B LA-9902***

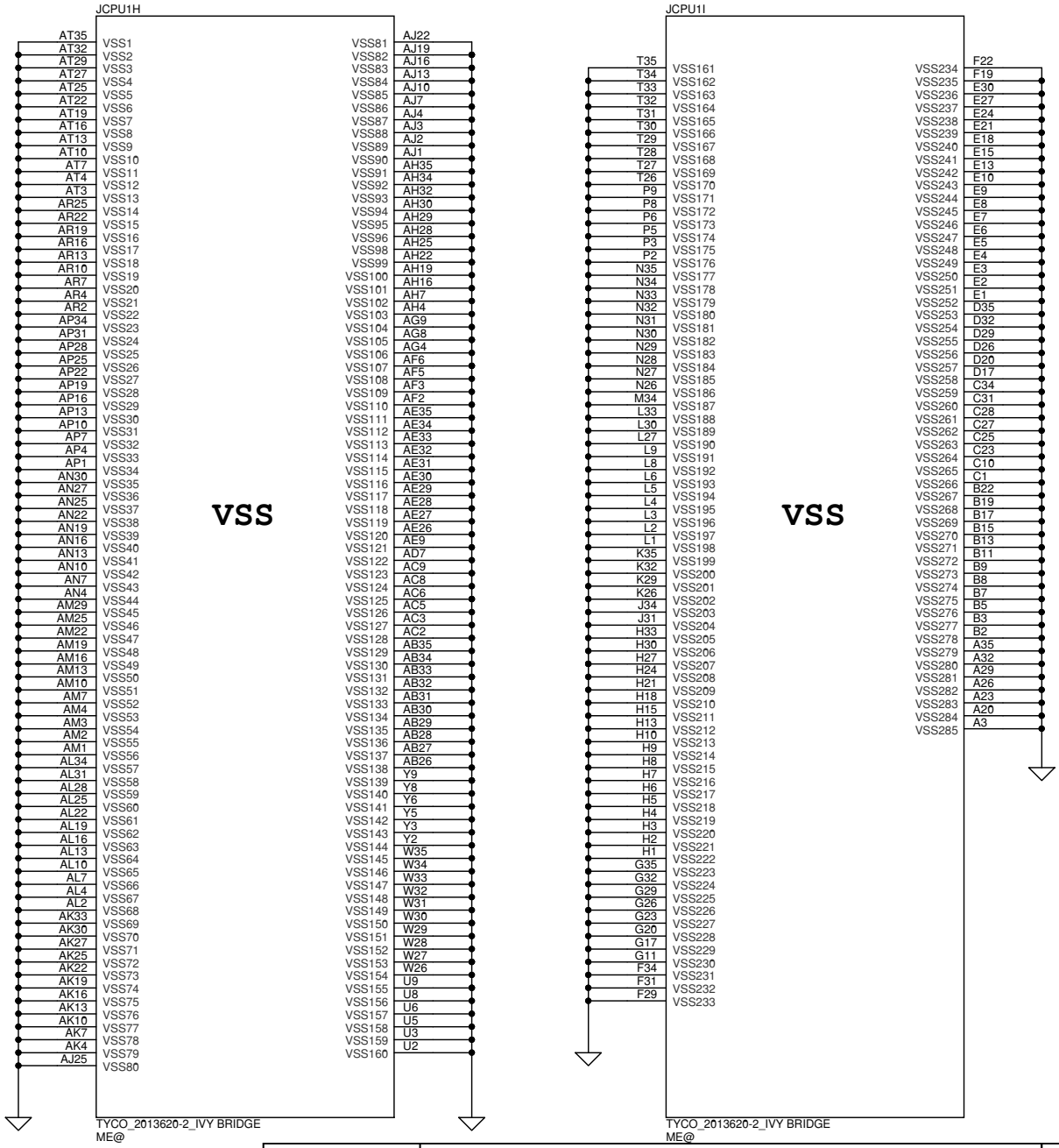
Size: Custom | Document Number: ***4019N1*** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 9 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	SCHEMATIC M/B LA-9902		
Size Custom	Document Number 4019N1		Rev B
Date: Wednesday, May 08, 2013	Sheet 10 of 52		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 11 of 52

DDR3 SO-DIMM A

3401.5V

JDIMM1

LCN_DAN06-K4806-0103

ME@

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

RP15 1K_0804_8P4R_1%

RP16 1K_0804_8P4R_1%

+VREF_DQ_DIMMA
+VREF_DQ_DIMMB
+VREF_CA
+VREF_CB

DDR3_DRAMRST# <13,7>

DDR_CKE0_DIMMA <7>
DDR_CKE1_DIMMA <7>
DDR_A_BS2 <7>
M_CLK_DDR0 <7>
M_CLK_DDR#0 <7>
DDR_A_BS0 <7>
DDR_A_WE# <7>
DDR_A_CAS# <7>
DDR_CS1_DIMMA# <7>
M_CLK_DDR1 <7>
M_CLK_DDR#1 <7>
DDR_A_BS1 <7>
DDR_A_RAS# <7>
DDR_CS0_DIMMA# <7>
M_ODT0 <7>
M_ODT1 <7>

SMB_DATA_S3 <13,15,26>
SMB_CLK_S3 <13,15,26>

+0.75VS

0.65A@.75V

+3V_DIMM
+3VS
R136 0_0402_5%

C133 0.1U_0402_10V6K
C135 0.1U_0402_10V6K
C156 0.1U_0402_10V6K

```
VDDQ(1.5V) =
   3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
   6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
   3*0805 10uf  4*0402 1uf
VREF =
   1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
   1*0402 0.1uf  1*0402 2.2uf
```

Layout Note:
Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

C139 10U_0603_6.3V6M
C140 10U_0603_6.3V6M
C141 10U_0603_6.3V6M
C142 10U_0603_6.3V6M
C143 10U_0603_6.3V6M
C144 10U_0603_6.3V6M
C145 @ 0.1U_0402_10V6K
C146 0.1U_0402_10V6K
C147 0.1U_0402_10V6K
C148 0.1U_0402_10V6K
C149 @ 220U_6.3V_M

Layout Note:
Place near DIMM

C150 1U_0402_6.3V6K
C152 1U_0402_6.3V6K

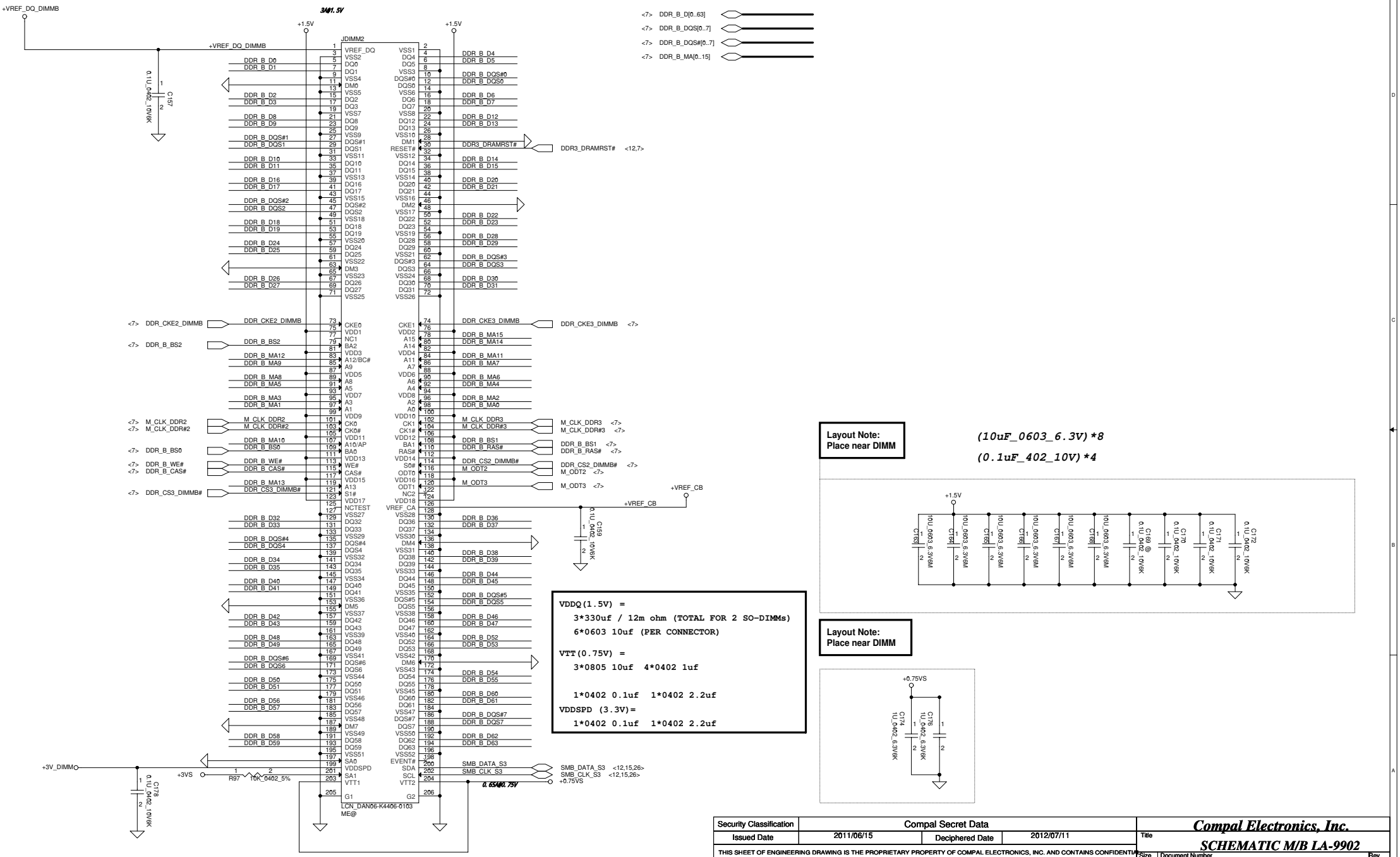
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 12 of 52



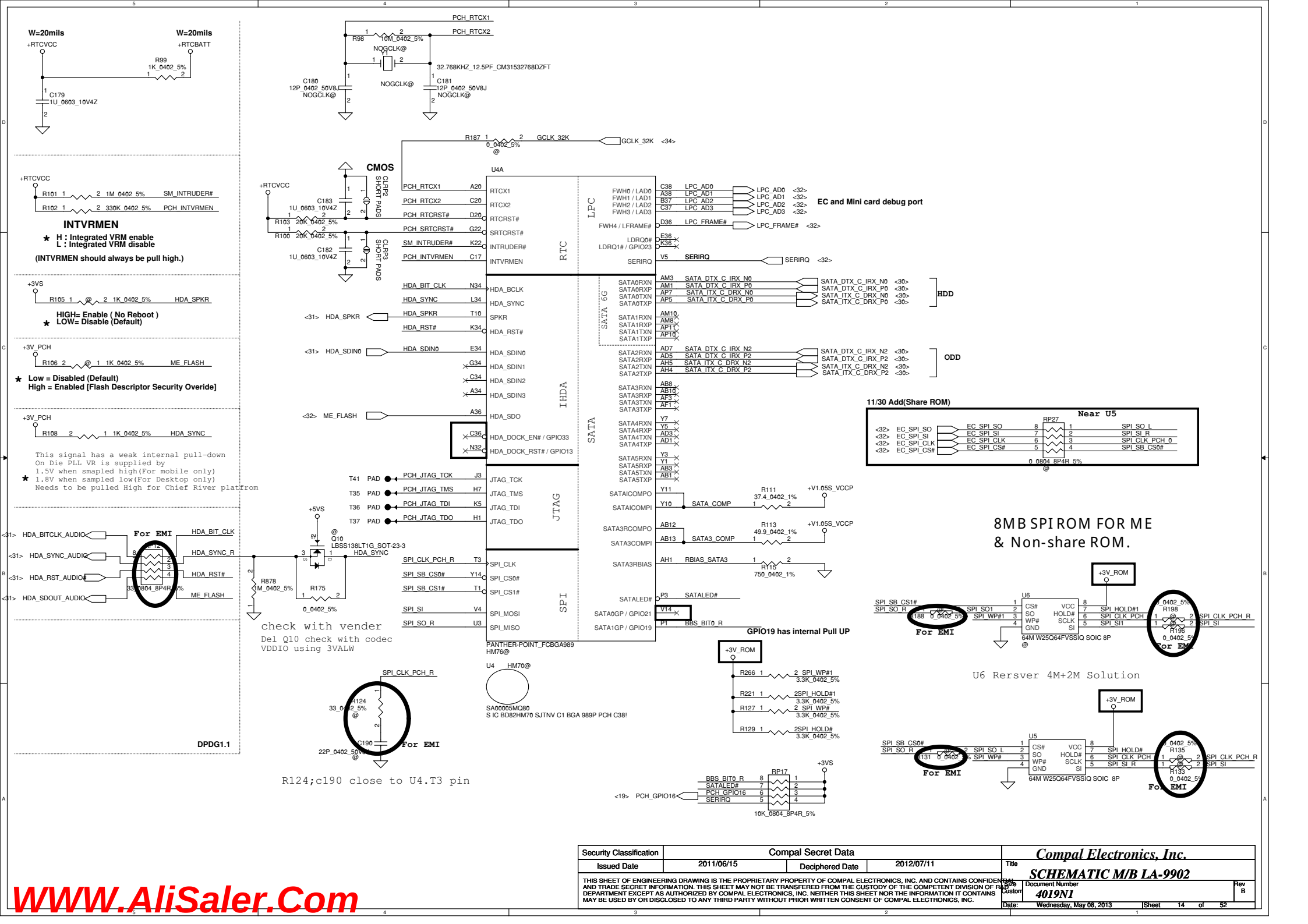
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 13 of 52



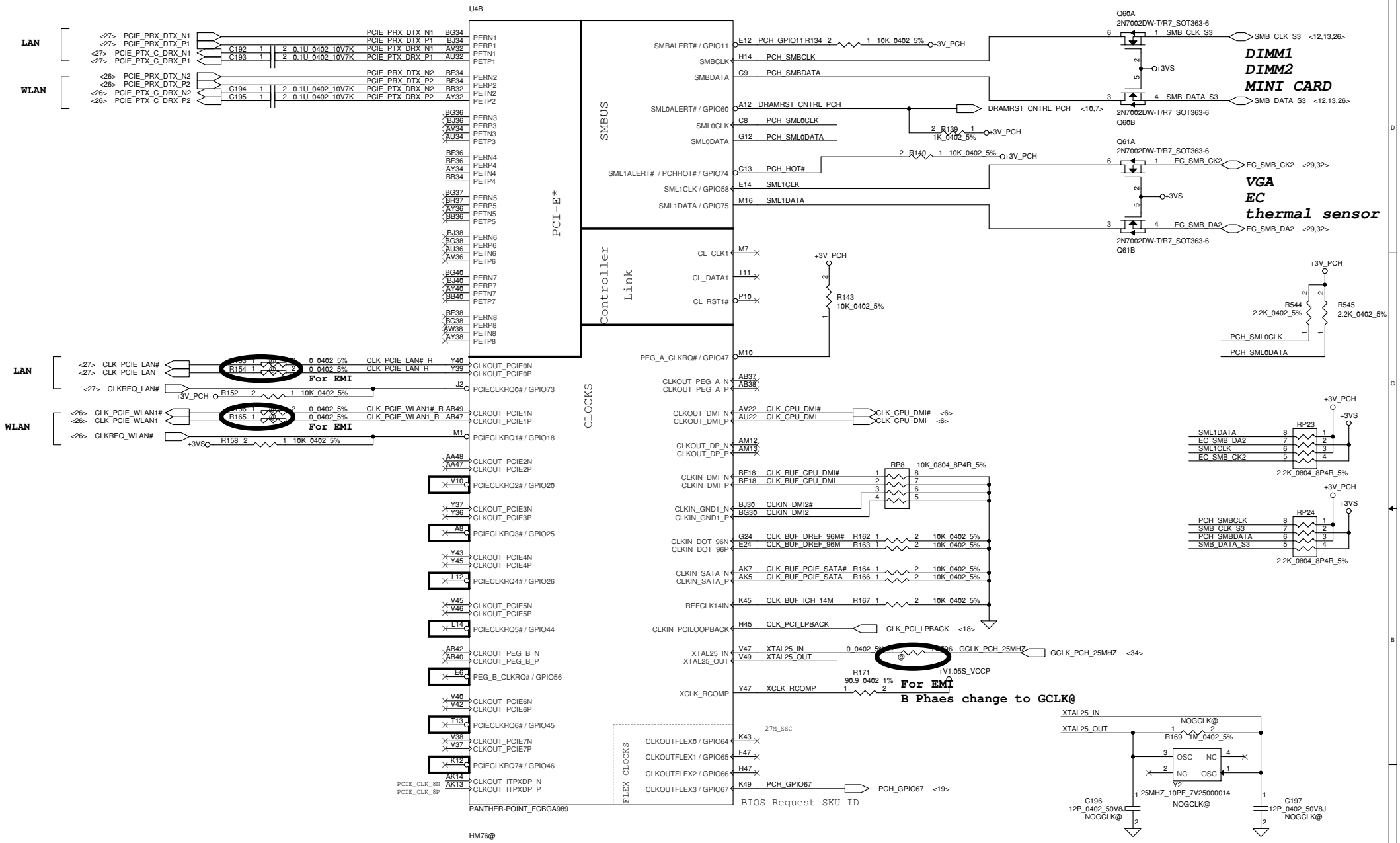
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 14 of 52



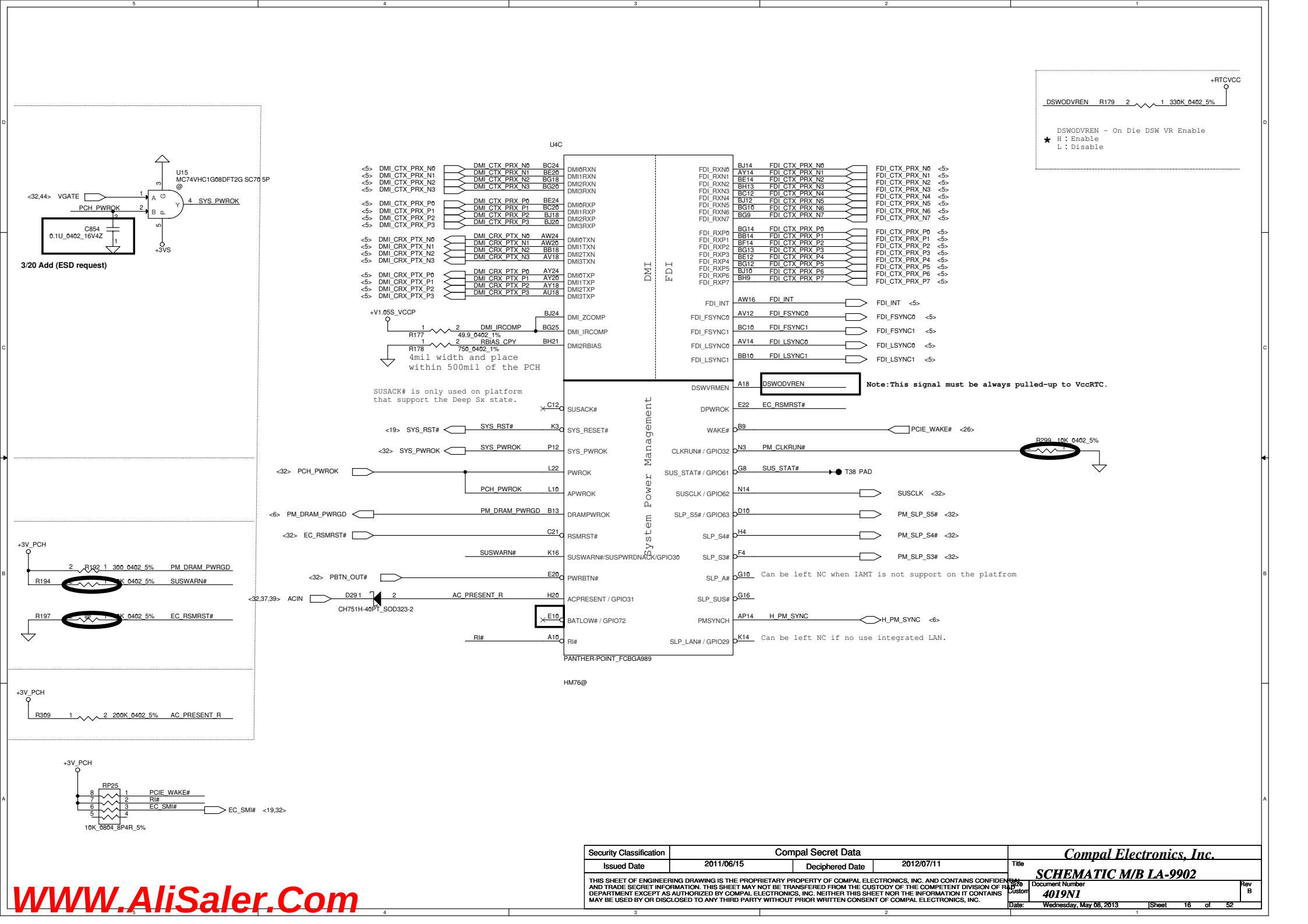
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 15 of 52



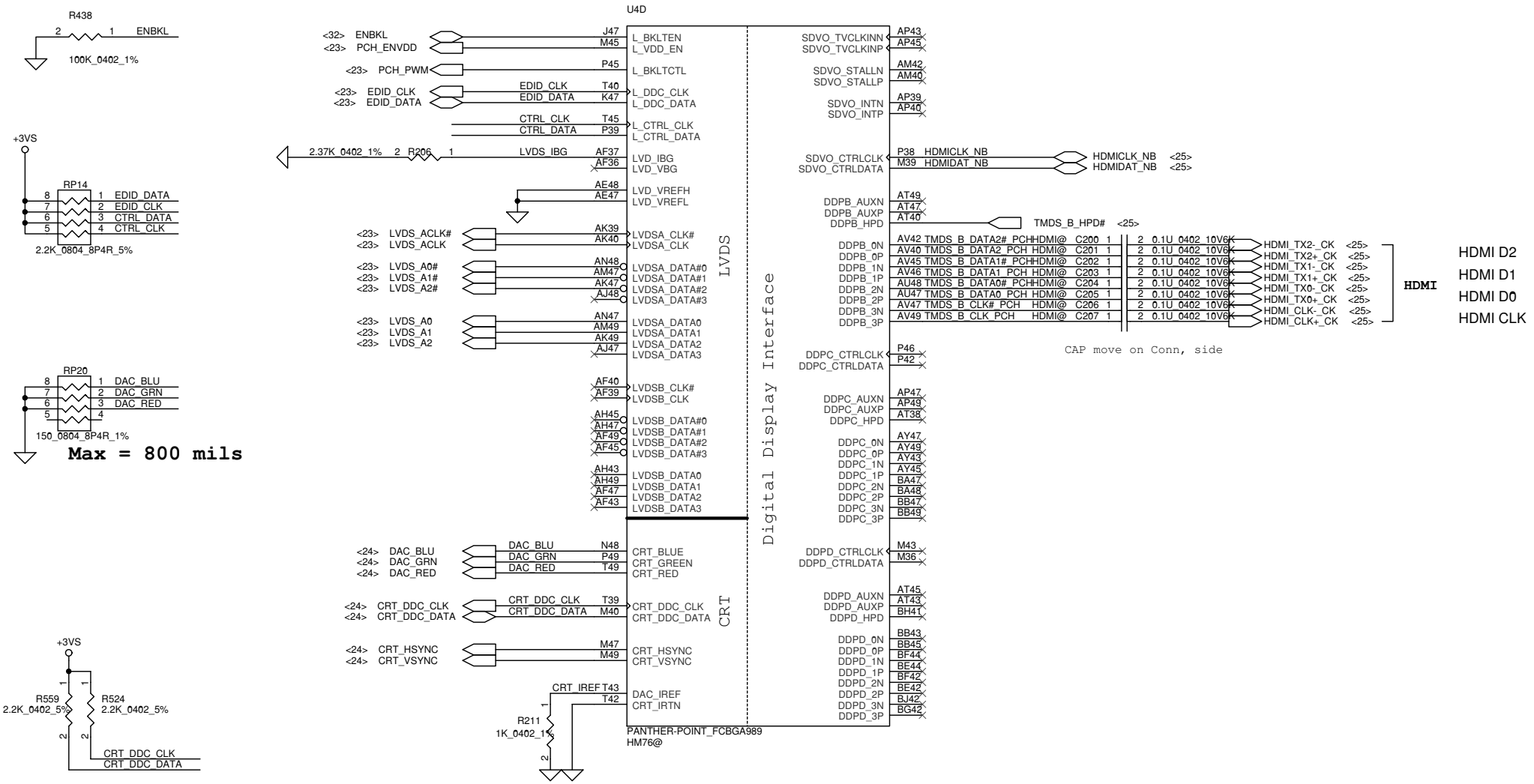
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 16 of 52



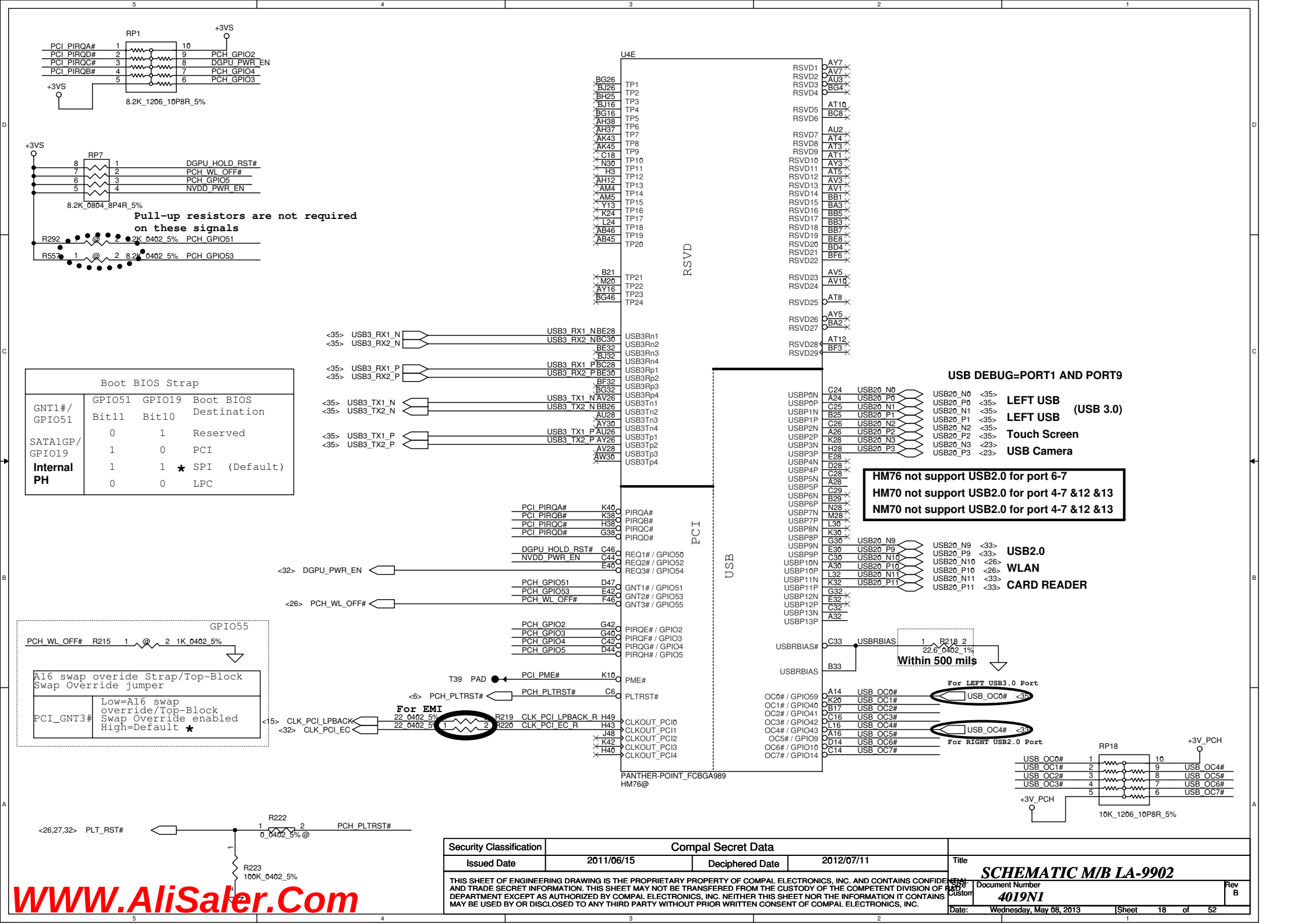
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: B | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 17 of 52



Boot BIOS Strap			
GNT1#/ GPIO51	GPIO51 Bit11	GPIO19 Bit10	Boot BIOS Destination
	0	1	Reserved
SATA1GP/ GPIO19	1	0	PCI
Internal PH	1	1 ★	SPI (Default)
	0	0	LPC

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title	SCHEMATIC M/B LA-9902		
Size: Custom	Document Number: 4019N1		Rev: B
Date: Wednesday, May 08, 2013	Sheet 18 of 52		

PCH_GPIO69	PCH_GPIO70	Function
-	-	NM70
-	-	Reserved
-	1	HM70
-	0	HM76

PCH_GPIO71	Function
1	N14M-GE 1000MHz
0	N14M-GE 900MH

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

★ PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

GPIO36, 37
When Unused as GPIO or SATA*GP
Use 8.2K-10K pull-down to ground.

R244 @ 10K_0402_5% PCH_GPIO37
R881 10K_0402_5% @
R250 @ 10K_0402_5% PCH_GPIO36
R547 10K_0402_5% @

BIOS Request SKU ID

R711 UMA@ 10K_0402_5%
R246 UMA@ 10K_0402_5%
PCH_GPIO38
PCH_GPIO67 PCH_GPIO67 <15>
R708 OPT@ 10K_0402_5%
R298 OPT@ 10K_0402_5%

RP10 10K_0804_8P4R_5%
PCH_GPIO39
SYS_RST# SYS_RST# <16>
PCH_BT_ON#
PCH_GPIO35

R702 @ 10K_0402_5% PCH_GPIO69
R707 @ 10K_0402_5%
R703 HM70@ 10K_0402_5% PCH_GPIO70
R705 HM76@ 10K_0402_5%
R704 1000M@ 10K_0402_5% PCH_GPIO71
R706 900M@ 10K_0402_5%

U4F

GPIO:
T7 BMBUSY# / GPIO0
A42 TACH1 / GPIO1
H36 TACH2 / GPIO6
E38 TACH3 / GPIO7
C10 GPIO8
C4 LAN_PHY_PWR_CTRL / GPIO12
G2 GPIO15
U2 SATA4GP / GPIO16
D40 TACH0 / GPIO17
T5 SCLOCK / GPIO22
E8 GPIO24
E16 GPIO27
P8 GPIO28
K1 STP_PCI# / GPIO34
K4 GPIO35
V8 SATA2GP / GPIO36
M5 SATA3GP / GPIO37
N2 SLOAD / GPIO38
M3 SDATAOUT0 / GPIO39
V13 SDATAOUT1 / GPIO48
V3 SATA5GP / GPIO49 / TEMP_ALERT#
D6 GPIO57

CPU/MISC:
C40 TACH4 / GPIO68
B41 TACH5 / GPIO69 PCH_GPIO69
C41 TACH6 / GPIO70 PCH_GPIO70
A40 TACH7 / GPIO71 PCH_GPIO71
P4 A20GATE
AU16 PECI
P5 RCIN# KBRST# KBRST# <32>
AY11 PROCPWRGD H_CPUPWRGD <6>
AY10 THRMTRIP# PCH_THRMTRIP#_R 1 R239 2 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
T14 INIT3_3V#
AY1 DF_TVS
AH8 TS_VSS1
AK11 TS_VSS2
AH10 TS_VSS3
AK10 TS_VSS4
P37 NC_1

NCTF:
A4 VSS_NCTF_1
A44 VSS_NCTF_2
A45 VSS_NCTF_3
A46 VSS_NCTF_4
A5 VSS_NCTF_5
A6 VSS_NCTF_6
B3 VSS_NCTF_7
B47 VSS_NCTF_8
BD1 VSS_NCTF_9
BD49 VSS_NCTF_10
BE1 VSS_NCTF_11
BE49 VSS_NCTF_12
BF1 VSS_NCTF_13
BF49 VSS_NCTF_14
BG2 VSS_NCTF_15
BG48 VSS_NCTF_16
BH3 VSS_NCTF_17
BH47 VSS_NCTF_18
BJ4 VSS_NCTF_19
BJ44 VSS_NCTF_20
BJ45 VSS_NCTF_21
BJ46 VSS_NCTF_22
BJ5 VSS_NCTF_23
BJ6 VSS_NCTF_24
C2 VSS_NCTF_25
C48 VSS_NCTF_26
D1 VSS_NCTF_27
D49 VSS_NCTF_28
E1 VSS_NCTF_29
E49 VSS_NCTF_30
F1 VSS_NCTF_31
F49 VSS_NCTF_32

PANTHER-POINT_FCBGA989

HM76@

R236 10K_0402_5%
GATEA20 <32>
KBRST# R226 1 2 10K_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
Weak internal PU,Do not pull low
CLOSE TO THE BRANCHING POINT

PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
0	1	Reserved
1	0	DIS
1	1	UMA

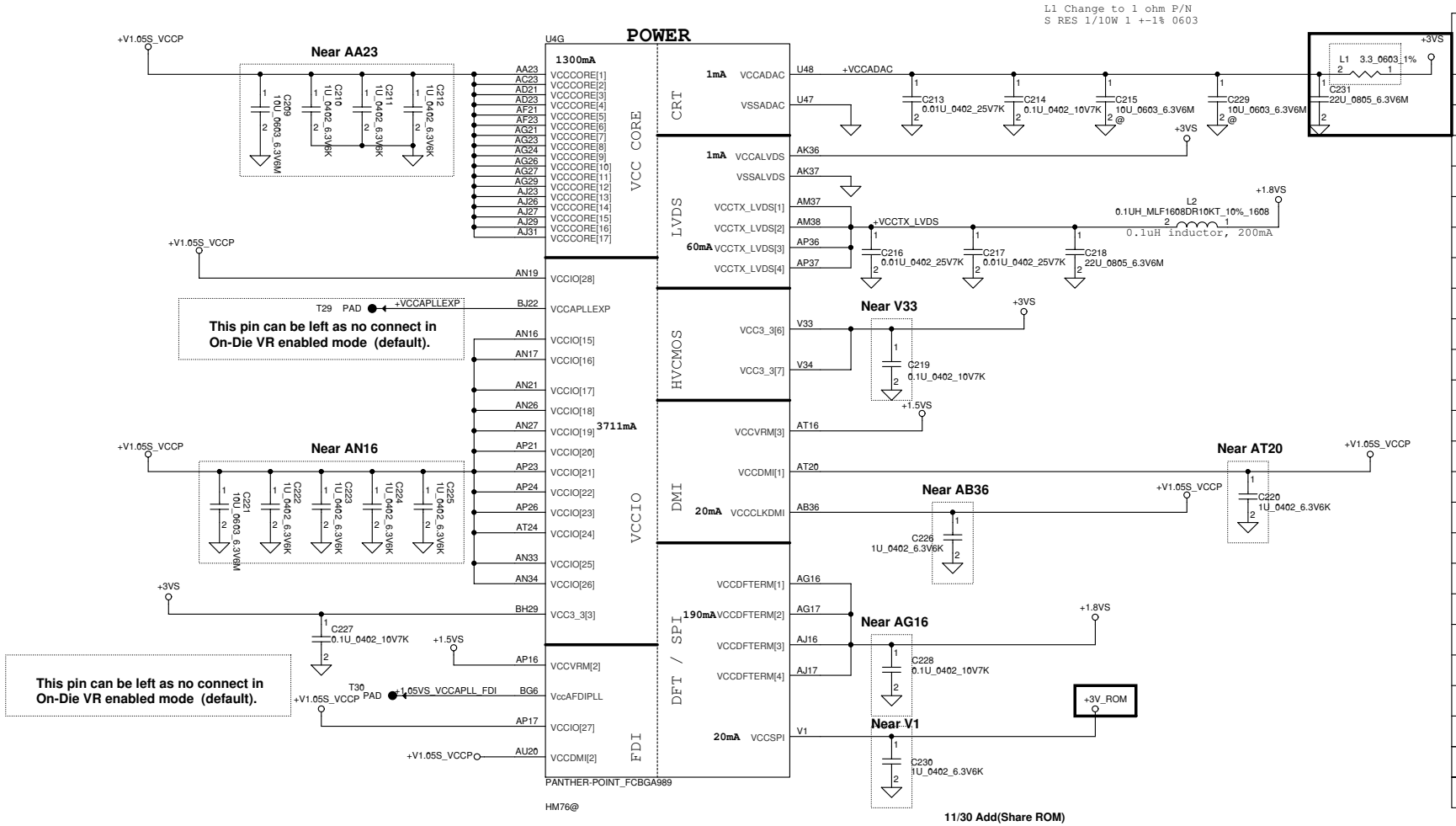
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 19 of 52



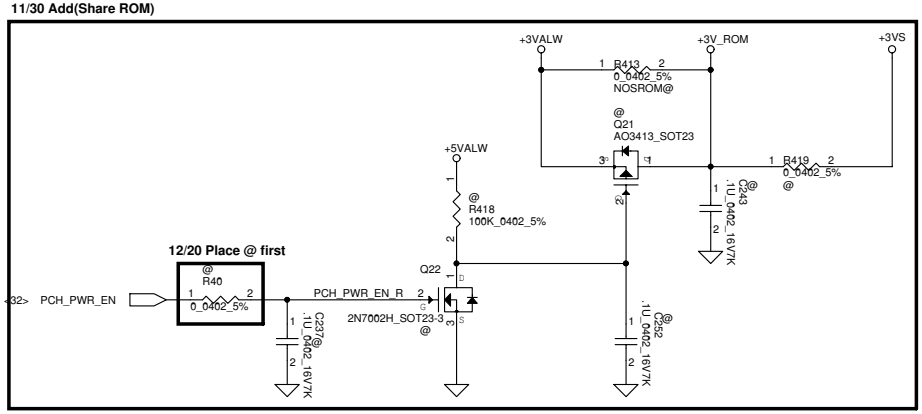
PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Intel recommand stuff R265 and unstuff R266

VCCVRM==>1.5V FOR MOBILE
VCCVRM==>1.8V FOR DESKTOP

VCCVRM = 160mA detal waiting for newest spec

11/30 Add(Share ROM)



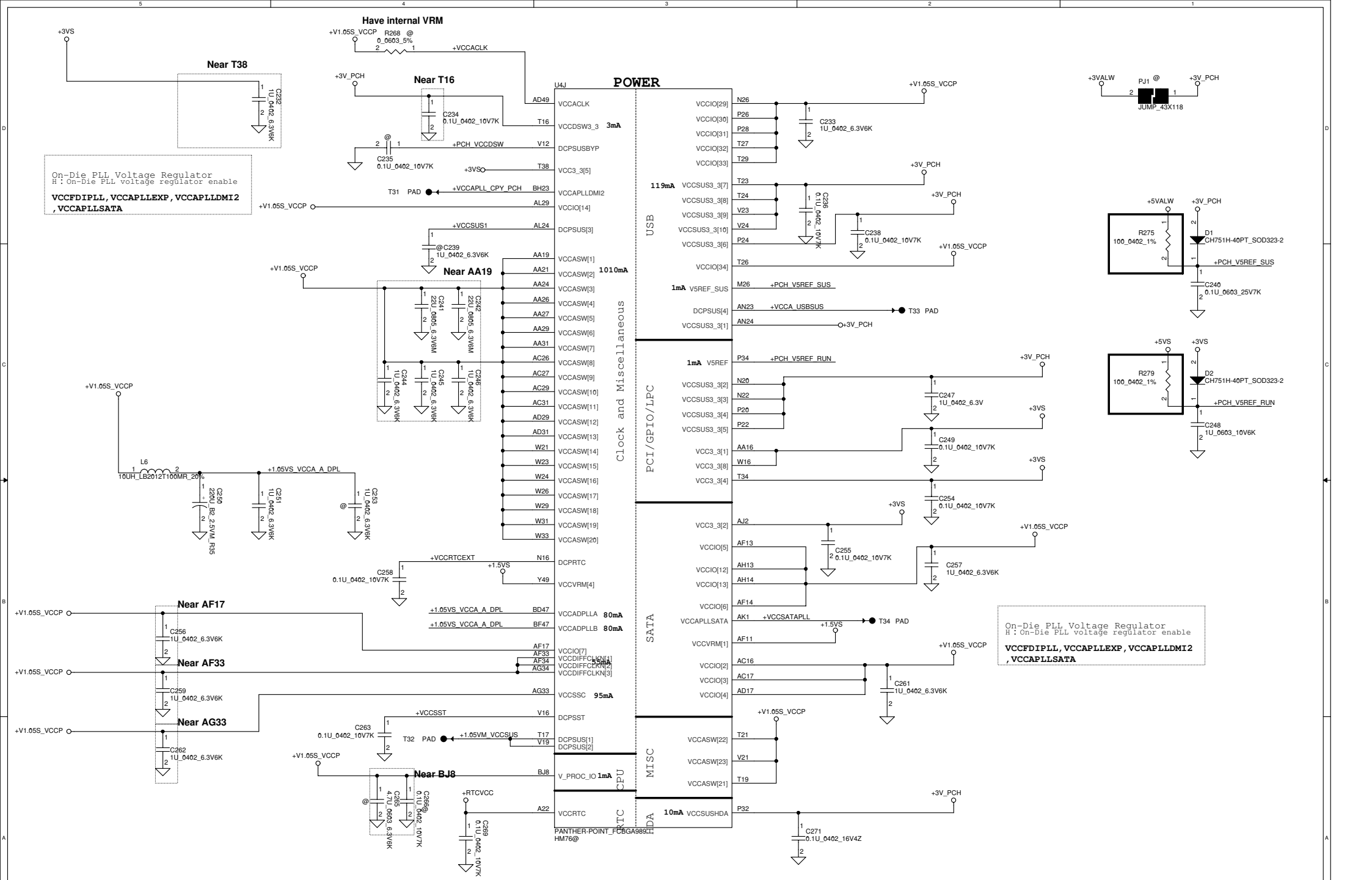
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 20 of 52



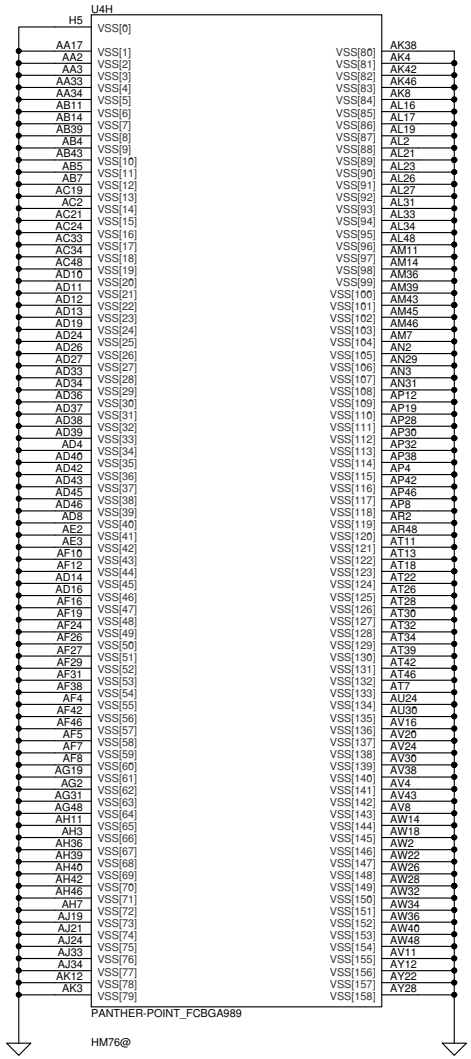
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

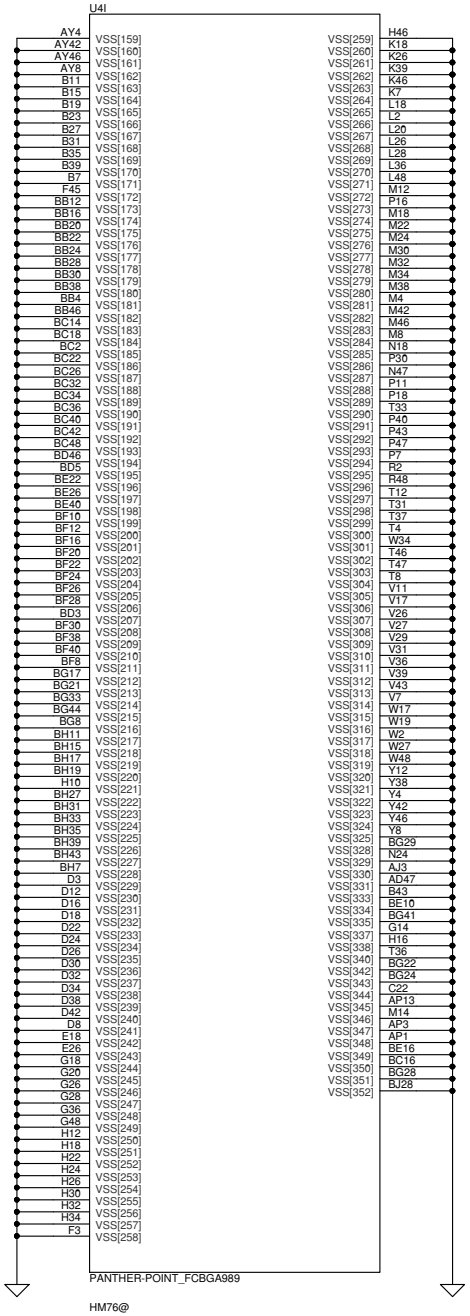
Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 21 of 52





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

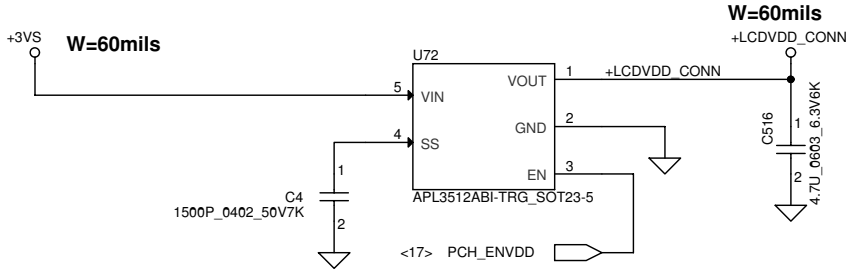
Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

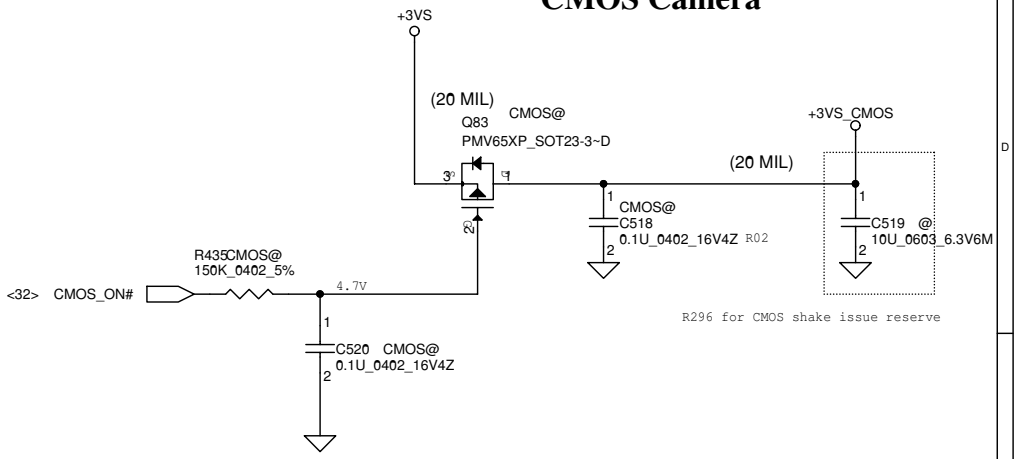
Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 22 of 52

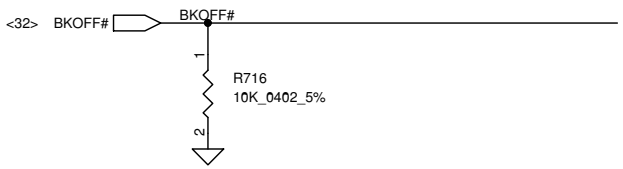
LCD POWER CIRCUIT



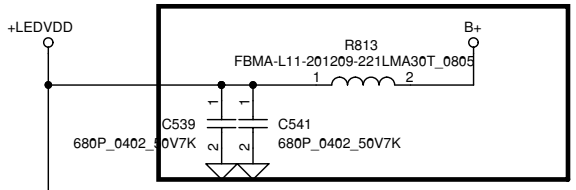
CMOS Camera



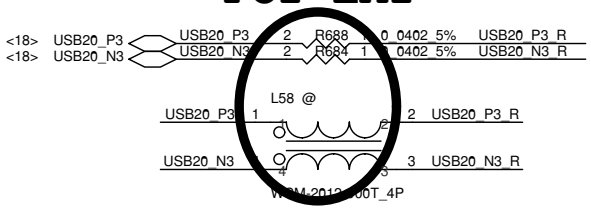
VGA LCD/PANEL BD. Conn.

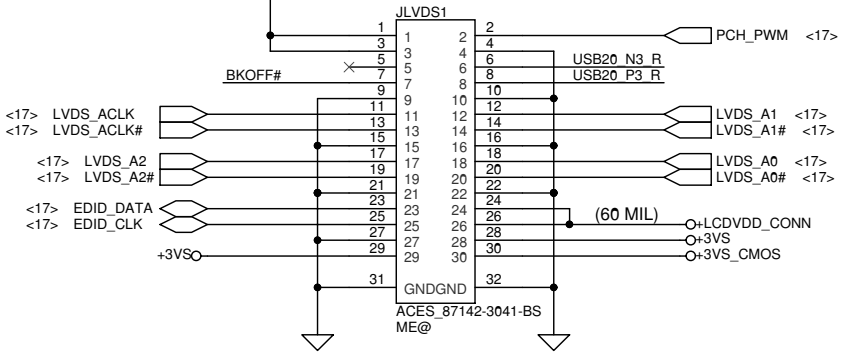


12/12 Mount C539/C541 of 680pF,Chanage R813 to 220 ohm bead.(For EMI request)



For EMI





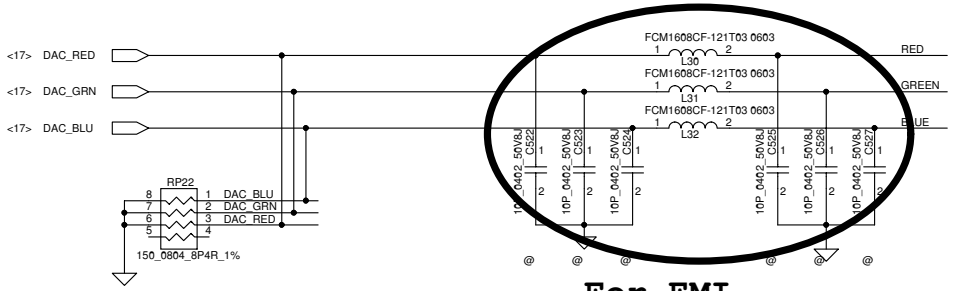
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

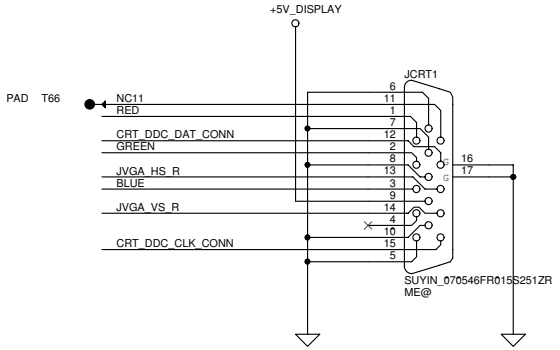
Title: **SCHEMATIC M/B LA-9902**

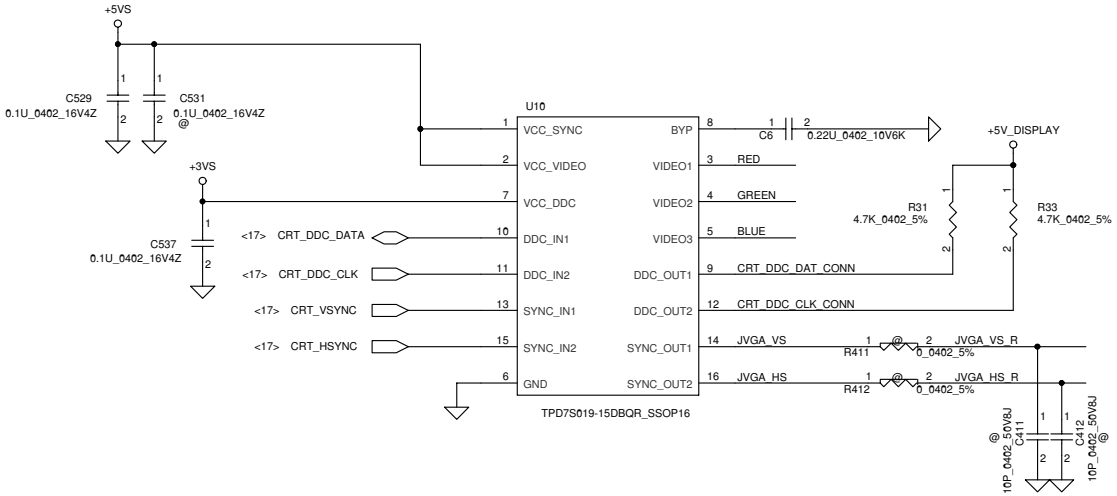
Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 23 of 52



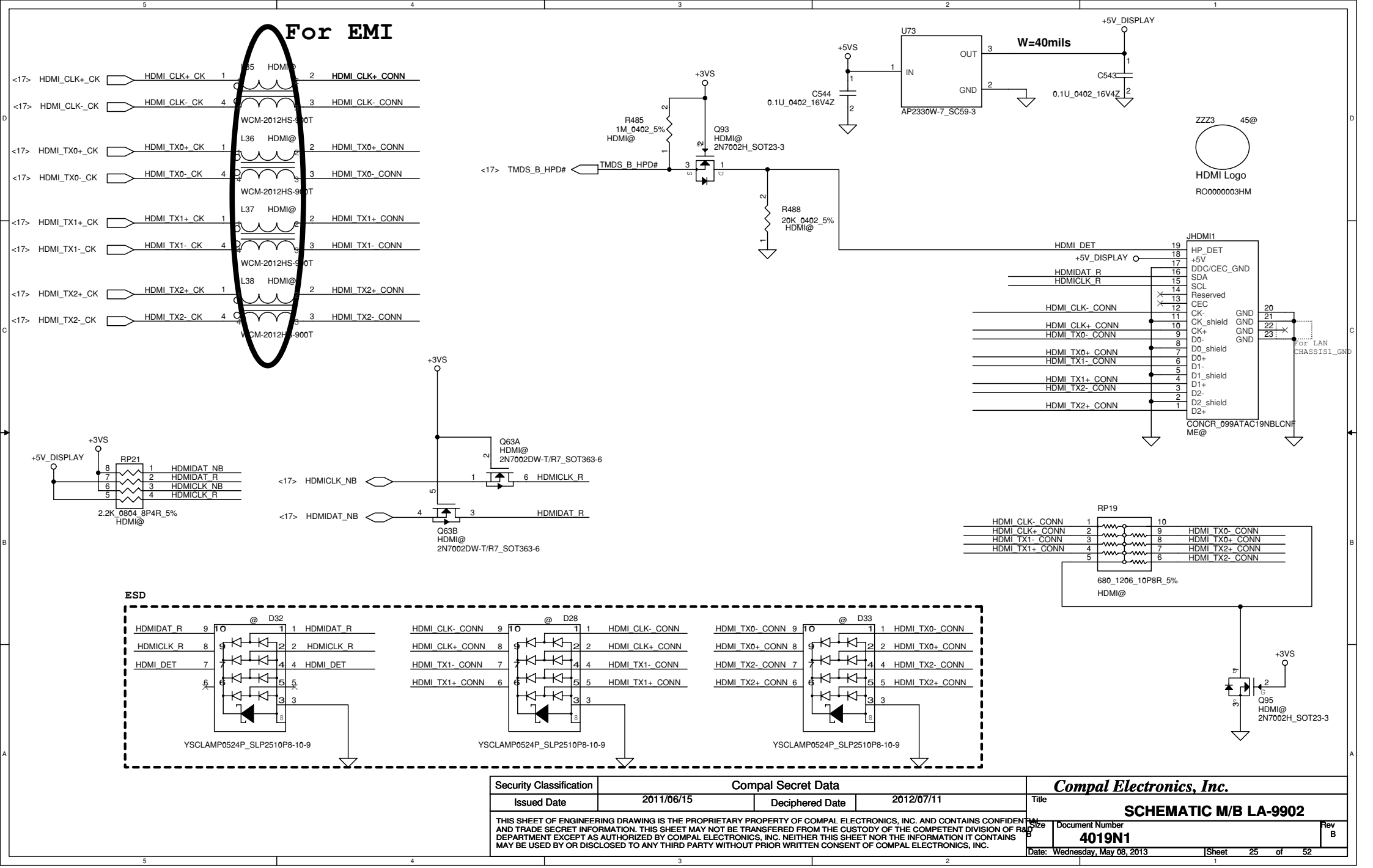
For EMI





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: SCHEMATIC M/B LA-9902			
Size: Custom	Document Number: 4019N1		Rev: B
Date: Wednesday, May 08, 2013	Sheet 24 of 52		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

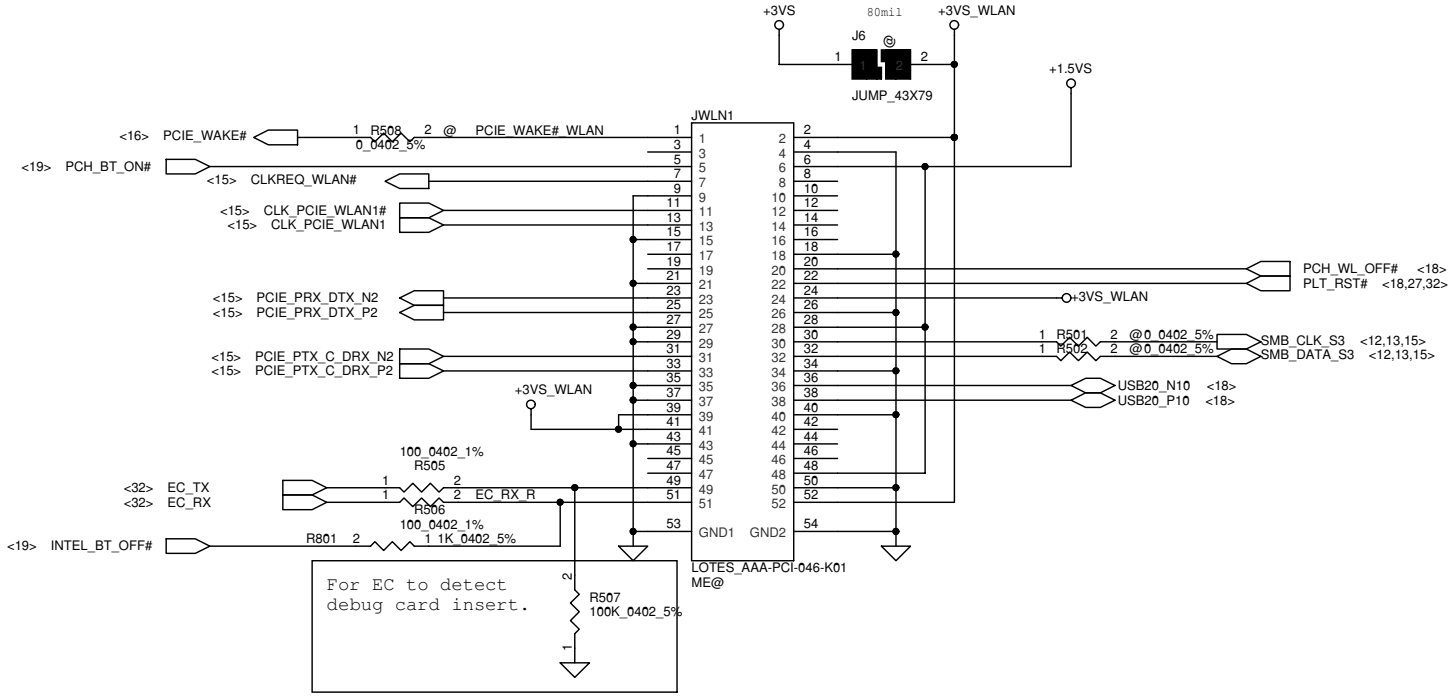
Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
B	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 25 of 52

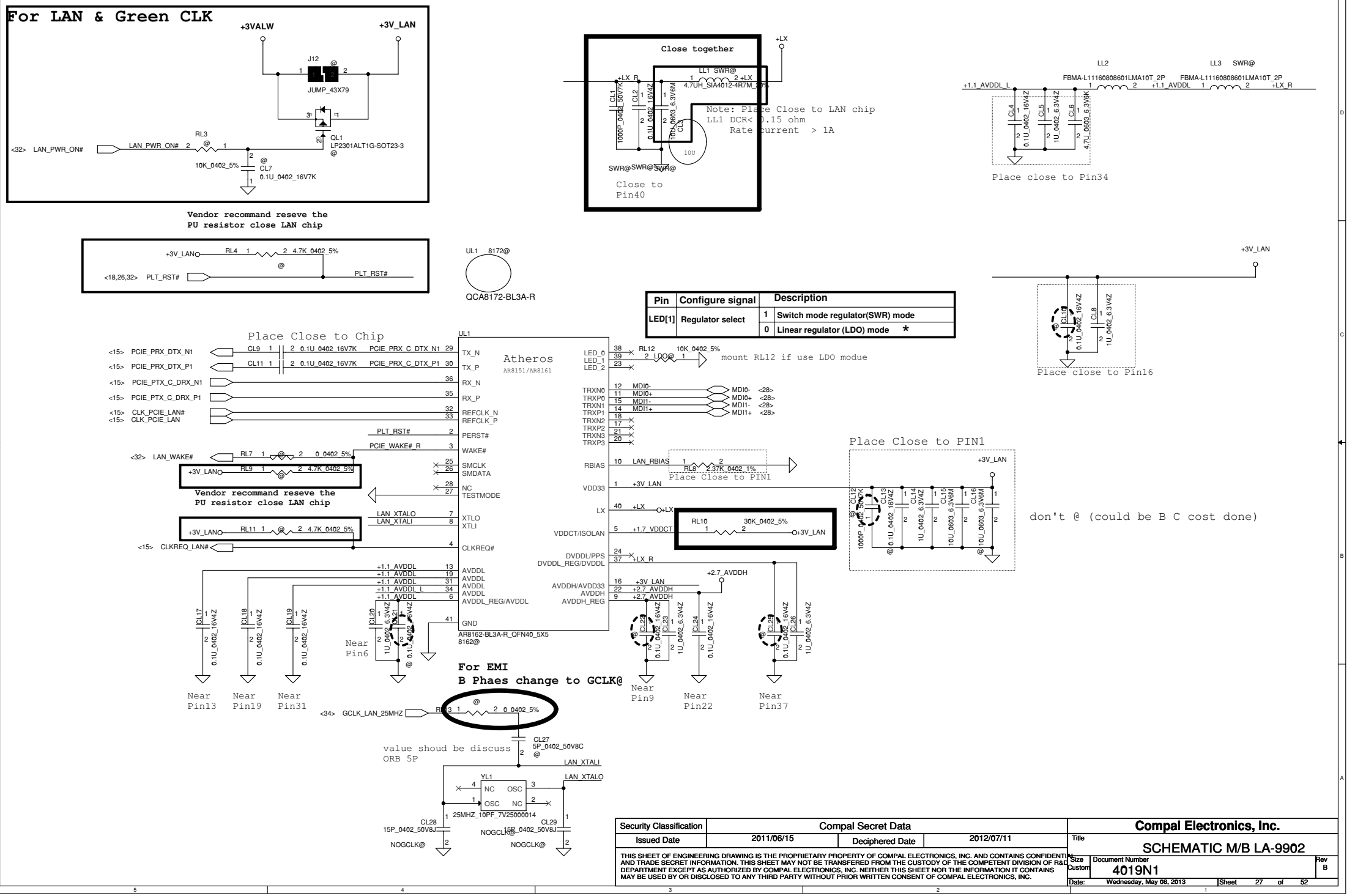
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: SCHEMATIC M/B LA-9902			
Size	Document Number: 4019N1		Rev: B
Date: Wednesday, May 08, 2013	Sheet 26 of 52		



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 27 of 52

ESD

Place Close to TL1

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

@
DL1
AZC099-04S.R7G_SOT23-6
MDI1+ 1 I/O1
2 GND
MDI0- 3 I/O2
I/O3 4 MDI0+
VDD 5
I/O4 6 MDI1-

Reserve gas tube for EMI go rural solution

For EMI

CL30 10P_0603_50V
CHASSIS1_GND
BS4200N-C-LV_SMB-F2
GAS@

Place Close to TL1

For EMI

12/12 Change BOM Structure of CL31 from @ to mount(EMI request)

CL31 0.01U_0402_16V7K

TL1
<27> MDI0+ MDI0+ 1 TD+ TX+ 16 MDO0+
<27> MDI0- MDI0- 2 TD- TX- 15 MDO0-
3 CT CT 14 MCT
4 NC NC 13
5 NC NC 12
6 NC NC 11 MCT
<27> MDI1+ MDI1+ 7 CT CT 10 MDO1+
<27> MDI1- MDI1- 8 RD+ RX+ 9 MDO1-
RD- RX-
MHPC_NS681612A

For EMI

CL63 0.1U_0603_50V7K
CHASSIS1_GND

JLAN1
MCT 8 PR4-
MCT 7 PR4+
MDO1- 6 PR2-
MCT 5 PR3-
MCT 4 PR3+
MDO1+ 3 PR2+
MDO0- 2 PR1-
MDO0+ 1 PR1+
SHLD1 10
SHLD2 9
PS_HPKR0125-08A1A0R
ME@
CHASSIS1_GND

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

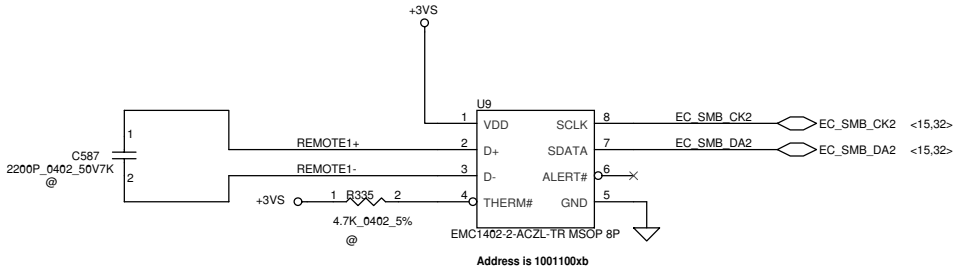
Title: SCHEMATIC M/B LA-9902

Size: B | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 28 of 52

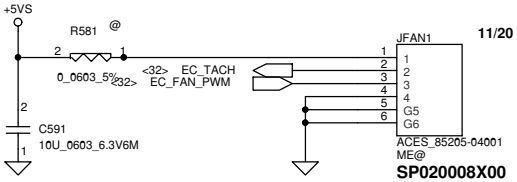
2 Channel

SMSC thermal sensor placed near VRAM



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



11/20 Change symbol of JFAN1 to SP020008X00

MINI WLAN VGA CPU

H1 H_3P3 H2 H_3P3 H4 H_3P3 H5 H_3P8 H6 H_3P8 H7 H_3P8

FD1 FD2 FD3 FD4

H14 H_2P8 H15 H_2P8 H19 H_2P8 H20 H_2P8 H22 H_2P8 H23 H_2P8

R

H16 H_3P0X4P0N H24 H_3P0N H25 H_3P0N

E

M/B 橢圓孔 M/B 圓孔

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

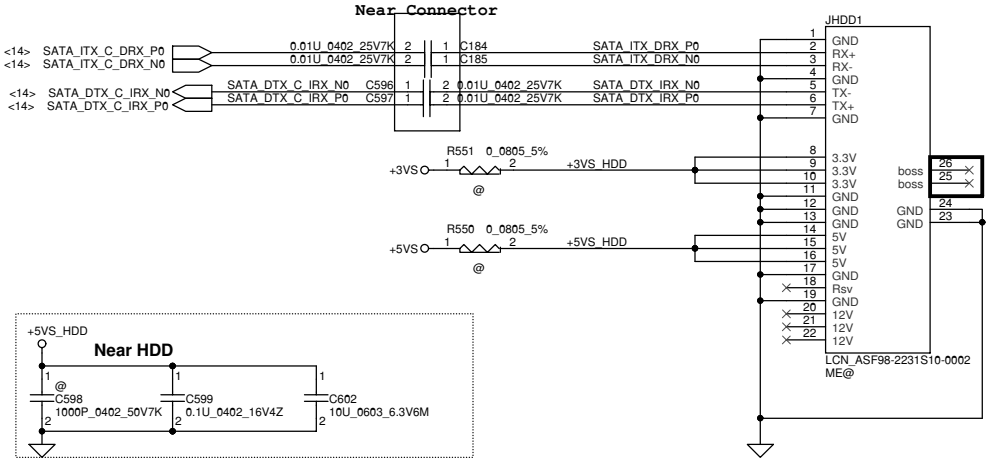
Compal Electronics, Inc.

Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: **4019N1** | Rev: B

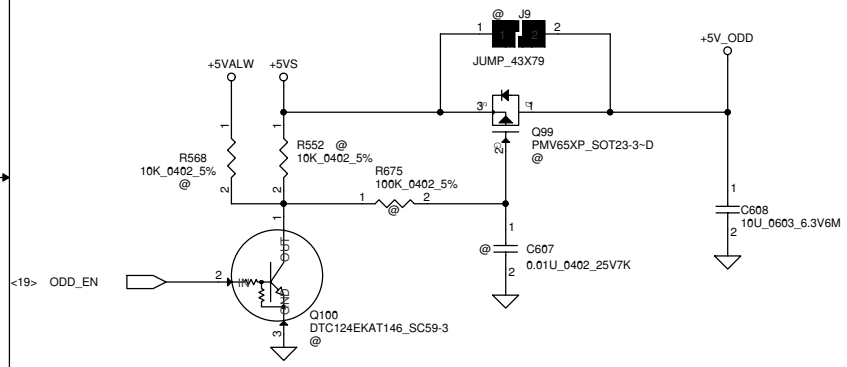
Date: Wednesday, May 08, 2013 | Sheet 29 of 52

SATA HDD Conn.



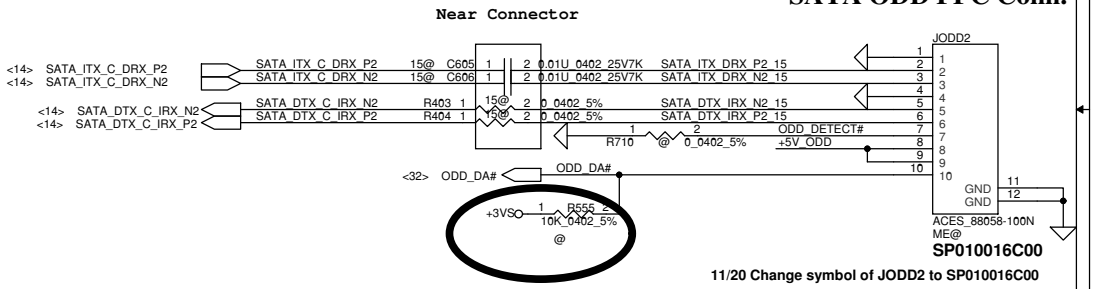
1/16 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)

ODD Power Control



FOR 15"

SATA ODD FFC Conn.

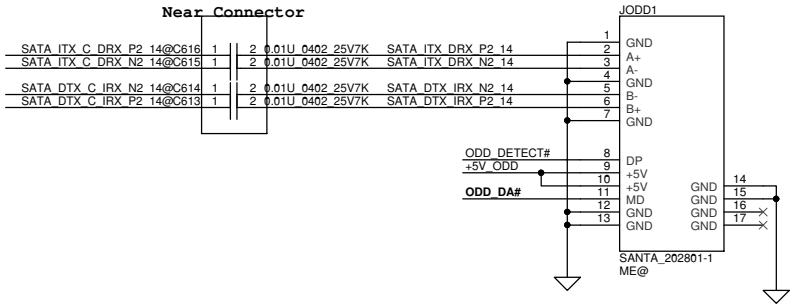


11/20 Change symbol of JODD2 to SP010016C00

Co-lay

FOR 14"

SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

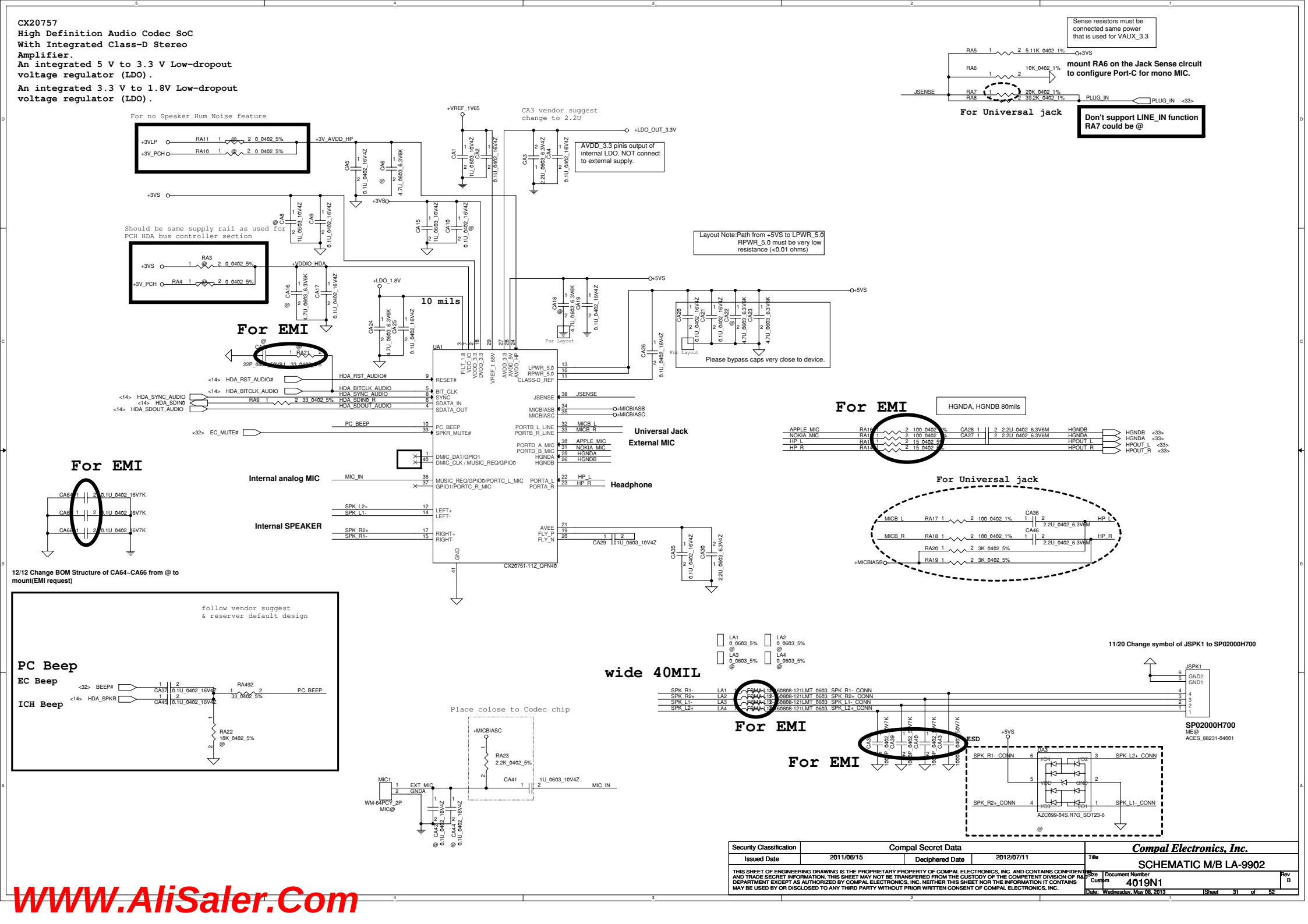
Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 30 of 52

CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



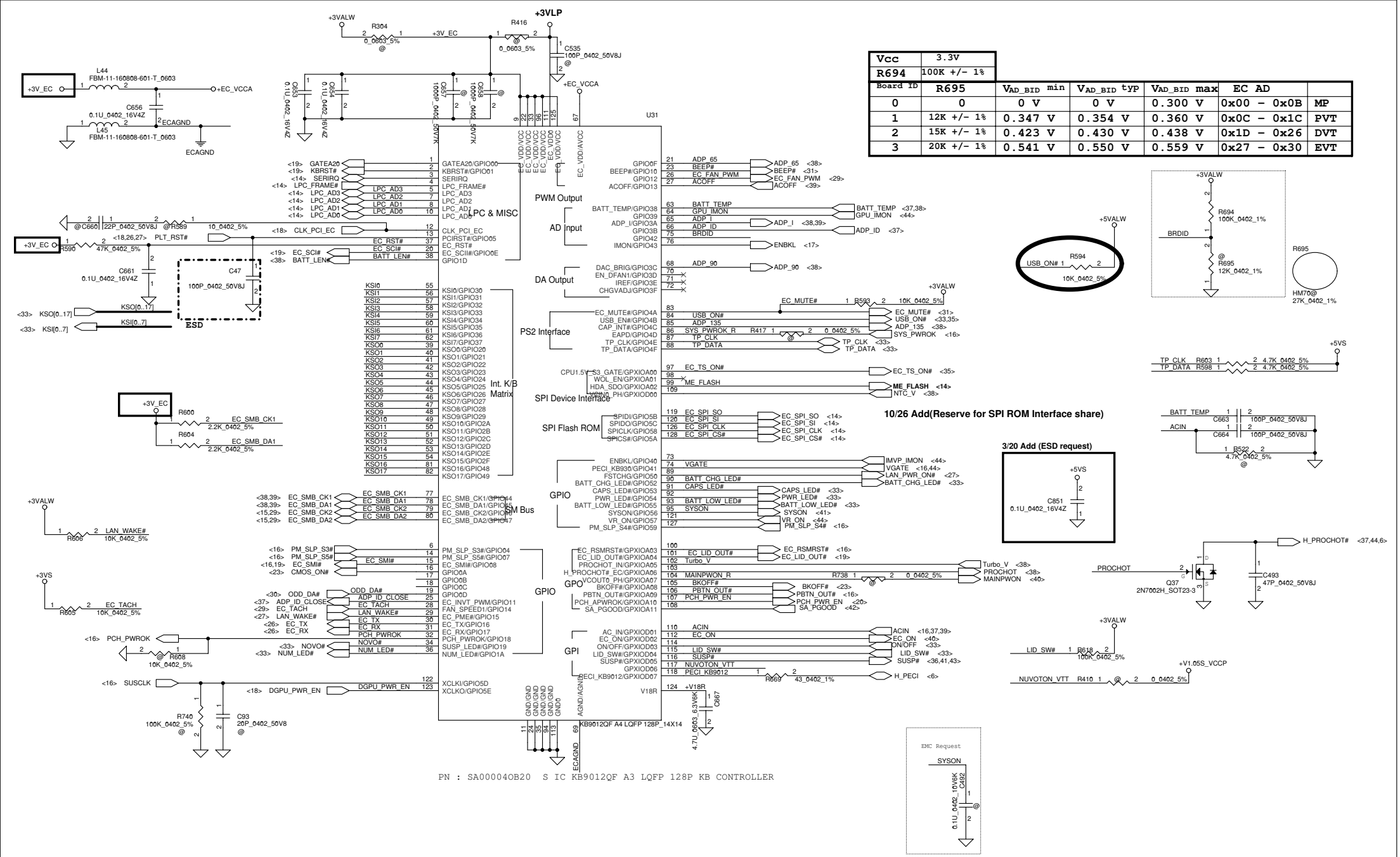
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 31 of 52



Vcc	3.3V					
R694	100K +/- 1%					
Board ID	R695	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD	
0	0	0 V	0 V	0.300 V	0x00 - 0x0B	MP
1	12K +/- 1%	0.347 V	0.354 V	0.360 V	0x0C - 0x1C	PVT
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26	DVT
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30	EVT

PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

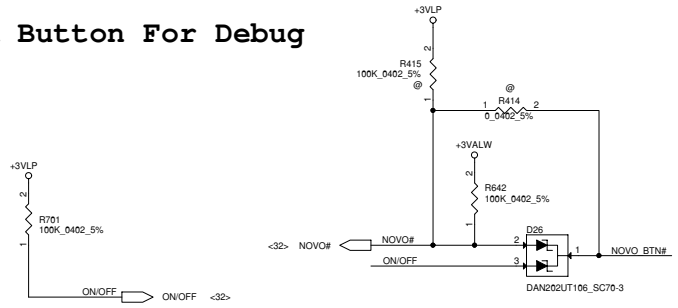
Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

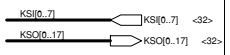
Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 32 of 52

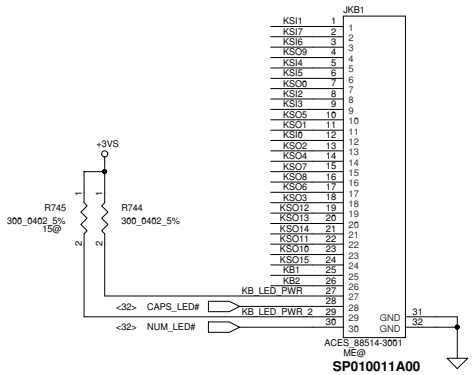
PWR Button For Debug



Key Board Conn.



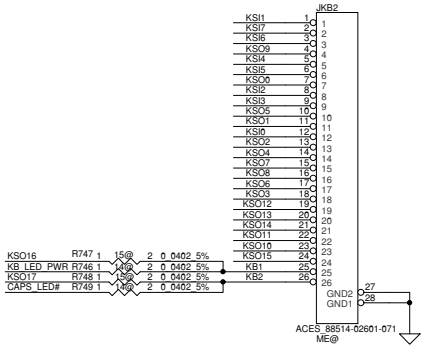
For 15"



SP010011A00

11/20 Change symbol of JKB1 to SP010011A00

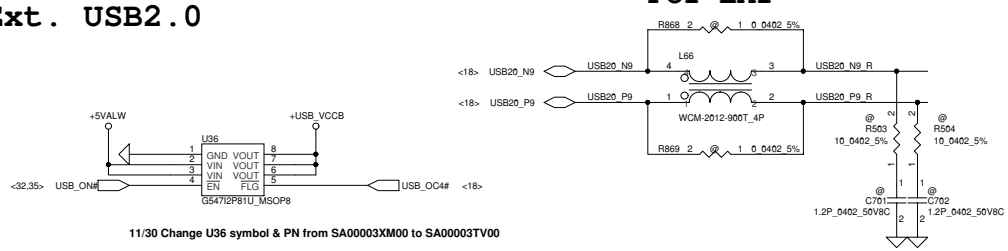
For 14"



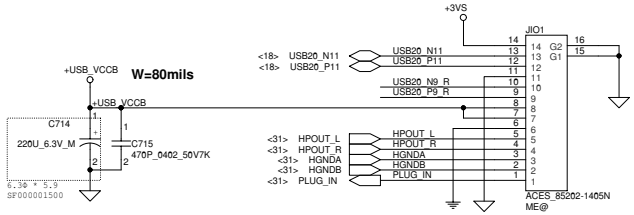
IO/B Conn.

Ext. USB2.0

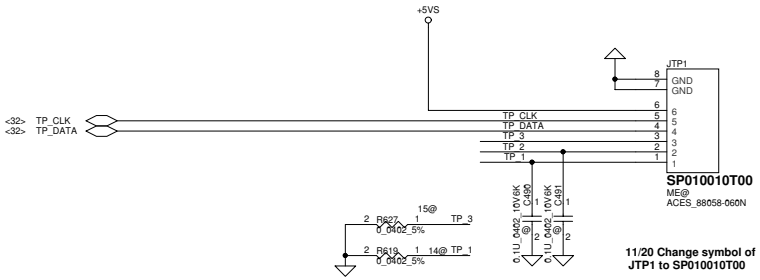
For EMI



11/30 Change U36 symbol & PN from SA00003XM00 to SA00003TV00



TP Switch & TP Conn.

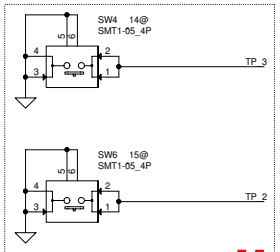


SP010010T00

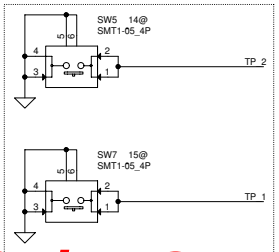
ME@
ACES_88058-060N

11/20 Change symbol of JTP1 to SP010010T00

L



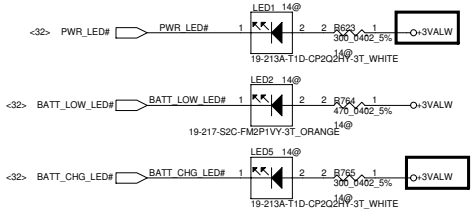
R



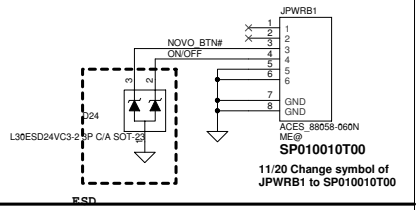
15"	
1	VCC
2	CLK
3	DAT
4	GND
5	L
6	R

14"	
1	VCC
2	CLK
3	DAT
4	L
5	R
6	GND

LED



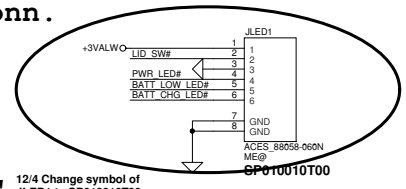
PWR/B Conn.



SP010010T00

11/20 Change symbol of JPWRB1 to SP010010T00

LED/B Conn.

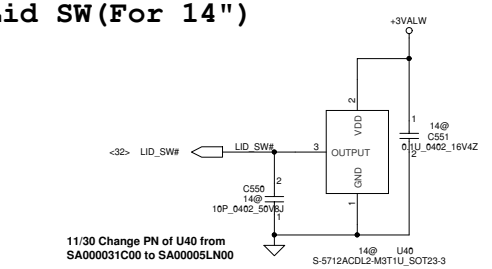


SP010010T00

For 15"

12/4 Change symbol of JLED1 to SP010010T00

Lid SW(For 14")



11/30 Change PN of U40 from SA000031C00 to SA00005LN00

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: C | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 33 of 52

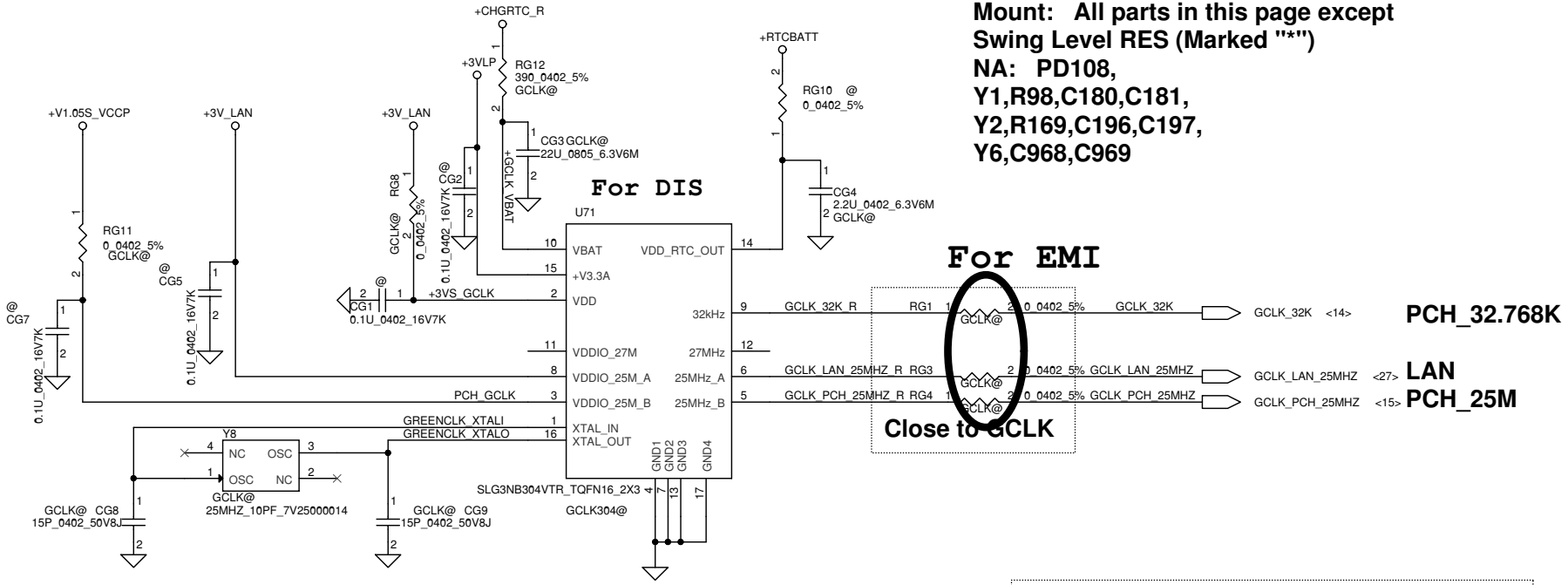
For UMA

U71 GCLK244@

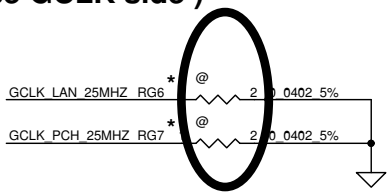
SLG3NB244VTR_TQFN16_2X3

Every power trace need:
W=20mils

For GreenCLK generate CLK:
Mount: All parts in this page except Swing Level RES (Marked "*")
NA: PD108,
Y1,R98,C180,C181,
Y2,R169,C196,C197,
Y6,C968,C969



Reserved for Swing Level adjustment
(Close GCLK side)



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

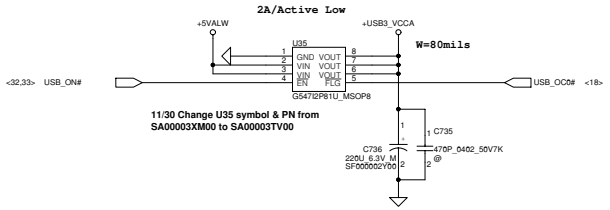
Title: SCHEMATIC M/B LA-9902

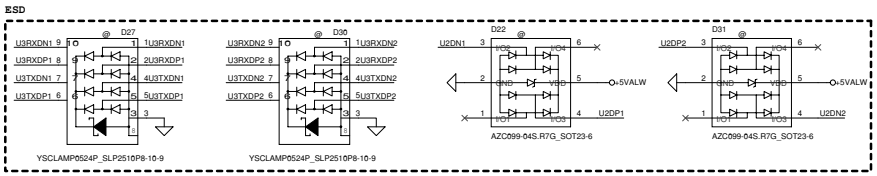
Size: B | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 34 of 52

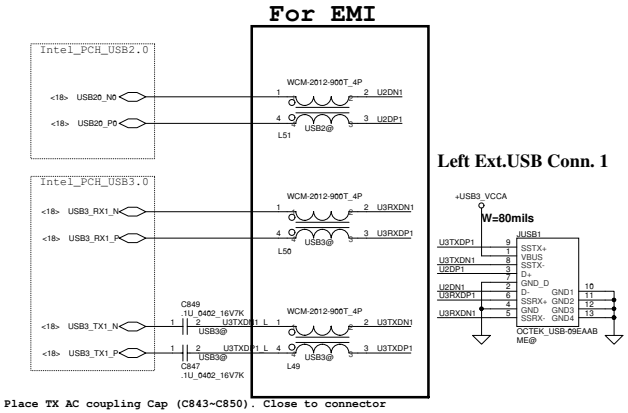
Touch Screen

USB3.0





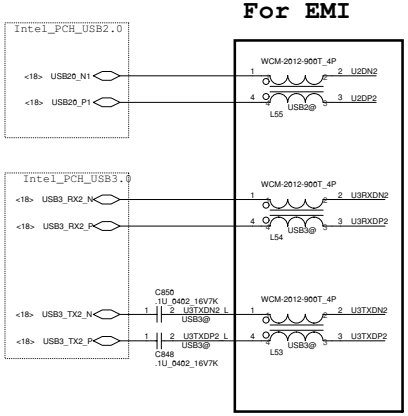
For EMI



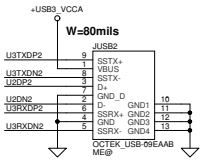
Place TX AC coupling Cap (C843~C850). Close to connector

Left Ext.USB Conn. 1

For EMI



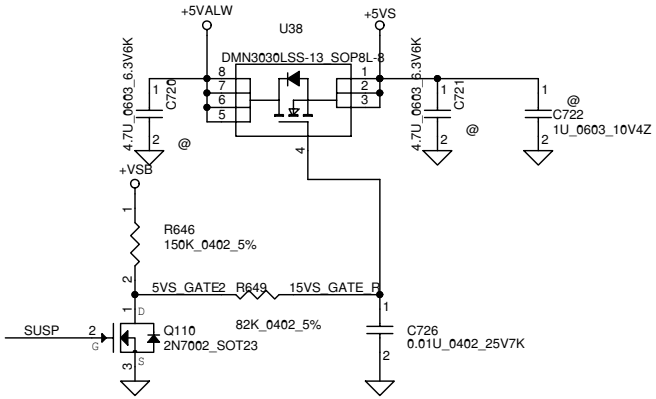
Left Ext.USB Conn. 2



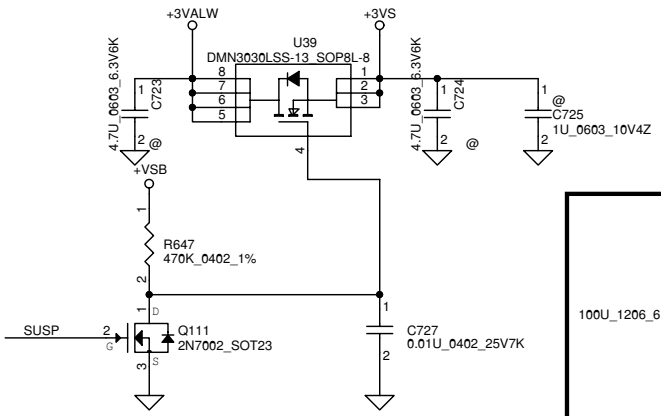
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

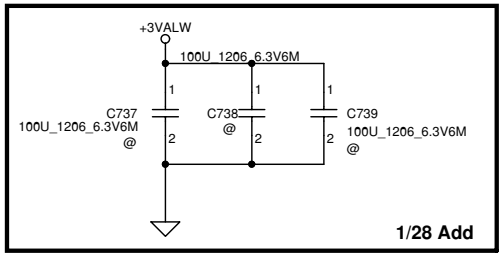
Compal Electronics, Inc.			
Title: SCHEMATIC M/B LA-9902			
Size: Custom	Document Number: 4019N1		Rev: B
Date: Wednesday, May 08, 2013	Sheet 35 of 52		

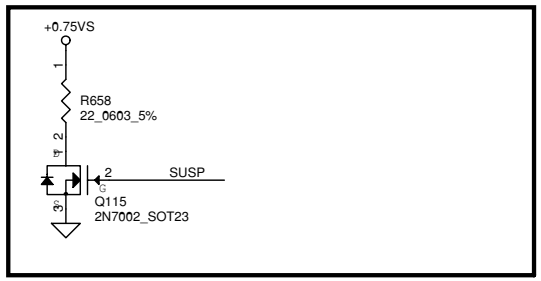
+5VALW to +5VS



+3VALW to +3VS

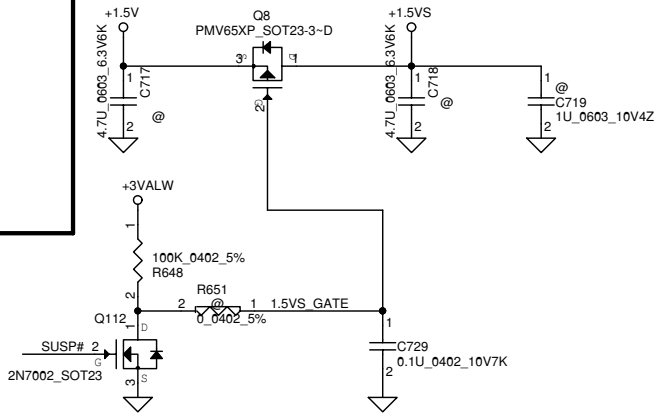


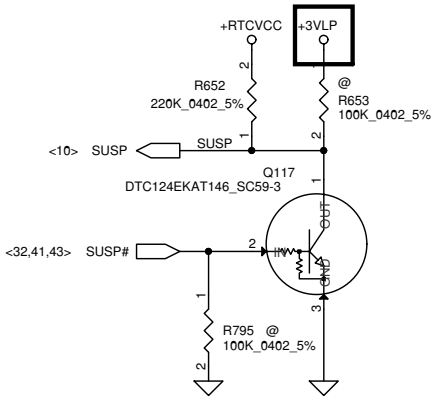




For Intel S3 Power Reduction.

+1.5V to +1.5VS





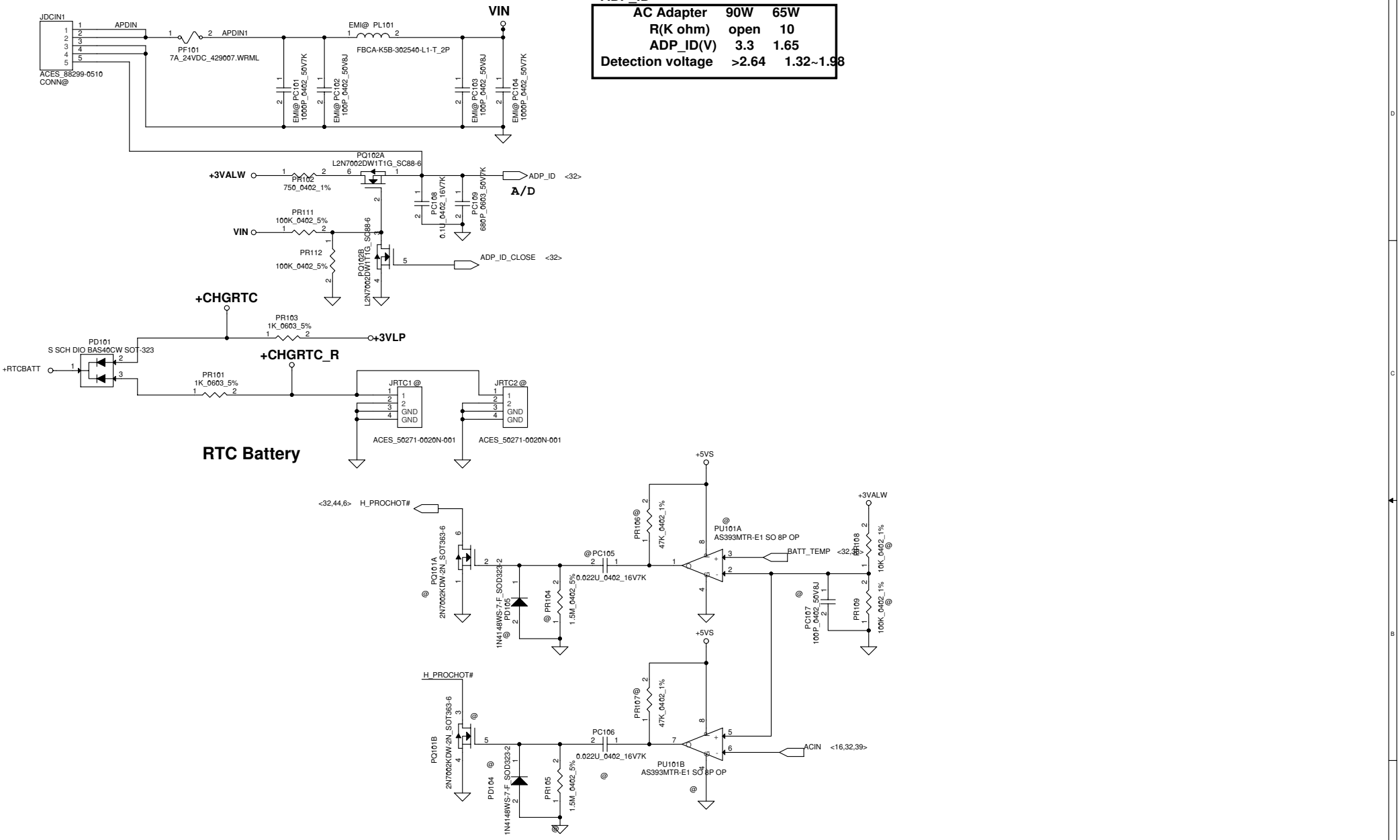
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 36 of 52



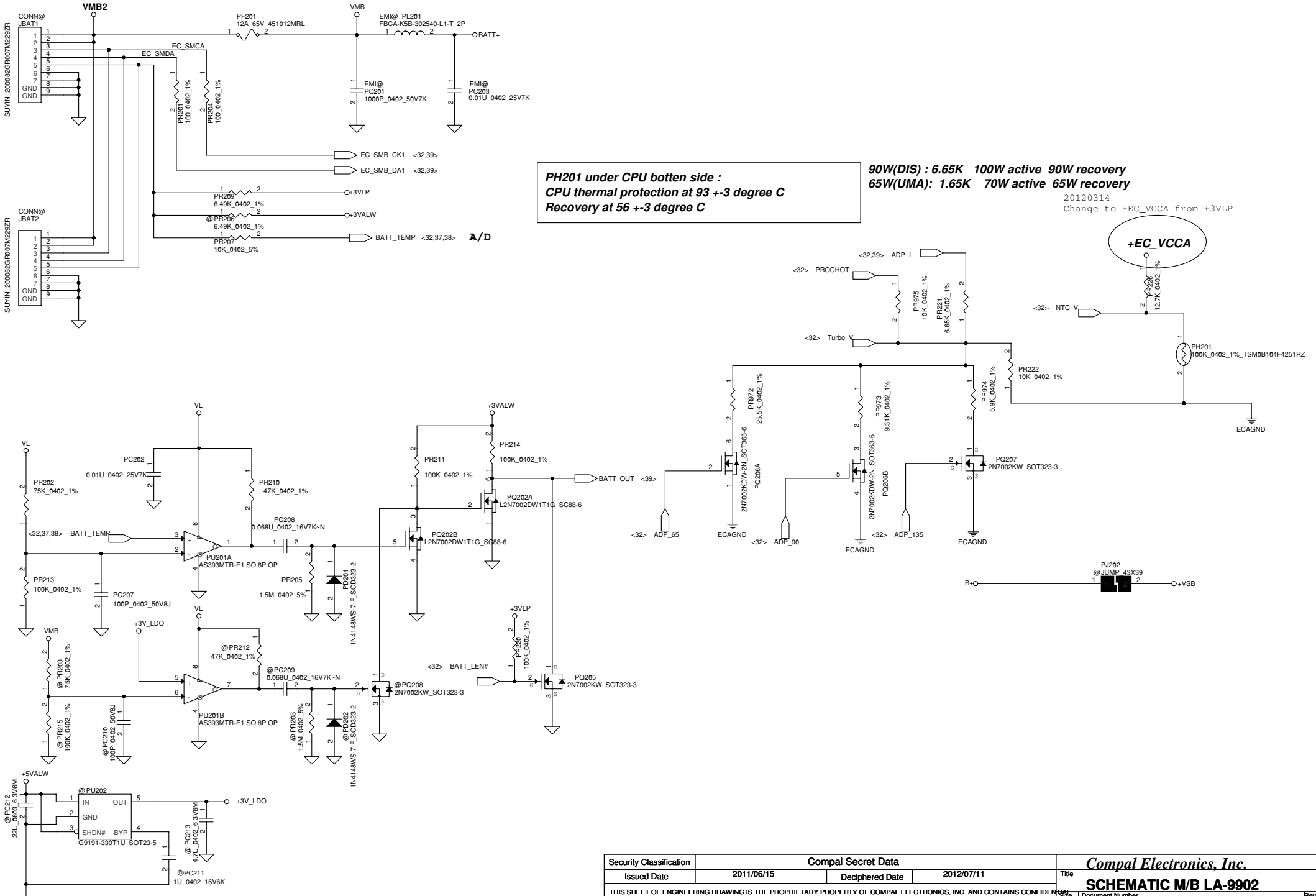
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 37 of 52



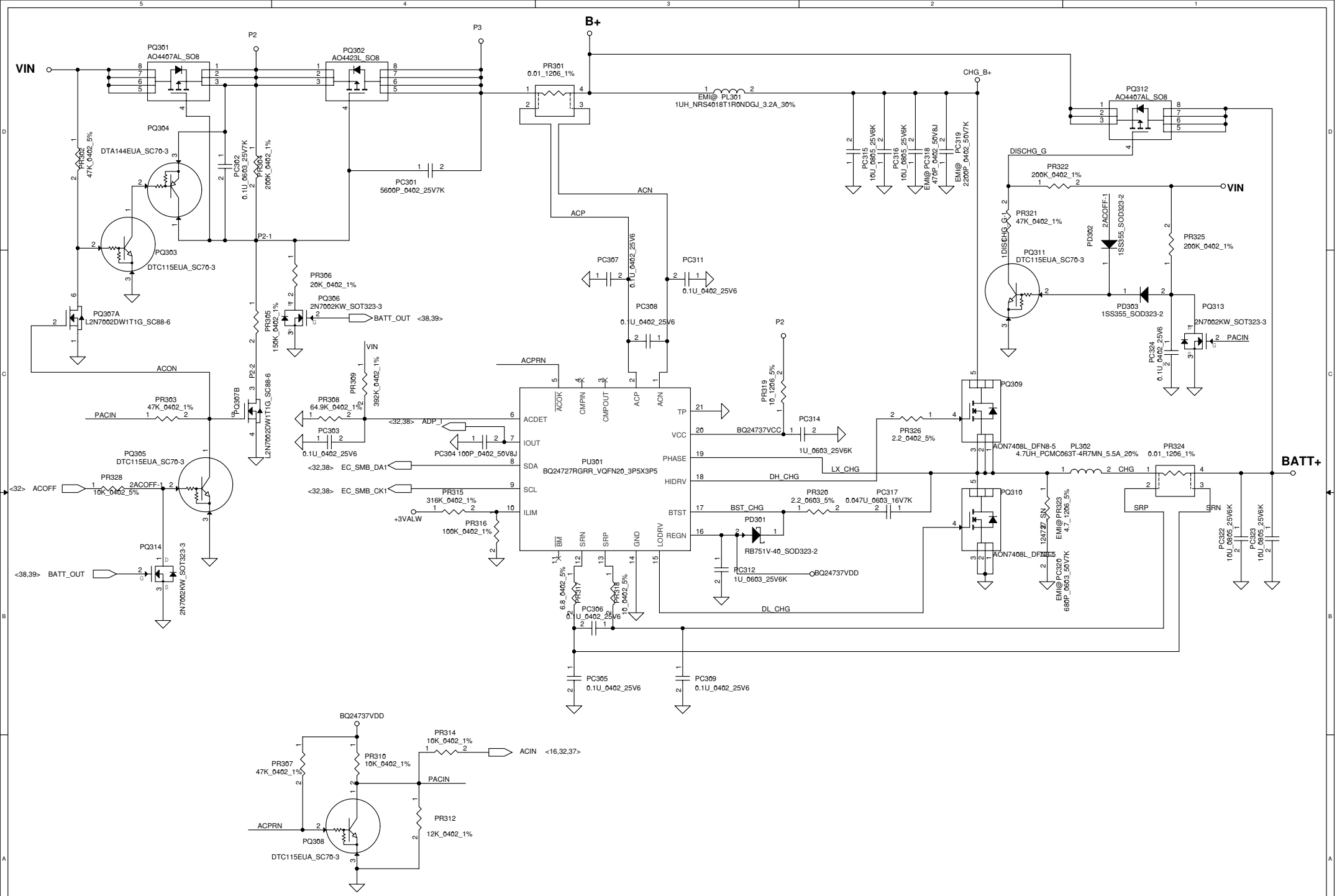
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 38 of 52



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

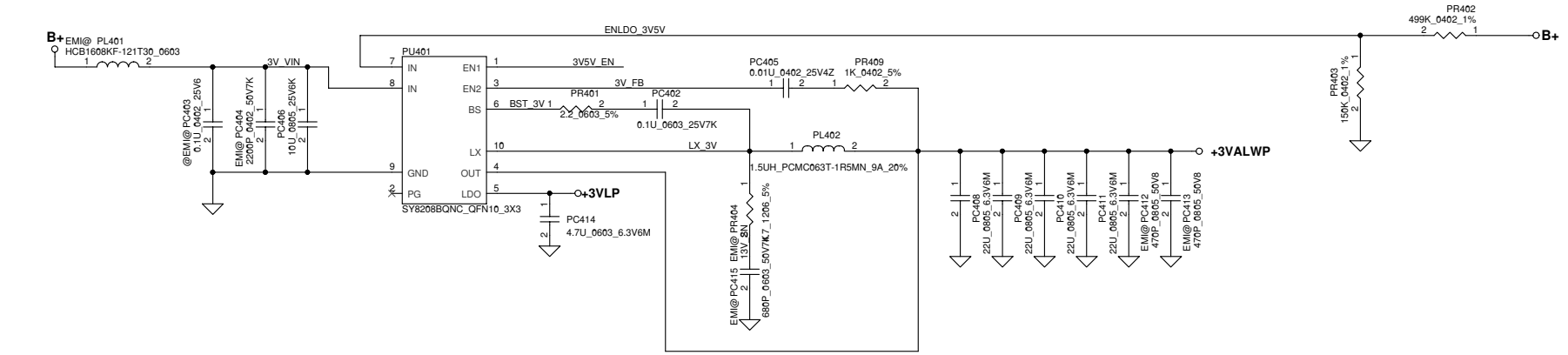
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

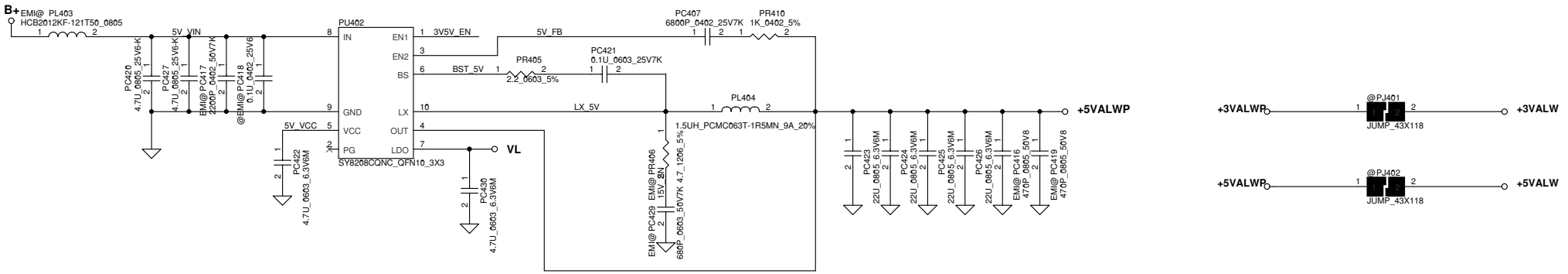
Compal Electronics, Inc.

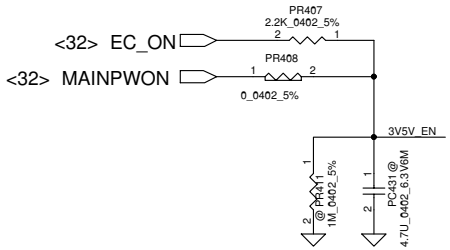
Title: **CHARGER**

Size | Document Number: **VILG1/G2 MB LA9902P Schematic** | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 39 of 52







Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

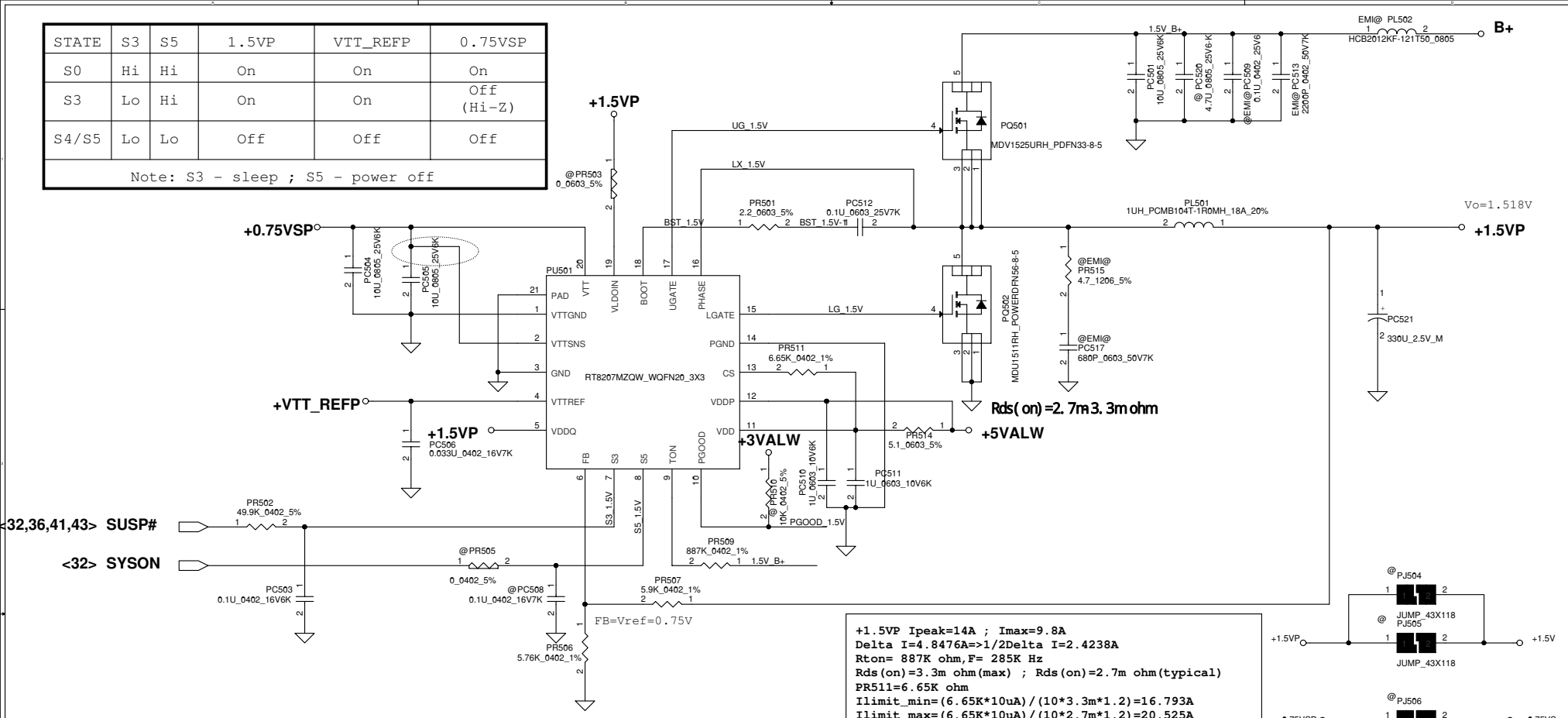
Compal Electronics, Inc.

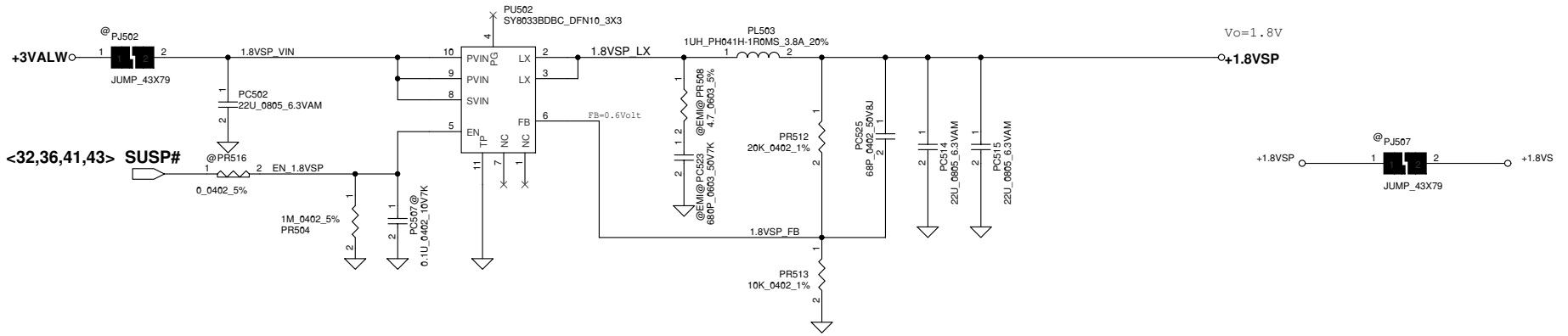
Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 40 of 52

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					





Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

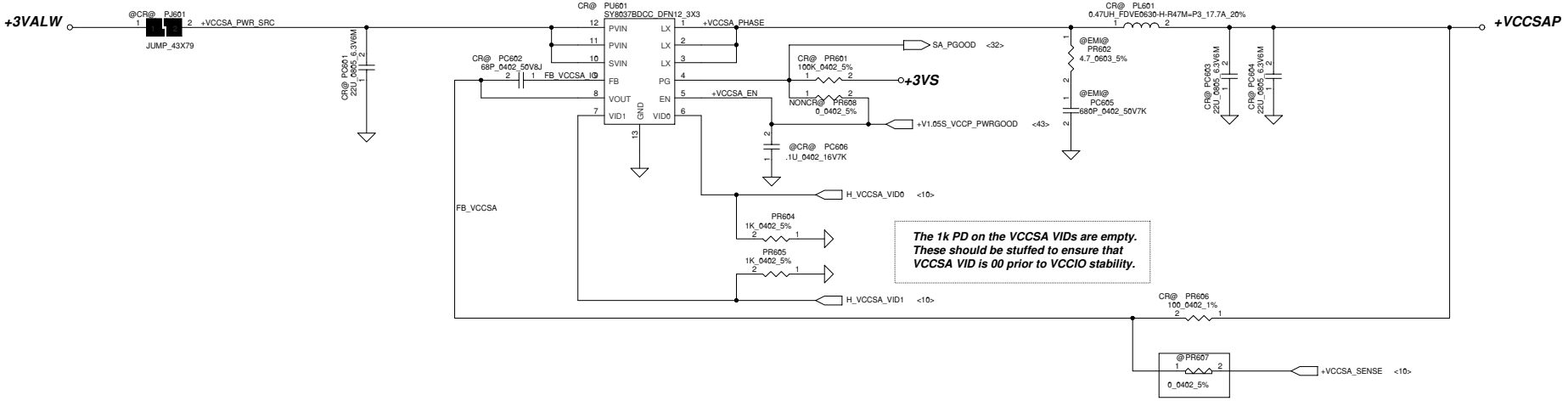
Title: **SCHEMATIC M/B LA-9902**

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 41 of 52

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



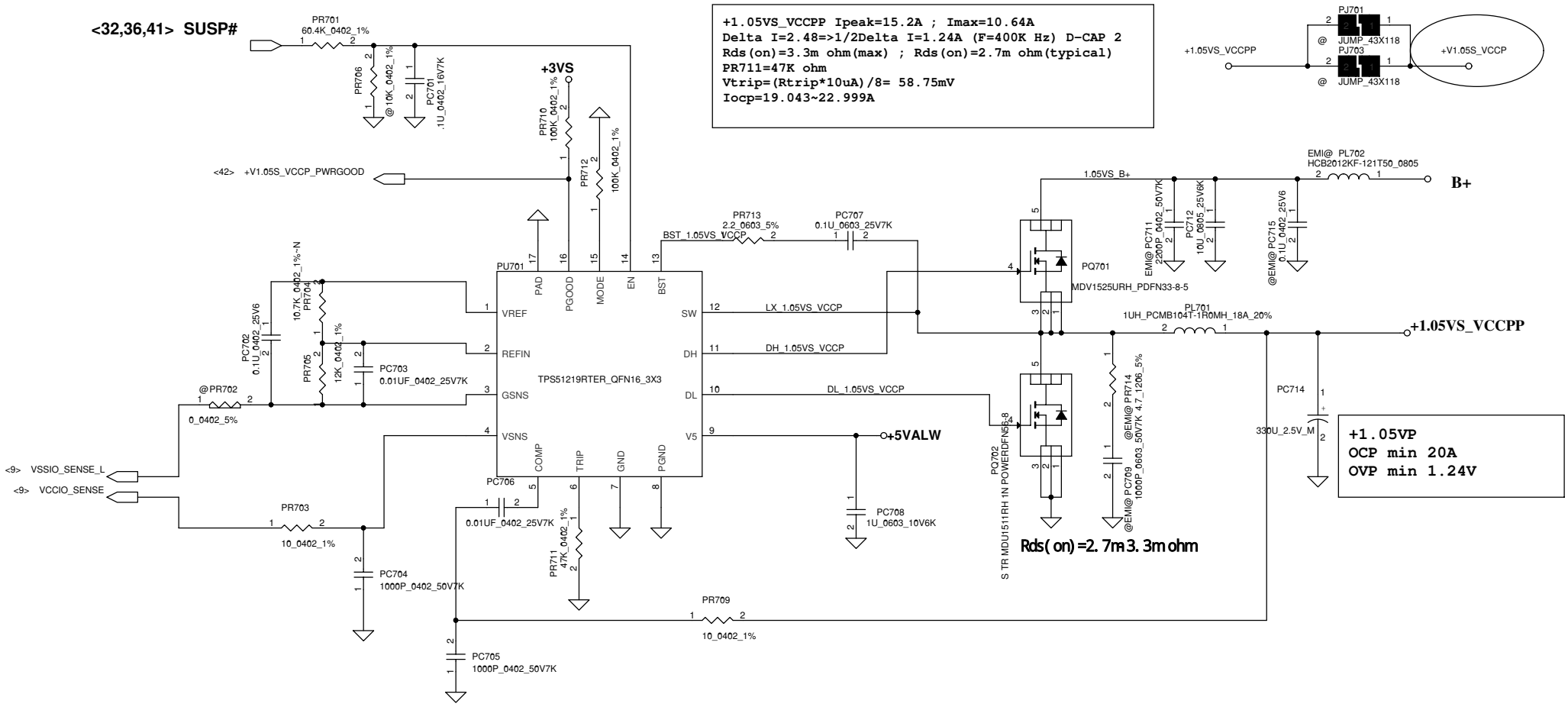
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
C	VILG1/G2 MB LA9902P Schematic	B

Date: Wednesday, May 08, 2013 Sheet 42 of 52



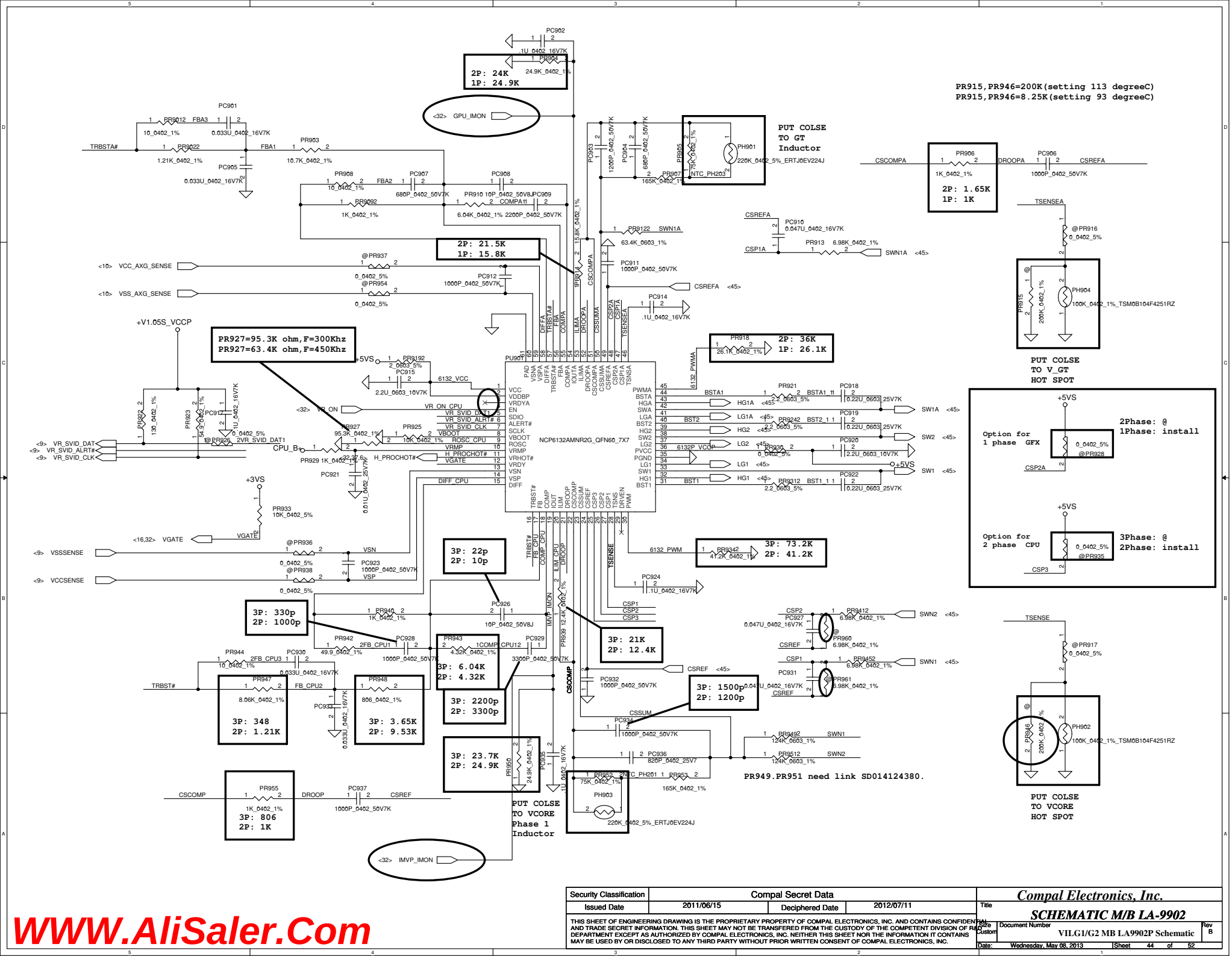
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 43 of 52

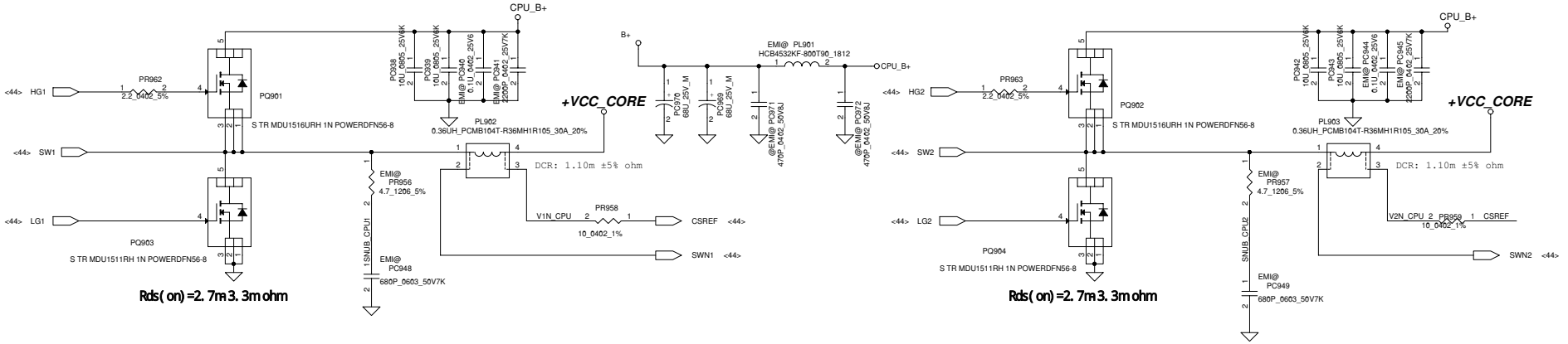


Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

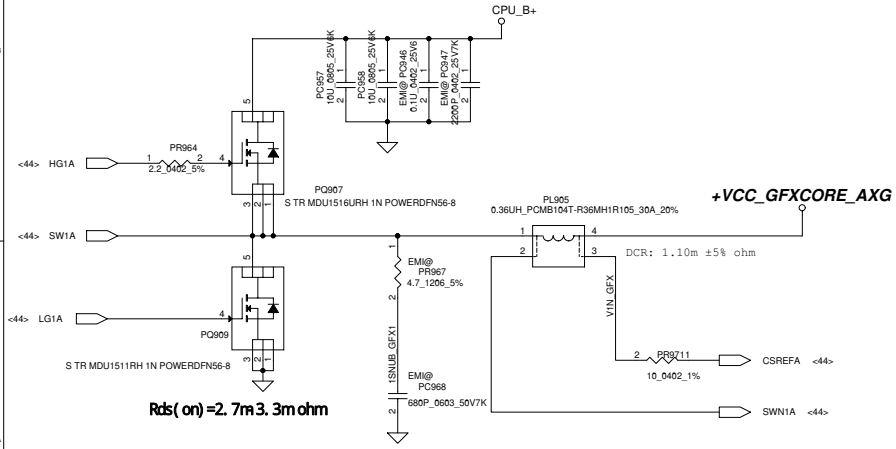
Title: SCHEMATIC M/B LA-9902

Size: Custom	Document Number: VILG1/G2 MB LA9902P Schematic	Rev: B
Date: Wednesday, May 08, 2013	Sheet 44 of 52	



QC 45W CPU
VID1=0.9V
IccMax=94A
Icc_Dyn=66A
Icc_TDC=52A
R_LL=1.9m ohm
OCP~110A

DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



QC 45W GT2
VID1=1.23V
IccMax=46A
Icc_Dyn=37A
Icc_TDC=38A
R_LL=3.9m ohm
OCP~55A

DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

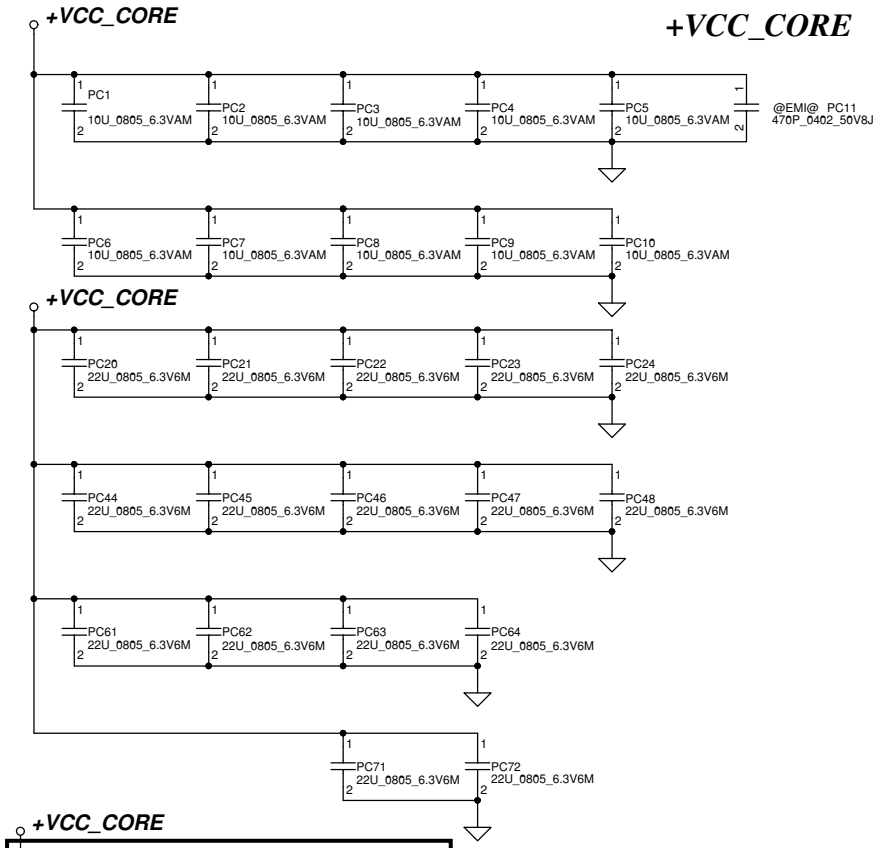
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

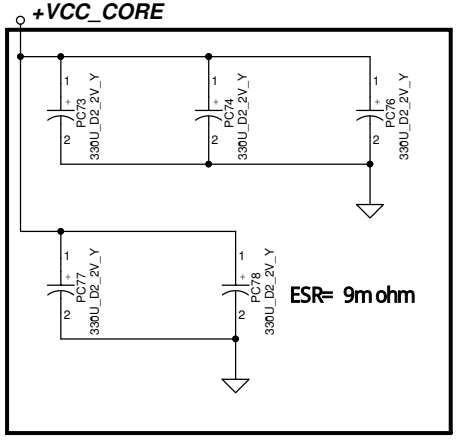
Compal Electronics, Inc.

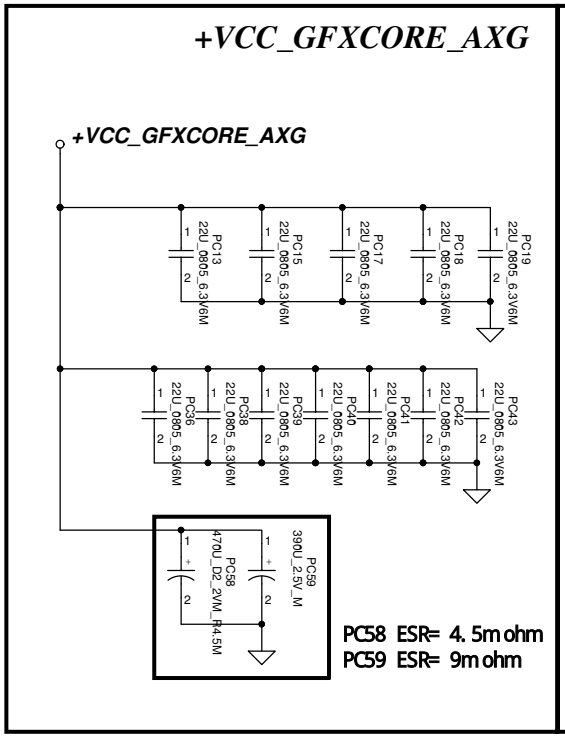
Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
C	VILG1/G2 MB LA9902P Schematic	B

Date: Wednesday, May 08, 2013 Sheet 45 of 52

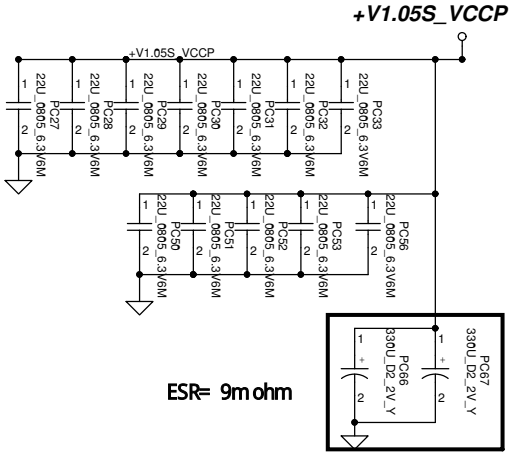






Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 46 of 52

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Design Change of IC Package.	40	Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM)	2012/11/22	DVT
2	Design Change of IC Package.	40	Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM)	2012/11/22	DVT
3	Add ADP_ID Circuit.	37	Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT) Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402)	2012/12/03	DVT
4	Factory lack of material.	41	Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL)	2012/12/06	DVT
5	Factory lack of material.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2012/12/06	DVT
6	EMI request adjust +3VALWP/+5VALWP snubber function.	40	Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429.	2012/12/06	DVT
7	EMI request adjust +3VALWP/+5VALWP boost resistor.	40	Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603).	2012/12/06	DVT
8	EMI request add bypass capacitor.	40	Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6)	2012/12/06	DVT
9	EMI request adjust CPU/GFX CORE snubber function.	45	Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968.	2012/12/06	DVT
10	EMI request adjust bypass capacitor.	45	Change @PC940 to PC940.	2012/12/06	DVT
11	EMI request add bypass capacitor.	45	Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402) Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402)	2012/12/06	DVT
12	Design Change of input capacitor.	40	Change PC420 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25) Add PC427 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25)	2012/12/07	DVT
13	Design Change of IC Application.	40	Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402) Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402) Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402) Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2012/12/10	DVT
14	Design Change of IC Application.	44	Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402) Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402) Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402) Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402) Change PR943 to SD00000J280(S RES 1/16W 4.32K +-1% 0402) Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO)	2012/12/17	DVT
15	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A)	2012/12/21	DVT
16	Design Change of VCCSA(LDO).	42	Delete PC607.PC608.PC609.PC610.PC611.PC612.PC613.PC614.PJ603.PJ604.PR608.PR609.PR610.PR611.PU602	2012/12/21	DVT
17	Reduction Part Count.	37	Delete PR110.	2013/01/18	PVT
18	Reduction Part Count.	42	Delete PR603.	2013/01/18	PVT
19	Reduction Part Count.	44	Delete PC916.	2013/01/18	PVT
20	Design Change of IC Application.	40	Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410. Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

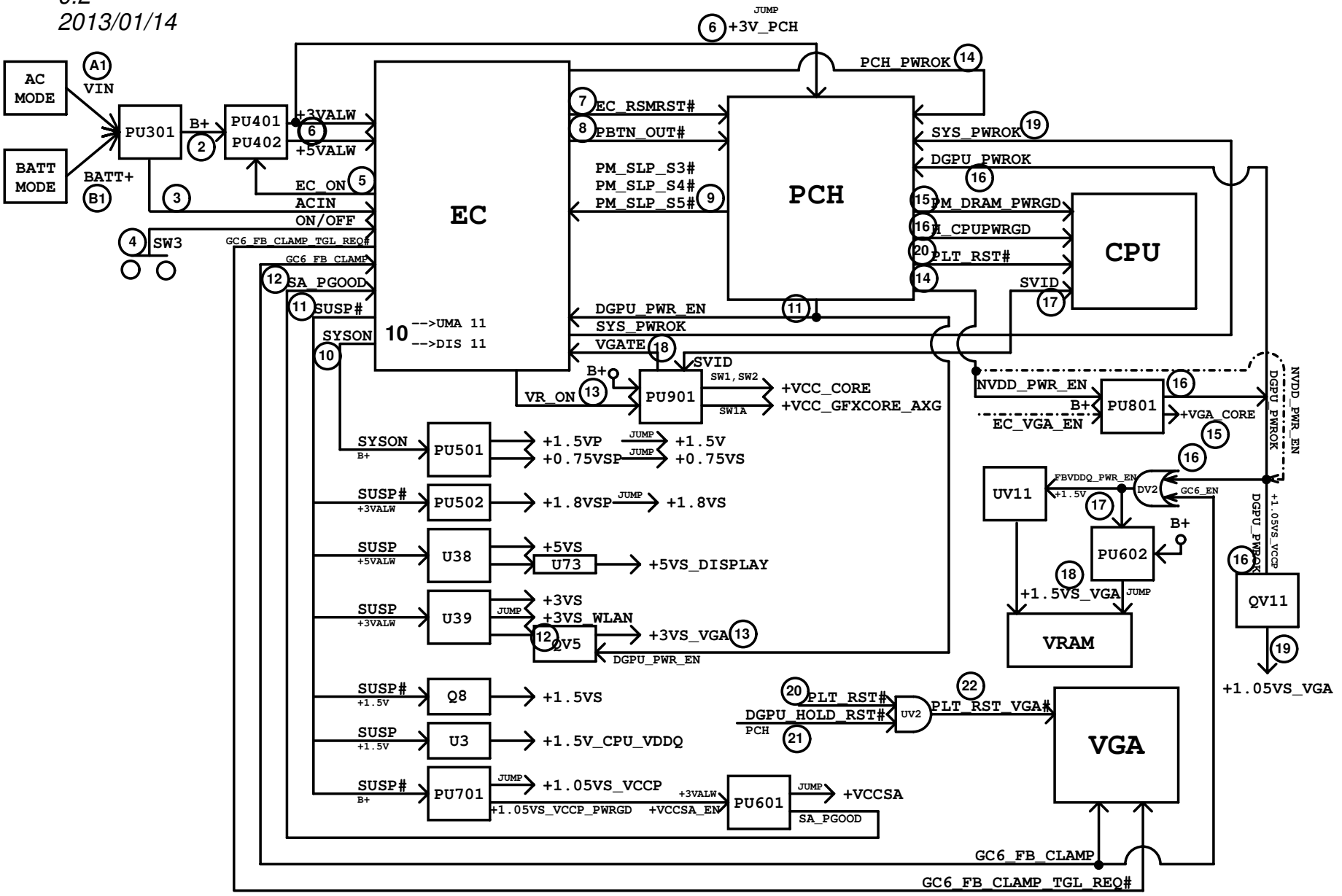
Size: Custom | Document Number: VILG1/G2 MB LA9902P Schematic | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 47 of 52

Item	Reason for change	PG#	Modify List	Date	Phase
21	Reduction Part Count.	41	Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402) Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603)	2013/01/18	PVT
22	Design Change of Thermal Application.	41	Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2013/01/18	PVT
23	Reduction Part Count.	43	Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
24	Reduction Part Count.	44	Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/01/18	PVT
25	Design Change of CPU/GFX CORE Choke.	45	Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE)	2013/01/18	PVT
26	Design Change of CPU/GFX CORE Frequence.	44	Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402)	2013/01/18	PVT
27	Factory lack of material.	40	Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25)	2013/01/18	PVT
28	Reduction Part Count.	40	Delete PR411.	2013/01/21	PVT
29	Design Change of Power Circuit Application.	38	Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402)	2013/01/23	PVT
30	Design Change of Power Circuit Application.	39	Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402) Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3)	2013/01/23	PVT
31	Design Change of Power Circuit Application.	40	Change PC405 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402) Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402)	2013/03/04	PVT
32	Design Change of Power Circuit Application.	42	Add PR608 to SD028000080(S RES 1/16W 0 +-5% 0402)	2013/03/14	Pre-MP

COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-9901P*
REVISION: *0.2*
DATE: *2013/01/14*



Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Title: *SCHEMATIC M/B LA-9902*
Size: Custom | Document Number: *4019N1* | Rev: B
Date: Wednesday, May 08, 2013 | Sheet 49 of 52

VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.5~11	Change footprint of JCPU1	For Lenovo rule
2	P.14	Add R406, R407, R408, R409	Reserve for improvement factory processes
3	P.42	Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC	Reserve for improvement factory processes
4	P.42	Add PCH_PWR_EN to EC Pin.107	Reserve for improvement factory processes
5	P.42	Reserve R410	Reserve Pull-high for GPIO use
6	P.42	Change EC_FAN_PWM from EC Pin.34 to EC Pin.26	For common design
7	P.42	Change NOVO# from EC Pin.26 to EC Pin.34	For common design
8	P.42	Change ENBKL from EC Pin.73 to EC Pin.76	For common design
9	P.42	Change IMVP_IMON from EC Pin.76 to EC Pin.73	For common design
10	P.42	Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123	For common design
11	P.34	Add R411, R412, C411, C412	Reserve for EMI
12	P.20	Add Q21, R40, C237, Q22, R418, C243, C252, R413	Reserve for power consumption
13	P.25	Del Q12/R806	For Change Audio Jack type from Normal close to Normal open

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: SCHEMATIC M/B LA-9902

Size	Document Number	Rev
Custom	4019N1	B

Date: Wednesday, May 08, 2013 Sheet 50 of 52

VILG1/G2 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			DVT TO PVT
1	P.26	Reserve R508	For leakage current issue of Atheros WLAN
2	P.31	Change RA22 to reserve	For PC Beep issue(can't heard sound of "di" on BIOS setup menu)
3	P.31	Reserve RA10/RA11	For solve Codec speaker Hum noise issue(Zizi)
4	P.32	Reserve R416	Reserve +3VLP power rail to EC
5	P.32	Change EC_RST# power rail to +3V_EC	Using power rail which the same with EC
6	P.32	Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC	Using power rail which the same with EC
7	P.14	Change U5 from 4MB to 8MB ROM	Follow common design
			PVT TO Pre-MP
1	P.32	Chagne R416 to shortpad	
2	P.42	Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PGOOD	For Celeron/Pentium CPU

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	SCHEMATIC M/B LA-9902		
Size: Custom	Document Number: 4019N1		Rev: B
Date: Wednesday, May 08, 2013	Sheet 51 of 52		

Item	Reason for change	PG#	Modify List	Date	Phase
44					
45					
46					
47					
48					
49					
50					
51					
52					
52					
53					

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: *SCHEMATIC M/B LA-9902*

Size: Custom | Document Number: 4019N1 | Rev: B

Date: Wednesday, May 08, 2013 | Sheet 52 of 52