# Compal Confidential

## G400S/G500S DIS M/B Schematics Document

### Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

### nVIDIA N14X

**LA-9901P**

**2013-03-20**

**REV:1.0**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: Cover Page | | |
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Compal confidential
File Name :LA-9901P

# Chief River

NVIDIA GB4-128 29 x 29 mm
N14M-GE/N14P-GV2/N14P-GS
VRAM 512MB/1GB/2GB
N14M-GE/N14P-GV2: DDR3 x 4
N14P-GS: DDR3 x 8
page 23~32

PEG 8x
Gen2 / Gen3

Intel
Processor
Ivy Bridge
rPGA989
37.5mm x 37.5mm
page 5~11

Memory Bus
Dual Channel
DDR3 1600MHz
DDR3 1333MHz
DDR3 1066MHz

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2 page 12,13

FDI *8
2.7GT/s

DMI2 *4
5GT/s

LVDS Conn. page 33

HDMI Conn. page 35

CRT Conn. page 34

RJ45 Conn. page 38

LAN
PCIe Port 1
Atheros
AR8162/QCA8172(10/100)
page 37

PCIe x1

PCIe Mini Card
WiMax
USB20 Port 10
page 36

PCIe x1

PCIe Mini Card
WLAN
PCIe Port 2
page 36

USB20 x1

Intel
PCH
Panther Point
FCBGA 989Balls
25mm x 25mm
page 14~22

USB30 x2

USB20 x6

Left USB3.0 x2
USB30 Port 0,1
page 45

Right USB2.0
USB20 Port 9
page 43

Int. Camera
USB20 Port 3
page 33

Touch Screen
USB20 Port 2
page 45

Card Reader
Realtek RTS5170
USB20 Port 11 page 43

SATA Gen3

HDD Conn.
SATA Port 0
page 40

SATA

ODD Conn.
SATA Port 2
page 40

AZALIA

Audio Codec
CONEXANT
CX20757
page 41

Int. MIC Conn.
page 41

Int. Speaker Conn.
page 41

Audio Combo Jacks
HP & MIC
page 43

SPI ROM
2MB + 4MB
page 14

EC
ENE KB9012
page 42

Thermal Sensor
page 39

Touch Pad
page 43

Int. KBD
page 43

Sub-borad

15"

14"

Power/B
LS9902P
page 43

LED/B
LS9903P
page 43

IO/B
LS9901P
page 43

ODD/B
LS9904P
page 40

| | | | |
|---|---|---|---|
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Title: MB Block Diagram

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## Voltage Rails

| State \ power plane | +B | +5VALW<br>+3VALW | +1.5V | +5VS<br>+3VS<br>+1.5VS<br>+V1.05S_VCCP<br>+VCC_CORE<br>+VGA_CORE<br>+VCC_GFXCORE_AXG<br>+1.8VS<br>+0.75VS<br>+1.05VS |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC | O | O | X | X |
| S5 S4/ Battery only | O | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| 0 | 1.0 |
| 1 | 0.3 |
| 2 | 0.2 |
| 3 | 0.1 |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## Board ID table for AD channel

| Vcc | 3.3V | | | | | |
|---|---|---|---|---|---|---|
| Ra | 100K +/- 1% | | | | | |
| Board ID | Rb | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max | EC AD | |
| 0 | 0 | 0 V | 0 V | 0.300 V | 0x00 – 0x0B | MP |
| 1 | 12K +/- 1% | 0.347 V | 0.354 V | 0.360 V | 0x0C – 0x1C | PVT |
| 2 | 15K +/- 1% | 0.423 V | 0.430 V | 0.438 V | 0x1D – 0x26 | DVT |
| 3 | 20K +/- 1% | 0.541 V | 0.550 V | 0.559 V | 0x27 – 0x30 | EVT |

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 011X b |

## EC SM Bus2 address

| Device | Address |
|---|---|
| Thermal Sensor | 1001 100xb |

## PCH SM Bus address

| Device | Address |
|---|---|
| DDR DIMM0 | 1010 000Xb |
| DDR DIMM2 | 1010 010Xb |

## NV-GPU SM Bus address

| Device | Address |
|---|---|
| Internal thermal sensor | 1001 111Xb (0x9E) |

## USB Port Table

| | USB 2.0 | Port | 3 External USB Port |
|---|---|---|---|
| EHCI1 USB3.0 | UHCI0 | 0 | USB Port (Left Side) USB3.0 |
| | | 1 | USB Port (Left Side) USB3.0 |
| | UHCI1 | 2 | Touch Screen |
| | | 3 | USB Camera |
| | UHCI2 | 4 | |
| | | 5 | |
| | UHCI3 | 6 | |
| | | 7 | |
| EHCI2 | UHCI4 | 8 | |
| | | 9 | USB/B (Right Side USB2.0) |
| | UHCI5 | 10 | Mini Card(WLAN) |
| | | 11 | Card Reader |
| | UHCI6 | 12 | |
| | | 13 | |

## BOM Structure Table

| BTO Item | BOM Structure |
|---|---|
| 45 LEVEL | 45@ |
| Connector | ME@ |
| For VILG2 (14") | 14@ |
| For VILG1 (15") | 15@ |
| GPU:N14M-GE | N14@ |
| HDMI | HDMI@ |
| Camera | CMOS@ |
| LAN LDO Mode | LDO@ |
| LAN Switch mode | SWR@ |
| 10/100 LAN(AR8162L) | 8162@ |
| 10/100 LAN(QCA8172) | 8172@ |
| N14M-GE SKU | GE@ |
| N14P-GS SKU | GS@ |
| N14P-GV2 SKU | GV2@ |
| N14P-GV2&N14P-GS SKU | GVGS@ |
| Green clock(DIS sku) | GCLK304@ |
| Green clock(UMA sku) | GCLK244@ |
| Green clk support | GCLK@ |
| No Green clk support | NOGCLK@ |
| Nvidia GC6 state | GC6@ |
| Touch Screen SKU | TS@ |
| Optimus SKU | OPT@ |
| UMA SKU | UMA@ |
| PCH(NM70 sku) | NM70@ |
| PCH(HM70 sku) | HM70@ |
| PCH(HM76 sku) | HM76@ |
| VRAM(1000MHz) | 1000M@ |
| VRAM(900MHz) | 900M@ |
| Unpop | @ |

## SMBUS Control Table

| | SOURCE | VGA | BATT | KB9012 | SODIMM | WLAN | Thermal Sensor | PCH |
|---|---|---|---|---|---|---|---|---|
| SMB_EC_CK1<br>SMB_EC_DA1 | KB9012<br>+3VALW | X | V<br>+3VALW | X | X | X | X | X |
| SMB_EC_CK2<br>SMB_EC_DA2 | KB9012<br>+3VALW | V<br>+3VS_VGA | X | X | X | X | X | V<br>+3VS |
| SMBCLK<br>SMBDATA | PCH<br>+3VALW | X | X | X | V<br>+3VS | V<br>+3VS | X | X |
| SML0CLK<br>SML0DATA | PCH<br>+3VALW | X | X | X | X | X | X | X |
| SML1CLK<br>SML1DATA | PCH<br>+3VALW | V<br>+3VS_VGA | X | V<br>+3VS | X | X | V<br>+3VS | X |

| | | | |
|---|---|---|---|
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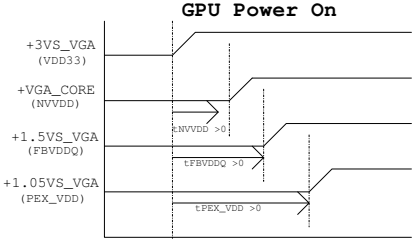
## N14x GPIO Pin Definition Table

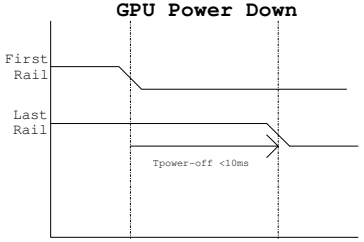
| Pin Name | Normal Function | I/O | Functional Description | Default PU/PD |
|---|---|---|---|---|
| GPIO0 | FB_CLAMP_MON | I | FB Clamp monitor | |
| GPIO1 | MEM_VDD_CTL | O | Memory VDD VID | MEM VID:Strap to boot FBVDD/Q |
| GPIO2~4 | Non-support for LCD | O | Panel | 100k PD |
| GPIO5 | Reserve | | | |
| GPIO6 | FB_CLAMP_TGL_REQ# | O | Active low FB Clamp toggle request | |
| GPIO7 | 3DVision | O | 3D Vision L/R signal | 100k PD |
| GPIO8 | OVERT | IO | Active Low Thermal Catastrophic Over Temperature | 100k PU |
| GPIO9 | ALERT | IO | Active Low Thermal Alert | 100k PU |
| GPIO10 | MEM_VREF_CTL | O | Memory VREF Control | 100k PD |
| GPIO11 | PWM_VID | O | GPU Core VDD PWM control supply overdraw input | |
| GPIO12 | PWR_LEVEL | I | AC power detact or control signal | 100k PU |
| GPIO13 | PSI | O | Phase Shedding | PSI:100k PU to enable two phase |
| GPIO14~19 | Non-support for HDA | I | Hot Plug | |
| GPIO20~21 | Reserve | | | |

### GPU Power On



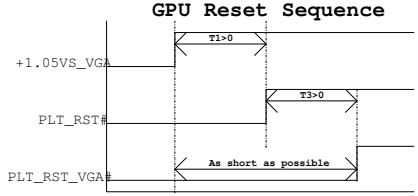

1. all power rail ramp up time should be larger than 40us
2. The total time for all rails to ramp should be within 6ms.
3. A power rail has to ramp up 90% before the next power rail in sequence can start ramping up.
4. No signal should be applied to the GPU before the power rail are fully ramped.

### GPU Power Down

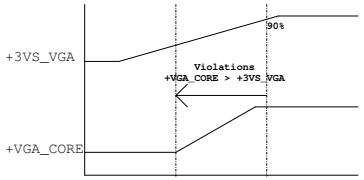



1.All GPU power rails should be turned off within 10ms

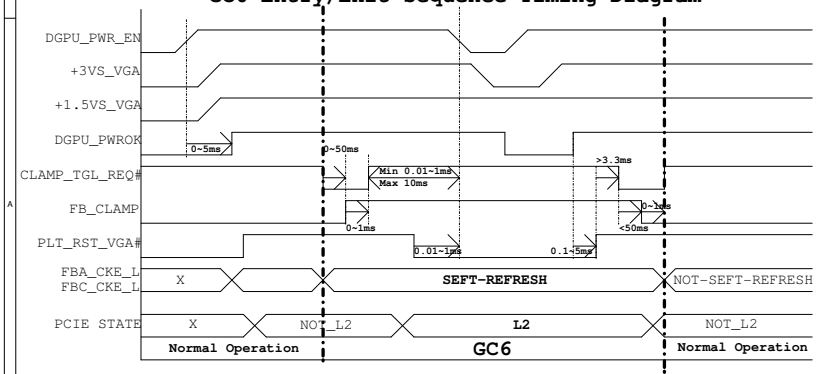
### GPU Reset Sequence




### Power sequencing violations




### GC6 Entry/Exit Sequence Timing Diagram




### For N14P-GV2 strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N14P-GV2 | 1 GHz | 128M* 16* 4 1GB | Samsung K4W2G1646E-BC1A | R PU 45K | R PD 45K | R PD 15K | R PD 5K | R PD 45K | R PD 45K | R PU 5K | R PU 5K |
| N14P-GV2 | 1 GHz | 128M* 16* 4 1GB | Micron MT41J128M16JT-093G:K | R PU 45K | R PD 45K | R PD 15K | R PD 5K | R PD 45K | R PD 30K | R PU 5K | R PU 5K |
| N14P-GV2 | 1 GHz | 128M* 16* 4 1GB | **Hynix H5TC2G63FFR-11C** | R PU 45K | R PD 45K | R PD 15K | R PD 5K | R PD 45K | **R PD 25K** | R PU 5K | R PU 5K |
| N14P-GV2 | 900 MHz | 256M* 16* 4 2GB | Samsung K4W4G1646B-HC11 | R PU 45K | R PD 45K | R PD 15K | R PD 5K | R PD 45K | R PD 20K | R PU 5K | R PU 5K |
| N14P-GV2 | 900 MHz | 256M* 16* 4 2GB | Micron MT41K256M16HA-107G:E | R PU 45K | R PD 45K | R PD 15K | R PD 5K | R PD 45K | R PD 10K | R PU 5K | R PU 5K |

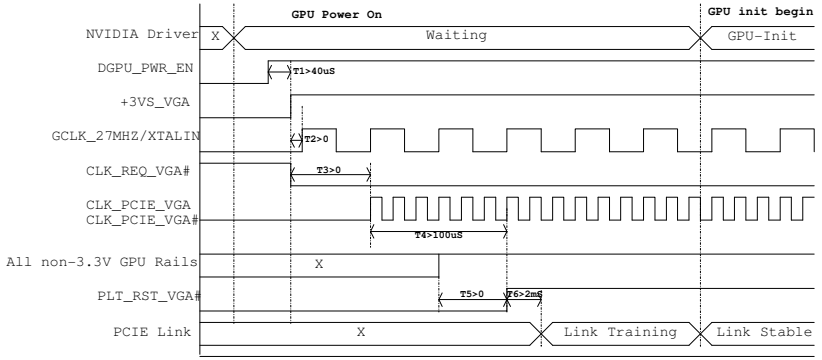
### For N14P-GS strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N14P-GS | 1 GHz | 128M* 16* 8 2GB | Samsung K4W2G1646E-BC1A | R PU 45K | R PD 5K | R PD 20K | R PD 5K | R PD 45K | R PD 45K | R PU 5K | R PD 15K |
| N14P-GS | 1 GHz | 128M* 16* 8 2GB | Micron MT41J128M16JT-093G:K | R PU 45K | R PD 5K | R PD 20K | R PD 5K | R PD 45K | R PD 30K | R PU 5K | R PD 15K |
| N14P-GS | 1 GHz | 128M* 16* 8 2GB | **Hynix H5TC2G63FFR-11C** | R PU 45K | R PD 5K | R PD 20K | R PD 5K | R PD 45K | **R PD 25K** | R PU 5K | R PD 15K |
| N14P-GS | 900 MHz | 256M* 16* 8 4GB | Samsung K4W4G1646B-HC11 | R PU 45K | R PD 5K | R PD 20K | R PD 5K | R PD 45K | R PD 20K | R PU 5K | R PD 15K |
| N14P-GS | 900 MHz | 256M* 16* 8 4GB | Micron MT41K256M16HA-107G:E | R PU 45K | R PD 5K | R PD 20K | R PD 5K | R PD 45K | R PD 10K | R PU 5K | R PD 15K |

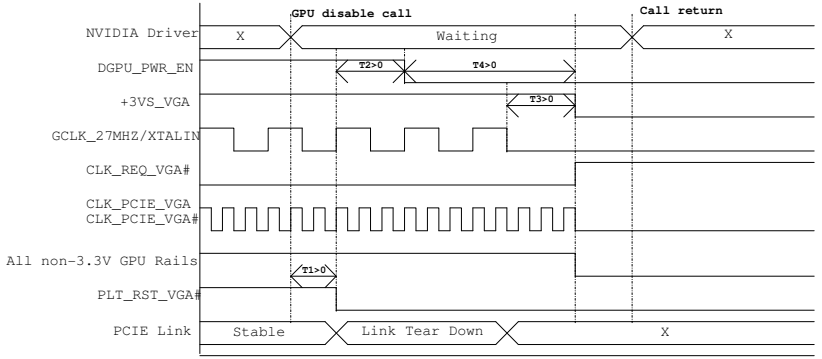
### For N14M-GE strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N14M-GE | 1 GHz | 128M* 16* 4 1GB | Samsung K4W2G1646E-BC1A | R PU 10K | R PD 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 1 GHz | 128M* 16* 4 1GB | Micron MT41J128M16JT-093G:K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 1 GHz | 128M* 16* 4 1GB | **Hynix H5TC2G63FFR-11C** | R PD 10K | R PD 10K | R PU 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 900 MHz | 256M* 16* 4 2GB | Samsung K4W4G1646B-HC11 | R PU 10K | R PU 10K | R PD 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 900 MHz | 256M* 16* 4 2GB | Micron MT41K256M16HA-107G:E | R PU 10K | R PD 10K | R PU 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |

### Optimus Typical Power-Up Sequence




### Optimus Typical Power-Down Sequence

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|---|---|---|---|
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Title: VGA Notes List

| Size | Document Number | Rev |
|---|---|---|
| Custom | VILG1/G2 MB LA-9901P Schematic | 0.3 |

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ZZZ1 PCB DAG1@

ZZZ2 PCB DAG2@

**PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms**
**PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms**

+V1.05S_VCCP

R1 24.9_0402_1%

JCPU1A

PEG_ICOMPI J22
PEG_ICOMPO J21
PEG_RCOMPO H22

PEG_COMP

**PEG Static Lane Reversal - CFG2 is for the 16x**

| | |
|---|---|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition |
| | * 0:Lane Reversed |

PCIE_CRX_GTX_N[0..15] <23>

PCIE_CRX_GTX_P[0..15] <23>

PCIE_CTX_GRX_N[0..15] <23>

PCIE_CTX_GRX_P[0..15] <23>

**DMI**

| | | | |
|---|---|---|---|
| <16> DMI_CRX_PTX_N0 | B27 | DMI_RX#[0] | PEG_RX#[0] K33 PCIE_CRX_GTX_N15 |
| <16> DMI_CRX_PTX_N1 | B25 | DMI_RX#[1] | PEG_RX#[1] M35 PCIE_CRX_GTX_N14 |
| <16> DMI_CRX_PTX_N2 | A25 | DMI_RX#[2] | PEG_RX#[2] L34 PCIE_CRX_GTX_N13 |
| <16> DMI_CRX_PTX_N3 | B24 | DMI_RX#[3] | PEG_RX#[3] J35 PCIE_CRX_GTX_N12 |
| <16> DMI_CRX_PTX_P0 | B28 | DMI_RX[0] | PEG_RX#[4] J32 PCIE_CRX_GTX_N11 |
| <16> DMI_CRX_PTX_P1 | B26 | DMI_RX[1] | PEG_RX#[5] H34 PCIE_CRX_GTX_N10 |
| <16> DMI_CRX_PTX_P2 | A24 | DMI_RX[2] | PEG_RX#[6] H31 PCIE_CRX_GTX_N9 |
| <16> DMI_CRX_PTX_P3 | B23 | DMI_RX[3] | PEG_RX#[7] G33 PCIE_CRX_GTX_N8 |
| <16> DMI_CTX_PRX_N0 | G21 | DMI_TX#[0] | PEG_RX#[8] G30 PCIE_CRX_GTX_N7 |
| <16> DMI_CTX_PRX_N1 | E22 | DMI_TX#[1] | PEG_RX#[9] F35 PCIE_CRX_GTX_N6 |
| <16> DMI_CTX_PRX_N2 | F21 | DMI_TX#[2] | PEG_RX#[10] E34 PCIE_CRX_GTX_N5 |
| <16> DMI_CTX_PRX_N3 | D21 | DMI_TX#[3] | PEG_RX#[11] E32 PCIE_CRX_GTX_N4 |
| <16> DMI_CTX_PRX_P0 | G22 | DMI_TX[0] | PEG_RX#[12] D33 PCIE_CRX_GTX_N3 |
| <16> DMI_CTX_PRX_P1 | D22 | DMI_TX[1] | PEG_RX#[13] D31 PCIE_CRX_GTX_N2 |
| <16> DMI_CTX_PRX_P2 | F20 | DMI_TX[2] | PEG_RX#[14] B33 PCIE_CRX_GTX_N1 |
| <16> DMI_CTX_PRX_P3 | C21 | DMI_TX[3] | PEG_RX#[15] C32 PCIE_CRX_GTX_N0 |

**Intel(R) FDI**

| | | | |
|---|---|---|---|
| <16> FDI_CTX_PRX_N0 | A21 | FDI0_TX#[0] | PEG_RX[0] J33 PCIE_CRX_GTX_P15 |
| <16> FDI_CTX_PRX_N1 | H19 | FDI0_TX#[1] | PEG_RX[1] L35 PCIE_CRX_GTX_P14 |
| <16> FDI_CTX_PRX_N2 | E19 | FDI0_TX#[2] | PEG_RX[2] K34 PCIE_CRX_GTX_P13 |
| <16> FDI_CTX_PRX_N3 | F18 | FDI0_TX#[3] | PEG_RX[3] H35 PCIE_CRX_GTX_P12 |
| <16> FDI_CTX_PRX_N4 | B21 | FDI1_TX#[0] | PEG_RX[4] H32 PCIE_CRX_GTX_P11 |
| <16> FDI_CTX_PRX_N5 | C20 | FDI1_TX#[1] | PEG_RX[5] G34 PCIE_CRX_GTX_P10 |
| <16> FDI_CTX_PRX_N6 | D18 | FDI1_TX#[2] | PEG_RX[6] G31 PCIE_CRX_GTX_P9 |
| <16> FDI_CTX_PRX_N7 | E17 | FDI1_TX#[3] | PEG_RX[7] F33 PCIE_CRX_GTX_P8 |
| <16> FDI_CTX_PRX_P0 | A22 | FDI0_TX[0] | PEG_RX[8] F30 PCIE_CRX_GTX_P7 |
| <16> FDI_CTX_PRX_P1 | G19 | FDI0_TX[1] | PEG_RX[9] E35 PCIE_CRX_GTX_P6 |
| <16> FDI_CTX_PRX_P2 | E20 | FDI0_TX[2] | PEG_RX[10] E33 PCIE_CRX_GTX_P5 |
| <16> FDI_CTX_PRX_P3 | G18 | FDI0_TX[3] | PEG_RX[11] F32 PCIE_CRX_GTX_P4 |
| <16> FDI_CTX_PRX_P4 | B20 | FDI1_TX[0] | PEG_RX[12] D34 PCIE_CRX_GTX_P3 |
| <16> FDI_CTX_PRX_P5 | C19 | FDI1_TX[1] | PEG_RX[13] E31 PCIE_CRX_GTX_P2 |
| <16> FDI_CTX_PRX_P6 | D19 | FDI1_TX[2] | PEG_RX[14] C33 PCIE_CRX_GTX_P1 |
| <16> FDI_CTX_PRX_P7 | F17 | FDI1_TX[3] | PEG_RX[15] B32 PCIE_CRX_GTX_P0 |
| <16> FDI_FSYNC0 | J18 | FDI0_FSYNC | PEG_TX#[0] M29 PCIE_CTX_GRX_C_N15 C1 GS@ |
| <16> FDI_FSYNC1 | J17 | FDI1_FSYNC | PEG_TX#[1] M32 PCIE_CTX_GRX_C_N14 C2 GS@ |
| <16> FDI_INT | H20 | FDI_INT | PEG_TX#[2] M31 PCIE_CTX_GRX_C_N13 C3 GS@ |
| <16> FDI_LSYNC0 | J19 | FDI0_LSYNC | PEG_TX#[3] L32 PCIE_CTX_GRX_C_N12 C5 GS@ |
| <16> FDI_LSYNC1 | H17 | FDI1_LSYNC | PEG_TX#[4] L29 PCIE_CTX_GRX_C_N11 C7 GS@ |
| | | | PEG_TX#[5] K31 PCIE_CTX_GRX_C_N10 C8 GS@ |
| | | | PEG_TX#[6] K28 PCIE_CTX_GRX_C_N9 C9 GS@ |
| | | | PEG_TX#[7] J30 PCIE_CTX_GRX_C_N8 C10 GS@ |
| | | | PEG_TX#[8] J28 PCIE_CTX_GRX_C_N7 C11 GVGS@ |
| | | | PEG_TX#[9] H29 PCIE_CTX_GRX_C_N6 C12 GVGS@ |
| | | | PEG_TX#[10] G27 PCIE_CTX_GRX_C_N5 C13 GVGS@ |
| | | | PEG_TX#[11] E29 PCIE_CTX_GRX_C_N4 C14 GVGS@ |
| | | | PEG_TX#[12] F27 PCIE_CTX_GRX_C_N3 C15 GVGS@ |
| | | | PEG_TX#[13] D28 PCIE_CTX_GRX_C_N2 C16 GVGS@ |
| | | | PEG_TX#[14] F26 PCIE_CTX_GRX_C_N1 C17 GVGS@ |
| | | | PEG_TX#[15] E25 PCIE_CTX_GRX_C_N0 C18 GVGS@ |
| | | | PEG_TX[0] M28 PCIE_CTX_GRX_C_P15 C19 GS@ |
| | | | PEG_TX[1] M33 PCIE_CTX_GRX_C_P14 C20 GS@ |
| | | | PEG_TX[2] M30 PCIE_CTX_GRX_C_P13 C21 GS@ |
| | | | PEG_TX[3] L31 PCIE_CTX_GRX_C_P12 C22 GS@ |
| | | | PEG_TX[4] L28 PCIE_CTX_GRX_C_P11 C23 GS@ |
| | | | PEG_TX[5] K30 PCIE_CTX_GRX_C_P10 C24 GS@ |
| | | | PEG_TX[6] K27 PCIE_CTX_GRX_C_P9 C25 GS@ |
| | | | PEG_TX[7] J29 PCIE_CTX_GRX_C_P8 C26 GS@ |
| | | | PEG_TX[8] J27 PCIE_CTX_GRX_C_P7 C27 GVGS@ |
| | | | PEG_TX[9] H28 PCIE_CTX_GRX_C_P6 C28 GVGS@ |
| | | | PEG_TX[10] G28 PCIE_CTX_GRX_C_P5 C29 GVGS@ |
| | | | PEG_TX[11] E28 PCIE_CTX_GRX_C_P4 C30 GVGS@ |
| | | | PEG_TX[12] F28 PCIE_CTX_GRX_C_P3 C31 GVGS@ |
| | | | PEG_TX[13] D27 PCIE_CTX_GRX_C_P2 C32 GVGS@ |
| | | | PEG_TX[14] E26 PCIE_CTX_GRX_C_P1 C36 GVGS@ |
| | | | PEG_TX[15] D25 PCIE_CTX_GRX_C_P0 C37 GVGS@ |

+V1.05S_VCCP

R7 24.9_0402_1%

**eDP**

| | | |
|---|---|---|
| EDP_COMP | A18 | eDP_COMPIO |
| | A17 | eDP_ICOMPO |
| eDP_HPD | B16 | eDP_HPD# |
| | C15 | eDP_AUX |
| | D15 | eDP_AUX# |
| | C17 | eDP_TX[0] |
| | F16 | eDP_TX[1] |
| | C16 | eDP_TX[2] |
| | G15 | eDP_TX[3] |
| | C18 | eDP_TX#[0] |
| | E16 | eDP_TX#[1] |
| | D16 | eDP_TX#[2] |
| | F15 | eDP_TX#[3] |

**eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms**

TYCO_2013620-2_IVY BRIDGE ME@

0.22U_0402_10V6K PCIE_CTX_GRX_N[0..15] <23>

0.22U_0402_10V6K PCIE_CTX_GRX_P[0..15] <23>

C11 C12 C13 C14 C15 C16 C17 C18

0.1U_0402_10V7K SE102104K00 GE@

C27 C28 C29 C30 C31 C32 C36 C37

0.1U_0402_10V7K SE102104K00 GE@

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

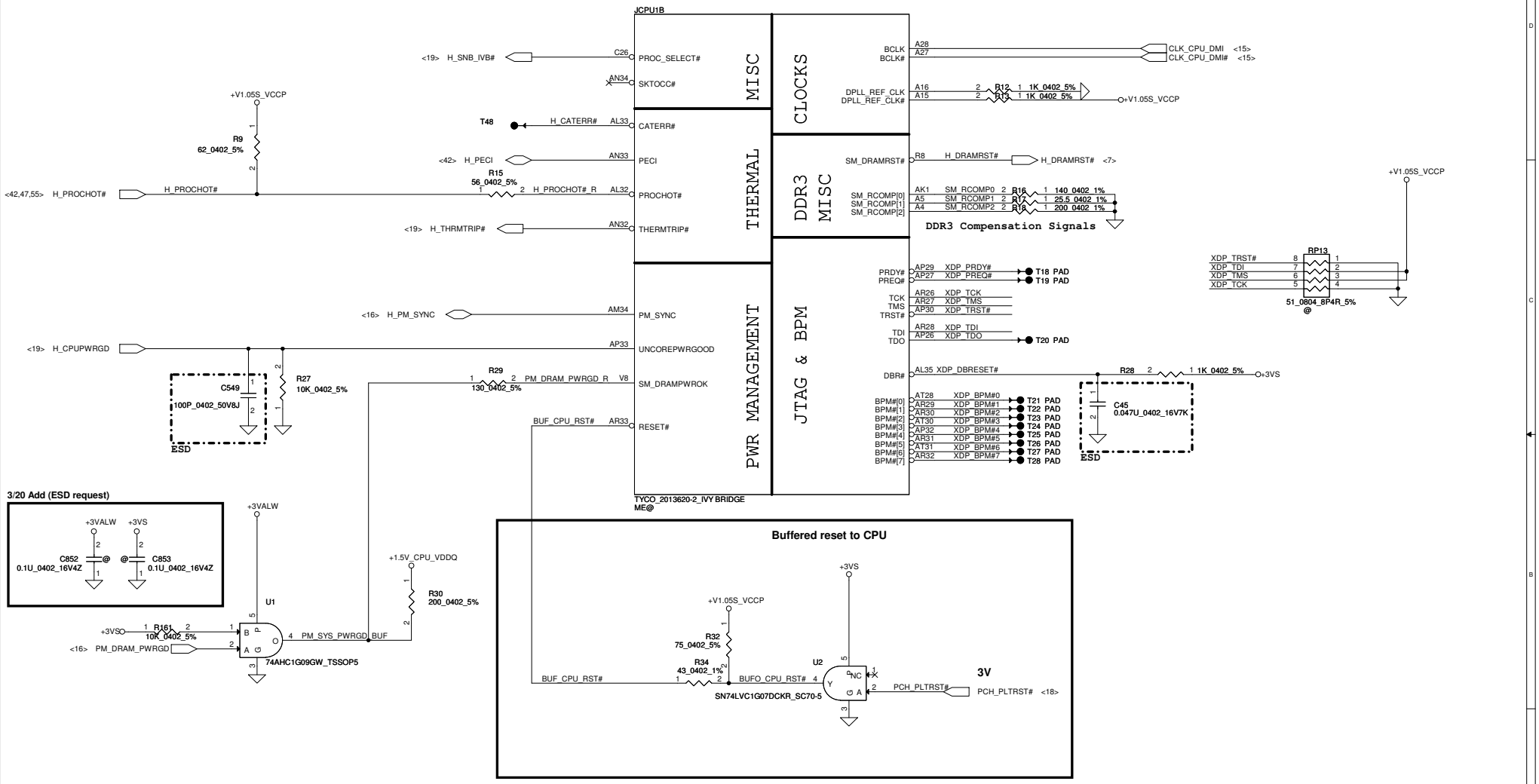


Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 5 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

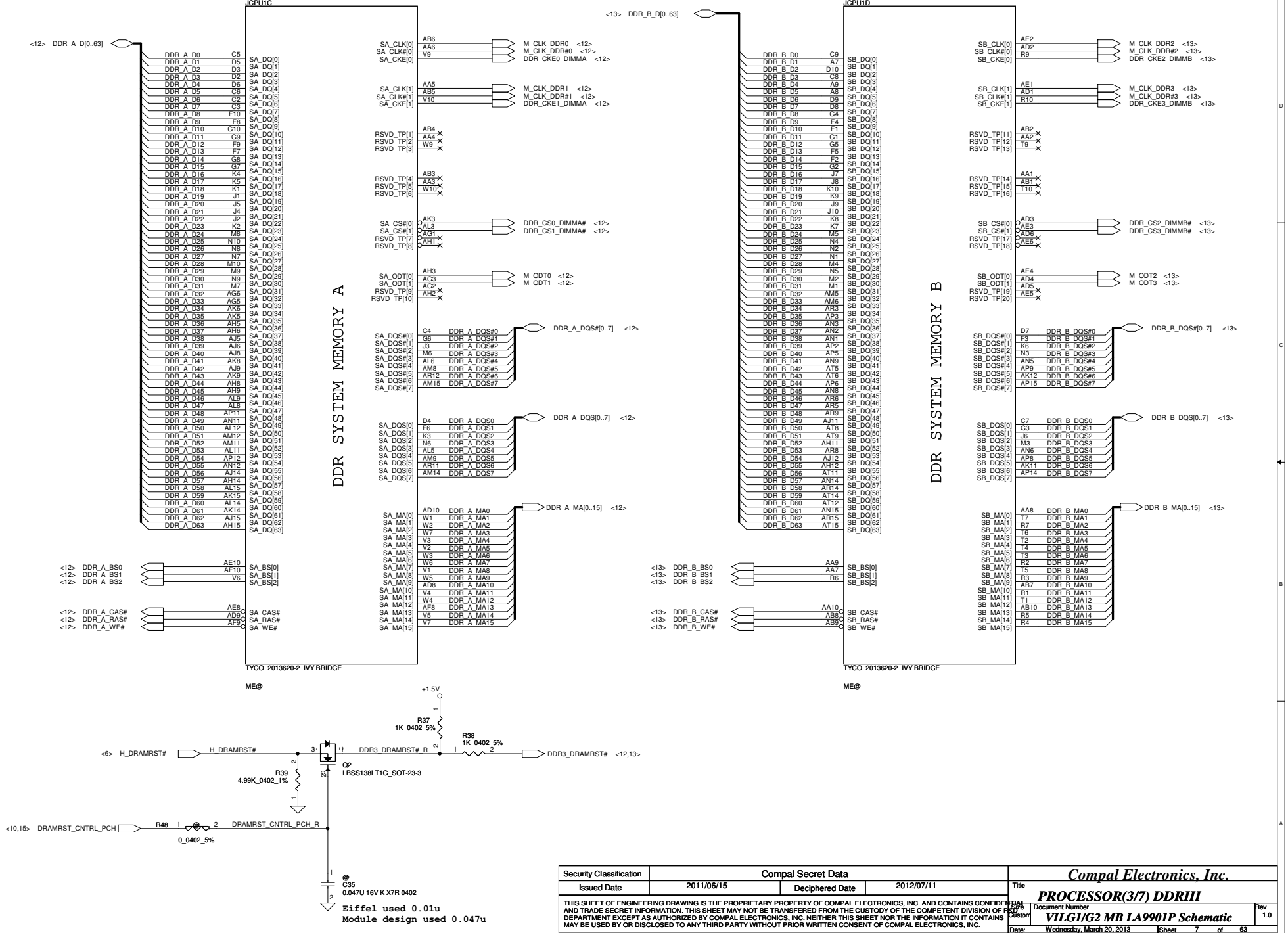


Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 6 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

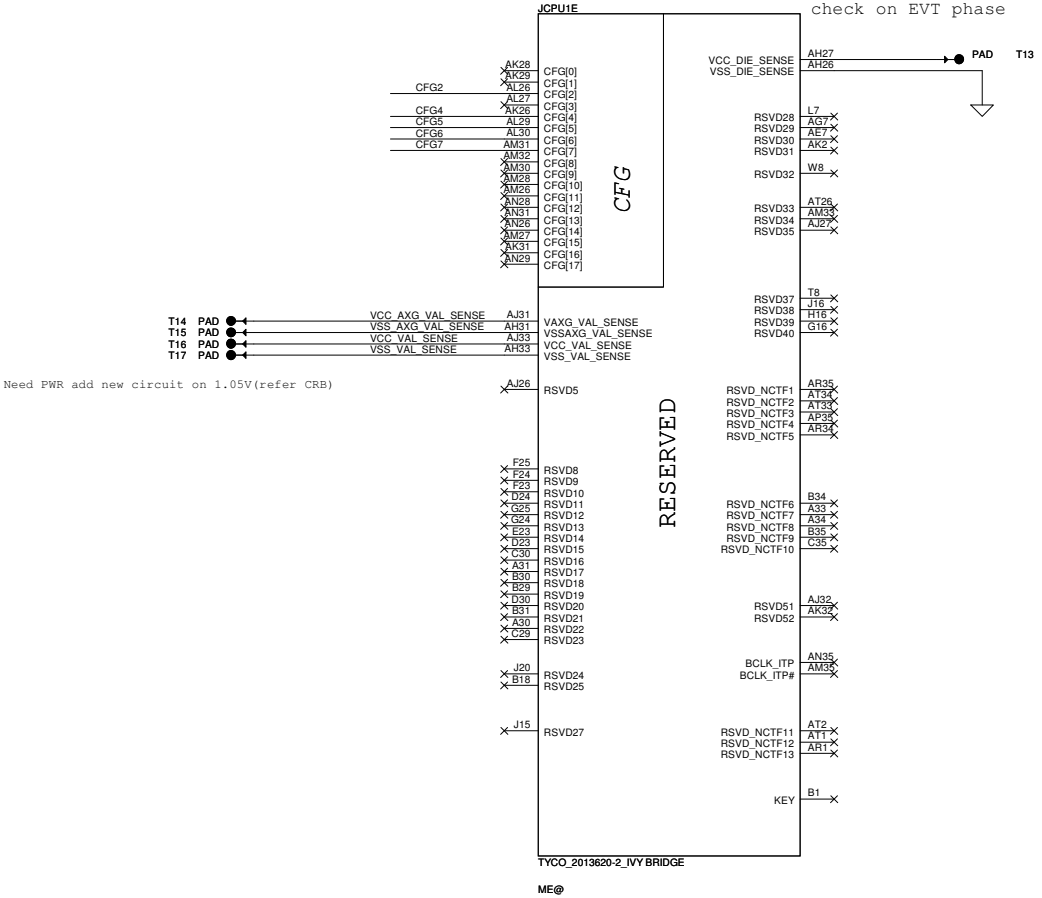
Title: PROCESSOR(3/7) DDRIII

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

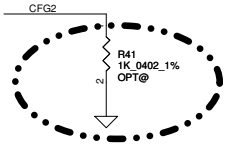
Date: Wednesday, March 20, 2013 | Sheet 7 of 63

# CFG Straps for Processor

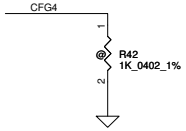
Interl request AH26 short GND
check on EVT phase



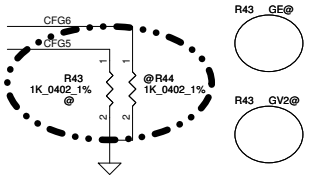

Need PWR add new circuit on 1.05V(refer CRB)



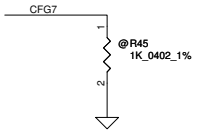

| PEG Static Lane Reversal – CFG2 is for the 16x | |
|---|---|
| CFG2 | 1: Normal Operation; Lane # definition matches socket pin map definition<br>* 0:Lane Reversed |




| Display Port Presence Strap | |
|---|---|
| CFG4 | * 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |




| PCIE Port Bifurcation Straps | |
|---|---|
| CFG[6:5] | 11: (Default) x16 – Device 1 functions 1 and 2 disabled<br>*10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved – (Device 1 function 1 disabled ; function 2 enabled)<br>00: x8,x4,x4 – Device 1 functions 1 and 2 enabled |




| PEG DEFER TRAINING | |
|---|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 8 of 63

# POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

## CORE SUPPLY

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

## PEG AND DDR

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

## SVID

+V1.05S_VCCP

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# — R47 43_0402_5% — VR_SVID_ALRT# <55>
VIDSCLK AJ30 — VR_SVID_CLK <55>
VIDSOUT AJ28 — VR_SVID_DAT <55>

R50 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

## SENSE LINES

+VCC_CORE

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

R51 100_0402_1%

VCC_SENSE AJ35 — VCCSENSE <55>
VSS_SENSE AJ34 — VSSSENSE <55>

R54 100_0402_1%

VCCIO_SENSE B10 — VCCIO_SENSE <53>
VSS_SENSE_VCCIO A10 — VSSIO_SENSE_L — R74 10_0402_1%

R74 & R79 put together

+V1.05S_VCCP

R79 10_0402_1%

VSSIO_SENSE_L <53>

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

ME@

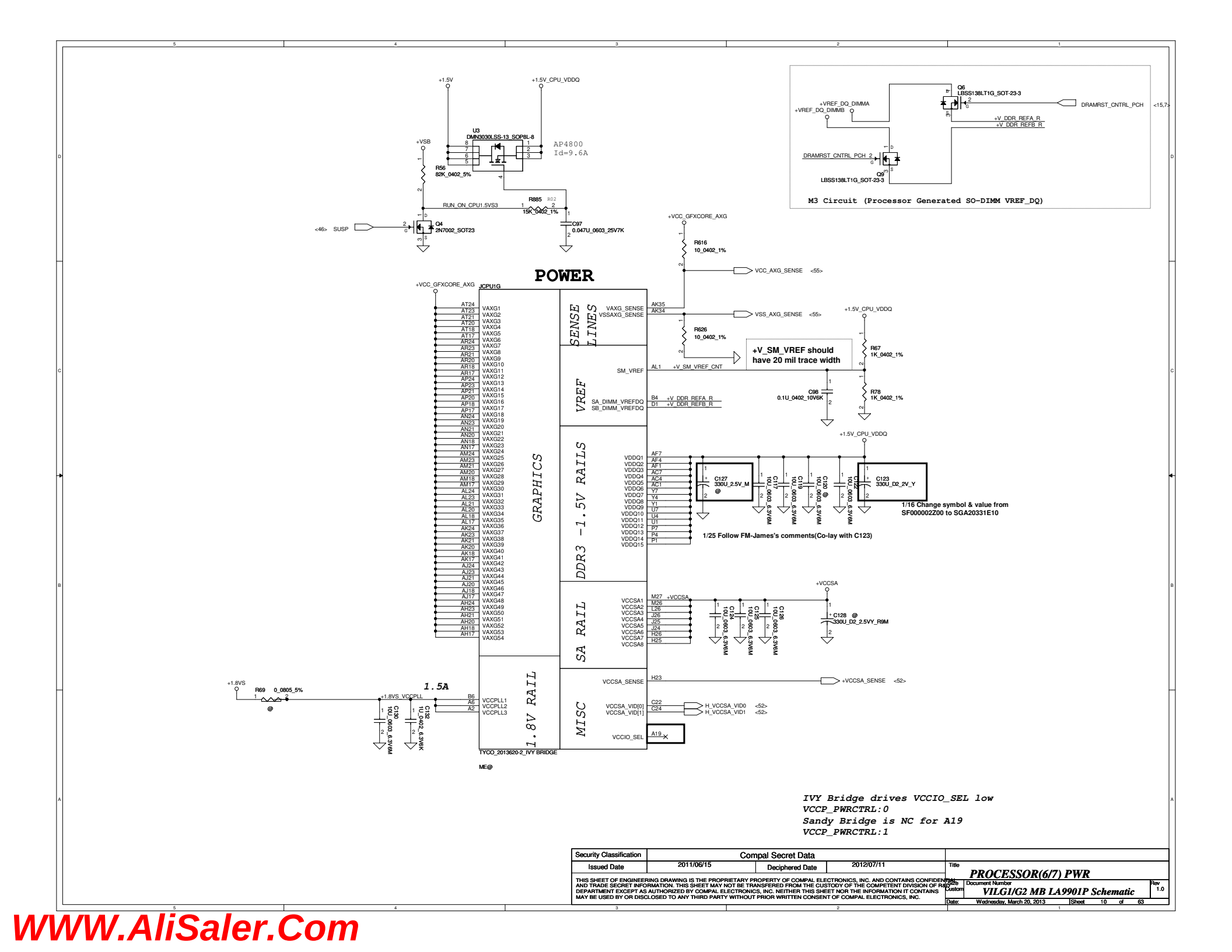
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Title: PROCESSOR(5/7) PWR,BYPASS

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 9 of 63



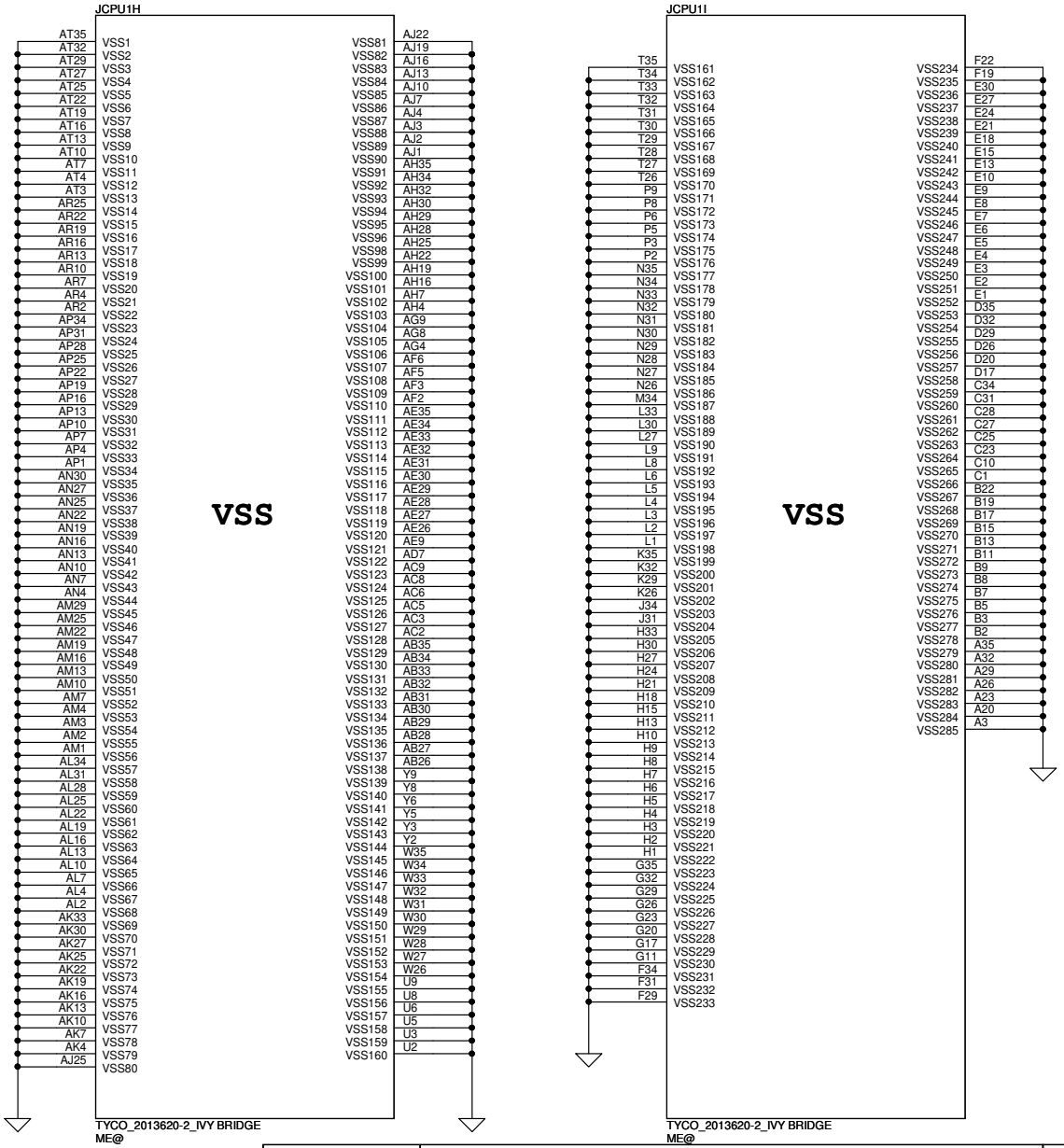

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Title: **PROCESSOR(6/7) PWR**

| Size | Document Number | Rev |
|---|---|---|
| Custom | VILG1/G2 MB LA9901P Schematic | 1.0 |

Date: Wednesday, March 20, 2013 Sheet 10 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

| Size | Document Number | Rev |
|---|---|---|
| Custom | VILG1/G2 MB LA9901P Schematic | 1.0 |

Date: Wednesday, March 20, 2013 Sheet 11 of 63

# DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4806-0103

ME@

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

RP15 1K_0804_8P4R_1%

RP16 1K_0804_8P4R_1%

Layout Note: Place near DIMM

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

Layout Note: Place near DIMM

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

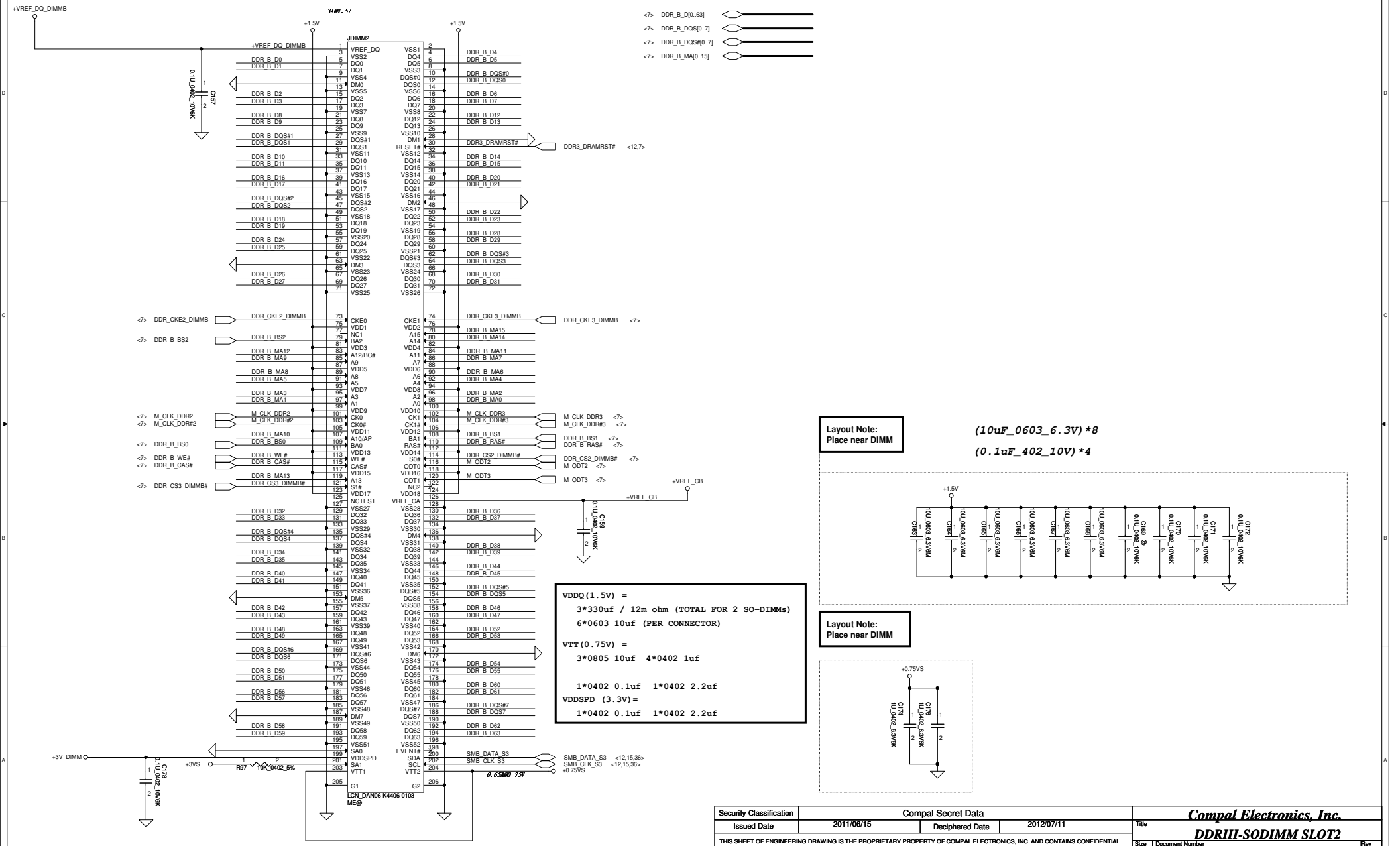


Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

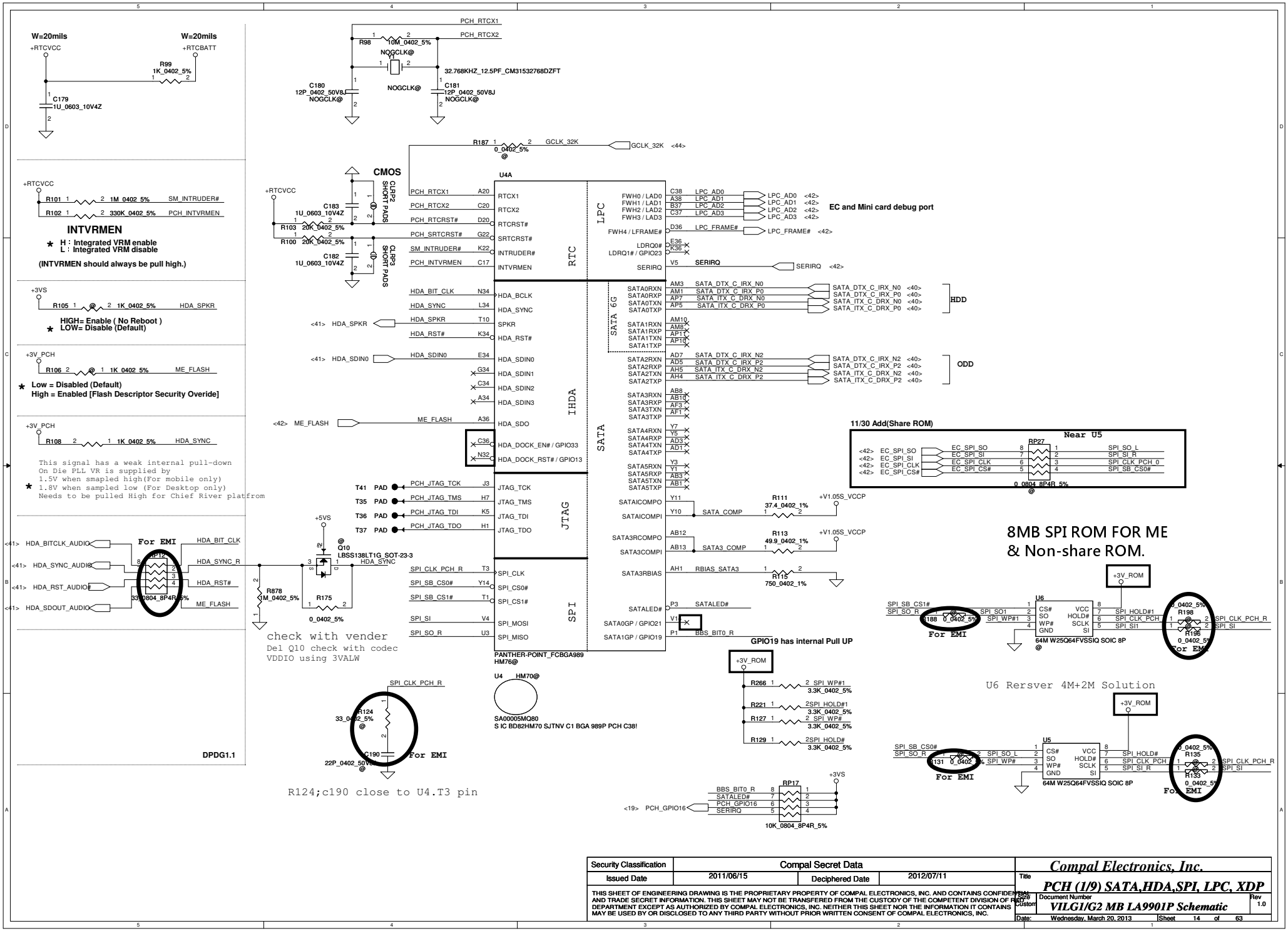
Date: Wednesday, March 20, 2013 | Sheet 12 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



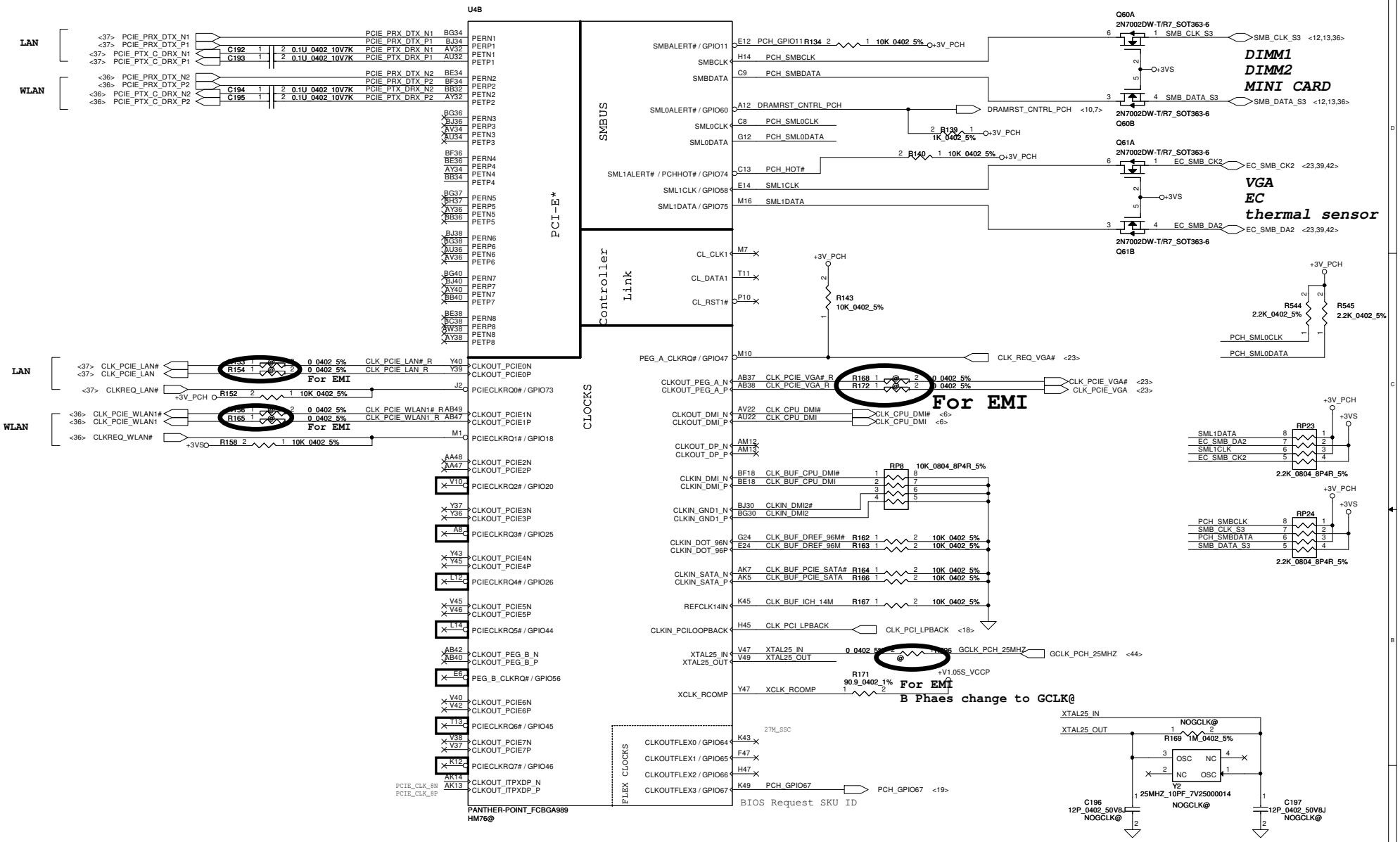
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | DDRIII-SODIMM SLOT2 | | |
| Size | Document Number | VILG1/G2 MB LA9901P Schematic | Rev 1.0 |
| Date: Wednesday, March 20, 2013 | Sheet 13 of 63 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | PCH (1/9) SATA,HDA,SPI, LPC, XDP | | |
| Size | Document Number | | Rev |
| Custom | VILG1/G2 MB LA9901P Schematic | | 1.0 |
| Date: | Wednesday, March 20, 2013 | Sheet | 14 of 63 |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

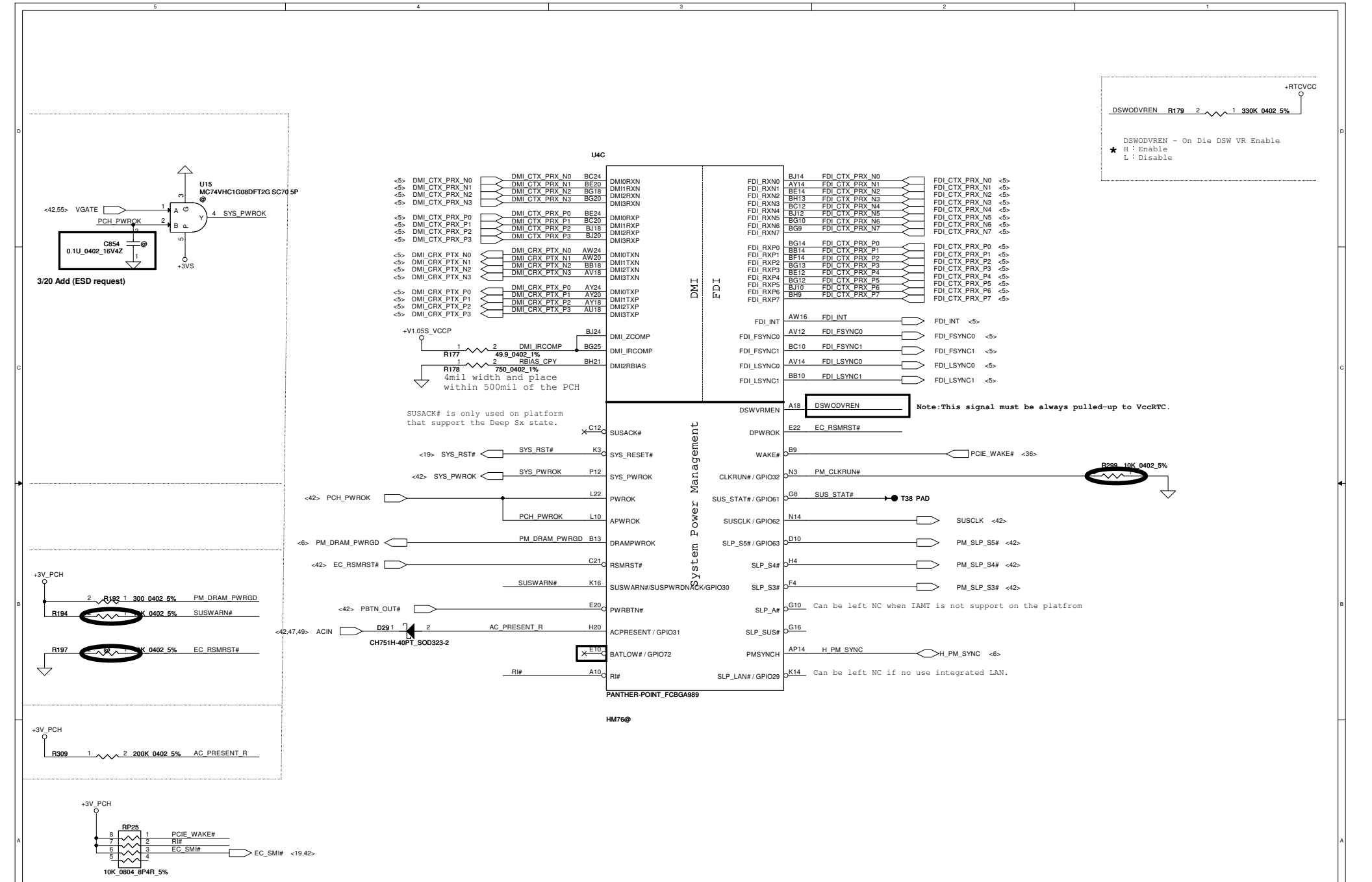


Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 15 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

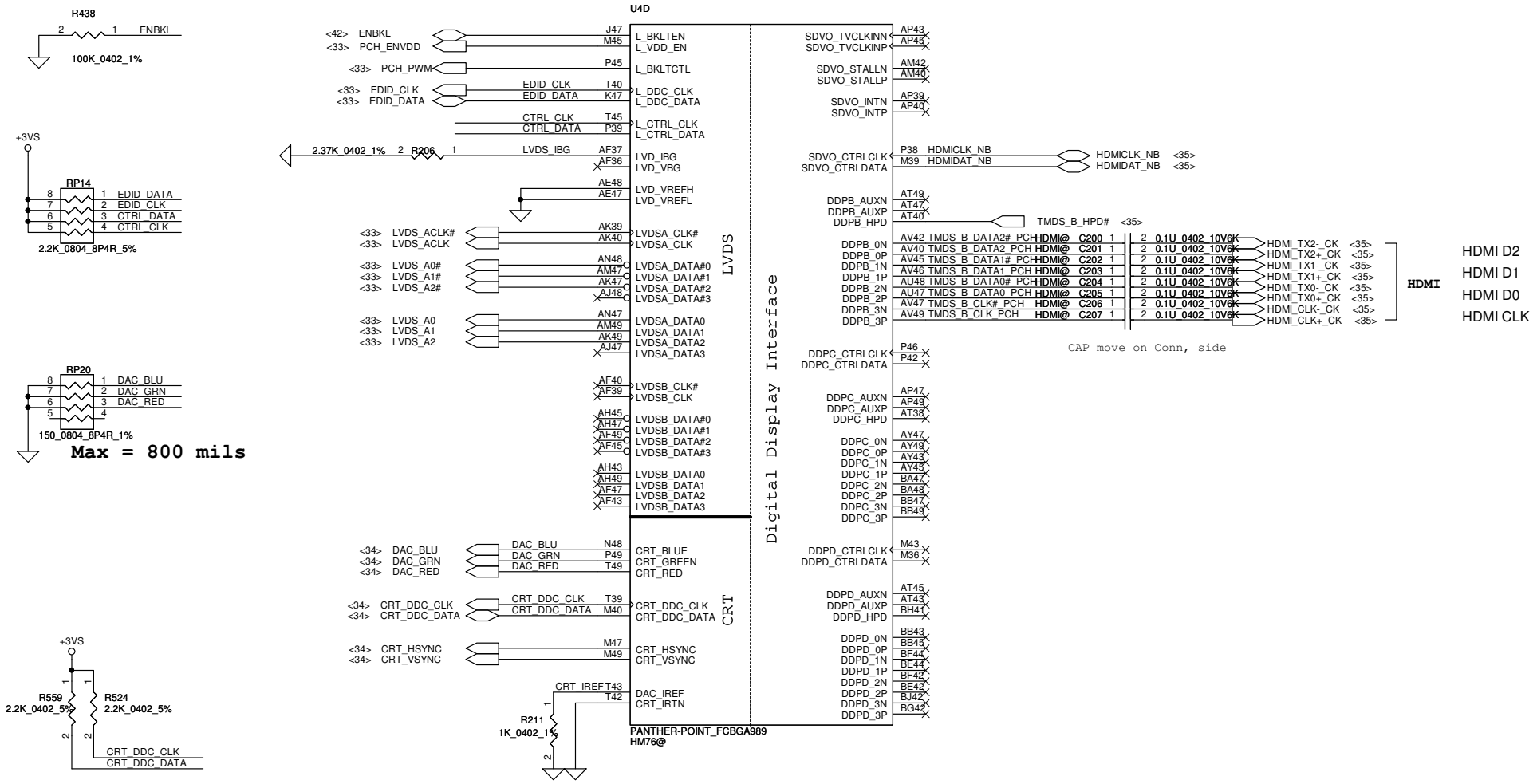


Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 16 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

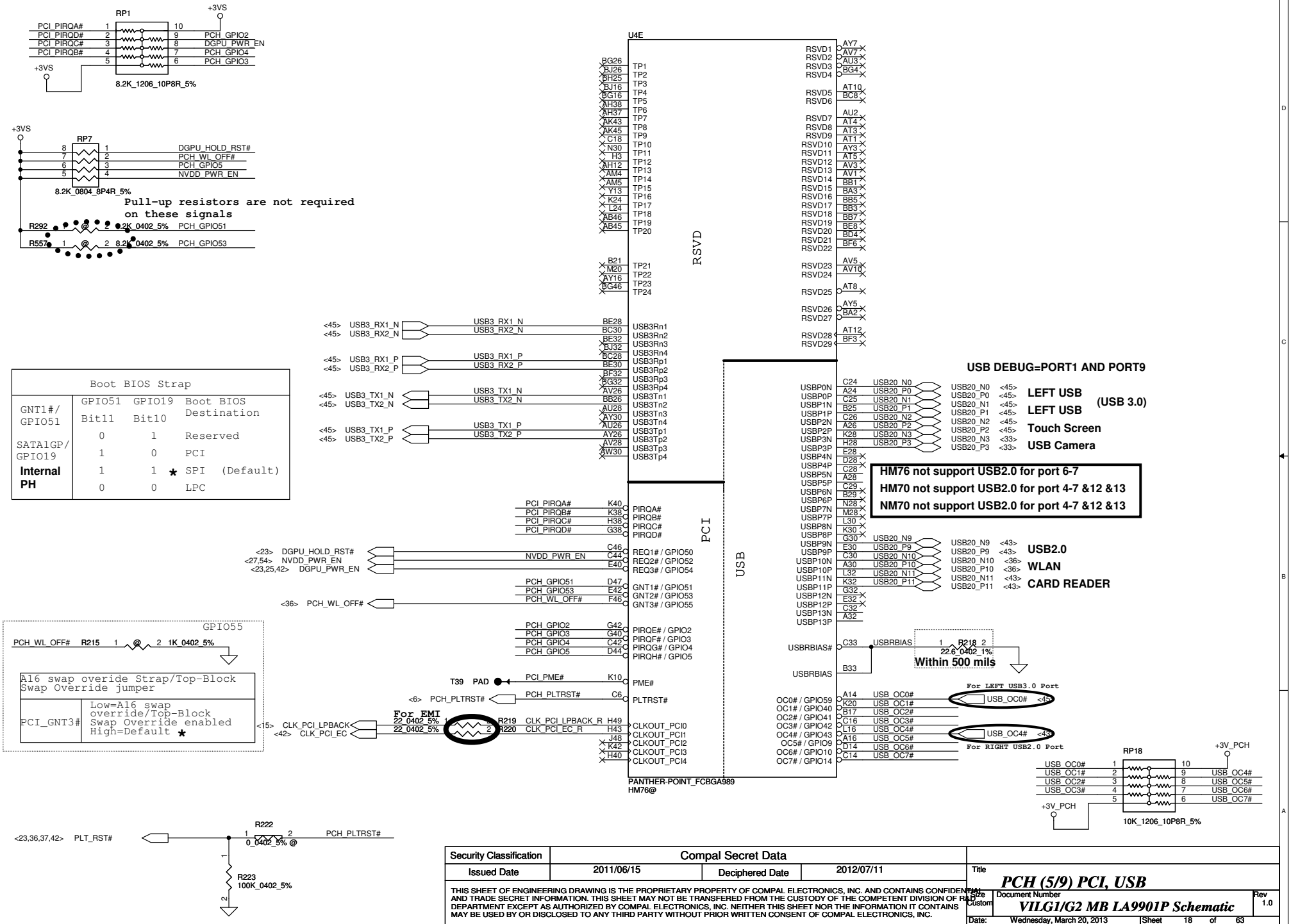


Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size: B | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 17 of 63






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 18 of 63

| PCH_GPIO69 | PCH_GPIO70 | Function |
|---|---|---|
| – | – | NM70 |
| – | – | Reserved |
| – | 1 | HM70 |
| – | 0 | HM76 |

| PCH_GPIO71 | Function |
|---|---|
| 1 | N14M-GE 1000MHz |
| 0 | N14M-GE 900MH |

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

R240 1 @ 2 1K_0402_5% PCH_GPIO28

★ PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

R245 1 @ 2 10K_0402_5% PCH_GPIO27

**GPIO36, 37**
**When Unused as GPIO or SATA*GP**
**Use 8.2K-10K pull-down to ground.**

R248 @ 10K_0402_5% PCH_GPIO37 R881 10K_0402_5% @
R250 @ 10K_0402_5% PCH_GPIO36 R547 @ 10K_0402_5%

R702 @ 10K_0402_5% PCH_GPIO69 R707 @ 10K_0402_5%
R703 HM70@ 10K_0402_5% PCH_GPIO70 R705 HM76@ 10K_0402_5%
R704 1000M@ 10K_0402_5% PCH_GPIO71 R706 900M@ 10K_0402_5%

U4F

| | | | |
|---|---|---|---|
| T7 | BMBUSY# / GPIO0 | TACH4 / GPIO68 | C40 |
| A42 | TACH1 / GPIO1 | TACH5 / GPIO69 | B41 PCH_GPIO69 |
| H36 | TACH2 / GPIO6 | TACH6 / GPIO70 | C41 PCH_GPIO70 |
| E38 | TACH3 / GPIO7 | TACH7 / GPIO71 | A40 PCH_GPIO71 |
| C10 | GPIO8 | | |
| C4 | LAN_PHY_PWR_CTRL / GPIO12 | | |
| G2 | GPIO15 | A20GATE | P4 |
| U2 | SATA4GP / GPIO16 | PECI | AU16 |
| D40 | TACH0 / GPIO17 | RCIN# | P5 |
| T5 | SCLOCK / GPIO22 | PROCPWRGD | AY11 |
| E8 | GPIO24 | THRMTRIP# | AY10 |
| E16 | GPIO27 | INIT3_3V# | T14 |
| P8 | GPIO28 | DF_TVS | AY1 |
| K1 | STP_PCI# / GPIO34 | TS_VSS1 | AH8 |
| K4 | GPIO35 | TS_VSS2 | AK11 |
| V8 | SATA2GP / GPIO36 | TS_VSS3 | AH10 |
| M5 | SATA3GP / GPIO37 | TS_VSS4 | AK10 |
| N2 | SLOAD / GPIO38 | NC_1 | P37 |
| M3 | SDATAOUT0 / GPIO39 | | |
| V13 | SDATAOUT1 / GPIO48 | VSS_NCTF_15 | BG2 |
| V3 | SATA5GP / GPIO49 / TEMP_ALERT# | VSS_NCTF_16 | BG48 |
| D6 | GPIO57 | VSS_NCTF_17 | BH3 |
| | | VSS_NCTF_18 | BH47 |
| A4 | VSS_NCTF_1 | VSS_NCTF_19 | BJ4 |
| A44 | VSS_NCTF_2 | VSS_NCTF_20 | BJ44 |
| A45 | VSS_NCTF_3 | VSS_NCTF_21 | BJ45 |
| A46 | VSS_NCTF_4 | VSS_NCTF_22 | BJ46 |
| A5 | VSS_NCTF_5 | VSS_NCTF_23 | BJ5 |
| A6 | VSS_NCTF_6 | VSS_NCTF_24 | BJ6 |
| B3 | VSS_NCTF_7 | VSS_NCTF_25 | C2 |
| B47 | VSS_NCTF_8 | VSS_NCTF_26 | C48 |
| BD1 | VSS_NCTF_9 | VSS_NCTF_27 | D1 |
| BD49 | VSS_NCTF_10 | VSS_NCTF_28 | D49 |
| BE1 | VSS_NCTF_11 | VSS_NCTF_29 | E1 |
| BE49 | VSS_NCTF_12 | VSS_NCTF_30 | E49 |
| BF1 | VSS_NCTF_13 | VSS_NCTF_31 | F1 |
| BF49 | VSS_NCTF_14 | VSS_NCTF_32 | F49 |

GPIO | CPU/MISC | NCTF

PANTHER-POINT_FCBGA989

HM76@

<42> EC_SCI# EC_SCI#
<16,42> EC_SMI# EC_SMI#
+3V_PCH R230 1 2 1K_0402_5% EC_LID_OUT#
<42> EC_LID_OUT#
<14> PCH_GPIO16 PCH_GPIO16
<26,27,54> DGPU_PWROK PU on power side
<36> PCH_BT_ON# PCH_BT_ON#
<40> ODD_EN ODD_EN
+3V_PCH R241 1 2 10K_0402_5% PCH_GPIO27
PCH_GPIO28
<36> INTEL_BT_OFF# INTEL_BT_OFF#
+3VSO R242 1 2 10K_0402_5%
PCH_GPIO35
PCH_GPIO36
PCH_GPIO37
PCH_GPIO38
PCH_GPIO39

+3VS R236 10K_0402_5% GATEA20 <42>
KBRST# <42>
H_CPUPWRGD <6>
PCH_THRMTRIP# R 1 R239 2 390_0402_5% H_THRMTRIP# <6>
KBRST# R226 1 2 10K_0402_5%

INIT3_3V
This signal has weak internal PU,can't pull low

| DMI Termination Voltage | |
|---|---|
| NV_CLE | Set to Vcc when HIGH |
| | Set to Vss when LOW |

+1.8VS R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
Weak internal PU,Do not pull low
CLOSE TO THE BRANCHING POINT

BIOS Request SKU ID

+3VS R711 UMA@ 10K_0402_5% R246 UMA@ 10K_0402_5%
PCH_GPIO38
PCH_GPIO67 PCH_GPIO67 <15>
R708 OPT@ 10K_0402_5% R298 OPT@ 10K_0402_5%

+3VS RP10 10K_0804_8P4R_5%
8 PCH_GPIO39
7 SYS_RST# SYS_RST# <16>
6 PCH_BT_ON#
5 PCH_GPIO35

| PCH_GPIO38 | PCH_GPIO67 | Function |
|---|---|---|
| 0 | 0 | Optimus |
| 0 | 1 | Reserved |
| 1 | 0 | DIS |
| 1 | 1 | UMA |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



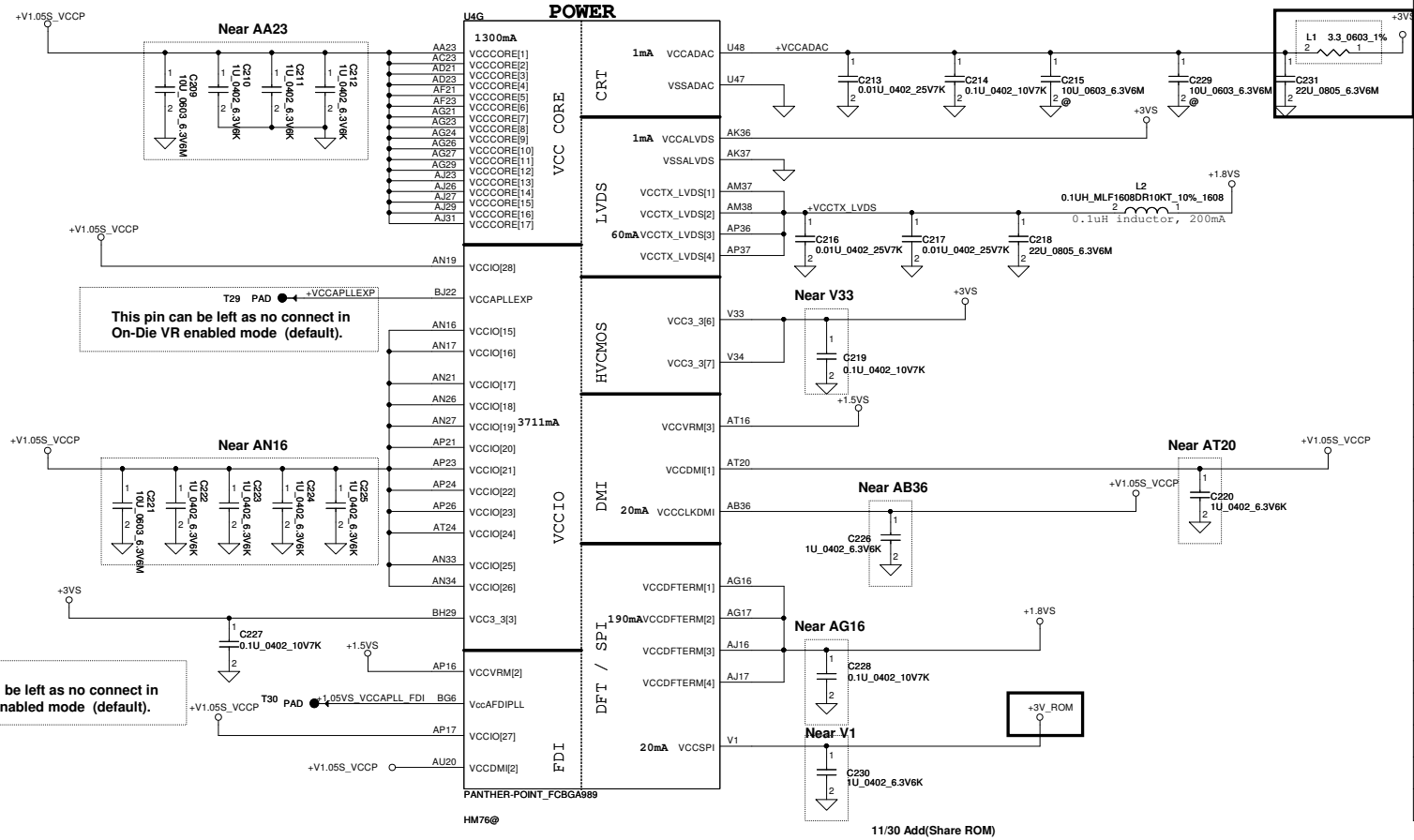
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 19 of 63

L1 Change to 1 ohm P/N
S RES 1/10W 1 +-1% 0603



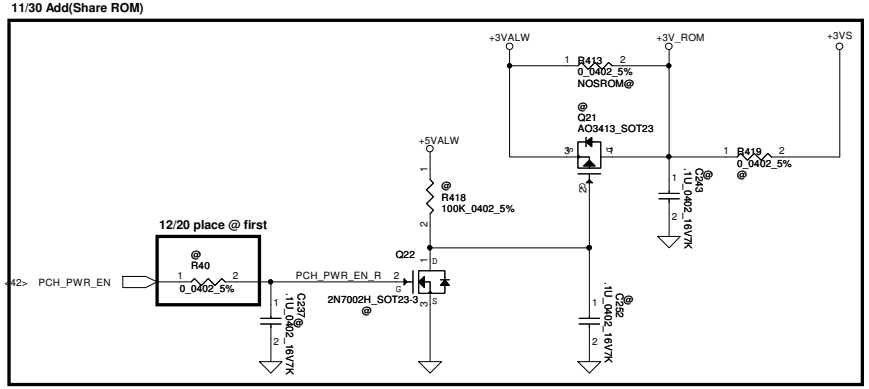

| PCH Power Rail Table Refer to CPU EDS R1.5 | | |
|---|---|---|
| Voltage Rail | Voltage | S0 Iccmax Current (A) |
| V_PROC_IO | 1.05 | 0.001 |
| V5REF | 5 | 0.001 |
| V5REF_Sus | 5 | 0.001 |
| Vcc3_3 | 3.3 | 0.228 |
| VccADAC | 3.3 | 0.001 |
| VccADPLLA | 1.05 | 0.075 |
| VccADPLLB | 1.05 | 0.075 |
| VccCore | 1.05 | 1.3 |
| VccDMI | 1.05 | 0.042 |
| VccIO | 1.05 | 3.709 |
| VccASW | 1.05 | 0.903 |
| VccSPI | 3.3 | 0.01 |
| VccDSW | 3.3 | 0.001 |
| VccDFTERM | 1.8 | 0.002 |
| VccRTC | 3.3 | 6 uA |
| VccSus3_3 | 3.3 | 0.065 |
| VccSusHDA | 3.3 / 1.5 | 0.01 |
| VccVRM | 1.8 / 1.5 | 0.167 |
| VccCLKDMI | 1.05 | 0.075 |
| VccSSC | 1.05 | 0.095 |
| VccDIFFCLKN | 1.05 | 0.055 |
| VccALVDS | 3.3 | 0.001 |
| VccTX_LVDS | 1.8 | 0.04 |

Intel recommand stuff R265 and unstuff R266

VCCVRM==>1.5V FOR MOBILE
VCCVRM==>1.8V FOR DESKTOP

VCCVRM = 160mA detal waiting for newest spec

11/30 Add(Share ROM)




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

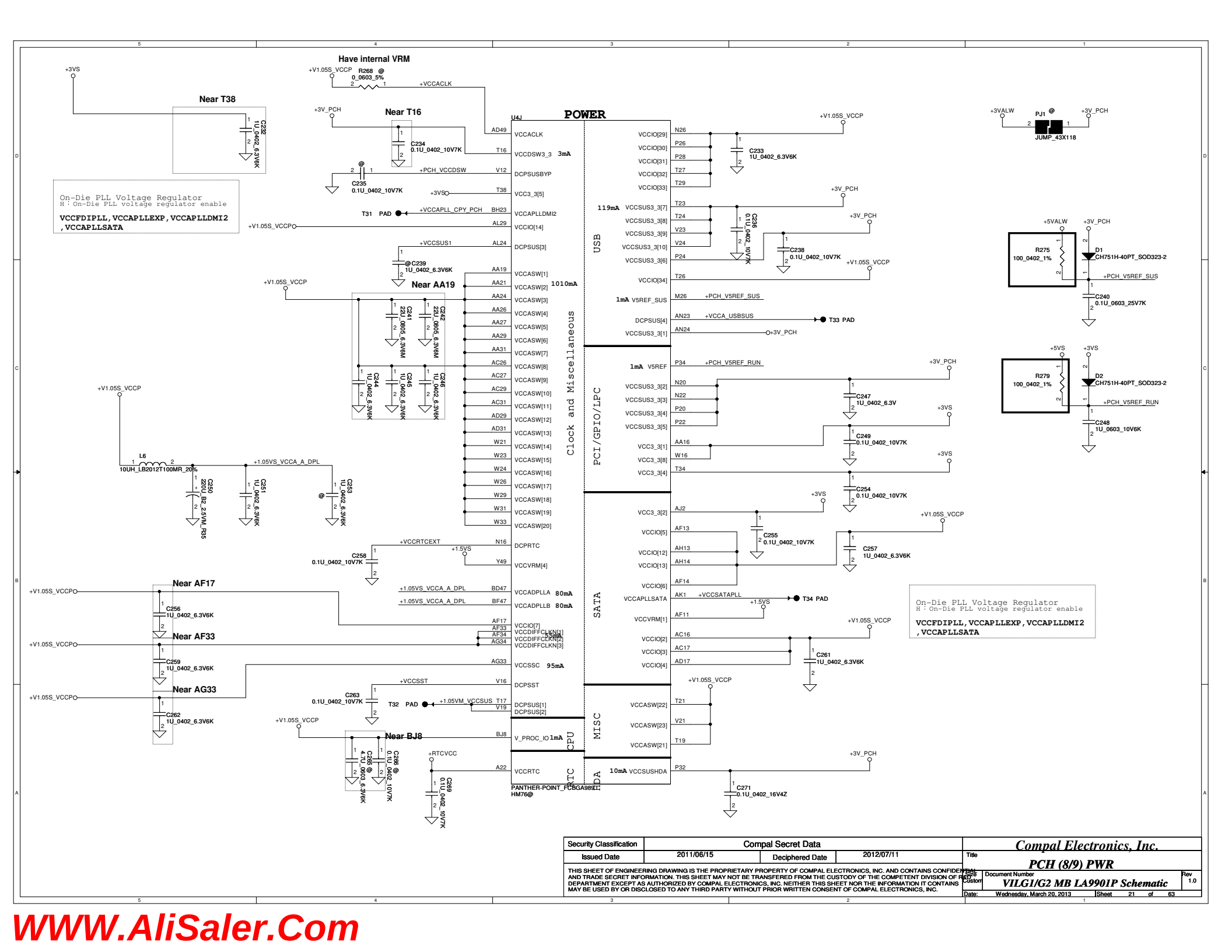


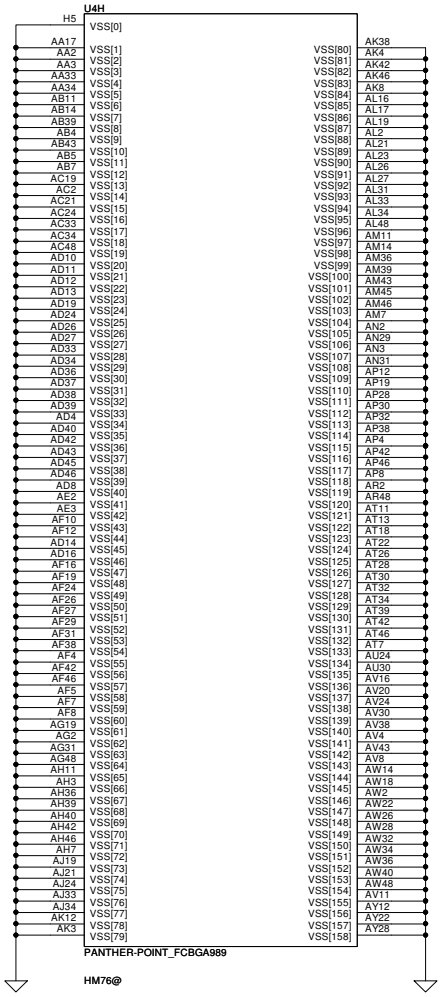
Compal Electronics, Inc.

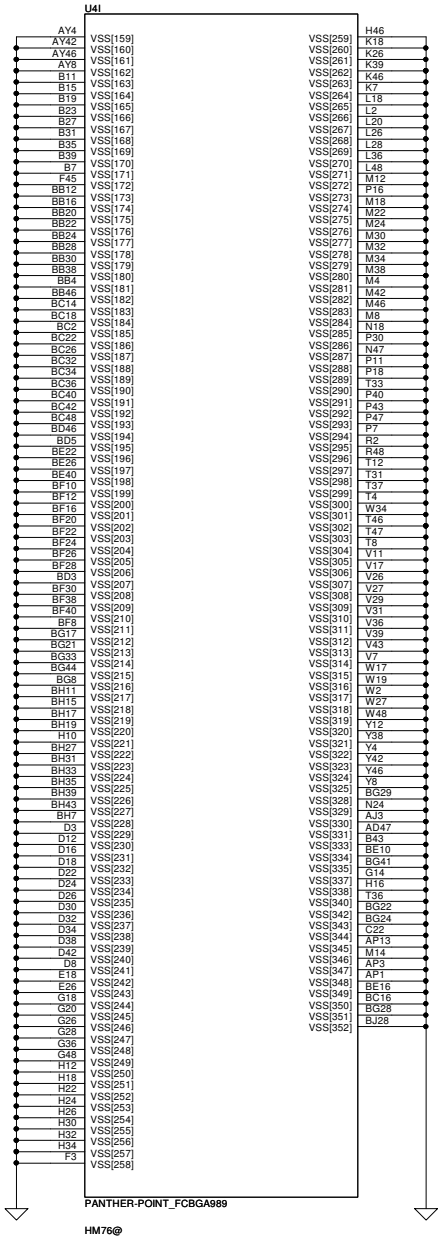
Title: PCH (7/9) PWR

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 20 of 63






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

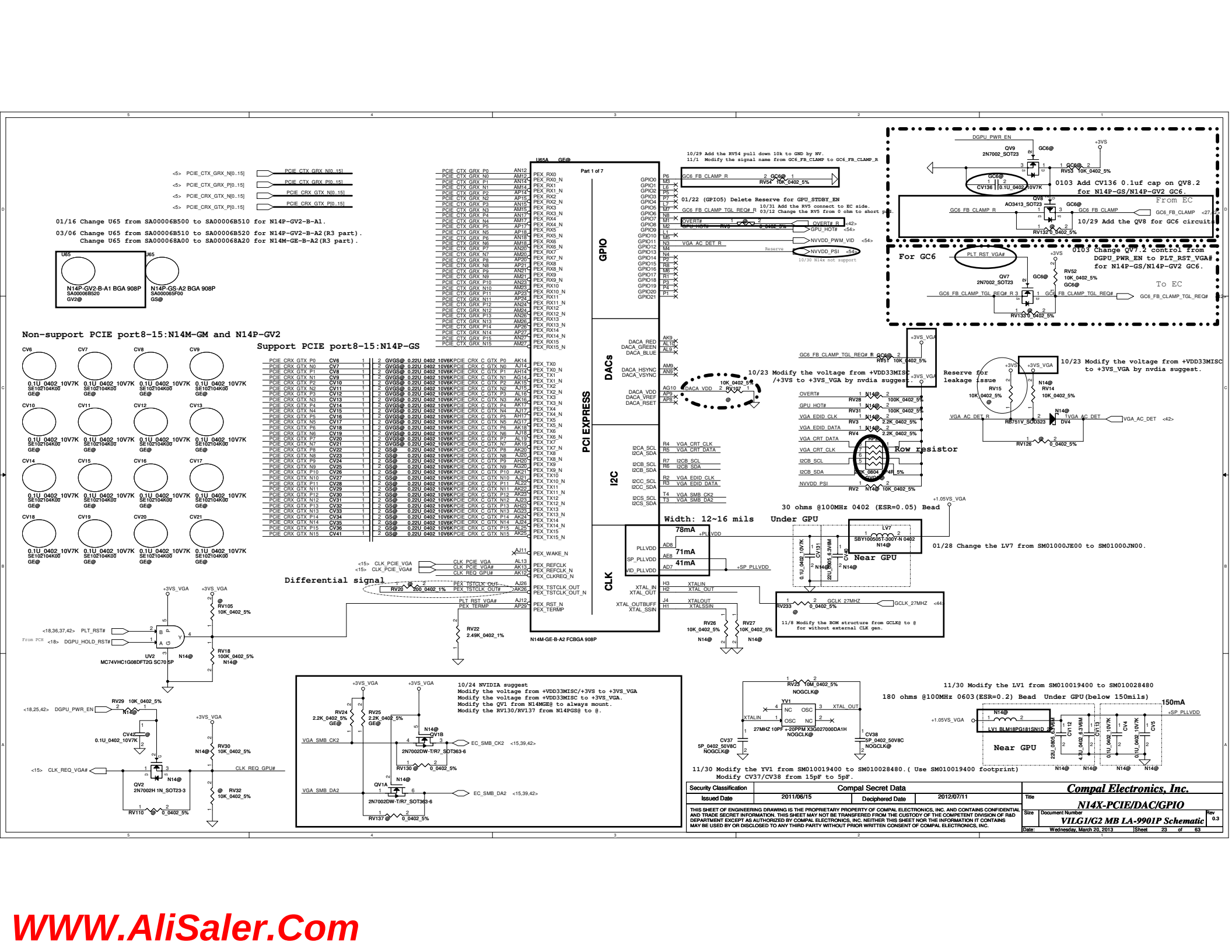


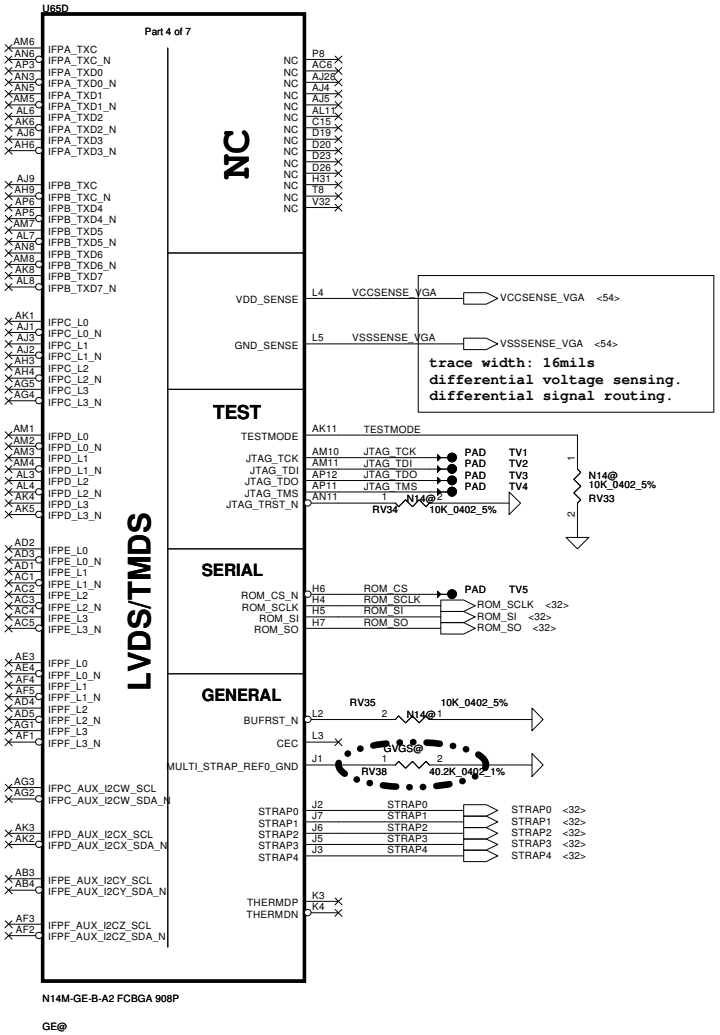
Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 22 of 63






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



**Compal Electronics, Inc.**

Title: **N14X-LVDS/HDMI/DP/THM**

Size: D | Document Number: **VILG1/G2 MB LA-9901P Schematic** | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 24 of 63

0128: Change the BOM structure of CV58/CV59/CV278/CV282 from N14@ to GS@.

rise 1.5v system source voltage to 1.55-1.57V

| CALIBRATION PIN | DDR3 |
|---|---|
| FB_CAL_x_PD_VDDQ | 40.2Ohm |
| FB_CAL_x_PU_GND | 42.2Ohm |
| FB_CAL_xTERM_GND | 51.1Ohm |

+3VS to +3VS_VGA

For R-short

Row resistor

+1.5V to +1.5VS_VGA

For R-short

11/30 Modify the CV63 from 0.01uF to 1uF.
01/28 Change the RV41 from 1k to 150k.
Change the CV63 to SE000000U00.

11.27 Add the QV4 and RV42.
Modify the RV41 from 200k to 1K for EVT test.
Modify the QV3 from SB00000QP00 to SB00000EN00.
Modify the UV11 from SB00000RV00 to SB548000210.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

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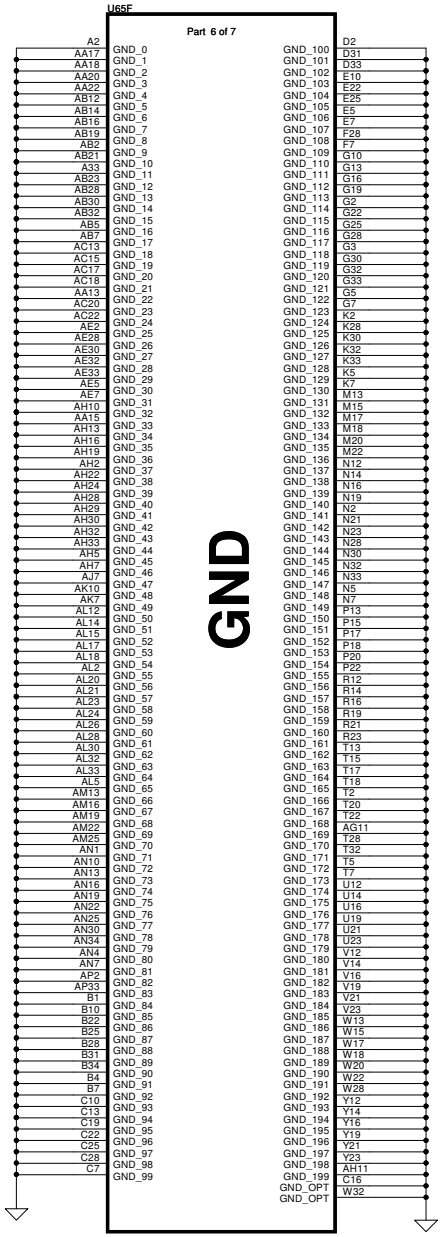
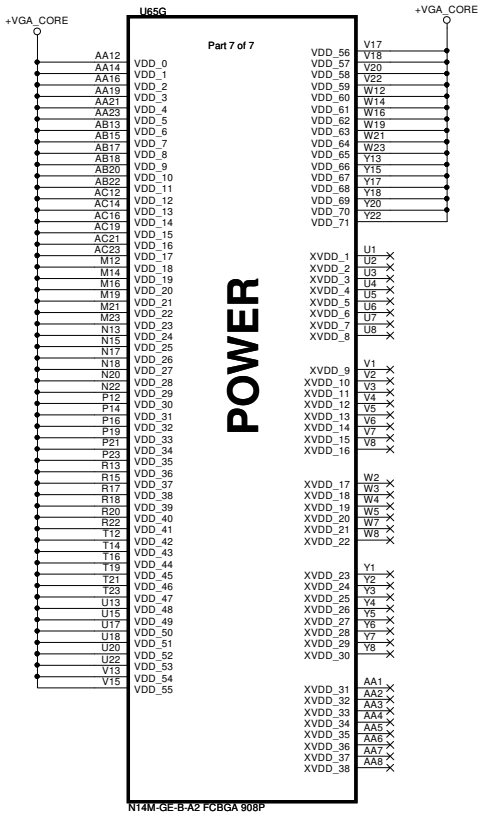
Compal Electronics, Inc.

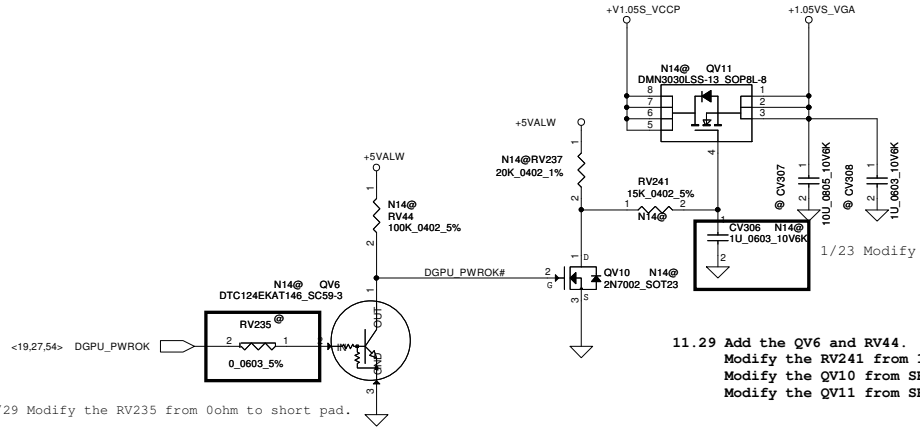
Title: N14X-POWER

Size: C | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 25 of 63




1/23 Modify the CV306 from 0.1uF to 1uF.

11/29 Modify the RV235 from 0ohm to short pad.

11.29 Add the QV6 and RV44.
Modify the RV241 from 100k to 15K for EVT test.
Modify the QV10 from SB00000QP00 to SB00000EN00.
Modify the QV11 from SB00000TO00 to SB548000210.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

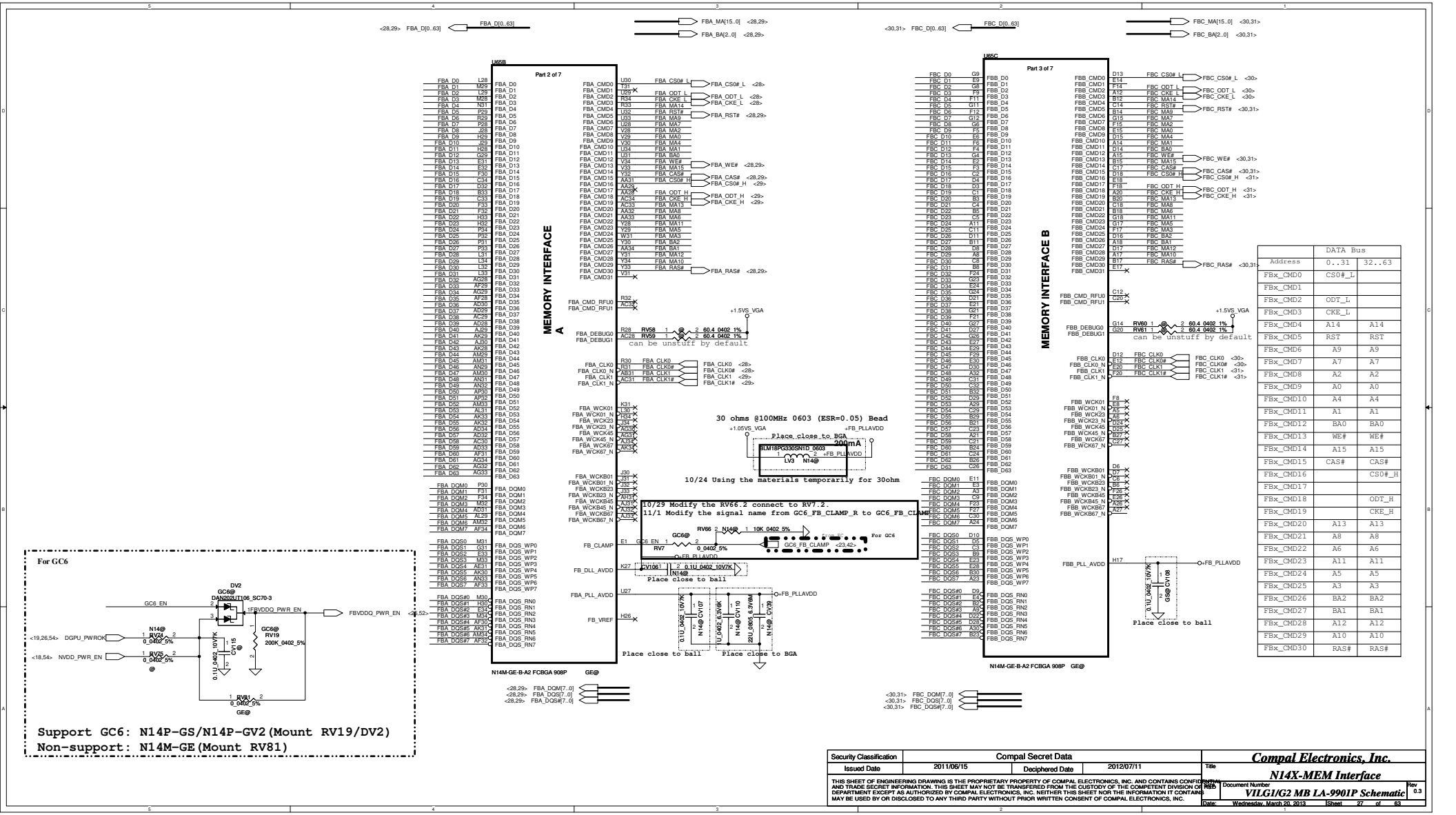


Compal Electronics, Inc.

Title: N14X-VGA CORE, GND

Size: C | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 26 of 63




| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |

For GC6

Support GC6: N14P-GS/N14P-GV2(Mount RV19/DV2)
Non-support: N14M-GE(Mount RV81)

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

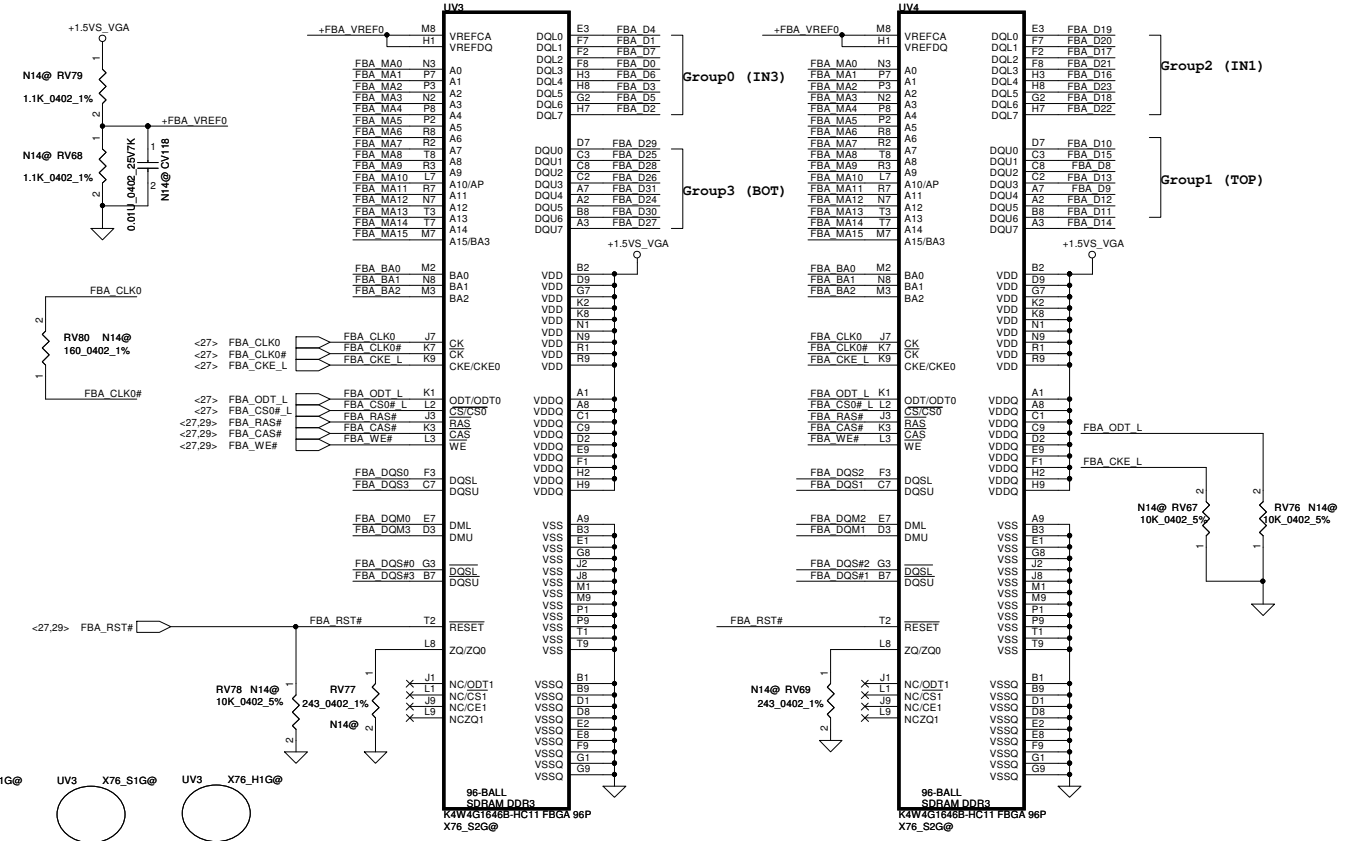
Title: N14X-MEM Interface

Document Number: VILG1/G2 MB LA-9901P Schematic

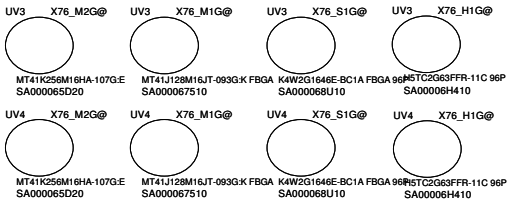
Rev: 0.3

Date: Wednesday, March 20, 2013 Sheet 27 of 63

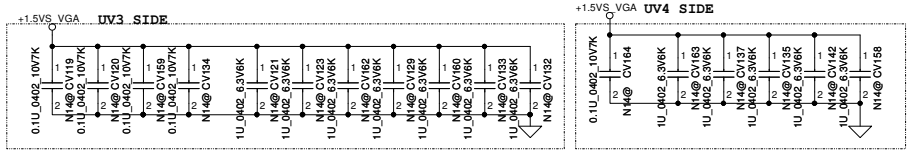
# Memory Partition A - Lower 32 bits



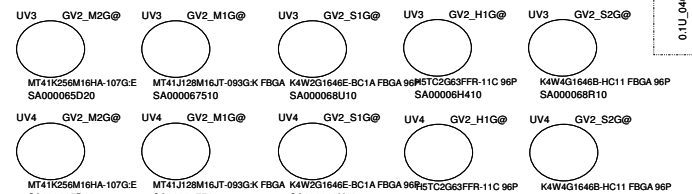

| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |




03/18 Change UV3/UV4/UV5/UV6 from SA000068R00 to SA000068R10 for SAM 2G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA000065D00 to SA000065D20 for MIC 2G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA000068U00 to SA000068U10 for SAM 1G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA000067500 to SA000067510 for MIC 1G VRAM(R3 part).
Change UV3/UV4/UV5/UV6 from SA00006H400 to SA00006H410 for HYN 1G VRAM(R3 part).




0111 Change UV3/UV4/UV5/UV6
from SA000065300 to SA00006H400 for Hynix VRAM




0206 Add UV3/UV4/UV5/UV6 BOM structure for N14P-GV2.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



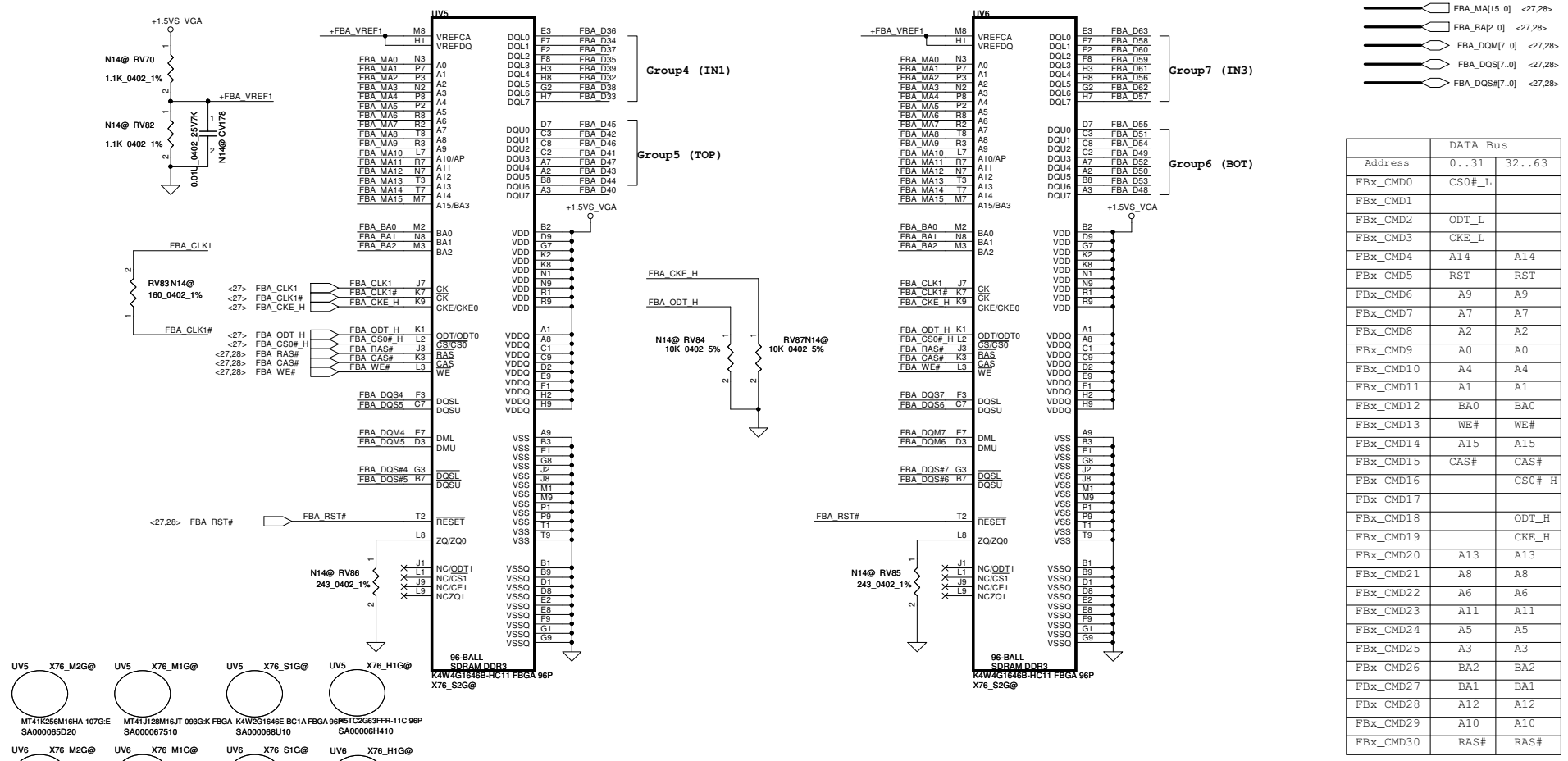
Compal Electronics, Inc.

Title: N14X-VRAM A Lower

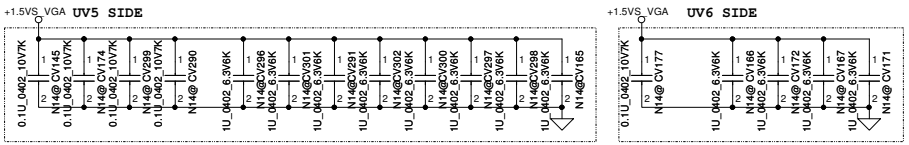
Size: B | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 28 of 63

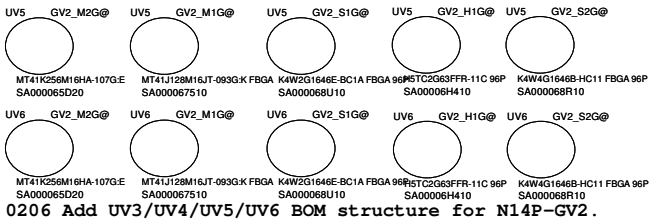
# Memory Partition A - Upper 32 bits




| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |




0111 Change UV3/UV4/UV5/UV6
from SA000065300 to SA00006H400 for Hynix VRAM




0206 Add UV3/UV4/UV5/UV6 BOM structure for N14P-GV2.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



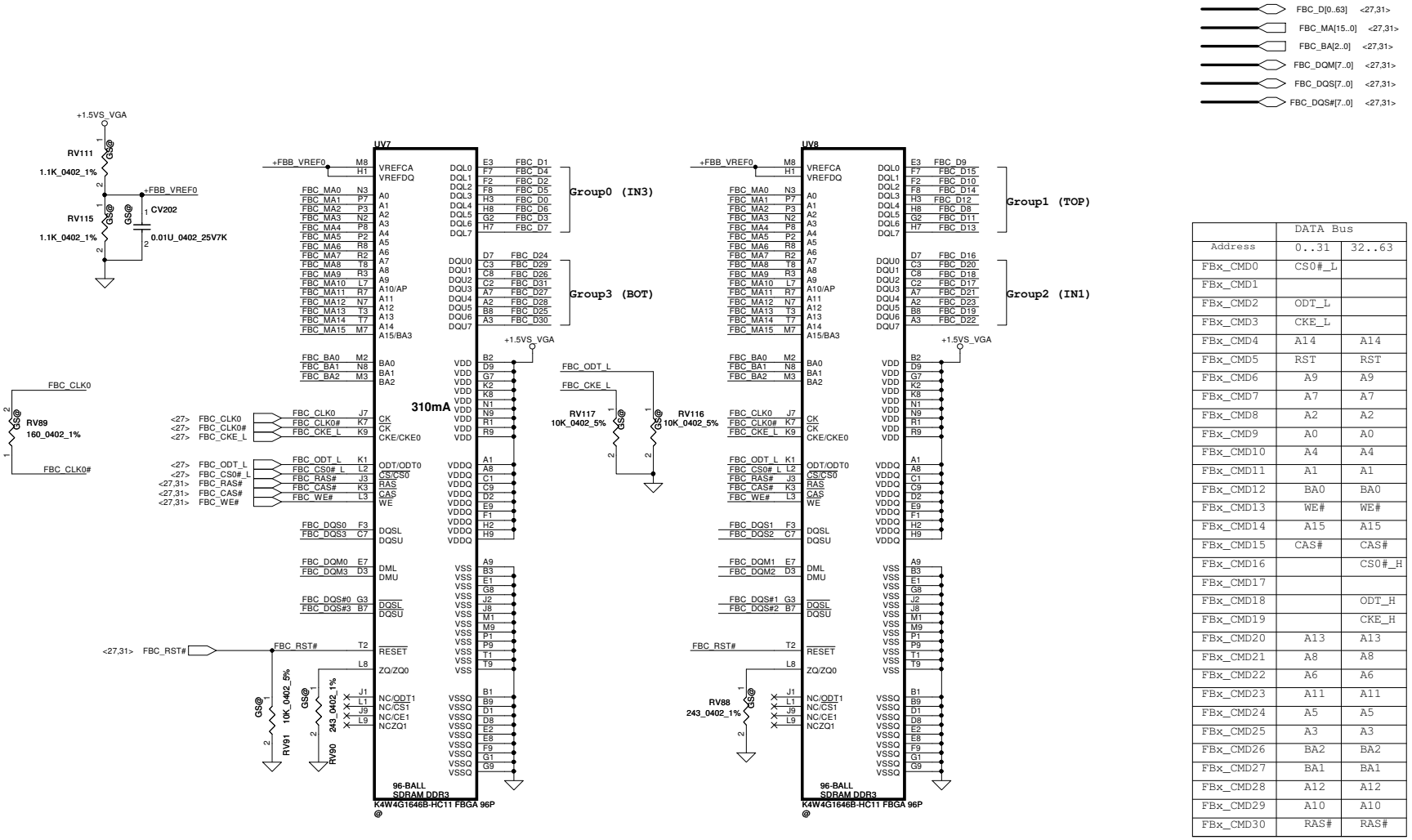
Compal Electronics, Inc.

Title: N14X-VRAM A Upper

Size: B | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 29 of 63

# Memory Partition C – Lower 32 bits




| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



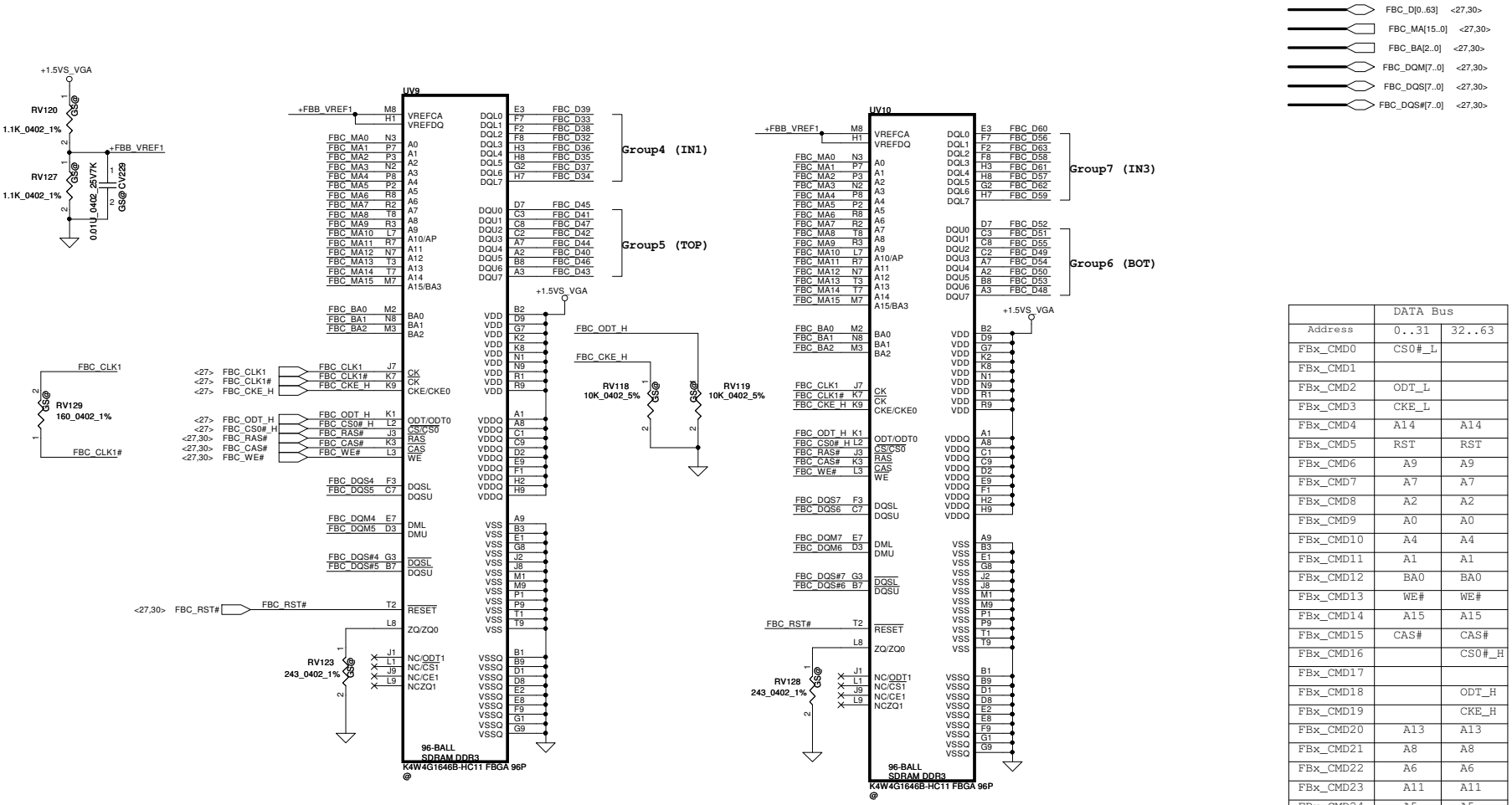
**Compal Electronics, Inc.**

Title: N14X-VRAM C Lower

Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 30 of 63

# Memory Partition C – Upper 32 bits




| | DATA Bus | |
|---|---|---|
| Address | 0..31 | 32..63 |
| FBx_CMD0 | CS0#_L | |
| FBx_CMD1 | | |
| FBx_CMD2 | ODT_L | |
| FBx_CMD3 | CKE_L | |
| FBx_CMD4 | A14 | A14 |
| FBx_CMD5 | RST | RST |
| FBx_CMD6 | A9 | A9 |
| FBx_CMD7 | A7 | A7 |
| FBx_CMD8 | A2 | A2 |
| FBx_CMD9 | A0 | A0 |
| FBx_CMD10 | A4 | A4 |
| FBx_CMD11 | A1 | A1 |
| FBx_CMD12 | BA0 | BA0 |
| FBx_CMD13 | WE# | WE# |
| FBx_CMD14 | A15 | A15 |
| FBx_CMD15 | CAS# | CAS# |
| FBx_CMD16 | | CS0#_H |
| FBx_CMD17 | | |
| FBx_CMD18 | | ODT_H |
| FBx_CMD19 | | CKE_H |
| FBx_CMD20 | A13 | A13 |
| FBx_CMD21 | A8 | A8 |
| FBx_CMD22 | A6 | A6 |
| FBx_CMD23 | A11 | A11 |
| FBx_CMD24 | A5 | A5 |
| FBx_CMD25 | A3 | A3 |
| FBx_CMD26 | BA2 | BA2 |
| FBx_CMD27 | BA1 | BA1 |
| FBx_CMD28 | A12 | A12 |
| FBx_CMD29 | A10 | A10 |
| FBx_CMD30 | RAS# | RAS# |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

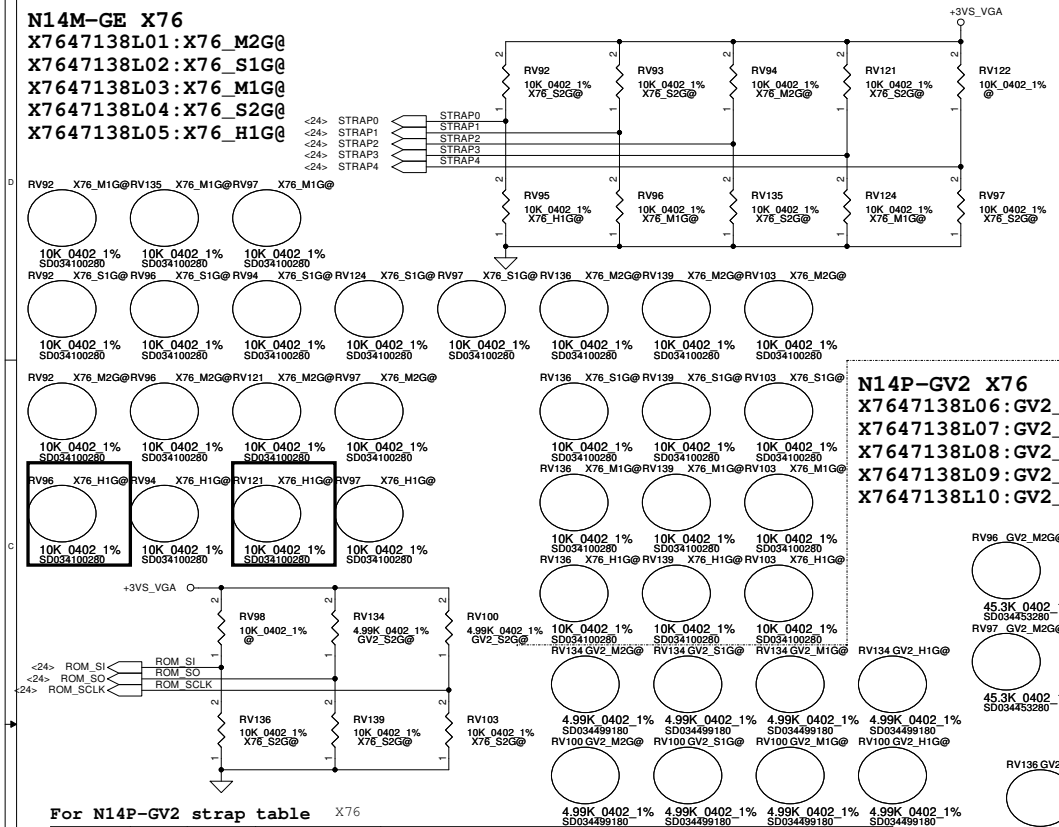
Title: N14X-VRAM C Upper

Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 31 of 63

# N14M-GE X76

X7647138L01:X76_M2G@
X7647138L02:X76_S1G@
X7647138L03:X76_M1G@
X7647138L04:X76_S2G@
X7647138L05:X76_H1G@




## Multi-Level Mode

| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|---|---|---|---|---|---|
| ROM_SCLK | +3VS_VGA | PCI_DEVID[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM |
| ROM_SI | +3VS_VGA | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VS_VGA | FB[1] | FB[0] | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VS_VGA | USER[3] | USER[2] | USER[1] | USER[0] |
| STRAP1 | +3VS_VGA | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] |
| STRAP2 | +3VS_VGA | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] |
| STRAP3 | +3VS_VGA | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| STRAP4 | +3VS_VGA | RESERVED | PCIE_SPEED_ CHANGE_GEN3 | PCIE_MAX_SPEED | DP_PLL_VDD33V |

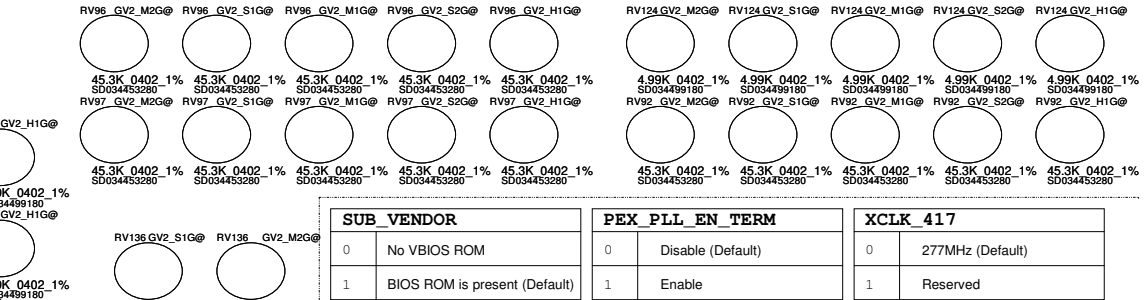
| Resistor Values | Pull-up to +3VS_VGA | Pull-down to Gnd |
|---|---|---|
| 4.99K | 1000 | 0000 |
| 10.0K | 1001 | 0001 |
| 15.0K | 1010 | 0010 |
| 20.0K | 1011 | 0011 |
| 24.9K | 1100 | 0100 |
| 30.1K | 1101 | 0101 |
| 34.8K | 1110 | 0110 |
| 45.3K | 1111 | 0111 |

## Binary-Level Mode

| Physical Strapping pin | Strapping Mapping | Resistance | Polarity |
|---|---|---|---|
| ROM_SCLK | SMB_ALT_ADDR | 10K | PD |
| ROM_SI | SUB_VENDOR | 10K | PU(VBIOS ROM) PD(Non-VBIOS ROM) |
| ROM_SO | VGA_DEVICE | 10K | PD(No display) |
| STRAP0 | RAM_CFG[0] | 10K | PU (Binary=1) PD (Binary=0) |
| STRAP1 | RAM_CFG[1] | 10K | |
| STRAP2 | RAM_CFG[2] | 10K | |
| STRAP3 | RAM_CFG[3] | 10K | |
| STRAP4 | PCIE_MAX_SPEED | 10K | PD |

# N14P-GV2 X76

X7647138L06:GV2_M2G@
X7647138L07:GV2_S1G@
X7647138L08:GV2_M1G@
X7647138L09:GV2_S2G@
X7647138L10:GV2_H1G@




0206 Change R136 from SD034200200 to SD034200280 for GV2_S2G.
0206 Change R136 from SD034249200 to SD034249280 for GV2_H1G.

## For N14P-GV2 strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N14P-GV2 | 1 GHz | 128M* 16* 4 1GB | Samsung K4W2G1646E-BC1A | R PU 45K | R PD 45K | R PD 15K | R PD_5K | R PD 45K | R PD 45K | R PU 5K | R PU 5K |
| N14P-GV2 | 1 GHz | 128M* 16* 4 1GB | Micron MT41J128M16JT-093G:K | R PU 45K | R PD 45K | R PD 15K | R PD_5K | R PD 45K | R PD 30K | R PU 5K | R PU 5K |
| N14P-GV2 | 1 GHz | 128M* 16* 4 1GB | **Hynix H5TC2G63FFR-11C** | R PU 45K | R PD 45K | R PD 15K | R PD_5K | R PD 45K | **R PD 25K** | R PU 5K | R PU 5K |
| N14P-GV2 | 900 MHz | 256M* 16* 4 2GB | Samsung K4W4G1646B-HC11 | R PU 45K | R PD 45K | R PD 15K | R PD_5K | R PD 45K | R PD 20K | R PU 5K | R PU 5K |
| N14P-GV2 | 900 MHz | 256M* 16* 4 2GB | Micron MT41K256M16HA-107G:E | R PU 45K | R PD 45K | R PD 15K | R PD_5K | R PD 45K | R PD 10K | R PU 5K | R PU 5K |

## For N14P-GS strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N14P-GS | 1 GHz | 128M* 16* 8 2GB | Samsung K4W2G1646E-BC1A | R PU 45K | R PD_5K | R PD 20K | R PD_5K | R PD 45K | R PD 45K | R PU 5K | R PD 15K |
| N14P-GS | 1 GHz | 128M* 16* 8 2GB | Micron MT41J128M16JT-093G:K | R PU 45K | R PD_5K | R PD 20K | R PD_5K | R PD 45K | R PD 30K | R PU 5K | R PD 15K |
| N14P-GS | 1 GHz | 128M* 16* 8 2GB | **Hynix H5TC2G63FFR-11C** | R PU 45K | R PD_5K | R PD 20K | R PD_5K | R PD 45K | **R PD 25K** | R PU 5K | R PD 15K |
| N14P-GS | 900 MHz | 256M* 16* 8 4GB | Samsung K4W4G1646B-HC11 | R PU 45K | R PD_5K | R PD 20K | R PD_5K | R PD 45K | R PD 20K | R PU 5K | R PD 15K |
| N14P-GS | 900 MHz | 256M* 16* 8 4GB | Micron MT41K256M16HA-107G:E | R PU 45K | R PD_5K | R PD 20K | R PD_5K | R PD 45K | R PD 10K | R PU 5K | R PD 15K |

## For N14M-GE strap table X76

| GPU | Frenq. | Memory Size | Memory Config | strap0 | strap1 | strap2 | strap3 | strap4 | ROM_SI | ROM_SO | ROM_SCLK |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N14M-GE | 1 GHz | 128M* 16* 4 1GB | Samsung K4W2G1646E-BC1A | R PU 10K | R PD 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 1 GHz | 128M* 16* 4 1GB | Micron MT41J128M16JT-093G:K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 1 GHz | 128M* 16* 4 1GB | **Hynix H5TC2G63FFR-11C** | R PU 10K | R PD 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 900 MHz | 256M* 16* 4 2GB | Samsung K4W4G1646B-HC11 | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |
| N14M-GE | 900 MHz | 256M* 16* 4 2GB | Micron MT41K256M16HA-107G:E | R PU 10K | R PD 10K | R PU 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K | R PD 10K |

## VRAM Part Number

| Frenq. | Memory Size | Samsung K4W2G1646E-BC1A | Micron MT41J128M16JT-093G:K | Hynix H5TC2G63FFR-11C | Samsung K4W4G1646B-HC11 | Micron MT41K256M16HA-107G:E |
|---|---|---|---|---|---|---|
| 1 GHz | 128M* 16* 8 2GB | SA000068U10 | SA000067510 | SA00006H410 | | |
| 900 MHz | 256M* 16* 8 4GB | | | | SA000068R10 | SA000065D20 |

## SUB_VENDOR

| | |
|---|---|
| 0 | No VBIOS ROM |
| 1 | BIOS ROM is present (Default) |

## PEX_PLL_EN_TERM

| | |
|---|---|
| 0 | Disable (Default) |
| 1 | Enable |

## XCLK_417

| | |
|---|---|
| 0 | 277MHz (Default) |
| 1 | Reserved |

## FB_0_BAR_SIZE

| | |
|---|---|
| 0 | Reserved |
| 1 | Reserved |
| 2 | 256MB (Default) |
| 3 | Reserved |

## SLOT_CLK_CFG

| | |
|---|---|
| 0 | GPU and MCH don't share a common reference clock |
| 1 | GPU and MCH share a common reference clock (Default) |

## SMBUS_ALT_ADDR

| | |
|---|---|
| 0 | 0x9E (Default) |
| 1 | 0x9C (Multi-GPU usage) |

## VGA_DEVICE

| | |
|---|---|
| 0 | Non-Primary 3D Acceleration Device (Class Code 302h) |
| 1 | Primary Display or VGA Device (Class Code 300h) |

## USER Straps

| | |
|---|---|
| User[3:0] | |
| 1000-1100 | Customer defined |

## 3GIO_PADCFG

| [3:0] | Description |
|---|---|
| 0110 | Gen 1 / Gen 2 Support only |
| 0000 | Gen 3 Support |

NV update PUN doc for the definition of 3GIO_CONFIG.

## PCI_DEVID

| GPU Type | DEVID[5] | DEVID[4] | DEVID[3] | DEVID[2] | DEVID[1] | DEVID[0] |
|---|---|---|---|---|---|---|
| N14P-GV2 | 0 | 1 | 0 | 0 | 1 | 0 |
| N14P-GS | 1 | 0 | 0 | 0 | 1 | 1 |

| PCIE_SPEED_CHANGE_GEN3 | PCIE_MAX_SPEED |
|---|---|
| N14P-GV2 1 | 1 |
| N14P-GS 1 | 1 |

0: Disable PCIE Gen3 operation 0: Limit to PCIE Gen1
1: Enable PCIE Gen3 operation 1: PCIE Gen 2/3 Capable

## 3GIO_PADCFG[3:0]

| Strap1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] |
|---|---|---|---|---|
| N14P-GV2 | 0 | 1 | 1 | 1 |
| N14P-GS | 0 | 0 | 0 | 0 |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



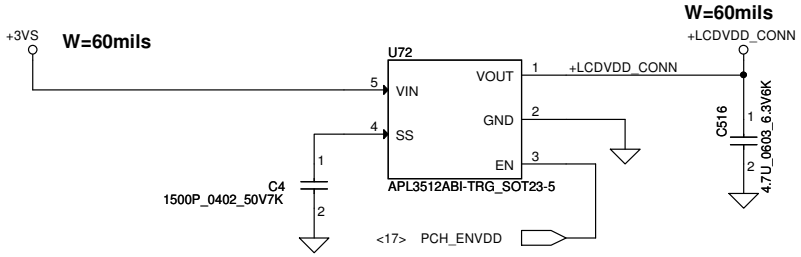
Compal Electronics, Inc.

Title: N14X-MISC

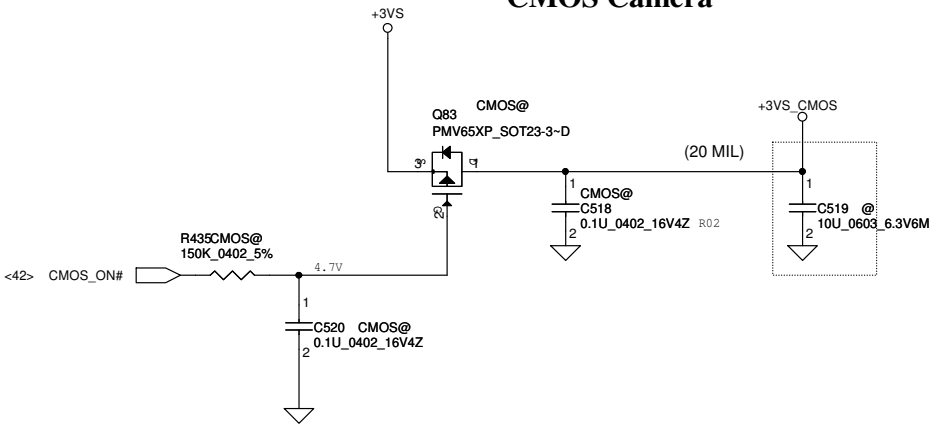
Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 0.3

Date: Wednesday, March 20, 2013 | Sheet 32 of 63

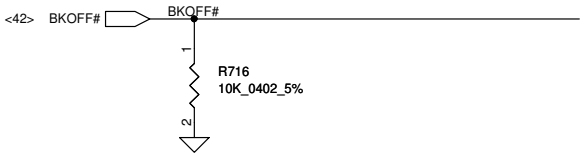
## LCD POWER CIRCUIT

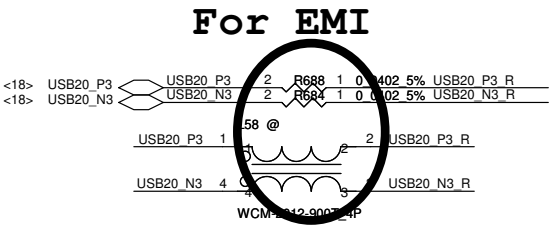



## CMOS Camera

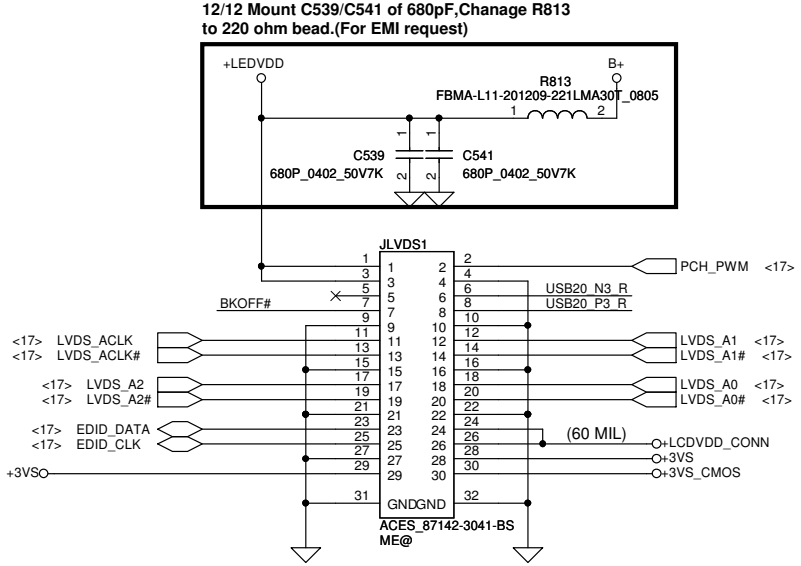



## VGA LCD/PANEL BD. Conn.




12/12 Mount C539/C541 of 680pF,Chanage R813 to 220 ohm bead.(For EMI request)




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

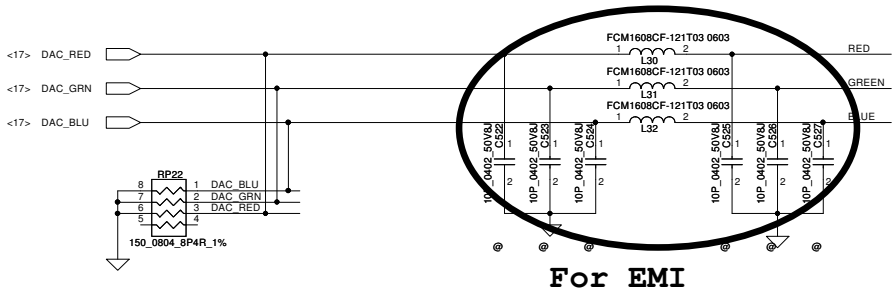


Compal Electronics, Inc.

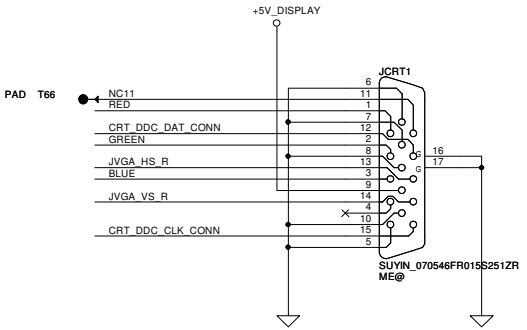
Title: LVDS/CAMERA

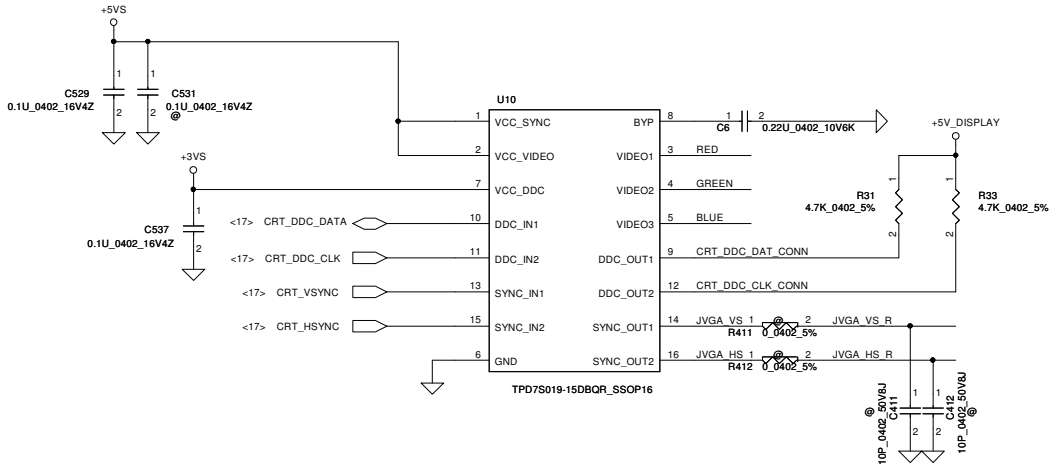
Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 33 of 63




**For EMI**




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

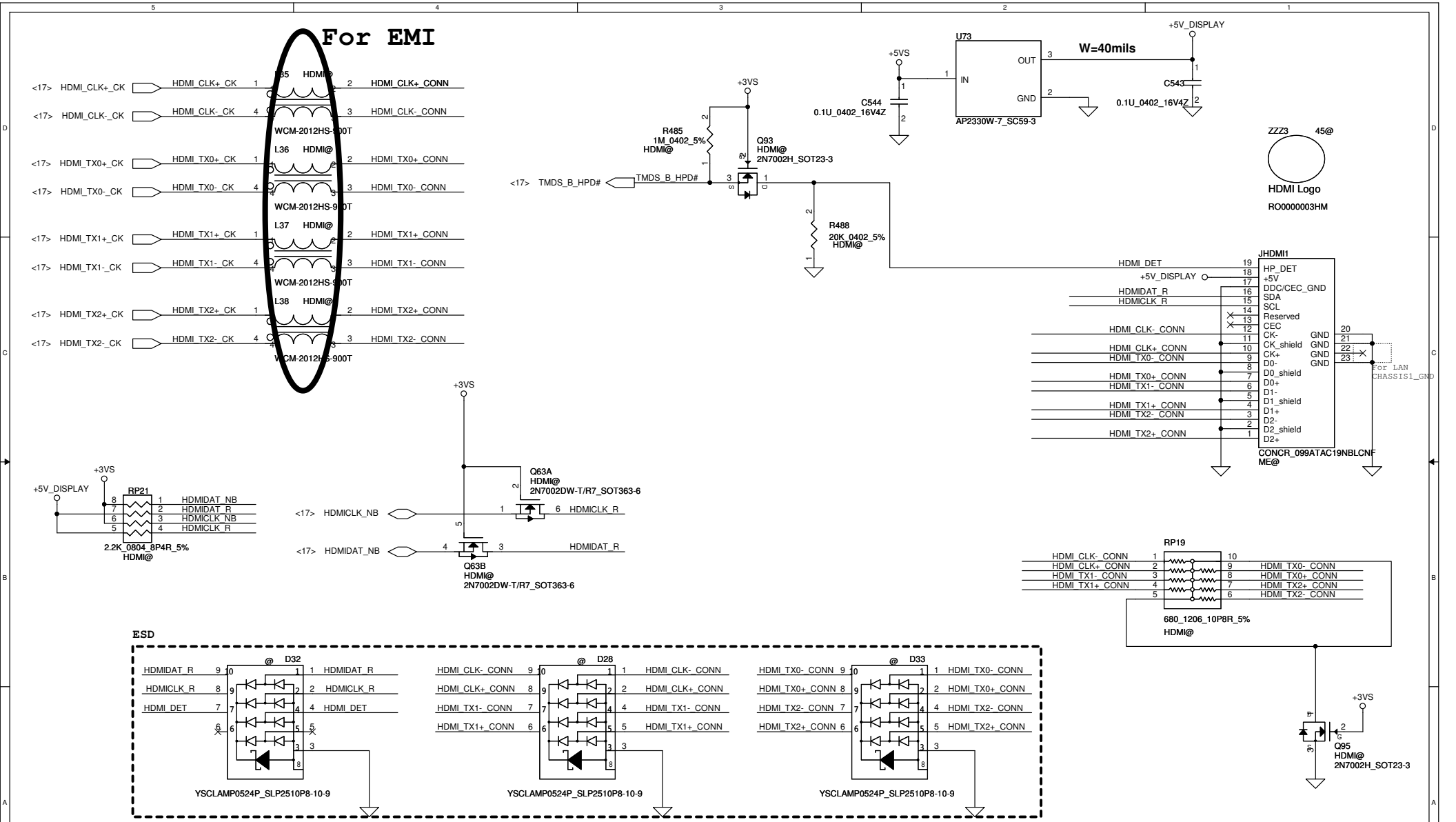


**Compal Electronics, Inc.**

Title: **CRT Connector**

Size: Custom | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 34 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



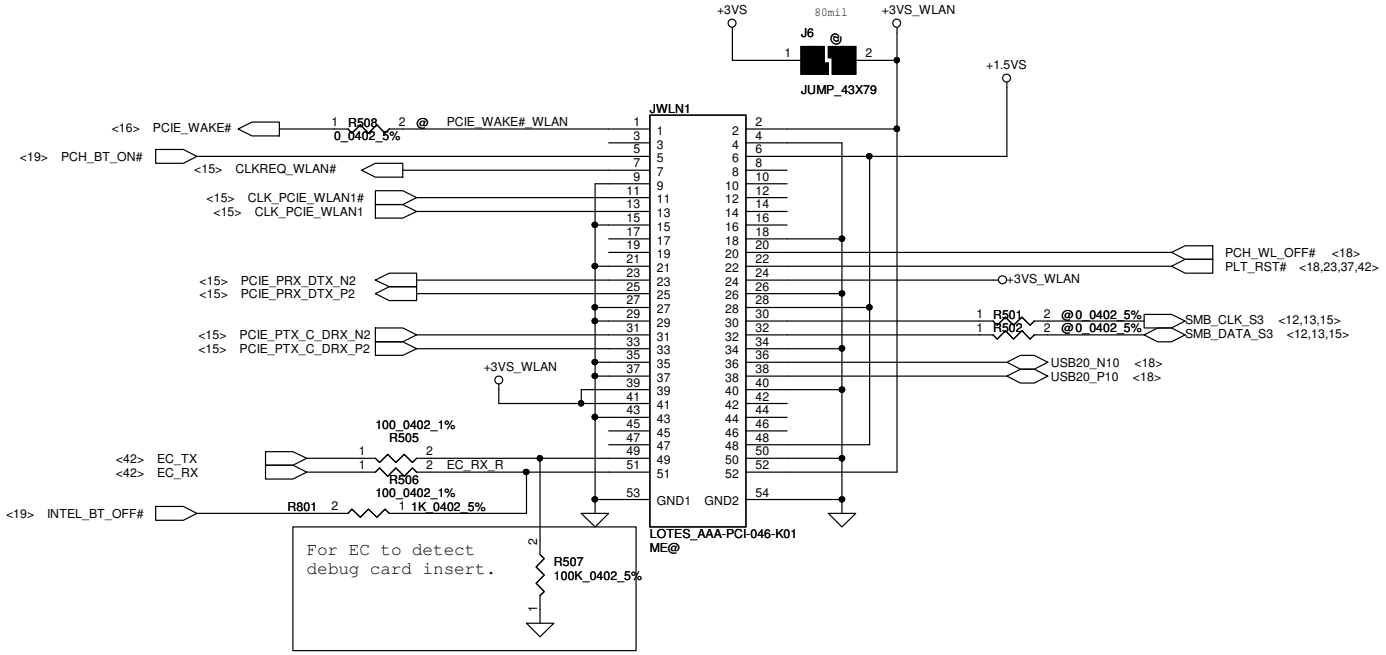
*Compal Electronics, Inc.*

Title: **HDMI CONN**

Size: B | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 35 of 63

# Mini-Express Card for WLAN/WiMAX(Half)




**Reserve for SW mini-pcie debug card.**
**Series resistors closed to KBC side.**

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

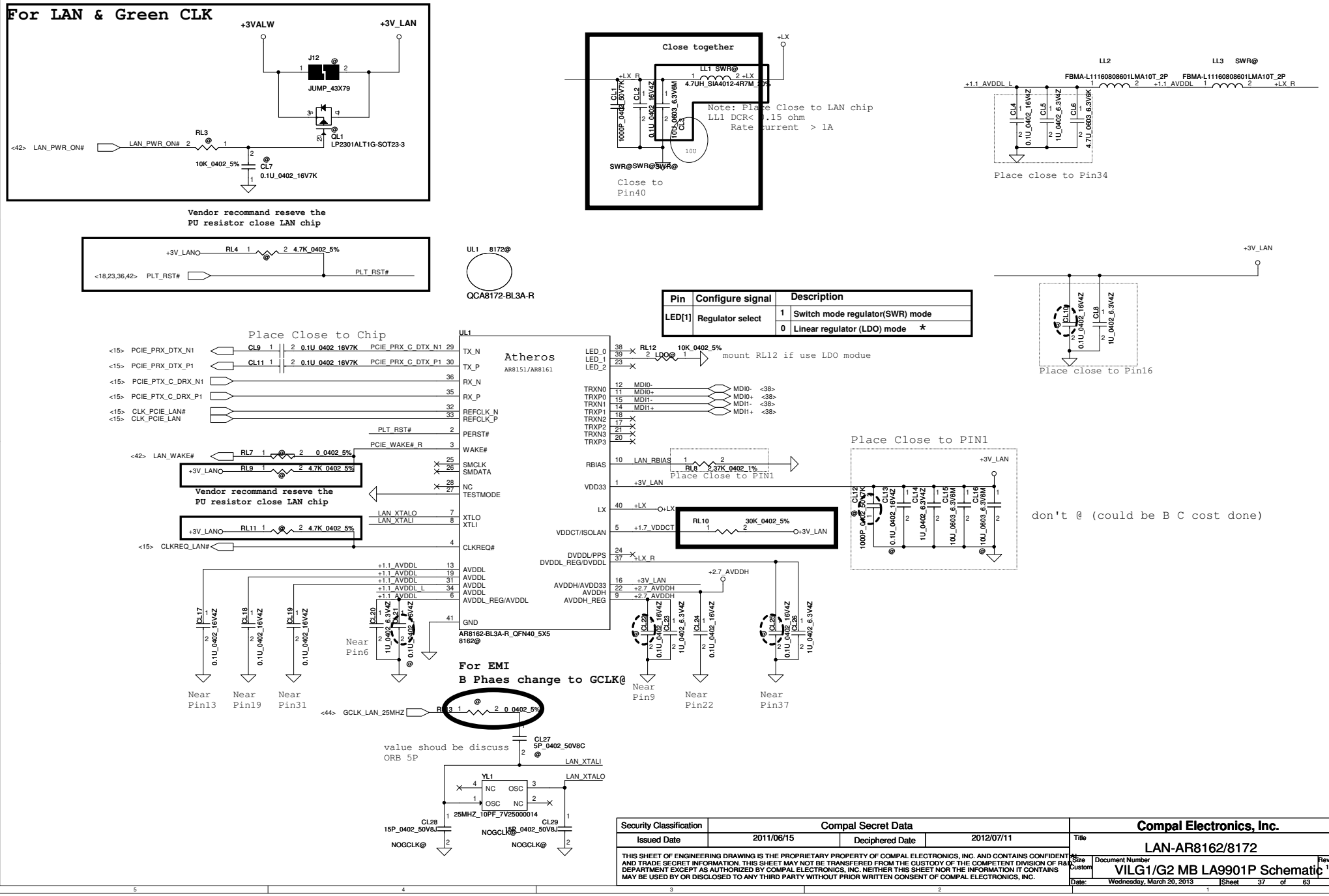


**Compal Electronics, Inc.**

Title: **Mini-Card/NEW Card/SIM**

Size | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 36 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

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**Compal Electronics, Inc.**

Title: LAN-AR8162/8172

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 37 of 63

ESD

Place Close to TL1

DL1
1'S PN:SC300001G00
2'S PN:SC300002E00

@
DL1
AZC099-04S.R7G_SOT23-6

Reserve gas tube for EMI go rural solution

For EMI

CL30
10P_0603_50V

CHASSIS1_GND

DL14
BS4200N-C-LV_SMB-F2
GAS@

Place Close to TL1

TL1
MHPC_NS681612A

<37> MDI0+
<37> MDI0-
<37> MDI1+
<37> MDI1-

For EMI

12/12 Change BOM Structure of CL31 from @ to mount(EMI request)

CL31
0.01U_0402_16V7K

For EMI

CL63
0.1U_0603_50V7K

CHASSIS1_GND

JLAN1
PS_HPKR0125-08A1A0R
ME@

MCT
MDO1-
MDO1+
MDO0-
MDO0+
PR4-
PR4+
PR2-
PR3-
PR3+
PR2+
PR1-
PR1+
SHLD1
SHLD2

CHASSIS1_GND

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



**Compal Electronics, Inc.**

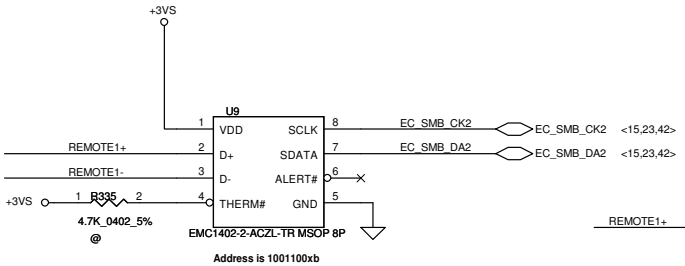
Title: LAN_Transformer

Size: B | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 38 of 63

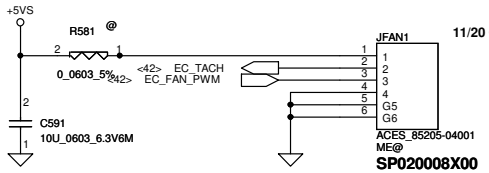
## 2 Channel

### SMSC thermal sensor placed near VRAM




**REMOTE1,2+/-:**
**Trace width/space:10/10 mil**
**Trace length:<8"**

### FAN1 Conn




11/20 Change symbol of JFAN1 to SP020008X00

MINI WLAN VGA CPU

H1 H_3P3 H2 H_3P3 H3 H_3P3 H4 H_3P3 H5 H_3P8 H6 H_3P8 H7 H_3P8

FD1 FD2 FD3 FD4

H14 H_2P8 H15 H_2P8 H19 H_2P8 H20 H_2P8 H21 H_4P6 H22 H_2P8 H23 H_2P8

R

H16 H_3P0X4P0N H17 H_7P0N H24 H_3P0N H25 H_3P0N

E

M/B 橢圓孔 M/B 圓孔

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



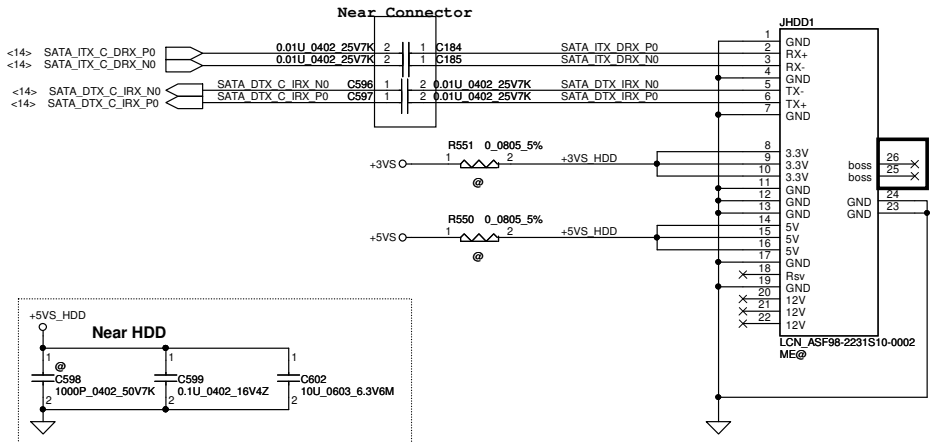
**Compal Electronics, Inc.**

Title: **Fintek-Thermal IC/FAN/screw**

Size: Custom | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 39 of 63

## SATA HDD Conn.

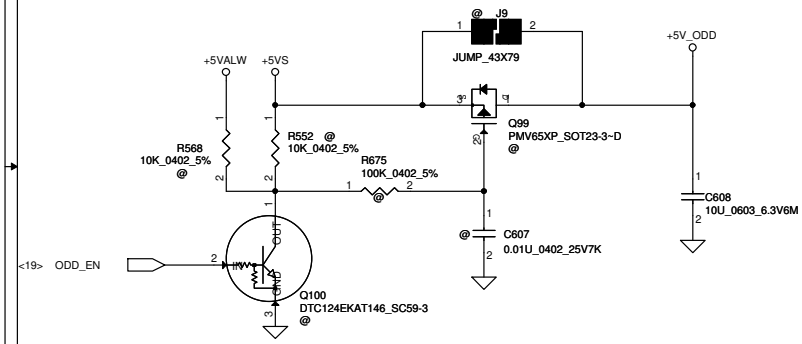






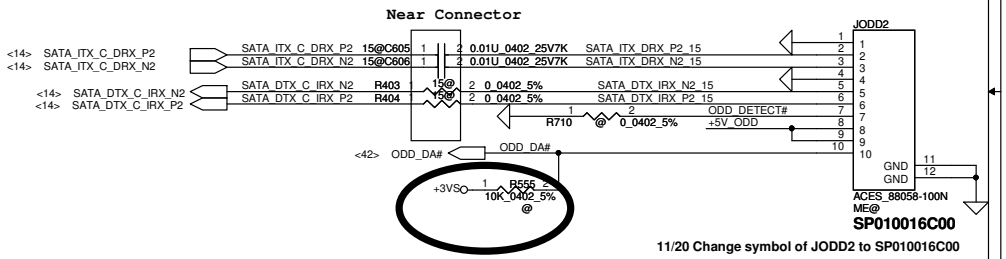
1/16 Change footprint of JHDD1 from SANTA_191501-1_22P to LCN_ASF98-2231S10-0002_22P (DC010005W00 toDC010009C00)

## ODD Power Control




FOR 15"

## SATA ODD FFC Conn.

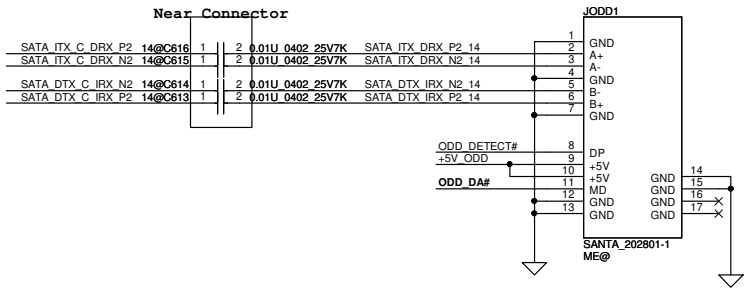



11/20 Change symbol of JODD2 to SP010016C00

Co-lay

FOR 14"

## SATA ODD Conn.

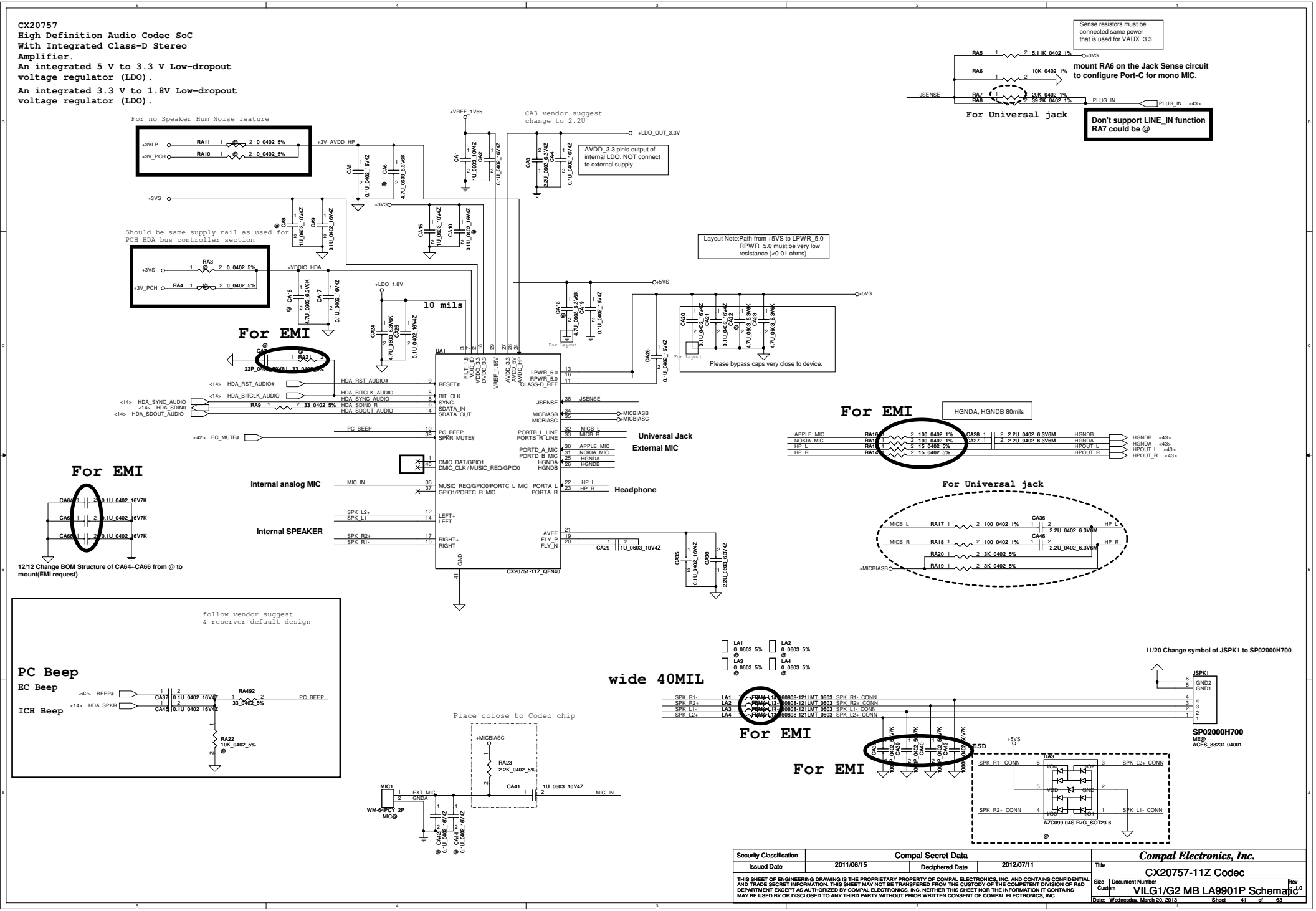



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: HDD/ODD/BT Connector | | | |
| Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | | Rev: 1.0 |
| Date: Wednesday, March 20, 2013 | Sheet 40 of 63 | | |

CX20757
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

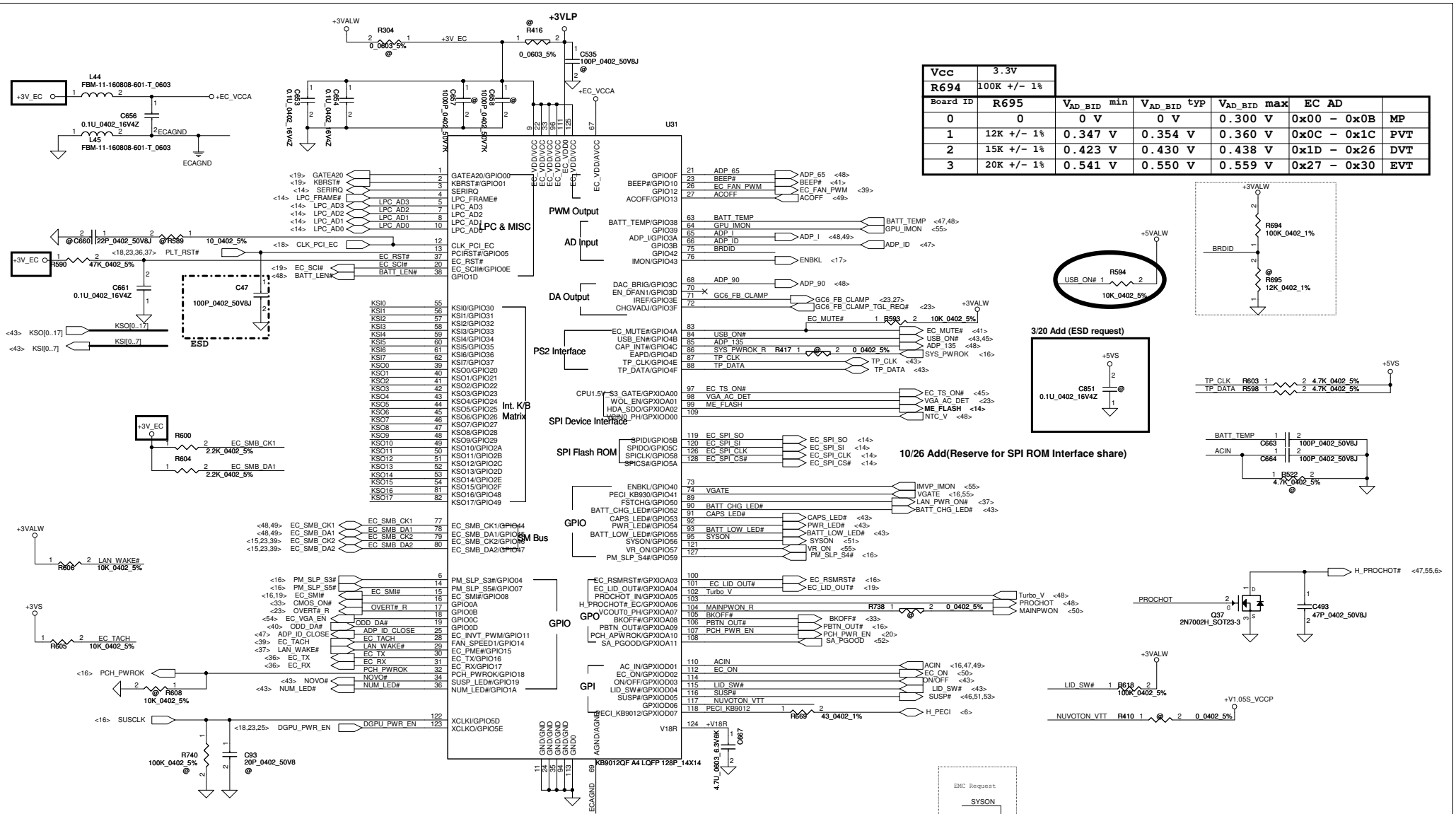


Compal Electronics, Inc.

Title: CX20757-11Z Codec

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 41 of 63




| Vcc | 3.3V | | | | | |
|---|---|---|---|---|---|---|
| R694 | 100K +/- 1% | | | | | |
| Board ID | R695 | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max | EC AD | |
| 0 | 0 | 0 V | 0 V | 0.300 V | 0x00 – 0x0B | MP |
| 1 | 12K +/- 1% | 0.347 V | 0.354 V | 0.360 V | 0x0C – 0x1C | PVT |
| 2 | 15K +/- 1% | 0.423 V | 0.430 V | 0.438 V | 0x1D – 0x26 | DVT |
| 3 | 20K +/- 1% | 0.541 V | 0.550 V | 0.559 V | 0x27 – 0x30 | EVT |

PN : SA00004OB20 S IC KB9012QF A3 LQFP 128P KB CONTROLLER

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



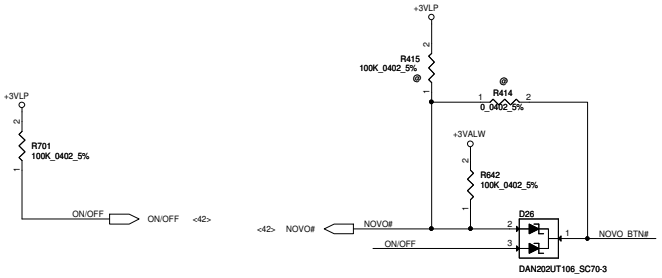
**Compal Electronics, Inc.**

Title: **BIOS & EC I/O Port**

Size: Custom | Document Number: **VILG1/G2 MB LA9901P Schematic** | Rev: 1.0

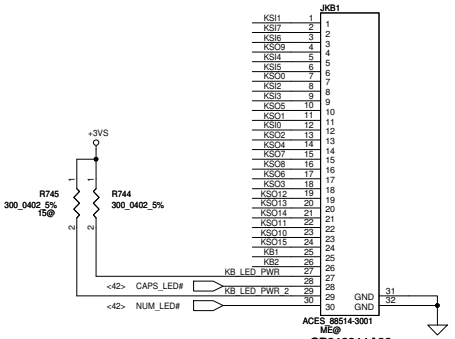
Date: Wednesday, March 20, 2013 | Sheet 42 of 63

## PWR Button For Debug




## Key Board Conn.

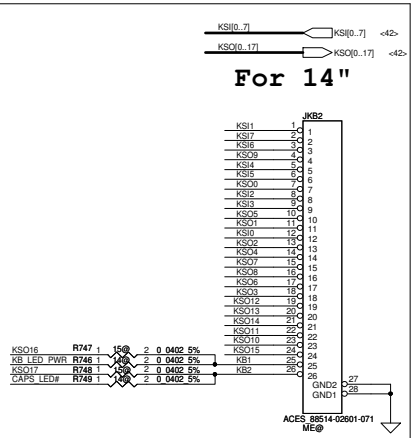
### For 15"




**SP010011A00**

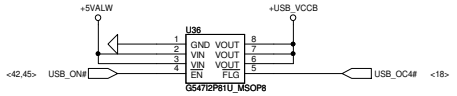
11/20 Change symbol of JKB1 to SP010011A00

### For 14"



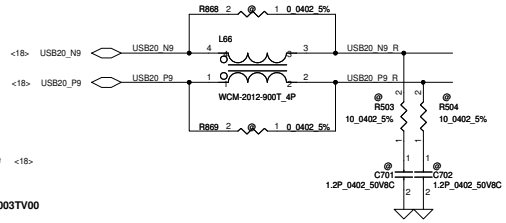

## IO/B Conn.

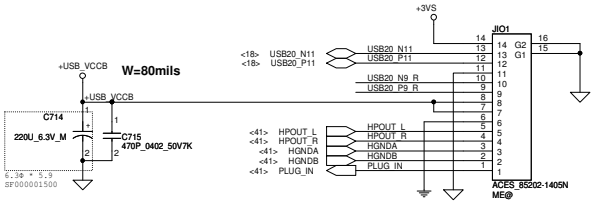
### Ext. USB2.0



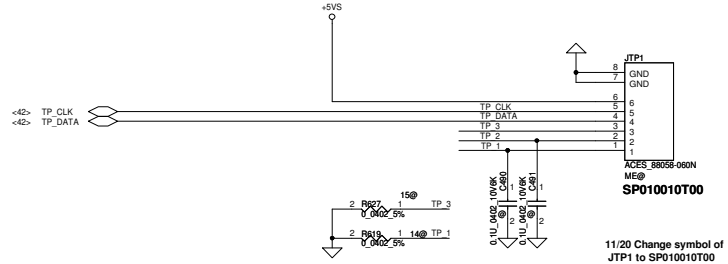

11/30 Change U36 symbol & PN from SA00003XM00 to SA00003TV00

### For EMI



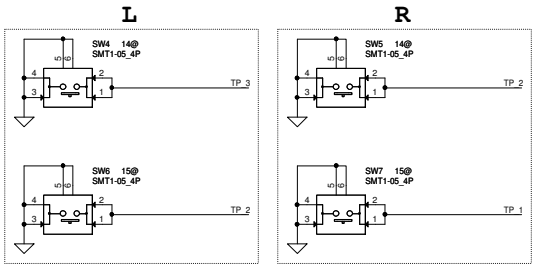




## TP Switch & TP Conn.




**SP010010T00**

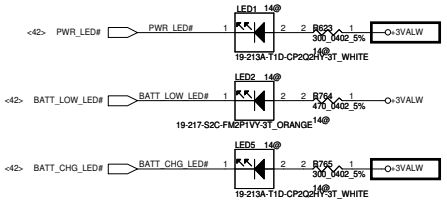
11/20 Change symbol of JTP1 to SP010010T00



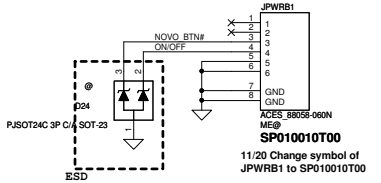

| 15" | |
|---|---|
| 1 | VCC |
| 2 | CLK |
| 3 | DAT |
| 4 | GND |
| 5 | L |
| 6 | R |

| 14" | |
|---|---|
| 1 | VCC |
| 2 | CLK |
| 3 | DAT |
| 4 | L |
| 5 | R |
| 6 | GND |

## LED



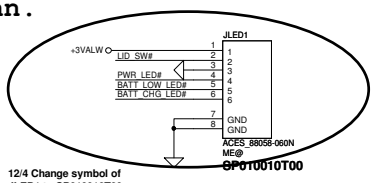

## PWR/B Conn.




**SP010010T00**

11/20 Change symbol of JPWRB1 to SP010010T00

## LED/B Conn.

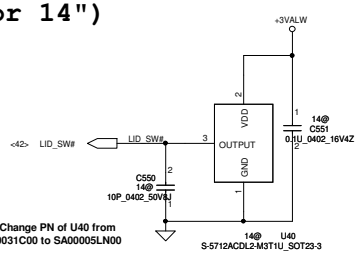



**SP010010T00**

For 15"

12/4 Change symbol of JLED1 to SP010010T00

## Lid SW(For 14")




11/30 Change PN of U40 from SA000031C00 to SA00005LN00

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | ROM/KBD/PWR/CR/LED/TP Conn. | | |
| Size C | Document Number VILG1/G2 MB LA9901P Schematic | | Rev 1.0 |
| Date: Wednesday, March 20, 2013 | | Sheet 43 of 63 | |

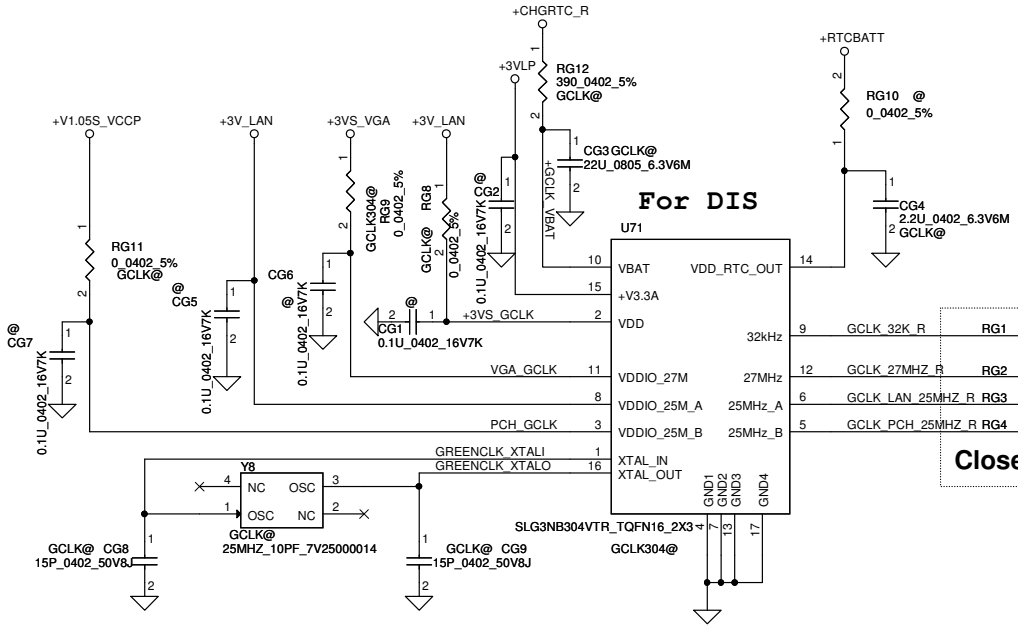
**For UMA**

U71 GCLK244@

SLG3NB244VTR_TQFN16_2X3

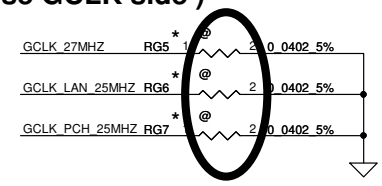
**Every power trace need:**
**W=20mils**

**For GreenCLK generate CLK:**
**Mount: All parts in this page except Swing Level RES (Marked "*")**
**NA: PD108,**
**Y1,R98,C180,C181,**
**Y2,R169,C196,C197,**
**Y6,C968,C969**



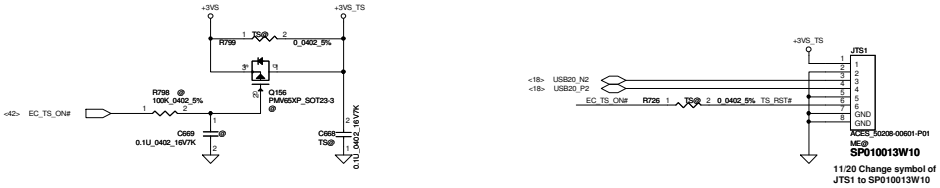

**PCH_32.768K**
**NV_GPU**
**LAN**
**PCH_25M**

**Reserved for Swing Level adjustment**
**( Close GCLK side )**

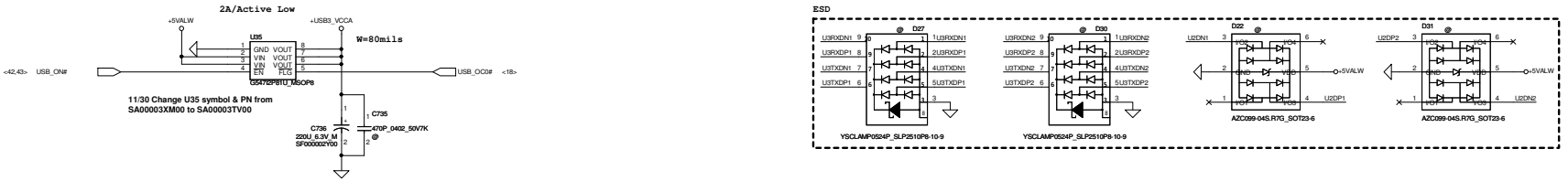


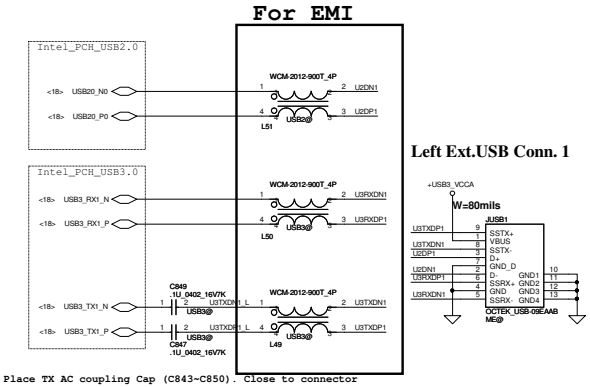

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2011/06/15 | Deciphered Date 2012/07/11 | Title: USB ext. ports |
| | | | Size: B; Document Number: VILG1/G2 MB LA9901P Schematic; Rev: 1.0 |
| | | | Date: Wednesday, March 20, 2013; Sheet 44 of 63 |

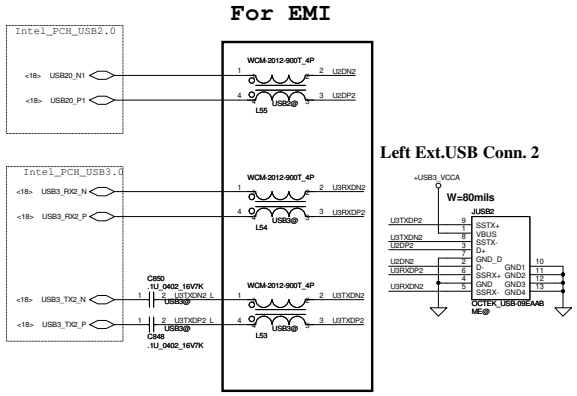
# Touch Screen




# USB3.0




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



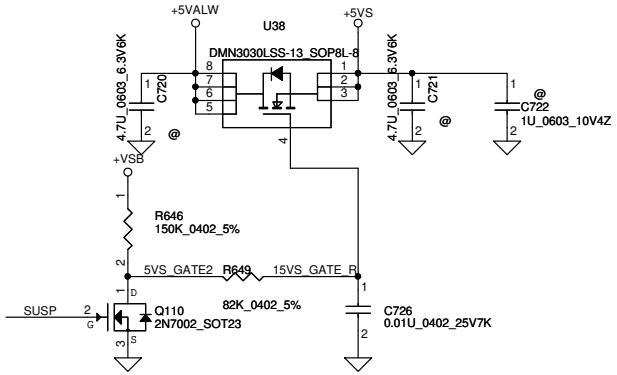
Compal Electronics, Inc.

Title: *USB3.0/Left USB Ports*

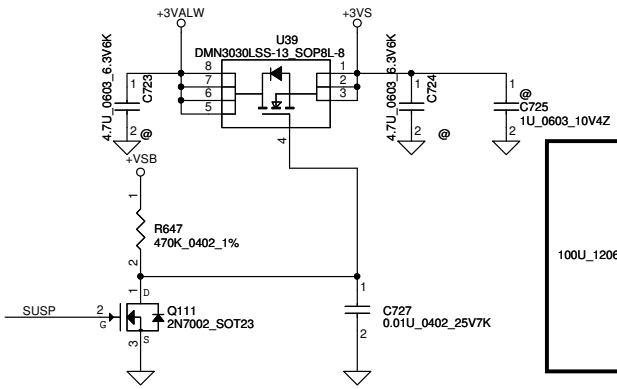
Size: Document Number: VILG1/G2 MB LA9901P Schematic — Rev: 1.0

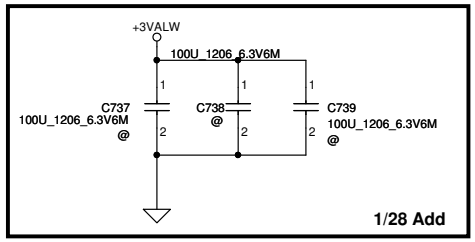
Date: Wednesday, March 20, 2013 — Sheet 45 of 63

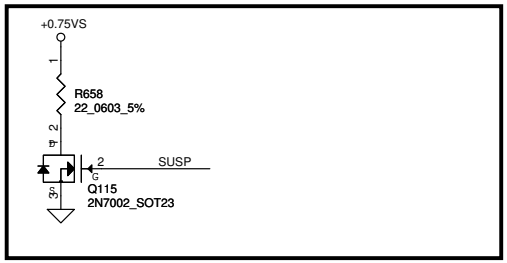
## +5VALW to +5VS




## +3VALW to +3VS

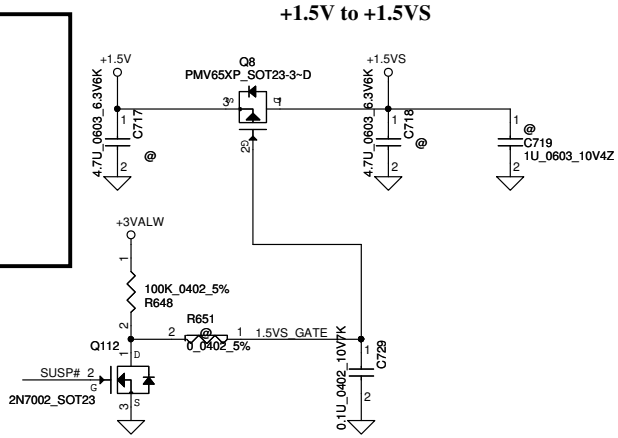


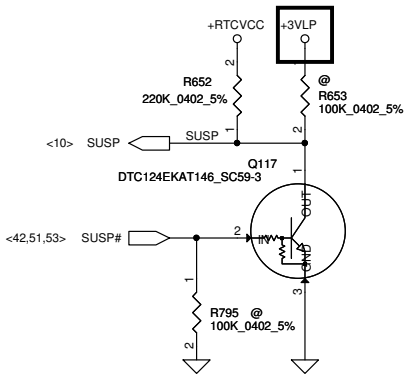




For Intel S3 Power Reduction.

## +1.5V to +1.5VS




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

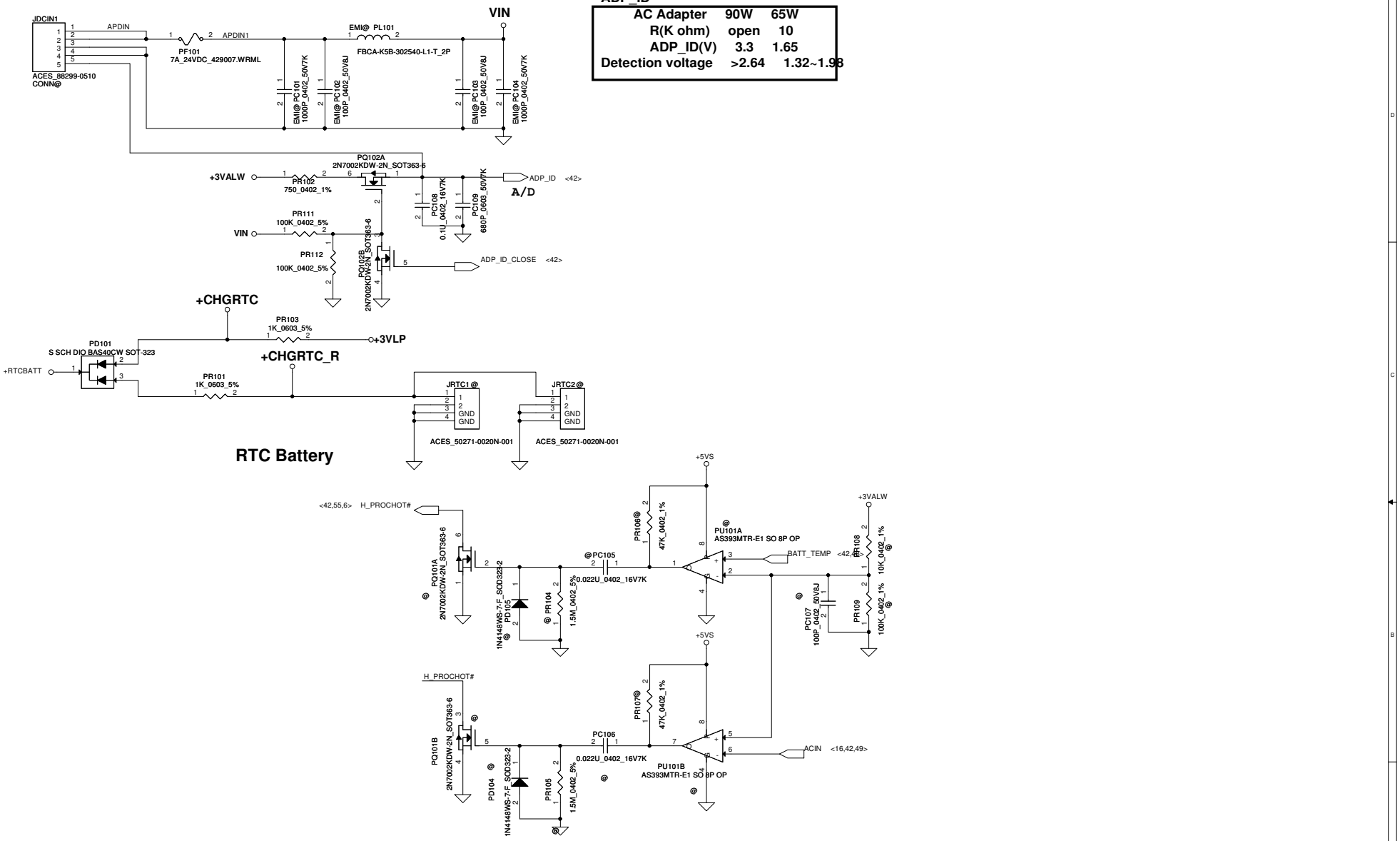


**Compal Electronics, Inc.**

Title: DC Interface

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 46 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

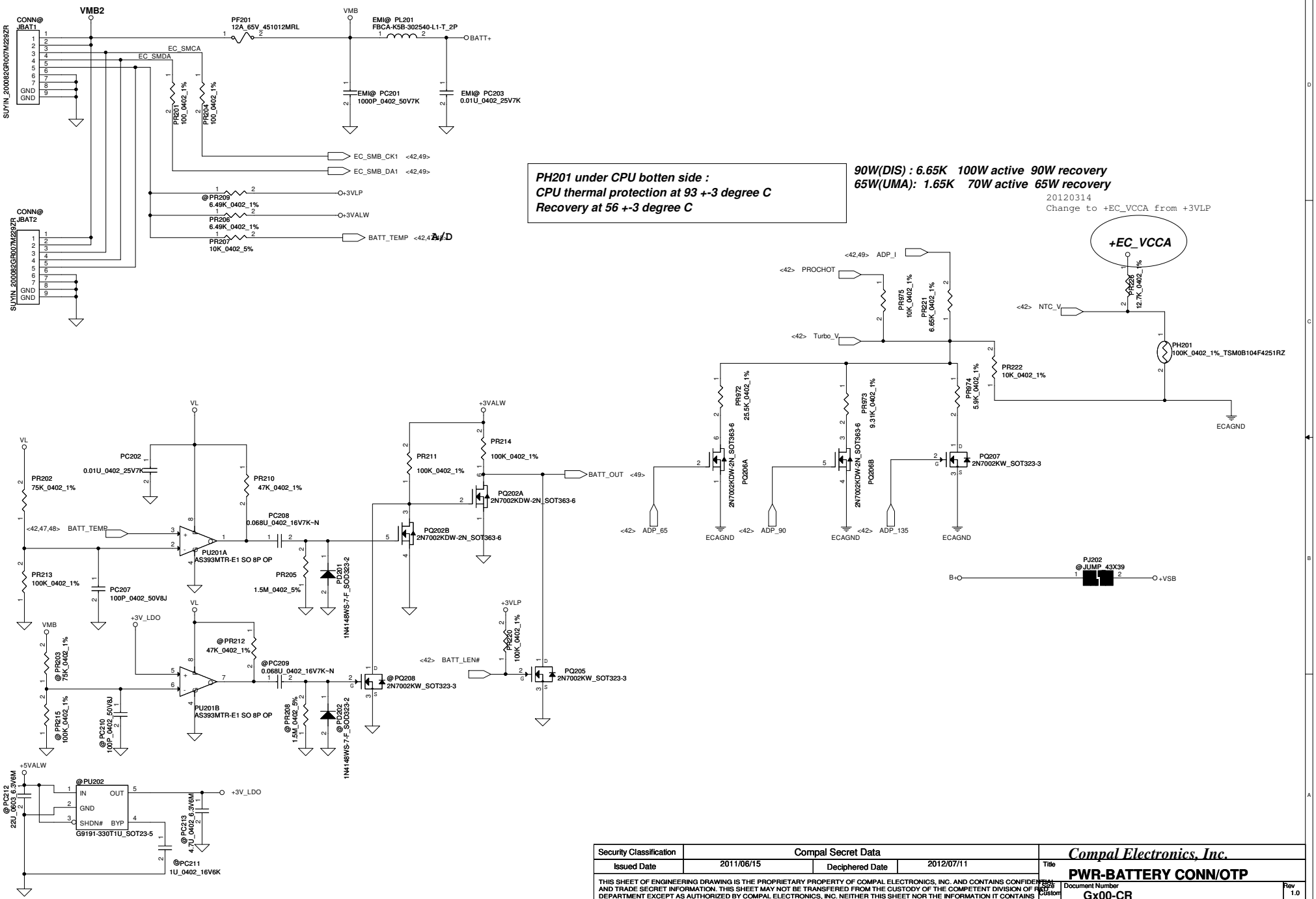


Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

| Size | Document Number | Rev |
|---|---|---|
| Custom | Gx00 | 1.0 |

Date: Wednesday, March 20, 2013 Sheet 47 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

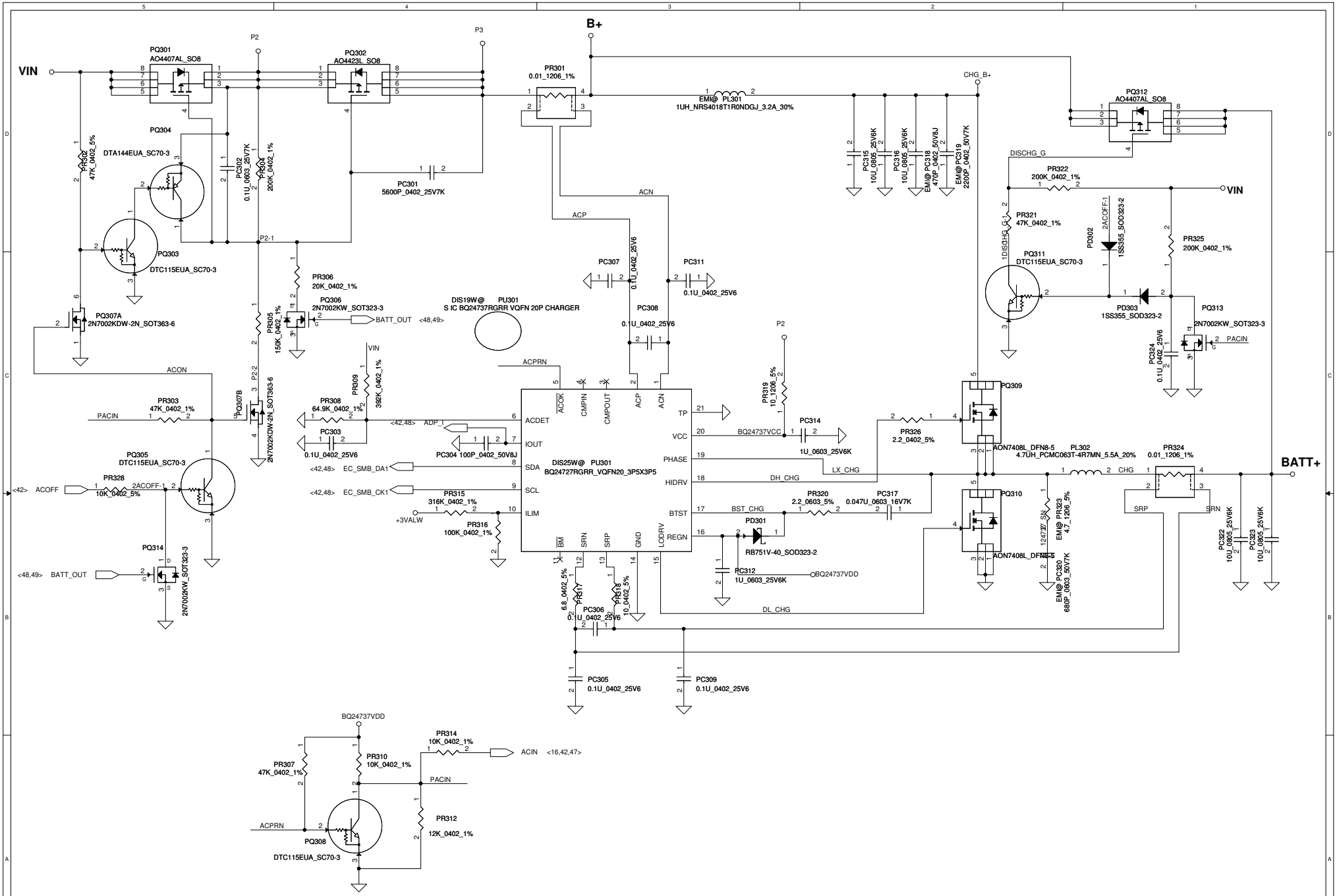


Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 48 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

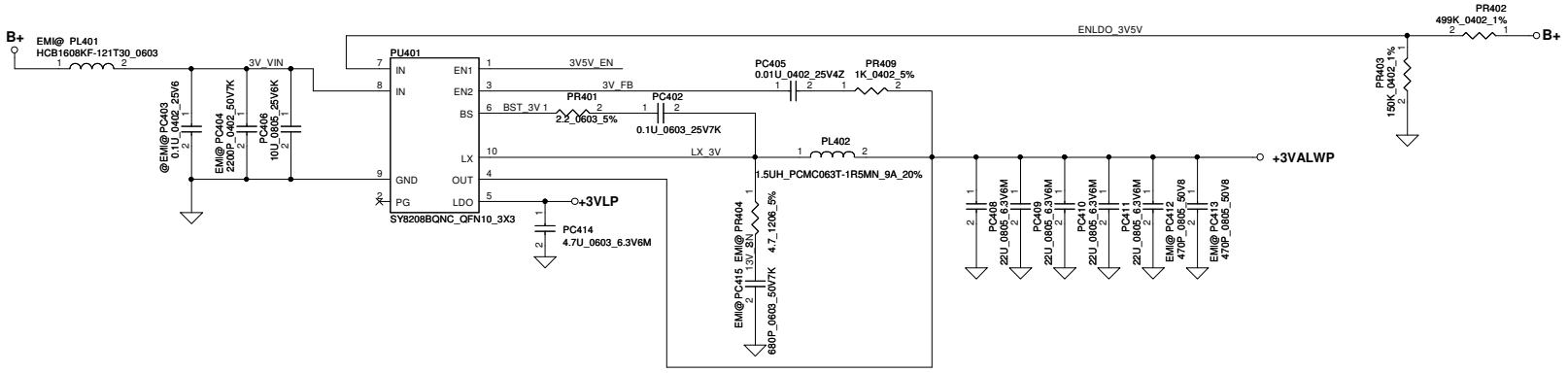


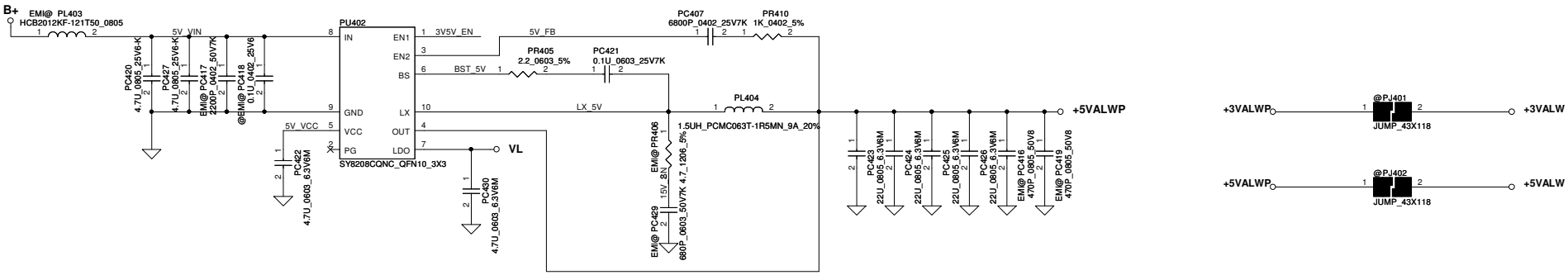
**Compal Electronics, Inc.**

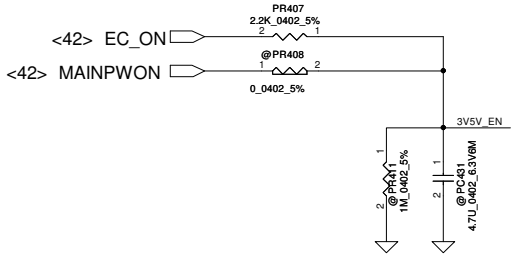
Title: **CHARGER**

| Size | Document Number | Rev |
|---|---|---|
| | Gx00-CR | 1.0 |

Date: Wednesday, March 20, 2013 | Sheet 49 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



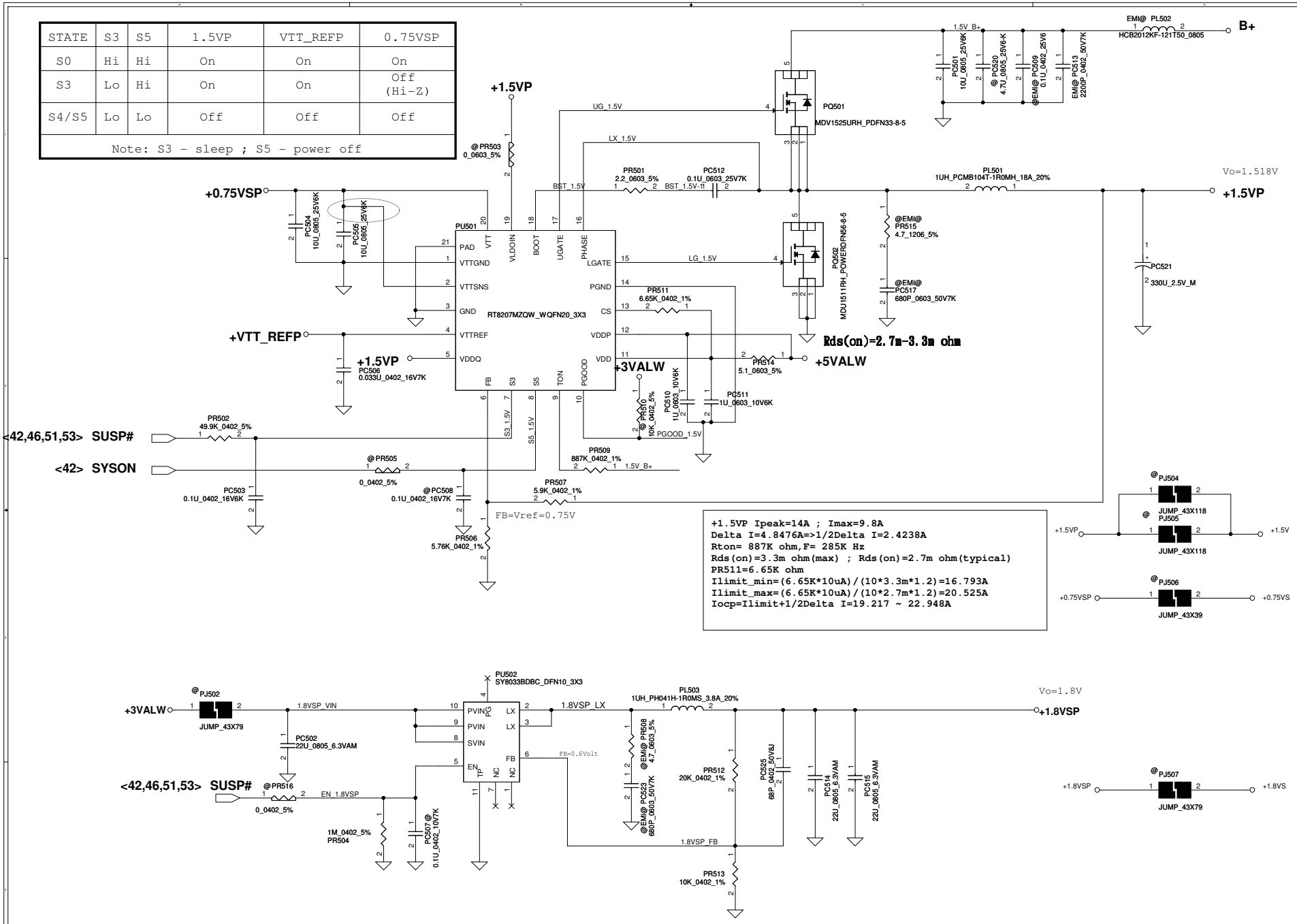
Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 50 of 63

| STATE | S3 | S5 | 1.5VP | VTT_REFP | 0.75VSP |
|---|---|---|---|---|---|
| S0 | Hi | Hi | On | On | On |
| S3 | Lo | Hi | On | On | Off (Hi-Z) |
| S4/S5 | Lo | Lo | Off | Off | Off |
| Note: S3 - sleep ; S5 - power off | | | | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

Title: +1.5VP/+1.8VSP

| Size | Document Number | Rev |
|---|---|---|
| Custom | Gx00-CR | 1.0 |

Date: Wednesday, March 20, 2013 | Sheet 51 of 63

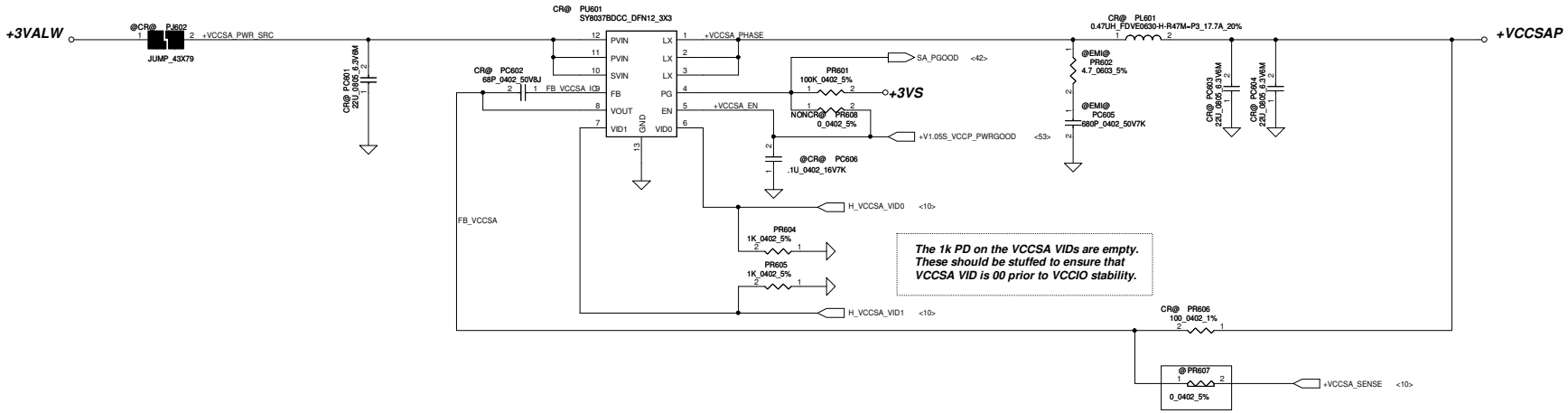
| VID [0] | VID[1] | VCCSA Vout |
|---|---|---|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.8V |
| 1 | 0 | 0.725V |
| 1 | 1 | 0.675V |

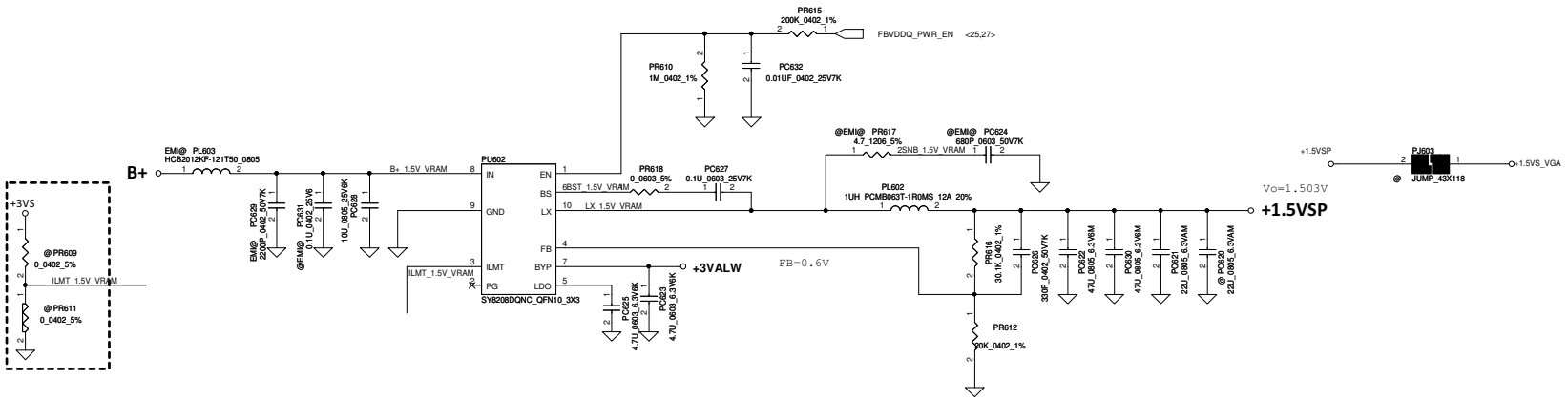
output voltage adjustable network

+V1.05S_VCCP — NONCR@ PR603 0.001_1206_1% — +VCCSA

+VCCSAP — @CR@ PJ601 JUMP_43X118 — +VCCSA

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
OVP 1.06V




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

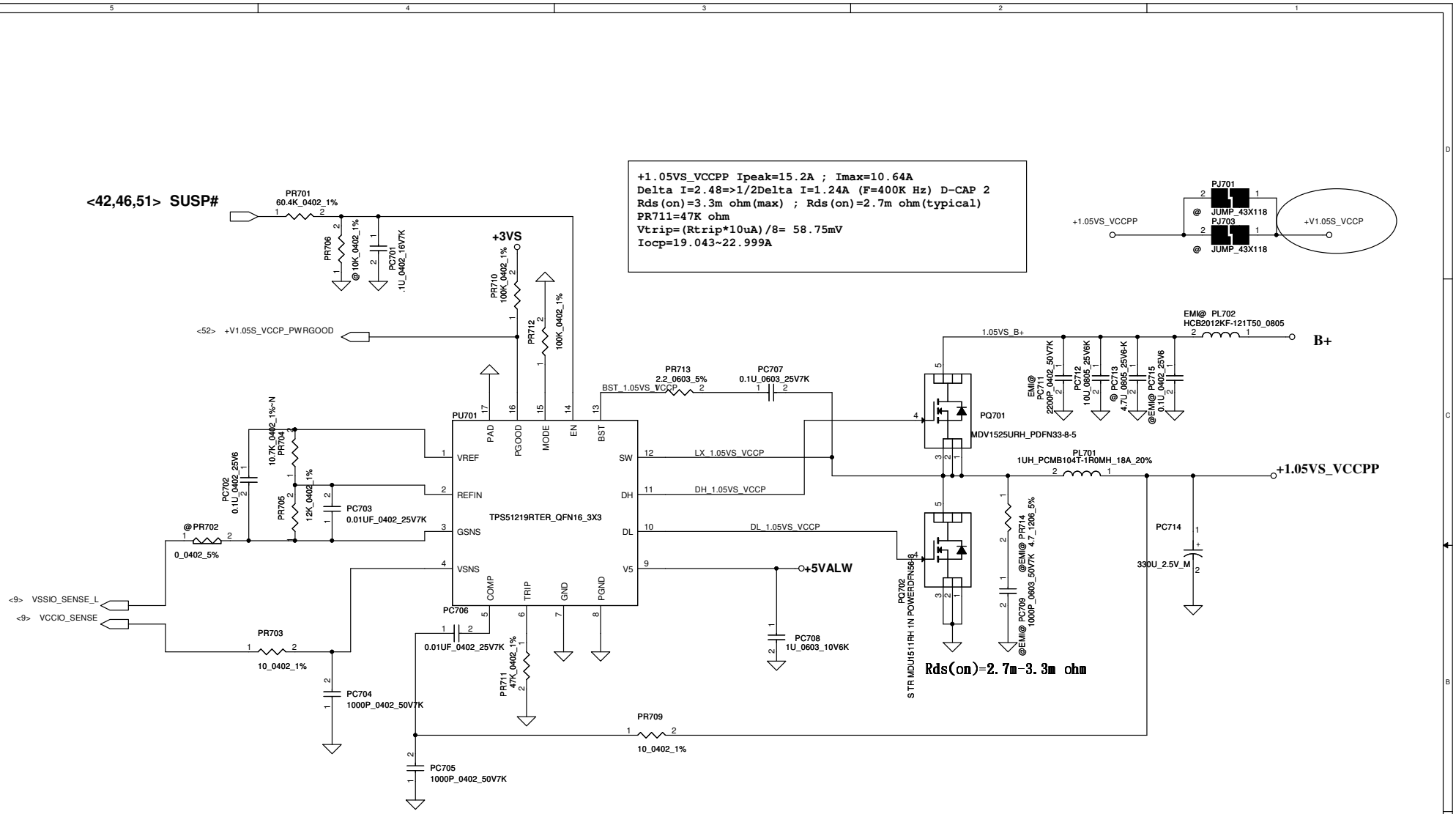


Compal Electronics, Inc.

Title: +VCCSAP/+1.5VSP(VRAM)

Size: C | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 52 of 63




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Title: **+1.05VS_VCCP**

| Size | Document Number | Rev |
|---|---|---|
| Custom | | 1.0 |

Date: Wednesday, March 20, 2013 Sheet 53 of 63

| | GSGV2 (25W) | GE (19W) | |
|---|---|---|---|
| PR842 | 20 | 39 | (kohm) |
| PR845 | 20 | 30 | (kohm) |
| PR831 | 2 | 3 | (kohm) |
| PR816 | 18 | 24 | (kohm) |
| PR832 | 0 | 3 | (kohm) |
| PC863 | 2.7 | 1.8 | (nF) |

If fix to one phase, PR838 and PR836 must mount.

1phase CCM=>1.2V<PSI<1.8V

Rds(on)=2.6m-3.1m ohm

Rds(on)=2.6m-3.1m ohm

+VGA_CORE Under VGA Core

+VGA_CORE Near VGA Core

PR853=18K ohm, OCP=103A
PR853=15K ohm, OCP=83A
PR853=12K ohm, OCP=63A

PR822=499K ohm, F=300Khz
PR822=360K ohm, F=450Khz

RT8813AGQW_WQFN24_4X4

DCR: 0.98m ±5% ohm

DCR: 0.98m ±5% ohm

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

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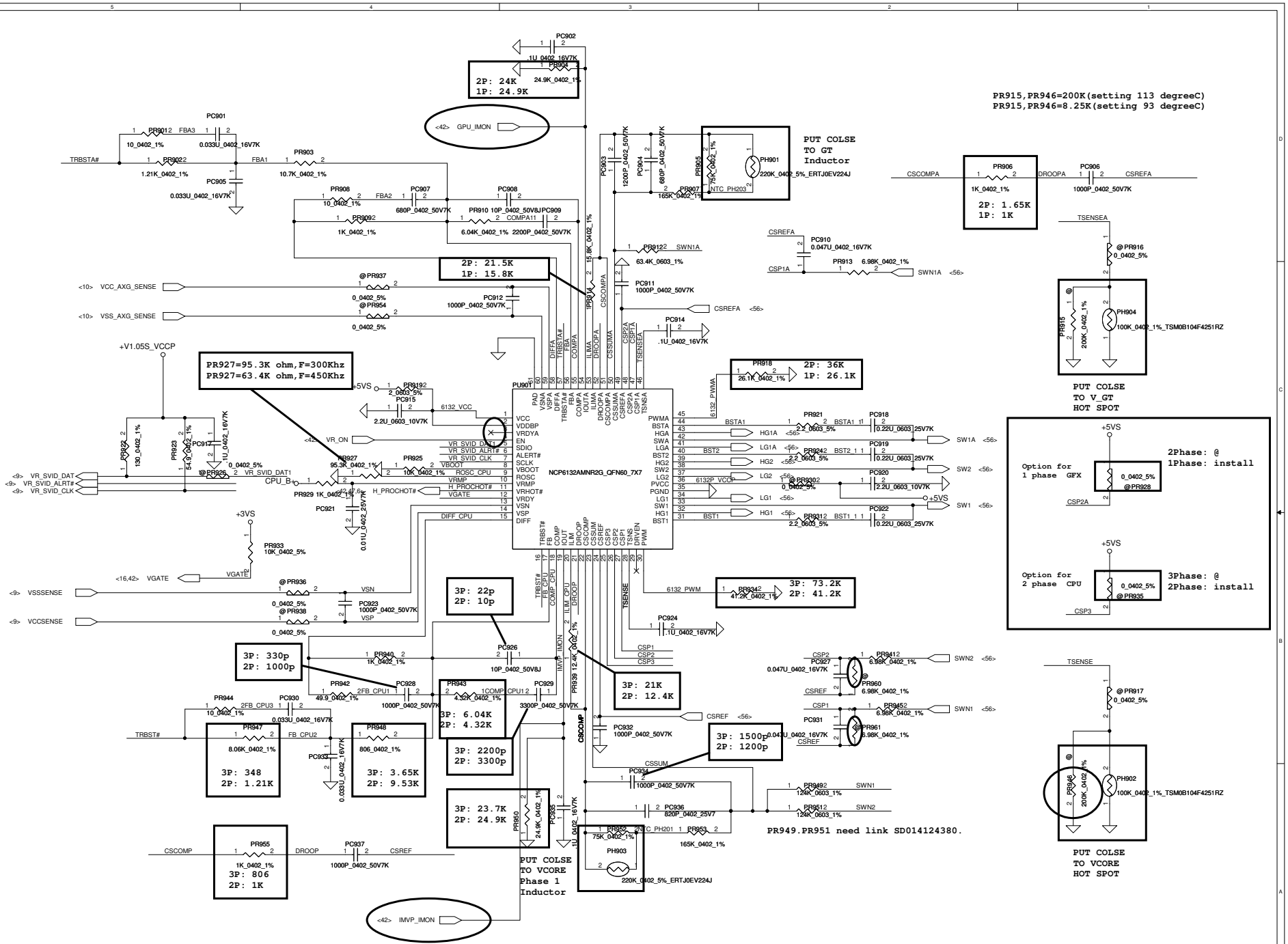
Compal Electronics, Inc.

Title: VGA_CORE

Size: C | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 54 of 63




| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

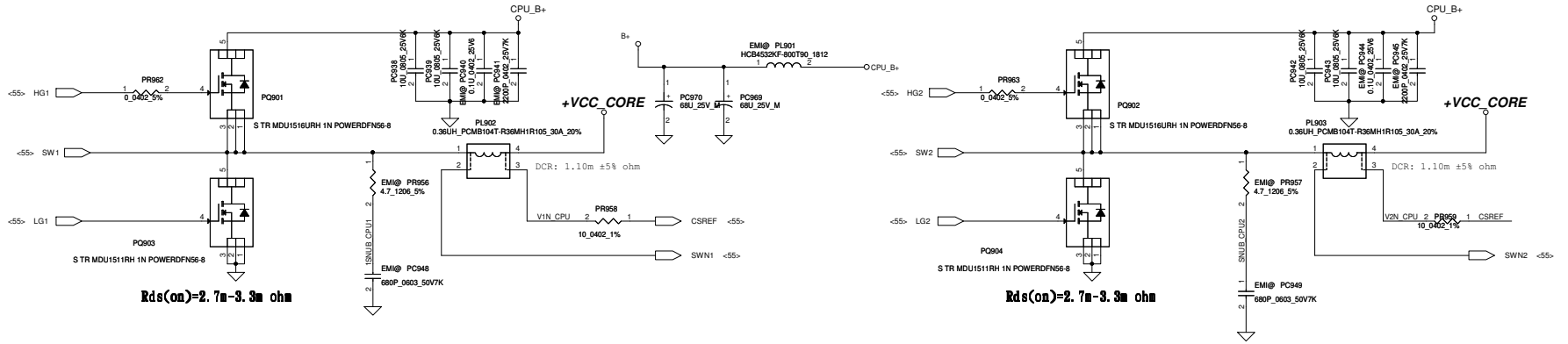


Compal Electronics, Inc.

Title: PWR-CPU_CORE

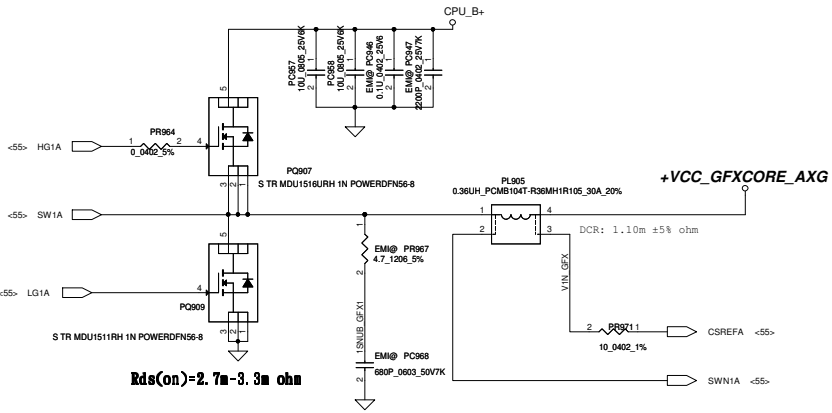
Size: Custom | Document Number: Gx00-CR | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 55 of 63




**QC 45W CPU**
**VID1=0.9V**
**IccMax=94A**
**Icc_Dyn=66A**
**Icc_TDC=52A**
**R_LL=1.9m ohm**
**OCP~110A**

**DC 35W CPU**
**VID1=1.05V**
**IccMax=53A**
**Icc_Dyn=43A**
**Icc_TDC=36A**
**R_LL=1.9m ohm**
**OCP~65A**




**QC 45W GT2**
**VID1=1.23V**
**IccMax=46A**
**Icc_Dyn=37A**
**Icc_TDC=38A**
**R_LL=3.9m ohm**
**OCP~55A**

**DC 35W GT2**
**VID1=1.23V**
**IccMax=33A**
**Icc_Dyn=20.2A**
**Icc_TDC=21.5A**
**R_LL=3.9m ohm**
**OCP~40A**

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |

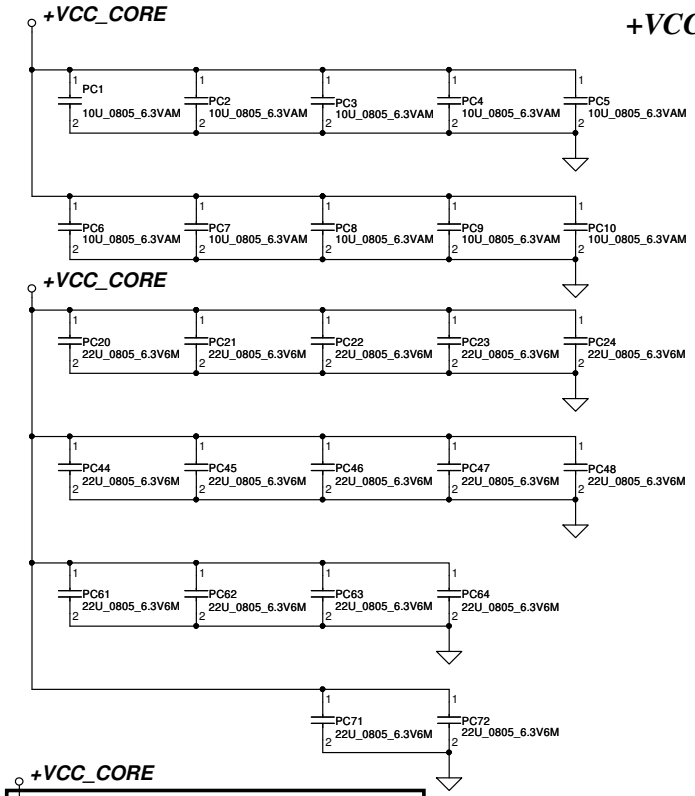


*Compal Electronics, Inc.*

Title: ***PWR-CPU_CORE***

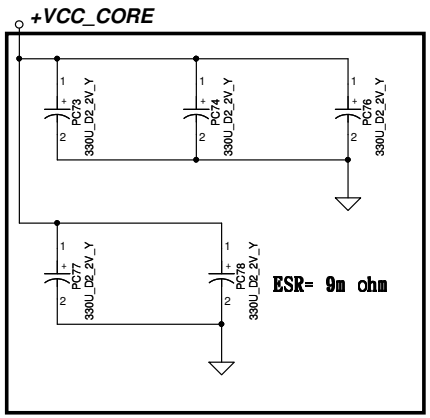
| Size | Document Number | Rev |
|---|---|---|
| C | Gx00-CR | 1.0 |

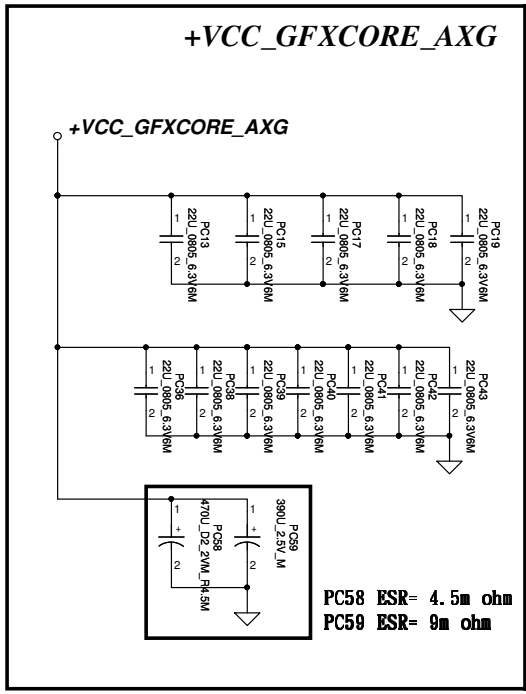
Date: Wednesday, March 20, 2013 Sheet 56 of 63





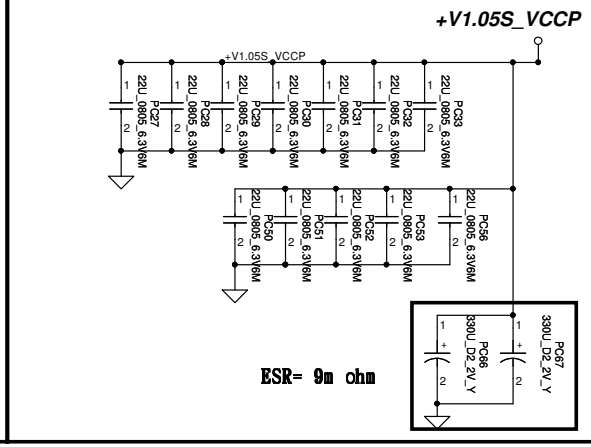





Below is 458544_CRV_PDDG_0.5 Table 5-8.

| | |
|---|---|
| Socket Bottom | 5 x 22 µF (0805)<br>5 x (0805) no-stuff sites |
| Socket Top | 7 x 22 µF (0805)<br>2 x (0805) no-stuff sites |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

| Size | Document Number | Rev |
|---|---|---|
| | LA-9631P | 1.0 |

Date: Wednesday, March 20, 2013 Sheet 57 of 63

# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | Design Change of IC Package. | 50 | Change PU401 to SA000061M00(S IC SY8208BQNC QFN 10P PWM) | 2012/11/22 | DVT |
| 2 | Design Change of IC Package. | 50 | Change PU402 to SA000061N00(S IC SY8208CQNC QFN 10P PWM) | 2012/11/22 | DVT |
| 3 | Design Change of IC Package. | 52 | Change PU602 to SA000061Q00(S IC SY8208DQNC QFN 10P PWM) | 2012/11/22 | DVT |
| 4 | Add ADP_ID Circuit. | 47 | Add PQ102 to SB00000EO10(S TR 2N7002KDW 2N SOT-363-6 PANJIT)<br>Add PR111.PR112 to SD028100380(S RES 1/16W 100K +-5% 0402) | 2012/12/03 | DVT |
| 5 | Factory lack of material. | 52 | Change PC521 to SF000003H00(S_A-P_CAP 330U 2.5V M 6.3X4.2 LESR16M SL) | 2012/12/06 | DVT |
| 6 | Factory lack of material. | 56 | Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE) | 2012/12/06 | DVT |
| 7 | EMI request adjust +3VALWP/+5VALWP snubber function. | 50 | Change @PR404.@PC415.@PR406.@PC429 to PR404.PC415.PR406.PC429. | 2012/12/06 | DVT |
| 8 | EMI request adjust +3VALWP/+5VALWP boost resistor. | 50 | Change PR401.PR405 to SD013220B80(S RES 1/10W 2.2 +-5% 0603). | 2012/12/06 | DVT |
| 9 | EMI request add bypass capacitor. | 50 | Add PC412.PC413.PC416.PC419 to SE001471J80(S CER CAP 470P 50V J NPO 0805 H0.6) | 2012/12/06 | DVT |
| 10 | EMI request adjust CPU/GFX CORE snubber function. | 56 | Change @PR956.@PC948.@PR957.@PC949.@PR967.@PC968 to PR956.PC948.PR957.PC949.PR967.PC968. | 2012/12/06 | DVT |
| 11 | EMI request adjust bypass capacitor. | 56 | Change @PC940 to PC940. | 2012/12/06 | DVT |
| 12 | EMI request add bypass capacitor. | 56 | Add PC944.PC946 to SE00000G880(S CER CAP 0.1U 25V K X5R 0402)<br>Add PC945.PC947 to SE075222K80(S CER CAP 2200P 25V K X7R 0402) | 2012/12/06 | DVT |
| 13 | Design Change of input capacitor. | 50 | Change PC420 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25)<br>Add PC427 to SE00000OF80(S CER CAP 4.7U 25V K X6S 0805 H1.25) | 2012/12/07 | DVT |
| 14 | Design Change of IC Application. | 50 | Add @PR409.@PR410 to SD028100180(S RES 1/16W 1K +-5% 0402)<br>Add @PC405 to SE075472K80(S CER CAP 4700P 25V K X7R 0402)<br>Add @PC407 to SE075472K80(S CER CAP 0.047U 25V K X7R 0402)<br>Add PR411 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2012/12/10 | DVT |
| 15 | Design Change of IC Application. | 55 | Change PC936 to SE000008980(S CER CAP 820P 25V K X7R 0402)<br>Change PC929 to SE074332K80(S CER CAP 3300P 50V K X7R 0402)<br>Change PC926 to SE071100J80(S CER CAP 10P 50V J NPO 0402)<br>Change PC928 to SE074102K80(S CER CAP 1000P 50V K X7R 0402)<br>Change PR943 to SD00000J280(S RES 1/16W 4.32K +-1% 0402)<br>Change PR949.PR951 to SD014124380(S RES 1/10W 124K +-1% 0603 YAGEO) | 2012/12/17 | DVT |
| 16 | Design Change of CPU/GFX CORE Choke. | 56 | Change PL902.PL903.PL905 to SH00000NM00(S COIL 0.22UH +-20% PCMB104T-R22MS 35A) | 2012/12/21 | DVT |
| 17 | Design Change of VGA CORE(Standby mode Circuit). | 54 | Delete PC864.PQ810.PR802.PR803.PR805 | 2012/12/21 | DVT |
| 18 | Reduction Part Count. | 47 | Delete PR110. | 2013/01/18 | PVT |
| 19 | Reduction Part Count. | 52 | Delete PR603. | 2013/01/18 | PVT |
| 20 | Reduction Part Count. | 54 | Delete PR814.PC849.PR825.PR835.PR850.PD802.PD801. | 2013/01/18 | PVT |



Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: 1.0
Date: Wednesday, March 20, 2013 | Sheet 58 of 63

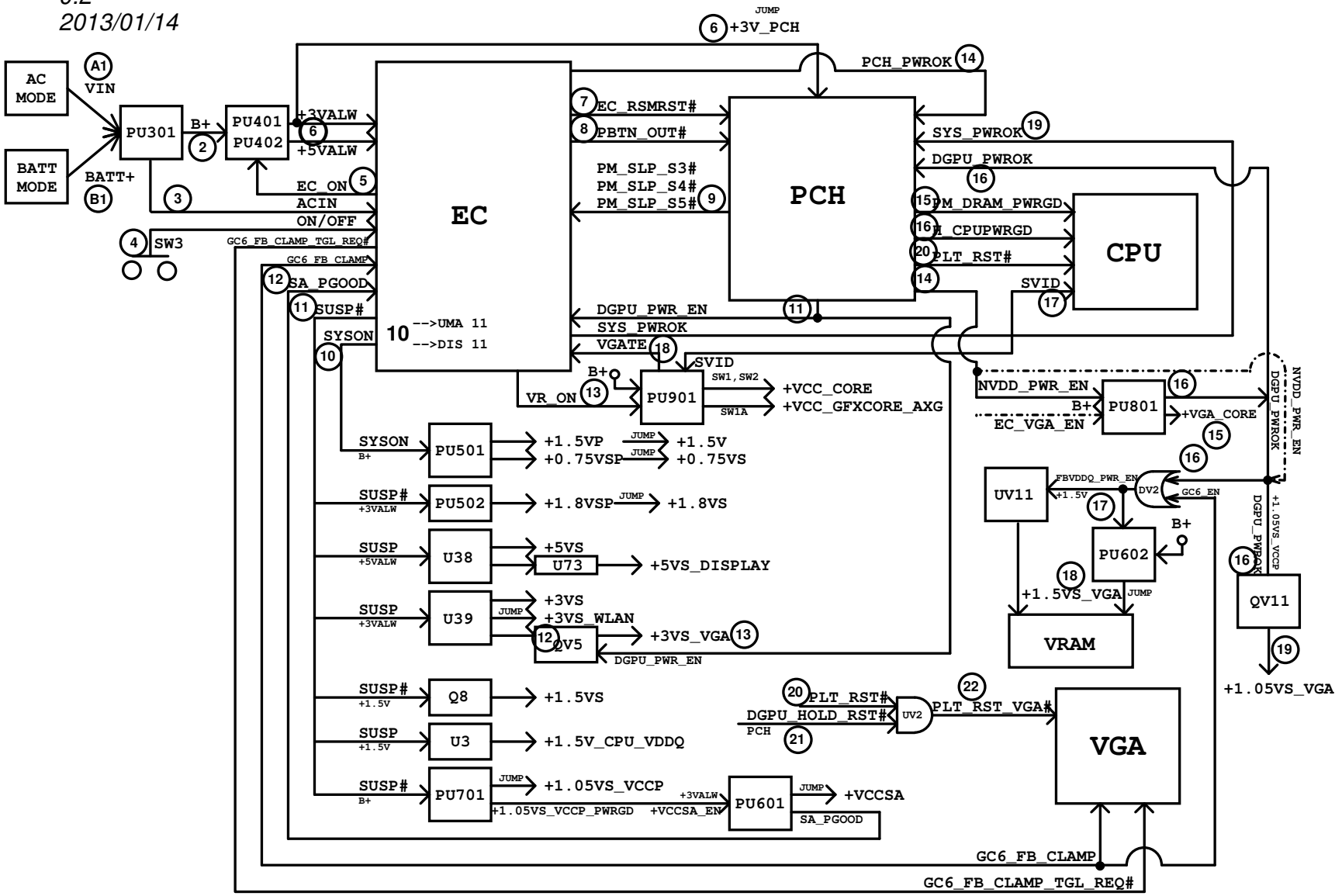
# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 21 | Reduction Part Count. | 55 | Delete PC916. | 2013/01/18 | PVT |
| 22 | Design Change of IC Application. | 50 | Change @PC405.@PR490.@PC407.@PR410 to PC405.PR490.PC407.PR410.<br>Change PR411 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 23 | Reduction Part Count. | 51 | Change PR505.PR516 to SD028000080(S RES 1/16W 0 +-5% 0402)<br>Change PR503 to SD013000080(S RES 1/10W 0 +-5% 0603) | 2013/01/18 | PVT |
| 24 | Design Change of Thermal Application. | 51 | Change PC521 to SGA20331E10(S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9) | 2013/01/18 | PVT |
| 25 | Reduction Part Count. | 52 | Change PR611 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 26 | Reduction Part Count. | 53 | Change PR702 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 27 | Reduction Part Count. | 54 | Change PR823.PR824 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 28 | Reduction Part Count. | 55 | Change PR926.PR916.PR917 to SD028000080(S RES 1/16W 0 +-5% 0402) | 2013/01/18 | PVT |
| 29 | Design Change of CPU/GFX CORE Choke. | 56 | Change PL902.PL903.PL905 to SH00000N900(S COIL .36U PCMB104T-R36MH1R105 30A GLUE) | 2013/01/18 | PVT |
| 30 | Design Change of CPU/GFX CORE Frequence. | 55 | Change PR927 to SD034953280(S RES 1/16W 95.3K +-1% 0402) | 2013/01/18 | PVT |
| 31 | Factory lack of material. | 50 | Change PC420.PC427 to SE000006R80(S CER CAP 4.7U 25V K X5R 0805 H1.25) | 2013/01/18 | PVT |
| 32 | Reduction Part Count. | 50 | Delete PR411. | 2013/01/21 | PVT |
| 33 | Design Change of Power Circuit Application. | 48 | Change PC208 to SE000003J80(S CER CAP 0.068U 16V K X7R 0402) | 2013/01/23 | PVT |
| 34 | Design Change of Power Circuit Application. | 49 | Add PR328 to SD028100280(S RES 1/16W 0 +-5% 0402)<br>Add PR327 to SD028000080(S RES 1/16W 0 +-5% 0402)<br>Add PQ314 to SB000009Q80(S TR 2N7002KW 1N SOT323-3) | 2013/01/23 | PVT |
| 35 | Design Change of Power Circuit Application. | 50 | Change PC405 to SE072103Z80(S CER CAP .01U 25V Z Y5V 0402)<br>Change PC407 to SE075682K80(S CER CAP 6800P 25V K X7R 0402) | 2013/03/04 | PVT |

# COMPAL CONFIDENTIAL

**MODEL NAME:** *Power Sequence Block Diagram*
**PCB NAME:** *LA-9901P*
**REVISION:** *0.2*
**DATE:** *2013/01/14*

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



Title: **Power sequence**

| | | |
|---|---|---|
| Size: Custom | Document Number: VILG1/G2 MB LA-9901P Schematic | Rev: 1.0 |
| Date: Wednesday, March 20, 2013 | Sheet 60 of 63 | |

# VILG1/G2 HW PIR List

| Item | Page | MODIFICATION LIST | PURPOSE | EVT TO DVT |
|---|---|---|---|---|
| 1 | P.5~11 | Change footprint of JCPU1 | For Lenovo rule | |
| 2 | P.14 | Add R406, R407, R408, R409 | Reserve for improvement factory processes | |
| 3 | P.42 | Add EC_SPI_SO, EC_SPI_SI, EC_SPI_CLK, EC_SPI_CS# to EC | Reserve for improvement factory processes | |
| 4 | P.42 | Add PCH_PWR_EN to EC Pin.107 | Reserve for improvement factory processes | |
| 5 | P.42 | Reserve R410 | Reserve Pull-high for GPIO use | |
| 6 | P.42 | Change EC_FAN_PWM from EC Pin.34 to EC Pin.26 | For common design | |
| 7 | P.42 | Change NOVO# from EC Pin.26 to EC Pin.34 | For common design | |
| 8 | P.42 | Change ENBKL from EC Pin.73 to EC Pin.76 | For common design | |
| 9 | P.42 | Change IMVP_IMON from EC Pin.76 to EC Pin.73 | For common design | |
| 10 | P.42 | Change DGPU_PWR_EN from EC Pin.107 to EC Pin.123 | For common design | |
| 11 | P.42 | Change OVERT#_R from EC Pin.117 to EC Pin.17 | For common design | |
| 12 | P.34 | Add R411, R412, C411, C412 | Reserve for EMI | |
| 13 | P.20 | Add Q21, R40, C237, Q22,R418, C243,C252,R413 | Reserve for power consumption | |
| 14 | P.25 | Change RV41 to 1K ohm, CV63 to 1uF | For VGA Sequence | |
| 15 | P.25 | Add QV4/RV42 | For VGA Sequence | |
| 16 | P.25 | Change QV3/UV11 | For VGA Sequence | |
| 17 | P.26 | Change RV241 to 15K ohm | For VGA Sequence | |
| 18 | P.26 | Add QV6 and RV44. | For VGA Sequence | |
| 19 | P.26 | Change QV10/QV11 | For VGA Sequence | |
| 20 | P.43 | Del Q12/R806 | For Change Audio Jack type from Normal close to Normal open | |




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Title: HW-PIR1

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 61 of 63

# VILG1/G2 HW PIR List

| Item | Page | MODIFICATION LIST | PURPOSE |
|---|---|---|---|
| | | | **DVT TO PVT** |
| 1 | P.36 | Reserve R508 | For leakage current issue of Atheros WLAN |
| 2 | P.41 | Change RA22 to reserve | For PC Beep issue(can't heard sound of "di" on BIOS setup menu) |
| 3 | P.41 | Reserve RA10/RA11 | For solve Codec speaker Hum noise issue(Zizi) |
| 4 | P.42 | Reserve R416 | Reserve +3VLP power rail to EC |
| 5 | P.42 | Change EC_RST# power rail to +3V_EC | Using power rail which the same with EC |
| 6 | P.42 | Change EC_SMB_CK1 & EC_SMB_DA1 power rail to +3V_EC | Using power rail which the same with EC |
| 7 | P.14 | Change U5 from 4MB to 8MB ROM | Follow common design |
| | | | **PVT TO Pre-MP** |
| 1 | P.23 | Change RV5 to shortpad | |
| 2 | P.42 | Chagne R416 to shortpad | |
| 3 | P.52 | Reserve +1.05S_VCCP_PWRGOOD of +V1.05S_VCCP to connect to SA_PGOOD | For Celeron/Pentium CPU |

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2011/06/15 | Deciphered Date | 2012/07/11 |



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| Compal Electronics, Inc. | | |
| Title: HW-PIR2 | | |
| Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0 |
| Date: Wednesday, March 20, 2013 | Sheet 62 of 63 | |

## Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 44 | | | | | |
| 45 | | | | | |
| 46 | | | | | |
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Compal Electronics, Inc.

Title: HW-PIR2

Size: Custom | Document Number: VILG1/G2 MB LA9901P Schematic | Rev: 1.0

Date: Wednesday, March 20, 2013 | Sheet 63 of 63