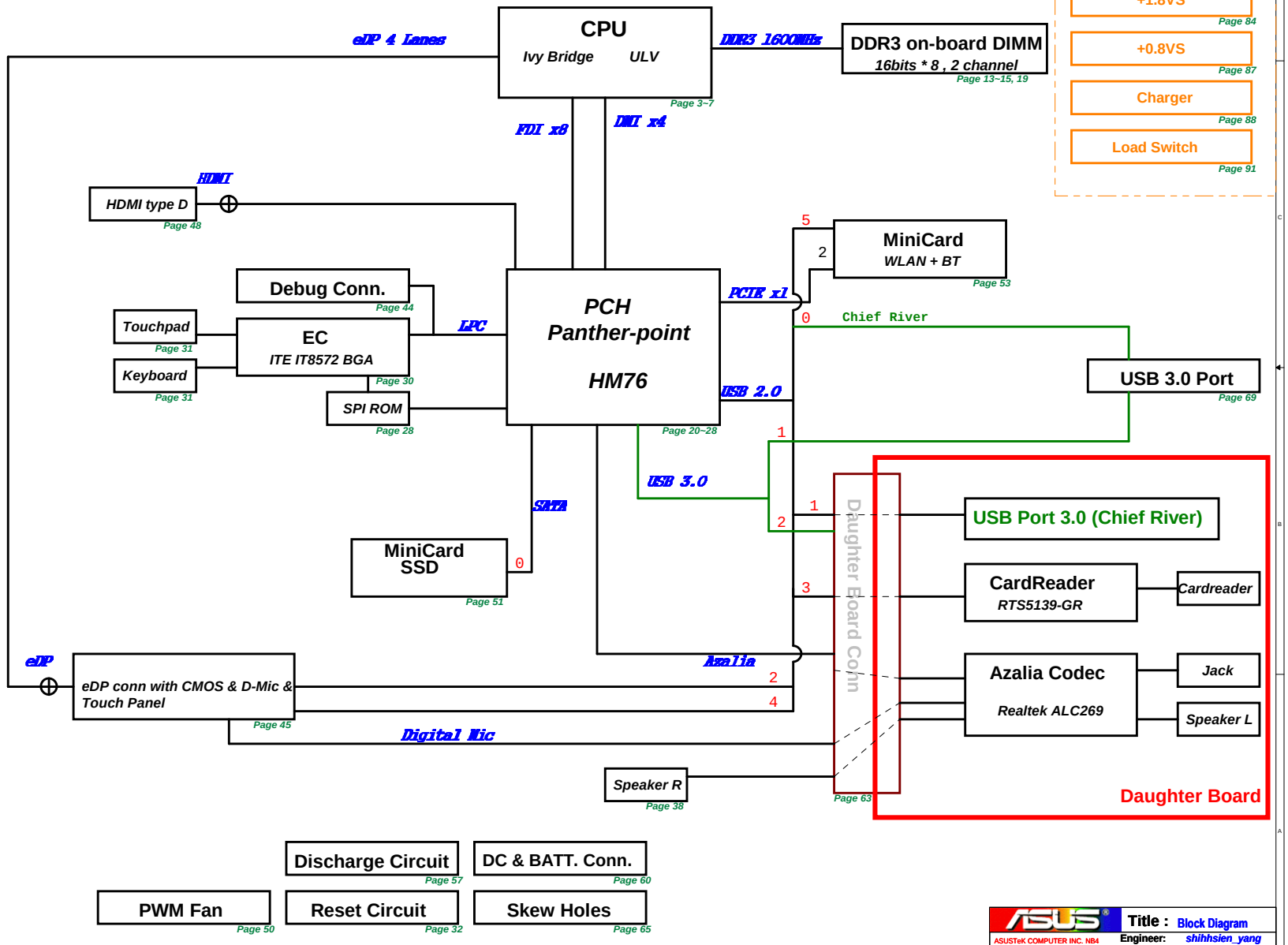
UX31A2 SCHEMATIC Revision R2.0

SYSTEM PAGE REF.

80_PW_VCORE(RT8168B)
81_PW_SYSTEM(RT8239B)
82_PW_I/O_VCCP(TPS51317)
83_PW_I/O_DDR(RT8207M)
84_PW_+1.8VS(RT8015B)
87_PW_+0.8VS(RT8015B)
88_PW_CHARGER(BQ24725)
91. PWR_LOAD SWITCH

BLOCK DIAGRAM



ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 1 of 99

PCH_CPT GPIO

PCH_IBEX GPIO	Use As	Signal Name	Int.& Ext Pull up / down	Power
GPIO 00	Native	NC_TP	EXT PU 1K	+3VS
GPIO 01	GPI	EXT_SMI#	INT PU 20K, EXT PU 10K	+3VS
GPIO 02	Native	NC_TP	EXT PU 10K	+3VS
GPIO 03	GPI	SATA_ODD_DA#	EXT PU 10K	+5VS
GPIO 04	GPI	PCB_ID0	EXT PD 10K	
GPIO 05	GPI	PCB_ID1	EXT PD 10K	
GPIO 06	Native	TMDS_HDMI_HPD	INT PU 20K, EXT PU 10K	+3VS
GPIO 07	GPI	USB3_SMI#	INT PU 20K, EXT PU 10K	+3VS
GPIO 08	Straping	ICC_EN#		
GPIO 09	Native	EXT_SCI#	EXT PU 10K	+3VSUS
GPIO 10	Native	OC#6	EXT PU 10K	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU 10K	+3VSUS
GPIO 12	GPO			
GPIO 13	Native	HDA_DOCK_RST#		
GPIO 14	Native	OC#7	EXT PU 10K	+3VSUS
GPIO 15	GPO	BT_LED	INT PD 20K, EXT PU 1K	+3VSUS
GPIO 16	Native	SATA_DET#4	EXT PU 10K	+3VS
GPIO 17	GPI		INT PU 20K, EXT PD 10K	
GPIO 18	Native	CLK_REQ1#	EXT PU 10K	+3VS
GPIO 19	Native	SATA1GP	INT PU 20K, EXT PU 10K	+3VS
GPIO 20	Native	CLK_REQ2#	EXT PU 10K	+3VS
GPIO 21	Native	SATA0GP	EXT PU 10K	+3VS
GPIO 22	GPO	WLAN_LED	EXT PU 10K	+3VS
GPIO 23	Native	LPC_DRQ#1	INT PU 20K	
GPIO 24	GPO		EXT PU 10K	+3VSUS
GPIO 25	Native	CLKREQ_USB3#	EXT PU 10K	+3VSUS
GPIO 26	Native	CLK_REQ4#	EXT PU 10K	+3VSUS
GPIO 27	Native	DSW_WAKE#	INT PU 20K	
GPIO 28	Straping	WLAN_ON#	INT PU 20K	+3VSUS
GPIO 29	Native	SLP_LAN#	EXT PU 10K	+3VSUS
GPIO 30	Native	ME_SusPwrDnAck	EXT PU 10K	+3VSUS
GPIO 31	Native	ME_AC_PRESENT_PCH	INT PD 20K,EXT PU 10K	+VCCPDSW
GPIO 32	Native	PM_CLKRUN#	EXT PU 10K	+3VS
GPIO 33	Native	HDA_DOCK_EN#		
GPIO 34	Native	STP_PCI#	EXT PU 10K	+3VS
GPIO 35	GPO	GPIO35_PCH		
GPIO 36	Native	DMI_OVRVLTG	INT PD 20K, EXT PU 200K	+3VS
GPIO 37	Native	FDI_OVRVLTG	INT PD 20K, EXT PD 100K	
GPIO 38	Native	MFG_MODE	EXT PU 10K	+3VS
GPIO 39	Native	GFX_CRB_DET	EXT PU 10K	+3VS
GPIO 40	Native	OC#1	EXT PU 10K	+3VSUS
GPIO 41	Native	DIMM_SEL0	EXT PU 10K	+3VSUS
GPIO 42	Native	DIMM_SEL1	EXT PU 10K	+3VSUS
GPIO 43	Native	DIMM_SEL2	EXT PU 10K	+3VSUS
GPIO 44	Native	CLKREQ_GLAN#	INT PU 20K, EXT PU 10K	+3VSUS
GPIO 45	Native	CLK_REQ6#	EXT PU 10K	+3VSUS
GPIO 46	Native	CLK_REQ7#	INT PU 20K, EXT PU 10K	+3VSUS
GPIO 47	Native	CLK_PEGA_REQ#	EXT PU 1K	+3VSUS
GPIO 48	GPIO	TEST_SET_UP	EXT PU 10K	+3VS
GPIO 49	GPI	SATA_DET#5	EXT PU 10K	+3VS
GPIO 50	GPO	GPU_RST#	EXT PD 10K	
GPIO 51	Straping	PCI_GNT1#	INT PU 20K, EXT PU 10K	+3VS
GPIO 52	Native	PCI_REQ#2	EXT PU 10K	+3VS
GPIO 53	Native	DGPU_PWM_SELECT#	INT PU 20K	
GPIO 54	GPO	DGPU_PWR_EN#	EXT PD 1K	
GPIO 55	Straping	STP_A16OVR	INT PU 20K, EXT PD 1K	
GPIO 56	Native	CLK_PEGB_REQ#	EXT PU 10K	+3VSUS
GPIO 57	GPO	BT_ON	EXT PD 100K	
GPIO 58	Native	SML1_CLK	EXT PU 2.2K	+3VSUS
GPIO 59	Native	OC#0	EXT PU 10K	+3VSUS
GPIO 60	GPO	DRAMRST_PCH	EXT PU 2.2K	+3VSUS
GPIO 61	Native	PM_SUS_STAT#		
GPIO 62	Native	SUS_CLK#		
GPIO 63	Native	SLP_S5#		
GPIO[66:64]	Native	CLK_OUT[2:0]	INT PD 20K	
GPIO 67	Native		INT PD 20K	
GPIO 68	GPO	NC_TP	INT PU 20K	
GPIO 69	GPI	NC_TP	INT PU 20K, EXT PD 1K	
GPIO[71:70]	Native	NC_TP	INT PU 20K, EXT PU 1K	+3VS
GPIO 72	Native	PM_BATLOW#	INT PU 20K, EXT PU 10K	+3VSUS
GPIO 73	Native	CLK_REQ0#	EXT PU 10K	+3VSUS
GPIO 74	Native	PCHHOT#	EXT PU 10K	+3VSUS
GPIO 75	Native	SUS_STAT#	EXT PU 2.2K	+3VSUS

EC IT8572 GPIO

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	O	
GPA2	O	CHG_FULL_LED#
GPA3	O	
GPA4	O	
GPA5	O	FAN_PWM
GPA6		-
GPA7	O	KB_LED_PWM
GPB0	O	ME_AC_PRESENT
GPB1	O	
GPB2	O	+3VA_ON
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0		
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5		
GPC6	I	BAT1_IN_OC#
GPC7		
GPD0	I	PWRLIMIT#_EC
GPD1	O	CAP_LED#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	OP_SD#
GPD6	I	FAN0_TACH
GPD7		-
GPE0	O	SUSC_EC#
GPE1		
GPE2	O	1.5V_ON
GPE3	O	BIOS_WP#
GPE4	I	PWR_SW#
GPE5	I	PM_SUSC#
GPE6	I	LID_SW_EC#
GPE7		
GPF0	O	PM_SYSPWROK
GPF1	O	3VSUS_ON
GPF2		-
GPF3	O	USB_CHARGE_ON#
GPF4	IO	TP_CLK
GPF5	IO	TP_DAT
GPF6	I	PECI_EC
GPF7	O	PCH_SPI_OV
GPG0	I	ME_SusPwrDnAck
GPG1	I	PM_SUSB#
GPG2		
GPG6		-
GPH0	IO	PM_CLKRUN#
GPH1	O	THRO_CPU#
GPH2	O	LCD_BACKOFF#
GPH3	O	SUSB_EC#
GPH4	O	USB_CHARGE_VBUS_EC
GPH5		
GPH6	I	5VSUS_PWRGD
GPI0	I	Light_Sensor_AD
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	CORE_PWRGD
GPI4		-
GPI5		-
GPI6		-
GPI7	I	Adaptor_Sense
GPJ0	O	
GPJ1	O	PM_PWROK
GPJ2	O	
GPJ3	O	
GPJ4	O	5VSUS_PWRON
GPJ5	O	DRAMRST_EC

Design IP Source: N53S

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
EC Master (SMB1)	**SM-Bus Address**	
SM-Bus Device		
DIMM TEMP.	9Ah	
CPU Thermal Sensor	90h	

PCI Express

PCIE 1	
PCIE 2	Minicard WLAN
PCIE 3	
PCIE 4	USB 3.0
PCIE 5	
PCIE 6	
PCIE 7	
PCIE 8	

USB Port

USB 0	USB 3.0 Port
USB 1	USB Port 1
USB 2	Touch Panel
USB 3	Card Reader
USB 4	CMOS Camera
USB 5	Bluetooth
USB 6	
USB 7	
USB 8	
USB 9	
USB 10	
USB 11	
USB 12	
USB 13	

SATA Port

SATA 0	SATA SSD
SATA1	
SATA2	
SATA4	

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

Memory Thermal Senser		
1st	06G023048020	G781-1
2nd		

ASUSTeK COMPUTER INC. NB3

Title : System Setting

Engineer: shihhsien_yang

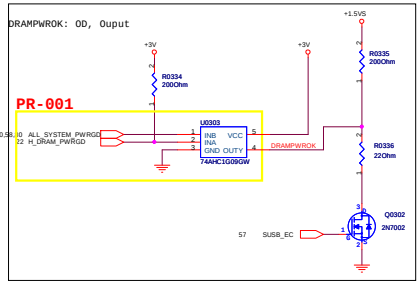
Size	Project Name	Rev
C	UX31A2	R2.0

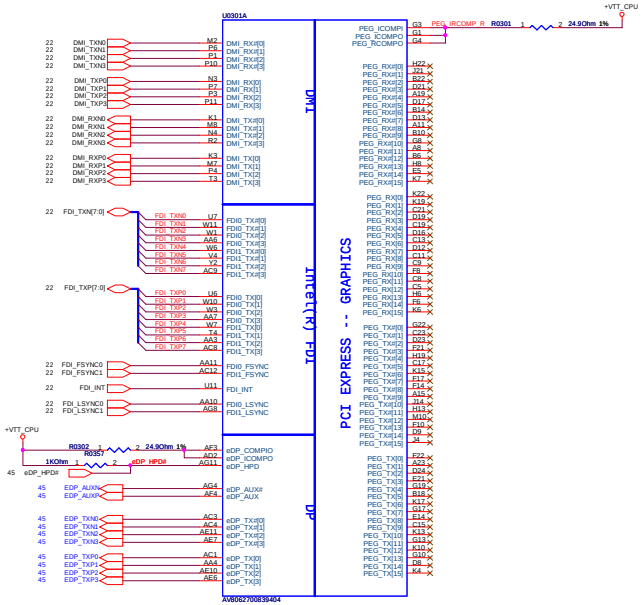
Date: Tuesday, March 27, 2012 Sheet 2 of 99

FDI disable: (For discrete graphic)

1. NC:
   FDI_TX#[0:7],FDI_TX[0:7],VCC_AXGSENSE,VSS_AXGSENSE
2. Pull-down to GND via 1KΩ ± 5% resistor:
   FDI_FSYNC[0:1],FDI_LSYNC[0:1],FDI_INT,GFX_IMON
   ~15mW power saving
3. Connected to GND:
   VCCAXG
4. Can be connected to GND directly:
   DPLL_REF_CLK,DPLL_REF_CLK#
5. Connect to +V1.05S rail:
   VCCFDIPLL

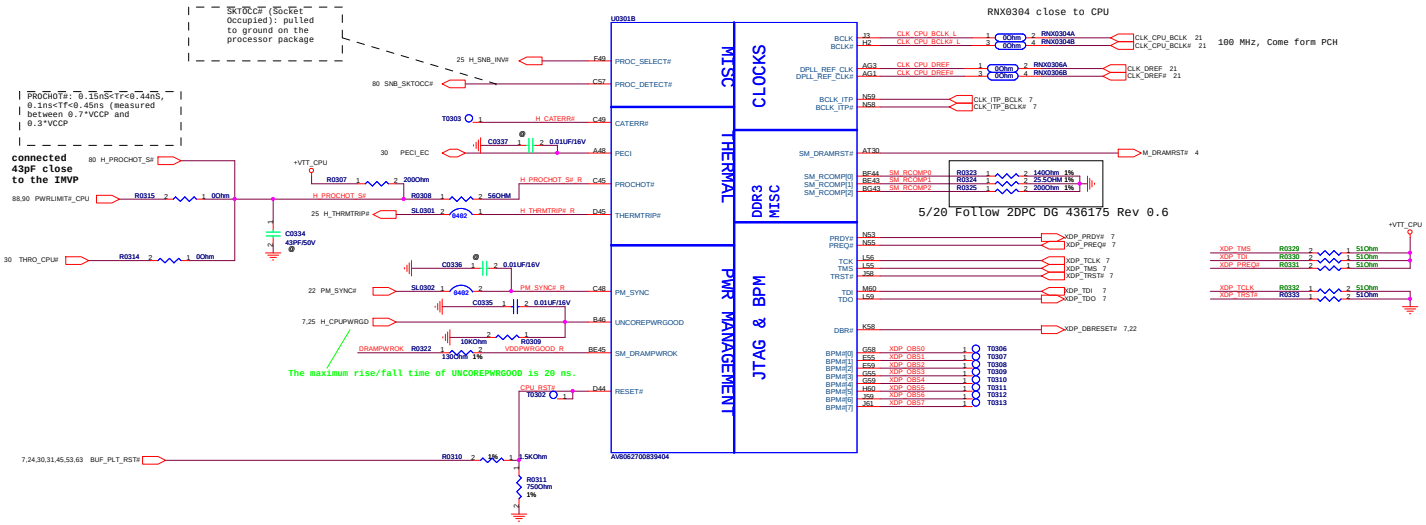
eDP disable/Enable
CFG[4]:
Enable: Mount R0503, R0303=1K
Disable: un-mount R0503, R0303=10Kohm

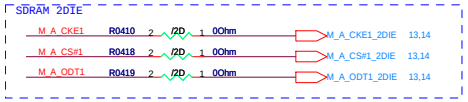


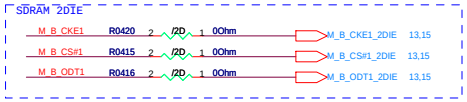


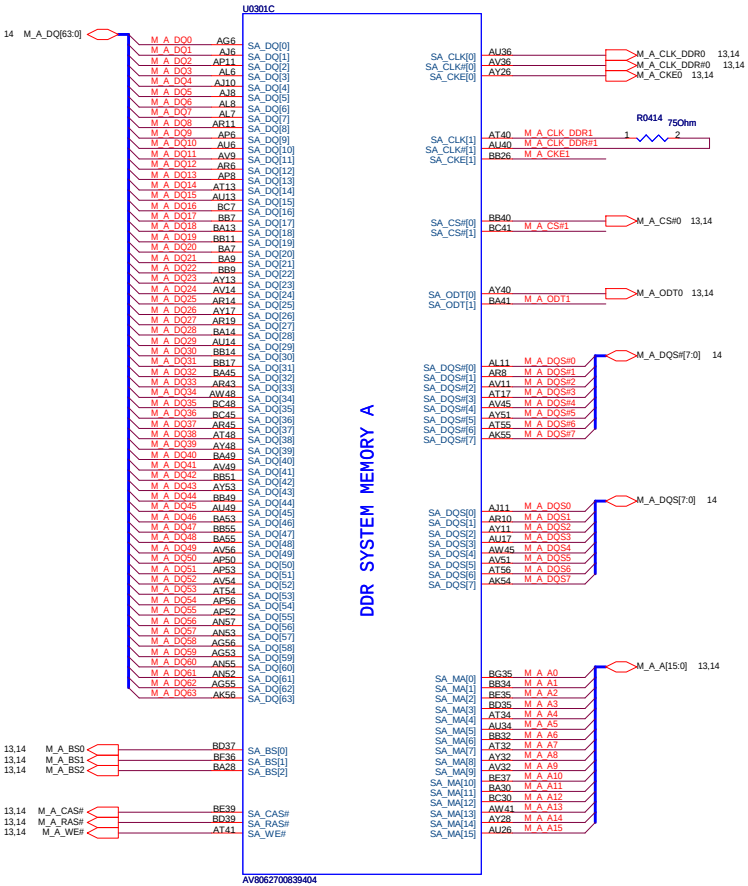
Huron River PCIE support 2.5 GT/s, 5 GT/s and 8 GT/s

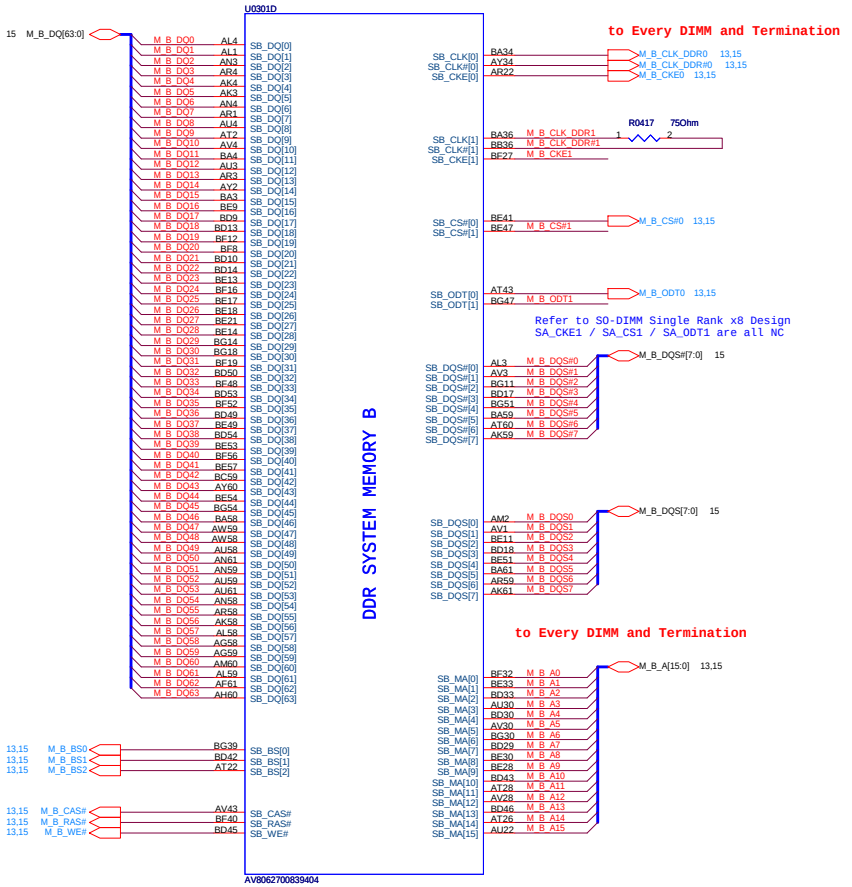
PCIE AC Coupling Capacitors:
1. 436735 PDG Page 39, 75nF~200nF
2. 431433 EMERALD LAKE Schematic 220nF
3. 436735 PDG Page 41, 180nF~265nF



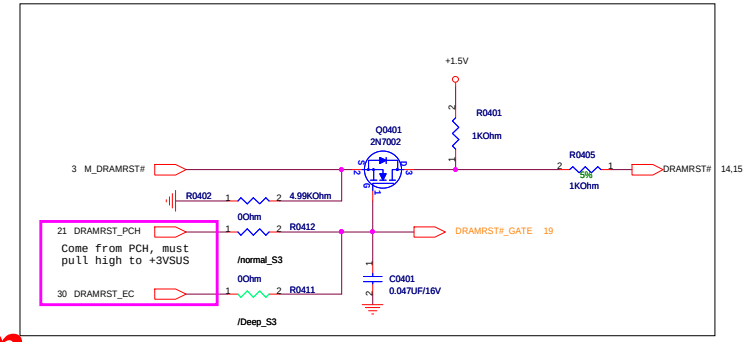




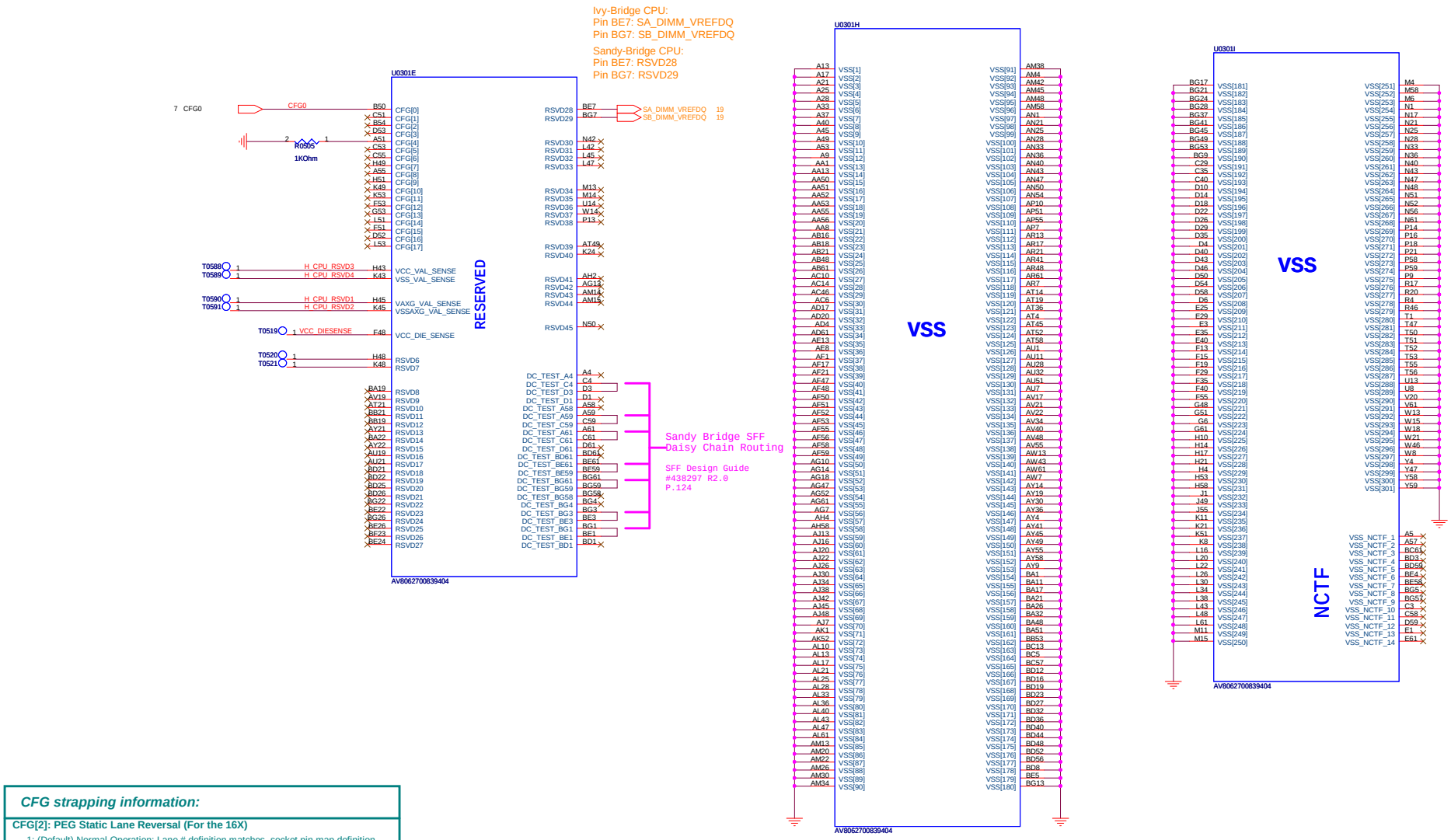




DRAM RESET



ASUSTeK COMPUTER INC. NB3	Title : CPU_DDR3	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 4 of 99	



CFG strapping information:

CFG[2]: PEG Static Lane Reversal (For the 16X)

- 1: (Default) Normal Operation; Lane # definition matches socket pin map definition
- 0: Lane Reversed

CFG[4]: Display Port Presence Strap

- 1 : (Default) Disable; No Physical Display Port attached to Embedded Display Port
- 0 : Enable; An external Display Port device is connected to the Embeded Display port

CFG[6:5]: PCIE Port Bifurcation Straps

- 11 : (Default) X16 - Device 1 functions 1 and 2 disable
- 10 : X8, X8 - Device 1 function 1 enabled; Function 2 disable
- 01 : Reserved - (Device 1 Function 1 disable ; Function 2 enable
- 00 : X8, X4 X4 - Device 1 function 1 and 2 enabled

CFG[7]: Defer Training

-1: (Default) PEG Train immediately following xxRESETB de assertion

-0: PEG Wait for BIOS for training

ASUSTeK COMPUTER INC. NB3

Title : CPU_CFG,RSVD,GND

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 5 of 99

+VCORE
+VCORE_CPU
HFM: 0.7V ~ 1.2V
LFM: 0.65V ~ 0.9V
+1.05VS
+VTT_CPU
+VGFX_CORE
+VGFX
ULV: 0.65V ~ 1.35V

ULV
P0 (Turbo): 33A
P1 (HFM): 21.5A
Px (LFM): 12.5A

ULV
GT2 (Turbo): 26A
GT2 (TDC) : 10A
GT1 (Turbo) :16A
GT1(TDC) : 8A

ER-014

+V_SM_VREF should have 10 mil trace width

U0301F
U0301G

POWER
CORE SUPPLY
PEG AND DDR
GRAPHICS
DDR3 - 1.5V RAILS
1.8V RAIL
SA RAIL
QUIET RAILS
SVID
SENSE LINES

8.5A
5A
6A
1.2A

SVID signal is very critical.
Please follow Intel design guide

It must be min 100 ns after to +1.5Vs reaches 80%

H_SNB_IVB#_PWRCTRL= LOW, VCCP=1.0V
H_SNB_IVB#_PWRCTRL= High/NC, VCCP=1.05V

VCCSA_SEL0	VCCSA_SEL1	VCCSA_SEL
L	L	0.9V
L	H	0.85V for ULV only
H	L	0.75V
H	H	0.65V

AV8062700839404

ASUSTeK COMPUTER INC. NB3
Title : CPU_PWR
Engineer: shihhsien_yang
Size: C
Project Name: UX31A2
Rev: R2.0
Date: Tuesday, March 27, 2012
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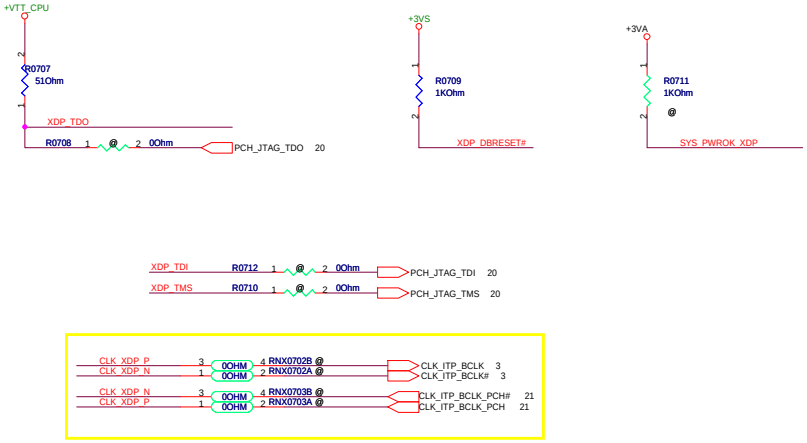
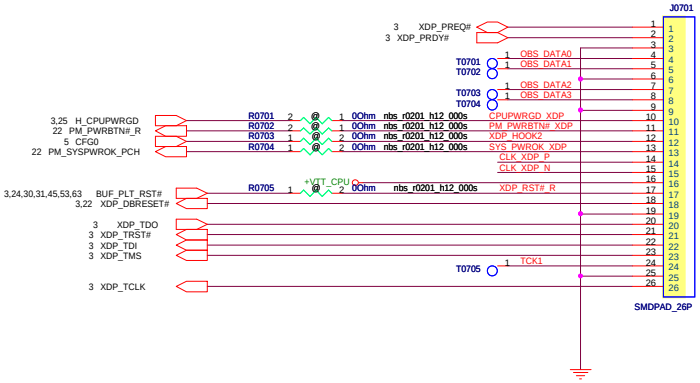
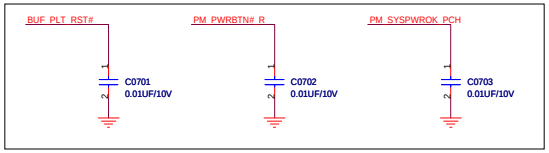




Please mount J0701,
R0701~R0705 and RNX0702
for debug on SR and ER

Place near J0701



ASUSTeK COMPUTER INC. NB3	Title : CPU_XDP	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 7 of 99	

Title :	NB_****
ASUSTeK COMPUTER INC. NB1	Engineer: shihhsien_yang
Size: Custom	Project Name: UX31A2
Rev: R2.0	
Date: Tuesday, March 27, 2012	Sheet 8 of 99

Main Board

ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: shihhsien_yang		
Size: Custom	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 9 of 99		

Main Board

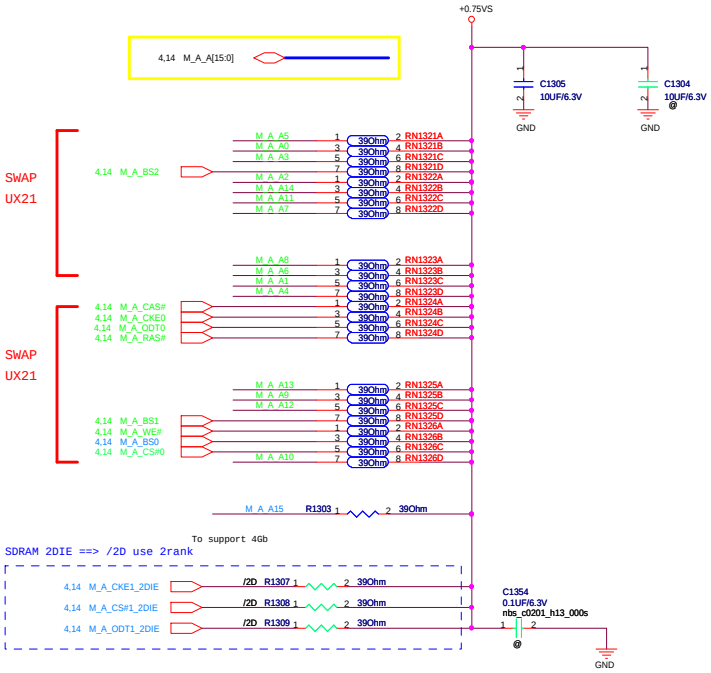
ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: shihhsien_yang		
Size: Custom	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 10 of 99		

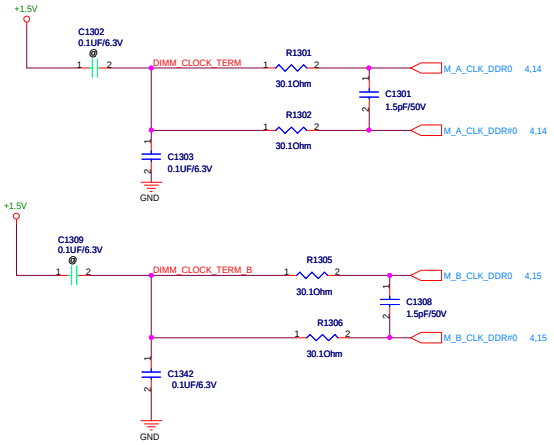
Main Board

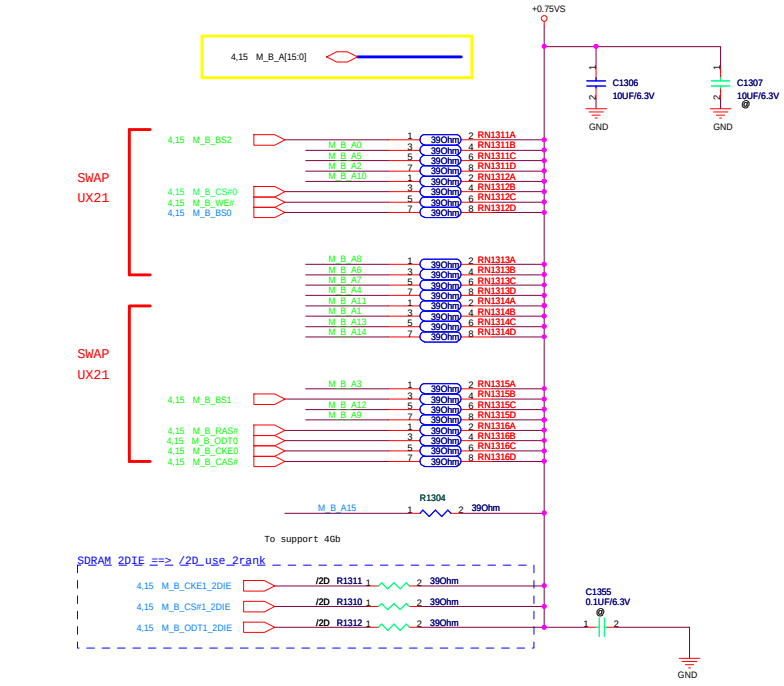
ASUSTeK COMPUTER INC. NB1	Title : NB_****	
	Engineer: shihhsien_yang	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 11 of 99	

Main Board

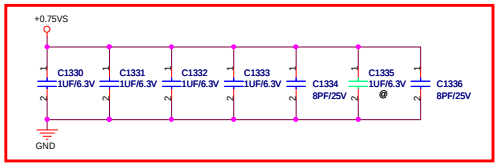
ASUSTeK COMPUTER INC. NB1	Title : NB_****		
	Engineer: shihhsien_yang		
Size: Custom	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 12 of 99		



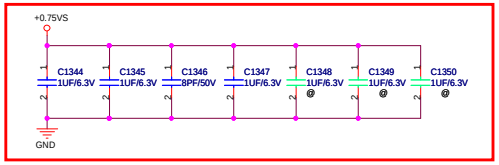




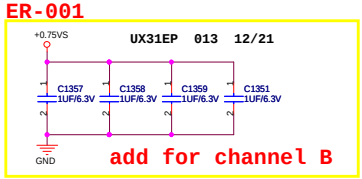
Refer to Intel CRB

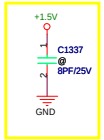


Refer to Intel CRB



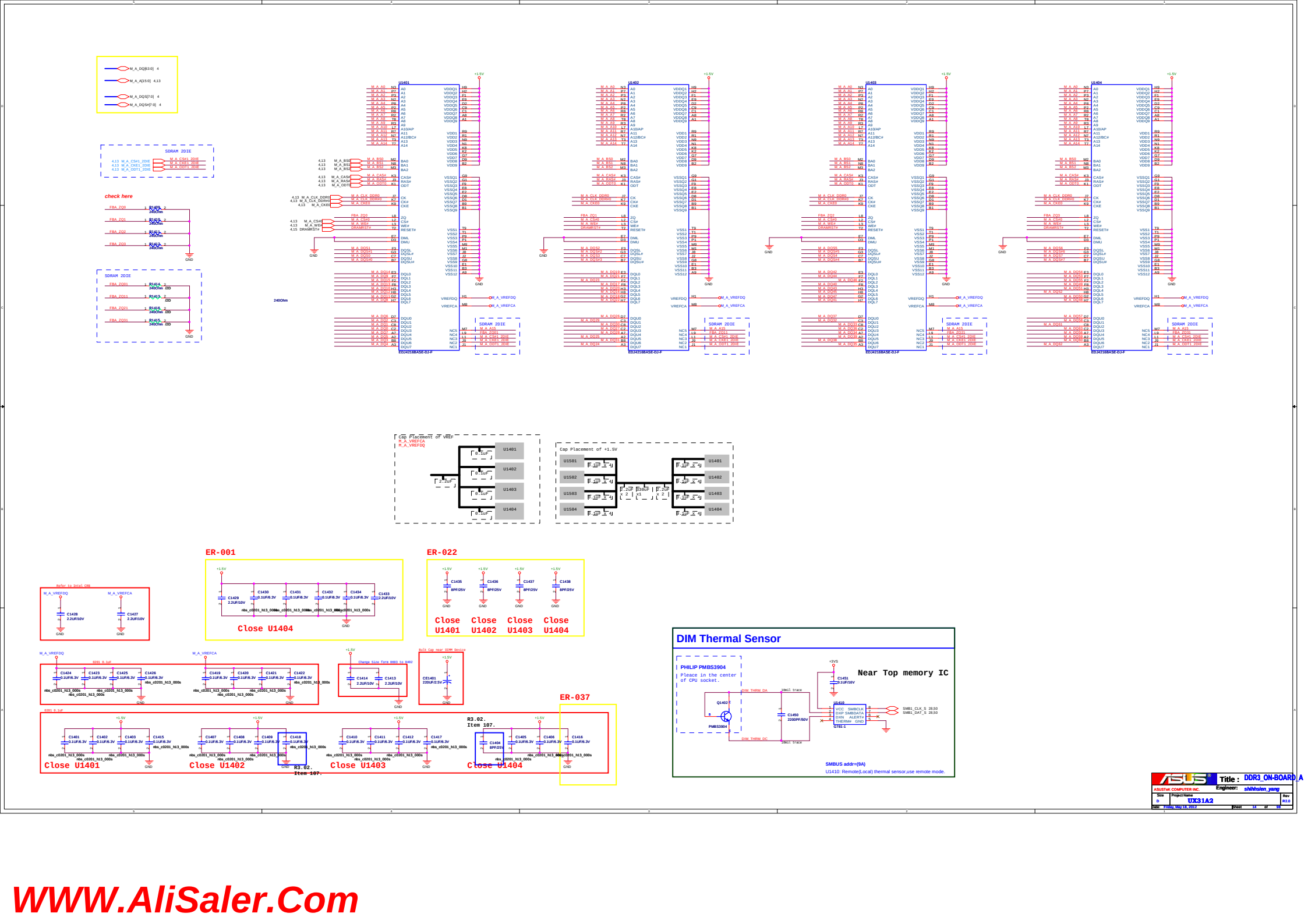
ER-001

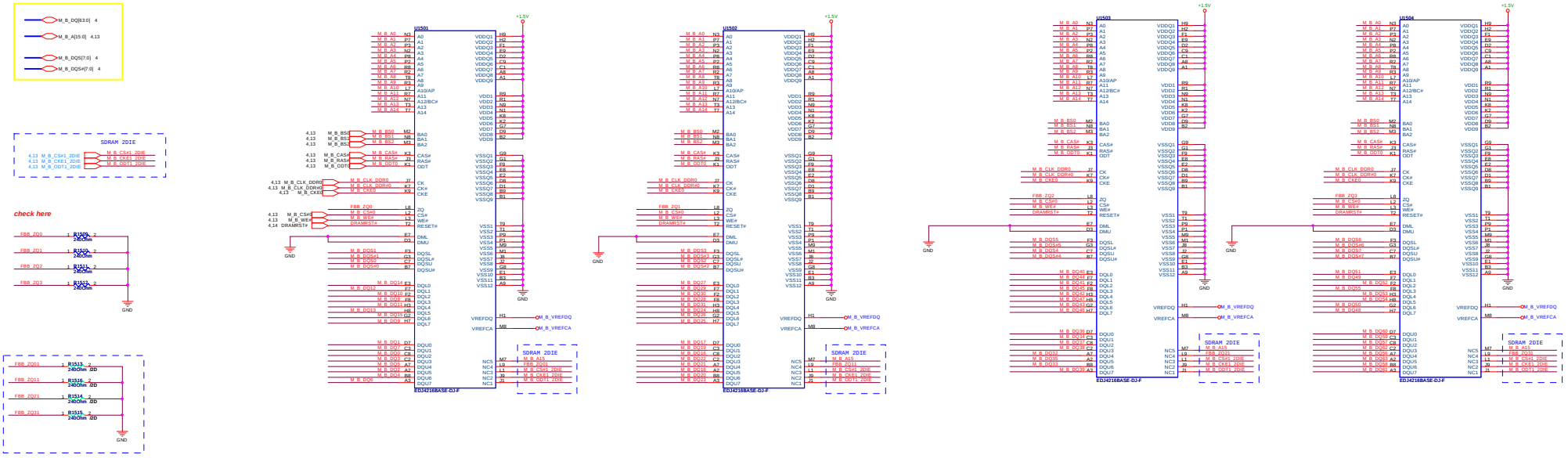




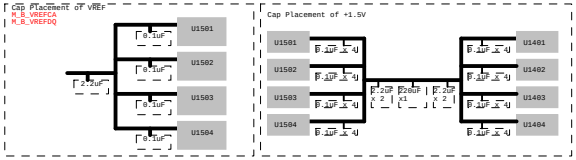
ER-022

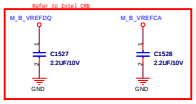
ASUSTeK COMPUTER INC.	Title : DDR3_TERMINATION	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Friday, May 18, 2012	Sheet 13 of 98	

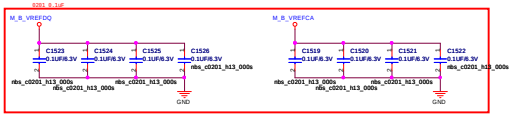


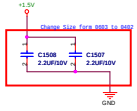


R3.0. Item 100.

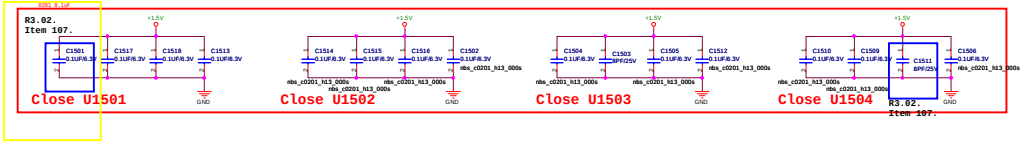




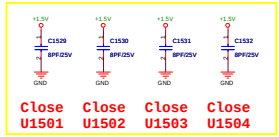




ER-037



ER-022



ASUSTeK COMPUTER INC.	Title : DDR3_ON-BOARD_B		
	Engineer: shihhsien_yang		
Size: D	Project Name: UX31A2		Rev: R2.0
Date: Friday, May 18, 2012	Sheet 15 of 98		

ASUSTeK COMPUTER INC.	Title : DDR3_TERMINATION_B		
	Engineer: shihhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 16 of 99		

Title : DDR3_ON-BOARD_B_L32

ASUSTeK COMPUTER INC.

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

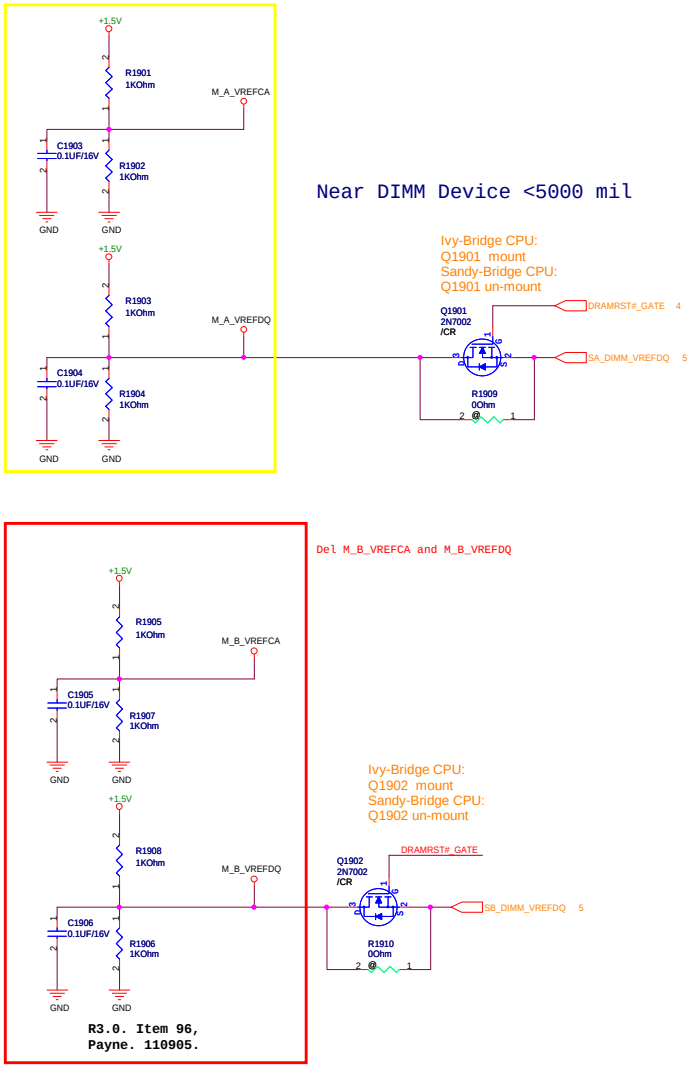
Date: Tuesday, March 27, 2012 Sheet 17 of 99

ASUSTeK COMPUTER INC.	Title : DDR3_ON-BOARD_B_H32	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 18 of 99	

Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

DDR3 Vref

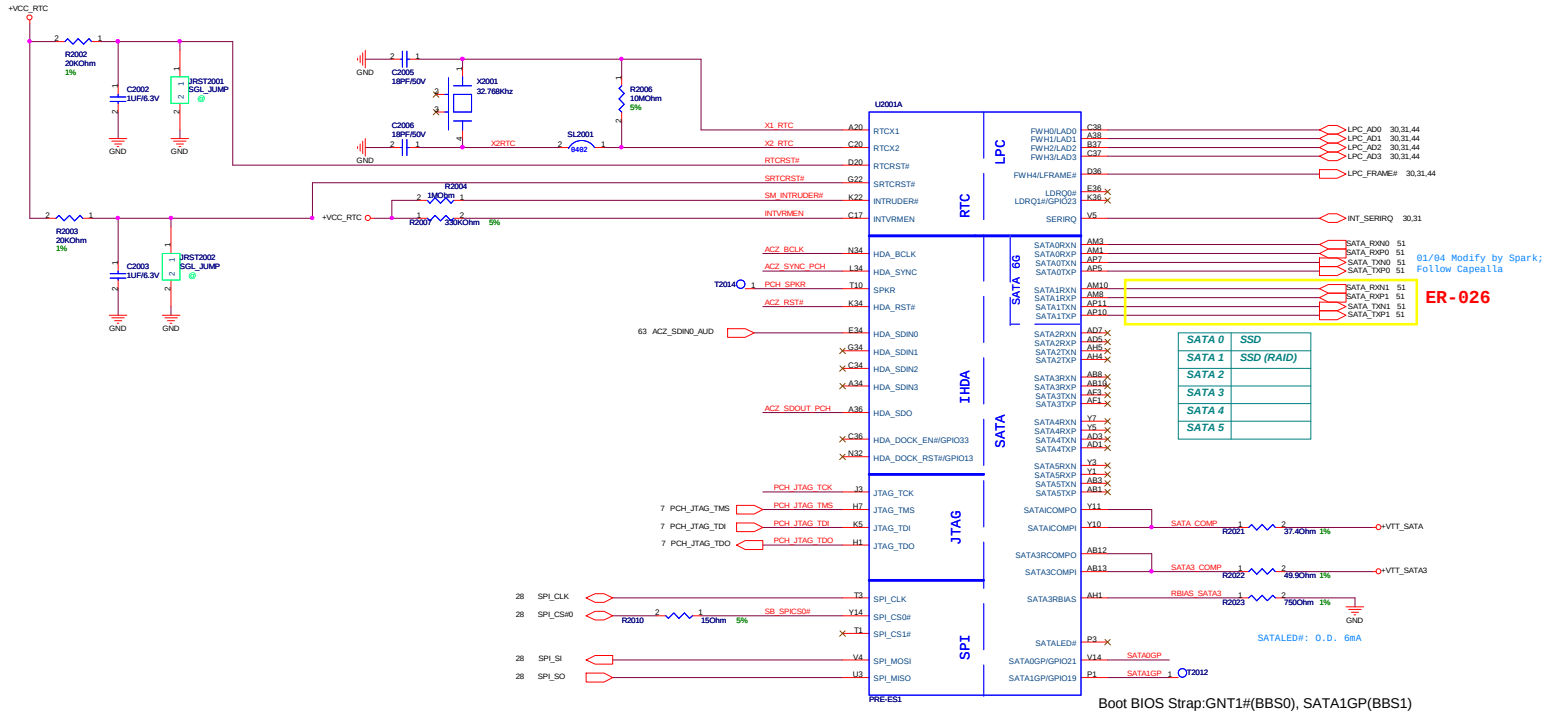
Intel Document Number: 400755



ASUSTeK COMPUTER INC. NB6	Title DDR3 CA_DQ VOLTAGE	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 19 of 98	

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)



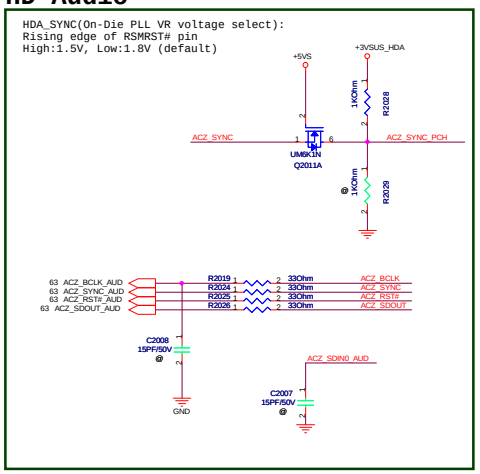
SATA 0	SSD
SATA 1	SSD (RAID)
SATA 2	
SATA 3	
SATA 4	
SATA 5	

01/04 Modify by Spark; Follow Capealla

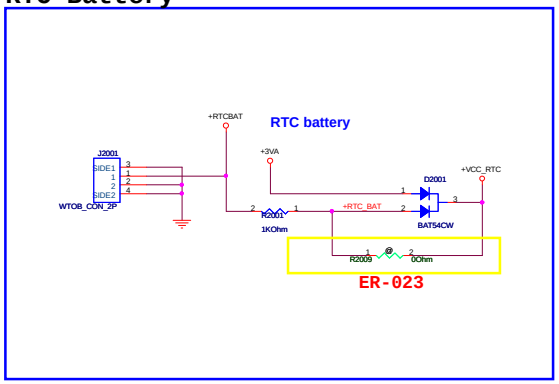
ER-026

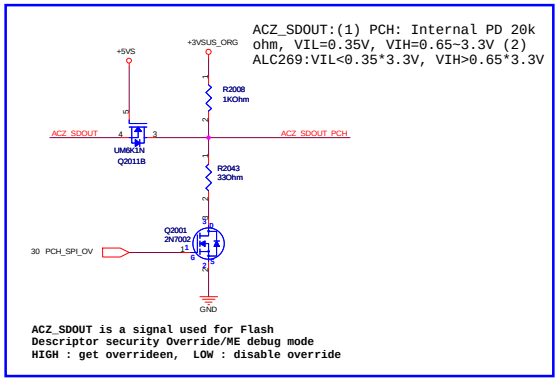
Boot BIOS Strap:GNT1#(BBS0), SATA1GP(BBS1)

HD Audio



RTC Battery

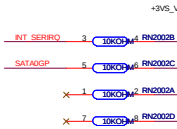




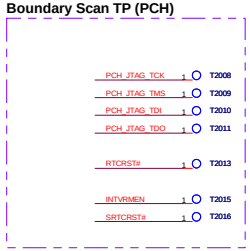
JTAG

U37 001

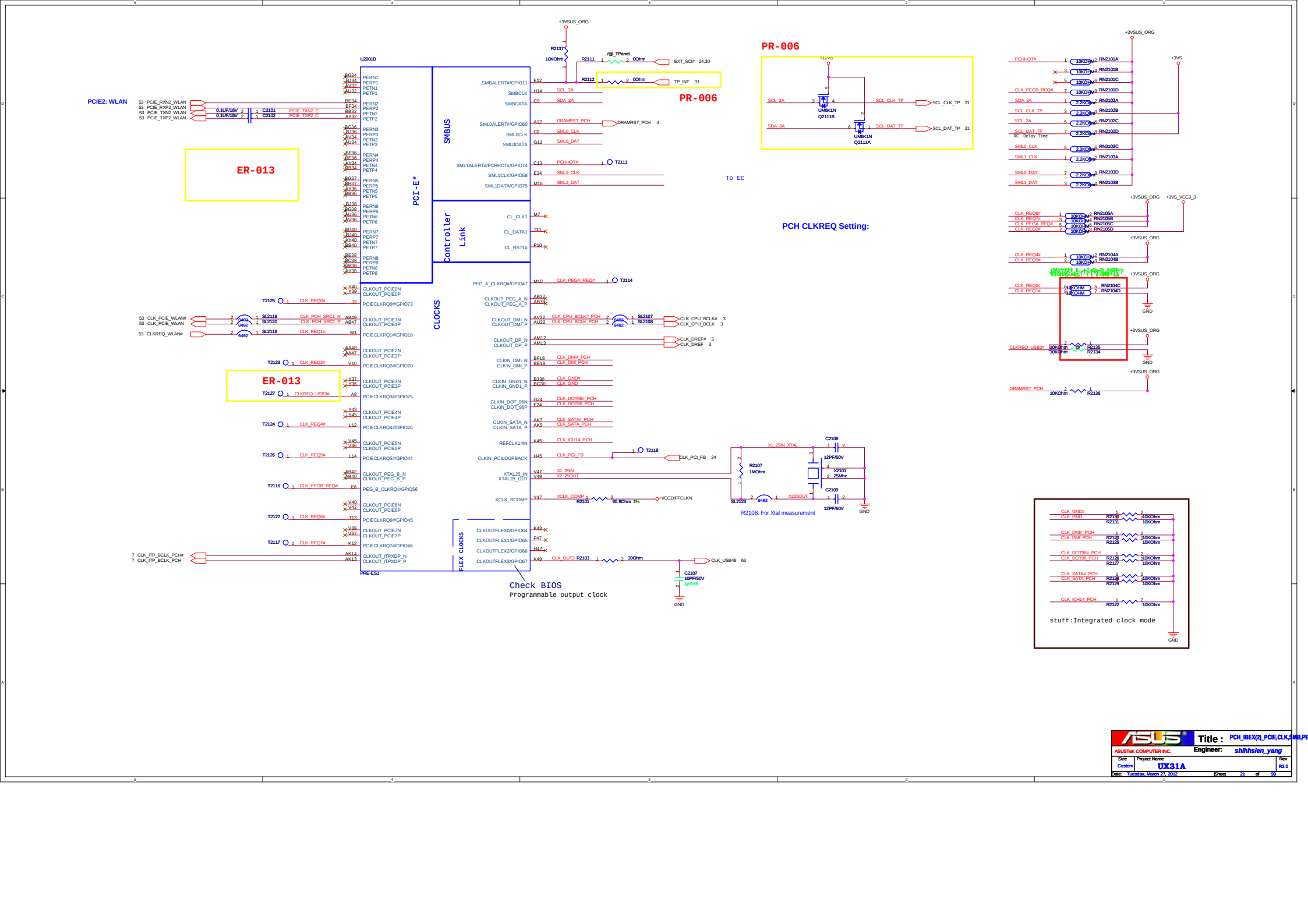
For PU/PD



Boundary Scan TP (PCH)



Title	CPU_BGA(1)SATA,HDA,RTC,LPC
ASUSTeK COMPUTER INC.	Engineer: shihhsien_yang
Size: Custom	Project Name: UX31A2
Rev: R2.0	
Date: Tuesday, March 27, 2012	Sheet 20 of 99


PCIE2: WLAN
ER-013
ER-013
U2001B
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PRE-ES1
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SML0ALERT#/GPIO60
SML0CLK
SML0DATA
SML1ALERT#/PCHHOT#/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ#/GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND1_N
CLKIN_GND1_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
PCIECLKRQ0#/GPIO73
PCIECLKRQ1#/GPIO18
PCIECLKRQ2#/GPIO20
PCIECLKRQ3#/GPIO25
PCIECLKRQ4#/GPIO26
PCIECLKRQ5#/GPIO44
PEG_B_CLKRQ#/GPIO56
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
CLK_REQ0#
CLK_REQ1#
CLK_REQ2#
CLKREQ_USB3#
CLK_REQ4#
CLK_REQ5#
CLK_REQ6#
CLK_REQ7#
CLKREQ_WLAN#
CLK_ITP_BCLK_PCH#
CLK_ITP_BCLK_PCH
CLK_PCH_SRC1_N
CLK_PCH_SRC1_P
CLK_PCIE_WLAN#
CLK_PCIE_WLAN
T2125
T2123
T2127
T2124
T2126
T2122
T2117
T2116
SL2119
SL2120
SL2118
0.1UF/16V
C2101
C2102
PCIE_TXN2_C
PCIE_TXP2_C
PCIE_RXN2_WLAN
PCIE_RXP2_WLAN
PCIE_TXN2_WLAN
PCIE_TXP2_WLAN
+3VSUS_ORG
R2137
10KOhm
R2111
/@_TPanel
0Ohm
EXT_SCI# 24,30
R2112
TP_INT 31
PR-006
PR-006
SCL_3A
SDA_3A
SCL_CLK_TP
SCL_DAT_TP
SCL_CLK_TP 31
SCL_DAT_TP 31
UM6K1N
Q2111B
Q2111A
To EC
DRAMRST_PCH
DRAMRST_PCH 4
SML0_CLK
SML0_DAT
PCHHOT#
T2111
SML1_CLK
SML1_DAT
PCH CLKREQ Setting:
CLK_PEGA_REQ#
T2114
CLK_CPU_BCLK# PCH
CLK_CPU_BCLK PCH
CLK_CPU_BCLK# 3
CLK_CPU_BCLK 3
CLK_DREF# 3
CLK_DREF 3
CLK_DMI# PCH
CLK_DMI PCH
CLK_GND#
CLK_GND
CLK_DOT96# PCH
CLK_DOT96 PCH
CLK_SATA# PCH
CLK_SATA PCH
CLK_ICH14 PCH
CLK_PCI_FB
T2118
CLK_PCI_FB 24
X1_25IN
X2_25OUT
XCLK_COMP
90.9Ohm 1%
+VCCDIFFCLKN
R2101
R2107
1MOhm
X2101
25Mhz
C2108
C2109
12PF/50V
X1_25IN_XTAL
X225OUT
SL2123
R2108: For Xtal measurement
CLK_OUT3
R2103
39Ohm
CLK_USB48 63
C2107
10PF/50V
@/EMI
Check BIOS
Programmable output clock
+3VS
+3VS_VCC3_3
RN2101A
RN2101B
RN2101C
RN2101D
RN2102A
RN2102B
RN2102C
RN2102D
RN2103C
RN2103A
RN2103D
RN2103B
RN2105A
RN2105B
RN2105C
RN2105D
RN2104A
RN2104B
RN2104C
RN2104D
10KOHM
2.2KOhm
R2135
R2134
R2136
CLKREQ_USB3#
DRAMRST_PCH
RC Delay Time
GND
R2130
R2131
R2132
R2125
R2126
R2127
R2128
R2129
R2122
stuff:Integrated clock mode
ASUSTeK COMPUTER INC.
Title : PCH_IBEX(2)_PCIE,CLK,SMB,PE
Engineer: shihhsien_yang
Size: Custom
Project Name: UX31A
Rev: R2.0
Date: Tuesday, March 27, 2012
Sheet 21 of 99

SUSACK#:
SUSACK# and SUSWARN# can be tied together
if EC does not want to involve in handshake
mechanism for the Deep Sleep state entry and exit.

APWROK:
For platform not supporting iAMT
it can be connected to PWROK.

SUSPWRDNACK (PCH to EC):
This pin requires a pull-up to +3VSUS.
Platforms are not expected to use this
signal when the PCH's Deep S4/S5 feature is used.

SUSWARN# (PCH to EC):
This pin aserts low when PCH is planning
to enter the DeepSx power state and remove
Suspend power(using SLP_SUS#)

Entry Into Deep S4/S5
A combination of condition is required for entry into Deep S4/S5
All of the following must be met:
-Intel ME in Moff.
-AND either "a" or "b"(EDS R0.7v1 p.186).

ASW Power well stable for at least 1ms
before platform logic asserts APWROK

Have Pull up Res. in CPU side

DSWVRMEN:
High -> DSW On-Die VR Enable
Low -> DSW On-Die VR disable

DPWROK:
This input is tied
together with RSMRST#
in platforms that do not
support DeepSx

VCCDSW stable to DPWROK
assertion is 10ms (min)

4/23 Delete R2222, R2228,
U2201, R2230, R2233, C2201
and D2203,Deeper
sleeper要刪掉

PMSYNCH is Low in C6/C7 states only

U2001C

DMI0RXN DMI1RXN DMI2RXN DMI3RXN
DMI0RXP DMI1RXP DMI2RXP DMI3RXP
DMI0TXN DMI1TXN DMI2TXN DMI3TXN
DMI0TXP DMI1TXP DMI2TXP DMI3TXP
DMI_ZCOMP DMI_IRCOMP DMI2RBIAS

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_INT FDI_FSYNC0 FDI_FSYNC1 FDI_LSYNC0 FDI_LSYNC1

DMI FDI

System Power Management

SUSACK# SYS_RESET# SYS_PWROK PWROK APWROK DRAMPWROK RSMRST# SUSWARN#/SUSPWRDNACK/GPIO30 PWRBTN# ACPRESENT/GPIO31 BATLOW#/GPIO72 RI#

DSWVRMEN DPWROK WAKE# CLKRUN#/GPIO32 SUS_STAT#/GPIO61 SUSCLK/GPIO62 SLP_S5#/GPIO63 SLP_S4# SLP_S3# SLP_A# SLP_SUS# PMSYNCH SLP_LAN#/GPIO29

PRE-ES1

CHECK PULL-UP OR DOWN

Power failure solution (S0-->G3,S5-->G3):

PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

09'MoW04:
Optional if ME FW is
Ignition FW

D2207: Prevent EC drive hign,
SUS_PWRGD sink low in S5-->G3.

For PU/PD

CRB:8.2K Ohm

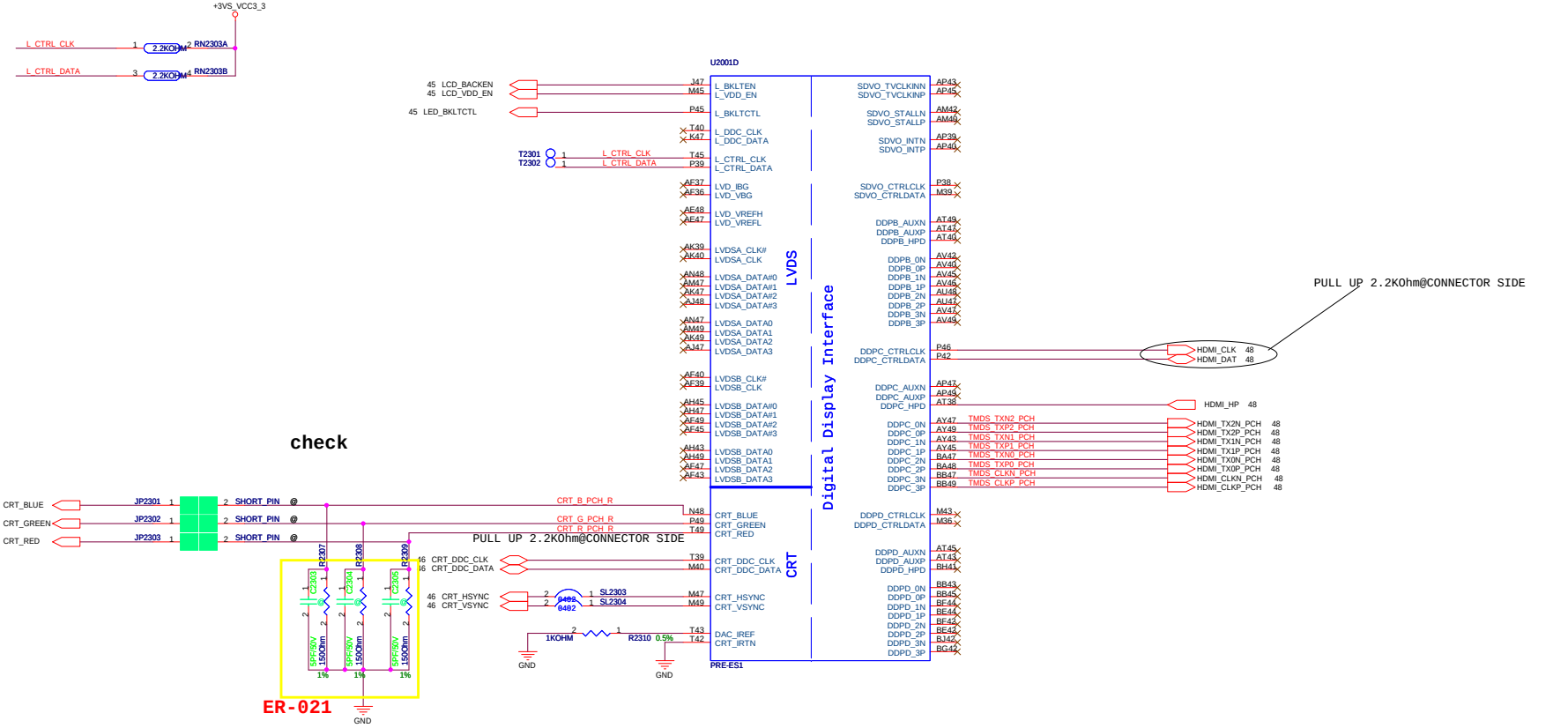
DG:Pull-up 10K Ohm to 3.3V(Core)
CRB:NO Pull-up or down resistor

Boundary Scan TP (PCH)

ASUSTeK COMPUTER INC.
Title : PCH_IBEX(3)_FDI,DMI,SYS PWR
Engineer: shihhsien_yang
Size C | Project Name UX31A2 | Rev R2.0
Date: Tuesday, March 27, 2012 | Sheet 22 of 99

PORT	STRAP	ENABLE PORT	DISABLE PORT
LVDS	L_DDC_DATA		
PORT B	SDVO_CTRLDATA	Pull up to 3.3(V) with 2.2k Ohm	NC
PORT C	DDPC_CTRLDATA		
PORT D	DDPD_CTRLDATA		

DG P.105,168



Title : PCH_IBEX(4)_DP,LVDS,CRT

ASUSTeK COMPUTER INC.

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 23 of 99

Tacoma Pass(NVRAM) Disabling and termination guidelines(DG R0.7 p.322)
If the tacoma Pass interface is not used,
the interface signals, inculding NV_RCOMP,
can be left as No connects with few exceptions.
VccpNAND, NV_ALE, NV_CLE

DMI & FDI Termination Voltage	
NV_CLE	LOW : Set to Vss
	HIGH : Set to Vcc

CRB

ER-018

ER-031

ER-030

USB2.0	
0	USB 3.0 Port
1	USB 2.0 Port (Debug)
2	
3	
4	Camera
5	WiFi/ WiMax/Blue Tooth
6	
7	
8	Touch Panel
9	Card Reader
10	
11	
12	
13	

USB 3.0	
1	USB 3.0 Port
2	USB 3.0 Port
3	
4	

PU / PD

DIMM_SEL

PCB_ID

PCB_ID1	PCB_ID0	On Board Memory
0	0	4GB(DDR3_1600、DDR3_L_1333、DDR3_L_1600)
0	1	N/A
1	0	4GB(DDR3_1333)
1	1	8GB(DDR3_1600)

PCBID:10 2GB (DDR3_1333)

DDR3_1333	Samsung	Hynix	ELPIDA	Micron
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	L	H	H
DIMM_SEL2	L	L	L	L

PCBID:10 4GB (DDR3_1333)

DDR3_1333	Samsung	ASINT	ELPIDA	Micron
DIMM_SEL0	L	H	L	H
DIMM_SEL1	L	L	H	H
DIMM_SEL2	H	H	H	H

PCBID:00 4GB (DDR3_L_1333、DDR3L_1600、DDR3_1600)

DDR3_L_1333		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		L	L	

DDR3L_1600	Micro			ELPIDA
DIMM_SEL0	L			H
DIMM_SEL1	L			H
DIMM_SEL2	H			H

DDR3_1600		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		H	H	

PCBID:11 8GB (DDR3_1600)

DDR3_1600		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		H	H	

Boot BIOS Strap : GNT1#, SATA1GP

Boot BIOS Strap		
GNT1#(BBS1)	SATA1GP(BBS0)	Boot BIOS Location
0	1	Reserved
1	0	PCI
1	1	SPI (PCH)
0	0	LPC

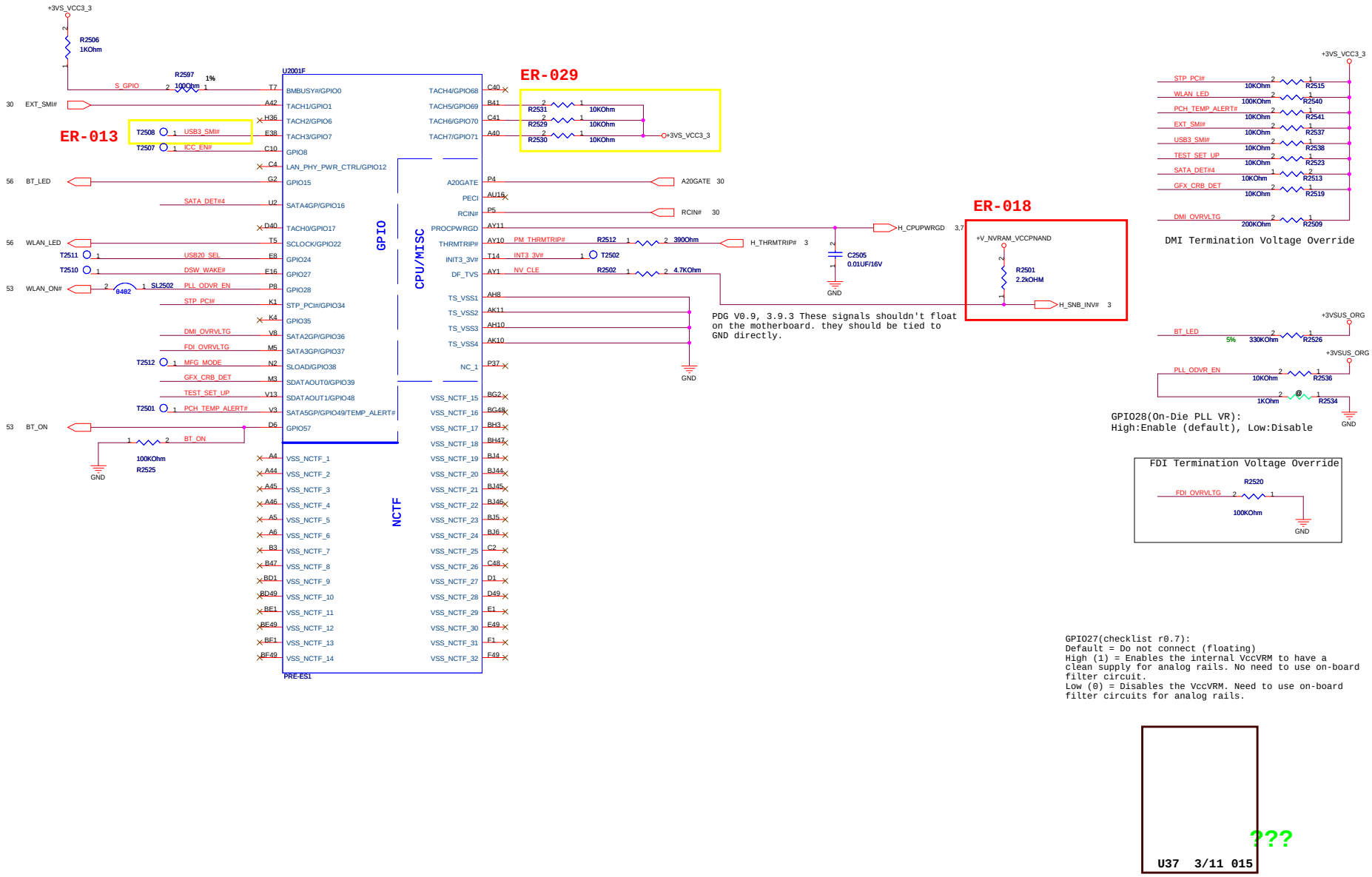
Sampled on rising edge of PWROK.

Default
PU 20K
OHM

GNT3#: A16 swap override Strap/ Top-Block swap override jumper

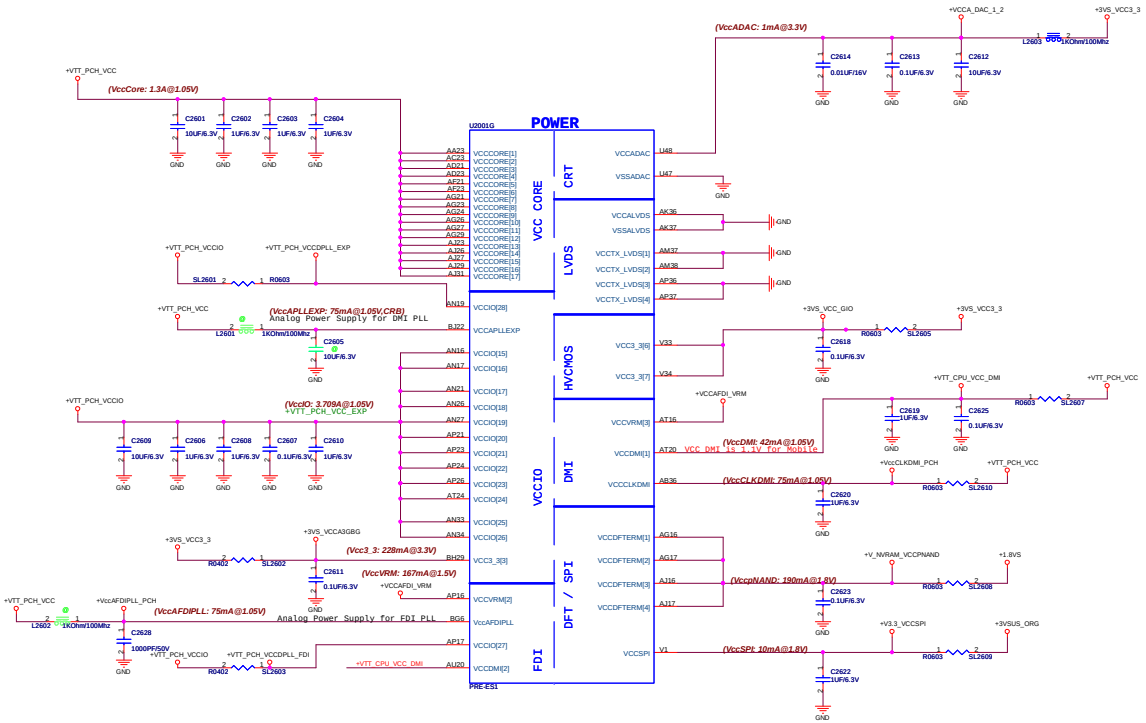
Low=Enabled A16 swap override/ Top-Block swap override
High=Default

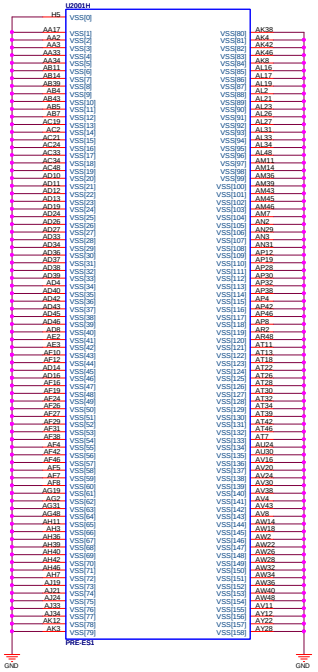
Title : PCH_IBEX(5)_PCI,NVRAM,USB		
ASUSTeK COMPUTER INC.	Engineer: shihhsien_yang	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Wednesday, April 11, 2012	Sheet 24 of 99	



ASUSTeK COMPUTER INC.	Title : PCH_IBEX(6)CPU,GPIO,MISC	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 25 of 99	

All Beads : 0603 !!





VccRAM : 1.5V/1.8V supply for internal PLL and VRMs

ER-024

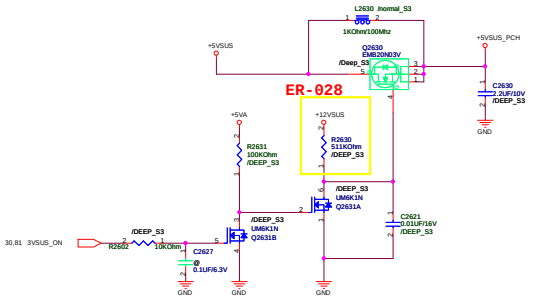
(+VTT_PCH: 4.68A@1.05V)

(+VTT_PCH_VCC: 1.412A@1.05V)

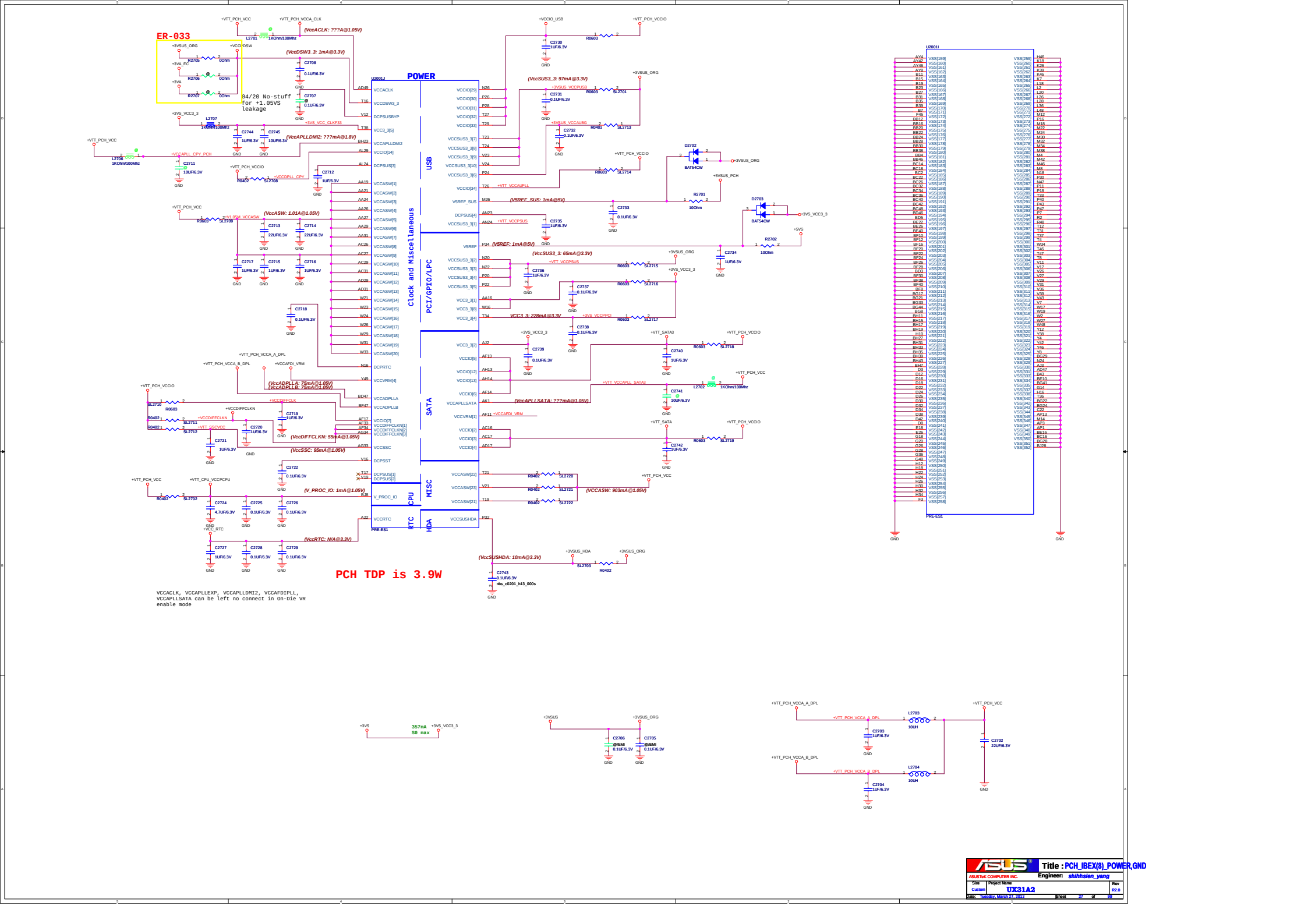
(+VTT_PCH_VCCIO: 3.709A@1.05V)

PCH ICC Description

+VTT	4.68A
+1.5VS	0.167A
+1.8VS	0.19A
+3VS	0.355A
+3VSUS	0.1A



ASUSTeK COMPUTER INC.	Title :	PCH_IBEX(7)_POWER,GND	
	Engineer:	shihhsien_yang	
Size: Custom	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 25 of 99		



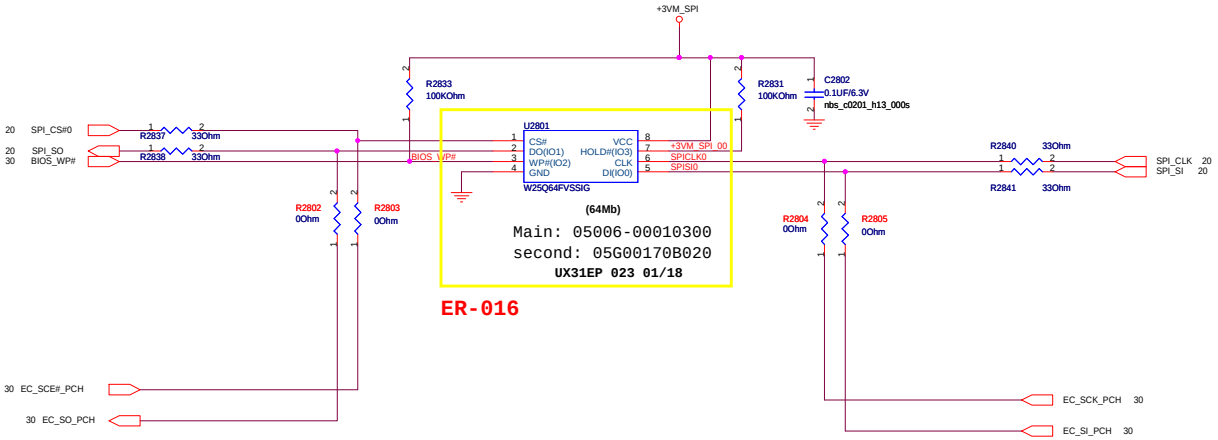
ASUSTeK COMPUTER INC.	Title : PCH_IBEX(8)_POWER,GND		
	Engineer: shihhsien_yang		
Size: Custom	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 27 of 99		

PCH SPI ROM

05/12 delete +3VA

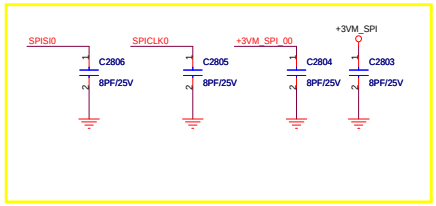
+3VSUS_ORG — +3VM_SPI

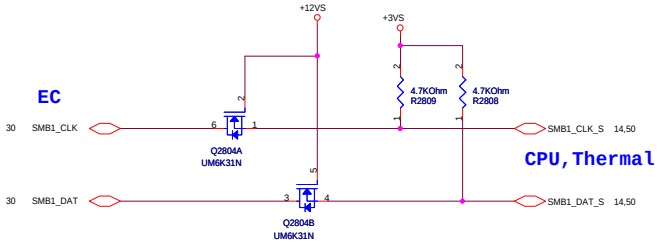
Remove SPI FLASH TOOL CON



ER-016

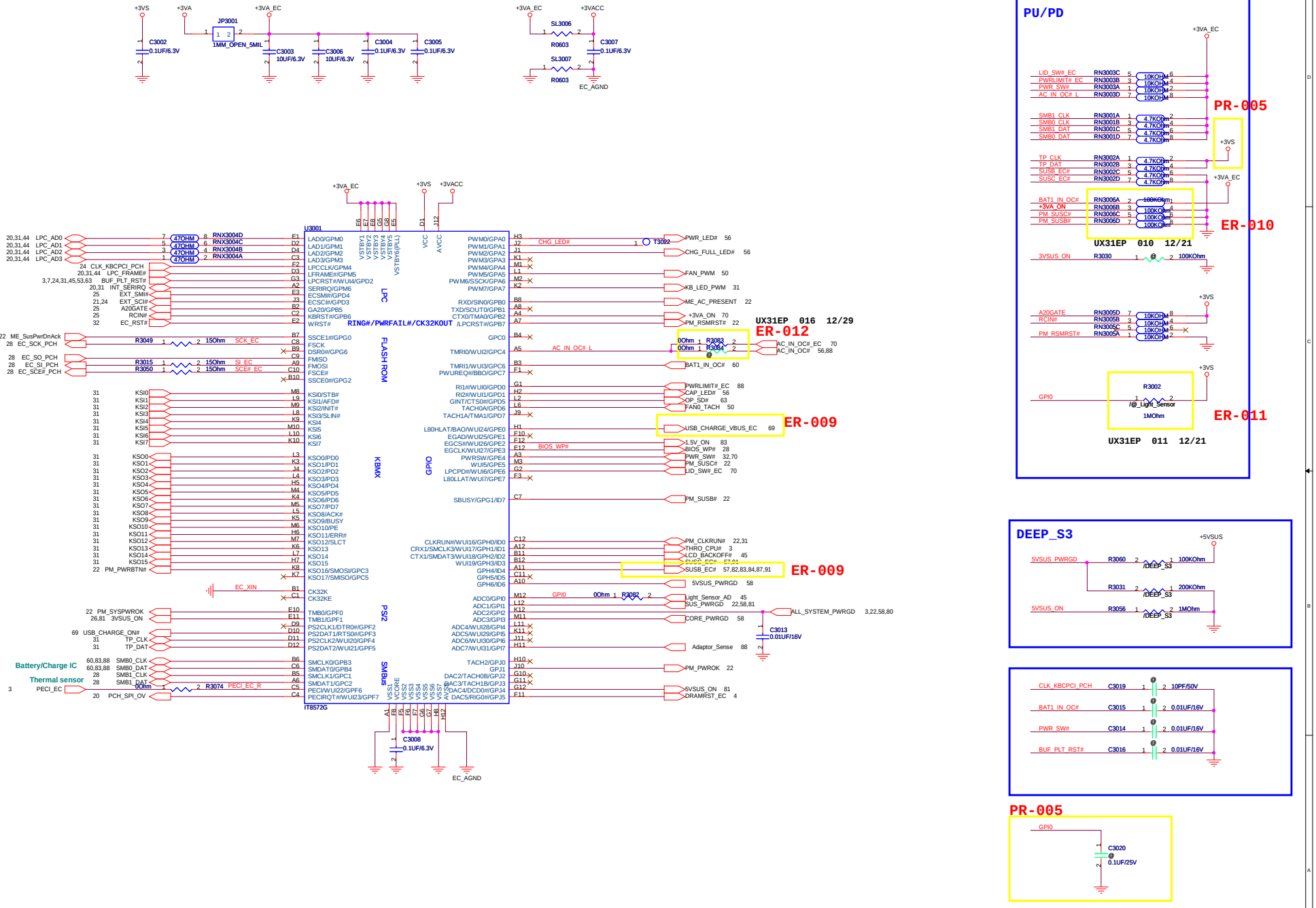
ER-025





ASUSTeK COMPUTER INC.	Title : PCH_SPI ROM,OTH	
	Engineer: Susi_Hong	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 28 of 99	

ASUSTeK COMPUTER INC. NB3	Title : CLK_ICS9LRS3161		
	Engineer: shihhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 29 of 99		



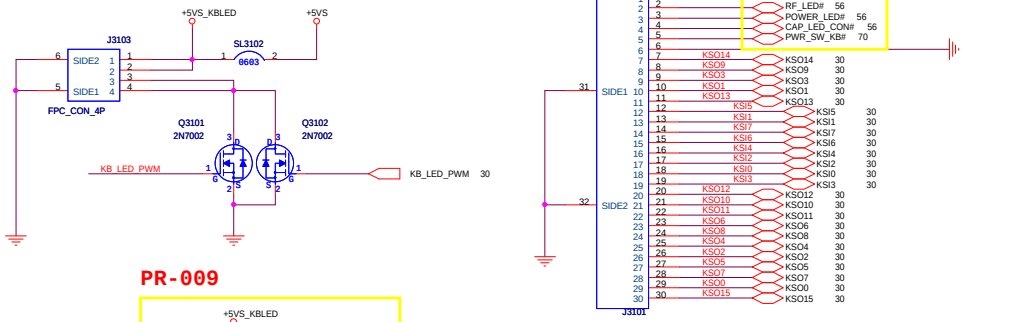
ASUSTeK COMPUTER INC. NB3	Title : KBC_IT8570E_BGA		
	Engineer: Susi_Hong		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 30 of 99		

Keyboard

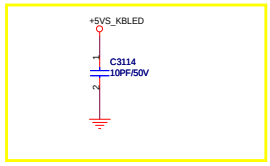
ER-003

Keyboard

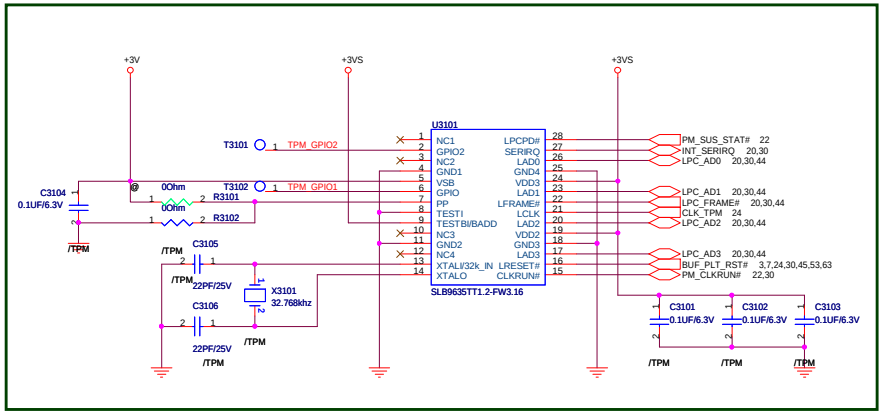
BL_CON



PR-009



TPM



ClickPad Schematic

BOM_Note

Normal TP option -> /PS2TP

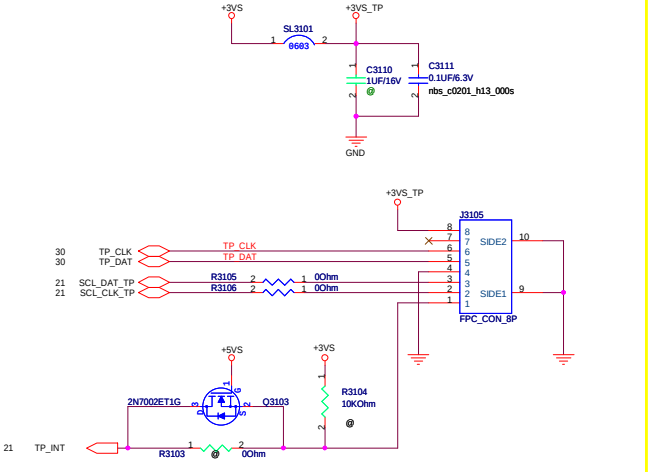
ELAN SMBUS TP option

Synaptics SMBUS TP option

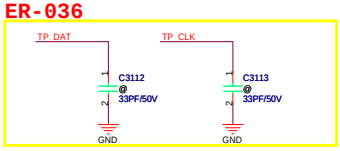
click pad option is for win8 requirement Function

PR-005

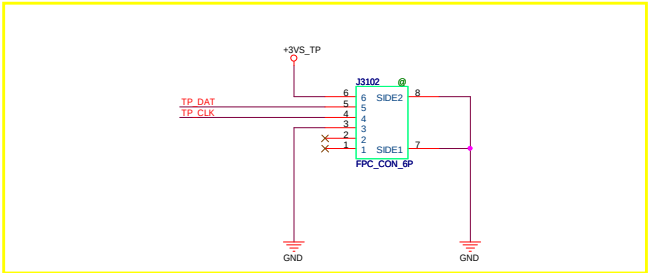
T/P



ER-036

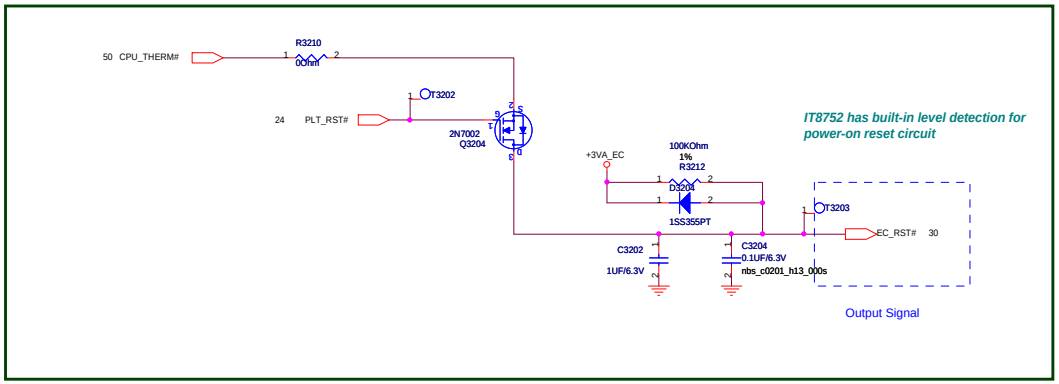


PR-010

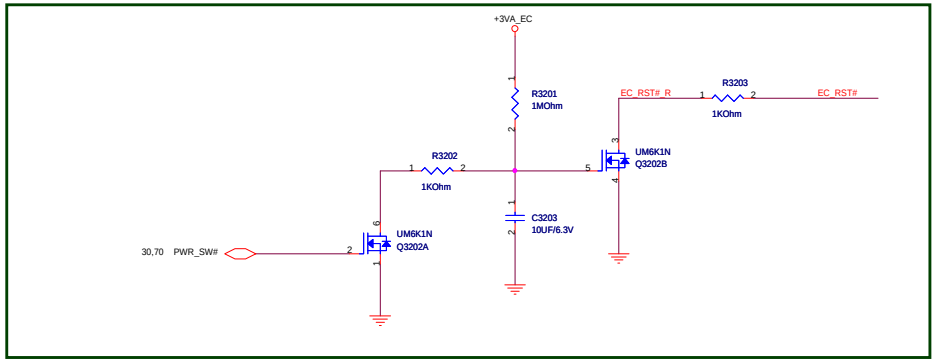


ASUSTeK COMPUTER INC. NB4	Title : EC_KB_TP_TPM	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 31 of 99	

Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)



ASUSTeK COMPUTER INC. NB4	Title : RST_Reset Circuit	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 32 of 99	

Title : LAN-***

ASUSTeK COMPUTER INC. NB3

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 33 of 99

ASUSTeK COMPUTER INC. NB3	Title : LAN-***	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 34 of 99	

Title :	****
ASUSTeK COMPUTER INC. NB1	Engineer: shihhsien_yang
Size: Custom	Project Name: UX31A2
Rev: R2.0	
Date: Tuesday, March 27, 2012	Sheet 35 of 99

<Variant Name>

Title : AUD-****

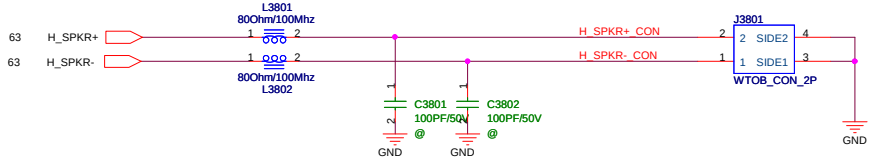
ASUSTeK COMPUTER INC

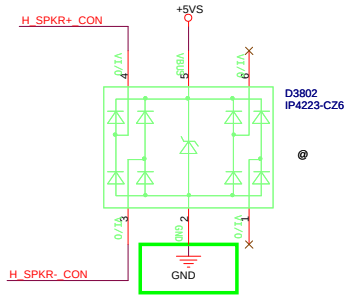
Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 36 of 99

ASUSTeK COMPUTER INC	Title : AUD-****	
	Engineer: shihhsien_yang	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 37 of 99	





<Variant Name>

Title : AUD SPK-R CONN

ASUSTeK COMPUTER INC

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 38 of 99

ASUSTeK COMPUTER INC. NB3	Title : AUD-****	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 39 of 99	

ASUSTeK COMPUTER INC. NB6	Title : CB-****
	Engineer: shihhsien_yang
Size: A	Project Name: UX31A2
	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 40 of 99

Title : CB-****

ASUSTeK COMPUTER INC. NB6

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 41 of 99

<Variant Name>

Title : CB-****

ASUSTeK COMPUTER INC.

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 42 of 99

<Variant Name>

Title : CB-****

ASUSTeK COMPUTER INC.

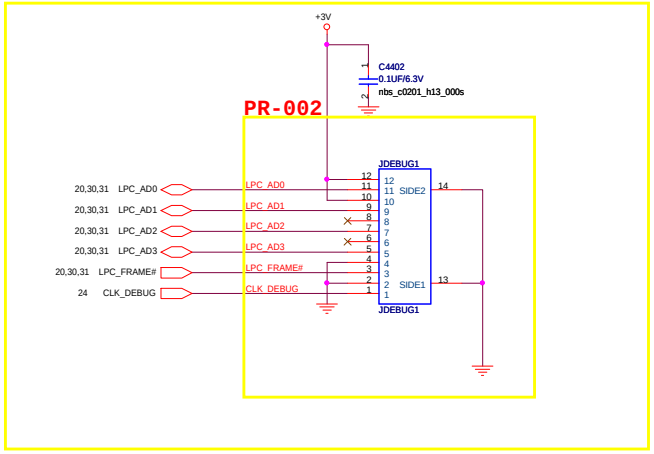
Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

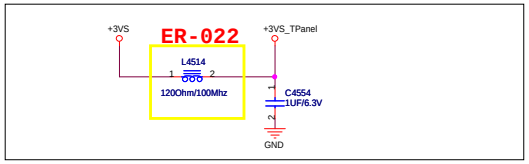
Date: Tuesday, March 27, 2012 Sheet 43 of 99

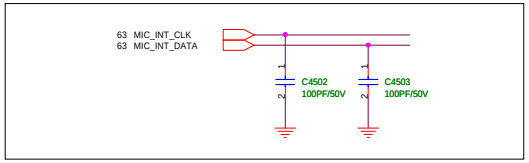
LPC Debug Port

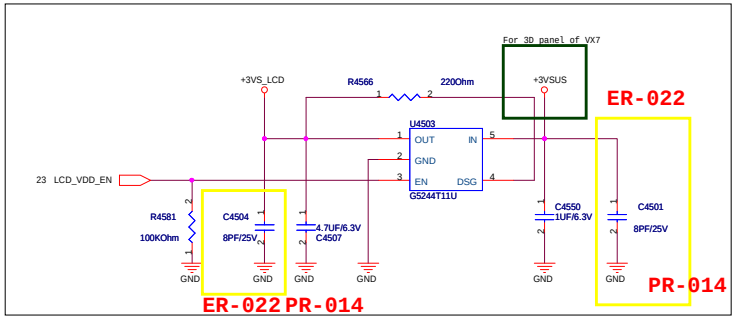
PR-013

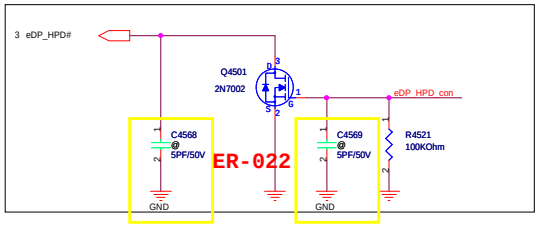


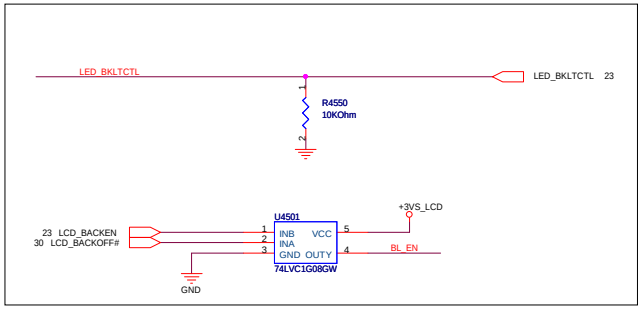
ASUSTeK COMPUTER INC. NB4	Title : BUG_Debug	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 44 of 99	

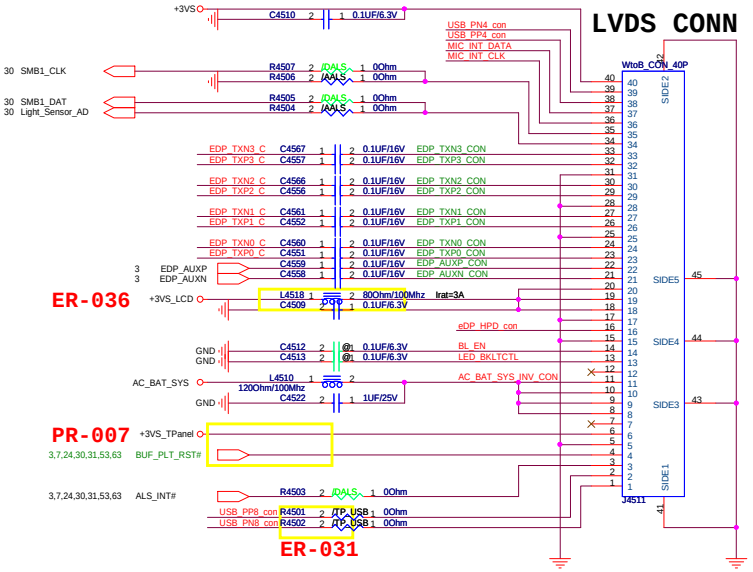


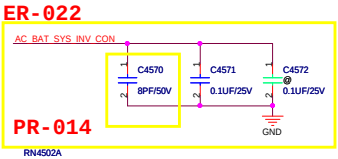


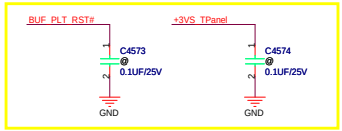


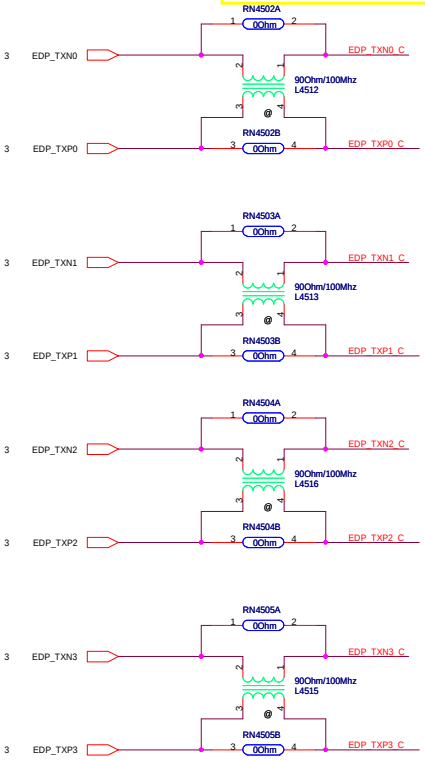


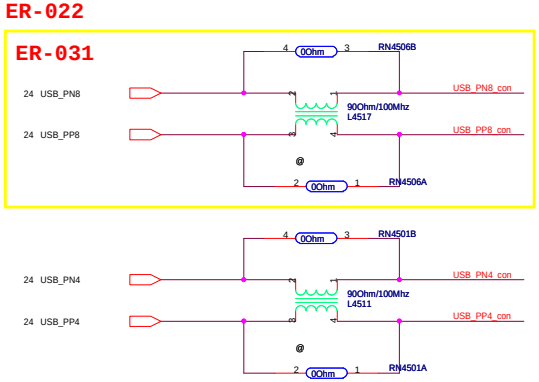












ASUSTeK COMPUTER INC. NB4

Title : LCD Panel_CMOS_DMIC

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

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Main Board

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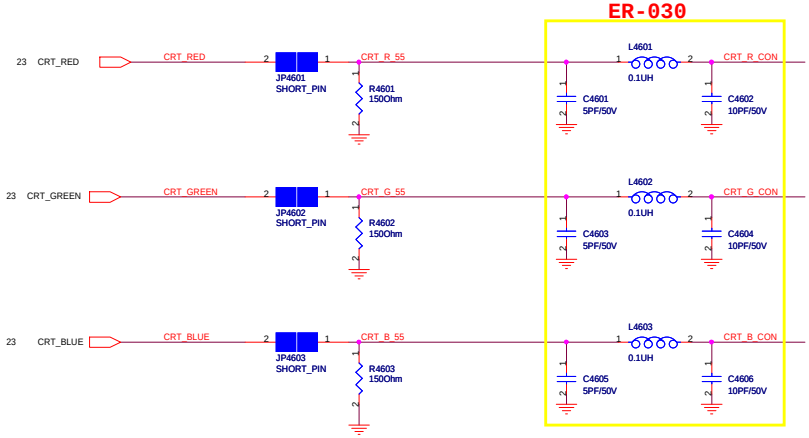
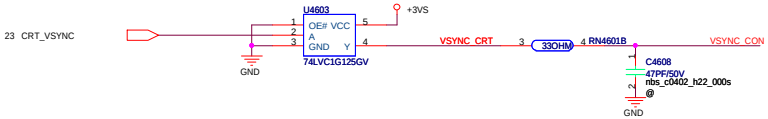
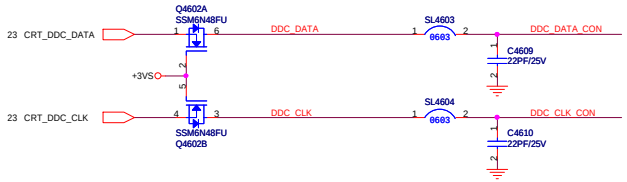
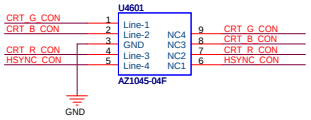
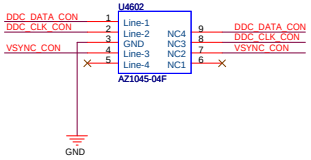




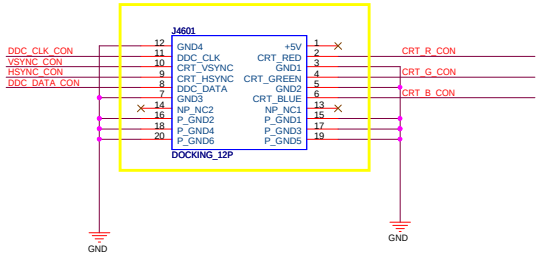






ER-004

UX31EP 004 12/21



ASUSTeK COMPUTER INC. NB4	Title : CRT_D-Sub		
	Engineer: shihhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 46 of 99		

Main Board

Title : Display Port

ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

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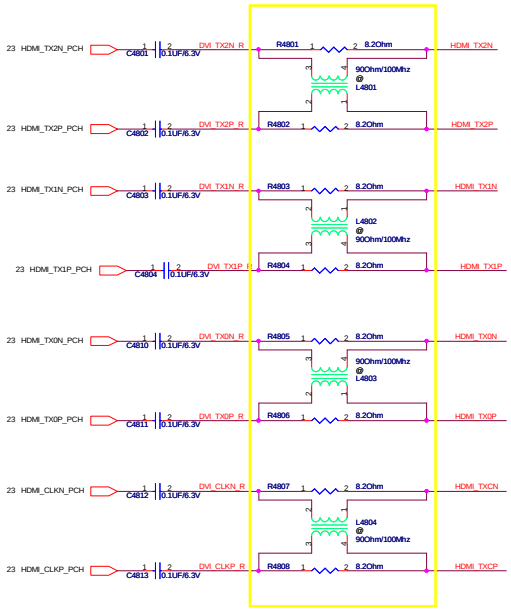
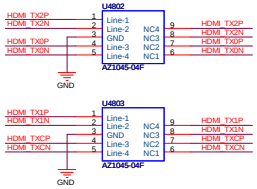
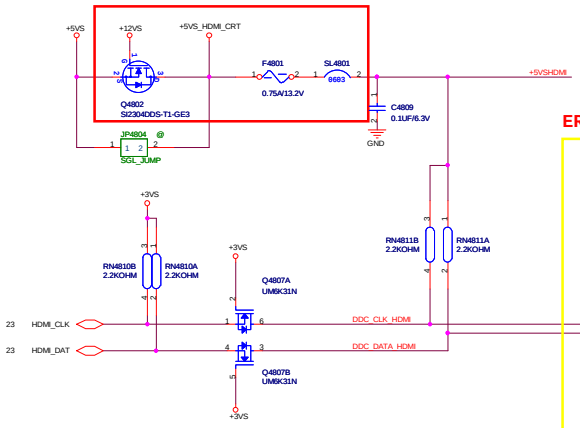
Close to CONNECTOR

Near CON J4801

ER-022

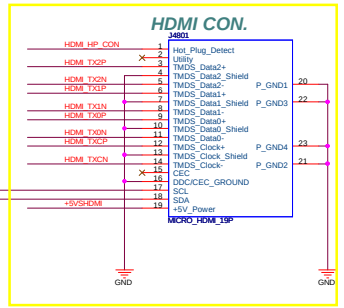


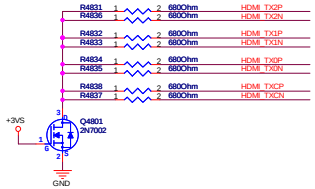


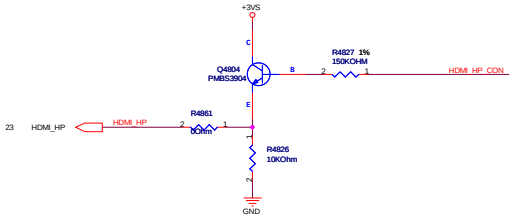


ER-005

UX31EP 005 12/21







ASUSTeK COMPUTER INC

Title : HDMI-type D

Engineer: shihhsien_yang

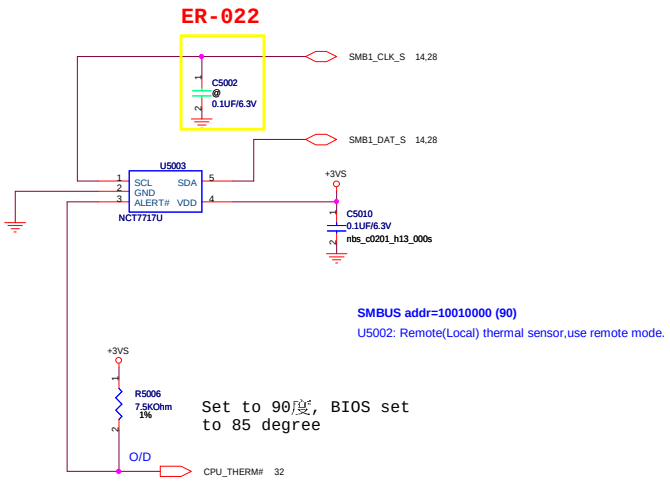
Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 48 of 99

Main Board

ASUSTeK COMPUTER INC. NB4	Title : TV_****		
	Engineer: shihhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 49 of 99		

CPU Thermal Sensor

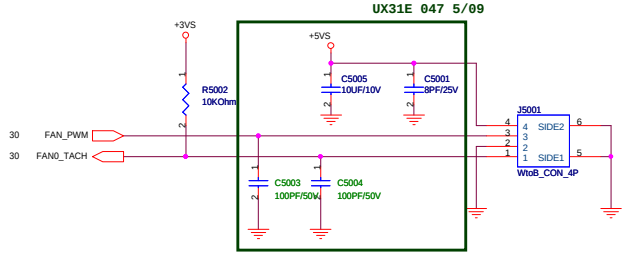


Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

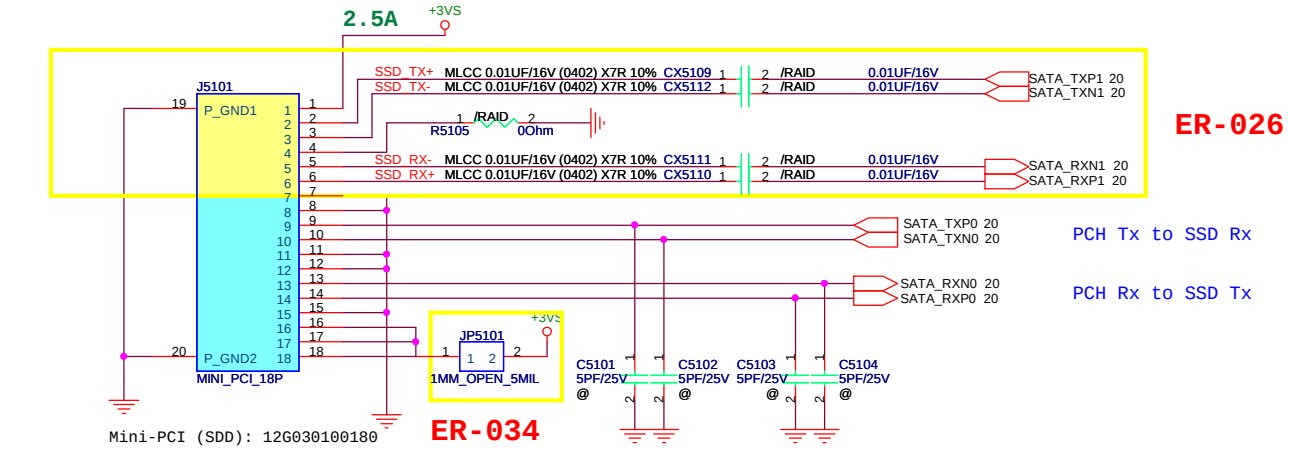
----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
10 mils
----------OTHER SIGNALS

Avoid FSB,Power

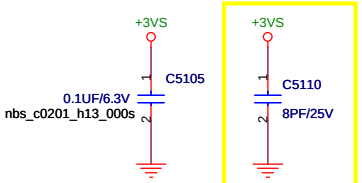
DC FAN Control



ASUSTeK COMPUTER INC. NB3	Title : FAN_Thermal Sensor	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Friday, May 18, 2012	Sheet 50 of 99	



Mini-PCI (SDD): 12G030100180

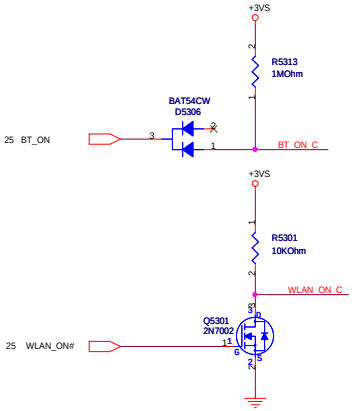


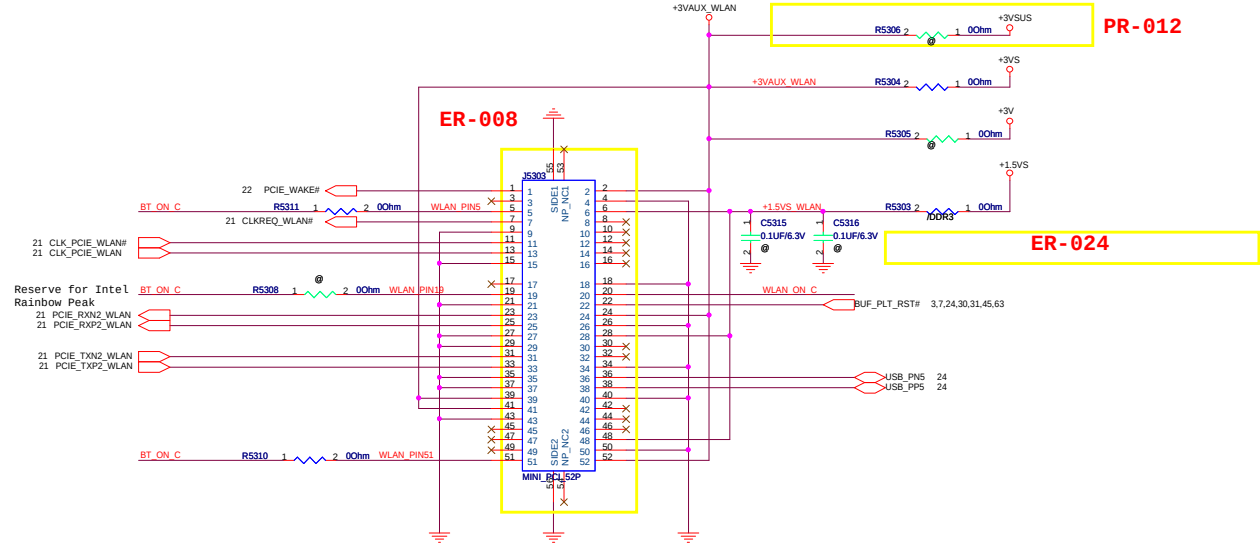
ER-022

ASUSTeK COMPUTER INC. NB4	Title : MiniCard_SSD	
	Engineer: shihhsien_yang	
Size: B	Project Name: UX31A2	Rev: R2.0
Date: Friday, May 18, 2012	Sheet 51 of 99	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : USB_USB Port *3	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 52 of 99	



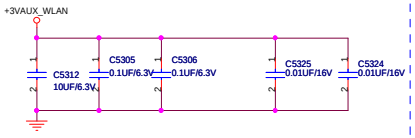


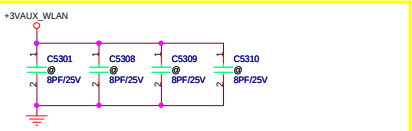
UX31EP 008 12/21

WLAN +3VAUX bypass capactor:

Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VAUX_WLAN source side.





ER-022

ASUSTeK COMPUTER INC. NB6

Title : MINICARD_Wlan & BT

Engineer: Susi_Hong

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 53 of 99

Main Board

Title : BAR_****

ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

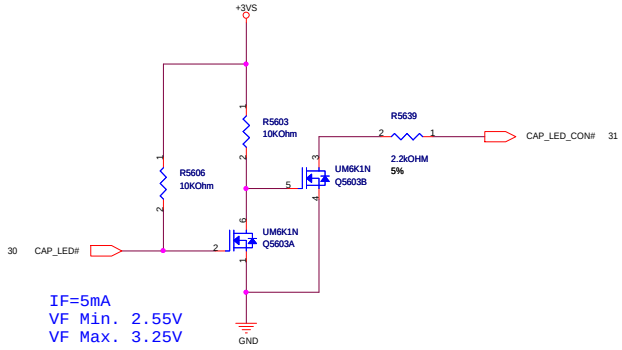
Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 54 of 99

Main Board

ASUSTeK COMPUTER INC. NB4	Title : SIO_****	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 55 of 99	

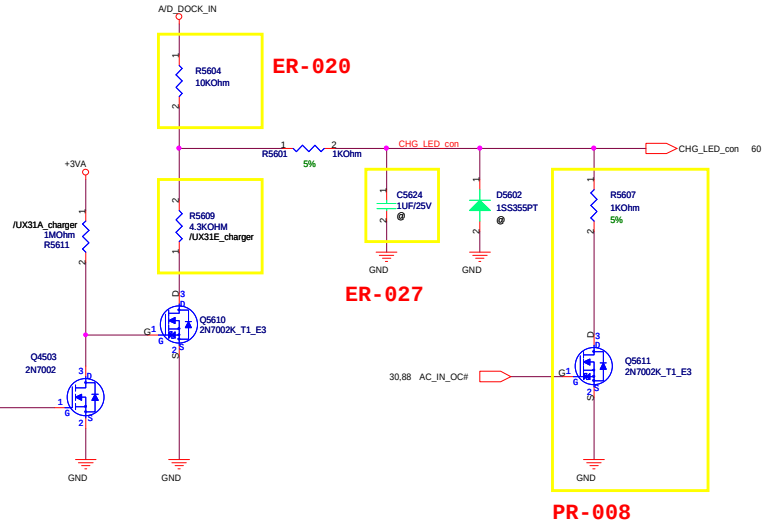
CAPS_LOCK LED



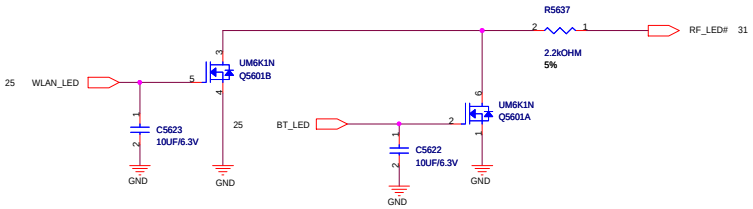
IF=5mA
VF Min. 2.55V
VF Max. 3.25V

For Charge LED

Close J6001



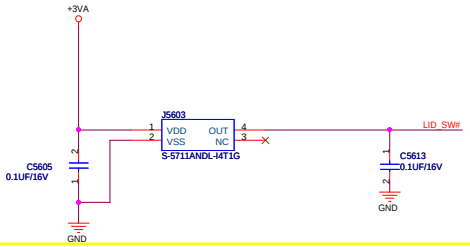
WireLess/BT LED



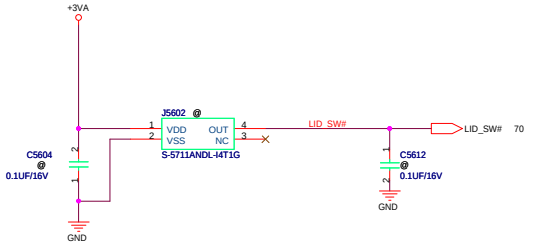
WirelessLAN & Bluetooth Status LED

PR-003

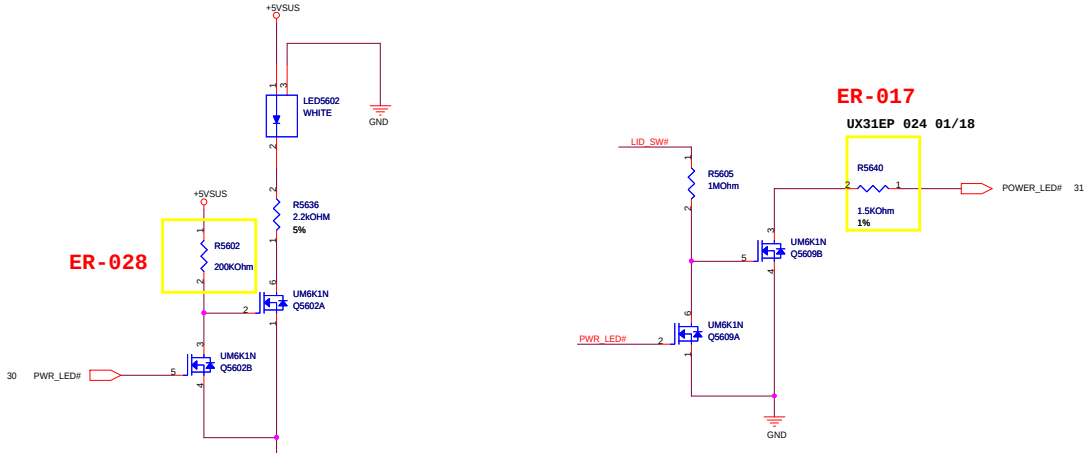
LID SW (no TouchPanel)



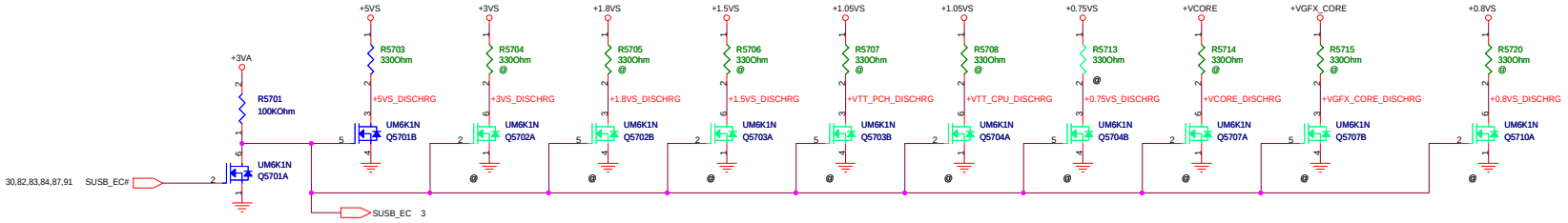
LID SW (for TouchPanel)



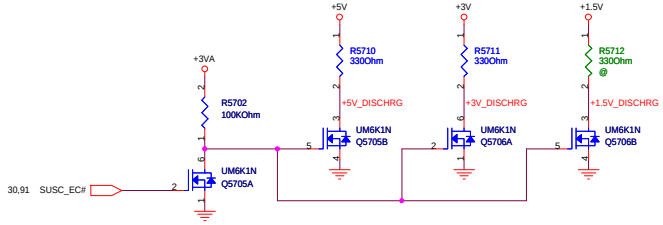
PWR LED



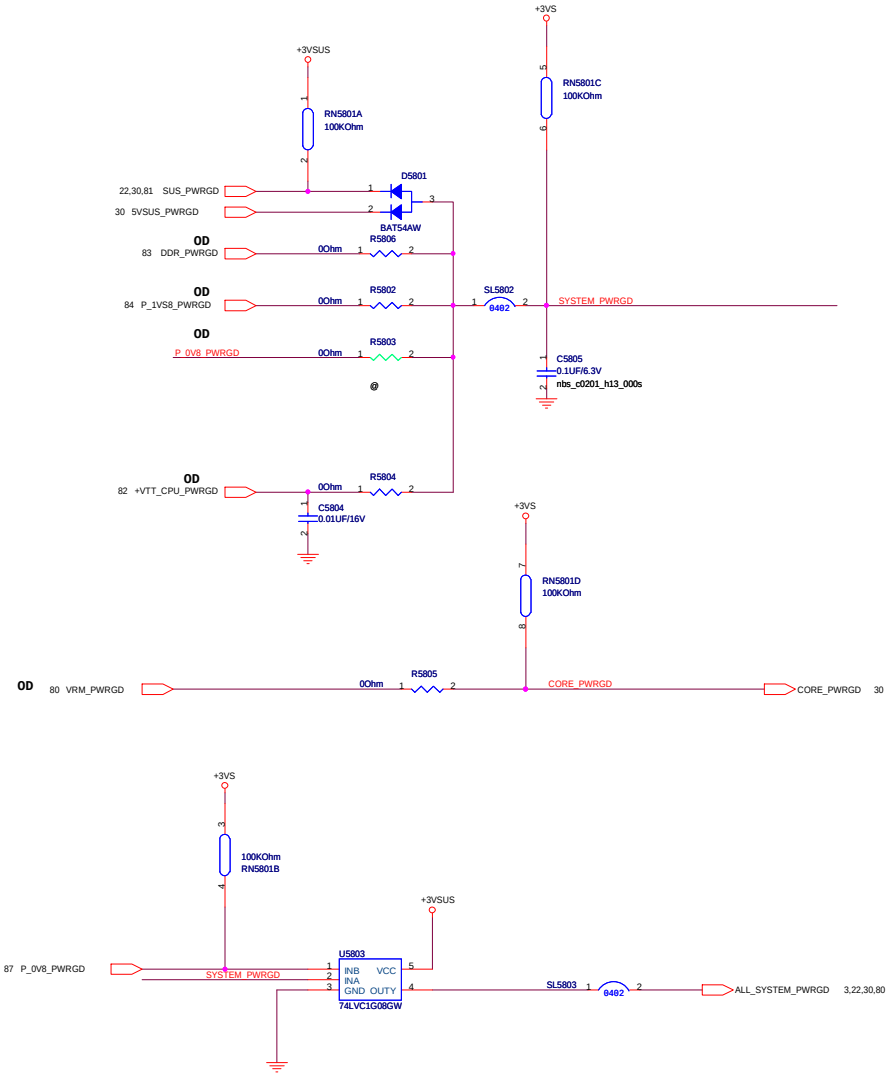
ASUSTeK COMPUTER INC. NB4	Title : LED_Indicator	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 56 of 99	



4/20 Stuff R5710 and R5711



ASUSTeK COMPUTER INC. NB3	Title : DSG_Discharge	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 57 of 99	

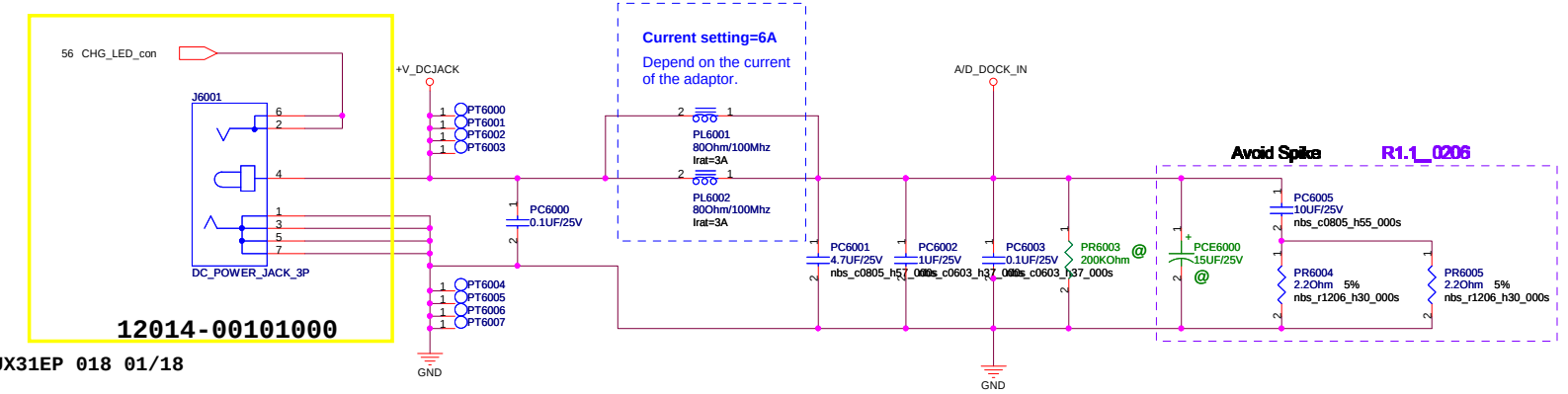


ASUSTeK COMPUTER INC. NB3	Title : PRO_Protect	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 58 of 99	

Main Board

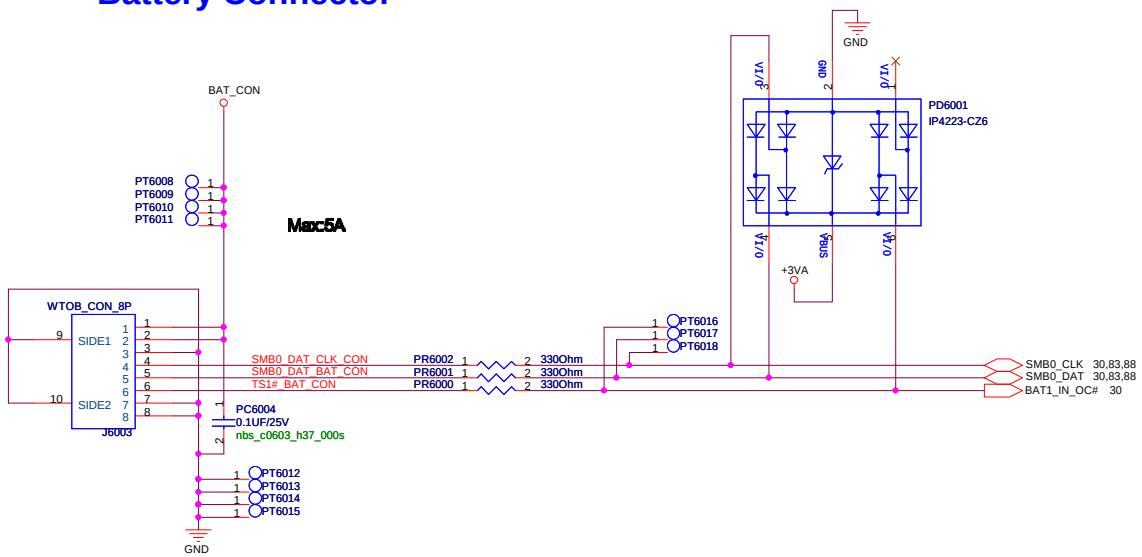
ASUSTeK COMPUTER INC. NB4	Title : DJ_****		
	Engineer: shihhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 59 of 99		

ER-015



UX31EP 018 01/18

Battery Connector



ASUSTeK COMPUTER INC.	Title : DC_DC & BAT IN	
	Engineer: Power	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 60 of 99	

Title : BT

ASUSTeK COMPUTER INC. NB1

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

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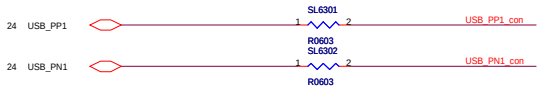
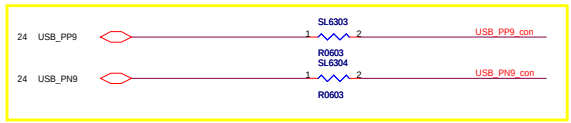
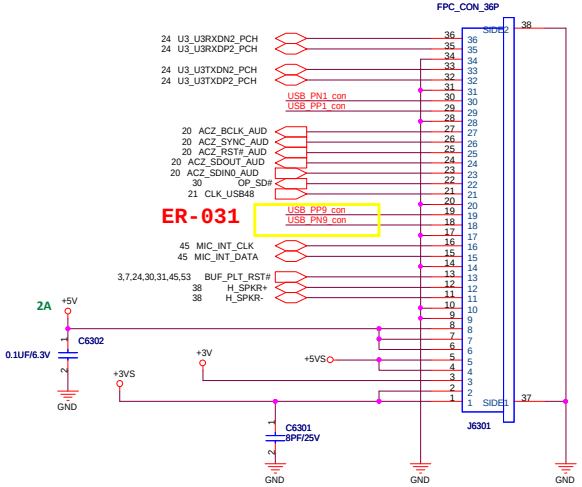
Main Board

ASUSTeK COMPUTER INC. NB4	Title : ****	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 62 of 99	

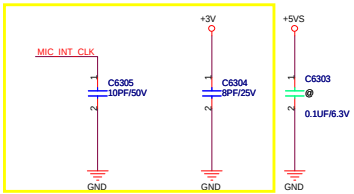


ER-031

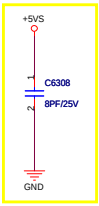




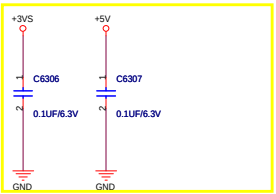
ER-022



PR-011



ER-035



ASUSTeK COMPUTER INC. NB4	Title : B TO B CONN	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Friday, May 18, 2012	Sheet 63 of 99	

Main Board

Title : TUN_TV Tuner

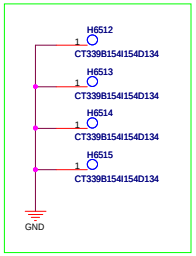
ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

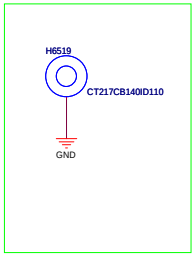
Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 64 of 99

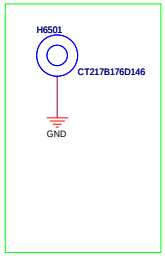
CPU Bracket



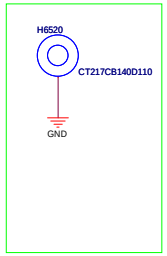
UX31A WLAN NUT



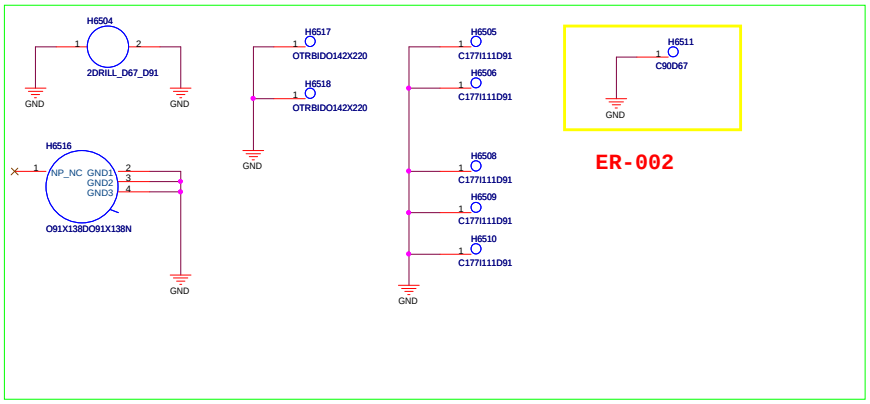
PCH NUT

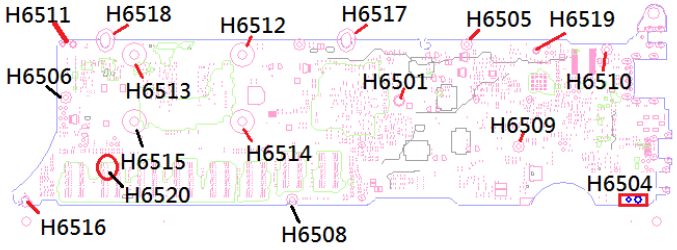


SSD NUT

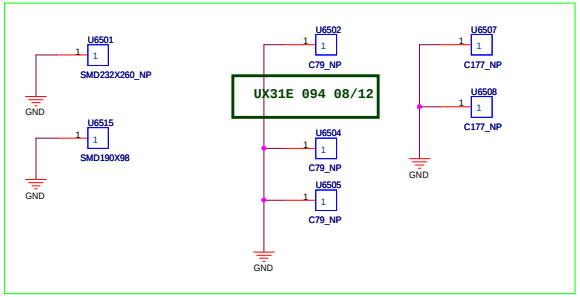


Screw hole

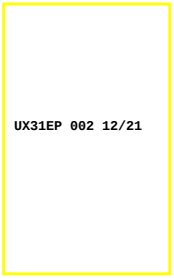




Bottom Pad



EMI Shrapnel



ER-002

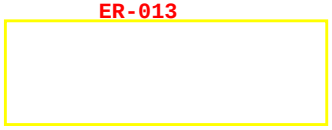
ASUSTeK COMPUTER INC. NB4	Title : ME_Conn & Skew Hole	
	Engineer: Susi_Hong	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 65 of 99	

Main Board

ASUSTeK COMPUTER INC. NB4	Title : ESA_ESATA	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 66 of 99	

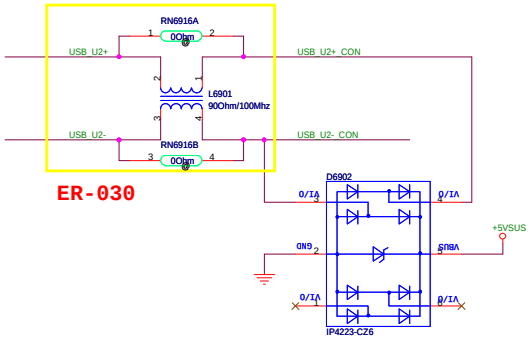
ASUSTeK COMPUTER INC. NB4	Title : PCH_XDP, ONFI		
	Engineer: hhhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 67 of 99		

ER-013

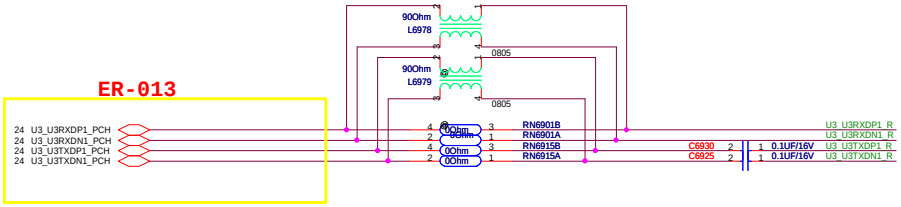


ASUSTeK COMPUTER INC. NB3	Title : ****	
	Engineer: Susi_Hong	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 68 of 99	

USB2.0 EMI-Protection & ESD-Protection

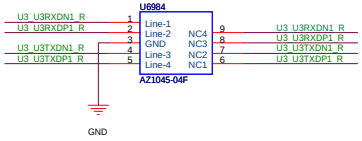


USB3.0 EMI-Protection



USB3.0 ESD-Protection

1st : 07G028076030
ESD PROTECTION AZ1045-04F
2nd : 07G028153010
ESD PROTECTION IP4284CZ10-TB

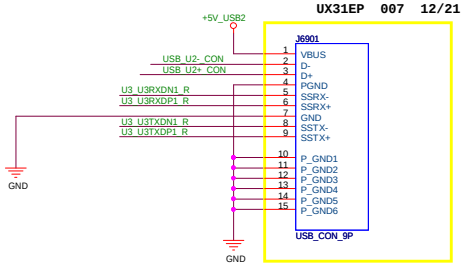


USB30 CONN

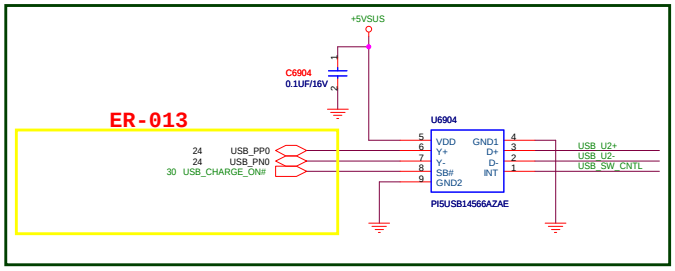
USB30 CONN

UX21 CON 12013-00011600

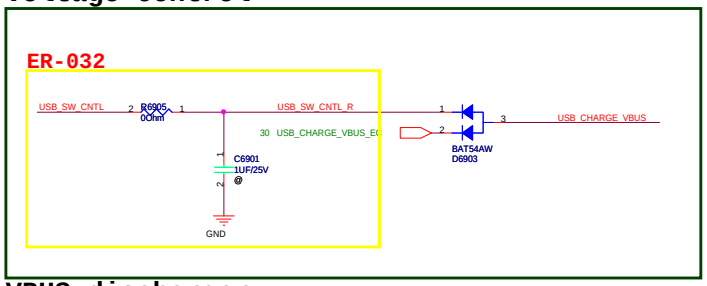
UX31EP 007 12/21



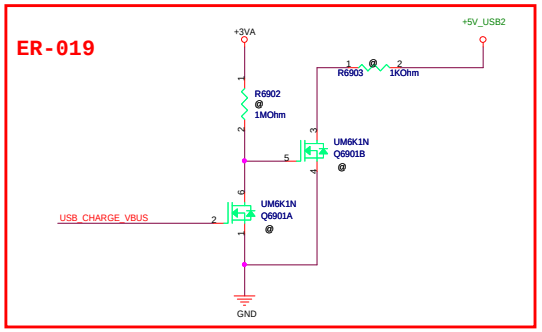
USB Charger



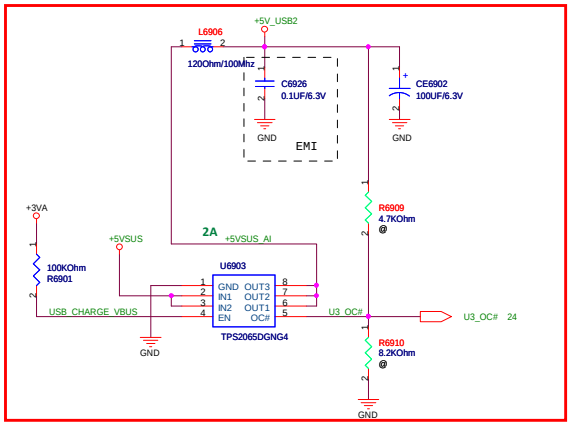
Charger_pwr_control & DC mode low voltage control



VBUS_discharger



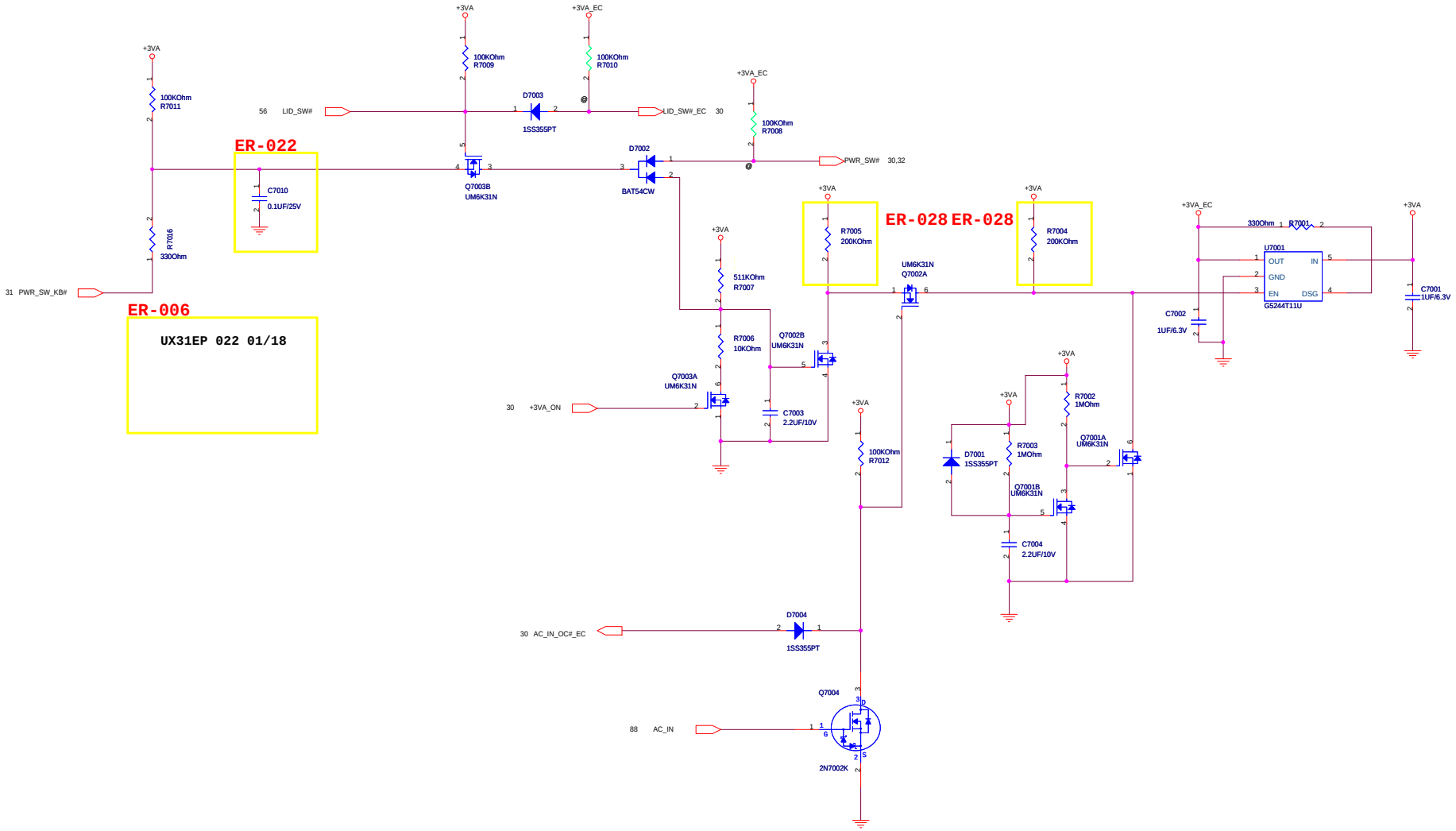
USB_SW VBUS Contorl Circuit



Using TI IC, then the iphone4S can't charger in S4&S3 mode.

ASUSTeK COMPUTER INC. NB4	Title : USB3.0_one Port	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 69 of 99	

Place close to EC



ASUSTeK COMPUTER INC. NB4	Title : EC_PWR_SW	
	Engineer: Susi_Hong	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 70 of 99	

ASUSTeK COMPUTER INC. NB4	Title : VGA_****		
	Engineer: shihhsien_yang		
Size: C	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 71 of 99		

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 72 of 99	

Title : VGA_****

ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 73 of 99

Title : VGA_****		
ASUSTeK COMPUTER INC. NB4	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 74 of 99	

Title : VGA_****

ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 75 of 99

Title : VGA_****		
ASUSTeK COMPUTER INC. NB4	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 76 of 99	

Title : VGA_****

ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 77 of 99

ASUSTeK COMPUTER INC. NB4	Title : VGA_****	
	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 78 of 99	

Title : VGA_****

ASUSTeK COMPUTER INC. NB4

Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

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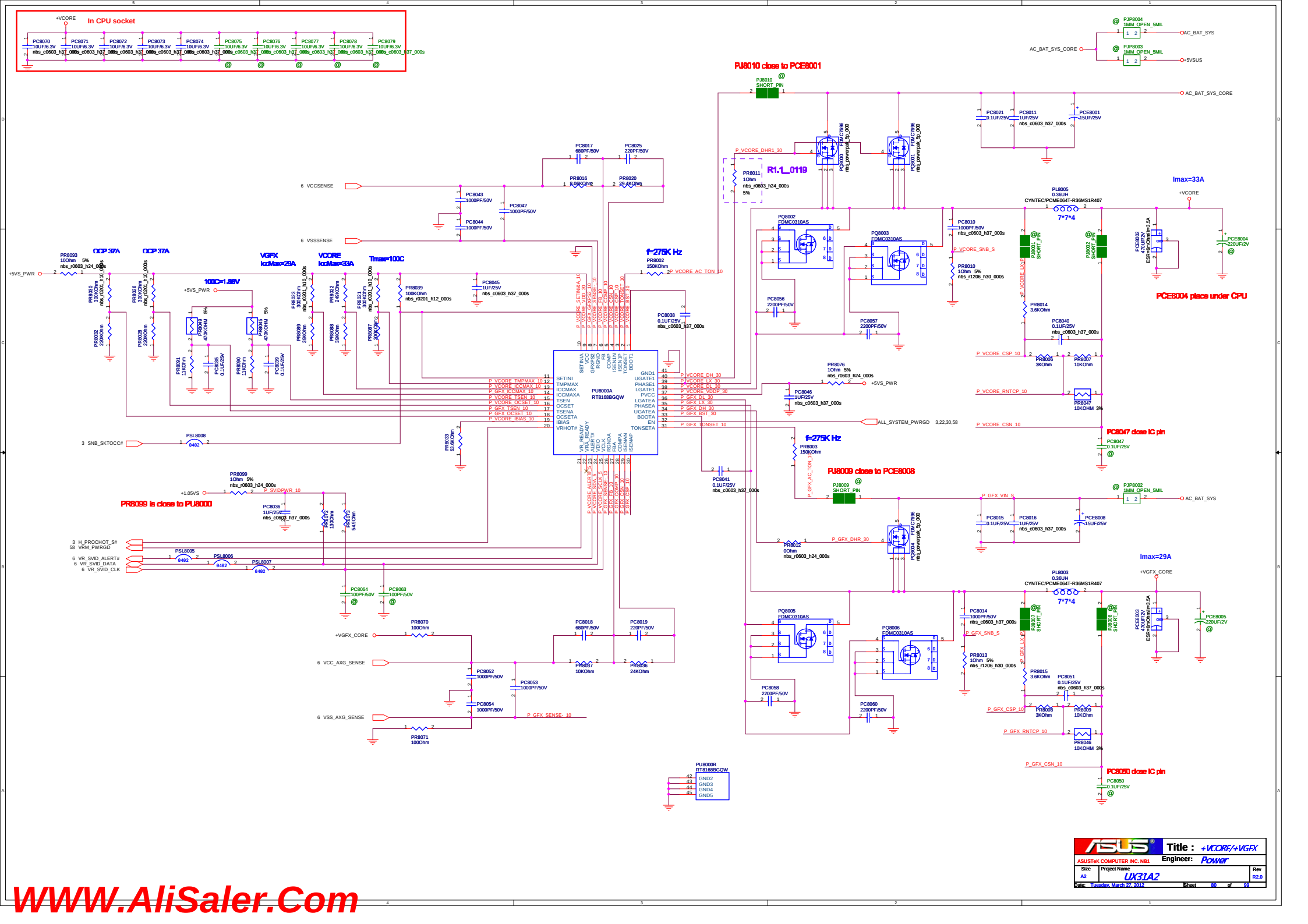

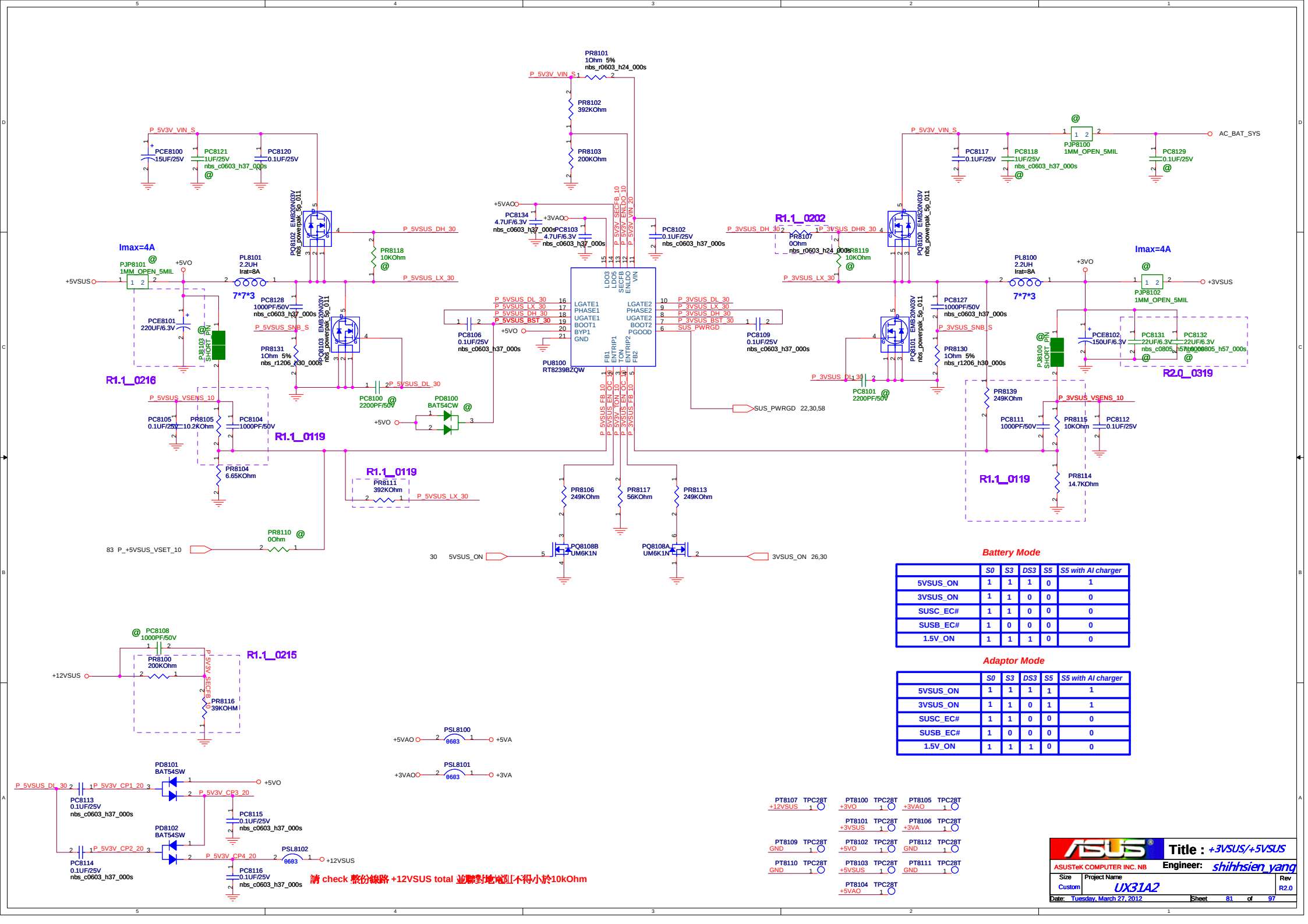

Battery Mode

	S0	S3	DS3	S5	S5 with AI charger
5VSUS_ON	1	1	1	0	1
3VSUS_ON	1	1	0	0	0
SUSC_EC#	1	1	0	0	0
SUSB_EC#	1	0	0	0	0
1.5V_ON	1	1	1	0	0

Adaptor Mode

	S0	S3	DS3	S5	S5 with AI charger
5VSUS_ON	1	1	1	1	1
3VSUS_ON	1	1	0	1	1
SUSC_EC#	1	1	0	0	0
SUSB_EC#	1	0	0	0	0
1.5V_ON	1	1	1	0	0

ASUSTeK COMPUTER INC. NB

Title : +3VSUS/+5VSUS

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

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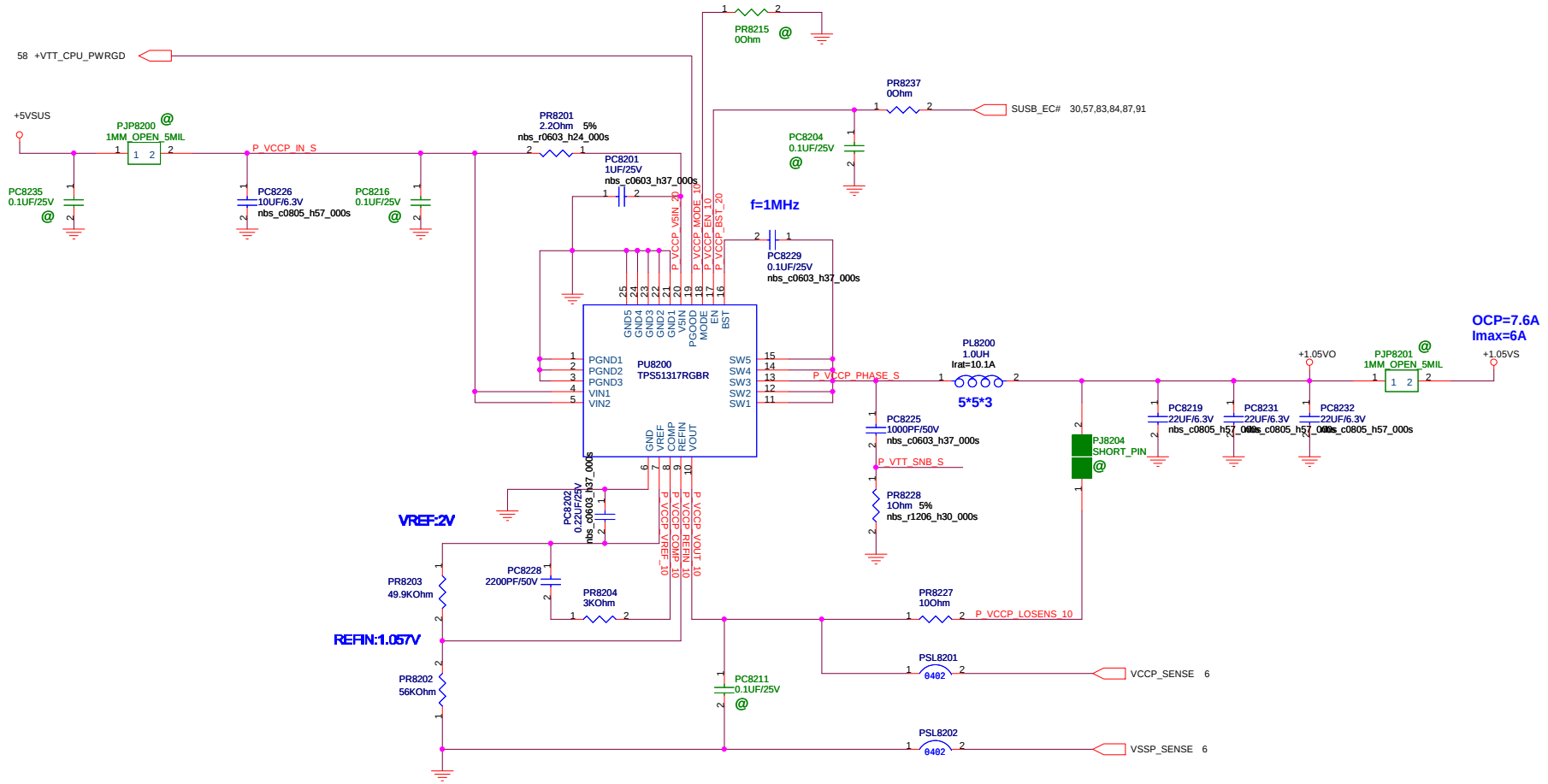
+VTT_CPU & +VTT_PCH & +1.05VS POWER SUPPLY



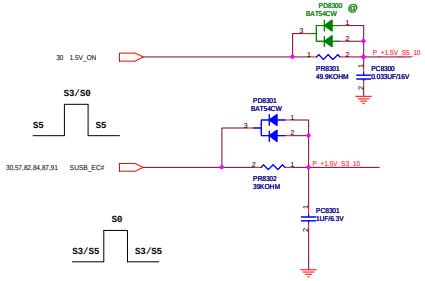
<Variant Name>

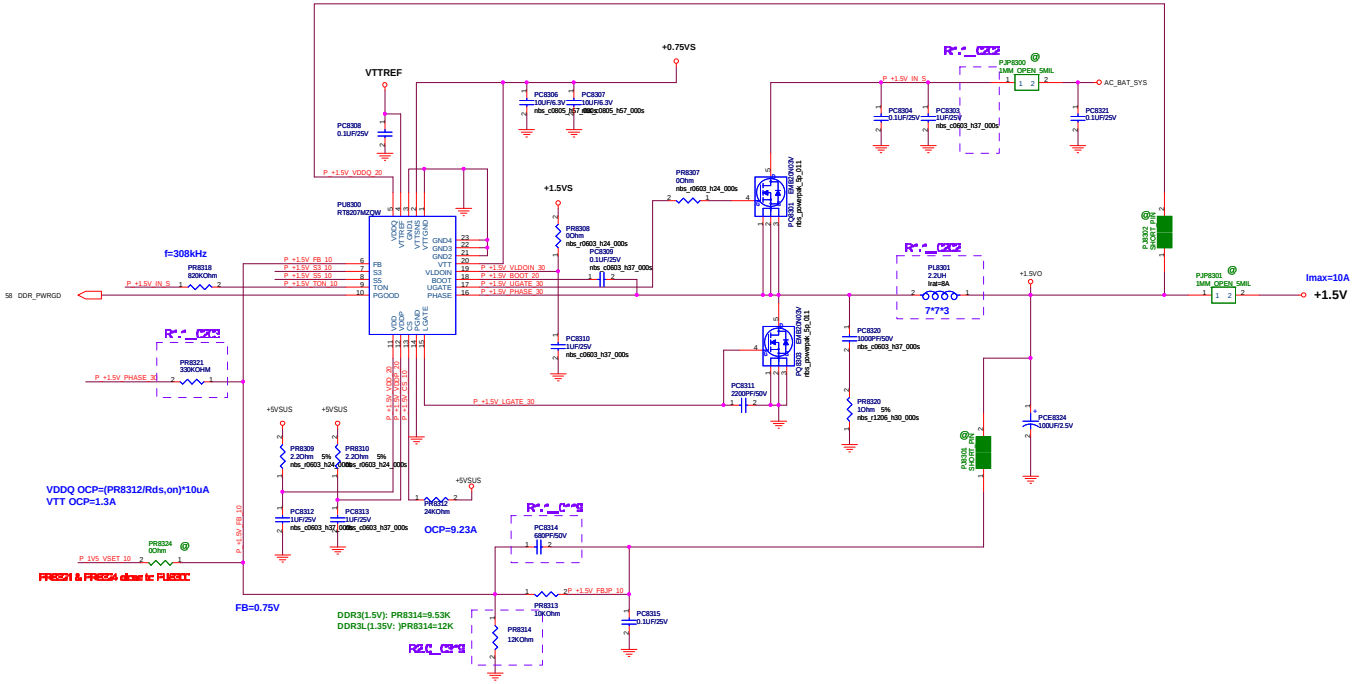
ASUSTeK COMPUTER INC. NB	Title : +1.05VS	
	Engineer: shihhsien_yang	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 82 of 99	

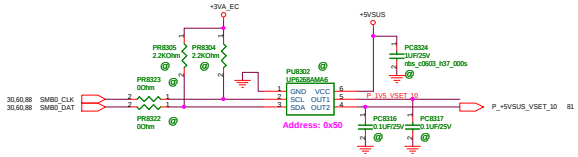
S3 And S5 Truth Table

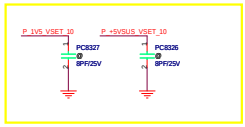
State	S3	S5	VDDQ
S0	1	1	On
S3	0	1	On
S4/S5	0	0	On

State	VTTREF	VTT
S0	On	On
S3	On	Off (Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)



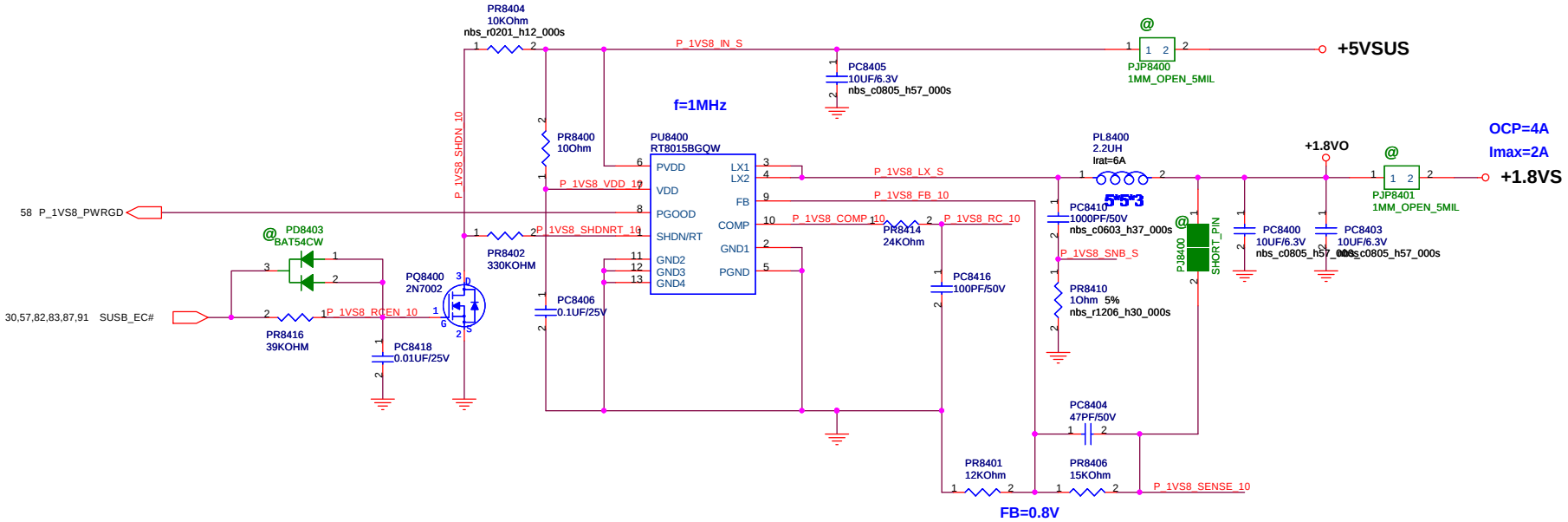






ASUSTek Computer INC.	Title : +1.5V/+0.75VS		
Engineer: shihhsien_wang			
Size: Custom	Project Name: UX31A2		Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet: 68 of 88		

+1.8VS POWER SUPPLY



PT8401 TPC28T
+1.8VS 1

PT8402 TPC28T
GND 1

PT8403 TPC28T
GND 1

ASUSTeK COMPUTER INC.

Title : +1.8VS

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 84 of 99

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : POWER_I/O_NVDD	
	Engineer: shihhsien_yang	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 85 of 99	

<Variant Name>

Title : POWER_+VGFX_CORE

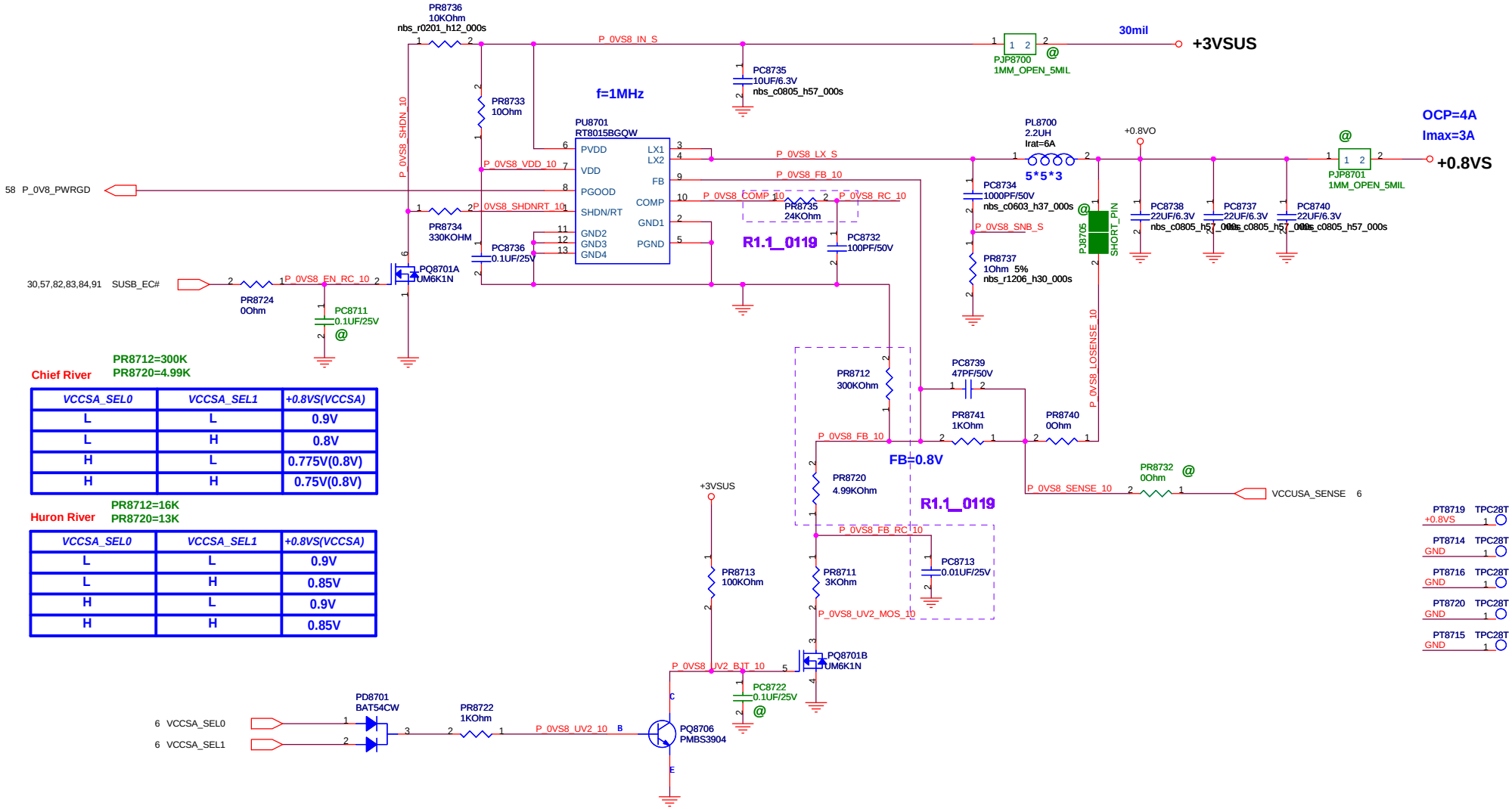
ASUSTeK COMPUTER INC.

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 86 of 99

+0.8VS POWER SUPPLY



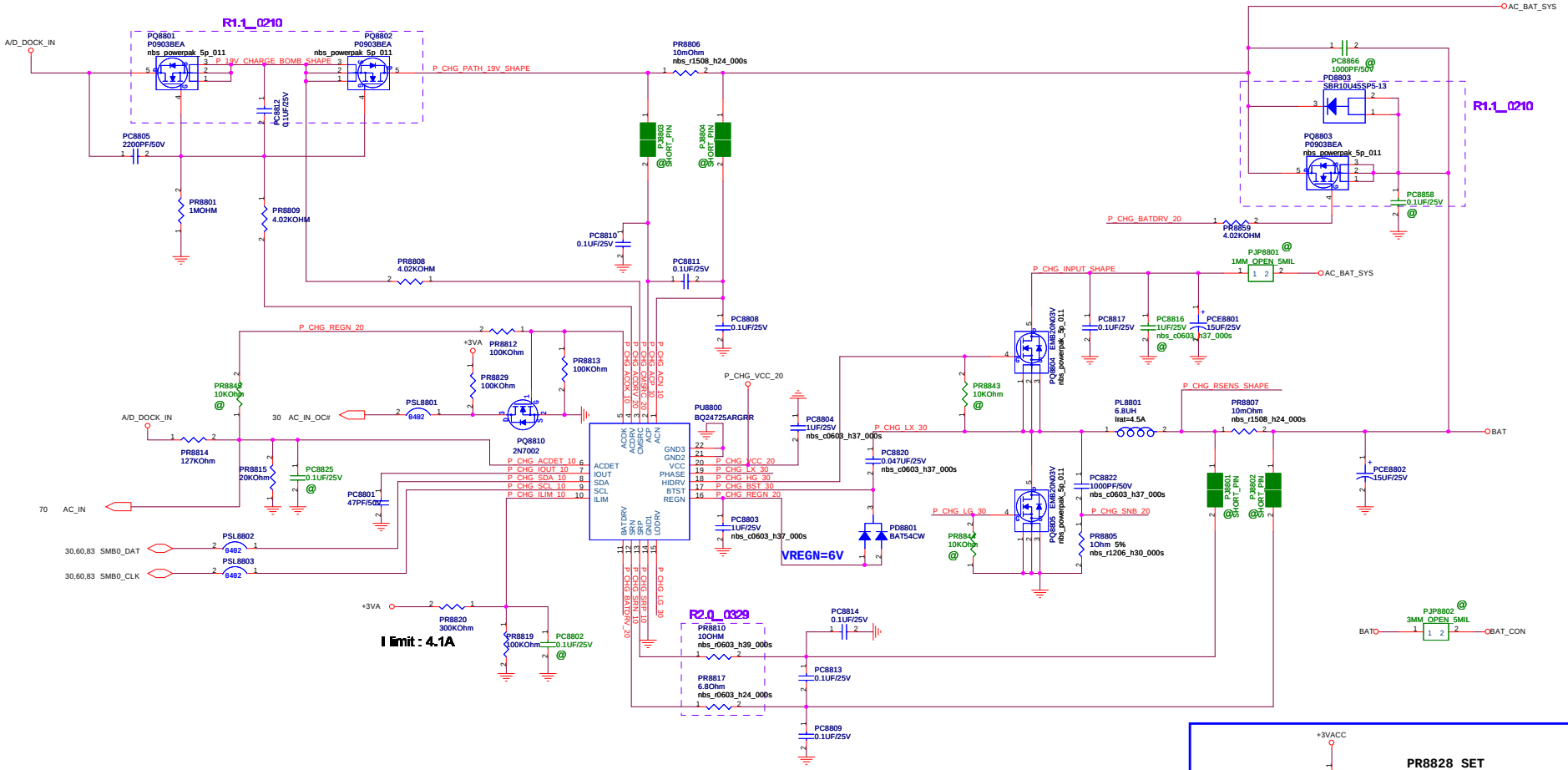
VCCSA_SEL0	VCCSA_SEL1	+0.8VS(VCCSA)
L	L	0.9V
L	H	0.8V
H	L	0.775V(0.8V)
H	H	0.75V(0.8V)

Huron River

PR8712=16K
PR8720=13K

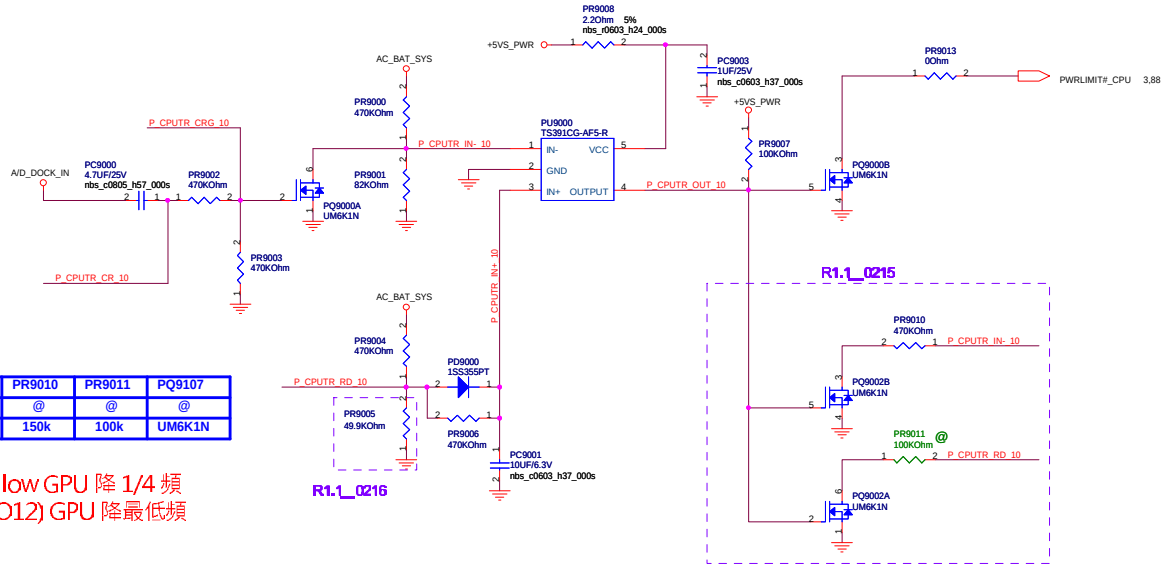
VCCSA_SEL0	VCCSA_SEL1	+0.8VS(VCCSA)
L	L	0.9V
L	H	0.85V
H	L	0.9V
H	H	0.85V

Title :	+0.8VS	
ASUSTeK COMPUTER INC.	Engineer:	shihhsien_yang
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 87 of 99	



ASUSTeK COMPUTER INC. NB3	Title : Charger	
	Engineer: POWER	
Size: Custom	Project Name: UX Series	Rev: 1.0
Date: Wednesday, April 11, 2012	Sheet 88 of 97	

Title :	PW_****	
ASUSTeK COMPUTER INC. NB1	Engineer:	shihhsien_yang
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 89 of 99	



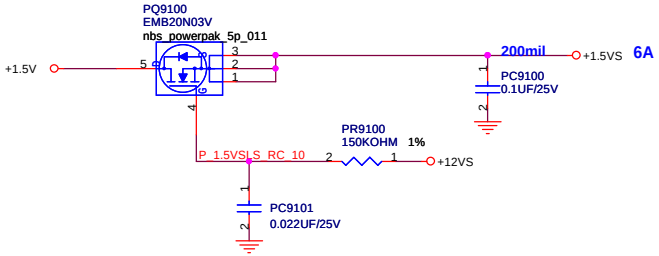
請遠離熱源！

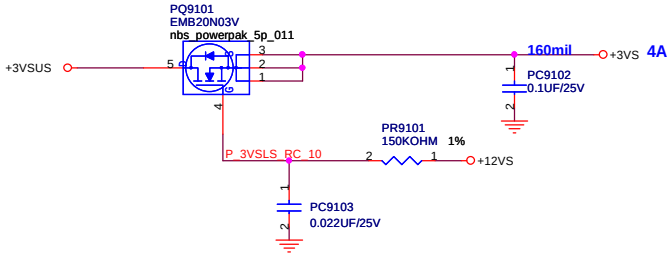
	PR9005	PR9010	PR9011	PQ9107
UX series 2S BAT	62k	@	@	@
Other series 3S/4S BAT	75k	150k	100k	UM6K1N

VGA_Alert (GPIO9) pull low GPU 降 1/4 頻
dGPU_PD pull low (GPIO12) GPU 降最低頻

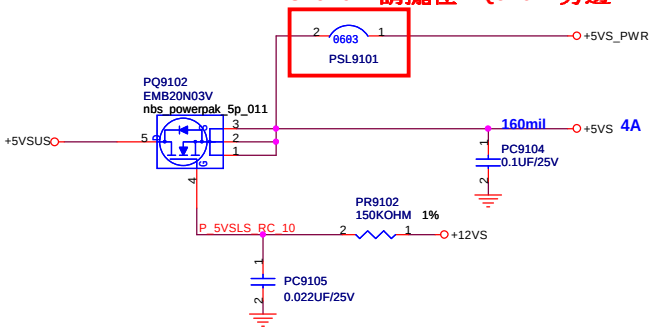
ASUSTeK COMPUTER INC. NB1	Title : HW_Throttle	
	Engineer: Power	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 90 of 99	

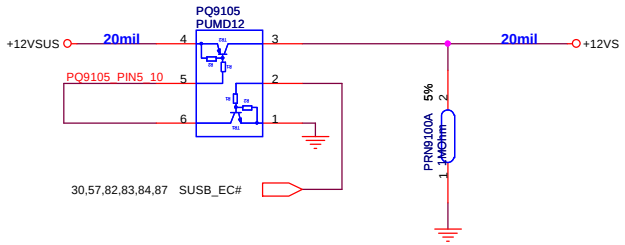
SUSB#_PWR POWER



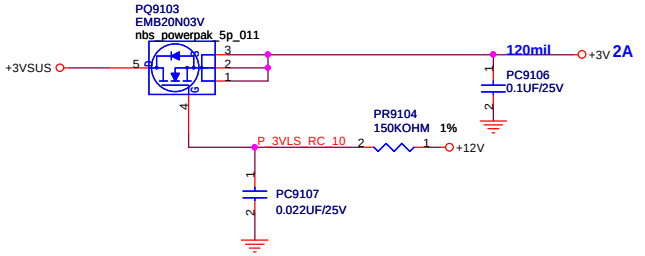


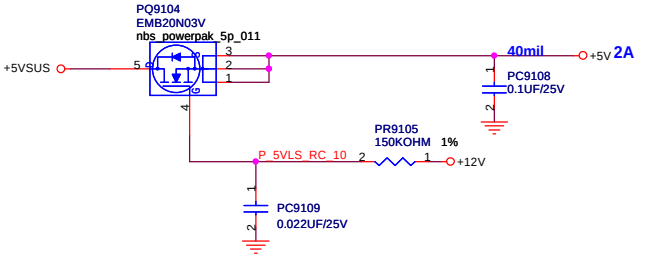
PSL9101 請擺在 PQ9102 旁邊

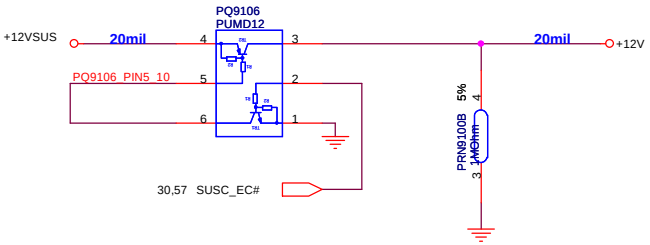


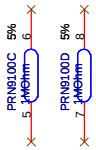


SUSC#_PWR POWER



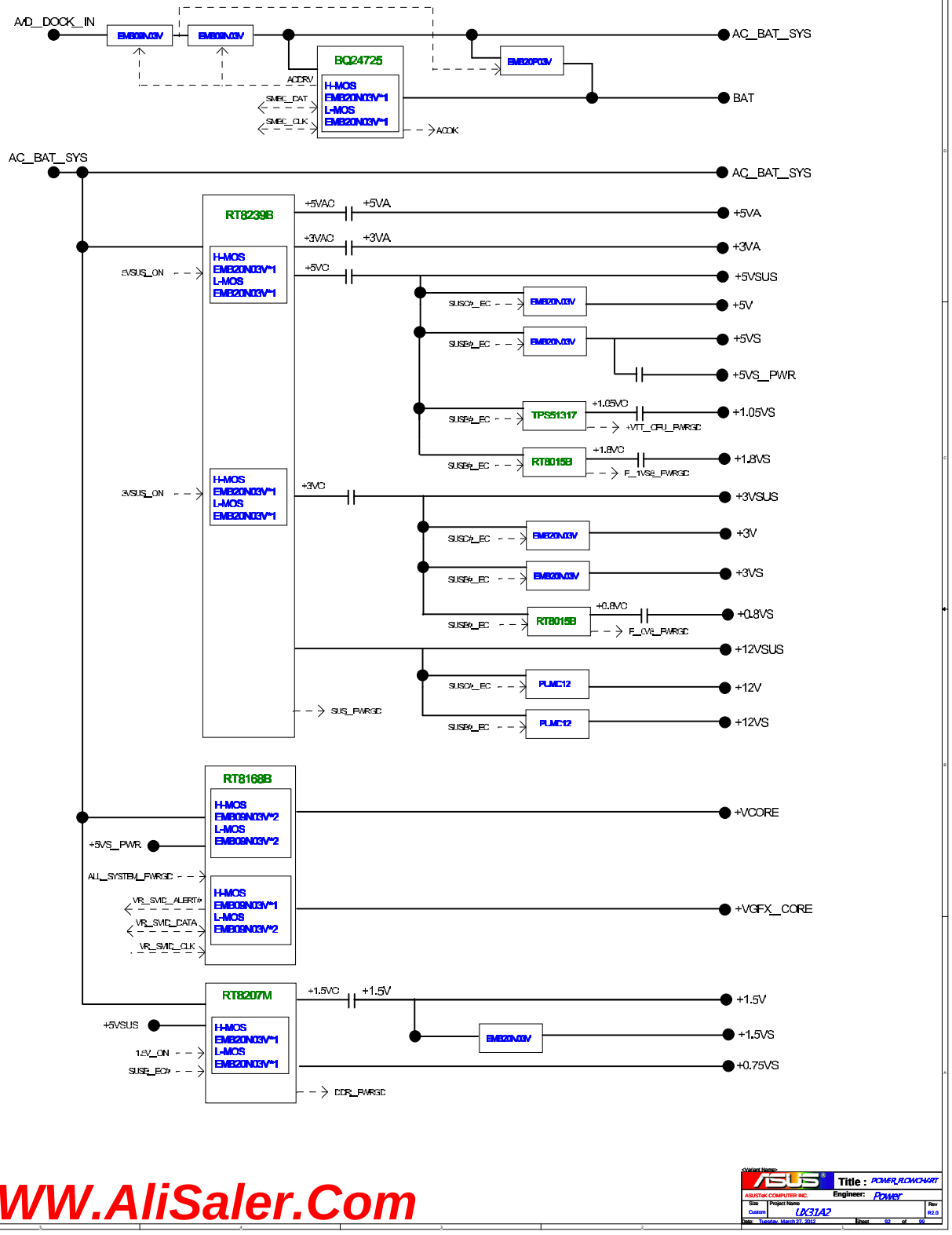






<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : Load Switch	
	Engineer: shihhsien_yang	
Size: Custom	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 91 of 98	



<Variant Name>
ASUSTeK COMPUTER INC.
Title : POWER_FLOWCHART
Engineer: Power
Size: Custom
Project Name: UX31A2
Rev: R2.0
Date: Tuesday, March 27, 2012
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AC_BAT_SYS	AC_BAT_SYS	45,80,81,83,88,90
BAT	BAT	88
+3VAO	+3VAO	81
+5VA	+5VA	26,81
+3VA	+3VA	7,20,27,30,56,57,60,69,70,81,88
+5VAO	+5VAO	81
+5VSUS_PCH	+5VSUS_PCH	26,27
+5VSUS	+5VSUS	26,30,31,56,69,80,81,82,83,84,91
+5V	+5V	57,63,91
+5VS	+5VS	20,27,31,38,46,48,50,57,63,91
+3VSUS	+3VSUS	6,20,21,22,24,25,26,27,28,45,53,58,81,87,91
+3V	+3V	3,24,31,44,53,57,63,91
+3VS	+3VS	7,14,20,21,22,23,24,25,26,27,28,30,31,45,46,48,50,51,53,56,57,58,63,91
+12VSUS	+12VSUS	26,81,91
+12V	+12V	91
+12VS	+12VS	21,28,48,91
+1.8VS	+1.8VS	6,26,57,84
+0.75VS	+0.75VS	13,57,83
+1.5V	+1.5V	4,13,14,15,19,57,83,91
+1.5VS	+1.5VS	3,6,26,53,57,83,91
+VGFX_CORE	+VGFX_CORE	6,57,80
+VCORE	+VCORE	6,57,80
+1.05VS	+1.05VS	3,6,7,22,26,27,57,80,82
A/D_DOCK_IN	A/D_DOCK_IN	56,60,88,90

<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: shihhsien_yang

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 93 of 99

<Variant Name>

Title : POWER_FLOWCHART

ASUSTeK COMPUTER INC. NB

Engineer: Morris/Ding

Size	Project Name	Rev
Custom	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 94 of 99

[U36SD] R1.1

1. Change source of PQ9102 and PQ9104 from +5VSUS to +5VSYS p91
2. transform pin1,4,7,10 trace to +1.7v_lan p34
3. WLAN clk_req1 follow u36jc pull low p21
4. ALC269 pin9 trace to +3vsus for leakage current p36
5. EC PIN3 is NC p30
6. Add ESD protect part for HDMI p48
7. Add capacitance for EMI request on H_CPUPWRGD p25
8. Change C3404 trace from GND_LAN to GND p34
9. Follow U36JC CRT solution p46

ASUSTeK COMPUTER INC. NB	Title : System History Engineer:	
Size: C	Project Name: UX31A2	Rev
Date: Tuesday, March 27, 2012	Sheet 95 of 99	

[M61JA] R1.0 => R1.1

1. Follow E.E RC delay
   +5v R9107 100K change to 68K
   +3v R9106 200K change to 121K
   +1.5v R8306 49.9K change to 68K
   +5VS R9104 200K change to 68K
   +3VS R9103 200K change to 121K
   +1.8VS R8401 33.2K change to 121K
   +1.5VS R9102 470K change to 390K
   +1.05VS R8252 39K change to 200K
   +0.75VS R8312 0 change to 2.49K C8310 0.1U change to 2.2U

2.VR_VID0~2 pull high 1K VR_VID6 pull low 1K.

3.U8401 RT8015A change to RT8015B

4.Reserve GVR_VID0~VID6 pull high and low resistor R8627~R8633

5.Reserve R8517~R5720 pull high & pull low risistor for MCP_CORE_VID

6.page86 component option change to ARD (CFD no stuff)

7.R8004 option change to CFD & R8049 change to ARD(For IMON)

8.Change RN8801A RN8801B(layout request)

9.R8517 R8519 change to stuff

10.R8406 13K change to 12K

11.CE8005 no stuff , CE8007 stuff

12.C8403 C8406 size 0603 change to 0805

13.R8213 R8305 ohm change to 2.2 ohm

14.R8621~R8633 stuff 1K ohm

15.R8512 change form 200K to 33K ohm

16.VTT_PCH component option change to CFD

17.Delete U8502 & GPU_PWRON signal change to GPU_PWRON_1.8VSG_&_3.3VSG

18.L8601 1uH => 0.56uH , C8608 0.01uF/50 => 0.01uF/16V , R8621 43K => 36K , C8617 =>0.1uF/16V 1uF/10V ,
   C8607 68pF/50V => 33pF/50V , R8625 10K => 18.7K , R8613 3.6K => 4.02K

19.R8057 change form 10K to 2.05K

20.Add Q8007 & Q8008 form thermal issue

ASUSTeK COMPUTER INC. NB	Title : System History	
	Engineer:	
Size: Custom	Project Name: UX31A2	Rev
Date: Tuesday, March 27, 2012	Sheet 96 of 99	

ER
001 Page 13 & 14 : add +0.75VS de-coupling capacitors for channel B by samsung simulation recommand , and add +1.5V de-coupling capacitors around U1404 by samsung simulation recommand
002 Page 65 : remove U6511~14, U6516
003 Page 31 : change J3101 to 12G183000403 and add PWR_SW ↘ PWR_LED function on Keyboard
004 Page 46 : change J4601 to 12019-00020000
005 Page 48 : change J4801 to 12022-00013700
006 Page 70 : remove SW7001
007 Page 69 : change J6901 to 12013-00011600
008 Page 53 : change J5303 to 12003-00020700
009 Page 30 : swap EC GPE0 and GPH4 for EC request
010 Page 30 : +3VA_ON pull low
011 Page 30 : add R3002 for without Light_sensor system
012 Page 30 : unmount R3084, mount R3083 for S4/S5 EC power down
013 Page 21,68,69 : remove about FL1009 circuit
014 Page 06 : modify R0617,R0618 to 1K follow intel DG
015 Page 60 : change J6001 to 12014-00101000 for MP
016 Page 28 : change U2801 to 05006-00010300 (64M)
017 Page 56 : add R5640 for PWR_LED# current limit
018 Page 24,25 : change (H_SNB_INV#) AV10 to AY1 for following VC circuit.
019 Page 69 : add +5V_USB2 discharge for AI-charger function fail on iPhone 4S
020 Page 56 : Change R5604 size from 0201 to 0402.
021 Page 23 : Reserve 5pF cap. of RGB signals for EMI suggestion.
022 Page 45 : Reserved 8pF cap. to +3VS_LCD & +3VSUS for RF suggestion.
Page 45 : Reserved 5pF cap. to G & D sides of Q4501 for RF suggestion.
Page 45 : Reserved 5pF cap. to G & D sides of Q4501 for RF suggestion.
Page 45 : Reserved 0.1pF cap. to AC_BAT_SYS_INV_CON for RF suggestion.
Page 45 : Changed R4503 to L4514 for RF suggestion.
Page 45 : Colay USB_PP2 0 ohm & choke for RF suggestion.
Page 13 : Add cap. to +1.5V for RF suggestion.
Page 14 : Add cap. to +1.5V for RF suggestion.
Page 15 : Add cap. to +1.5V for RF suggestion.
Page 48 : Colay HDMI ohm & choke for RF suggestion.
Page 50 : Reserved cap. to SMB1_CLK_S for RF suggestion.
Page 51 : Reserved cap. to +3VS for RF suggestion.
Page 53 : Reserved cap. to +3VAUX_WLAN for RF suggestion.
Page 70 : Reserved cap. to pin 4 of Q7003 for RF suggestion.
Page 70 : Reserved cap. to pin 4 of Q7003 for RF suggestion.
Page 63 : Reserved cap. to +3V for RF suggestion.
Page 63 : Reserved cap. to net of for RF suggestion.
023 Page 20 : Reserved R2009 for RTC battery change type.
024 Page 26 : Deleting R2606 for DDR3L power change path.
Page 53 : Deleting R5302 for DDR3L power change path.
025 Page 28 : Add cap. to pin 5~8 of SPI ROM for RF suggestion.
026 Page 20 & 51 : Add SATA_TX1 net to SSD for SSD support RAID .
027 Page 56 : Change R5609 and reserve C5624 for DC jack change size.
028 Page 26 : Change resistor value of R2630 to 511K ohm and change size from 0201 to 0402 for reducing power consumption.
Page 70 : Change resistor value of R7004 ↘ R7005 to 200K ohm for reducing power consumption.
Page 56 : Change resistor value of R5602 to 200K ohm for reducing power consumption.
029 Page 25 : Change R2529 ↘ R2530 ↘ R2531 for following sedding schematic design.
030 Page 46 : Change C4602 ↘ C4604 ↘ C4606 cap. value to 10PF and L4601 ↘ L4602 ↘ L4603 for EMI suggestion & EA measure pass.
Page 24 : Change R2428 resistor value to 39 ohm for EA measure pass.
Page 69 : Delete RN6916 and add L6901 for EMI suggestion.
031 Page 24 & 45 & 63 : Change USB port2 & port3 to port 8 & port 9 for BIOS suggestion.
032 Page 69 : Add R6905 & C6901 for USB problem.
033 Page 27 : Change power plane of VCCDSW3_3 for supporting hybrid sleep mode.
034 Page 51 : Add JP5101 for measurement.
035 Page 63 : Add 0.1UF cap. to +3VS & +5V for RF suggestion.
036 Page 45 : Reserve 0.1UF cap. to BUF_PLT_RST# & TPanel_INT#_C for EMI suggestion.
Page 31 : Reserve 0.1UF cap. to TP_DAT & TP_CLK for EMI suggestion.
Page 45 : Add L4518 to +3VS_LCD for EMI suggestion.
037 Page 14 & 15 : Change C1416 & C1501 cap. value from 8PF to 0.1UF for RF suggestion.

PWR modify
Page 88 : Updating CHG IC to BQ24725A
Page 88 : Add shut down sche.
Page 90 : Add HW_throttle sche.
Page 90 : Add PR8107 for WLAN noise.
Page 83 : Delete PCE8301 for WLAN noise.
Page 83 : Change PL8300 to 2.2uH for WLAN noise.
Page 83 : Add PC8326 ↘ PC8327 for RF suggestion.
Page 83 : Add PR8321 to 330k
Page 83 : Change PR8314 to 9.53k
Page 60 & 90 : Change BOM
Page 81 & 90 : Change BOM & sche. for power design ip sche change.
Page 81 & 90 : Change BOM PCE8101 to 220uF, and PR9005 to 49.9k ohm

PR
001 Page 03 : Change U0303 to 06G004753010 for CR sche.
002 Page 44 : Change JDEBUG1 to 12G18340120R
003 Page 56 : Add a new lid sw for touchpanel using. (Panel PCB length change)
004 Page 30 : Reserved 0.1UF to light_sensor.
005 Page 31 : Change 6 pin to 8 pin for TP changing.
006 Page 21 : Change SMBus and INT for TP using.
007 Page 45 : Change Touch Panel pin define.
008 Page 56 : Change control method of charger led.
009 Page 31 : Add C3114 for RF suggestion.
010 Page 31 : Add and reserve the old 6 pins con and delete +5VS_TP.
011 Page 63 : Add 8PF cap. to +5VS for RF suggestion.
012 Page 53 : Add R5306 and Pull high to +3VSUS for intel smart card function using.
013 Page 44 : Change pin define for footprint vs datasheet aren't the same.
014 Page 45 : Add C4570 ↘ C4501 ↘ C4504 Cap. for RF suggestion.

PWR modify
Page 81 : Add PC8131, PC8132
Page 83 : Add PC8317 / P8316 / PR8305 / PC8305
Page 83 : Change PR8314=>12k
Page 88 : Update Adaptor voltage table
Page 84 : Change PL8400 BOM
Page 87 : Change PL8700 BOM
Page 83 : PR8304 & PR8305 pull high to +3VA_EC
Page 88 : PR8810 & PR8817 change 10ohm/0603 to 0ohm/0603.
Page 88 : PR8838 change 95.3kohm/0402 to 100kohm/0402.

ASUSTeK COMPUTER INC. NB
Title : System History
Engineer:
Size
Project Name
UX31A2
Rev
Custom
Date: Tuesday, March 27, 2012
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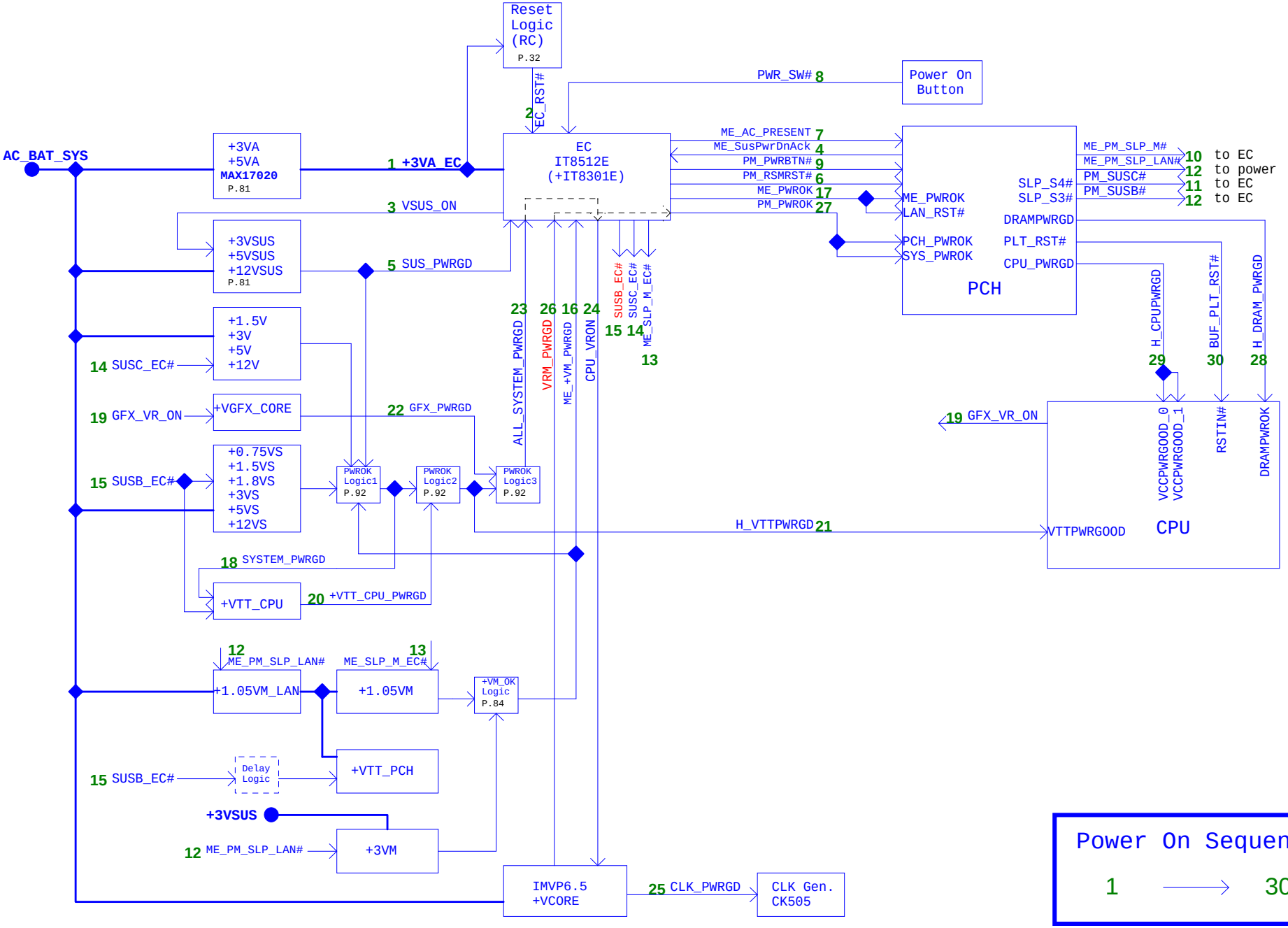
AC-IN Mode

M52J Power On Sequence Diagram Rev. 0.31



Power On Sequence

1 → 30

ASUSTeK COMPUTER INC

Title : POWER SEQUENCE

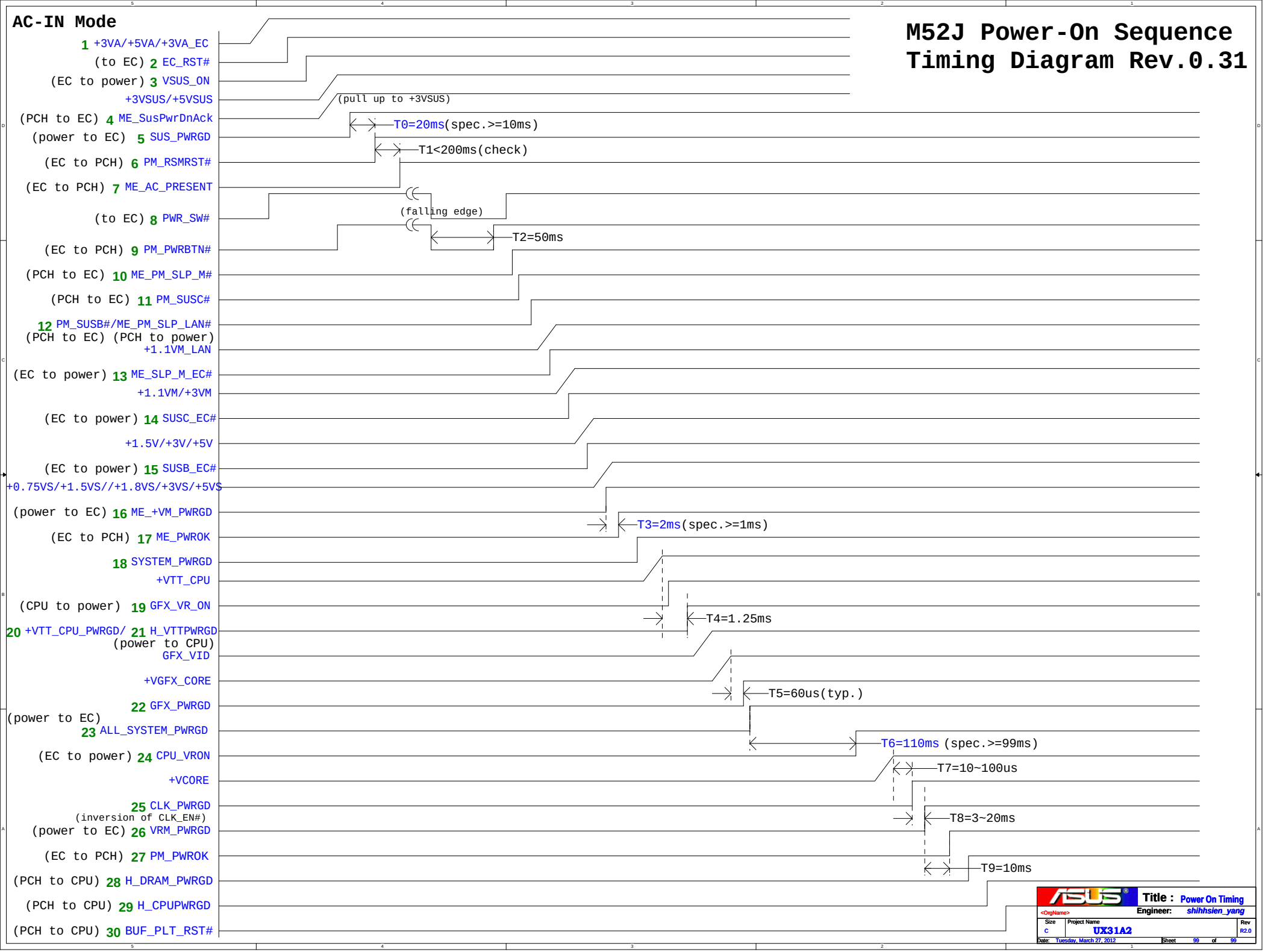
Engineer: shihhsien_yang

Size	Project Name	Rev
C	UX31A2	R2.0

Date: Tuesday, March 27, 2012 Sheet 98 of 99

M52J Power-On Sequence Timing Diagram Rev.0.31

AC-IN Mode



ASUS	Title : Power On Timing	
<OrgName>	Engineer: shihhsien_yang	
Size: C	Project Name: UX31A2	Rev: R2.0
Date: Tuesday, March 27, 2012	Sheet 99 of 99	

UX31A R2.0 SKU table

BOM	CPU	Memory	TPM	SSD	PANEL
Option	/CPU	/MEM	/TPM		
60-NIOMB160*-B0*	I7-3517U	Elpida 4G DDR3LRS-1600	/TPM	A-DATA/XM11-256GB-V2	CMO/N133HSE-EA1
60-NIOMB1C0*-A0*	I7-3517U	Elpida 4G DDR3LRS-1600	N/A		
60-NIOMB1A0*-B0*	I5-3317U	Elpida 4G DDR3LRS-1600	/TPM		
60-NIOMB180*-B0*	I5-3317U	Elpida 4G DDR3LRS-1600	N/A	A-DATA/XM11-128GB-V2	CMO/N133HSE-EA1
60-NIOMB1B0*-A0*	I7-3667U	Micron 4G DDR3LRS-1600	/TPM		
60-NIOMB1D0*-A0*	I7-3517U	Elpida 4G DDR3-1600	N/A	SANDISK/SDSA5JK-128G	CPT/CLAA133UA03 CW

1. CPU:
   INT I7-3667U 2G/4M : 01001-00173400 (MP)
   INT I7-3517U 1.9G/4M : 01001-00172300 (MP)
   INT I5-3317U 1.7G/3M : 01001-00172400 (MP)
2. PCH:
   INT PANTHERPOINT HM76 : 02001-00051100 (MP)
3. MEM: Differential memory DIMM & Vendor have the differential DIMM_SEL[2:0] defined on board memory.
   Elpida 4G DDR3LRS 1600 256M*16 : 03006-00051300
   Elpida 4G DDR3 1600 256M*16 : 03006-00050800
   Micron 4G DDR3LRS 1600 256M*16 : 03006-00051100

DDR3L_1600	Micro			ELPIDA
DIMM_SEL0	L			H
DIMM_SEL1	L			H
DIMM_SEL2	H			H

DDR3_1600		Hynix	ELPIDA	
DIMM_SEL0		H	L	
DIMM_SEL1		L	H	
DIMM_SEL2		H	H	

ASUSTeK COMPUTER INC.
Title : SKU Table R1.2
Engineer: shihhsien_yang
Size: Custom | Project Name: UX31A2 | Rev: 02.0
Date: Wednesday, April 10, 2013 | Sheet of