Main Board

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003. Schematic Information
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005. CPU_Silverthorne (2)
006. CPU_******
007. DIM_SO-DIMM 0
008. DIM_******
009. DIM_DDR2 Terminatin
010. SCH_Poulsbo_HOST
011. SCH_Poulsbo_DDR2
012. SCH_Poulsbo_LVDS/SDVO
013. SCH_Poulsbo_PM/USB/AZ
014. SCH_Poulsbo_POWER
015. SCH_Poulsbo_GND
016. SCH_******
017. SCH_******
018. SCH_******
019. SCH_******
020. SCH_******
021. SCH_******
022. SCH_******
023. SCH_******
024. SCH_******
025. SCH_******
026. SCH_******
027. SCH_******
028. SCH_******
029. CLK_ICS9LPRS427
030. KBC_IT8512
031. KBC_KB CON
032. KBC_RESET MAP
033. LAN_RTL8111C
034. LAN_RJ45
035. LAN_******
036. AUD_IC CON
037. AUD_******
038. AUD_******
039. AUD_******
040. CB_******
041. CB_******
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043. CB_******
044. BUG_LPC DEBUG
045. CRT_LVDS
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052. USB_USB Port *2
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054. BAR_******
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057. DSG_DISCHARGE
058. SUB_******
059. SEQ_******
060. DC_DC & BAT IN
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062. TPM_******
063. FP_******
064. TUN_******
065. ME_NUT & SCREW HOLE
066. ESA_SATA JMB360
067. SDVO_CH7317
068. OTH_POWER ON CIRCUIT
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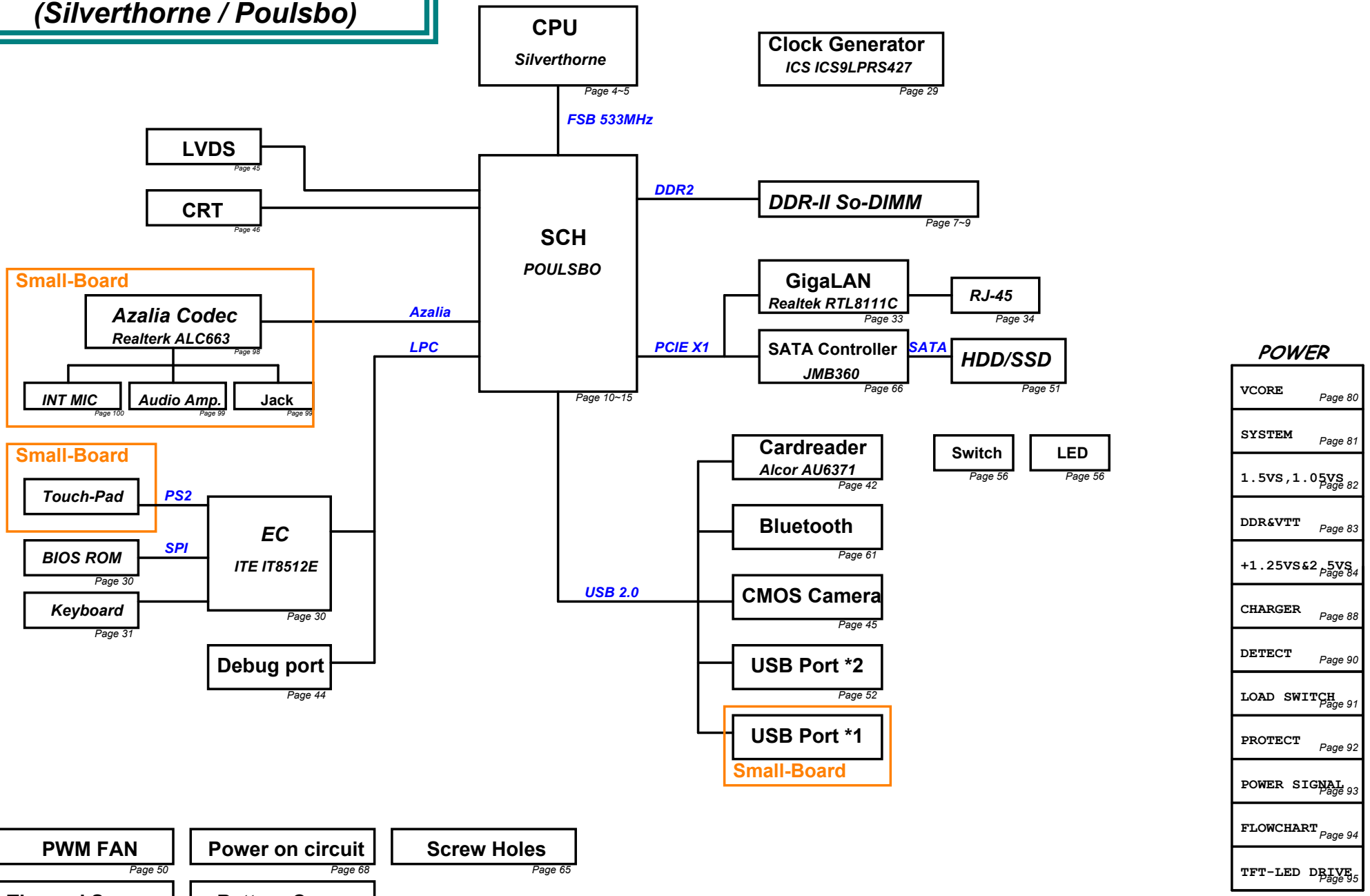
Power

080. PWR_VCORE
081. PWR_SYSTEM
082. POWER_I/O_+1.05VO
083. PWR_I/O_DDR & VTT
084. PWR_I/O_POWER_I/O_ +1.5V_+2.5VS
085. POWER_+1.05VO & +1.5VO
086. POWER_+MCP_VDD_CORE(Empty)
087. PWR_SHUTDOWN# (Empty))
088. PWR_CHARGER
089. PWR_PIC(Empty)
090. PWR_DETECT
091. PWR_LOAD SWITCH
092. PWR_PROTECT
093. PWR_SIGNAL
094. POWER_FLOWCHART
095. PWR_LED_VCC_BOOST
096. HISTORY
097. POWER ON SEQUENCE

Revision History

UX20 Block Diagram (Silverthorne / Poulsbo)



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ASUS	Title : Block Diagram	
ASUSTeK COMPUTER INC. NB1	Engineer:	
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 2 of 97	

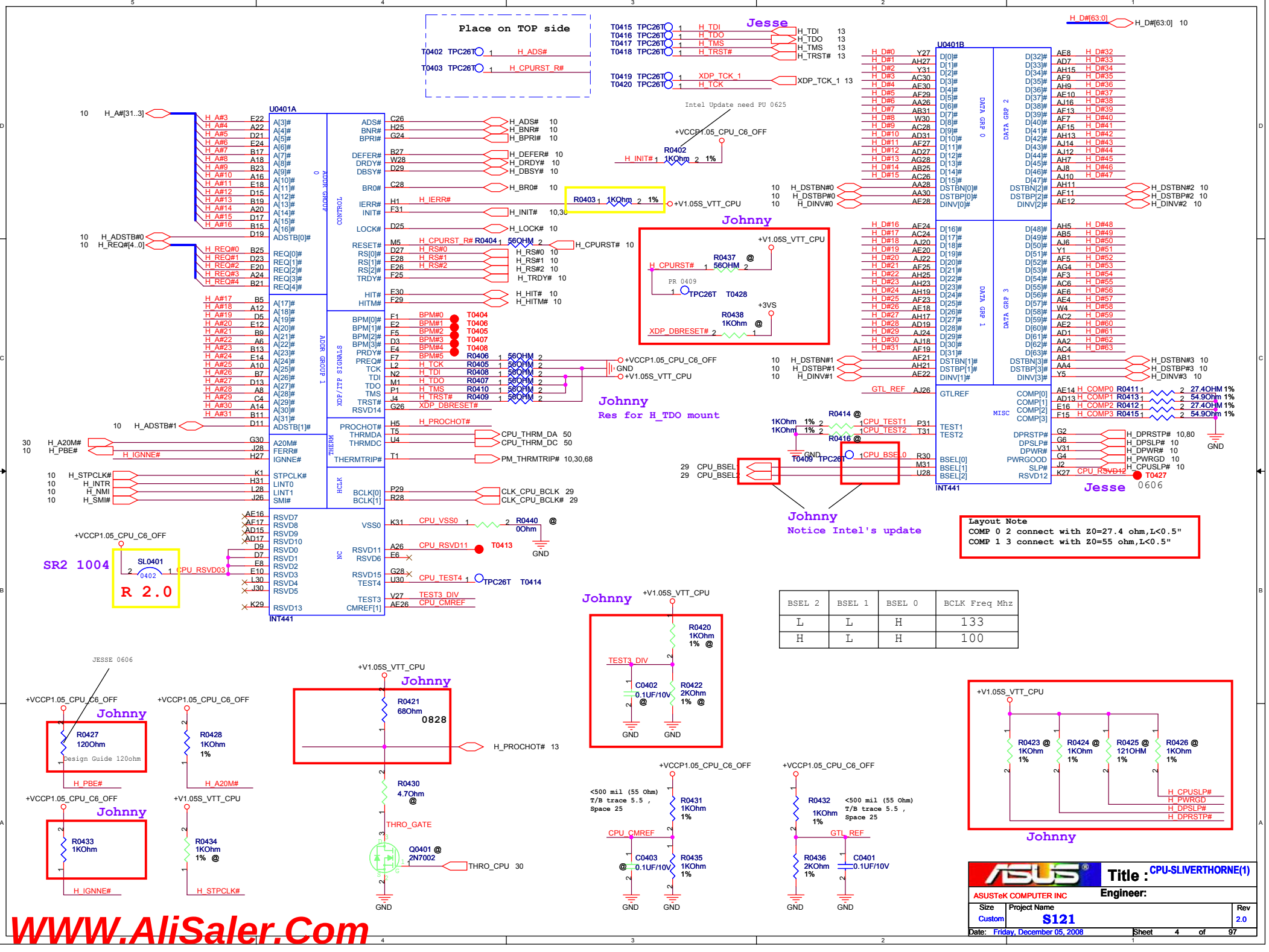
Poulsbo GPIO SETTING

Name	Signal Name	Type
GPIOSUS0	RTLAN_DSM#	GPI
GPIOSUS1	RTLAN_DSM_EN	GPO
GPIOSUS2	PM_PWRBTN#	GPI
GPIOSUS3	****	TP
GPIO0	WLAN_LED_ON	GPO
GPIO1	PCB_ID0	GPI
GPIO2	PCB_ID1	GPI
GPIO3	CLK_OC	GPO
GPIO4	VCORE_CNT	GPO
GPIO5	OC_CTL#	GPO
GPIO6	DDR_MEM_CONFIG	GPI
GPIO7	SLPIOVR#	GPO
GPIO8	H_PROCHOT#	GPO
GPIO9	****	TP

EC IT8512E GPIO SETTING

Name	Signal Name	Type
A0	PWR_LED#	GPO
A1	CHG_LED#	GPO
A2	****	NC
A3	MARATHON_LED#	GPO
A4	LCD_BL_PWM	GPO
A5	FAN0_PWM	GPO
A6	EC_RSTWRN	GPO
A7	PM_RSTRDY#	GPI
B0	RST#	GPO
B1	SCH_RST#_R	GPO
B2	PM_SLPMODE	GPI
B3	SMB0_CLK	GPIO
B4	SMB0_DAT	GPIO
B5	A20GATE	GPO
B6	RC_IN#	GPO
B7	PM_RSMRST#	GPO
C0	VOL_SEL	GPO
C1	SMB1_CLK	GPIO
C2	SMB1_DAT	GPIO
C3	PM_PWRBTN#	GPO
C4	AC_IN_OC#	GPI
C5	OP_SD#	GPO
C6	BAT1_IN_OC#	GPI
C7	RFON_SW#	GPI
D0	****	NC
D1	PM_SUSC#	GPI
D2	BUF_RST#	GPI
D3	EXT_SCI#	GPO
D4	EXT_SMI#	GPO
D5	LCD_BACKOFF#	GPO
D6	FAN0_TACH	GPI
D7	SD_CD_EC#	GPO
E0	VSUS_ON	GPO
E1	SUSC_EC#	GPO
E2	SUSB_EC#	GPO
E3	CPU_VRON	GPO
E4	PWR_SW#	GPI
E5	DDR2_VOL_0	GPO
E6	LID_SW#	GPI
E7	MARATHON#	GPO
F0	CRT_2.5V_PWR#	GPO
F1	CRT_RST	GPO
F2	CRT_IN#	GPI
F3	SATA_RST#	GPO
F4	TP_CLK	GPIO
F5	TP_DAT	GPIO
F6	THRO_CPU	GPO
F7	BT_ON#	GPO

Name	Signal Name	Type
G0	PM_THERM#	GPO
G1	PM_SUSB#	GPI
G2	****	NC
G6	****	NC
H0	PM_CLKRUN#	GPIO
H1	WLAN_ON#	GPO
H2	****	NC
H3	BAT_LEARN	GPO
H4	DDR2_VOL_1	GPO
H5	NUM_LED#	GPO
H6	CAP_LED#	GPO
I0	****	NC
I1	SUS_PWRGD	GPI
I2	ALL_SYSTEM_PWRGD	GPI
I3	VRM_PWRGD	GPI
I4	****	NC
I5	****	NC
I6	****	NC
I7	****	NC
J0	EC_CLK_EN	GPO
J1	PM_PWROK	GPO
J2	VSET_EC	GPO
J3	ISET_EC	GPO
J4	EXTTSO#	GPO
J5	FB	GPO



BSEL 2	BSEL 1	BSEL 0	BCLK Freq Mhz
L	L	H	133
H	L	H	100

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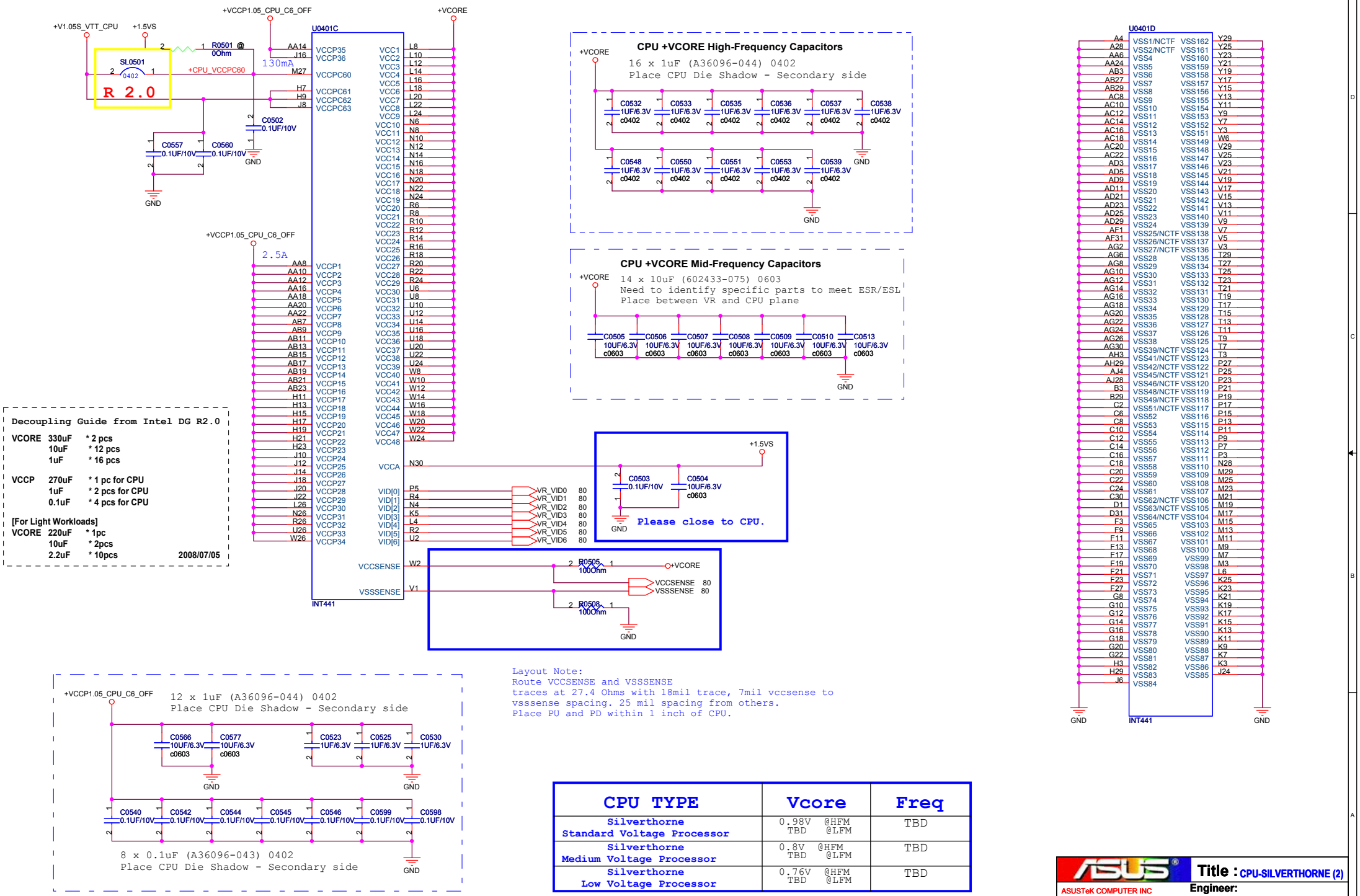

Layout Note:
Route VCCSENSE and VSSSENSE
traces at 27.4 Ohms with 18mil trace, 7mil vccsense to
vsssense spacing. 25 mil spacing from others.
Place PU and PD within 1 inch of CPU.

CPU TYPE	Vcore	Freq
Silverthorne Standard Voltage Processor	0.98V @HFM TBD @LFM	TBD
Silverthorne Medium Voltage Processor	0.8V @HFM TBD @LFM	TBD
Silverthorne Low Voltage Processor	0.76V @HFM TBD @LFM	TBD

ASUSTeK COMPUTER INC

Title : CPU-SILVERTHORNE (2)

Engineer:

Size	Project Name	Rev
A3	S121	2.0

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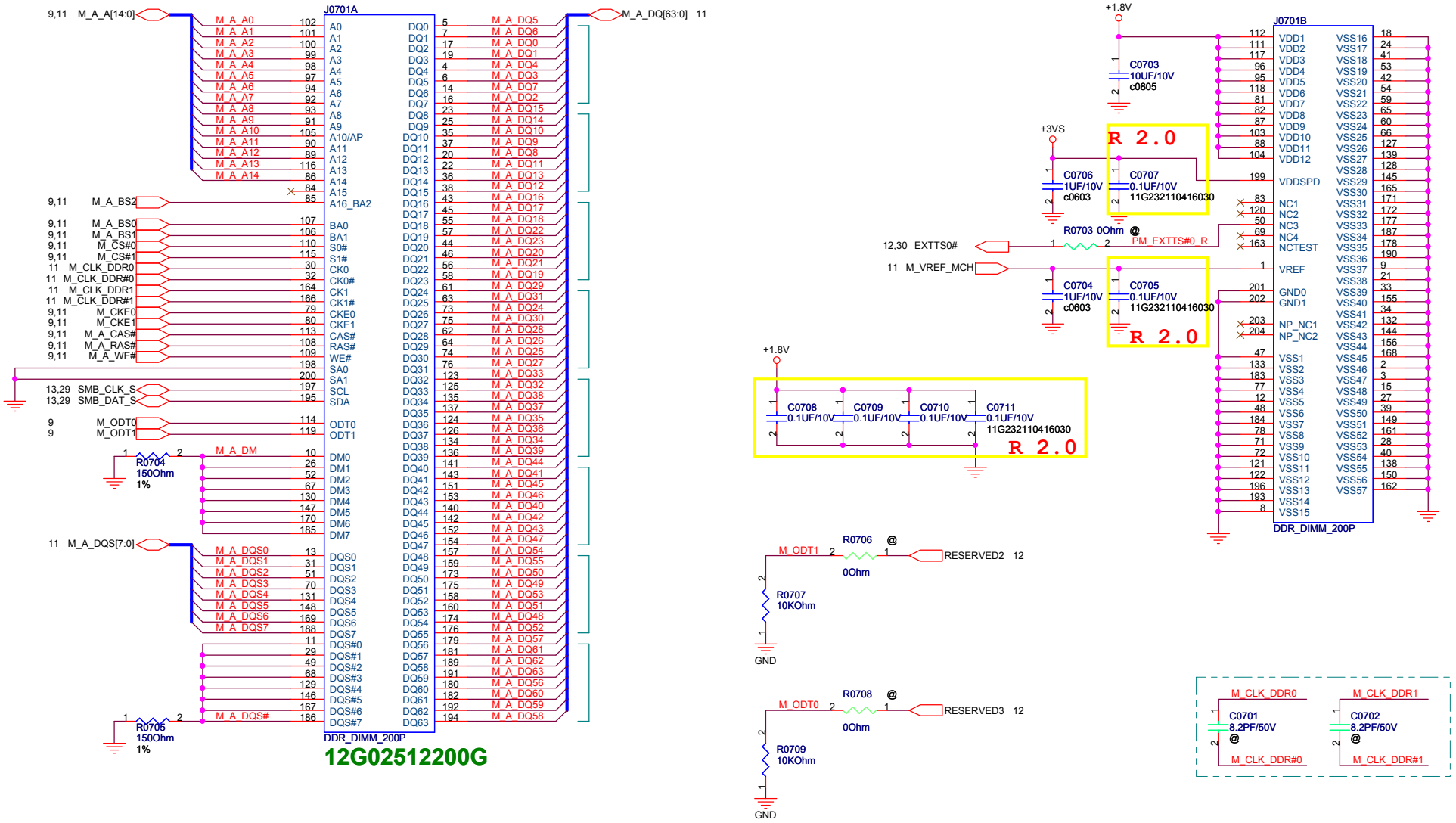

ASUS	Title : DIM_SO-DIMM 0	
ASUSTeK COMPUTER INC. NB1	Engineer:	
Size B	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 7 of 97	

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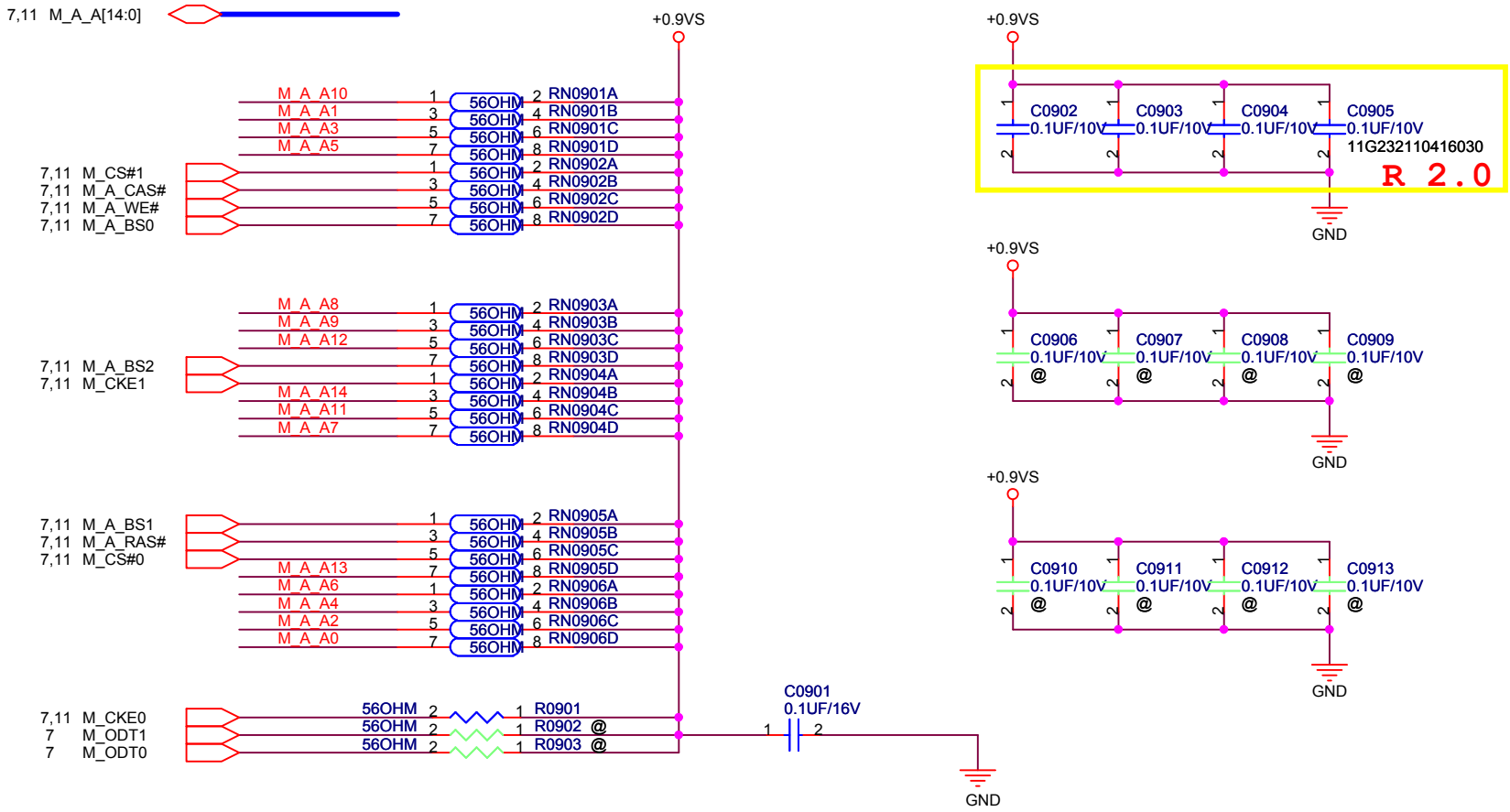
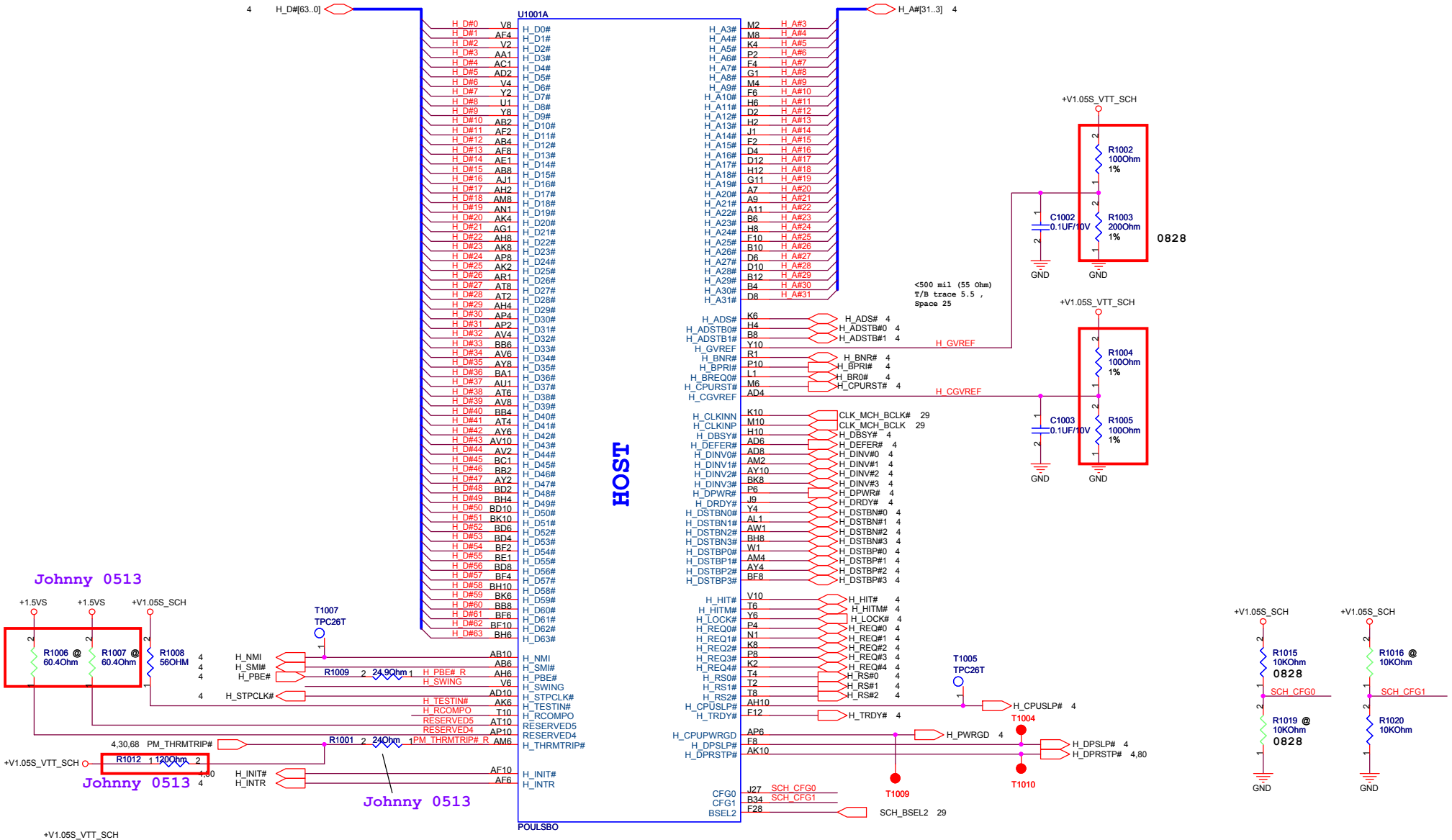
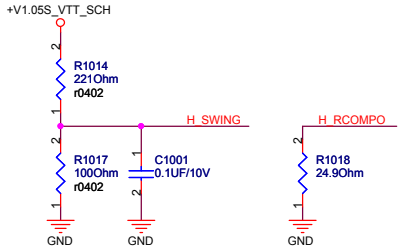


ASUSTeK COMPUTER INC. NB1	Title : DIM_DDR2 Termination	Engineer:
Size A4	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 9 of 97	





FSB	SCH_CFG1	SCH_CFG0	Gfx_Freq
400	0	0	200
533	0	1	200

Note: Clock Frequencies are in Mhz
Default Frequency determined by FSB speed

ASUSTeK COMPUTER INC	Title : Poulsbo_HOST (1)	Engineer:
Size A3	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 10 of 97	

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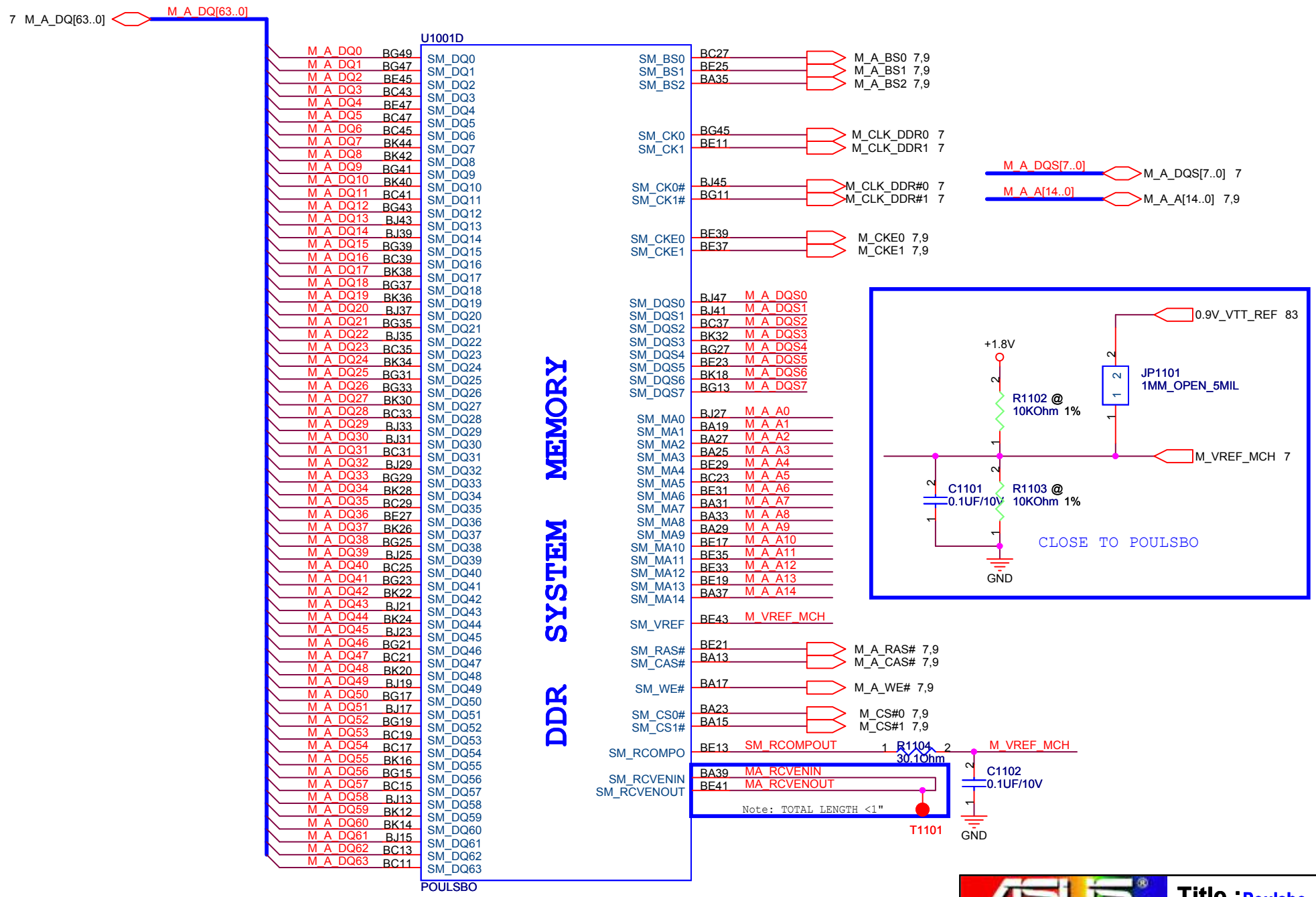
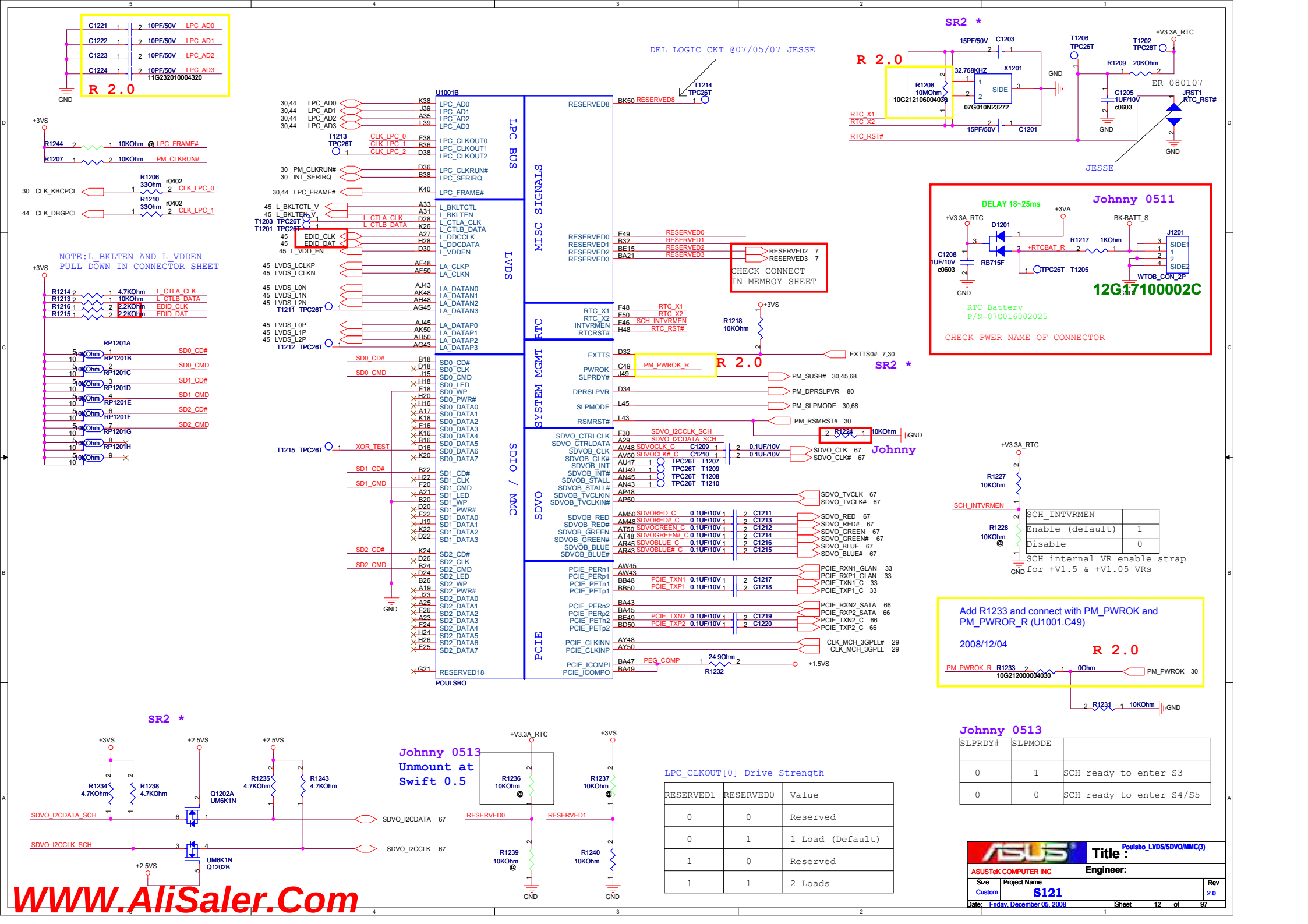


ASUSTeK COMPUTER INC	Title : Poulsbo_DDR2 (2)	Engineer:
Size A4	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 11 of 97	


C1221 10PF/50V LPC_AD0
C1222 10PF/50V LPC_AD1
C1223 10PF/50V LPC_AD2
C1224 10PF/50V LPC_AD3
11G232010004320
R 2.0
GND
+3VS
R1244 10KOhm @ LPC_FRAME#
R1207 10KOhm PM_CLKRUN#
R1206 33Ohm r0402 CLK_LPC_0
R1210 33Ohm r0402 CLK_LPC_1
30 CLK_KBCPCI
44 CLK_DBGPCI
NOTE:L_BKLTEN AND L_VDDEN
PULL DOWN IN CONNECTOR SHEET
R1214 4.7KOhm L_CTLA_CLK
R1213 10KOhm L_CTLB_DATA
R1216 2.2KOhm EDID_CLK
R1215 2.2KOhm EDID_DAT
RP1201A
RP1201B SD0_CD#
RP1201C SD0_CMD
RP1201D SD1_CD#
RP1201E SD1_CMD
RP1201F SD2_CD#
RP1201G SD2_CMD
RP1201H
10KOhm
U1001B
LPC BUS
LVDS
SDIO / MMC
MISC SIGNALS
RTC
SYSTEM MGMT
SDVO
PCIE
POULSBO
30,44 LPC_AD0 K38 LPC_AD0
30,44 LPC_AD1 J39 LPC_AD1
30,44 LPC_AD2 A35 LPC_AD2
30,44 LPC_AD3 L39 LPC_AD3
T1213 TPC26T
CLK_LPC_0 F38 LPC_CLKOUT0
CLK_LPC_1 B36 LPC_CLKOUT1
CLK_LPC_2 D38 LPC_CLKOUT2
30 PM_CLKRUN# D36 LPC_CLKRUN#
30 INT_SERIRQ B38 LPC_SERIRQ
30,44 LPC_FRAME# K40 LPC_FRAME#
45 L_BKLTCTL_V A33 L_BKLTCTL
45 L_BKLTEN_V A31 L_BKLTEN
T1203 TPC26T L_CTLA_CLK D28 L_CTLA_CLK
T1201 TPC26T L_CTLB_DATA K26 L_CTLB_DATA
45 EDID_CLK A27 L_DDCCLK
45 EDID_DAT H28 L_DDCDATA
45 L_VDD_EN D30 L_VDDEN
45 LVDS_LCLKP AF48 LA_CLKP
45 LVDS_LCLKN AF50 LA_CLKN
45 LVDS_L0N AJ43 LA_DATAN0
45 LVDS_L1N AK48 LA_DATAN1
45 LVDS_L2N AH48 LA_DATAN2
T1211 TPC26T AG45 LA_DATAN3
45 LVDS_L0P AJ45 LA_DATAP0
45 LVDS_L1P AK50 LA_DATAP1
45 LVDS_L2P AH50 LA_DATAP2
T1212 TPC26T AG43 LA_DATAP3
SD0_CD# B18 SD0_CD#
SD0_CMD D18 SD0_CLK
J15 SD0_CMD
H18 SD0_LED
F18 SD0_WP
H20 SD0_PWR#
H16 SD0_DATA0
A17 SD0_DATA1
K18 SD0_DATA2
F16 SD0_DATA3
K16 SD0_DATA4
B16 SD0_DATA5
T1215 TPC26T XOR_TEST D16 SD0_DATA6
K20 SD0_DATA7
SD1_CD# B22 SD1_CD#
H22 SD1_CLK
SD1_CMD F20 SD1_CMD
A21 SD1_LED
B20 SD1_WP
D20 SD1_PWR#
F22 SD1_DATA0
J19 SD1_DATA1
K22 SD1_DATA2
D22 SD1_DATA3
SD2_CD# K24 SD2_CD#
D26 SD2_CLK
SD2_CMD B24 SD2_CMD
D24 SD2_LED
B26 SD2_WP
A19 SD2_PWR#
J23 SD2_DATA0
A25 SD2_DATA1
F26 SD2_DATA2
A23 SD2_DATA3
F24 SD2_DATA4
H24 SD2_DATA5
H26 SD2_DATA6
E25 SD2_DATA7
G21 RESERVED18
RESERVED8 BK50 RESERVED8
T1214 TPC26T
DEL LOGIC CKT @07/05/07 JESSE
RESERVED0 F49 RESERVED0
RESERVED1 B32 RESERVED1
RESERVED2 BE15 RESERVED2
RESERVED3 BA21 RESERVED3
RESERVED2 7
RESERVED3 7
CHECK CONNECT
IN MEMROY SHEET
RTC_X1 F48 RTC_X1
RTC_X2 F50 RTC_X2
INTVRMEN F46 SCH_INTVRMEN
RTCRST# H48 RTC_RST#
R1218 10KOhm
EXTTS D32 EXTTS0# 7,30
PWROK C49 PM_PWROK_R
SLPRDY# J49 PM_SUSB# 30,45,68
DPRSLPVR D34 PM_DPRSLPVR 80
SLPMODE L45 PM_SLPMODE 30,68
RSMRST# L43 PM_RSMRST# 30
R 2.0
SR2 *
R1224 10KOhm
Johnny
SDVO_CTRLCLK F30 SDVO_I2CCLK_SCH
SDVO_CTRLDATA A29 SDVO_I2CDATA_SCH
SDVOB_CLK AV48 SDVOCLK_C C1209 0.1UF/10V SDVO_CLK 67
SDVOB_CLK# AV50 SDVOCLK# C C1210 0.1UF/10V SDVO_CLK# 67
SDVOB_INT AU47 TPC26T T1207
SDVOB_INT# AU49 TPC26T T1209
SDVOB_STALL AN45 TPC26T T1208
SDVOB_STALL# AN43 TPC26T T1210
SDVOB_TVCLKIN AP48 SDVO_TVCLK 67
SDVOB_TVCLKIN# AP50 SDVO_TVCLK# 67
SDVOB_RED AM50 SDVORED_C 0.1UF/10V C1211 SDVO_RED 67
SDVOB_RED# AM48 SDVORED# C 0.1UF/10V C1213 SDVO_RED# 67
SDVOB_GREEN AT50 SDVOGREEN_C 0.1UF/10V C1212 SDVO_GREEN 67
SDVOB_GREEN# AT48 SDVOGREEN# C 0.1UF/10V C1214 SDVO_GREEN# 67
SDVOB_BLUE AR45 SDVOBLUE_C 0.1UF/10V C1216 SDVO_BLUE 67
SDVOB_BLUE# AR43 SDVOBLUE# C 0.1UF/10V C1215 SDVO_BLUE# 67
PCIE_PERn1 AW45 PCIE_RXN1_GLAN 33
PCIE_PERp1 AW43 PCIE_RXP1_GLAN 33
PCIE_PETn1 BB48 PCIE_TXN1 0.1UF/10V C1217 PCIE_TXN1_C 33
PCIE_PETp1 BB50 PCIE_TXP1 0.1UF/10V C1218 PCIE_TXP1_C 33
PCIE_PERn2 BA43 PCIE_RXN2_SATA 66
PCIE_PERp2 BA45 PCIE_RXP2_SATA 66
PCIE_PETn2 BE49 PCIE_TXN2 0.1UF/10V C1219 PCIE_TXN2_C 66
PCIE_PETp2 BD50 PCIE_TXP2 0.1UF/10V C1220 PCIE_TXP2_C 66
PCIE_CLKINN AY48 CLK_MCH_3GPLL# 29
PCIE_CLKINP AY50 CLK_MCH_3GPLL 29
PCIE_ICOMPI BA47 PEG_COMP 24.9Ohm R1232 +1.5VS
PCIE_ICOMPO BA49
SR2 *
R 2.0
15PF/50V C1203
32.768KHZ X1201
R1208 10MOhm 10G212106004039
07G010N23272
15PF/50V C1201
RTC_X1
RTC_X2
RTC_RST#
T1206 TPC26T
T1202 TPC26T
+V3.3A_RTC
R1209 20KOhm
ER 080107
C1205 1UF/10V c0603
JRST1 RTC_RST#
JESSE
Johnny 0511
DELAY 18~25ms
+V3.3A_RTC
+3VA
D1201 RB715F
C1208 1UF/10V c0603
R1217 1KOhm
+RTCBAT_R
BK-BATT_S
J1201 WTOB_CON_2P
T1205 TPC26T
12G17100002C
RTC Battery
P/N=07G016002025
CHECK PWER NAME OF CONNECTOR
+V3.3A_RTC
R1227 10KOhm
SCH_INTVRMEN
R1228 10KOhm @
SCH_INTVRMEN
Enable (default) 1
Disable 0
SCH internal VR enable strap
for +V1.5 & +V1.05 VRs
Add R1233 and connect with PM_PWROK and
PM_PWROR_R (U1001.C49)
2008/12/04
R 2.0
PM_PWROK_R R1233 0Ohm 10G212000004030 PM_PWROK 30
R1231 10KOhm
Johnny 0513
SLPRDY# SLPMODE
0 1 SCH ready to enter S3
0 0 SCH ready to enter S4/S5
SR2 *
+3VS
+2.5VS
R1234 4.7KOhm
R1238 4.7KOhm
Q1202A UM6K1N
R1235 4.7KOhm
R1243 4.7KOhm
SDVO_I2CDATA_SCH
SDVO_I2CCLK_SCH
UM6K1N Q1202B
SDVO_I2CDATA 67
SDVO_I2CCLK 67
Johnny 0513
Unmount at
Swift 0.5
+V3.3A_RTC
+3VS
R1236 10KOhm @
R1237 10KOhm @
RESERVED0
RESERVED1
R1239 10KOhm @
R1240 10KOhm
GND
LPC_CLKOUT[0] Drive Strength
RESERVED1 RESERVED0 Value
0 0 Reserved
0 1 1 Load (Default)
1 0 Reserved
1 1 2 Loads
ASUSTeK COMPUTER INC
Title : Poulsbo_LVDS/SDVO/MMC(3)
Engineer:
Size Custom
Project Name S121
Rev 2.0
Date: Friday, December 05, 2008
Sheet 12 of 97
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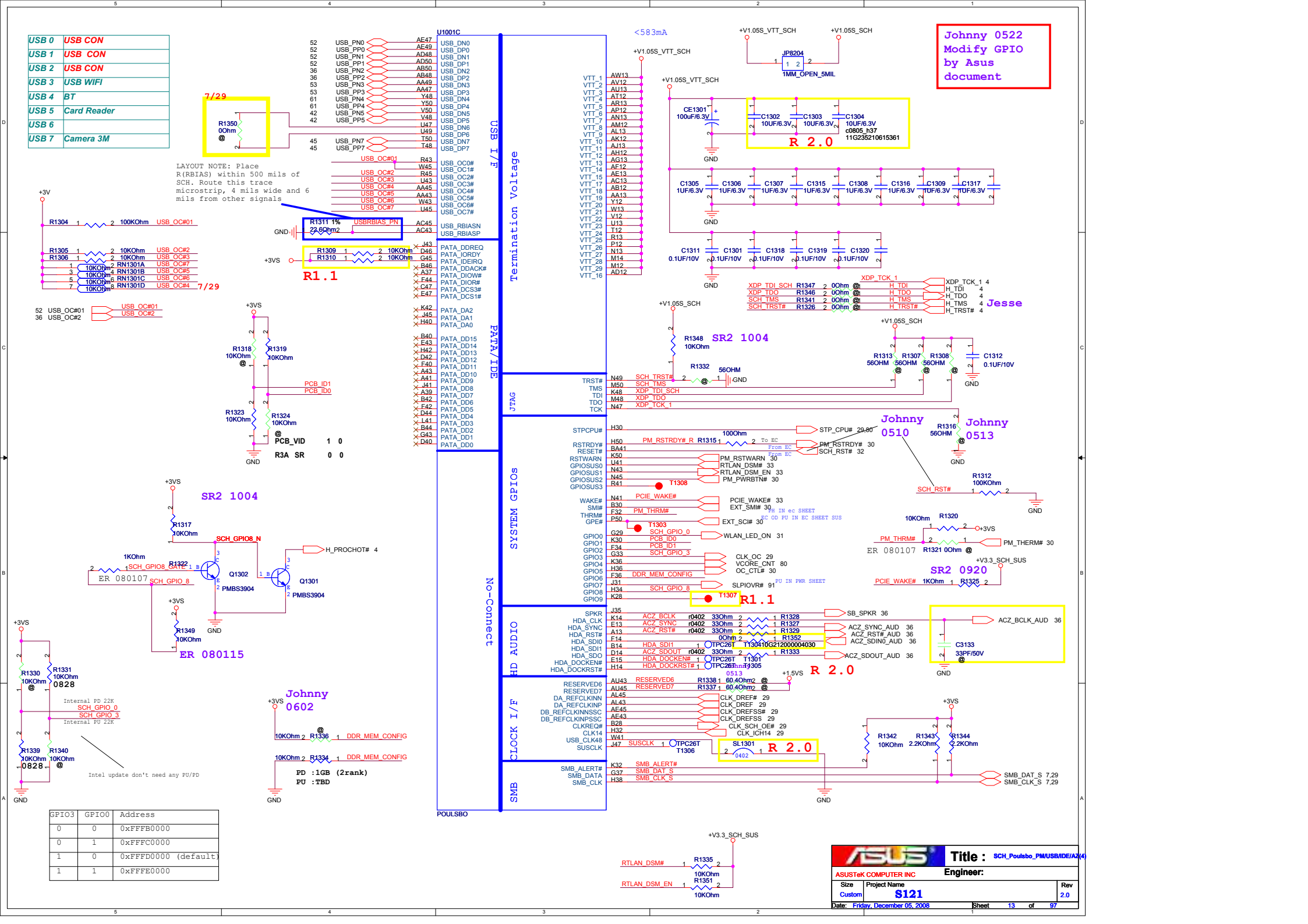
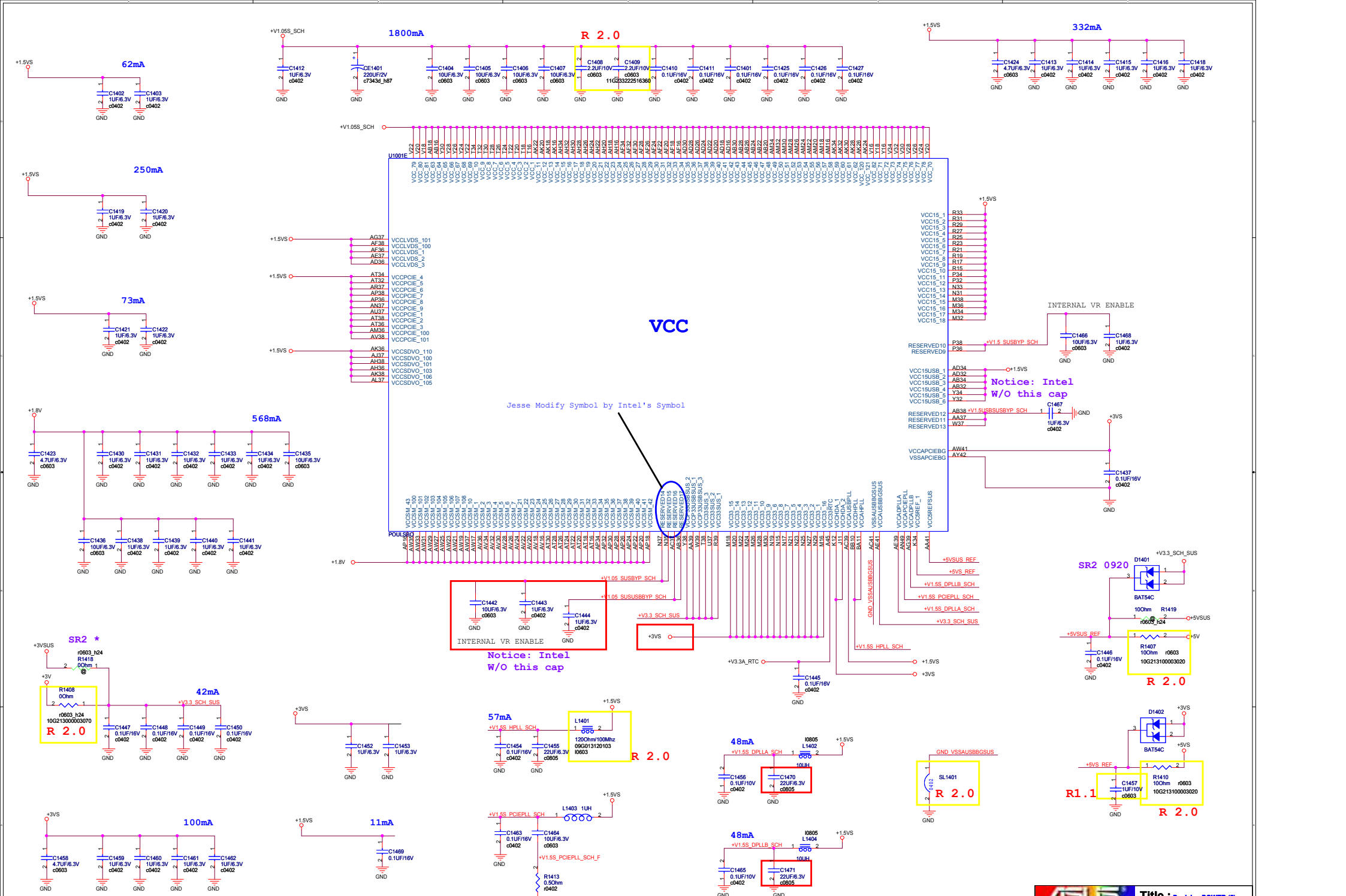
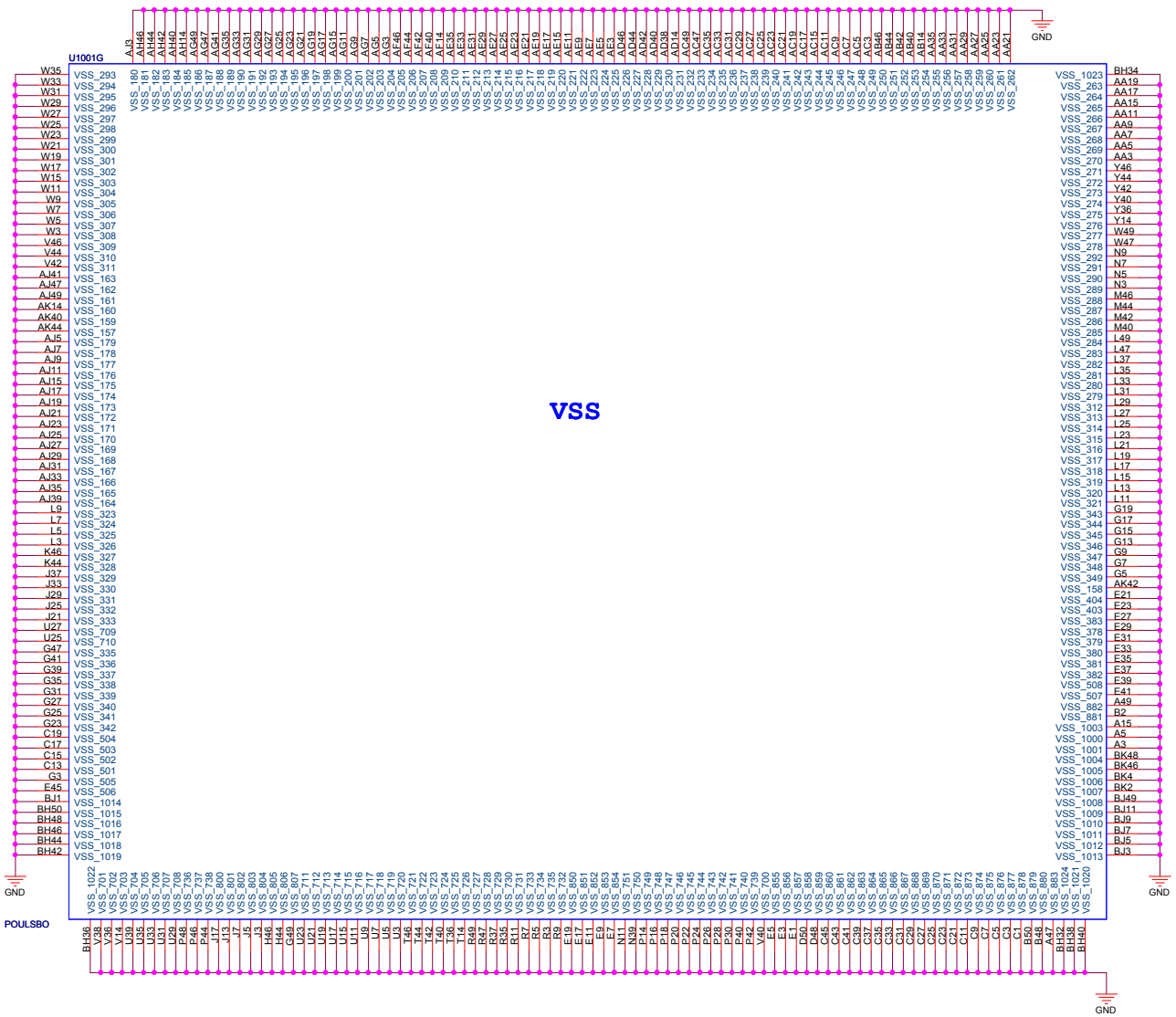
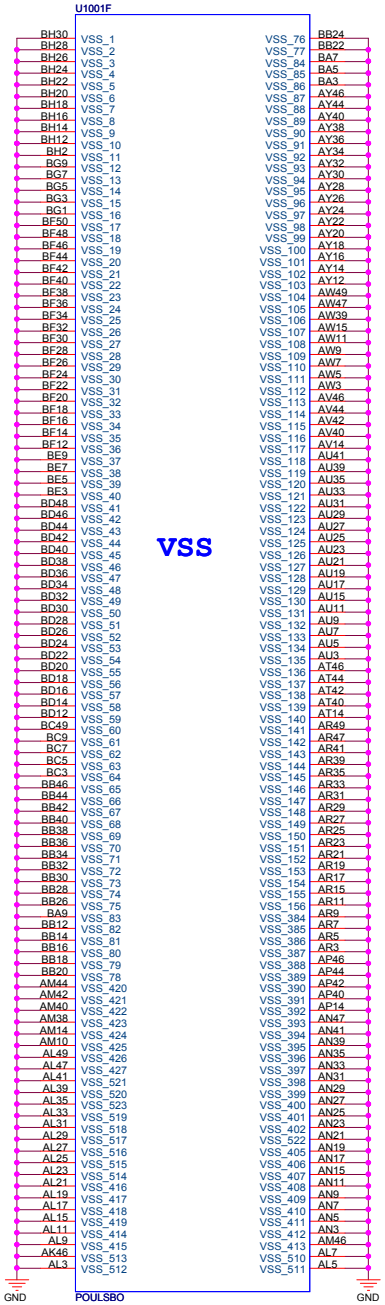


GPIO3	GPIO0	Address
0	0	0xFFFB0000
0	1	0xFFFC0000
1	0	0xFFFD0000 (default)
1	1	0xFFFE0000


VCC
U1001E
Jesse Modify Symbol by Intel's Symbol
1800mA
R 2.0
332mA
62mA
250mA
73mA
568mA
42mA
100mA
11mA
57mA
48mA
48mA
INTERNAL VR ENABLE
Notice: Intel
W/O this cap
INTERNAL VR ENABLE
Notice: Intel
W/O this cap
SR2 0920
SR2 *
R 2.0
R 2.0
R 2.0
R 2.0
R 2.0
R1.1
WWW.AliSaler.Com
Title : Poulsbo_POWER (5)
ASUSTeK COMPUTER INC
Engineer:
Size C
Project Name S121
Rev 2.0
Date: Friday, December 05, 2008
Sheet 14 of 97





ASUSTeK COMPUTER INC

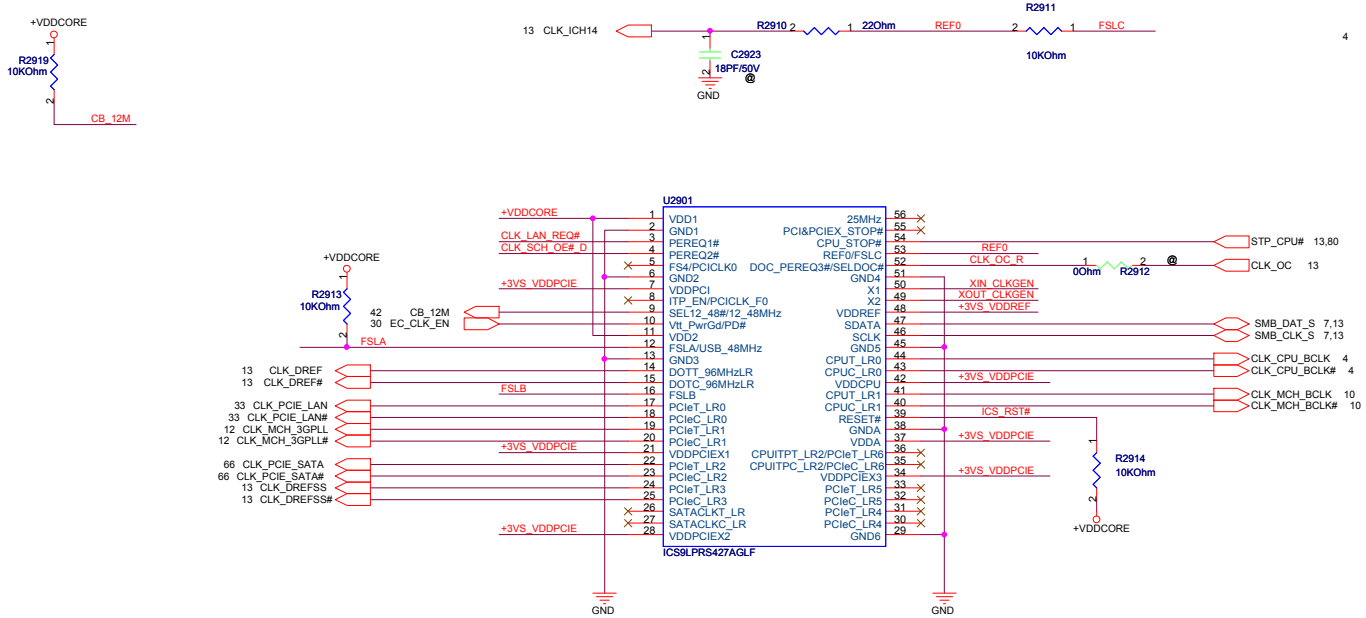
Title : POULSBO_GND (6)

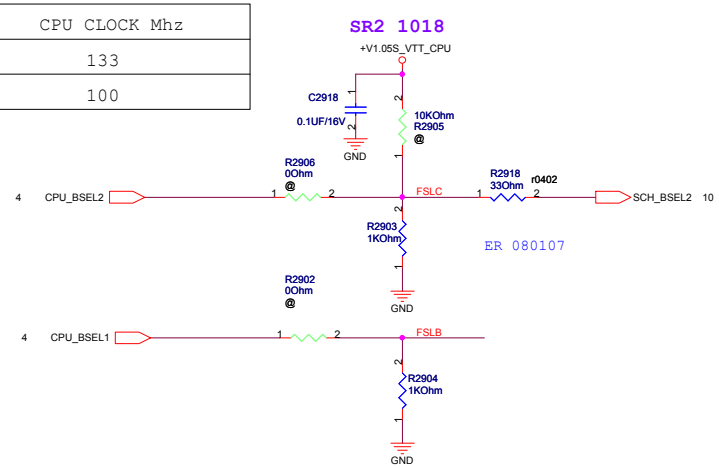
Engineer:

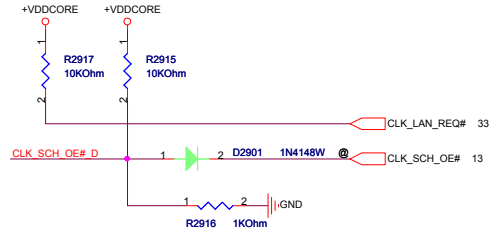
Size	Project Name	Rev
Custom	S121	2.0

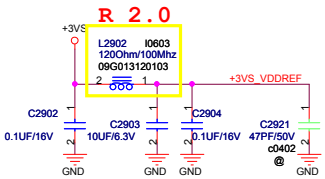
Date: Friday, December 05, 2008 Sheet 15 of 97

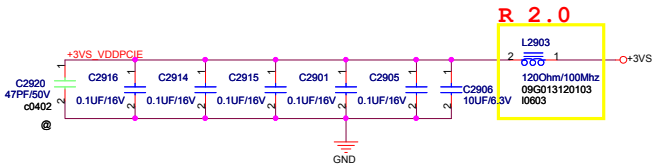
FSC	FSB	CPU CLOCK Mhz
0	0	133
1	0	100

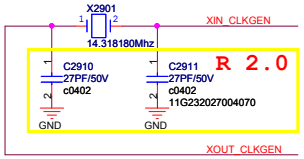






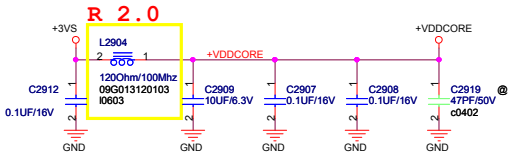






CLK REQUEST

REQ1:	SRC0	GLAN
REQ2:	SRC1	SCH
REQ3:	X	OVER CLOCK



ASUSTeK COMPUTER INC	Title : CLOCK GEN	Engineer:
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 29 of 97	

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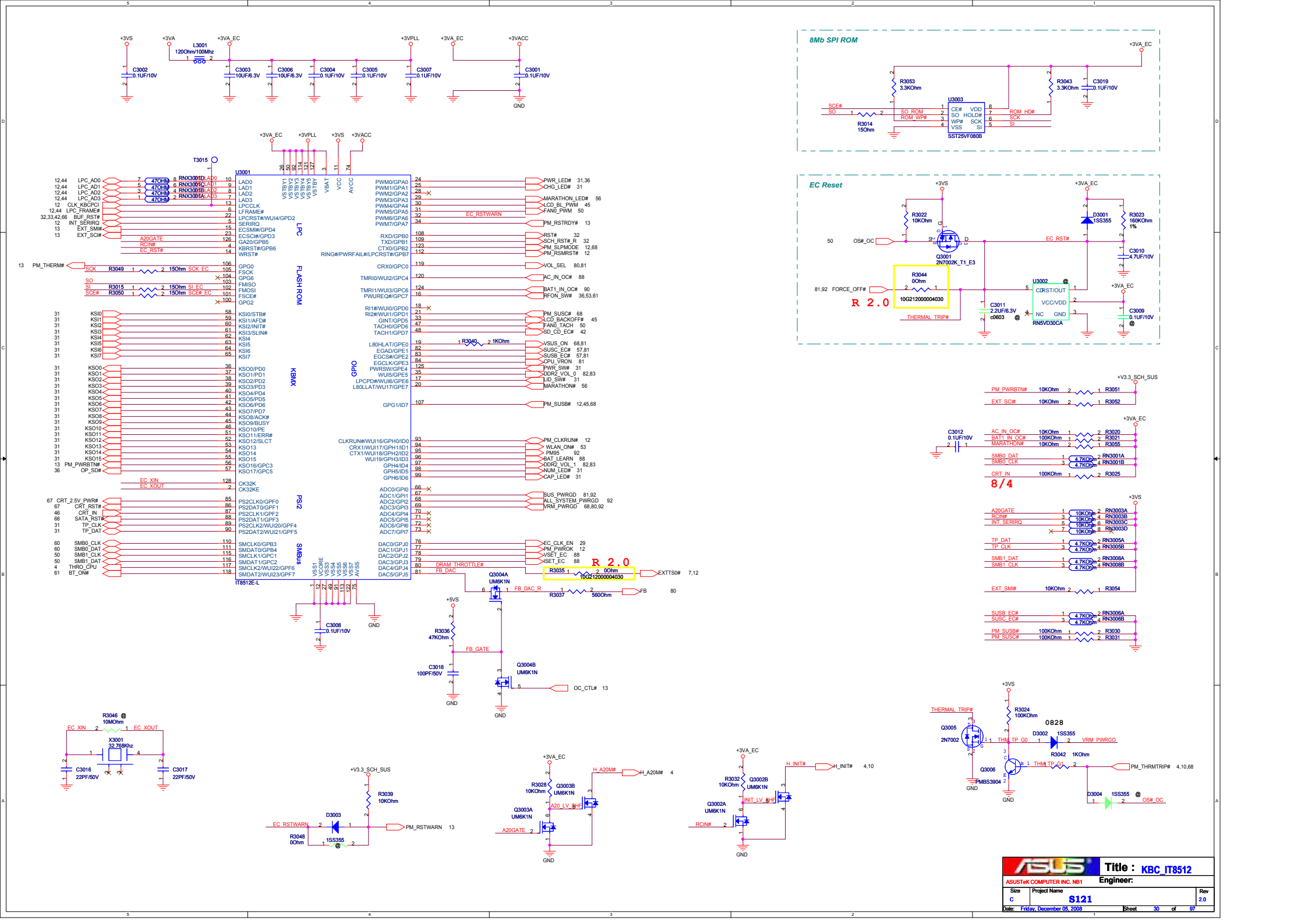
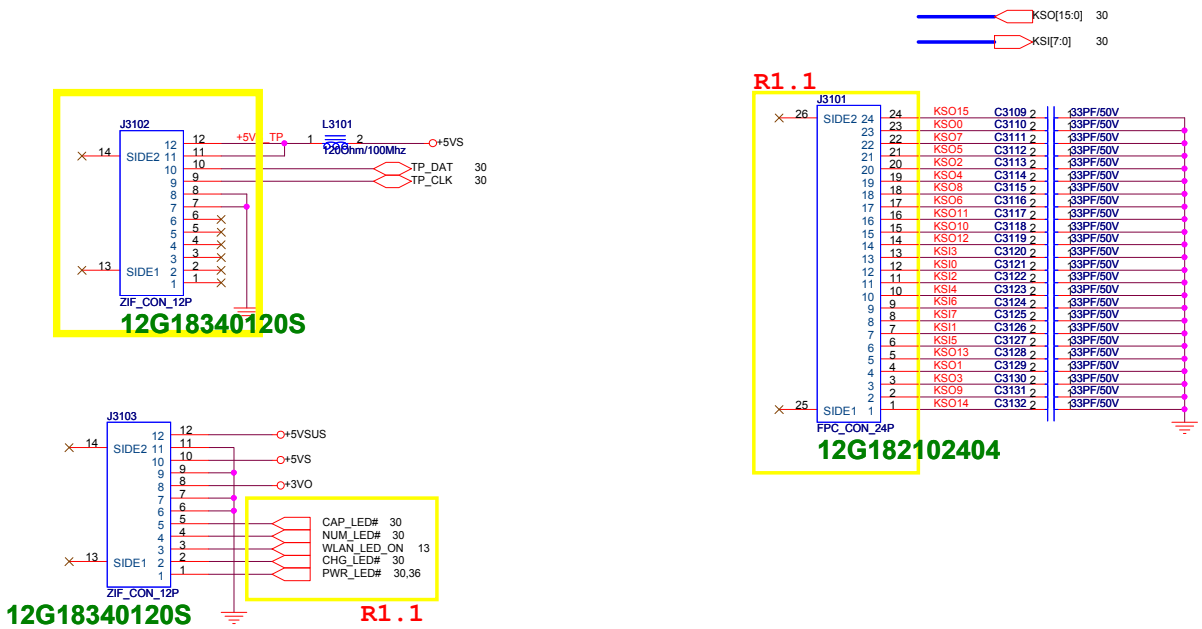

8Mb SPI ROM
U3003
SST25VF080B
EC Reset
Q3001
2N7002K_T1_E3
U3002
RN5VD30CA
U3001
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS/2
SMBus
8/4
R 2.0
Q3004A
UM6K1N
Q3004B
UM6K1N
Q3003A
UM6K1N
Q3003B
UM6K1N
Q3002B
UM6K1N
Q3002A
UM6K1N
Q3005
2N7002
Q3006
PMBS3904
X3001
32.768Khz
Title : KBC_IT8512
ASUSTeK COMPUTER INC. NB1
Engineer:
Size C
Project Name S121
Rev 2.0
Date: Friday, December 05, 2008
Sheet 30 of 97



ASUSTeK COMPUTER INC. NB1	Title : KBC_KB Conn.	Engineer:
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 31 of 97	

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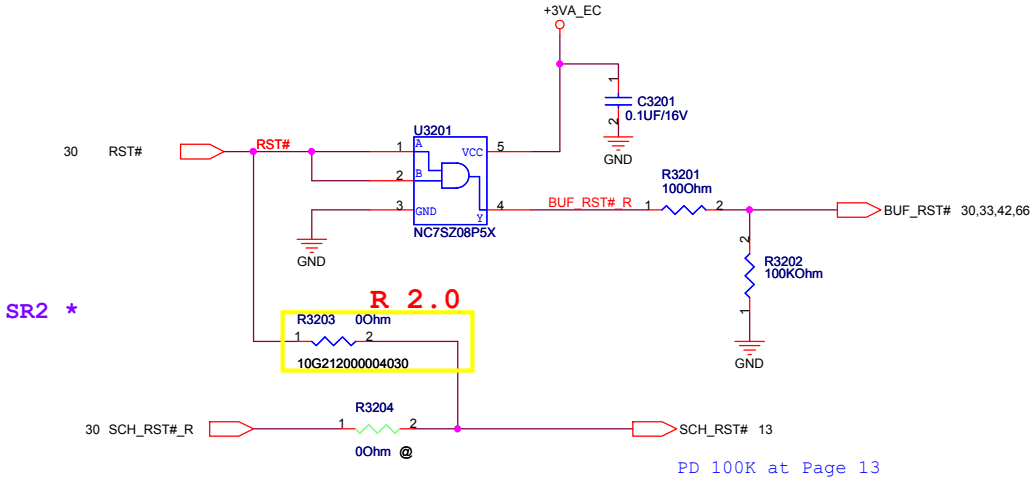
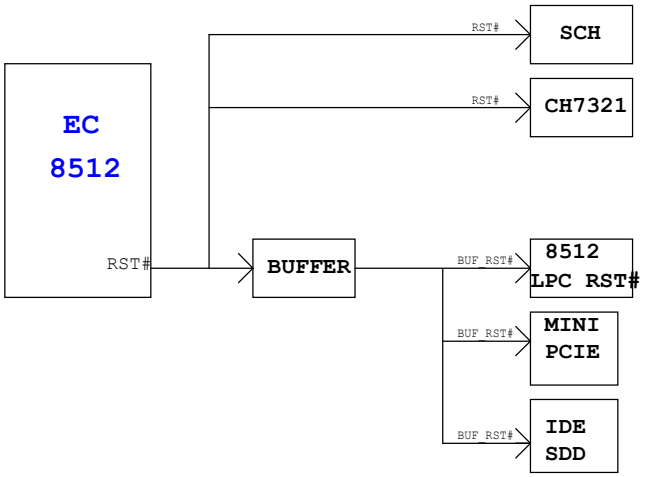
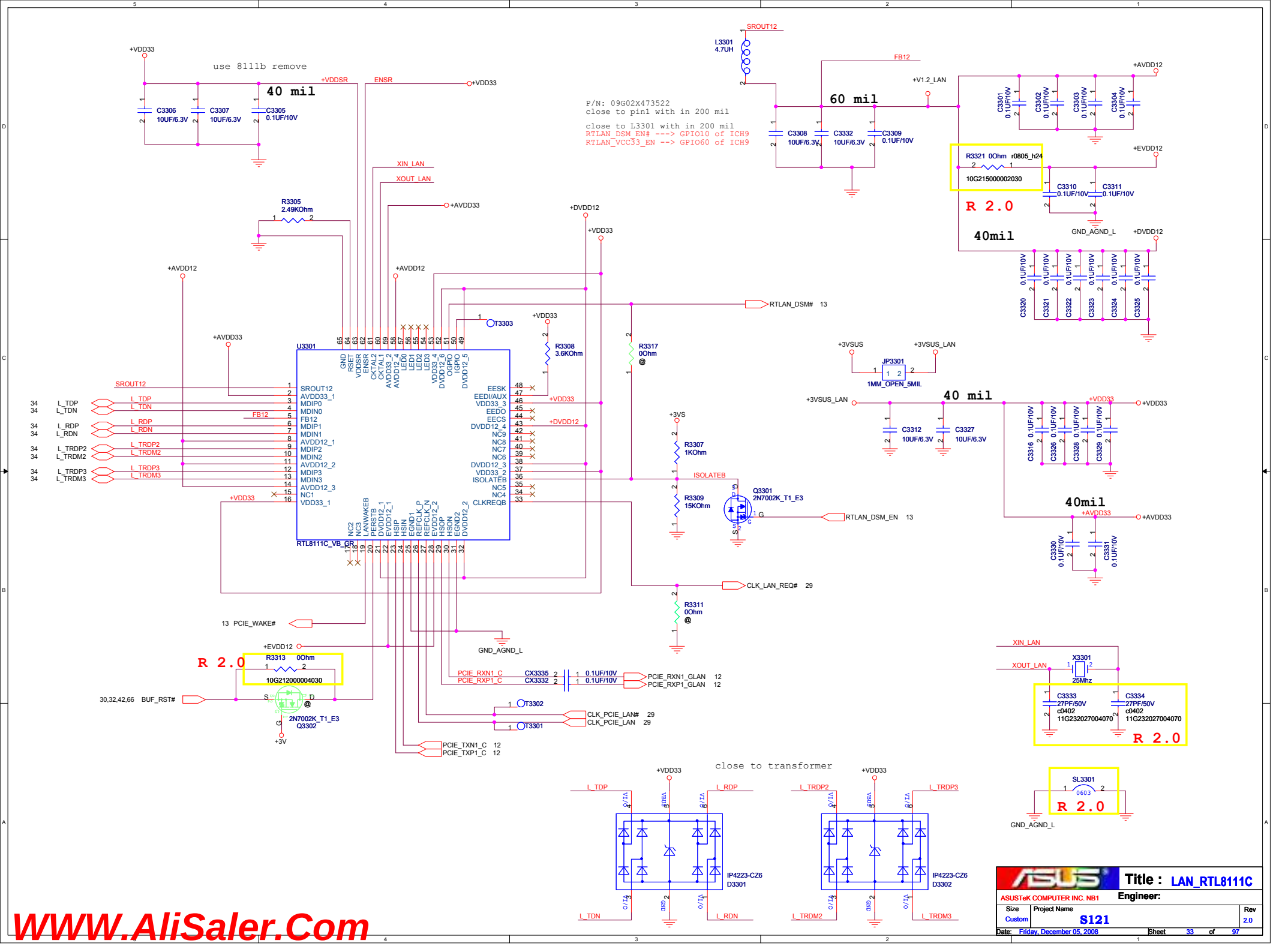




ASUS	Title : Reset Map	
ASUSTeK COMPUTER INC	Engineer:	
Size B	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 32 of 97	



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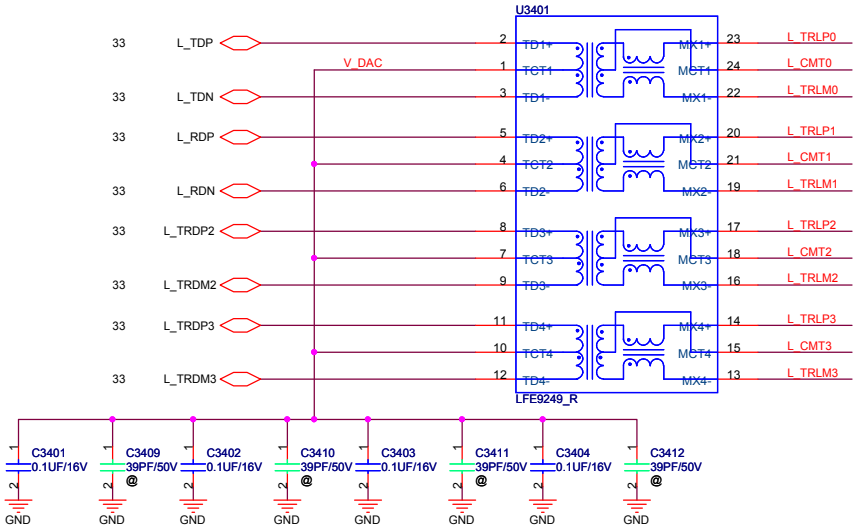
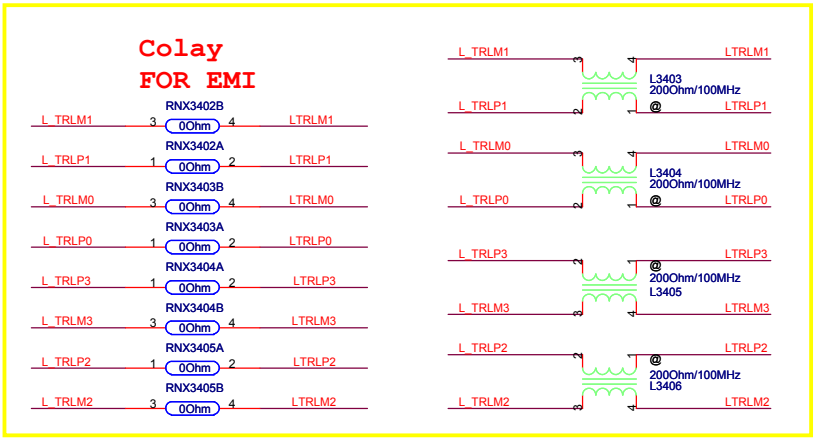
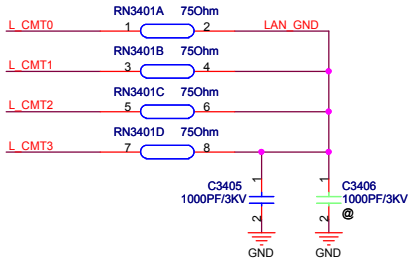
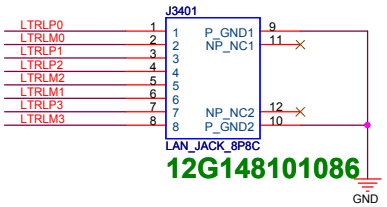
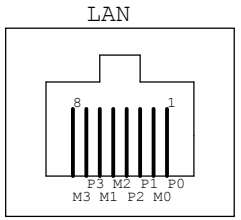


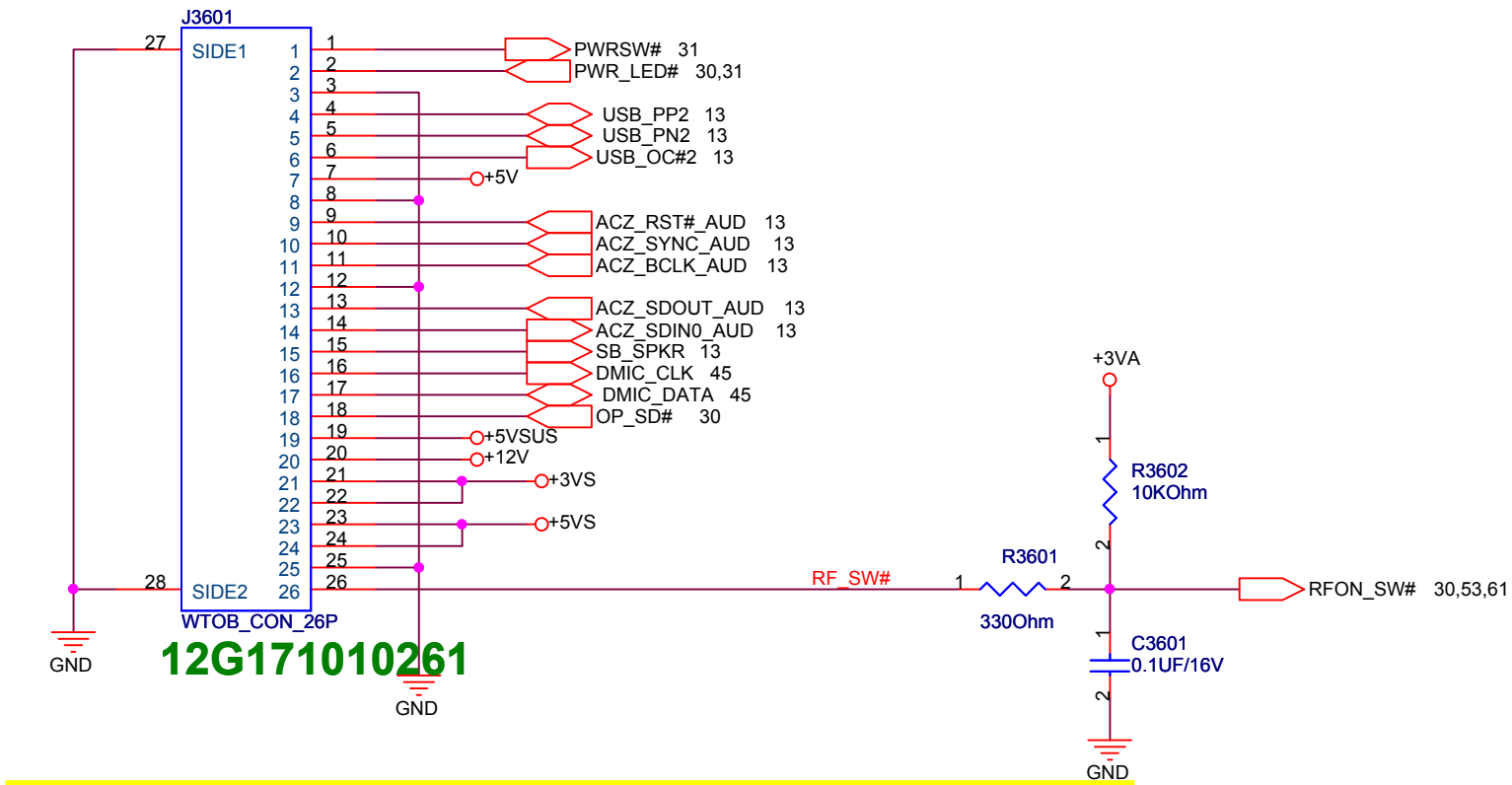








ASUSTeK COMPUTER INC. NB1	Title : RJ45	Engineer: <OrgAddr1>
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 34 of 97	



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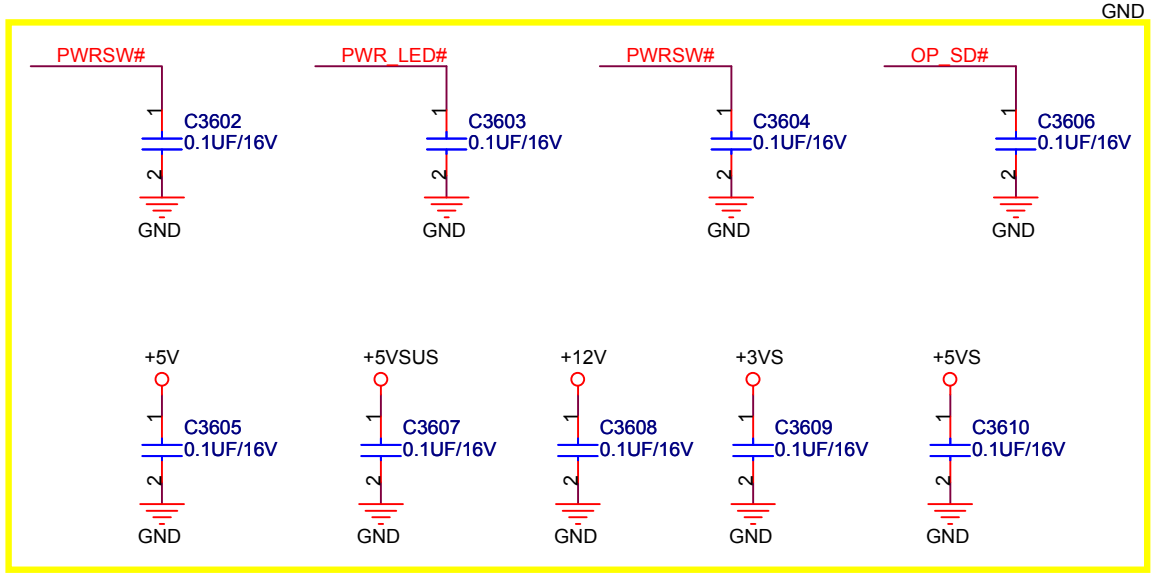

ASUSTeK COMPUTER INC. NB1	Title : IO CON	
	Engineer:	
Size A	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 36 of 97	

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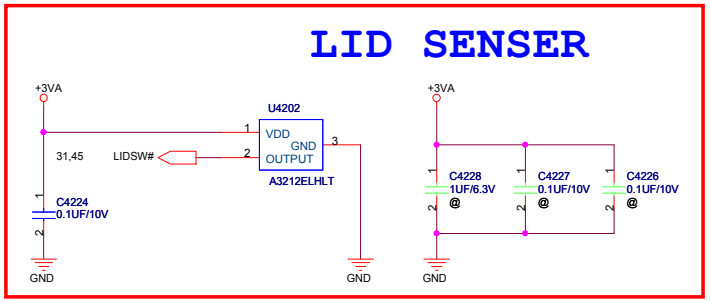
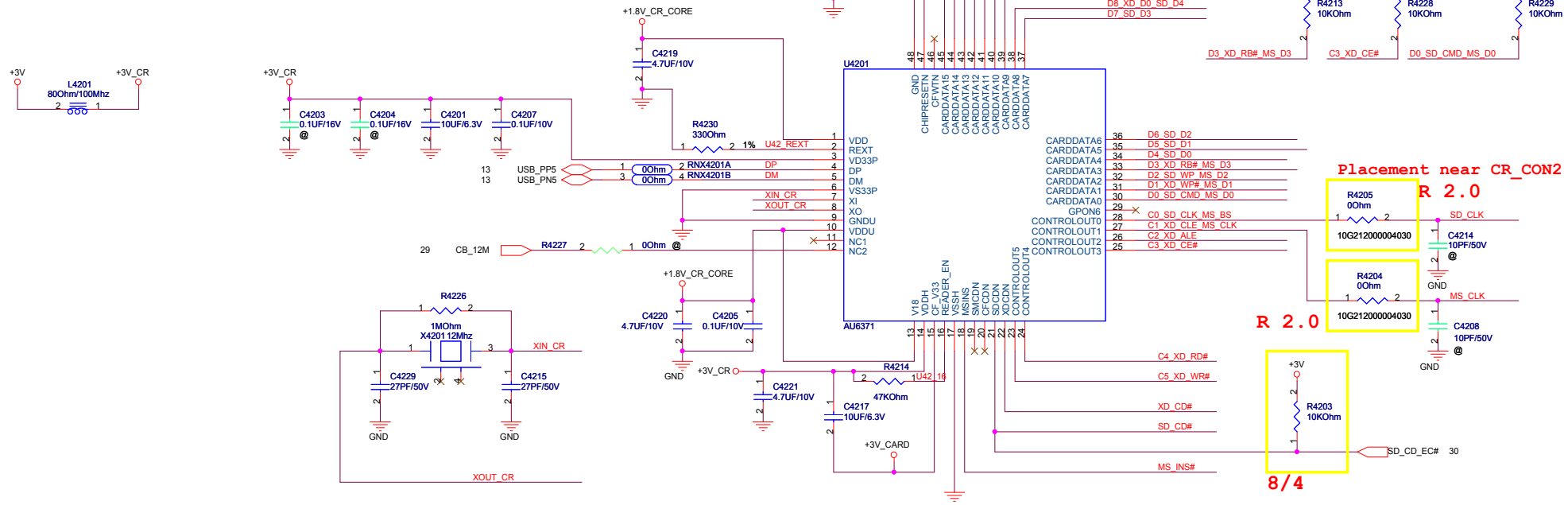
LID SENSER



Delete R4223 and R4206

2008/12/02 R 2.0



Placement near CR_CON2 R 2.0

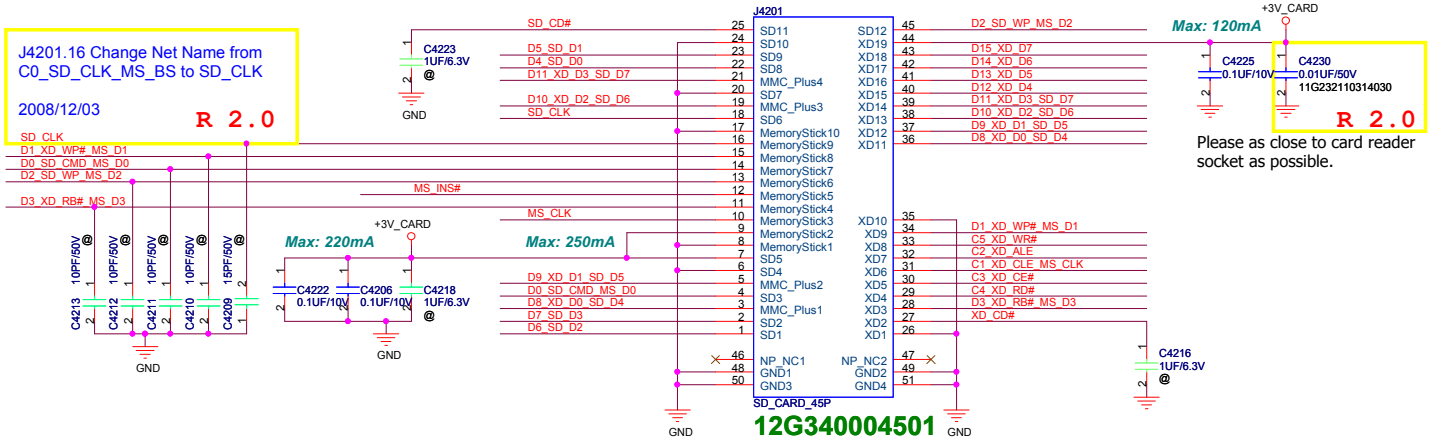
R 2.0

8/4

CARD READER

J4201.16 Change Net Name from C0_SD_CLK_MS_BS to SD_CLK

2008/12/03 R 2.0



Please as close to card reader socket as possible.

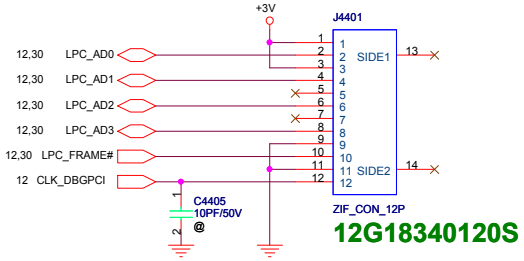
Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

Only SD2 disconnect

Delete R4224, R4225, R4222, Q4201 and Q4203

2008/12/02 R 2.0

ASUSTeK COMPUTER INC. NB1	Title : CB_AU6371		
	Engineer:		
Size: Custom	Project Name: S121		Rev: 2.0
Date: Friday, December 05, 2008	Sheet 42 of 97		



ASUSTeK COMPUTER INC. NB1	Title : BUG_LPC Debug		
	Engineer:		
Size: Custom	Project Name: S121		Rev: 2.0
Date: Friday, December 05, 2008	Sheet 44 of 97		

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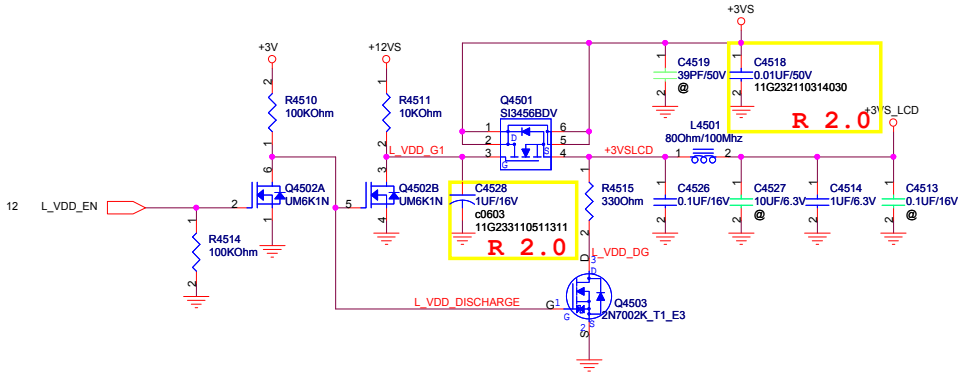
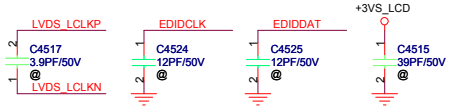
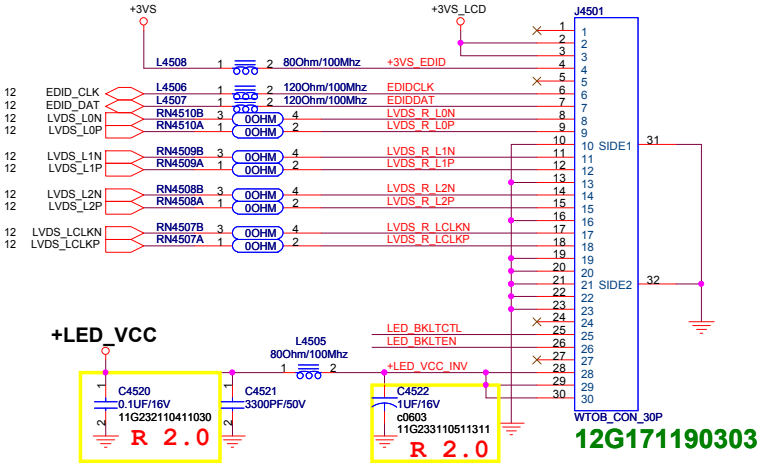
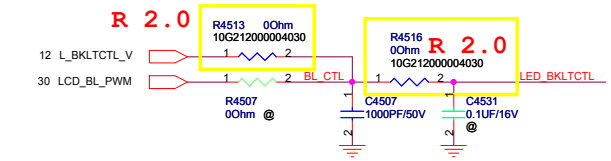
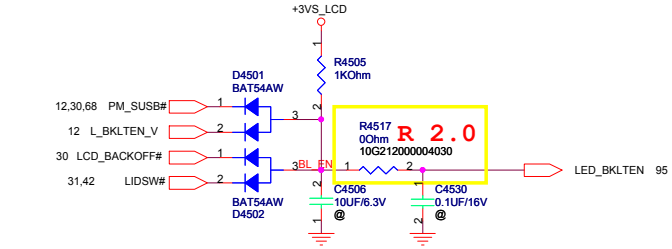
LCD Power

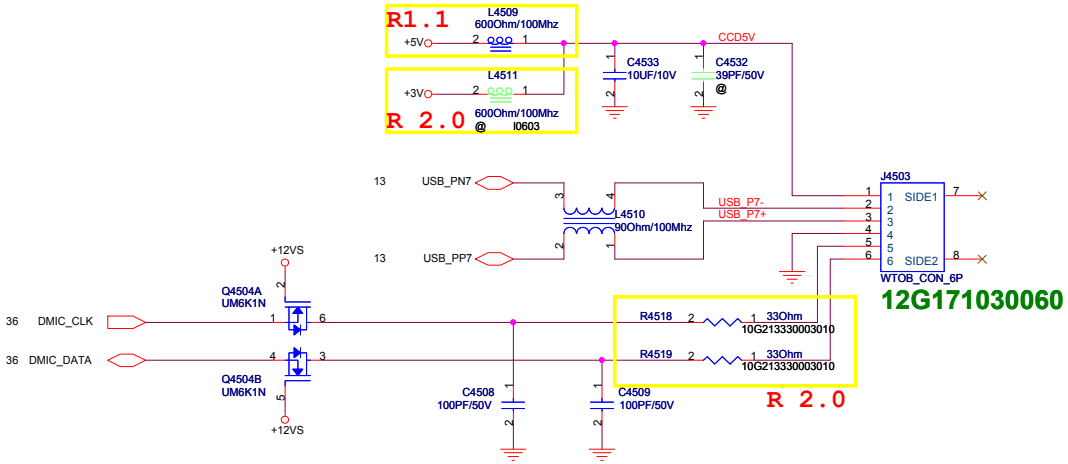




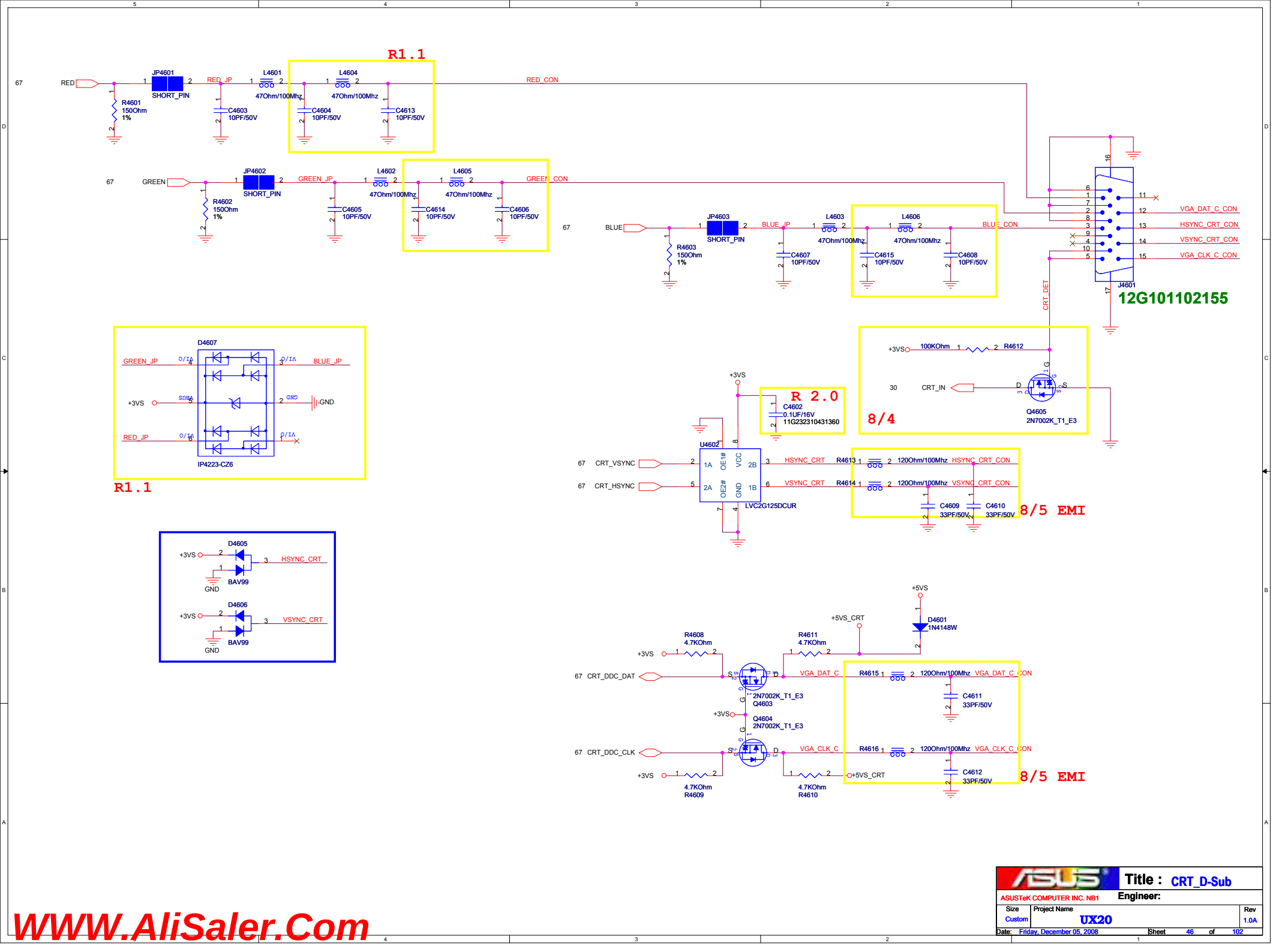








ASUSTeK COMPUTER INC. NB1	Title : CRT_LVDS	Engineer:
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 45 of 97	



ASUSTeK COMPUTER INC. NB1	Title : CRT_D-Sub	Engineer:
Size: Custom	Project Name: UX20	Rev: 1.0A
Date: Friday, December 05, 2008	Sheet 46 of 102	

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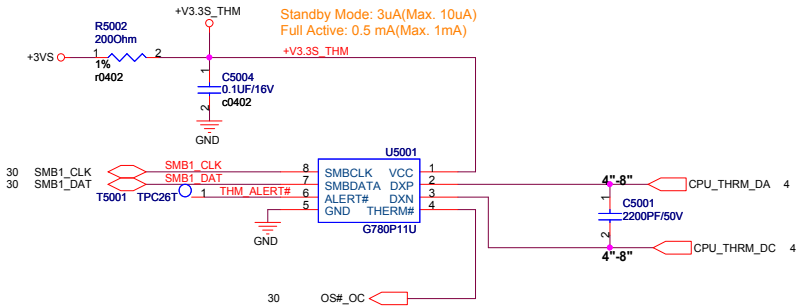
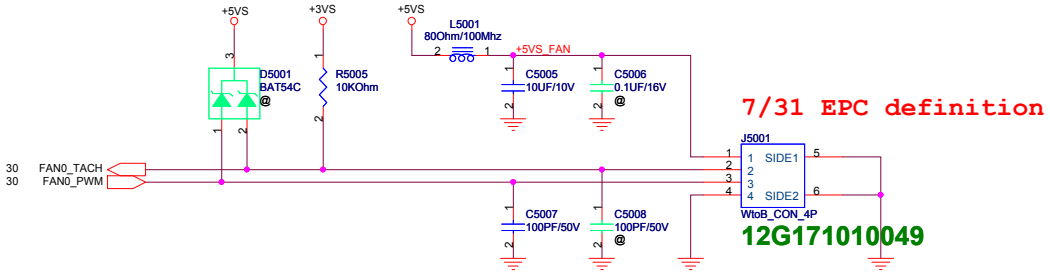
Thermal Sensor

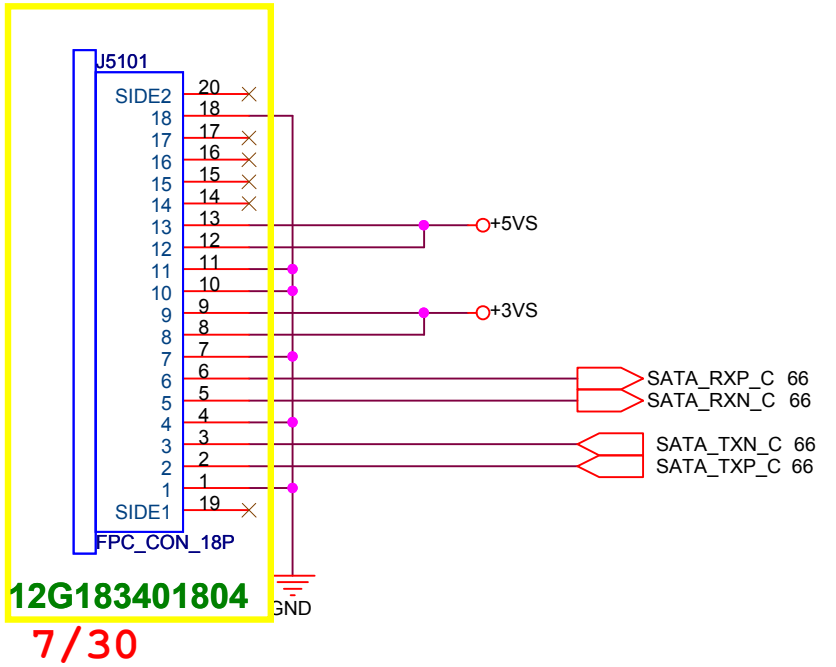


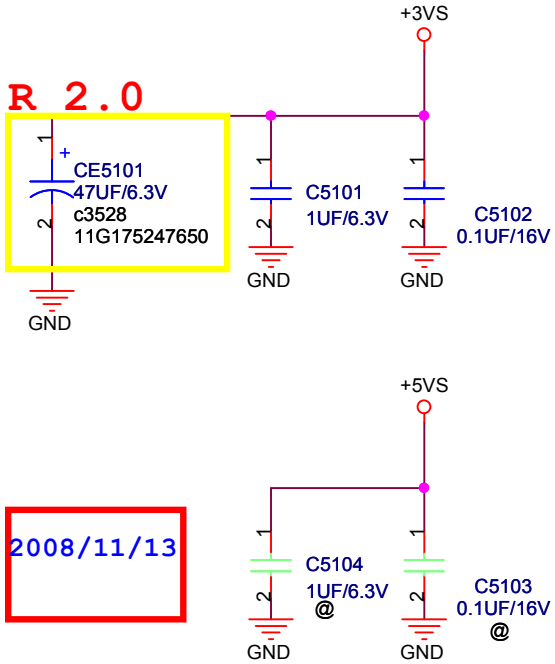
SMB Addr: 98

DC FAN Control



ASUSTeK COMPUTER INC. NB1	Title : FAN_Ther Sensor & Fan	
	Engineer:	
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 50 of 97	





ASUSTeK COMPUTER INC	Title : HDD CONNECTOR	
	Engineer:	
Size A	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 51 of 97	

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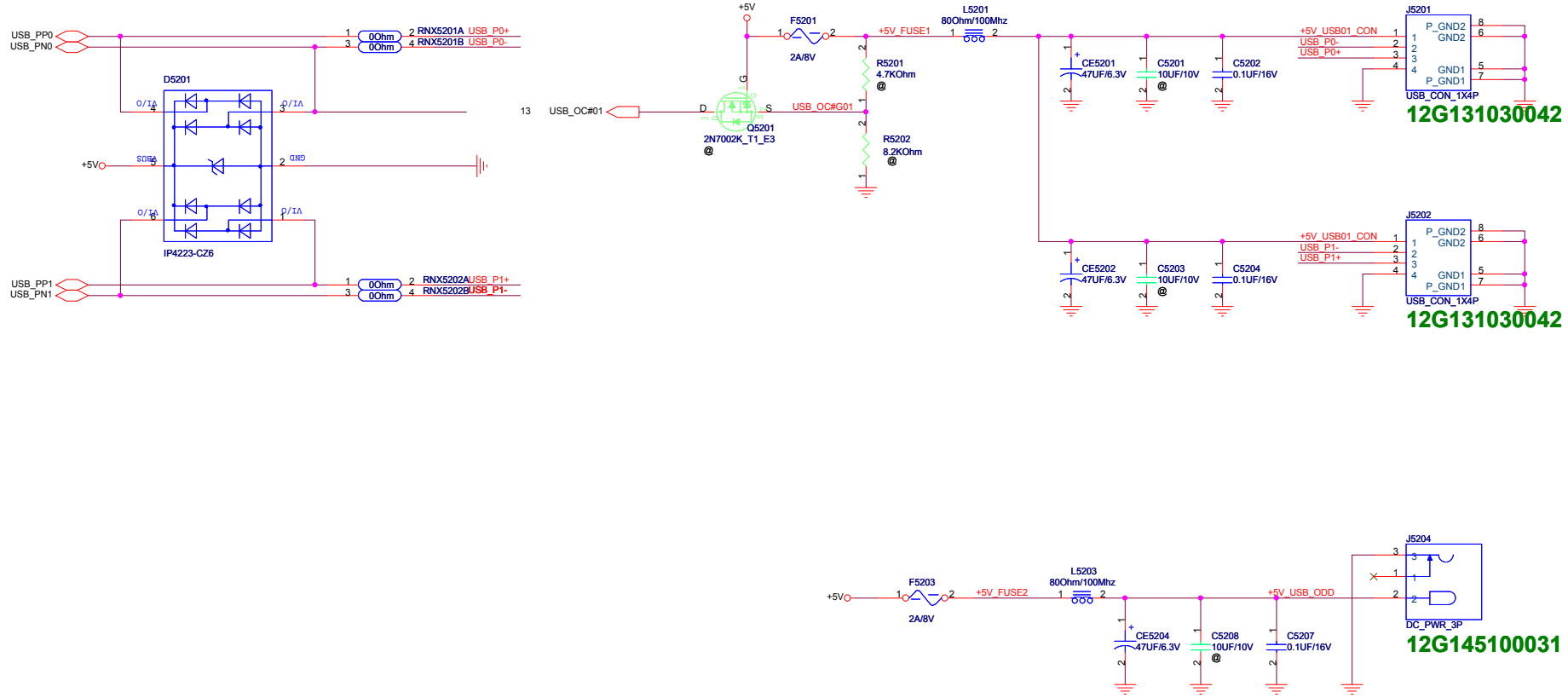
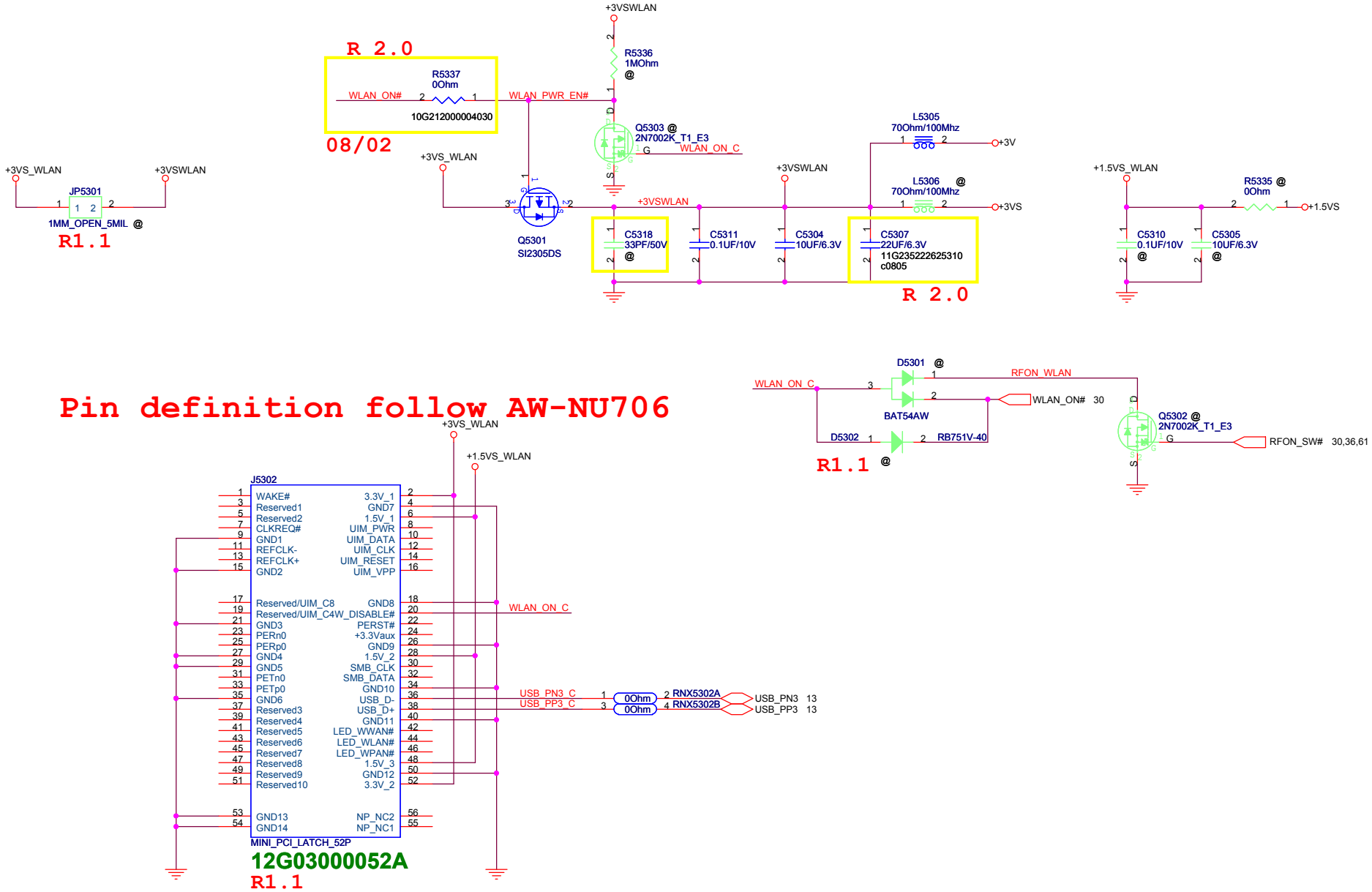


ASUSTeK COMPUTER INC. NB1	Title : USB_USB Port	Engineer:
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 52 of 97	



ASUSTeK COMPUTER INC. NB1	Title : PCI_MiniCard	
	Engineer:	
Size B	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 53 of 97	

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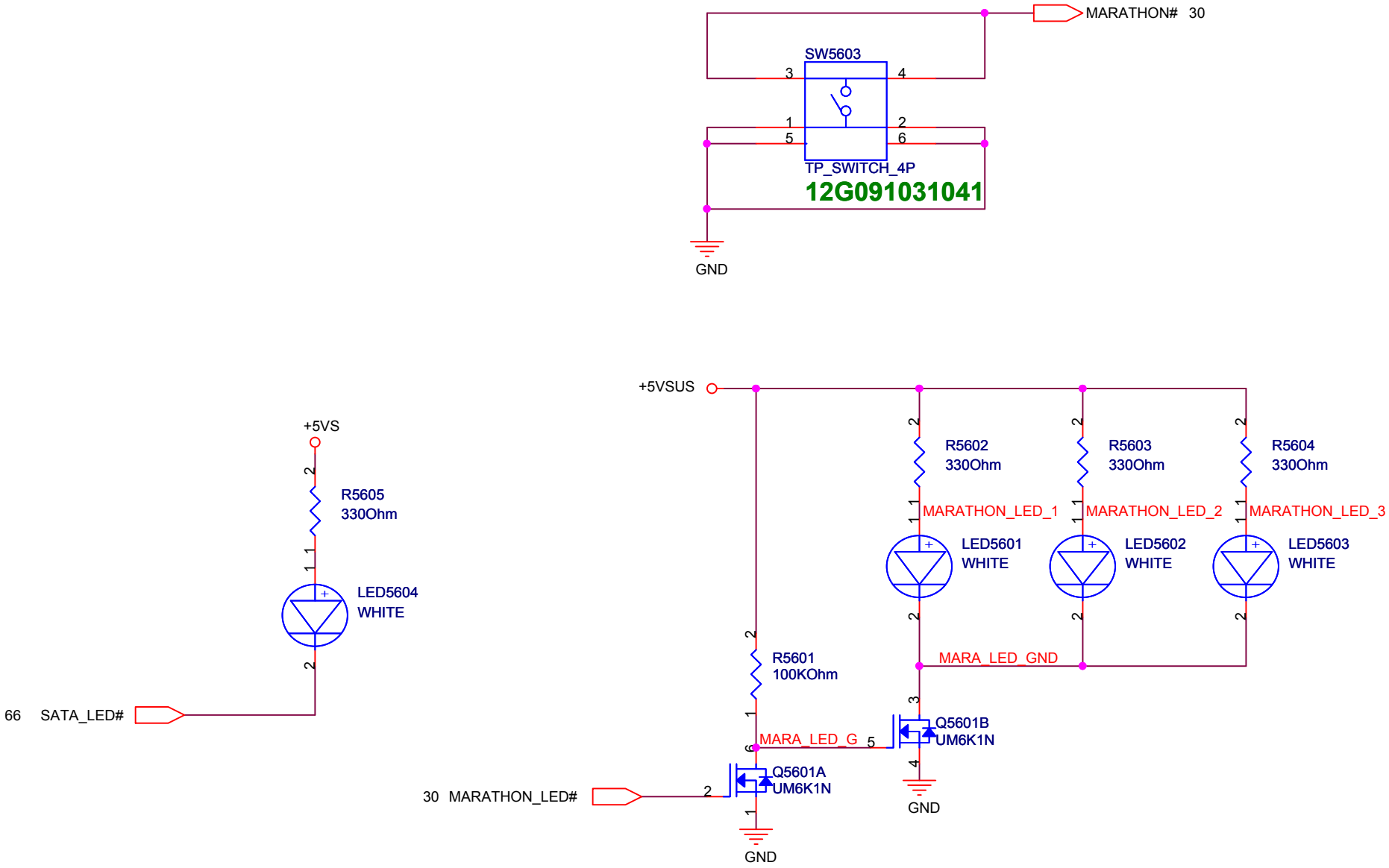
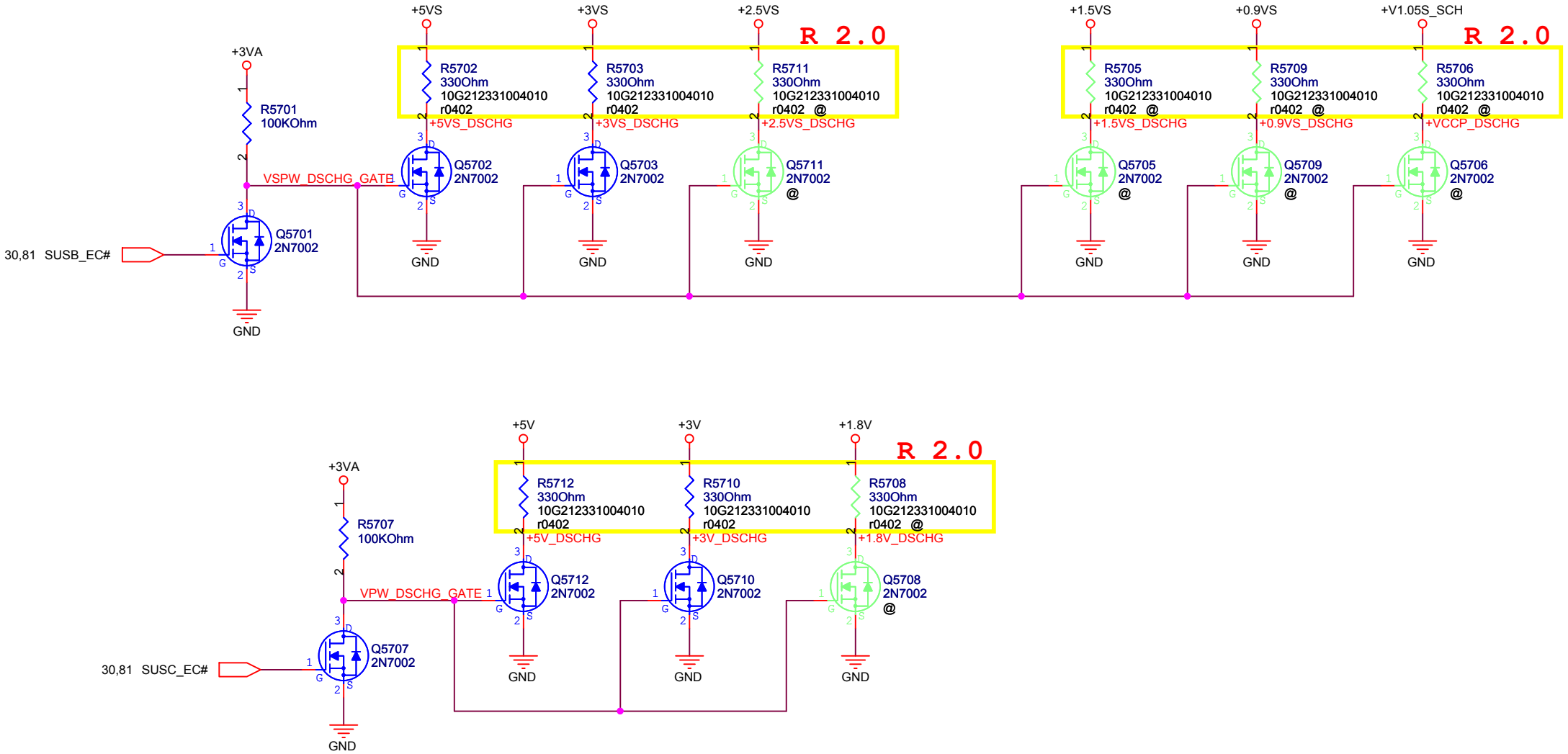


ASUSTeK COMPUTER INC. NB1	Title : SW&LED	
	Engineer:	
Size: A	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 56 of 97	



ASUSTeK COMPUTER INC. NB1	Title : Discharge	
	Engineer:	
Size A4	Project Name UX20	Rev 1.0A
Date: Friday, December 05, 2008	Sheet 57 of 102	

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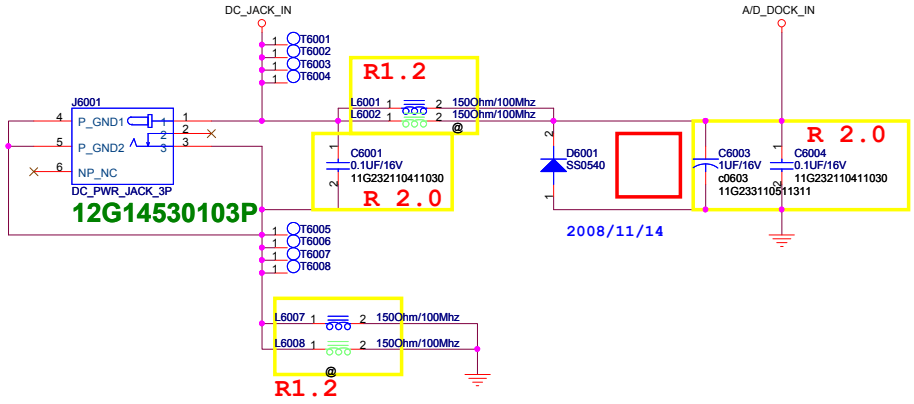
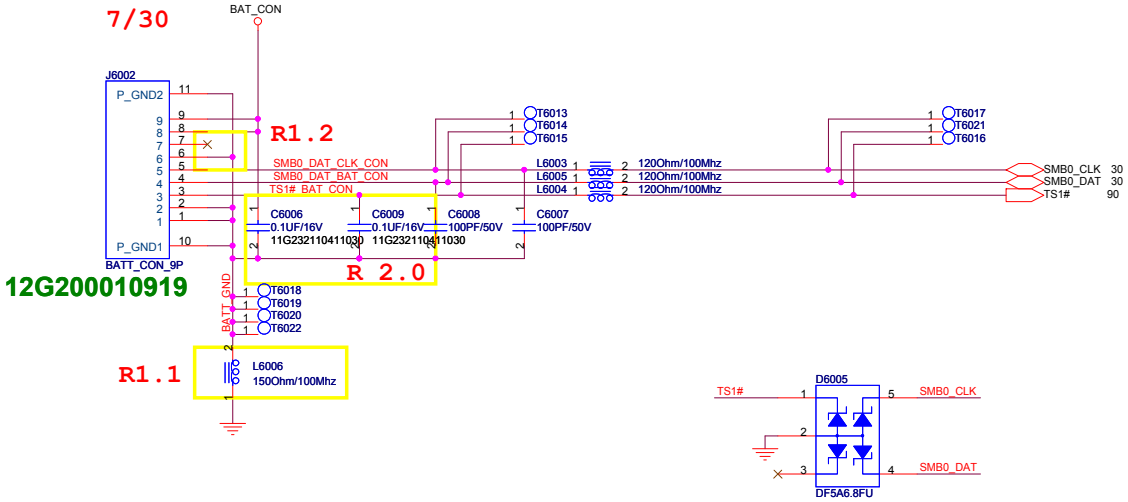
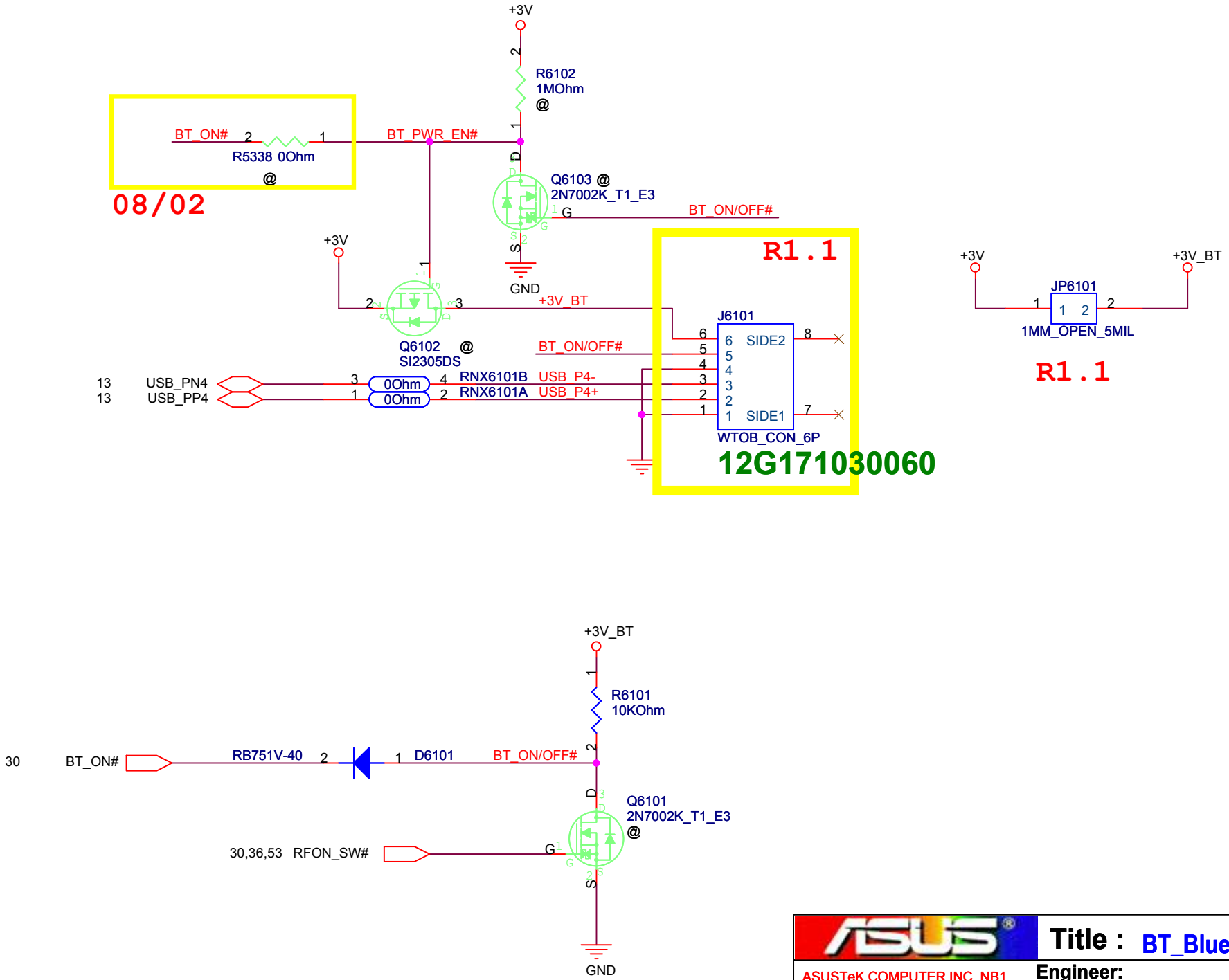
DC IN



BAT IN



ASUSTeK COMPUTER INC. NB1	Title : DC_DC & BAT IN	Engineer:
Size: Custom	Project Name: S121	Rev: 2.0
Date: Friday, December 05, 2008	Sheet 60 of 97	



ASUSTeK COMPUTER INC. NB1	Title : BT_Bluetooth	
	Engineer:	
Size A	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 61 of 97	

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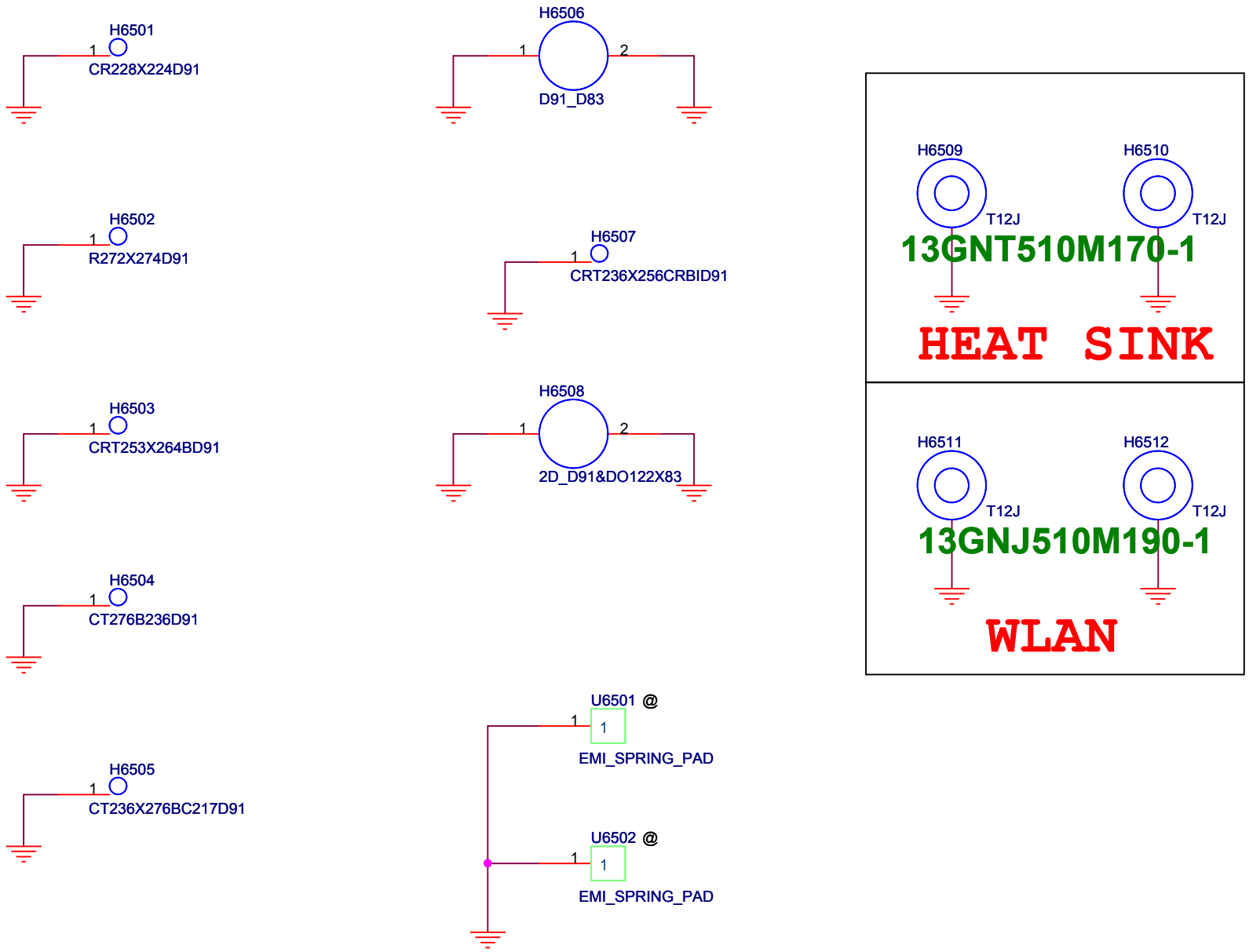
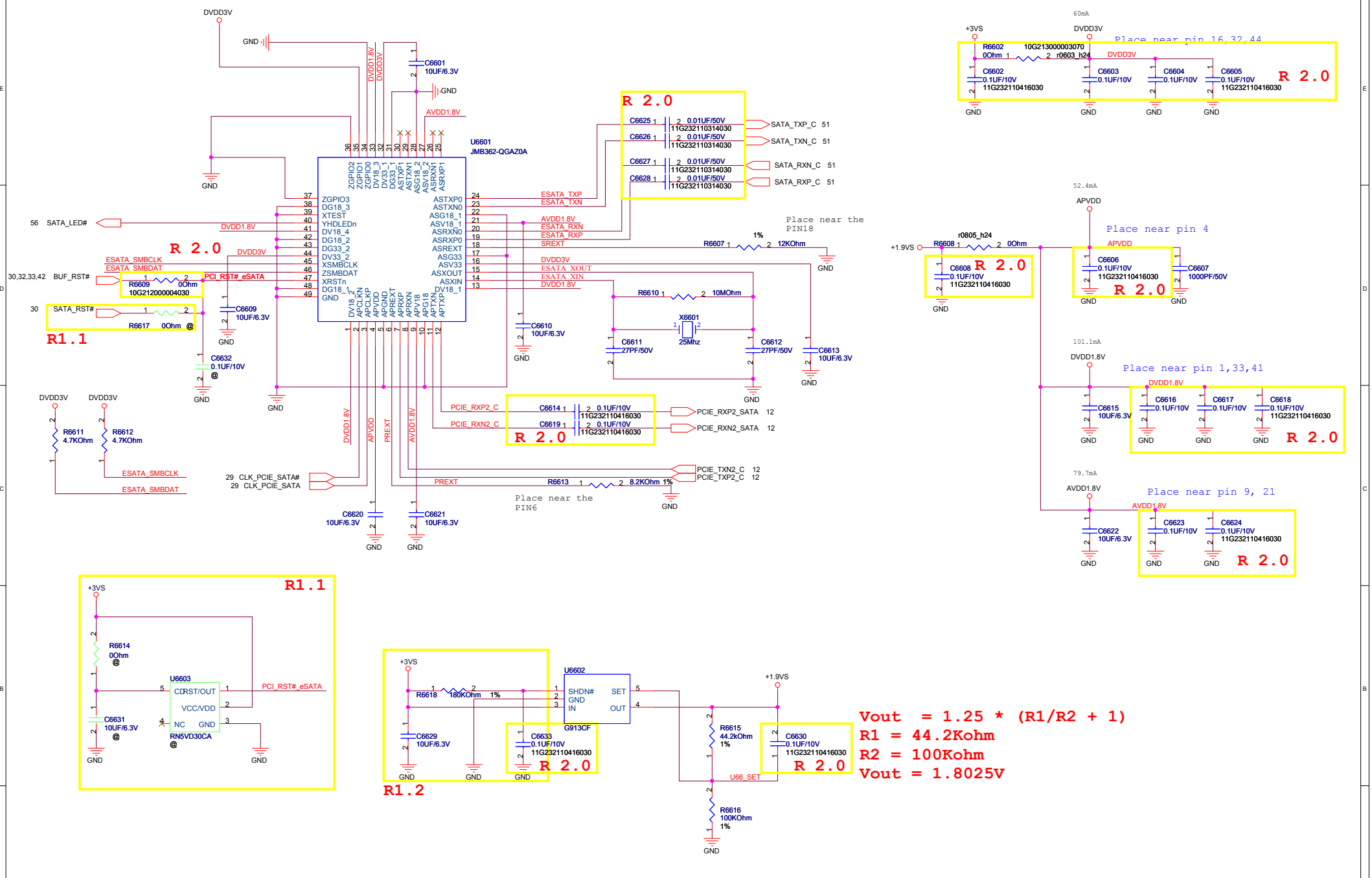


ASUS	Title : ME	
ASUSTeK COMPUTER INC. NB1	Engineer:	
Size A	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 65 of 97	



Title : ESA_E-SATA

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
Custom	S121	2.0

Date: Friday, December 05, 2008 Sheet 66 of 97

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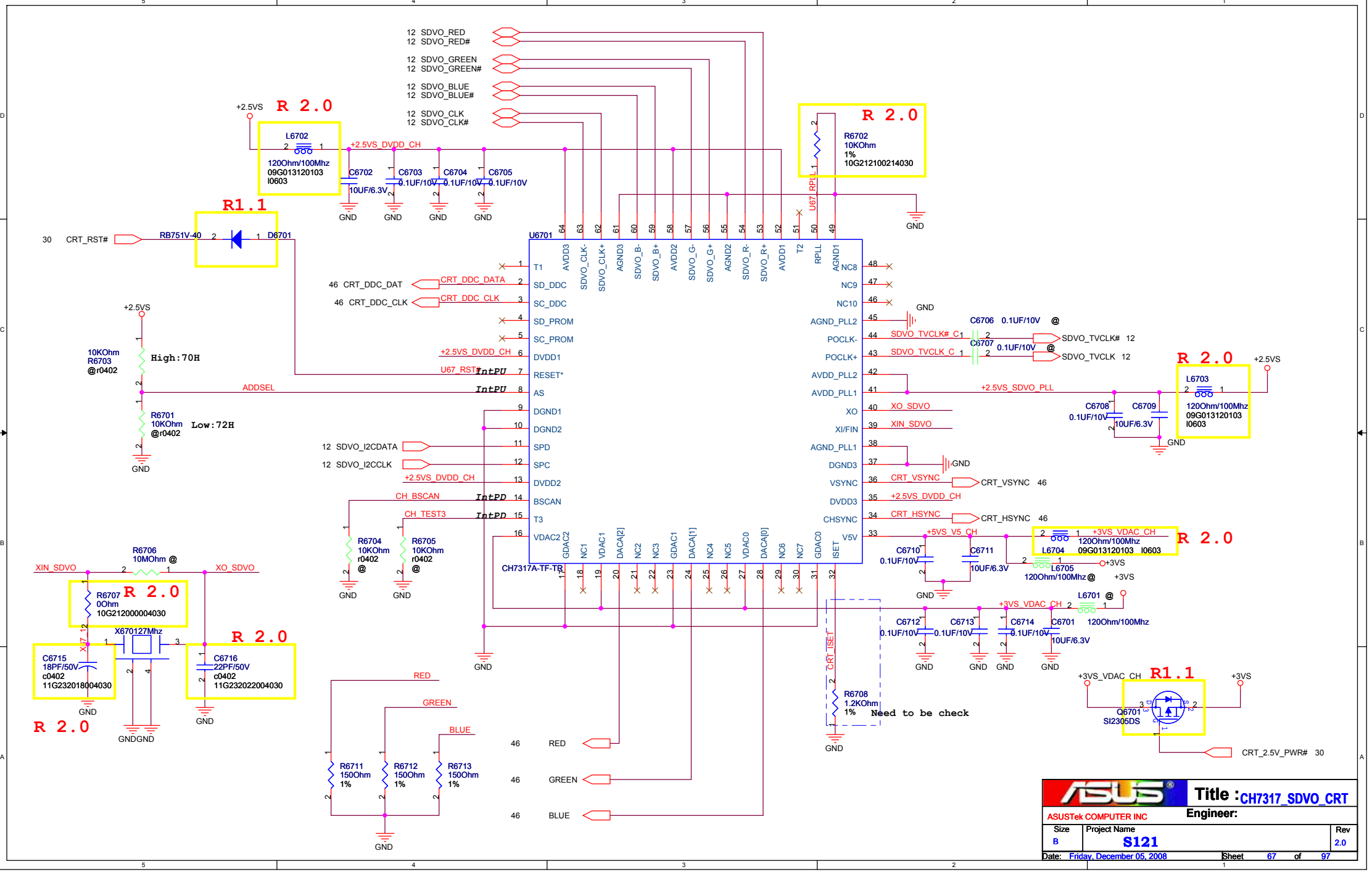
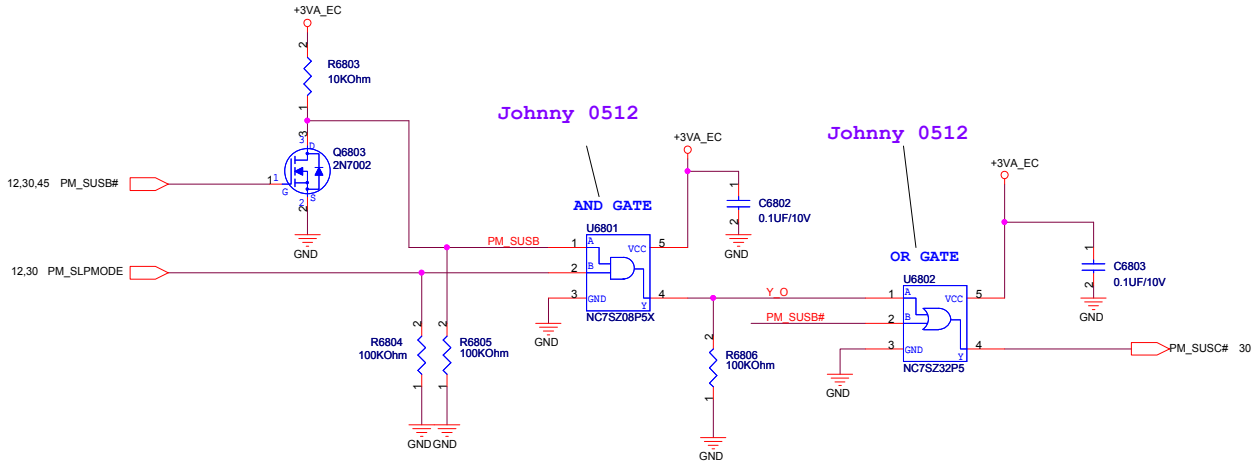
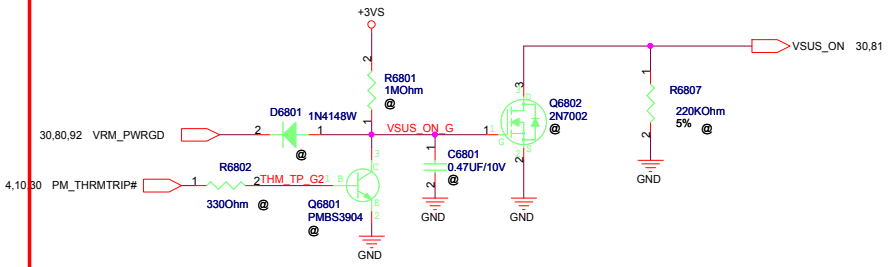

12 SDVO_RED
12 SDVO_RED#
12 SDVO_GREEN
12 SDVO_GREEN#
12 SDVO_BLUE
12 SDVO_BLUE#
12 SDVO_CLK
12 SDVO_CLK#
+2.5VS
R 2.0
L6702
120Ohm/100Mhz
09G013120103
I0603
+2.5VS_DVDD_CH
C6702
10UF/6.3V
C6703
0.1UF/10V
C6704
0.1UF/10V
C6705
0.1UF/10V
GND
R 2.0
R6702
10KOhm
1%
10G212100214030
U67_RPLL
R1.1
30 CRT_RST#
RB751V-40
D6701
U6701
46 CRT_DDC_DAT
CRT_DDC_DATA
46 CRT_DDC_CLK
CRT_DDC_CLK
+2.5VS
10KOhm
R6703
@r0402
High:70H
ADDSEL
R6701
10KOhm
@r0402
Low:72H
+2.5VS_DVDD_CH
U67_RST#
IntPU
12 SDVO_I2CDATA
12 SDVO_I2CCLK
CH_BSCAN
IntPD
CH_TEST3
R6704
10KOhm
r0402
@
R6705
10KOhm
r0402
@
CH7317A-TF-TR
SDVO_TVCLK# C
SDVO_TVCLK# 12
SDVO_TVCLK_C
SDVO_TVCLK 12
C6706 0.1UF/10V @
C6707 0.1UF/10V @
+2.5VS_SDVO_PLL
XO_SDVO
XIN_SDVO
CRT_VSYNC
CRT_VSYNC 46
CRT_HSYNC
CRT_HSYNC 46
+5VS_V5_CH
C6710
0.1UF/10V
C6711
10UF/6.3V
+3VS_VDAC_CH
L6704
09G013120103 I0603
L6705
120Ohm/100Mhz @
+3VS
L6703
120Ohm/100Mhz
09G013120103
I0603
C6708
0.1UF/10V
C6709
10UF/6.3V
R6706
10MOhm @
R6707
0Ohm
10G212000004030
X670127Mhz
C6715
18PF/50V
c0402
11G232018004030
C6716
22PF/50V
c0402
11G232022004030
GNDGND
CRT_ISET
R6708
1.2KOhm
1%
Need to be check
L6701 @
C6712
0.1UF/10V
C6713
0.1UF/10V
C6714
0.1UF/10V
C6701
10UF/6.3V
120Ohm/100Mhz
+3VS_VDAC_CH
R1.1
Q6701
SI2305DS
CRT_2.5V_PWR# 30
RED
GREEN
BLUE
R6711
150Ohm
1%
R6712
150Ohm
1%
R6713
150Ohm
1%
46 RED
46 GREEN
46 BLUE
ASUSTek COMPUTER INC
Title : CH7317_SDVO_CRT
Engineer:
Size B
Project Name S121
Rev 2.0
Date: Friday, December 05, 2008
Sheet 67 of 97



EC	SCH
PM_SUSB#	PM_SLPRDY#
PM_SUSC#	$\overline{\text{PM_SLPRDY\#}}$ * PM_SLPMODE +PM_SLPRDY#



ASUSTeK COMPUTER INC. NB1

Title : Power_UP

Engineer:

Size	Project Name	Rev
Custom	S121	2.0

Date: Friday, December 05, 2008 Sheet 68 of 97

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History

_R 2.0_

2008/11/28

1. Change Part Number from 11G232110311030 to 11G232110311030
   C3106,C3107,C4230,C4518
2. Change Part Number from 11G232110311150 to 11G232110311030
   C6625,C6626,C6627,C6628
3. Change Part Number from 11G232210416360 to 11G232110416030
   C0705,C0707,C0708,C0709,C0710,C0711,C0902,C0903,C0904,C0905
4. Change Part Number from 11G232110416360 to 11G232110416030
   C6602,C6603,C6604,C6605,C6606,C6608,C6614,C6616,C6617,C6618,C6619,C6623,C6624,C6630,C6633
5. Change Part Number from 11G232310431390 to 11G232310431360
   C4602
6. Change Part Number and Package Size from 11G233110412320 & 0603 to 11G232110411030 & 0402
   C4520,C6001,C6004,C6006,C6009
7. Change Part Number from 10G212000004010 to 10G213000003070
   R1408,R4518,R4519
8. Change Part Number from 10G213000003030 to 10G213000003070
   R6602
9. Change Part Number from 10G212000004010 to 10G212000004030
   R1352,R3035,R3044,R3203,R3313,R4204,R4205,R4223,R4224,R4225,R4513,R4516,R4517,R5337,R6609,R6707
10. Change Part Number from 10G215000002010 to 10G215000002030
    R3321
11. Change Part Number from 10G212100214010 to 10G212100214030
    R6702
12. Change Part Number from 10G212106004010 to 10G212106004030
    R1208
13. Change Part Number from 10G213100003030 to 10G213100003020
    R1407
14. Change Part Number & Package size from 10G212100004070 & 0402 to 10G213100003020 & 0603
    R1410
15. Change Part Number from 11G232010004030 to 11G232010004320
    C1221,C1222,C1223,C1224
16. Change Part Number from 11G235210615030 to 11G235210615361
    C1302,C1303,C1304
17. Change Part Number & Package size from 09G01C120400 & 0402 to 09G013120103 & 0603
    L1401
18. Change Part Number from 09G013120114 to 09G013120103
    L2902,L2903,L2904,L6702,L6703,L6704
19. Change Part Number from 11G235310532320 to 11G233110511311
    C4522,C4528,C6003
20. Change Part Number from 11G233222515320 to 11G233222516360
    C1408,C1409
21. Change Part Number and Package Size from 11G233022004320 & 0603 to 11G232022004030 & 0402
    C6716
22. Change Part Number from 11G235222625360 to 11G235222625310
    C5307
23. Change Part Number and Package Size from 11G233027004320 & 0603 to 11G232027004070 & 0402
    C2910,C2911,C3333,C3334
24. Change Part Number and Package Size from 10G213331003030 & 0603 to 10G213331003030 & 0402
    R5702,R5703,R5705,R5706,R5708,R5709,R5710,R5711,R5712
25. Change Part Number from 11G08B247650 to 11G175247650
    CE5101
26. Change Part Number and Package Size from 11G233018004320 & 0603 to 11G232018004030 & 0402
    C6715
27. Add a reserve resistor L4511 to connect with +3V and J4503.1

2008/12/02

28. Delete R4223, R4206, R4224, R4225, R4222, Q4201 and Q4203
29. J4201.23 change net name from D5_SD_D1_SDcon to D5_SD_D1
30. J4201.1 change net name from D6_SD_D2_SDcon to D6_SD_D2
31. J4201.27 change net name from XD_CD#_Dcon to XD_CD#

2008/12/03

32. J4201.16 Change Net Name from C0_SD_CLK_MS_BS to SD_CLK

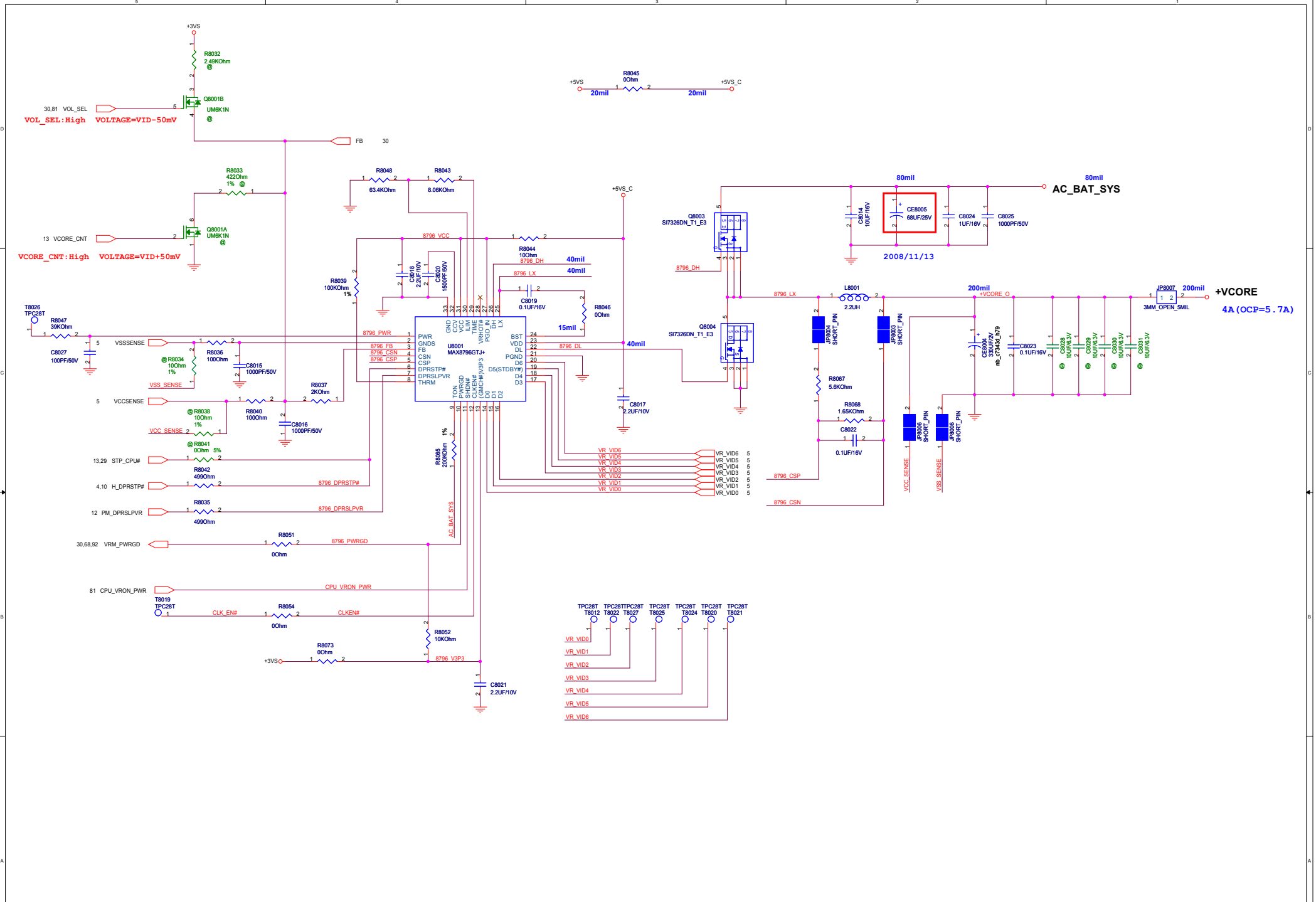
2008/12/04

33. Add R1233 and connect with PM_PWROK and PM_PWROR_R (U1001.C49)

2008/12/05

34. DNI C4216, C4223
35. Per EMI, add DMIC filter 33ohm, 100pF
    CRT filter 47ohm, 10pF
36. DNI discharge circuits: +2.5VS, +1.5VS, +0.9VS, +1.05S_SCH, +1.8V

ASUS	Title : EE_History	
ASUSTeK COMPUTER INC. NB1	Engineer:	
Size A4	Project Name S121	Rev 2.0
Date: Friday, December 05, 2008	Sheet 79 of 97	



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<Variant Name>

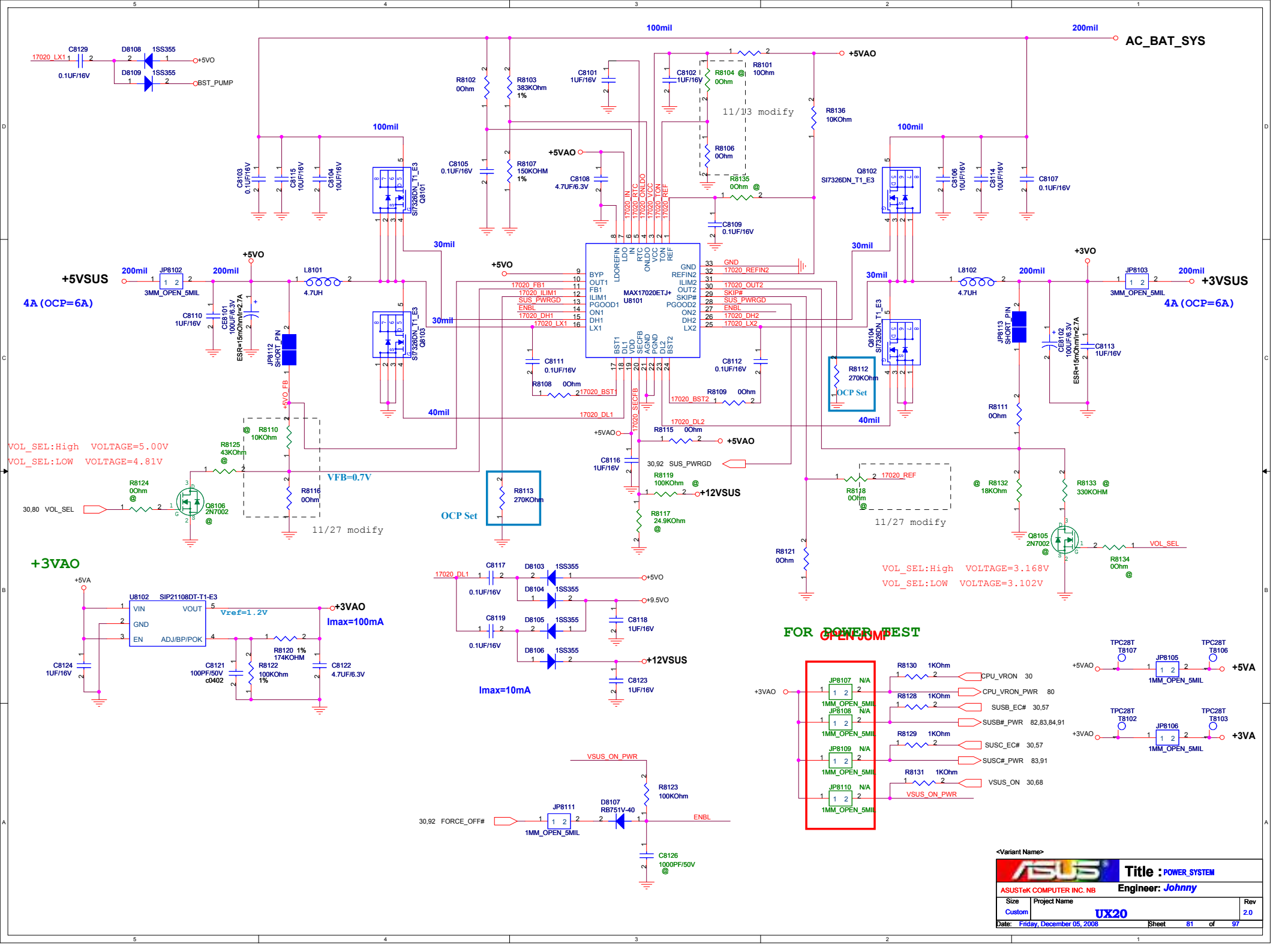
ASUSTeK COMPUTER INC. NB

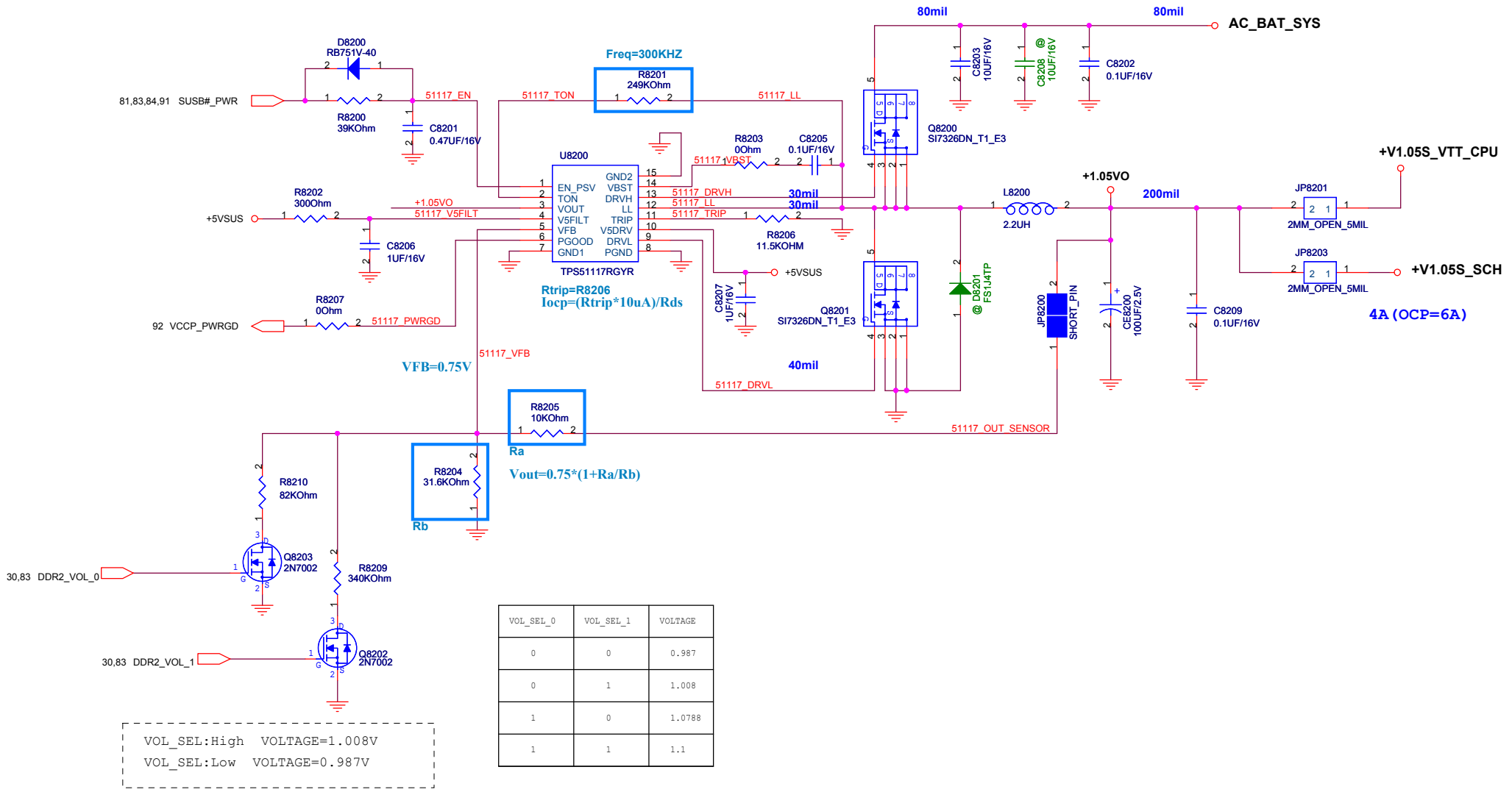
Title : POWER_VCORE

Engineer: Johnny

Size	Project Name	Rev
C	UX20	2.0

Date: Friday, December 05, 2008 Sheet 80 of 97


AC_BAT_SYS
+5VSUS
4A (OCP=6A)
+3VSUS
4A (OCP=6A)
MAX17020ETJ+
U8101
VOL_SEL:High VOLTAGE=5.00V
VOL_SEL:LOW VOLTAGE=4.81V
VFB=0.7V
OCP Set
11/27 modify
11/13 modify
+3VAO
Vref=1.2V
Imax=100mA
Imax=10mA
VOL_SEL:High VOLTAGE=3.168V
VOL_SEL:LOW VOLTAGE=3.102V
FOR POWER TEST
OPEN JUMP
Title : POWER_SYSTEM
ASUSTeK COMPUTER INC. NB
Engineer: Johnny
Project Name
UX20
Rev
2.0
Date: Friday, December 05, 2008
Sheet 81 of 97



VOL_SEL_0	VOL_SEL_1	VOLTAGE
0	0	0.987
0	1	1.008
1	0	1.0788
1	1	1.1

<Variant Name>

Title : POWER_I/O_+1.05VO

ASUSTeK COMPUTER INC. NB1

Engineer:

Size	Project Name	Rev
B	UX20	2.0

Date: Friday, December 05, 2008 Sheet 82 of 97

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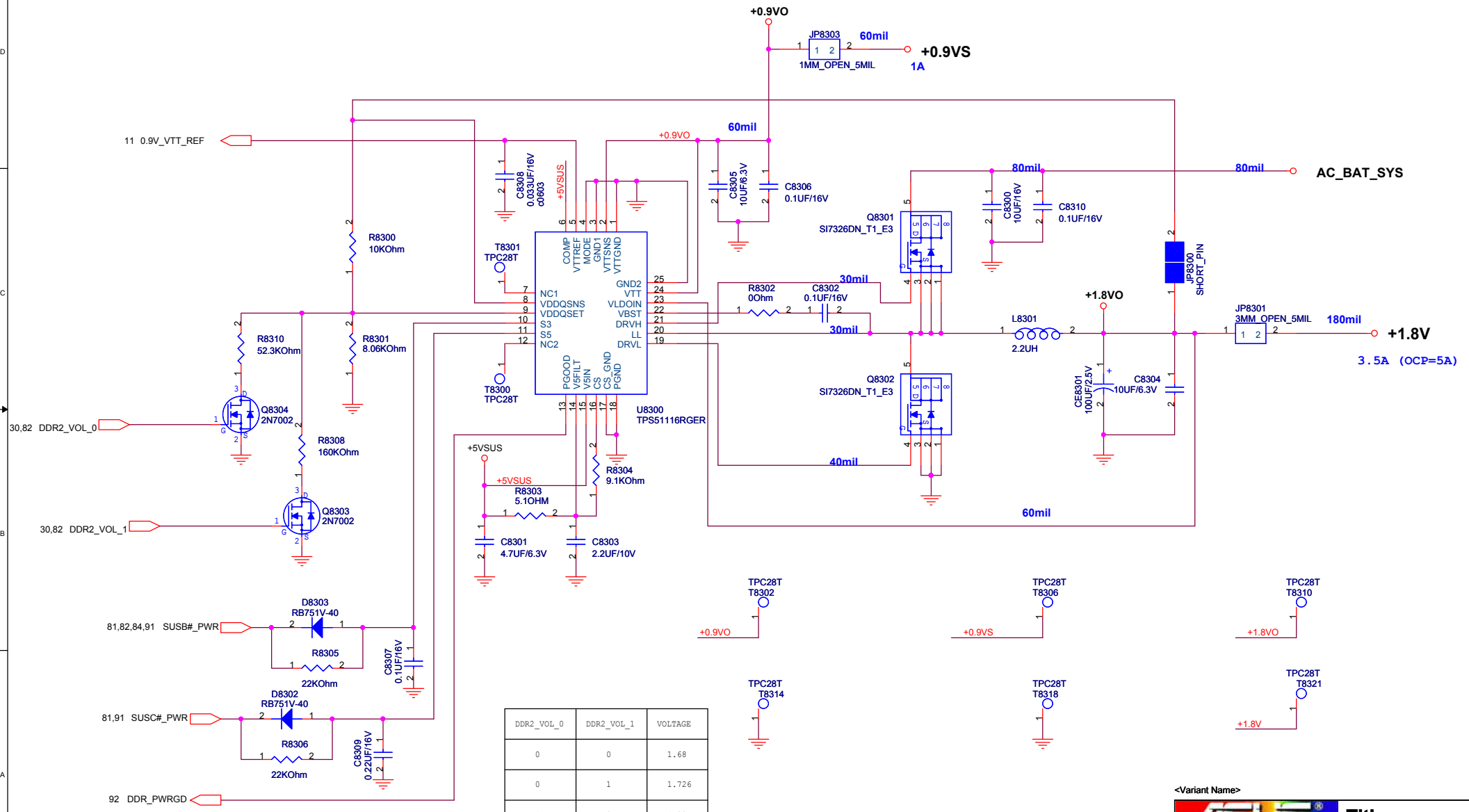

DDR2_VOL_0	DDR2_VOL_1	VOLTAGE
0	0	1.68
0	1	1.726
1	0	1.824
1	1	1.87

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : POWER_I/O_DDR & VTT	
	Engineer: Johnny	
Size: B	Project Name: UX20	Rev: 2.0
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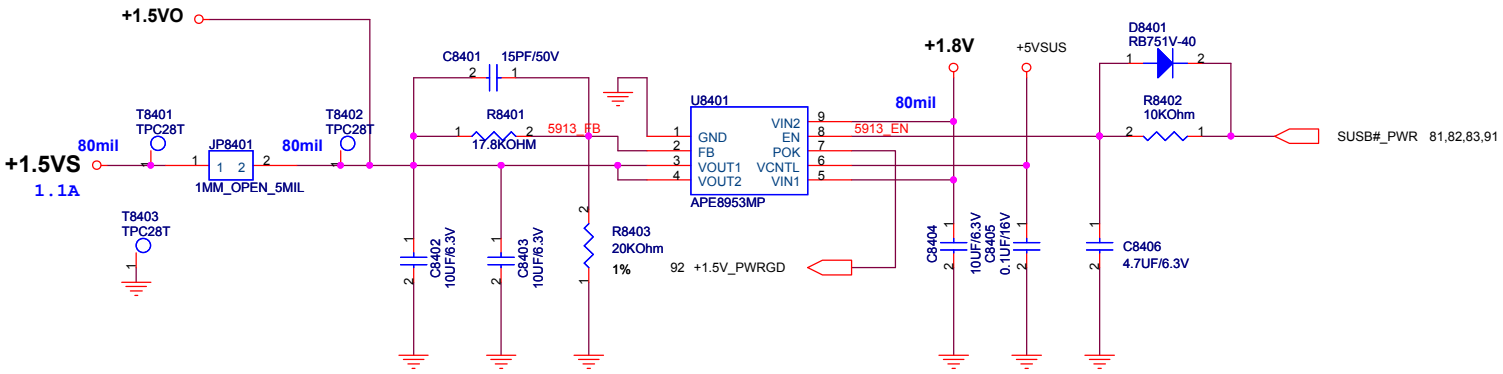
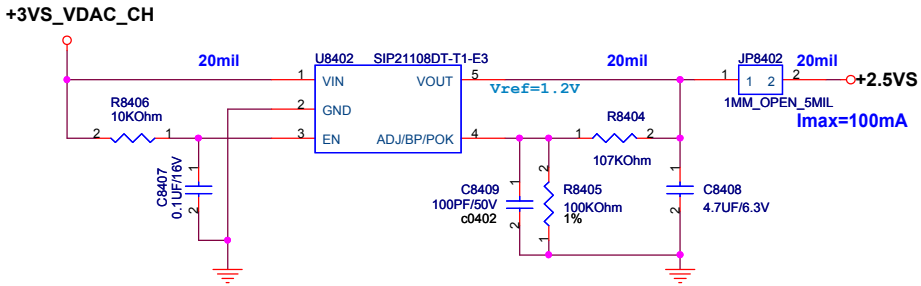
+1.5VS



+2.5VS



<Variant Name>

ASUS	Title : POWER_I/O_ +1.5VS_+2.5VS	
ASUSTeK COMPUTER INC. NB	Engineer: Johnny	
Size B	Project Name UX20	Rev 2.0
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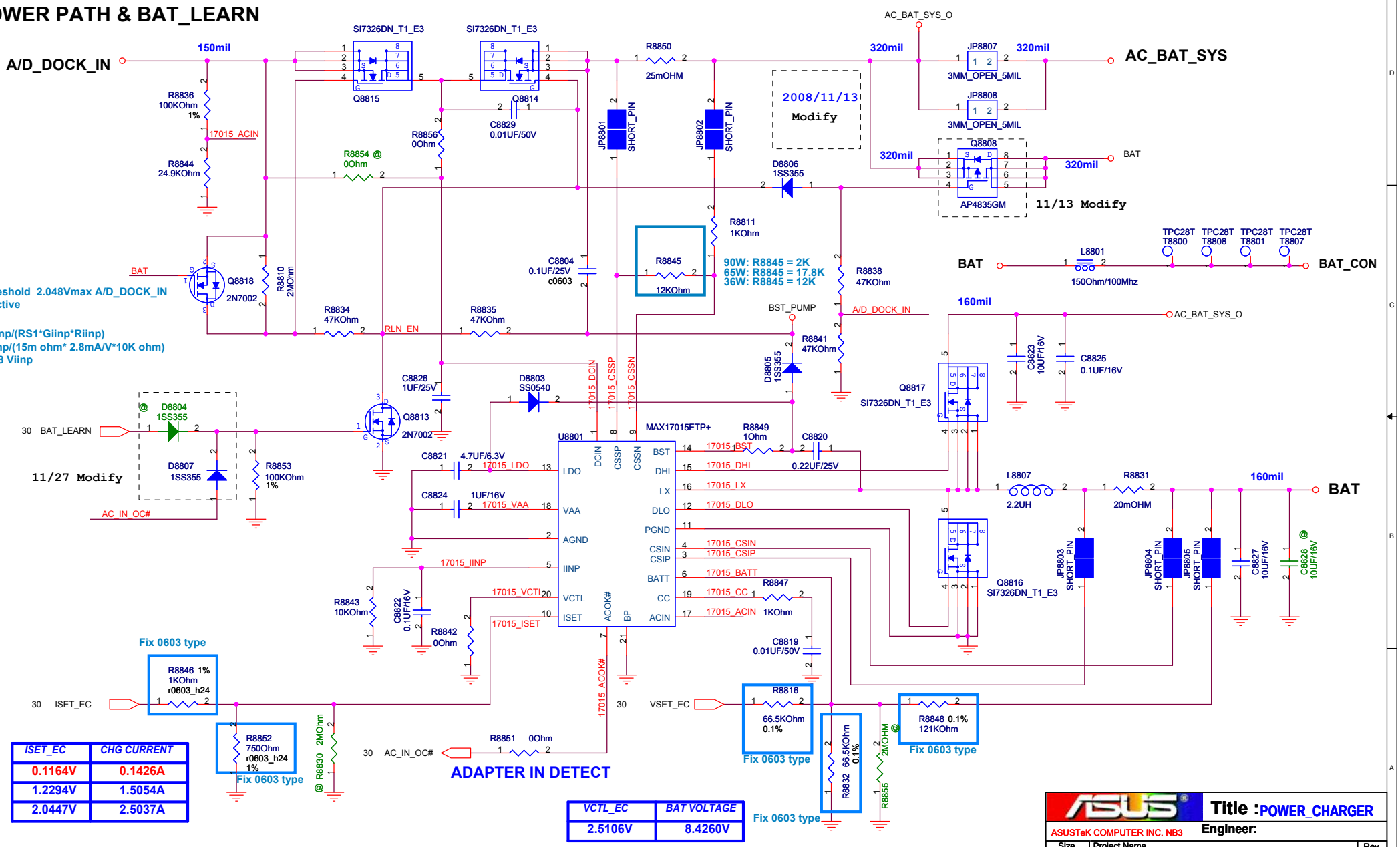
POWER PATH & BAT_LEARN



ISET_EC	CHG CURRENT
0.1164V	0.1426A
1.2294V	1.5054A
2.0447V	2.5037A

VCTL_EC	BAT VOLTAGE
2.5106V	8.4260V

ASUS

ASUSTeK COMPUTER INC. NB3

Title : POWER_CHARGER

Engineer:

Size	Project Name	Rev
B	UX20	2.0

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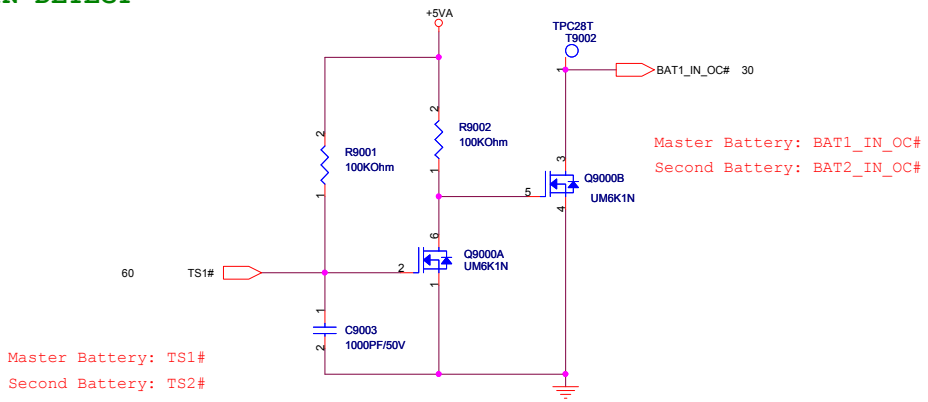
BATTERY IN DETECT



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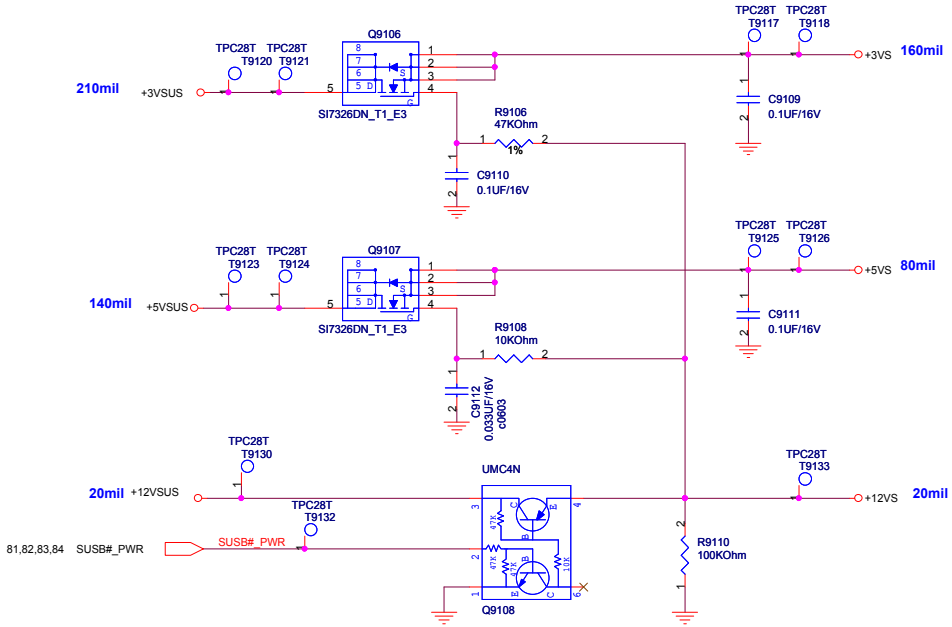
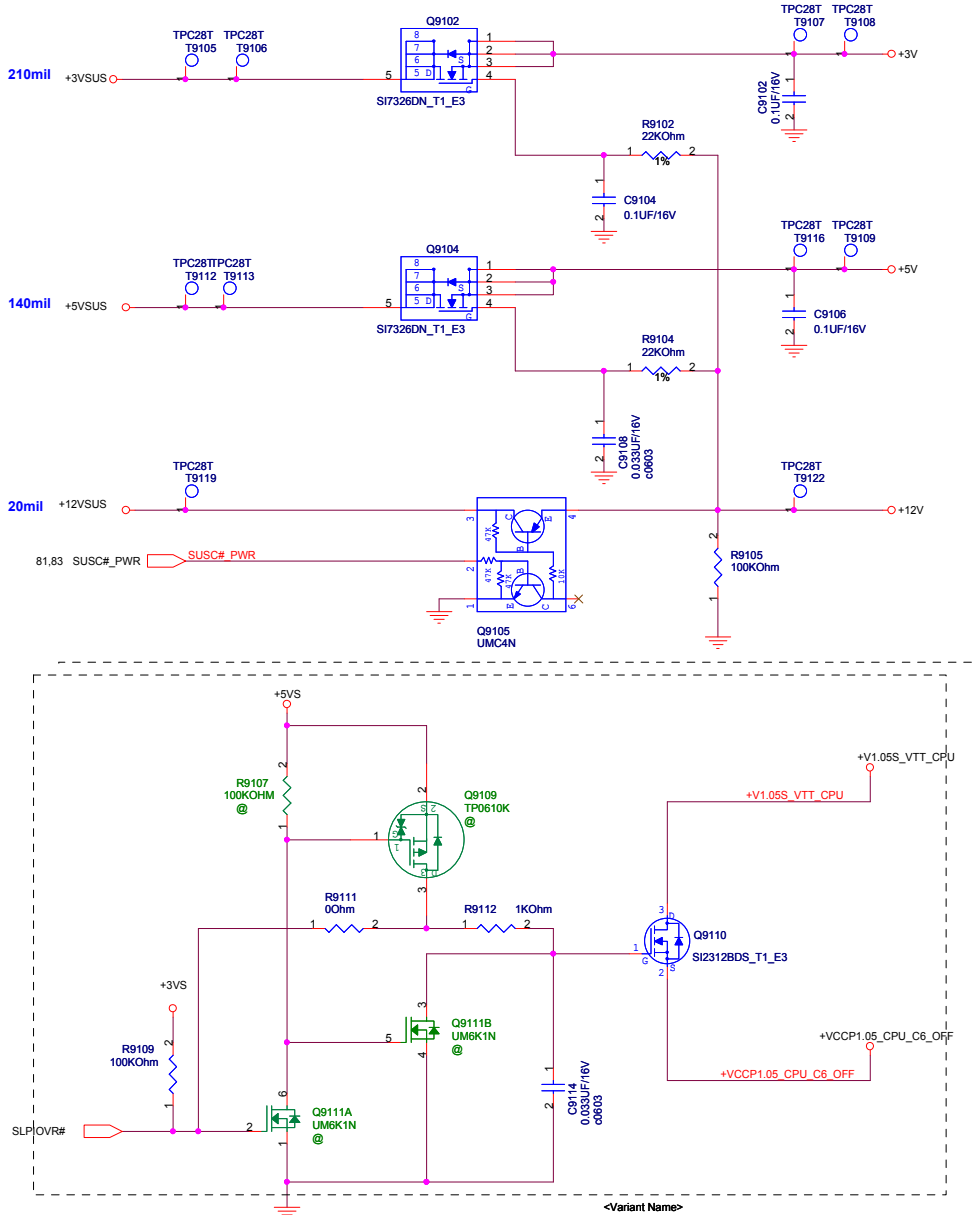
SUSB#_PWR POWER



SUSC#_PWR POWER



SLPIOVR# = 0 (C6) => SWITCH OFF

SLPIOVR# = 1 (NORMAN) => SWITCH ON

<Variant Name>

ASUS	Title : POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB	Engineer: Johnny	
Size: Custom	Project Name: UX20	Rev: 2.0
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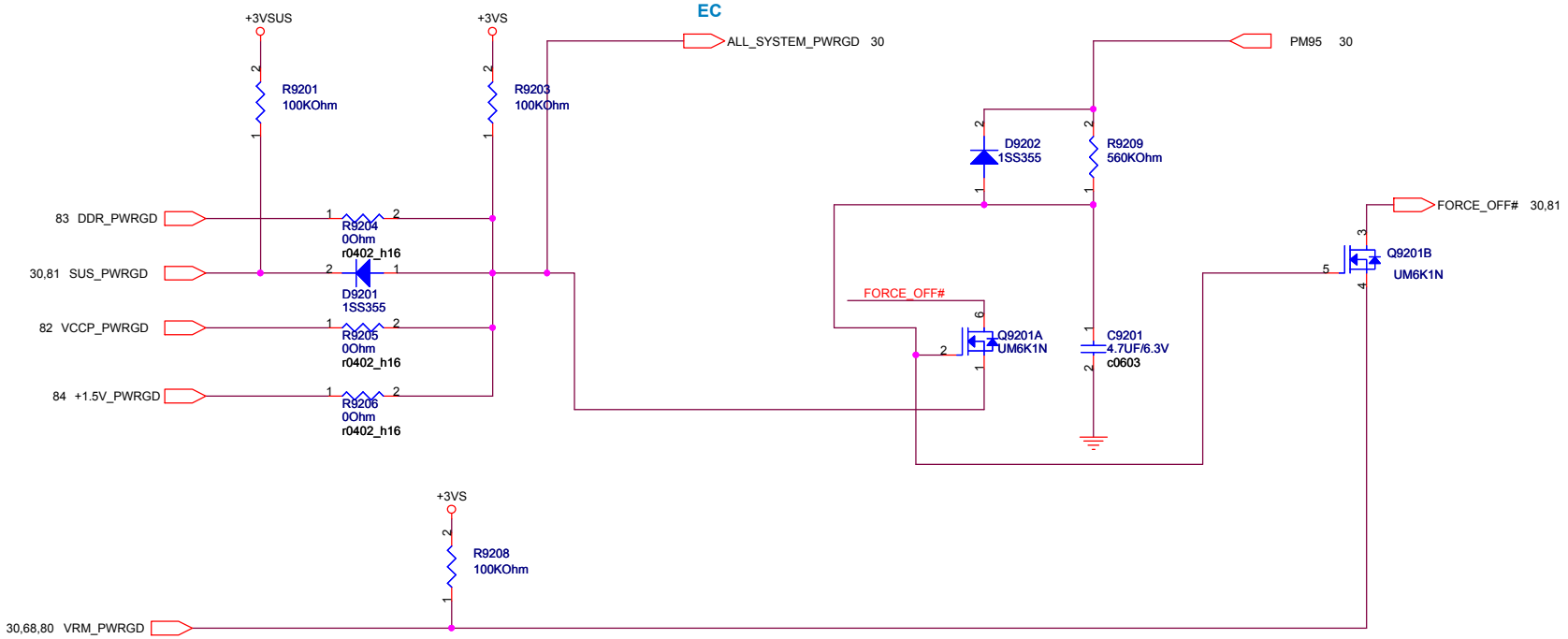
POWER GOOD DETECTER



<Variant Name>

ASUS	Title : POWER_PROTECT	
ASUSTeK COMPUTER INC. NB	Engineer: Johnny	
Size B	Project Name UX20	Rev 2.0
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AC_BAT_SYS	AC_BAT_SYS	80,81,82,83,88,95
BAT	BAT	88
+3VA	+3VA	12,30,36,42,57,81
+5VAO	+5VAO	81
+5VO	+5VO	81
+5VSUS	+5VSUS	14,31,36,56,81,82,83,84,91
+5V	+5V	14,36,45,52,57,91
+5VS	+5VS	14,30,31,36,46,50,51,56,57,80,91,95
+3VO	+3VO	31,81
+3VSUS	+3VSUS	14,33,81,91,92
+3V	+3V	13,14,33,42,44,45,53,57,61,91
+3VS	+3VS	4,7,12,13,14,29,30,33,36,45,46,50,51,53,57,66,67,68,80,91,92
+12VSUS	+12VSUS	81,91
+12V	+12V	36,42,91
+12VS	+12VS	45,91
+1.8VO	+1.8VO	83
+1.05VO	+1.05VO	82
+1.5VO	+1.5VO	84
+1.5VS	+1.5VS	5,10,12,13,14,53,57,84
+VCORE	+VCORE	5,80

<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Johnny

Size	Project Name	Rev
Custom	UX20	2.0

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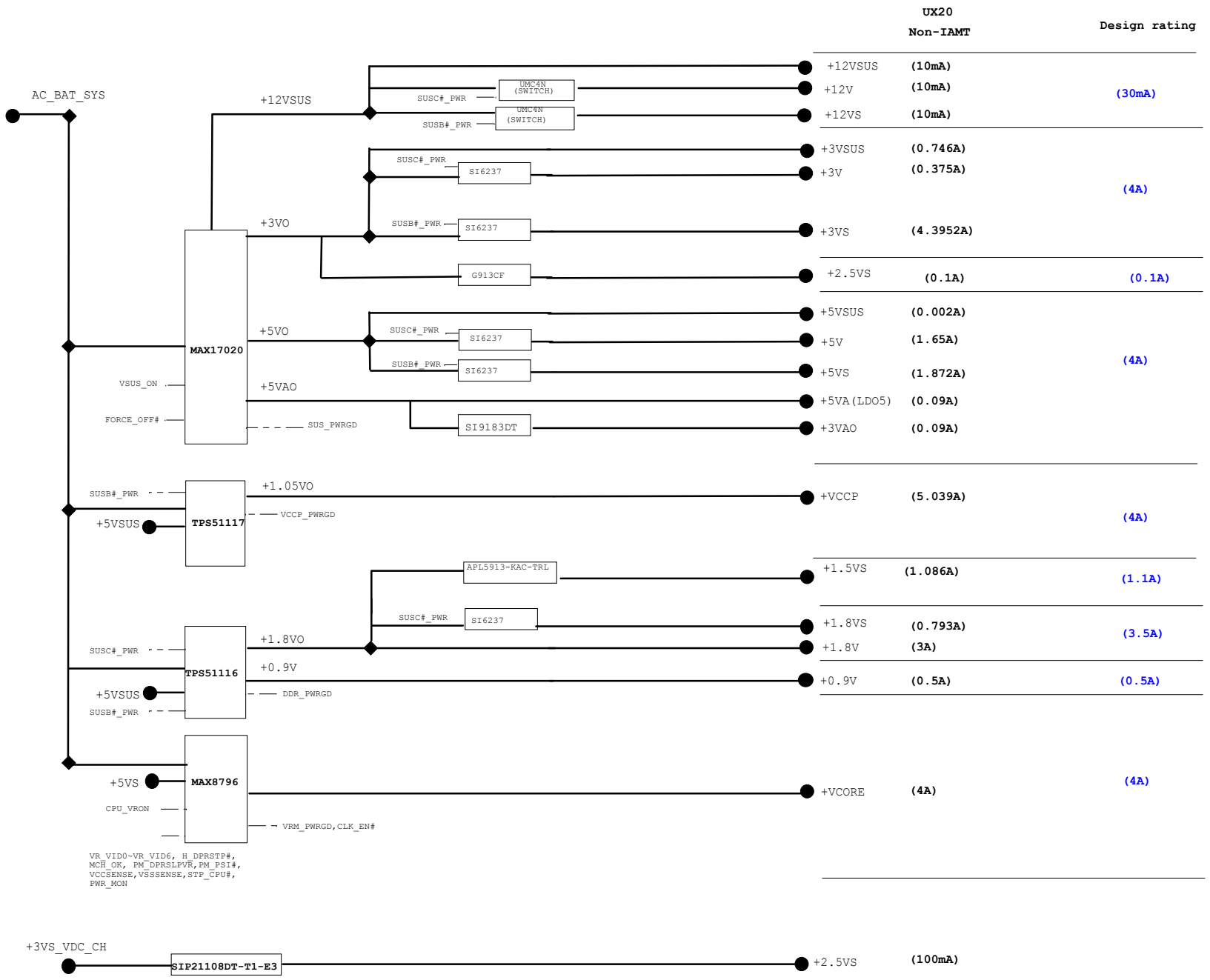

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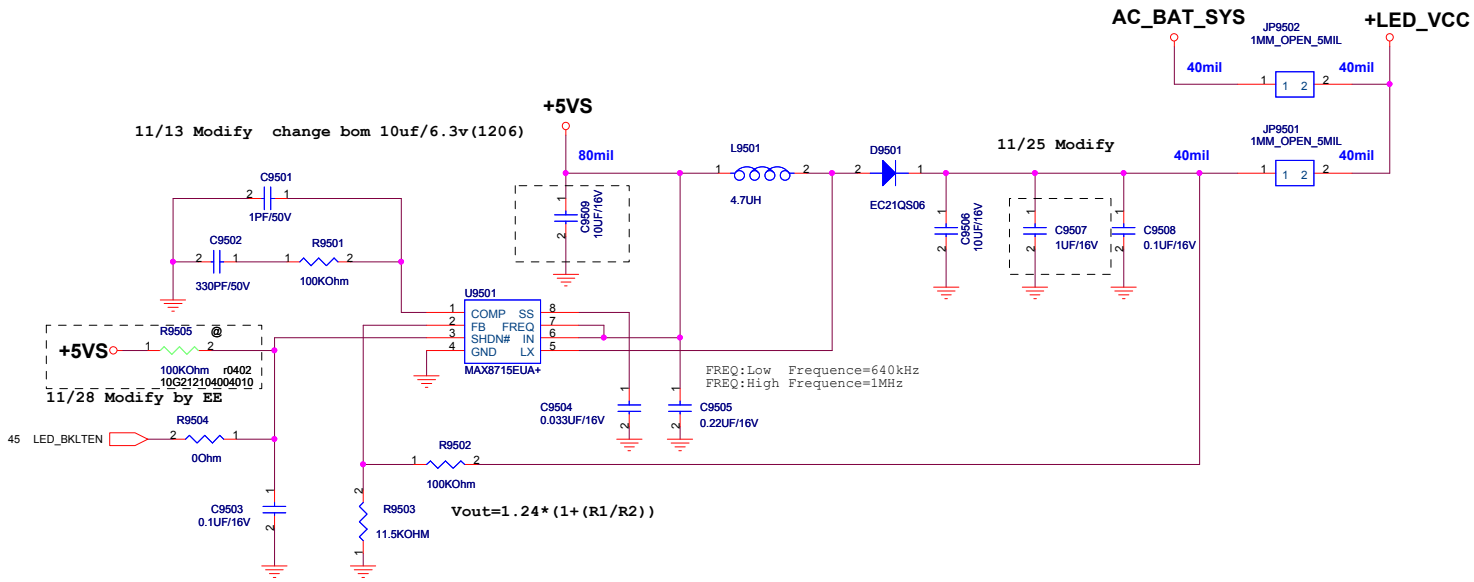

<Variant Name>

ASUS	Title : POWER_LED_VCC BOOST	
ASUSTeK COMPUTER INC. NB	Engineer: Johnny	
Size: Custom	Project Name: UX20	Rev: 2.0
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ASUS	Title : HISTORY		
<OrgName>	Engineer: Johnny		
Size: Custom	Project Name: UX20		Rev: 2.0
Date: Friday, December 05, 2008	Sheet 96 of 97		

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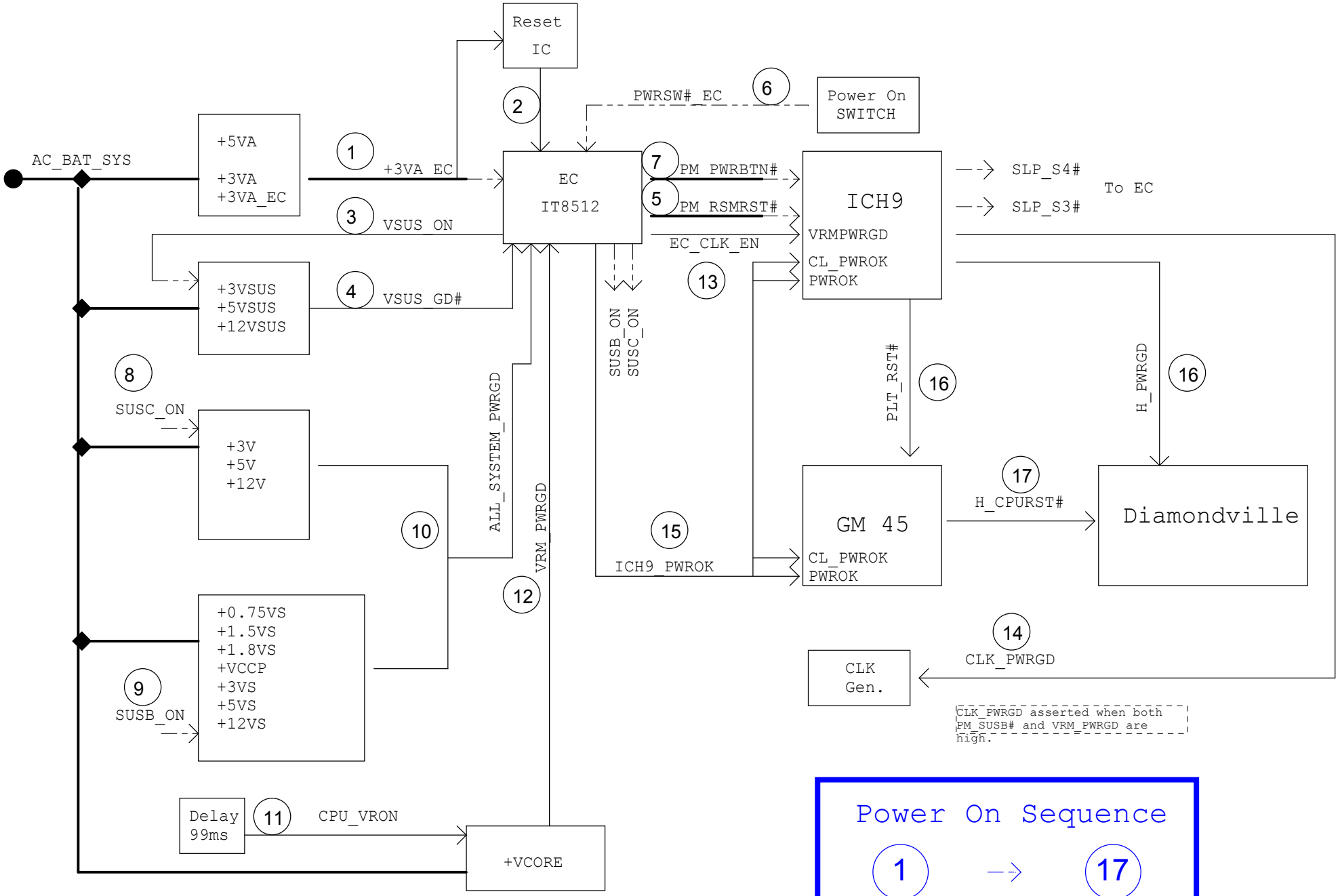

ASUS	Title : POWER SEQUENCE		
<OrgName>	Engineer: Johnny		
Size: Custom	Project Name: UX20		Rev: 2.0
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