ZR8 SYSTEM DIAGRAM

RAMP

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

```
SGN@---->Internal CLK GEN.
GN@  ---->External CLK GEN.
IV@  -----> iGPU
SW@ -----> dGPU
SP@  -----> iGPU & dGPU notice
SPE@  ----->Only for dGPU notice
SIDE@ ----> Side port
```

DDR3-SODIMM1 P5
DDR3-SODIMM2 P6
DDR3 channel A
DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)45W/35W
P2 ~ 4

CPU THERMAL SENSOR P4

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

CLOCK GEN From SB P11

HT3

PCI-E

NORTH BRIDGE
RS880
A12
21mm X 21mm, 528pin BGA
P7 ~ 10

PCI-Express 16X

ATI Madison LP 128-bit M2 Pkg
29mm X 29mm
P16 ~ 20

HDMI → HDMI P25
CRT → MUXs (S.G) P24 → CRT P24
LVDS → MUXs (S.G) P24 → LVDS P24

DDR3 800MHz
VRAM
64MX16X4,64 bit
64MX16X8,128 bit
P22,23

SIDE port P7

LAN
Atheros
PCIE-LAN
AR8151
(10/100/1000)
P26

Mini PCI-E Card
(Wireless LAN)
P27

RJ45 P26

CRT
LVDS

ALINK X4

SOUTH BRIDGE
SB820
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
P11 ~ 14

SATA - HDD1 P28 — SATA0 150MB
SATA - ODD P28 — SATA1 150MB

BT P31 — USB1.1

USB2.0

USB2.0 Ports X1 P31
Webcam P24
CardReader AU6433/AU6437 P30

USB BOARD
USB2.0 Ports x 3
P31

LPC
Azalia

Winbond KBC
NPCE781L
P34

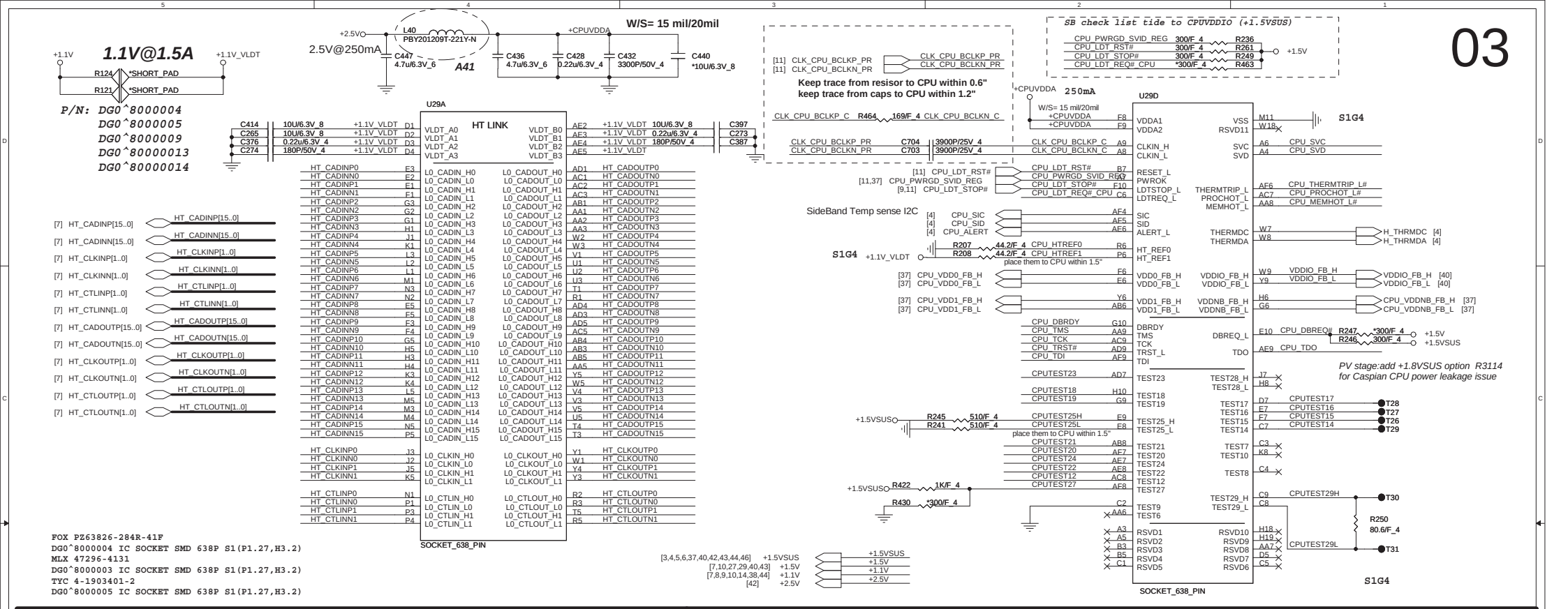
Codec
RTL ALC271X
P29

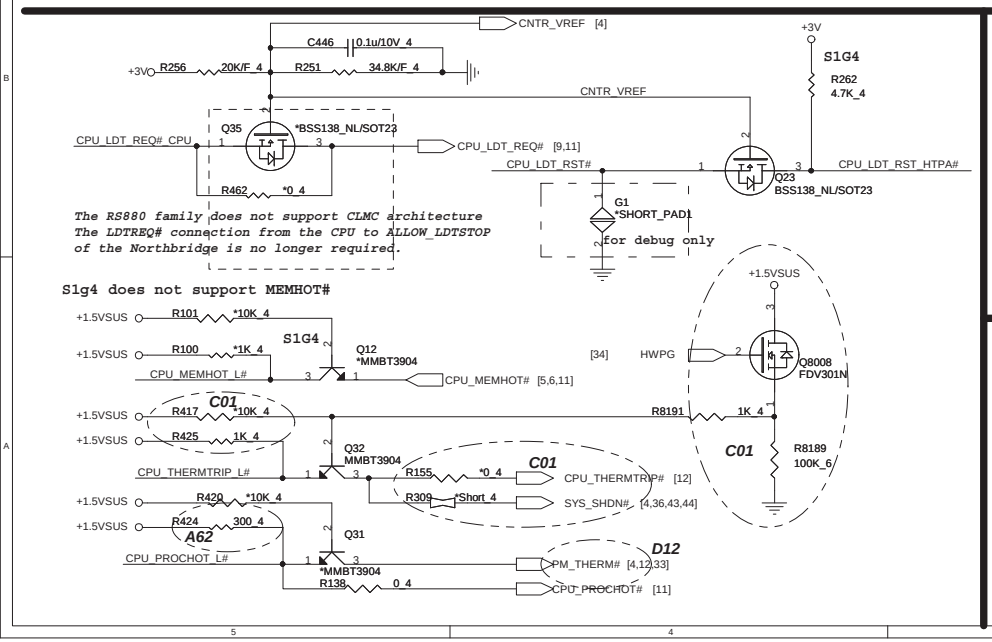
Keyboard P33
Touch Pad P31
FAN P33
SPI P34
Digital MIC P24
AUDIO CONN (Phone/ MIC) P29
Speaker P29

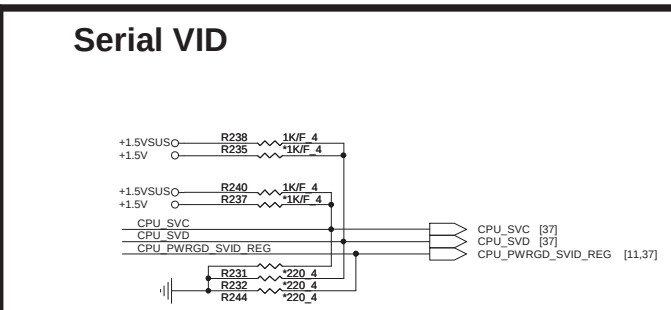
Charger (ISL88731A) P35
DC/DC (3VPCU / 5VPCU) RT8206B P36
CPU_VCORE (VCORE) ISL6265A P37
DC/DC (+1.1V_S5) UP6111AQD P38
DC/DC (NB_CORE) UP6111AQD P39
DC/DC (+1.5VSUS) RT8207A P40
DC/DC (GPU_CORE) MAX8792ETD+T P41
DC/DC (+1.8V/+1V/+2.5V) HPA00835RTER / RT9018A / RT9025-25PSP P42
DC/DC (CPU_VDDR) RT9025-25PSP P43

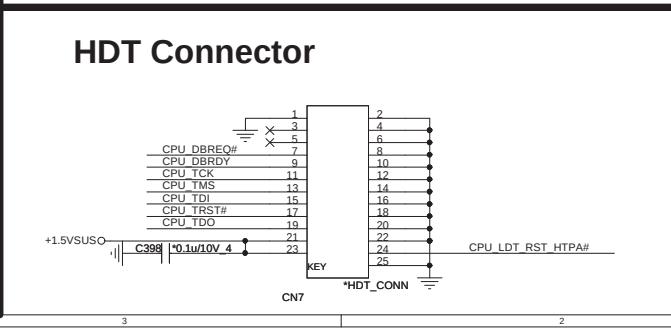
PROJECT : ZR8
Quanta Computer Inc.

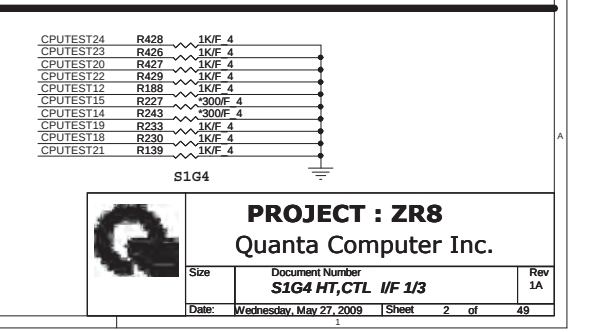
Size	Document Number	Rev
	Block Diagram	1A
Date: Wednesday, May 27, 2009	Sheet 1 of 49	











Processor Memory Interface

04

VDDR=>1.75A

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

D01

PLACE THEM CLOSE TO CPU WITHIN 1"

U29B — MEM:CMD/CTRL/CLK

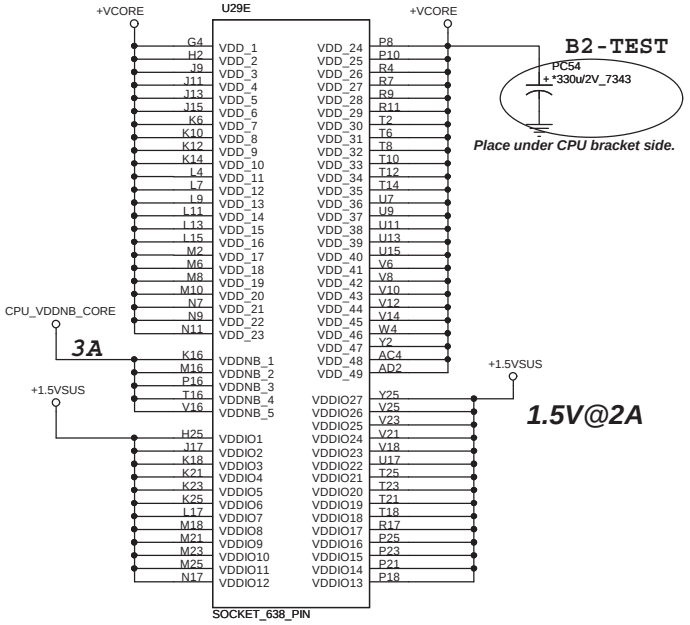
U29C — MEM:DATA

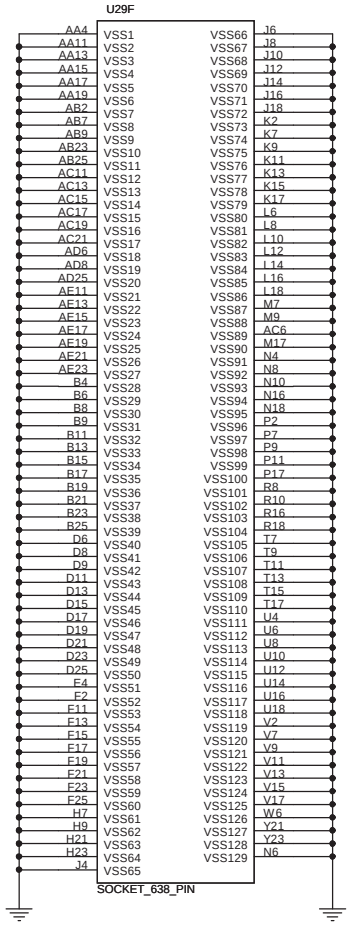
Place close to socket

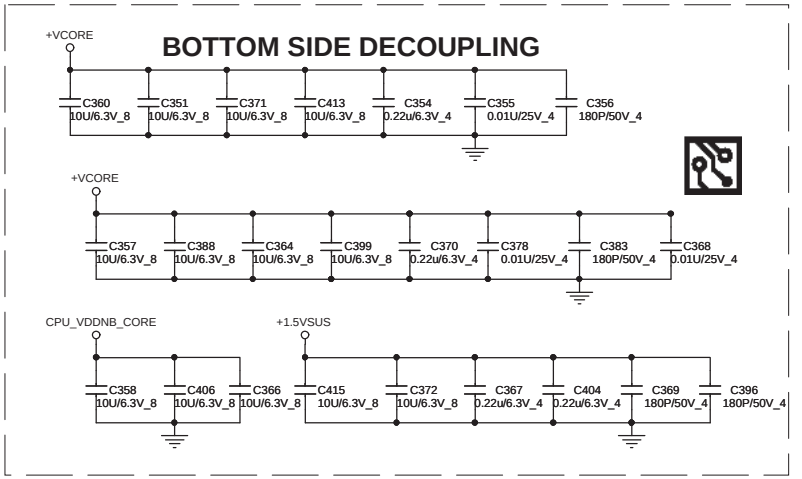
Reserved for AMD suggest

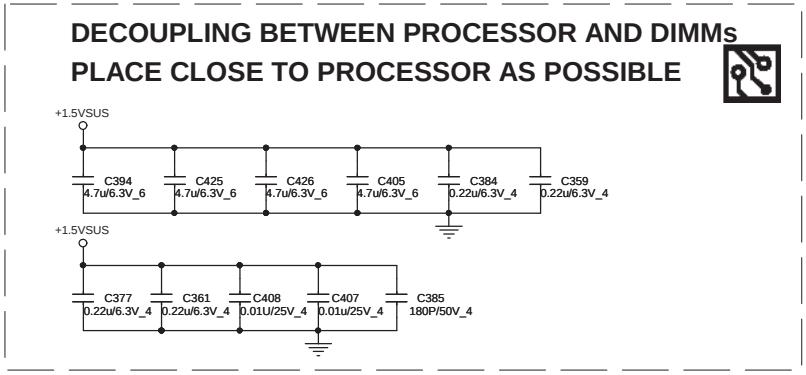
SOCKET_638_PIN

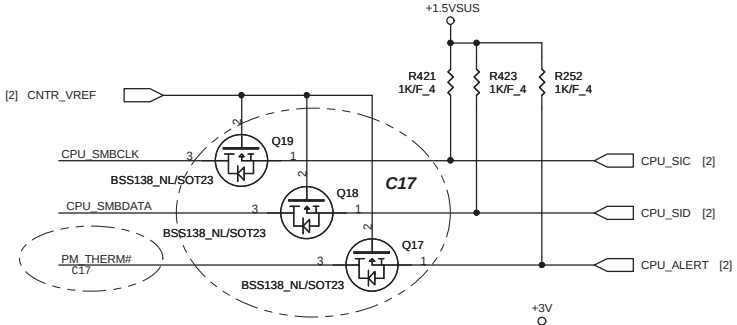
PROJECT : ZR8	
Quanta Computer Inc.	
Size	Document Number: S1G4 DDRIII MEMORY I/F 2/3 — Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 3 of 49



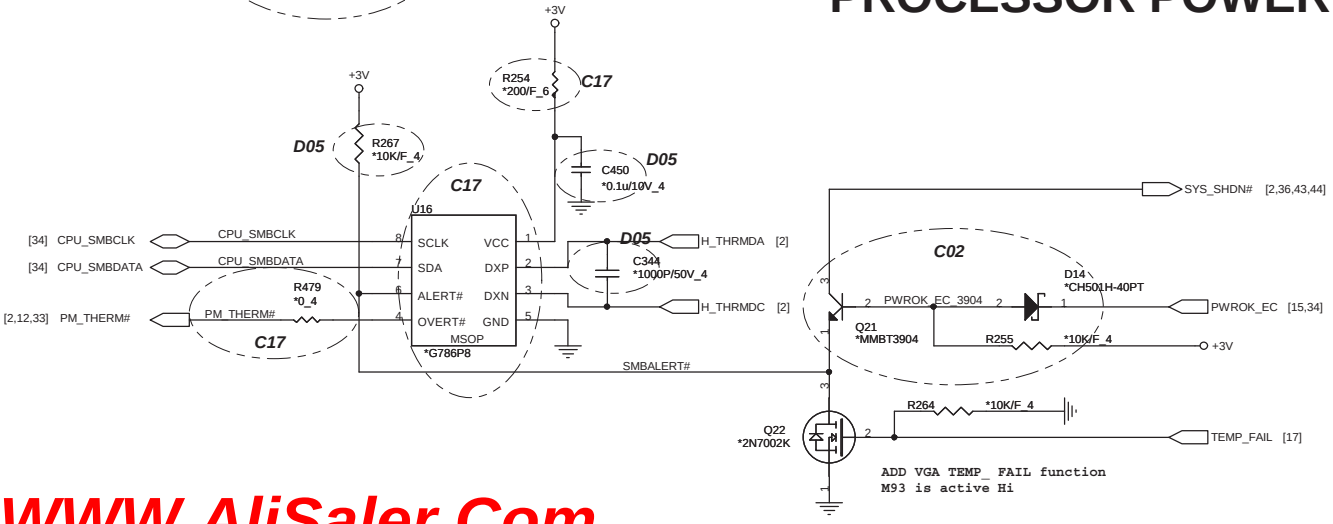




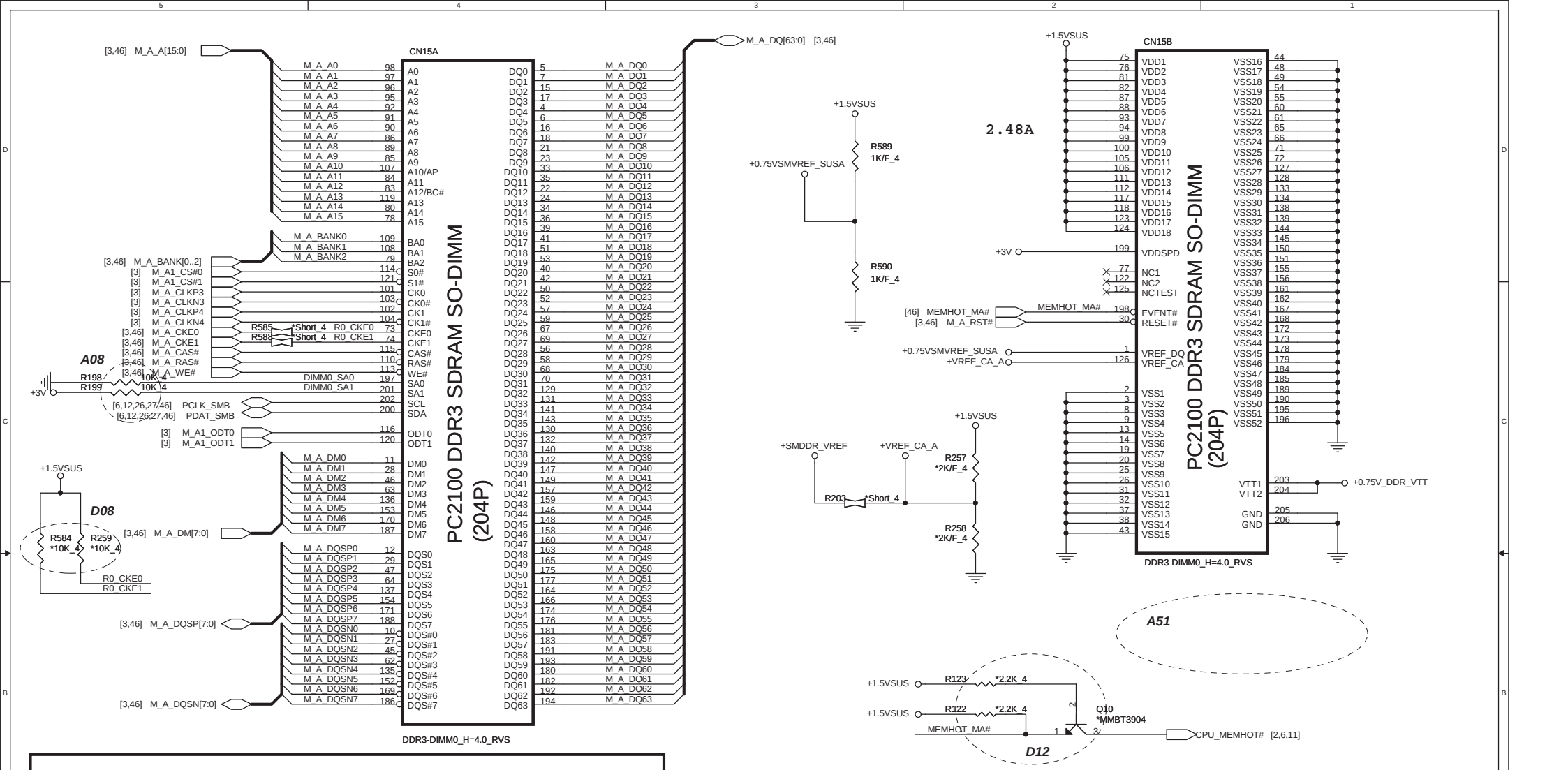




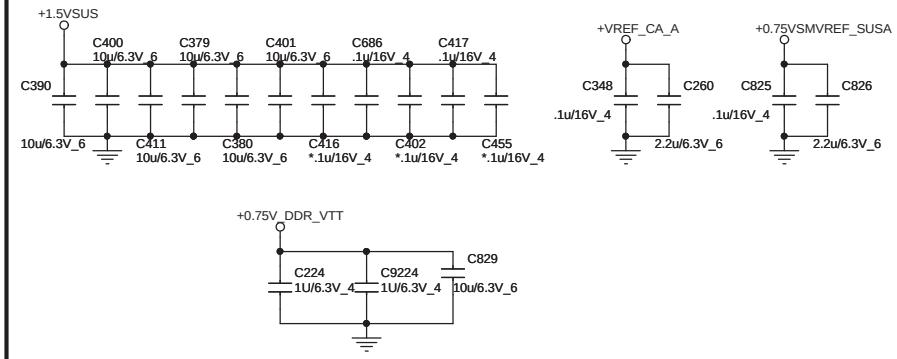
PROCESSOR POWER AND GROUND



PROJECT : ZR8	
Quanta Computer Inc.	
Size	Document Number: S1G4 PWR & GND 3/3 — Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 4 of 49



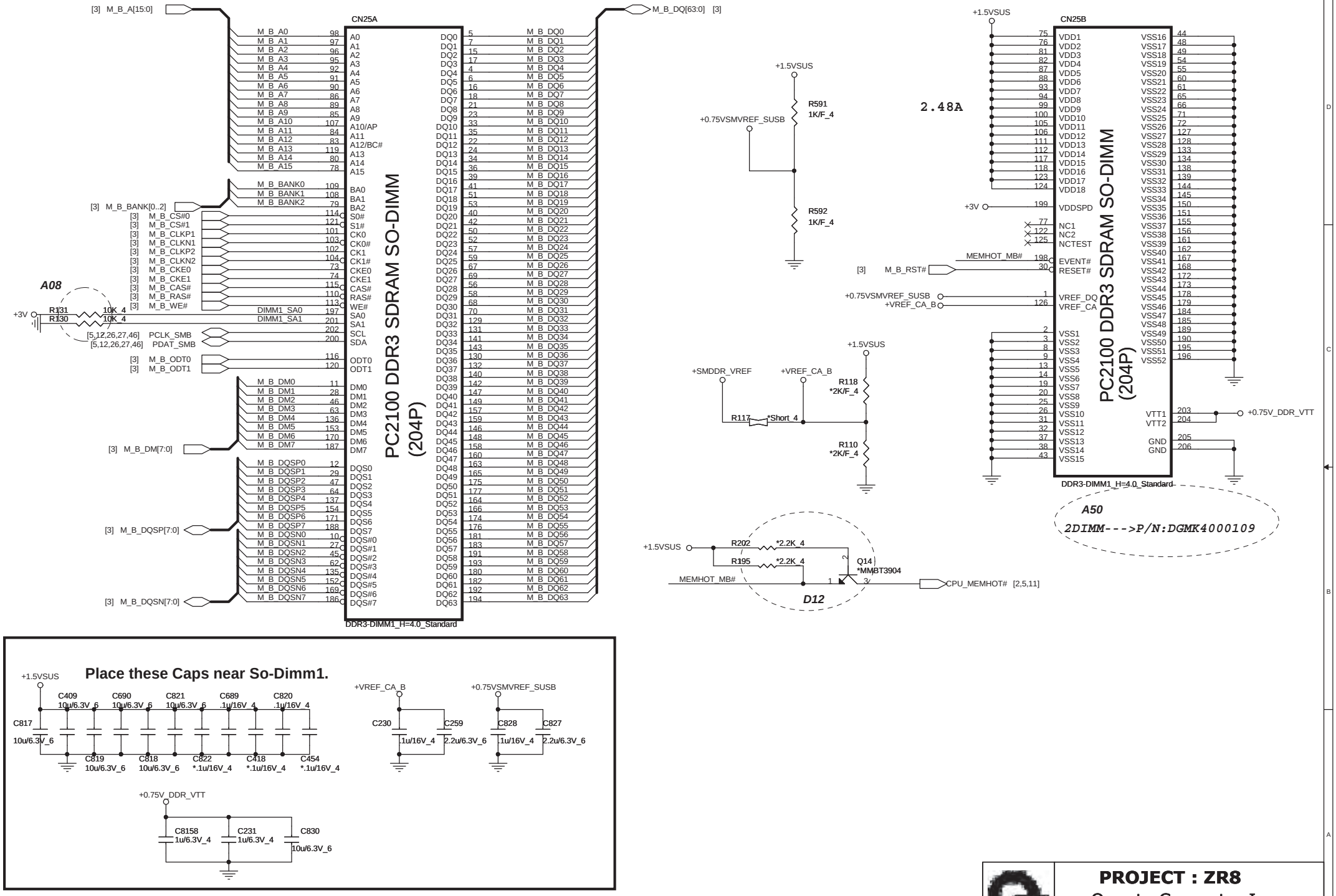
Place these Caps near So-Dimm0.



PROJECT : ZR8

Quanta Computer Inc.

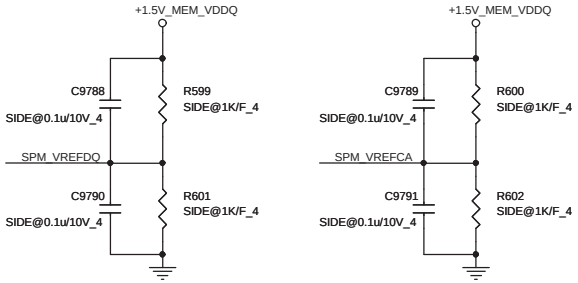
Size	Document Number	Rev
	DDR2 SODIMMS: A/B CHANNEL	1A
Date: Wednesday, May 27, 2009	Sheet 5 of 49	

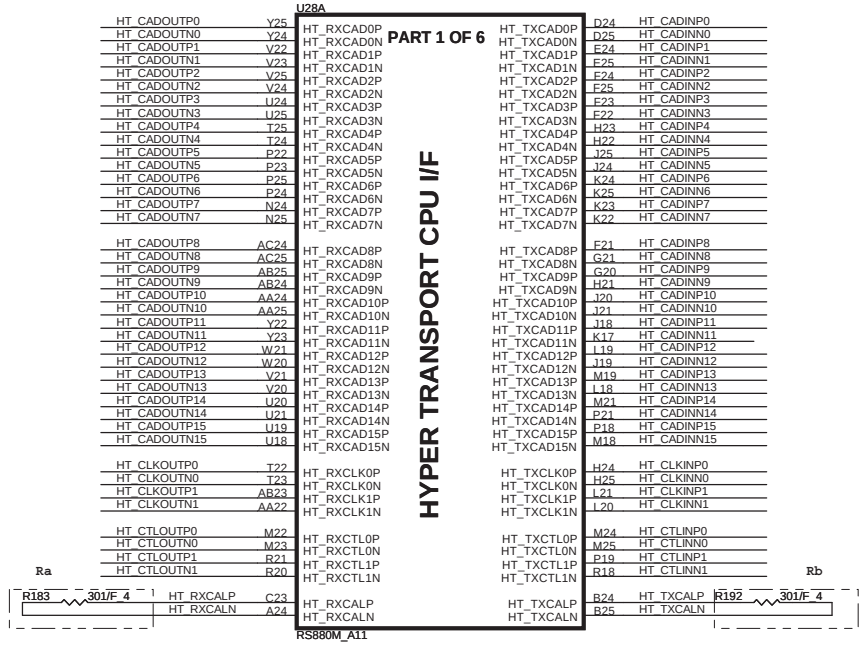


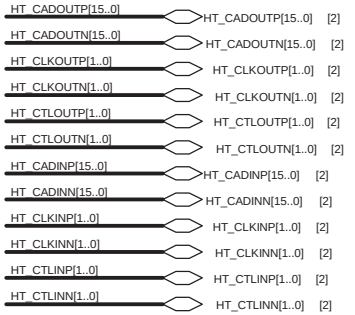
PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: DDR2 SODIMMS: A/B CHANNEL	Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 6 of 49	

SIDE PORT

11/4

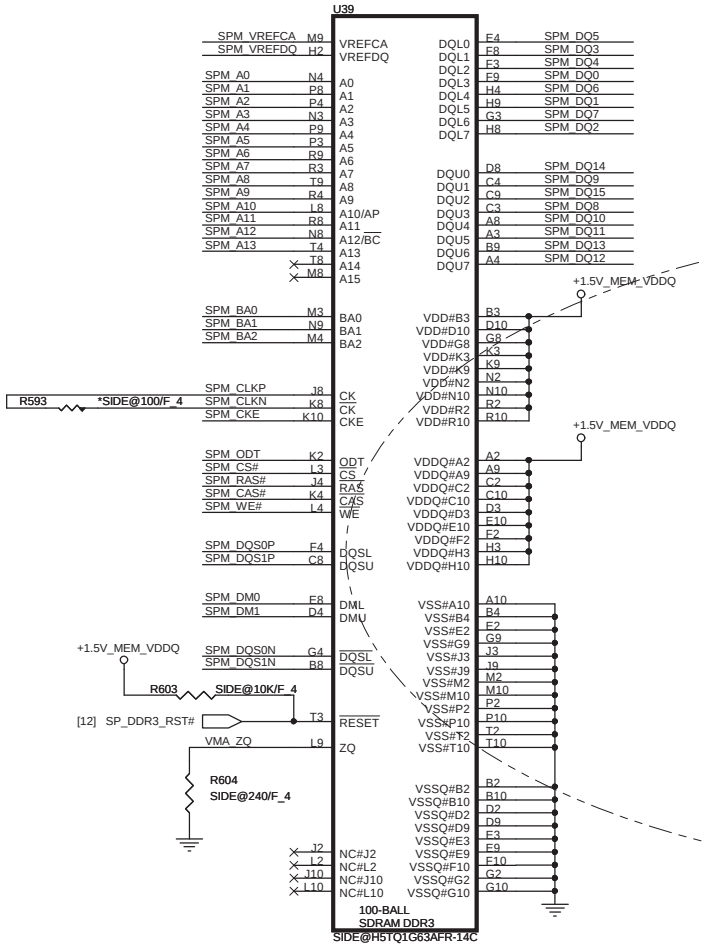






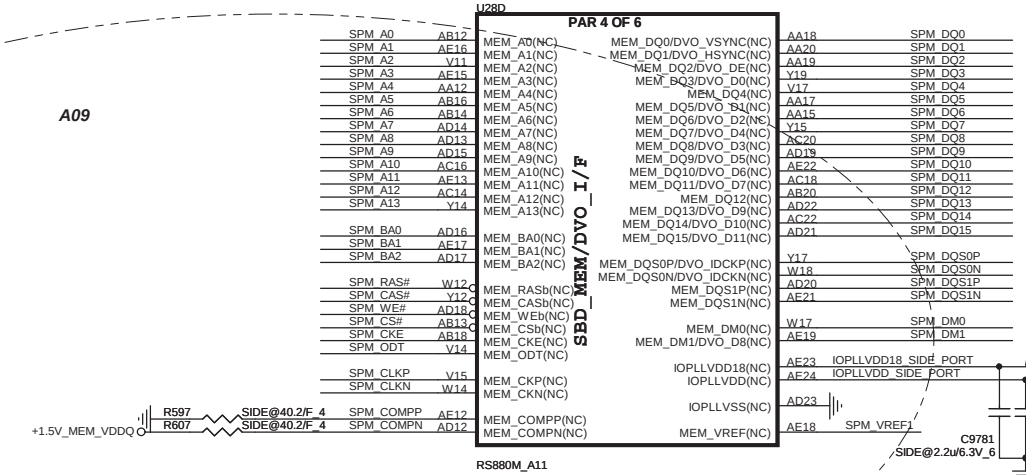
signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

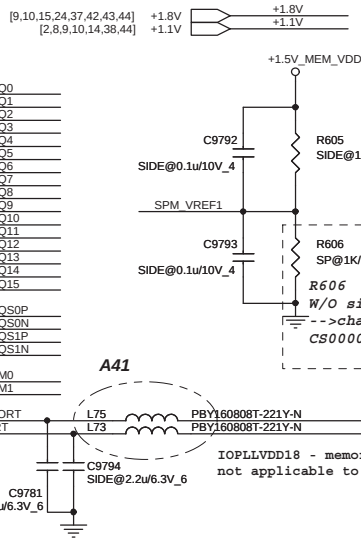
RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

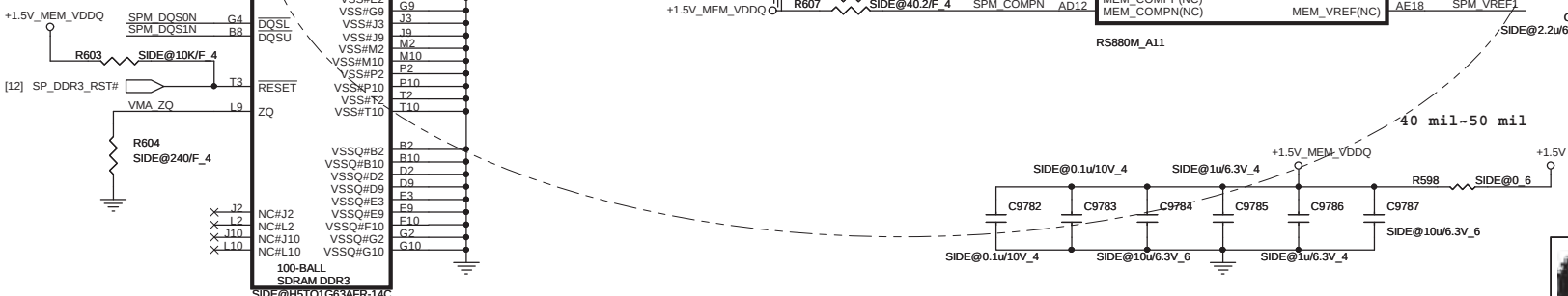


This block is for UMA only , Discrete can remove all component

A09



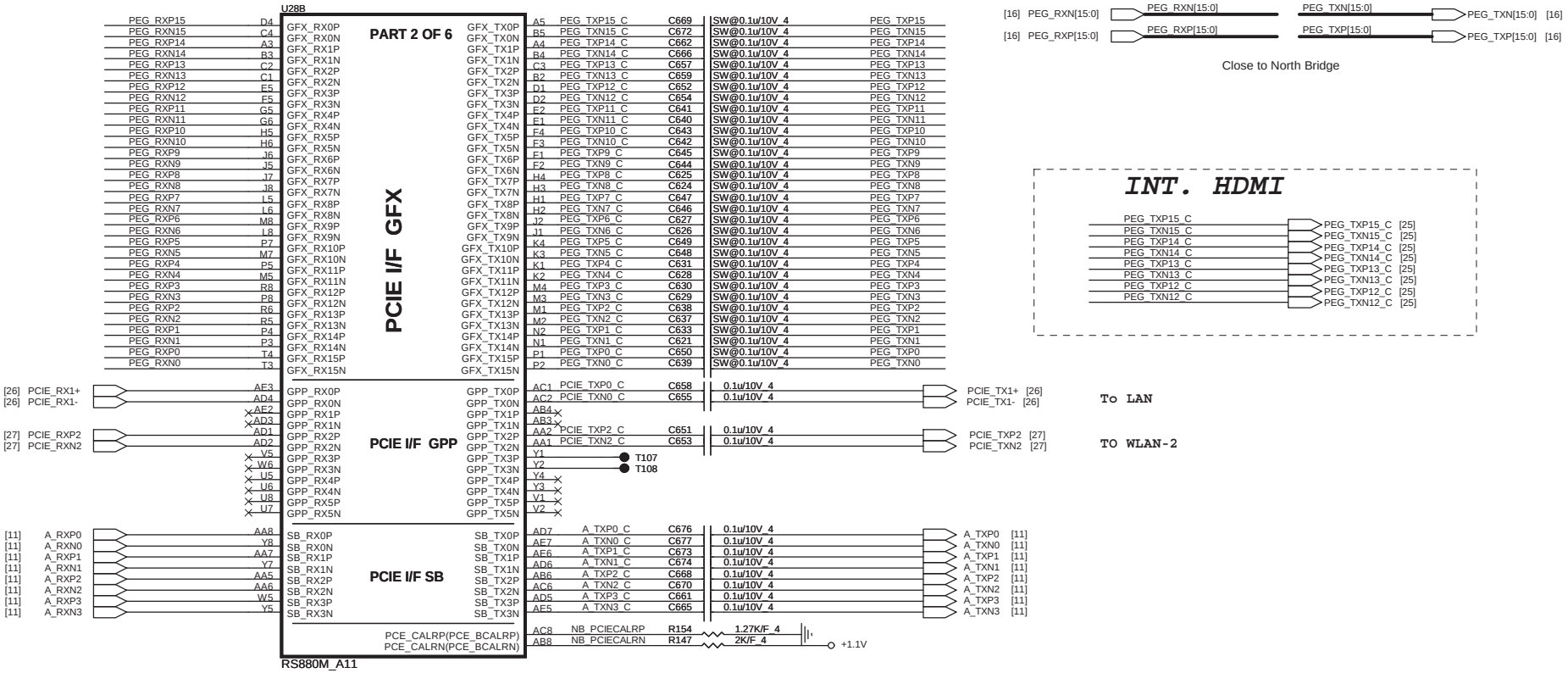




PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/5	1A
Date: Wednesday, May 27, 2009	Sheet 7 of 49	

08



Close to North Bridge

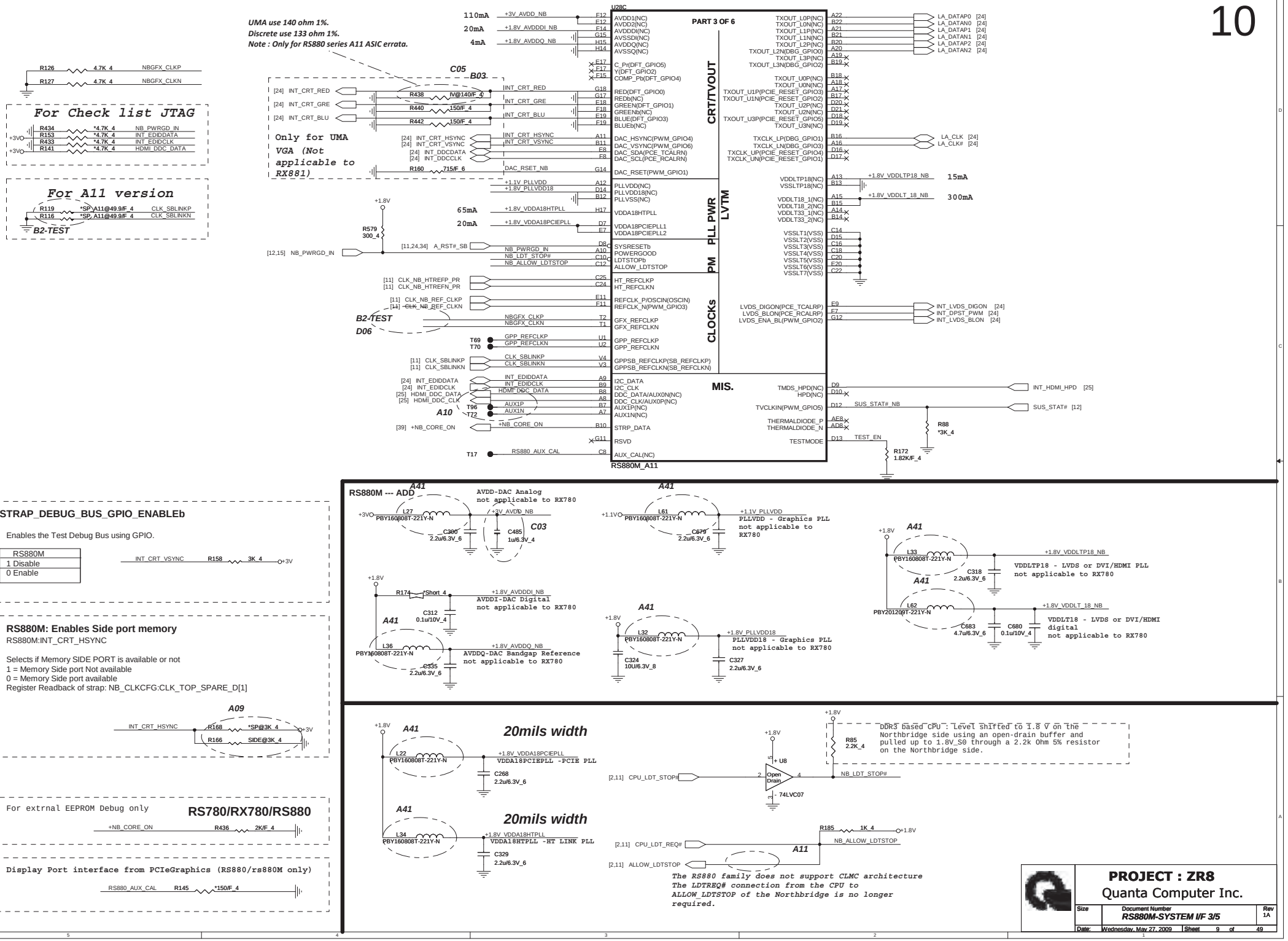
To LAN

TO WLAN-2

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : ZR8 Quanta Computer Inc.		
Size	Document Number RS880M-PCIE I/F 2/5	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 8 of 49	


UMA use 140 ohm 1%.
Discrete use 133 ohm 1%.
Note : Only for RS880 series A11 ASIC errata.
U28C
PART 3 OF 6
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKs
MIS.
RS880M_A11
For Check list JTAG
For A11 version
B2-TEST
Only for UMA
VGA (Not
applicable to
RX881)
C05
B03
D06
A10
A09
A41
C03
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.
RS880M
1 Disable
0 Enable
RS880M: Enables Side port memory
RS880M:INT_CRT_HSYNC
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
For extrnal EEPROM Debug only
RS780/RX780/RS880
Display Port interface from PCIeGraphics (RS880/rs880M only)
RS880M --- ADD
AVDD-DAC Analog
not applicable to RX780
PLLVDD - Graphics PLL
not applicable to
RX780
AVDDI-DAC Digital
not applicable to RX780
AVDDQ-DAC Bandgap Reference
not applicable to RX780
PLLVDD18 - Graphics PLL
not applicable to RX780
VDDLTP18 - LVDS or DVI/HDMI PLL
not applicable to RX780
VDDLT18 - LVDS or DVI/HDMI
digital
not applicable to RX780
20mils width
VDDA18PCIEPLL -PCIE PLL
VDDA18HTPLL -HT LINK PLL
DDR3 based CPU : Level shifted to 1.8 V on the
Northbridge side using an open-drain buffer and
pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor
on the Northbridge side.
The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to
ALLOW_LDTSTOP of the Northbridge is no longer
required.
PROJECT : ZR8
Quanta Computer Inc.
Size
Document Number
RS880M-SYSTEM I/F 3/5
Rev
1A
Date: Wednesday, May 27, 2009
Sheet 9 of 49

U28F

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC

+1.1V 2A for RS880M
+1.1V 1.3A for RX881

+1.1V

0.6A L31 *Short_8 → +1.1V_VDDHT

C317 4.7u/6.3V_6 | C321 0.1u/10V_4 | C322 0.1u/10V_4 | C323 0.1u/10V_4

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7

J17 K16 L16 M16 P16 R16 T16

0.7A L37 *Short_8 → +1.1V_VDDHTRX

C362 4.7u/6.3V_6 | C338 0.1u/10V_4 | C340 0.1u/10V_4 | C334 0.1u/10V_4

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7

H18 G19 F20 E21 D22 B23 A23

+1.1V 2A for RS880M
+1.2V 0.4A for Rx881

+1.1V — L35 *Short_8 — **2A** → +1.1V_VDDHTTX

B2-TEST

C333 4.7u/6.3V_6 | C331 0.1u/10V_4 | C337 0.1u/10V_4 | C332 0.1u/10V_4 | C341 0.1u/10V_4

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13

AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

+1.8V 1A for RS780M+SB700
+1.8V 1A for RX881

A41

+1.8V — L24 PBY201209T-221Y-N — **0.7A** → +1.8V_VDDA18PCIE

C299 4.7u/6.3V_6 | C297 4.7u/6.3V_6 | C292 0.1u/10V_4 | C295 0.1u/10V_4 | C287 0.1u/10V_4 | C301 0.1u/10V_4

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15

J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

+1.8V — R136 *Short_6 — **25mA** → +1.8V_VDDG18_NB

VDD18-RS880 I/O Transform

C286 1U/10V_4

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC)

F9 G9 AE11 AD11

+1.8V — R171 SIDE@0_6 — **25mA** → +1.8V_VDD18_MEM

A09

C835 SP@1U/10V_4

C835
W/O side port
-->stuff 0 Ohm
CS00002JB38

U28E

PART 5/6

POWER

RS880M_A11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17

A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22

K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC)

AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC)

H11 H12

+1.1V_VDD_PCIE — **2.5A** — VDDPCIE - PCIE-E Main power

C243 0.1u/10V_4 | C291 0.1u/10V_4 | C293 1U/10V_4 | C294 1U/10V_4 | C290 4.7u/6.3V_6

R115 *Short_8 → +1.1V

0.95~1.1V 10A

VDDC - Core Logic power

C315 0.1u/10V_4 | C311 0.1u/10V_4 | C310 0.1u/10V_4 | C307 0.1u/10V_4 | C314 10U/6.3V_8 → NB_CORE

C316 0.1u/10V_4 | C308 0.1u/10V_4 | C306 0.1u/10V_4 | C305 10U/6.3V_8

A09

C831
W/O side port
-->stuff 0 Ohm
CS00002JB38

+1.5V_VDD_MEM

SIDE@0.1u/10V_4 | C832 | C833 | SIDE@0.1u/10V_4 | C831 | C836 | L74 SIDE@0_8 → +1.5V | C834 SIDE@4.7u/6.3V_6

SIDE@0.1u/10V_4 | SP@0.1u/10V_4

+3V_VDDG33 — R169 *Short_4 — **60mA** → +3V

C302 0.1u/10V_4 | C303 0.1u/10V_4

VDD33 - 3.3V I/O
Not applicable to RX780

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

+1.1V → +1.1V [2,7,8,9,14,38,44]
+1.8V → +1.8V [7,9,15,24,37,42,43,44]
NB_CORE → NB_CORE [39,44]

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-POWER5/5	1A
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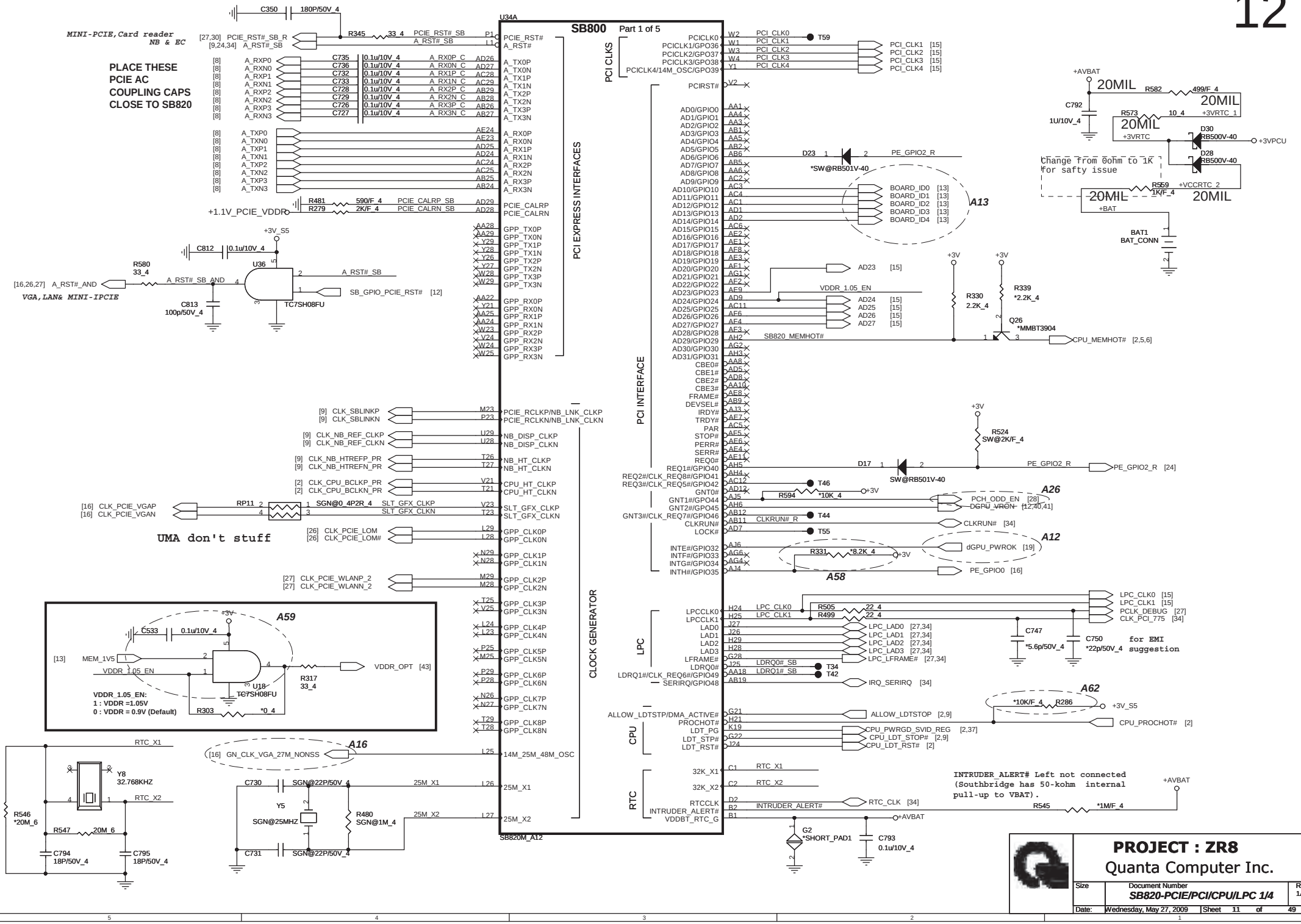

	PROJECT : ZR8	
	Quanta Computer Inc.	
Size	Document Number: *SB820-PCIE/PCI/CPU/LPC 1/4*	Rev: 1A
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NC only ,Can't be install

+3V_S5
R352 *2.2K_4 SB_TEST0
R350 *2.2K_4 SB_TEST1
R347 *2.2K_4 SB_TEST2

+3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R288 2.2K_4 PCLK_SMB
R287 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3V_S5
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R348 10K_4 SB_SMBCLK1
R346 10K_4 SB_SMBDATA1

+3V_S5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R290 10K_4 SB_SCLK2
R283 10K_4 SB_SDATA2

+3V
R338 4.7K_4 SUS_STAT#

B2-TEST
dGPU_VRON
2ms
MXM_PWR_EN
[19] MXM_PWREN
+3V
R307 SW@4.7K_4
D19 SW@RB501V-40
MXM_PWR_EN
C538 SW@0.1u/10V_4
[11,40,41] DGPU_VRON
D18 *SW@RB501V-40
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)
A14

[11,13,14,15,24,26,31,32,36,44] +3V_S5 +3V_S5
[2,4,5,6,9,10,11,13,14,15,19,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46] +3V +3V

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U34D
SB800
Part 4 of 5
SB820M_A12

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

[34] SUSB#
[34] SUSC#
[34] DNBSWON#
[15] SB_PWRGD_IN
[9] SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
[34] SIO_A20GATE
[34] SIO_RCIN#
T94 LANLINK_STATE#
[34] SIO_EXT_SMI#
[34] SIO_EXT_SCI#
T95 SYS_RST#
[26] PCIE_WAKE#
PCIE_WAKE#
T58 IR_RX1
[2] CPU_THERMTRIP#
[9,15] NB_PWRGD_IN
[34] ICH_RSMRST#
SB_THERMTRIP#

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
GPIO

[11] SB_GPIO_PCIE_RST#
[26] CLK_PCIE_LAN_REQ#
MXM_PWR_EN
T37 SB_GPIO59
[29] SPKR
[5,6,26,27,46] PCLK_SMB
[5,6,26,27,46] PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
[27] CLK_PCIE_2_REQ#
[17] VGA_REQ#
R306 *0_4 VGA_REQ#_GPIO61
C04
[7] SP_DDR3_RST#
T41

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC

[31] OC_7#
[31] OC_6#
[2,4,33] PM_THERM#
[31] OC_4#
R149 *Short_4
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

USBCLK/14M_25M_48M_OSC
USB_RCOMP
G19 USB_RCOMP_SB R293 11.8K/F_6
USB 1.1 USB MISC
USB_FSD1P/GPIO186
USB_FSD1N
USB_FSD0P/GPIO185
USB_FSD0N
USB_FDS12P
USB_FSD12N
T106
T47
T49

USB_HSD13P
USB_HSD13N
USB_HSD12P
USB_HSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0

USBP13+ [31] USBP13- [31] USB board
USBP12+ [31] USBP12- [31] USB board
USBP10+ [30] USBP10- [30] USB card reader
USBP9+ [31] USBP9- [31] BLUETOOTH
USBP8+ [31] USBP8- [31] USB board
USBP7+ [27] USBP7- [27] WLAN MINI CARD
T61
T105
USBP1+ [24] USBP1- [24] USB CAMERA
USBP0+ [31] USBP0- [31] On board USB connect
B2-TEST

HD audio interface is +3VS5 voltage
[15] ACZ_SDOUT
R555 *10K/F_4 ACZ_BCLK
ACZ_SDOUT
R337 *10K/F_4 ACZ_SDIN0
R336 *10K/F_4 ACZ_SDIN1
R571 *10K/F_4 ACZ_SDIN2
R327 *10K/F_4 ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

SCL2/GPIO193
SDA2/GPIO194
SCL3_LV/GPIO195
SDA3_LV/GPIO196
SB_SCLK2
SB_SDATA2
SB_GPIO195
SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197
EC_PWM1/EC_TIMER1/GPIO198
EC_PWM2/EC_TIMER2/GPIO199
EC_PWM3/EC_TIMER3/GPIO200
GPIO199 [15]
GPIO200 [15]

KSI_0/GPIO201
KSI_1/GPIO202
KSI_2/GPIO203
KSI_3/GPIO204
KSI_4/GPIO205
KSI_5/GPIO206
KSI_6/GPIO207
KSI_7/GPIO208
KSO_0/GPIO209
KSO_1/GPIO210
KSO_2/GPIO211
KSO_3/GPIO212
KSO_4/GPIO213
KSO_5/GPIO214
KSO_6/GPIO215
KSO_7/GPIO216
KSO_8/GPIO217
KSO_9/GPIO218
KSO_10/GPIO219
KSO_11/GPIO220
KSO_12/GPIO221
KSO_13/GPIO222
KSO_14/GPIO223
KSO_15/GPIO224
KSO_16/GPIO225
KSO_17/GPIO226
EMBEDDED CTRL

SB_GPIO195 R489 10K_4
SB_GPIO196 R275 10K_4

+3V A61
R474 8.2K_4 CLK_PCIE_LAN_REQ#
R486 8.2K_4 CLK_PCIE_2_REQ#

+3V_S5
D03
R553 10K_4 GBE_COL
R322 10K_4 GBE_CRS
R558 10K_4 GBE_MDIO
R343 10K_4 GBE_RXERR
R344 10K_4 GBE_PHY_INTR

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN

T35 ADP_PRES0
PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL

ACZ_SDOUT R570 33_4 ACZ_SDOUT_AUDIO [29]
C815 *10P/50V_4
ACZ_SYNC R552 33_4 ACZ_SYNC_AUDIO [29]
C800 *10P/50V_4
ACZ_BCLK R569 33_4 ACZ_BITCLK_AUDIO [29]
C814 *10P/50V_4
ACZ_RST# R554 33_4 ACZ_RST#_AUDIO [29]
ACZ_SDIN0 ACZ_SDIN0 [29]
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

B2-TEST
DEL C816
CN24
+3V_S5
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W_JTAG_DEBUG
SB JTAG

PROJECT : ZR8
Quanta Computer Inc.
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SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

SATA ODD

U34B

SB800
Part 2 of 5

[28] SATA_TX0+ — C777 0.01u/16V_4 — SATA_TX0+_C — AH9 SATA_TX0P
[28] SATA_TX0- — C775 0.01u/16V_4 — SATA_TX0-_C — AJ9 SATA_TX0N
[28] SATA_RX0- — AJ8 SATA_RX0N
[28] SATA_RX0+ — AH8 SATA_RX0P
[28] SATA_TX1+ — C774 0.01u/16V_4 — SATA_TX1+_C — AH10 SATA_TX1P
[28] SATA_TX1- — C769 0.01u/16V_4 — SATA_TX1-_C — AJ10 SATA_TX1N
[28] SATA_RX1- — AG10 SATA_RX1N
[28] SATA_RX1+ — AF10 SATA_RX1P
AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

SERIAL ATA

FC_CLK AH28 — T80
FC_FBCLKOUT AG28 — T81
FC_FBCLKIN AF26 — T78
FC_OE#/GPIOD145 AF28 — T75
FC_AVD#/GPIOD146 AG29 — T77
FC_WE#/GPIOD148 AG26 — T82
FC_CE1#/GPIOD149 AF27 — T76
FC_CE2#/GPIOD150 AE29 — T74
FC_INT1/GPIOD144 AF29 — T79
FC_INT2/GPIOD147 AH27 — T84
FC_ADQ0/GPIOD128 AJ27 — T83
FC_ADQ1/GPIOD129 AJ26 — T33
FC_ADQ2/GPIOD130 AH25 — T86
FC_ADQ3/GPIOD131 AH24 — T85
FC_ADQ4/GPIOD132 AG23 — T90
FC_ADQ5/GPIOD133 AH23 — T88
FC_ADQ6/GPIOD134 AJ22 — T91
FC_ADQ7/GPIOD135 AG21 — T93
FC_ADQ8/GPIOD136 AF21 — T92
FC_ADQ9/GPIOD137 AH22 — T87
FC_ADQ10/GPIOD138 AJ23 — T89
FC_ADQ11/GPIOD139 AF23 — T97
FC_ADQ12/GPIOD140 AJ24 — T98
FC_ADQ13/GPIOD141 AJ25 — T99
FC_ADQ14/GPIOD142 AG25 — T101
FC_ADQ15/GPIOD143 AH26 — T102

FLASH

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9
FANIN0/GPIO56 W7 WWAN_DET# — T52
FANIN1/GPIO57 V9 CPPE_NC1# — T48
FANIN2/GPIO58 W8 CRD_REQ1# — T54
TEMPIN0/GPIO171 B6 TEMPIN0
TEMPIN1/GPIO172 A6 TEMPIN1
TEMPIN2/GPIO173 A5 MB_THRMDA_SB
TEMPIN3/TALERT#/GPIO174 B5 SB_GPIO174
TEMP_COMM C7
VIN0/GPIO175 A3 SB_GPIO175
VIN1/GPIO176 R4 SB_GPIO176
VIN2/GPIO177 A4 SIDE_PORT_ID0
VIN3/GPIO178 C5 SIDE_PORT_ID1
VIN4/GPIO179 A7 — MEM_1V5 [11]
VIN5/GPIO180 R7
VIN6/GBE_STAT3/GPIO181 B8
VIN7/GBE_LED3/GPIO182 A8

HW MONITOR

[32] SATA_ACT# — AD11 SATA_ACT#/GPIO67
AD16 SATA_X1
AC16 SATA_X2

SPI_DI/GPIO164 J5 — SB_GPIO164 — T53
SPI_DO/GPIO163 E2 — SB_GPIO163 — T60
SPI_CLK/GPIO162 K4 — SB_GPIO162 — T56
SPI_CS1#/GPIO165 K9 — SB_GPIO165 — T45
ROM_RST#/GPIO161 G2 — SB_GPIO161 — T57
NC1 G27
NC2 Y2

SPI ROM

SB820M_A12

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: 1k ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

+1.1V_AVDD_SATA
R300 SP_A12@1K/F_4 — SATA_CALRP — AB14 SATA_CALRP
R298 SP_A12@931/F_4 — SATA_CALRN — AA14 SATA_CALRN

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

+3V R302 10K_4
C760 GN@22P/50V_4 — SATA_X1
A60
Y7 GN@25MHZ
R507 GN@1M_4
C754 GN@22P/50V_4 — SATA_X2

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

TEMPIN0 R519 10K_4
TEMPIN1 R511 10K_4
MB_THRMDA_SB R521 10K_4
SB_GPIO174 R313 10K_4
SB_GPIO175 R526 10K_4
SB_GPIO176 R523 10K_4

[14] +1.1V_AVDD_SATA — +1.1V_AVDD_SATA
[11,12,14,15,24,26,31,32,36,44] +3V_S5 — +3V_S5

A05
+3V_S5
R528 SP@10K_4 — SIDE_PORT_ID0 — R316 SP@10K_4
R437 *10K_4 — SIDE_PORT_ID1 — R320 10K_4
B2-TEST

	ID1	ID0
HYX	0	0
SAM	0	1
ATI	1	0

BOARD_ID0 — BOARD_ID0 [11]
BOARD_ID1 — BOARD_ID1 [11]
BOARD_ID2 — BOARD_ID2 [11]
BOARD_ID3 — BOARD_ID3 [11]
BOARD_ID4 — BOARD_ID4 [11]

A55
+3V
R311 10K_4 — BOARD_ID0 — R314 *10K_4
R324 SW@10K_4 — BOARD_ID1 — R323 *IV@10K_4
R517 SP@10K_4 — BOARD_ID2 — R304 *SP@10K_4
A04
R273 *SP@10K_4 — BOARD_ID3 — R274 SP@10K_4
R272 *10K_4 — BOARD_ID4 — R271 10K_4

DDR3 Sideport Memory Device

Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

Board ID

	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A (Default)	JV51-DN (3-DIMM) (Default)	WO/Sideport	UMA	14"
1	N/A	JM51-DN (2-DIMM)	W/Sideport (Default)	Discrete (Default)	15.6" (Default)

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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power

VDDQ--3.3V I/O power

U34C

SB800

Part 3 of 5

POWER

SB820M_A12

SB820 without GBE: Connected to GND plane.

U34E

SB800

GROUND

Part 5 of 5

SB820M_A12

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

For support USB wakeup-->3V_S5

[2,4,5,6,9,10,11,12,13,15,19,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46] +3V
[2,7,8,9,10,38,44] +1.1V
[11,12,13,15,24,26,31,32,36,44] +3V_S5
[38] +1.1V_S5

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Quanta Computer Inc.

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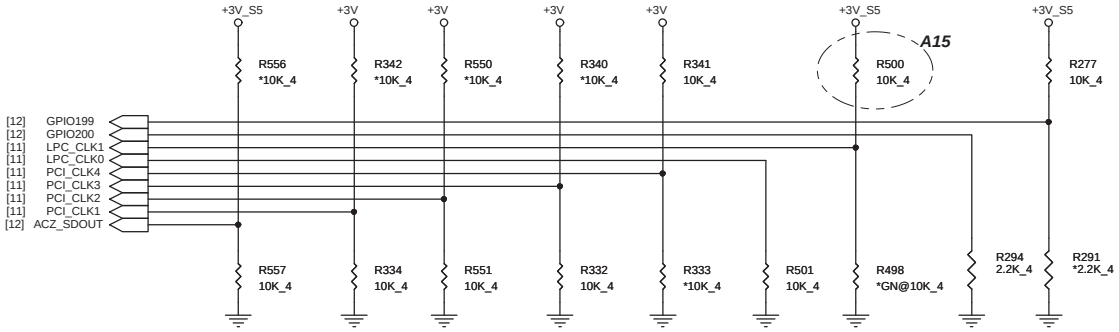
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

SB820M is supported Gen1 mode only.

For internal clock GEN.



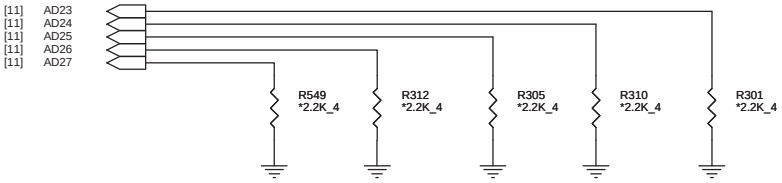
D02	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

[11,12,13,14,24,26,31,32,36,44] +3V_S5
[7,9,10,24,37,42,43,44] +1.8V
+3V_S5
+1.8V

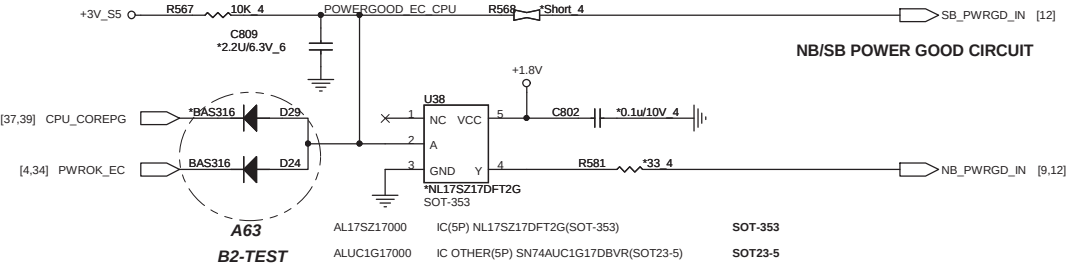
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



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Quanta Computer Inc.

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	SB820-STRAPS	1A
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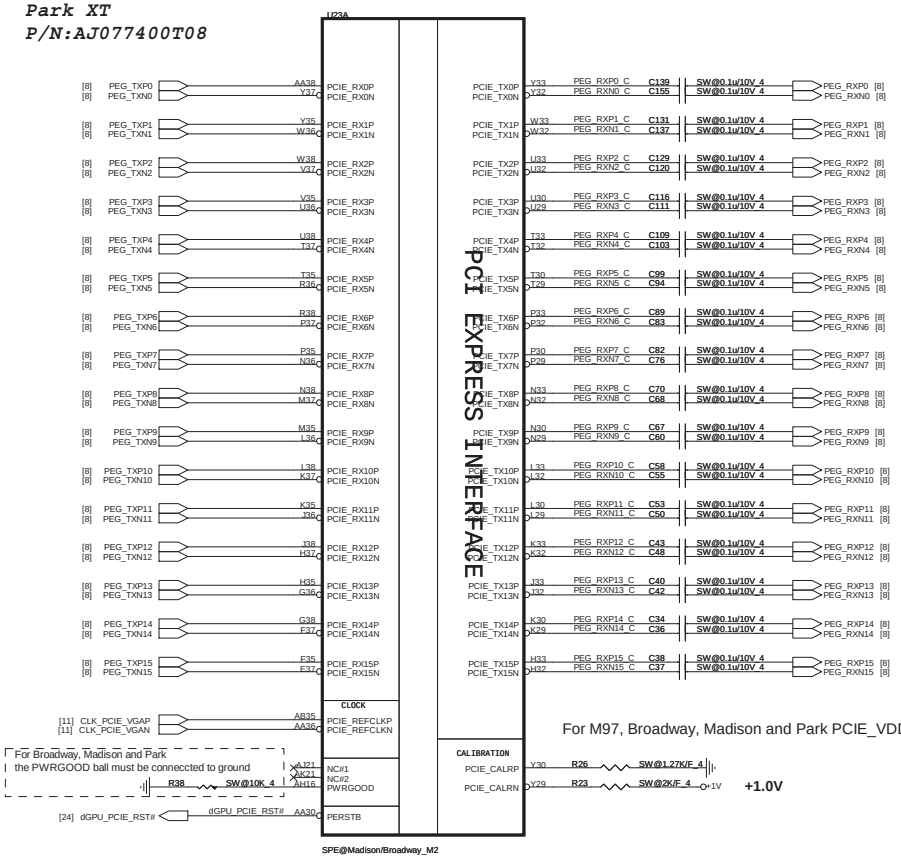
Park XT
P/N:AJ077400T08

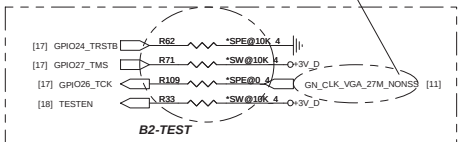


For Broadway, Madison and Park
the PWRGOOD ball must be connected to ground

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

+1.0V

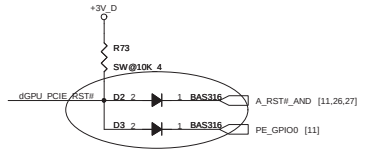
Add extra OSC for use SB clock.



B2-TEST

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
TESTEN	"1" (PU)	"1" (PU)



B2-TEST
FORM RB501 CHANGE TO BAS316

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A
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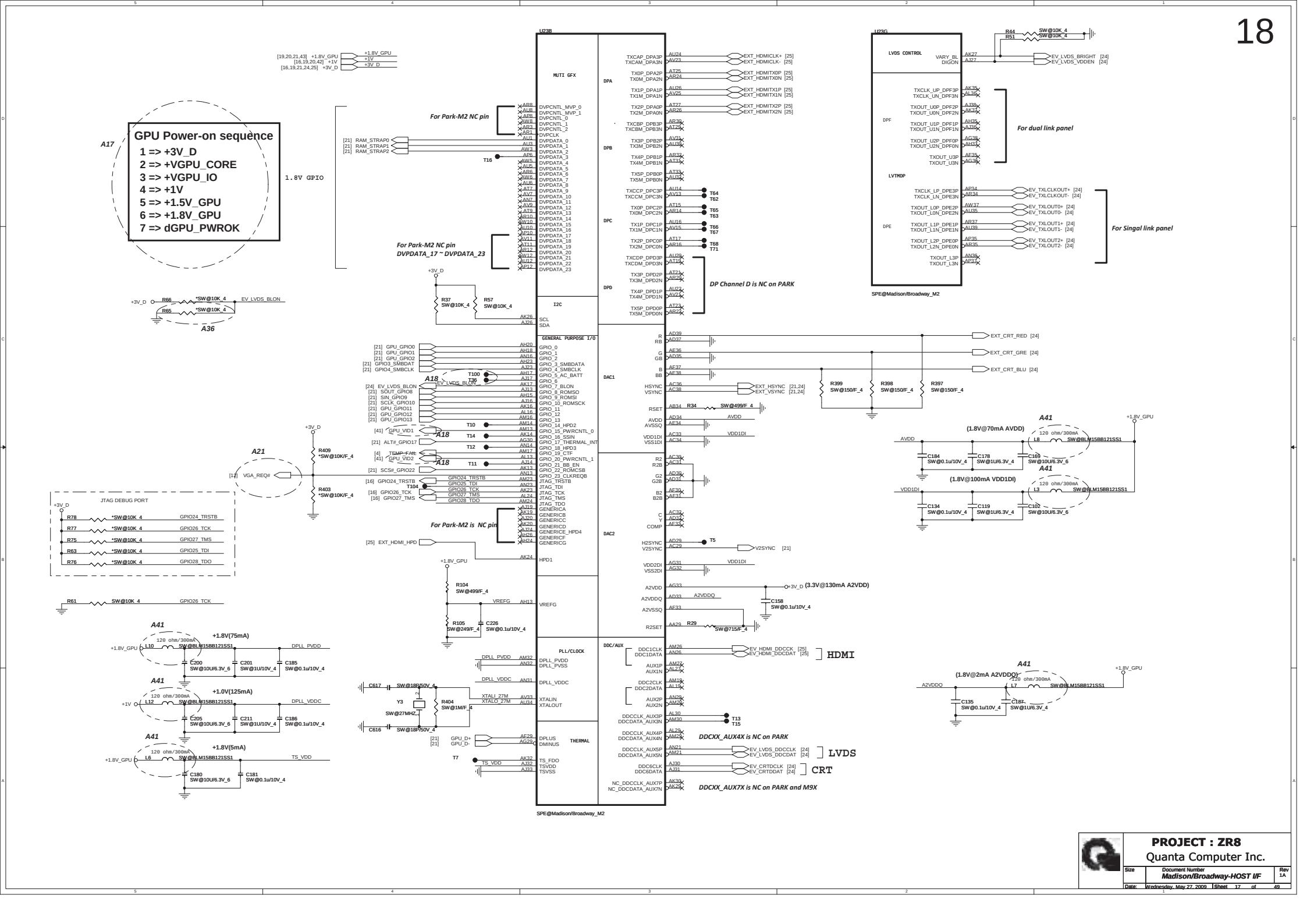
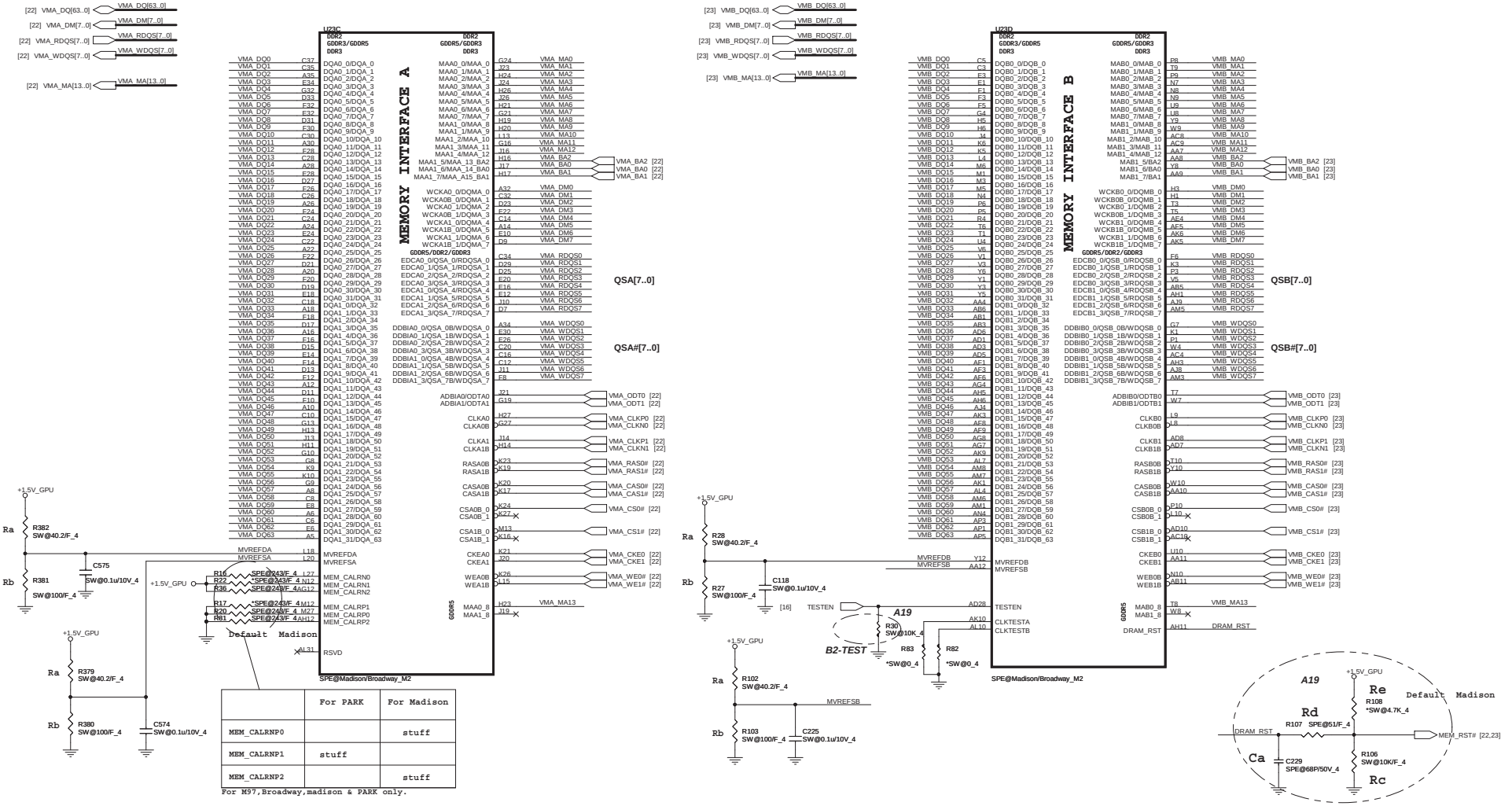

A17
GPU Power-on sequence
1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK
1.8V GPIO
U23B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
PLL/CLOCK
DDC/AUX
THERMAL
For Park-M2 NC pin
DVPDATA_17 ~ DVPDATA_23
DP Channel D is NC on PARK
For Park-M2 is NC pin
DDCXX_AUX4X is NC on PARK
DDCXX_AUX7X is NC on PARK and M9X
SPE@Madison/Broadway_M2
U23G
LVDS CONTROL
LVTMDP
For dual link panel
For Singal link panel
SPE@Madison/Broadway_M2
A18
A21
A36
A41
JTAG DEBUG PORT
HDMI
LVDS
CRT
(3.3V@130mA A2VDD)
(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)



	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

For M97,Broadway,madison & PARK only.

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3(Default)
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.
Broadway no daul rank support for GDDR5

Designator	For M97-M2	For Mannhatton
Rc	10K	10K
Rd	0R/Short	51R
Re	DNI	DNI
Ca	2.2nF	68pF

This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

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+1.5V_GPU → +1.5V_GPU [18,22,23,40,43]
+1.8V_GPU → +1.8V_GPU [17,20,21,43]
+1V → +1V [16,17,20,42]
+VGPU_CORE → +VGPU_CORE [41,44]
+3V → +3V [2,4,5,6,9,10,11,12,13,14,15,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46]

For DDR3, MVDDQ = 1.5V (7.5A)

U23E

MEM I/O

LEVEL TRANSLATION

I/O

PLL

VOLTAGE SENESE

POWER

PCIE

CORE

ISOLATED CORE I/O

SPE@Madison/Broadway_M2

(1.8V@110mA VDD_CT)

(3.3V@60mA))

(1.8V@40mA PCIE_PVDD)

(1.8V@150mA MPV18)

(1.8V@75mA SPV18)

(1.0V@120mA SPV10)

(1.8V@400mA PCIE_VDDR)

(1.0V@1.1A PCIE_VDDR)

(30A or more)

BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
(Separate Core power for PCIe bus macros
Connector to VDDCin non-ower-Xpress desingns ZR8

PIN different between Broadway and Madison		
Pin	Broadway	Madison
VDDC#32 / BIF_VDDC (N27)	VDDC	BIF_VDDC
VDDC#42 / BIF_VDDC (T27)	VDDC	BIF_VDDC
GND#61 / PX_EN (AL21)	GND	PX_EN
(AL31)	TS_A	NC_TS_A

(GDDR5 1.12V@16A VDDCI)
(DDR3 1.12V@4A VDDCI) or more

GPU +3V power

GPU all PWROK

B2-TEST

GND

GND#61/ PX_EN
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.

Pin AL21 to Ground for Broadway

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	Madison/Broadway (PWR/GND)	1A
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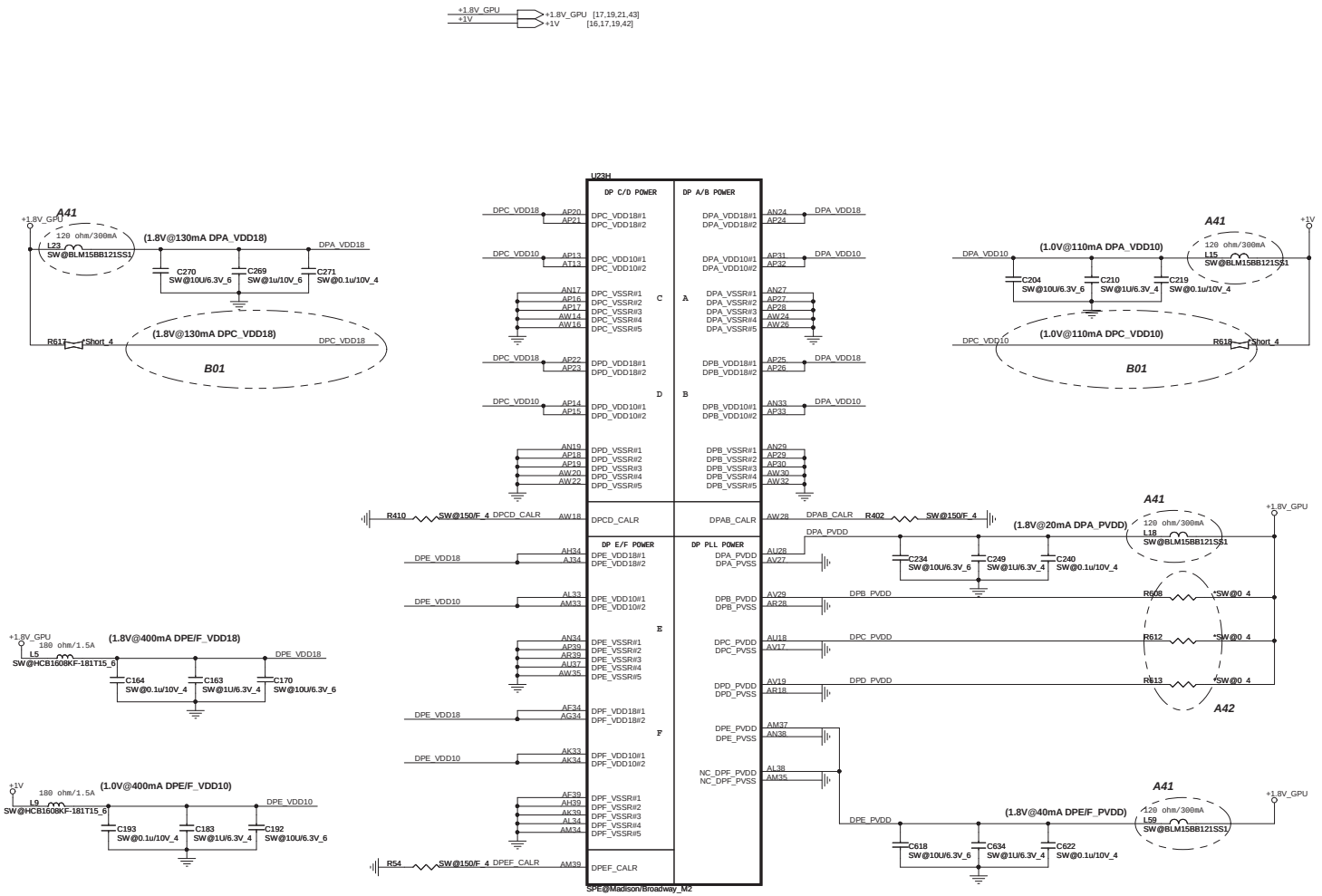

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	Quanta Computer Inc.	
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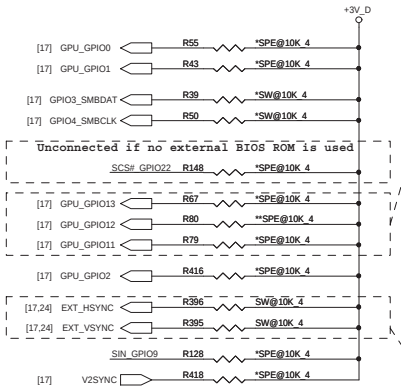
PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Function Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

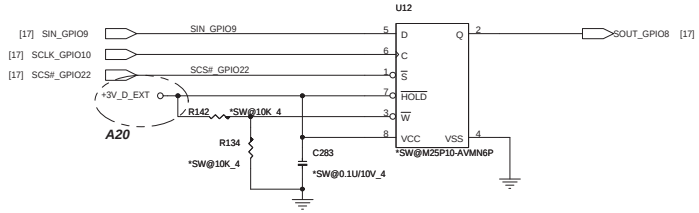
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

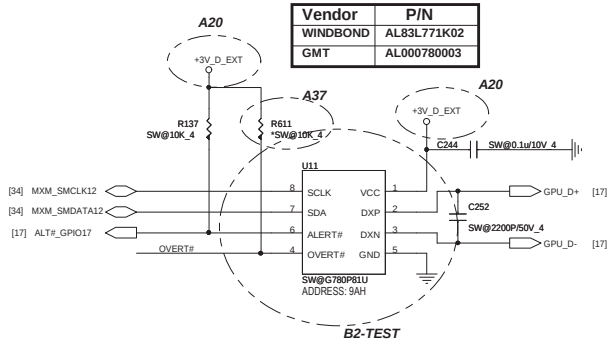
ZR8

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0 GT/s capability will be controlled by software.)
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disenable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

SERIAL ROM



Thermal Sensor



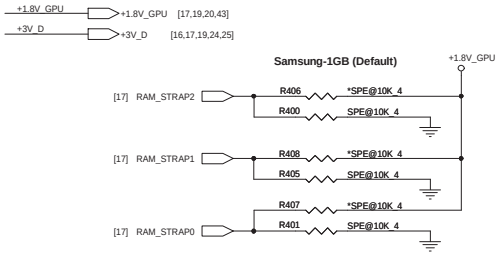
Vendor	P/N
WINDBOND	AL83L771K02
GMT	AL000780003

DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			Park	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Madison	1	0	0
			2Gb	1	1	1
Samsung			Park	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Madison	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD			Park	0	1	1
	23EY2387MA12-SZ	AKD5LGGT700	Madison	1	0	1

C14
D10



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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CHANNEL A: 512MB DDR3 (64M*16*4pcs)

[18] VMA_DQ[63..0] — VMA_DQ[63..0]
[18] VMA_DM[7..0] — VMA_DM[7..0]
[18] VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
[18] VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]

TOP Left

BOT Left

BOT Right

TOP Right

Group-A0 VREF

+1.5V_GPU
R378 SW@4.99K/F_4 — VREFC_VMA1 — R377 SW@4.99K/F_4 — C573 SW@0.1u/10V_4
R365 SW@4.99K/F_4 — VREFD_VMA1 — R366 SW@4.99K/F_4 — C565 SW@0.1u/10V_4
R3 SW@4.99K/F_4 — VREFC_VMA2 — R2 SW@4.99K/F_4 — C3 SW@0.1u/10V_4
R7 SW@4.99K/F_4 — VREFD_VMA2 — R6 SW@4.99K/F_4 — C22 SW@0.1u/10V_4

Group-A1 VREF

+1.5V_GPU
R367 SW@4.99K/F_4 — VREFC_VMA3 — R368 SW@4.99K/F_4 — C566 SW@0.1u/10V_4
R383 SW@4.99K/F_4 — VREFD_VMA3 — R375 SW@4.99K/F_4 — C576 SW@0.1u/10V_4
R8 SW@4.99K/F_4 — VREFC_VMA4 — R9 SW@4.99K/F_4 — C28 SW@0.1u/10V_4
R4 SW@4.99K/F_4 — VREFD_VMA4 — R5 SW@4.99K/F_4 — C13 SW@0.1u/10V_4

MEM_A0 CLK

VMA_CLKP0
VMA_CLKN0
R364 SW@56.2/F_4 — R363 SW@56.2/F_4
C558 SW@0.01u/25V_4

Group-A0 decoupling CAP

+1.5V_GPU
C578 SW@1U/6.3V_4 C569 SW@1U/6.3V_4 C564 SW@1U/6.3V_4 C571 SW@1U/6.3V_4 C561 SW@1U/6.3V_4 C8 SW@1U/6.3V_4 C560 SW@1U/6.3V_4 C559 SW@1U/6.3V_4
C579 SW@1U/6.3V_4 C9 SW@1U/6.3V_4 C21 SW@1U/6.3V_4 C572 SW@1U/6.3V_4 C30 SW@1U/6.3V_4 C23 SW@1U/6.3V_4 C7 SW@1U/6.3V_4 C20 SW@1U/6.3V_4
C562 SW@10U/6.3V_6 C18 SW@10U/6.3V_6 C2 SW@10U/6.3V_6 C5 SW@10U/6.3V_6 C17 SW@10U/6.3V_6

Group-A1 decoupling CAP

+1.5V_GPU
C567 SW@1U/6.3V_4 C563 SW@1U/6.3V_4 C14 SW@1U/6.3V_4 C27 SW@1U/6.3V_4 C31 SW@1U/6.3V_4 C29 SW@1U/6.3V_4 C16 SW@1U/6.3V_4 C568 SW@1U/6.3V_4
C12 SW@1U/6.3V_4 C15 SW@1U/6.3V_4 C11 SW@1U/6.3V_4 C10 SW@1U/6.3V_4 C26 SW@1U/6.3V_4 C6 SW@1U/6.3V_4 C19 SW@1U/6.3V_4 C580 SW@1U/6.3V_4
C4 SW@10U/6.3V_6 C570 SW@10U/6.3V_6 C1 SW@10U/6.3V_6 C556 SW@10U/6.3V_6 C557 SW@10U/6.3V_6

MEM_A1 CLK

VMA_CLKP1
VMA_CLKN1
R370 SW@56.2/F_4 — R371 SW@56.2/F_4
C555 SW@0.01u/25V_4

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	MEMORY 1 channel A	1A
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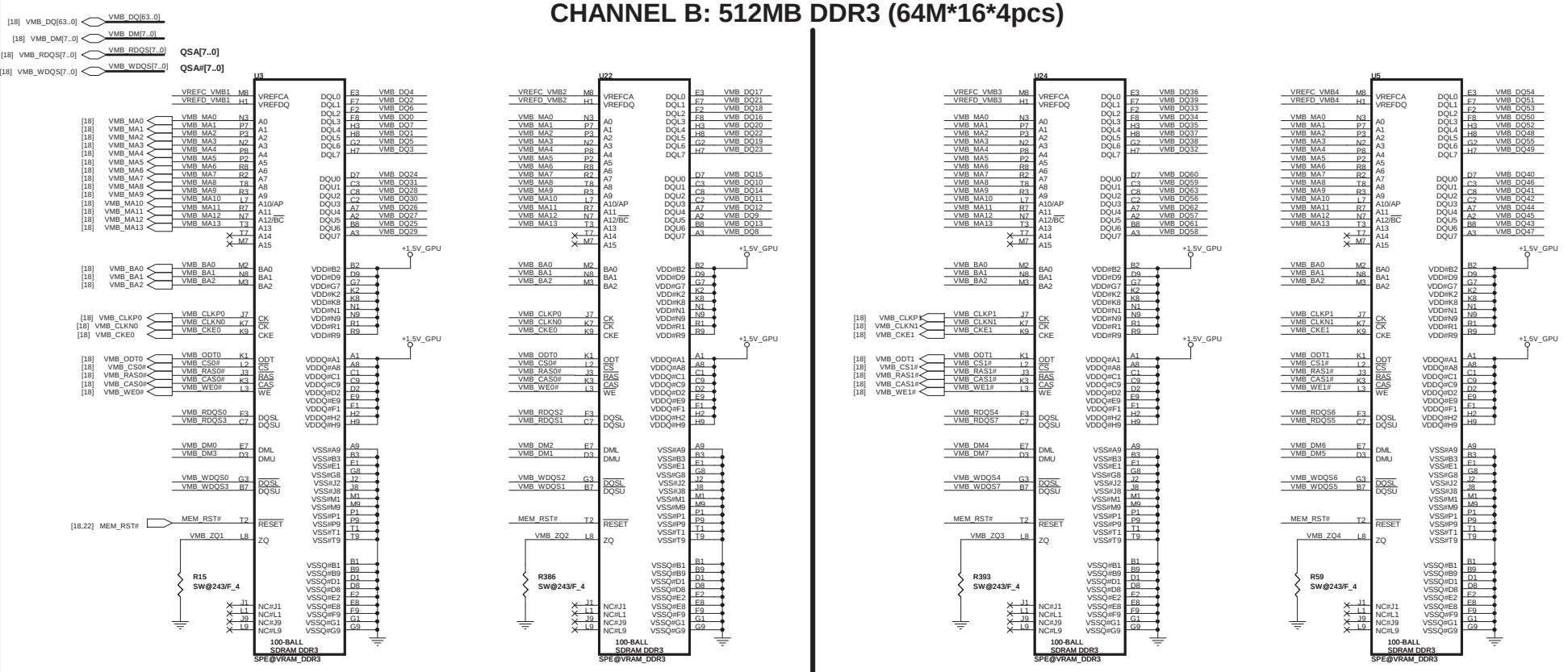
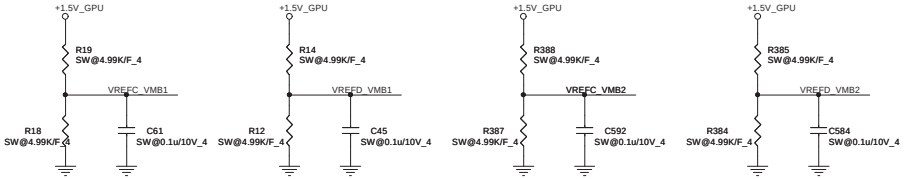
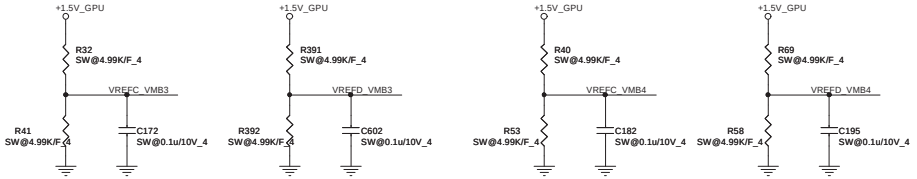
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



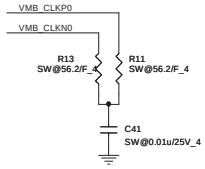
Group-B0 VREF



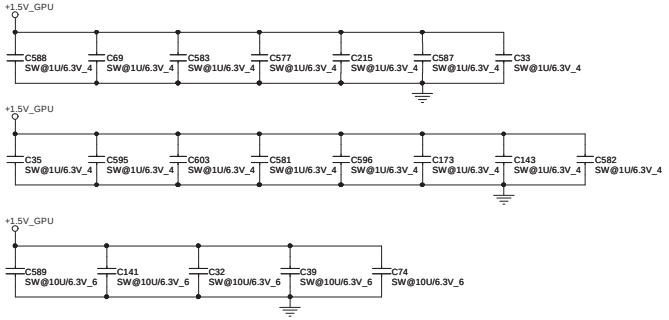
Group-B1 VREF



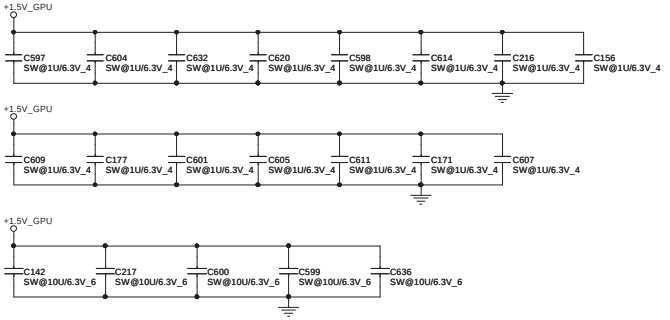
MEM_B0 CLK



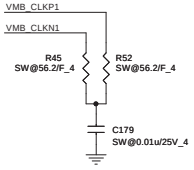
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



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Quanta Computer Inc.

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	MEMORY 2 channel B	1A
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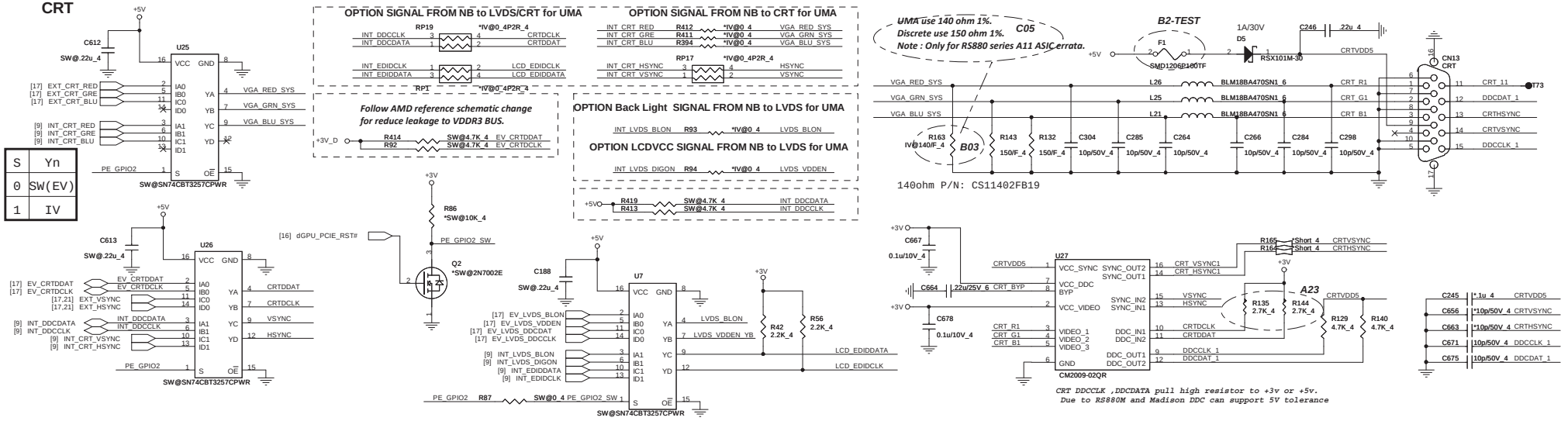
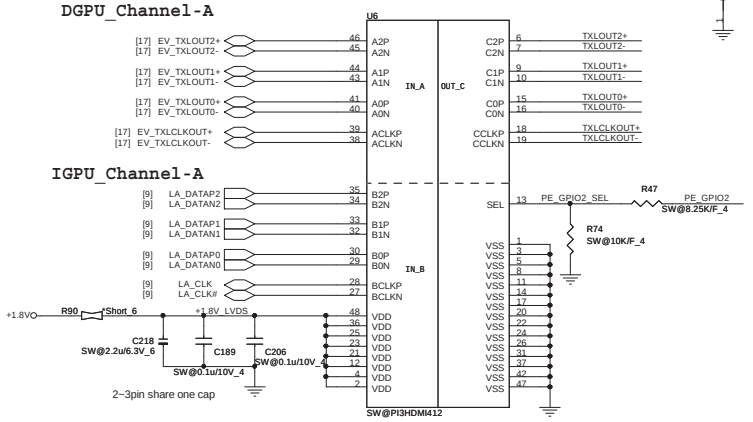
CRT



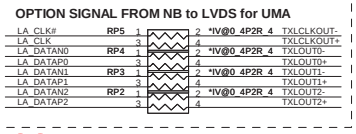
S	Yn
0	SW(EV)
1	IV

DGPU_Channel-A / IGPU_Channel-A



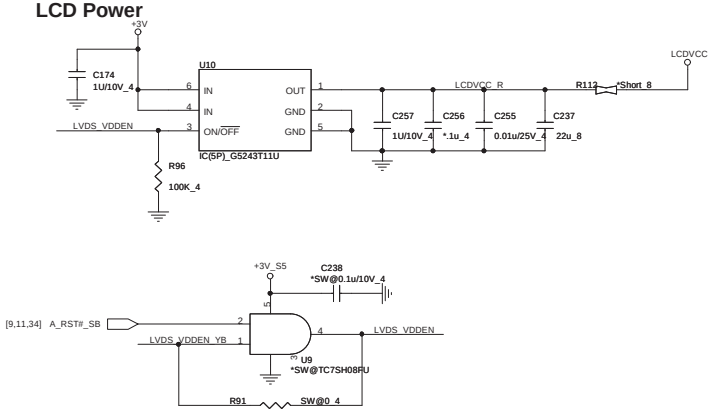
PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS

OPTION SIGNAL FROM NB to LVDS for UMA

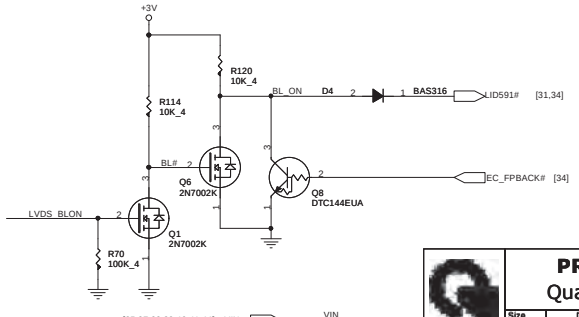


CAMERA Module(CCD)

LCD Power



Backlight Control



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Quanta Computer Inc.
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UMA/DISCRETE select for HDMI

From RS880M

for Layout concern ,placement close north bridge

for Layout concern ,placement close HDMI conn

[8] PEG_TXN15_C	C280	*IV@0.1U/10V_4	TX2_HDMI-L	RP10	1	2	*IV@0_4P2R_4	TX2_HDMI-
[8] PEG_TXP15_C	C272	*IV@0.1U/10V_4	TX2_HDMI+L		3	4		TX2_HDMI+
[8] PEG_TXN14_C	C267	*IV@0.1U/10V_4	TX1_HDMI-L	RP9	1	2	*IV@0_4P2R_4	TX1_HDMI-
[8] PEG_TXP14_C	C263	*IV@0.1U/10V_4	TX1_HDMI+L		3	4		TX1_HDMI+
[8] PEG_TXN13_C	C253	*IV@0.1U/10V_4	TX0_HDMI-L		1	2		TX0_HDMI-
[8] PEG_TXP13_C	C247	*IV@0.1U/10V_4	TX0_HDMI+L	RP8	3	4	*IV@0_4P2R_4	TX0_HDMI+
[8] PEG_TXN12_C	C239	*IV@0.1U/10V_4	TXC_HDMI-L		1	2		TXC_HDMI-
[8] PEG_TXP12_C	C232	*IV@0.1U/10V_4	TXC_HDMI+L	RP7	3	4	*IV@0_4P2R_4	TXC_HDMI+

From dGPU

[17] EXT_HDMITX2N	C698	SW@0.1u/10V_4	TX2_HDMI-	
[17] EXT_HDMITX2P	C697	SW@0.1u/10V_4	TX2_HDMI+	
[17] EXT_HDMITX1N	C696	SW@0.1u/10V_4	TX1_HDMI-	
[17] EXT_HDMITX1P	C695	SW@0.1u/10V_4	TX1_HDMI+	
[17] EXT_HDMITX0N	C694	SW@0.1u/10V_4	TX0_HDMI-	
[17] EXT_HDMITX0P	C693	SW@0.1u/10V_4	TX0_HDMI+	
[17] EXT_HDMICLK-	C692	SW@0.1u/10V_4	TXC_HDMI-	
[17] EXT_HDMICLK+	C691	SW@0.1u/10V_4	TXC_HDMI+	

for Layout concern ,placement close HDMI conn

+5V

Q34 2N7002K

R460 100K/F_4

R457	SP_715@499/F_4	TX2_HDMI+	
R459	SP_715@499/F_4	TX2_HDMI-	
R454	SP_715@499/F_4	TX1_HDMI+	UMA RS880M 715 ohm CS17152FB17
R456	SP_715@499/F_4	TX1_HDMI-	
R451	SP_715@499/F_4	TX0_HDMI+	DIS Park-M2 499 ohm CS14992FB24
R453	SP_715@499/F_4	TX0_HDMI-	
R448	SP_715@499/F_4	TXC_HDMI+	
R450	SP_715@499/F_4	TXC_HDMI-	

Close to HDMI Connector

EMI reserve for HDMI(HDM)

Close connector

TX2_HDMI+	R458 *100/F_4	TX2_HDMI-
TX1_HDMI+	R455 *100/F_4	TX1_HDMI-
TX0_HDMI+	R452 *100/F_4	TX0_HDMI-
TXC_HDMI+	R449 *100/F_4	TXC_HDMI-

HDMI HPD SENSE

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin

+3V_D

R444 SW@10K_4

[17] EXT_HDMI_HPD

Q33 SW@2N7002K

+3V

R187 10K/F_4

Q16 2N7002K

R177 200K/F_4

HDMI_DET

R176 200K/F_4

+3V

R186 10K_4

[9] INT_HDMI_HPD

Q15 2N7002K

HDMI_HPD_EC# [34]

Close to HDMI Connector

*IV@0_4P2R_4

[9] HDMI_DDC_DATA
[9] HDMI_DDC_CLK

RP20

HDMI_SDATA
HDMI_SCLK

UMA

DIS

+3V
+5V

R443 SW@4.7K_4

[17] EV_HDMI_DDCCK

Q41 SW@2N7002K

HDMI_SCLK

R445 *SW@0_4

R614 SW@4.7K_4

[17] EV_HDMI_DDCDAT

Q42 SW@2N7002K

HDMI_SDATA

R534 *SW@0_4

A54

HDMI PORT

CN17

TX2_HDMI+	1	SHELL1	20
	2	D2+	
TX2_HDMI-	3	D2 Shield	
TX1_HDMI+	4	D2-	
	5	D1+	
TX1_HDMI-	6	D1 Shield	
TX0_HDMI+	7	D1-	
	8	D0+	
TX0_HDMI-	9	D0 Shield	
TXC_HDMI+	10	D0- GND	23
	11	CK+	
TXC_HDMI-	12	CK Shield GND	22
	13	CK-	
	14	CE Remote	
HDMI_SCLK	15	NC	
HDMI_SDATA	16	DDC CLK	
	17	DDC DATA	
	18	GND	
+5V_HDMI	19	+5V	
HDMI_DET		HP DET	
		SHELL2	21

SP@HDMI

B2-TEST

+5V

F2 SMD1206P100TF

D6 RSX101M-30

C363 0.22u/6.3V_4

P/N: AOP---->DFHD19MR083
LTS---->DFHD19MR085

A49

+5V

D21 CH501H-40PT

R446 2K/F_4

HDMI_SCLK

+5V

D22 CH501H-40PT

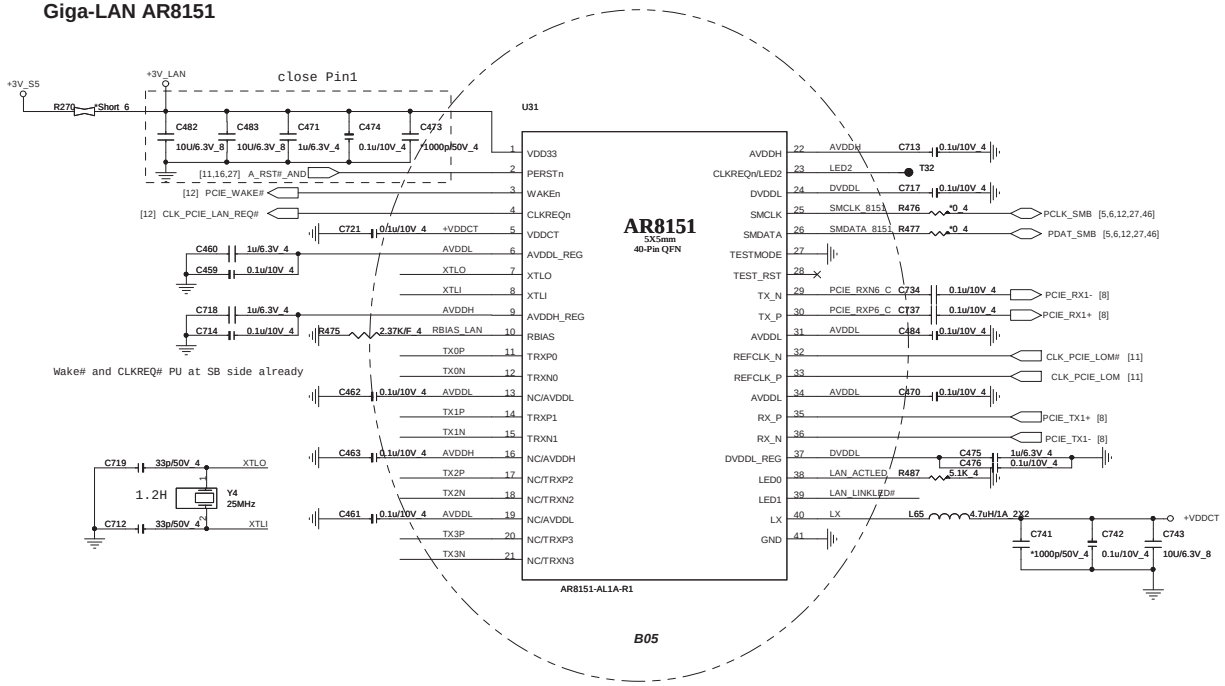
R447 2K/F_4

HDMI_SDATA

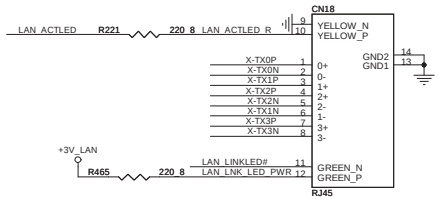
PROJECT : ZR8
Quanta Computer Inc.

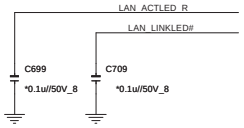
Size	Document Number	Rev
	HDMI	1A
Date: Wednesday, May 27, 2009	Sheet 25 of 49	

Giga-LAN AR8151

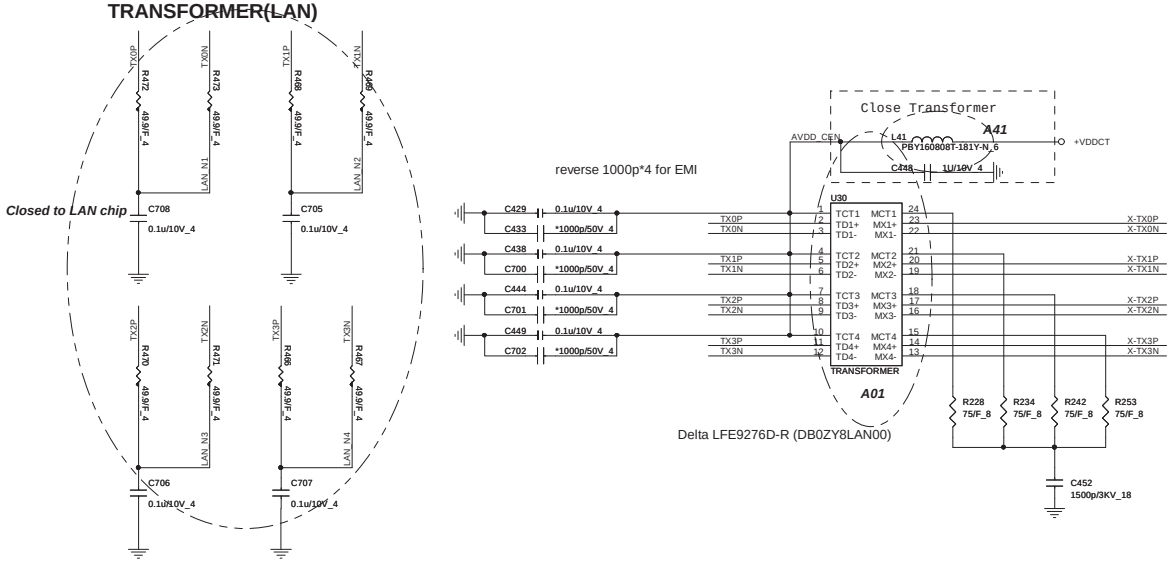


RJ45(LAN)





TRANSFORMER(LAN)

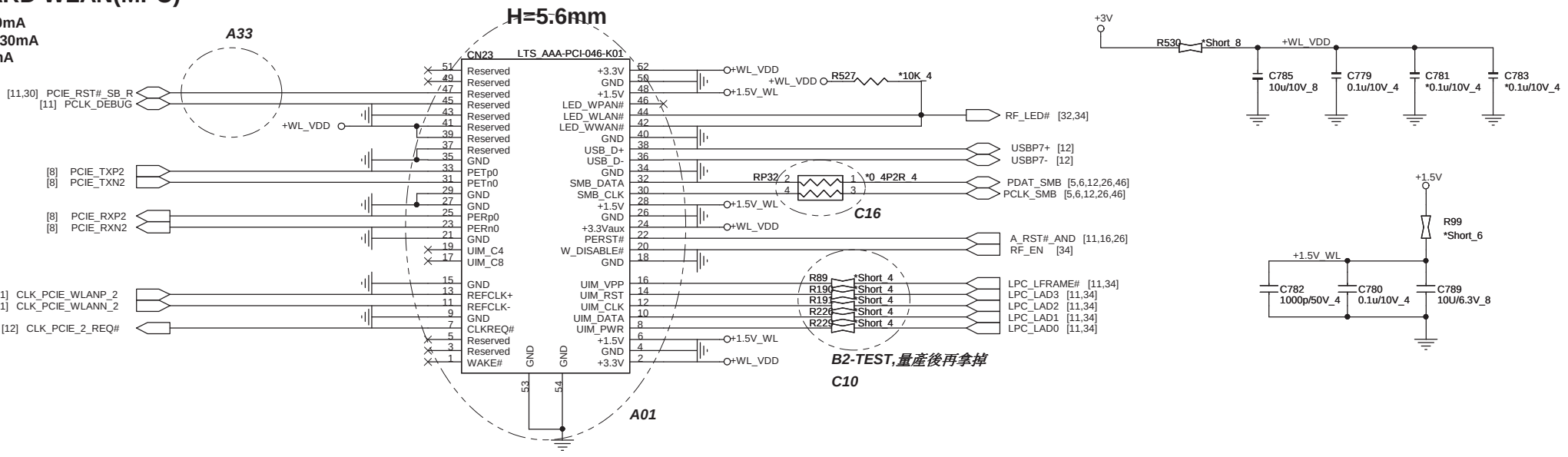


PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	LAN (AR8151)	1A
Date: Wednesday, May 27, 2009	Sheet 26 of 49	

MINI-CARD WLAN(MPC)

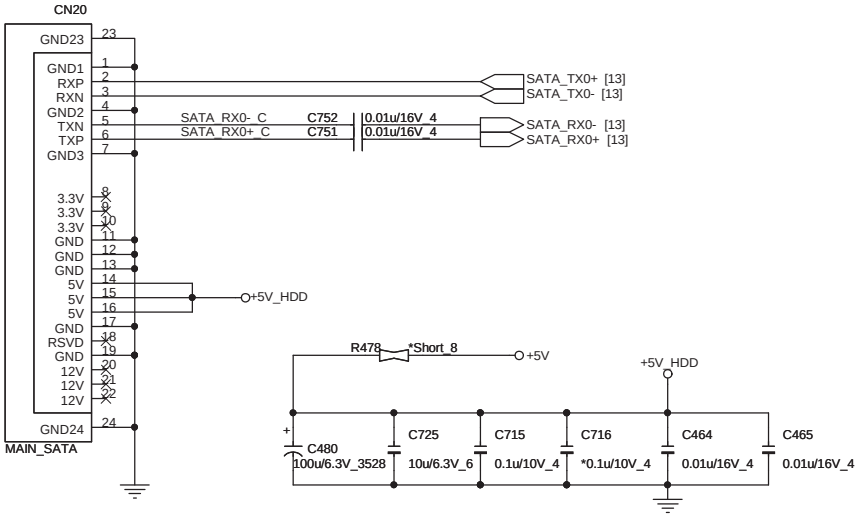
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



PROJECT : ZR8
Quanta Computer Inc.

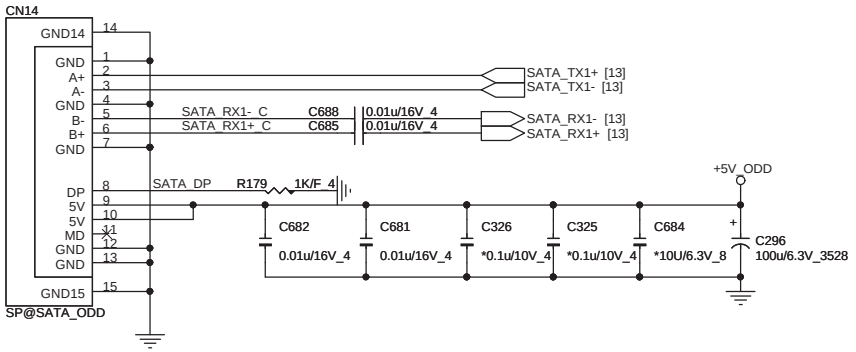
Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date: Wednesday, May 27, 2009	Sheet 27 of 49	

SATA HDD(HDD)



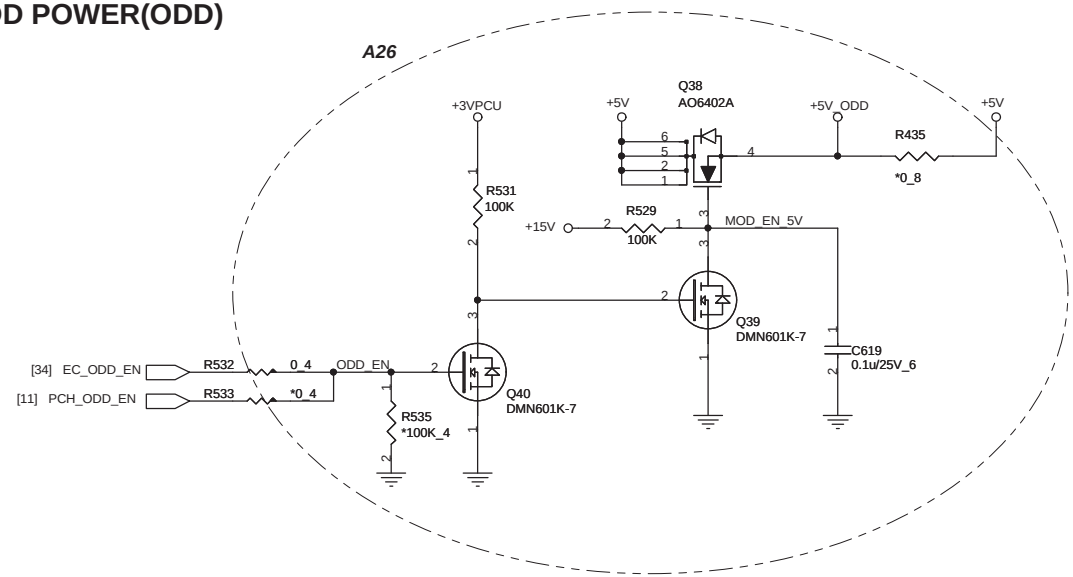
HOLE(OTH)

SATA ODD (ODD)



JM51(2-DIMM)-->CN14 P/N:DFHS13FR075
JV51(3-DIMM)-->CN14 P/N:DFHS13FR017
DFHS13FR022
DFHS13FR005
DFHS13FR006

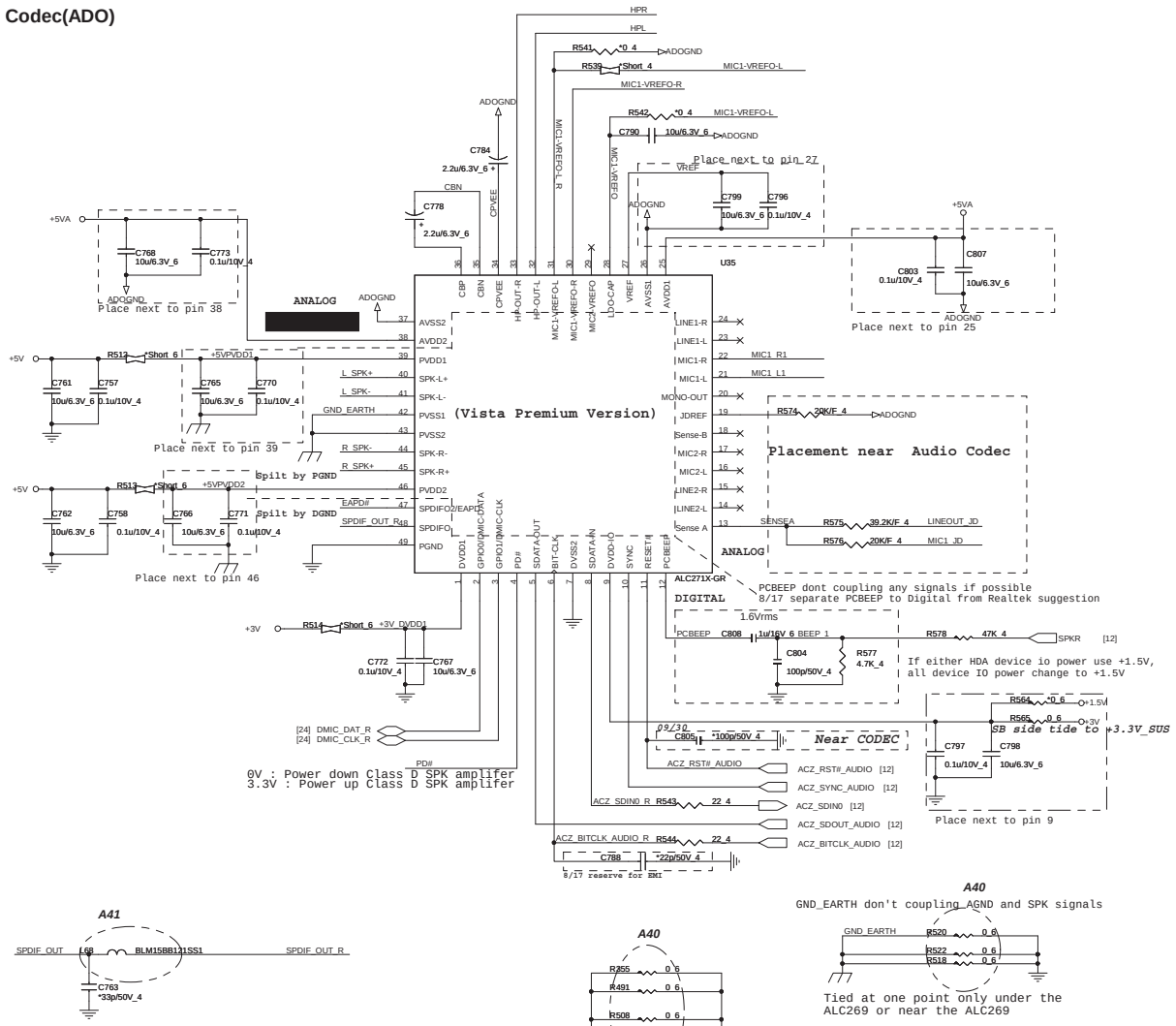
ODD POWER(ODD)



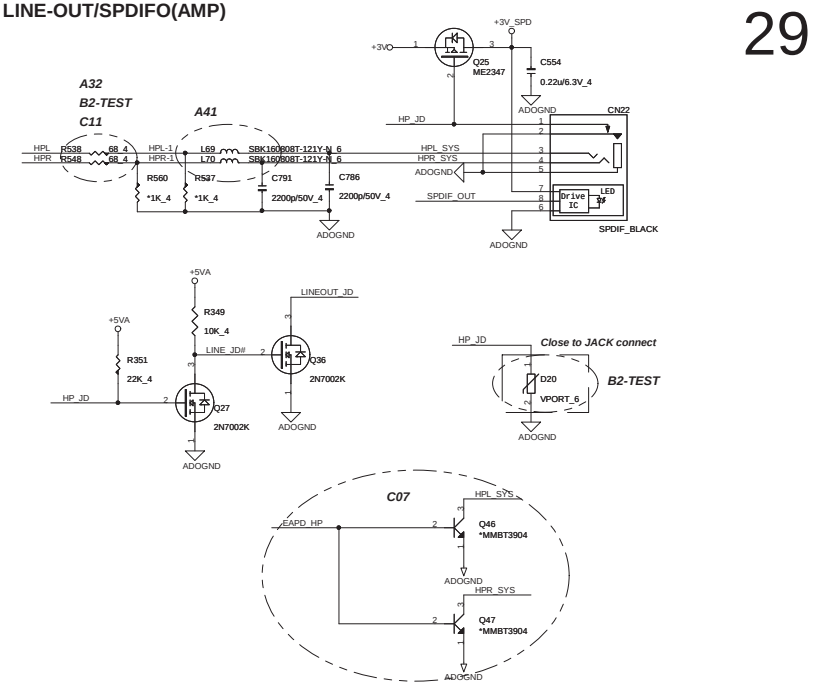
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Wednesday, May 27, 2009	Sheet 28 of 49	

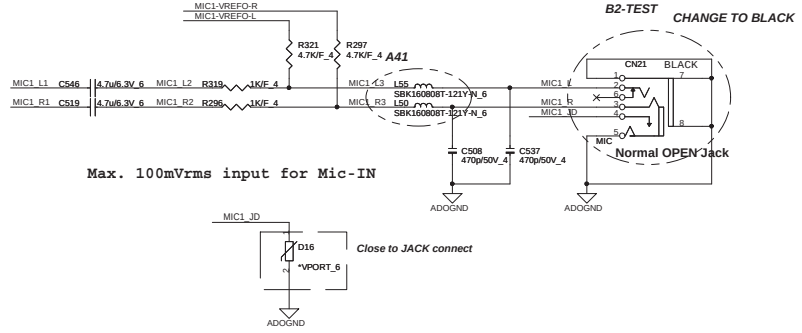
Codec(ADO)



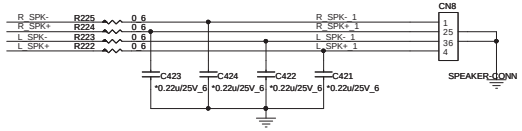
LINE-OUT/SPDIFO(AMP)



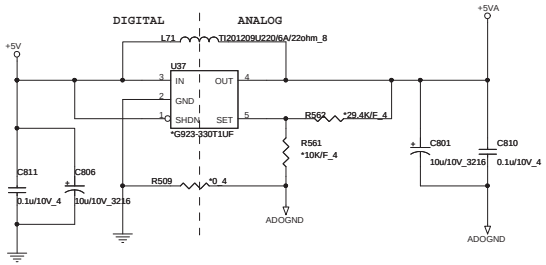
MIC(AMP)



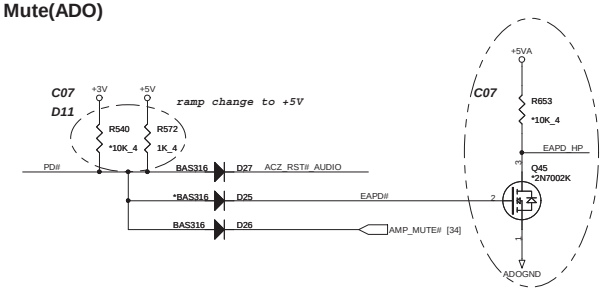
Internal Speaker(AMP)



Power (ADO)



Mute(ADO)



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	ALC271X / AMP / SPK	1A
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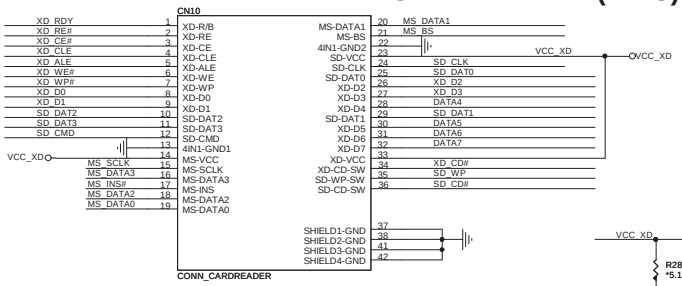
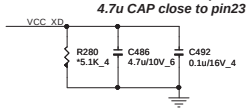
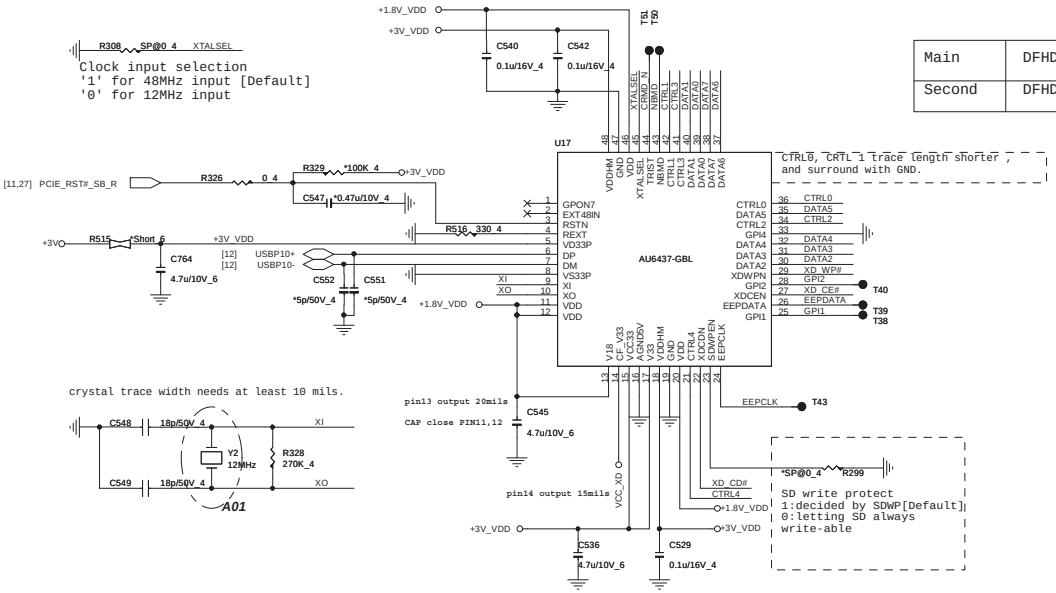
4 IN 1 CARD READER (MMC)

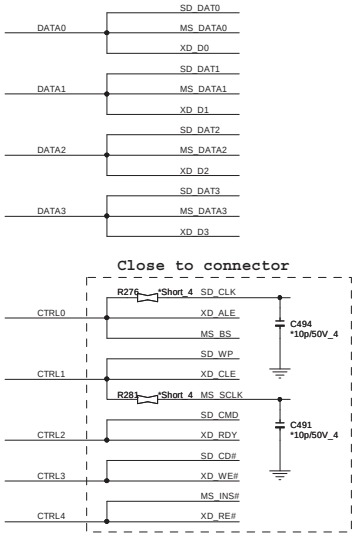


Close to Connect pin 14 & pin23
4.7u CAP close to pin23





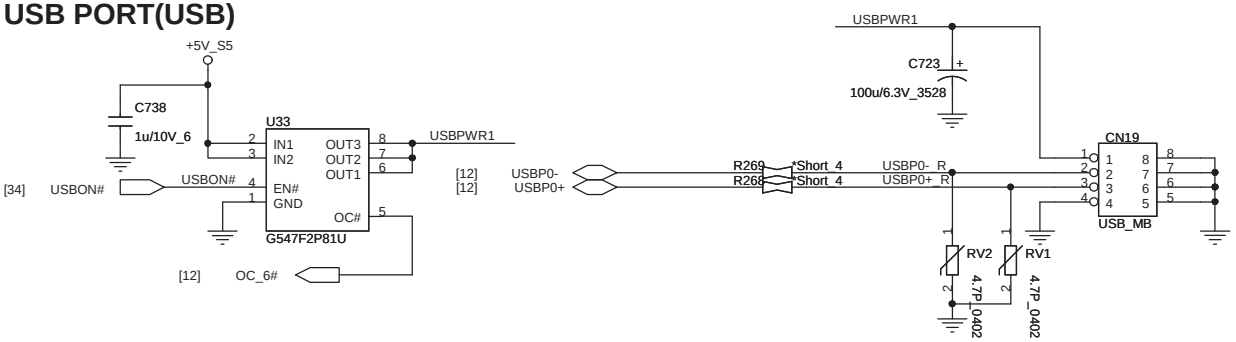
Main	DFHD36MS006
Second	DFHD36MS012



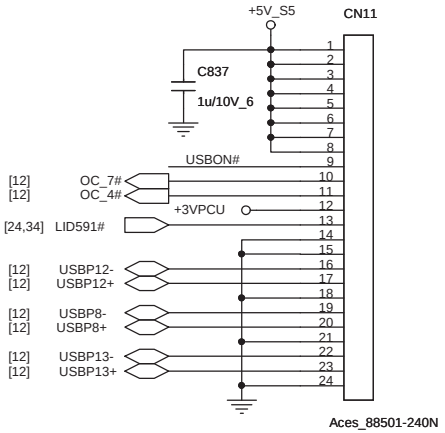
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	AU6437 CardReader	1A
Date: Wednesday, May 27, 2009	Sheet 30 of 49	

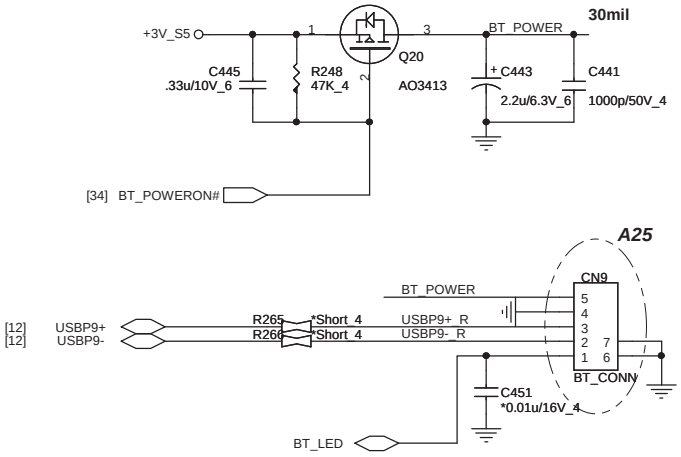
USB PORT(USB)



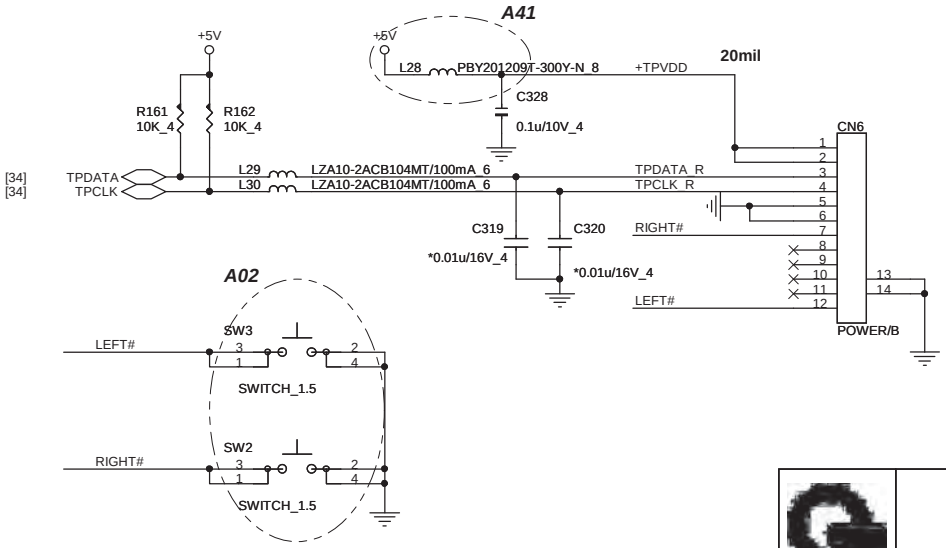
USB BOARD CONN(USB)



BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)

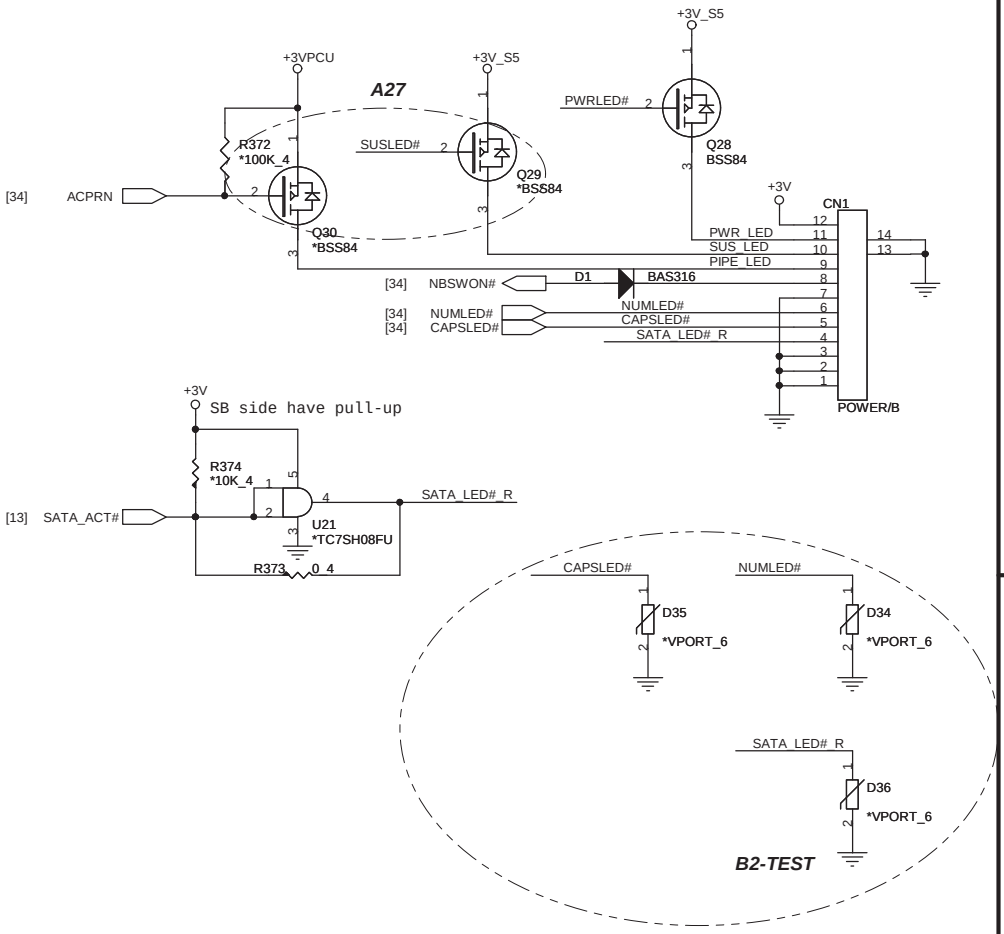


PROJECT : ZR8

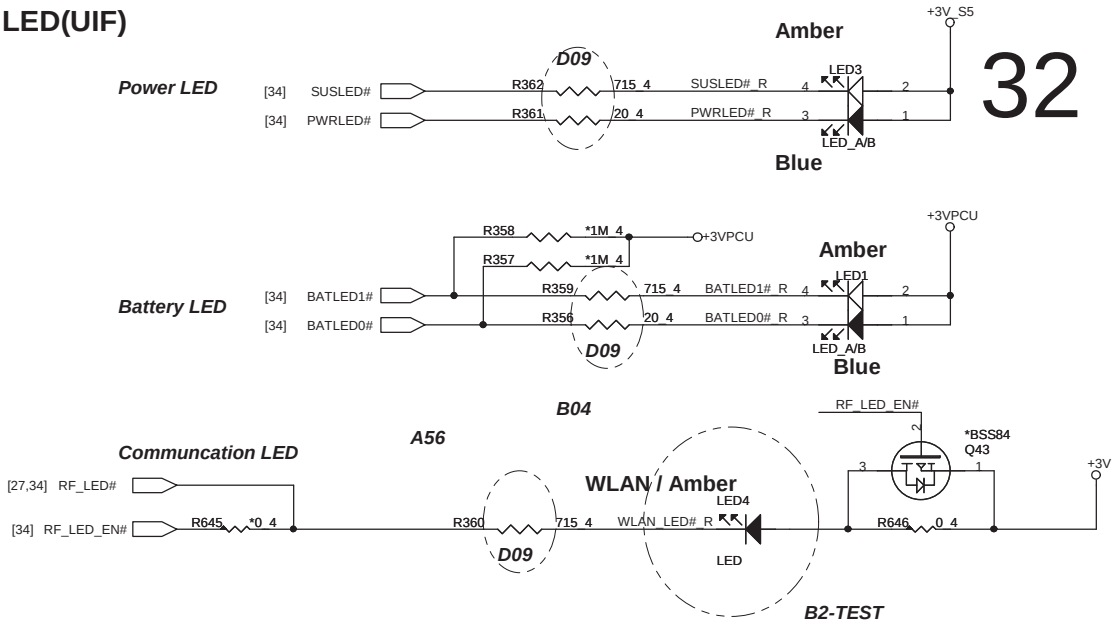
Quanta Computer Inc.

Size	Document Number	Rev
	eSATA/USB	1A
Date: Wednesday, May 27, 2009	Sheet 31 of 49	

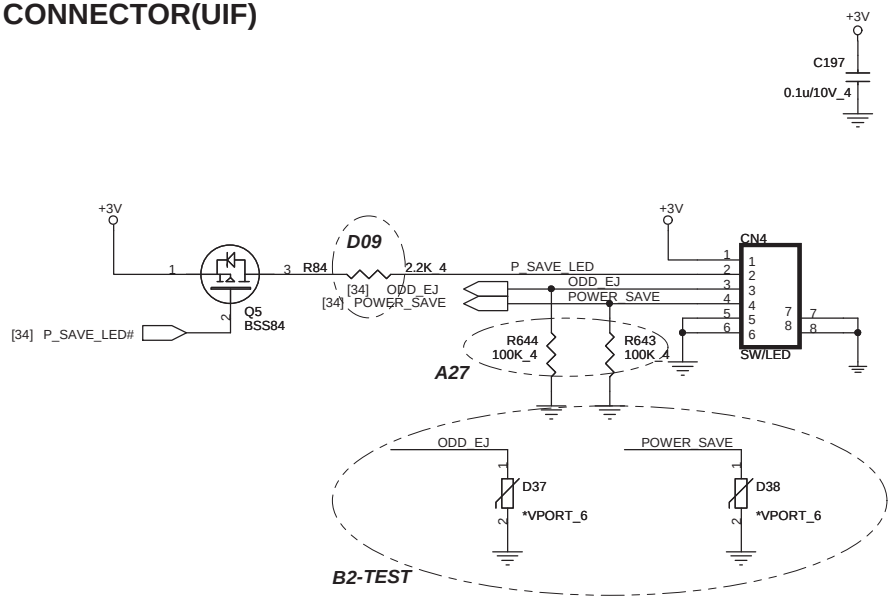
POWER BOARD CONN(UIF)



LED(UIF)



LED BOARD CONNECTOR(UIF)

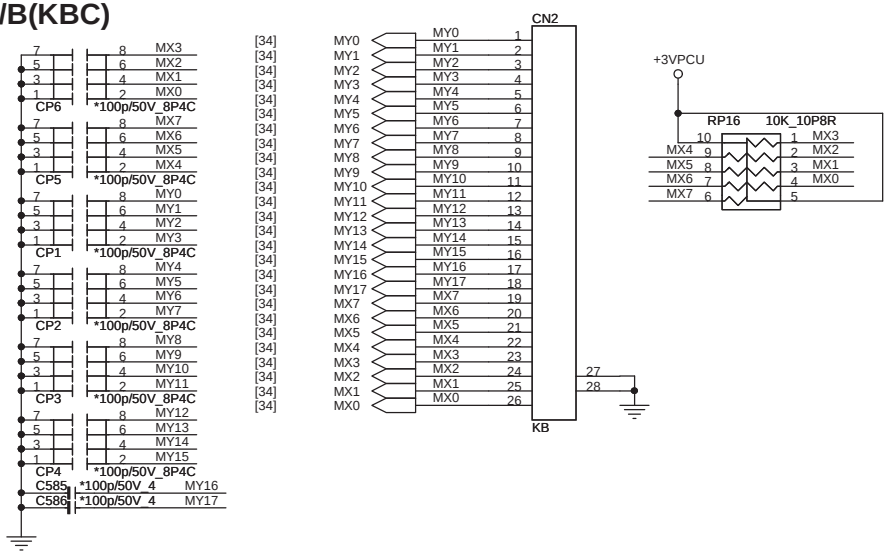


PROJECT : ZR8

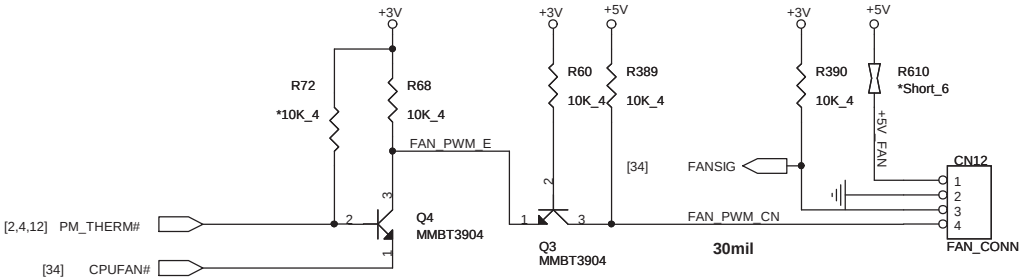
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
Date: Wednesday, May 27, 2009	Sheet 32 of 49	

K/B(KBC)

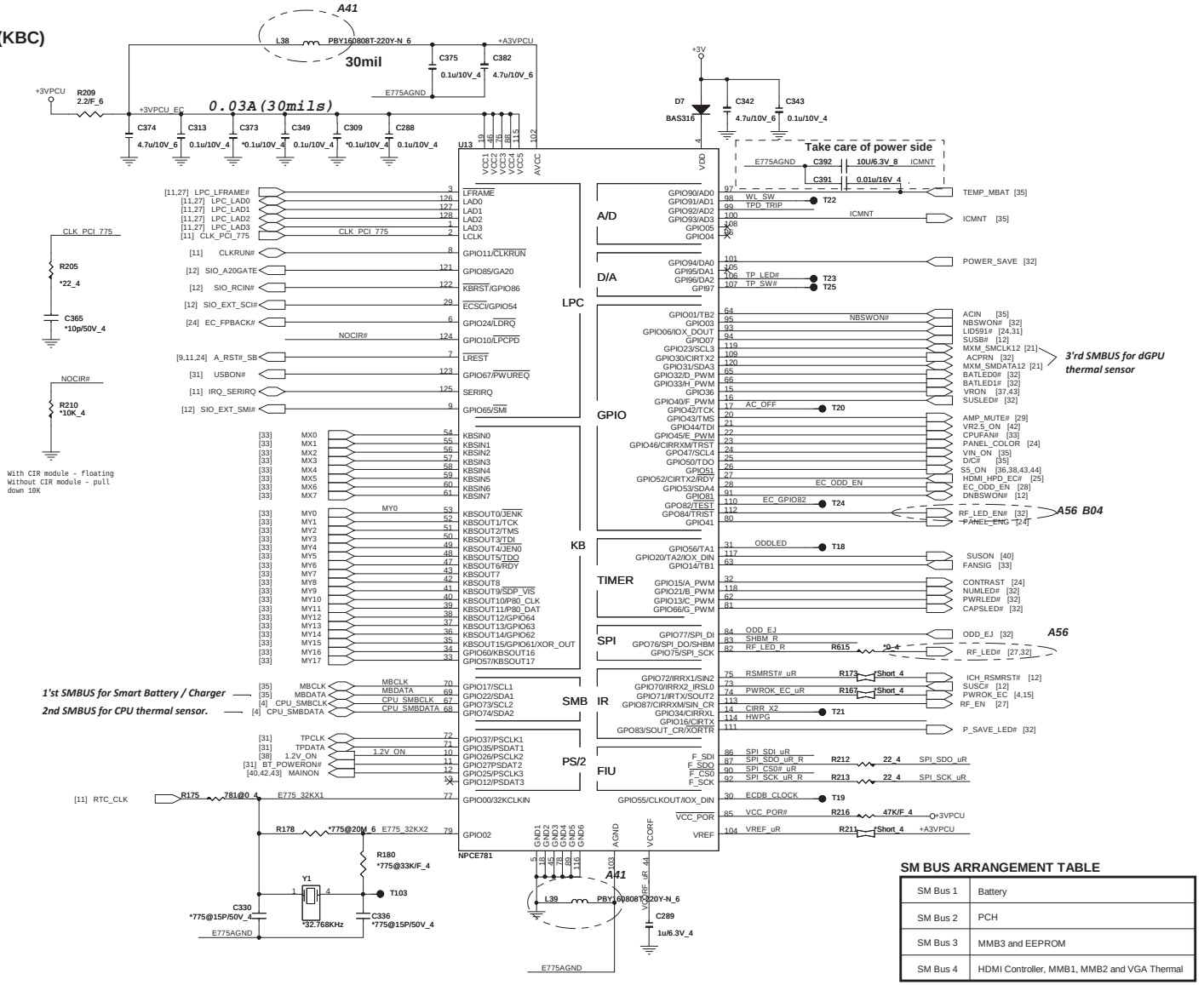


CPU FAN(THM)



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: *KB/FAN/EE RETURN CAP*	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 33 of 49	

EC(KBC)

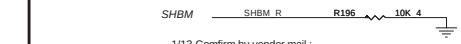


SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

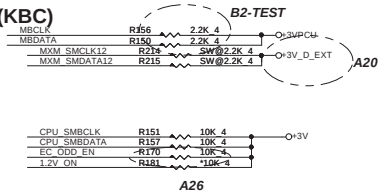
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS



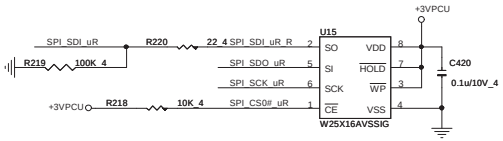
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)



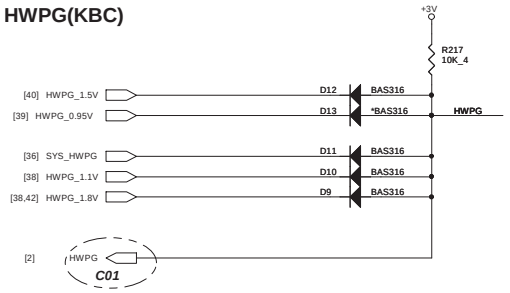
SPI FLASH(KBC)

U15 Change to 1M ==>AKE5GFK0Z09 / AKE3GZN0N00 / AKE3GZP0801

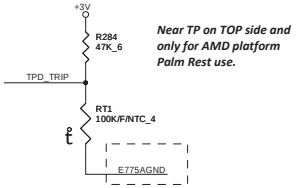


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)

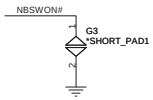


Palm Rest Thermal Sensor(THM)

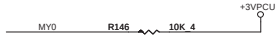


Near TP on TOP side and only for AMD platform Palm Rest use.

POWER-ON Switch(KBC)

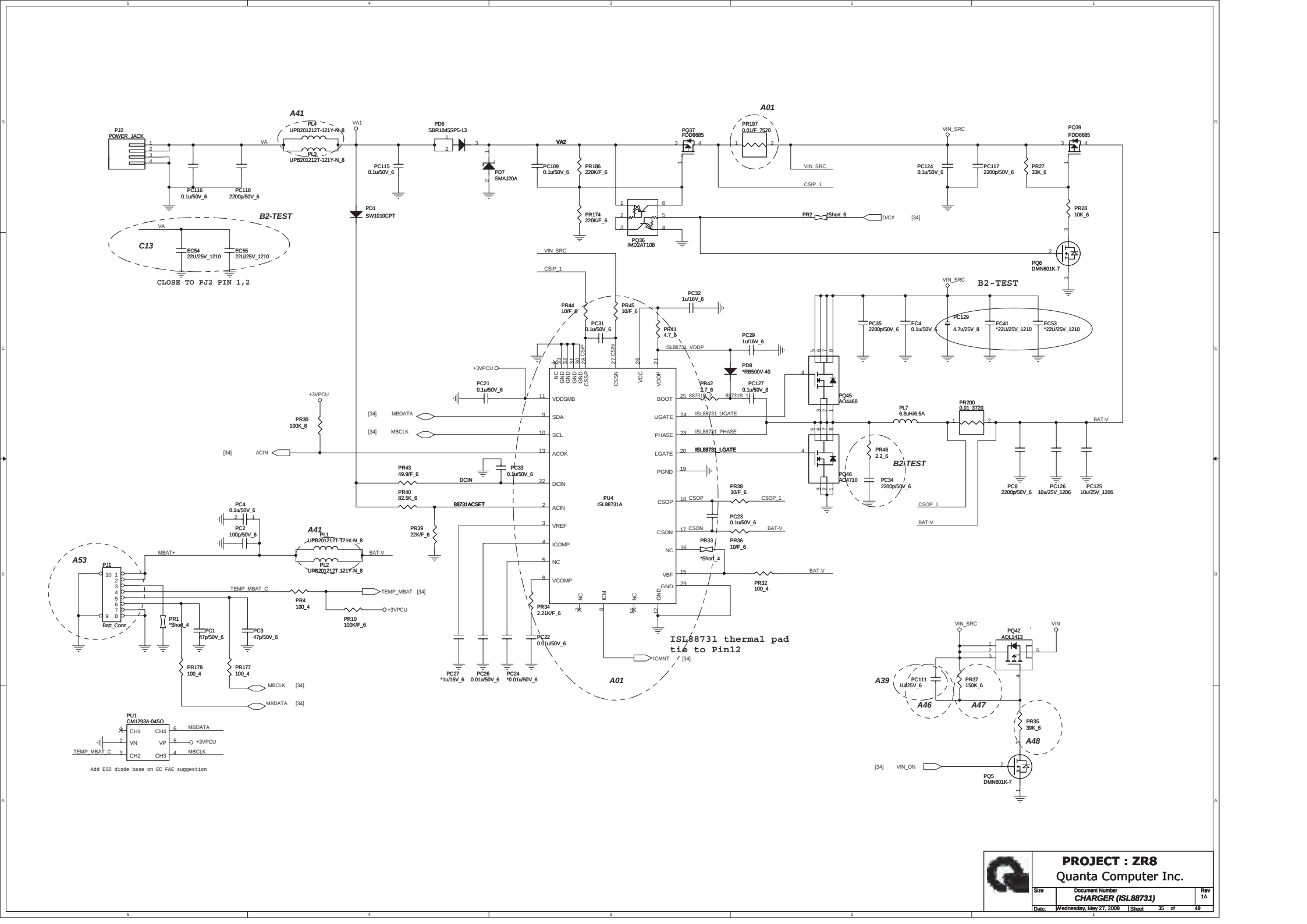


INTERNAL KEYBOARD STRIP SET(KBC)



PROJECT : ZR8
Quanta Computer Inc.

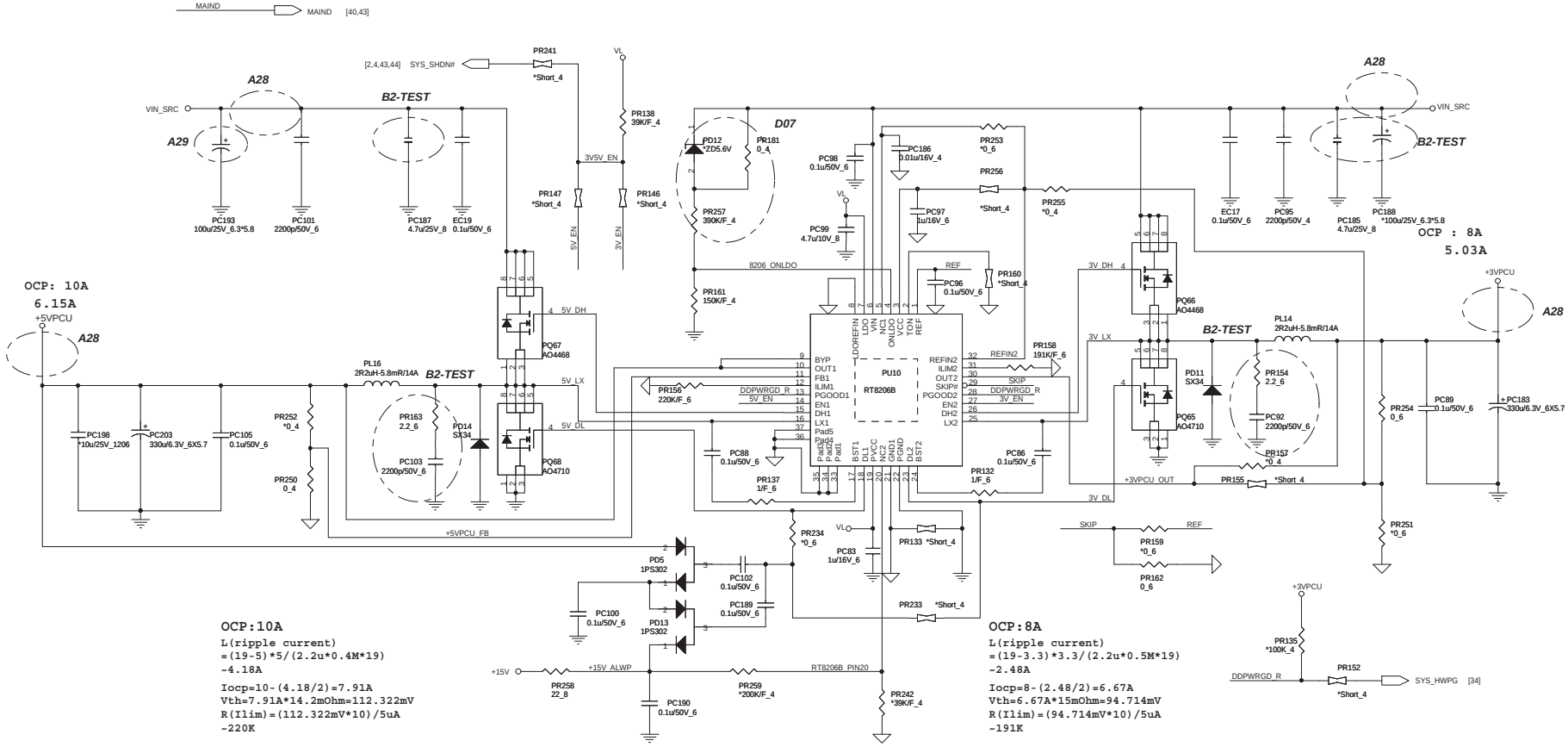
Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
Date: Wednesday, May 27, 2009	Sheet 34 of 49	



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (ISL88731)	1A
Date: Wednesday, May 27, 2009	Sheet 35 of 49	



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
Date: Wednesday, May 27, 2009	Sheet 36 of 49	

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

20A

20A

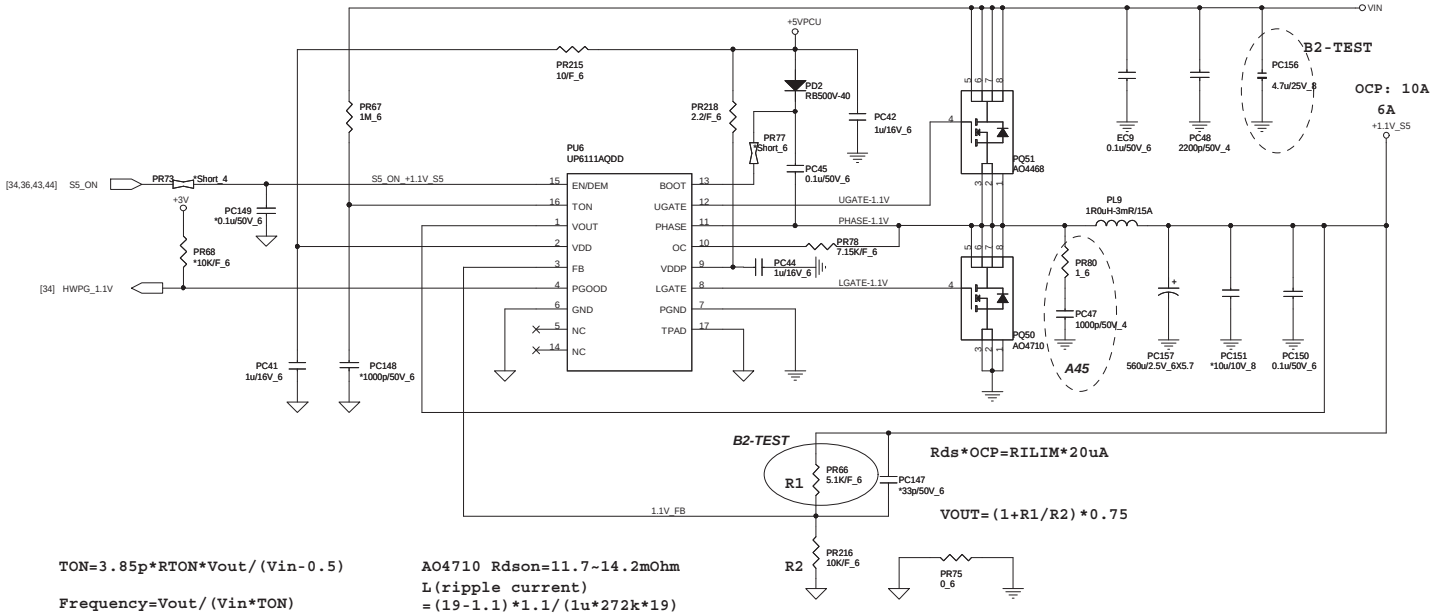
Pin 49 is GND Pin

Close to CPU socket

Close to CPU socket

Parallel

PROJECT : ZR8	
Quanta Computer Inc.	
Size	Document Number: CPU_CORE — Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 37 of 49



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

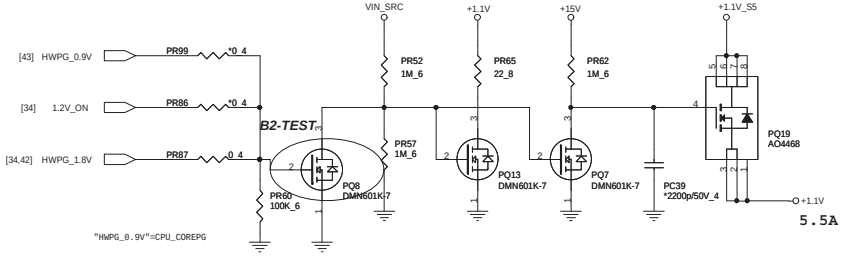
Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A

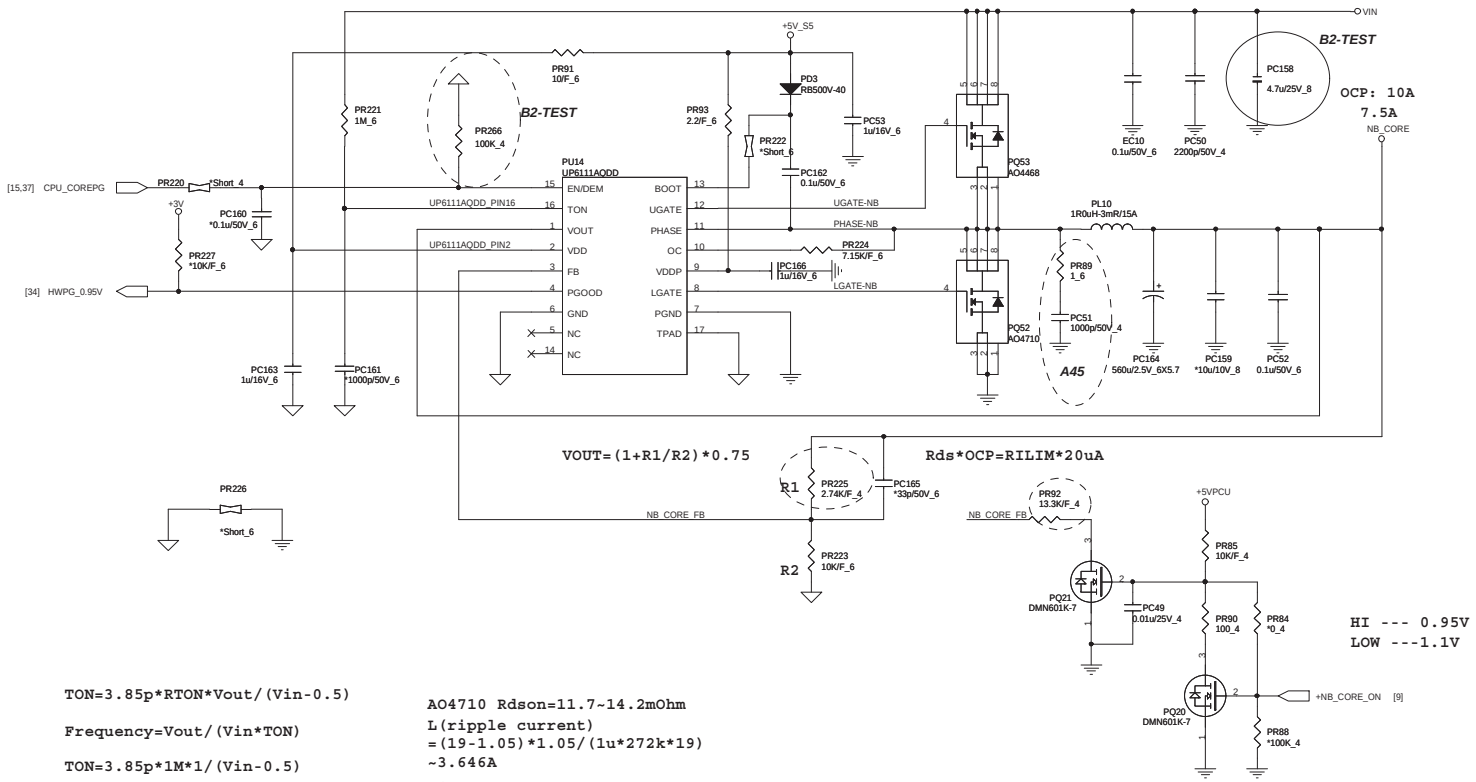
14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date: Wednesday, May 27, 2009	Sheet 38 of 49	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	NB_CORE(UP6111A)	1A
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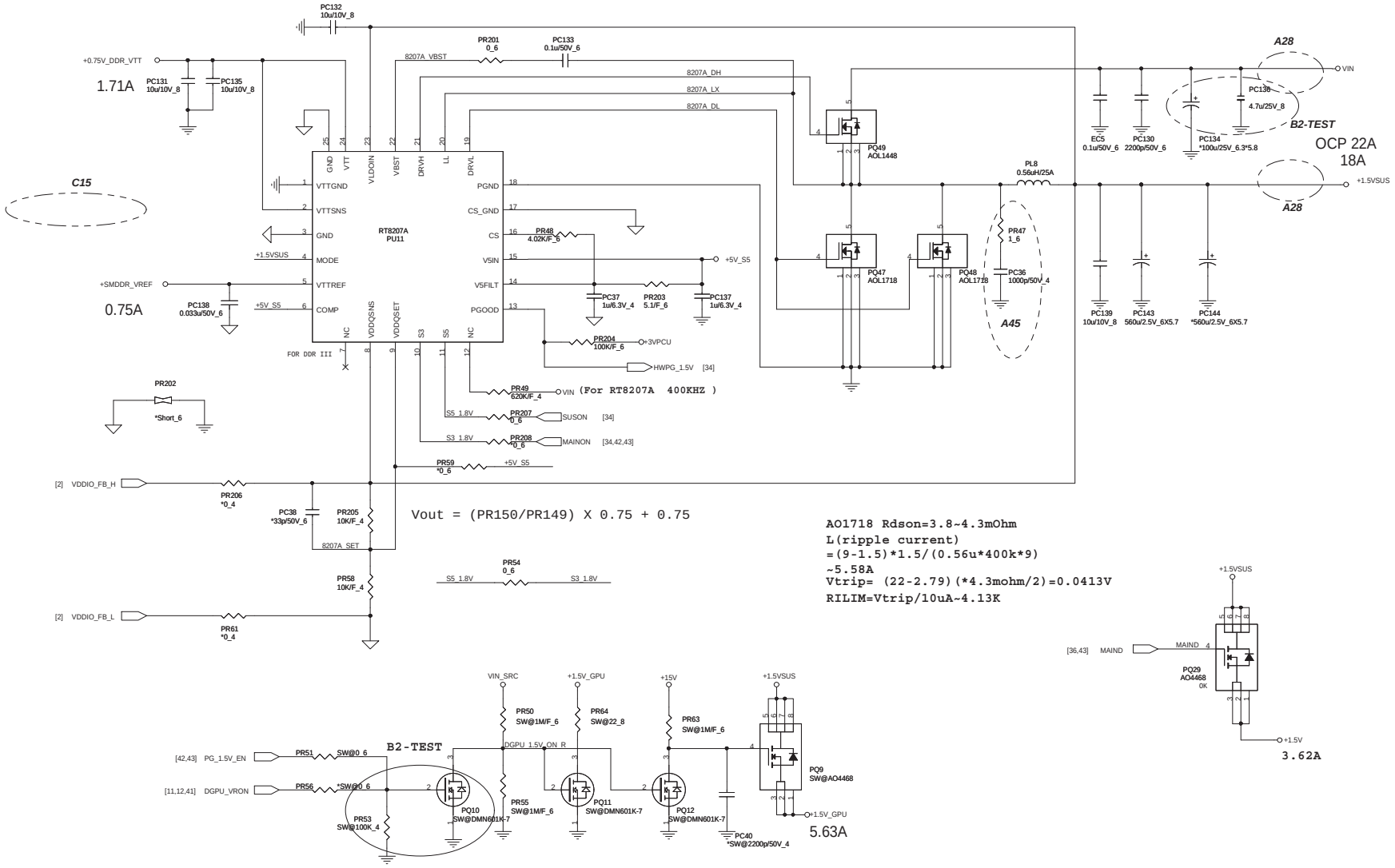
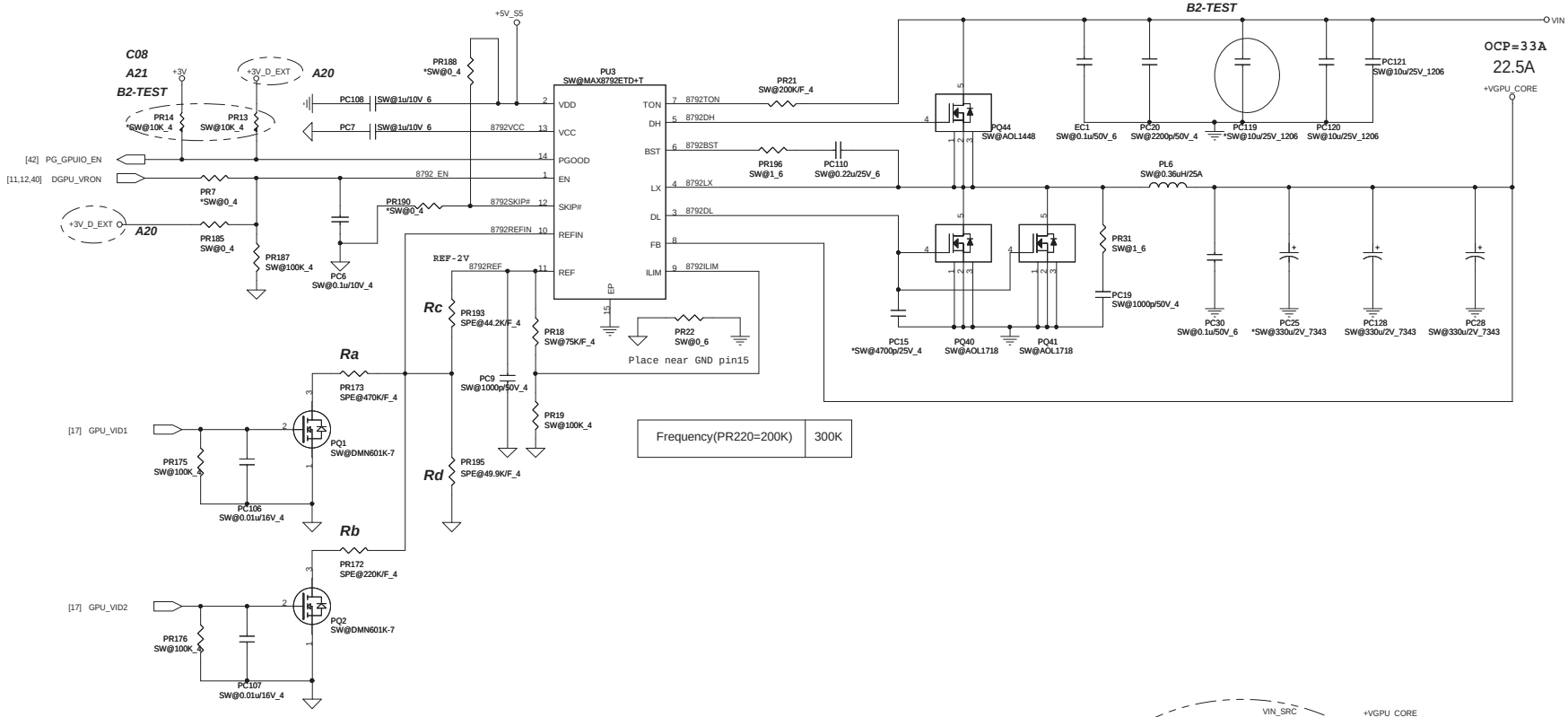
[PWM]



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Wednesday, May 27, 2009	Sheet 40 of 49	



Frequency(PR220=200K)	300K

Madison -Pro

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
470K	220K	44.2K	49.9K	2V

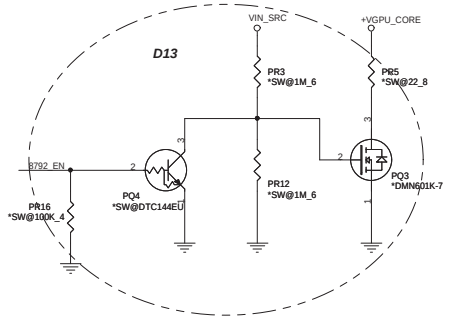
Park -XT

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
332K	130K	39.2K	49.9K	2V

A03

Rc --> 39.2K/F_4 (CS33922FB15)
Ra --> 332K/F_4 (CS43322FB15)
Rb --> 130K/F_4 (CS41302FB00)



PROJECT : ZR8
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Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
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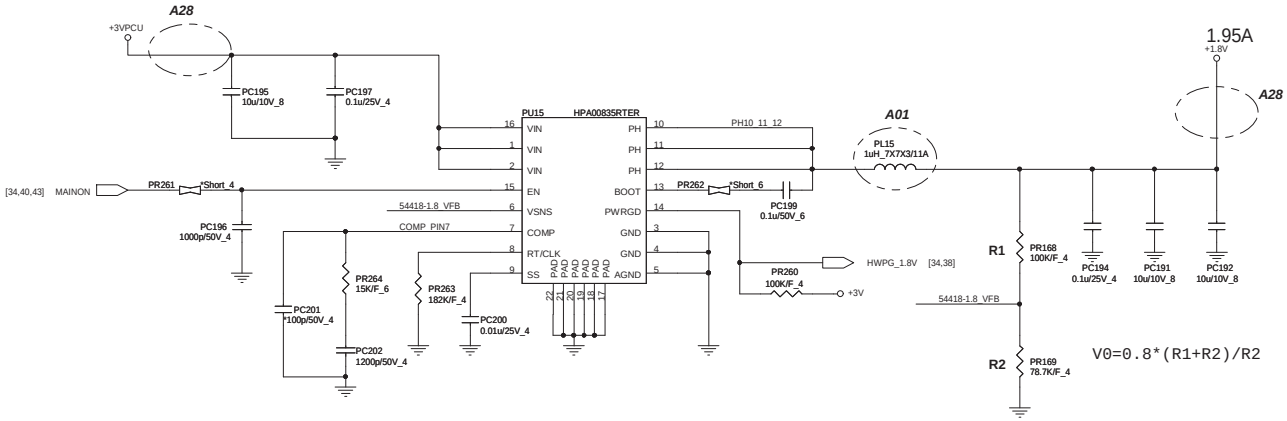

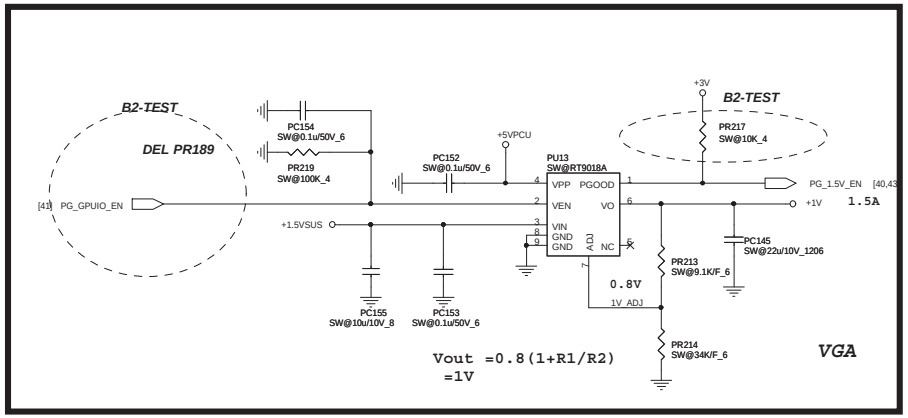

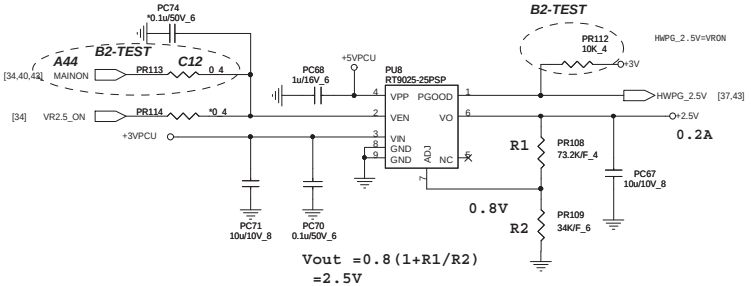

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Quanta Computer Inc.		
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	Discharge (2.5V/1.8V)	1A
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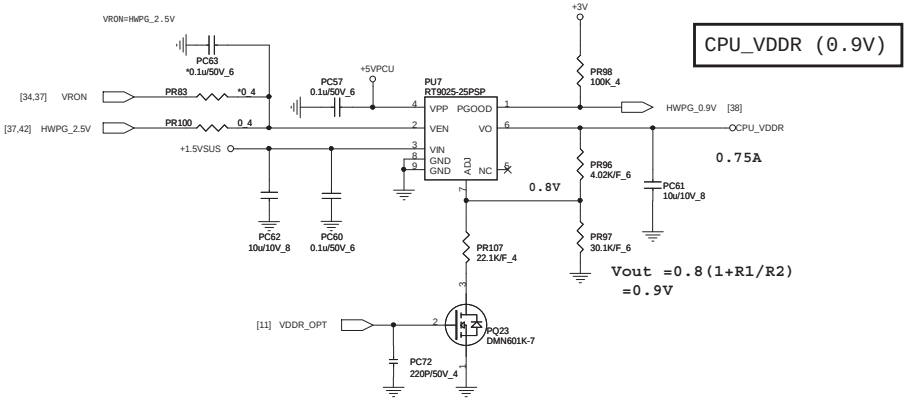

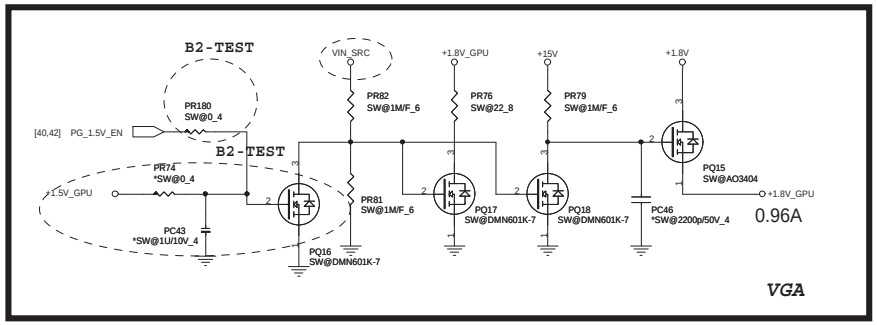

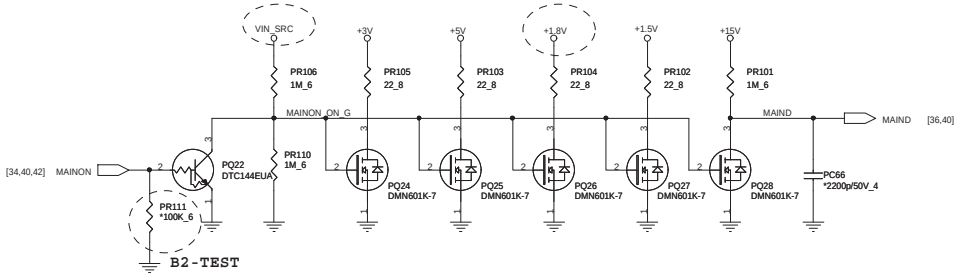

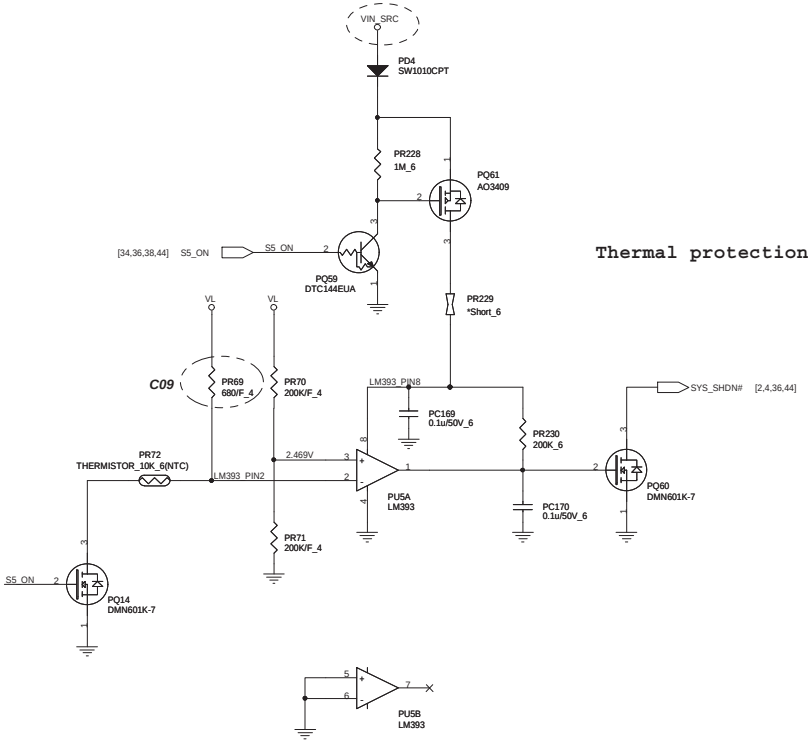

Thermal protection

For EC control thermal protection (output 3.3V)

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Quanta Computer Inc.		
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	Discharge /Thermal protection	1A
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HOLE26 *H-C276D110P2-8
HOLE21 *H-CT236B315D110P2
HOLE7 *O-ZR8-10
HOLE17 *H-C276D110P2-8
HOLE1 *H-C276D110P2-8
HOLE27 *HG-C315D110P2

CPU
HOLE11 *H-C236D142PB
HOLE12 *H-C236D142PB
HOLE15 *H-C236D142PB
HOLE16 *H-C236D142PB

HOLE3 *H-C276D110P2-8
HOLE2 *HG-C315D110P2
HOLE22 *H-C91D91N

HOLE25 * H-C276D110P2-8
HOLE19 *H-C236D161PB
HOLE13 *H-C236D161PB
HOLE18 *H-C236D161PB

HOLE14 *hg-c355d110p2
HOLE28 *hg-c394d110p2
HOLE30 *hg-c236d110p2

VGA
HOLE9 *H-C236D157P2
HOLE10 *H-TC197BC122D122P2
HOLE4 *H-C197D122PB
HOLE5 *H-TC197BC122D122P2

HOLE23 *H-C236D161PB
HOLE8 *H-C236D157P2
HOLE20 *H-C91D91N
HOLE6 * H-C236D142P2

HOLE29 *H-C157D79PT
HOLE24 *H-C157D102PT

HOLE31 *H-TC236BC161D161P2
HOLE32 *H-C276D110P2-8

B2-TEST
VIN EC52 0.1u/25V_4
VIN EC51 0.1u/25V_4

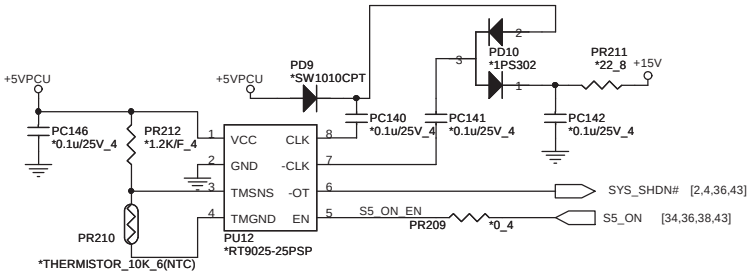
For EMI
NB_CORE EC11 *0.1u/25V_4
+VGPU_CORE EC3 *0.1u/25V_4
+5VA EC32 *0.1u/25V_4
+5VPCU EC18 *0.1u/25V_4

VIN_SRC EC26 *0.1u/25V_4 EC20 *0.1u/25V_4
+1.8V EC12 *0.1u/25V_4 EC31 *0.1u/25V_4
+3V_S5 EC21 *0.1u/10V_4
+3V_S5 EC22 *0.1u/10V_4
+3V EC6 *0.1u/10V_4
+3V EC43 *0.1u/10V_4
+3V EC42 *0.1u/10V_4
+1.1V EC8 *0.1u/25V_4 EC23 *0.1u/25V_4
+1.5VSUS EC14 *0.1u/25V_4 EC7 *0.1u/25V_4

B2-TEST
+5V EC50 0.1u/10V_4
+5V EC49 0.1u/10V_4
+5V EC48 0.1u/10V_4
+5V EC47 0.1u/10V_4
+5V EC46 0.1u/10V_4
+5V EC45 0.1u/10V_4
+5V EC44 0.1u/10V_4

+5V EC40 *0.1u/25V_4 EC30 *0.1u/25V_4 EC24 *0.1u/25V_4
+3VPCU EC28 *0.1u/25V_4 EC35 *0.1u/25V_4 EC39 *0.1u/25V_4 EC29 *0.1u/25V_4
+3V EC16 *0.1u/25V_4 EC15 *0.1u/25V_4 EC38 *0.1u/25V_4 EC36 *0.1u/25V_4 EC34 *0.1u/25V_4 EC27 *0.1u/25V_4 EC37 *0.1u/25V_4 EC33 *0.1u/25V_4

POWER TEST



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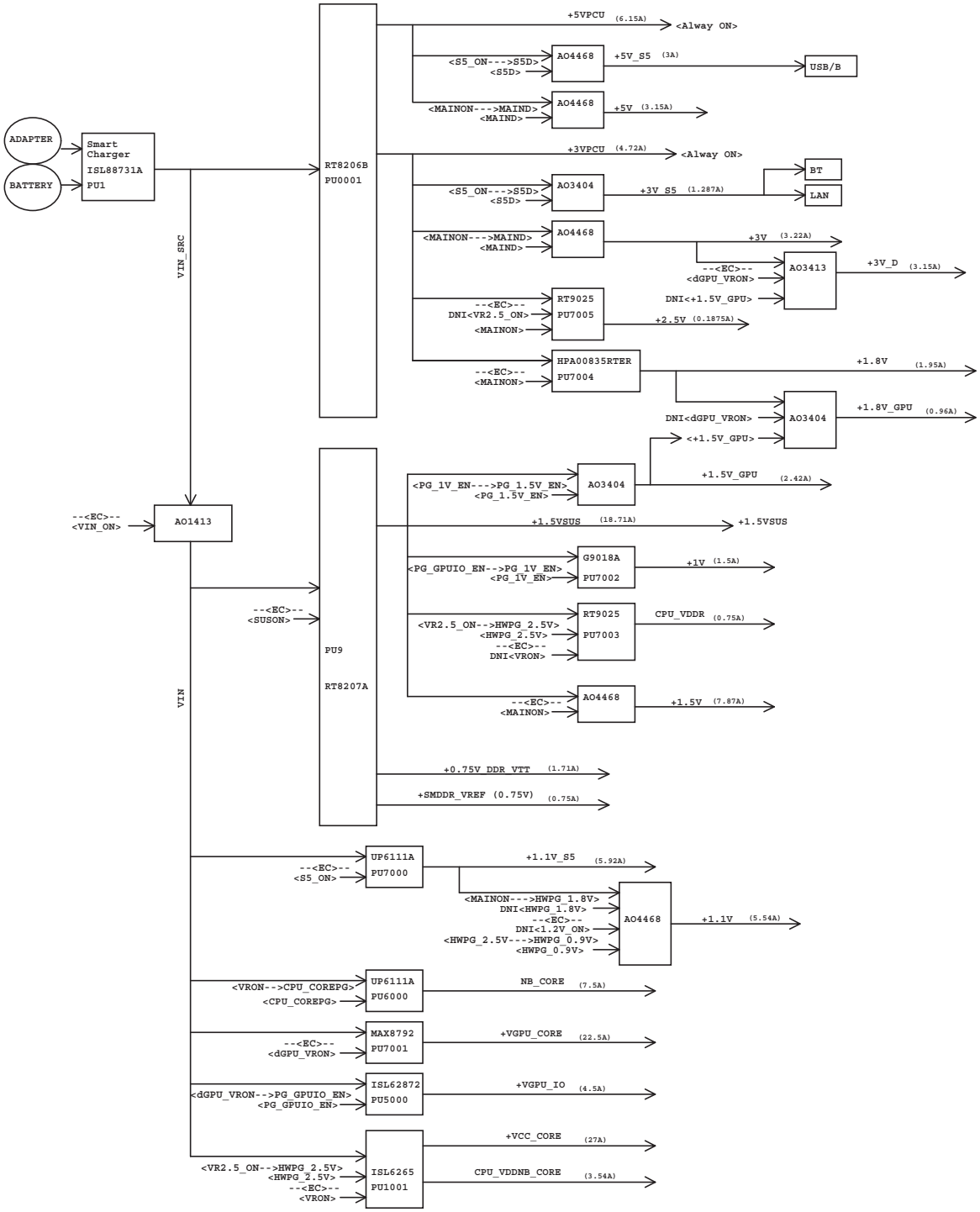
ZR8 Power tree



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	Power Tree	1A
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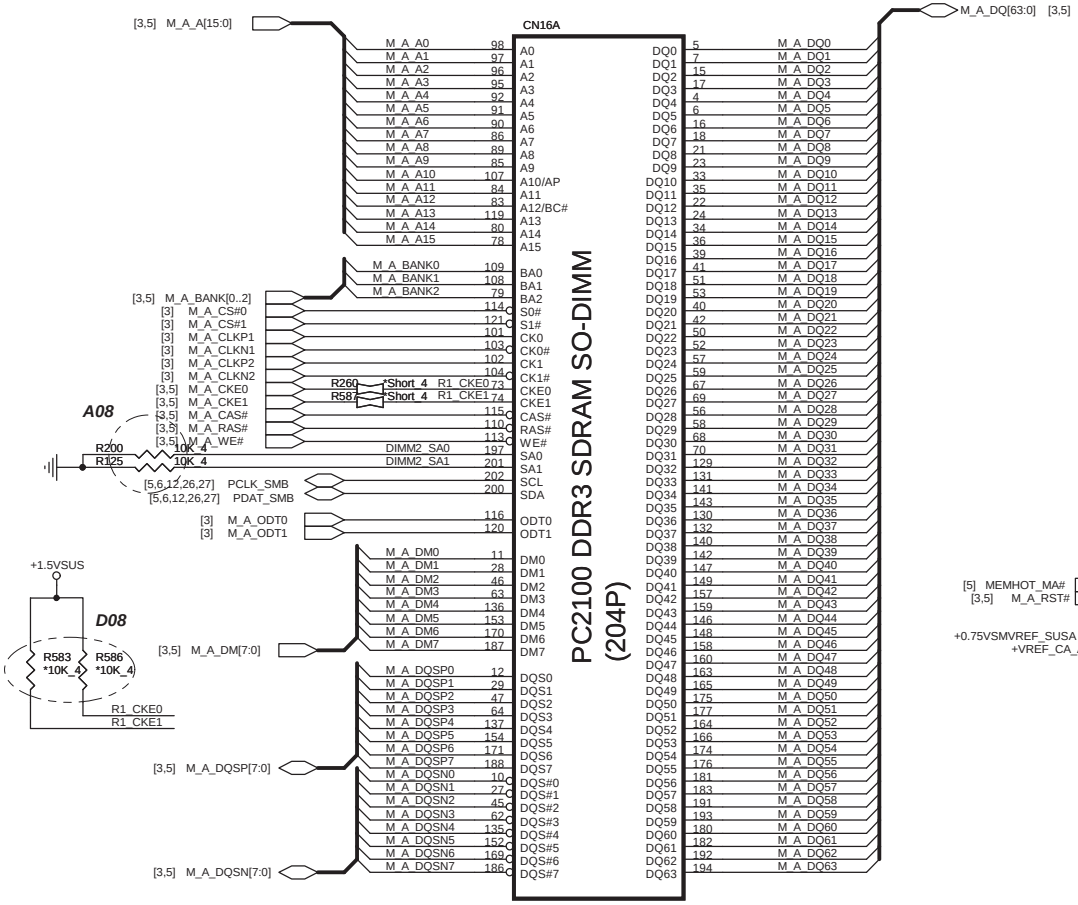
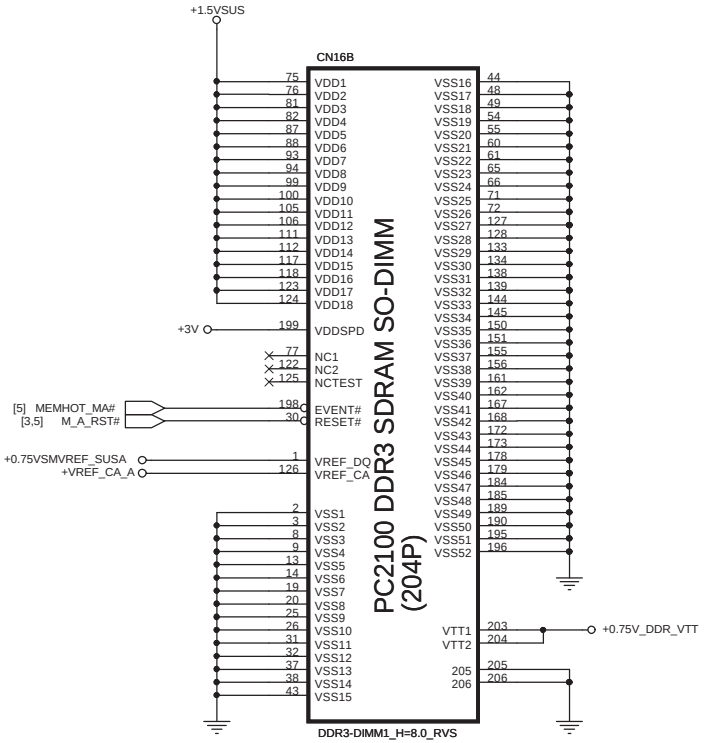
DDR3 (DDR)

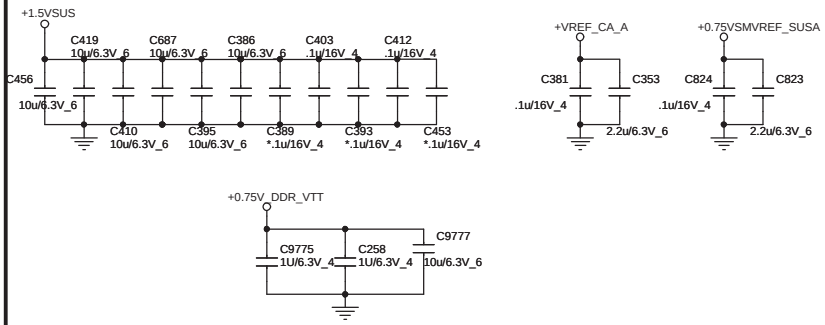




A52

2DIMM--->P/N:DGMK4000145

Place these Caps near So-Dimm0.



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-1(H=9.2)	1A
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ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009

EC / Page / Item / Description

A01 Page25/27/28/31/32/36/38/44 Change footprint , due to SMT open issue highlight.
A02 Page32 Change T/P switch P/N, due to SMT open issue highlight.
A03 Page42 Modify Madison-Pro & Park-XT VID table.
A04 Page14 Modify board ID table and R517,R304 support Side-port function.
A05 Page14 Add R528 support different Side-port VRAM type.
A06 Page44 Support CPU 45W solution.
A07 Page02 Change clock gen to no stuff, due to use internal clock source.
A08 Page06/07/48 Change SO-DIMM SMBUS address.
A09 Page08/10/11 Add Side-port function.
A10 Page10 Chane HDMI DDC CLK/DATA port.
A11 Page10 Stuff R190.
A12 Page12 Change dGPU_PWROK from GPIO1 to GPIO32.
A13 Page12 Change board ID GPIO pin.
A14 Page13 1. Stuff D19,R307,C538 and no stuff D18. 2. Change pull high power rail from +3V_D to +3V.
A15 Page16 Change R500 from 0ohm to 10k.
A16 Page12 Connect 25Mhz for GPU workaround design.
A17 Page18 Modify GPU Power-on sequence table.
A18 Page18 Remove GPU_IO VID contron pin and change GPU_CORE GPIO pin to GPIO15/20.
A19 Page19 Change R107 from 680ohm to 51 ohm and modify design of MEM_RST#. Also change R30 to no stuff.
A20 Page20/22/35/42 Reserve +3V_D_ZR8 power rail for GPU leakage issue.
A21 Page18 Reserve VGA_REQ# pin.
A22 Page25 Delete brightness switch IC control and change to 0ohm solution.
A23 Page25 Stuff R135,R144 ,due to some CRT monitor can't display.
A24 Page25 Stuff C776,C787 for EMI request.
A25 Page25/32 Change connect footprint and P/N.
A26 Page29/35 Add ODD power switch design and stuff R170.
A27 Page33 Change Q29,Q30 to no stuff.
A28 Page37/41/44 Remove jmuper.
A29 Page37 Change PC193 P/N to low highlimit, due to ME thermal door impact.
A30 Page38 Change PC179,PC180 from 22uF/25V to 100uF/25V.
A31 Page38 Change CPU_CORE enable from VRON to HWPG_2.5V.
A32 Page30 Change R538,R548 from 48ohm to 68ohm for audio performance.
A33 Page28 Change R572,R563 to short pad for debug use.
A34 Page20 Change +VGPU_IO power rail to +VGPU_CORE.
A35 Page25 Connect CN5 LCD connect shielding pin to GND for ESD issue.
A36 Page18 Change R65 to no stuff.
A37 Page22 Reserve OVERT# pull high resistor prevent noise.
A38 Page33 Add pull low 100k ohm for ODD_EJ,POWER_SAVE signal.
A39 Page36 Reserve cap for power team request.
A40 Page30 Stuff 0 ohm resistor for ESD protect use.
A41 Page02/03/10/11/15/18/20/21/27/30/32/35/36 Change bead P/N for EMI request, the reason is cost down and not STD parts.
A42 Page21 Reserve 0 ohm for PLL power use.
A43 Page38 Remove PR153 & change to 0402 package
A44 Page44 Change PR113 from 0 to 10K Ohm & Change enable source to +3V
A45 Page38/39/40/41 Stuff PR80,PR89,PR94,PR95,PR47 to 1 Ohm & PC47,PC51,PC64,PC65,PC36 of value to 1000p for EMI request
A46 Page36 Change PC111 of value to 1U/25V
A47 Page36 Change PR37 of value, from 33K to 150K
A48 Page36 Change PR35 of value, from 10K to 39K
A49 Page26 Change HDMI connector PN
A50 Page7 Change P/N for 3-DIMM H=4.0 STD
A51 Page6 Change P/N for 3-DIMM H=4.0 RVS
A52 Page48 Change P/N for 3-DIMM H=8.0 RVS
A53 Page36 Change battery connector P/N to DFHD08MR099
A54 Page26 Modify HDMI's I2C for DIS.

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	A Change List - 1	1A
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ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009
EC / Page / Item / Description

A55 Page14 Change board ID power rail from +3V_S5 to +3V.
A56 Page33/35 Modify WLAN RF_LED control design.
A57
A58 Page12 Remove R331 only for A11 version.
A59 Page12 Add U18,C533 & remove R303 for power sequence.
A60 Page14 Remove C760,C754,R507& Y7, due to it's for external clock use.
A61 Page2 Stuff R474,R486 for LAN & WLAN of REQ#.
A62 Page3/12 Stuff R424 and no stuff R286, due to CPU_PRPCHOT# is +1.5VSUS level.
A63 Page16 Change D29 package & Add D24.

Note : Change 0ohm to short pad
R276,R281,R415,R443,R445,R531,R532,R533,R534,R535,R539,R566,R174,R512,R513,R263,R437,R439,R441,R99

ZR8 Schematic EC Tracking Record B1 (For B1 TEST) Dec.09 , 2009
EC / Page / Item / Description

B01 Page21 Remove DP/TMDS Output Driver Analog Supply from port C&D. Due to it's don't to use.
B02 Page25 Stuff R48 for Discrete platform use.
B03 Page/10/25 Modify R signal pull low resistor value to 140ohm, due to keep 70 ohm trace impedance.
B04 Page33 Modify WLAN LED design and change from GPIO82 to GPIO84.
B05 Page27 Change LAN layout footprint for "SAW" new package.
B06 Page13/25 Reserve CCD USB host from for Port2, due to CCD issue.
B07 Page33 Reserve blue LED power source to 5V, due to White/Blue LED max Vf is more than Green/Orange LED.

ZR8 Schematic EC Tracking Record C (For C TEST) Jan.28 , 2010
EC / Page / Item / Description

C01 Page02/34 Remove "CPU_THERMTRIP#" control from SB820, due to BIOS don't support this function. Add another "SYS_SHDN#" for H/W shutdown function and add HWPG shutdown design.
C02 Page04 No stuff Q21,D14,R255 for thermal sensor Alert fnction and change to EC or H/W shutdown function.
C03 Page09 Add 1uF for monitor test noise issue.
C04 Page12 Add 0ohm to separate VGA_REQ function, due to it's don't support the function and cause by leakage current concern.
C05 Page24 Modify VGA note text for R signal impedance control.
C06 Page24 Add brightness switch control by iGPU switch mode. Due to BIOS for C test already support.
C07 Page29 Reserve EAPD# audio design for "Bo" sound.
C08 Page41 Change PG_GPUIO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue.
C09 Page43 Change PR69 FROM 1.2K to 680ohm , the reason is for SDA high temperature (40 degree/20% humidity) auto shutdown issue.
C10 Page27 Short LPC signal for debug card use.
C11 Page29 Change R538,R548 from 56ohm to 68ohm for audio performance test FSOV spec requirement.
C12 Page42 Change PR113 from 10k to 0ohm.
C13 Page35 Change EC54,EC55 to stuff for ISN issue.
C14 Page21 Modify DDR3 Memory Aperture size table.
C15 Page03/40 Reserve VDDR_SENSE signal to controller IC.
C16 Page27 Change RP32 to no stuff.
C17 Page04 Modify CPU thermal control design from EC or BIOS control and change U16,R254 to no stuff ,Q17,Q18,Q19 to stuff.
C18 Page03 No stuff R189.

Note : Change 0ohm to short pad
R124,R121,R174,L31,L37,L35,R136,R115,R169,R325,R315,R295,R292,R278,R31,R90,R21,R112,R24,R25,R270,R530,R99,R478,R512,R513,R514,R326,R269,R268,R265,R266,R610,PR73,PR220,PR261
,PR229

ZR8 Schematic EC Tracking Record A (For Ramp) Feb.25 , 2010
EC / Page / Item / Description

D01 Page03 Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC.
D02 Page15 Modify text note.
D03 Page12 Change "GBE_COL" ,"GBE_CRS" ,"GBE_RXERR" to GND follow SCL V1.04 version.
D04 Page14 Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version.
D05 Page04 No stuff R267,C450,C344.
D06 Page09 Delete R149,R152 layout pad.
D07 Page36 No stuff PD12 and add PR181, change PR257 from 1k to 390k. The purpose is for panasonic battery low power protect issue.
D08 Page05/46 No stuff R584,R259,R583,R586 for CKE signal.
D09 Page32 Change LED current sense resistor value for LED light measure requirement. (Follow ZR7B)
D10 Page21 Modify VRAM table.
D11 Page05/06 Change R123,R122,Q10,R202,R195,Q14 to no stuff, due to S1g4 don't support MEMHOT function.
D12 Page02 Reserve prochot# for FAN control.
D13 Page41 No stuff PR16,PQ4,PR3,PR12,PR5,PQ3. Due to MAX8792 had integrate discharge design.
D14 Page37 Change some component to no stuff, dut to for S1g4 use the same VDD power don't need to compensation difference voltage.

Note : Change 0ohm to hort pad.
R203,117,R585,R588,R260,R587,PR1,PR2,PR33,PR241,PR147,PR146,PR160,PR256,PR133,PR233,PR152,PR155,PR128,PR142,PR143,PR144,PR145,PR130,PR131,PR115,PR120,PR77,PR226,PR222,PR202,PR262.

	PROJECT : ZR8 Quanta Computer Inc.	
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