

WWW.AliSaler.Com
MODEL NAME : QCL00_QCL20

PCB NO : LA-8241P

BOM P/N : 4619GP31L21 Inspiron DIS
4619GQ31L21 Inspiron UMA
4619GP31L01 Vostro DIS
4619GQ31L01 Vostro UMA

Dell / Compal Confidential

Schematic Document

Inspron A5 & Vostro 3560 (Intel Chief River)
Ivy Bridge (rPGA) + Panther Point (mainstream)

Discrete AMD Thames-XT

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB930@ : ENE KB930 Implemented

KB9012@ : ENE KB9012 Implemented

EXP@ : Express Card Implemented

FFS@ : Only for Free Fall Sensor

VOS@ : Only for Vostro

INS@ : Only for Inspiron

UMA@ : Only for UMA

GCLK@ : Green CLK implemented

AMP@ : External Amplifier implemented

KBBL@ : Keyboard Back Light implemented

2012-02-01

Rev: 1.0

X76@ : VRAM Group

CH@ : Chelsea M2

SE@ : Seymour M2

TH@ : Thames-XT

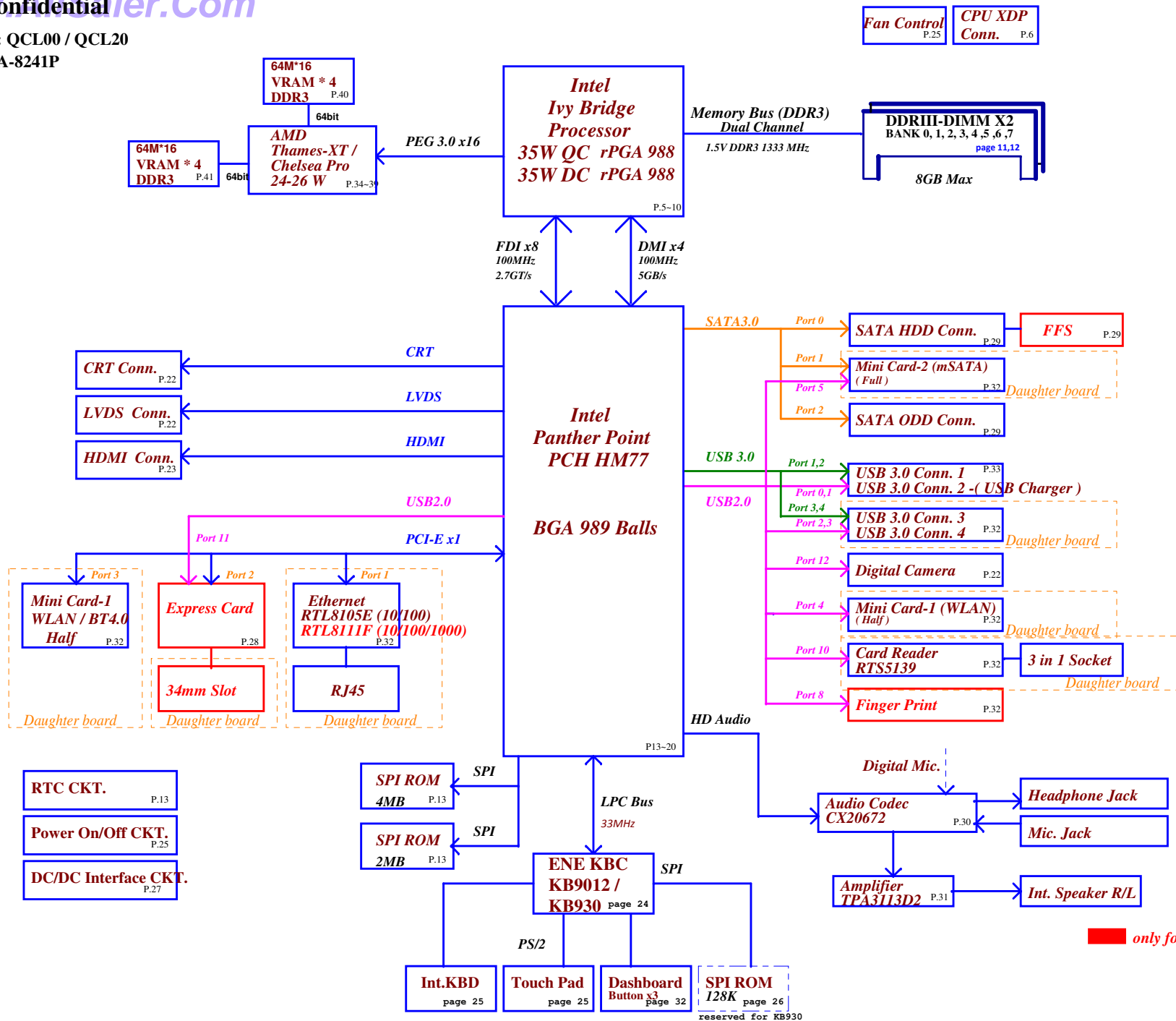
DIS@ : Only for Discrete

MB Type	BOM P/N	Config

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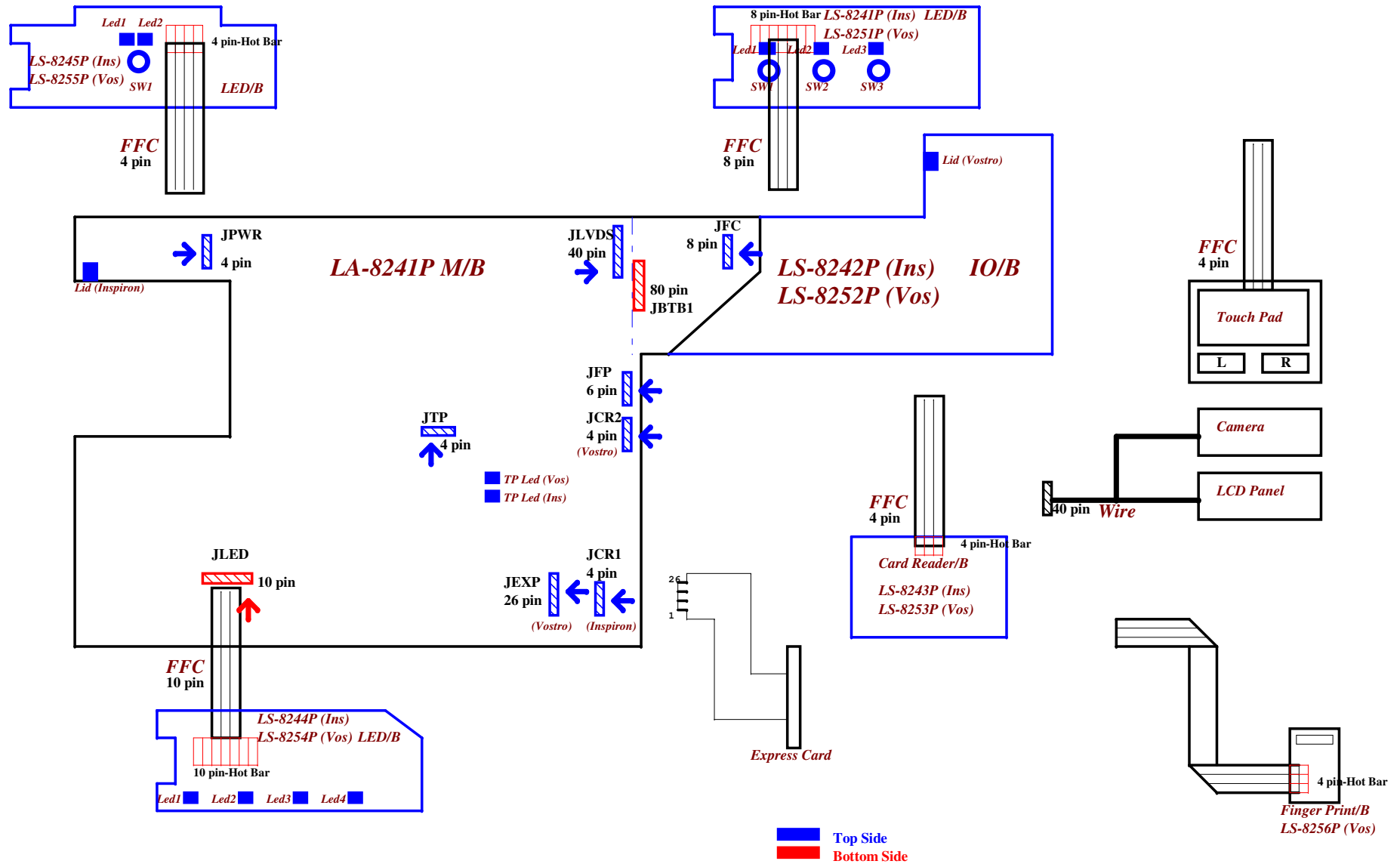
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Project Code : QCL00 / QCL20
File Name : LA-8241P



only for Vostro 3560

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		Block Diagram
		Document Number
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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	

CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-1 WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	Express Card	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.1
2	0.2
3	0.2
4	0.3
5	0.3
6	1.0
7	1.0



Link

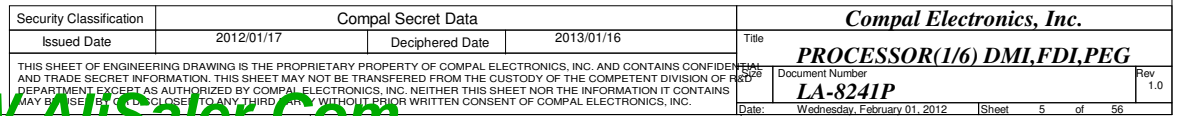
USB PORT#	DESTINATION
0	USB conn.1
1	USB conn.2 - Power Share
2	USB conn.3
3	USB conn.4
4	MINI CARD-1 (WLAN)
5	NC
6	NC
7	NC
8	Finger Print
9	NC
10	Card Reader
11	Express Card
12	Camera
13	NC

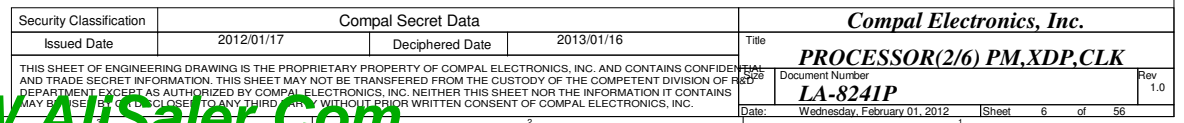
SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

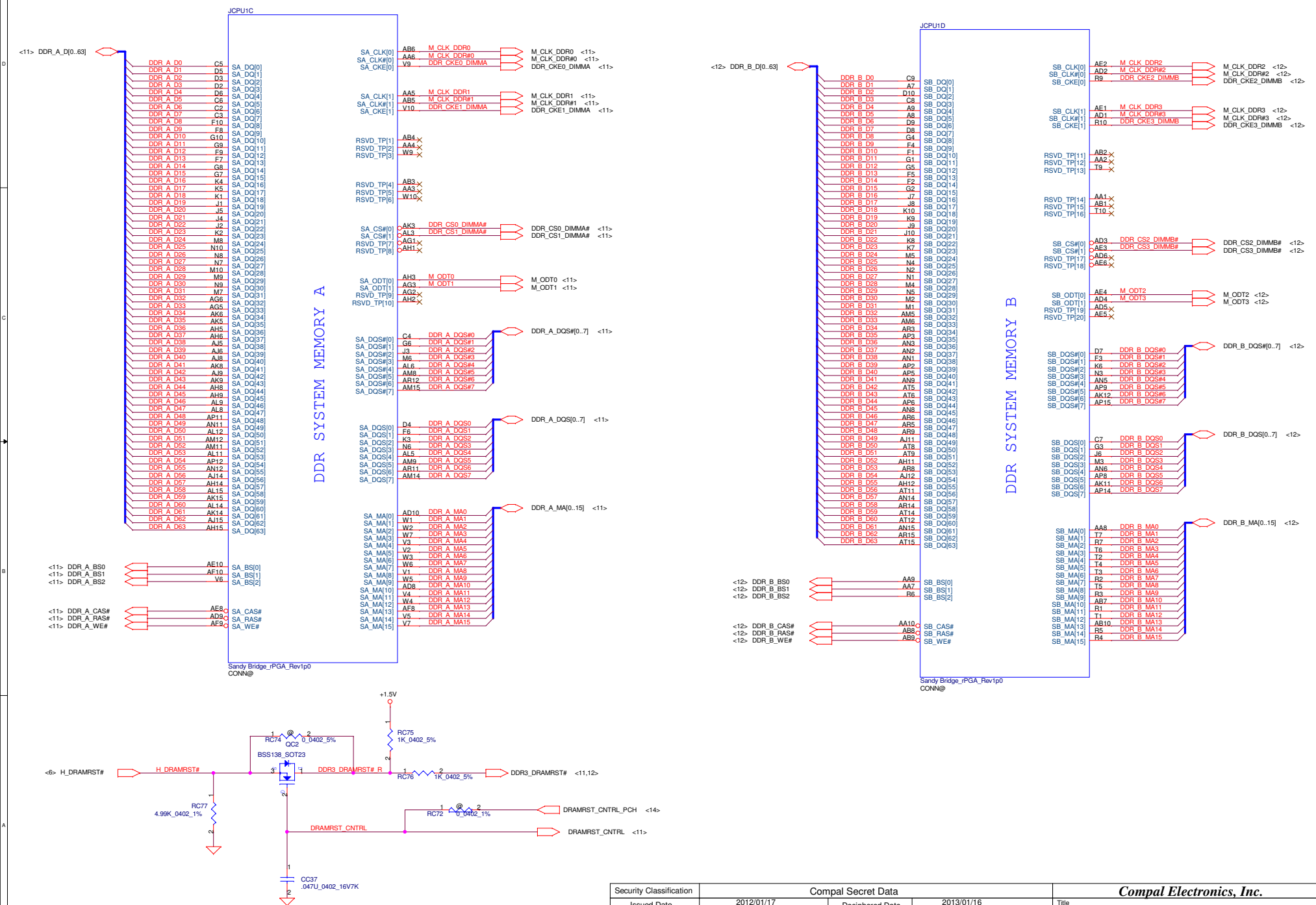
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-1 (WLAN)
Lane 3	Express Card
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

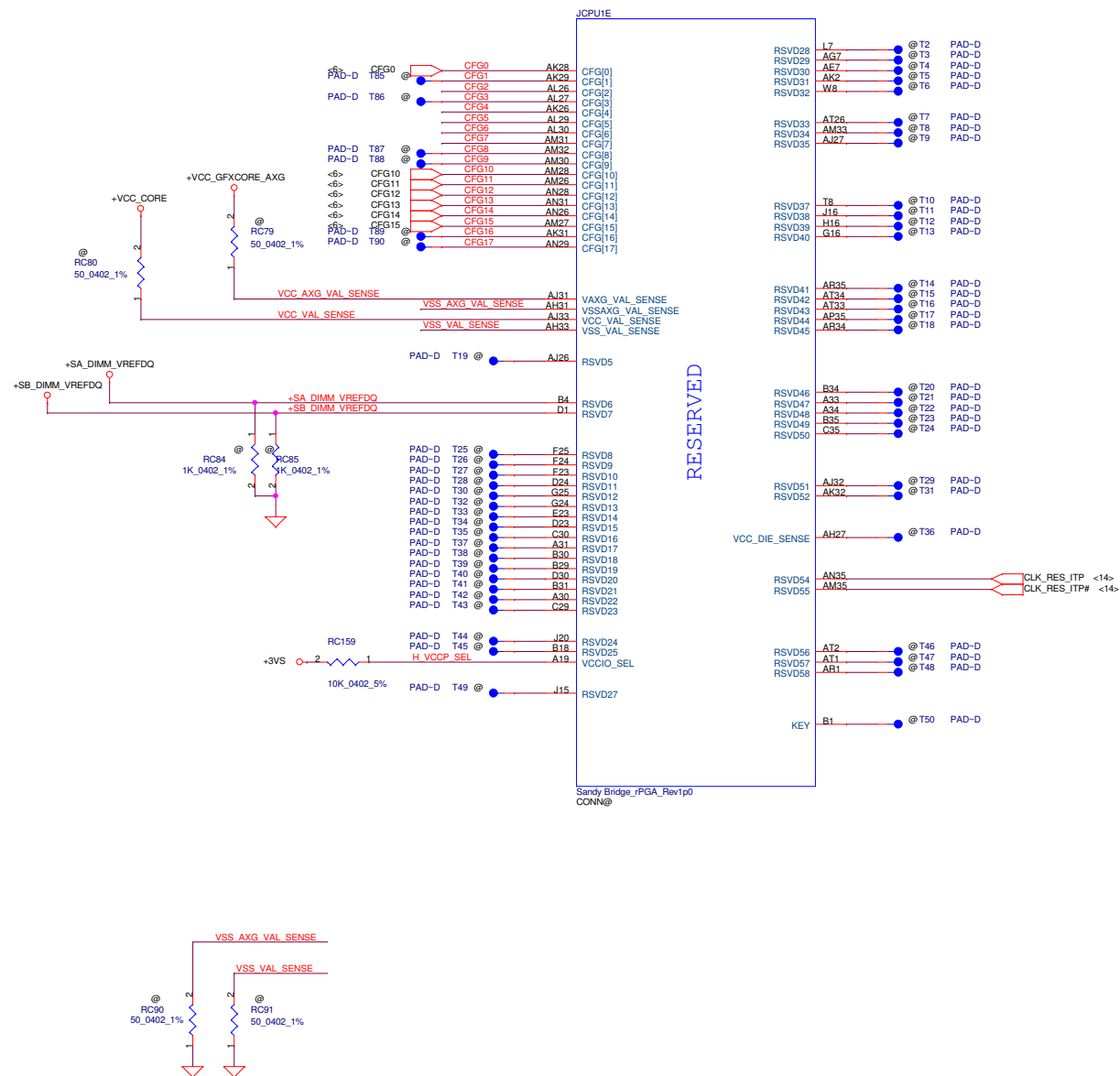
Symbol Note :

 : means Digital Ground
 : means Analog Ground

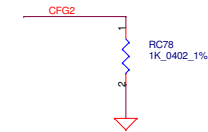




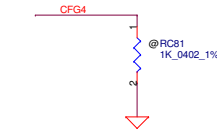




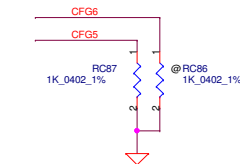
CFG Straps for Processor



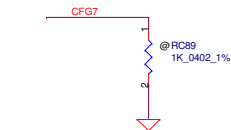
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition *0:Lane Reversed



Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

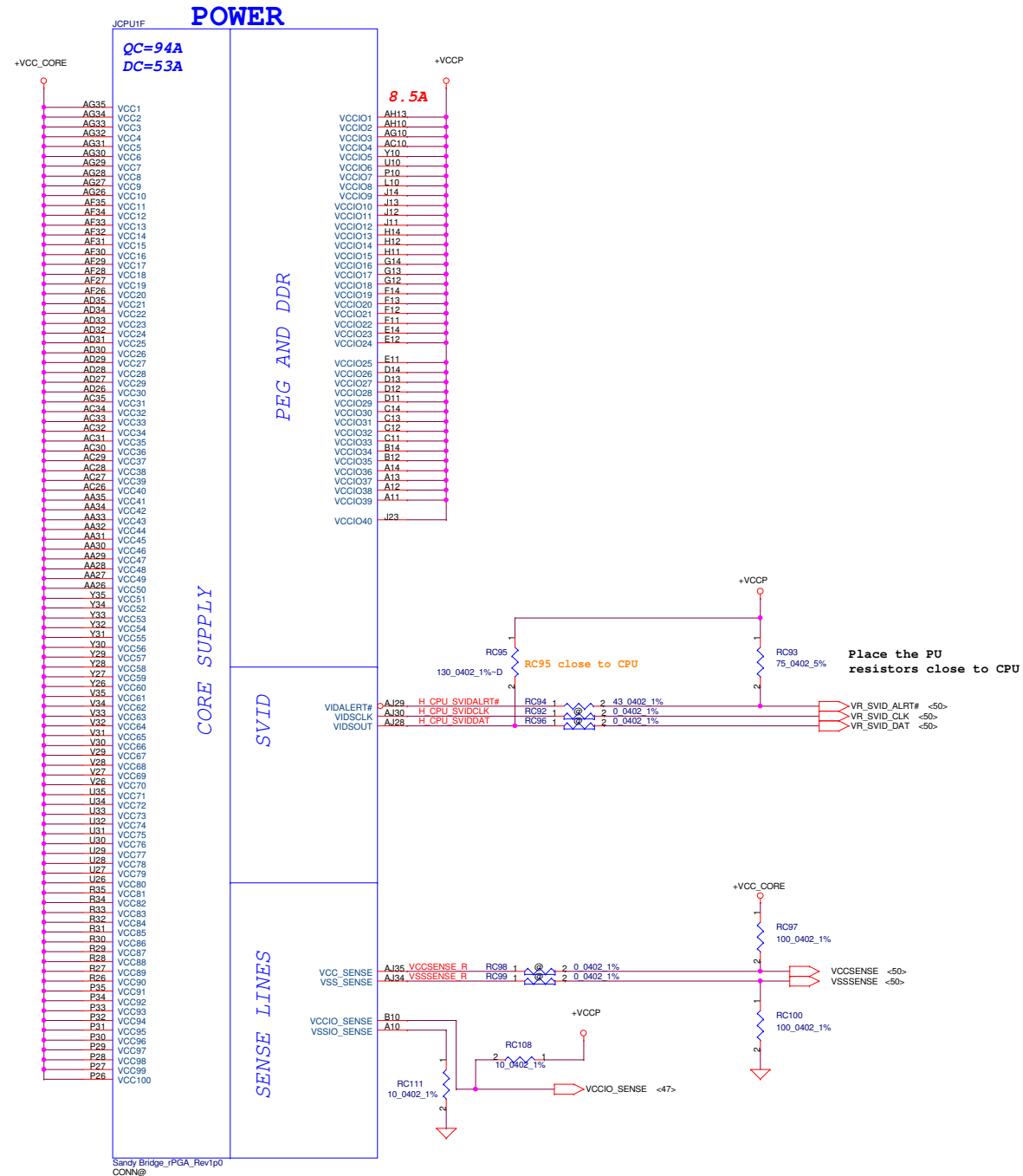


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *0x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

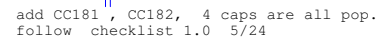


PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

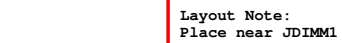
INTEL 12/28 recomment
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1



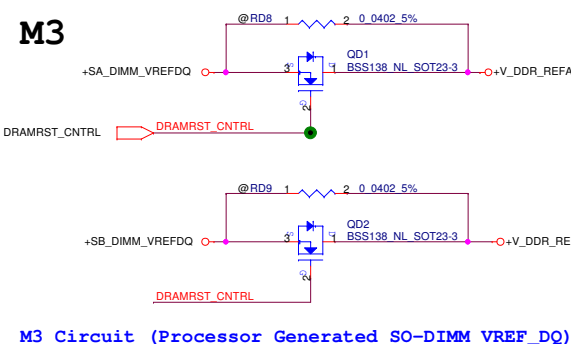
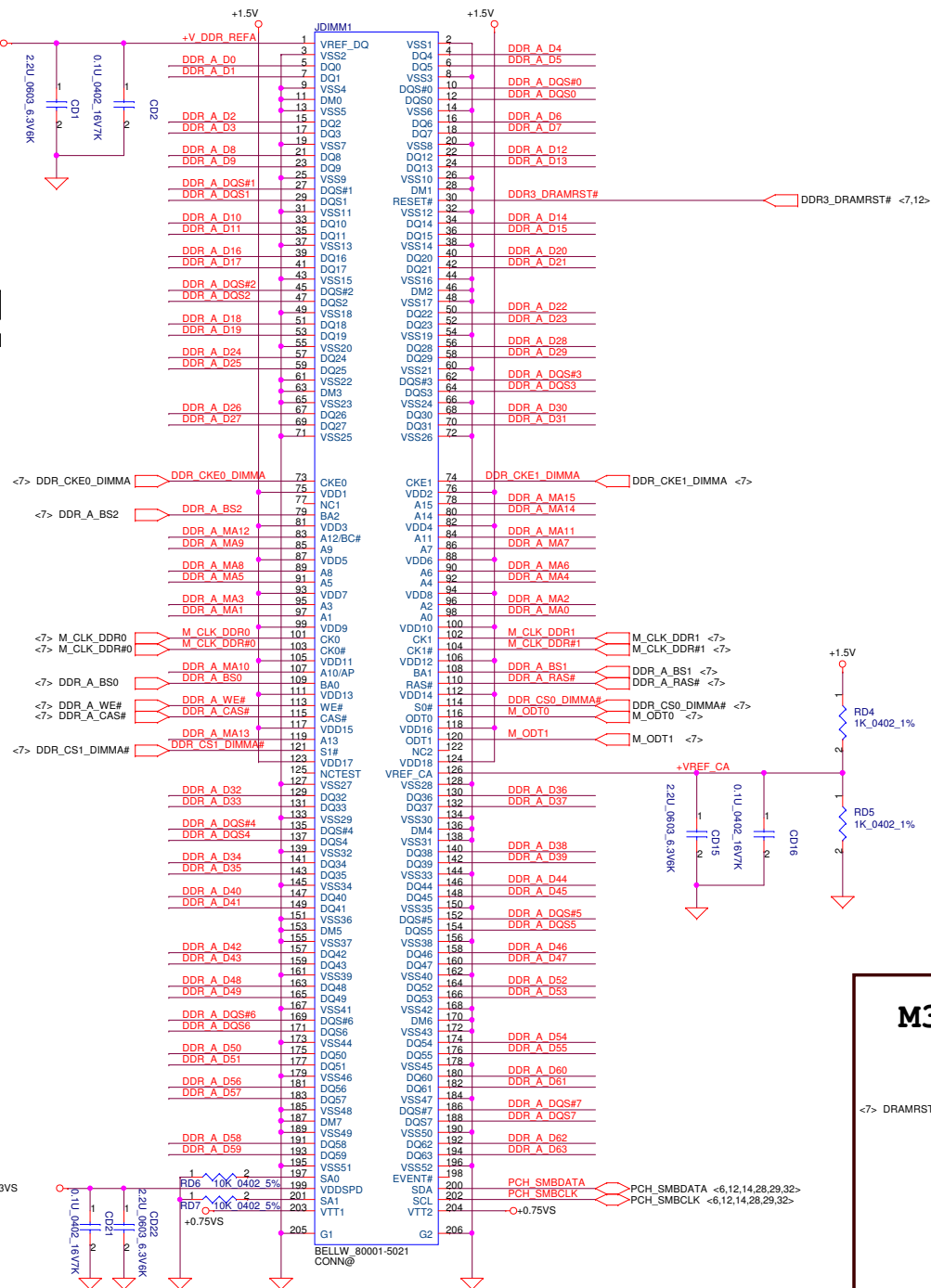
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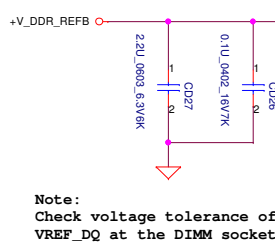
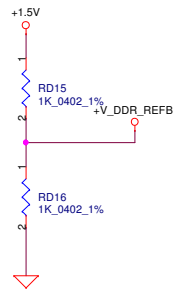


Layout Note:
Place near JDIMM1.203,204



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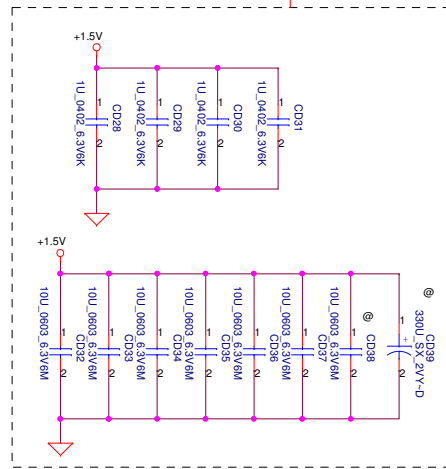
<7> DDR_B_DQS#[0..7]
<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_MA[0..15]



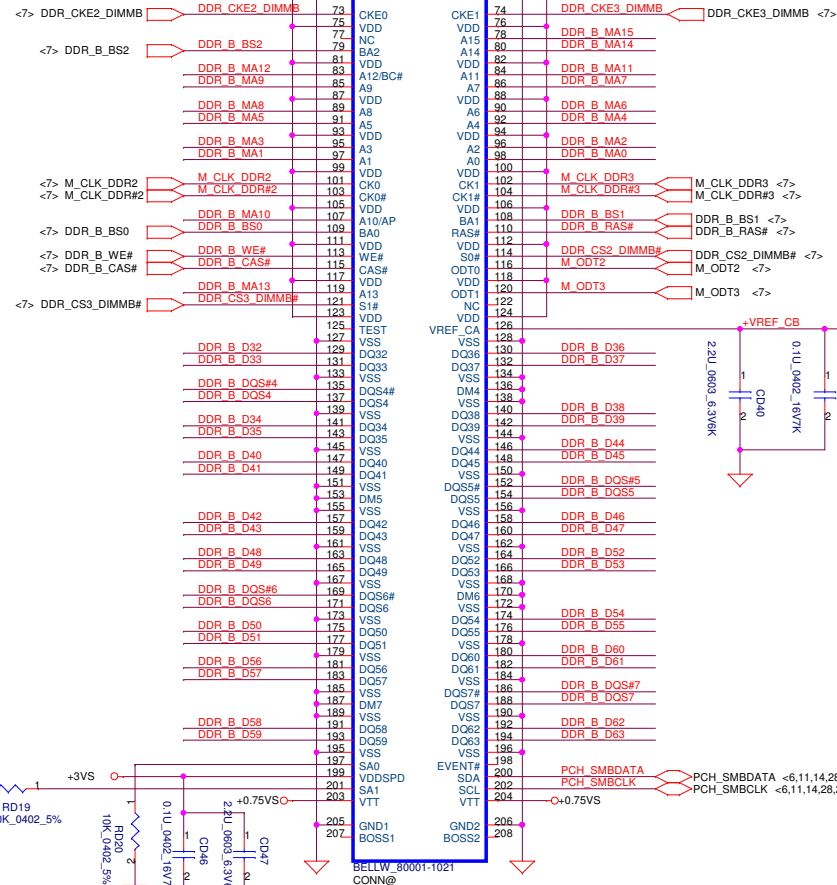
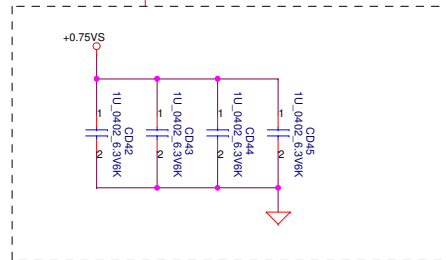
Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

All VREF traces should
have 10 mil trace width

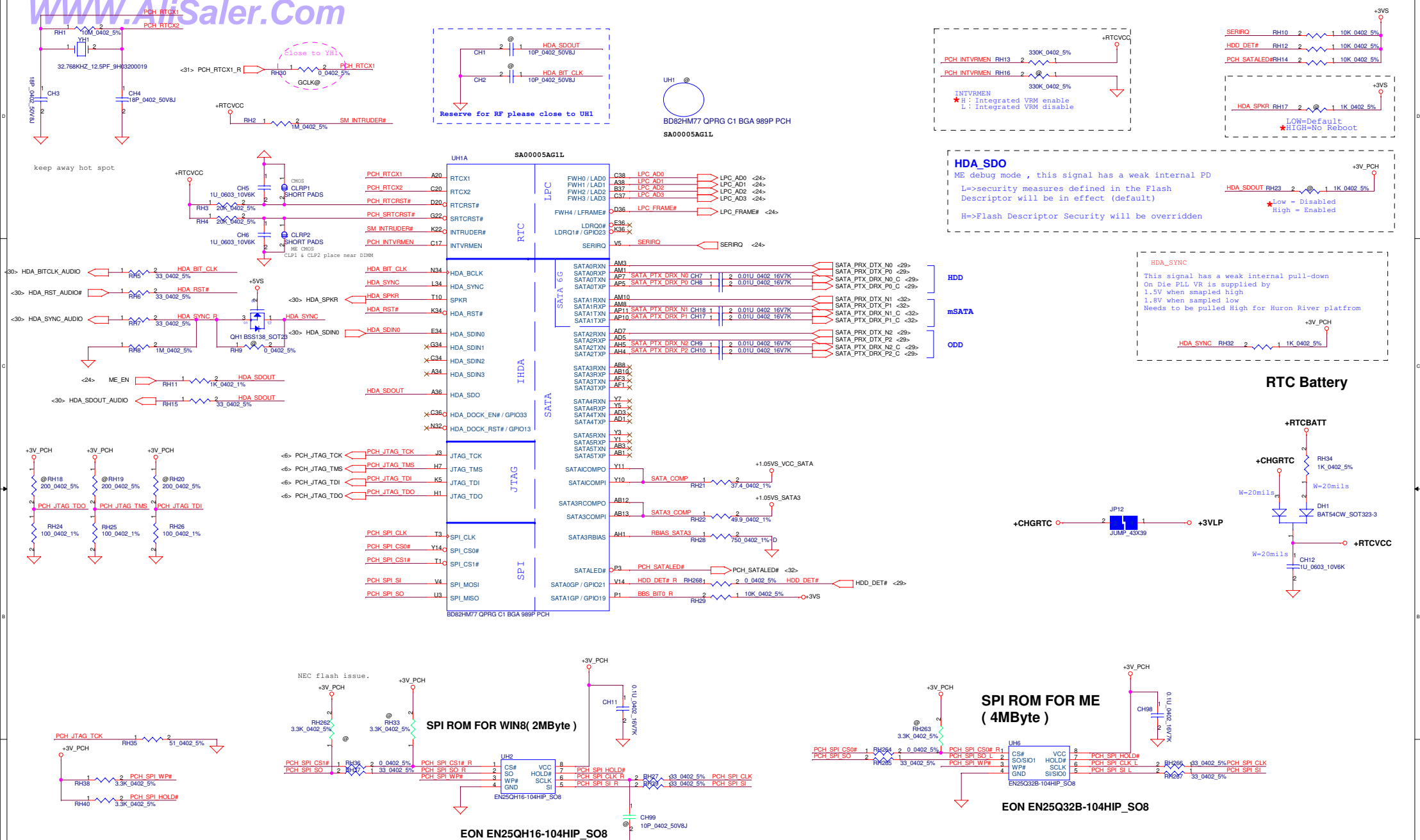
Layout Note:
Place near JDIMMB



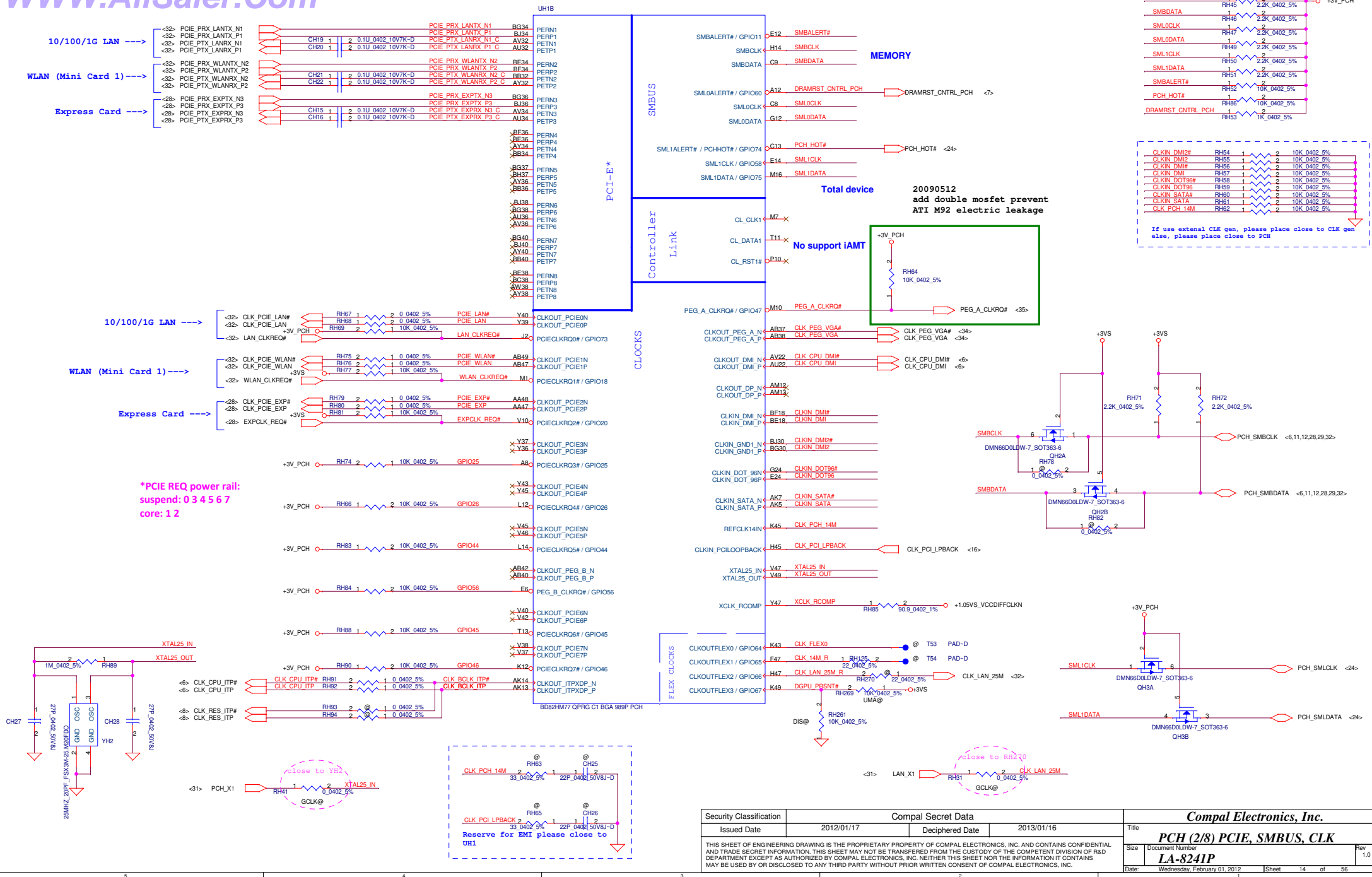
Layout Note:
Place near JDIMMB. 203, 204

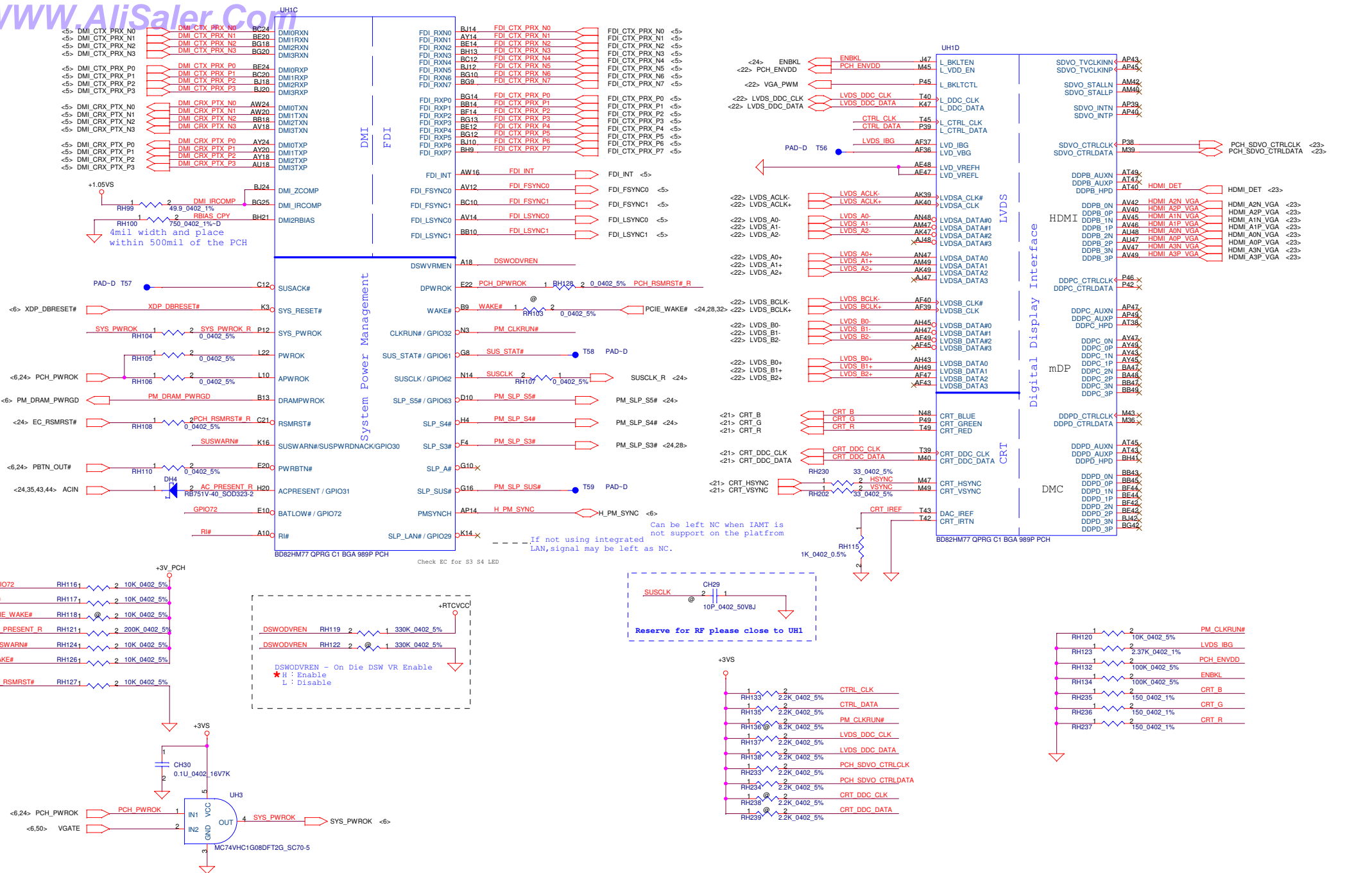


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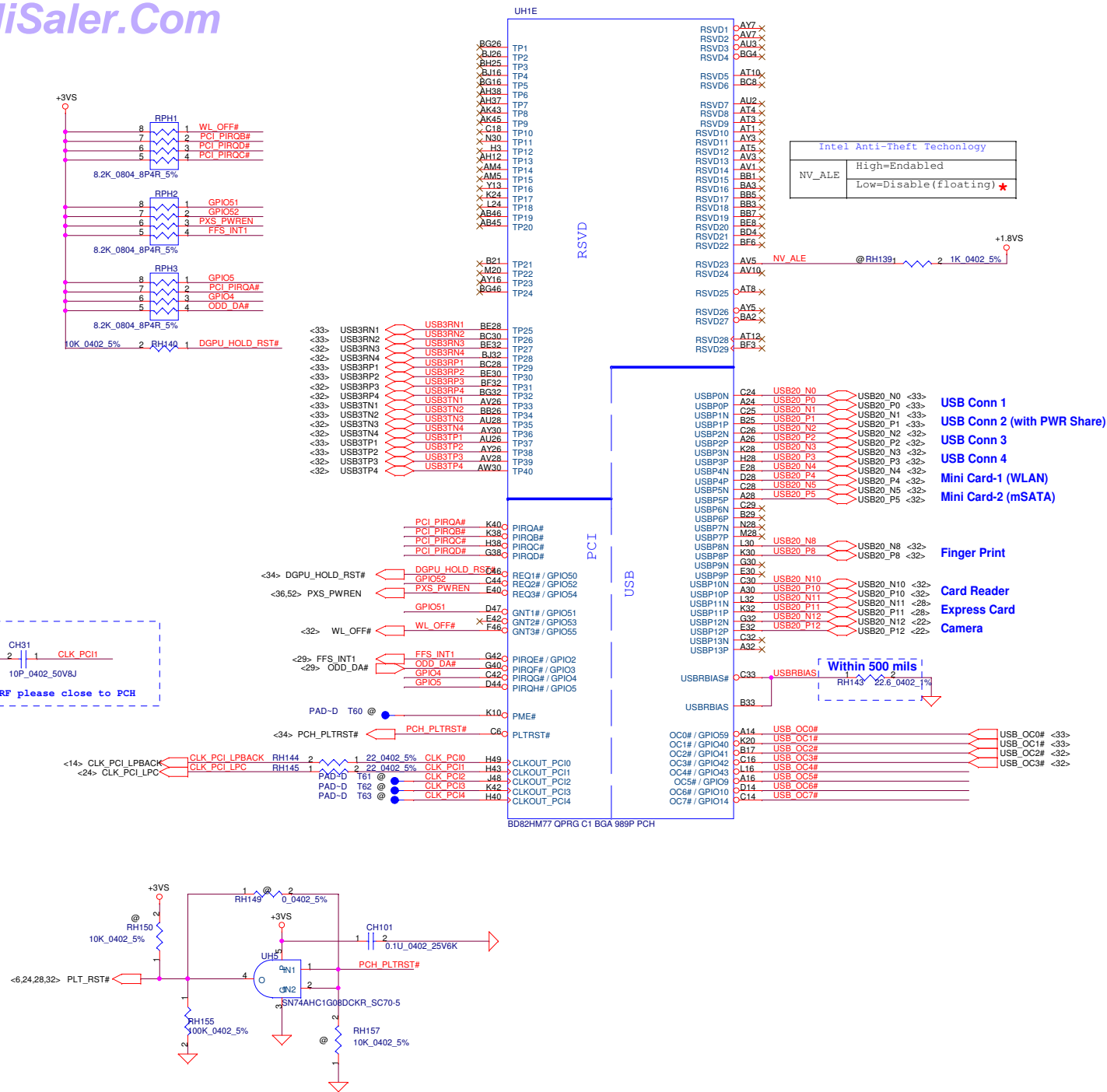


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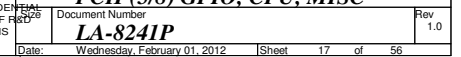


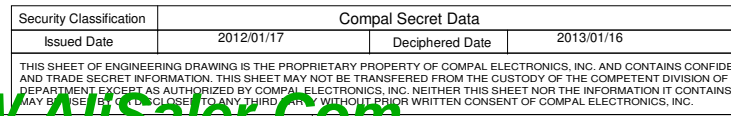


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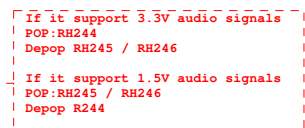


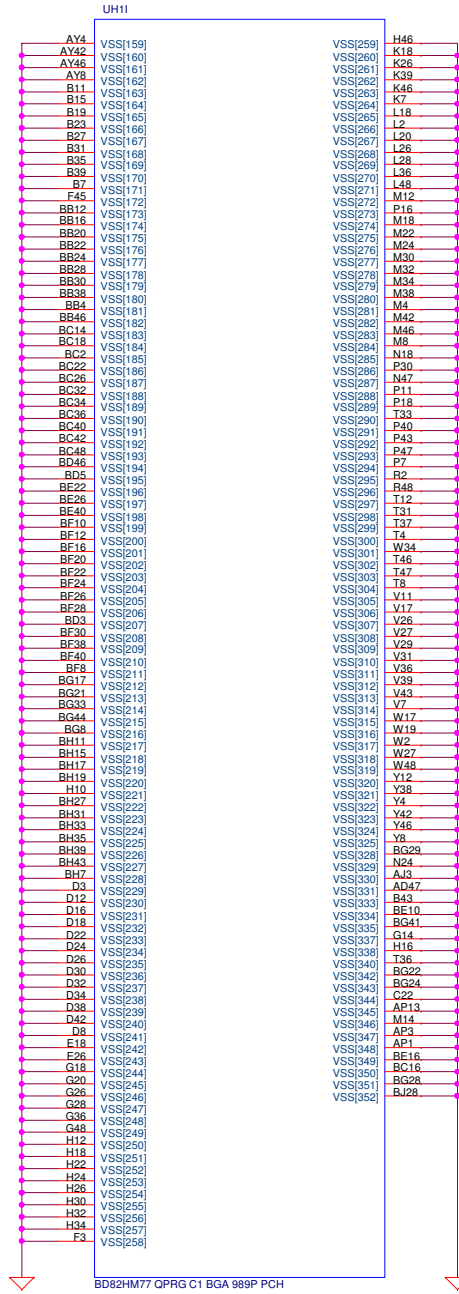
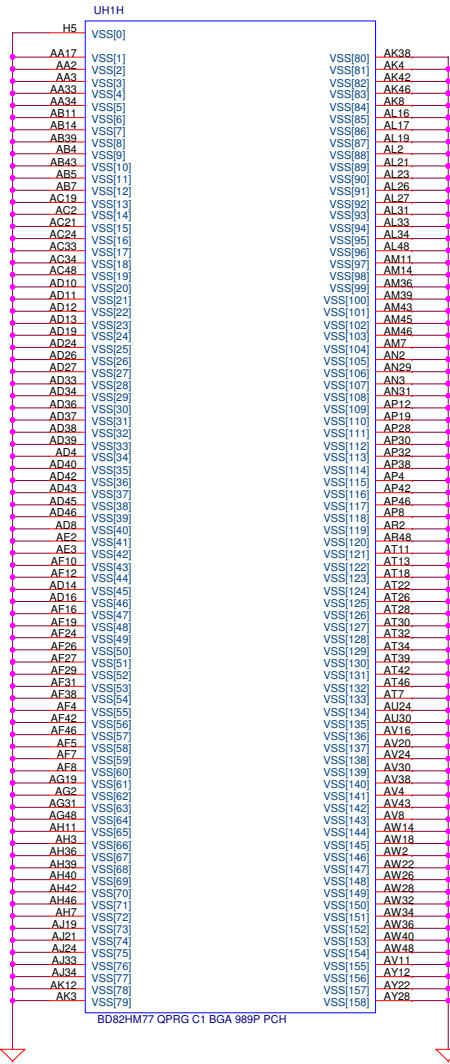
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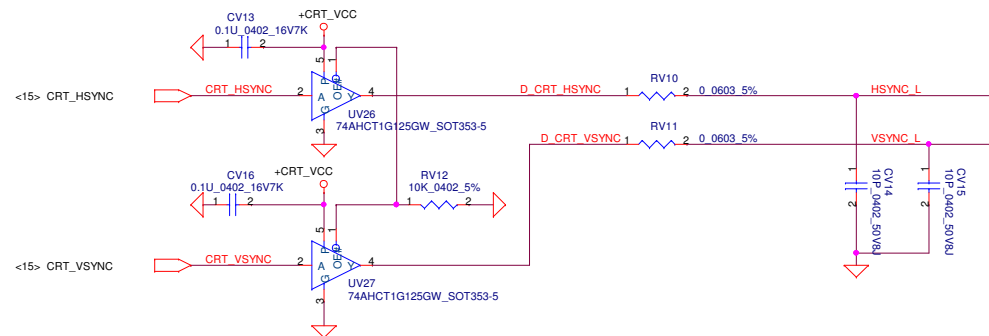
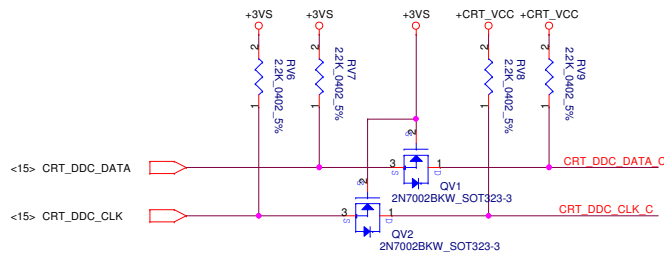
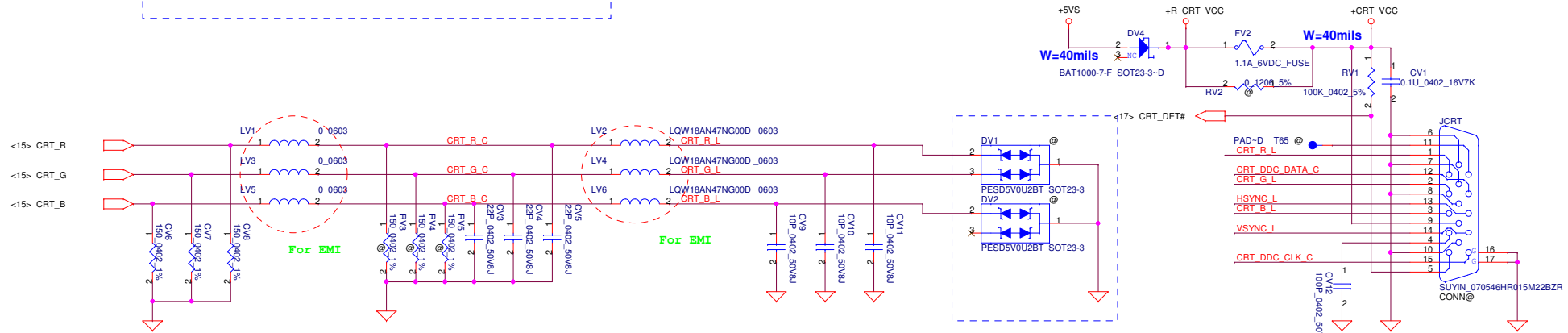
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Title			
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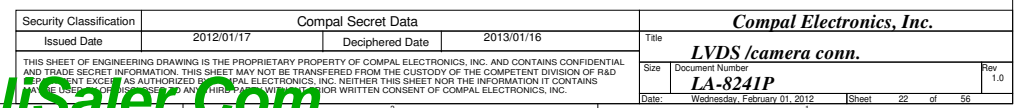
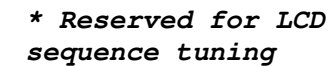
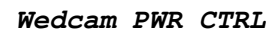
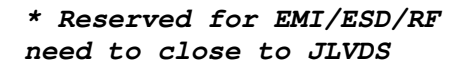
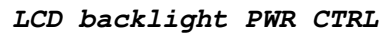


From VGA for debug CRT

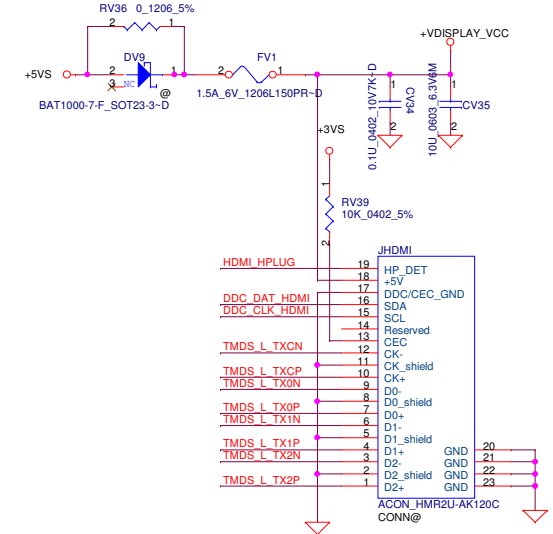
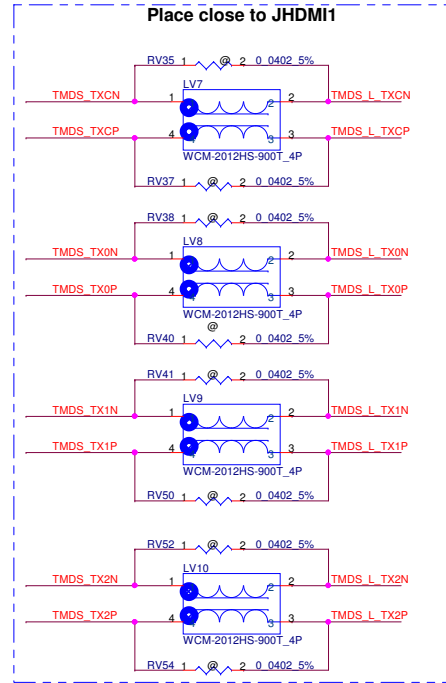
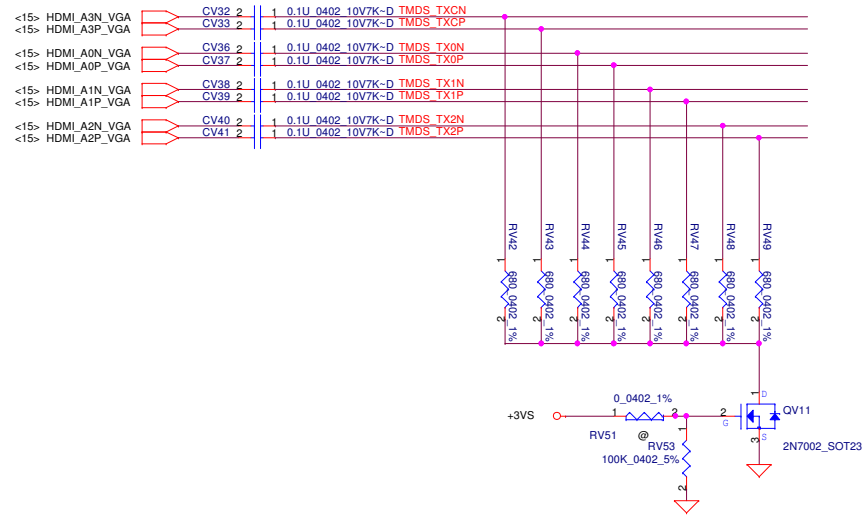
<35> VGA_CRT_R	VGA CRT R RV2231	0.0402 5%	CRT R
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<35> VGA_CRT_B	VGA CRT B RV2251	0.0402 5%	CRT B
<35> VGA_CRT_HSYNC	VGA CRT HSYNC RV2261	0.0402 5%	CRT HSYNC
<35> VGA_CRT_VSYNC	VGA CRT VSYNC RV2271	0.0402 5%	CRT VSYNC
<35> VGA_CRT_CLK	VGA CRT CLK RV2281	0.0402 5%	CRT DDC CLK
<35> VGA_CRT_DATA	VGA CRT DAT RV2291	0.0402 5%	CRT DDC DATA



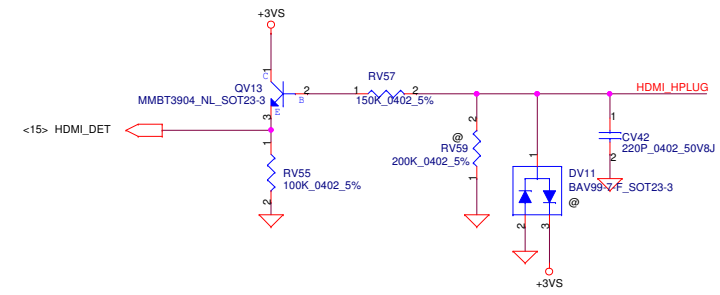
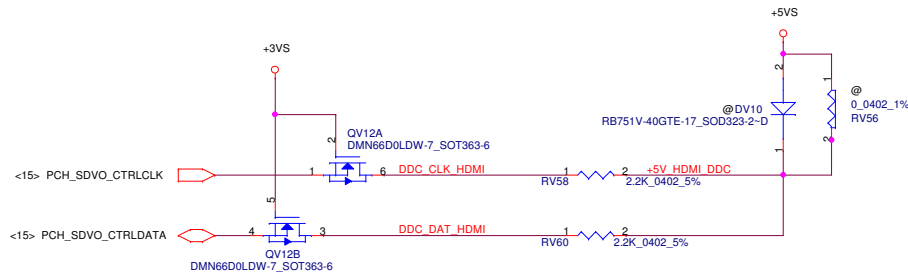
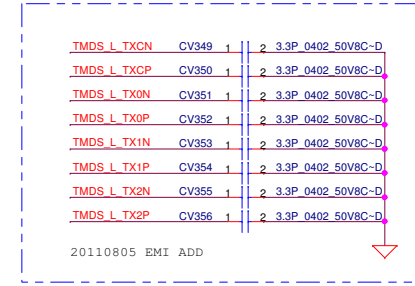
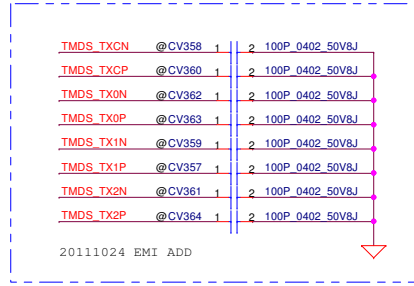
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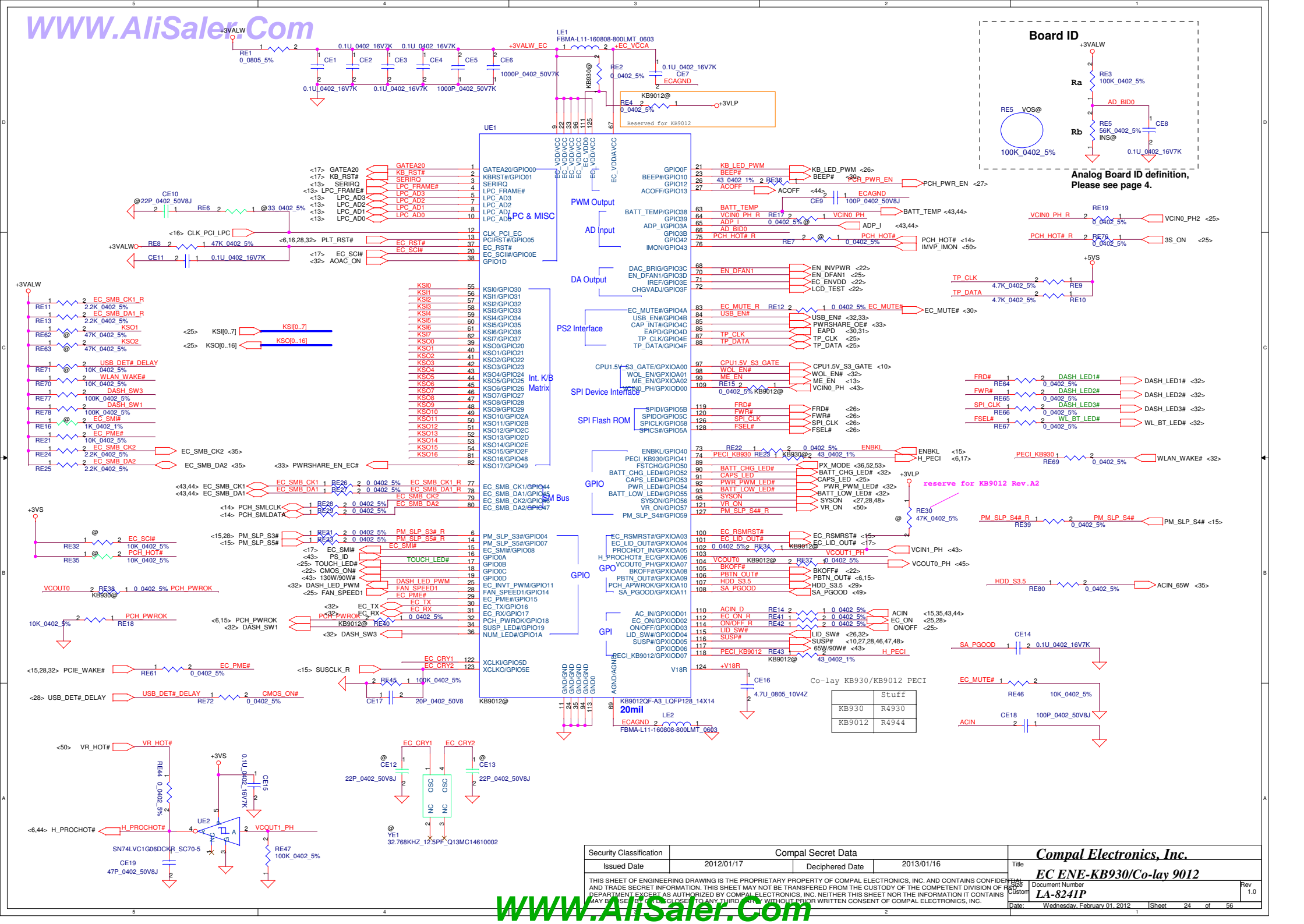
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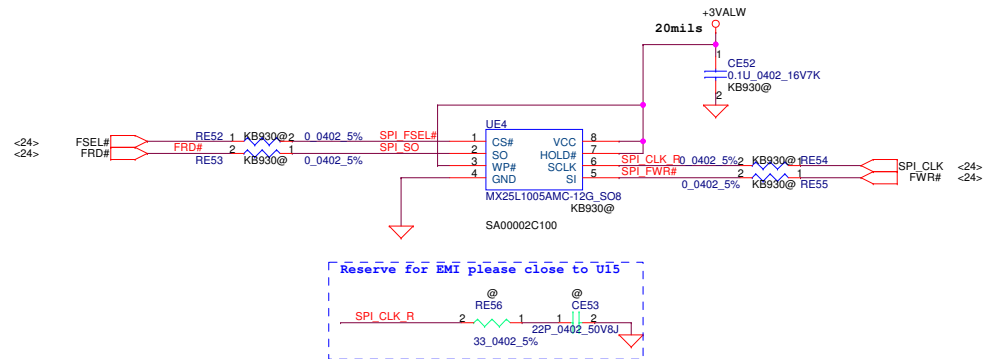
Part Number	Description
ROG000002HM	HDMI W/Logo:ROG000002HM



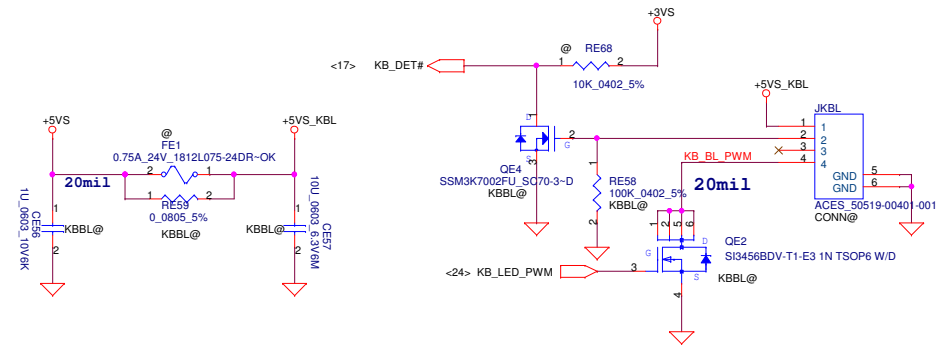
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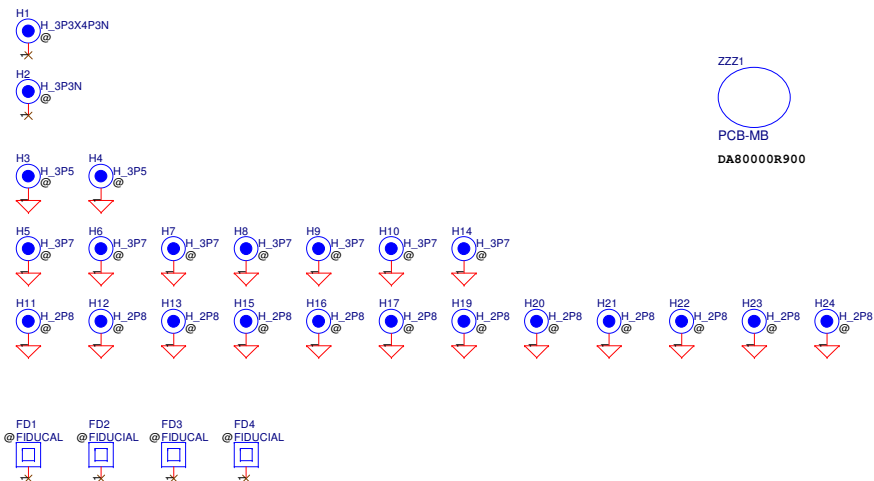
SPI ROM 128KB



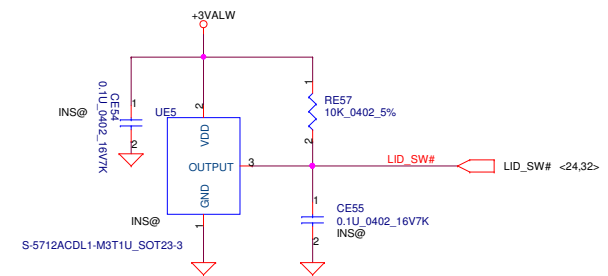
Keyboard back light



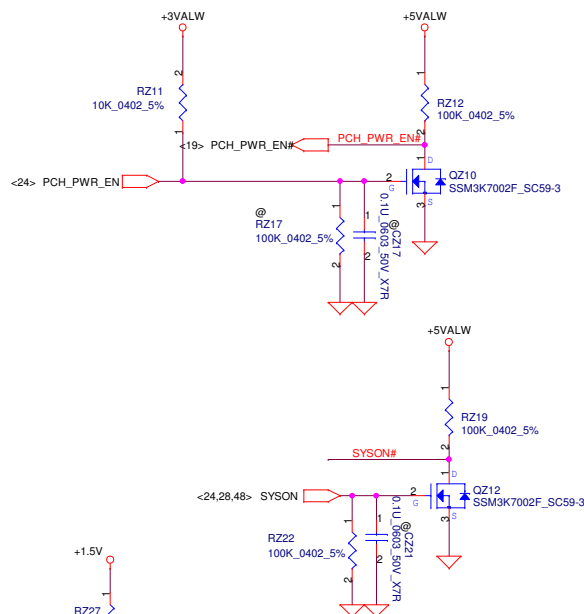
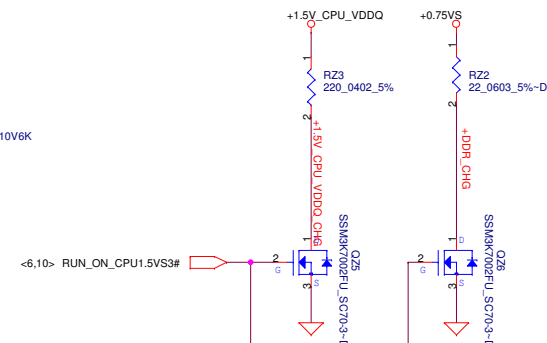
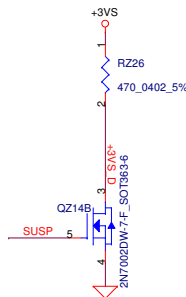
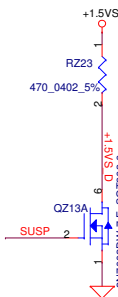
Screw Hole



Lid Switch

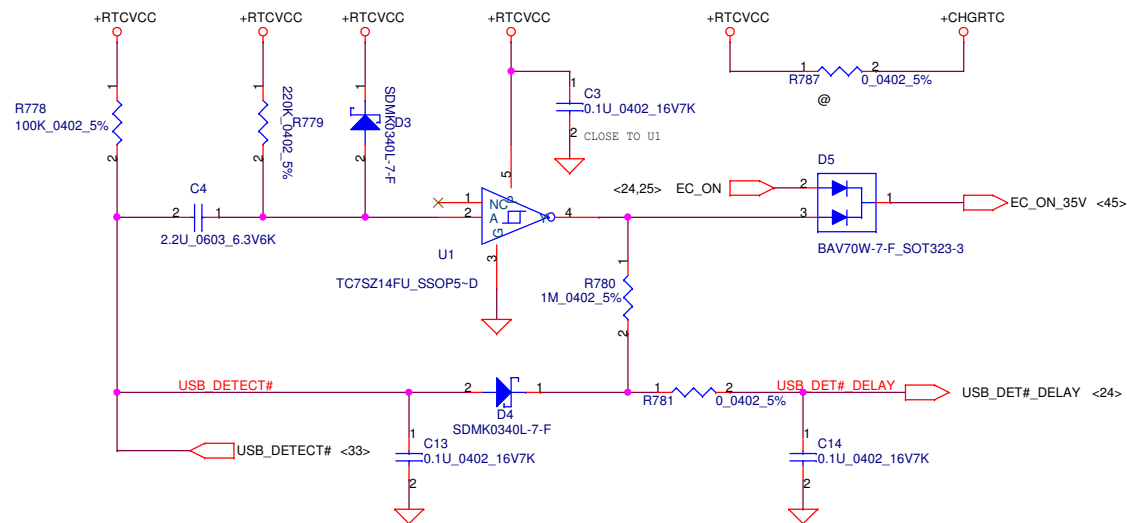


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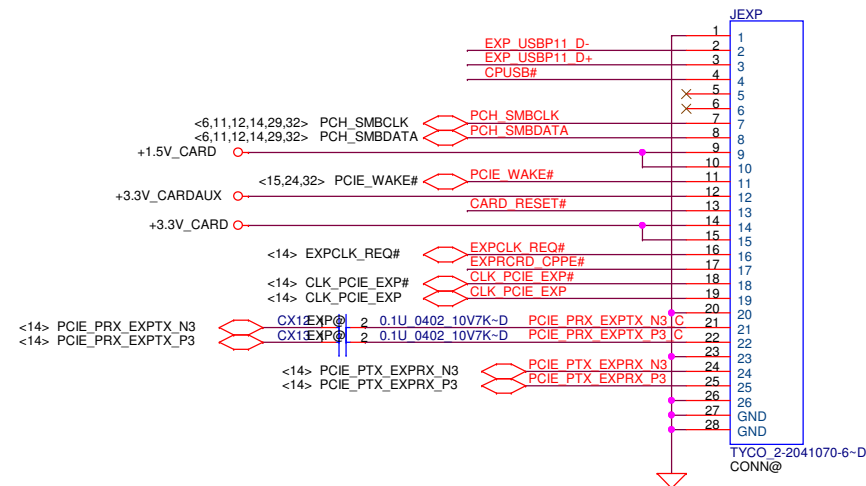


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MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR

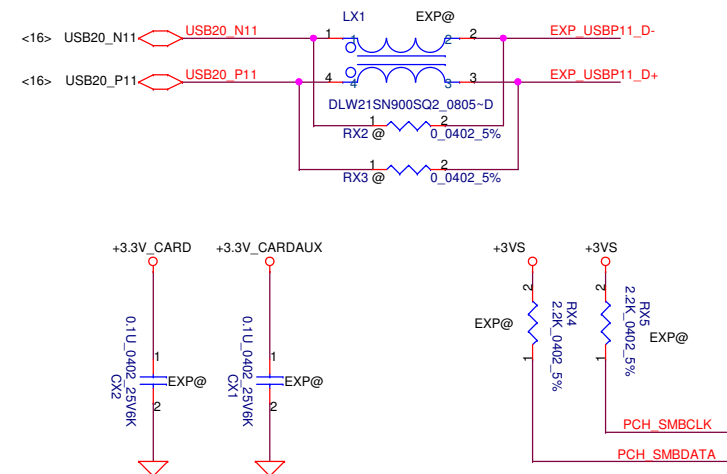
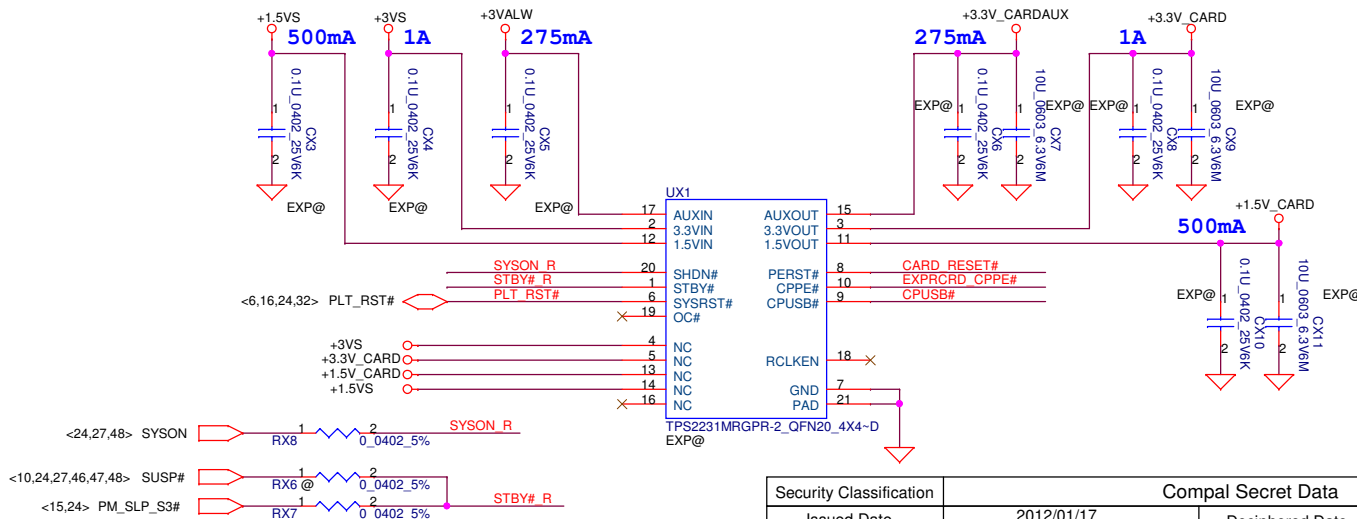
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Express Card

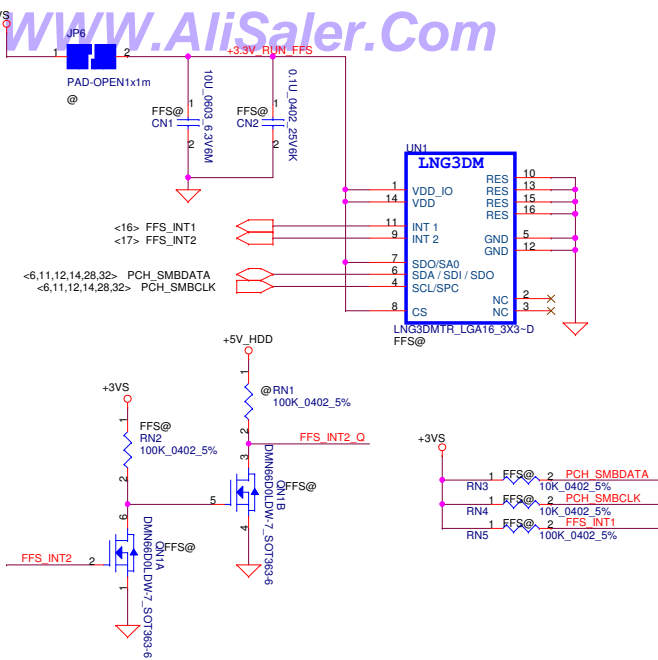


Express Card PWR S/W

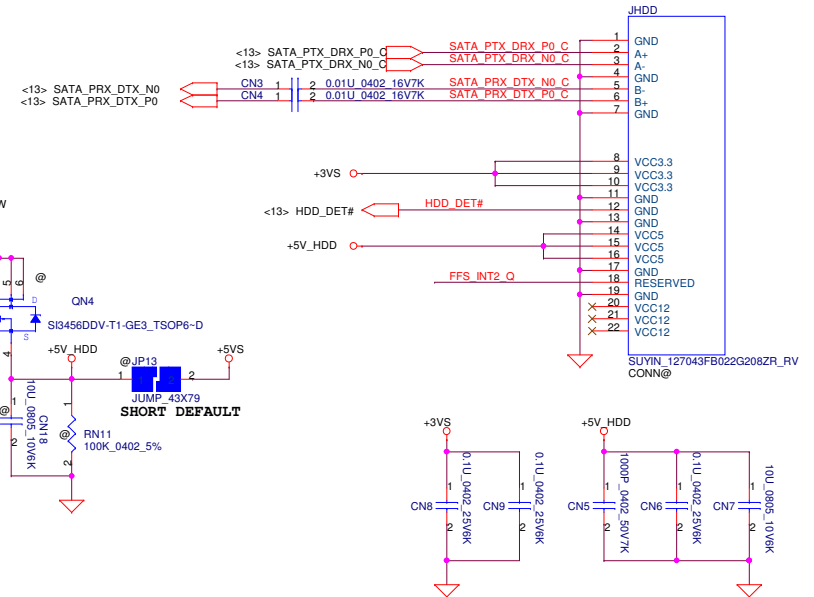
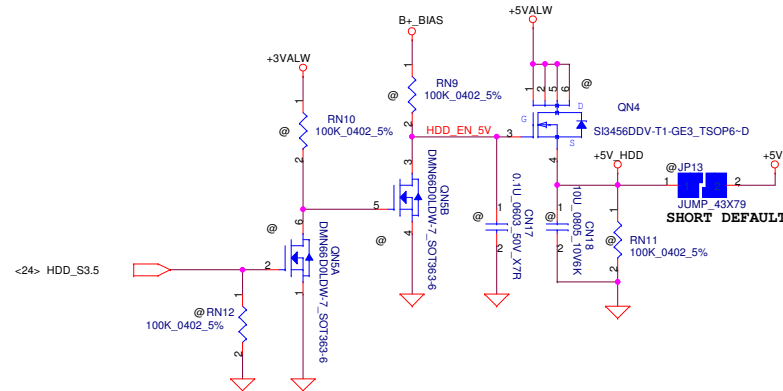


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Title				PROCESSOR(1/6) DMI,FDI,PEG				Rev			
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SATA HDD Conn.

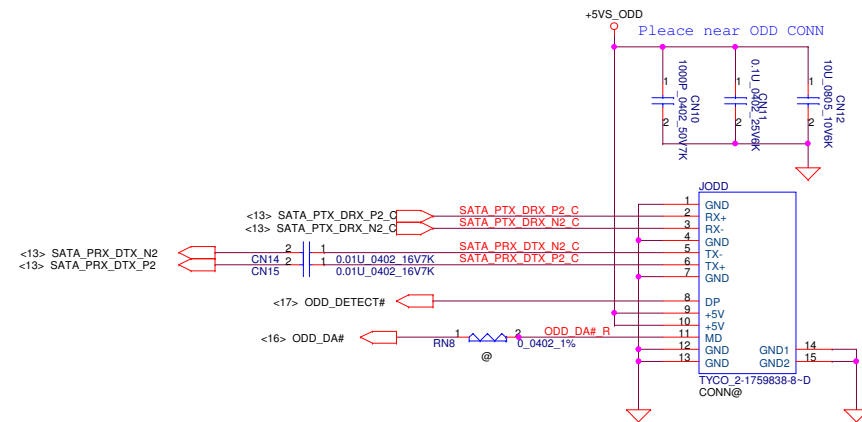
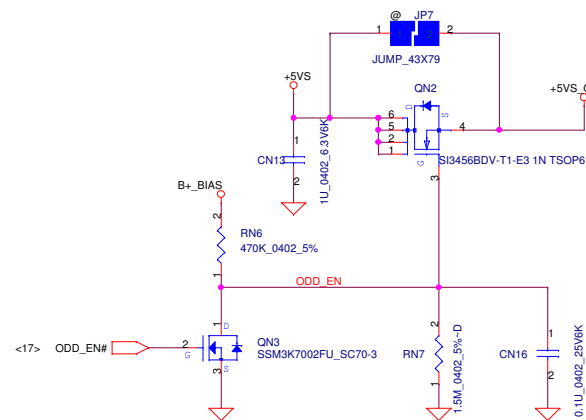


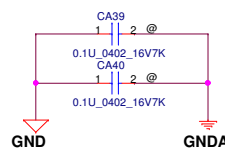
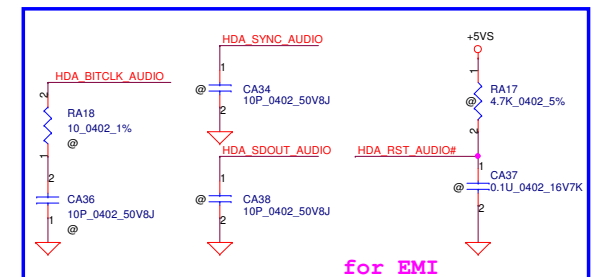
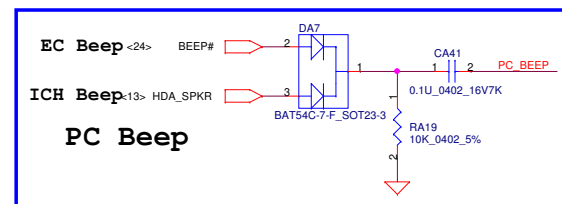
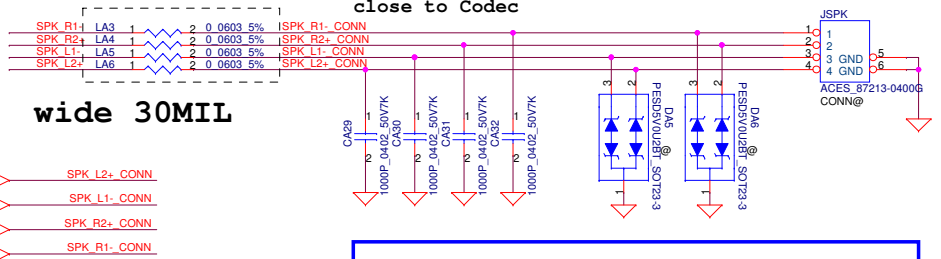
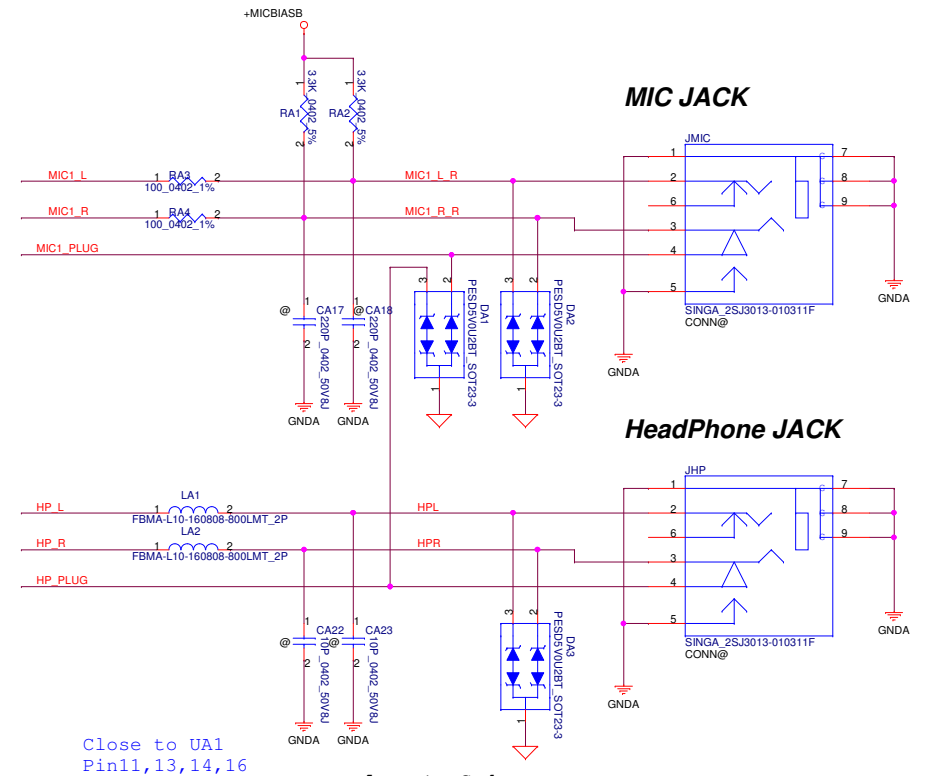
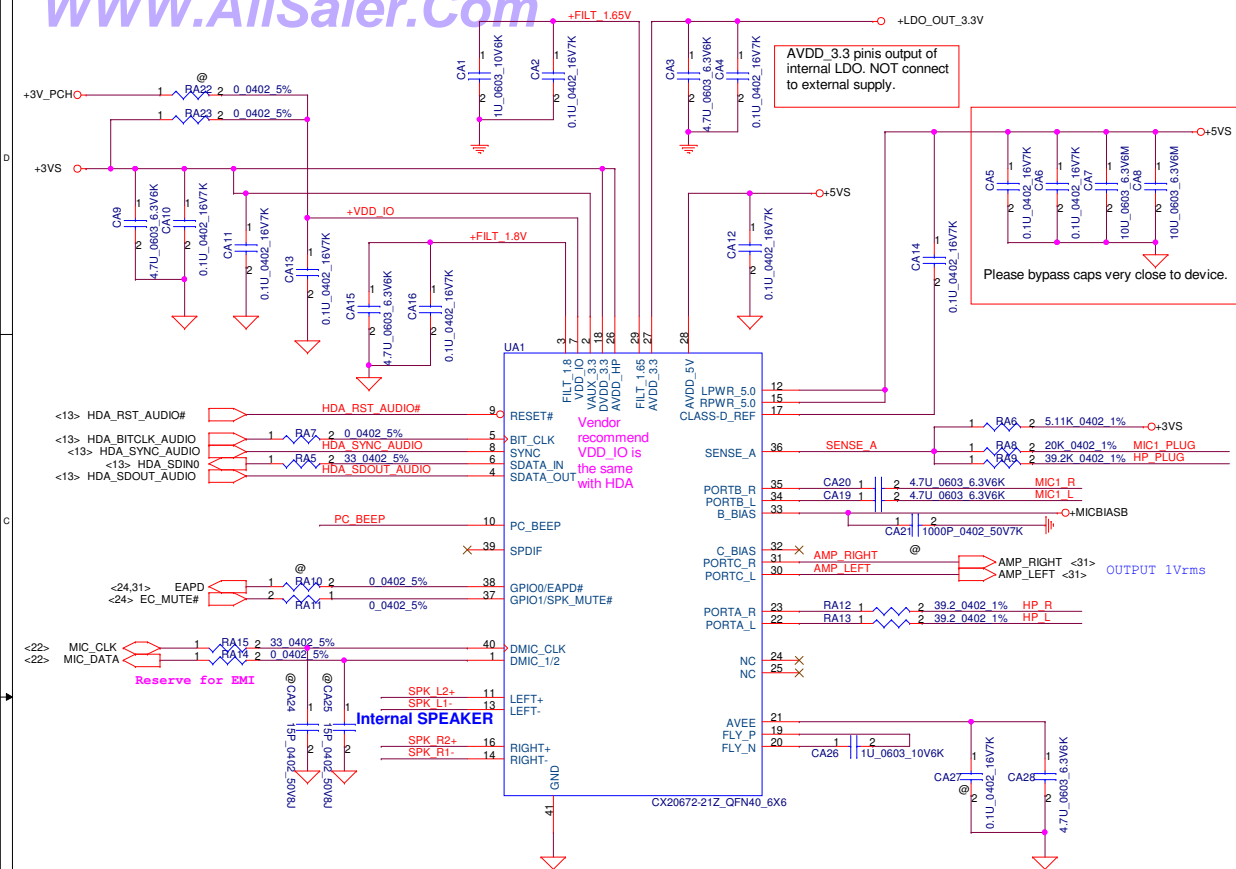
+5V_HDD Source



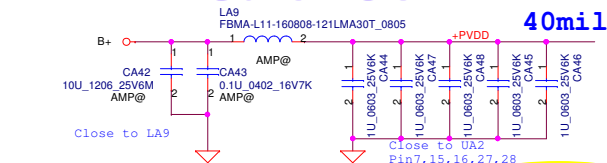
SATA ODD Conn.

ODD Power Control

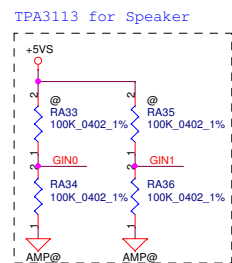




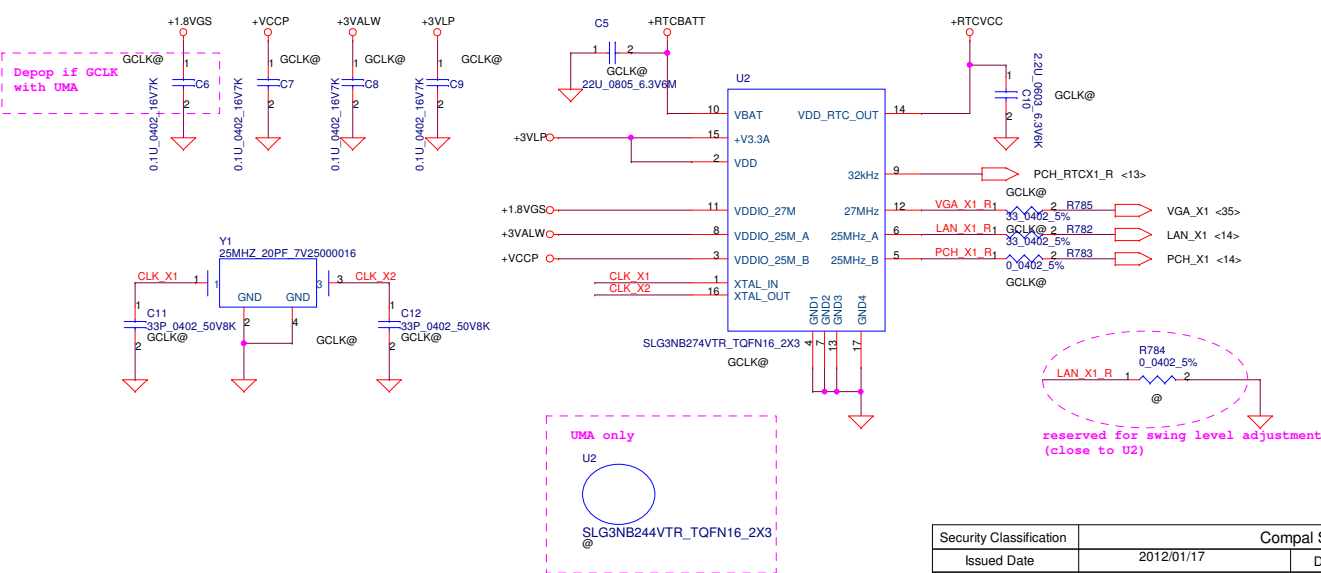
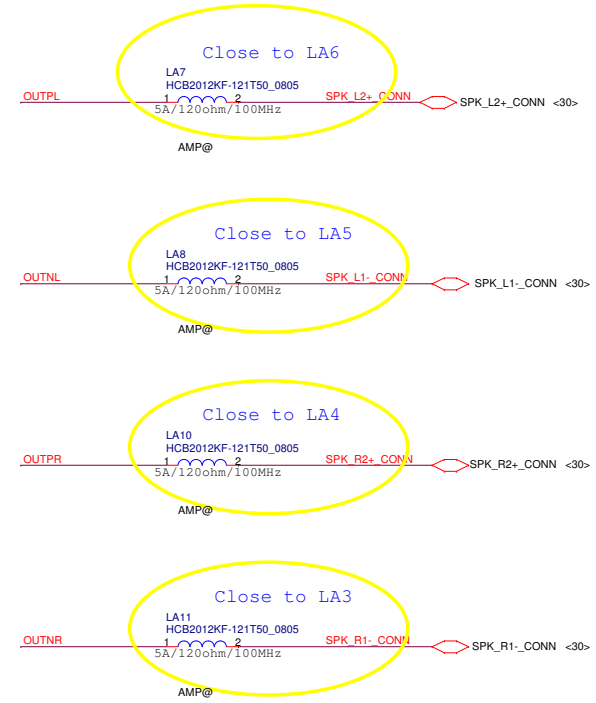
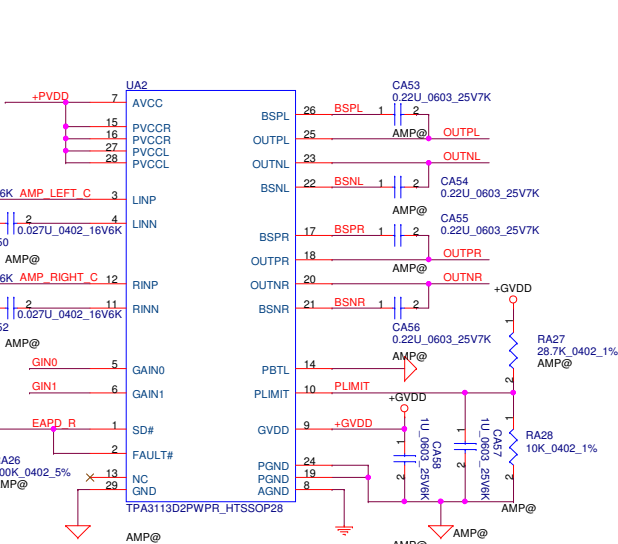
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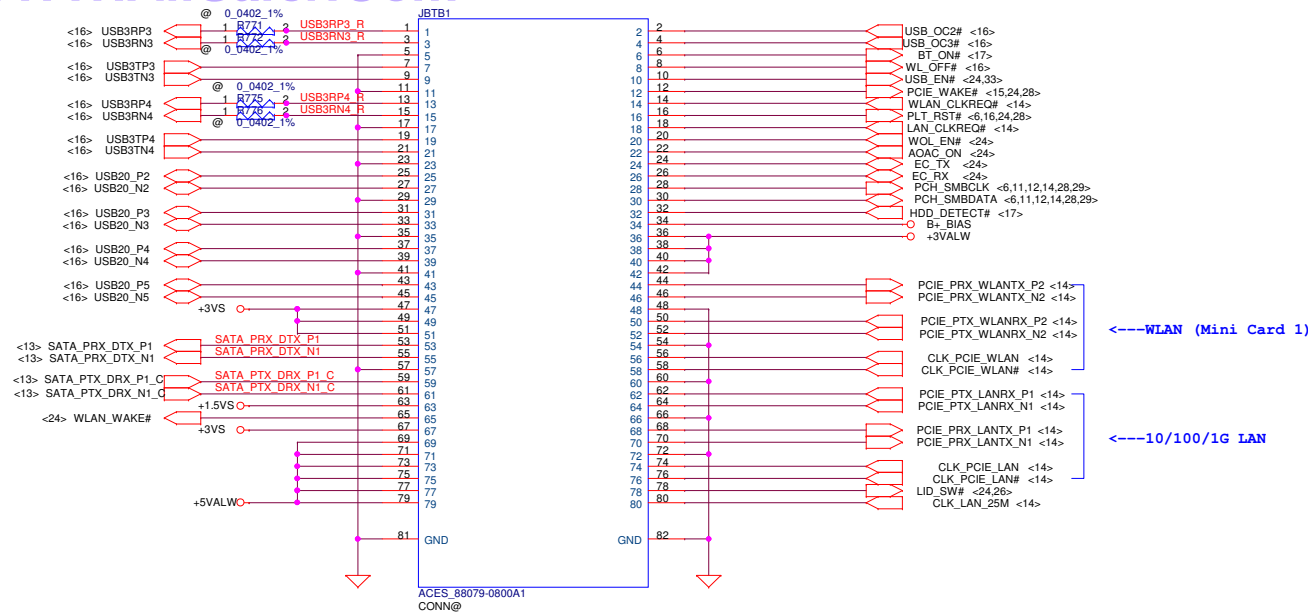


Need final turn R/C
10/24



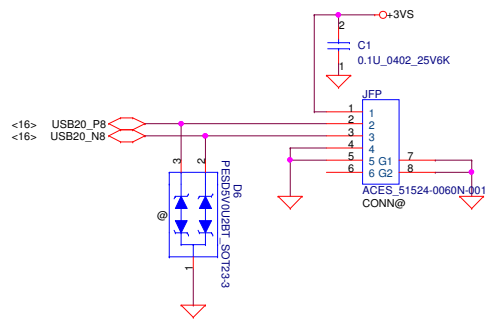
GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm





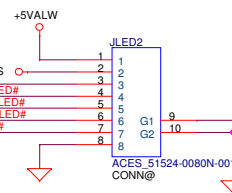
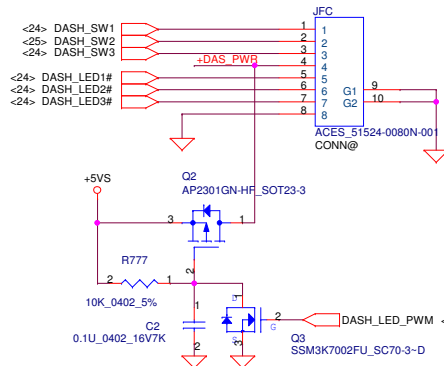
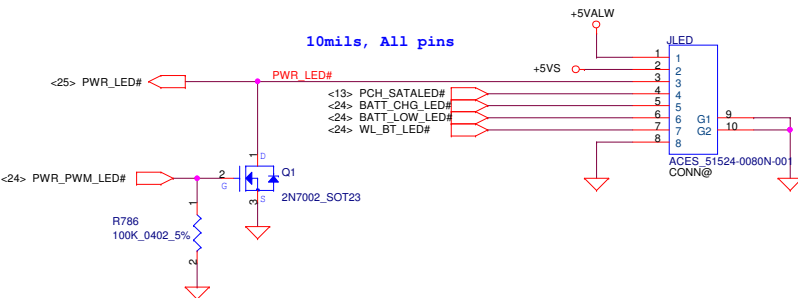
TO Function/B

To Finger Print



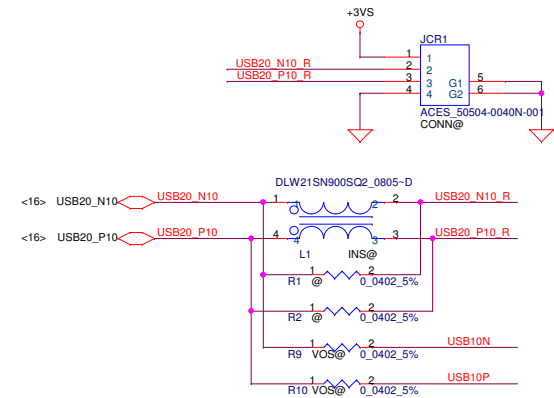
To LED/B

10mils, All pins



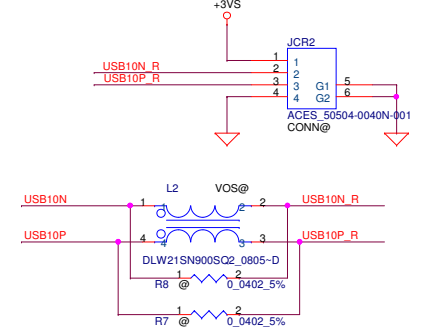
To CardReader/B

* Inspiron only

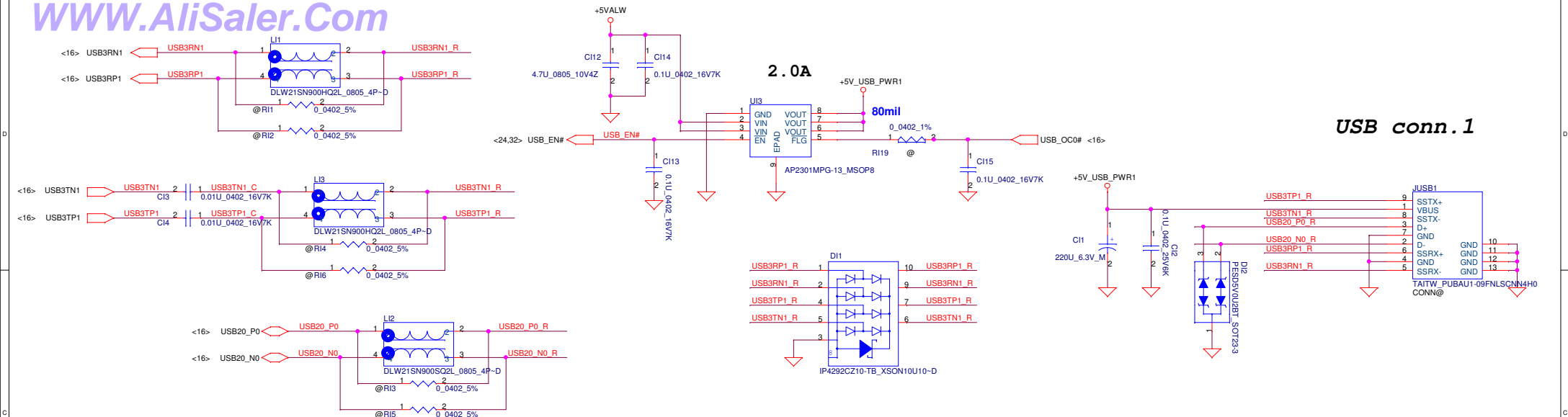


To CardReader/B

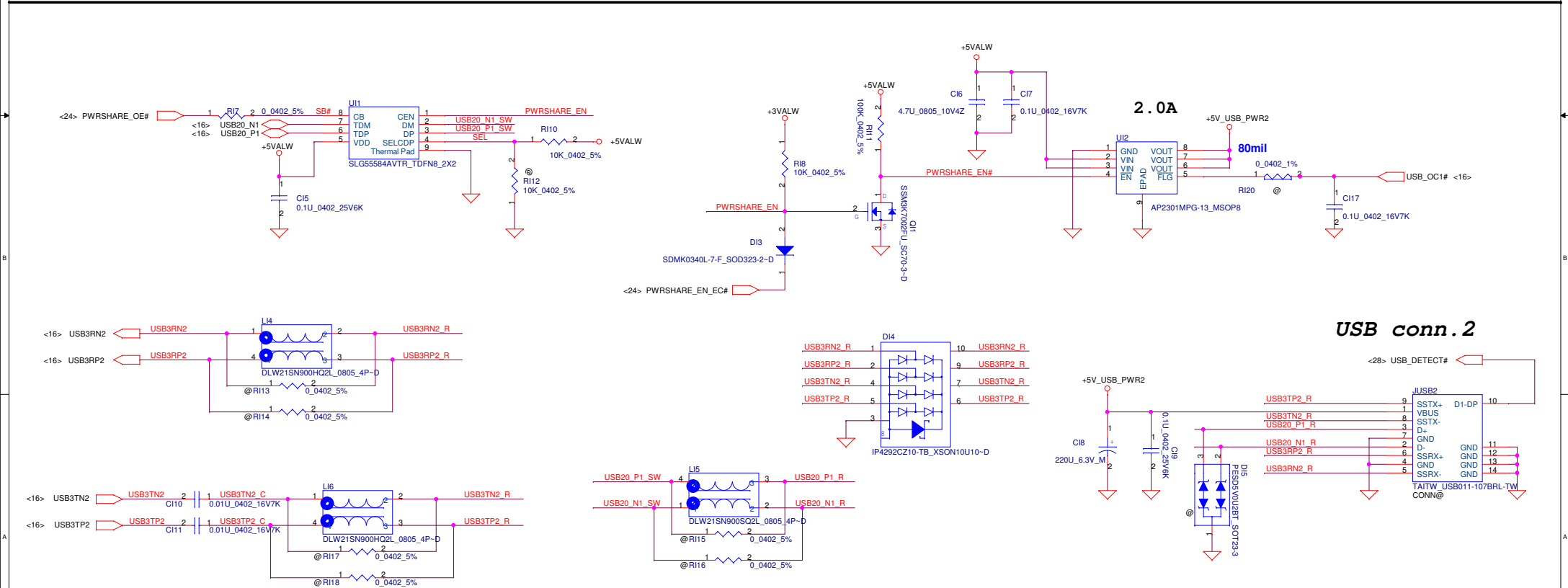
* Vostro only



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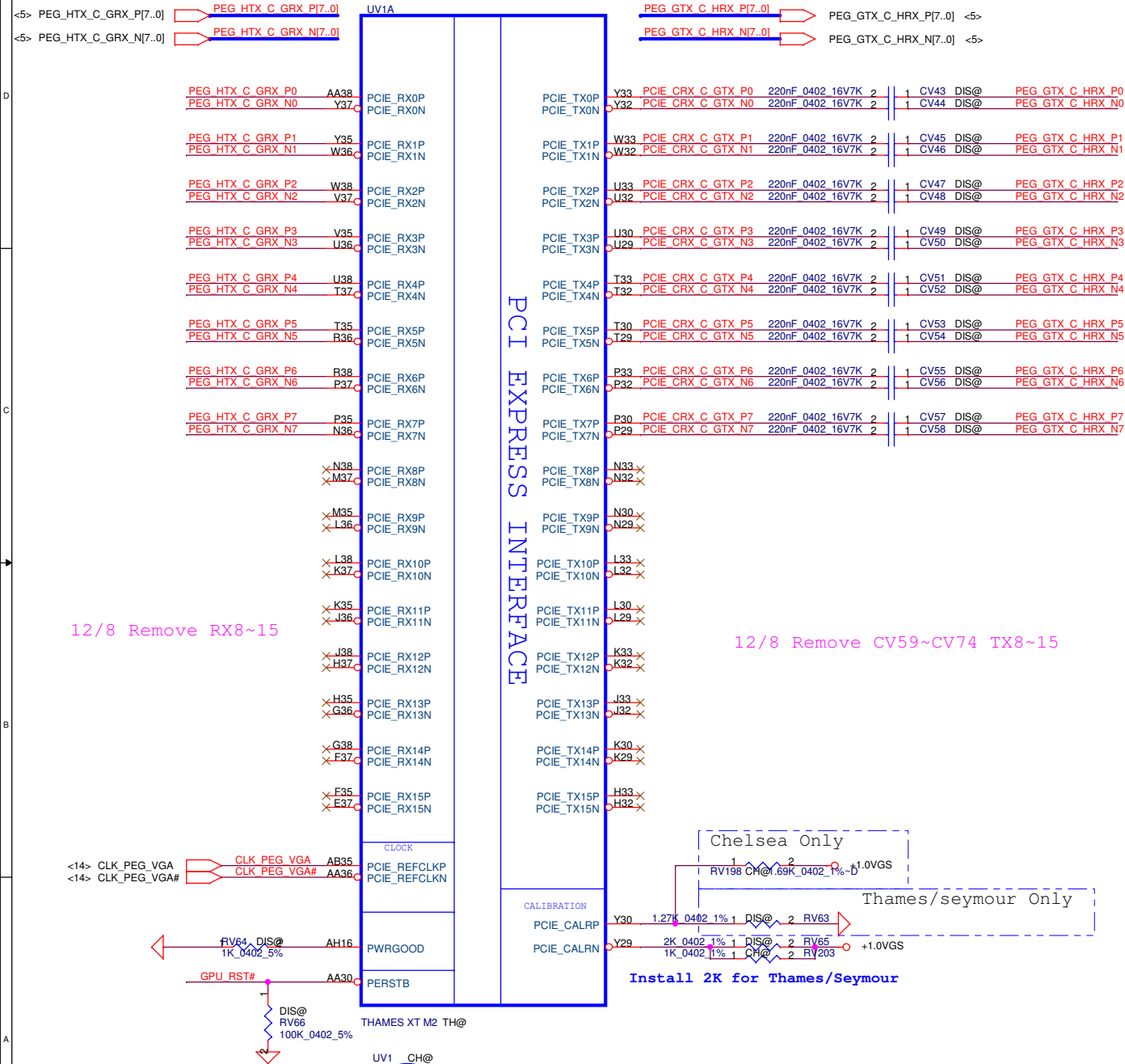
USB conn. 1



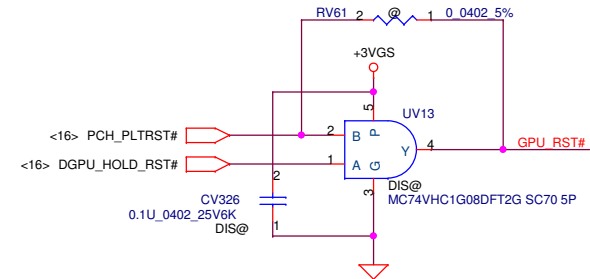
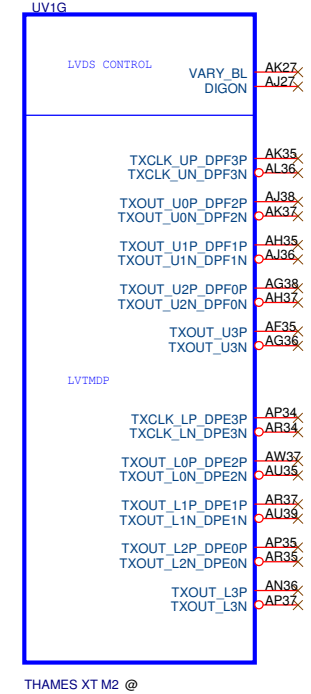
USB conn. 2

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				PROCESSOR(1/6) DMI,FDI,PEG			
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				LA-8241P			1.0
				Date:			Wednesday, February 01, 2012
				Sheet		33 of 56	

GFX PCIE LANE REVERSAL

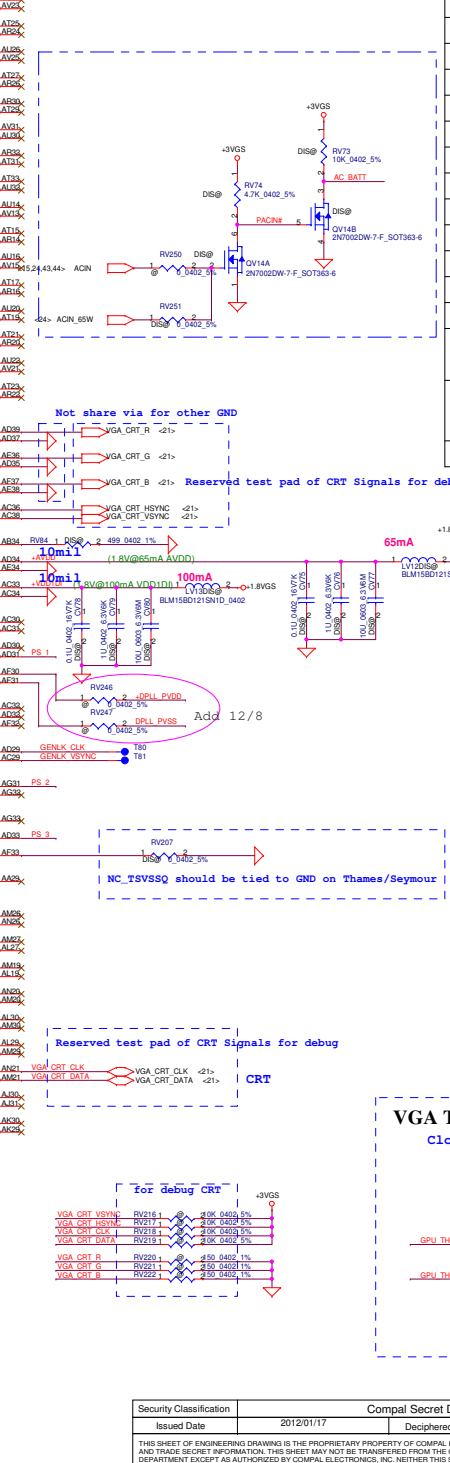
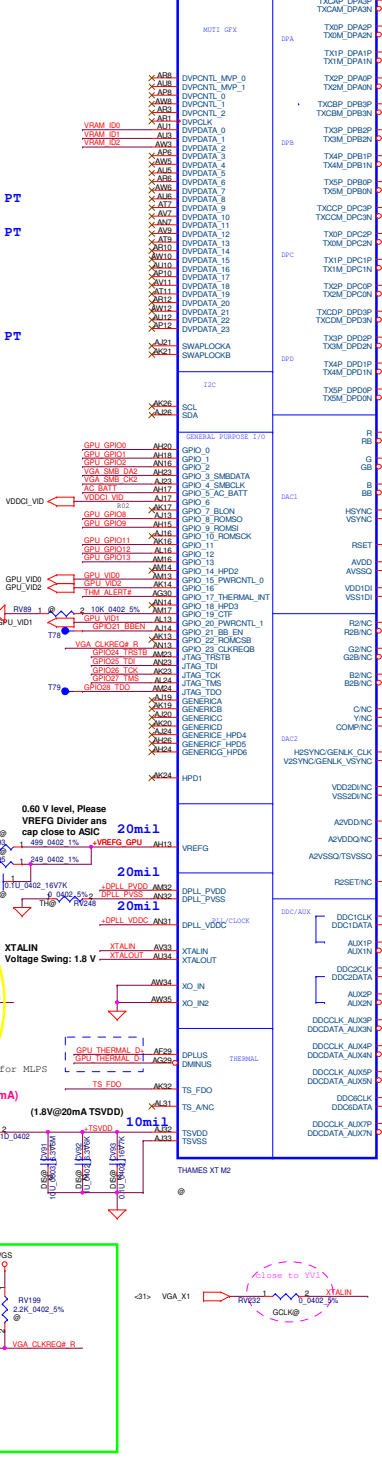
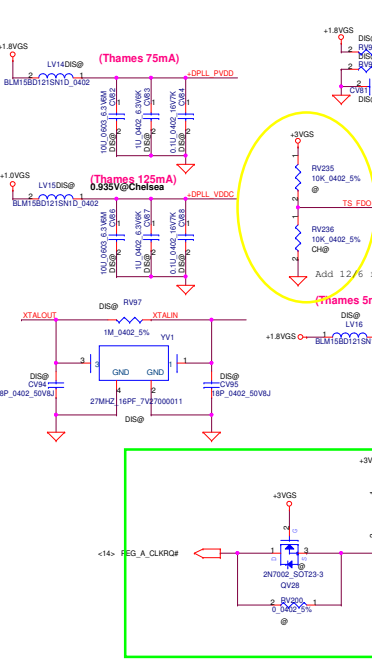
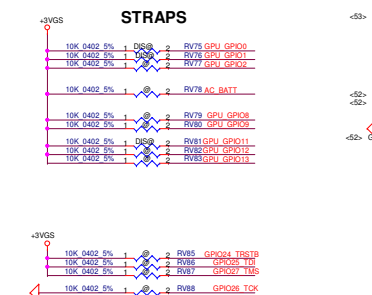


LVDS Interface



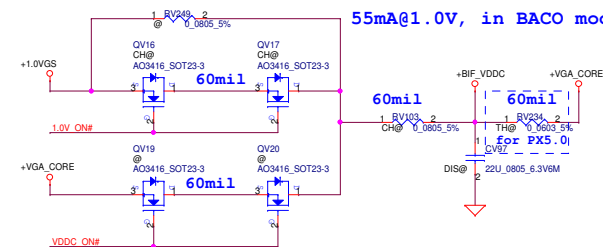
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Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
64MX16 (1G)	Hynix 1GB PN-SA000041S3L	RV67	RV70	RV72
64MX16 (1G)	Samsung 1GB PN-SA00004GS1L	RV68	RV69	RV72
128M16 (2G)	Hynix 2GB PN-SA00003Y01L	RV67	RV70	RV71
128M16 (2G)	Samsung 2GB PN-SA000047Q1L	RV68	RV69	RV71
64MX16 (1G)	Micron 1GB PN-SA00004Y20L	RV67	RV69	RV71

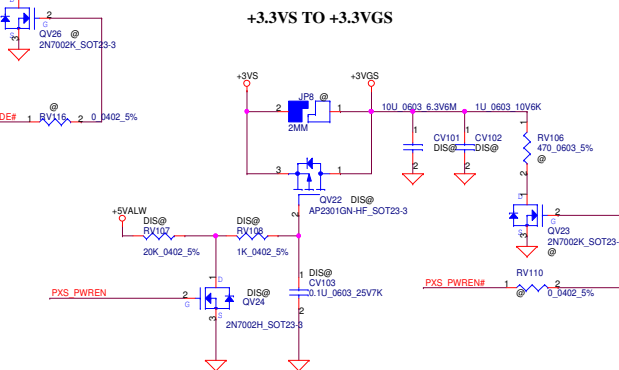
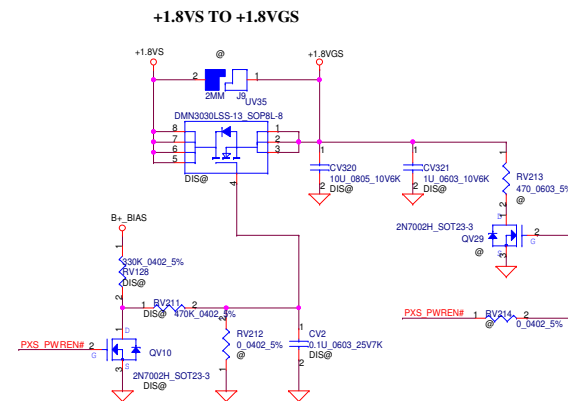
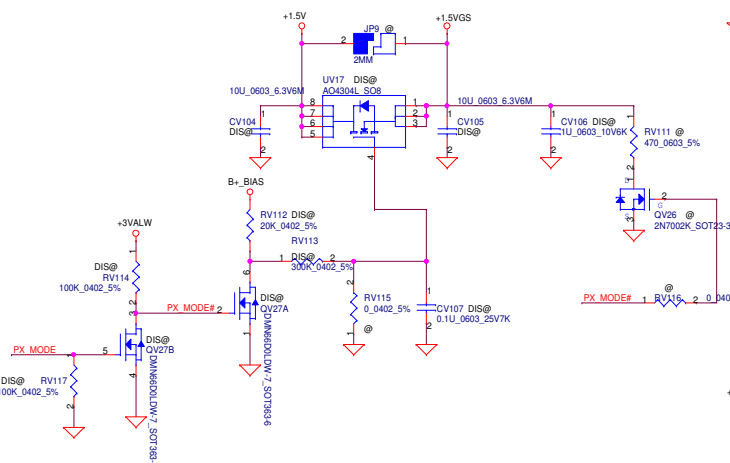
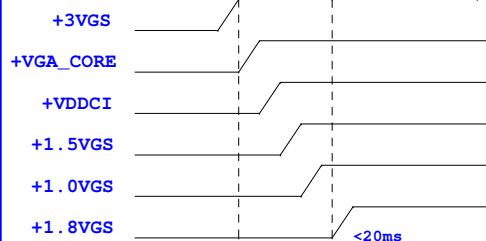


AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET			
STRAPS	GPIO	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	POE FULL TX OUTPUT SWING	0: 50% swing 1: Full swing
TX_DEEMPH_EN	GPIO1	PCI TRANSMITTER DE-EMPHASIS	0: enable 1: enable
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 2.5GT/s 1: 5GT/s
RSVD	GPIO8	RESERVED	0
BF_VGA_DS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22, ROMCSB	ENABLE EXTERNAL BIOS ROM	0: enable 1: enable
ROMCFG2(0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VP_DEVICE_STRAP_ENA	V2SYN	IGNORE VIP DEVICE STRAPS	0
RSVD	HSYN	HSYN	0
RSVD	GENERIC	GENERIC	0
ADD[1]	ADD[0]	ADD[1] ADD[0]	11

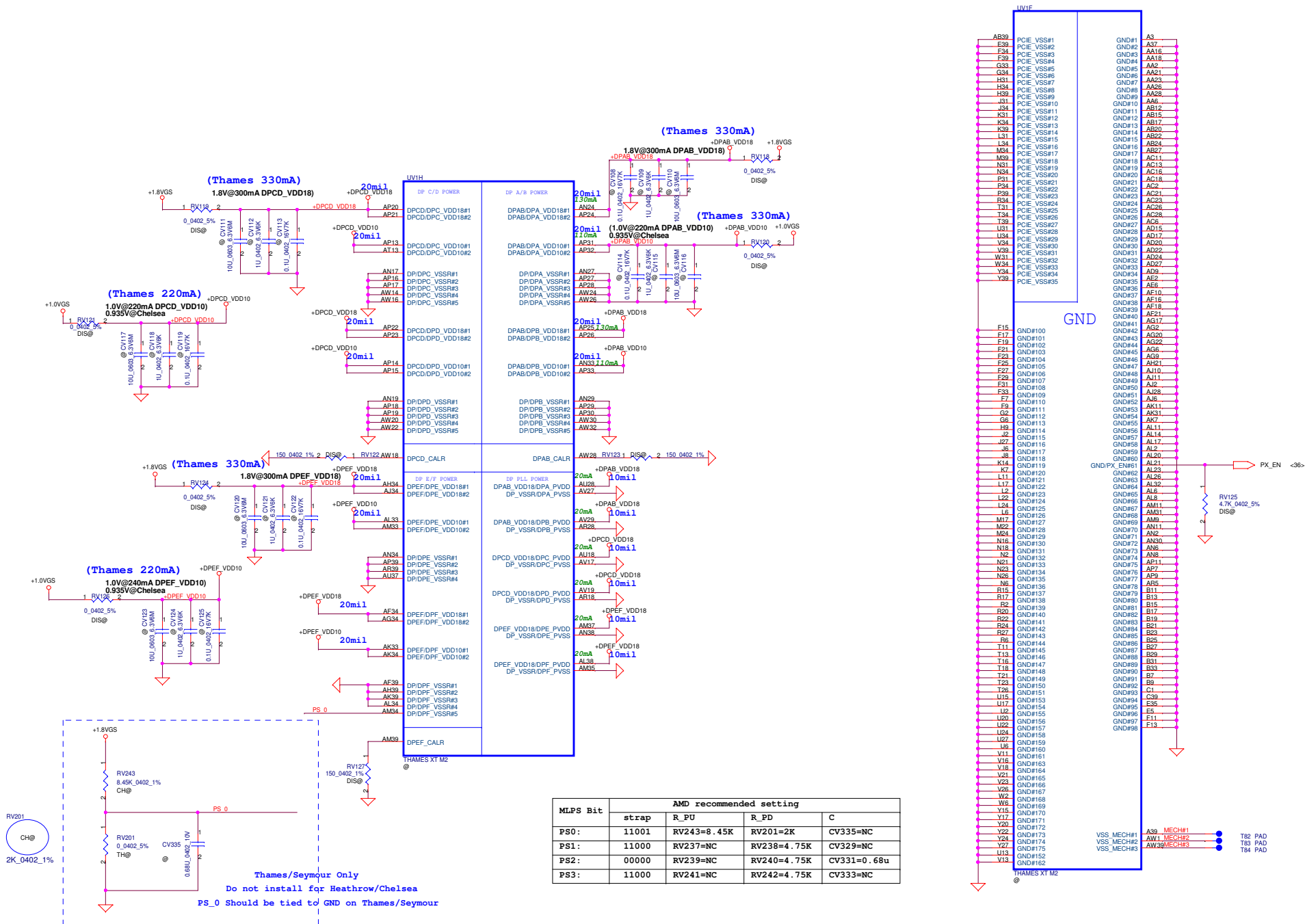
55mA@1.0V, in BACO mode



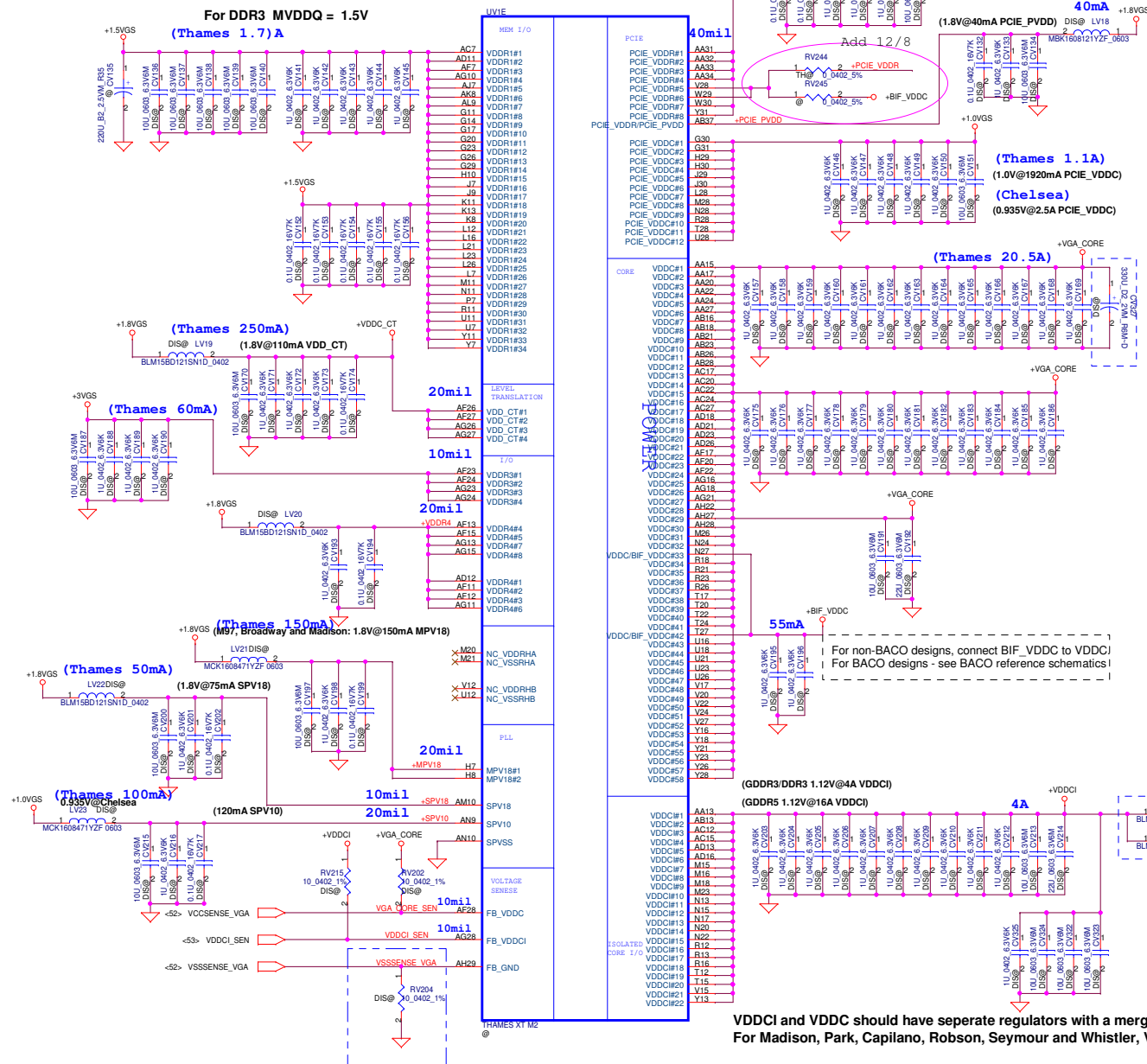
Power Sequence of Thames and Chelsea



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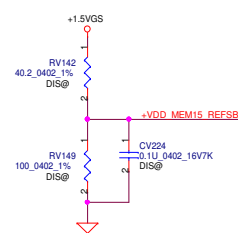
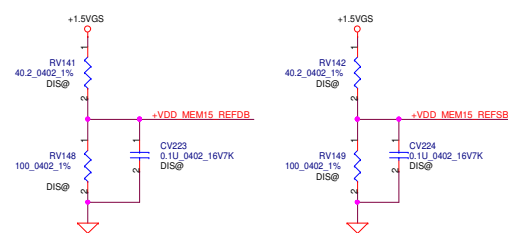
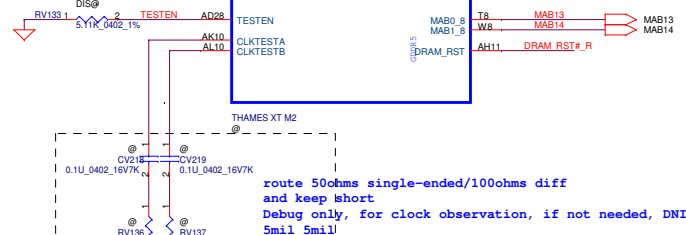
MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

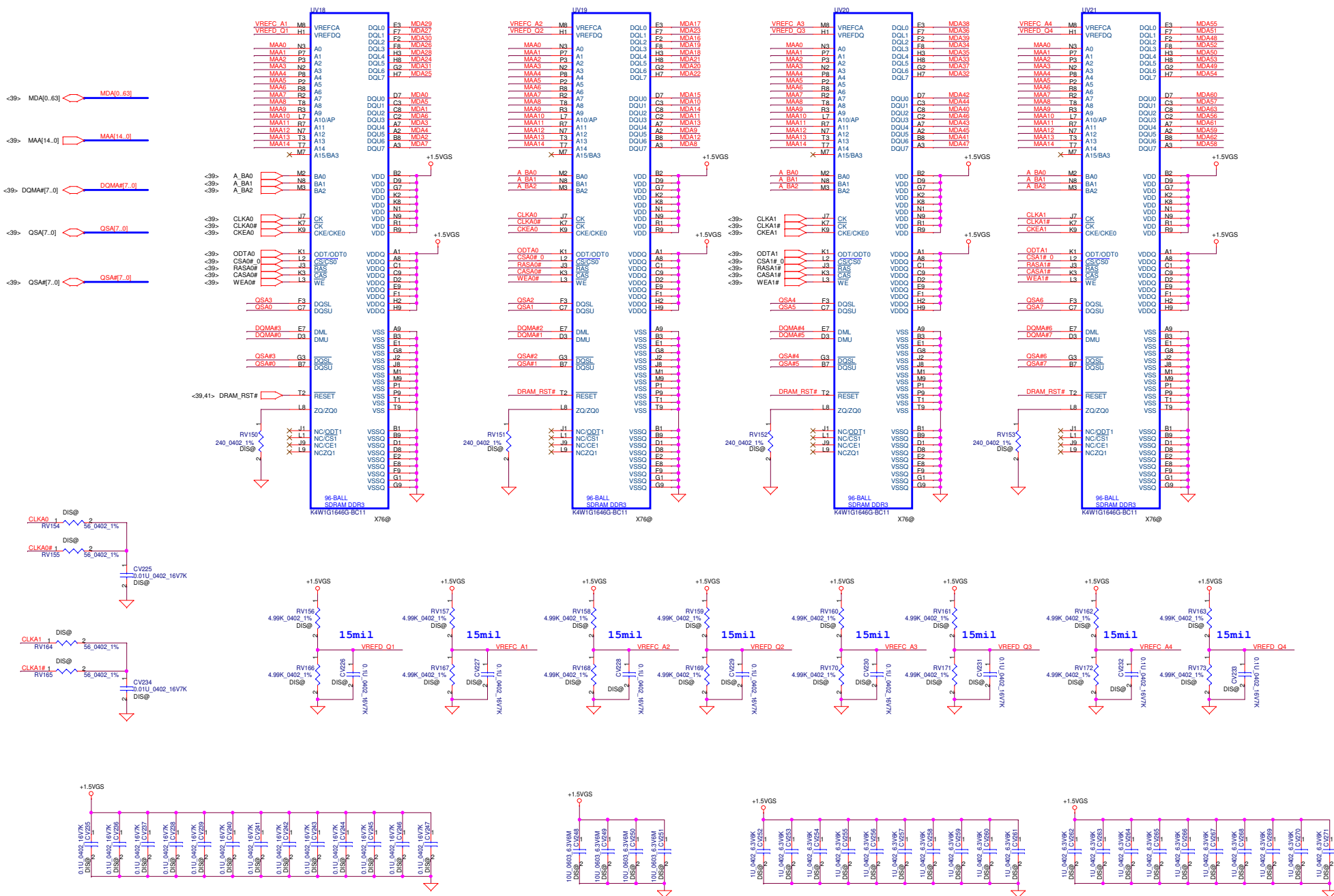




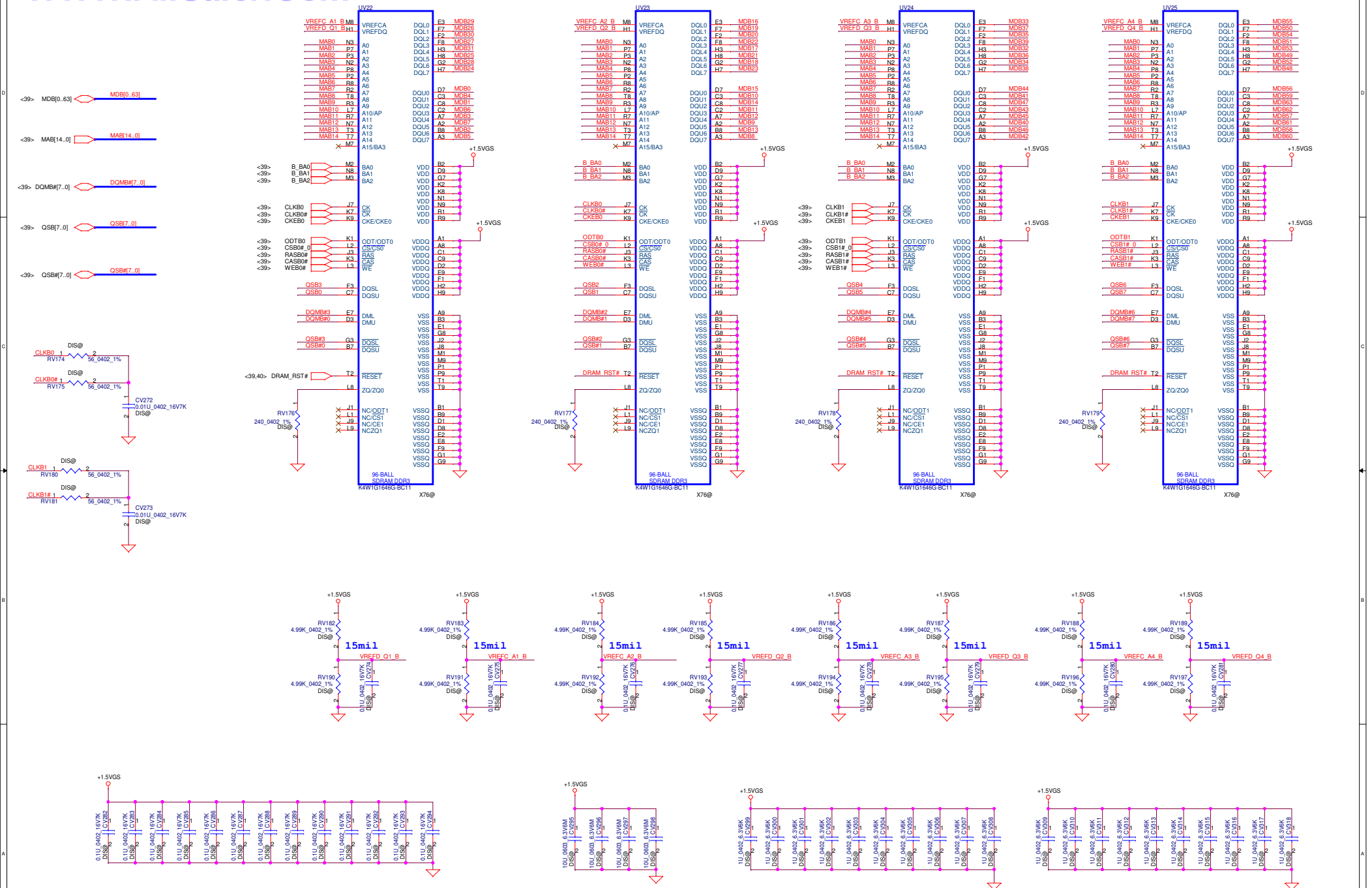
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2





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						Size C	Document Number			LA-8241P		Rev
Date: Wednesday, February 01, 2012						Sheet	40	of	56			




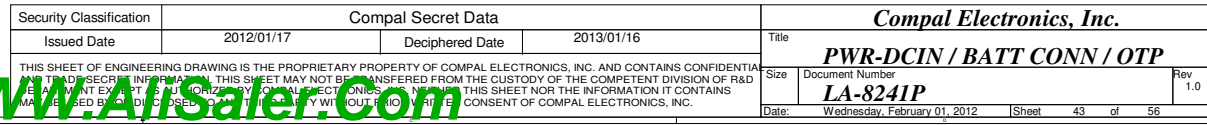
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				ATI SeymourXT M2 VRAM B		
Size C		Document Number		LA-8241P		
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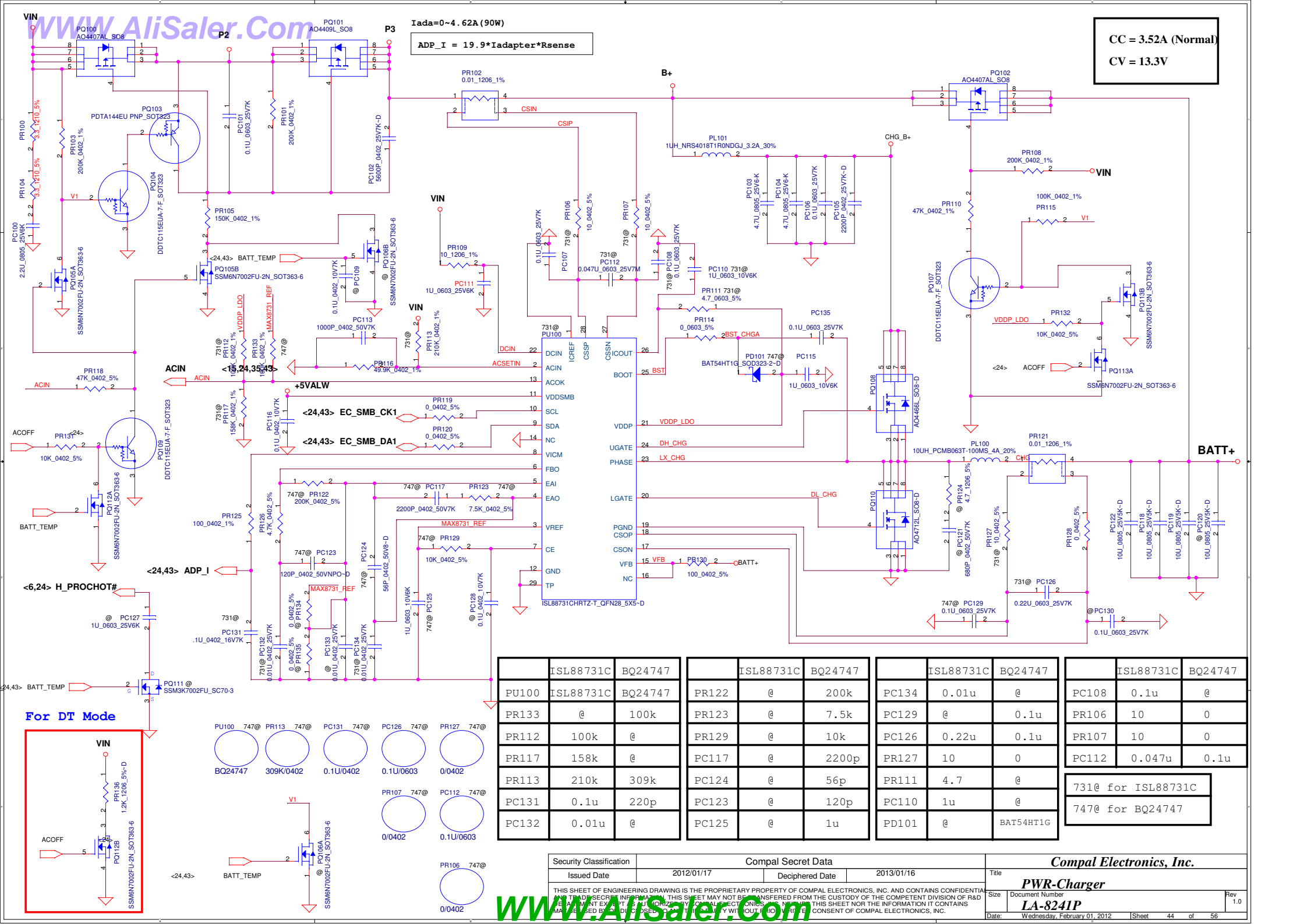
Version Change List (P. I. R. List)

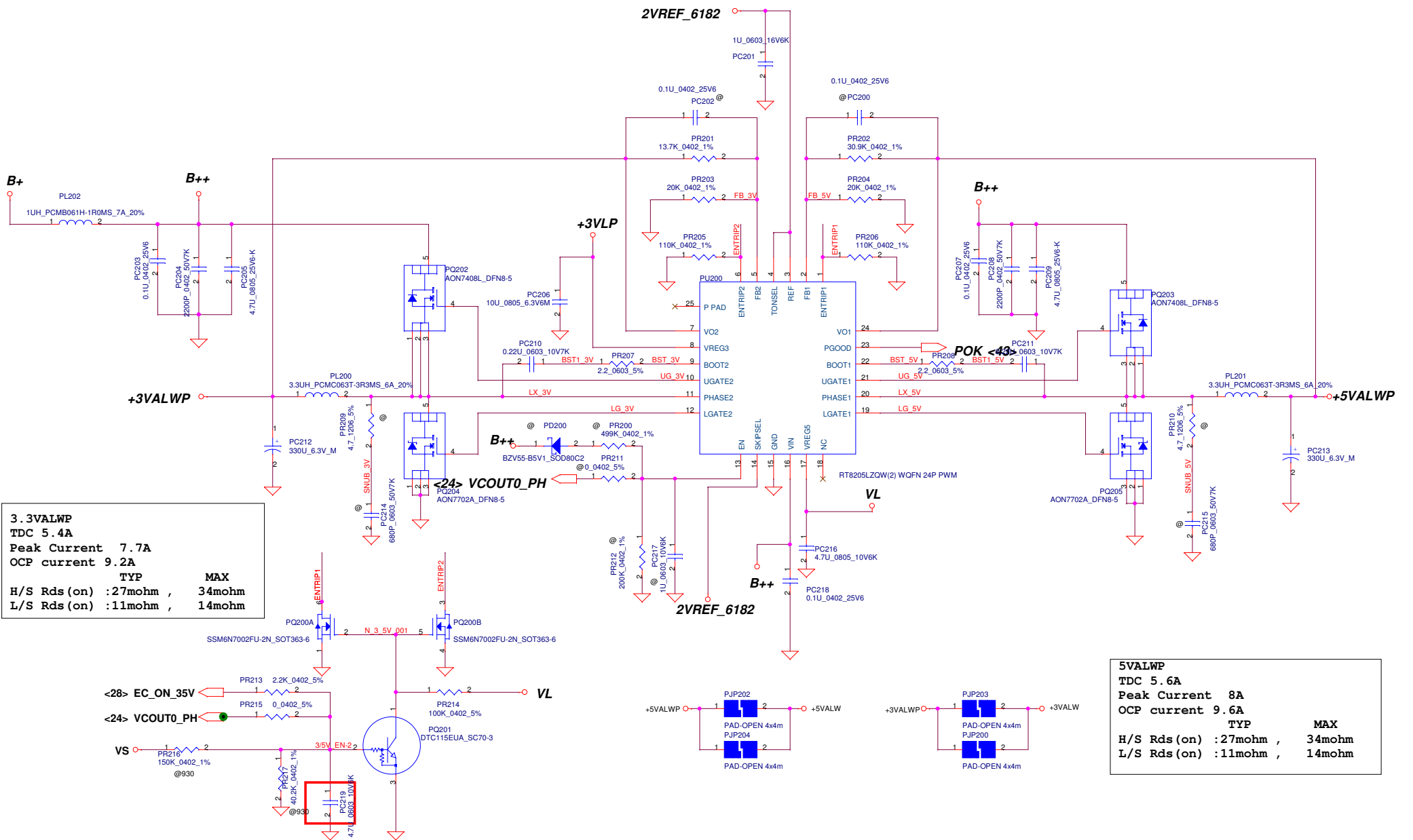
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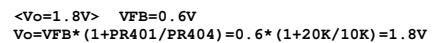
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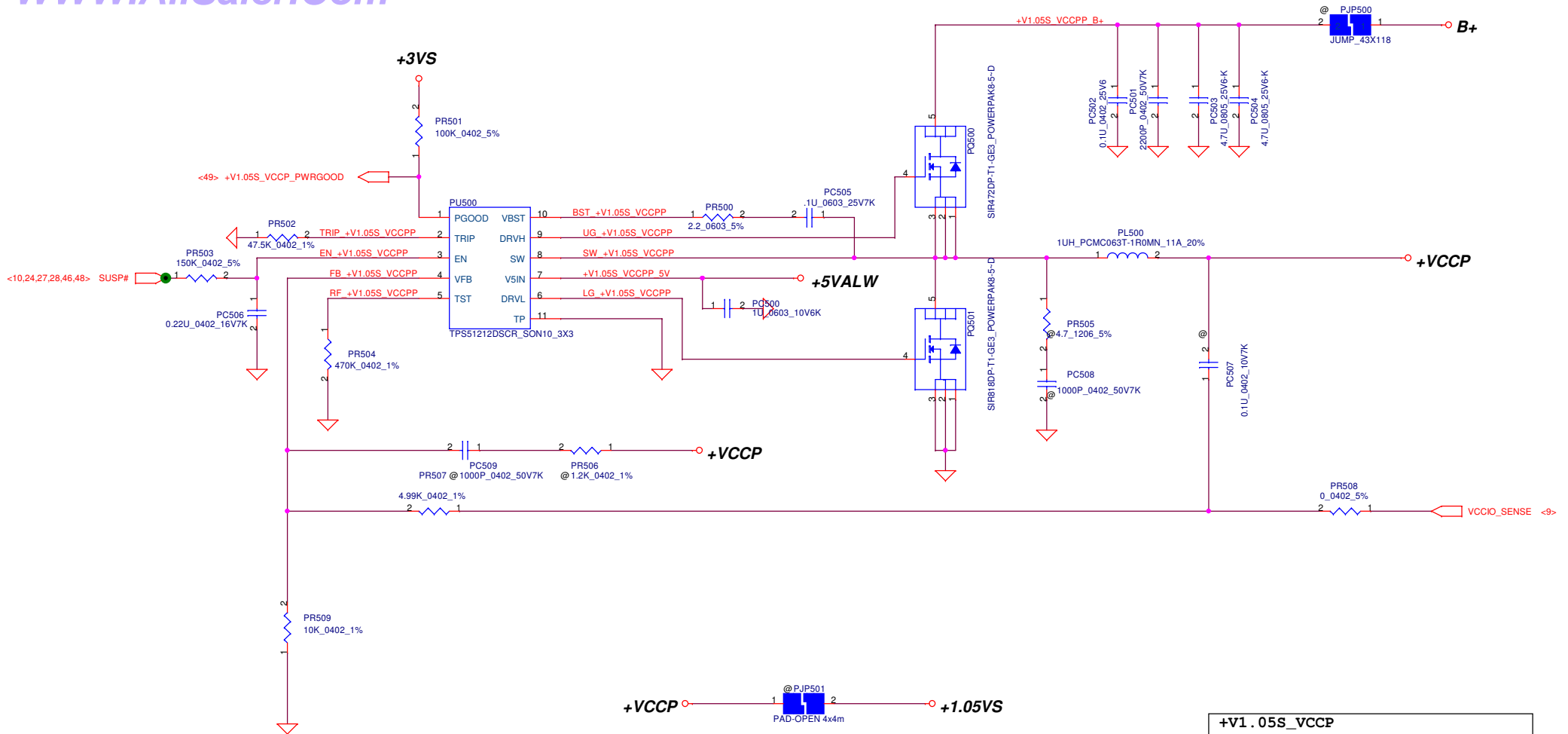




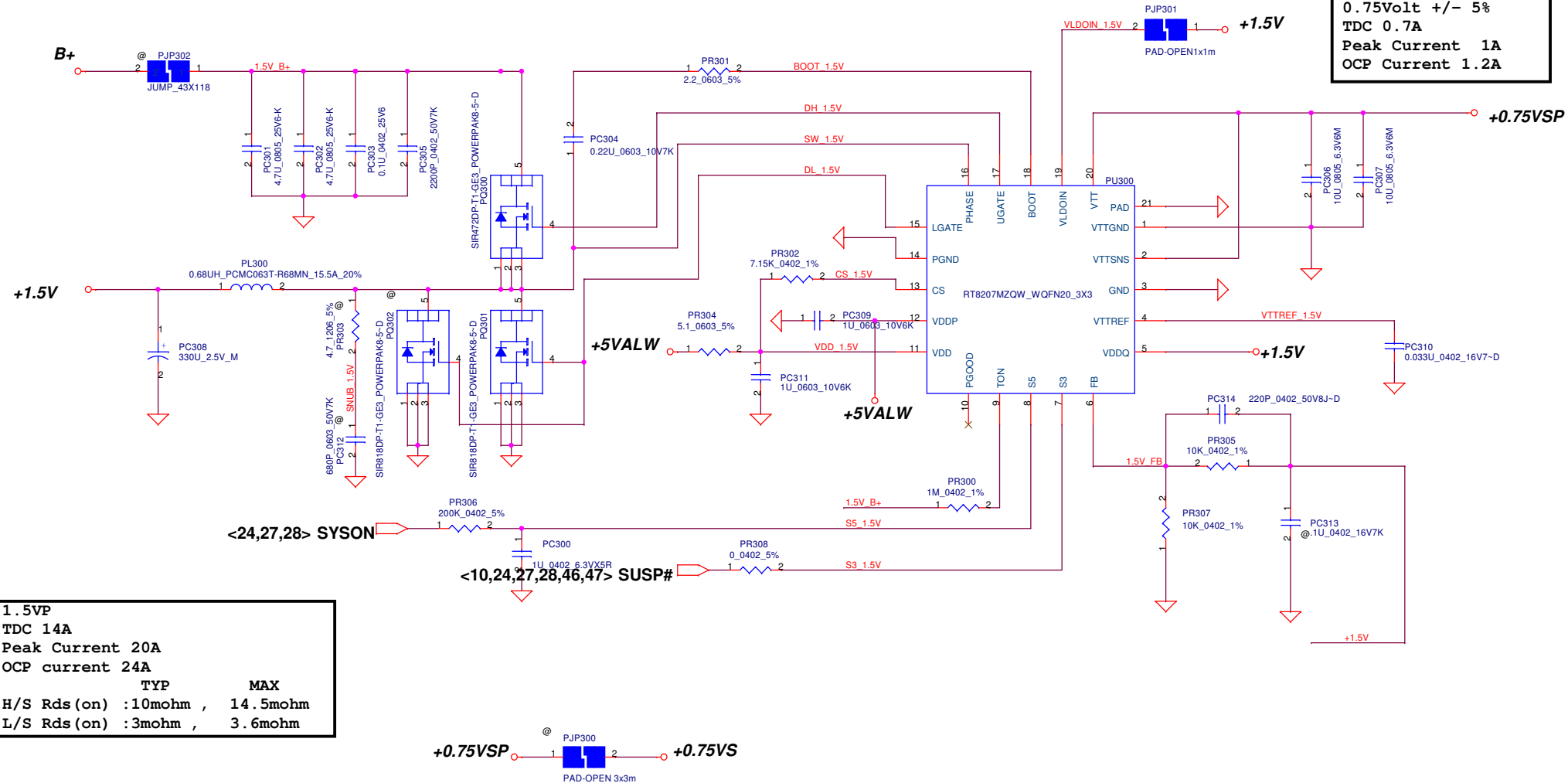
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				Sheet	46 of 56

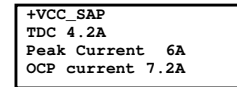


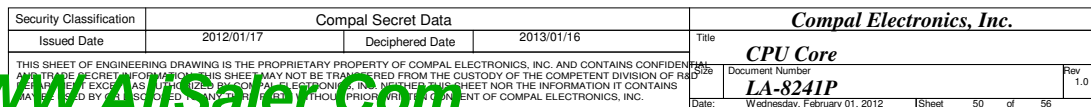
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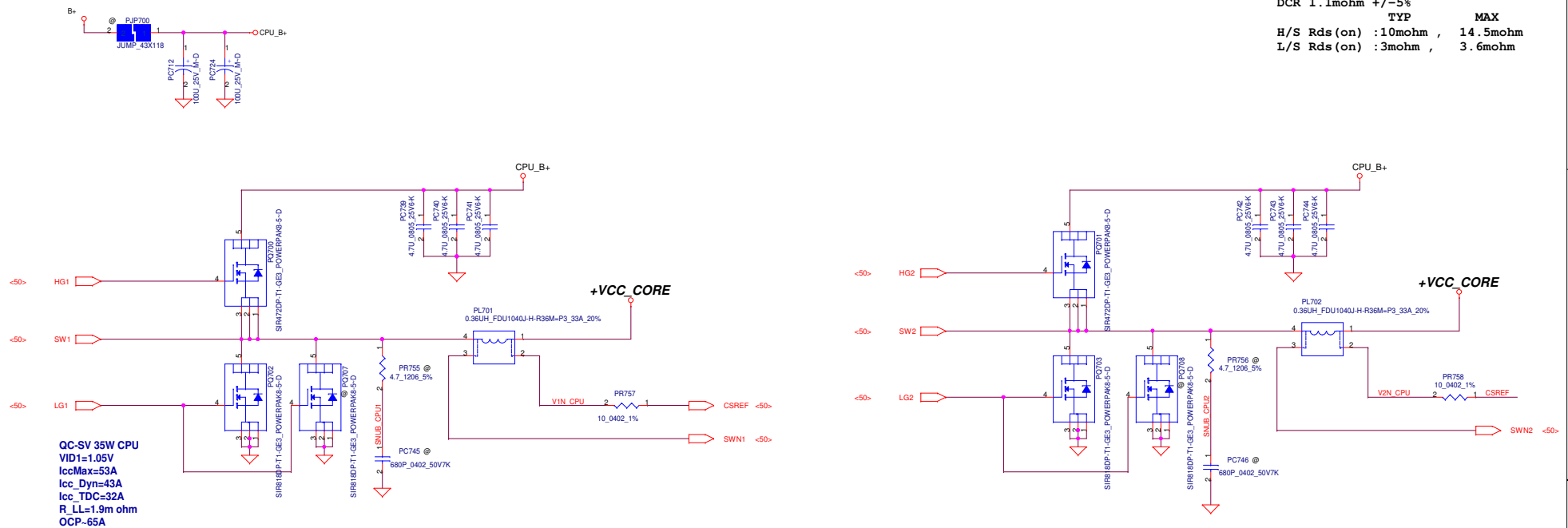
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output voltage adjustable network



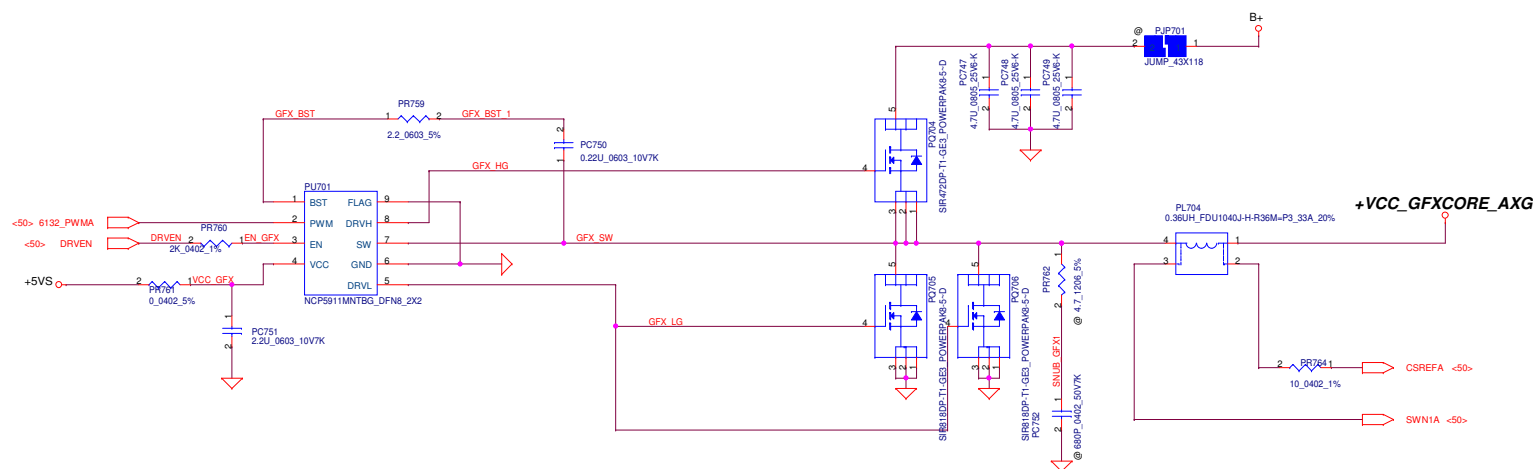


VCC_core		
TDC 32A		
Peak Current	53A	
OCP current	65	
Load line	-1.9mV/A	
FSW=300kHz		
DCR 1.1mohm	+/-5%	
	TYP	MAX
H/S Rds(on)	:10mohm	, 14.5mohm
L/S Rds(on)	:3mohm	, 3.6mohm

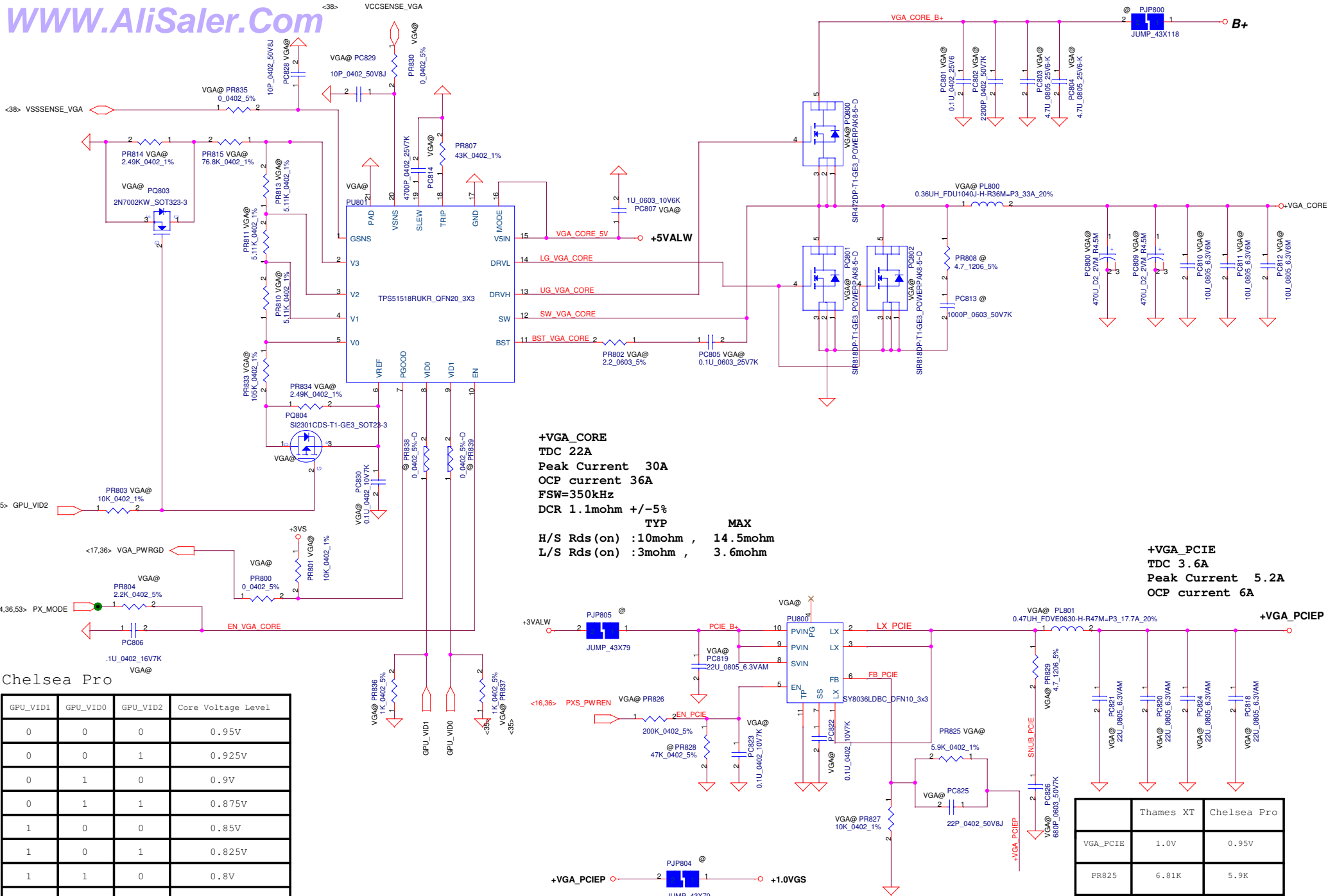


+VCC_GFXCORE_AXG
TDC 21.5A
Peak Current 33A
OCP current 40A
Load line -3.9mV/A
FSW=300kHz
DCR 1.1mohm +/-5%

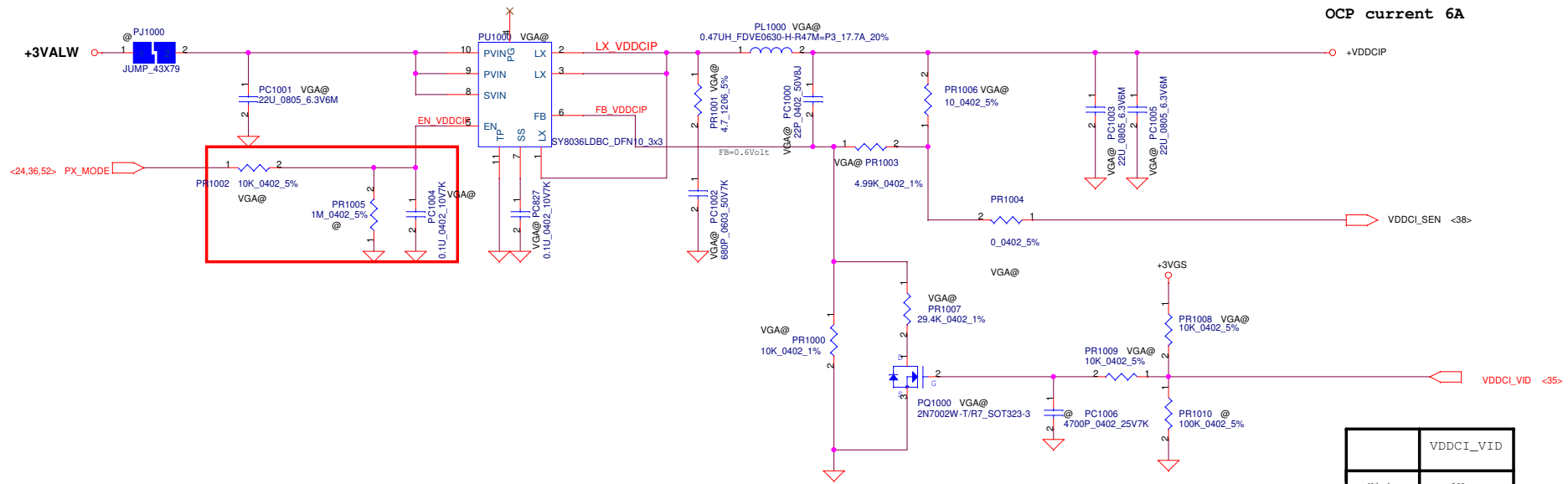
	TYP	MAX
H/S Rds(on)	:10mohm	:14.5mohm
L/S Rds(on)	:3mohm	:3.6mohm



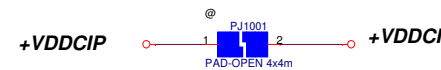
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				Size	Document Number	Rev	
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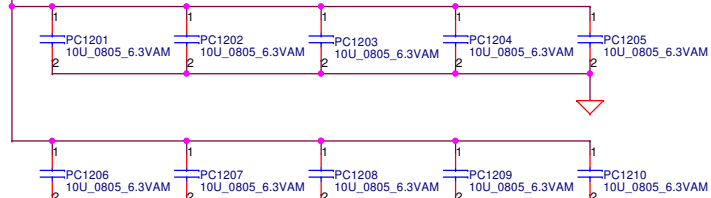
+VDDCI
TDC 2.8A
Peak Current 4A
OCP current 6A



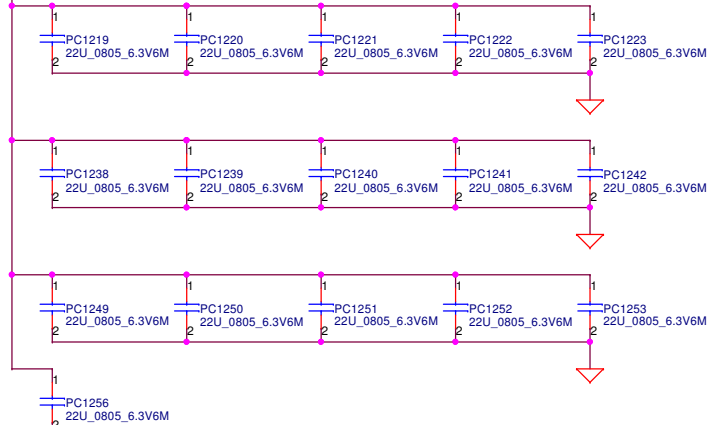
	VDDCI_VID
High	1V
Low	0.9V



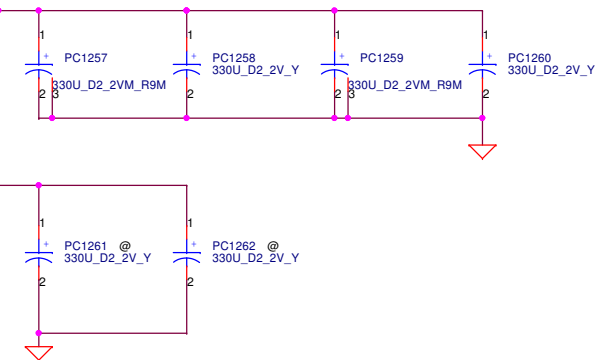
+VCC_CORE



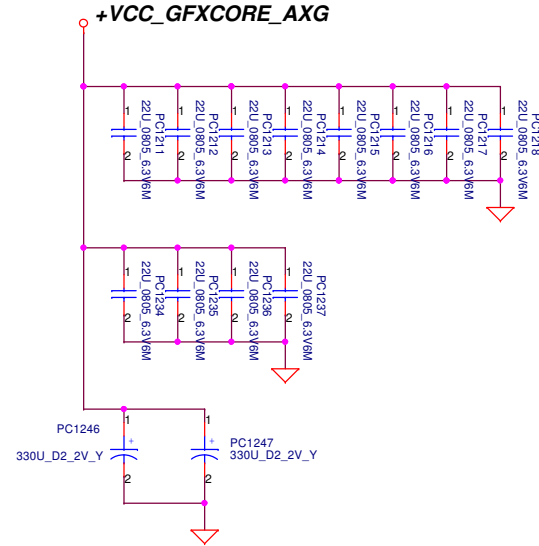
+VCC_CORE



+VCC_CORE



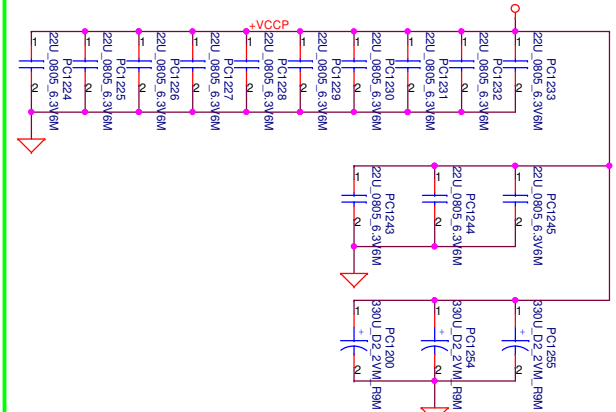
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

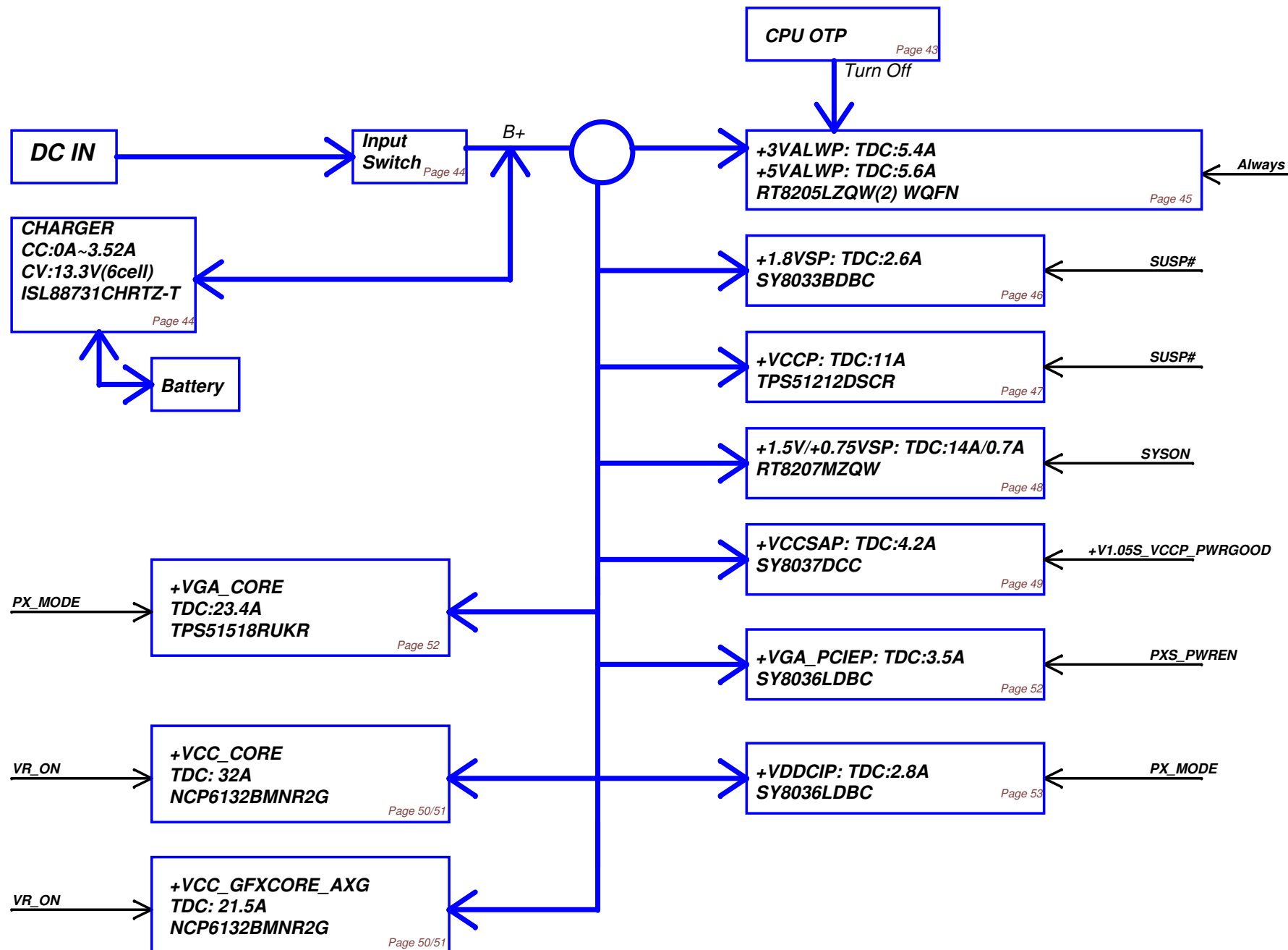
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+VCCP



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Power block



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