

# LCFC Confidential


## G Project M/B Schematics Document

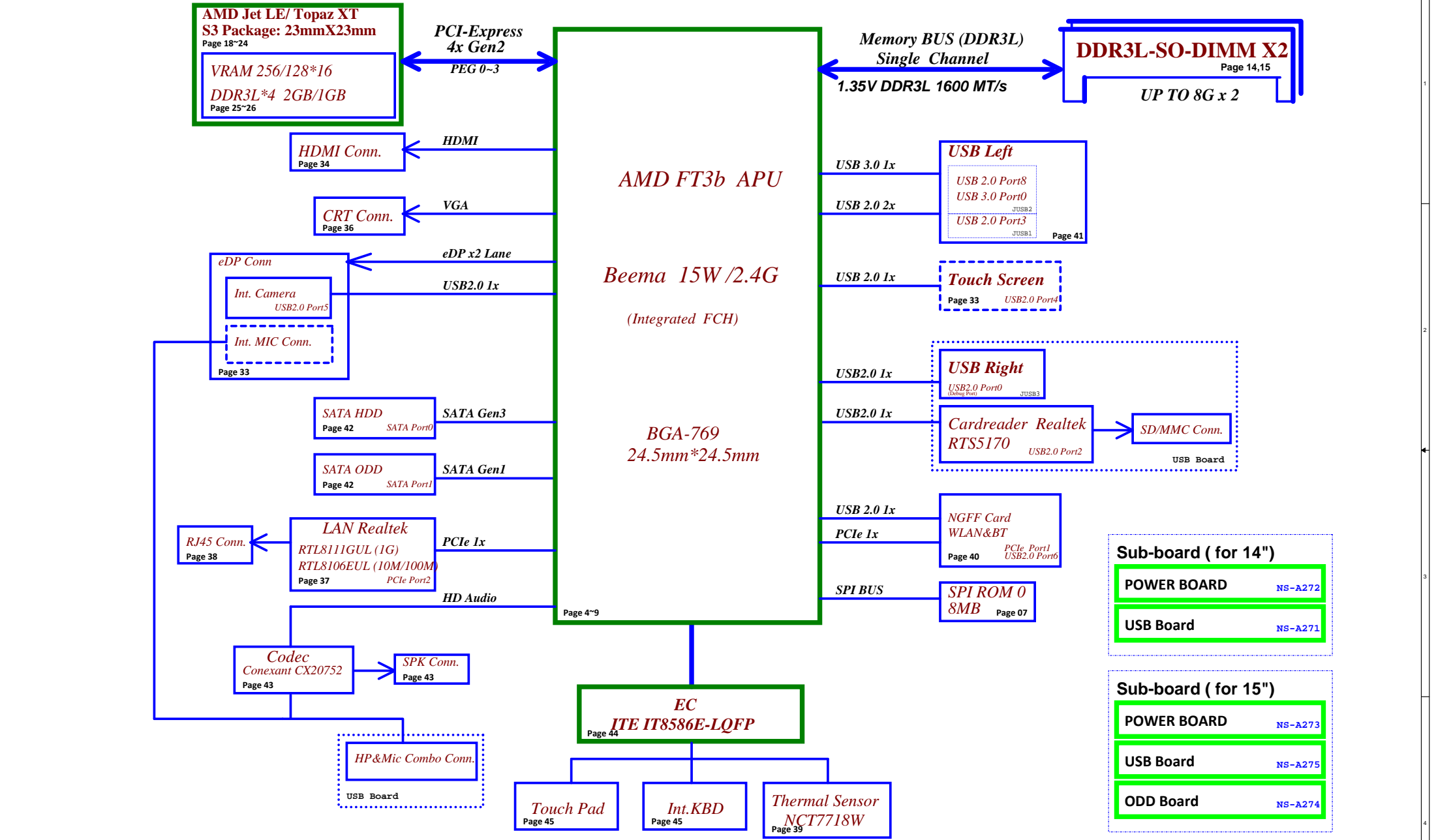
AMD FT3B Beema SOC with DDRIIL

AMD JET-LE

2014-1-3

REV:0.3

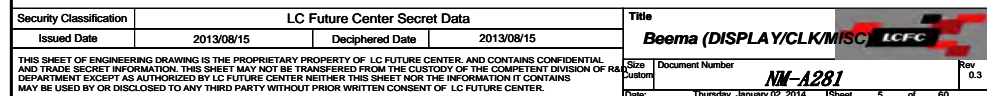
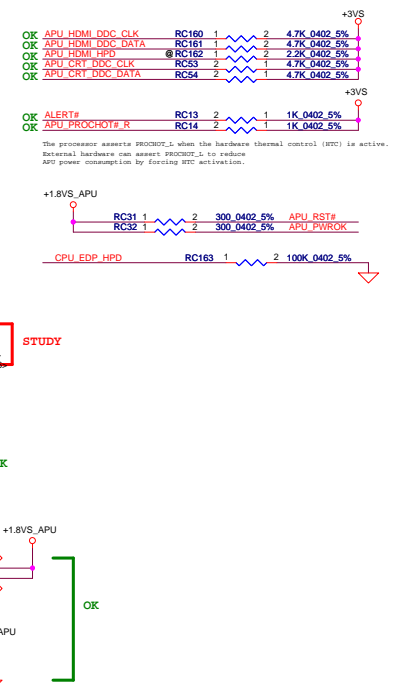
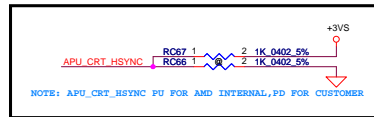
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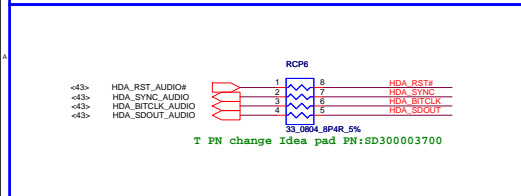
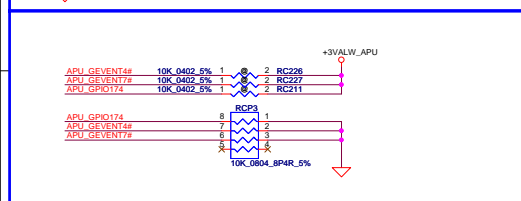
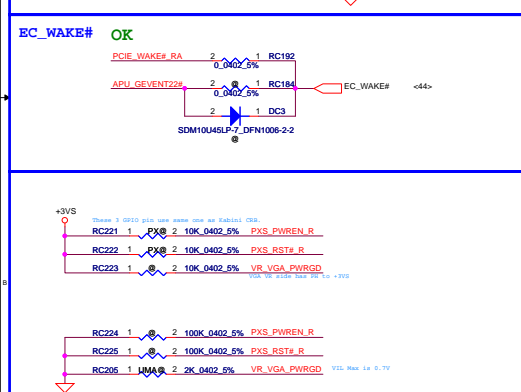
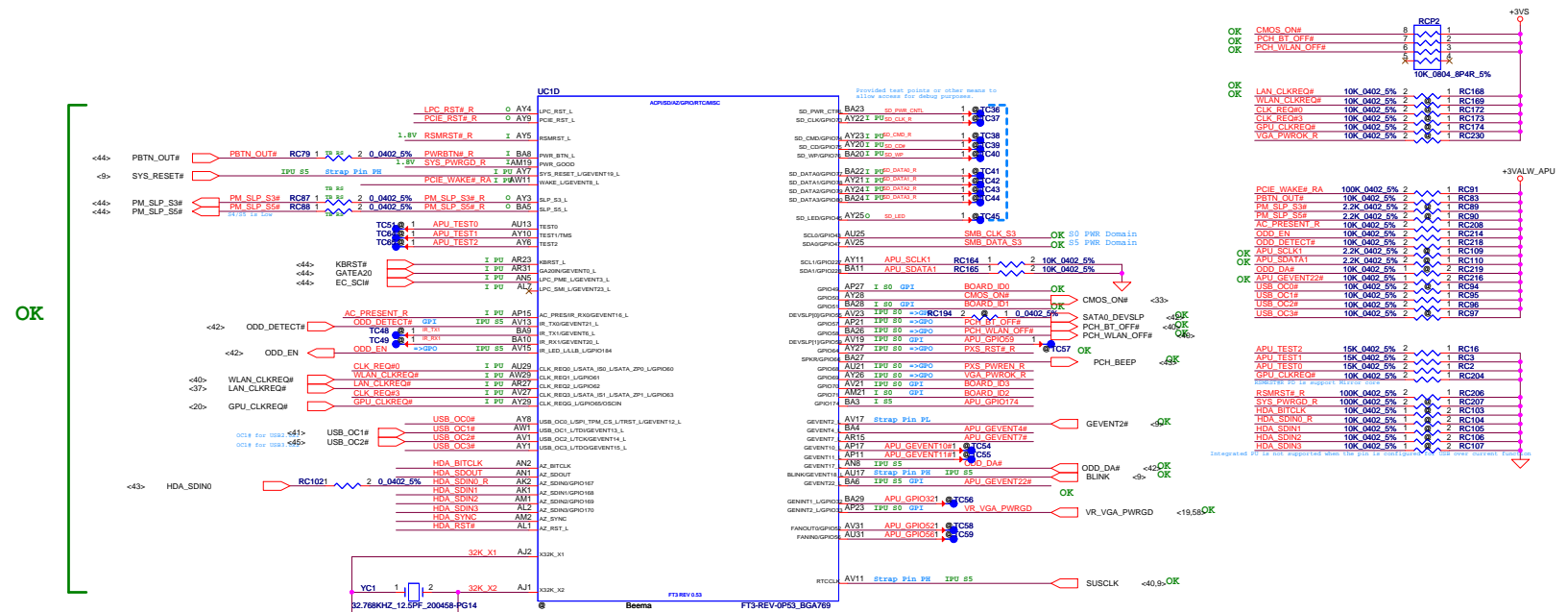
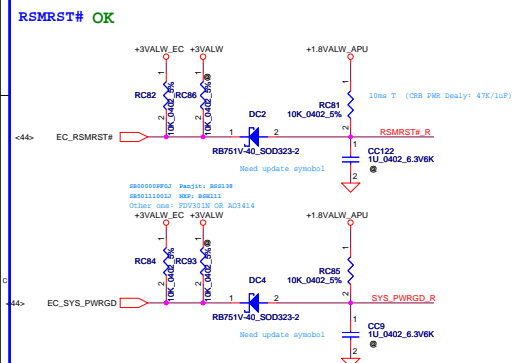
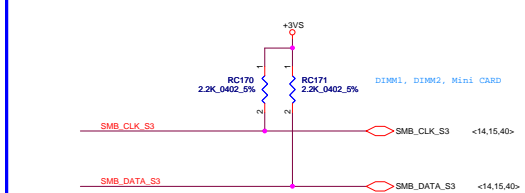
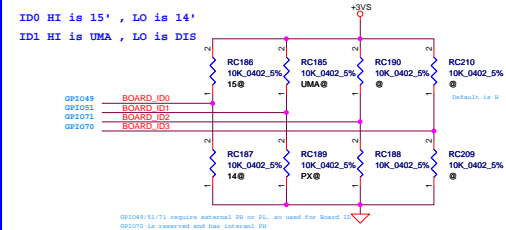
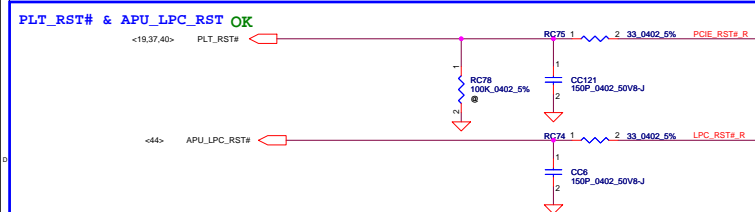






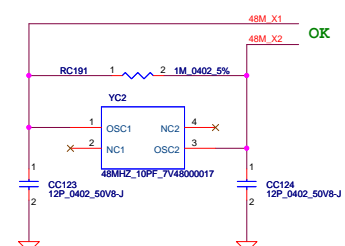
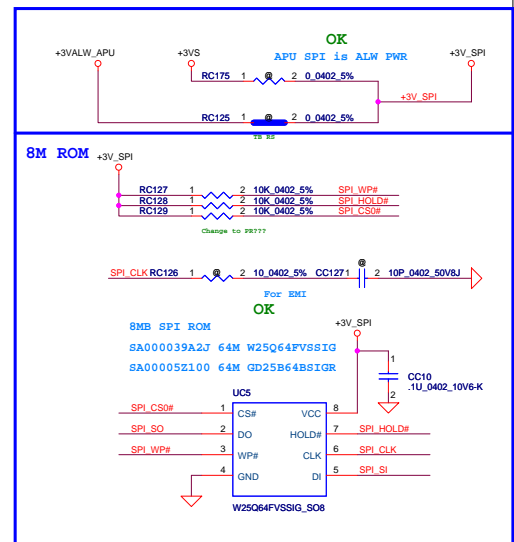
## Beema (DISPLAY/CLK/MISC)




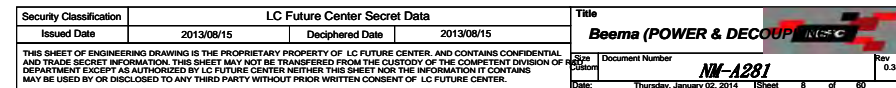


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48MHz/10pF Crystal



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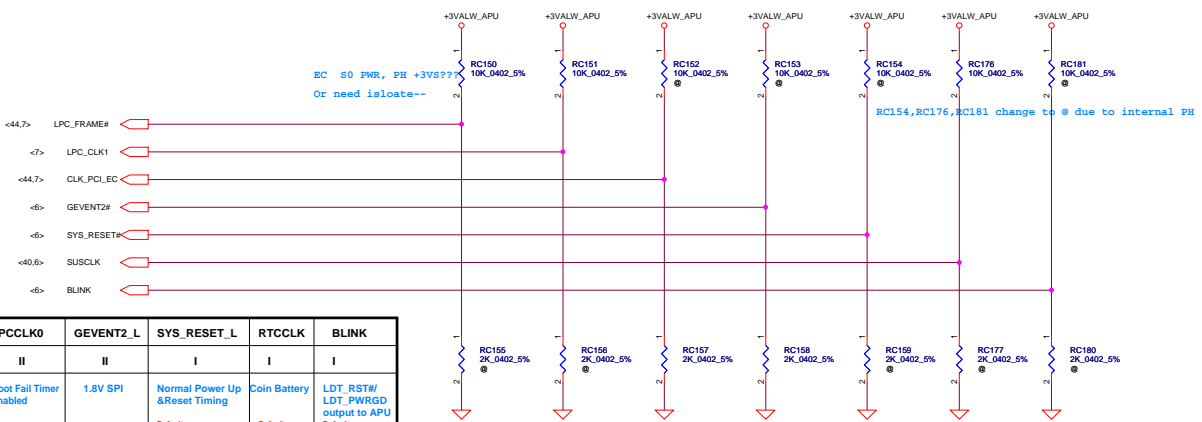





STRAP PINS


Signal	LFRAME_L	LPCCLK1	LPCCLK0	GEVENT2_L	SYS_RESET_L	RTCCLK	BLINK
Type	II	II	II	II	I	I	I
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled Default	1.8V SPI Default	Normal Power Up & Reset Timing Default	Coin Battery Default	LDT_RST#/ LDT_PWRGD output to APU Default
PULL LOW	LPC ROM	External CLK Gen	Boot Fail Timer Disabled Default	3.3V SPI Default	Reserved	Direct DC	Reserved


Type I straps become valid immediately after capture with the rising edge of RSMRST\_L.  
Type II straps become valid after PWR\_GOOD is asserted  
All Strap pins must be configured with either external pull-up or pull-down resistors.

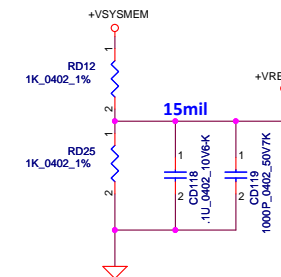
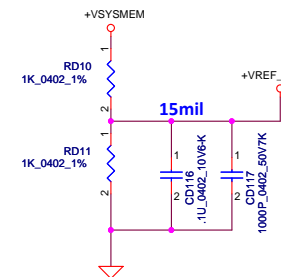
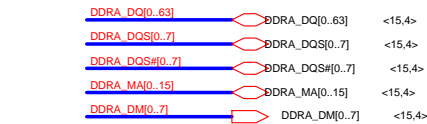
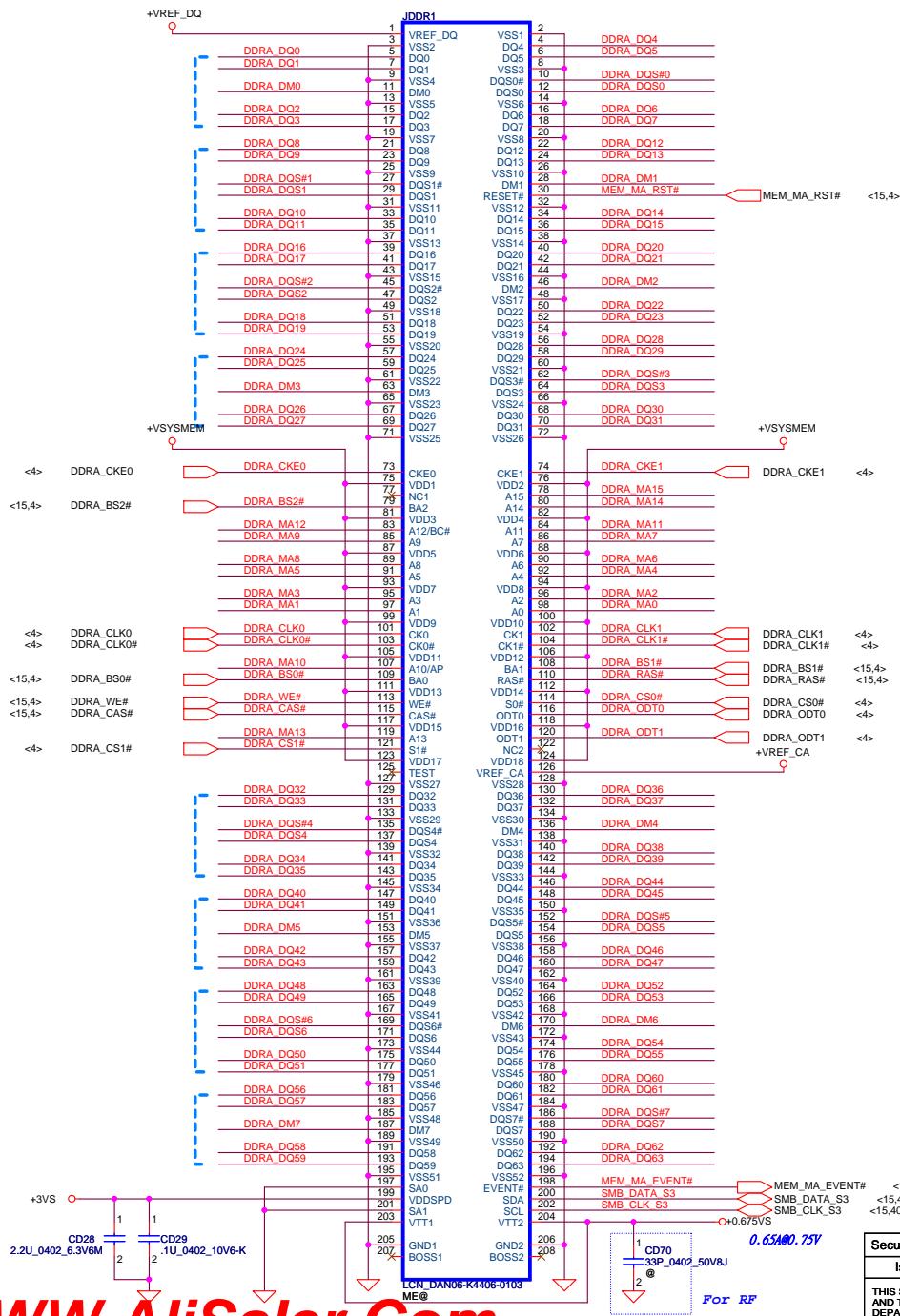


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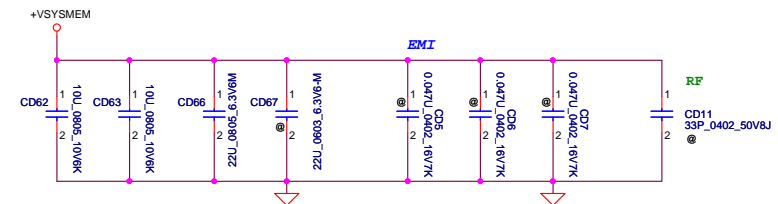
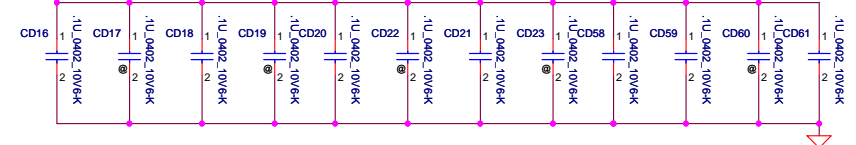
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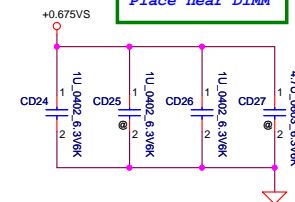
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**DDR3 SO-DIMM A**


**Layout Note:**  
**Place near DIMM1**



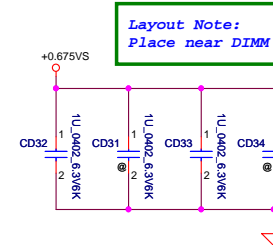
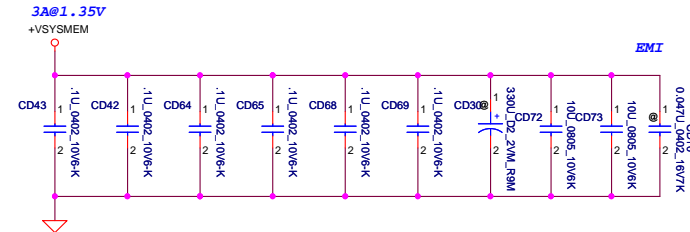
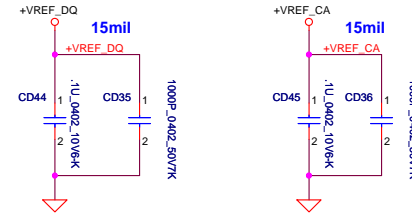
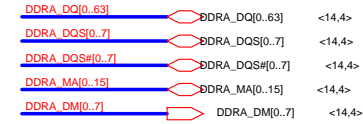
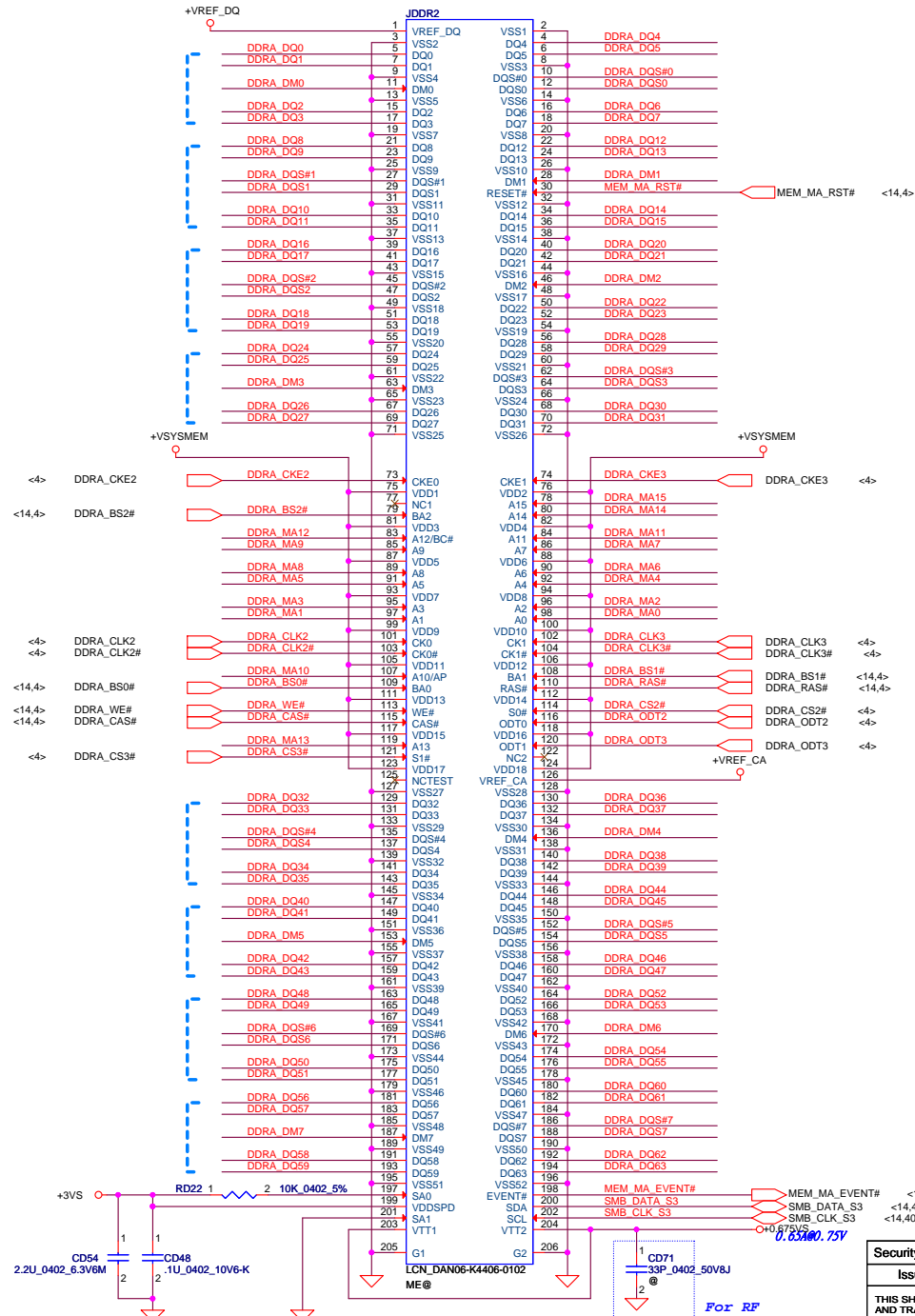
Layout Note:  
Place near DIMM



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# DDR3 SO-DIMM B



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C									
B									
A									





## VGA Note list need to be update!

### Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.

VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).

For power down, reversing the ramp-up sequence is recommended.

VDDR3(+3VGS)

VDDC(+VGA\_CORE)

VDDCI(+VGA\_CORE)

PCIE\_VDDC(+0.95VGS)

VDDR1(+1.5VGS)

VDD\_CT(+1.8VGS)

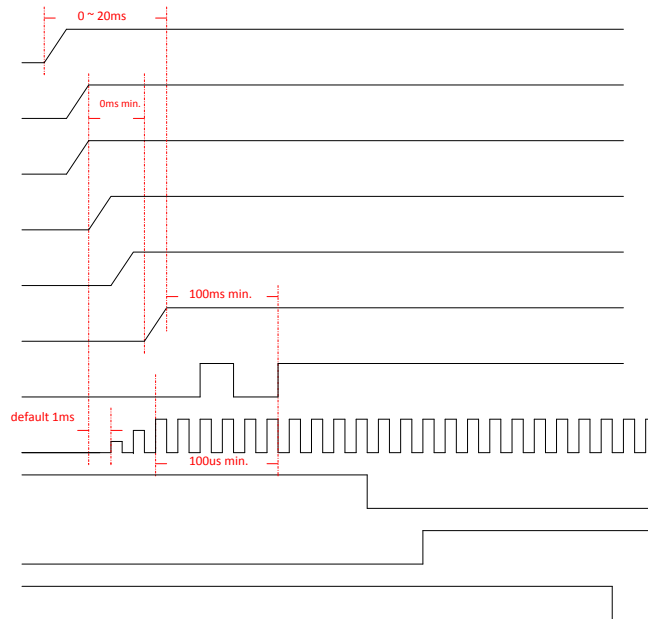
PERSTb(GPU\_RST#)

REFCLK(CLK\_PCIE\_VGA)

Straps Reset

Straps Valid

Global ASIC Reset

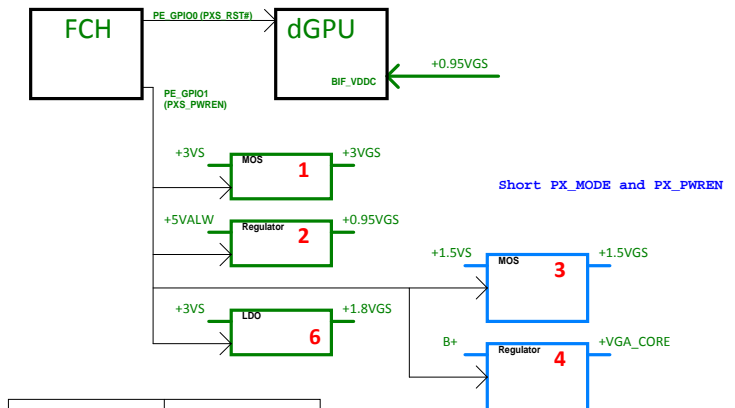


### Without BACO option :

PE\_GPIO0 : Low -> Reset dGPU ; High -> Normal operation  
PE\_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

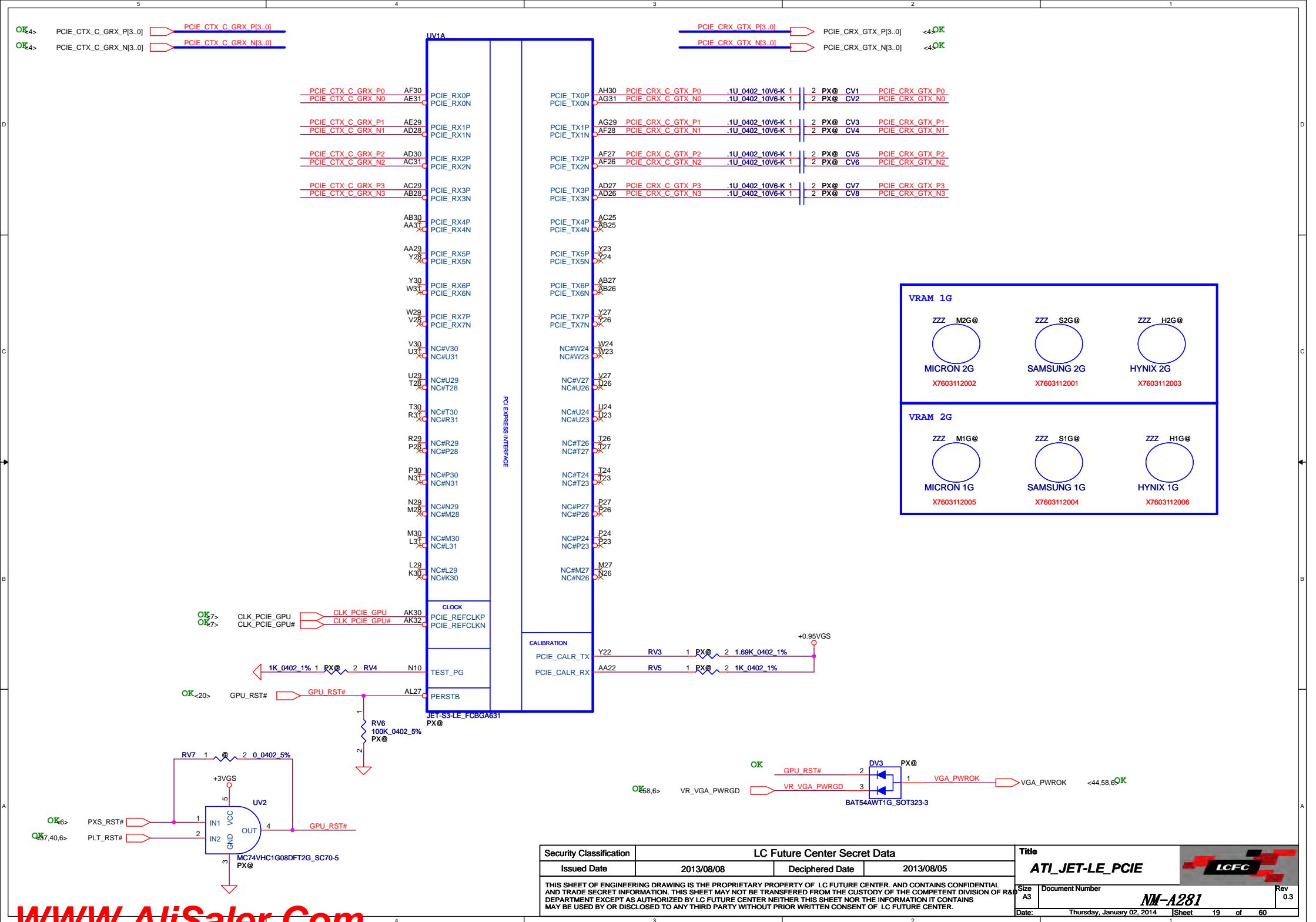
dGPU Power Pins	Voltage	Max current
VDD_CT, DP_VDDR, SPLL_PVDD, MPLL_PVDD, PCIE_PVDD, TSVDD, VDDR4, AVDD, VDD1DI	1.8V	1243mA
DP_VDDC, SPLL_VDDC, PCIE_VDDC, BIF_VDDC	0.95V	4560mA
VDDR3	3.3V	25mA
VDDR1	1.5V	1.5A
VDDC	0.8~1.125V	TBD
VDDCI	0.8~1.1V	8.8A

### PX5.5



Name	Pin Assignment
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192

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UV1F

NC\_VARY\_BL  
NC\_DIGON

AB11  
AB12

NC\_UPHYAB\_TMDPA\_TX0N  
NC\_UPHYAB\_TMDPA\_TX0P  
NC\_UPHYAB\_TMDPA\_TX1N  
NC\_UPHYAB\_TMDPA\_TX1P

AL15  
AK14  
AH16  
AJ15

NC\_UPHYAB\_TMDPA\_TX2N  
NC\_UPHYAB\_TMDPA\_TX2P

AL17  
AK16

NC\_UPHYAB\_TMDPA\_TX3N  
NC\_UPHYAB\_TMDPA\_TX3P

AH18  
AJ17

NC\_TXOUT\_L3P  
NC\_TXOUT\_L3N

AL19  
AK18

TMDP

NC\_UPHYAB\_TMDPB\_TX0N  
NC\_UPHYAB\_TMDPB\_TX0P

AH20  
AJ19

NC\_UPHYAB\_TMDPB\_TX1N  
NC\_UPHYAB\_TMDPB\_TX1P

AL21  
AK20

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NC\_UPHYAB\_TMDPB\_TX2P

AH22  
AJ21

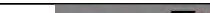
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AK22

NC\_TXOUT\_U3P  
NC\_TXOUT\_U3N

AK24  
AJ23

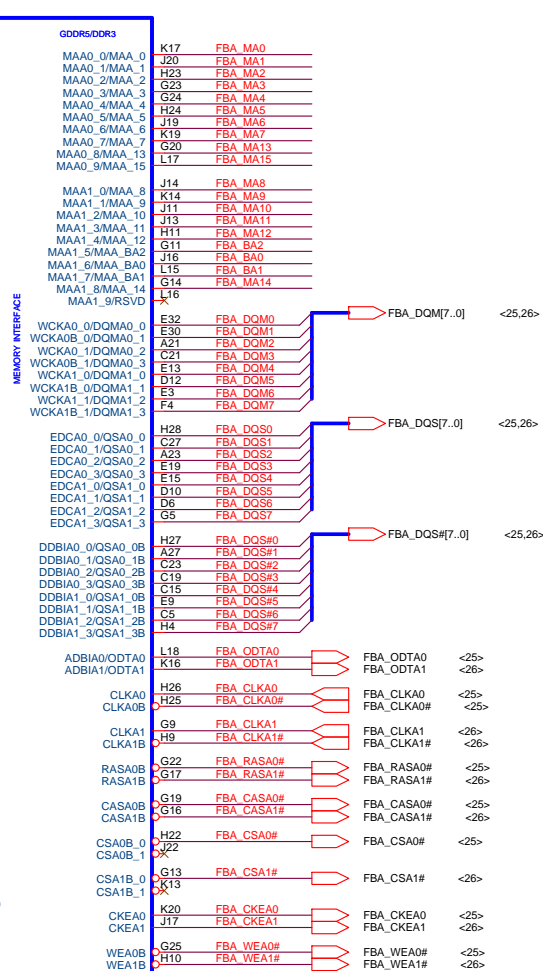
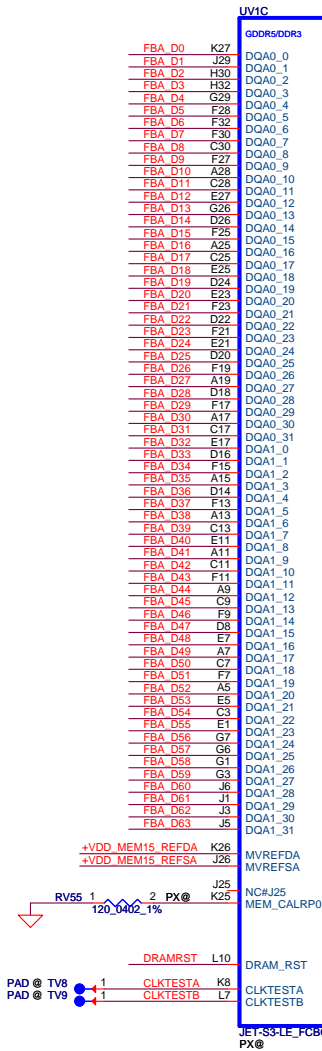
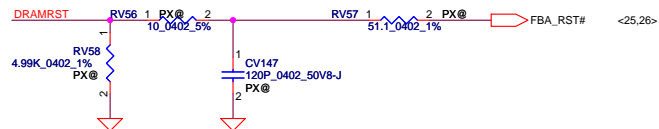
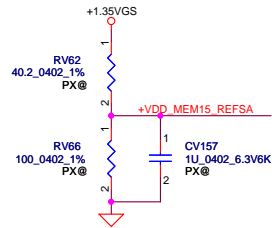
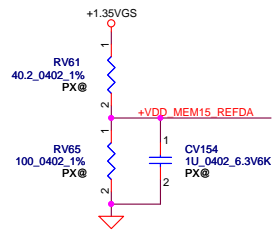
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FBA\_MA[15..0] FBA\_MA[15..0] <25,26>  
FBA\_BA[2..0] FBA\_BA[2..0] <25,26>

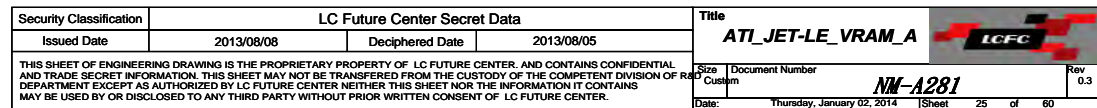


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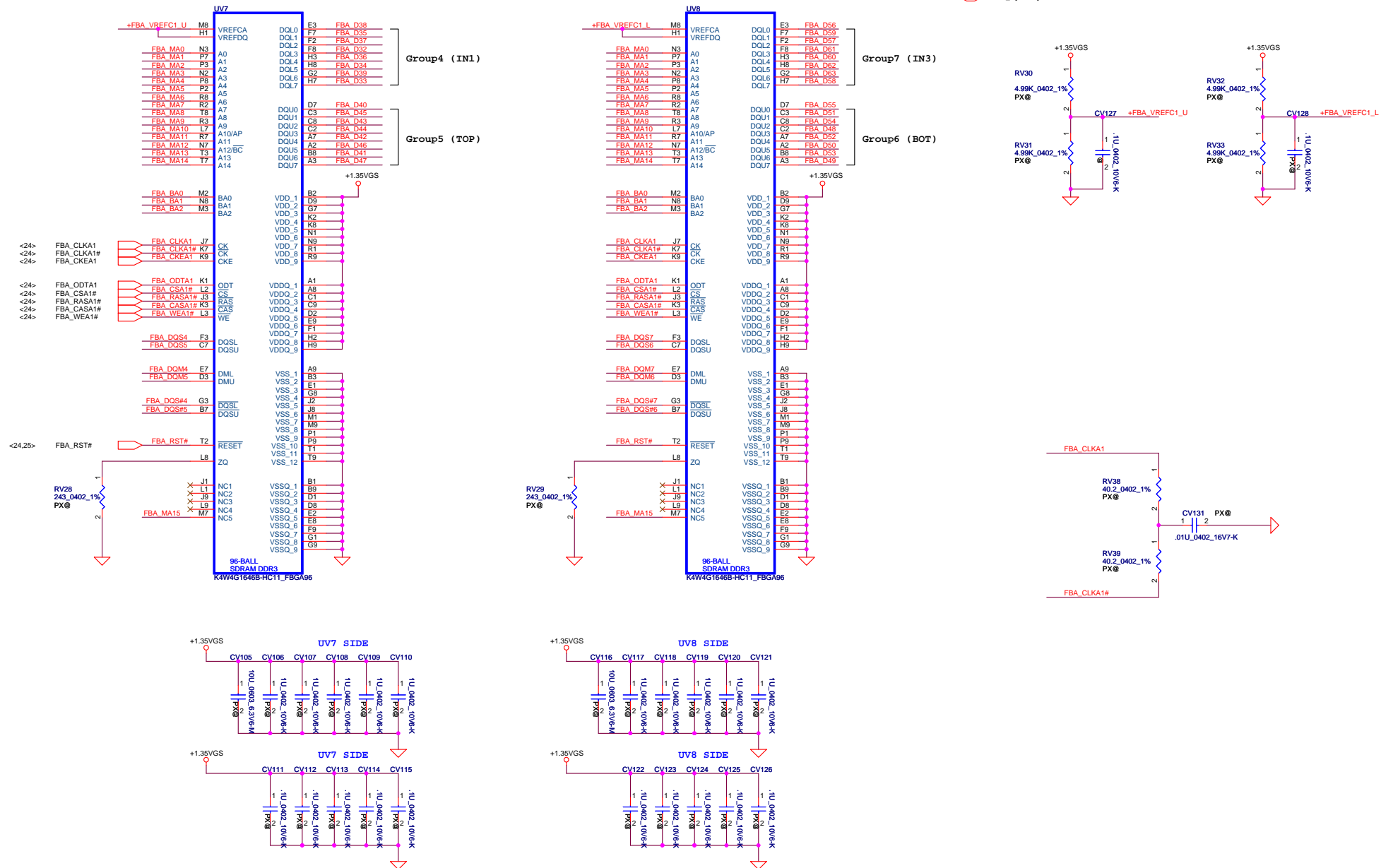
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Device	VRAM	VRAM Size	VRAM Size
FBA_MA[15..0]	<24,26>	ACLUS swap the VRAM Data @ 08/26	VRAM 8 pcs change to 4 pcs @ 09/26
FBA_BA[2..0]	<24,26>		
FBA_DQS[3..0]	<24>		
FBA_DQM[3..0]	<24>		
FBA_DQS#[3..0]	<24>		
FBA_D[31..0]	<24>		



### Memory Partition A - Upper 32 bits






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D				D																										
C				C																										
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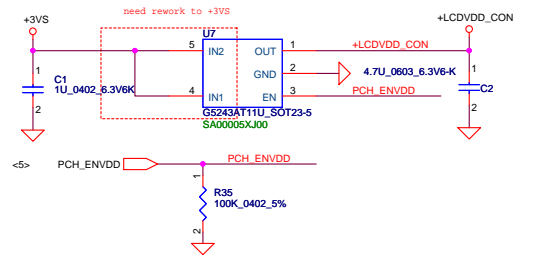


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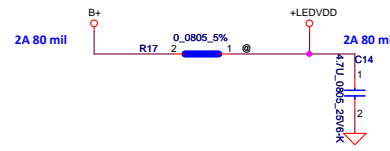
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## LCD POWER CIRCUIT OK

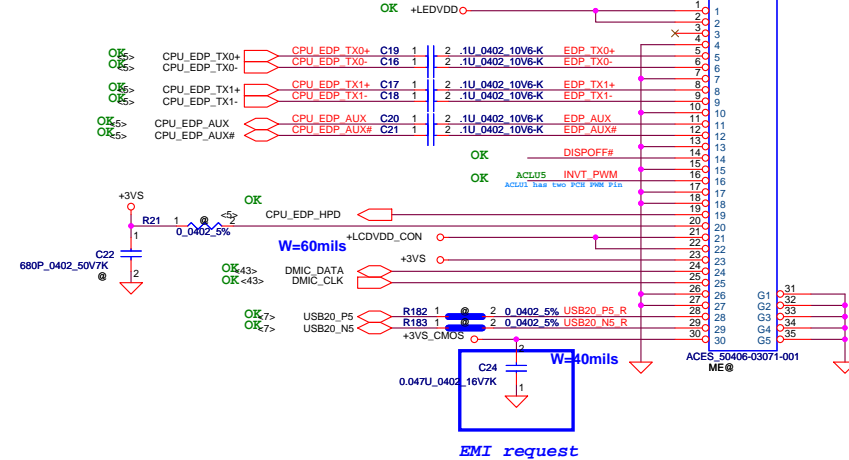
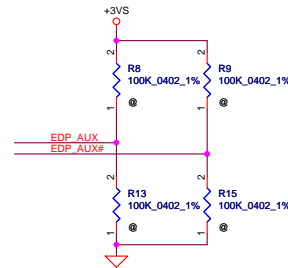
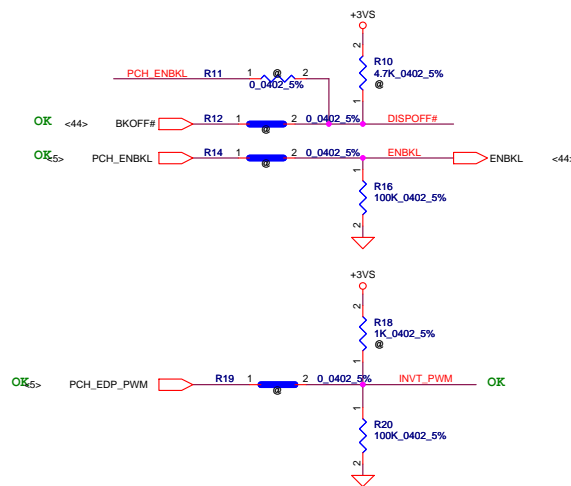
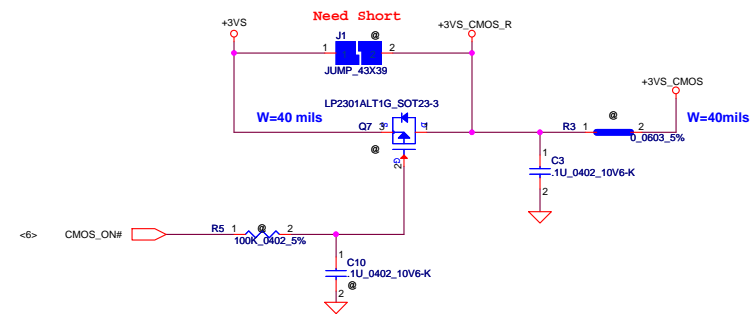


## B+ to +LEDVDD POWER OK

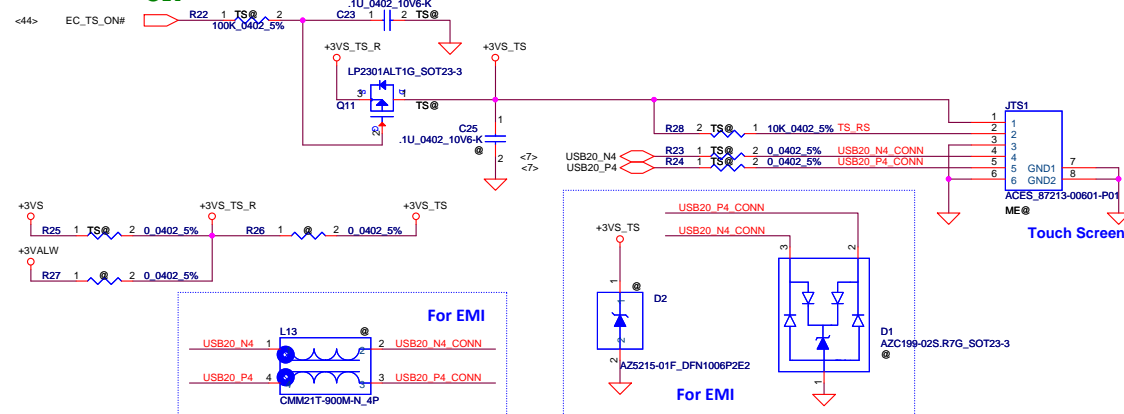


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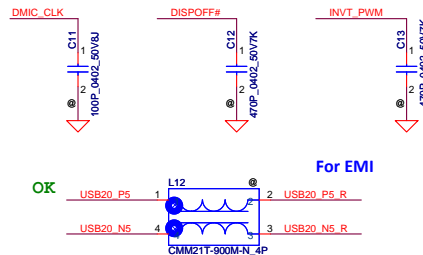
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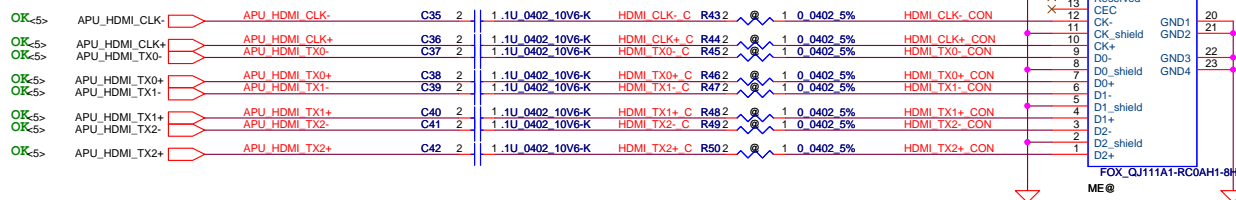
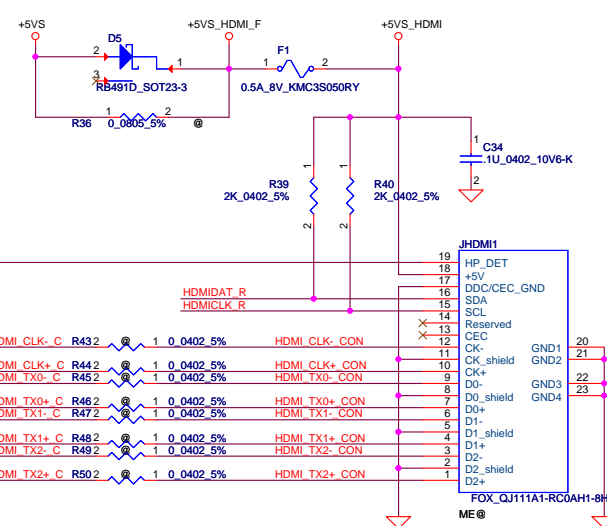
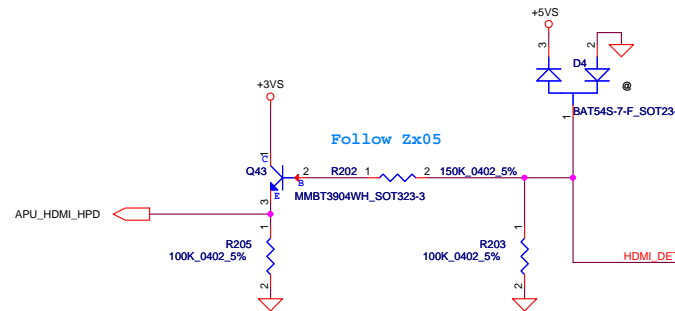
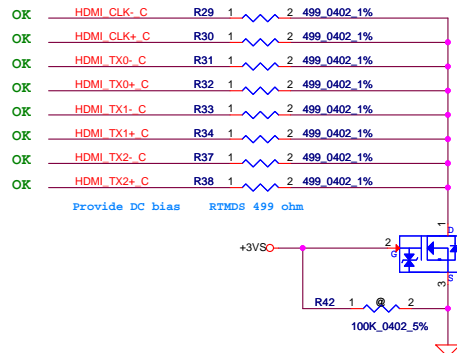
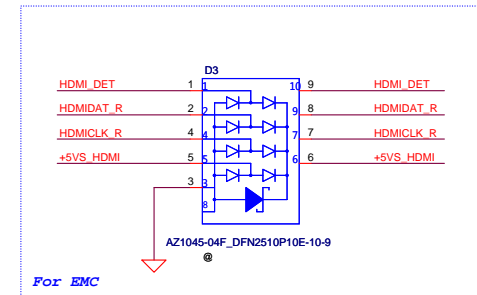
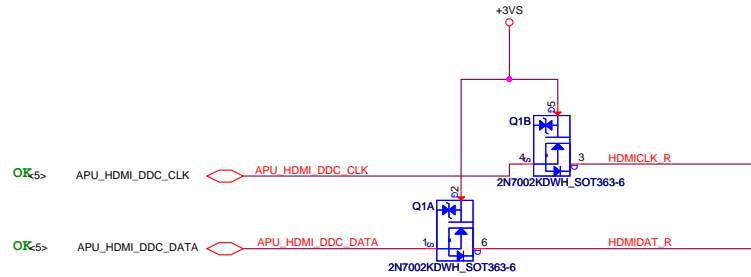
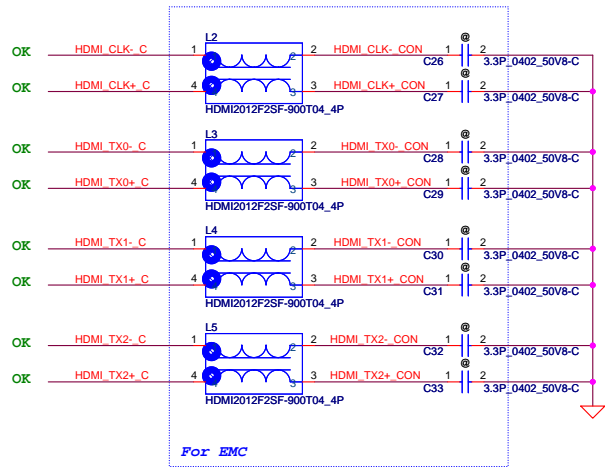
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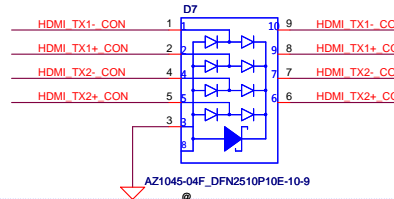
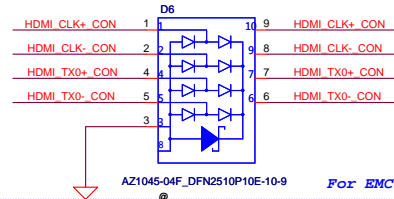
## EMI request



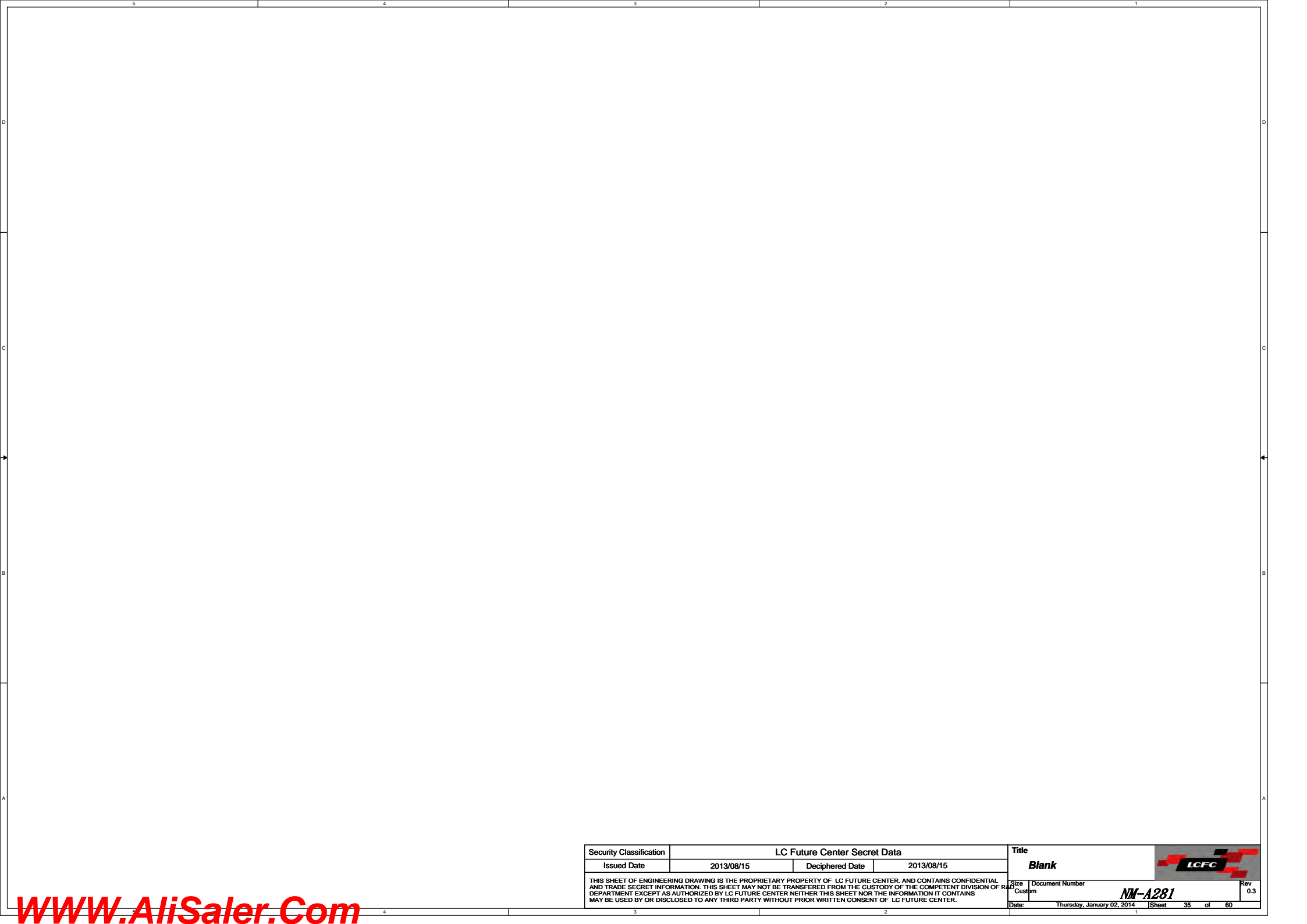
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				Size		Document Number	
				Custom		NM-A281	
				Date:		Thursday, January 02, 2014	
				Sheet		33 of 60	




Close to JHDMI1

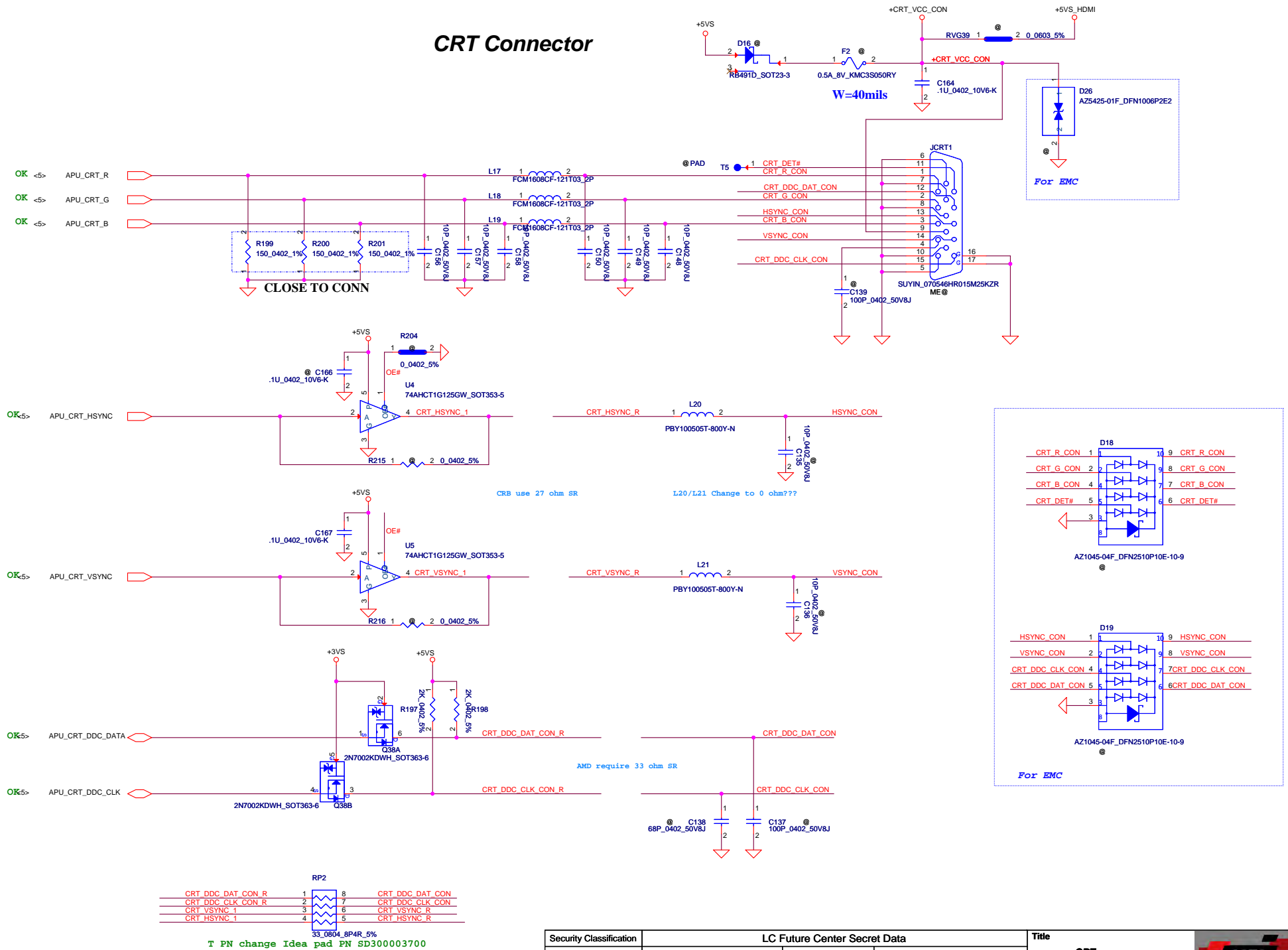



Security Classification				LC Future Center Secret Data		Title		HDMI_CONN	
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Issued Date	2013/08/15	Deciphered Date	2013/08/15		Blank		
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					Custom	NM-A281	0.3
					Date:	Thursday, January 02, 2014	Sheet 35 of 60

# CRT Connector

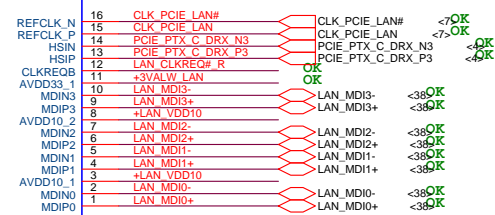
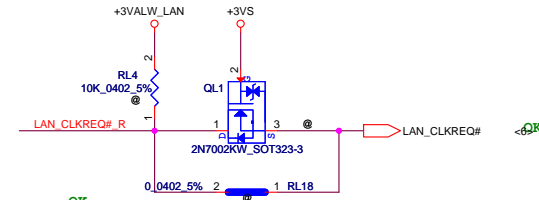
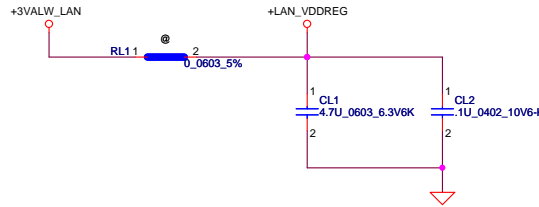
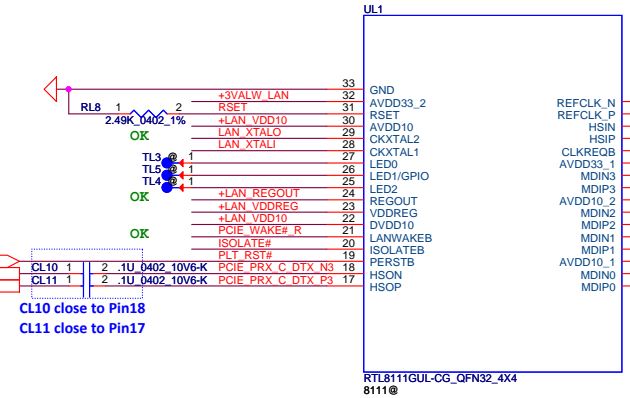
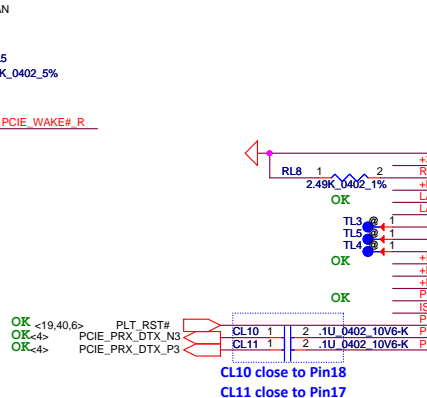
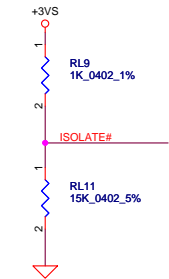
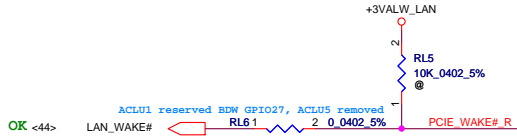
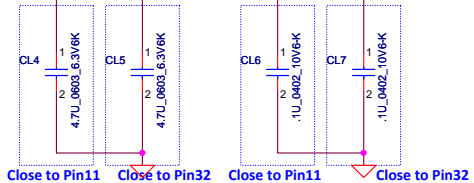


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Size	Custom	Document Number	NM-A281			Rev 0.3
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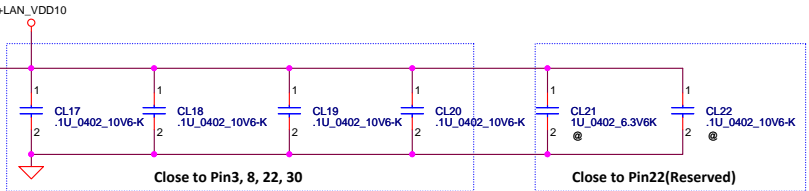
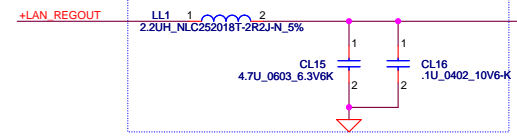
+3VALW TO +3VALW\_LAN

+3VALW\_LAN rising time (10%~90%):  
0.5ms~spec~100ms

width : 40 mils

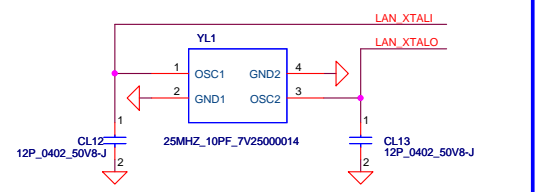


For RTL8111GUL/RTL8106EUL (SWR mode)



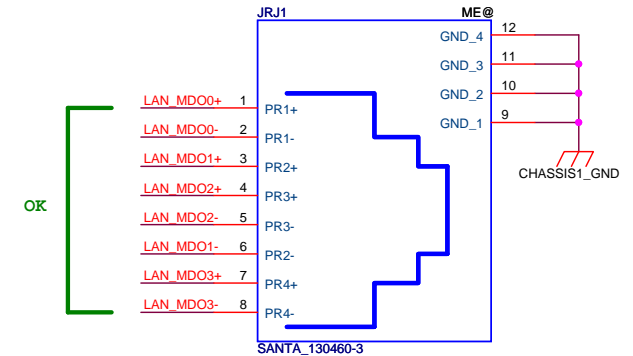
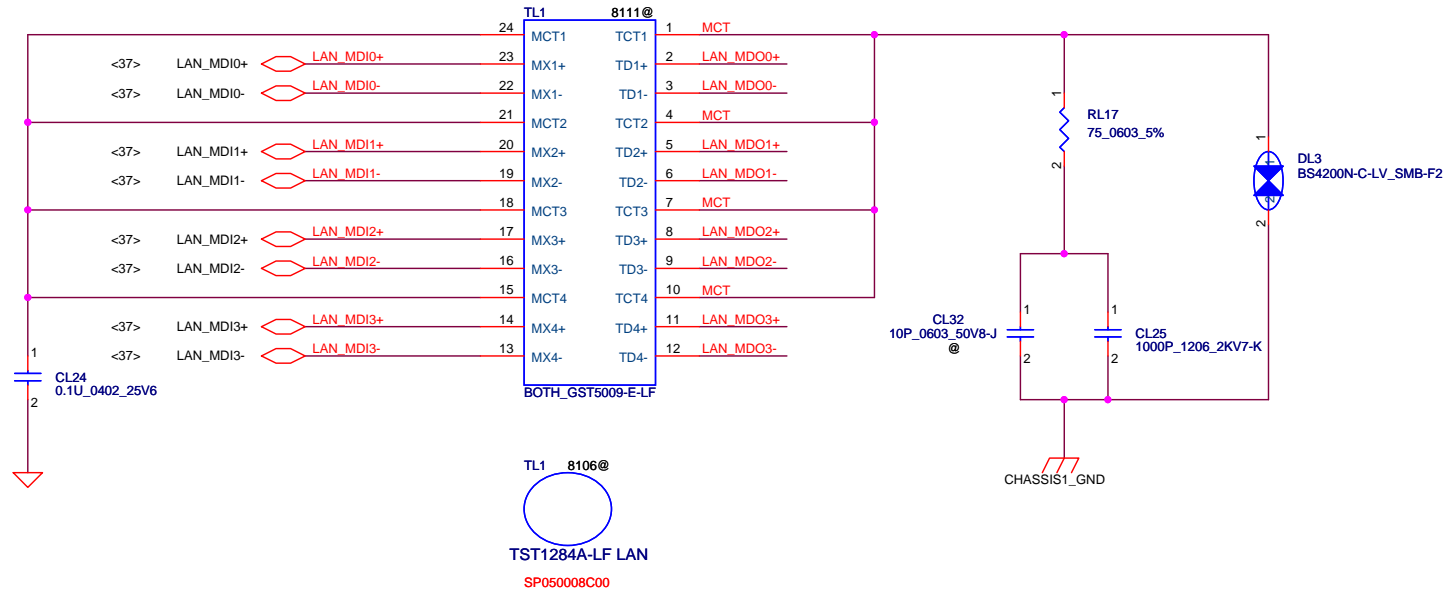
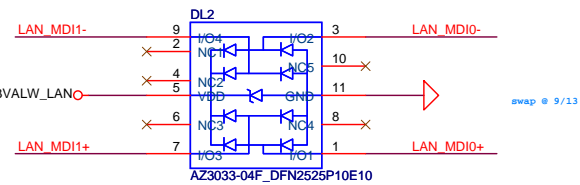
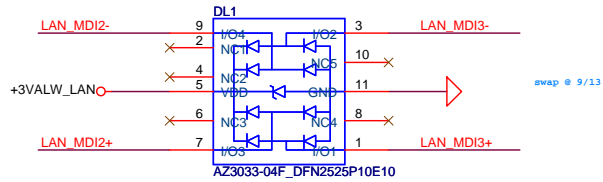
Layout Note: LL1 must be within 200mil to Pin36,  
CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil

LAN ROM OK



Security Classification	LC Future Center Secret Data			Title	LAN_RTL8111GUL/RTL8106EUL	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size	Document Number	Rev
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DL1/DL2  
1'S PN:SC300003M00

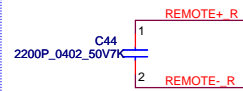


Security Classification				LC Future Center Secret Data				Title		LAN_Transformer	
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										NM-A281	
										Rev	
										0.3	
										Date:	
										Thursday, January 02, 2014	
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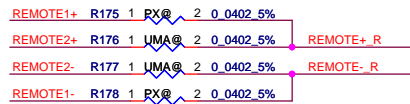
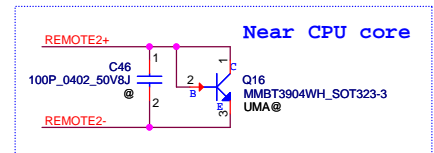
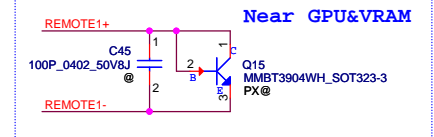
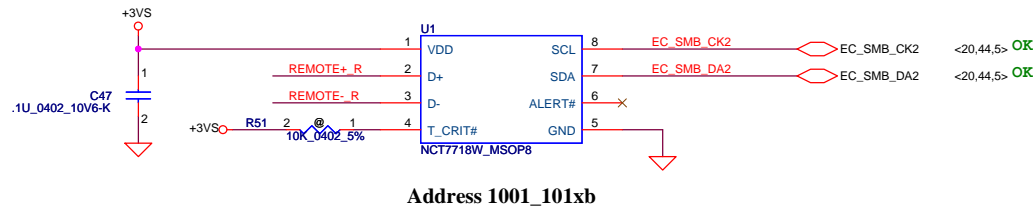


Close to U1



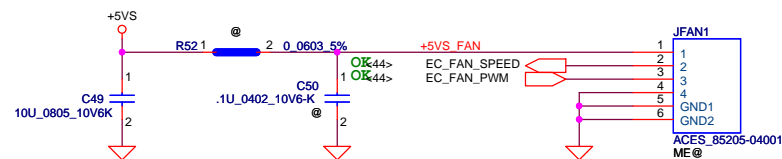
SMSC thermal sensor  
placed near DIMM

OK



REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

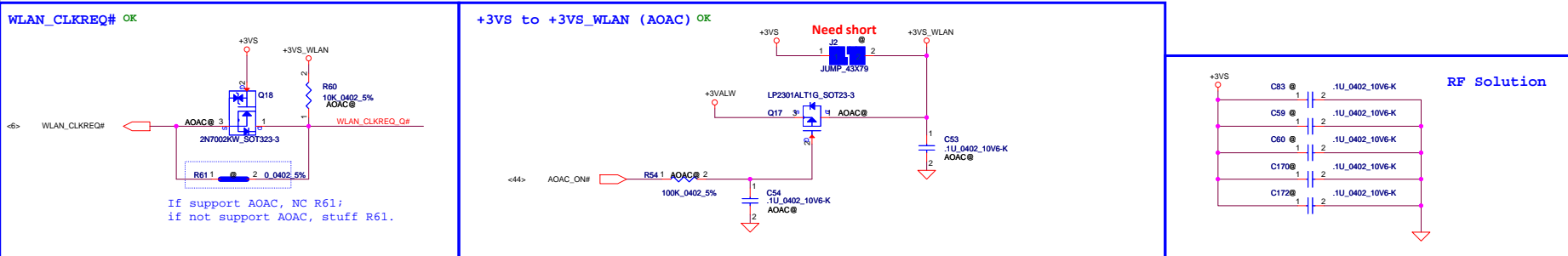
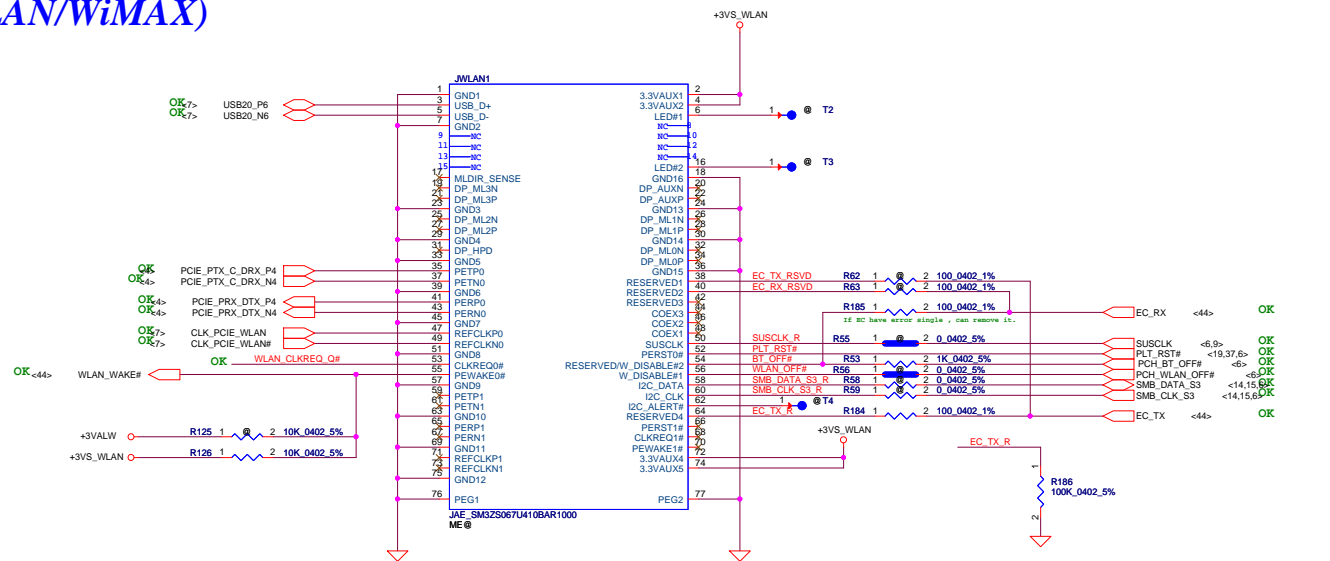
FAN Conn



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Thermal sensor/FAN CONN	
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				Date:	Thursday, January 02, 2014
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				Rev	0.3

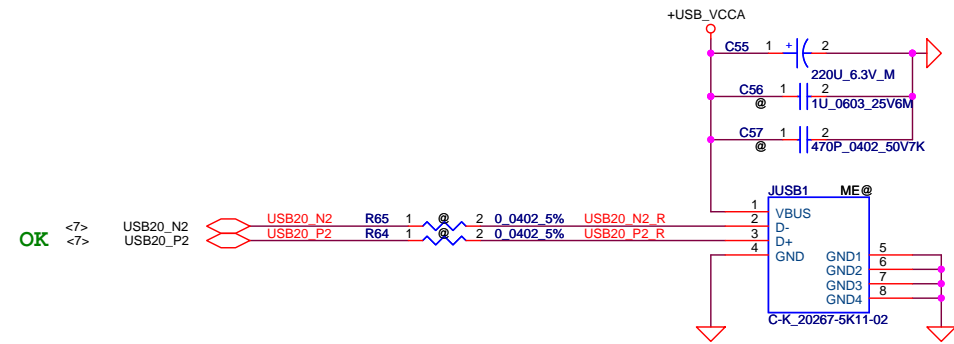
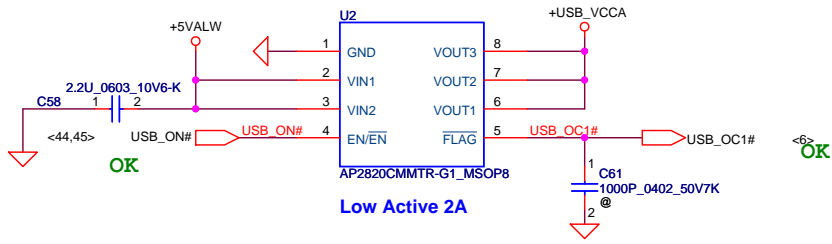


# Mini-Express Card(WLAN/WiMAX)

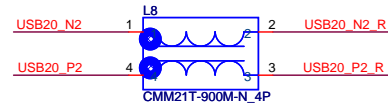




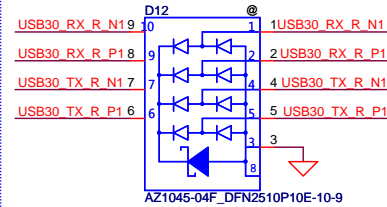
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OK

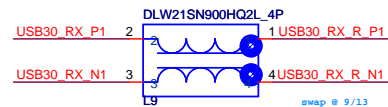


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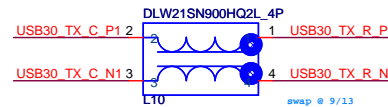


For EMC

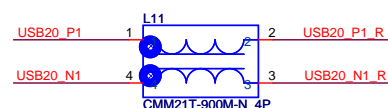
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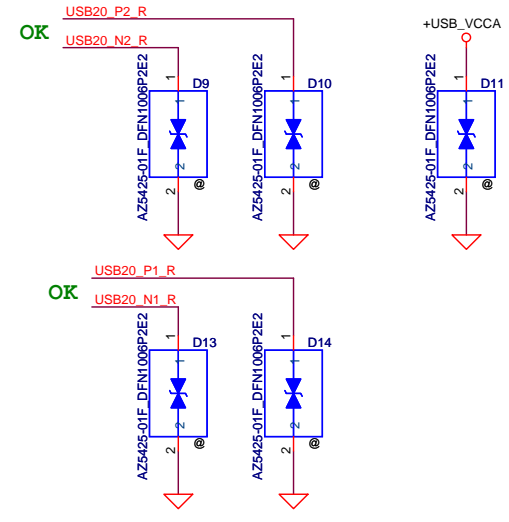
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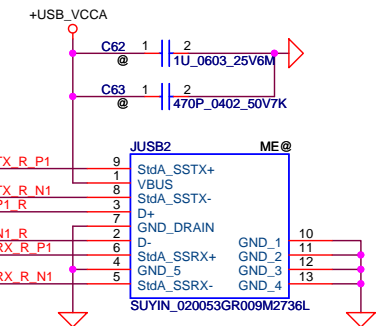
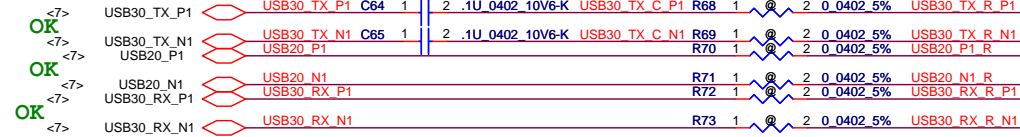
OK



For EMC

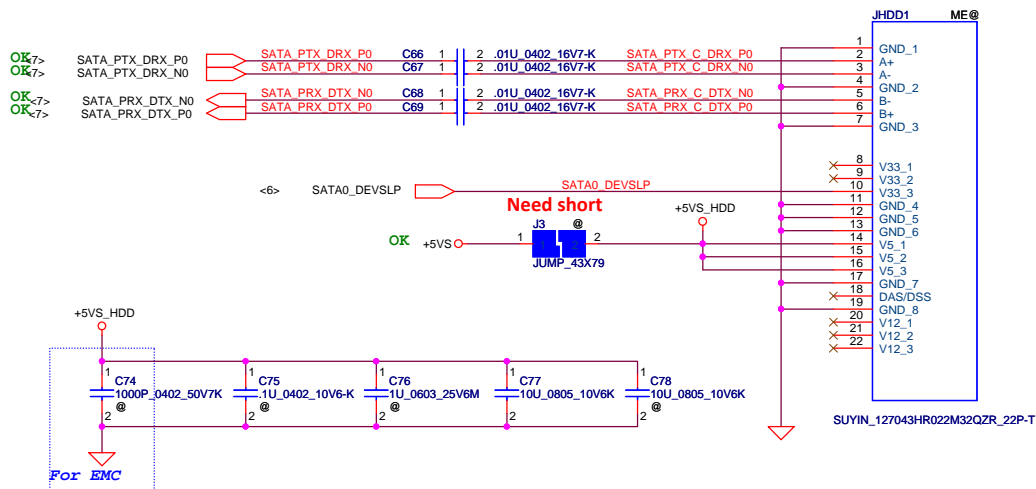


OK

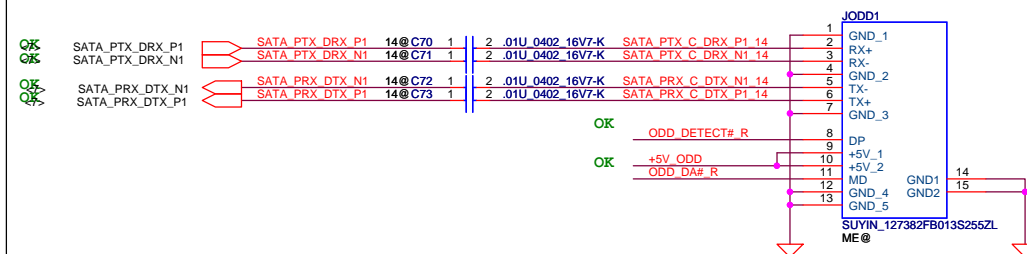


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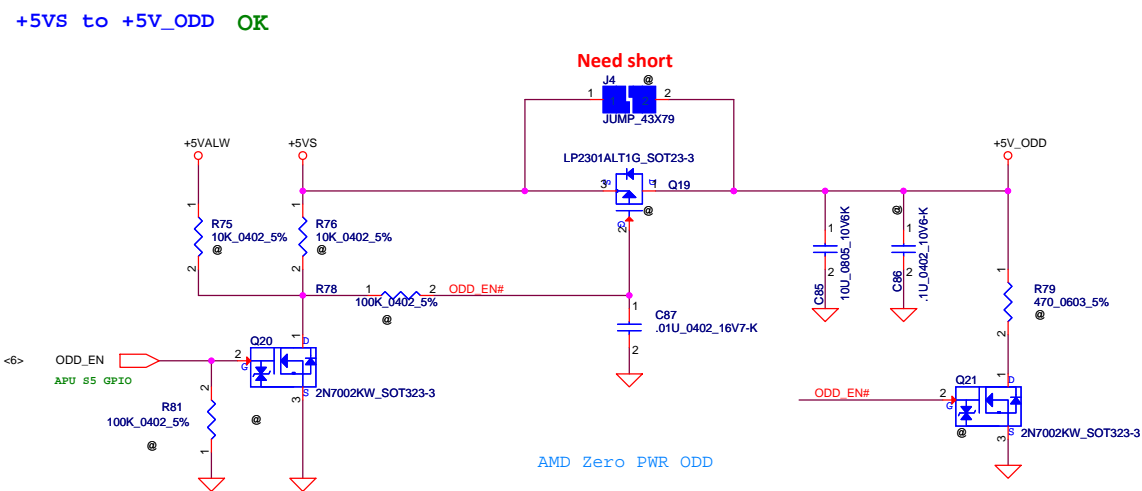
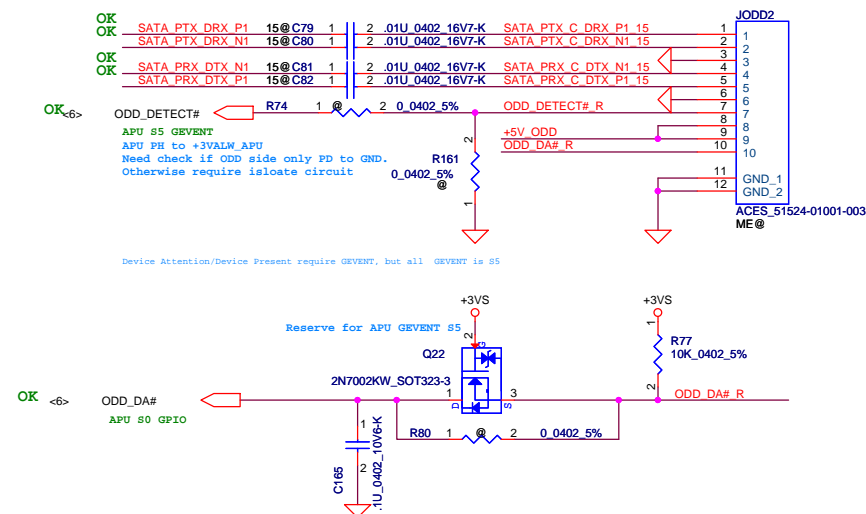
Title		LCFC	
USB2.0/USB3.0 PORT (LEFT)		Rev 0.3	
Size	Document Number	Date	
Custom	NM-A281	Thursday, January 02, 2014	
Sheet		41 of 60	


**SATA HDD Conn.**

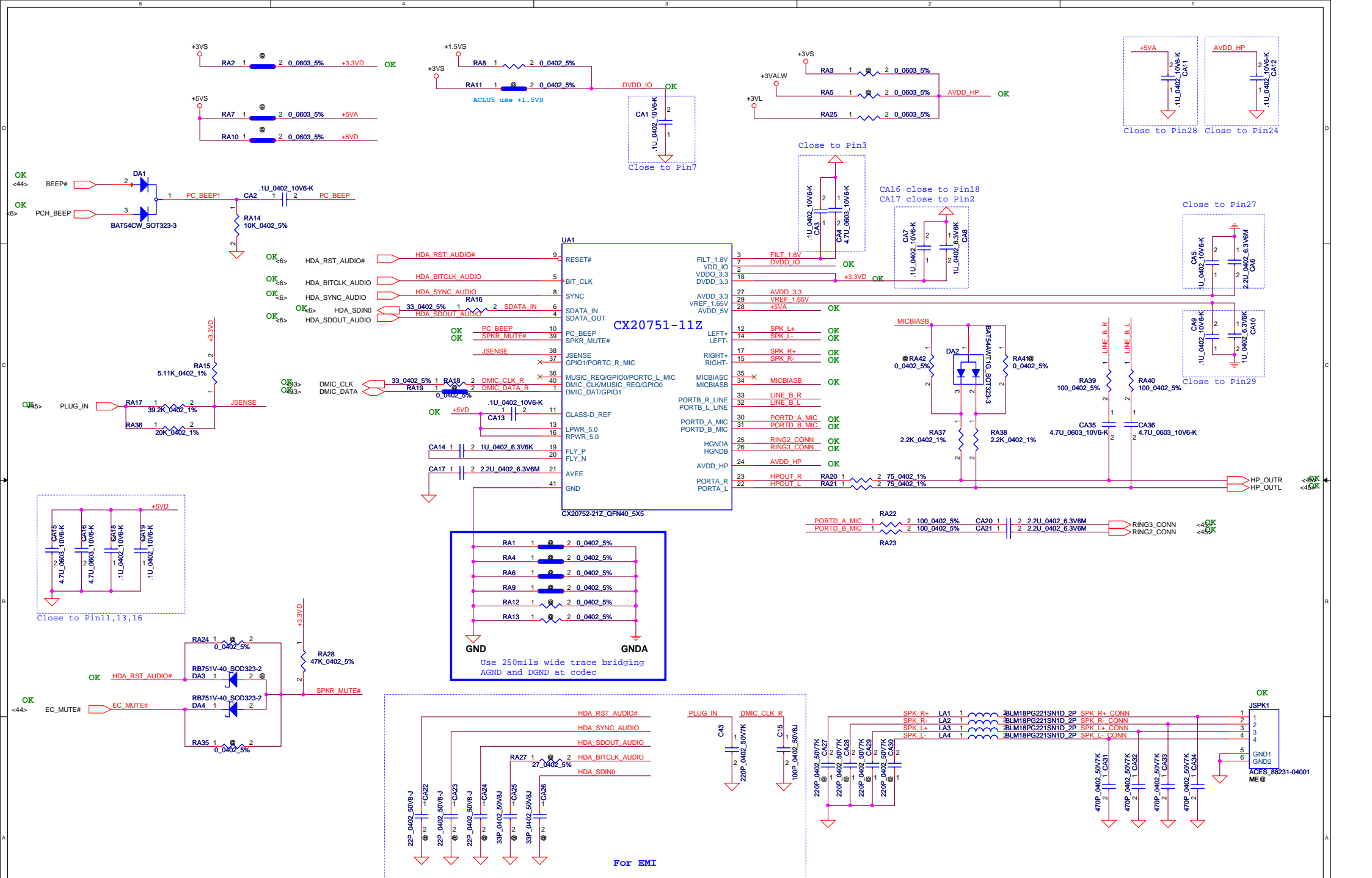
**FOR 14"  
SATA ODD Conn.**



**FOR 15"**  
**SATA ODD FFC Conn**

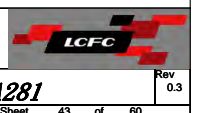


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				Custom	NM-A281	0.	
Date:				Thursday, January 02, 2014	Sheet	42	of 60



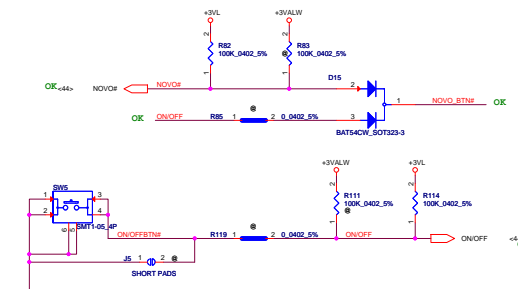
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Codec_CX20752		Document Number	Custom
Date		Thursday, January 02, 2014	Sheet 43 of 60
Rev		0.3	



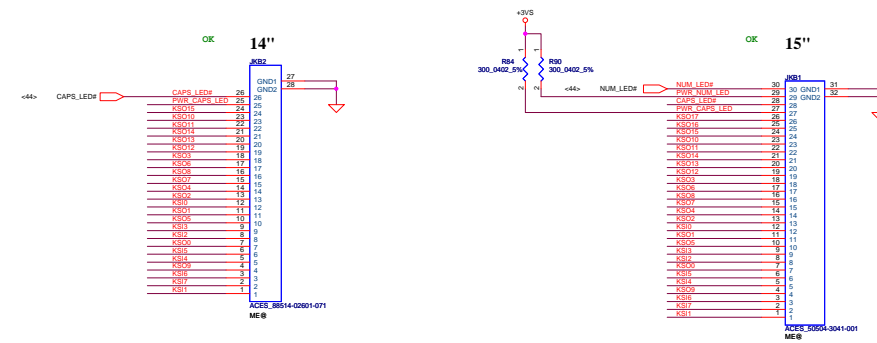
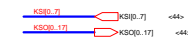


## ON/OFF switch

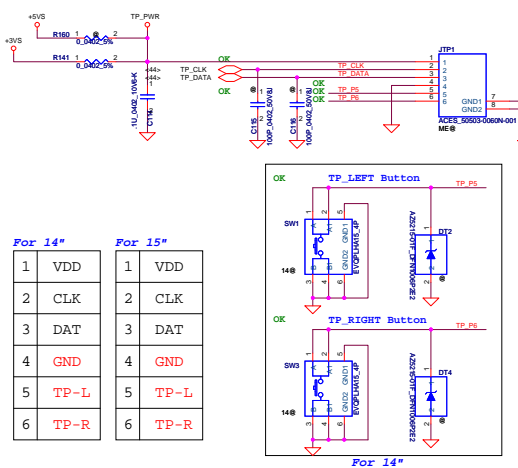


TP/B Connector

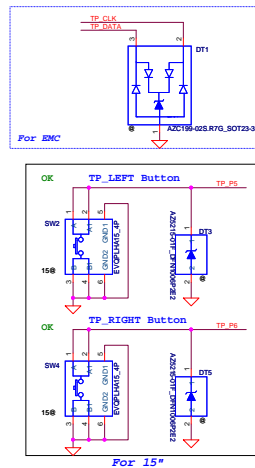
## K/B Connector



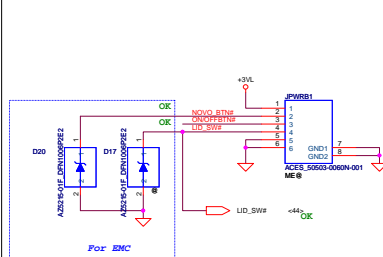
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KB_1 KS11_14	KS00_15
KB_2 KS17_14	KS12_15
KB_3 KS16_14	KS13_15
KB_4 KS09_14	KS05_15
KB_5 KS14_14	KS01_15
KB_6 KS15_14	KS02_15
KB_7 KS00_14	KS04_15
KB_8 KS12_14	KS03_15
KB_9 KS13_14	KS07_15
KB_10 KS05_14	KS08_15
KB_11 KS01_14	KS06_15
KB_12 KS10_14	KS03_15
KB_13 KS02_14	KS01_15
KB_14 KS04_14	KS01_15
KB_15 KS07_14	KS01_15
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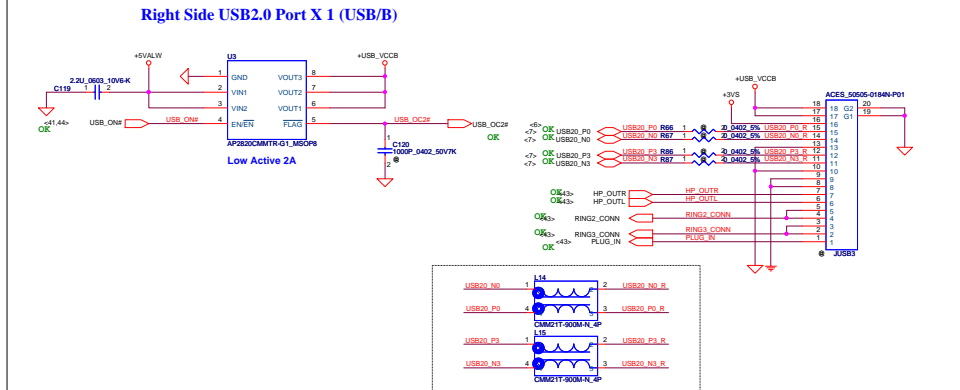
For 14"	For 15"
1 VDD	1 VDD
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 GND
5 TP-L	5 TP-L
6 TP-R	6 TP-R



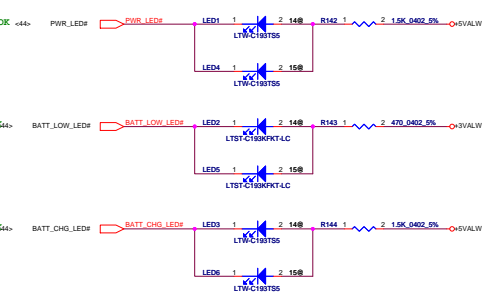
## PWR/B Connector



## USB I/O Connector

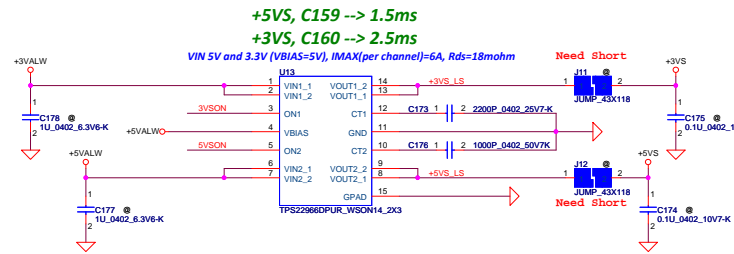
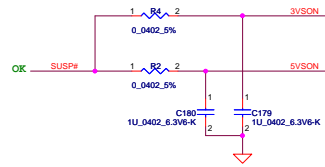


## LED

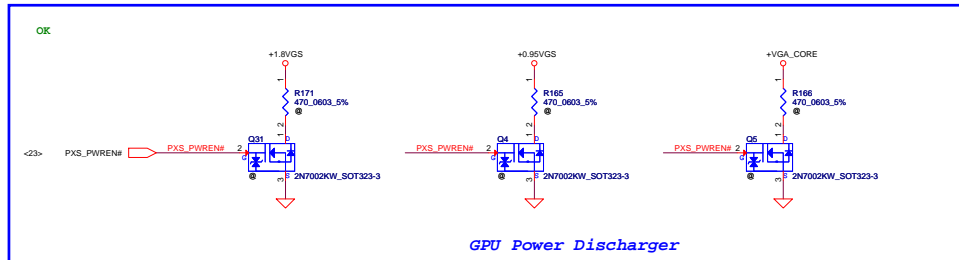
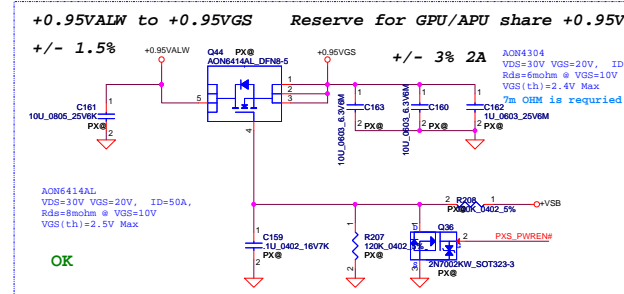
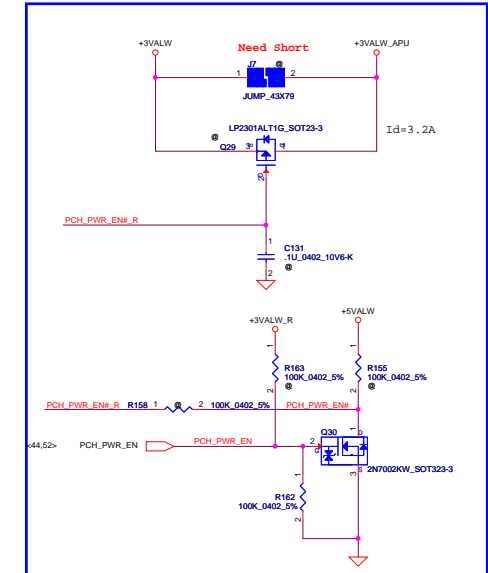
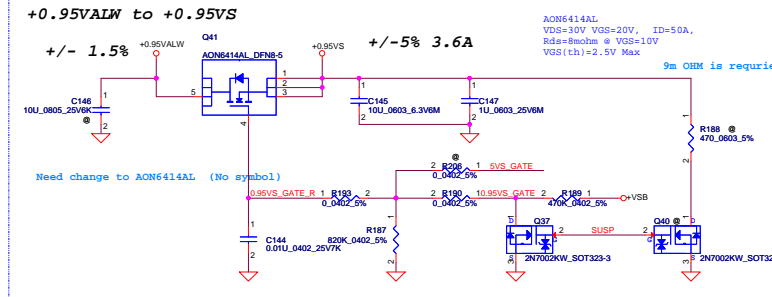
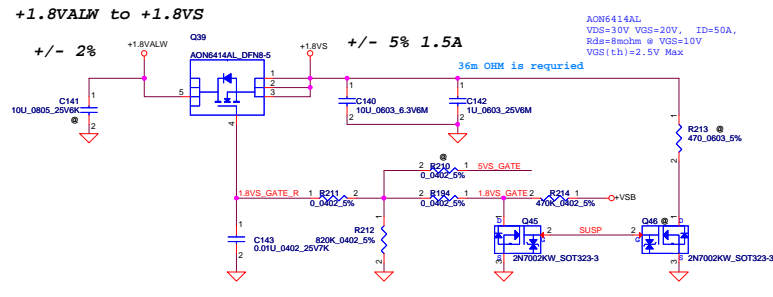
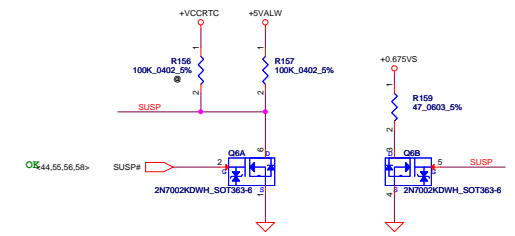


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Size	Document Number	Rev	0.3
Comp	1N-A281	Date	Thursday, January 10, 2014 10:45:45 AM

**Load Switch**  
**+5VALW To +5VS** OK  
**+3VALW To +3VS**

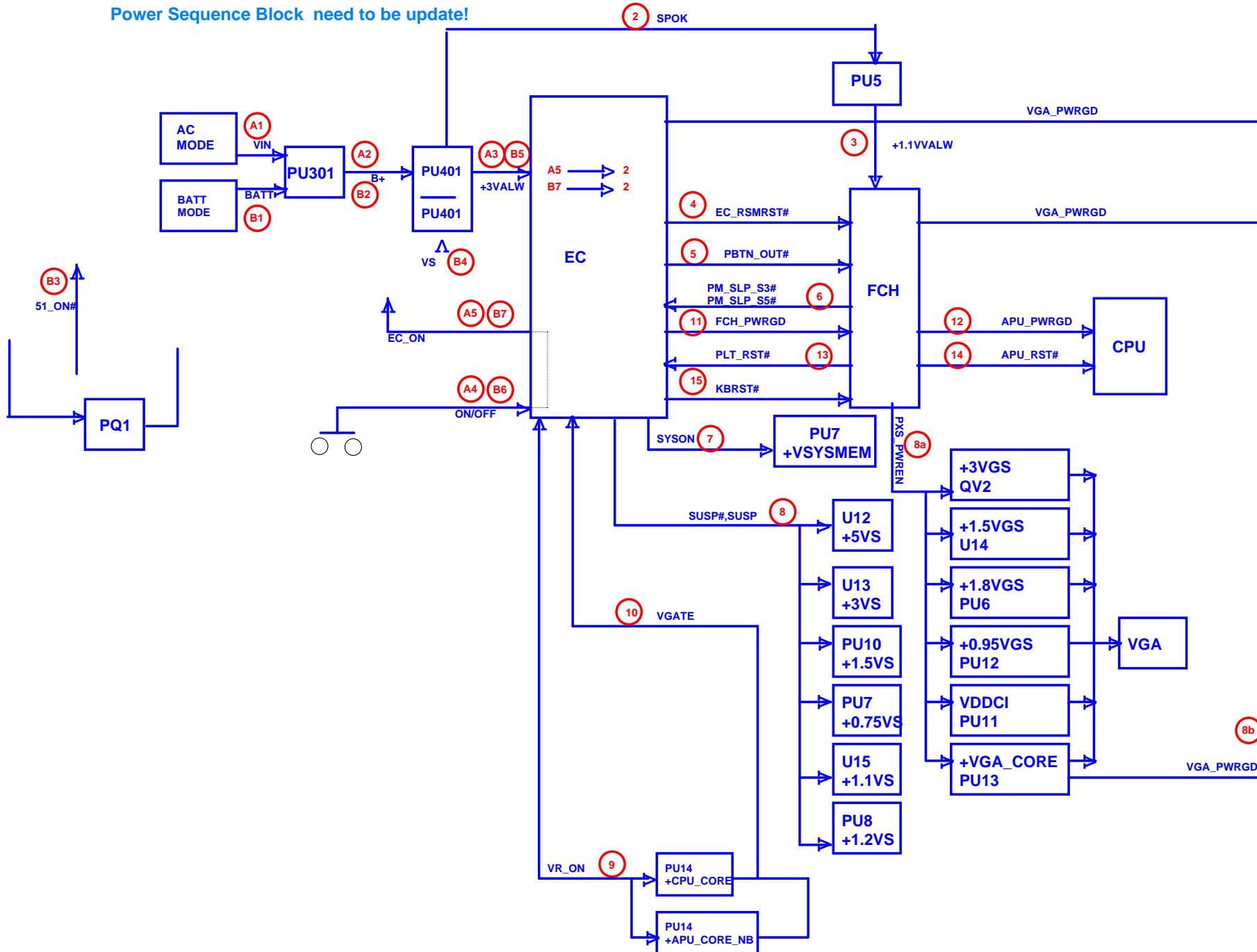


**For DisCharge**



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Customer	Document Number	Rev	Rev
	NM-A281	0.3	0.3
Date	Thursday, January 03, 2014	Sheet	46 of 60

Power Sequence Block need to be update!



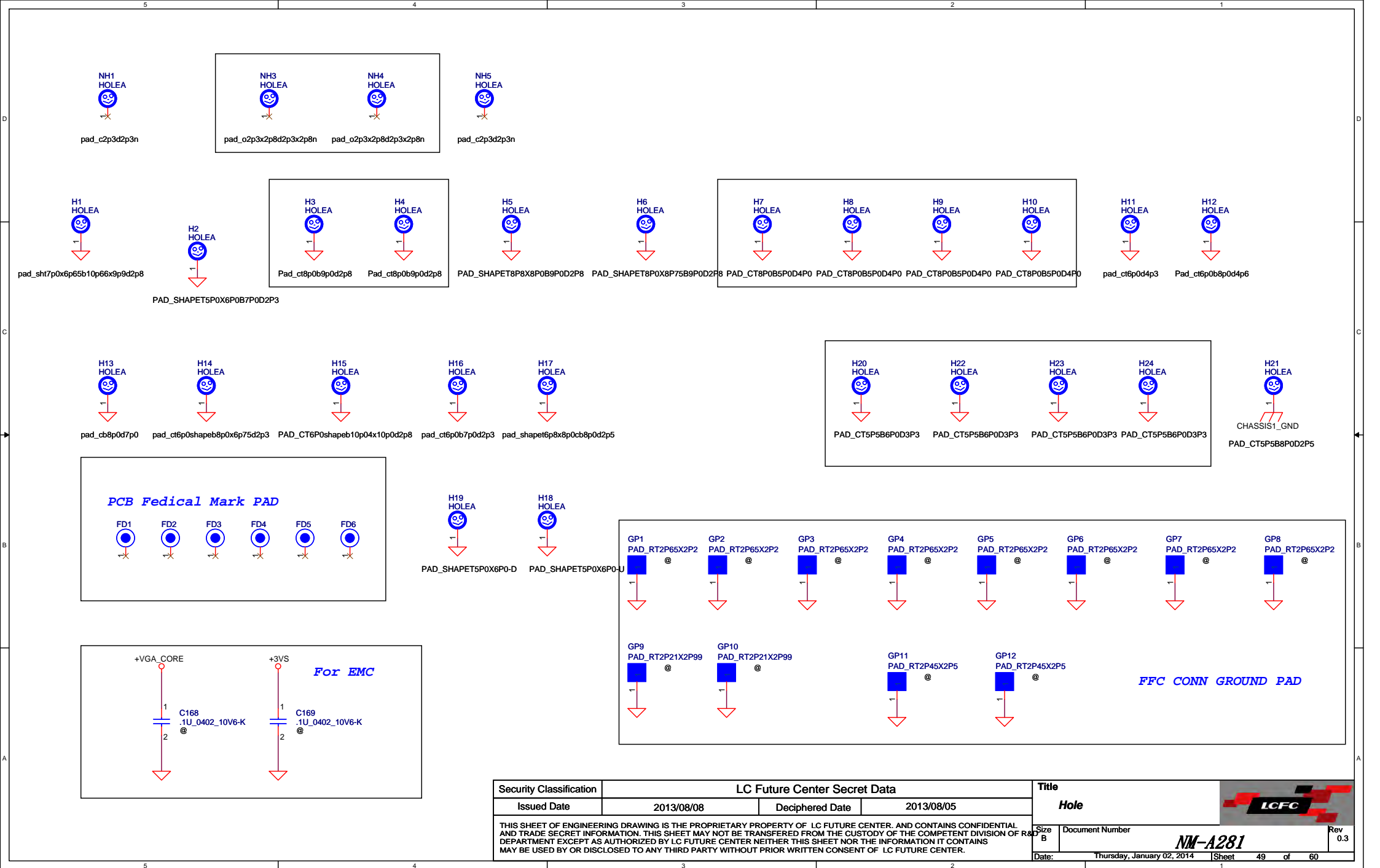
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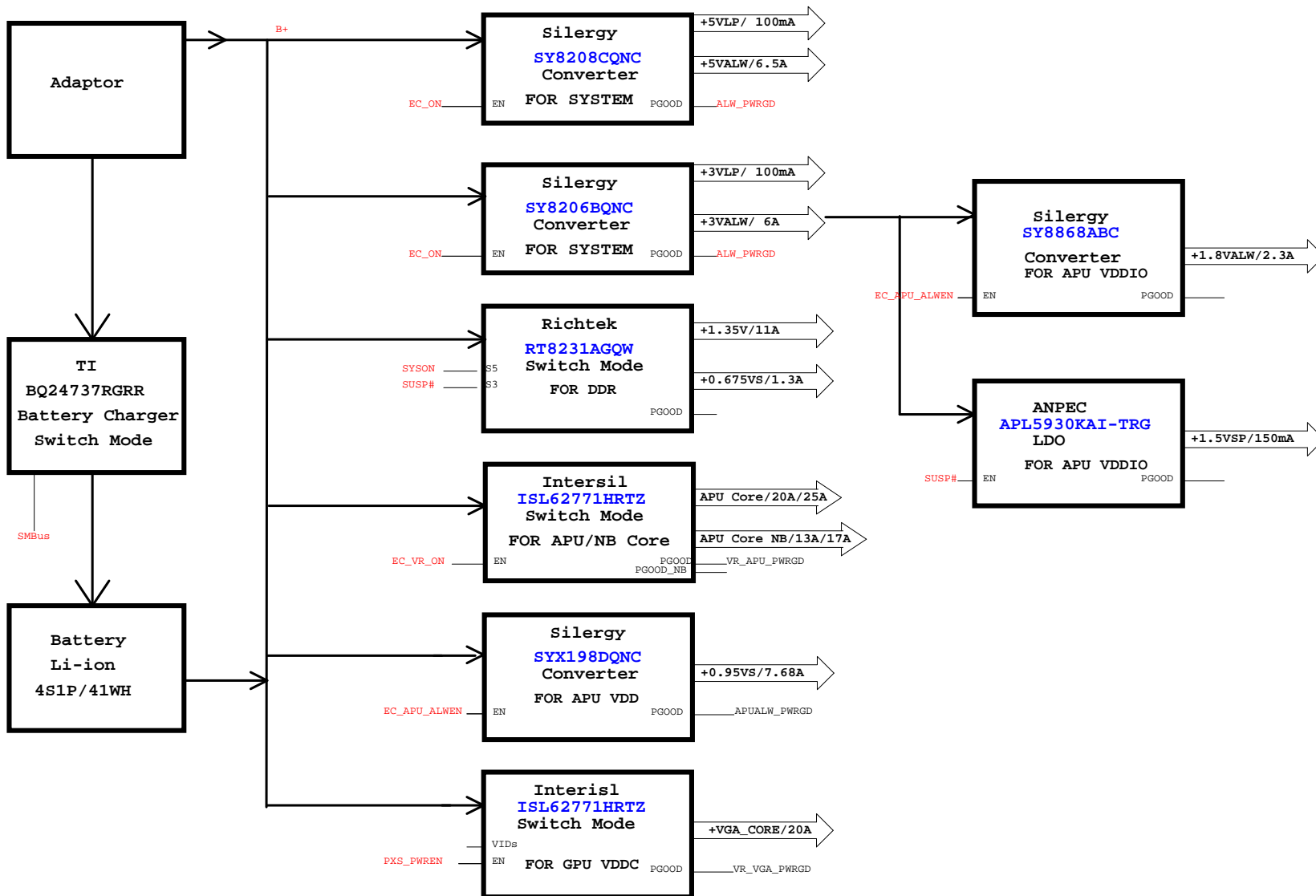
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Size	Document Number	NM-A281	
Custom			
Date:	Thursday, January 02, 2014	Sheet	47 of 60

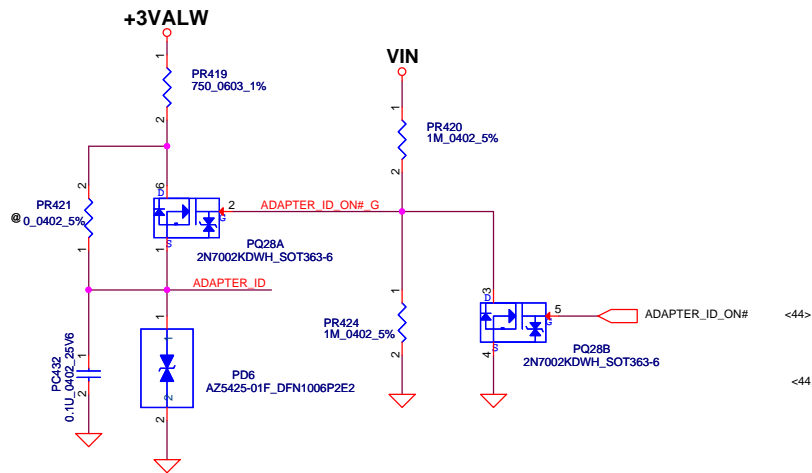
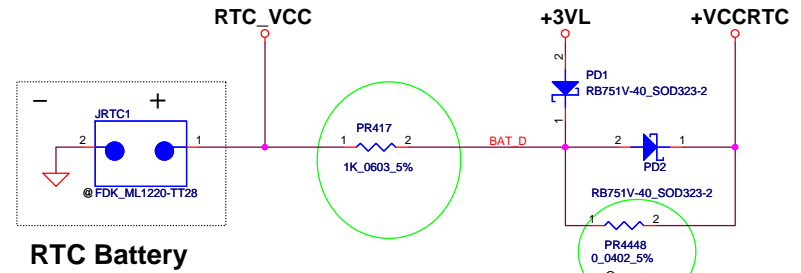
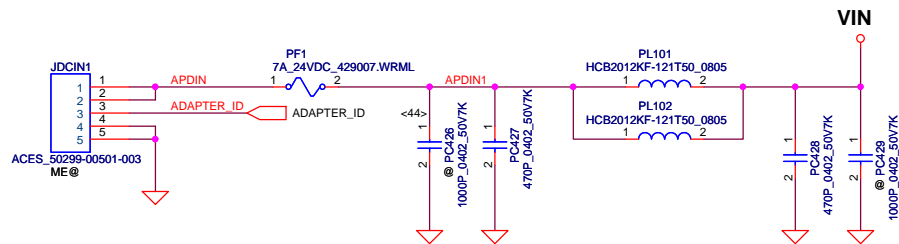




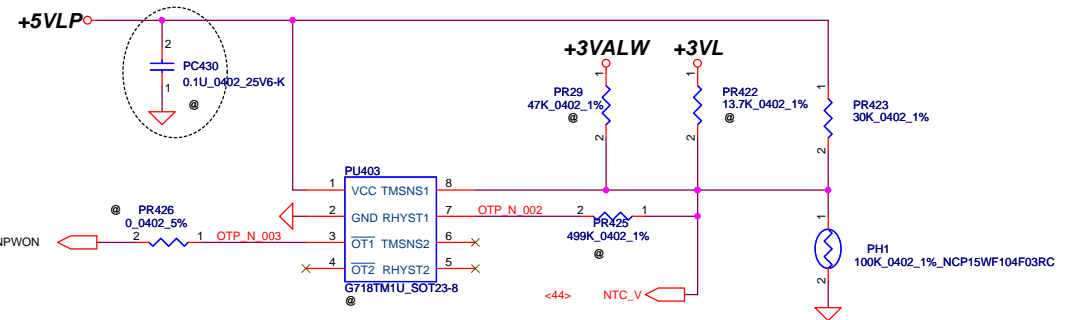





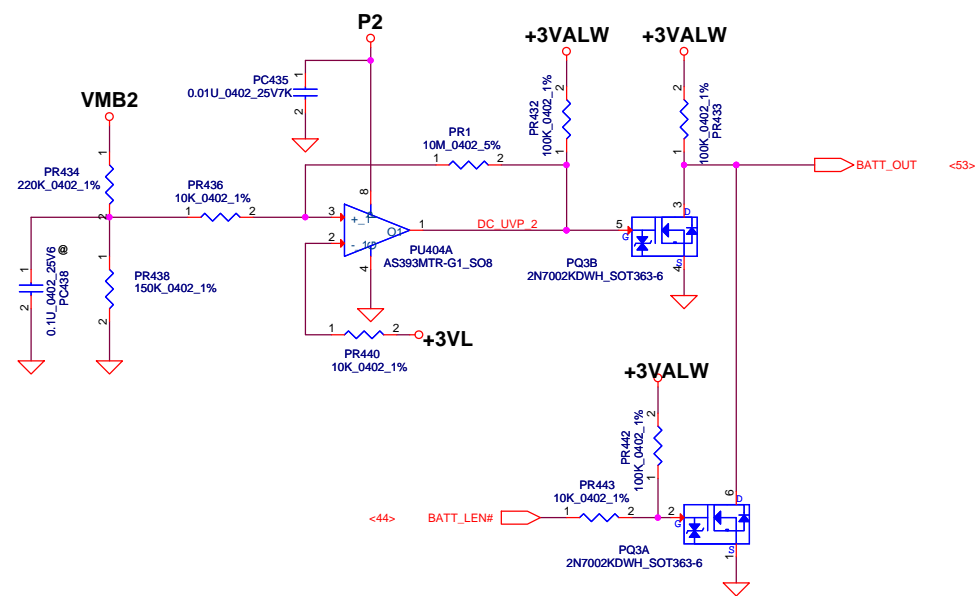
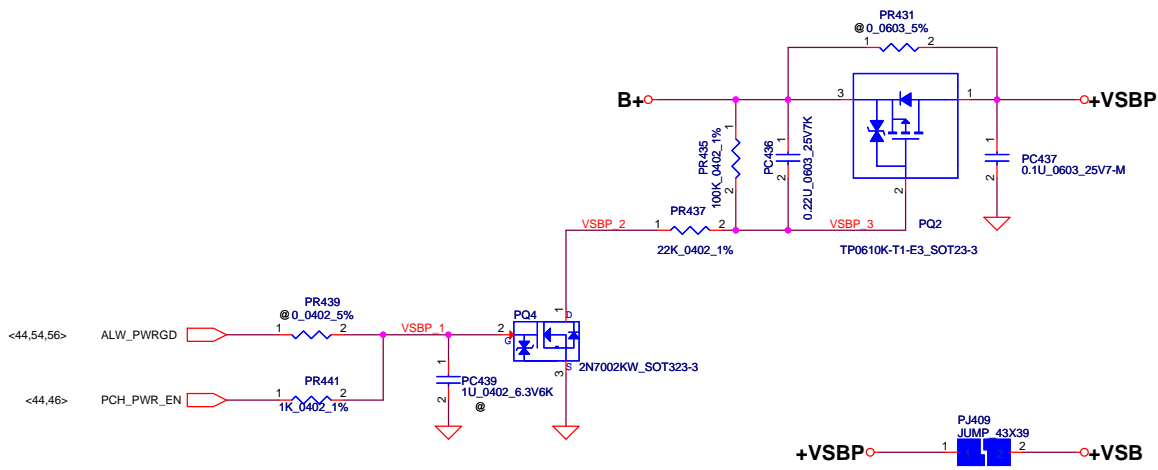
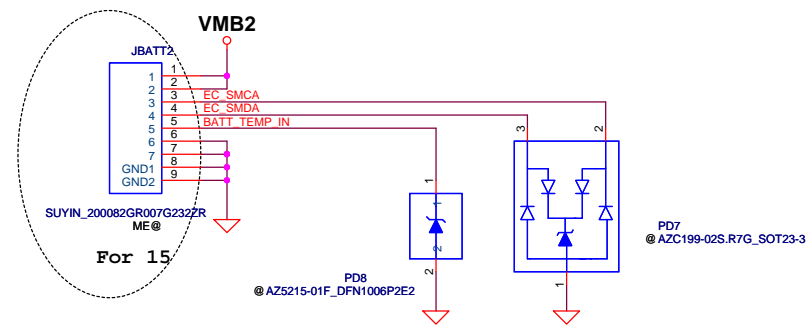
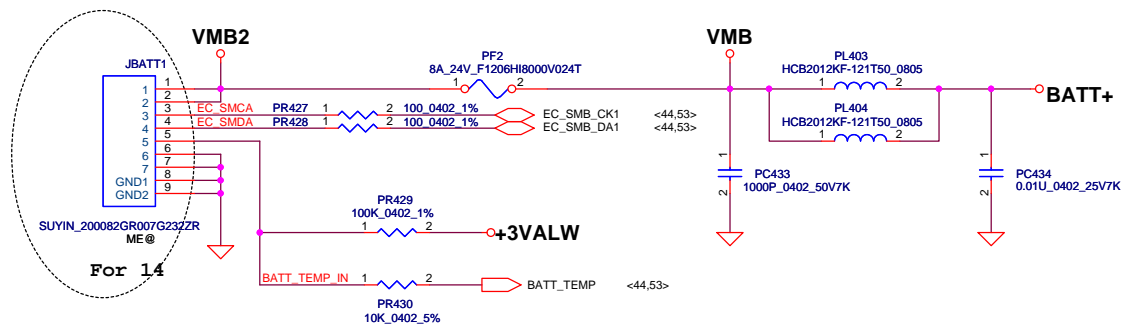





PH1 under CPU bottom side :  
CPU thermal protection at 92+3 degree C  
Recovery at 56 +3 degree C

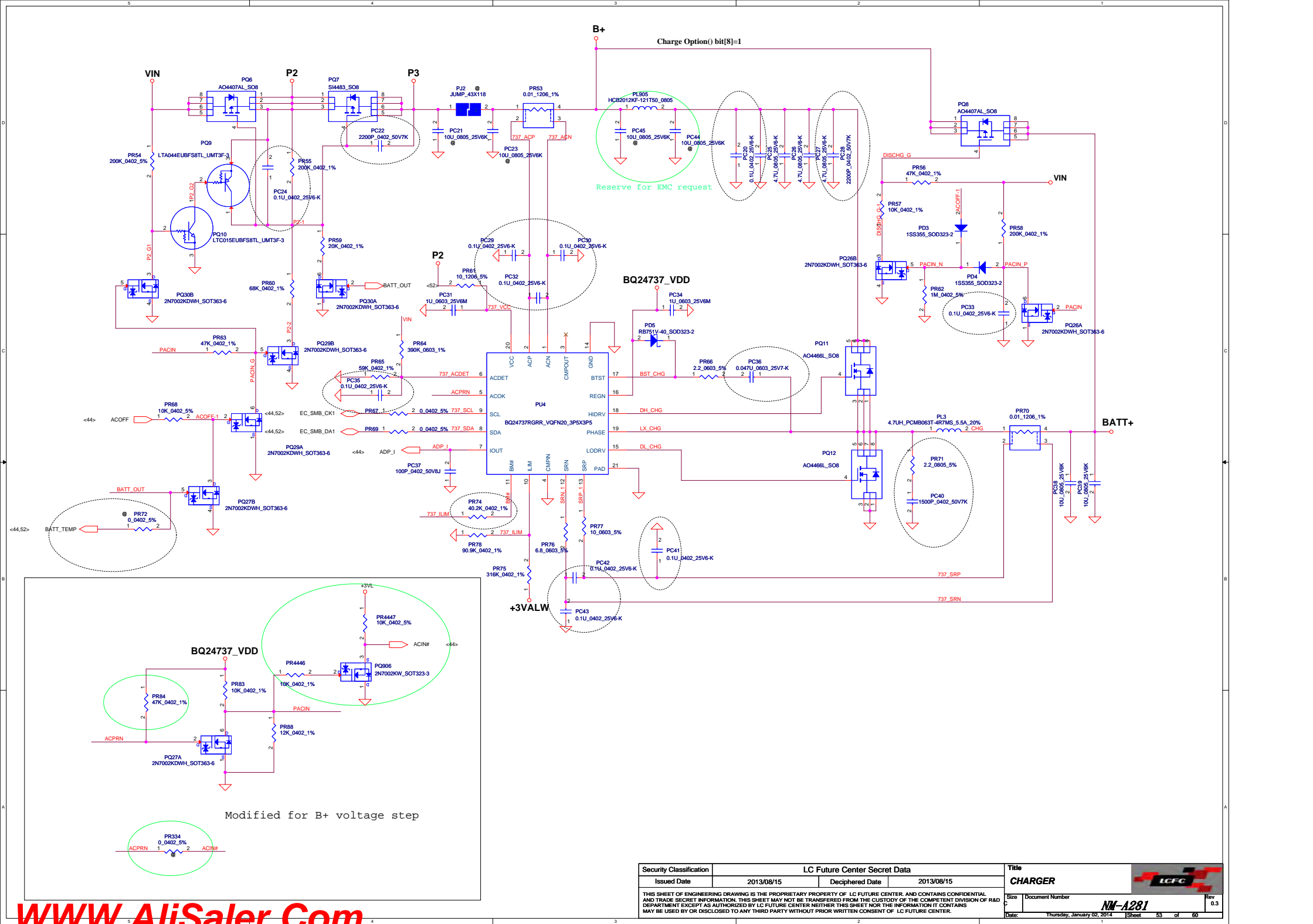


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										Custom			0.3			
										Date:		Thursday, January 02, 2014	Sheet	51	of	60

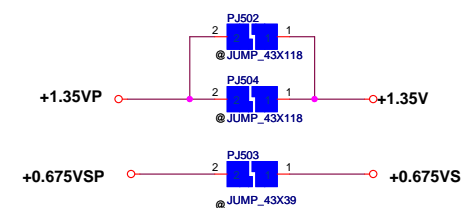


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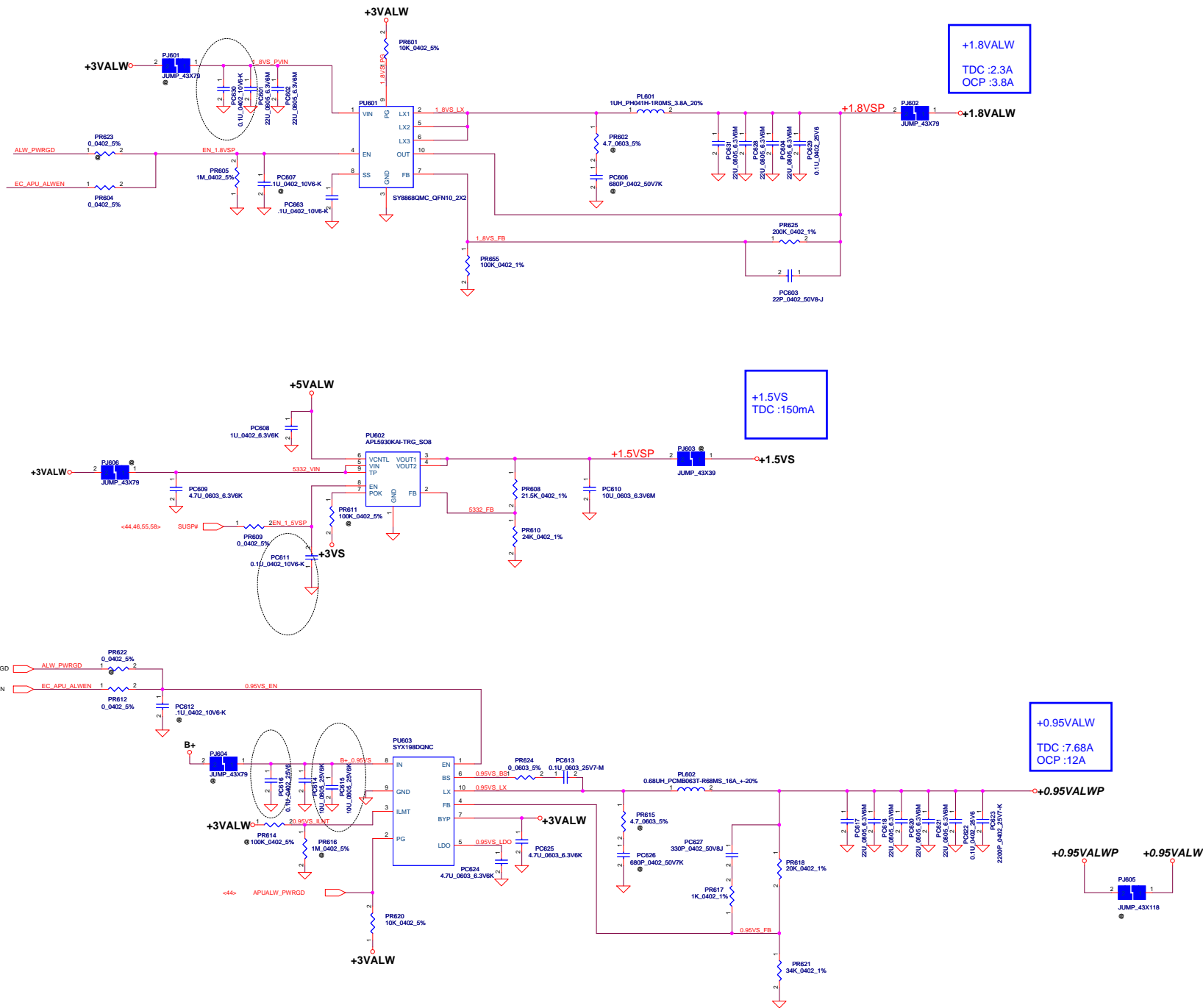
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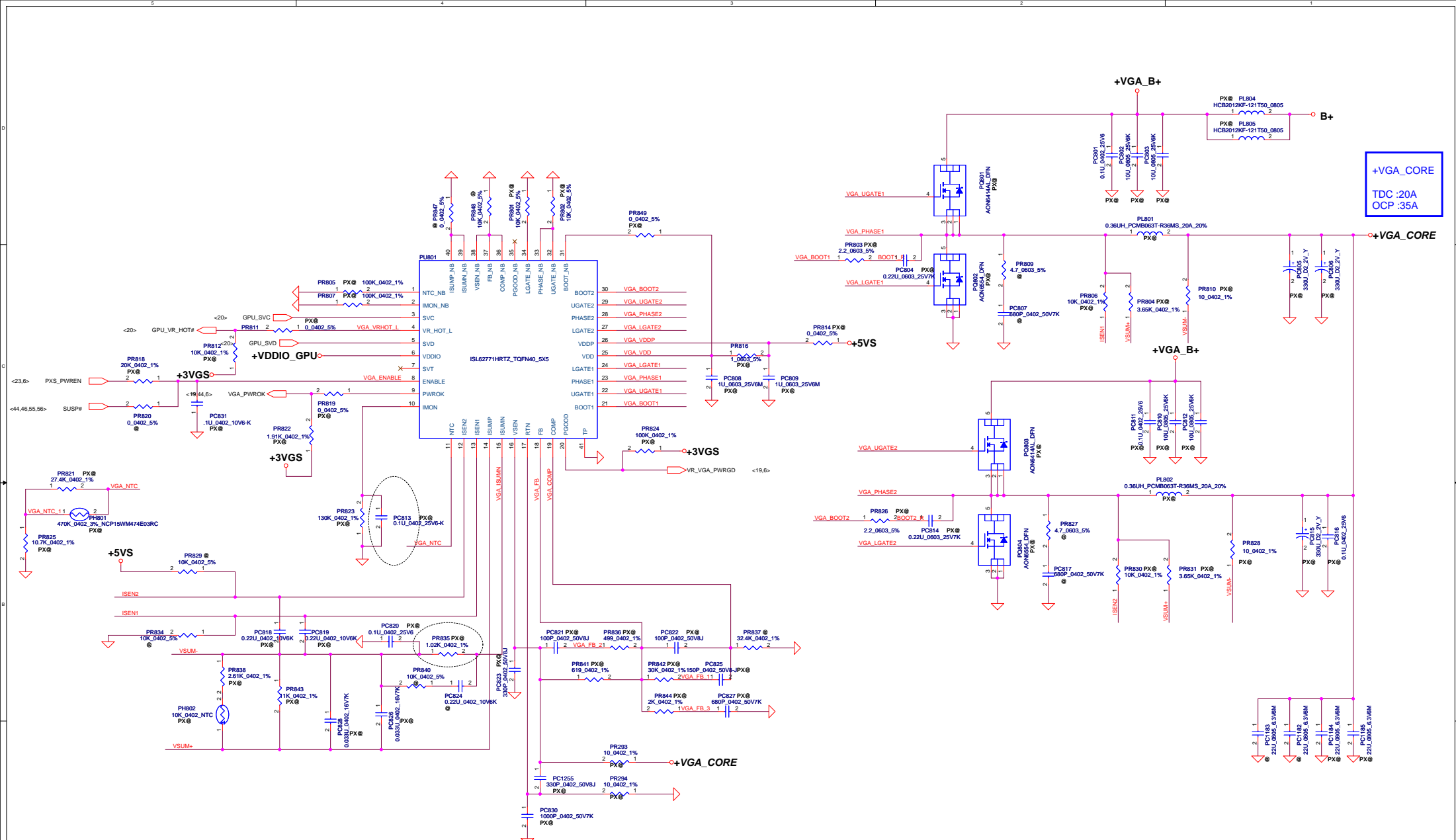


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1.35VS/+0.675VS			
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Date:	Thursday, January 02, 2014, 1:58pm		









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Security Classification		LC Future Center Secret Data			Title
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				5	NM-A281
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