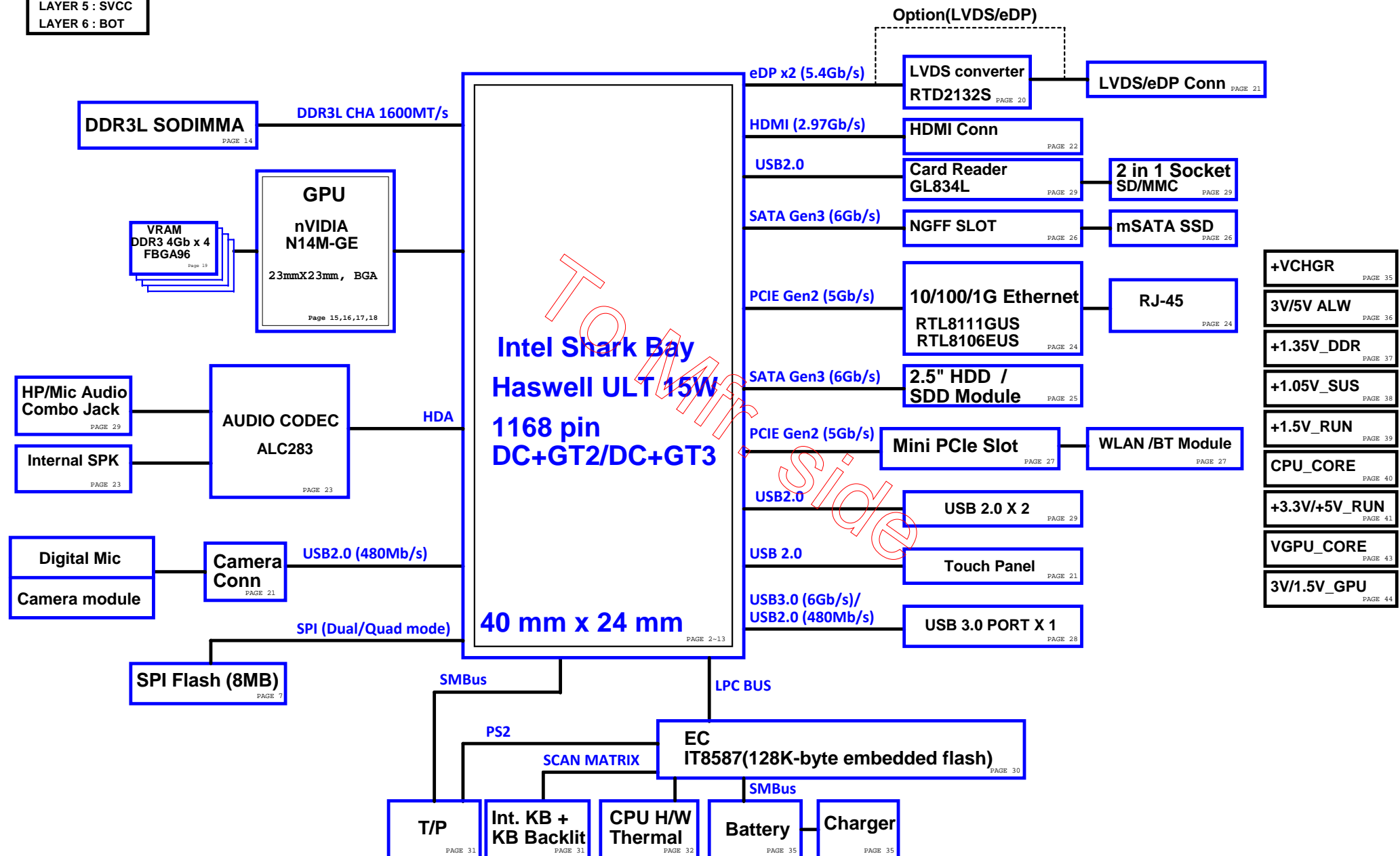


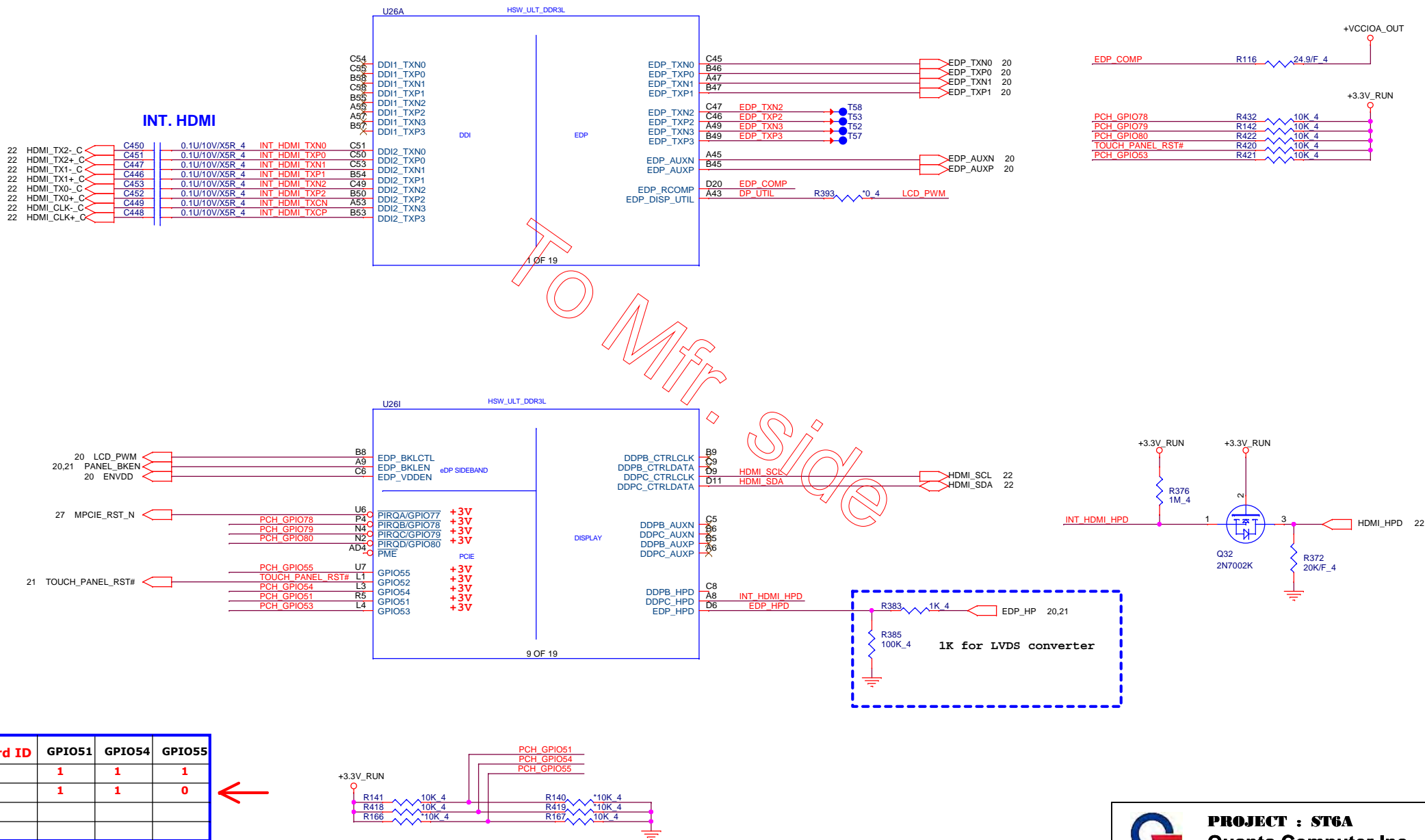
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

ST6/6A 14" OPTIMUS INTEL SHARK BAY ULT ONE CHIP PLATFORM

1

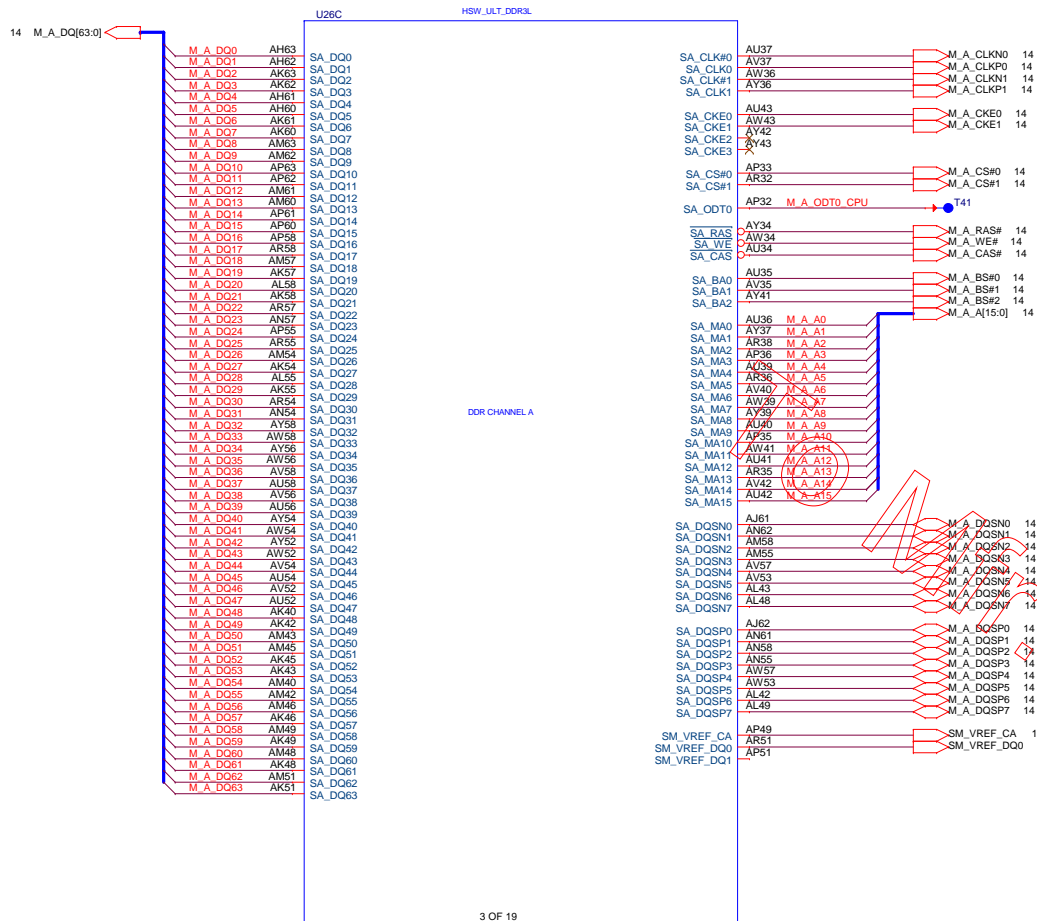



Haswell ULT (DISPLAY)



Haswell ULT (DDR3L)

3





PROJECT : ST6A

Quanta Computer Inc.

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	Haswell ULT 2/12	1A
Date: Monday, April 01, 2013	Sheet	3 of 46

GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DsX

Haswell ULT(GPIO,LPIO,MISC)

+V1.05S_VCCST

R110
1K_4

+3V

THRMTRIP#
RCIN#
SIO RCIN#
PCH_OPIRCOMP

NGFF_WLAN_PWR_EN

TOUCH_FINGER_EN

ALS_INT_N#

DGPU_HOLD_RST#

SDA_ALS_L

SCL_ALS_L

GPIO66

GPIO68

GPIO69

GPIO70

GPIO71

GPIO72

GPIO73

GPIO74

GPIO75

GPIO76

GPIO77

GPIO78

GPIO79

GPIO80

GPIO81

GPIO82

GPIO83

GPIO84

GPIO85

GPIO86

GPIO87

GPIO88

GPIO89

GPIO90

GPIO91

GPIO92

GPIO93

GPIO94

GPIO95

GPIO96

GPIO97

GPIO98

GPIO99

GPIO100

GPIO101

GPIO102

GPIO103

GPIO104

GPIO105

GPIO106

GPIO107

GPIO108

GPIO109

GPIO110

GPIO111

GPIO112

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GPIO315

GPIO316

GPIO317

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GPIO320

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GPIO348

GPIO349

GPIO350

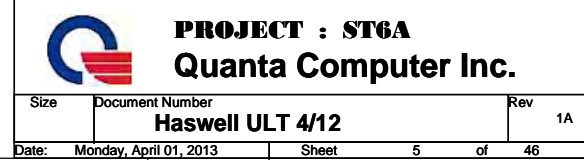
GPIO351

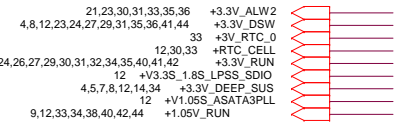
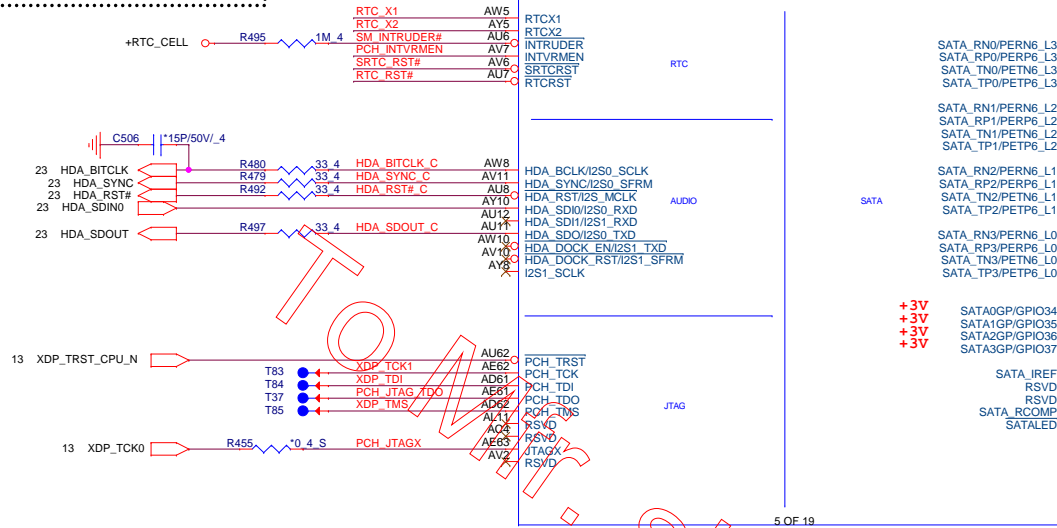
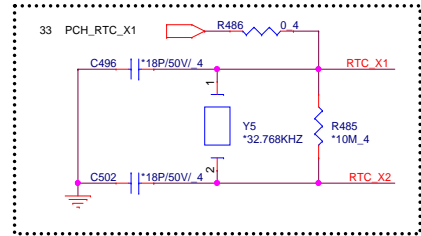
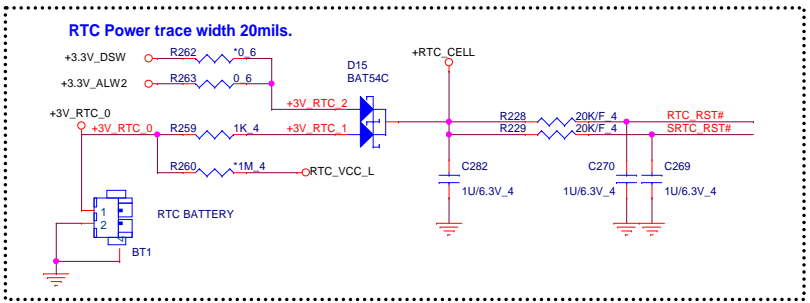
GPIO352

GPIO353

GPIO354

U26K HSW_ULT_DDR3L

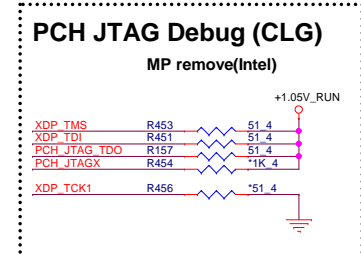




6

PCH Strap Table

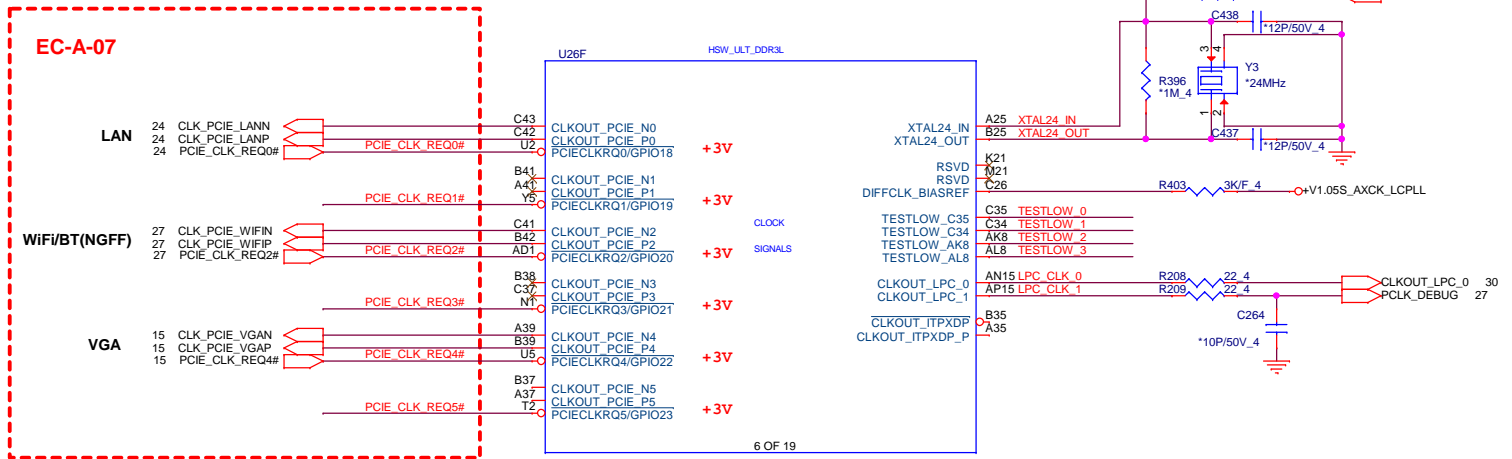
Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN R429 1K 4 ACZ_SPKR 4,23
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	30 ME_WR# R491 1K 4 HDA_SDOUT_C
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL R493 330K 4 PCH_INTVRMEN R481 330K 4
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO R394 1K 4 GPIO66 4 R404 1K 4
GPIO86	BBS(Boot BIOS Strap Bit)		0 = Default SPI (iPD 20K) 1 =LPC	+3.3V_RUN R106 1K 4 BBS 4 R105 1K 4
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	+3.3V_DEEP_SUS R182 10K 4 GPIO15 4
DSWVREN	Deep Sx well on die DSW VR enable		1=Should be always pull-up	+RTC_CELL R483 330K 4 DSWVRMEN 8



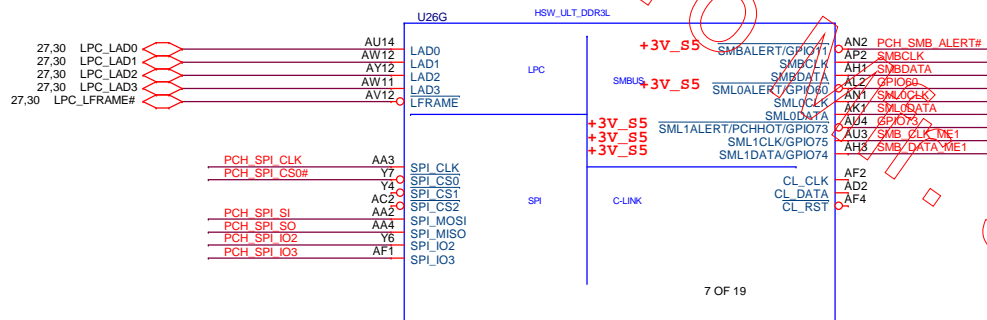
PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	Haswell ULT 5/12	1A
Date: Monday, April 01, 2013	Sheet 6 of 46	

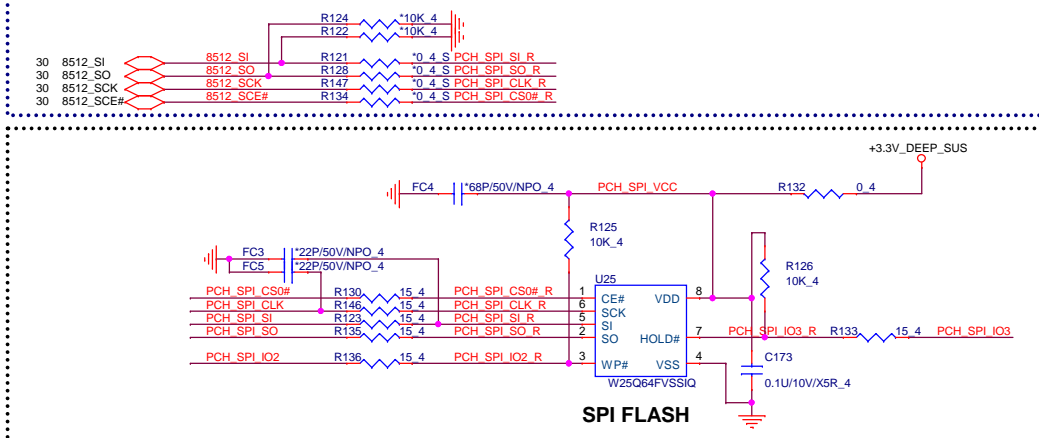
Haswell ULT (CLK)



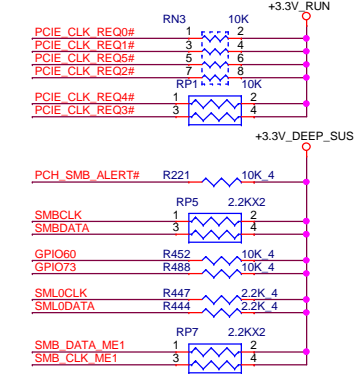
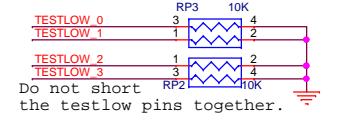
Haswell ULT (LPC/SPI/SMB/CLINK)



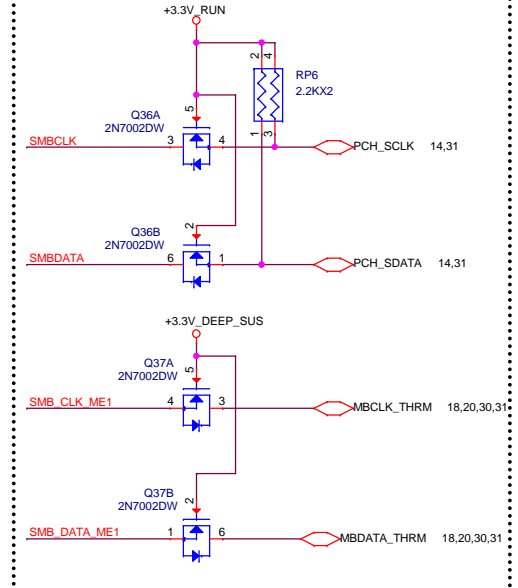
For EC(IT8587 e-flash) load code from BIOS flash ROM



2,4,6,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42
+3.3V_RUN
4,5,6,8,12,14,34
12 +V1.05S_AXCK_LCPILL

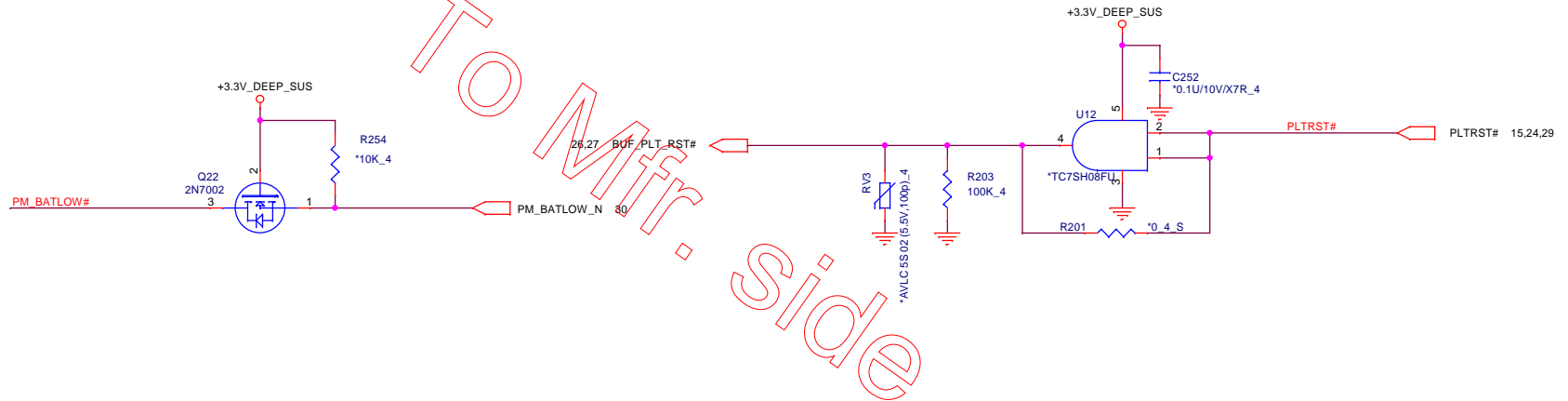


SMBus/Pull-up(CLG)



PROJECT : ST6A
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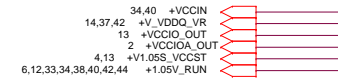


WWW.AliSaler.Com

Haswell ULT MCP(POWER)

CPU VCC

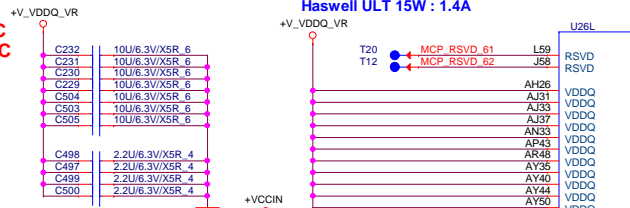
Haswell ULT 15W : 32A



CPU VDDQ

Haswell ULT 15W : 1.4A

7X10UF MLCC
4X2.2UF MLCC



VCCST_PWRGD_L

+V1.05S_VCCST

+V1.05S_VCCST

SVID ALERT

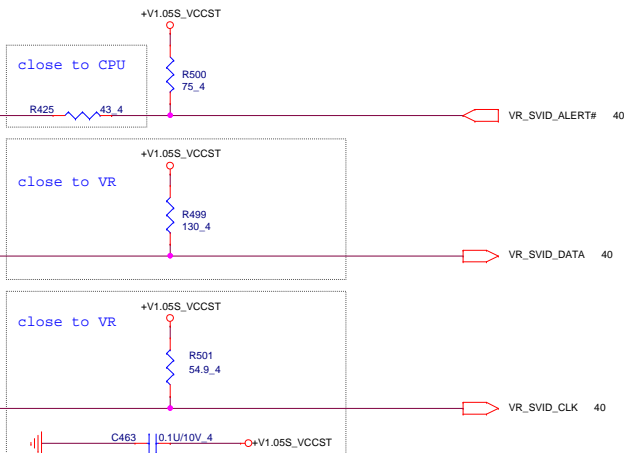
H_CPU_SVIDALRT_N

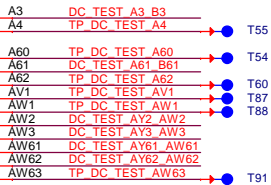
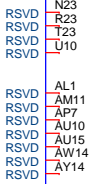
SVID DATA

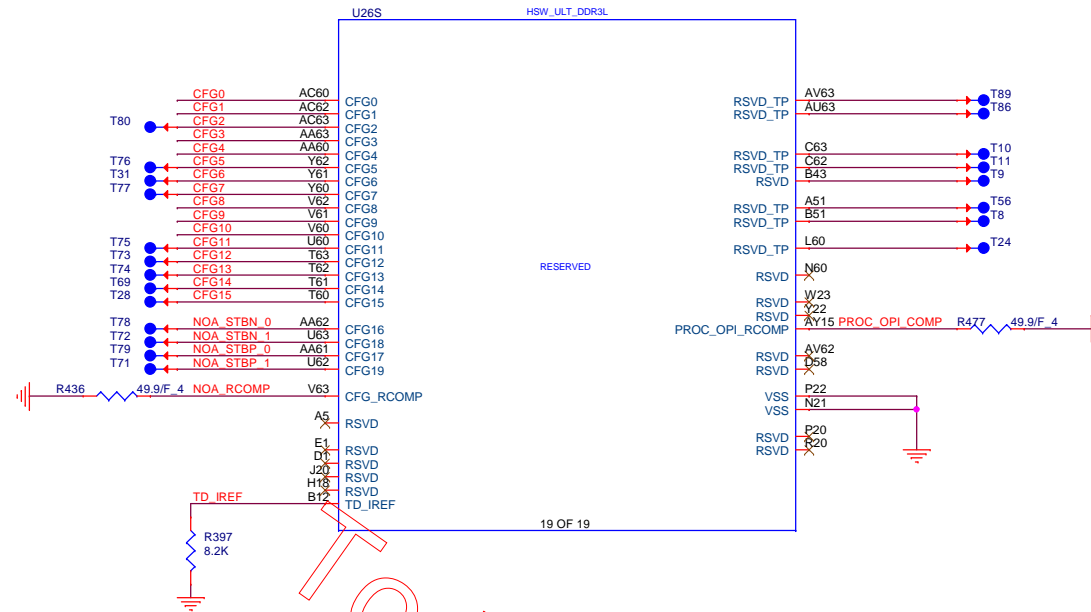
VR_SVID_DATA

SVID CLK

VR_SVID_CLK







Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED: NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	

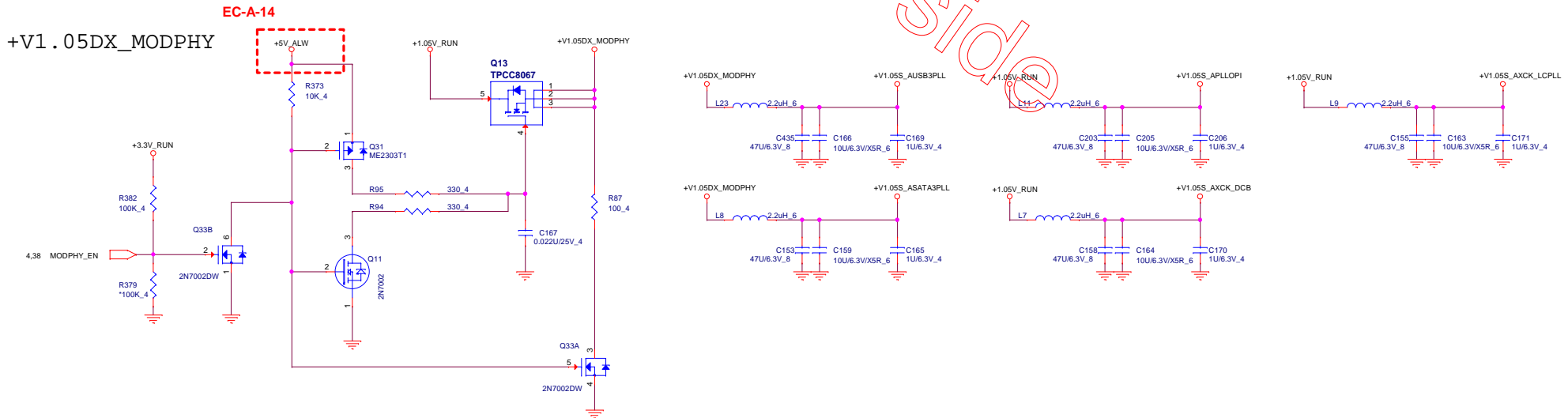
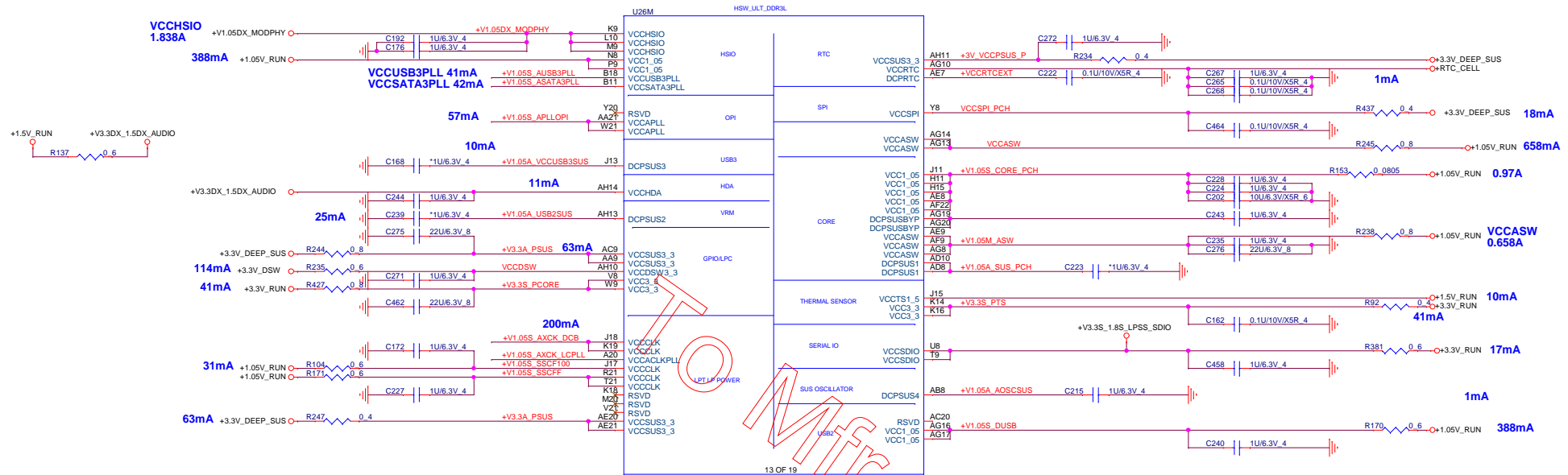


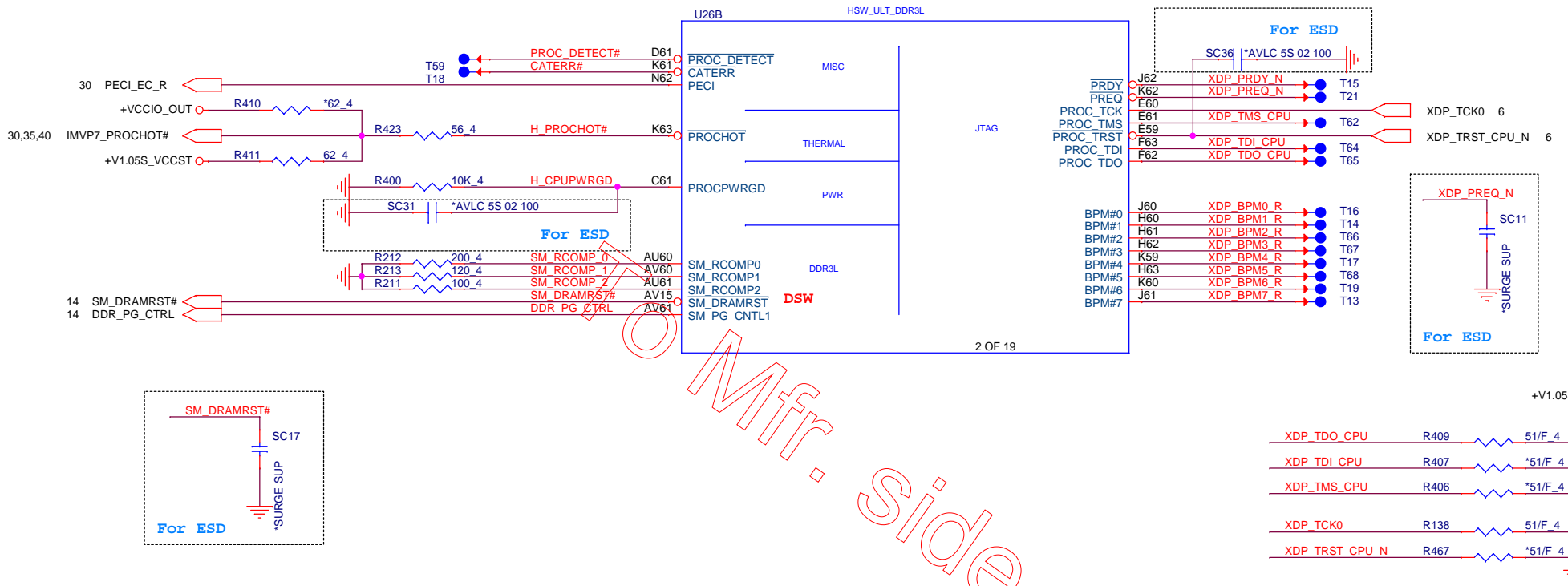
PROJECT : ST6A
Quanta Computer Inc.

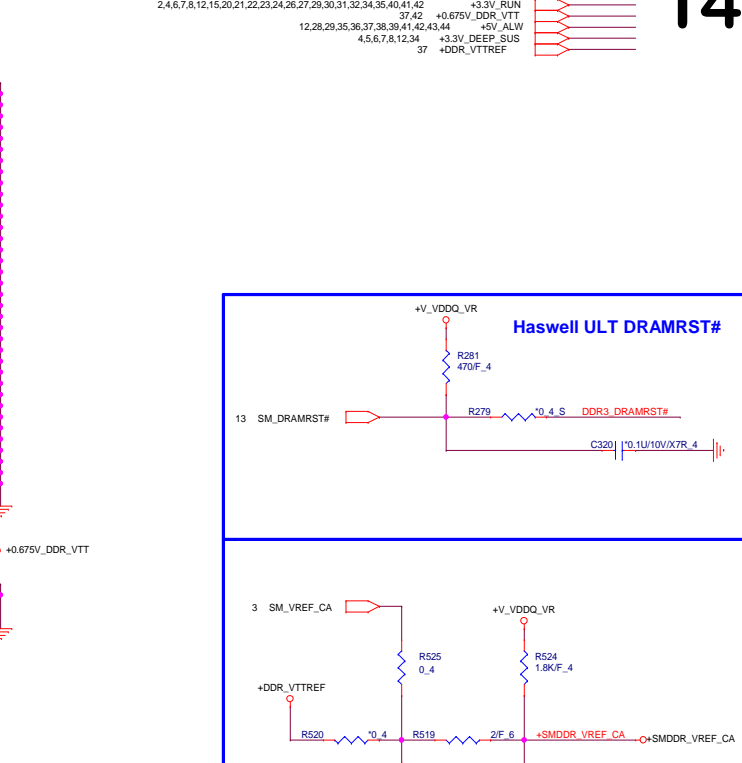
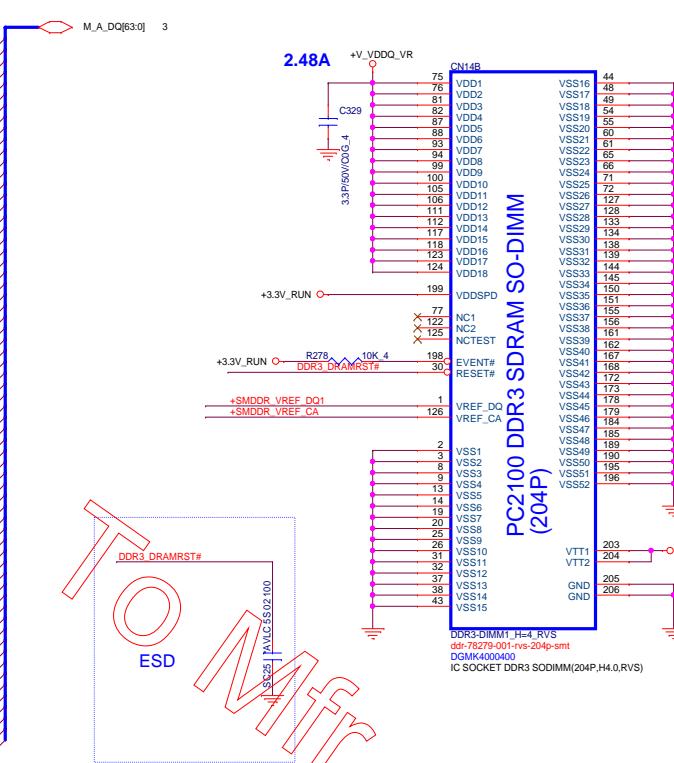
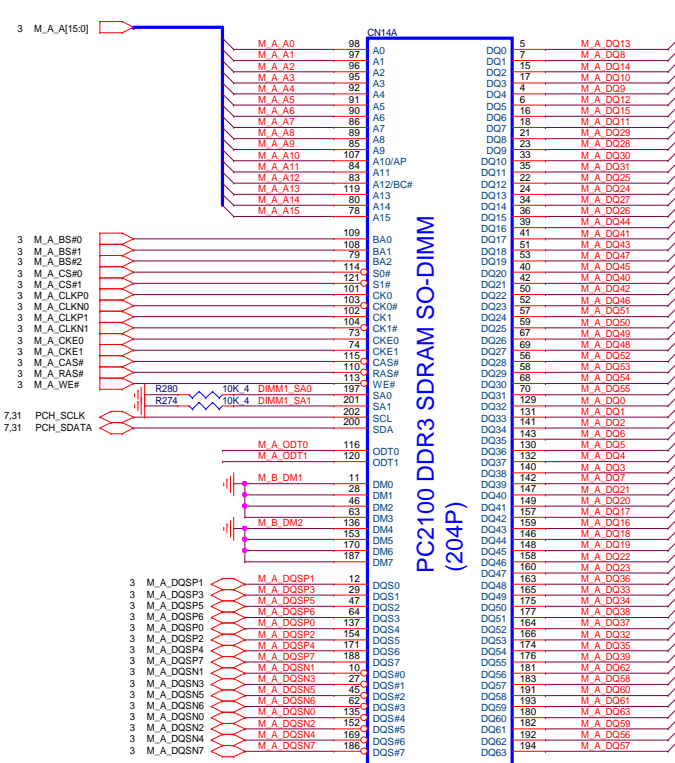
Haswell ULT PCH(POWER)

12

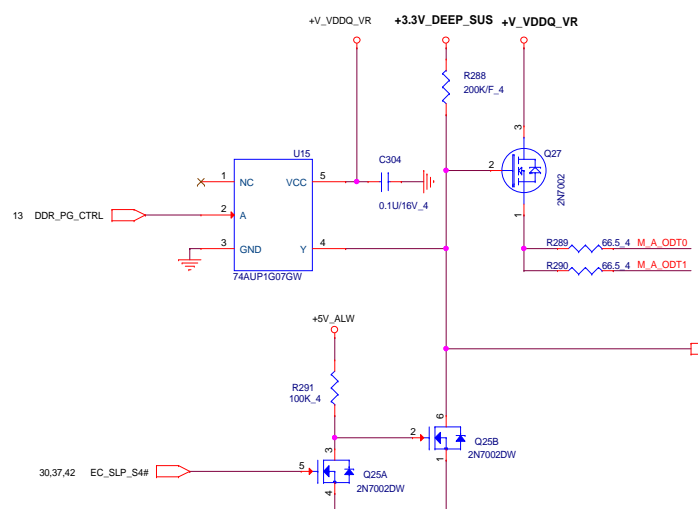
6,9,33,34,38,40,42,44	+1.05V_RUN
4,5,6,7,8,14,34	+3.3V_DEEP_SUS
4,6,8,23,24,27,29,31,35,36,41,44	+3.3V_DSX
2,4,6,7,8,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42	+3.3V_RUN
23,27,34,39,42,44	+1.5V_RUN
36,41,44	+1.5V_ALW
6,30,33	+RTC_CELL
5	+V1.05S_AUSB3PLL
6	+V1.05S_ASATA3PLL
7	+V1.05S_AXCK_LCPLL



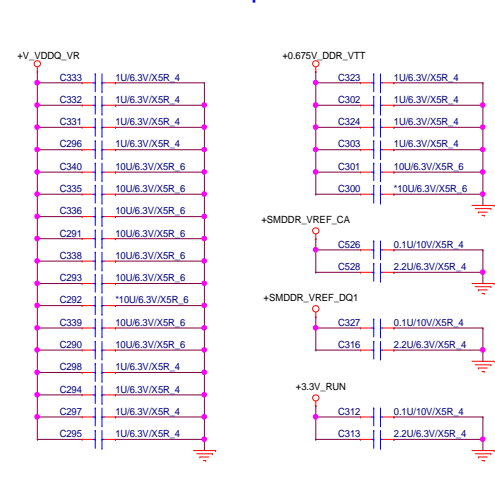




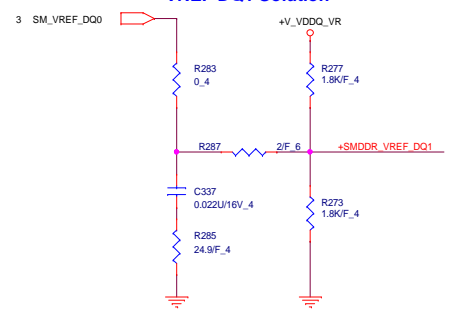
DDR3L SODIMM ODT DERATION



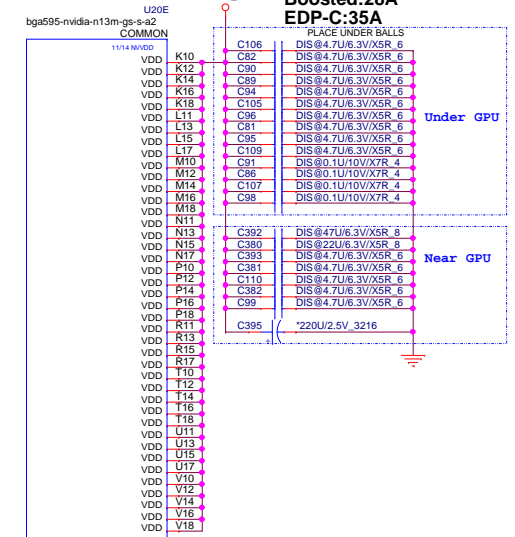
Place these Caps near So-Dimm1



VREF DQ1 Solution



Peak current:40.89A
Boosted:28A
EDP-C:35A



U_GPU_GB2_64

3V_GPU 56mA

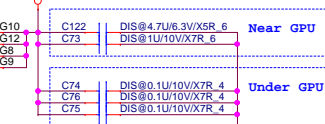


Table 2. GPU Power Rails

GPU Power Rail	Nominal Value	Comments
IVVDD	GPU SKU Specific	GPU Core power rail
FBVDD ¹	1.35 V or 1.5 V	VRAM Core power for Frame Buffer components
FBVDDQ ²	1.35 V or 1.5 V	VRAM I/O and GPU's Frame Buffer I/O power rail
IFP _X _IOVDD ³	1.05 V or 3.3V	Power/IFP blocks
IFP _X _PLLVD ³	1.05 V or 3.3 V	Integrated Digital Display PLL Power Rails
PEX _X _IOVDD/Q	1.05 V	GPUs PCIe interface power rail
PEX _X _SVDD_3V3, PEX _X _PLL_HVDD	3.3 V	GPU PCIe PLL Power Rails
PEX _X _PLLVD	1.05 V	GPU PCIe PLL Power Rails
FB _X _PLL_AVDD	1.05 V or 3.3 V	Frame Buffer PLL Power Rail
FB _X _DLL_AVDD (GB2-64 and GB4-128)	1.05 V	Frame Buffer PLL and DLL Power Rail
FB _X _PLL_DLL_AVDD (GB2-192 and GB3-256)	1.05 V	Frame Buffer PLL and DLL Power Rail
PLLVD, GPCPLL_AVDD LVS_PLLVD	1.05 V	Core Clock PLL Analog Power Rail
VID_PLLVD	1.05 V	Video Pixel Clock PLL Analog Power Rail
SP_PLLVD	1.05 V	Core Clock PLL Analog Power Rail
DAC _X _VDD ¹	3.3 V	Powers the DAC interfaces
VDD33(HV3V3) ⁴	3.3 V	Powers slower logic such as GPIOs, I2C, AUX channels and SLI

Notes: 1. The same power plane can be used for VDD33 and DAC_X_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays).
4. On GB1-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.

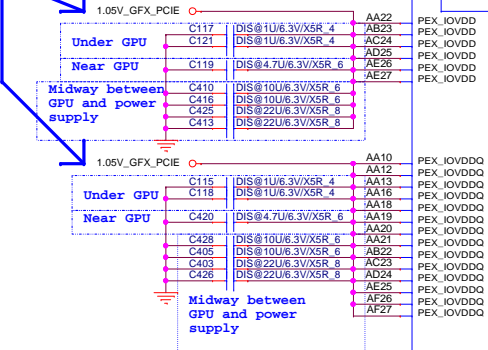


PROJECT : ST6A
Quanta Computer Inc.

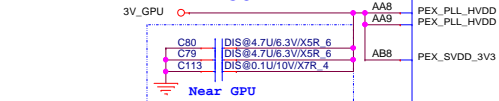
Size	Document Number	Rev
	N14M-GE (PCIE I/F) 1/5	1A
Date:	Monday, April 01, 2013	Sheet 15 of 46

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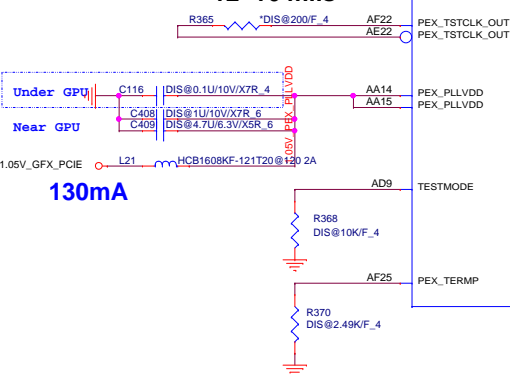
855mA



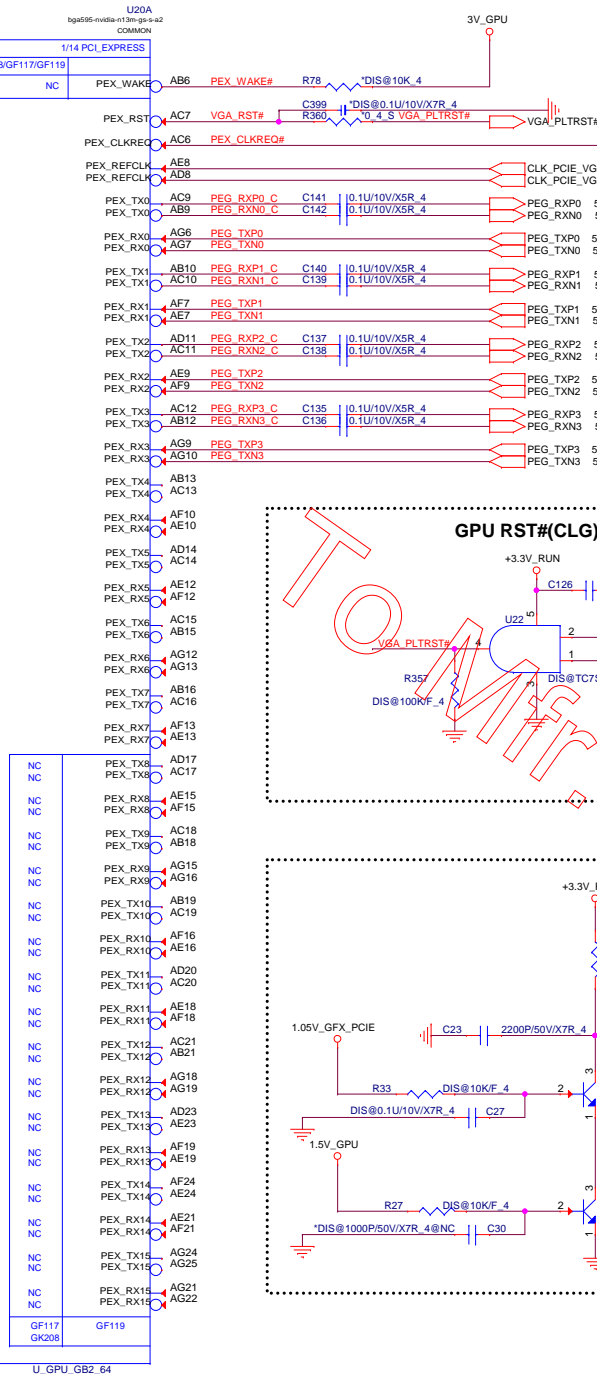
286mA



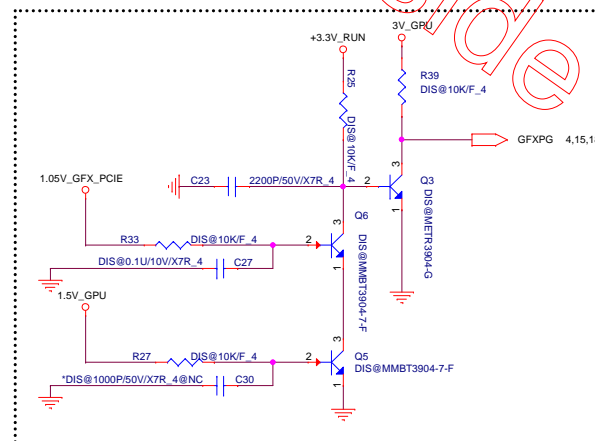
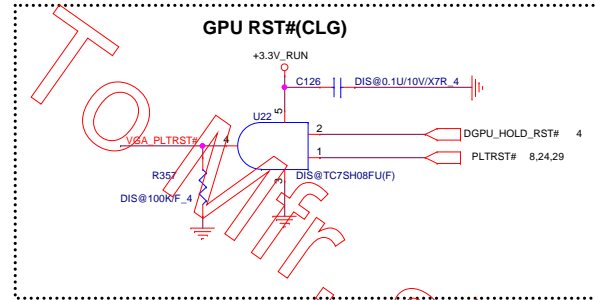
12~16 mils



130mA



GPU RST#(CLG)



U20C

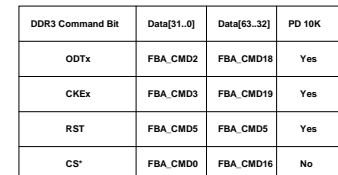
bga595-nvidia-n13m-gs-s-a2
COMMON

1/14 VDDQ33

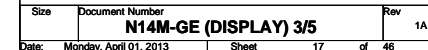
AD10
AD7
B19

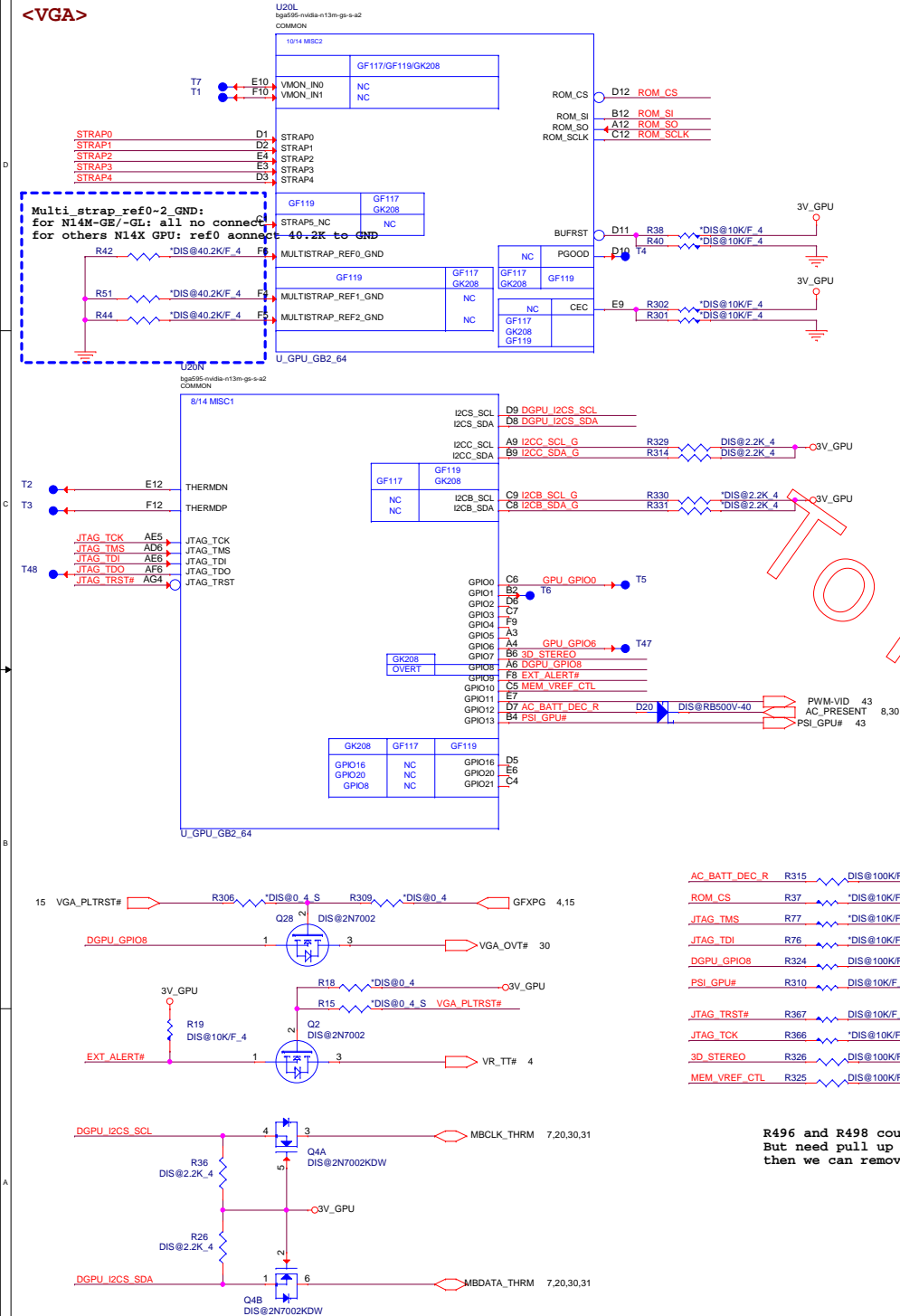
F11

V5
V6FERMI_RSVD1_NC
FERMI_RSVD2_NCV5
V6V5
V6V5
V6V5
V6V5
V6V5
V6V5
V6V5
V6V5
V6V5
V6V5
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V6V5
V6



Optimus:
All unstuff , one Cap stuff 10K ohm

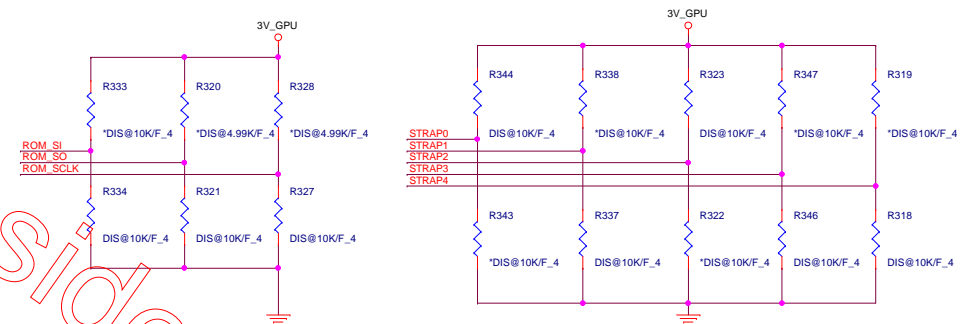




Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

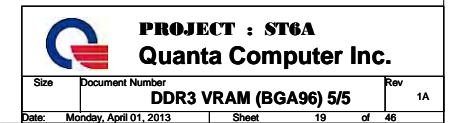
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0111

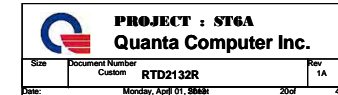
1GHz	Samsung	K4W2G1646E-BC1A	AKD5MGGT532
	Micron	MT41J128M16JT-093G:K	AKD5MGSTL15
	Hynix	Hynix 128x16 Vram H5TC2G63FFR-11C	AKD5MZDTW04
900MHz	Samsung	K4W4G1646B-HC11	AKD5MGWT516
	Micron	MT41K256M16HA-107G:E	AKD5PGSTL00



GF117		PC12M-G2-B-A-2
Item		
Device ID	011789	
Package	G84-128/022-48	
Internal P/N	GF117_23mm	
ROM_51	10kwhm pull down	
ROM_5Q	10kwhm pull down	
ROM_SCLK	10kwhm pull down	
Strap0	Refer to V124x_BA0M_Straps table	
Strap3		
Strap2		
Strap3		
Strap4	10kwhm pull down	
Open_VREG SWU	Config C	
NVVDIO Boot Voltage	0.9V	

GPU Name		GPU		VRAM Vendor		Config	VRAM P/N	Max Speed CLK	DVOM CLK	BASE CLK	Stage 1	Stage 2	Stage 3	Stage 4	Status
GPU ID#1		GPU		VRAM Vendor		Config	VRAM P/N	Max Speed CLK	DVOM CLK	BASE CLK	Stage 1	Stage 2	Stage 3	Stage 4	Status
G0127	A14M-6E/G/L	Micros	D0R3	L5VJ/5V	L20M15	MTF15L001040-100000	MTF15L001040-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Micros	D0R3	L5VJ/5V	L20M15	MTF15L001040-100000	MTF15L001040-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Samsung	D0R1	L5VJ/5V	L20M15	K6W201040E-083A	K6W201040E-083A	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Samsung	D0R1	L5VJ/5V	L20M15	K6W201040E-083A	K6W201040E-083A	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Hynix	D0R3	L5VJ/5V	L20M15	HT5201040E-100000	HT5201040E-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Hynix	D0R3	L5VJ/5V	L20M15	HT5201040E-100000	HT5201040E-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Hynix	D0R3	L5VJ/5V	L20M15	HT5201040E-100000	HT5201040E-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Hynix	D0R3	L5VJ/5V	L20M15	HT5201040E-100000	HT5201040E-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Hynix	D0R3	L5VJ/5V	L20M15	HT5201040E-100000	HT5201040E-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
		Hynix	D0R3	L5VJ/5V	L20M15	HT5201040E-100000	HT5201040E-100000	1200	1200	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready

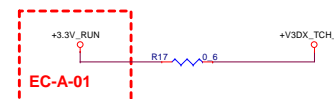




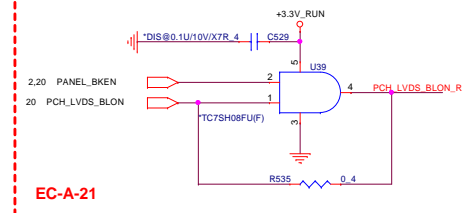
USB interface



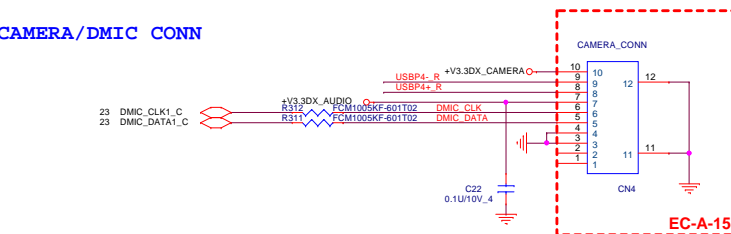
Touch Panel VCC Control



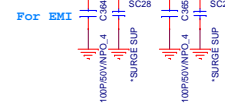
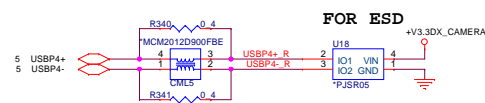
EC-A-21



CAMERA/DMIC CONN

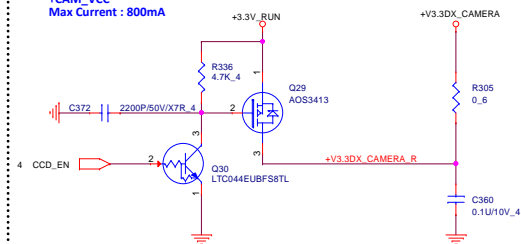


FOR ESD

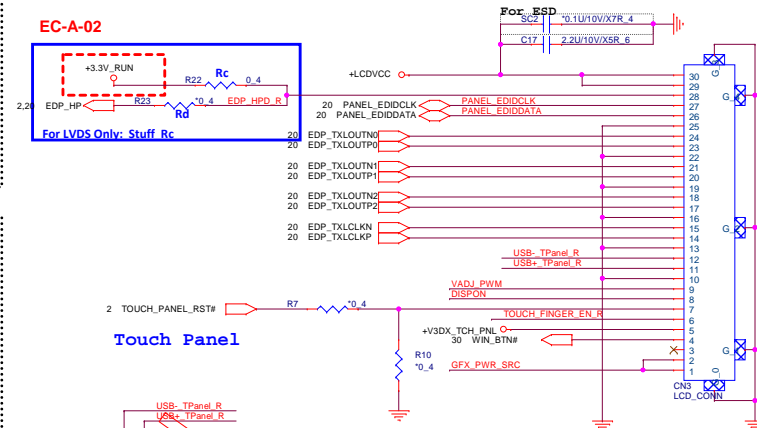


CAMERA VCC Control

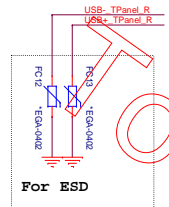
+CAM_VCC
Max Current : 800mA



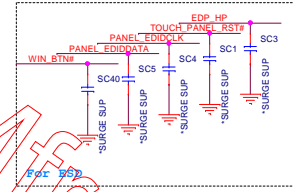
EC-A-02



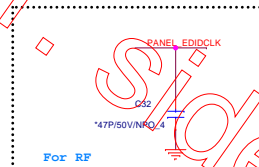
Touch Panel



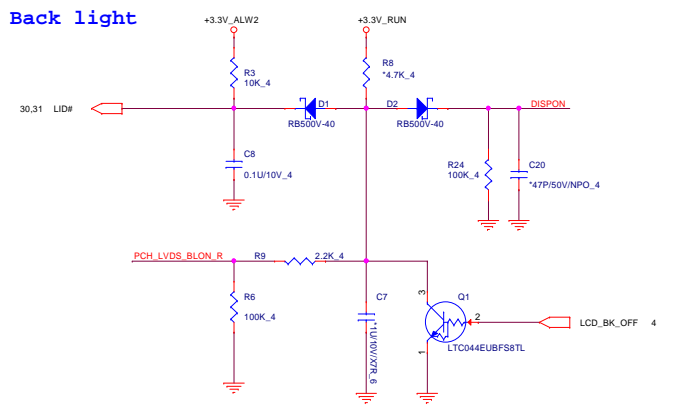
For ESD



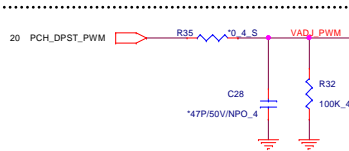
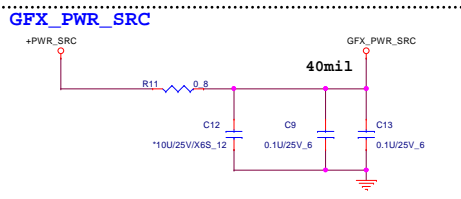
For RF

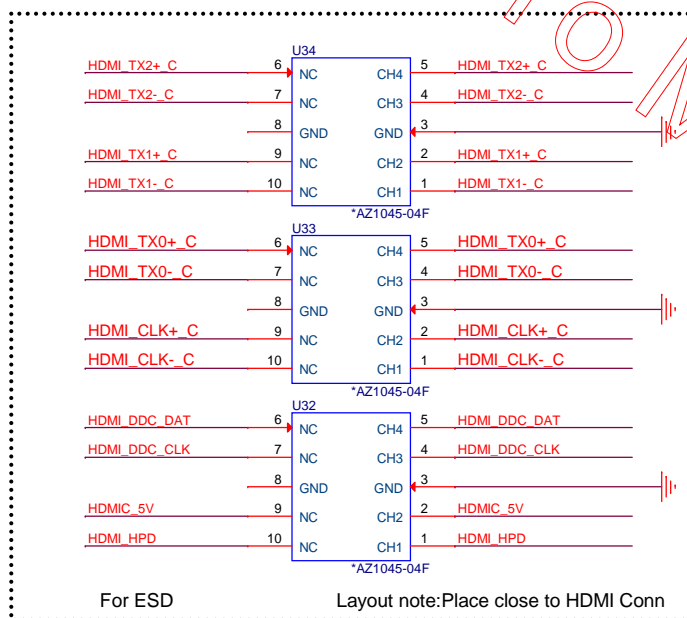
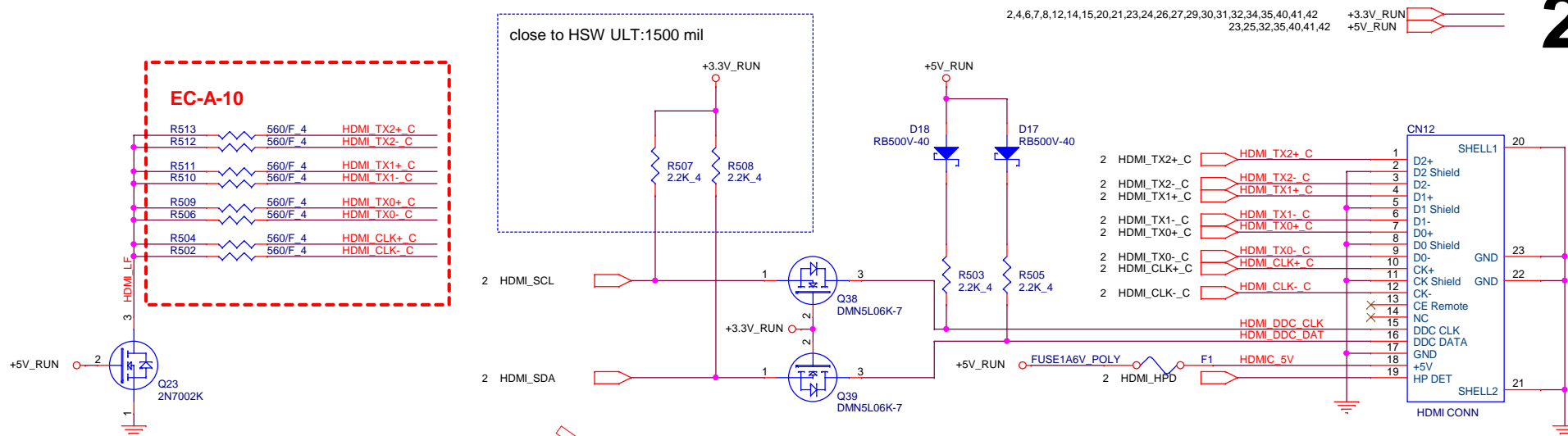


Back light

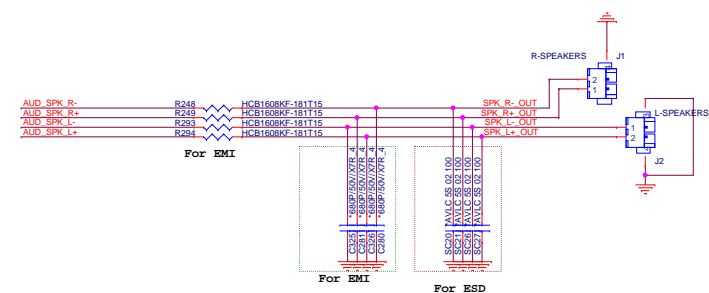
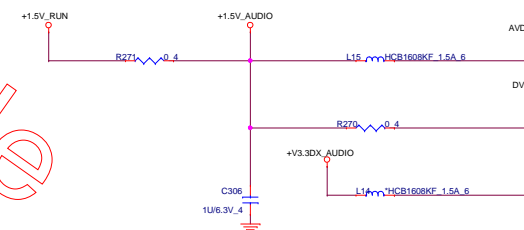
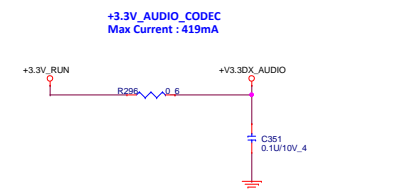
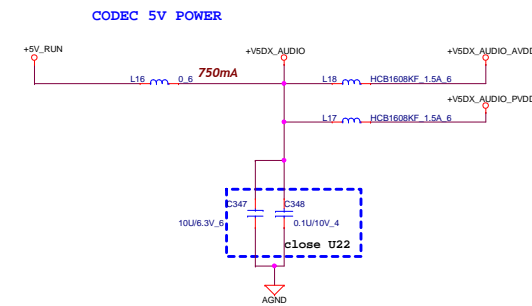
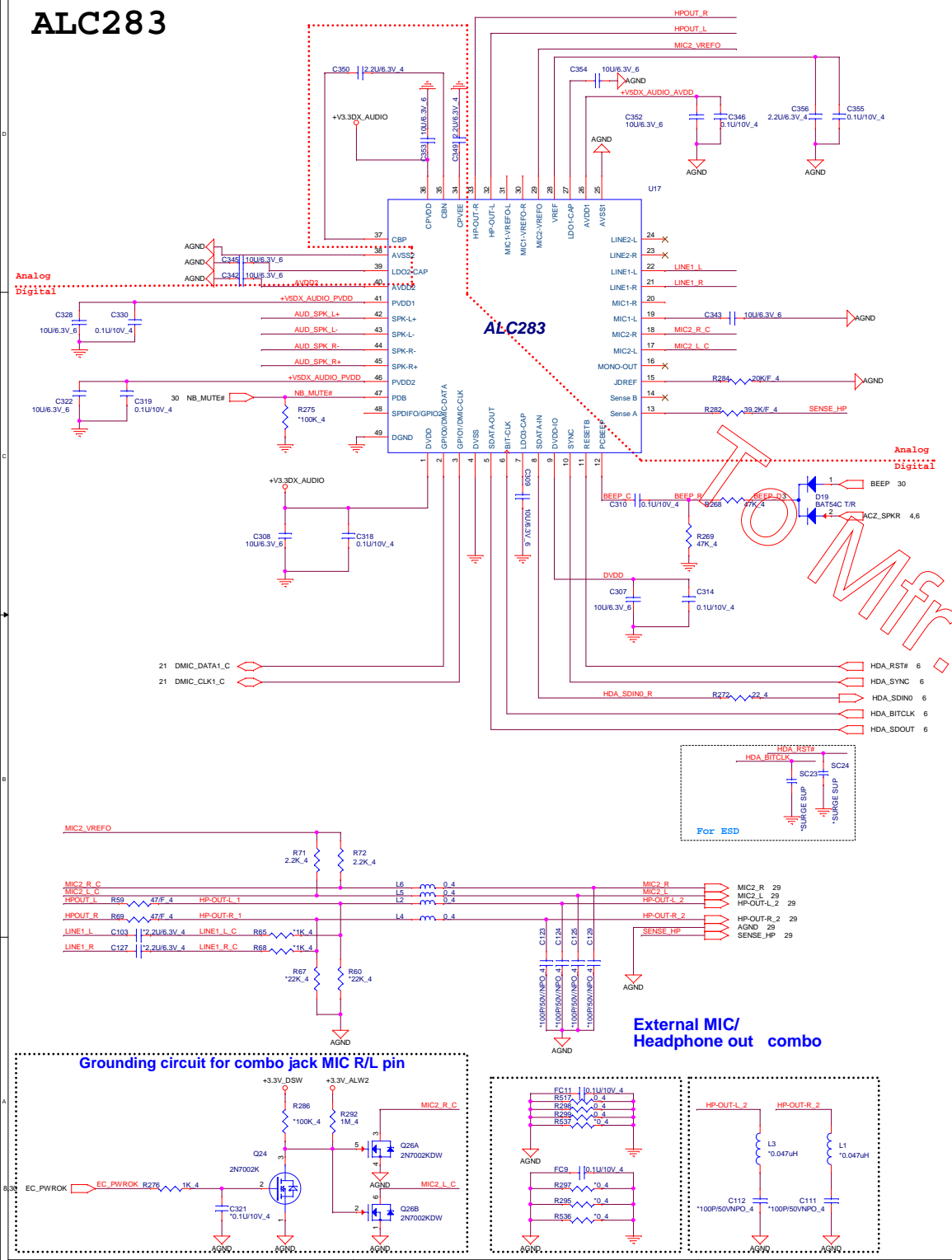


GFX_PWR_SRC

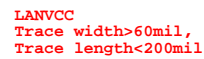




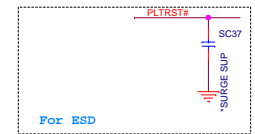
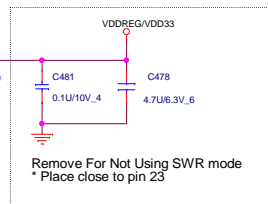
ALC283



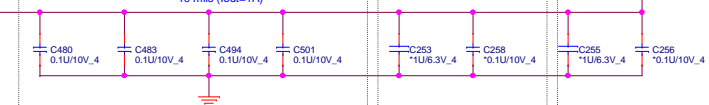
INT Speaker



10/100	RTL8106EUS-CG	AL008106002
1G	RTL8111GUS-CG	AL008111009

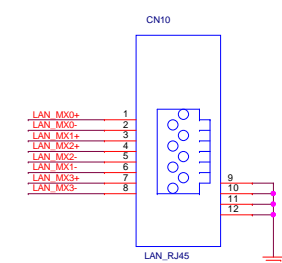
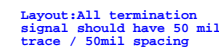


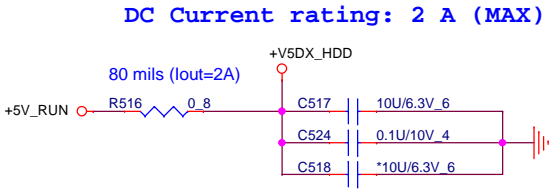
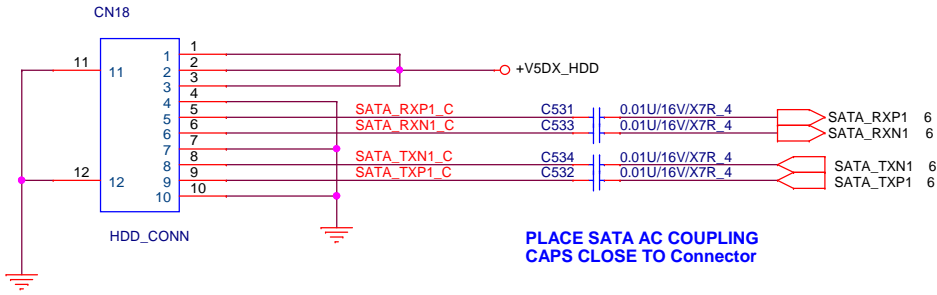
For RTL8111GUS
* Place 0.1uF CAP close to each
VDD10 pin-- 3, 8, 22, 30 For RTL8106E
* Place 0.1uF CAP close to each VDD10 pin-- 8, 30
40 mils (out=1A)




For RTL8111GUS
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

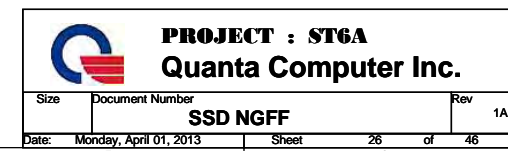
8 Transformer





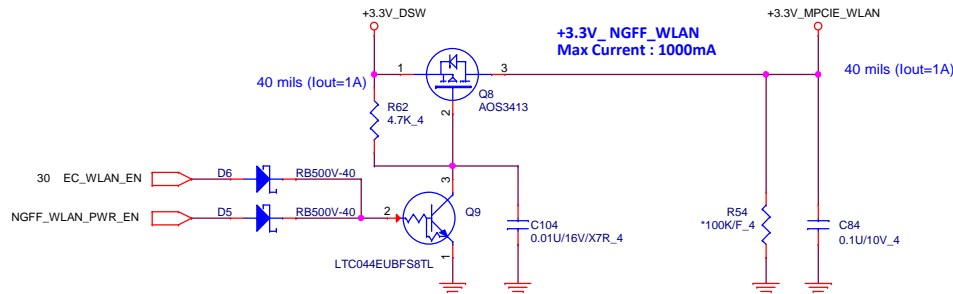
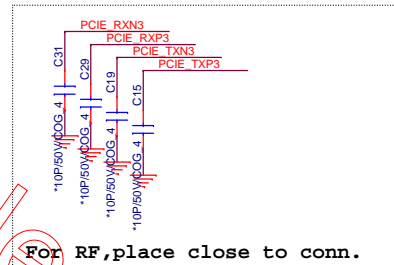
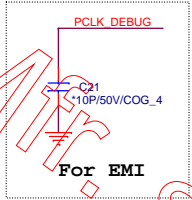
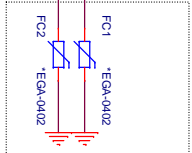
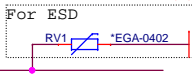
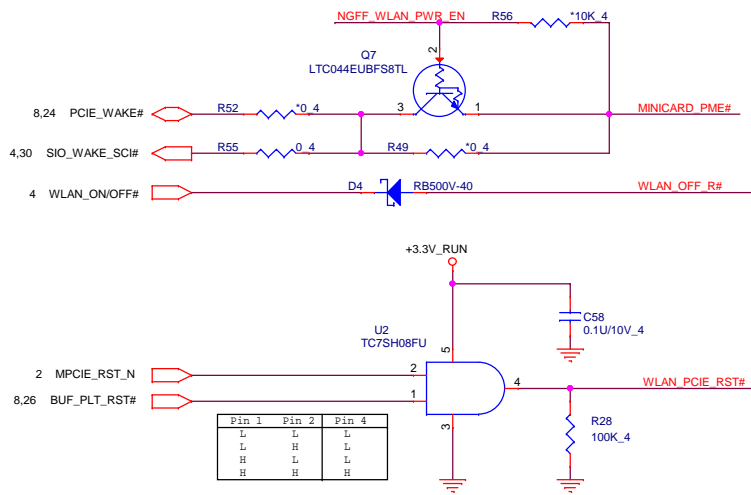
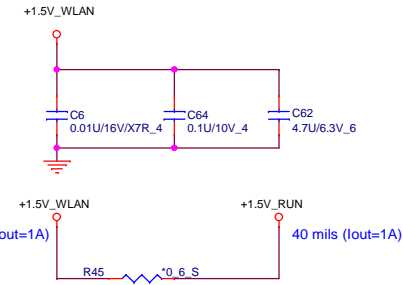
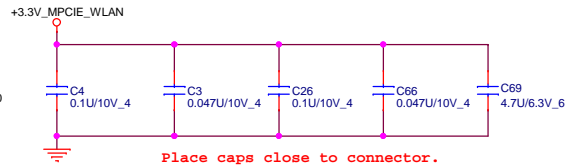
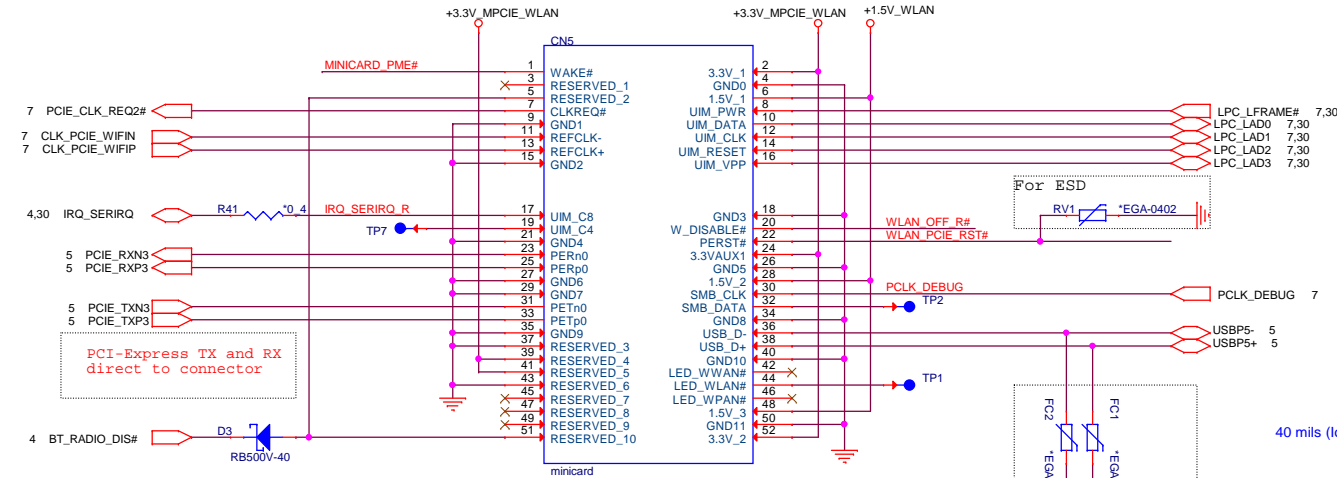
To Mfr. Side

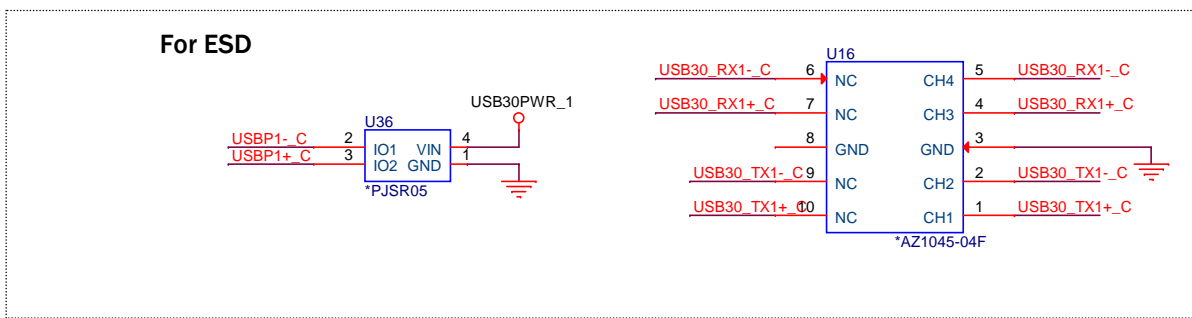
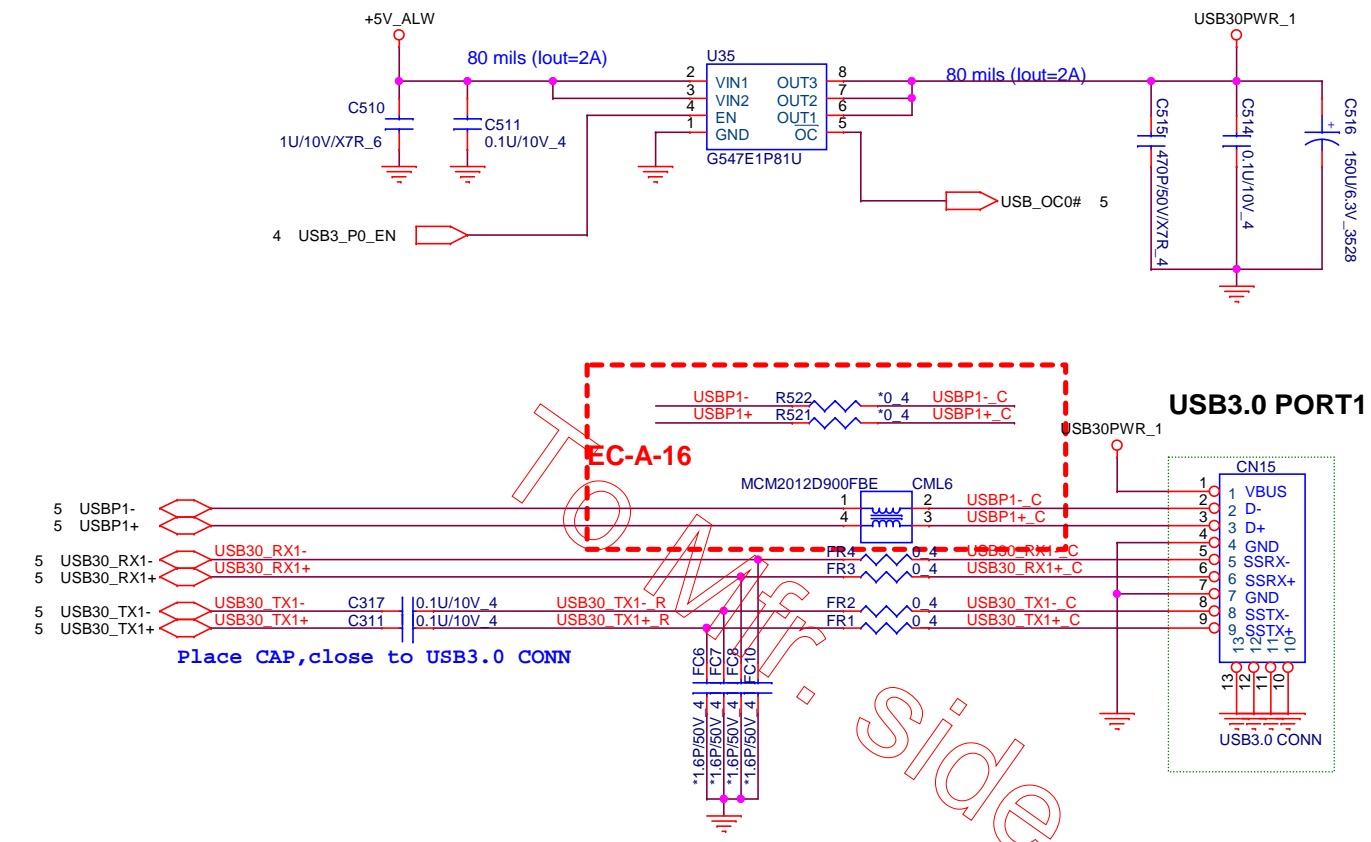
		PROJECT : ST6A	
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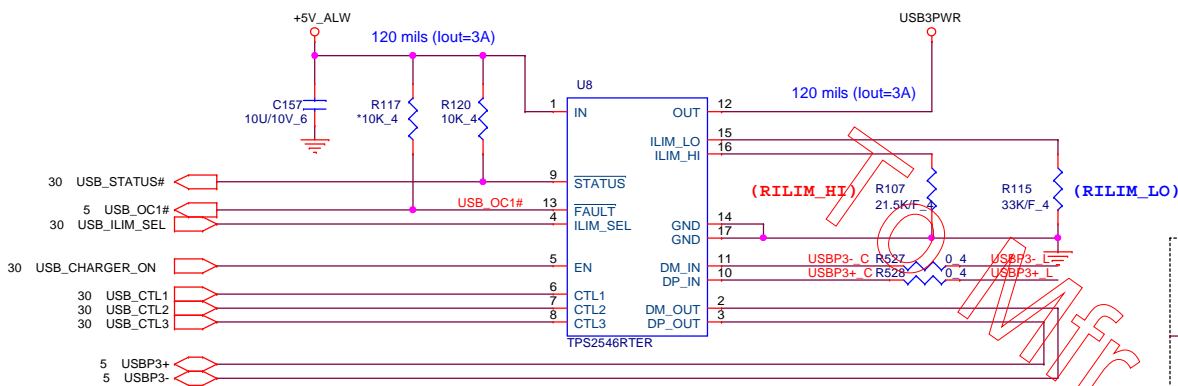
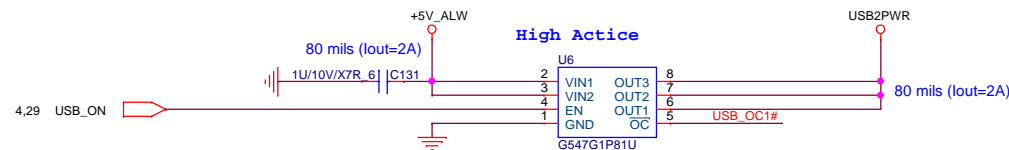
Mini PCIE Wifi/BT connector

27





USB 2.0 Port *2



RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:

1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used

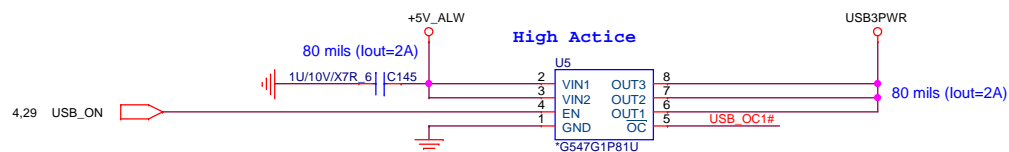
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.

The following equation programs the typical current limit:

(1)

RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS_typ}(mA) = \frac{50,500}{(R_{ILIM_XX}(k\Omega) + 0.1)}$$



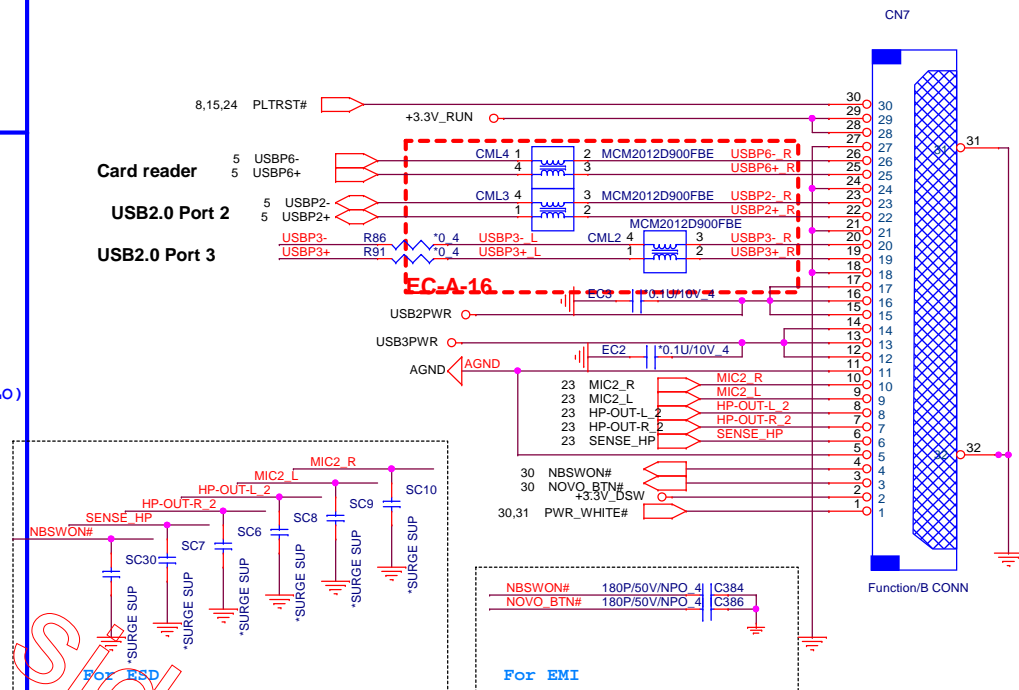
12,14,28,35,36,37,38,39,41,42,43,44 +5V_ALW
4,6,8,12,23,24,27,31,35,36,41,44 +3.3V_DSW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,30,31,32,34,35,40,41,42 +3.3V_RUN

29

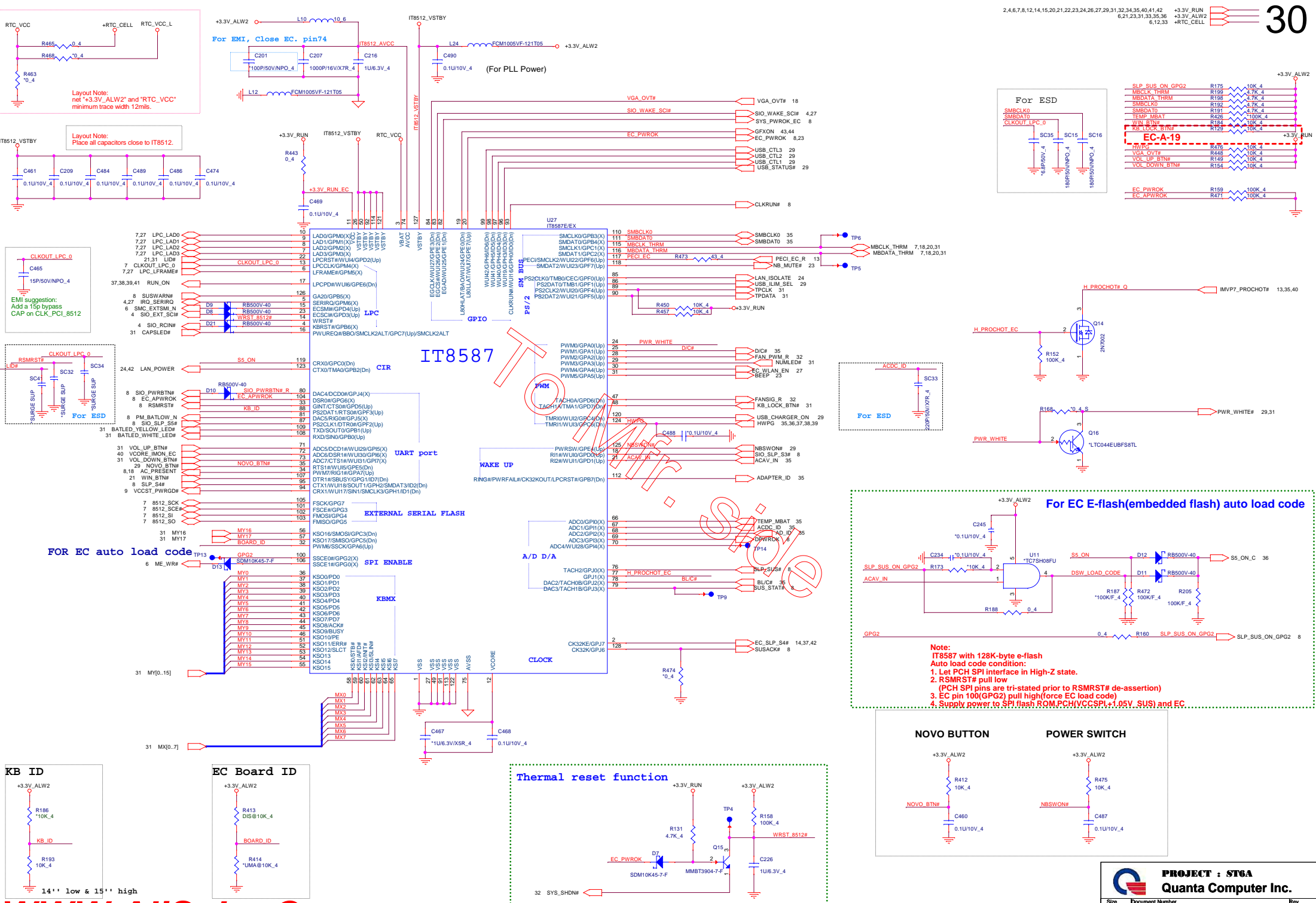
Card reader

USB2.0 Port 2

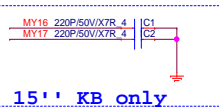
USB2.0 Port 3



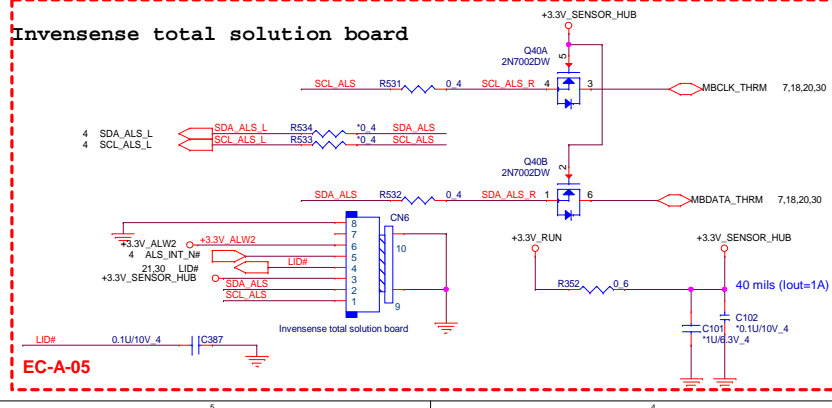
EC-A-04



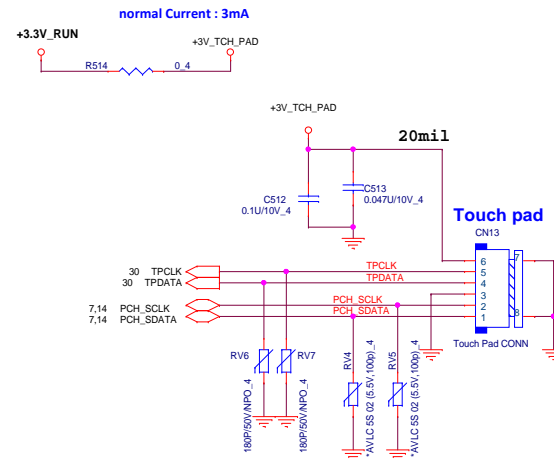
14'' KB



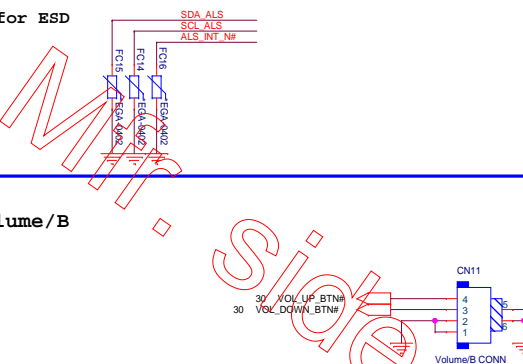
Invensense total solution board



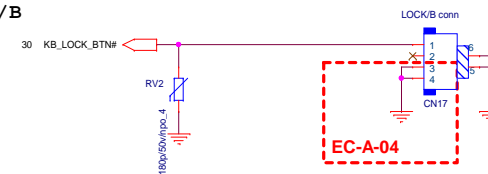
~~reserve~~ for ESD



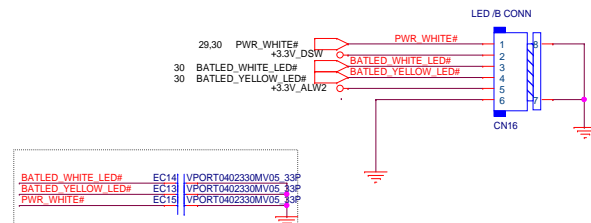
Volume/B



LOCK/B



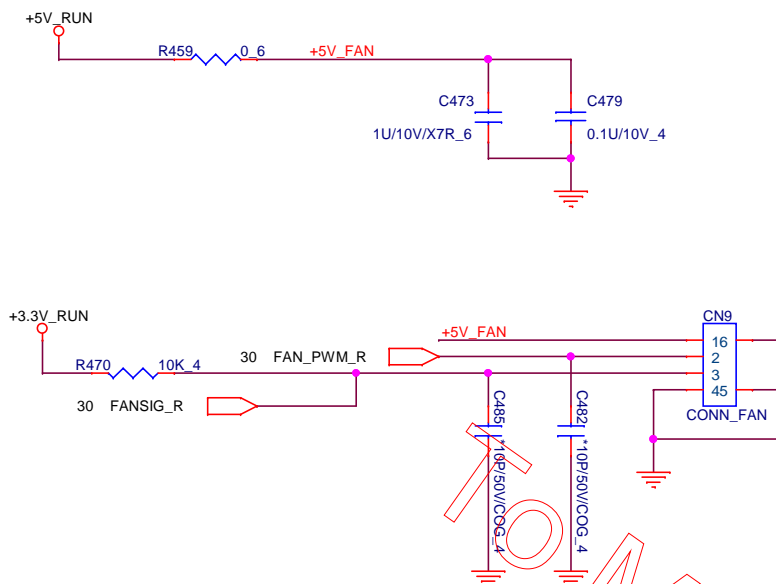
LED /B



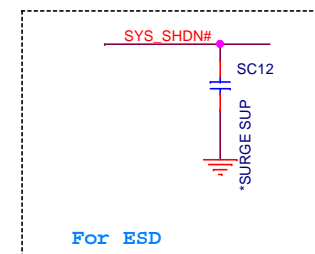
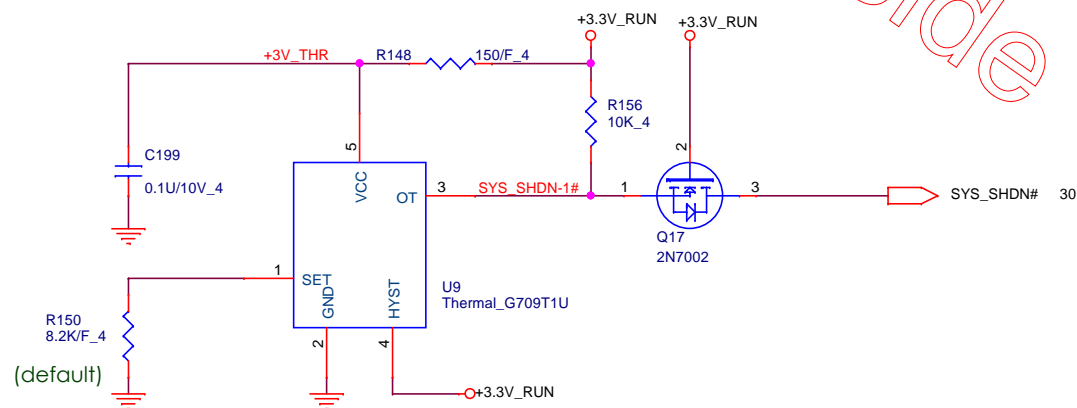
FAN CONTROL

2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,34,35,40,41,42 +3.3V_RUN
22,23,25,35,40,41,42 +5V_RUN

32

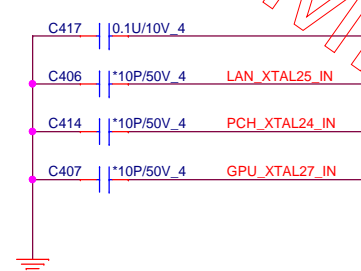
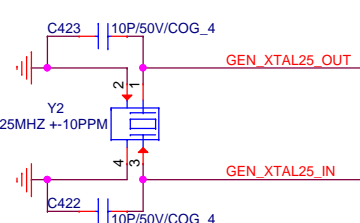
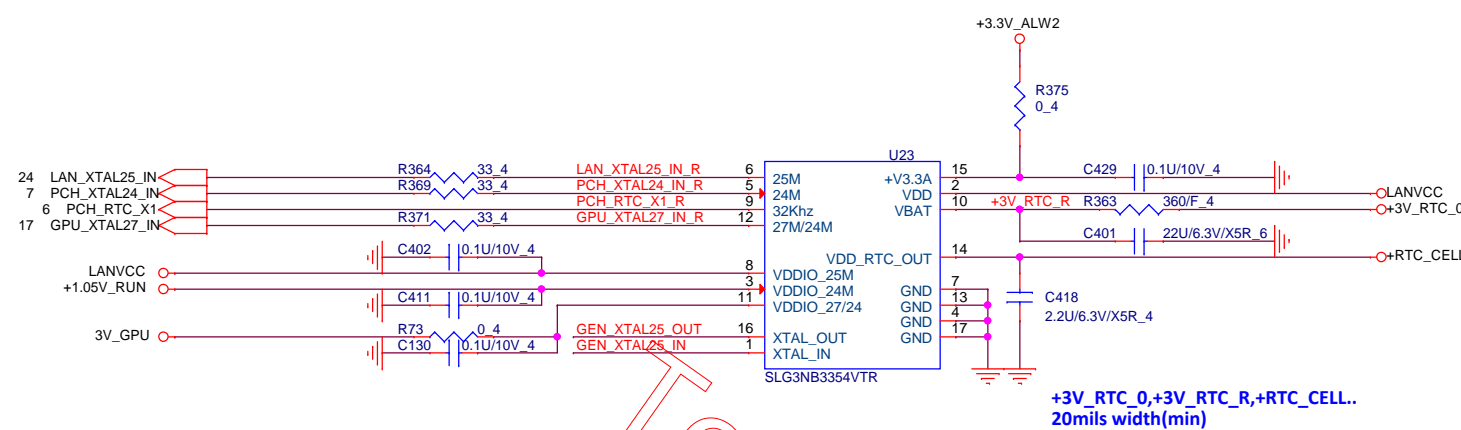


Thermal Sensor

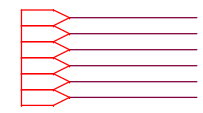


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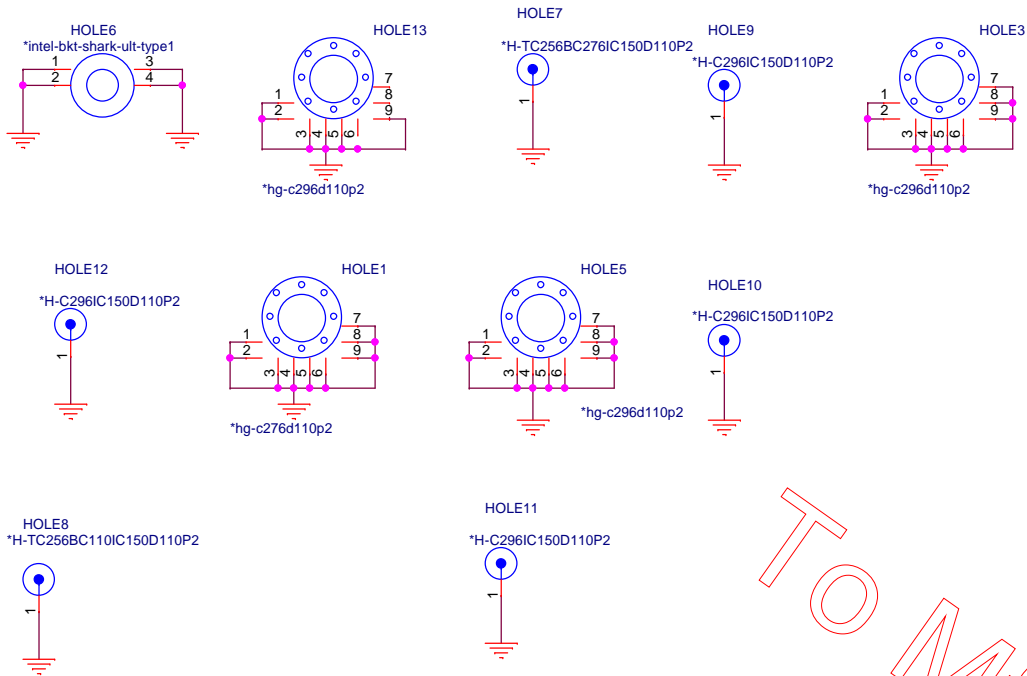
6,21,23,30,31,35,36 +3.3V_ALW2
24,42 LANVCC
6 +3V_RTC_0
6,12,30 +RTC_CELL
6,9,12,34,38,40,42,44 +1.05V_RUN
15,18,34,43,44,45 3V_GPU



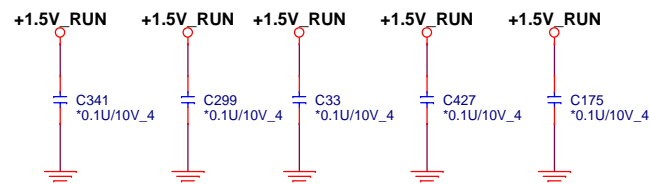
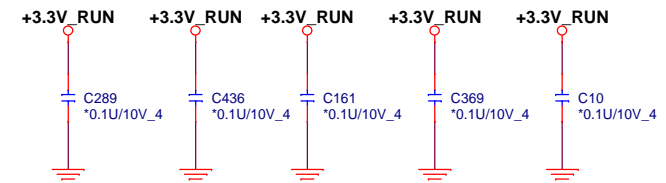
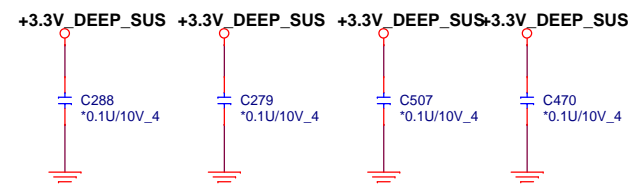
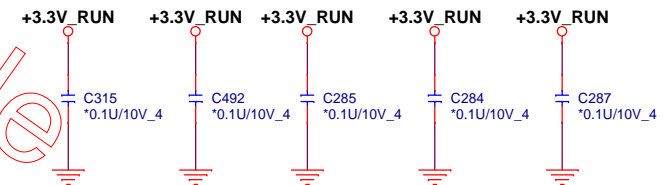
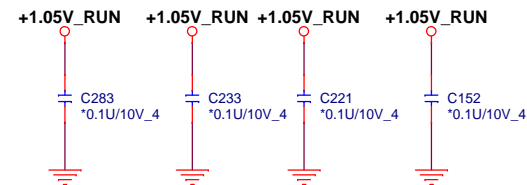
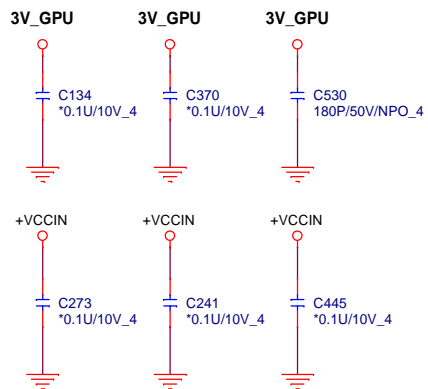
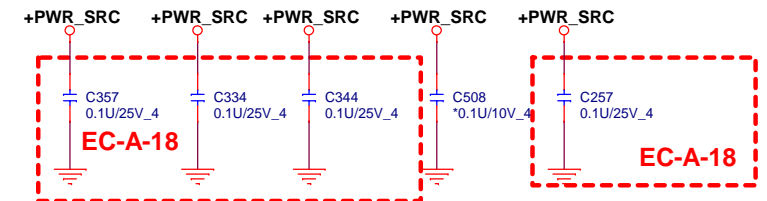
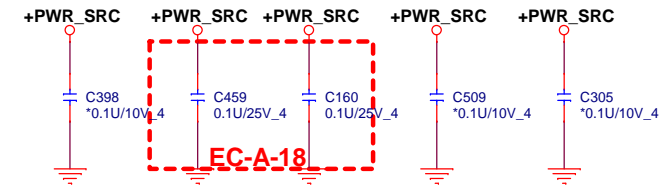
33

SLG3NB3354VTR(AL003354001)====>DIS
32Kx1+24M*1+25Mx1+27Mx1
1.S430-DIS --> SLG3NB3354
2.S430-UMA --> SLG3NB3355


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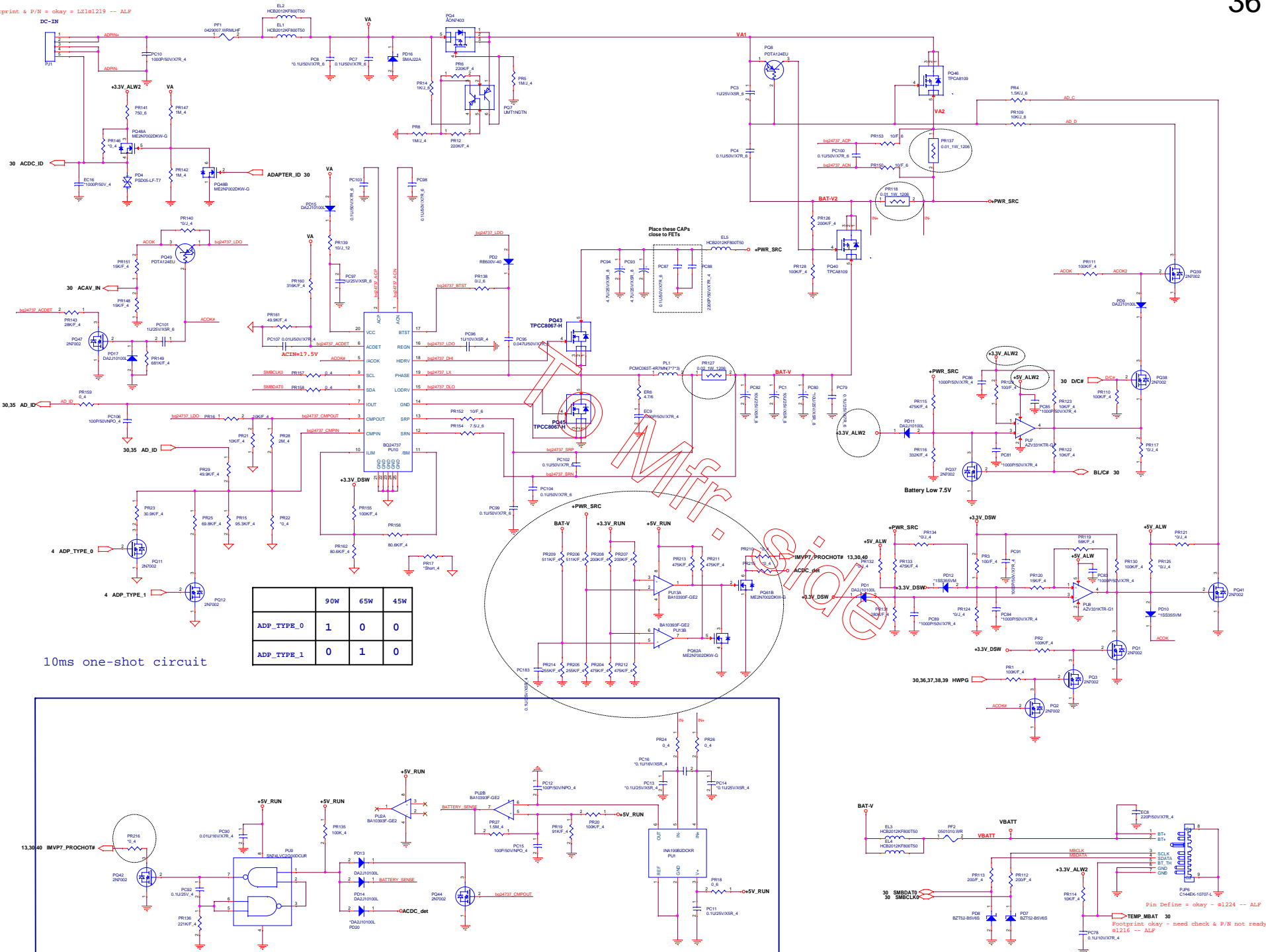
EC-A-18

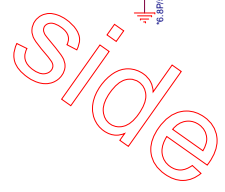


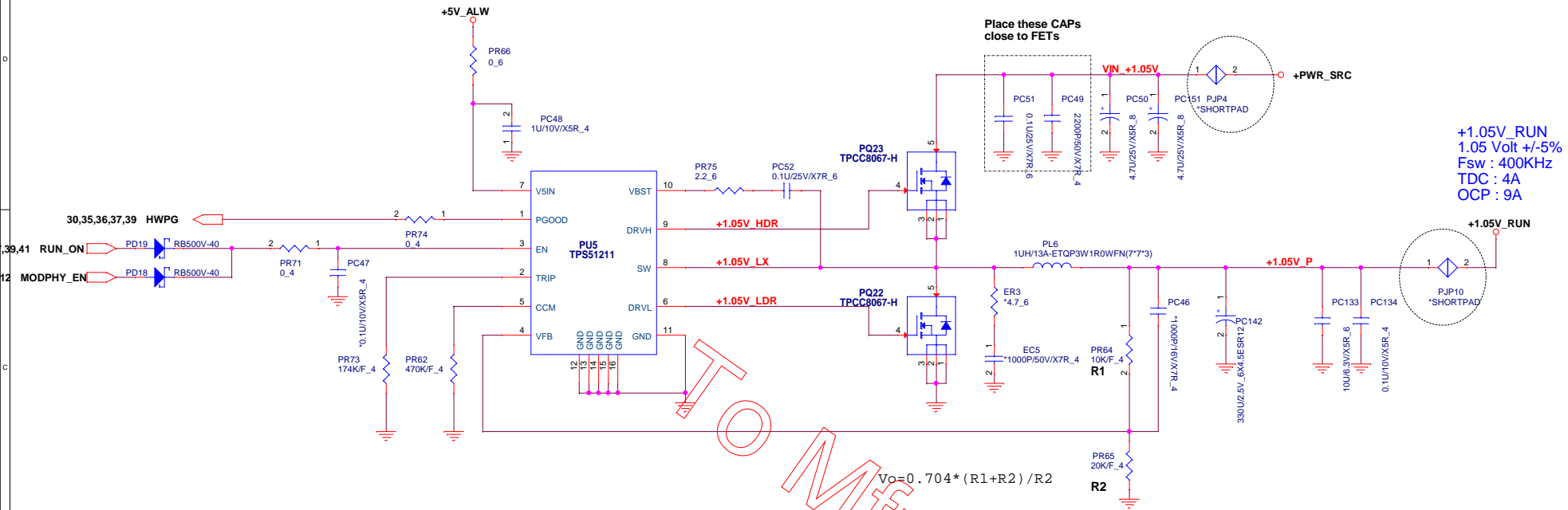
EMI reserve

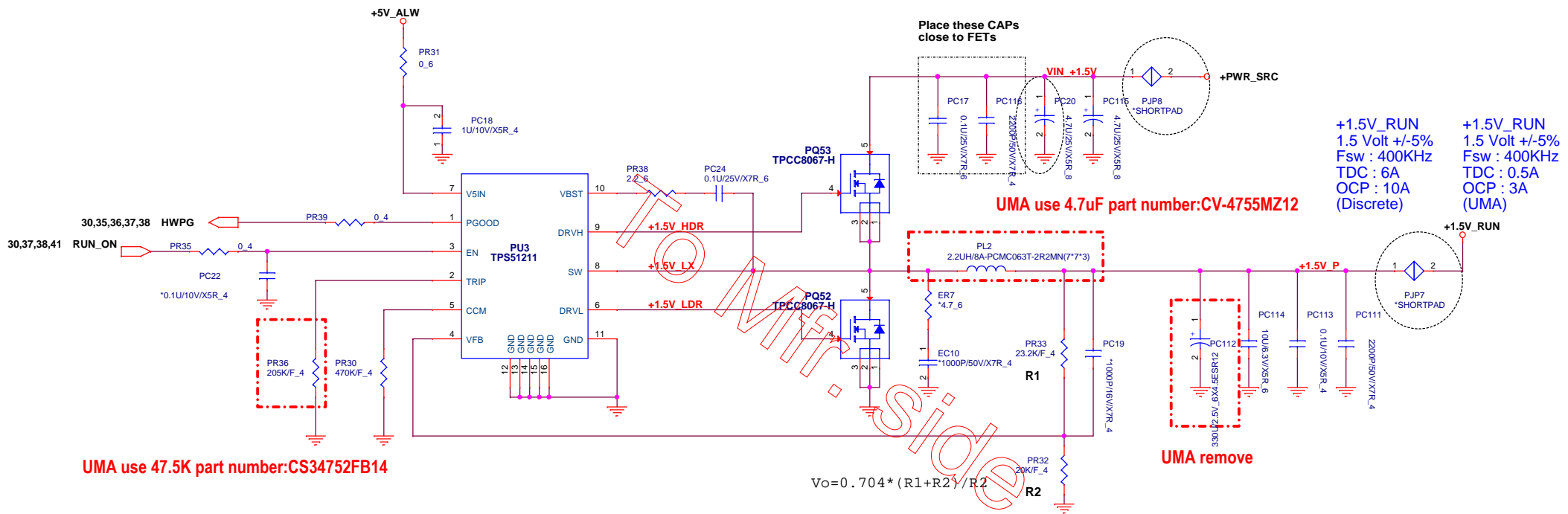
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	Screw Hole/EMI	1A
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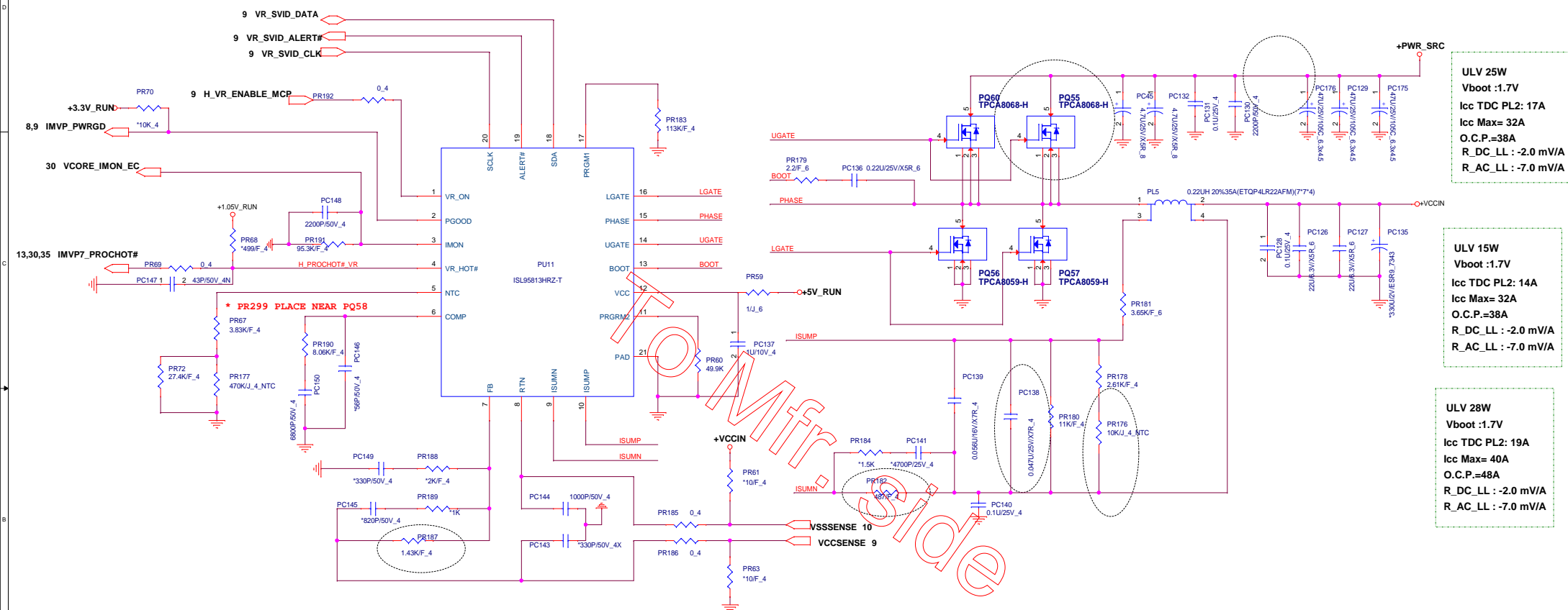
Footprint & P/N = okay = L2181219 -- ALP





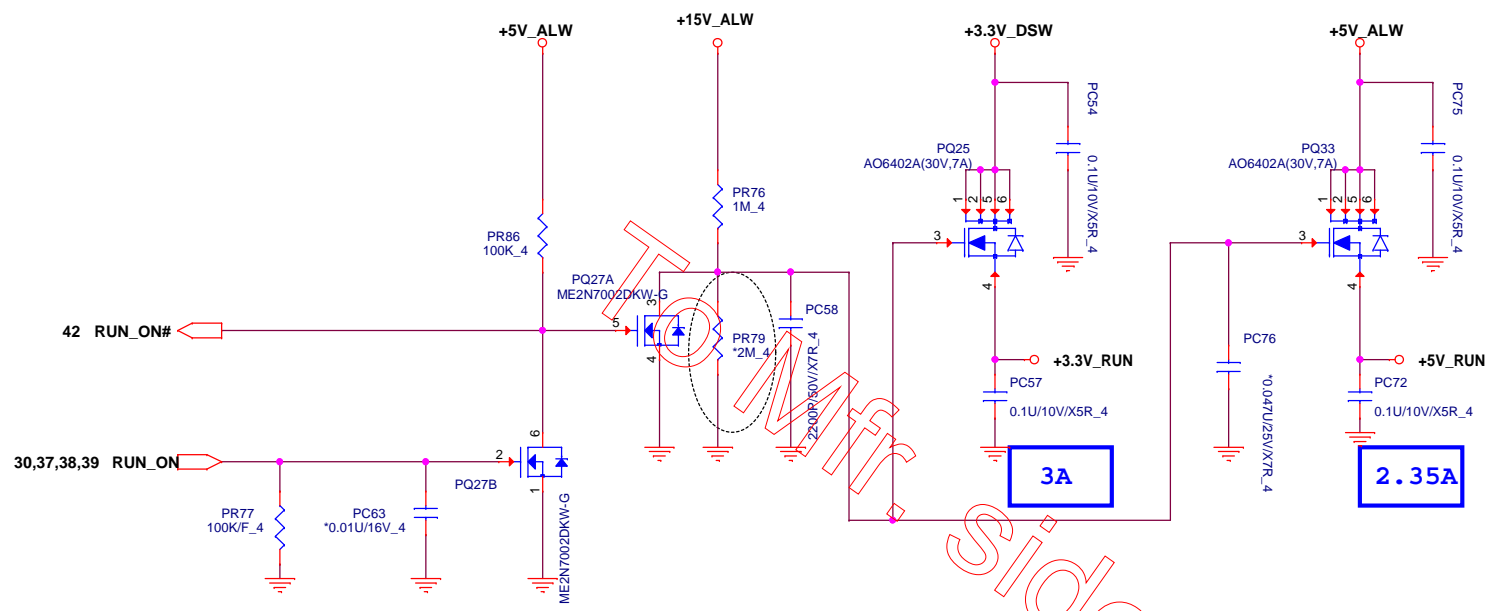






12,14,28,29,35,36,37,38,39,42,43,44
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,42
4,6,8,12,23,24,27,29,31,35,36,44
6,9,12,33,34,38,40,42,44

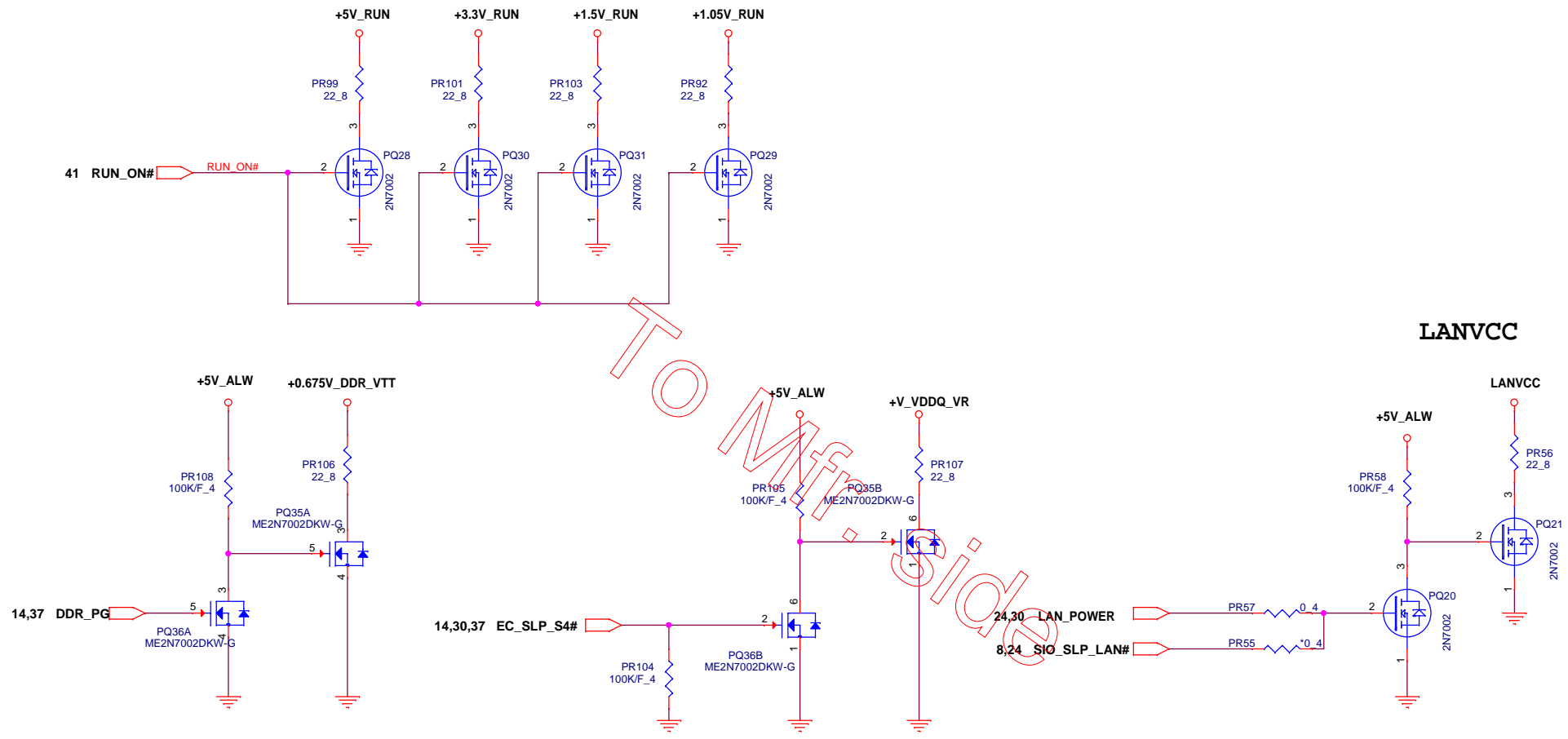
+5V_ALW
+15V_ALW
+5V_RUN
+3.3V_RUN
+3.3V_DSW
+1.05V_RUN




DISCHARGE

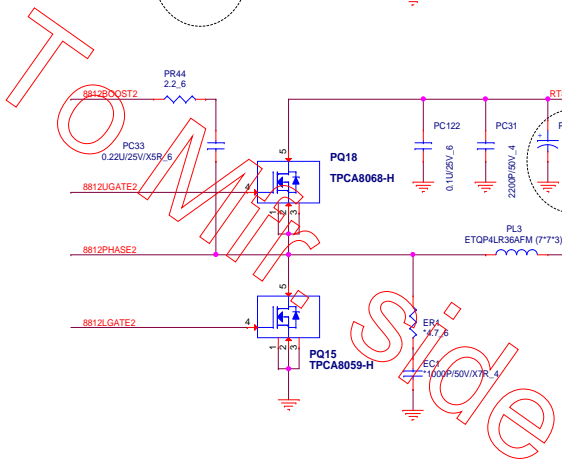
12,14,28,29,35,36,37,38,39,41,43,44	+5V_ALW
22,23,25,32,35,40,41	+5V_RUN
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41	+3.3V_RUN
12,23,27,34,39,44	+1.5V_RUN
6,9,12,33,34,38,40,44	+1.05V_RUN
14,37	+0.675V_DDR_VTT
4,5,6,7,8,12,14,34	+3.3V_DEEP_SUS
9,14,37	+V_VDDQ_VR
24,33	LANVCC
36,41,44	+15V_ALW

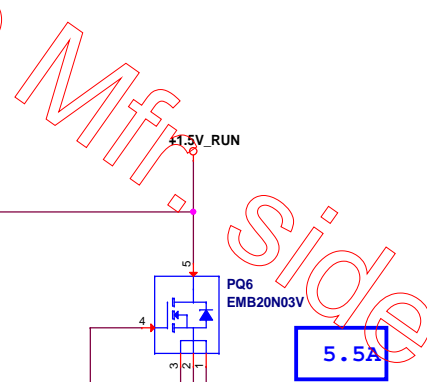
43



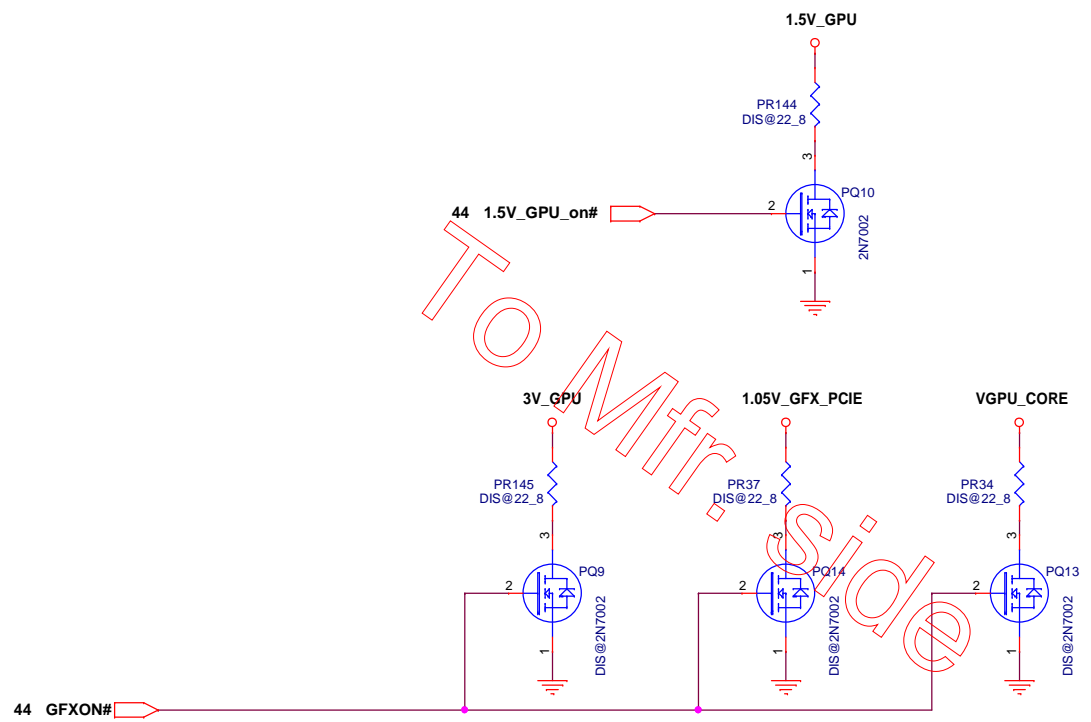
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12,14,28,29,35,36,37,38,39,41,42,43,44 +5V_ALW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
12,23,27,34,39,42,44 +1.5V_RUN
6,9,12,33,34,38,40,42,44 +1.05V_RUN
14,37,42 +0.675V_DDR_VTT
9,14,37,42 +V_VDDQ_VR
24,33,42 LANVCC
36,41,44 +15V_ALW



SDV~SIV

2013	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
SDV~SIV	EC-A-01	21	02/07		Change touch panel VCC control to +3.3V_RUN and stuff R17
	EC-A-02	21	02/07		Add +3.3V_RUN to provide LCD panel EDID VCC and stuff R22
	EC-A-03	20	02/08	C147	depop C147 from vendor request
	EC-A-04	29,31	02/22	U10,C466	remove U10,C466 for lid change to sensor B
	EC-A-05	29,31	03/05		sensor hub remove and reserve light sensor for I2C interface
	EC-A-06	29	03/05	R528,R528	add R527,R528 to avoid stub
	EC-A-07	7	03/05		CLKREQ change
	EC-A-08	24	03/05		lan surge solution change
	EC-A-09	21	03/06		RTD2132R support initial PWM to product LCDVCC
	EC-A-10	21	03/06	R502,R504,R506,R509 R510,R511,R512,R513	change value to meet design guide
	EC-A-11	29	03/13	R107	change to 21.5K for charger limit setting
	EC-A-12	15	03/15		Q10 pin2 change to GFXPG control
	EC-A-13	20	03/11	U24	depop
	EC-A-14	12	03/12		change to +5V_ALW
	EC-A-15	21	03/12	CN4	Change to 10 pin conn.
	EC-A-16	29	03/18	CML2,CML3,CML4,CML6 R85,R90,R96,R101,R118,R119,R521,R522	CML2,CML3,CML4,CML6 pop for EMI suggestion R85,R90,R96,R101,R118,R119,R521,R522 depop for EMI suggestion
	EC-A-17	22	03/18	R264,R265,R266,R267	R264,R265,R266,R267 pop for EMI suggestion
	EC-A-18	34	03/18	C160,C257,C334,C357 and C459	C160,C257,C334,C357 and C459 pop for EMI suggestion
	EC-A-19	30	03/19		KB_LOCK_BTN# pull up to +3.3V_ALW2
	EC-A-20	21	03/19	R20,R21,CML7	delete R20,R21 and add CML7
	EC-A-21	21	03/22	U39,R535,C529	reserve to meet LCD off sequence



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