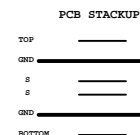


Project code: 91.4CG01.001  
PCB P/N : 48.4CG01.0SA  
REVISION : 08245-SA



<b>SYSTEM DC/DC</b>		<b>42</b>
<b>ISL62392</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCATOUT	SV_5V1(6A) 30DV_5V1(7A) 30V_AUX_5S 30DV_AUX_5S	
<b>SYSTEM DC/DC</b>		<b>43</b>
<b>TPS51124</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCATOUT	10DV_5S(8A) 10DV_5S(12A)	
<b>RT9026</b>		<b>44</b>
10DV_5S	20V_4REF_5S 11.2A	
<b>RT9018</b>		<b>44</b>
10DV_5S	10DV_5S(2A)	
<b>TPS51117</b>		<b>45</b>
DCATOUT	PWIDE(4A)	
<b>CHARGER</b>		
<b>ISL87931A</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCATOUT	B+	
<b>CPU DC/DC</b>		<b>41</b>
<b>ISL6266A</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCATOUT	VIO_CORE 10A	
<b>VGA CORE</b>		<b>47</b>
<b>RT9202A</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCATOUT	VGA_CORE 13A	
<b>GPU CORE</b>		<b>46</b>
<b>ISL6263A</b>		
<b>INPUTS</b>	<b>OUTPUTS</b>	
DCATOUT	VIO_GPUCORE 7A	

A

B

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

C

D

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPBSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

E

F

CantigaD Chipset and ICH9M I/O Controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0= The ITPM Host Interface is enabled(Note2) 1=The ITPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default);Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default); Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/HDMDI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 =Digital Display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G/MCH Power OK (PWROK) signal.  
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.  
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

JV50

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Wistron Corporation

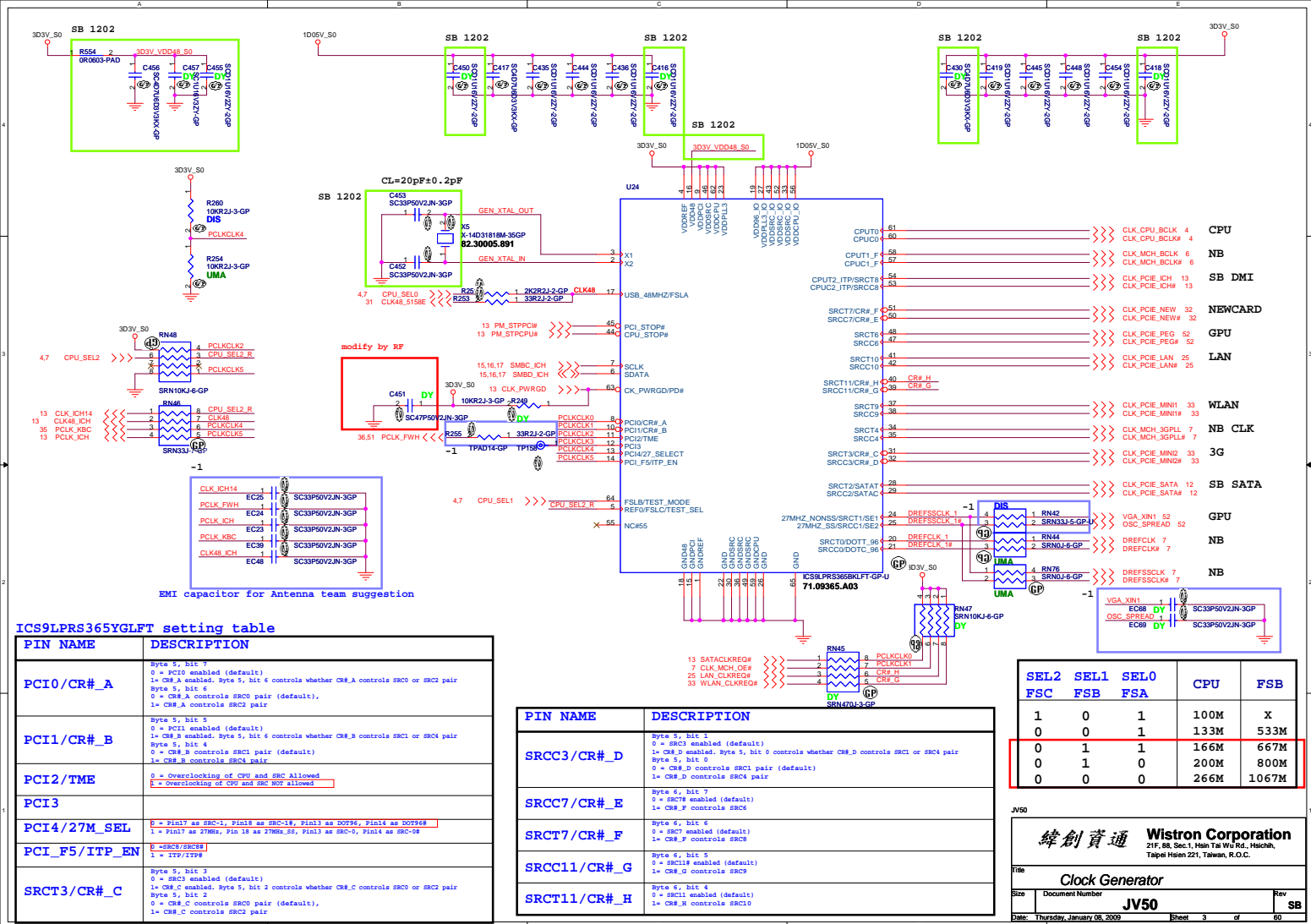
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Title

Reference

Size A3 Document Number JV50 Rev SB

Date: Thursday, January 08, 2009 Sheet 2 of 60



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

JV50

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Taipei Hsien 221, Taiwan, R.O.C.

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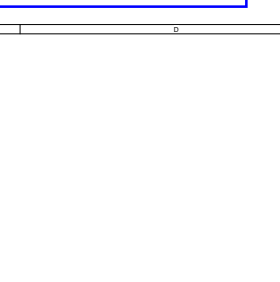
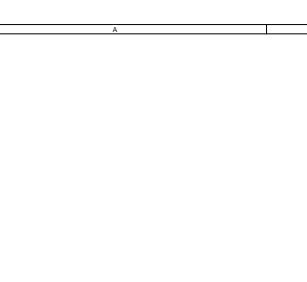
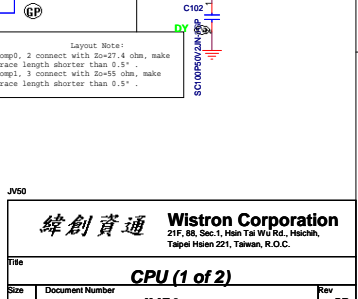
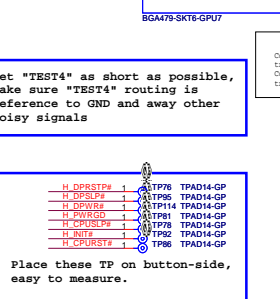
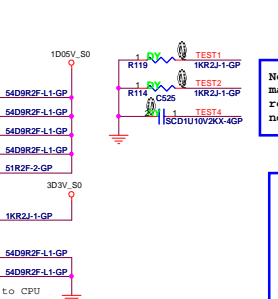
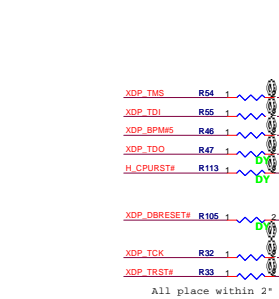
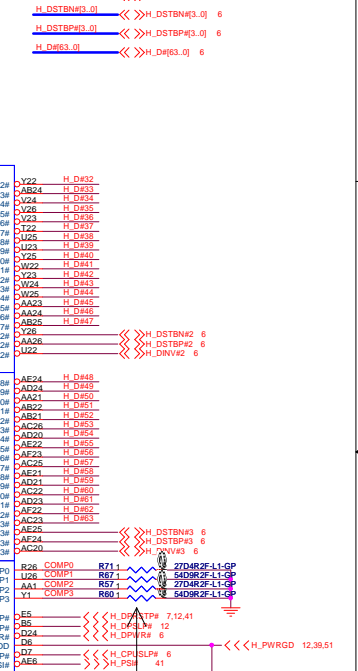
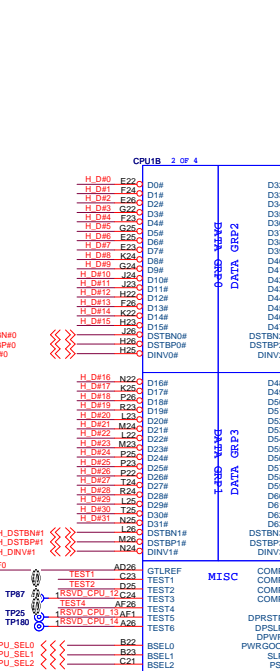
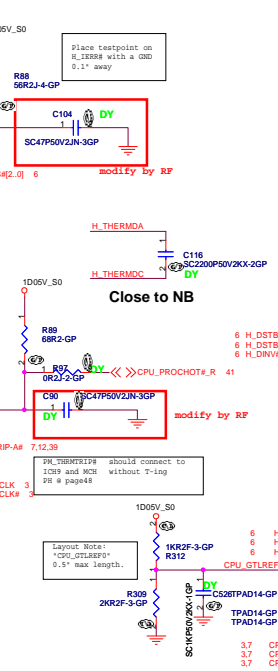
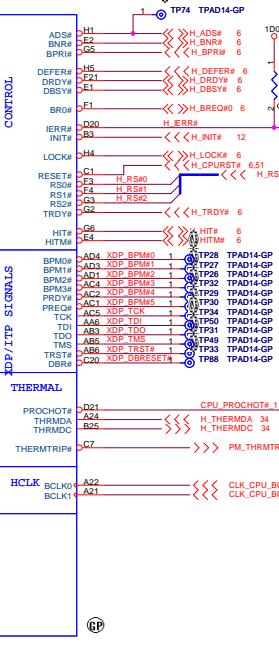
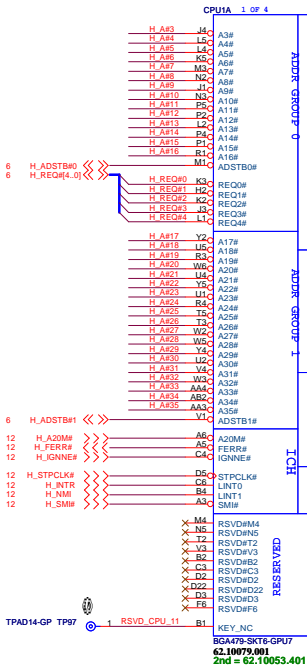
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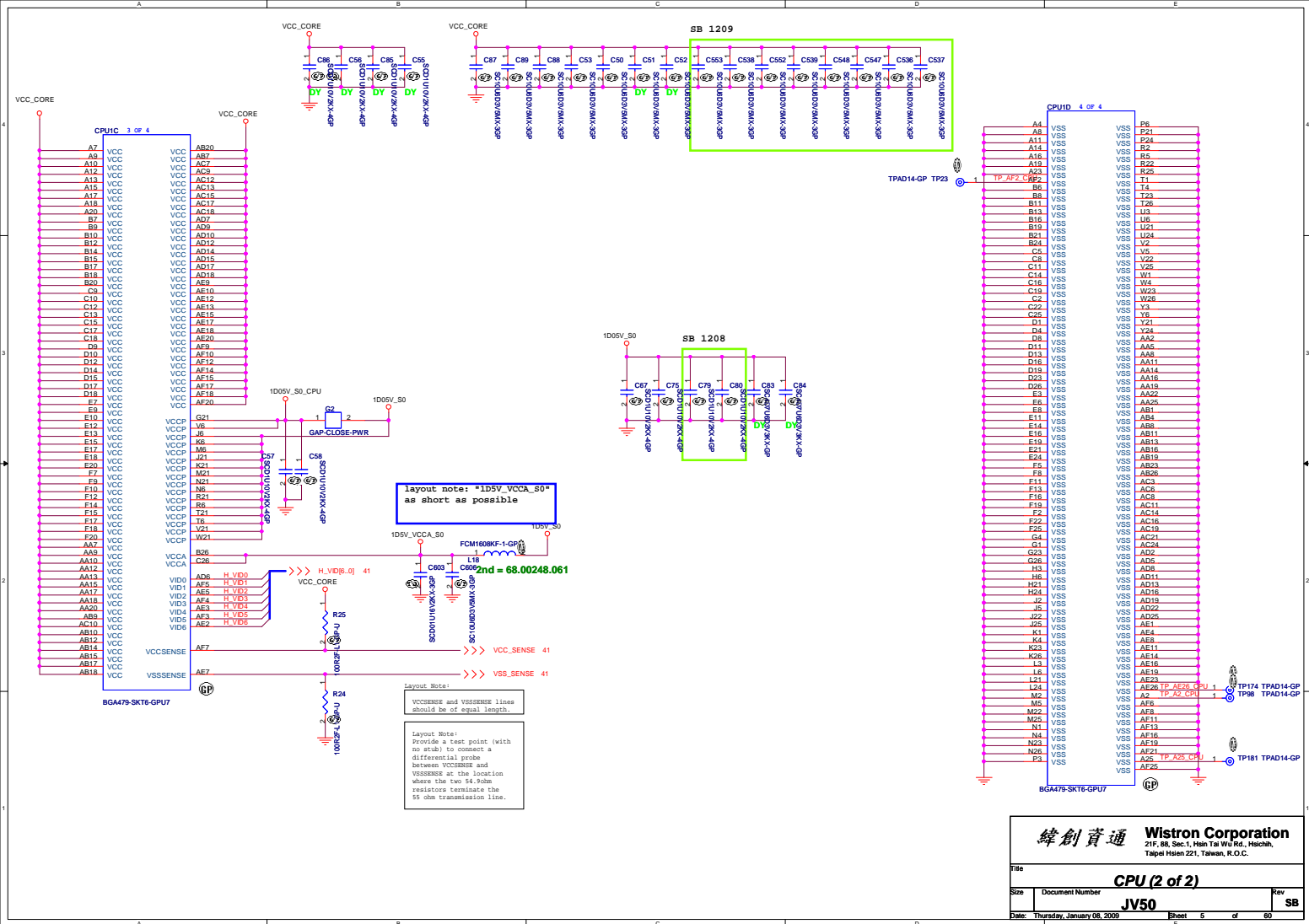
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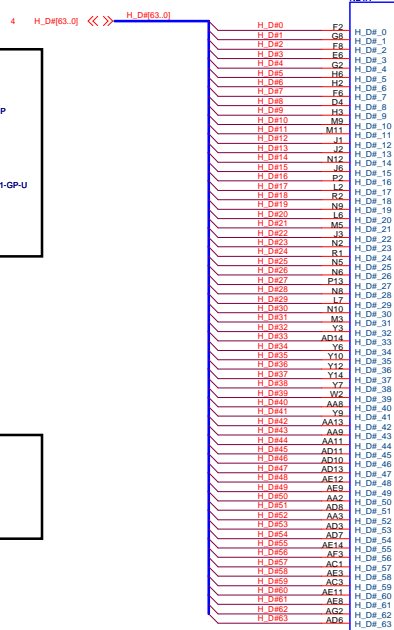
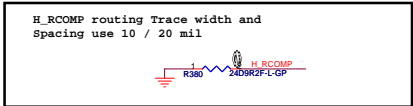
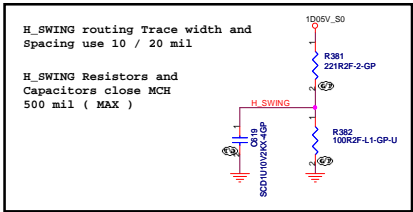
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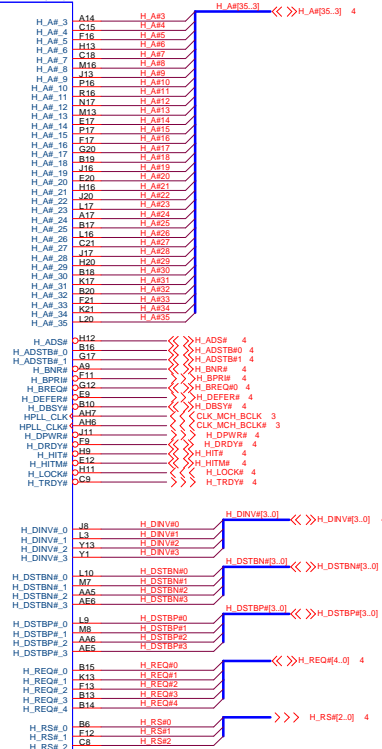
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HOST



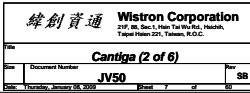
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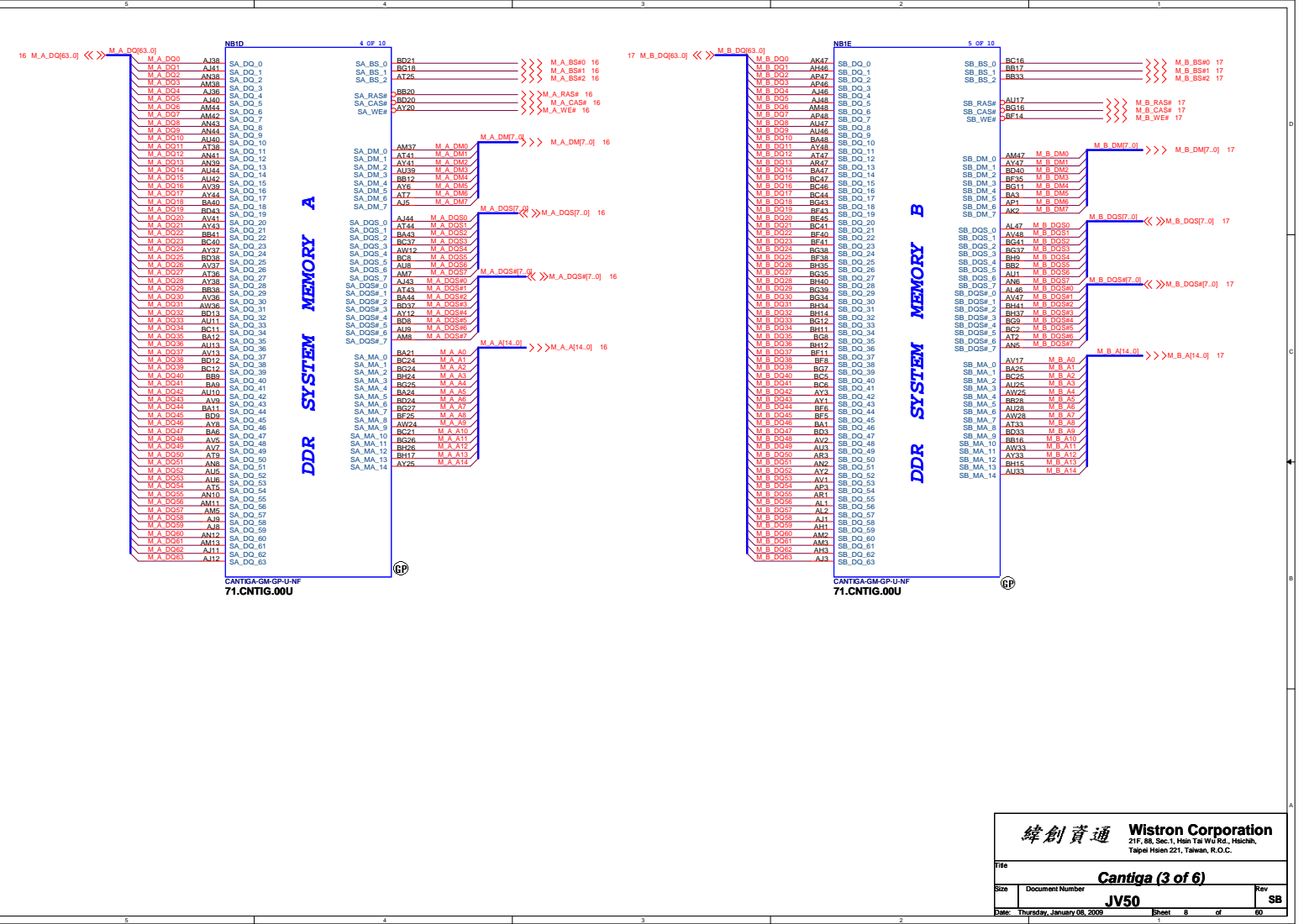
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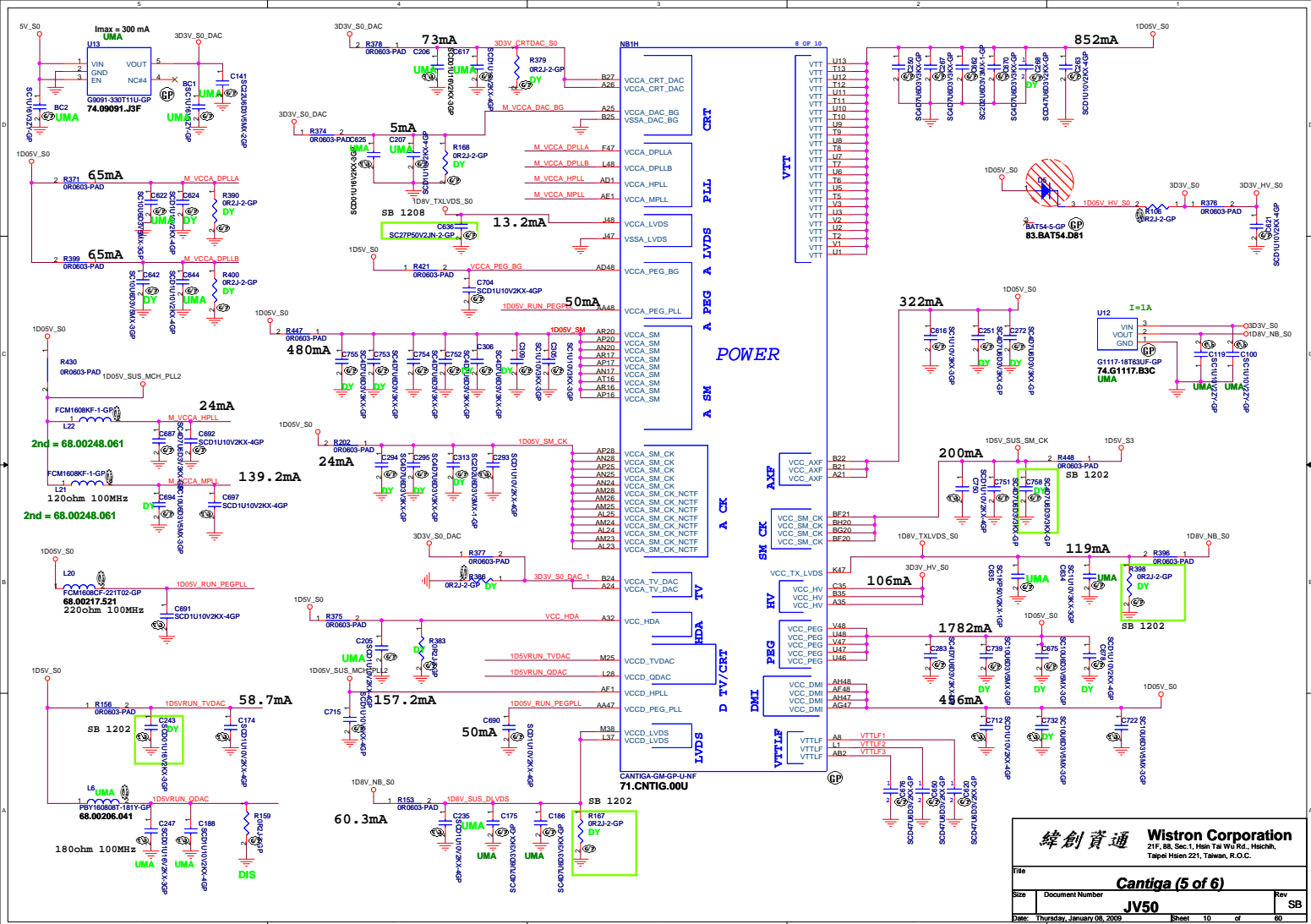
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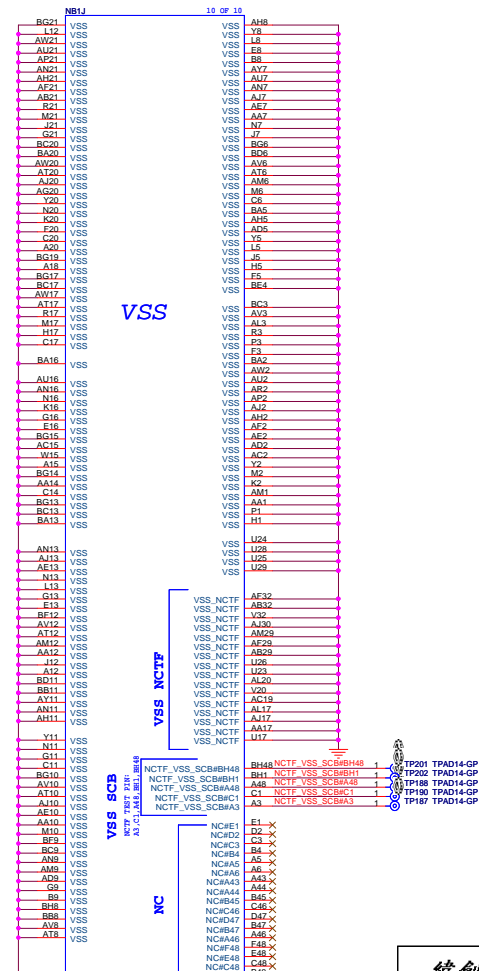
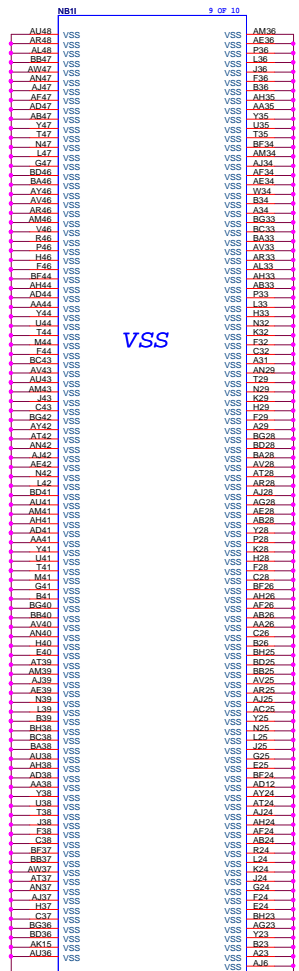
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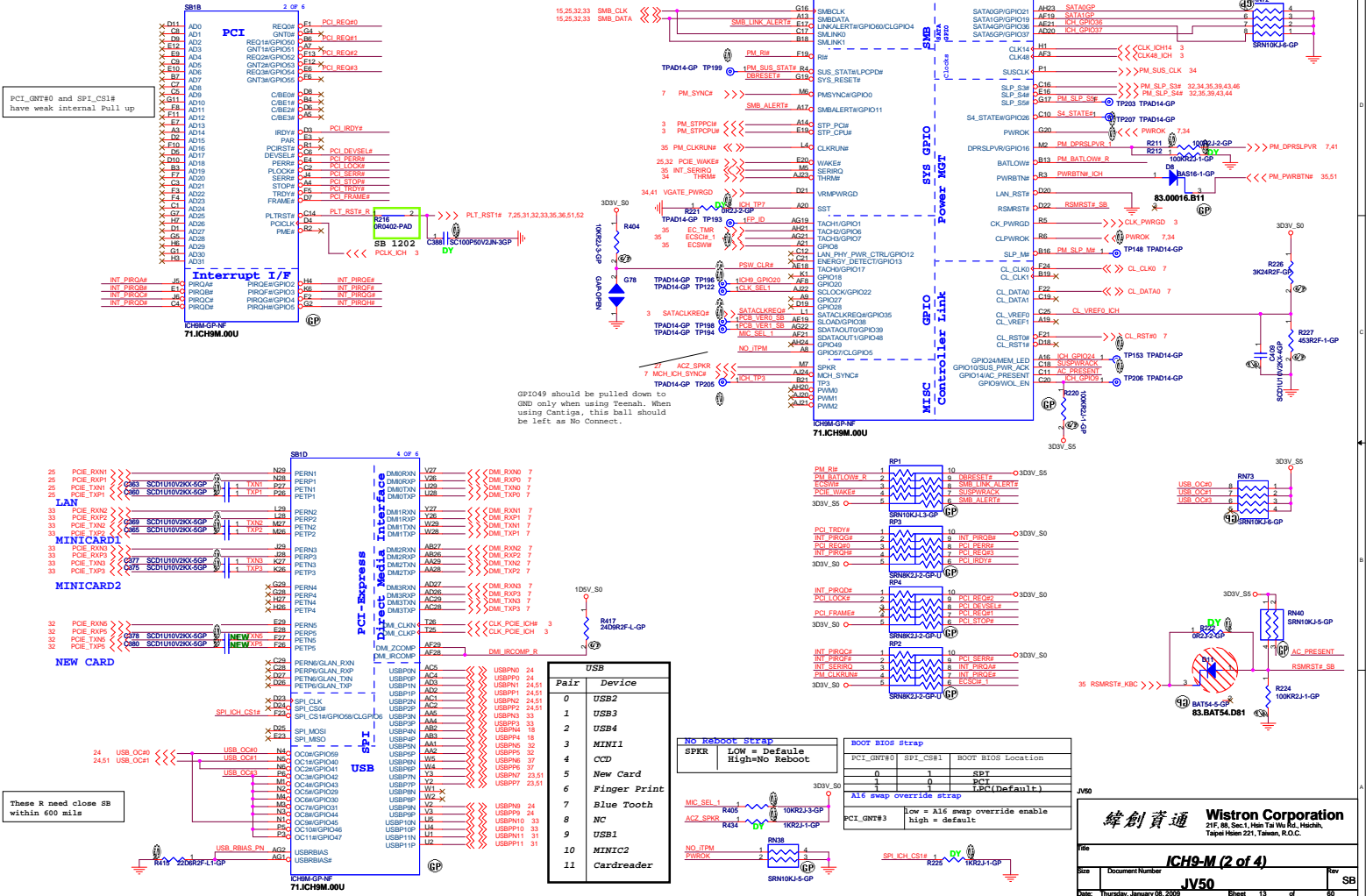
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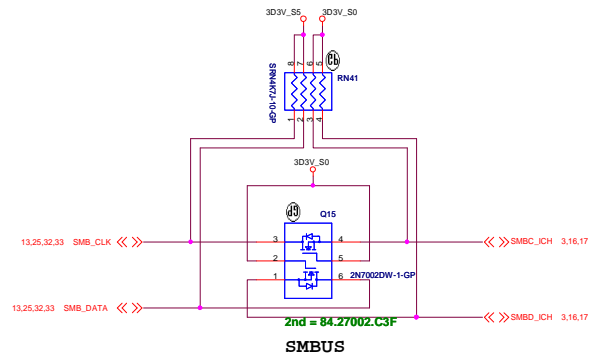
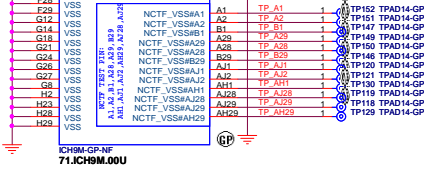
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AA26	VSS	H5
AA27	VSS	J23
AA3	VSS	J26
AA6	VSS	J27
AB1	VSS	AC22
AA23	VSS	K26
AB28	VSS	K29
AB39	VSS	L13
AB4	VSS	L15
AB5	VSS	L2
AC17	VSS	L26
AC26	VSS	L27
AC27	VSS	L6
AC3	VSS	L7
AD1	VSS	M12
AD10	VSS	M13
AD12	VSS	M14
AD13	VSS	M15
AD14	VSS	M16
AD17	VSS	M17
AD18	VSS	M23
AD21	VSS	M28
AD28	VSS	M29
AD29	VSS	N11
AD4	VSS	N12
AD5	VSS	N13
AD6	VSS	N14
AD7	VSS	N15
AE12	VSS	N18
AE13	VSS	N17
AE14	VSS	N18
AE16	VSS	N26
AE17	VSS	N27
AE20	VSS	P14
AE24	VSS	P15
AE3	VSS	P16
AE4	VSS	P17
AE6	VSS	P2
AE9	VSS	P23
AF13	VSS	P28
AF16	VSS	P29
AF18	VSS	P4
AF22	VSS	P7
AH26	VSS	R11
AF26	VSS	R12
AF27	VSS	R13
AF5	VSS	R14
AE7	VSS	R15
AE9	VSS	R16
AG13	VSS	R17
AG16	VSS	R18
AG18	VSS	R26
AG20	VSS	T12
AG23	VSS	T13
AG3	VSS	T14
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AH12	VSS	T17
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AH17	VSS	B26
AH19	VSS	U12
AH2	VSS	U13
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AH25	VSS	U15
AH28	VSS	U16
AH5	VSS	AD23
AH8	VSS	U26
AJ12	VSS	U27
AJ14	VSS	U3
AJ17	VSS	U3
A8	VSS	V1
B11	VSS	V13
B14	VSS	V15
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B2	VSS	V26
B20	VSS	V28
B23	VSS	V4
B5	VSS	V5
B8	VSS	W26
C26	VSS	W27
C27	VSS	W3
E11	VSS	Y1
E14	VSS	Y26
E18	VSS	Y29
E4	VSS	Y4
E41	VSS	Y5
E24	VSS	AG28
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E8	VSS	AF2
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G14	VSS	
G18	VSS	
G21	VSS	
G24	VSS	
G26	VSS	
G27	VSS	
G8	VSS	
H2	VSS	
H23	VSS	
H26	VSS	
H29	VSS	



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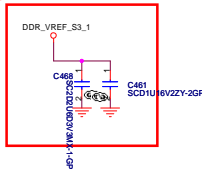
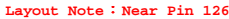
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Size Document Number JV50


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Rev SB

## DDR3 SOCKET\_1



High 9.2mm


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Size	Rev
Document Number	SB
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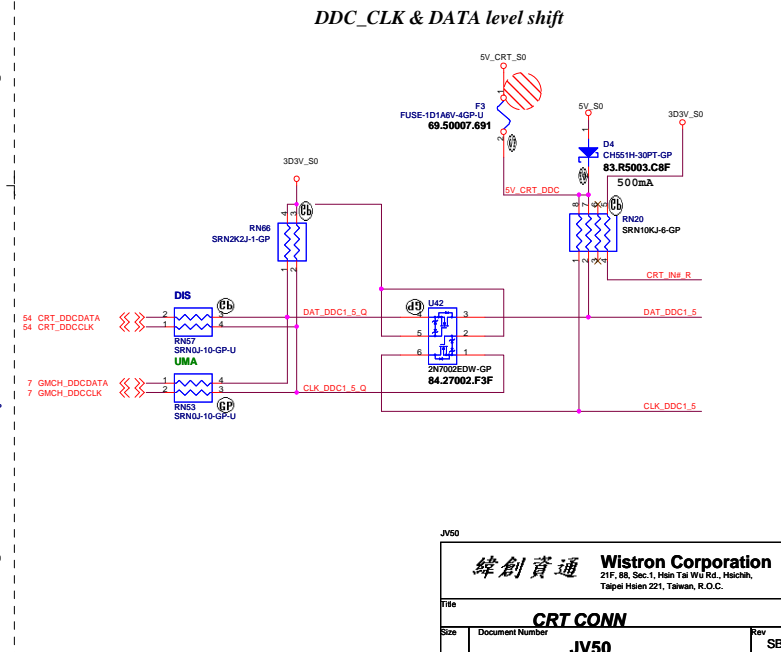
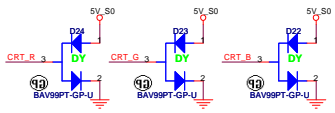


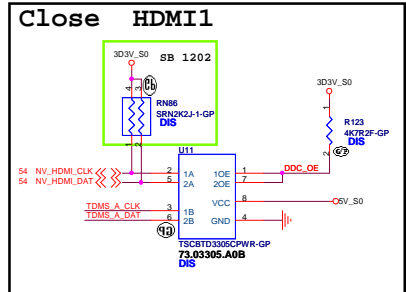
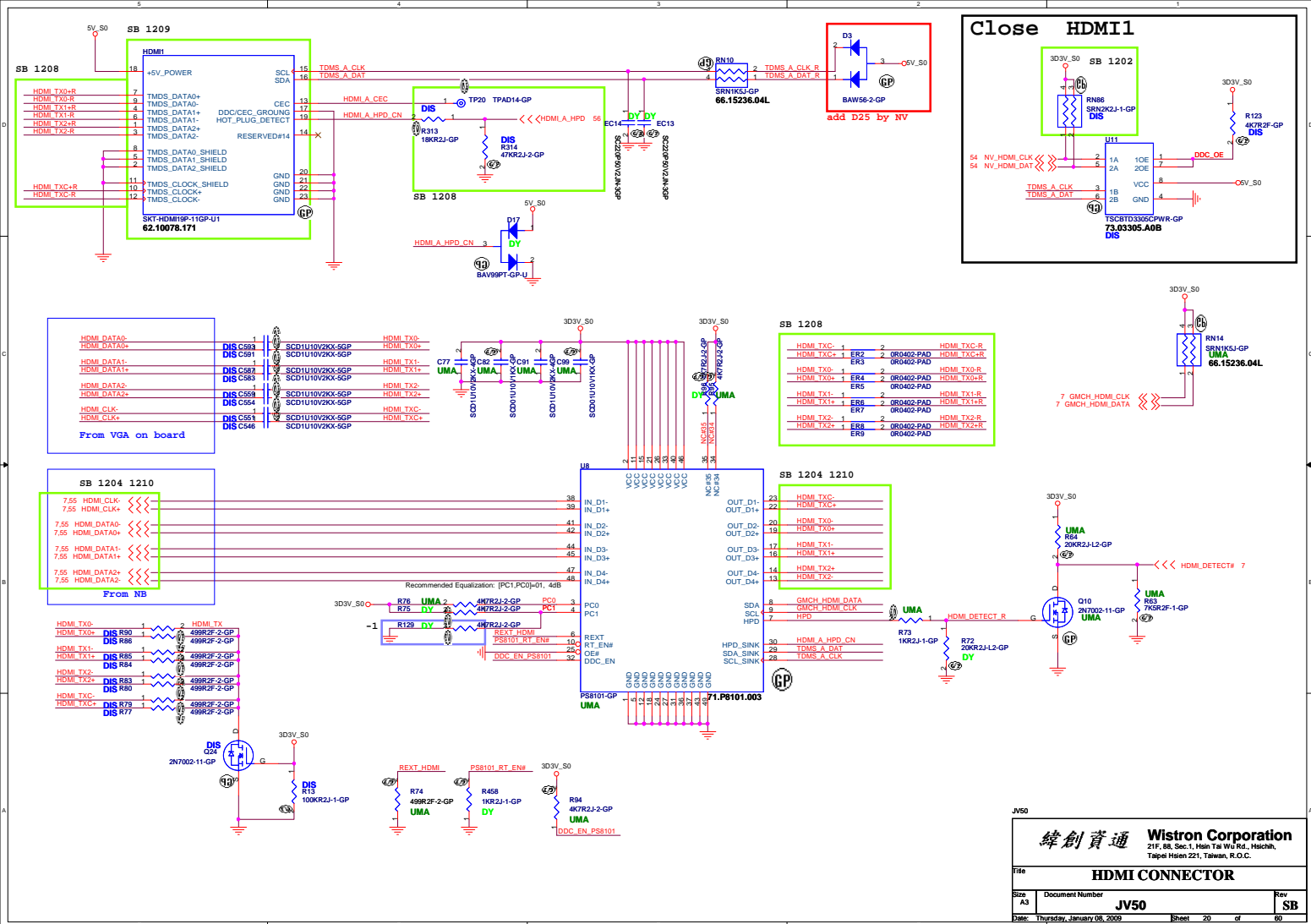
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Size	Document Number		Rev SB
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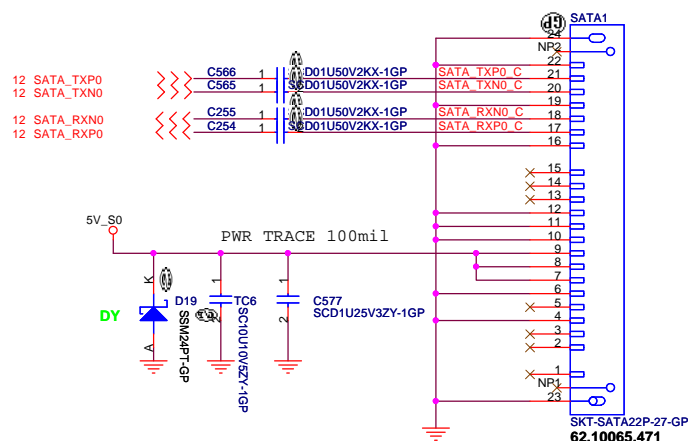
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Size: A3 Document Number: **JV50** Rev: **SB**

Date: Thursday, January 06, 2009 Sheet: 20 of 60

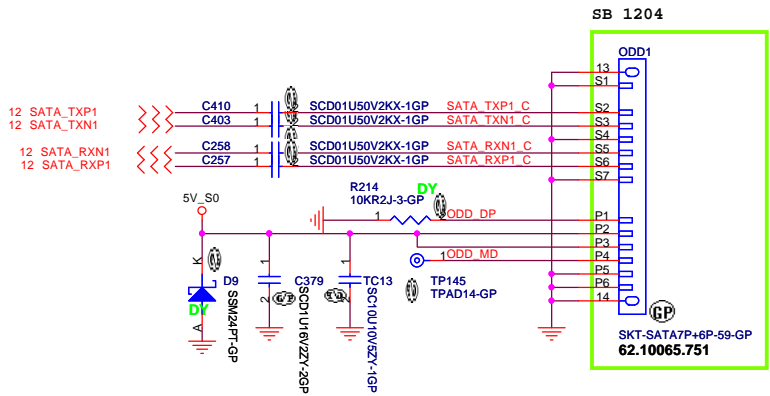
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JV50

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Size	Document Number		Rev
	JV50		SB
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# ODD Connector



JV50

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Title			
<b>ODD</b>			
Size	Document Number	Rev	SB
<b>JV50</b>			
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3D3V\_BT\_S0

3D3V\_BT\_S0

EC59 **DY**  
SCD1U16V2Z2-GP

U65  
OUT GND NC#3  
IN EN  
G5240B1T1U-GP

3D3V\_S0

C862  
SC4D7U10V5ZY-3GP

BLUETOOTH\_EN 35

EC20 put near  
BLUE1 / all  
USB put one  
choke near  
connector by  
EMI request

BT1

USBPN7 13.51  
USBPP7 13.51

3D3V\_BT\_S0

ACES-CON4-1-GP-U2  
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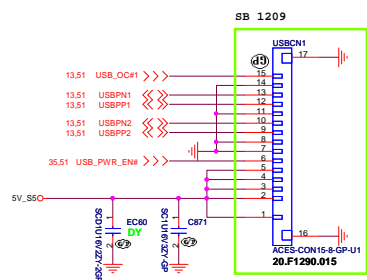
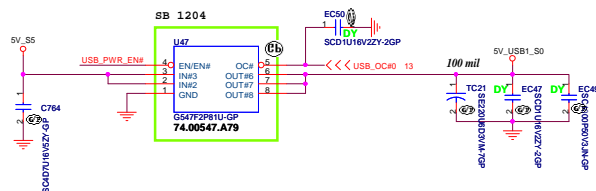
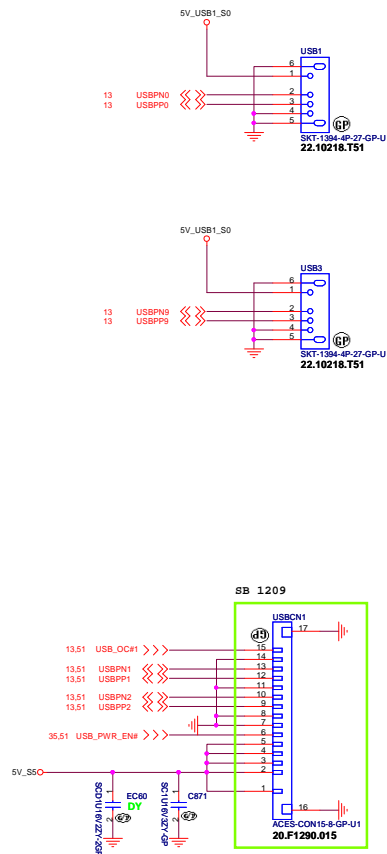
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
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## **BLUETOOTH**

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JV50		緯創資通 Wistron Corporation	
Title		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
Size		USB CONN	
Date: Thursday, January 08, 2009		Rev	
Sheet		24 of 60	

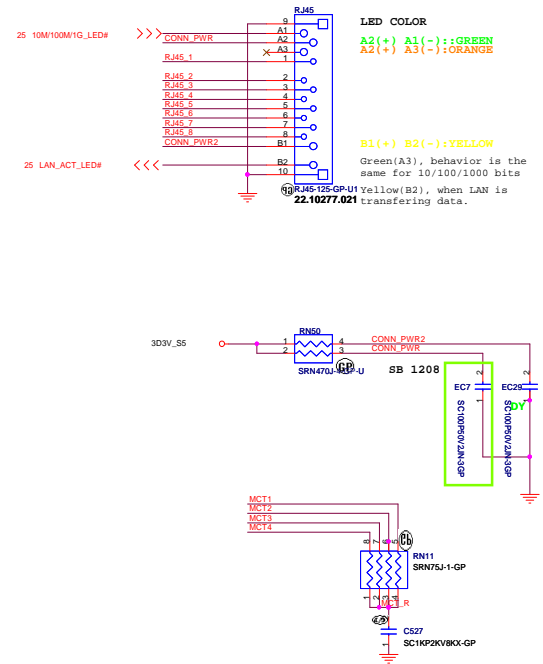
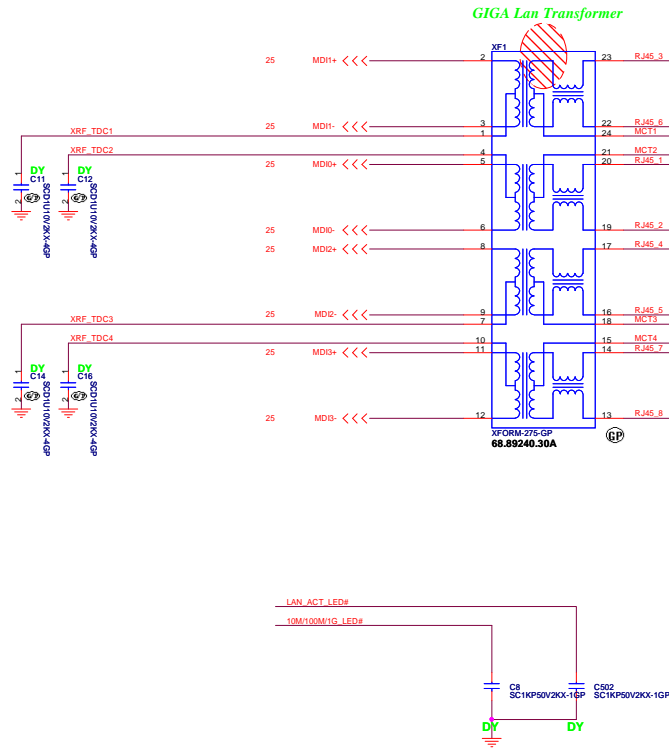




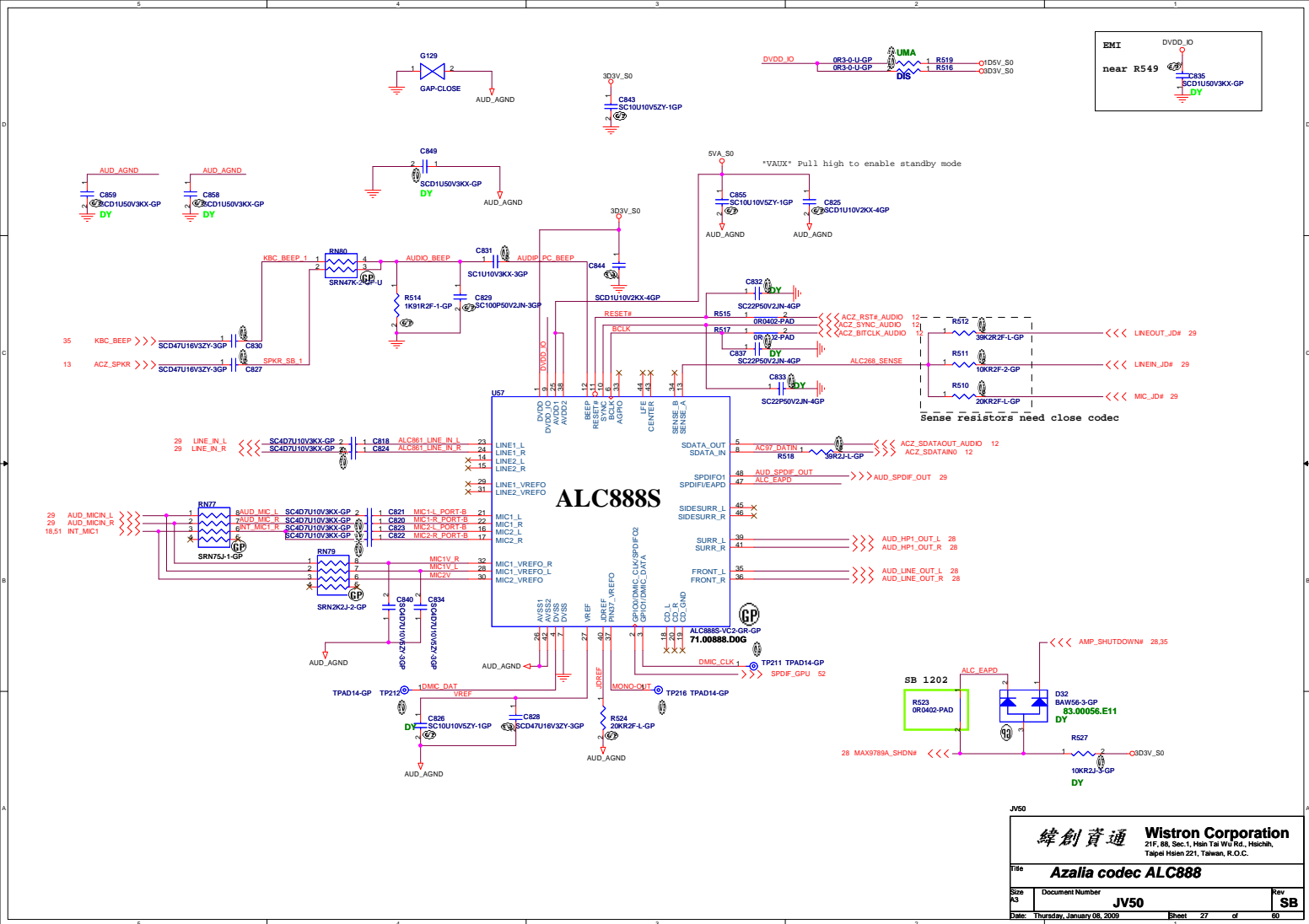
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.30mil between pairs and any other trace.
- 7.Must not cross ground most,except RJ-45 moat.

## LAN Connector

## LAN Connector

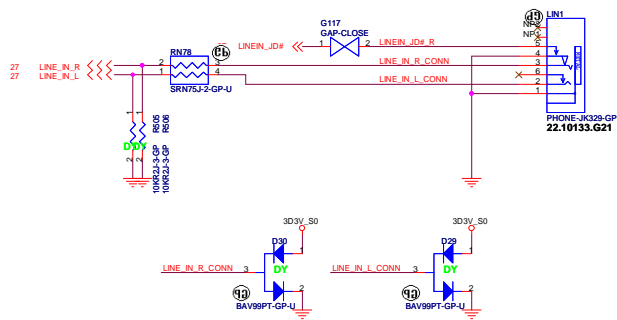


JV50		緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File		LAN CONN	
Size	Document Number	Rev	
A3	JV50	SB	
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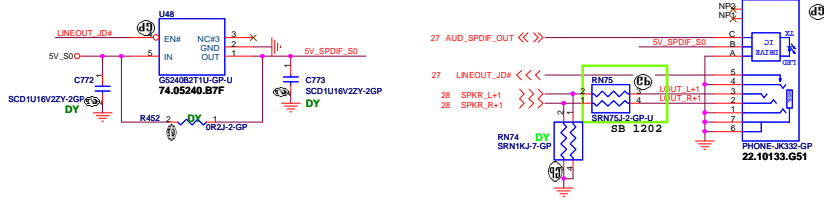




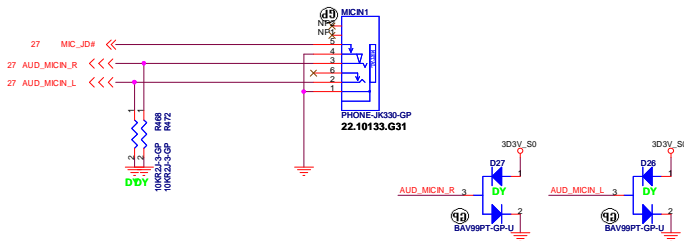
## LINE IN



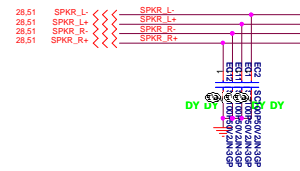
## LINE OUT



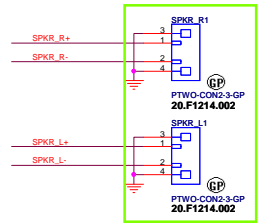
## MIC IN



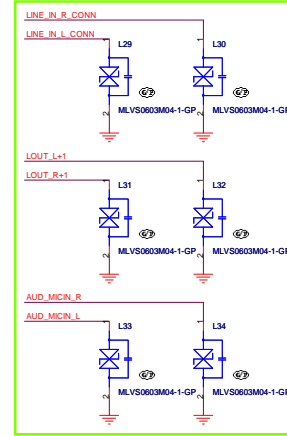
## Internal Speaker



SB 1202



SB 1202

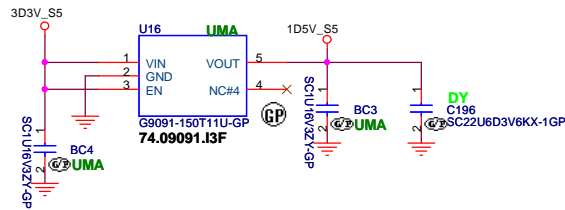
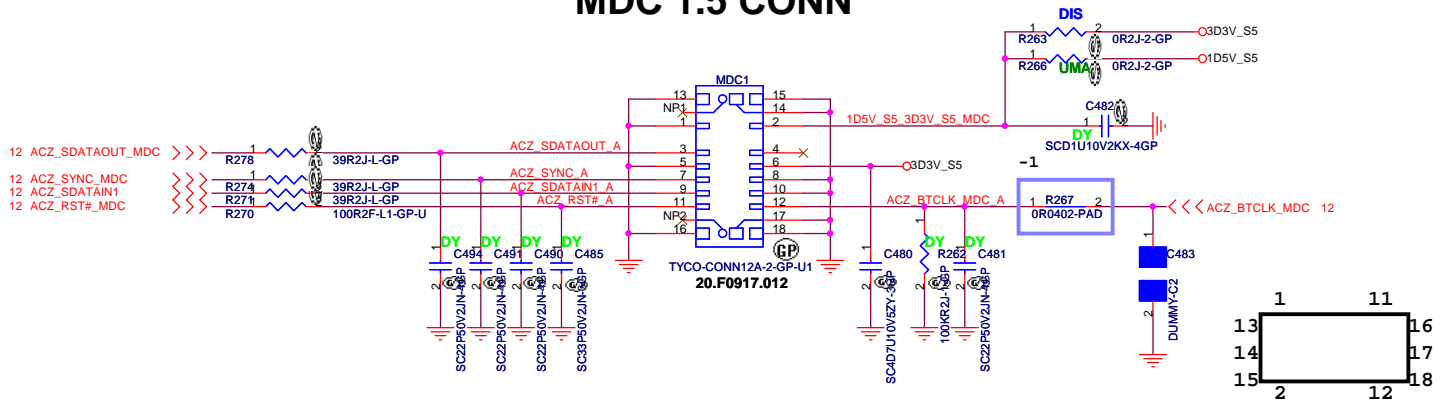


JV50

緯創資通 Wistron Corporation  
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

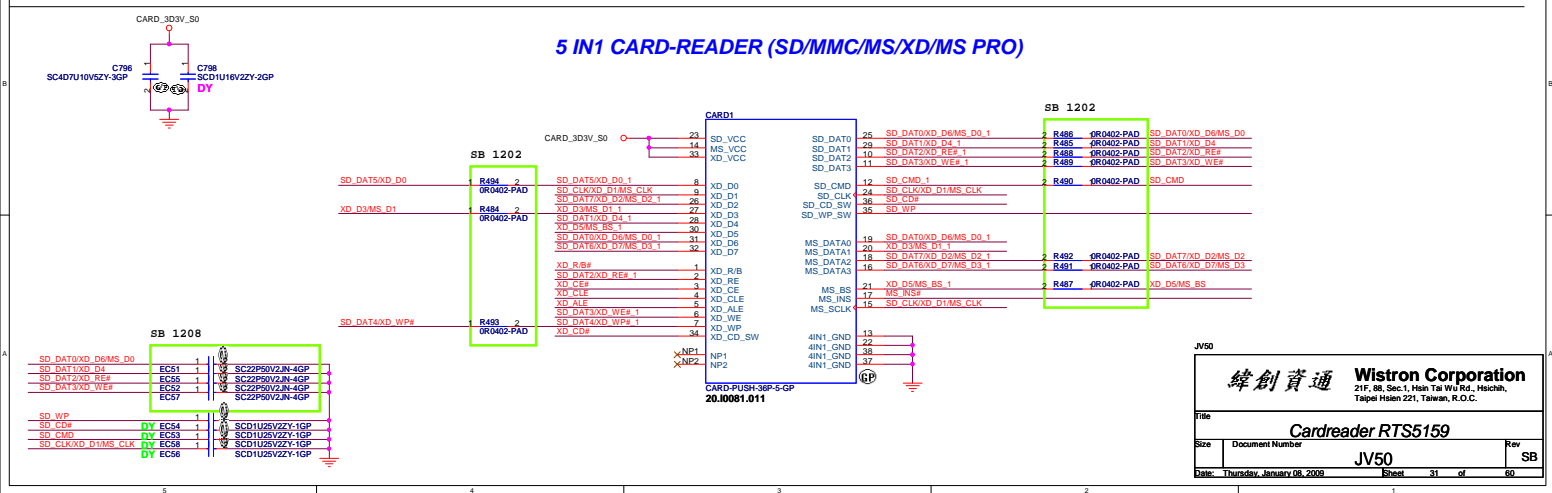
Title			
AUDIO jack			
Size	Document Number		Rev
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Date: Thursdav, January 08, 2009		Sheet 29 of	60

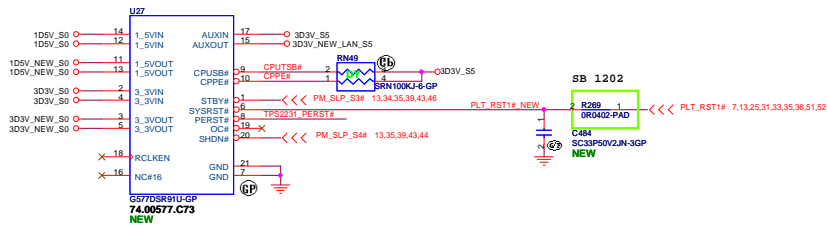
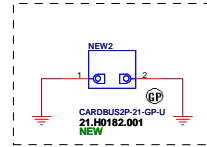
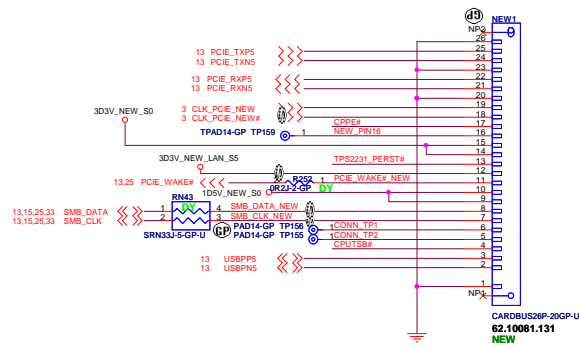
# MDC 1.5 CONN



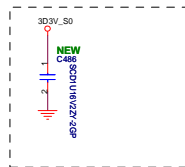
JV50

<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>MDC</b>			
Size	Document Number		Rev
	<b>JV50</b>		<b>SB</b>
Date:	Thursday, January 08, 2009	Sheet 30 of 60	

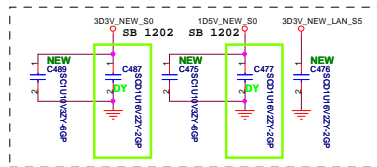




Place them Near to Chip



Place them Near to Connector

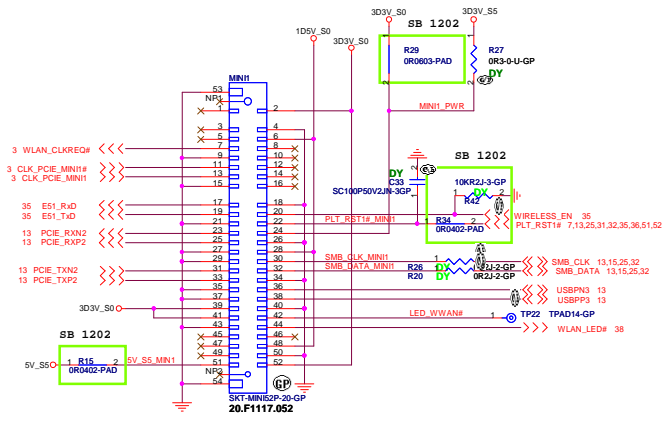
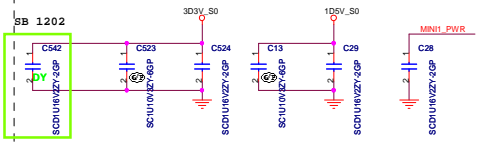


JV50

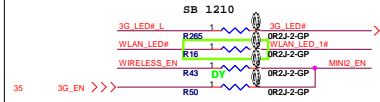
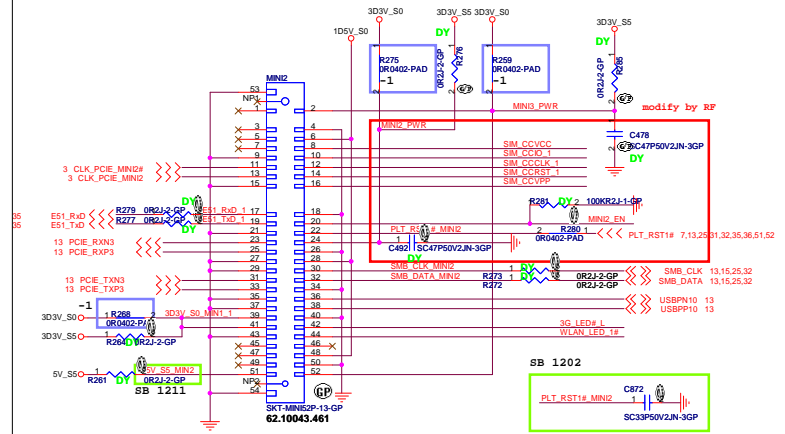
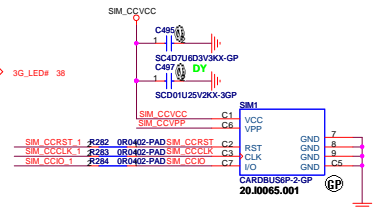
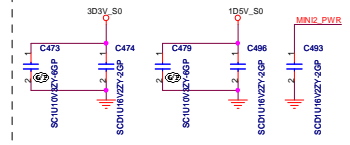
<b>緯創資通</b>		<b>Wistron Corporation</b>	
217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.			
<b>NEW CARD</b>		<b>JV50</b>	
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### *Mini Card Connector(WLAN) Support debug-card*

Place near MINI1  
.....

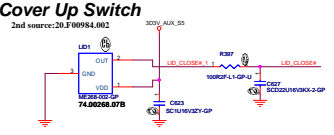
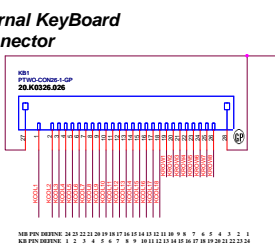
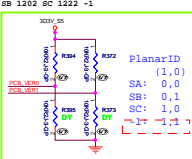
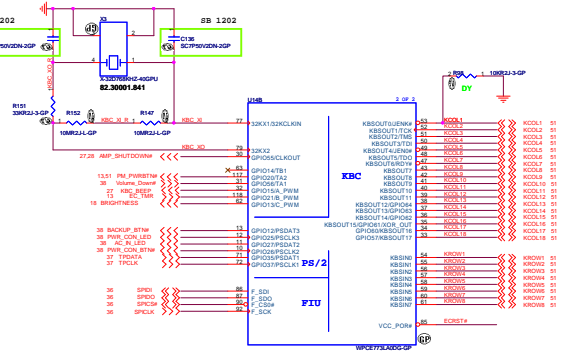
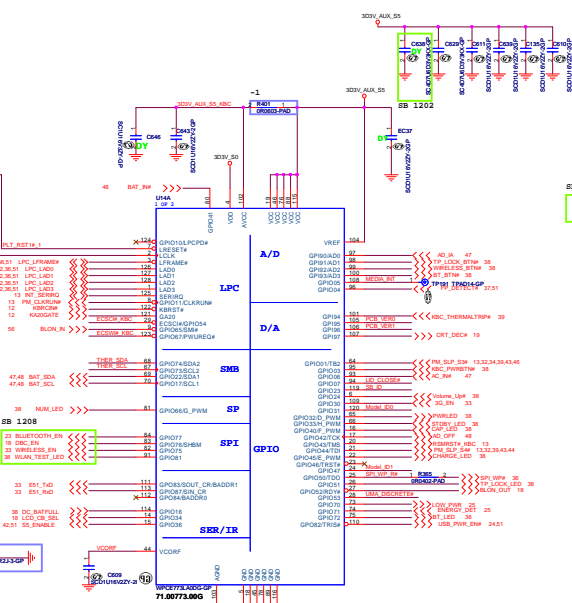
### ***Mini Card Connector(Robson2 and 3G)***

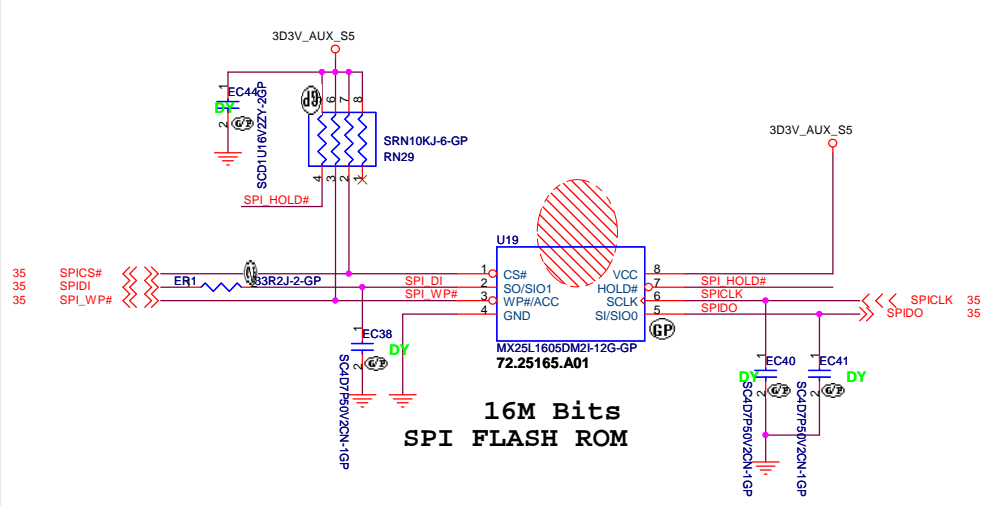
Place near MINIC2  
.....

JV50

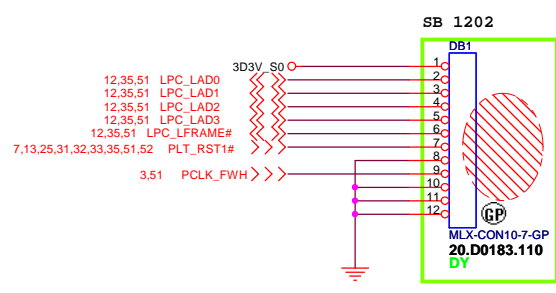
 <b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>MINI CARD</b>			
Size A3	Document Number	Rev	
<b>JV50</b>		<b>SB</b>	
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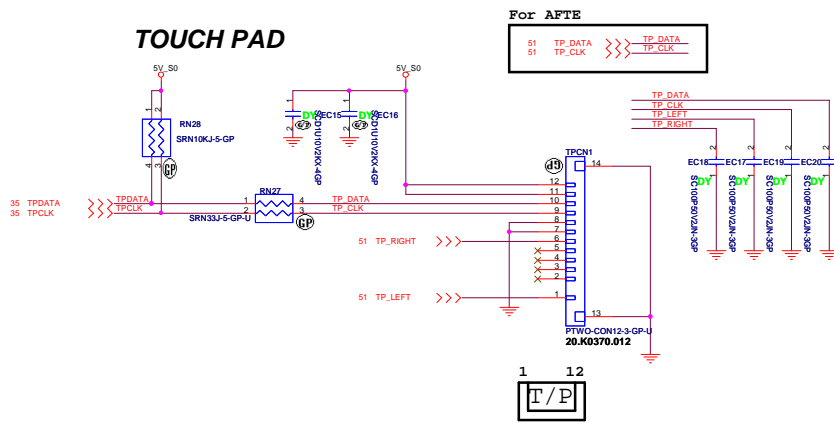
GOLDEN FINGER FOR DEBUG BOARD



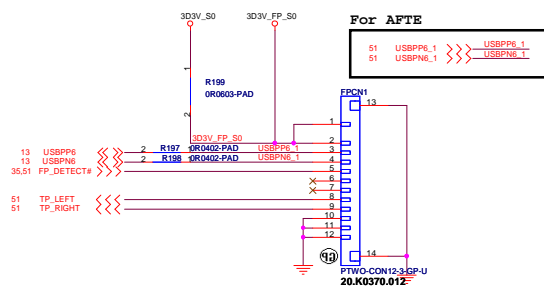
JV50

Title		BIOS	
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JV50			
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## TOUCH PAD



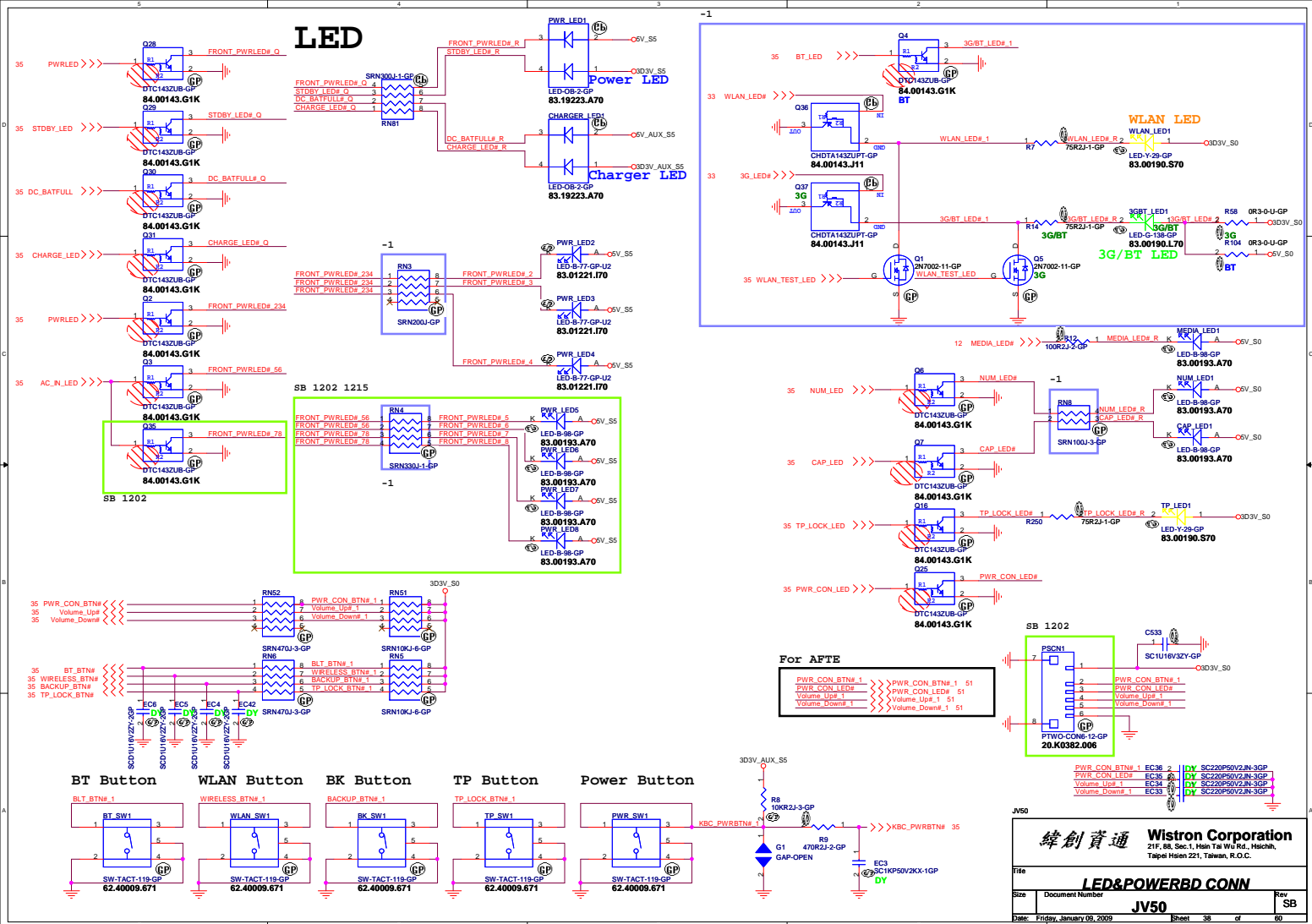
## Finger printer



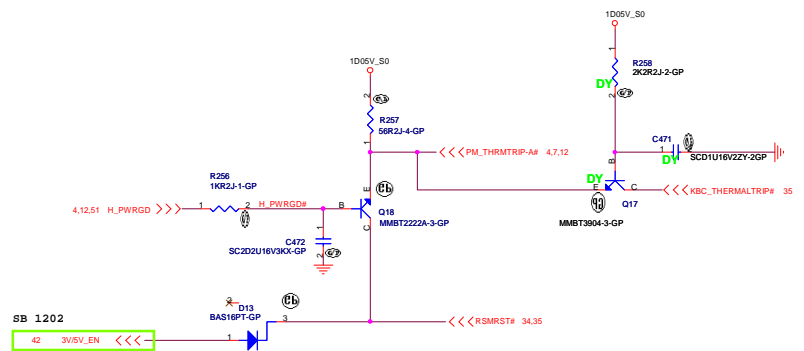
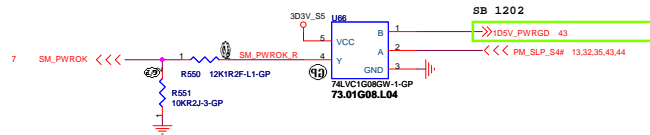
JV50

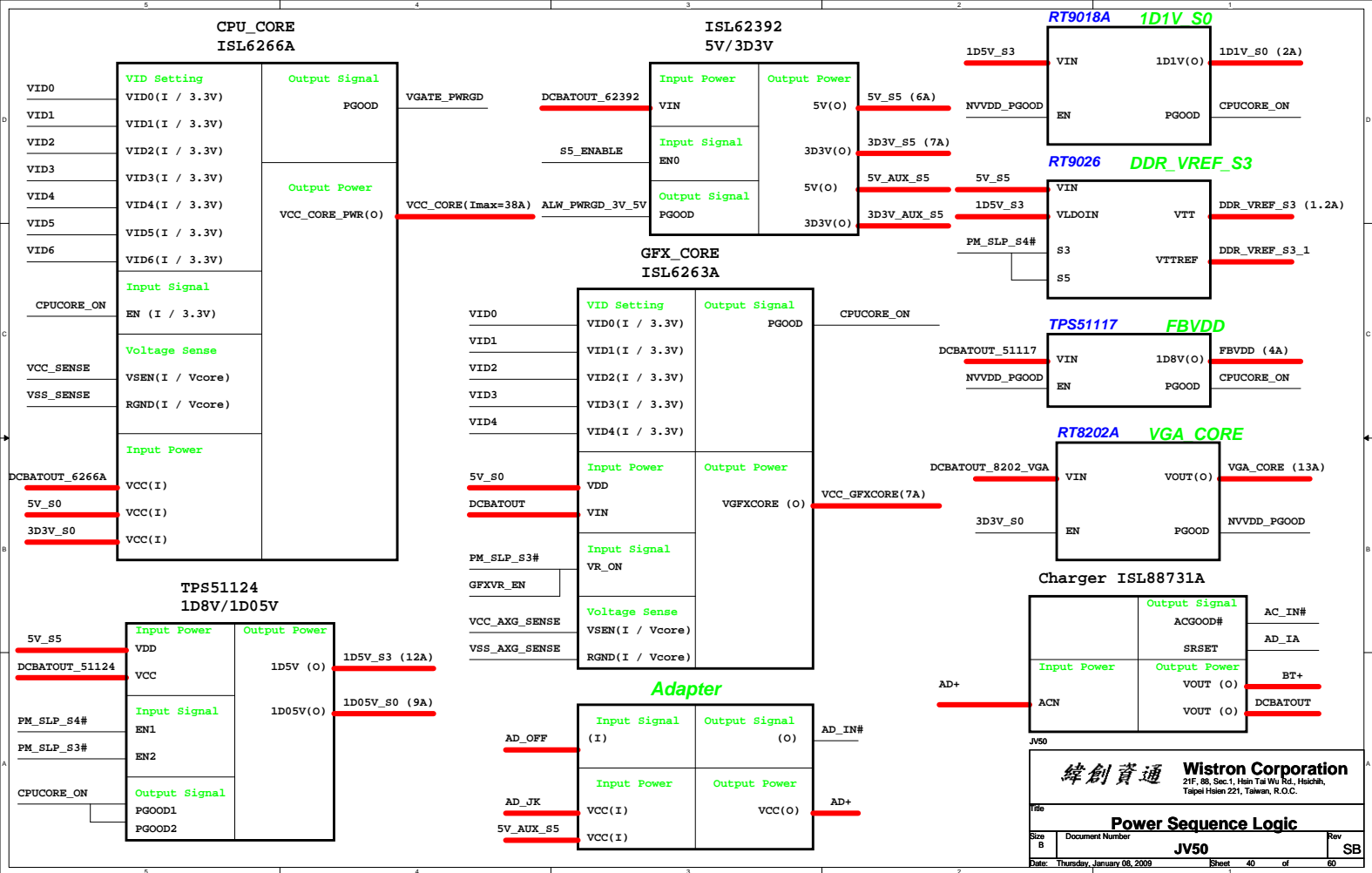
緯創資通 Wistron Corporation  
21F, 8th, Sec.1, Hsin-Tai Wu Rd., Hsinchu,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Touch PAD and FP		
Size	Document Number	Rev
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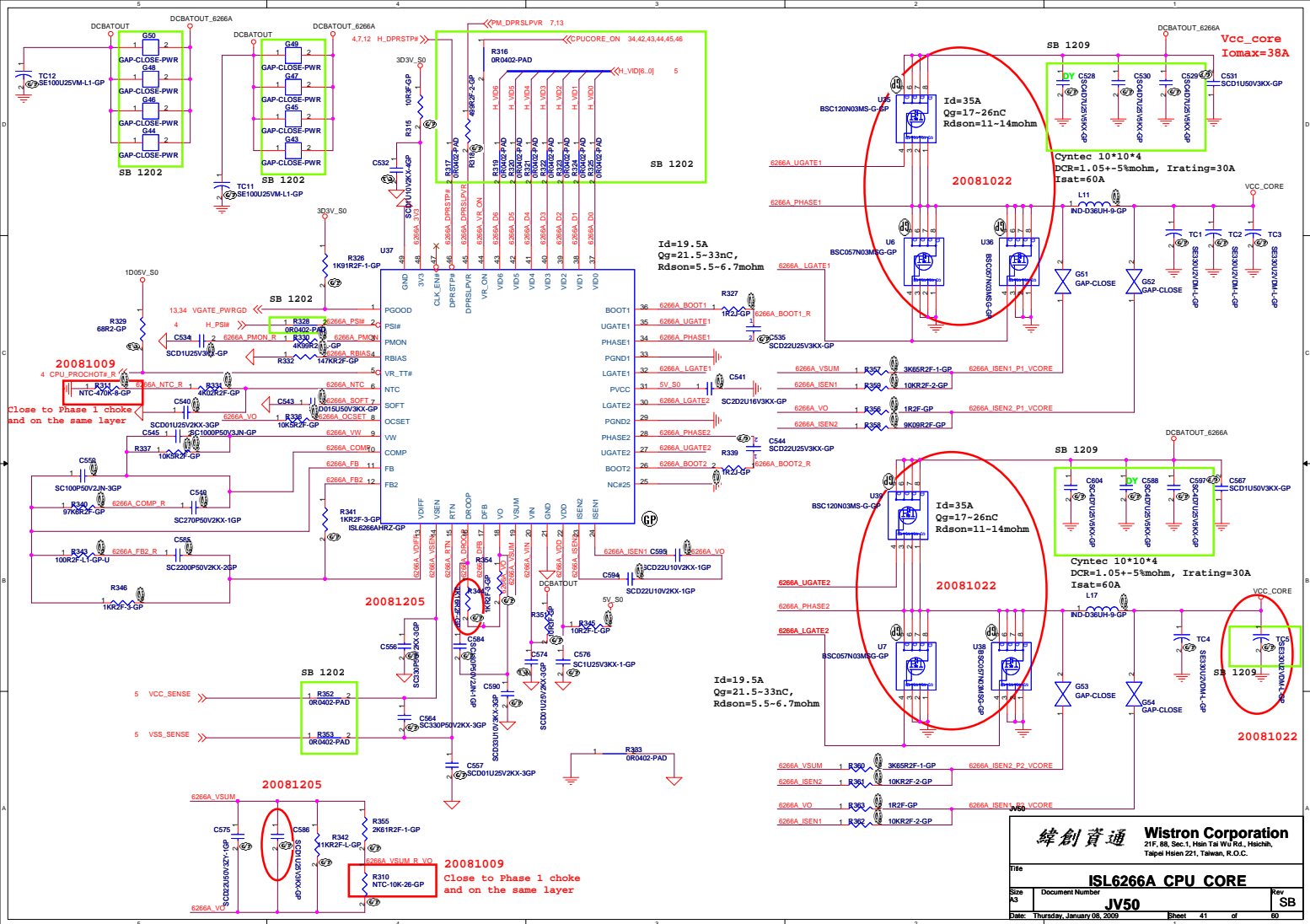


## 3D3V\_AUX\_S5

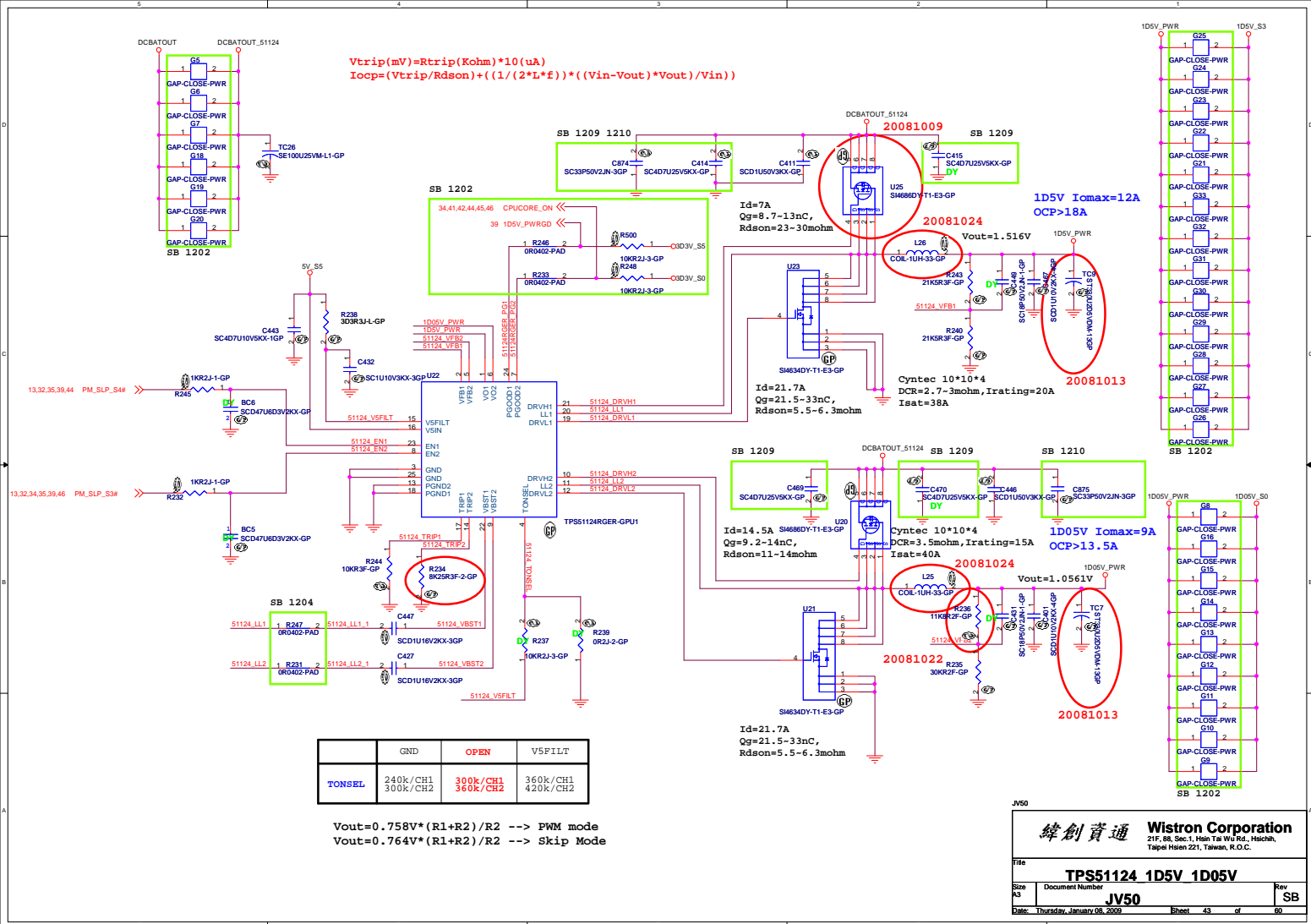


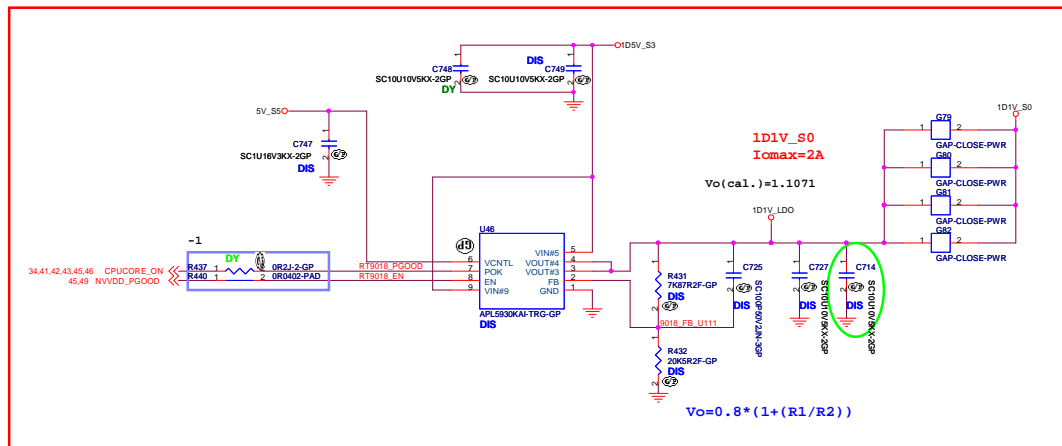
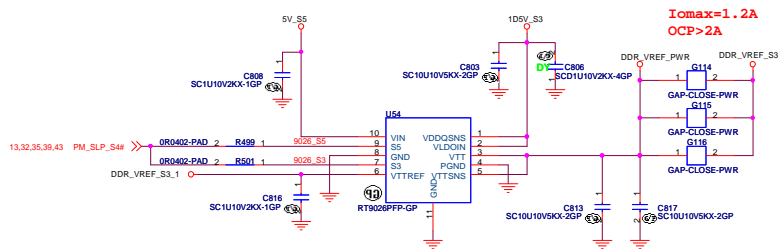










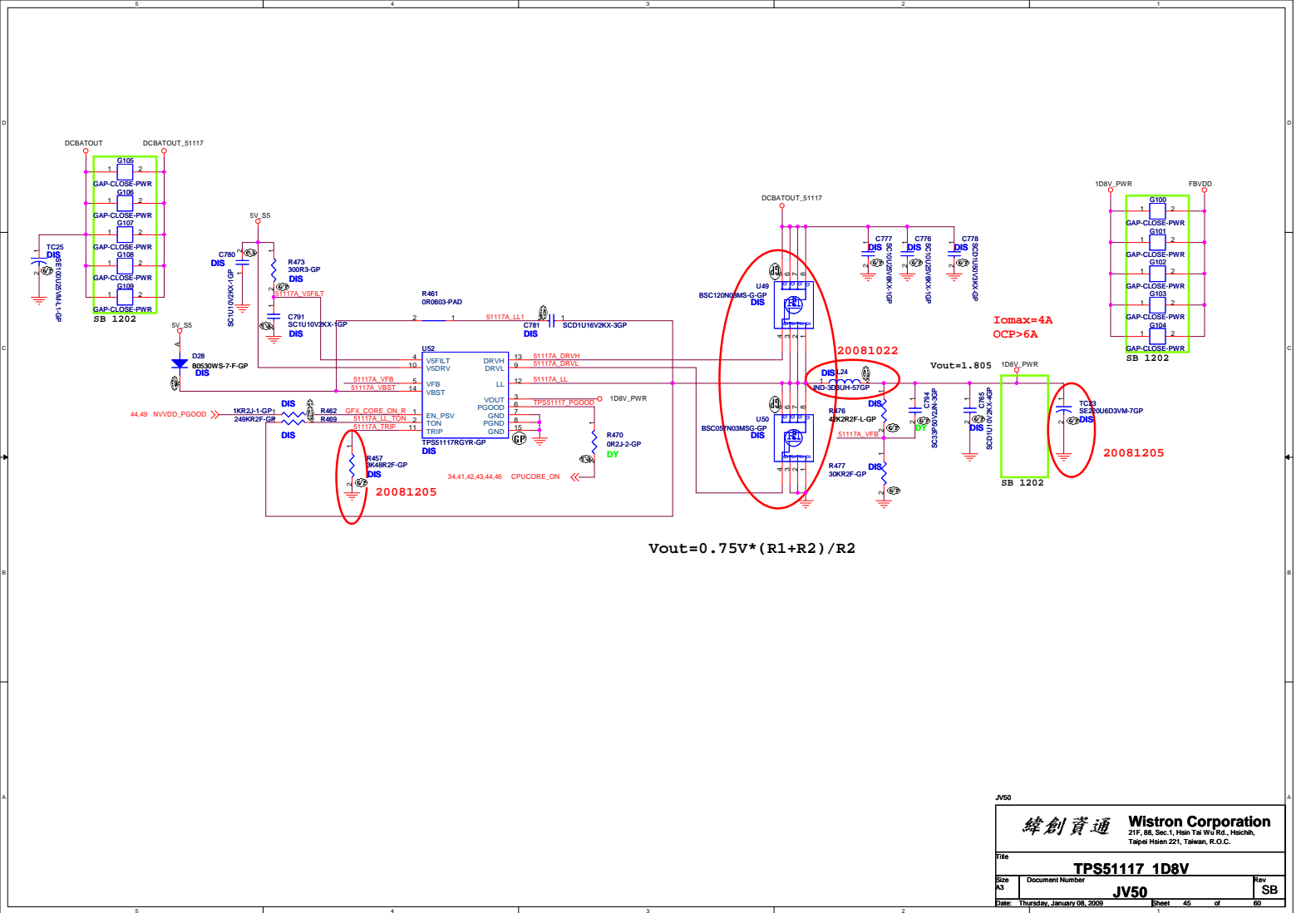


20090106

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緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

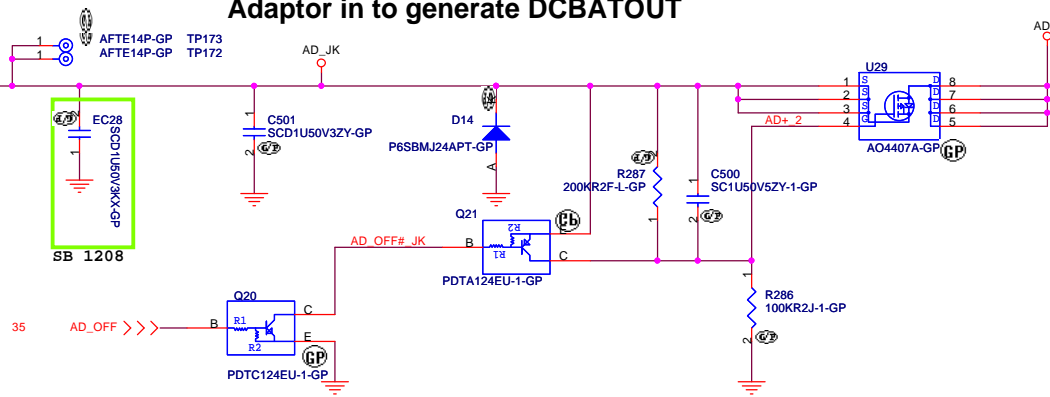
File	0D75V/1D1V
Size	Document Number
A3	JV50
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Rev	SB



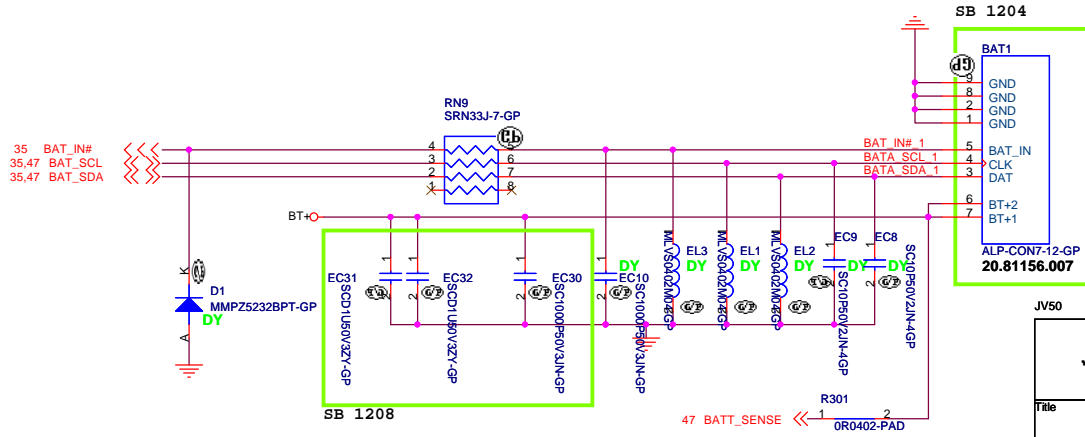




## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



For AFTE

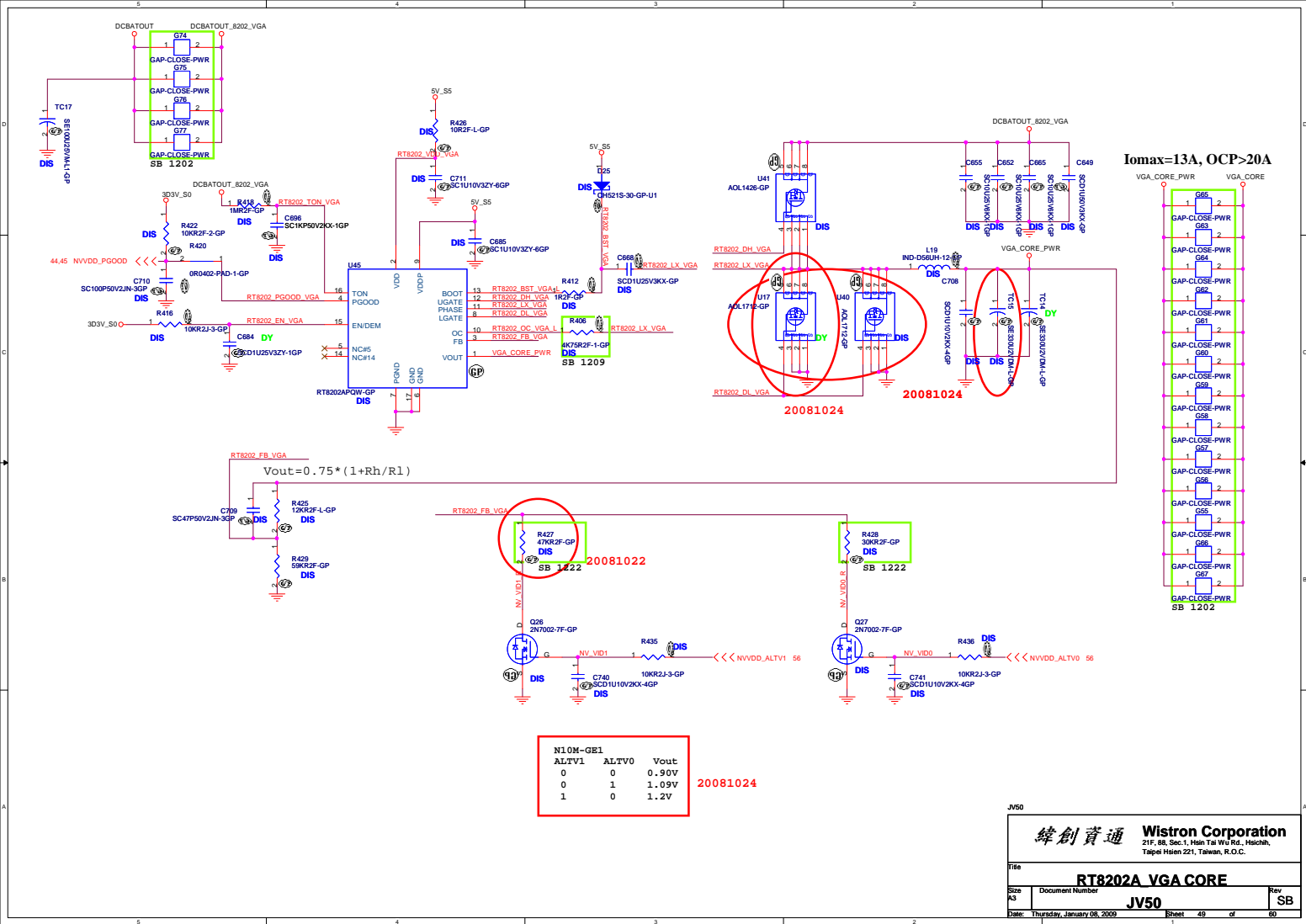
51 BATA\_SDA\_1 >>> BATA\_SDA\_1  
51 BATA\_SCL\_1 >>> BATA\_SCL\_1  
51 BAT\_IN#\_1 >>> BAT\_IN#\_1

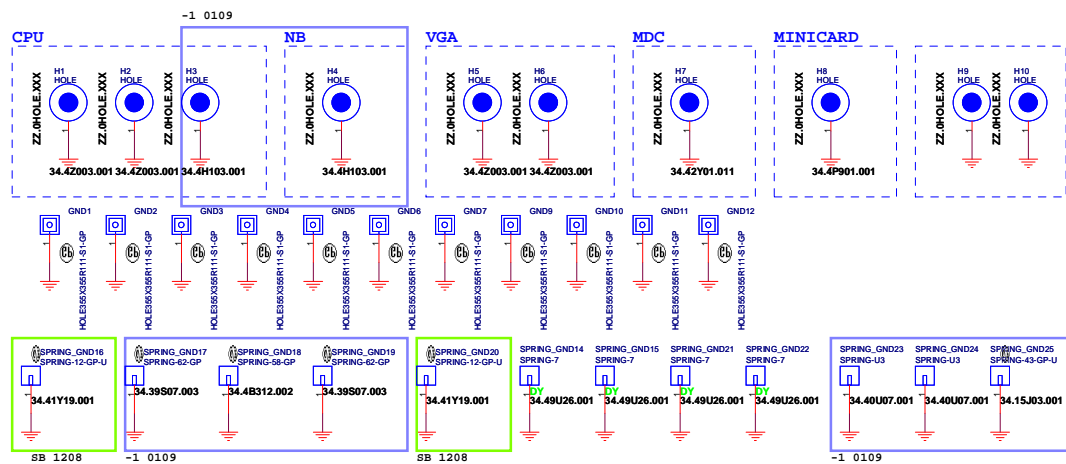
緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
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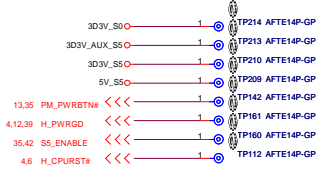


JV50

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>EMI/Spring/Boss</b>			
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## Check test point



Test Point放在Dimm Door打開可量測處

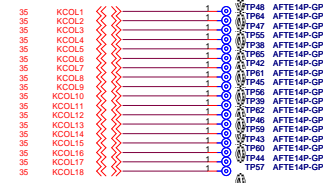
## SPKR\_L1 Conn. Test Point keep on connector side



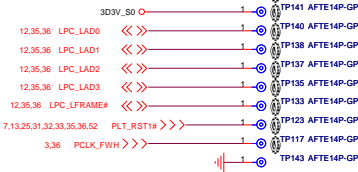
## FAN1 Conn. Test Point keep on connector side



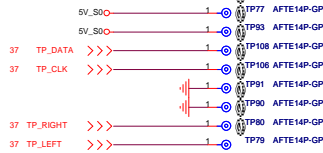
## KB1 Conn. Test Point keep on connector side



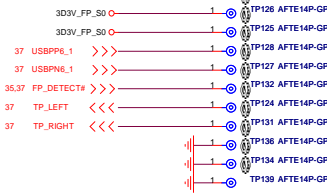
## DB1 Conn. Test Point keep on connector side



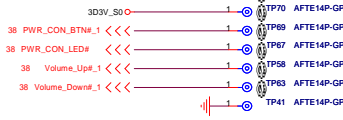
## TPCN1 Conn. Test Point keep on connector side



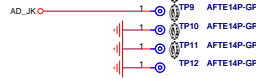
## FPCN1 Conn. Test Point keep on connector side



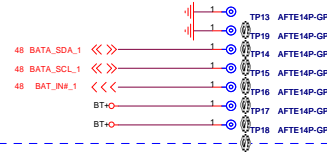
## PSCN1 Conn. Test Point keep on connector side



## DCIN1 Conn. Test Point keep on connector side



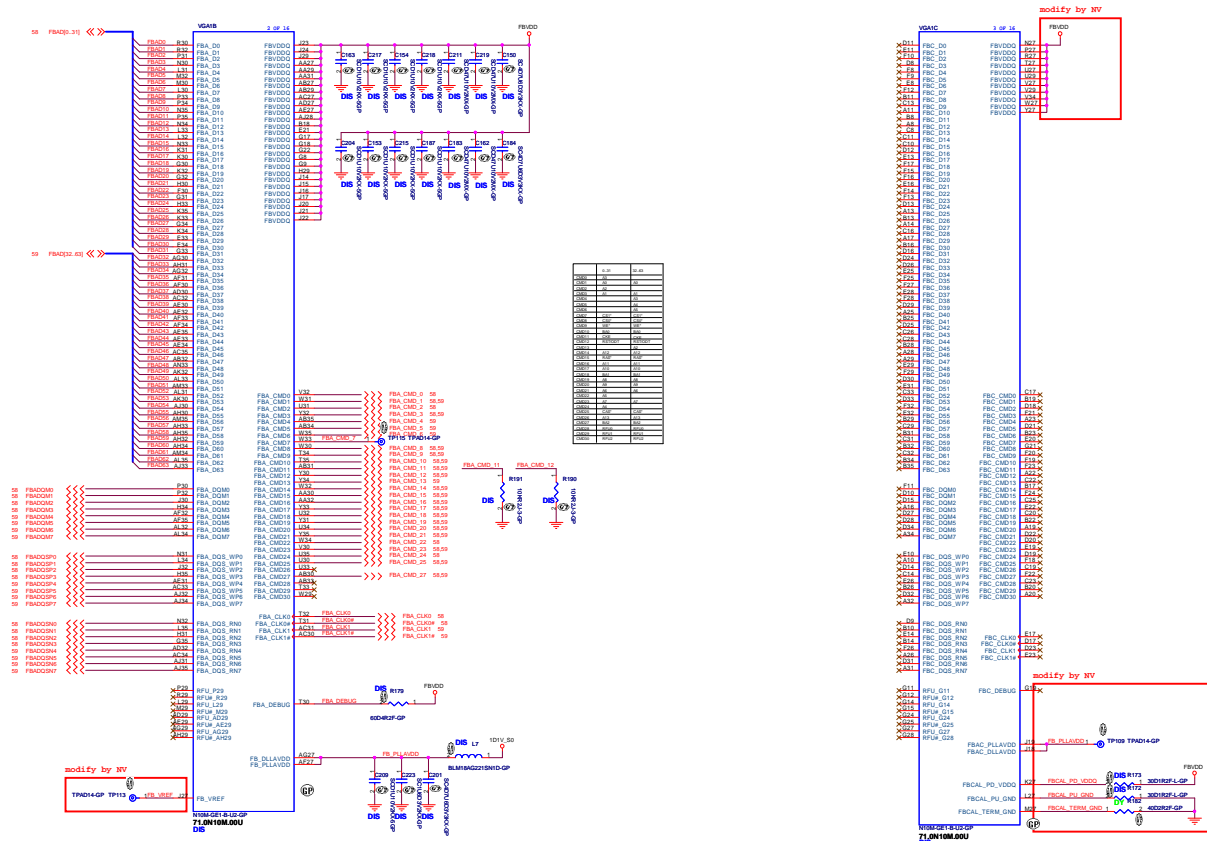
## TPCN1 Conn. Test Point keep on connector side

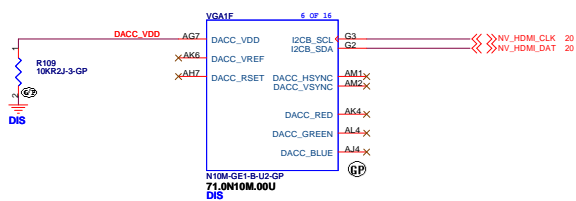
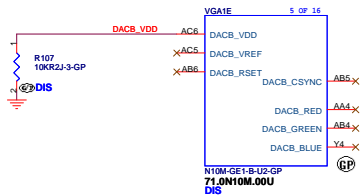
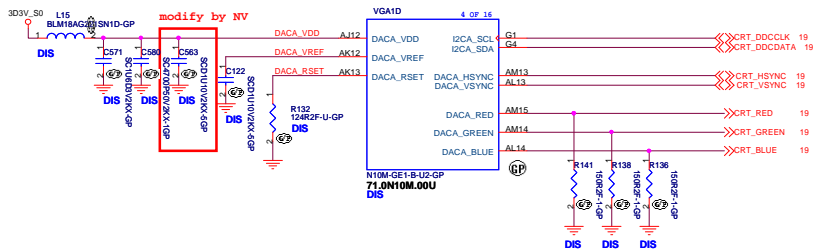


JV50

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
AFTE TP			
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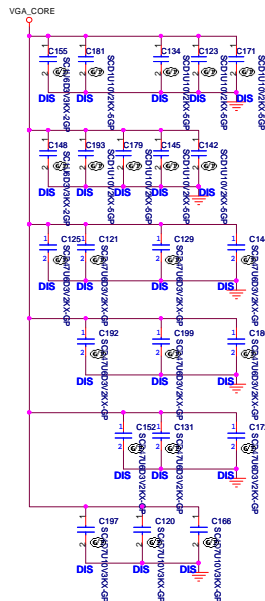
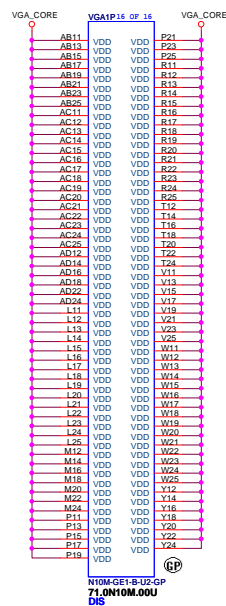
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipei Hsien 221, Taiwan, R.O.C.

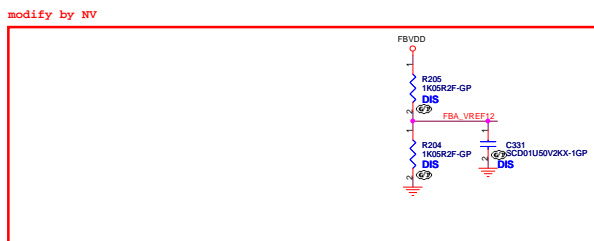
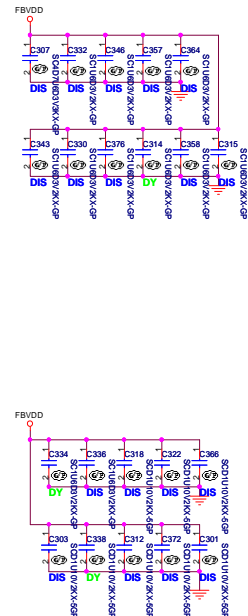
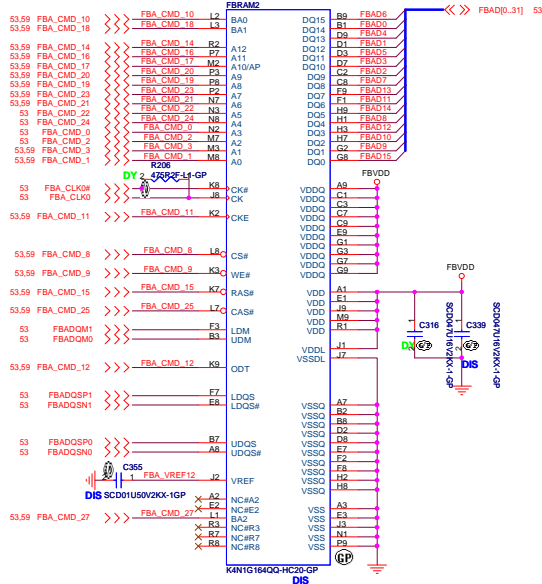
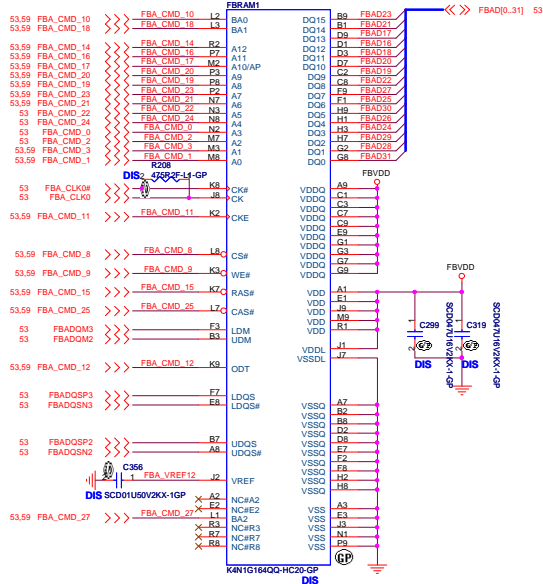
Title		N10M(3/6) DAC	
Size	A3	Document Number	Rev
JV50		SB	
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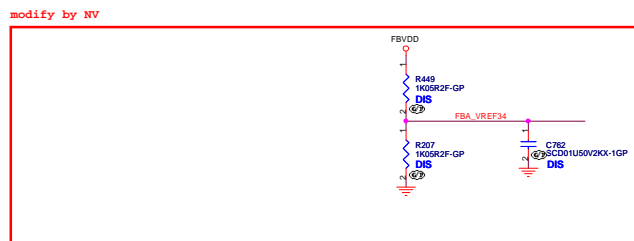
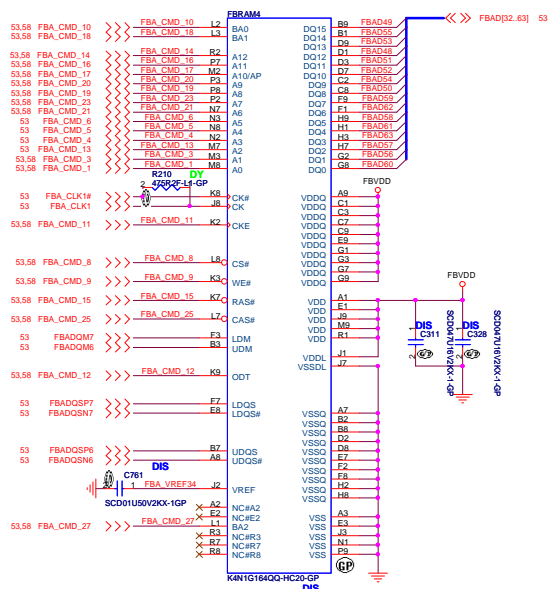






JV50

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsin 221, Taiwan, R.O.C.	
Title VRAM(1/2)	
Size A3	Document Number
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JV50		<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>VRAM(2/2)</b>			
Size A3	Document Number		Rev SB
Date: Thursday, January 08, 2009		Sheet 69 of 50	<b>JV50</b>

JW50		<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>HISTORY</b>			
Doc #2	Document Number		Rev <b>S8</b>
<b>JV50</b>			
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SB SB SC -1  
12/22  
Page49: change R427 from 30K 47K and R428 from 47K to 30K  
  
SC  
12/22  
Page42: modify by power team's request  
Page35: change R372 R395 from DY to mount and change R373 R394 from mount to DY  
  
-1  
01/06  
Page17: change C400 from mount to DY and change C399 from DY to mount  
Page30: change R267 from 39R to 0ohm pad  
Page38: delete RN7 and add Q36 Q37  
Page25: change U3 pin 38 52 from LAN\_AVDD to TP and change U3 pin 68 from NC to TP  
Page25: delete R58 and add RN87 and change U5 to 72.24C02.R01  
Page3: change R255 from 22R to 33R and change RN42 from 0ohm to 33R  
Page33: change R268 R275 R259 from 0ohm resistor to 0ohm pad  
Page35: change R394 from DY to mount and change R395 from mount to DY  
Page28: change R526 from 0ohm resistor to 0ohm pad  
Page35: change R401 from 0ohm resistor to 0ohm pad  
Page35: delete Q12 and add R502 R503  
Page35: change RN23 pin 5 6 from 3D3V\_AUX\_S5 to 3D3V\_S0  
Page44: change U46 to APL5930 by power team's request  
Page38: add 3G and BT option  
Page28: change R479 from 8K2 to 10K and change R480 from 6K2 to 4K99 for audio speaker gain  
Page28: merge C0D1 to LCD1  
  
01/07  
Page44: change R437 from 0ohm pad to 0ohm resistor  
Page9: change TC18 from UMA to DY and change C276 from DY to mount  
Page35: delete RN21 and add R507 10K DY  
Page38: change RN4 to 330R and change RN8 to 100R and delete R10 and change RN3 to 8P4R 200R  
Page47: change C515 to 78.15322.2FL by power team's request  
Page3: mount 33p on EC23 EC24 EC25 EC39 EC48 for RF's request  
Page3: add EC68 EC69 33p DY by RF's request  
Page20: add R129 4K7 for different vendor  
  
01/08  
Page42: change R541 from 200K to 100K and change R544 location  
Page42: change R532 R545 from 0ohm pad to 0ohm resistor  
  
01/09  
Page38: change name from 3G/ST\_LED1 to 3GBT\_LED1  
Page50: add SPRING\_GND23 34.40U07.001, SPRING\_GND24 34.40U07.001, SPRING\_GND25 34.15J03.001  
Page50: SPRING\_GND17, SPRING\_GND19 change from 34.41Y19.001 to 34.39S07.003  
Page50: SPRING\_GND18 change from 34.41Y19.001 to 34.4B312.002