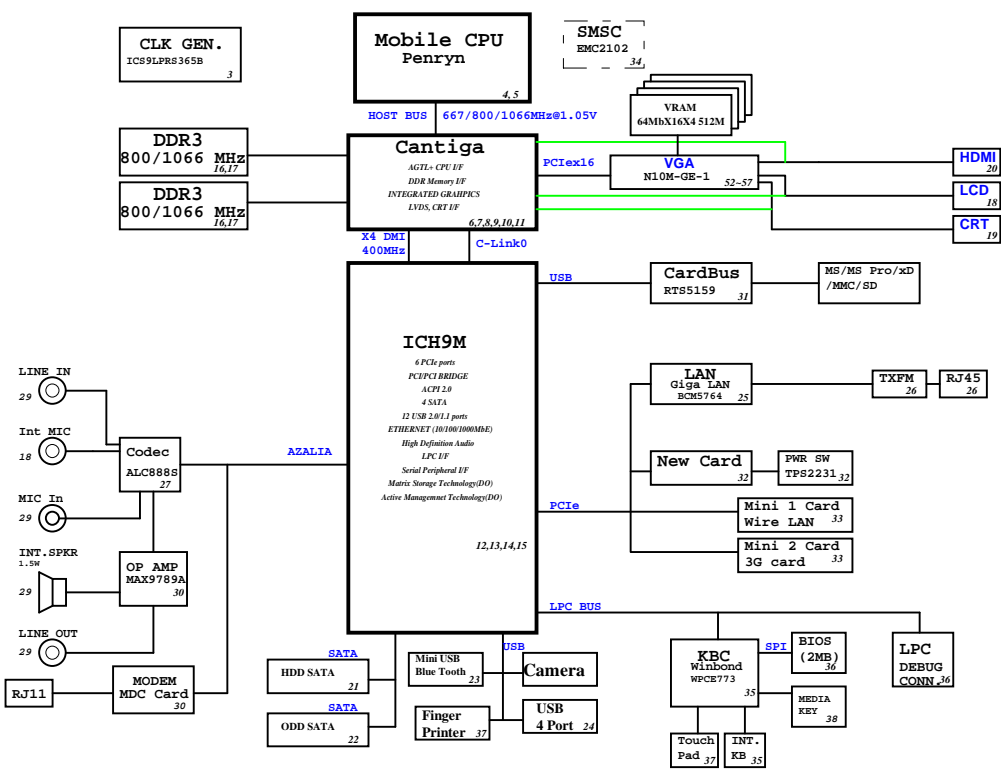


JV50 Block Diagram

Project code: 91.4CG01.001
PCB P/N : 48.4CG01.0SA
REVISION : 08245-SA



PCB STACKUP	
TOP	L1
GND	L2
S	L3
GND	L4
BOTTOM	L5
	L6

SYSTEM DC/DC	
ISL62392	42
INPUTS	OUTPUTS
DCRAT00T	SV_5S (6A) 3DSV_5S (7A) SV_ADR_5S 3DSV_ADR_5S

SYSTEM DC/DC	
TPS51124	43
INPUTS	OUTPUTS
DCRAT00T	1DSV_50 (9A) 1DSV_53 (12A)

RT9026	44
1DSV_53	DGR_VREF_53 (1.1.2A)

RT9018	44
1DSV_53	1DSV_50 (2A)

TPS51117	45
DCRAT00T	FRVDD (4A)

CHARGER	
ISL88731A	47
INPUTS	OUTPUTS
DCRAT00T	BT+

CPU DC/DC	
ISL6266A	41
INPUTS	OUTPUTS
DCRAT00T	VCC_CORE (3A)

VGA CORE	
RT6202A	47
INPUTS	OUTPUTS
DCRAT00T	VGA_CORE (1A)

GFXCORE	
ISL6263A	46
INPUTS	OUTPUTS
DCRAT00T	VCC_GFXCORE (7A)

A

B

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

C

D

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

E

F

CantigaD Chipset and ICH9M I/O Controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0= The ITPM Host Interface is enabled(Note2) 1=The ITPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default);Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default); Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/HDNMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 =Digital Display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:

1. All strap signals are sampled with respect to the leading edge of the (G/MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

JV50

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Title

Reference

Size A3

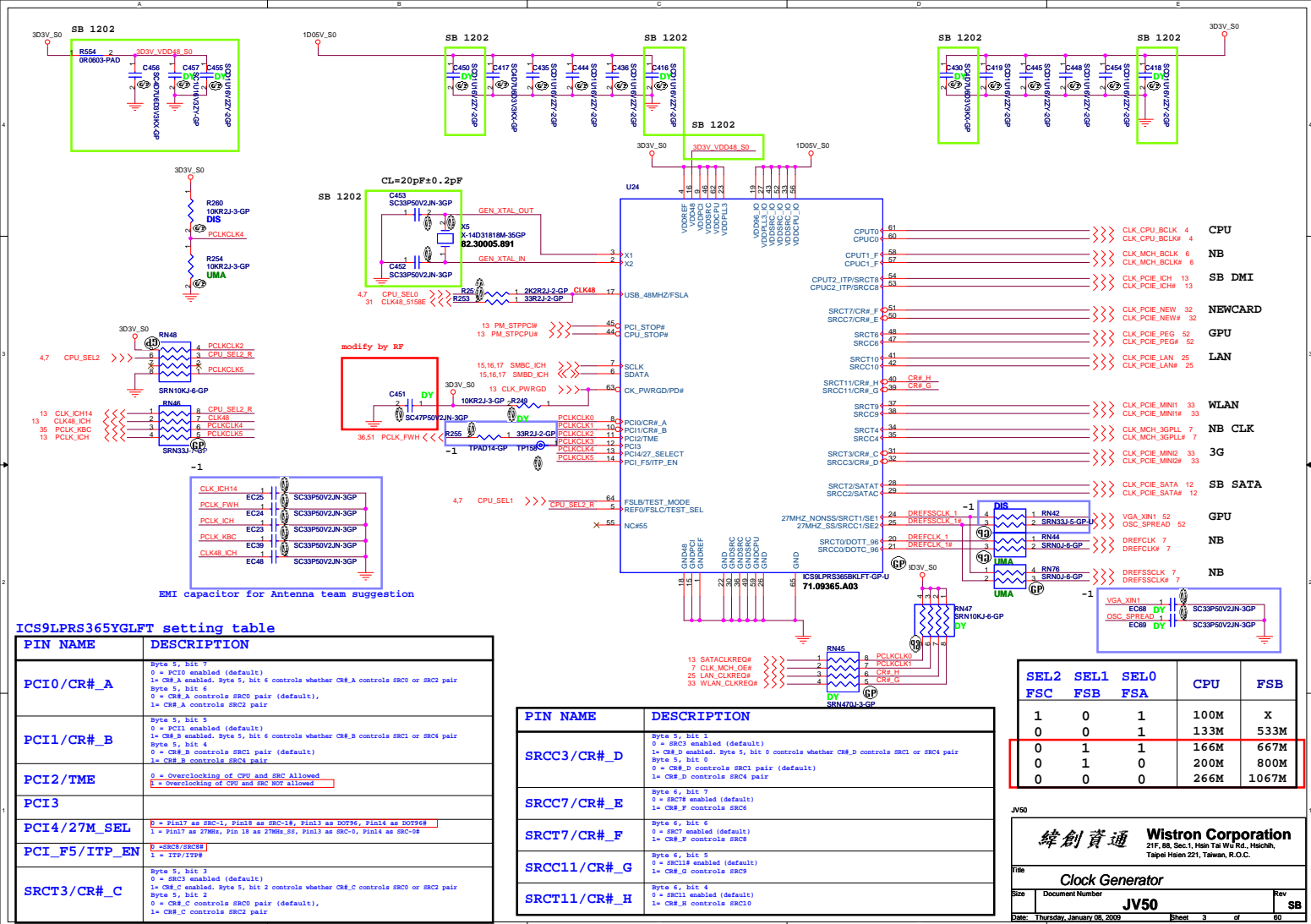
Document Number

Rev

SB

Date: Thursday, January 08, 2009

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SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

JV50

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Title

Clock Generator

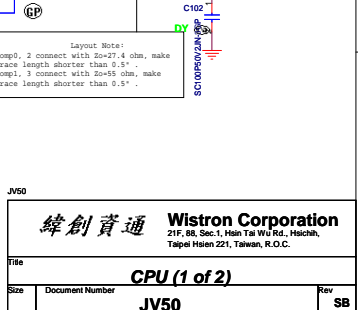
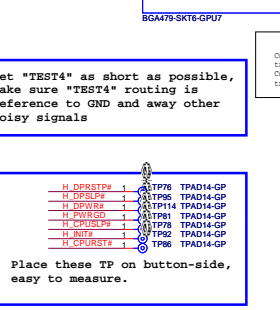
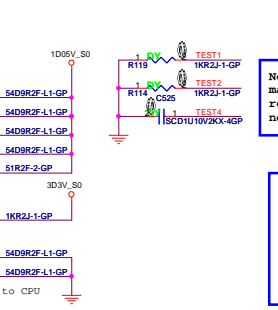
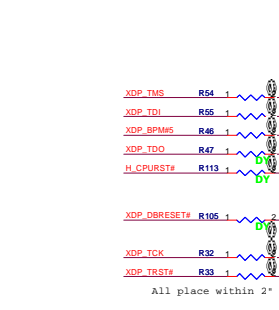
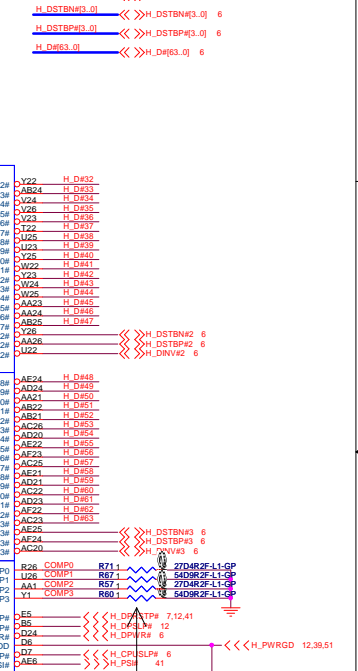
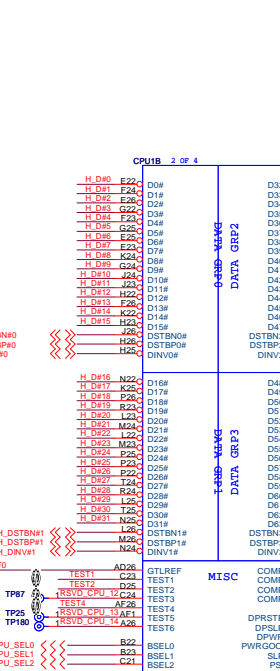
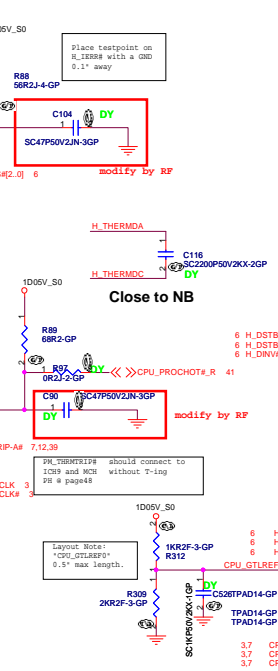
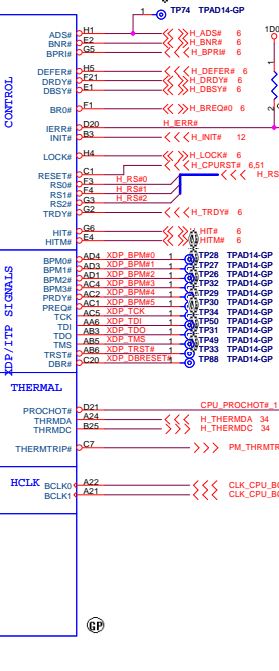
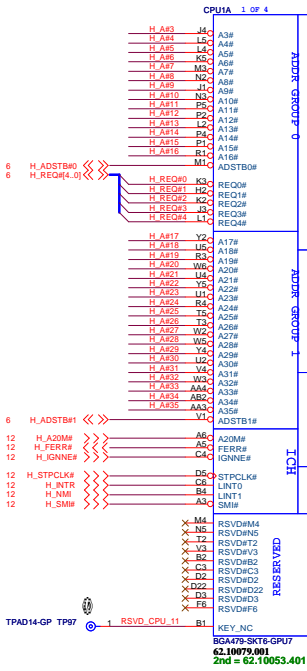
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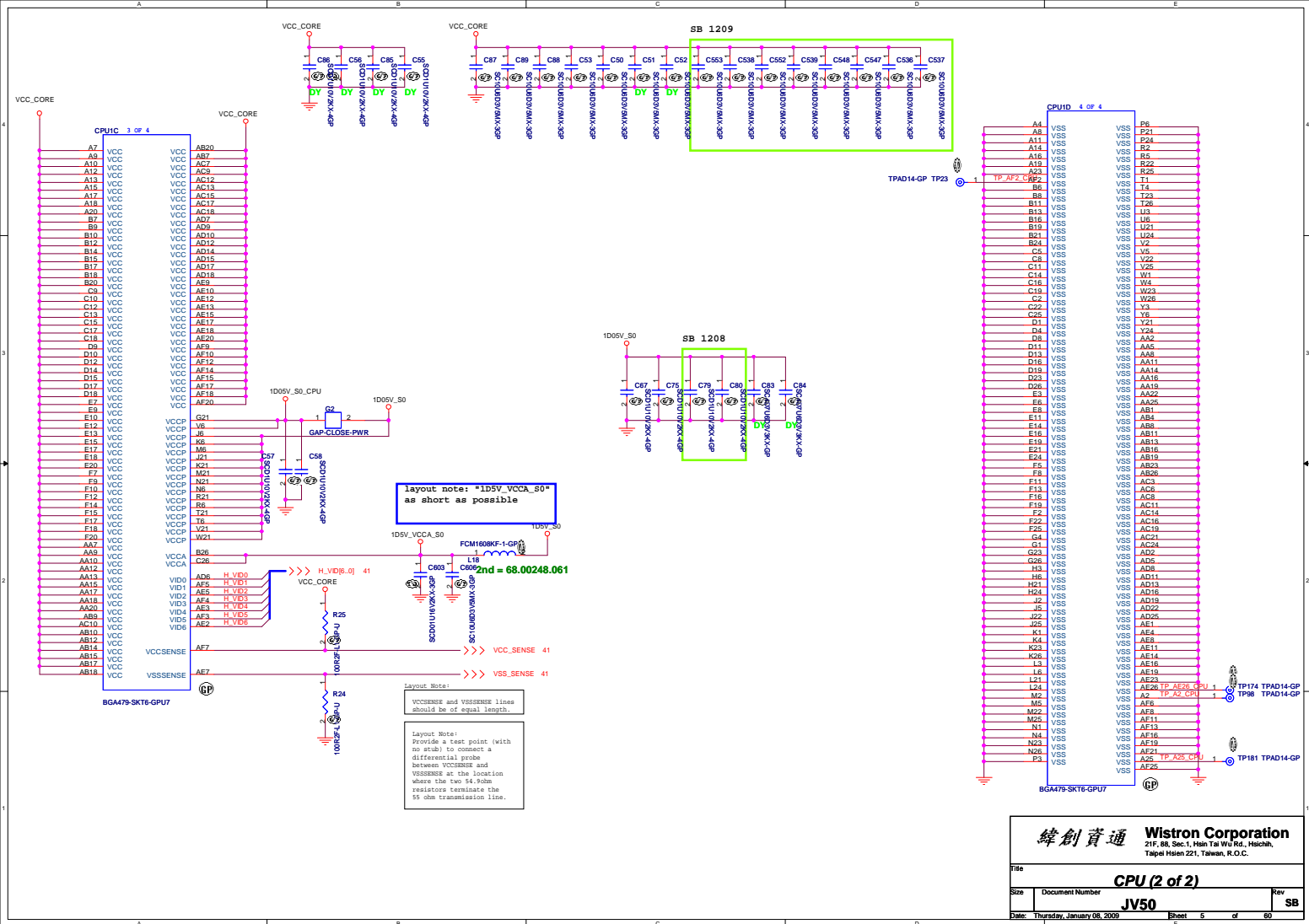
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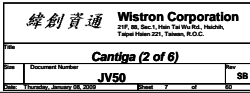
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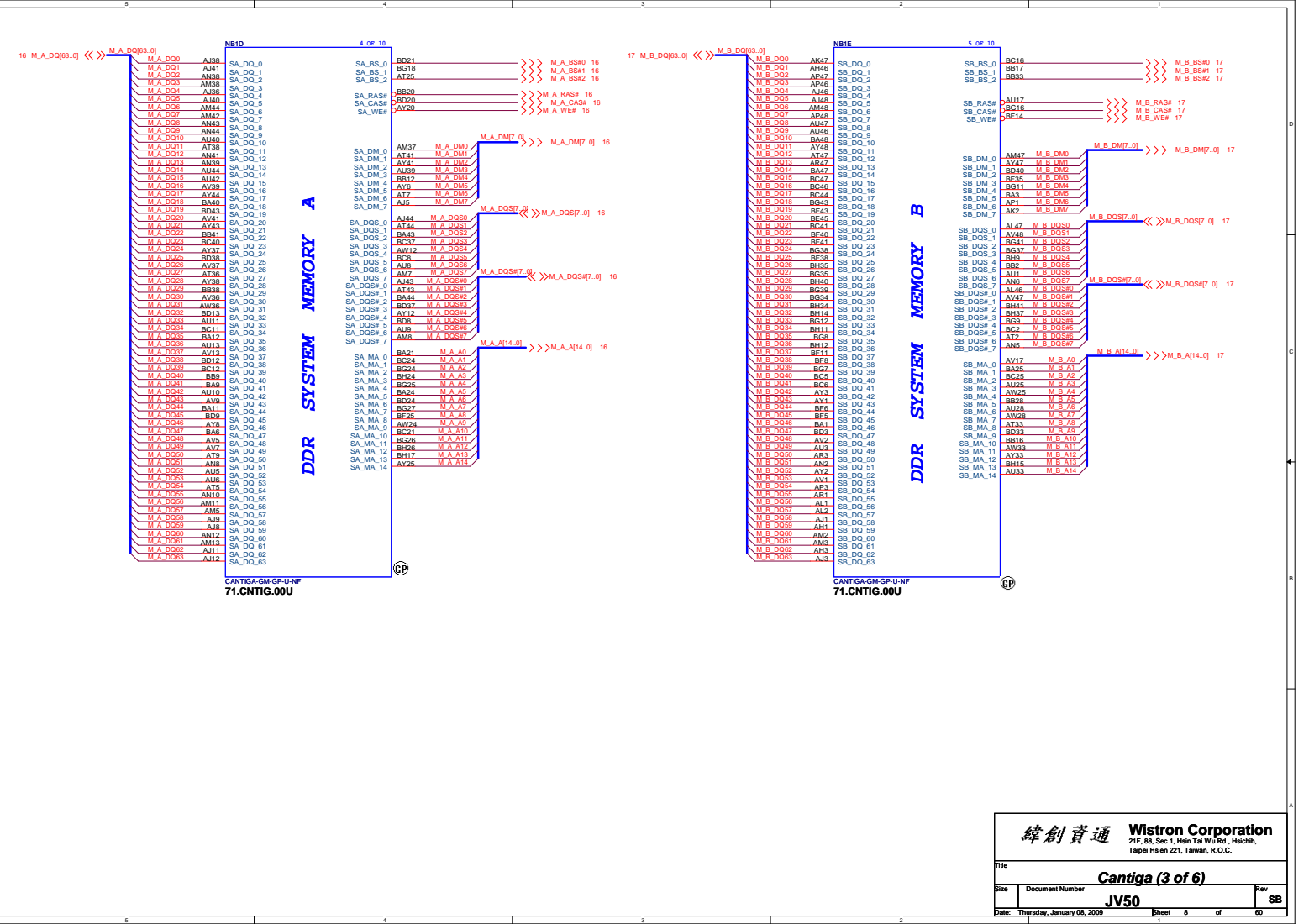
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6 H_AH35.3 <<> H_AH35.3



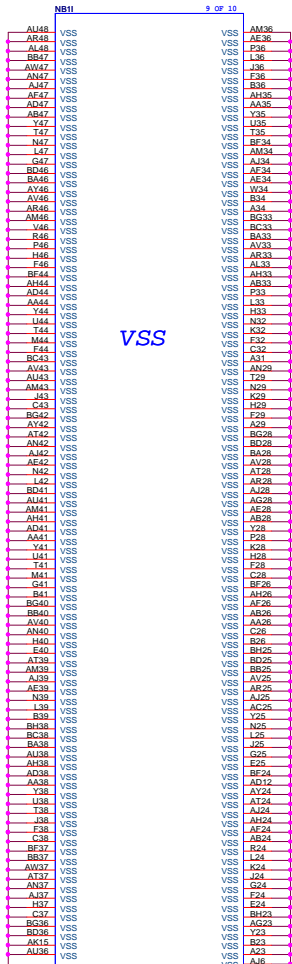




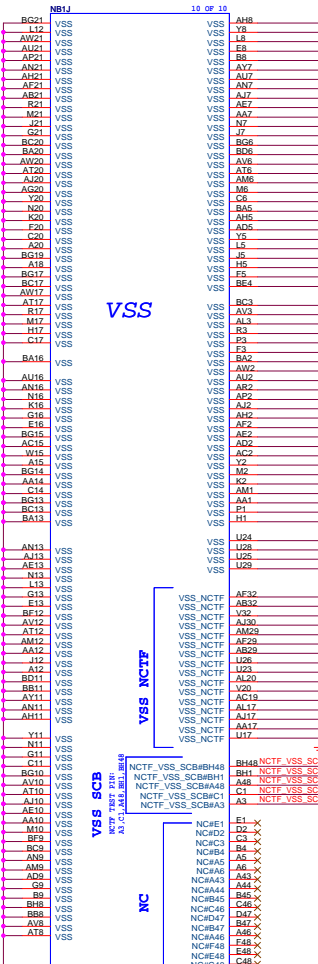


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Cantiga (3 of 6)	
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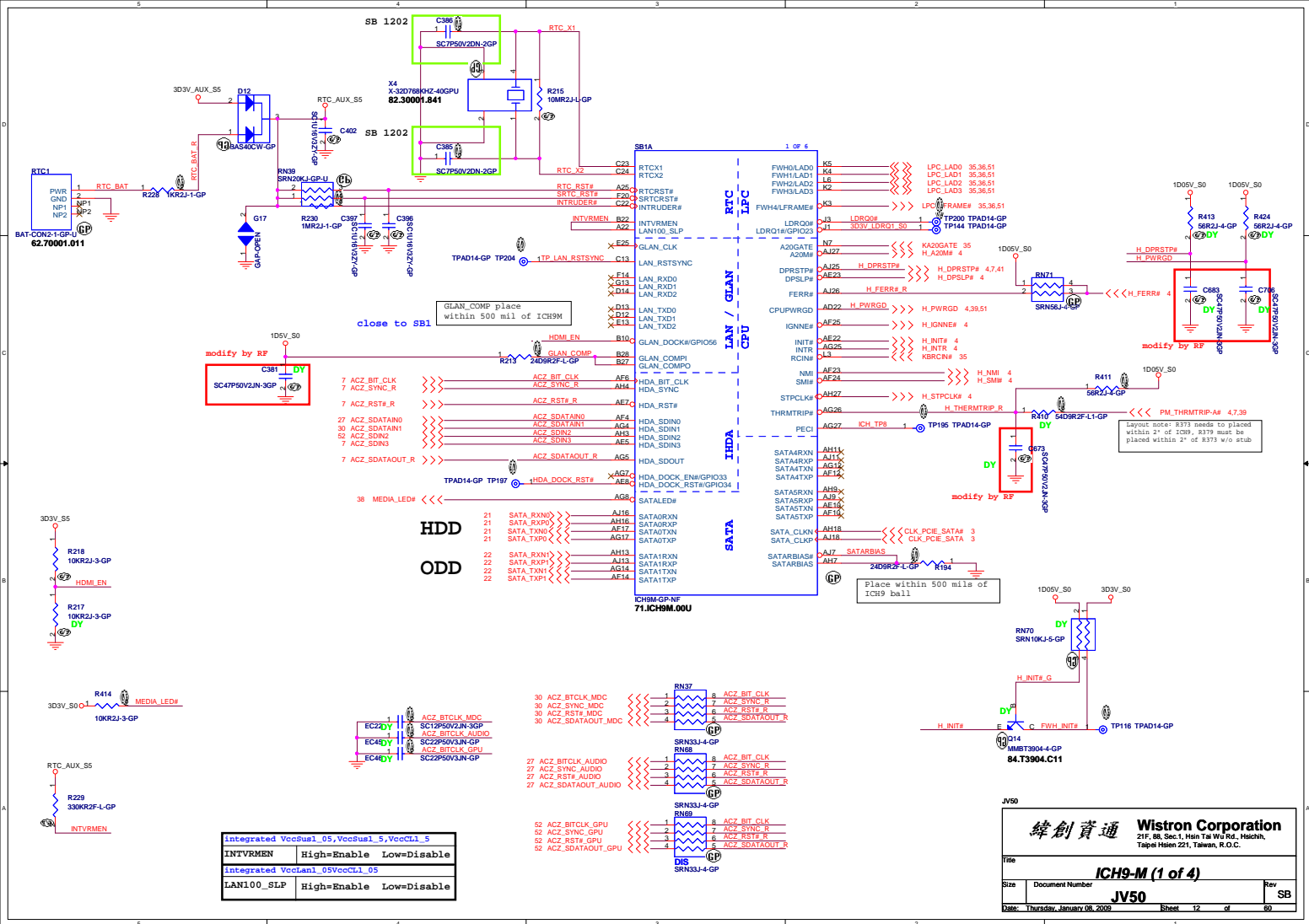


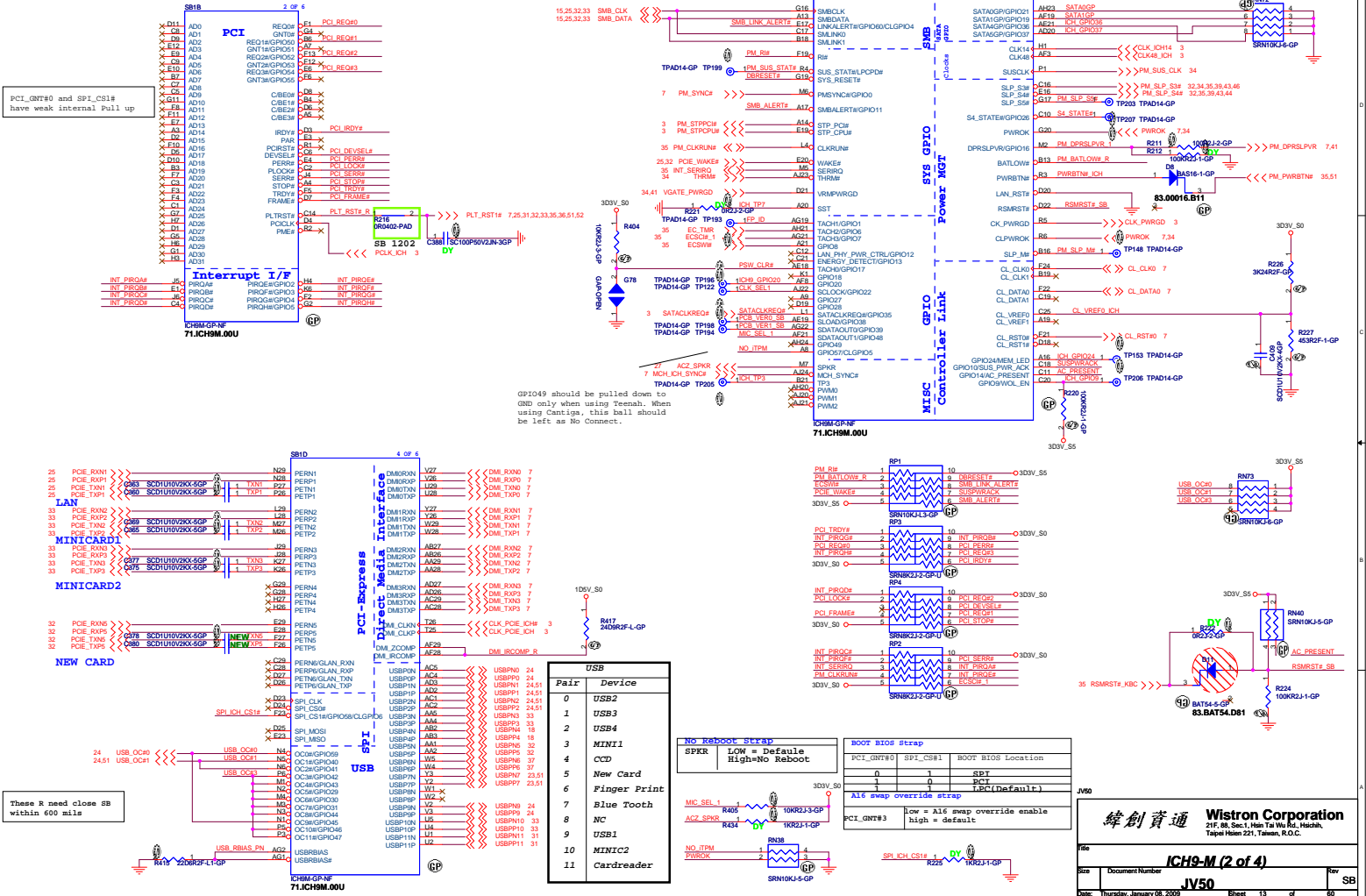
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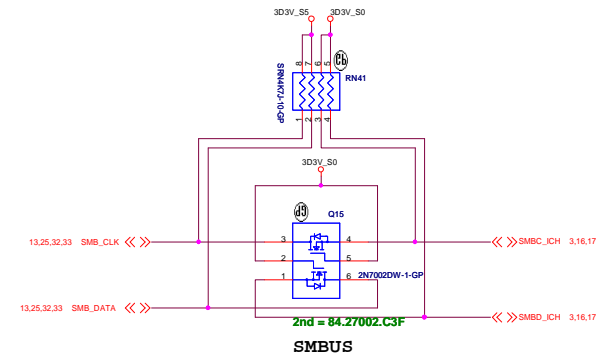
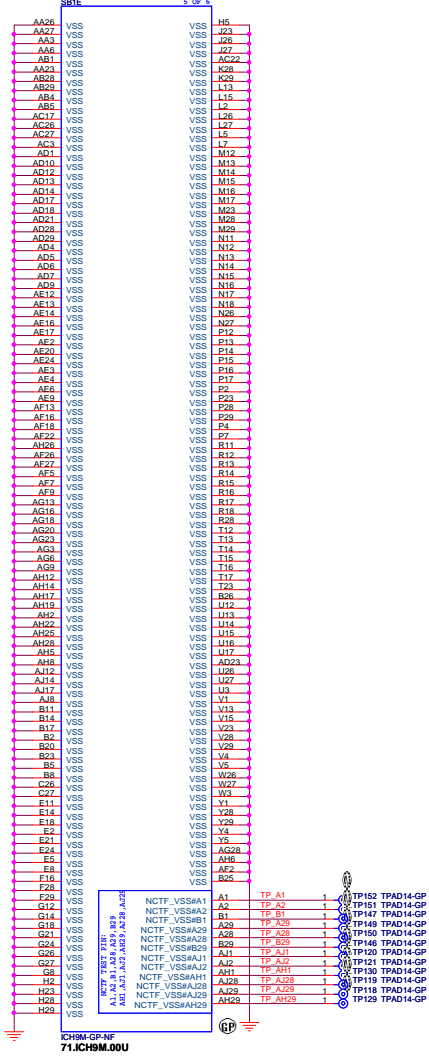


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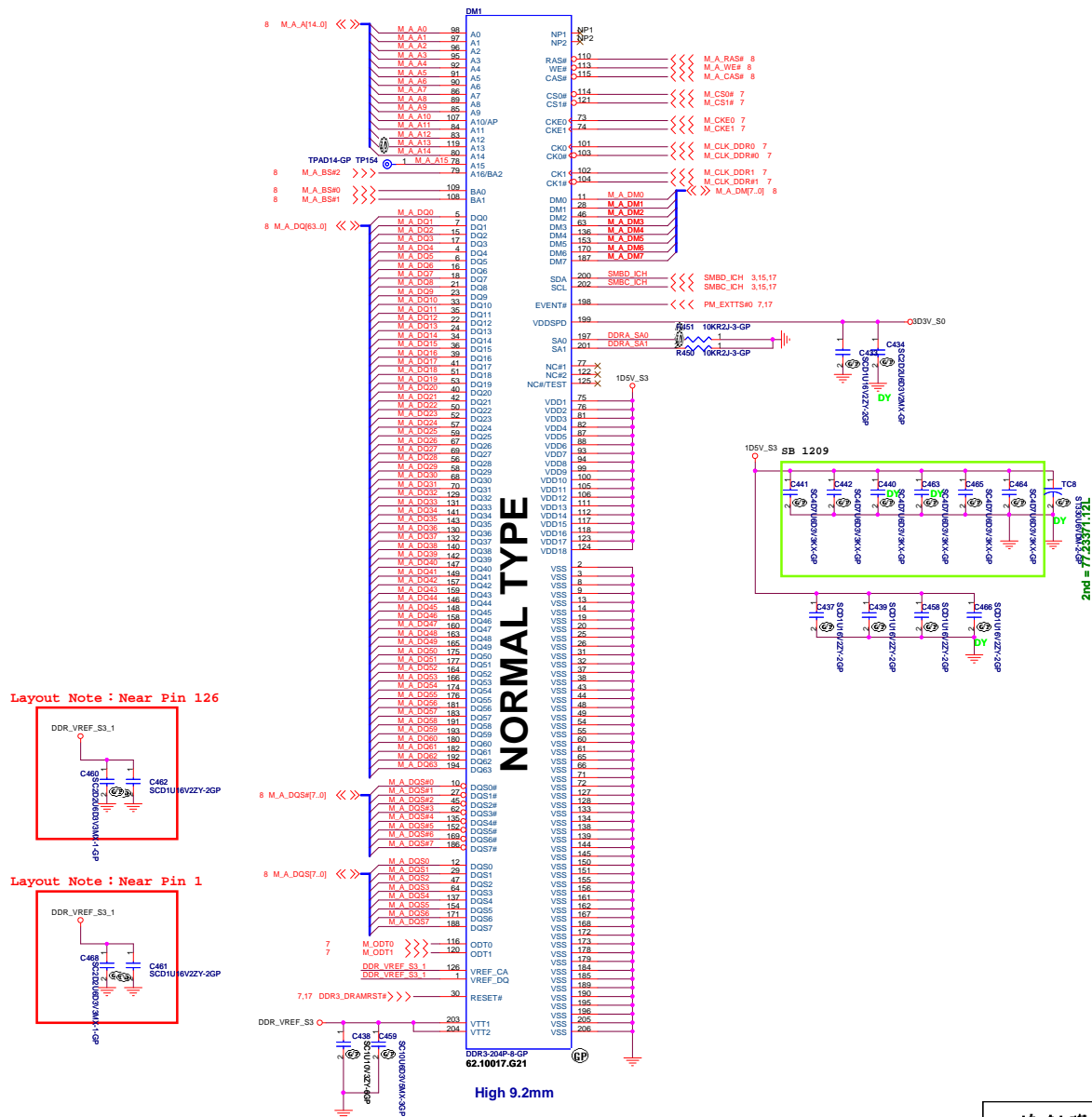
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DDR3 SOCKET_1



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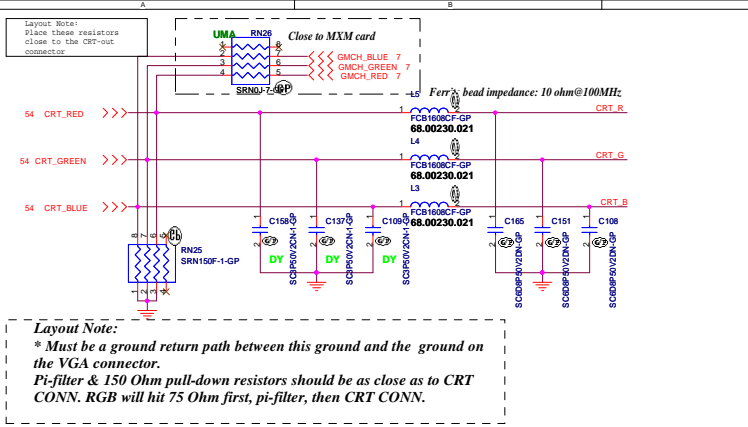
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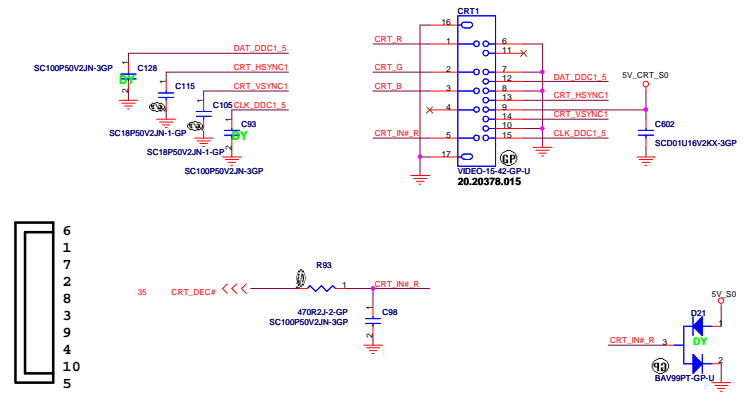


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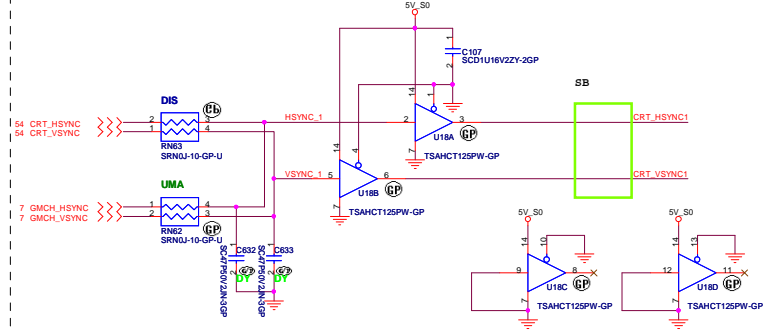
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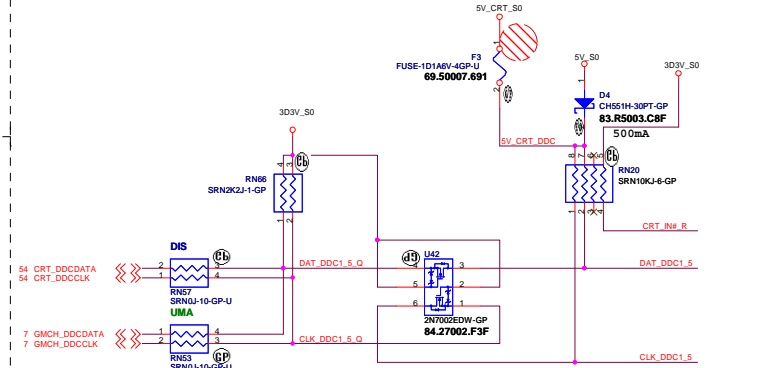
CRT I/F & CONNECTOR



Hsync & Vsync level shift



DDC_CLK & DATA level shift



JV50

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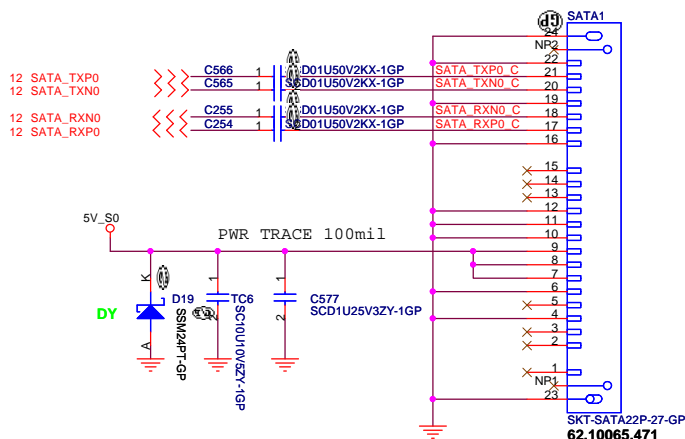
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Rev SB

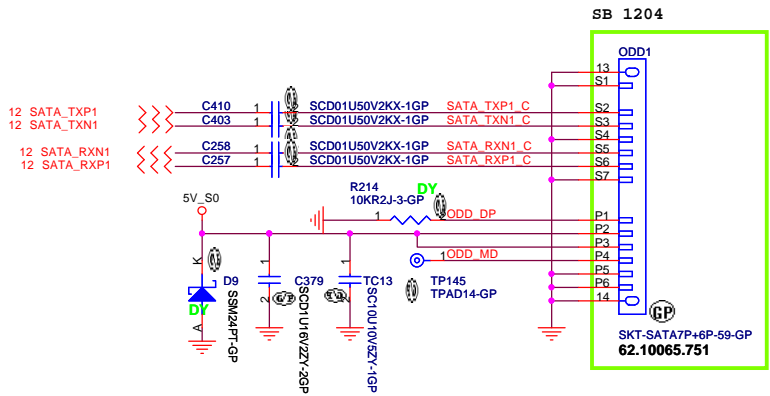
SATA Connector



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ODD Connector



JV50

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3D3V_BT_S0

3D3V_BT_S0

EC59 **DY**

SCD1U16V2ZY-2GP

U65

OUT GND NC#3

IN EN

G5240B1T1U-GP

3D3V_S0

C862

SC4D7U10V5ZY-3GP

BLUETOOTH_EN 35

EC20 put near BLUE1 / all

USB put one choke near connector by EMI request

BT1

ACES-CON4-1-GP-U2

20.D0197.104

USBPN7 13.51

USBPP7 13.51

3D3V_BT_S0

EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

JV50

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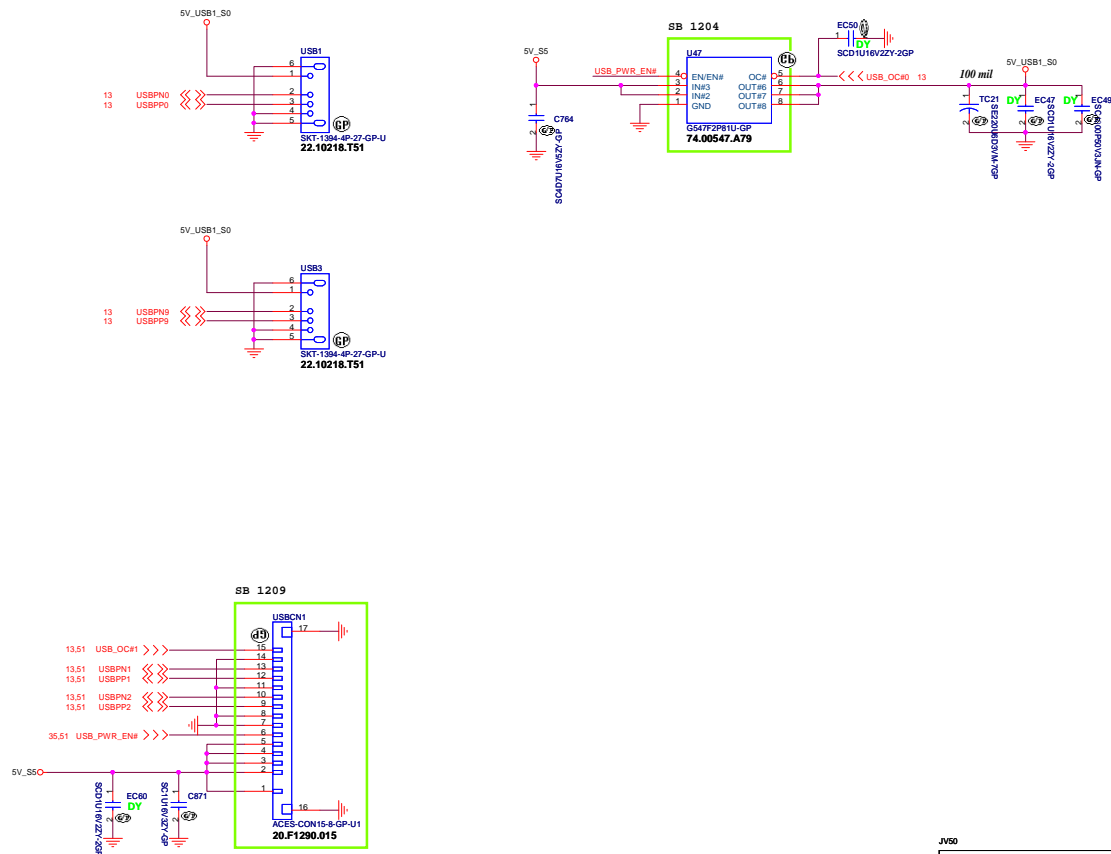
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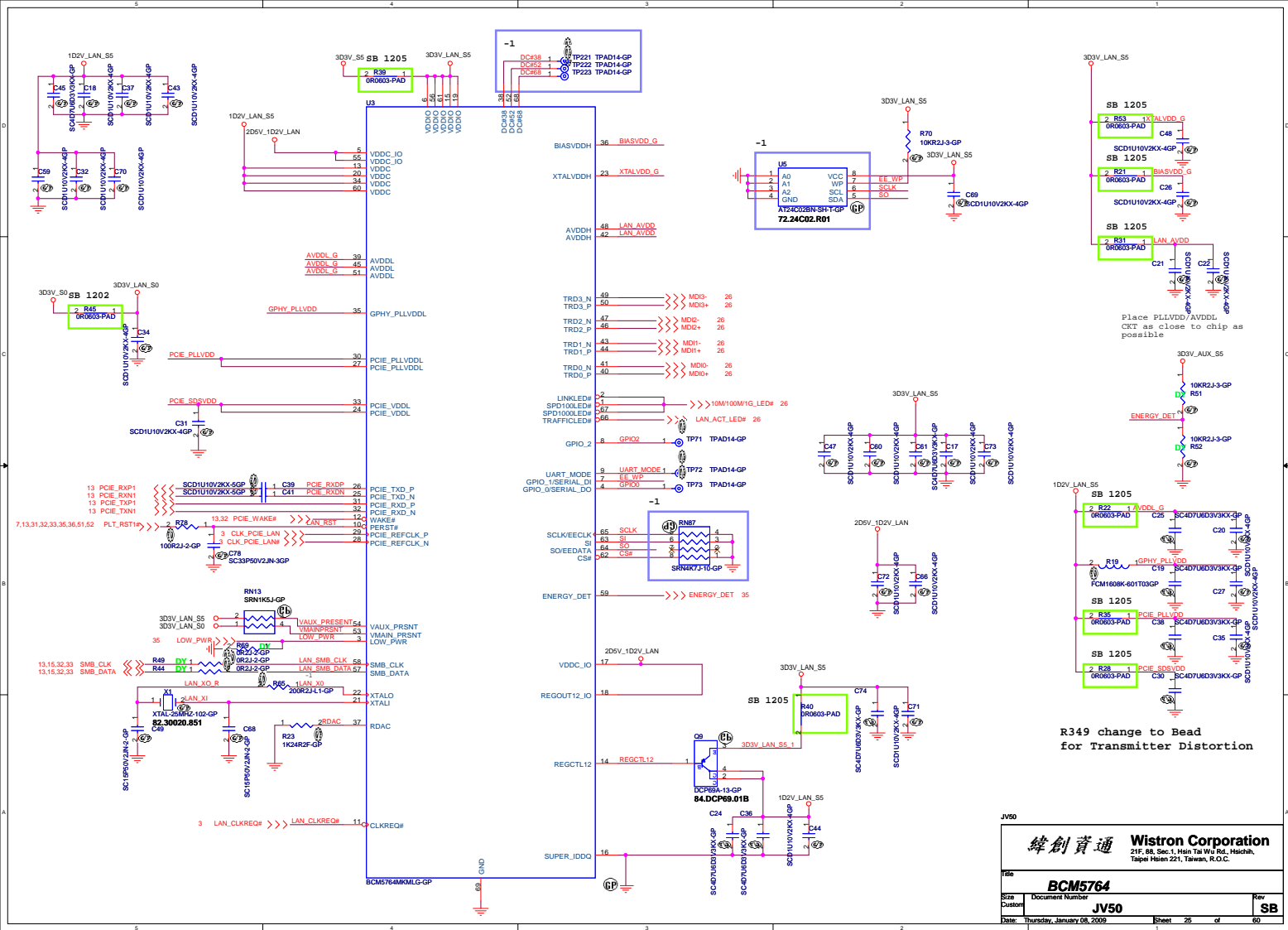
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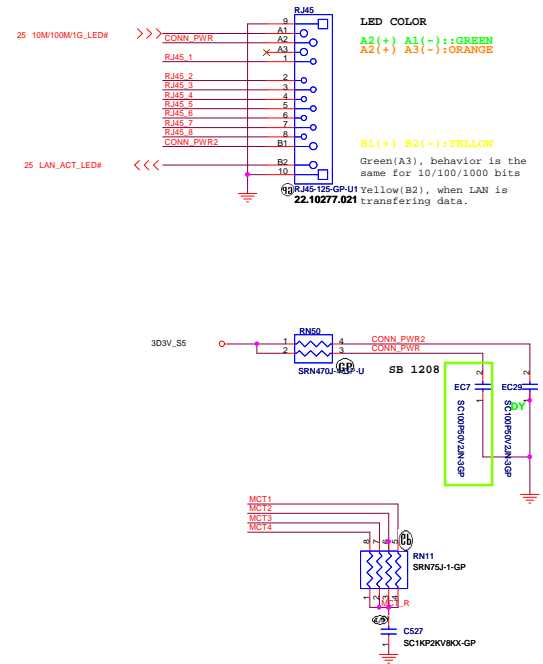
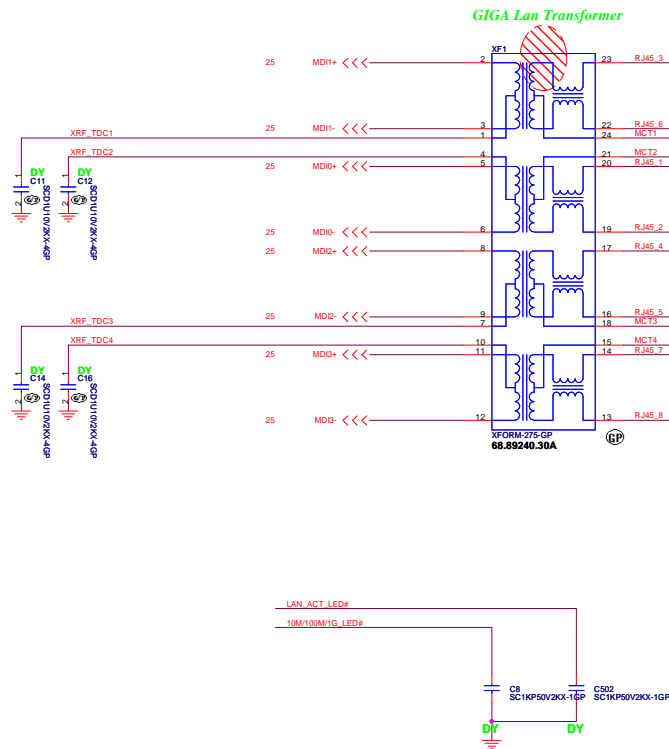
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LAN Connector

LAN Connector

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



JV50

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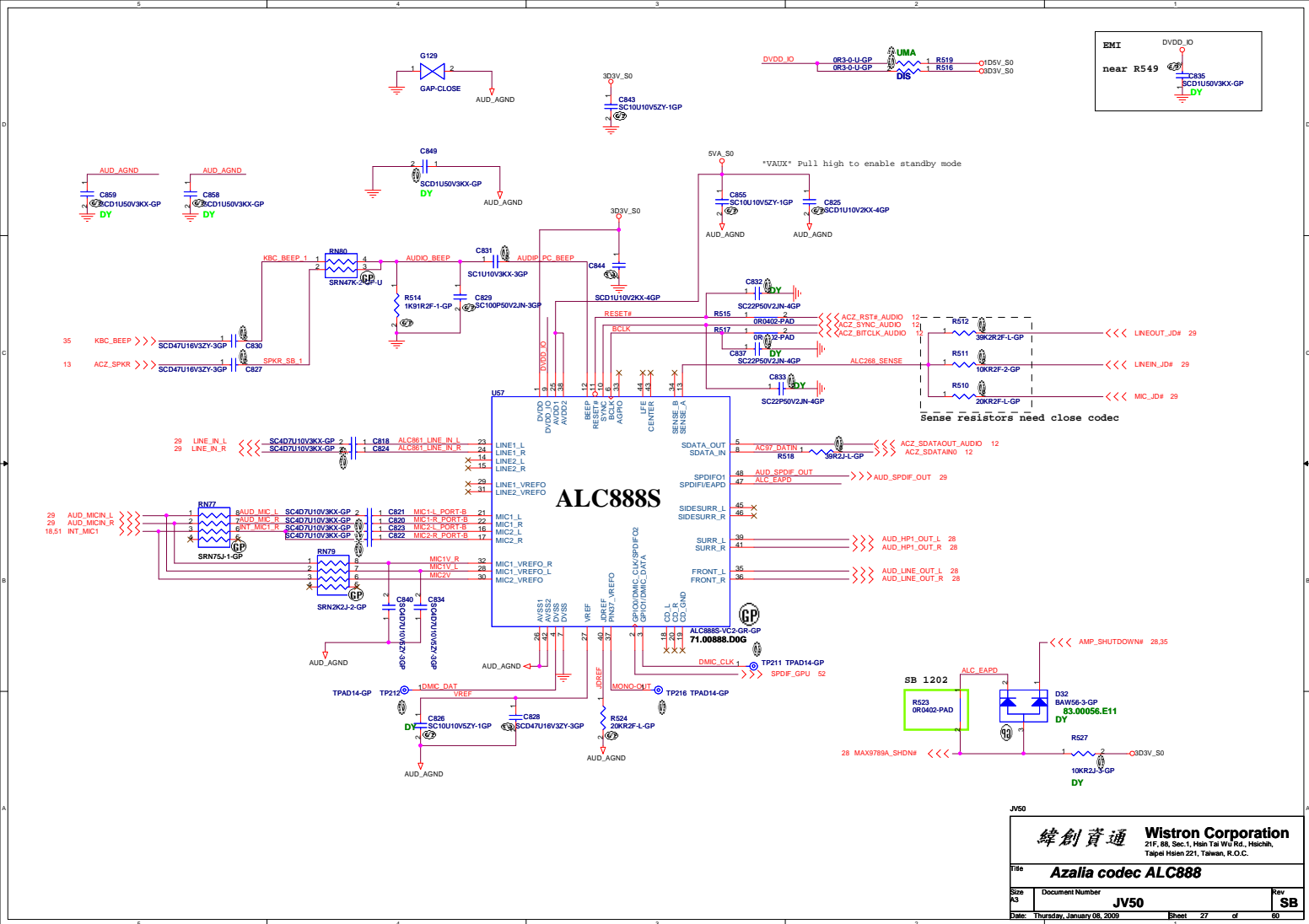
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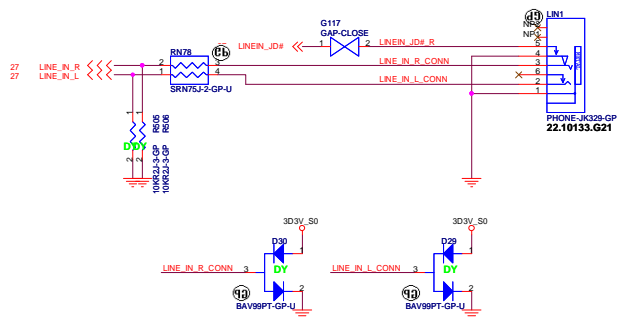
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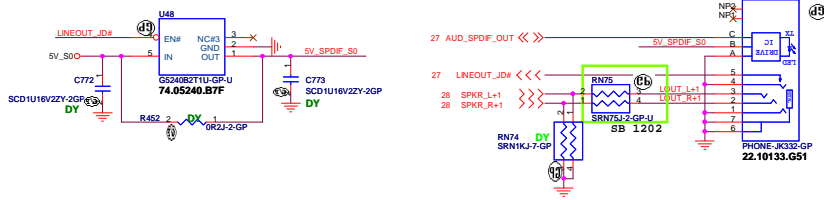
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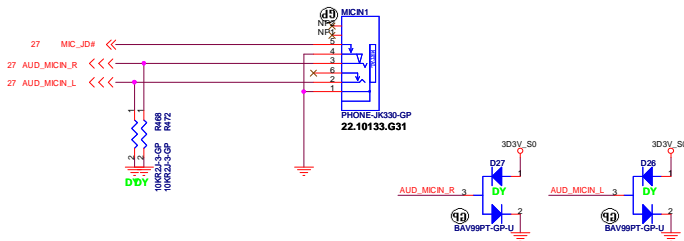
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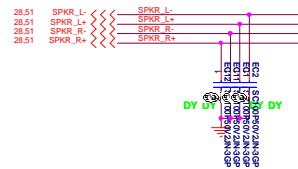
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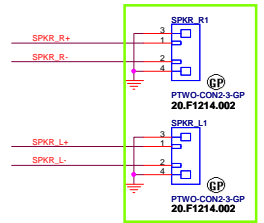
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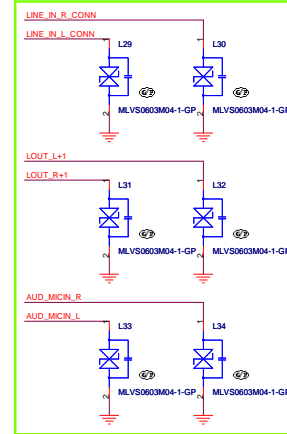
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SB 1202



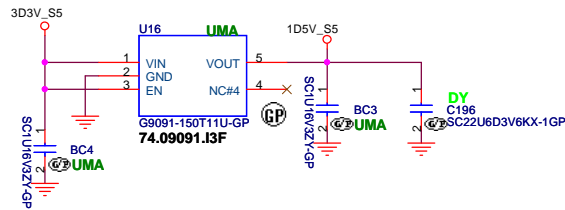
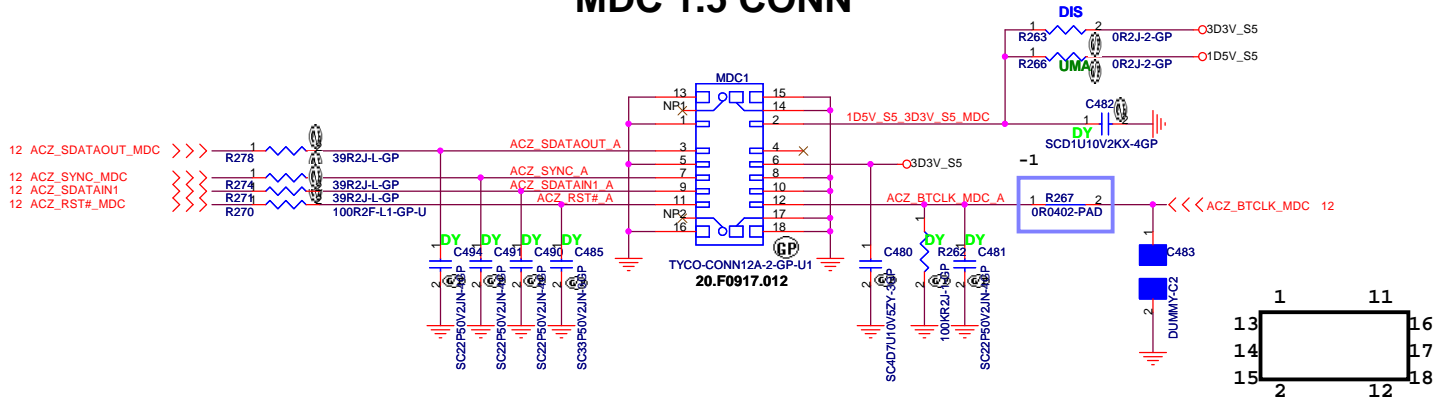
SB 1202



JV50

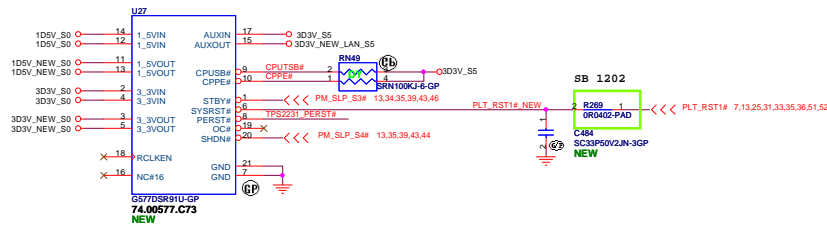
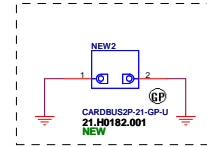
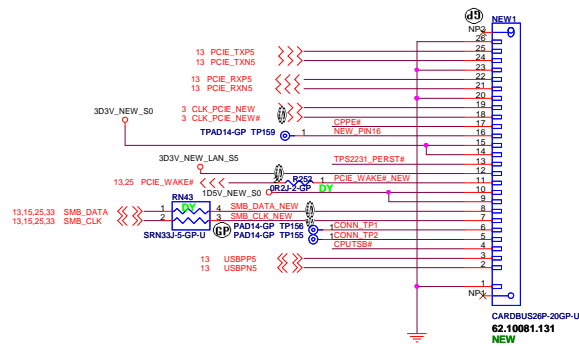
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipex Hsien 221, Taiwan, R.O.C.	
AUDIO jack			
Document Number	JV50		Rev SB
Thursday, January 08, 2009			
Sheet 29		of 60	

MDC 1.5 CONN

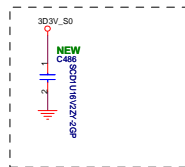


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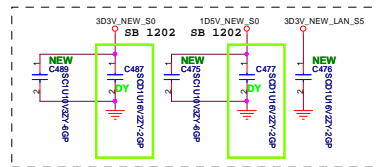
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MDC	
Size	Document Number
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Place them Near to Chip



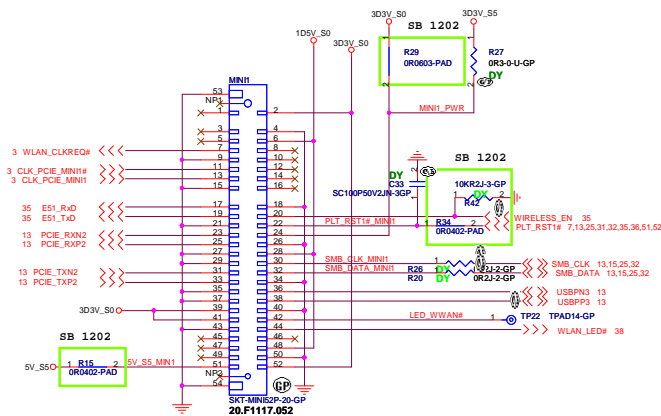
Place them Near to Connector



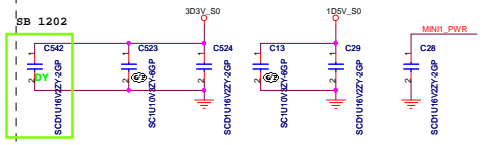
JV50

緯創資通		Wistron Corporation	
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.			
NEW CARD			
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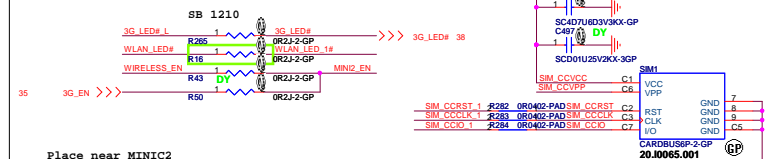
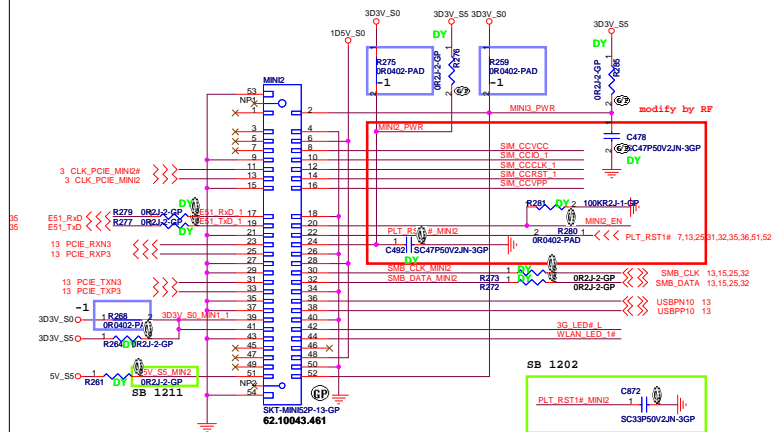
Mini Card Connector(WLAN) Support debug-card



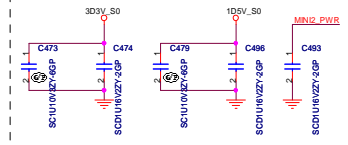
Place near MINI1



Mini Card Connector(Robson2 and 3G)



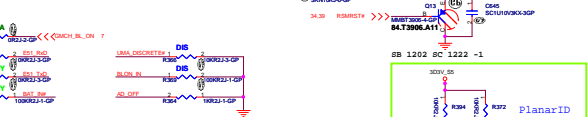
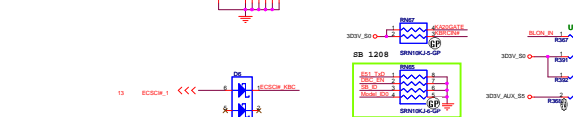
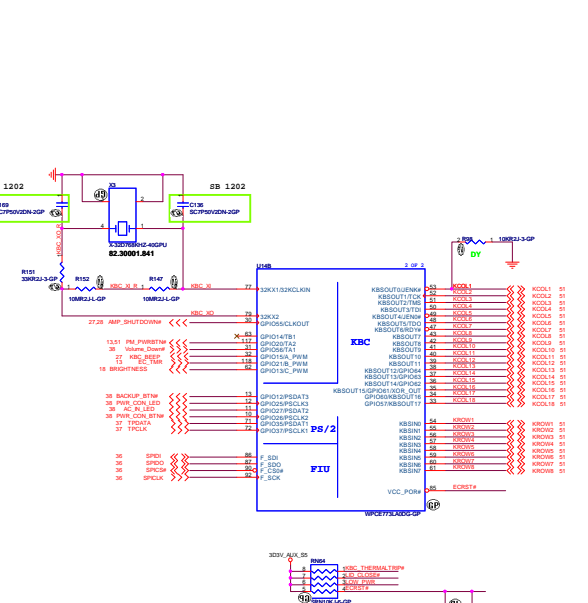
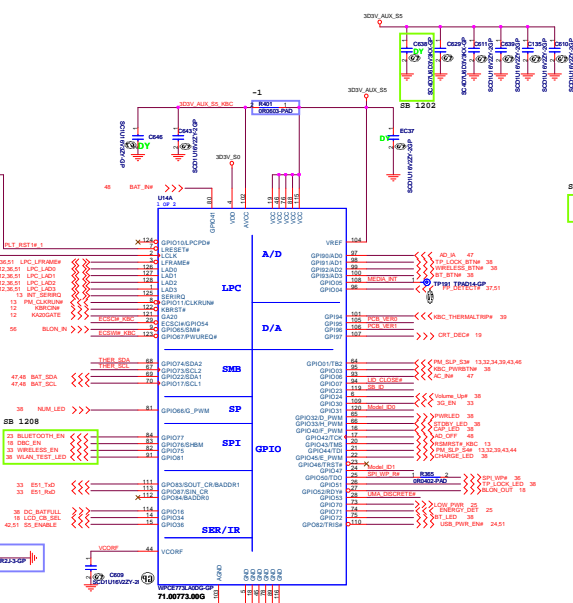
Place near MINIC2



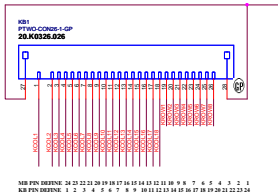
JV50

 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINI CARD JV50			
Size A3	Document Number	Rev	SB
Date:	Thursday, January 08, 2009	Sheet	23 of 28



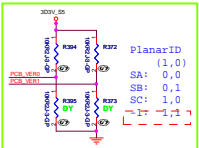
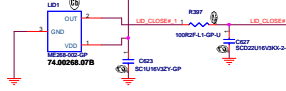


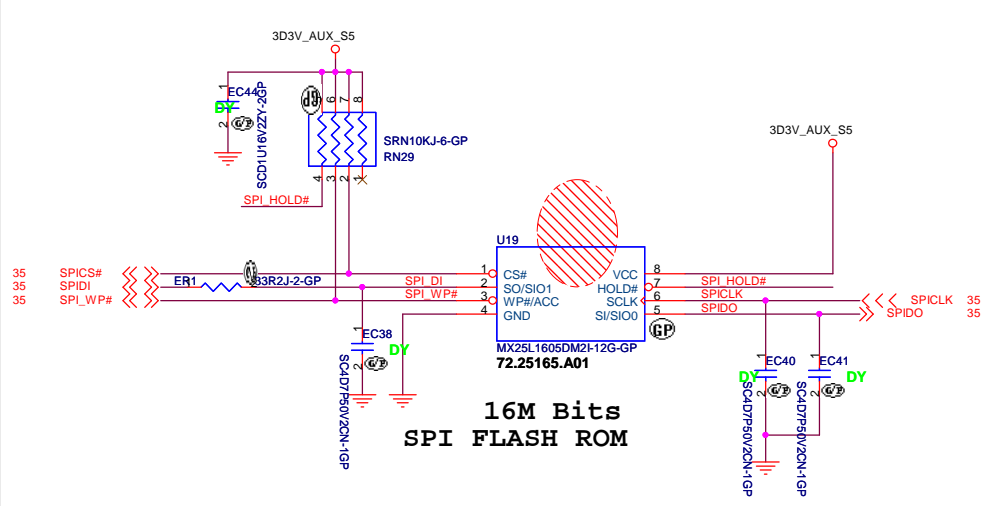
Internal KeyBoard Connector



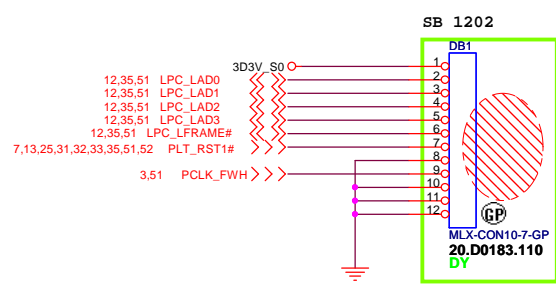
Cover Up Switch

2nd source:20.F00984.002





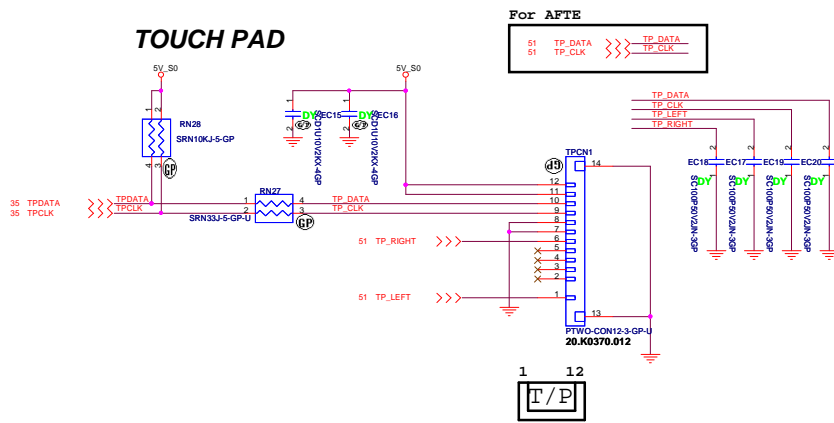
GOLDEN FINGER FOR DEBUG BOARD



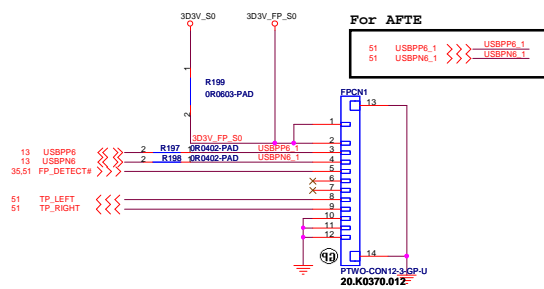
JV50

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		BIOS	
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TOUCH PAD



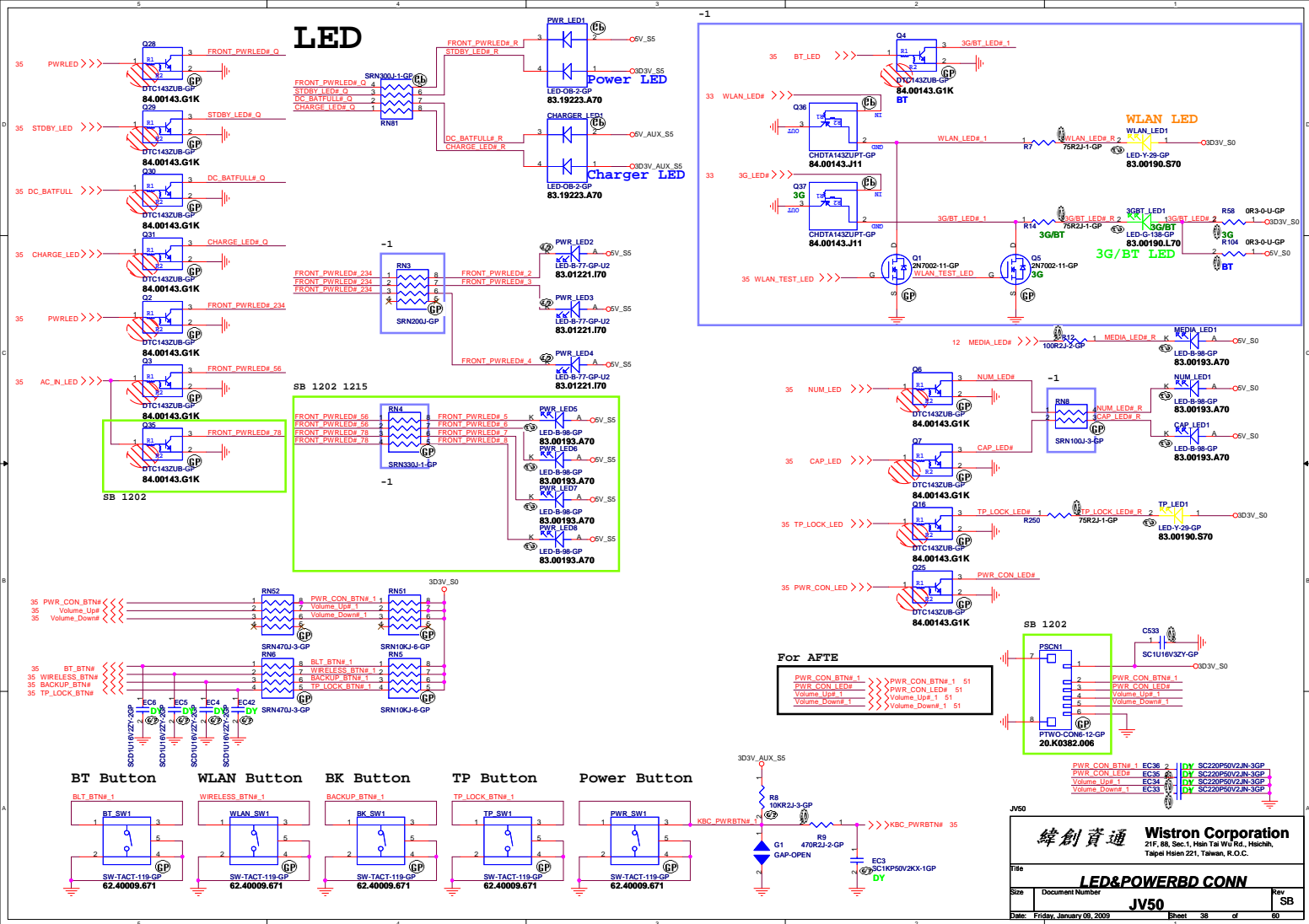
Finger printer

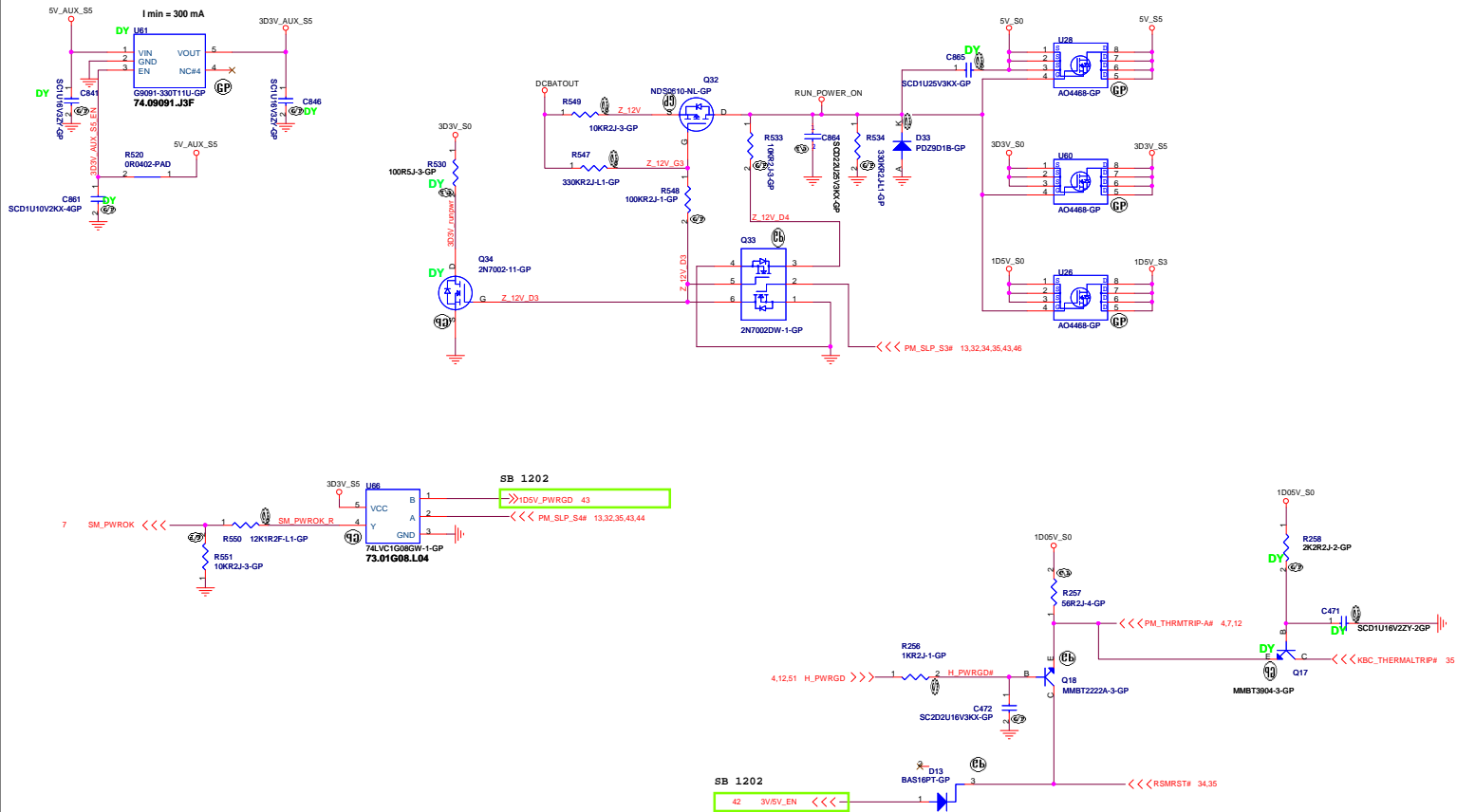


JV50

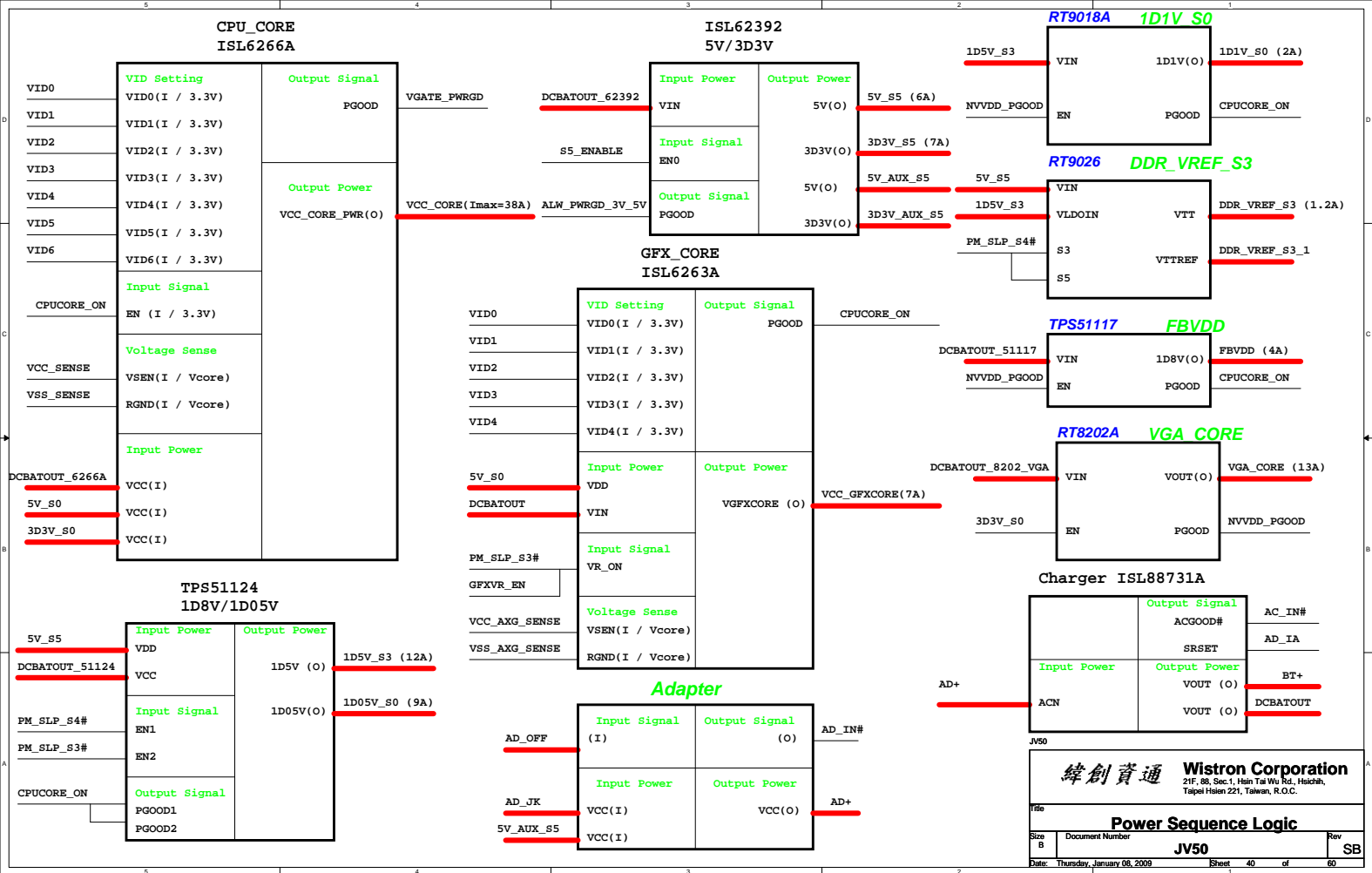
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21F, 8th, Sec.1, Hsin-Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

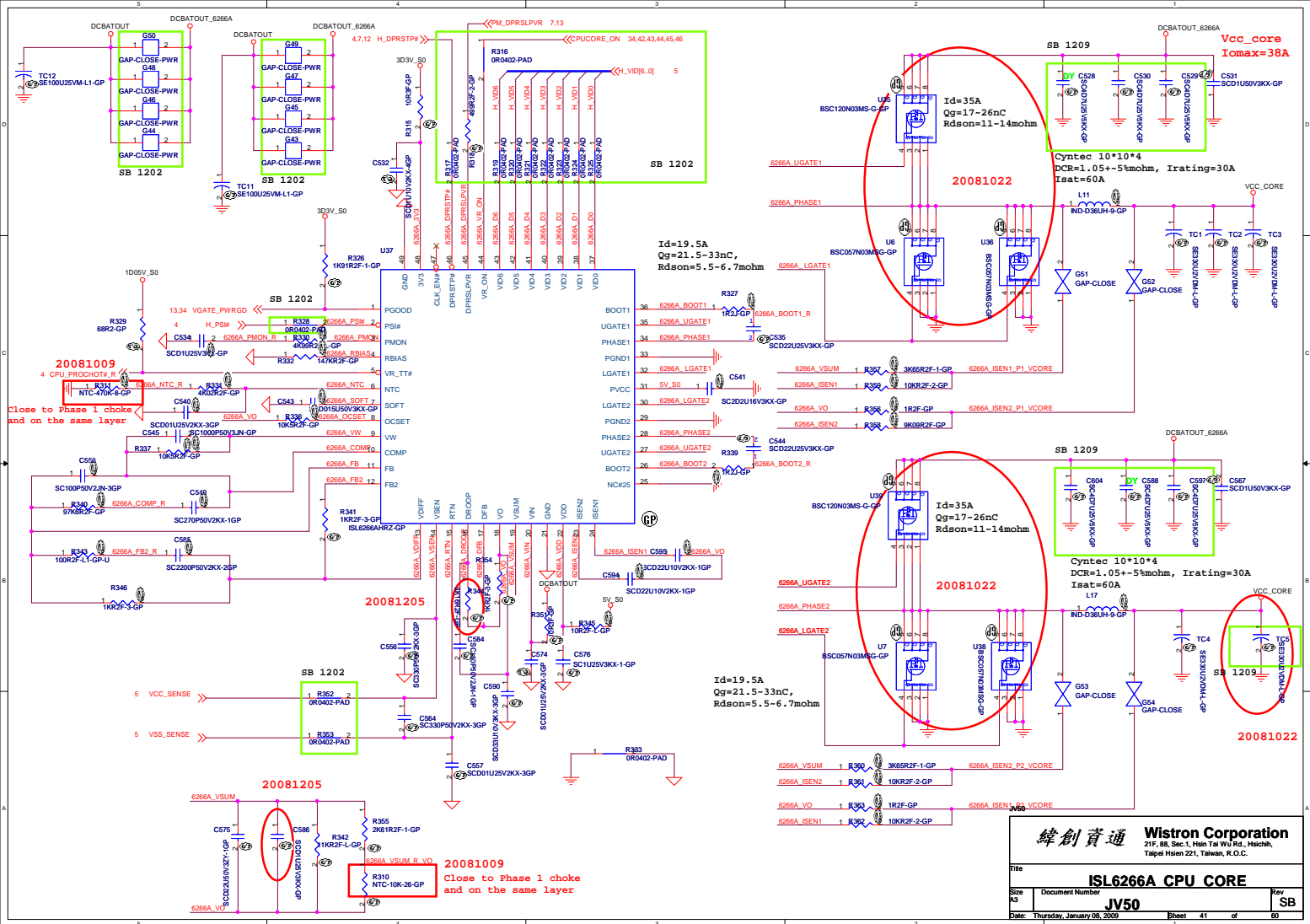
Title		
Touch PAD and FP		
Size	Document Number	Rev
	JV50	SB
Date: Thursday, January 08, 2009	Sheet 37 of 60	

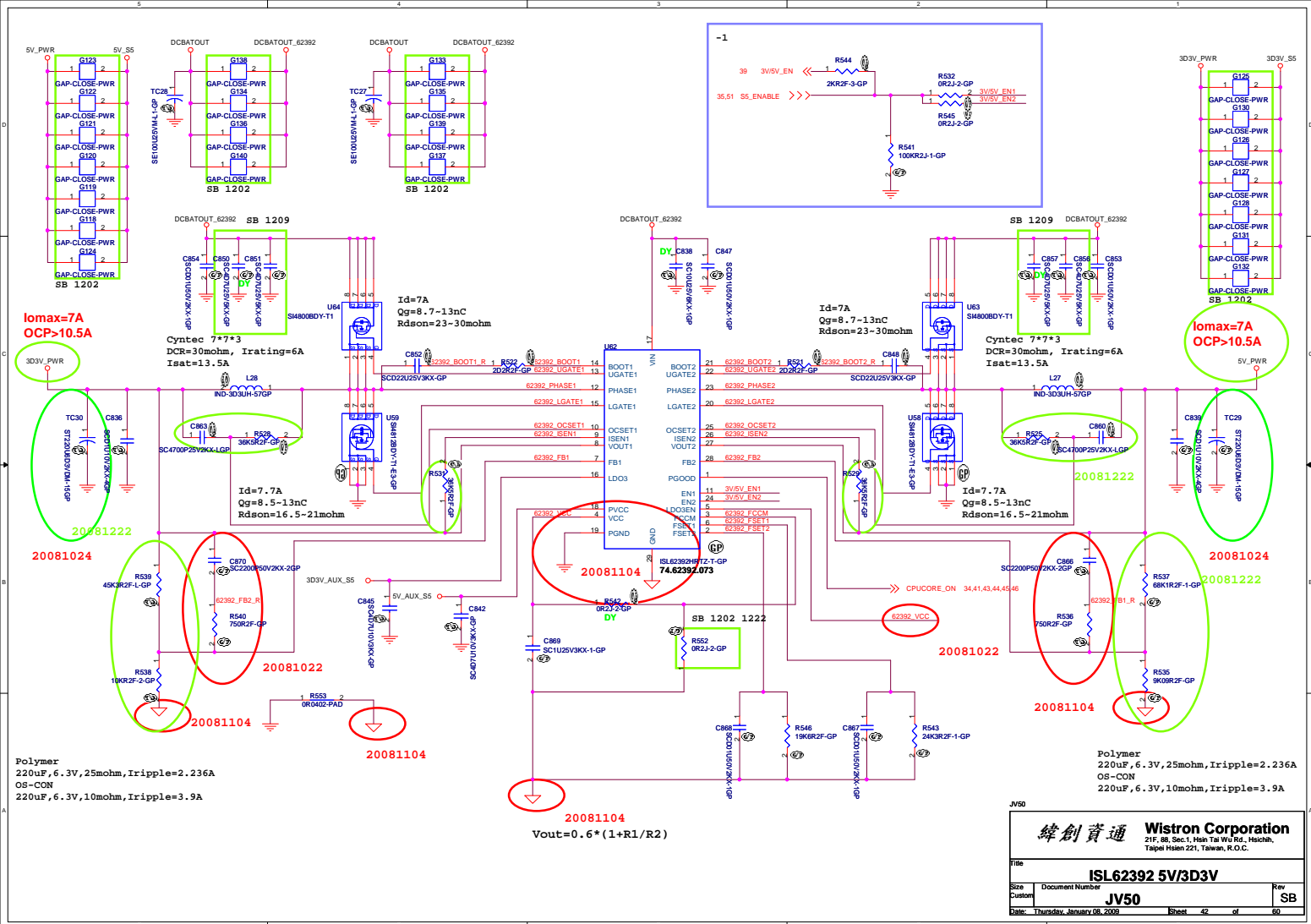


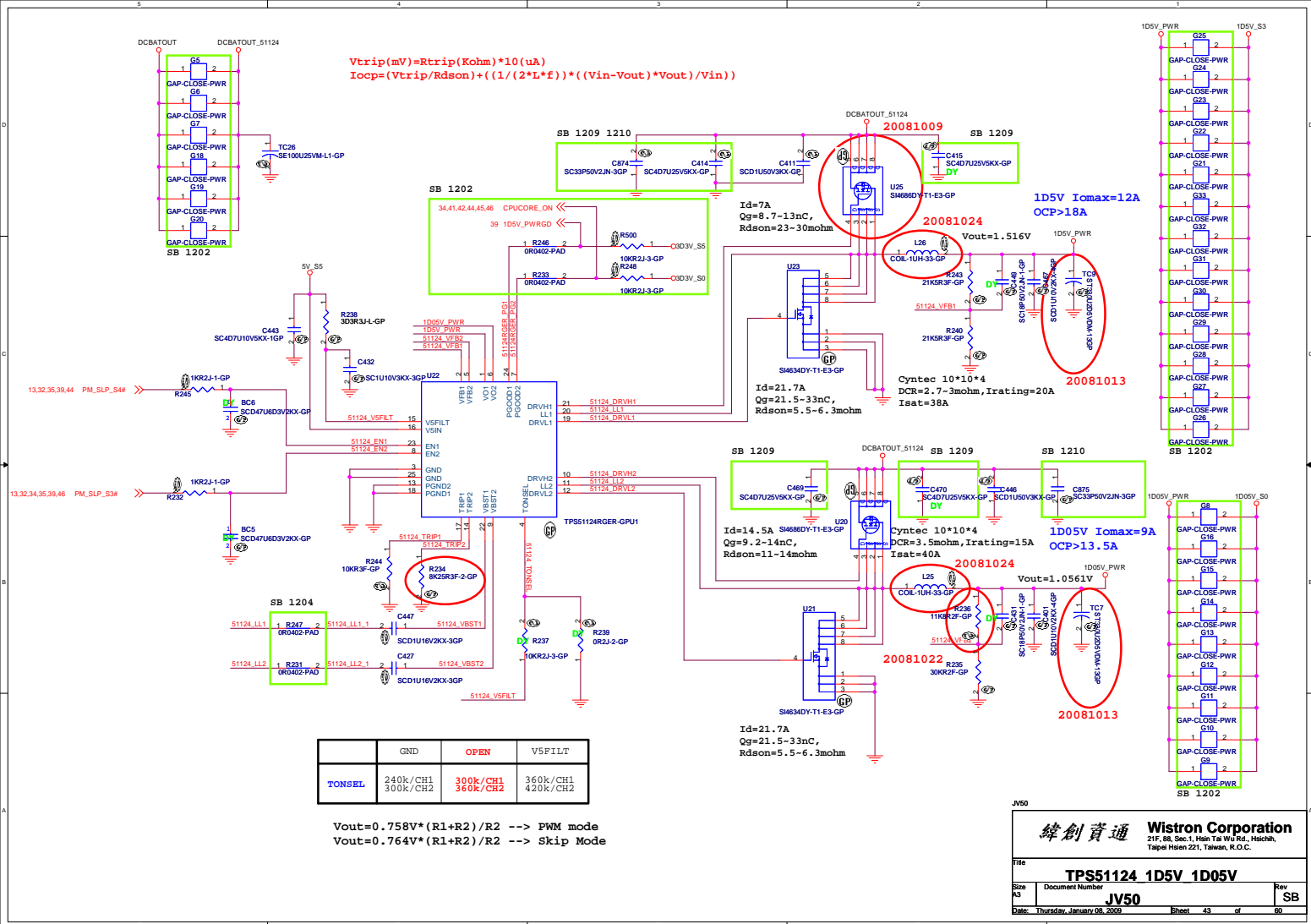


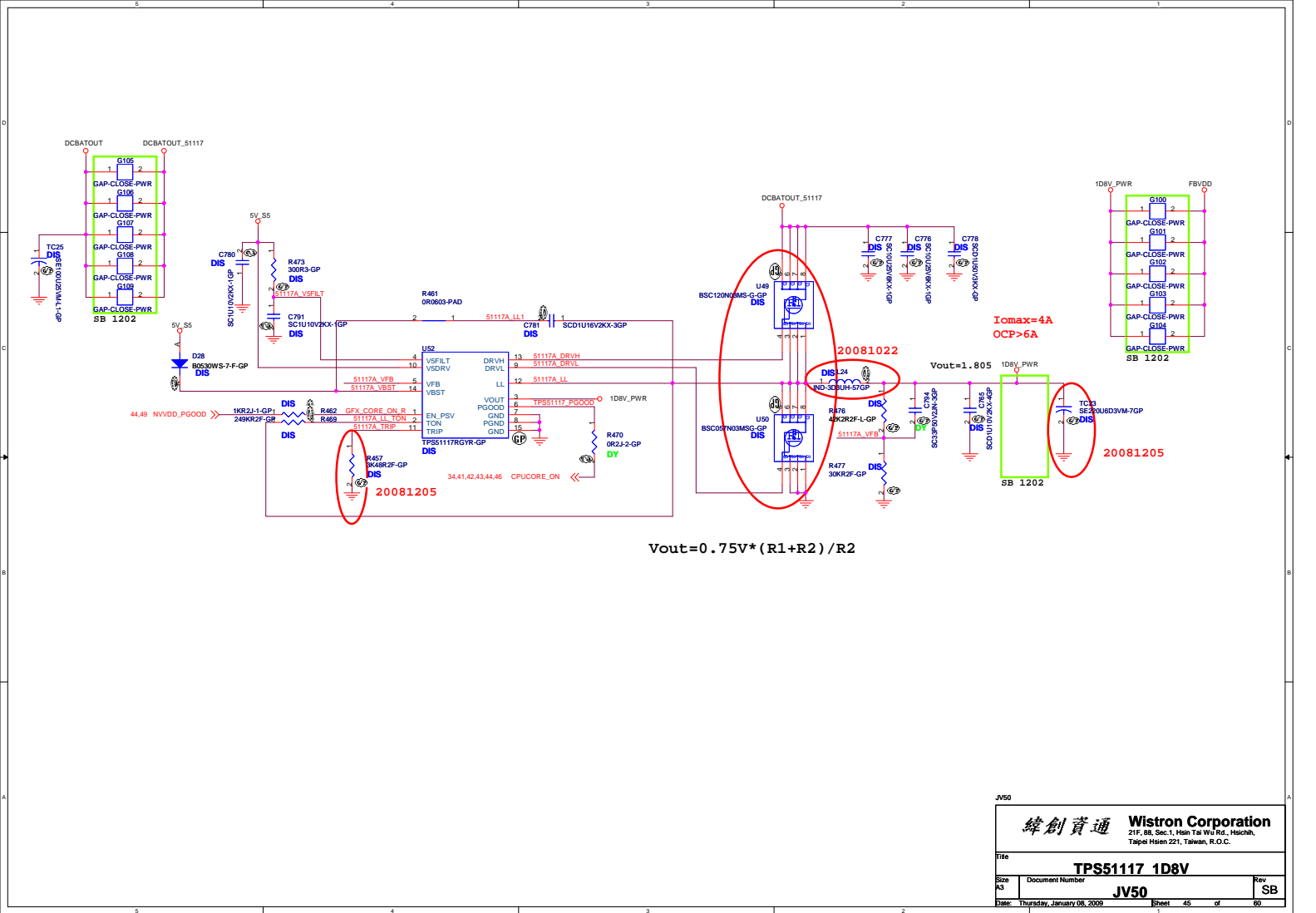
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
File	RUN POWER and 3D3V_AUX_S5
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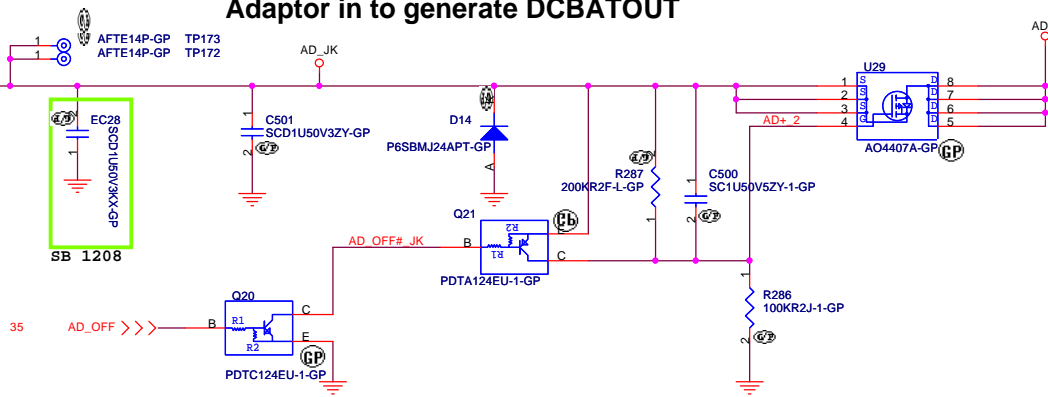




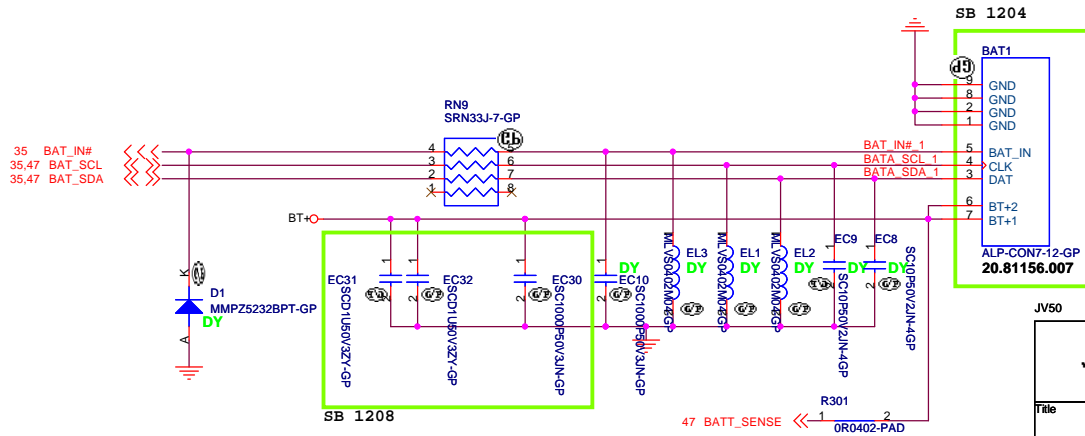




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



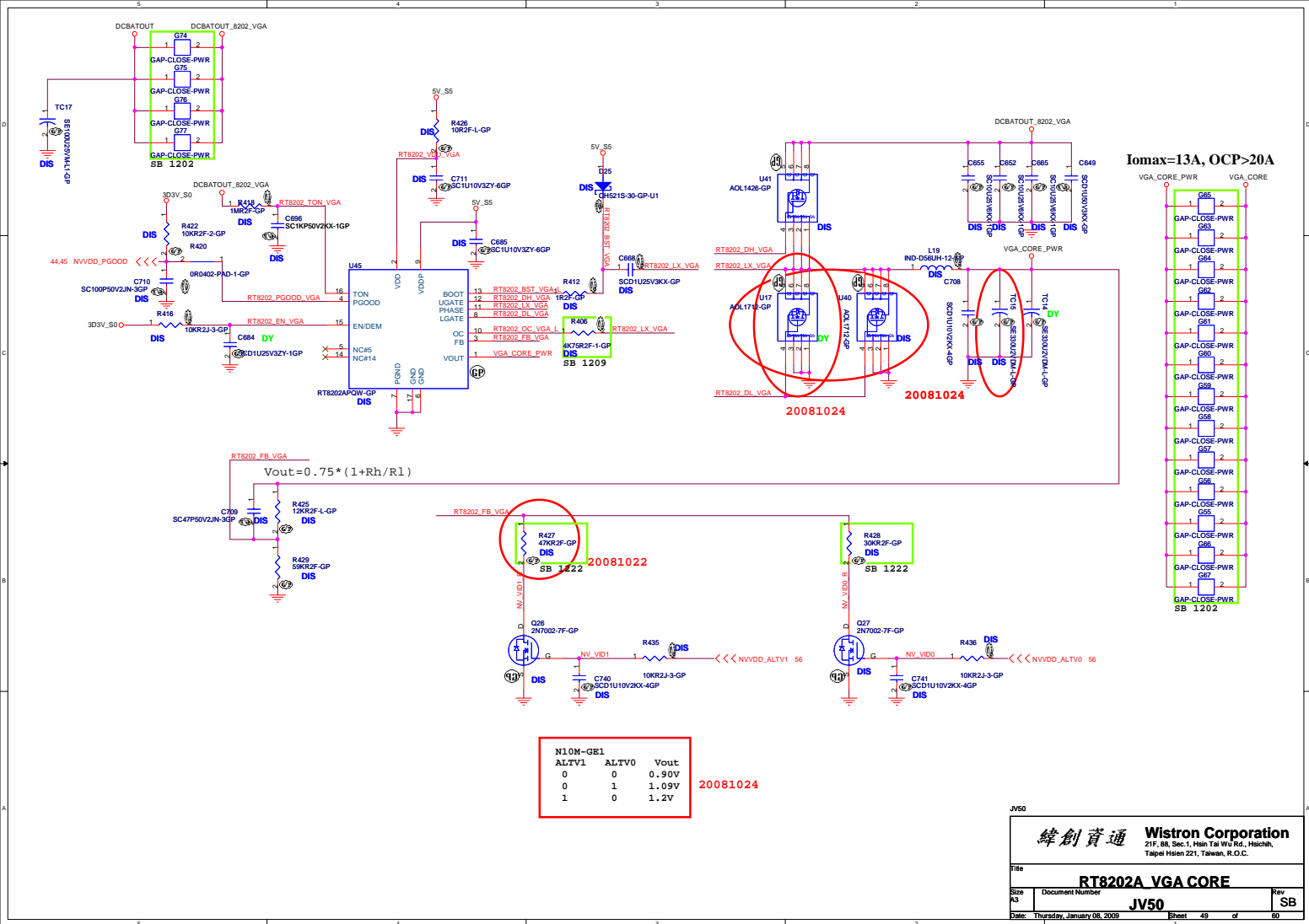
For AFTE

51 BATA_SDA_1 >>> BATA_SDA_1
51 BATA_SCL_1 >>> BATA_SCL_1
51 BAT_IN#_1 >>> BAT_IN#_1

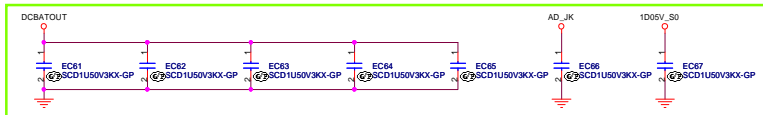
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

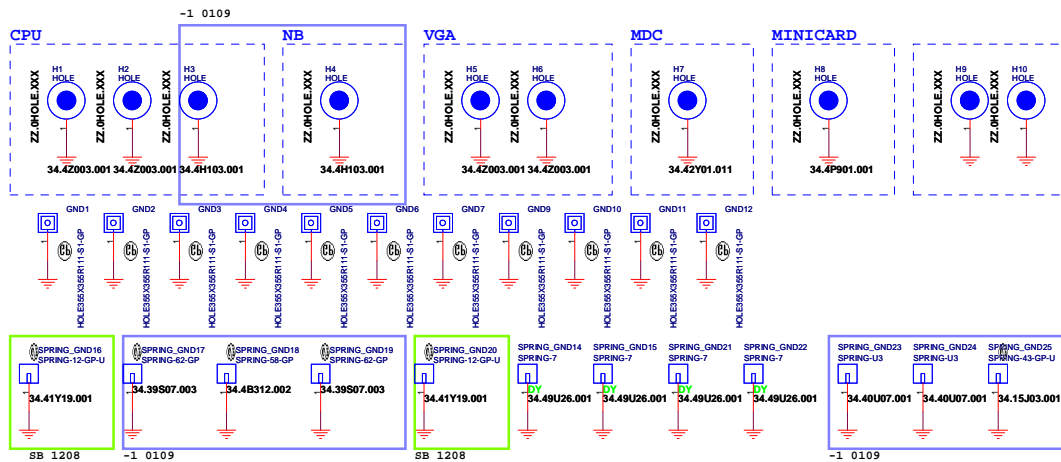
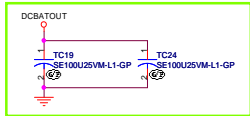
Title		
AD/BATT CONN		
Size	Document Number	Rev
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SB 1208



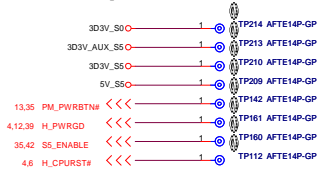
SB 1209



JV50

緯創資通		Wistron Corporation	
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taiwan 30001, Taiwan, R.O.C.			
File		EMI/Spring/Boss	
Size		Document Number	
Date: Friday, January 08, 2009		Rev	
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Check test point



Test Point放在Dimm Door打開可量測處

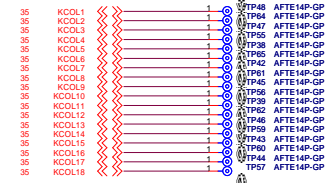
SPKR_L1 Conn. Test Point keep on connector side



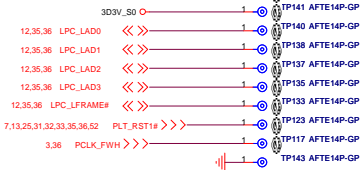
FAN1 Conn. Test Point keep on connector side



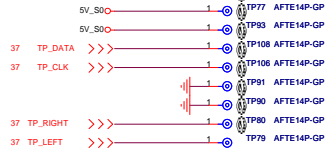
KB1 Conn. Test Point keep on connector side



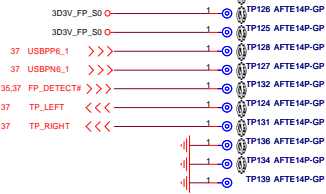
DB1 Conn. Test Point keep on connector side



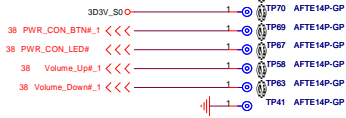
TPCN1 Conn. Test Point keep on connector side



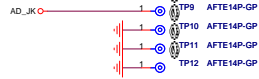
FPCN1 Conn. Test Point keep on connector side



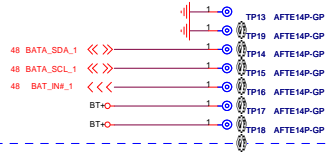
PSCN1 Conn. Test Point keep on connector side



DCIN1 Conn. Test Point keep on connector side

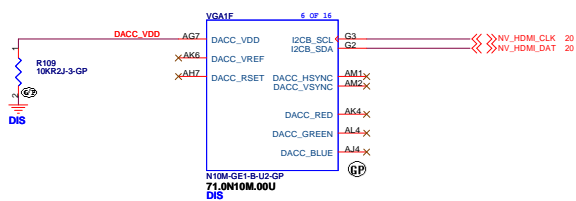
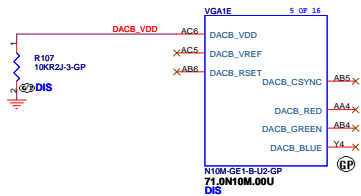
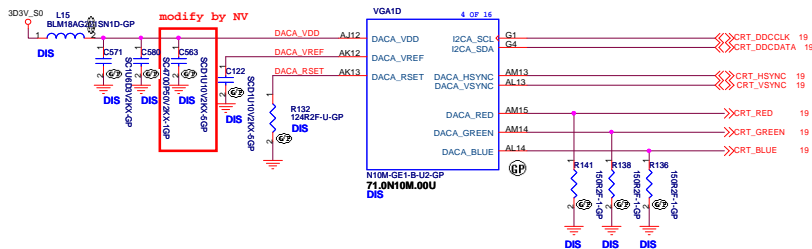


TPCN1 Conn. Test Point keep on connector side



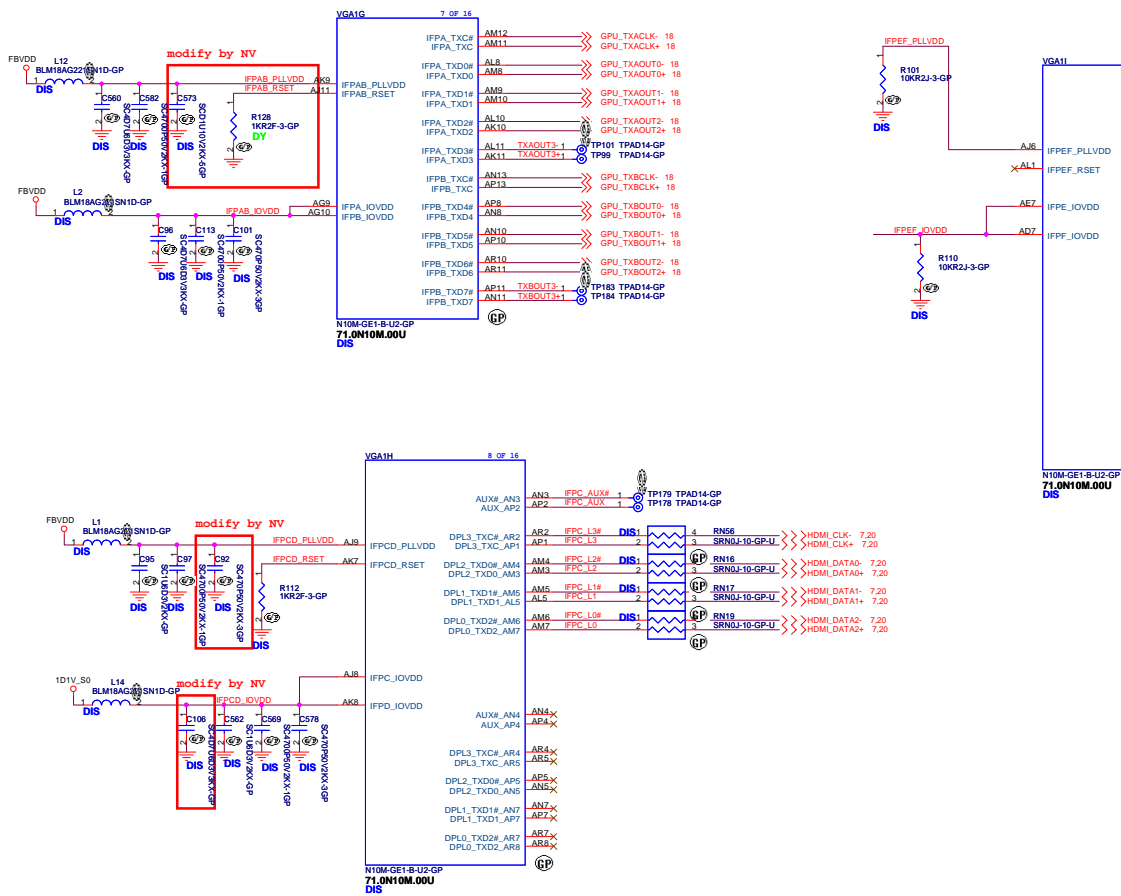
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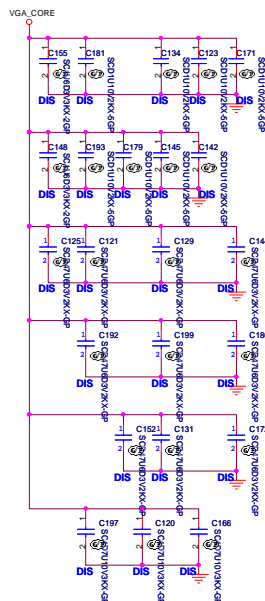
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.			
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
N10M(3/6) DAC			
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SB	SS	SC	-1
12/02	change C452 C453 from 27P to 33P by vendor's request		
Page33:	add C872 33P for SIV		
Page29:	change SPKR_R1 SPKR_L1 from 20.F1396.002 to 20.F1214.002 by CE's request		
Page18:	change LCD1 from 20.F1296.040 to 20.F1230.040 by CE's request		
Page24:	change USBCN1 from 20.F1290.015 to 20.F1035.015 by CE's request		
Page38:	change PSCN1 from 20.K0356.006 to 20.K0382.006 by CE's request		
Page18:	change AMIC1 from 20.F1396.002 to 20.F1214.002 by CE's request		
Page3:	add R554 and change U24 pin16 from 3D3V_S0 to 3D3V_VDD48_S0		
Page3:	change C457 C450 C416 C430 C418 from mount to DY and change C456 from DY to mount		
Page7:	change R192 R195 from 0ohm resistor to 0ohm pad and add R555 RN82 RN83 RN84 RN85 for reflection		
Page9:	change C275 from UMA to DY and change C349 from mount to DY		
Page10:	change C243 C758 from mount to DY and change R167 R398 from DIS to DY		
Page13:	change R216 from 0ohm resistor to 0ohm pad		
Page14:	change C413 C252 C703 C392 C707 C734 from mount to DY		
Page17:	change C426 C429 from mount to DY		
Page18:	change C7 C499 from mount to DY and change R1 from mount to DIS and change R3 from DY to UMA		
Page20:	add RN86 for DIS HDMI SMBus		
Page25:	change R45 from 0ohm resistor to 0ohm pad		
Page27:	change R523 from 0ohm resistor to 0ohm pad		
Page7:	add R556 pull-low DY for A1 NB		
Page28:	change AGND & GND and change R509 from 0ohm resistor to 0ohm pad		
Page38:	change C795 C790 C792 from mount to DY and change R480 R479 from 0ohm to 6K2 and 8K2		
Page28:	combine C801 C802 two 1u to C801 4.7u		
Page28:	delete C815 C814 C809 R500 R503 R513 R507 R502 R508 D31 U56 and change U55 to 84.2N702.E31		
Page28:	change R474 from DY to mount and change R475 from mount to DY for 10dB		
Page29:	add L29 L30 L31 L32 L33 L34 for ESD		
Page31:	change R463 R464 R471 R467 R466 R460 R459 R494 R484 R493 R486 R485 R488 R489 R490 R492 R491 R487 from 0ohm resistor to 0ohm pad		
Page32:	change C487 C477 from mount to DY and change R269 from 0ohm resistor to 0ohm pad		
Page12:	change C385 C386 from 10p to 7p by vendor's request		
Page35:	change C136 C169 from 15p to 7p by vendor's request		
Page33:	change R15 R29 R34 from 0ohm resistor to 0ohm pad and change C542 from mount to DY		
Page34:	change C42 from mount to DY		
Page35:	change C615 C626 C638 R395 from mount to DY and change R394 from DY to mount for PCB version		
Page36:	change DB1 from mount to DY		
Page38:	add Q35 PWR_LED7 PWR_LED8 and change RN4 from 4P2R to 8P4R and change PWR_LED5 PWR_LED6 from 83.01221.I70 to 83.00193.A70 for LED type		
Page39:	change U66 pin1 from CPUCORE_ON to 1D5V_PWRGD and change D13 pin1 from S5_ENABLE to 3V/5V_EN		
Page40:	update power sequence logic		
Page41:	change G43-G50 from open gap to close gap and change R328 R352 R353 R317 R316 R319-R325 from 0ohm resistor to 0ohm pad		
Page42:	change R532 R545 R552 from 0ohm resistor to 0ohm pad and change G118-G128 G130-G140 from open gap to close gap		
Page43:	change R246 R233 from 0ohm resistor to 0ohm pad and change G5-G16 G18-G33 from open gap to close gap		
Page43:	change R246 pin2 from CPUCORE_ON to 1D5V_PWRGD and add R500 pull-high 10K 3D3V_S5		
Page45:	change G100-G109 from open gap to close gap		
Page46:	change R157 R187 from 0ohm resistor to 0ohm pad and change G68-G73 G86 G87 G89 G90 G92 G93 G95 G96 G99 from open gap to close gap		
Page46:	delete TC19 and change TC20 from DY to GFX		
Page49:	change G55-G67 G74-G77 from open gap to close gap		
Page29:	change RN75 from 47ohm to 75ohm		
Page28:	change C804 C807 from 4.7u to 1u 25V X5R		
Page45:	delete TC24		
Page19:	delete R104 R129		
12/04	change U47 from 74.00545.A79 to 74.00547.A79		
Page20:	swap HDMI signals for routing		
Page28:	change U53 pin22 from AUD_HP1_EN to AMP_MUTE#_R		
Page48:	change BAT1 from 20.81094.007 to 20.81156.007		
Page22:	change ODD1 from 62.10065.541 to 62.10065.751		
Page22:	change R231 R247 from 0ohm resistor to 0ohm pad		
12/05	change R39 R53 R21 R31 R22 R35 R28 from 0ohm resistor to 0ohm pad		
Page46:	change L23 from 68.R8210.10V to 68.1R01A.20B and change U43 from 84.04812.A37 to 84.04168.037 by power team's request		
Page41:	change R344 from 2K87 to 3K16 and change C586 from 0.47u to 0.1u by power team's request		
Page41:	change U35 U39 from 84.01426.037 to 84.12003.A37 and change U6 U7 U36 U38 from 84.01712.037 to 84.57N03.A37 by power team's request		
Page45:	change R457 from 11K to 3K48 and change TC23 from 390u to 220u by power team's request		
12/08	change EC7 from DY to mount EMI's request		
Page48:	change EC28 EC30 EC31 EC32 from DY to mount EMI's request		
Page31:	change EC51 EC52 EC55 EC57 from 0.1u DY to 22p mount EMI's request		
Page5:	change C79 C80 from DY to mount EMI's request		
Page46:	change C659 from DY to GFX EMI's request		
Page50:	change SPRING_GND16-SPRING_GND20 from DY to mount EMI's request		
Page50:	add EC61-EC67 0.1u by EMI's request		
Page20:	change R313 R314 from 10K 100K to 18K 47K by NV's request		
Page35:	change U14 pin83 RN65 pin2 from SHBM to DBC_EN by annie's request		
Page18:	change LCD1 pin35 from NC to DBC_EN by annie's request		
Page20:	add ER1-ER8 0ohm pad by EMI's request		
Page10:	change C636 from 1000p DY to 27p mount by RF's request		
12/09	change R406 from 6K2 to 4K75 by power team's request		
Page46:	change TC16 from mount to GFX		
Page50:	add TC19 TC24 100u		
Page41:	change C528 C529 530 C588 C597 C604 from 10u to 4.7u and change C528 C588 from mount to DY		
Page46:	change C656 C653 from 10u to 4.7u and change C653 from GFX to DY		
Page42:	change C856 C857 C851 C850 from 10u to 4.7u and change C857 C850 from mount to DY		
Page41:	change TC5 from DY to mount		
Page5:	change C553 C538 C552 C539 C547 C536 C548 C537 from DY to mount		
Page17:	change C426 C428 C429 from 10u to 4.7u and change C429 from DY to mount		
Page16:	change C440-C442 C463-C465 from 10u to 4.7u and change C440 from DY to mount and change C464 from DY to mount		
Page20:	change HDMI from 62.10078.161 to 62.10078.171 by CE's request		
Page24:	change USBCN1 from 20.F1035.015 to 20.F1290.015 by CE's request		
12/10	add C873 33p GFX by RF's request		
Page43:	add C874 C875 33p by RF's request		
Page20:	swap U8 pin13 14 47 48		
Page33:	change R16 from DY to mount		
Page47:	change R292 from 0ohm resistor to 0ohm pad		
12/11	change MINI2 pin 51 from 5V_S5_MIN1 to 5V_S5_MIN2		
12/15	change VRAM strap R350		

AW

緯創資通

Wistron Corporation

237, 26, Sec. 1, Hsin-Tsu Rd., Hsinchu, Taipei 305, Taiwan, R.O.C.

Rev

Document Number

HISTORY

Rev

Document Number

JV50

SB

Date

Version

Rev

Rev

Rev

Rev

SB SB SC -1
12/22
Page49: change R427 from 30K 47K and R428 from 47K to 30K

SC
12/22
Page42: modify by power team's request
Page35: change R372 R395 from DY to mount and change R373 R394 from mount to DY

-1
01/06
Page17: change C400 from mount to DY and change C399 from DY to mount
Page30: change R267 from 39R to 0ohm pad
Page38: delete RN7 and add Q36 Q37
Page25: change U3 pin 38 52 from LAN_AVDD to TP and change U3 pin 68 from NC to TP
Page25: delete R58 and add RN87 and change U5 to 72.24C02.R01
Page3: change R255 from 22R to 33R and change RN42 from 0ohm to 33R
Page33: change R268 R275 R259 from 0ohm resistor to 0ohm pad
Page35: change R394 from DY to mount and change R395 from mount to DY
Page28: change R526 from 0ohm resistor to 0ohm pad
Page35: change R401 from 0ohm resistor to 0ohm pad
Page35: delete Q12 and add R502 R503
Page35: change RN23 pin 5 6 from 3D3V_AUX_S5 to 3D3V_S0
Page44: change U46 to APL5930 by power team's request
Page38: add 3G and BT option
Page28: change R479 from 8K2 to 10K and change R480 from 6K2 to 4K99 for audio speaker gain
Page28: merge C0D1 to LCD1

01/07
Page44: change R437 from 0ohm pad to 0ohm resistor
Page9: change TC18 from UMA to DY and change C276 from DY to mount
Page35: delete RN21 and add R507 10K DY
Page38: change RN4 to 330R and change RN8 to 100R and delete R10 and change RN3 to 8P4R 200R
Page47: change C515 to 78.15322.2FL by power team's request
Page3: mount 33p on EC23 EC24 EC25 EC39 EC48 for RF's request
Page3: add EC68 EC69 33p DY by RF's request
Page20: add R129 4K7 for different vendor

01/08
Page42: change R541 from 200K to 100K and change R544 location
Page42: change R532 R545 from 0ohm pad to 0ohm resistor

01/09
Page38: change name from 3G/ST_LED1 to 3GBT_LED1
Page50: add SPRING_GND23 34.40U07.001, SPRING_GND24 34.40U07.001, SPRING_GND25 34.15J03.001
Page50: SPRING_GND17, SPRING_GND19 change from 34.41Y19.001 to 34.39S07.003
Page50: SPRING_GND18 change from 34.41Y19.001 to 34.4B312.002