Winery13 CALPELLA DIS N11M-GE1 Schematics

uFCPGA Mobile Arrandale

Intel Ibex Peak-M

2010-01-13

REV : A00

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 1 of 88	

Winery CALPELLA Block Diagram

Project code : 91.4EX01.001
Part Number : 48.4EX01.001
PCB P/N : 09288
Revision : A00

PCB LAYER

L1: Top
L2: GND
L3: Signal
L4: Signal
L5: VCC
L6: Signal
L7: GND
L8: Bottom

Clock Generator SLG8SP585 7

Nvidia N11M-GE1(40nm) 80,81,82,83

VRAM(gDDR3) 64Mbx16x4 (512MB) 84,85

VRAM

100MHz/ 2.5Gbps

PCIe x 16

Bandwidth :8GB

LVDS

RGB CRT

Intel CPU Arrandale 8,9,10,11,12,13,14

DDRIII 1066 Channel A 800/1066MHz

DDRIII 1066 Slot 0 18

DDR III 1066 Channel B 800/1066MHz

DDRIII 1066 Slot 1 19

Power SW TPS2231R 34

New Card (FPC Cable to Connect) 34

PCIE x 1 & USB 2.0 x 1

CRT 55

LCD (Single Chanel) 54

Switchable 74

RGB CRT

LVDS

DMIx4 2.5 GT/s

FDI (UMA) 2.7 GT/s

100MHz 2.5Gbps PCIE

Intel PCH

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE

20,21,22,23,24,25,26,27,28

10/100/1000LOM RTL8111DL 35

PCIE x 1

RJ45 CONN

USB 2.0 x 2 PCIE x 1

Mini-Card WWAN/ WiMAX?

USB 2.0 x 1

Left Side: USB x 1

(On daughter board)

USB 2.0 480Mbps

USB 2.0 x 1 PCIE x 1

Mini-Card WLAN 802.11a/b/g/n 64

USB 2.0 x 1

Right Side: USB x 1 63

USB 2.0 x 1

Bluetooth 73

USB 2.0 x 1

Biometric 78

(3 in 1) SD/MMC/MMC+ 33

CardReader REALTEK RTS5138 32

USB 2.0 480Mbps

SM Bus 400KHz

Free fall sensor 40

LPC Bus 33MHz

73 CAMERA

USB2.0 x 1

Digital Mic Array

Azalia CODEC OP AMP IDT 92HD81UA 30

AZALIA 24MHz

MIC IN

HP OUT

1CH SPEAKER 60

SATA, USB

SATA 3Gbps

SPI

KBC NUVOTON NPCE781BA0DX 37

SPI

SM Bus

Thermal & Fan EMC2102 39,58

Capacity Board 78

Flash ROM 256kB 62

Touch PAD 68

Int. KB 68

USB,ESATA Multi-Port x1 63

ODD HDD 59

Flash ROM 4MB 62

CPU DC/DC ISL62883 47,48

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC RT8205B 46

INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

SYSTEM DC/DC TPS51116 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211 53

INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

SYSTEM DC/DC TPS51218 86

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

CHARGER BQ24745 45

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218 49

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

LDO APL5930 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

LDO RT9025 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

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Title: Block Diagram

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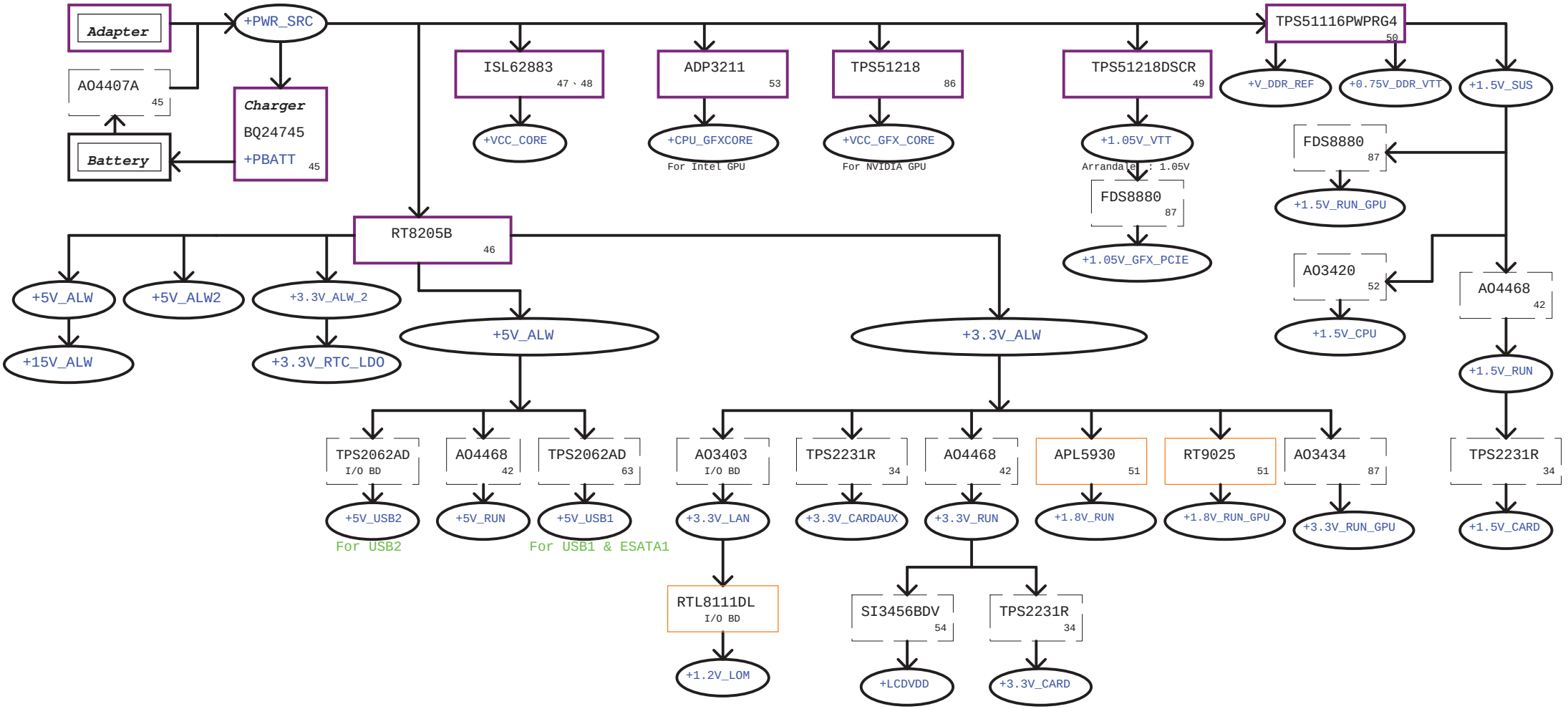

Power Shape

Regulator	LDO	Switch

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Title: **Power Block Diagram**

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

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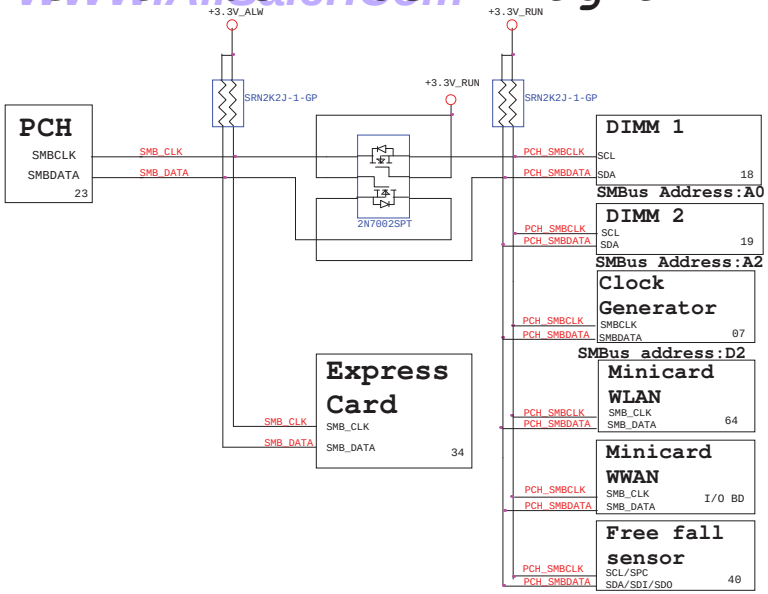
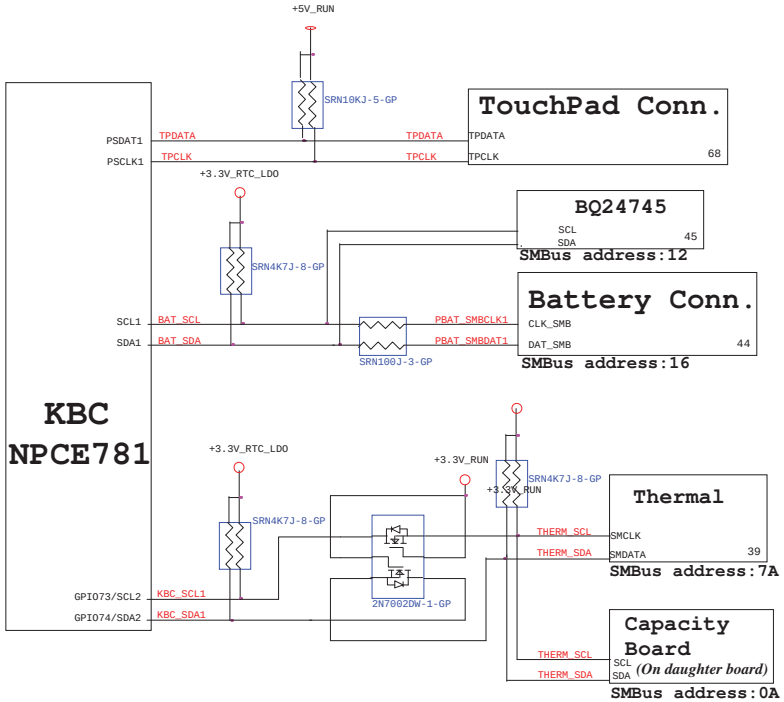
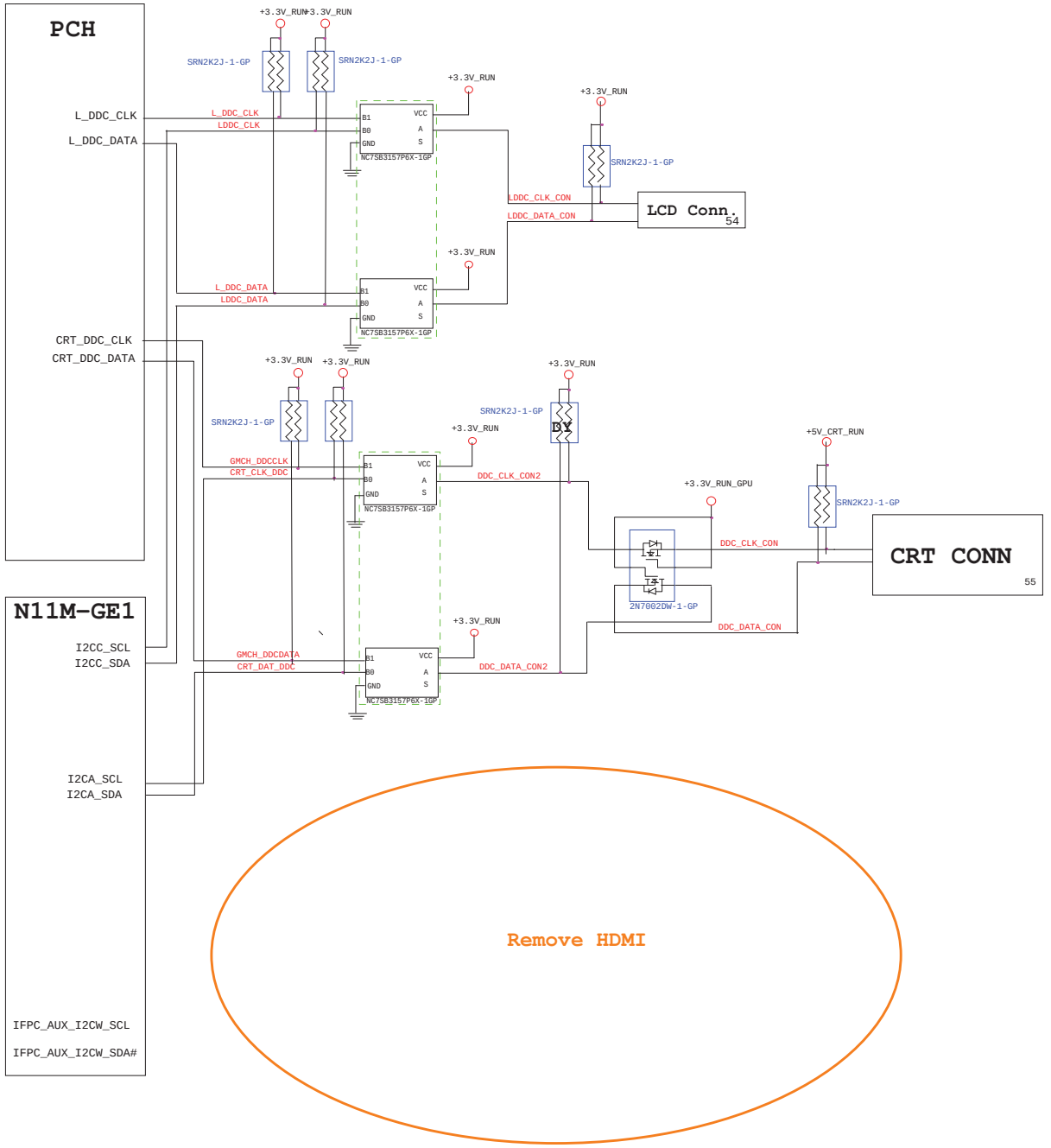
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Switchable Graphic SMBus Block Diagram



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Title: SMBUS Block Diagram

Size	Document Number	Rev
C	Winery13 MB DIS	A00

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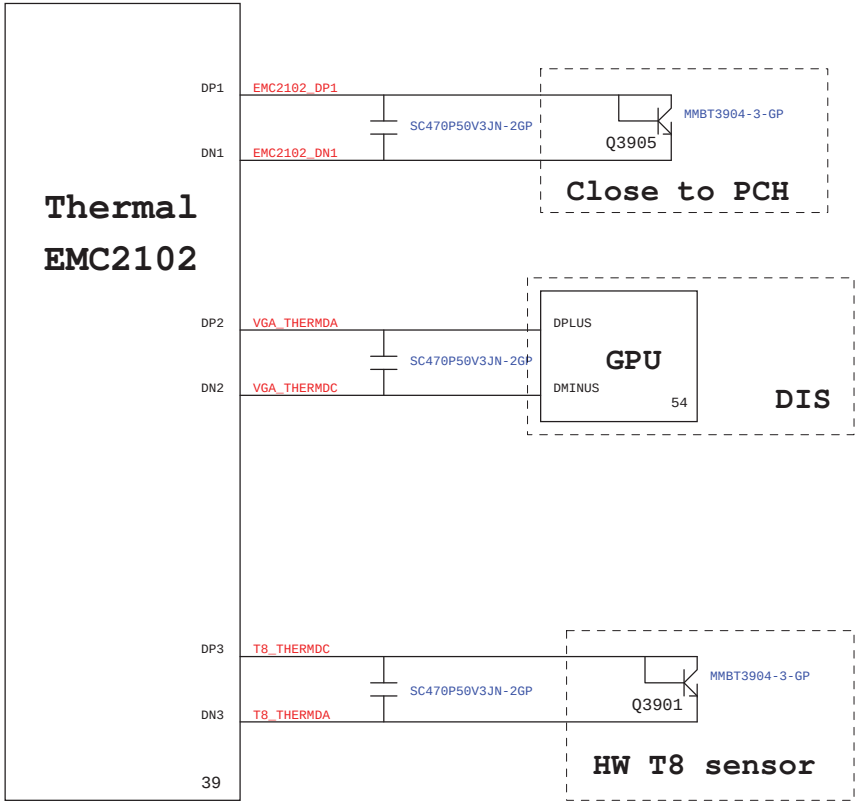
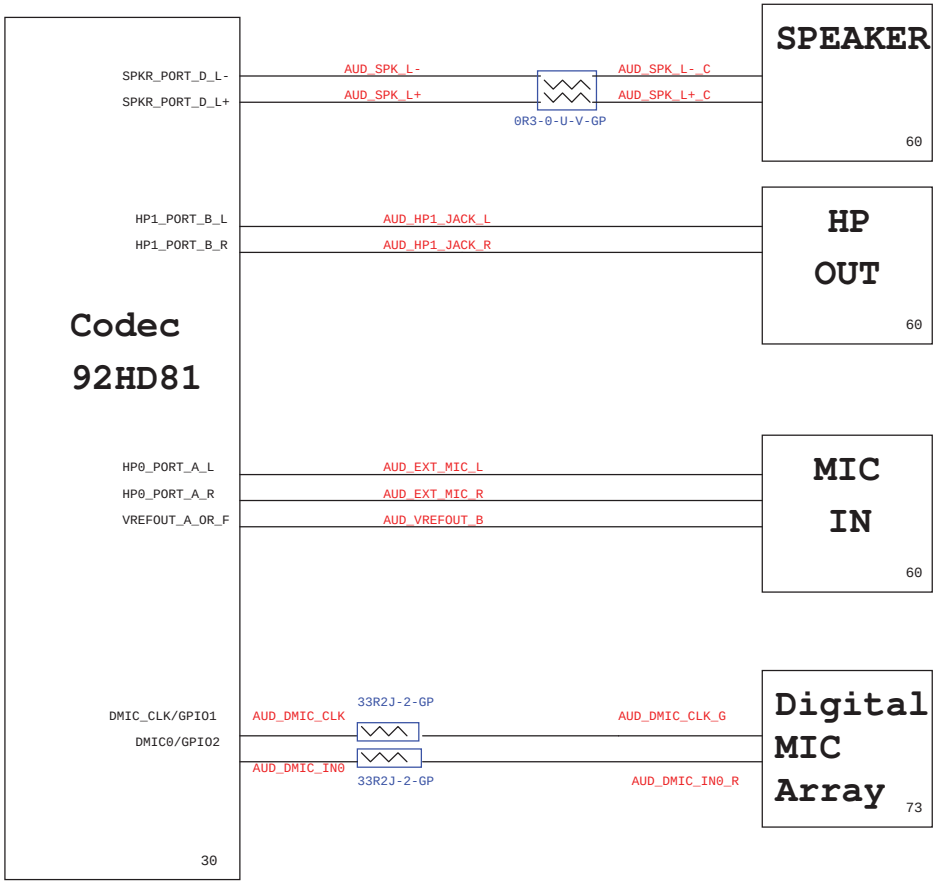
Thermal Block Diagram



Audio Block Diagram



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Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
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PCH Strapping

Calpella Schematic Checklist Rev1.6

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled** **Note:** CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	**Default (SPI):** Leave both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	**Enable Intel Anti-Theft Technology:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Intel Anti-Theft Technology:** Left floating, no pull-down required.
NV_ALE	**Enable Intel Anti-Theft Technology:** Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] **Disable Intel Anti-Theft Technology:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0)–** Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. **High (1)–:** Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. **Note:** CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	**Low (0)–** Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **High (1)–:** Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality **Note:** This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	**Default = Do not connect (floating). Internal pull-up.** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

USB Table

USB	
Pair	Device
0	USB1
1	USB for ESATA
2	USB2
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BlUETOOTH
9	Card Reader
10	Biometric
11	CAMERA
12	New Card
13	RESERVED

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Title: Table of Content

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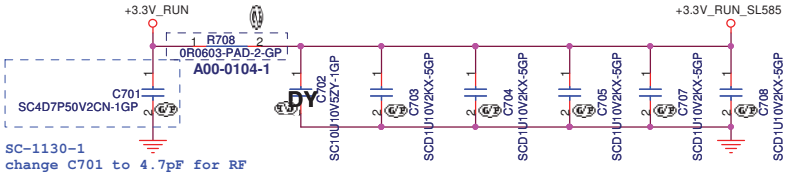
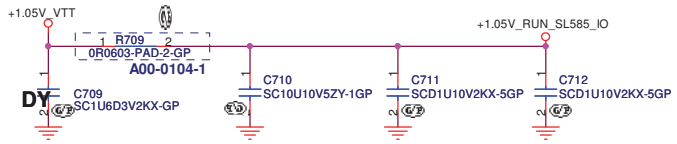
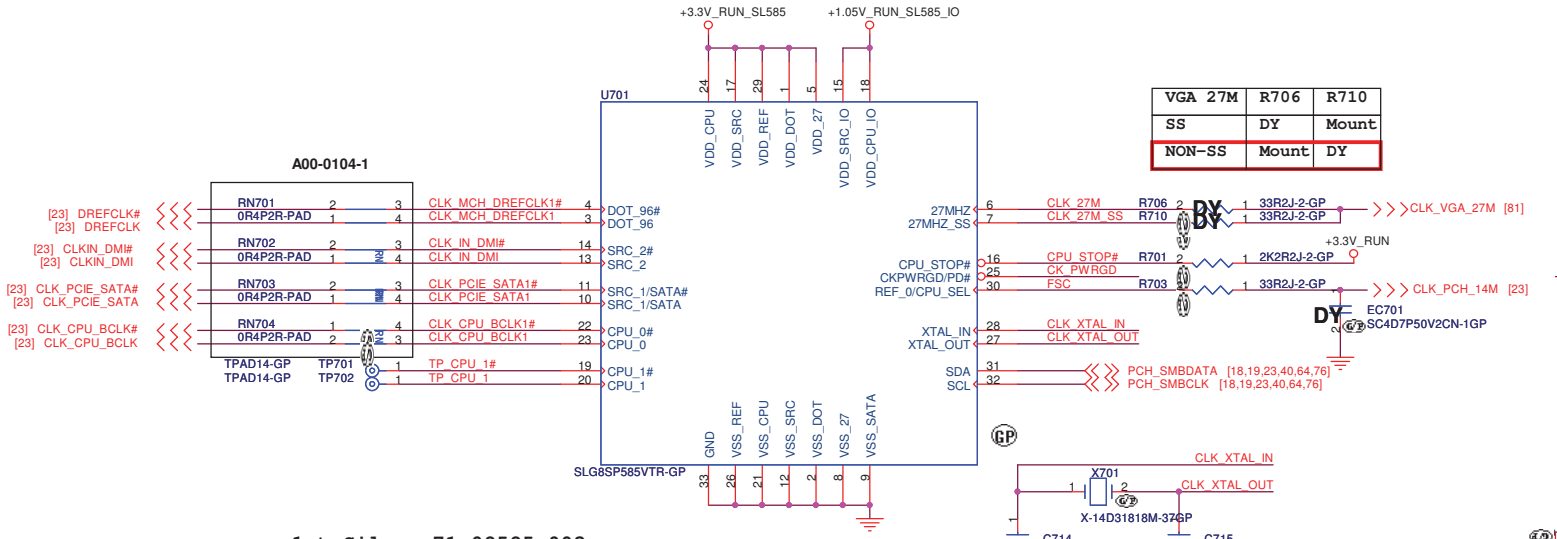
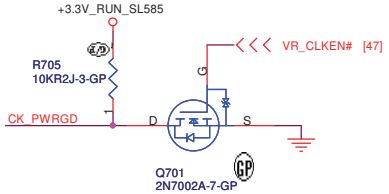
SSID = Clock GEN





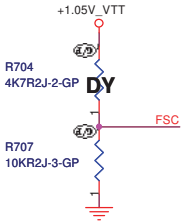


VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY



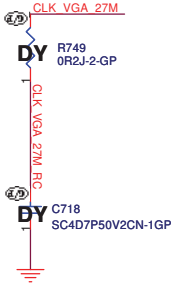
1ST: 84.2N702.E31
2ND: 84.2N702.D31

1st Silego 71.08585.003
2nd ICS 71.93197.003



1st: HARMONY 82.30005.901
2nd: ITTI 82.30005.C51
3rd: TXC 82.30005.B81

FSC	0	1
SPEED	133MHz (Default)	100MHz



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Title: Clock Generator SLG8SP585

Size | Document Number: Winery13 MB DIS | Rev: A00

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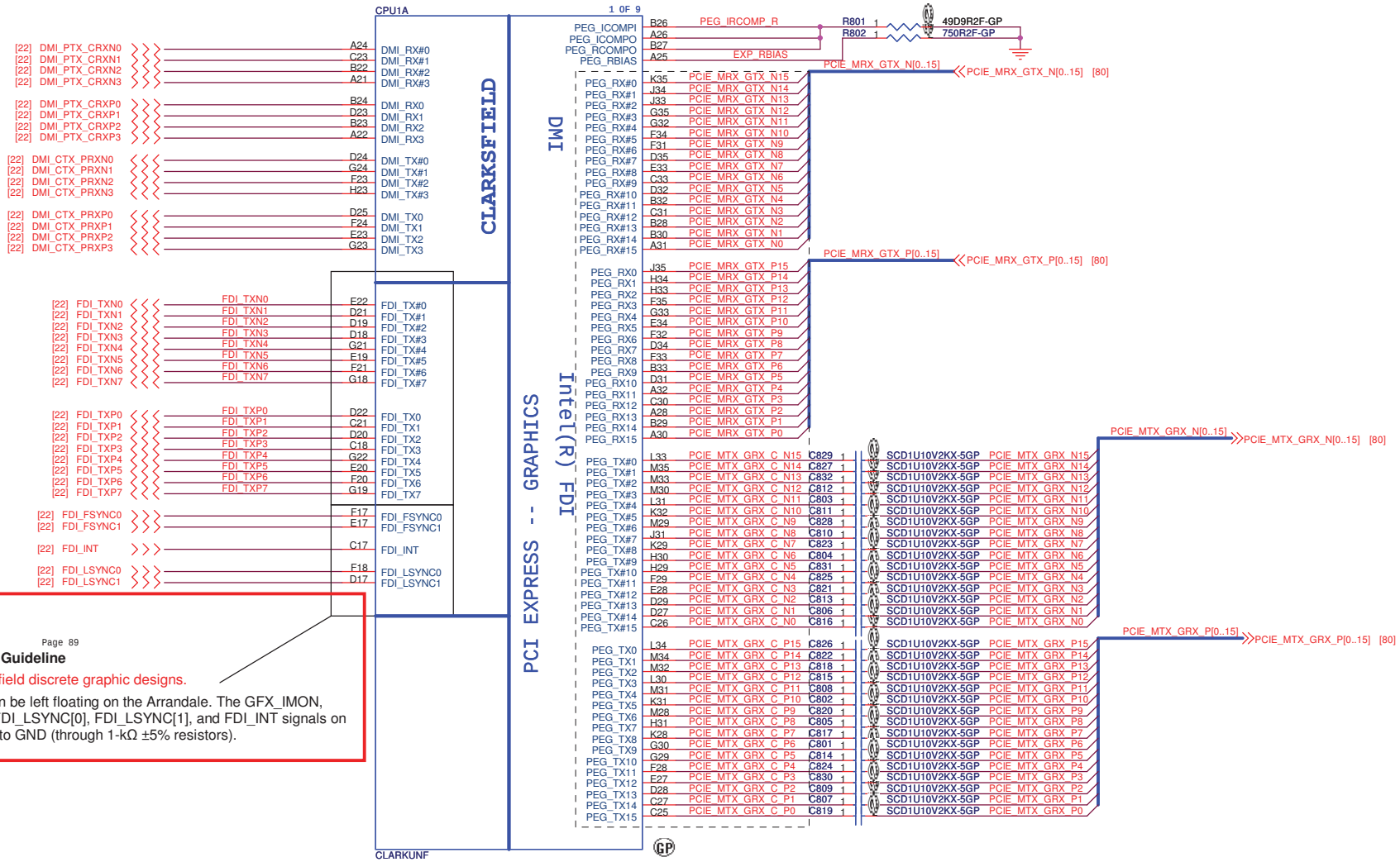
SSID = CPU



Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

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Title: CPU (PCIE/DMI/FDI)

Size | Document Number: Winery13 MB DIS | Rev: A00

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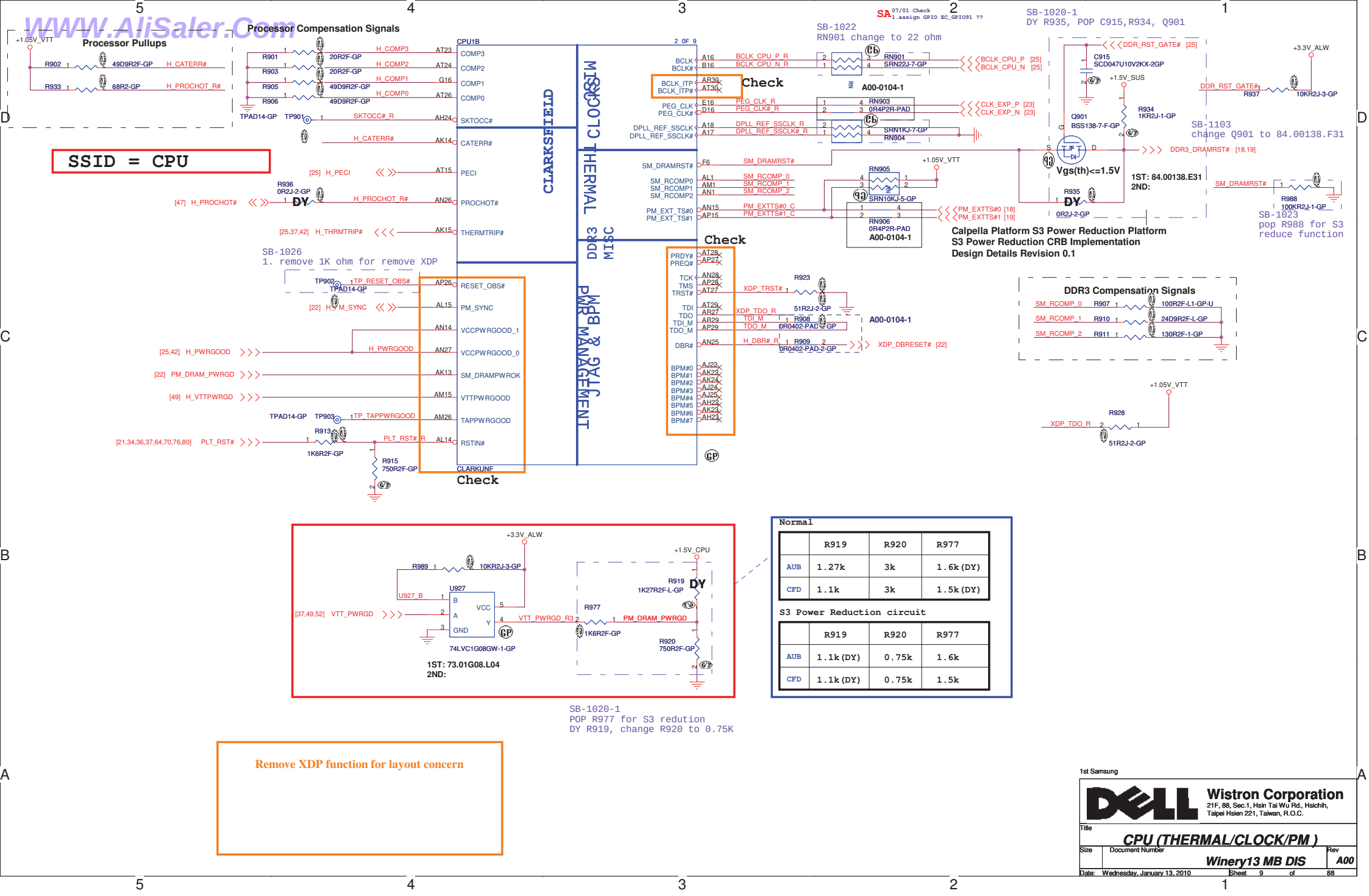

Normal

	R919	R920	R977
AUB	1.27k	3k	1.6k(DY)
CFD	1.1k	3k	1.5k(DY)

S3 Power Reduction circuit

	R919	R920	R977
AUB	1.1k(DY)	0.75k	1.6k
CFD	1.1k(DY)	0.75k	1.5k

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 9 of 88

SSID = CPU

CPU1C 3 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY A

CLARKUNF

CPU1D 4 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY - B

CLARKUNF

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Title: CPU (DDR)		
Size	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 10 of 88	

SSID = CPU

CFG0

R1101 3KR2F-GP

DY

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

DISABLE%

CFG3

R1102 3KR2F-GP

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

DW

07/10 Reversal
1.PCI-Express Static Lane Reversal

CFG4

R1103 3KR2F-GP

DY

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

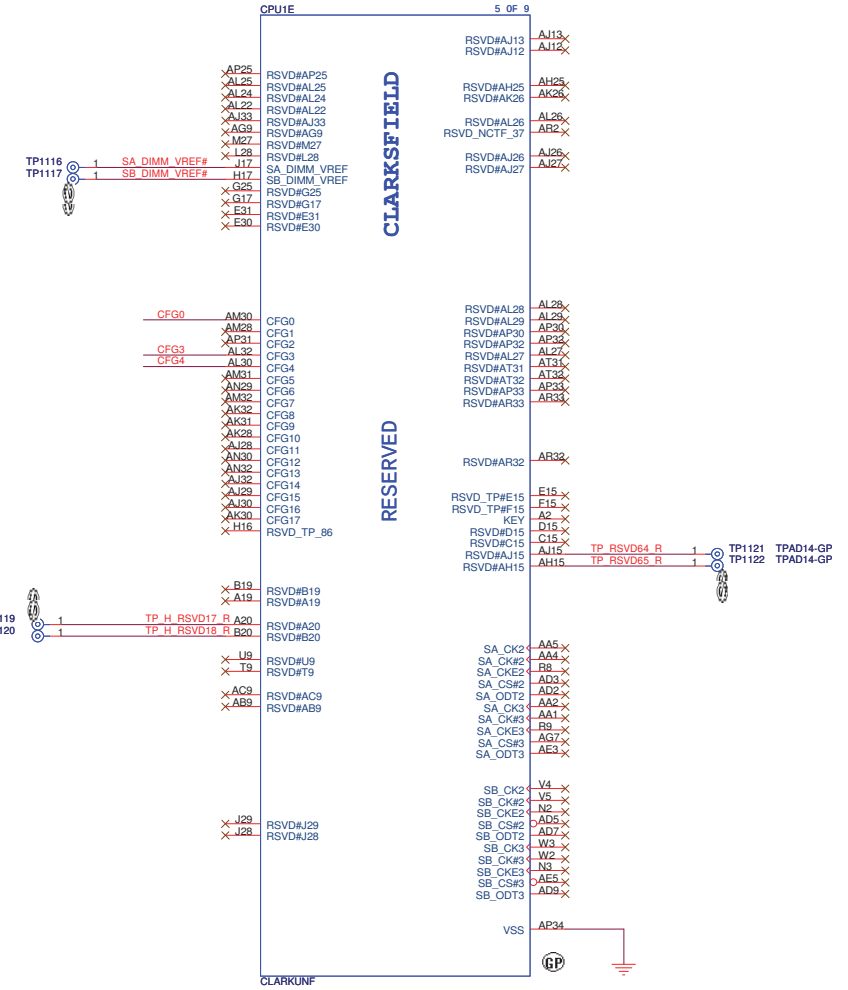
Page 482,486

DW

07/02 Added
1.Added display Switchable strap commentariat

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

DW30 Only support Arrandale, CFG7 no need pull down



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Title: CPU (RESERVED)

Size | Document Number: Winery13 MB DIS | Rev: A00

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SSID = CPU

PROCESSOR CORE POWER

48A (Arburdale)

18A

+VCC_CORE

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

CLARKUNF

POWER

CPU VIDS

SENSE LINES

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SA

07/01 Check
1.DPRSLPVR ??

SC-1207-1
pop C1243 and change size to 0603 for EMI

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Title: CPU (VCC_CORE)

Size | Document Number: Winery13 MB DIS | Rev: A00

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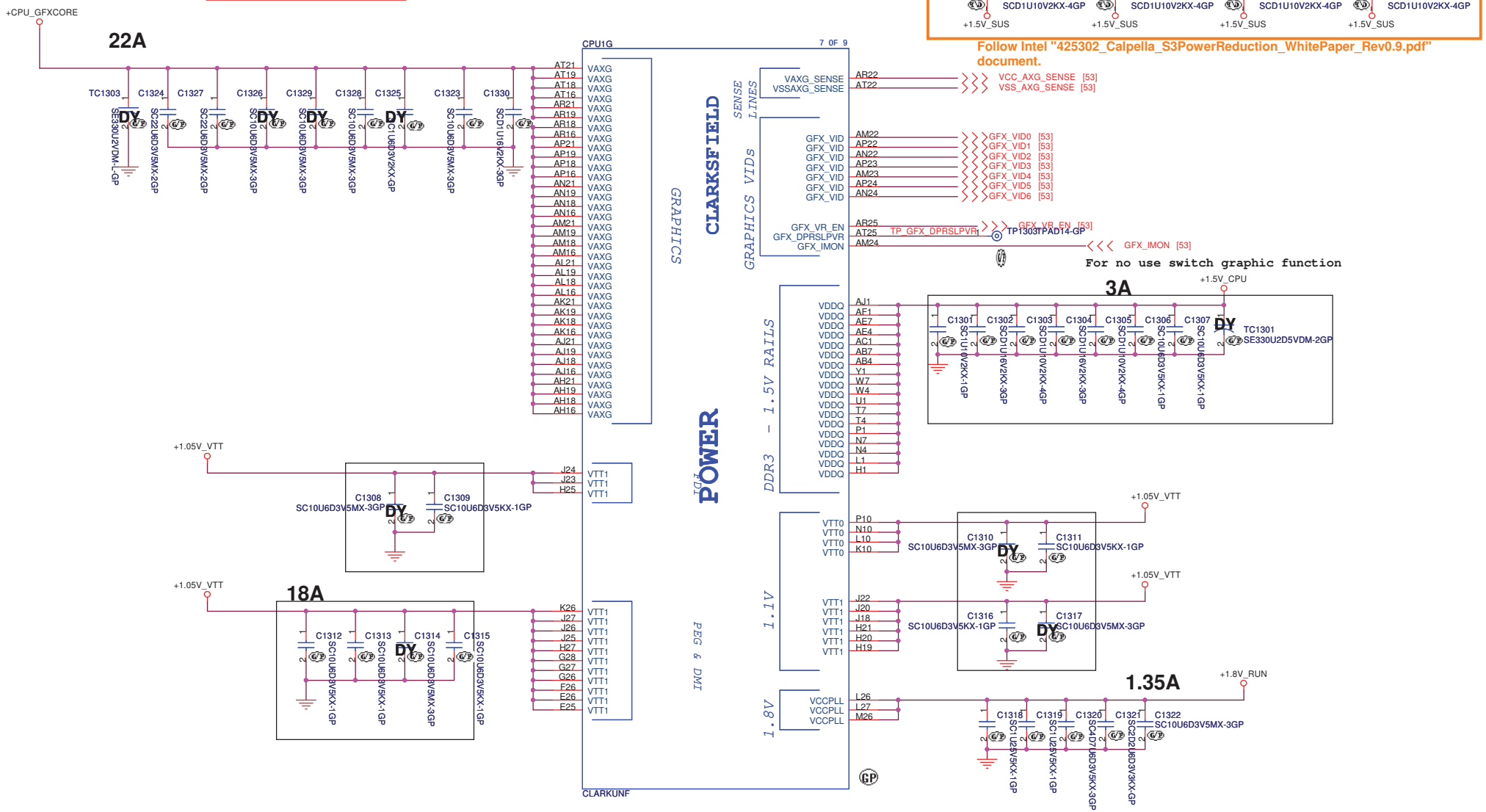
SSID = CPU



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Title	CPU (VCC_GFXCORE)	
Size	Document Number: Winery13 MB DIS	Rev: A00
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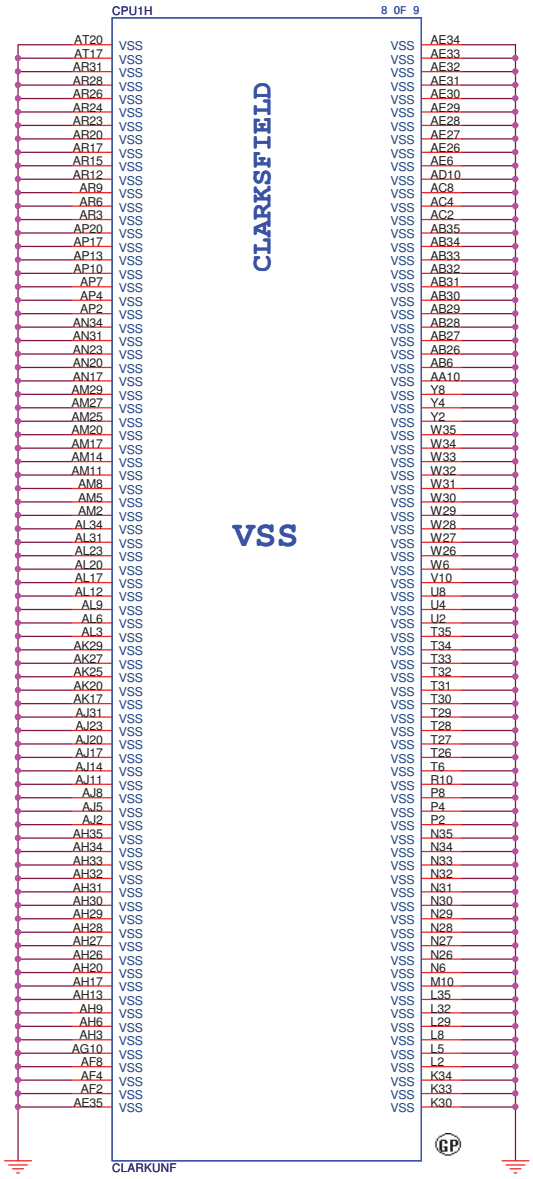
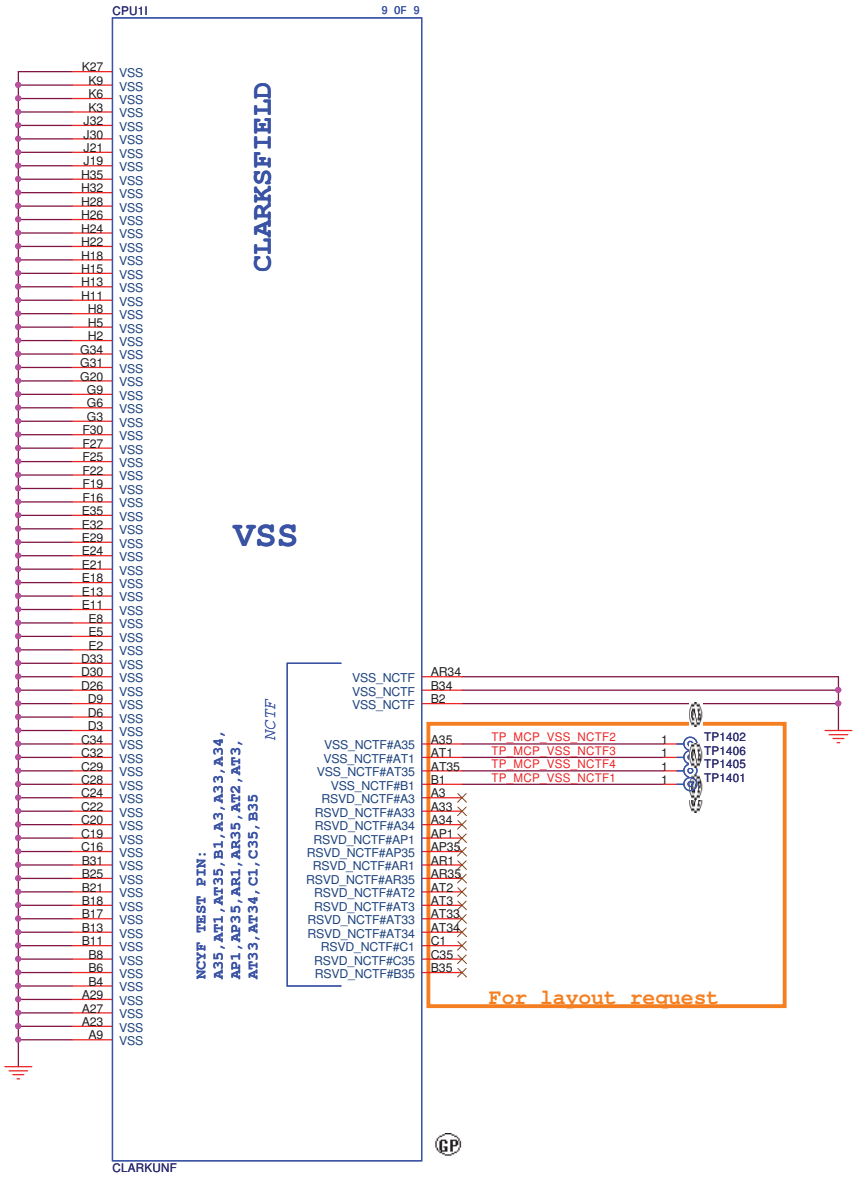
SSID = CPU





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Title: *Reserved*

Size	Document Number	Rev
A3	*Winery13 MB DIS*	*A00*

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A3	*Winery13 MB DIS*	*A00*

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Title

(Reserve)

Size	Document Number	Rev
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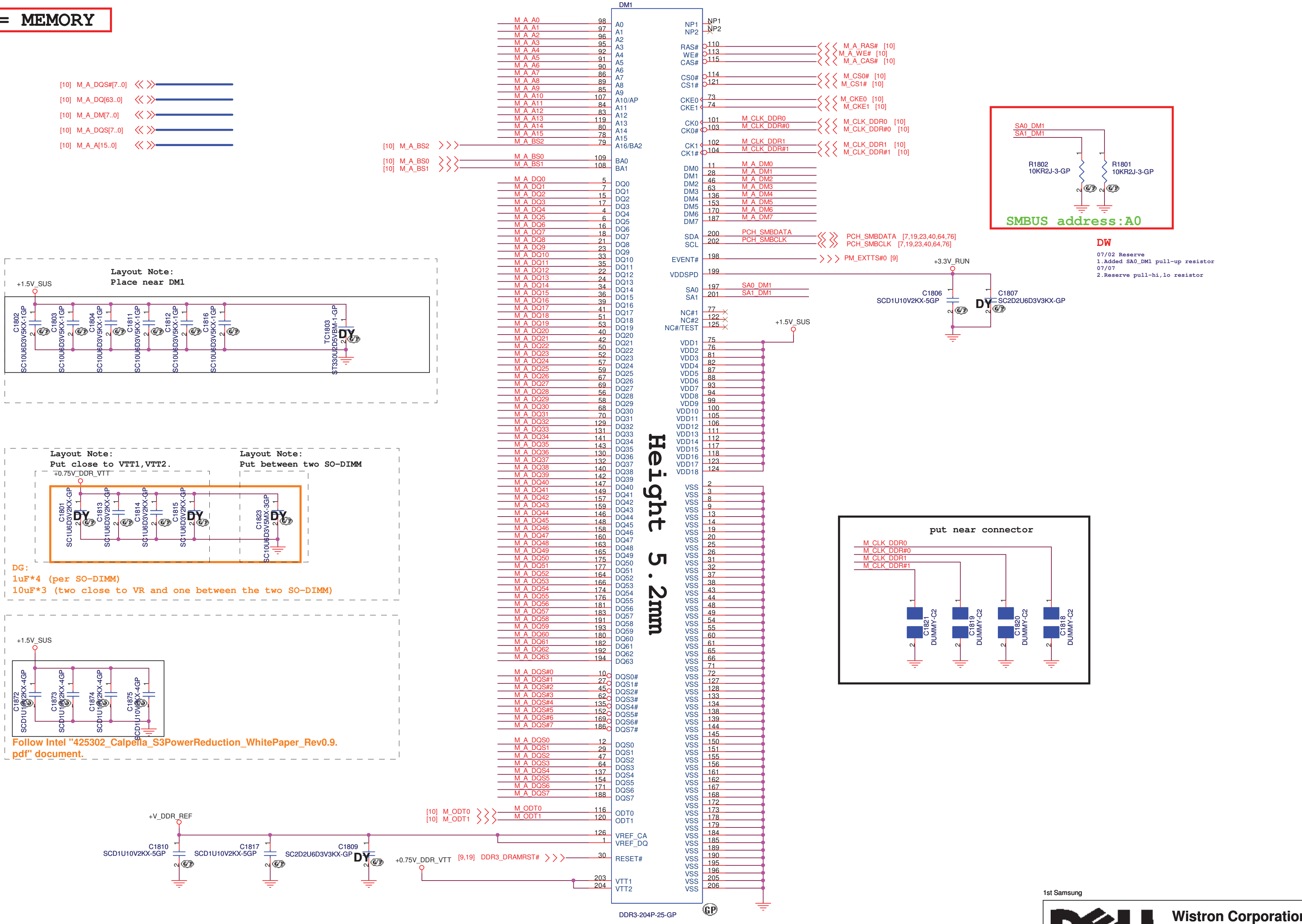
SSID = MEMORY


DM1
DDR3-204P-25-GP
Height 5.2mm
[10] M_A_DQS#[7..0]
[10] M_A_DQ[63..0]
[10] M_A_DM[7..0]
[10] M_A_DQS[7..0]
[10] M_A_A[15..0]
[10] M_A_BS2
[10] M_A_BS0
[10] M_A_BS1
M_A_A0 … M_A_A15, M_A_BS2, M_A_BS0, M_A_BS1
M_A_DQ0 … M_A_DQ63
M_A_DQS#0 … M_A_DQS#7
M_A_DQS0 … M_A_DQS7
[10] M_ODT0
[10] M_ODT1
M_A_RAS# [10]
M_A_WE# [10]
M_A_CAS# [10]
M_CS0# [10]
M_CS1# [10]
M_CKE0 [10]
M_CKE1 [10]
M_CLK_DDR0 [10]
M_CLK_DDR#0 [10]
M_CLK_DDR1 [10]
M_CLK_DDR#1 [10]
M_A_DM0 … M_A_DM7
PCH_SMBDATA [7,19,23,40,64,76]
PCH_SMBCLK [7,19,23,40,64,76]
PM_EXTTS#0 [9]
SA0_DM1
SA1_DM1
+3.3V_RUN
C1806 SCD1U10V2KX-5GP
C1807 SC2D2U6D3V3KX-GP
DY
+1.5V_SUS
+V_DDR_REF
C1810 SCD1U10V2KX-5GP
C1817 SCD1U10V2KX-5GP
C1809 SC2D2U6D3V3KX-GP
+0.75V_DDR_VTT
[9,19] DDR3_DRAMRST#
R1802 10KR2J-3-GP
R1801 10KR2J-3-GP
SMBUS address:A0
Layout Note:
Place near DM1
C1802 SC10U6D3V5KX-1GP
C1803 SC10U6D3V5KX-1GP
C1804 SC10U6D3V5KX-1GP
C1811 SC10U6D3V5KX-1GP
C1812 SC10U6D3V5KX-1GP
C1816 SC10U6D3V5KX-1GP
TC1803 ST330U2D5VBM-1-GP
Layout Note:
Put close to VTT1,VTT2.
Layout Note:
Put between two SO-DIMM
+0.75V_DDR_VTT
C1801 SC1U6D3V2KX-GP
C1813 SC1U6D3V2KX-GP
C1814 SC1U6D3V2KX-GP
C1815 SC1U6D3V2KX-GP
C1823 SC10U6D3V5MX-3GP
C1872 SCD1U10V2KX-4GP
C1873 SCD1U10V2KX-4GP
C1874 SCD1U10V2KX-4GP
C1875 SCD1U10V2KX-4GP
put near connector
C1821 DUMMY-C2
C1819 DUMMY-C2
C1820 DUMMY-C2
C1818 DUMMY-C2

DW
07/02 Reserve
1.Added SA0_DM1 pull-up resistor
07/07
2.Reserve pull-hi,lo resistor

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

1st Samsung

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Taipei Hsien 221, Taiwan, R.O.C.

Title	DDRIII-SODIMM SLOT1	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 18 of 88	

SSID = MEMORY

Change CONN
2009/06/01

[10] M_B_DQS#[7..0]
[10] M_B_DQ[63..0]
[10] M_B_DM[7..0]
[10] M_B_DQS[7..0]
[10] M_B_A[15..0]

DM2

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15
[10] M_B_BS2 M_B_BS2 79 A16/BA2
[10] M_B_BS0 M_B_BS0 109 BA0
[10] M_B_BS1 M_B_BS1 108 BA1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
M_B_DQ23 52 DQ23
M_B_DQ24 57 DQ24
M_B_DQ25 59 DQ25
M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
M_B_DQ32 129 DQ32
M_B_DQ33 131 DQ33
M_B_DQ34 141 DQ34
M_B_DQ35 143 DQ35
M_B_DQ36 130 DQ36
M_B_DQ37 132 DQ37
M_B_DQ38 140 DQ38
M_B_DQ39 142 DQ39
M_B_DQ40 147 DQ40
M_B_DQ41 149 DQ41
M_B_DQ42 157 DQ42
M_B_DQ43 159 DQ43
M_B_DQ44 146 DQ44
M_B_DQ45 148 DQ45
M_B_DQ46 158 DQ46
M_B_DQ47 160 DQ47
M_B_DQ48 163 DQ48
M_B_DQ49 165 DQ49
M_B_DQ50 175 DQ50
M_B_DQ51 177 DQ51
M_B_DQ52 164 DQ52
M_B_DQ53 166 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 181 DQ56
M_B_DQ57 183 DQ57
M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

M_B_DQS#0 10 DQS0#
M_B_DQS#1 27 DQS1#
M_B_DQS#2 45 DQS2#
M_B_DQS#3 62 DQS3#
M_B_DQS#4 135 DQS4#
M_B_DQS#5 152 DQS5#
M_B_DQS#6 169 DQS6#
M_B_DQS#7 186 DQS7#

M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

[10] M_ODT2 M_ODT2 116 ODT0
[10] M_ODT3 M_ODT3 120 ODT1

126 VREF_CA
1 VREF_DQ
[9,18] DDR3_DRAMRST# 30 RESET#

203 VTT1
204 VTT2

NP1 NP1
NP2 NP2

RAS# 110
WE# 113
CAS# 115
M_B_RAS# [10]
M_B_WE# [10]
M_B_CAS# [10]

CS0# 114
CS1# 121
M_CS2# [10]
M_CS3# [10]

CKE0 73
CKE1 74
M_CKE2 [10]
M_CKE3 [10]

CK0 101 M_CLK_DDR2
CK0# 103 M_CLK_DDR#2
M_CLK_DDR2 [10]
M_CLK_DDR#2 [10]

CK1 102 M_CLK_DDR3
CK1# 104 M_CLK_DDR#3
M_CLK_DDR3 [10]
M_CLK_DDR#3 [10]

DM0 11 M_B_DM0
DM1 28 M_B_DM1
DM2 46 M_B_DM2
DM3 63 M_B_DM3
DM4 136 M_B_DM4
DM5 153 M_B_DM5
DM6 170 M_B_DM6
DM7 187 M_B_DM7

SDA 200 PCH_SMBDATA
SCL 202 PCH_SMBCLK
PCH_SMBDATA [7,18,23,40,64,76]
PCH_SMBCLK [7,18,23,40,64,76]

EVENT# 198 PM_EXTTS#1 [9]

VDDSPD 199

SA0 197 SA0_DM2
SA1 201 SA1_DM2

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206

Height 9.2mm

DDR3-204P-24-GP

+1.5V_SUS
+0.75V_DDR_VTT
+V_DDR_REF
+3.3V_RUN

C1907 SCD1U10V2KX-5GP
C1910 SCD1U10V2KX-5GP
C1914 SC2D2U6D3V3KX-GP DY
C1906 SCD1U10V2KX-5GP
C1921 SC2D2U6D3V3KX-GP DY

+3.3V_RUN
R1903 10KR2J-3-GP DY
R1904 10KR2J-3-GP
EC1901 SCD1U25V3KX-GP DY
SA1_DM2
SA0_DM2
R1901 10KR2J-3-GP
R1902 10KR2J-3-GP DY

SMBUS address:A4

Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

Layout Note:
Place near DM2

+1.5V_SUS
C1905 SC10U6D3V5KX-1GP
C1911 SC10U6D3V5KX-1GP
C1913 SC10U6D3V5KX-1GP
C1916 SC1U6D3V5MX-3GP
C1919 SC10U6D3V5KX-1GP
C1920 SC10U6D3V5KX-1GP
TC1903 ST330U2D5VBM-1-GP DY

Layout Note:
Put close to VTT1,VTT2.

+0.75V_DDR_VTT
C1908 SC1U6D3V2KX-GP
C1917 SC1U6D3V2KX-GP
C1918 SC1U6D3V2KX-GP DY
C1909 SC1U6D3V2KX-GP DY

DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)

+1.5V_SUS
C1976 SCD1U10V2KX-4GP
C1977 SCD1U10V2KX-4GP
C1978 SCD1U10V2KX-4GP
C1979 SCD1U10V2KX-4GP

Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.

put near connector

M_CLK_DDR2
M_CLK_DDR#2
M_CLK_DDR3
M_CLK_DDR#3
C1901 DUMMY-C2
C1904 DUMMY-C2
C1902 DUMMY-C2
C1903 DUMMY-C2

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Title: DDRIII-SODIMM SLOT2
Size: Custom
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
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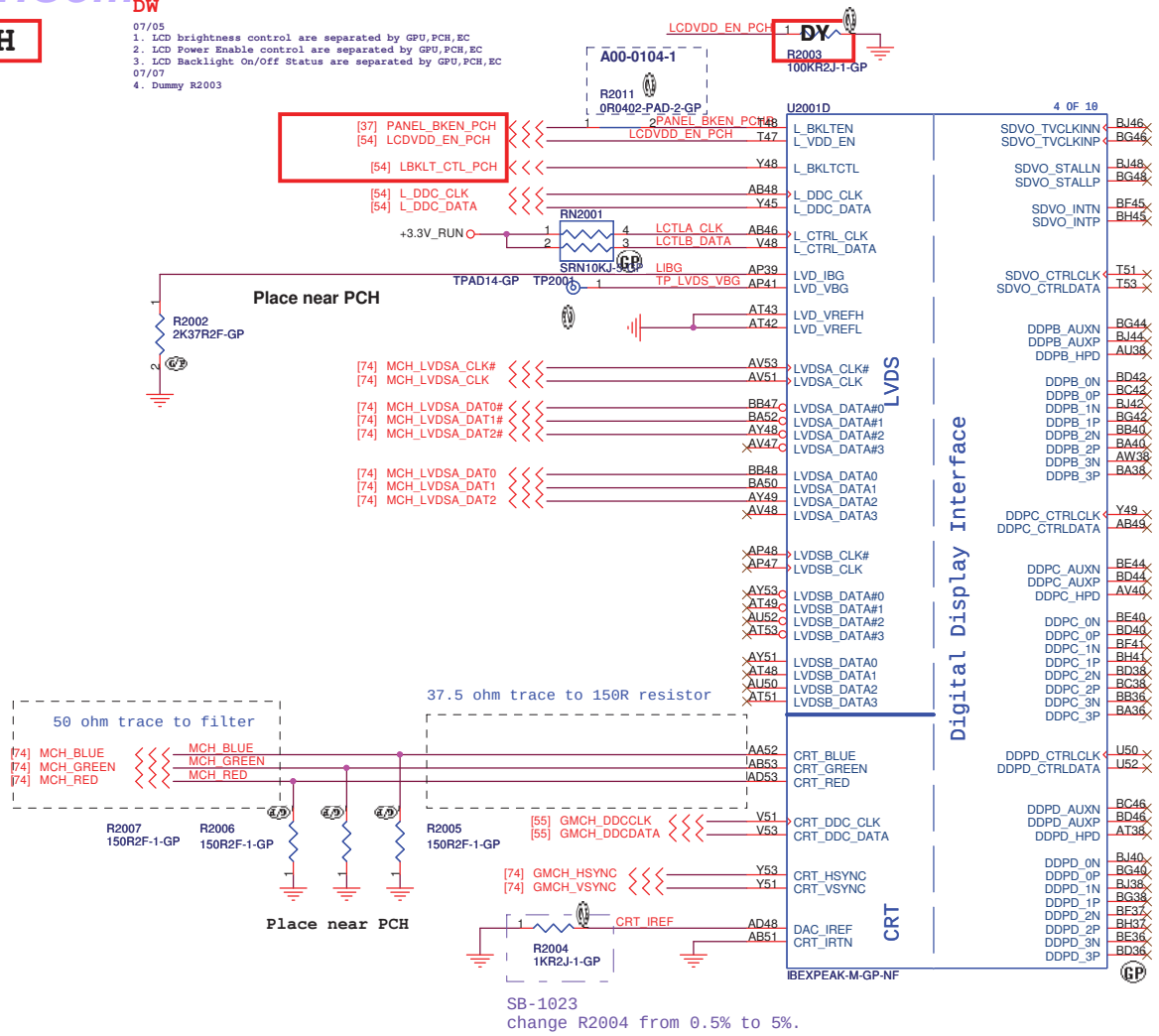
SSID = PCH

DW

07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/07
4. Dummy R2003



SB-1023
change R2004 from 0.5% to 5%.

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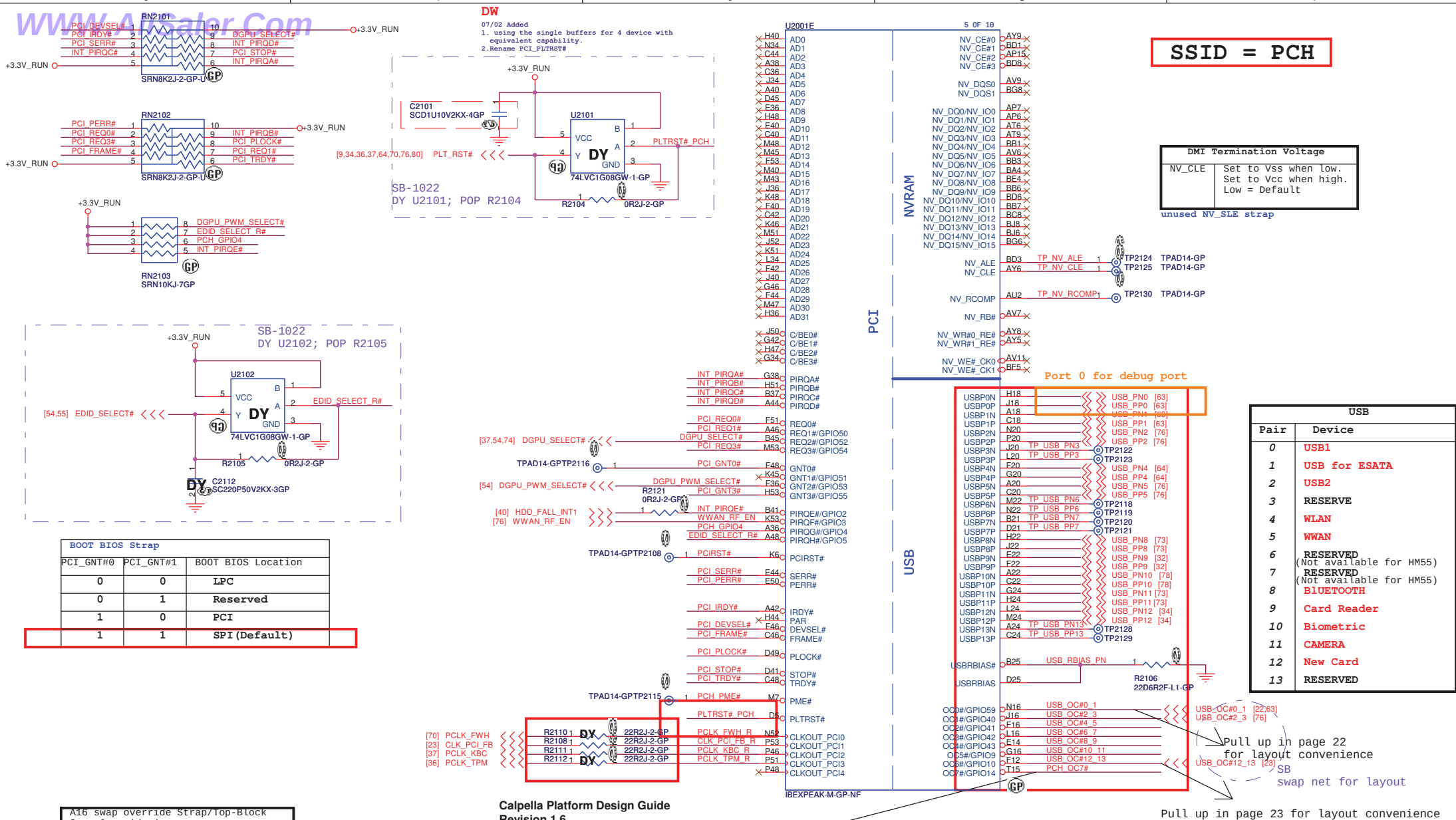
Title: PCH (LVDS/CRT/DDI)

Size | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 20 of 88



Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.

1st Samsung

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Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010 Sheet 21 of 88

SSID = PCH

U2001C

3 OF 10

DMI

FDI

System Power Management

IBEXPEAK-M-GP-NF

Remove XDP pull-up ?

Option to " Disable " clkrun.
Pulling it down will keep the clks running.

Close to PCH

Pull up in page 23 for layout convenience

SB-31

1st Samsung

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Title: PCH (DM I/FDI/PM)

Size | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 22 of 88

SSID = PCH

U2001B

2 OF 10

PCI-E*

WLAN

LAN

WWAN

New Card

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

Remove XDP pull-up

SB-1020

SB-1020

1ST: 84.DMN66.03F
2ND: 84.27002.F3F

1ST: 84.2N702.E31
2ND: 84.2N702.D31

un-stuff 25M X'tal without HDMI/eDP/DP

SC-1125-1
C2313 pop 0 ohm if no use 25MHz XTAL

SB-1104
pop for 25MHz

Pull up in page 21 for layout convenience

1ST: 84.03904.H11
2ND: 84.03904.L06

SB
swap net for layout

SB-1026
swap net for layout

SB-1023
RN2308 change to 2*1 size

SB-1020
move EDID_SELECT# from GPIO66 to GPIO5

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 23 of 88

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

SB-18

1st: EPSON 82.30001.861
2nd: QUARTECH 82.30001.A81
3rd: KDS 82.30001.691

DW
07/23 Added
1.Added "ME in Manufacturing Mode" strap
2.Added CardReader_Wake# to sent Card detect signal for PCH . (Only For JMB380)

Flash Descriptor Security Override/ ME Debug Mode	
ME_UNLOCK#	This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SB-1026
1. remove R2411 pull high INT_SERIRQ to RN2501.1

DW
07/02 Change
1.Change R2410 to dummy

SC-1208-1
change R2413,R2414,R2415 from 15ohm to 0 ohm

DW
07/10 assign GPIO
1.assign GPIO GPIO_DSM,Felic_DETECT#

IBEXPEAK-M-GP-NF

1st Samsung

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)
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SSID = PCH

U2001F

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BMBUSY#/GPIO0
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
SATA4GP/GPIO16
TACH0/GPIO17
SCLOCK/GPIO22
GPIO24
GPIO27
GPIO28
STP_PCI#/GPIO34
SATACLKREQ#/GPIO35
SATA2GP/GPIO36
SATA3GP/GPIO37
SLOAD/GPIO38
SDATAOUT0/GPIO39
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
SDATAOUT1/GPIO48
SATA5GP/GPIO49
GPIO57

MISC
GPIO
CPU
NCTF
RSVD

CLKOUT_PCIE6N AH45
CLKOUT_PCIE6P AH46
CLKOUT_PCIE7N AF48
CLKOUT_PCIE7P AF47
A20GATE U2
CLKOUT_BCLK0_N/CLKOUT_PCIE8N AM3
CLKOUT_BCLK0_P/CLKOUT_PCIE8P AM1
PECI BG10
RCIN# T1
PROCPWRGD BE10
THRMTRIP# BD10

TP1 BA22
TP2 AW22
TP3 BB22
TP4 AY45
TP5 AY46
TP6 AV43
TP7 AV45
TP8 AF13
TP9 M18
TP10 N18
TP11 AJ24
TP12 AK41
TP13 AK42
TP14 M32
TP15 N32
TP16 M30
TP17 N30
TP18 H12
TP19 AA23
NC_1 AB45
NC_2 AB38
NC_3 AB42
NC_4 AB41
NC_5 T39
INIT3_3V# P6
TP24 C10

IBEXPEAK-M-GP-NF

VSS_NCTF_1 A4
VSS_NCTF_2 A49
VSS_NCTF_3 A5
VSS_NCTF_4 A50
VSS_NCTF_5 A52
VSS_NCTF_6 A53
VSS_NCTF_7 B2
VSS_NCTF_8 B4
VSS_NCTF_9 B52
VSS_NCTF_10 B53
VSS_NCTF_11 BE1
VSS_NCTF_12 BE53
VSS_NCTF_13 BF1
VSS_NCTF_14 BF53
VSS_NCTF_15 BH1
VSS_NCTF_16 BH2
VSS_NCTF_17 BH52
VSS_NCTF_18 BH53
VSS_NCTF_19 BJ1
VSS_NCTF_20 BJ2
VSS_NCTF_21 BJ4
VSS_NCTF_22 BJ49
VSS_NCTF_23 BJ5
VSS_NCTF_24 BJ50
VSS_NCTF_25 BJ52
VSS_NCTF_26 BJ53
VSS_NCTF_27 D1
VSS_NCTF_28 D2
VSS_NCTF_29 D53
VSS_NCTF_30 E1
VSS_NCTF_31 E53

DEEP_IDLE# Y3
ECSCI# C38
BIO_DET# D37
ECSWI# J32
ECSMI# F10
PCH_GPIO15 T7
DGPU_HOLD_RST# AA2
DGPU_PWROK F38
LCD_CBL_DET_R# Y7
PCH_GPIO27 AB12
PCH_GPIO28 V13
STP_PCI# M11
PCH_GPIO35 V6
DGPU_PWR_EN# AB7
DGPU_PRSNT# AB13
PCH_GPIO38 V3
KB_DET_R# P3
PCIECLKRQ6# H3
DDR_RST_GATE# F1
FFS_INT2_R AB6
TURBO_BOOST_ALERT# AA4
PCH_GPIO57 F8

[81] DEEPIDLE_WAKE_INT_R#
[37] ECSCI#
[78] BIO_DET#
[37] ECSWI#
[37] ECSMI#
[86] GFX_CORE_PGOOD
[23,51] DGPU_1D8V_PGOOD
[54] LCD_CBL_DET#
[80] DGPU_HOLD_RST#
[37] DGPU_PWR_EN#
[68] KB_DET#
[23] KB_DET_R
[9] DDR_RST_GATE#
[40] FFS_INT2_R
[37] TURBO_BOOST_ALERT#

[9] BCLK_CPU_N
[9] BCLK_CPU_P
[9] H_PECI
[37] KBRCIN#
[9,42] H_PWRGOOD
PCH_THERMTRIP_R
[9,37,42] H_THRMTRIP#
Placed Within 2" from PCH
[37] KA20GATE
INIT3_3V#
TP2506TPAD14-GP

+3.3V_RUN_GPU +3.3V_RUN_GPU +3.3V_RUN
R2552 10KR2J-3-GP
R2555 2K2R2J-2-GP
R2503 10KR2J-3-GP
Q2515_1
Q2515 MMBT3904-7-F-GP
SB-32
C2501 SC47P50V2JN-3GP DY
A00-0104-1
R2505 0R0402-PAD-2-GP
R2506 0R0402-PAD-2-GP
R3749 100R2J-2-GP
+3.3V_RUN
R2507 10KR2J-3-GP DGPU_PWROK
R2526 10KR2J-3-GP DY PCH_GPIO27
DW
07/02 Change
1.Change CLK_SATA_OE# to pull-down
R2525 10KR2J-3-GP
R2548 100R2J-2-GP
TPAD14-GP TP2508
+1.05V_VTT
R2509 56R2J-4-GP
R2511 56R2J-4-GP

07/10 Added
1.Changed PCH GPIO DDR_RST_GATE from GPIO57 to GPIO46 , Bason on design guide
07/23 Added
1.Added Finger Printer Detect Pin, control by PCH
2.Change KB_DET signal from EC to PCH control
3.Change LCD_CBL_DET signal from EC to PCH control

For layout request
TPAD14-GP TP2511 PCH_NCTF_2
TPAD14-GP TP2512 PCH_NCTF_3
TPAD14-GP TP2510 PCH_NCTF_1
TPAD14-GP TP2509 PCH_NCTF_4

+3.3V_ALW
PCH_GPIO28 R2530 10KR2J-3-GP
PCH_GPIO15 R2532 1KR2J-1-GP
PCIECLKRQ6# R2521 10KR2J-3-GP
SB-
swap net for layout
RN2504 SRN10KJ-5-GP
ECSMI#
PCH_GPIO57
SB-1023
LCD_CBL_DET_R# R2520 10KR2J-3-GP
DGPU_HOLD_RST# R2516 DY 10KR2J-3-GP
STP_PCI# R2517 10KR2J-3-GP
+3.3V_RUN
RN2502 SRN10KJ-5-GP
ECSWI#
ECSCI#
RN2503 SRN10KJ-5-GP
PCH_GPIO19
PCH_GPIO38
[24] PCH_GPIO19
SB-1026
swap net for layout
RN2501 SRN10KJ-5-GP
[24,36,37] INT_SERIRQ
INT_SERIRQ
FFS_INT2_R
DGPU_PWR_EN#
BIO_DET#
[78] BIO_DET#
SB-1023
RN2501 change to 4.7K size
R2527 10KR2J-3-GP DY
DGPU_PRSNT#
R2528 10KR2J-3-GP

1st Samsung
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Title: PCH (GPIO/CPU)
Size: Document Number: Winery13 MB DIS
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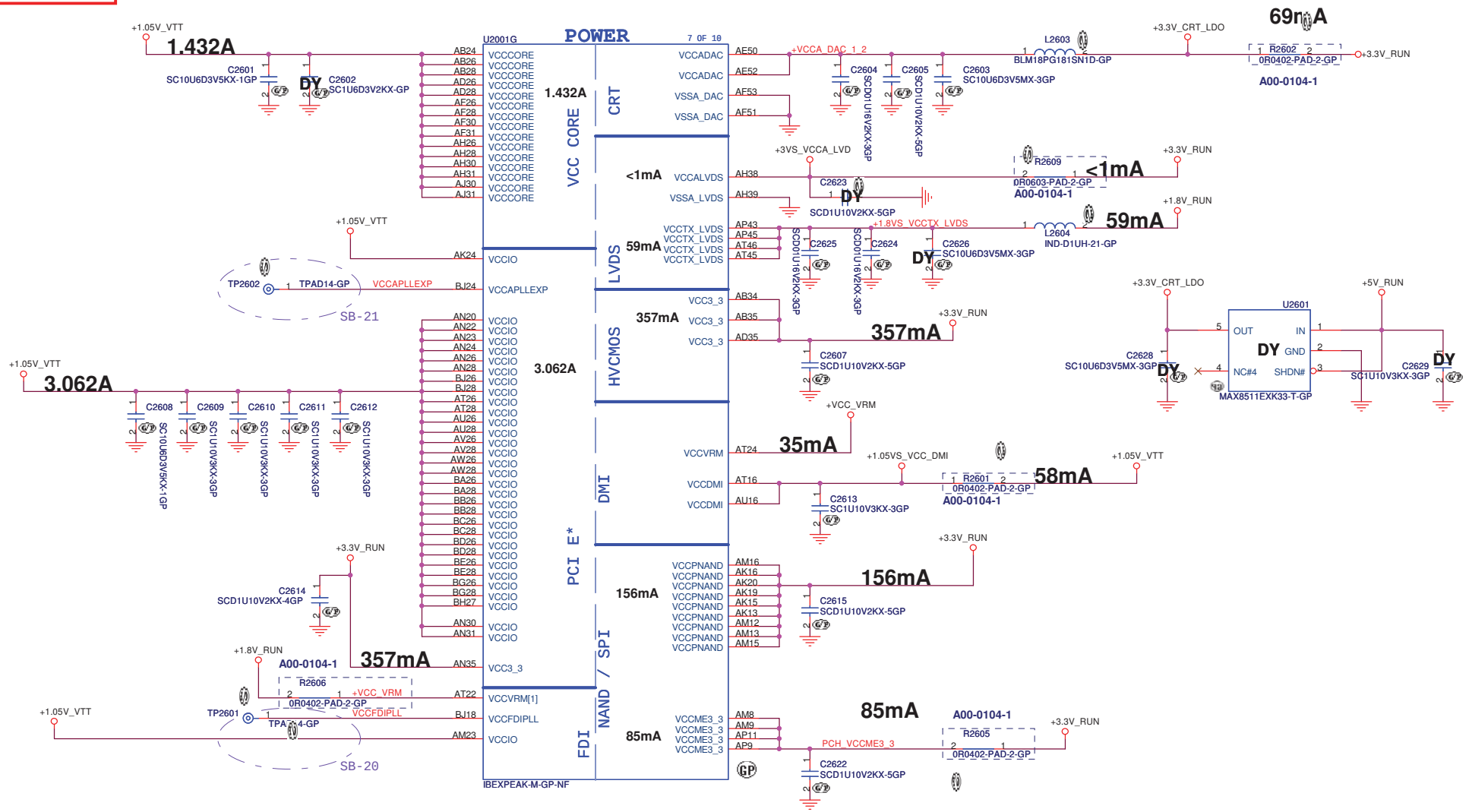
Sheet 25 of 88

SSID = PCH



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Title: PCH (POWER1)

Size	Document Number	Rev
	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 26 of 88

SSID = PCH

U2001J POWER 10 OF 10

SB-15

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK
52mA

AF23 VCCLAN
AF24 VCCLAN
320mA

DCPSUSBYP Y20 DCPSUSBYP
C2707 SCD1U10V2KX-4GP

AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
1.849A

+1.05V_VTT
C2705 SC10U6D3V5KX-1GP
C2708 SC1U6D3V2KX-GP DY
C2704 SC10U6D3V5KX-1GP
C2710 SC1U6D3V2KX-GP DY

SB-17

+1.05V_VTT
L2702 IND-10UH-218-GP
+1.05VS_VCCA_A_DPL
C2734 SC10U6D3V5MX-3GP DY
C2711 SC1U6D3V2KX-GP
L2703 IND-10UH-218-GP
+1.05VS_VCCA_B_DPL
C2735 SC10U6D3V5MX-3GP DY
C2714 SC1U6D3V2KX-GP

+VCCRTCEXT V9 DCPRTC
C2713 SCD1U10V2KX-4GP
+VCC_VRM
AU24 VCCVRM

68mA +1.05VS_VCCA_A_DPL
BB51 VCCADPLLA
BB53 VCCADPLLA
68mA

69mA +1.05VS_VCCA_B_DPL
BD51 VCCADPLLB
BD53 VCCADPLLB
69mA

+1.05V_VTT
C2718 SC1U6D3V2KX-GP
C2719 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO

+VCCSST V12 DCPSST
C2723 SCD1U10V2KX-4GP
+1.05VALW_INT_VCCSUS Y22 DCPSUS
C2724 SCD1U10V2KX-4GP

P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
163mA
+3.3V_ALW
C2726 SCD1U10V2KX-4GP

+3.3V_RUN
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
C2727 SCD1U10V2KX-4GP

+1.05V_VTT
<1mA
C2728 SC10U6D3V5KX-1GP
C2729 SCD1U16V2KX-3GP
C2730 SCD1U16V2KX-3GP
AT18 V_CPU_IO
AU18 V_CPU_IO
<1mA

+RTC_CELL
2mA
A12 VCCRTC
C2732 SCD1U10V2KX-4GP
C2733 SCD1U10V2KX-4GP
IBEXPEAK-M-GP-NF

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

USB
163mA
V24 VCCIO
V26 VCCIO
Y24 VCCIO
Y26 VCCIO
C2706 SC1U10V2KX-1GP DY
+1.05V_VTT
+3.3V_ALW
C2703 SCD1U10V2KX-4GP
VCCSUS3_3 ×28
U23 VCCSUS3_3
V23 VCCIO
<1mA V5REF_SUS F24 +5VALW_PCH_VCC5REFSUS
+3.3V_ALW
C2709 SCD1U10V2KX-4GP
+1.05V_VTT
+3.3V_ALW
D2701 CH751H-40PT-GP
+5V_ALW
R2701 100R2J-2-GP
C2712 SC1U6D3V2KX-GP

DW
07/10 Change resistor Value
1.R2701,R2702 value corrected to 100 Ohms following PDG doc

<1mA V5REF K49 +5VS_PCH_VCC5REF
+3.3V_RUN
D2702 CH751H-40PT-GP
+5V_RUN
R2702 100R2J-2-GP
C2715 SC1U6D3V2KX-GP

PCI/GPIO/LPC
VCC3_3 ×7
+3.3V_RUN
C2716 SCD1U10V2KX-4GP
+3.3V_RUN
C2717 SCD1U10V2KX-4GP
VCC3_3 AD13

VCCSATAPLL AK3 AK1
VCCSATAPLL
TP2702 TPAD14-GP
SB-16

SATA
196mA
VCCIO AH22
VCCVRM AT20
+VCC_VRM
C2725 SC1U6D3V2KX-GP
+1.05V_VTT
VCCIO ×12

CPU
VCCME ×8
+1.05V_VTT

RTC
HDA
6mA VCCSUSHDA L30
R2707 0R0402-PAD-2-GP
A00-0104-1
+3.3V_ALW
C2731 SC1U6D3V2KX-GP
+3VS_+1.5VS_HDA_IO

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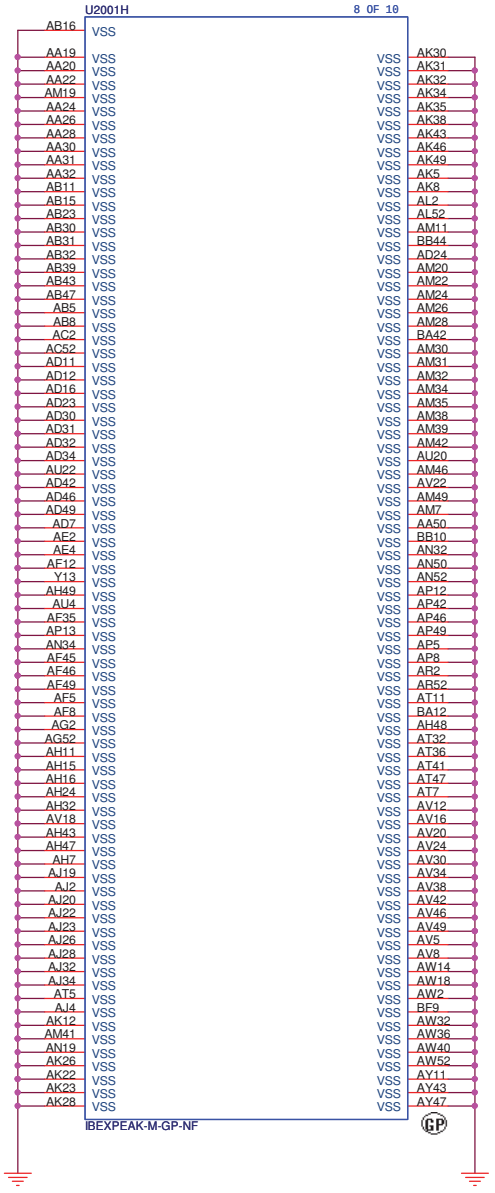
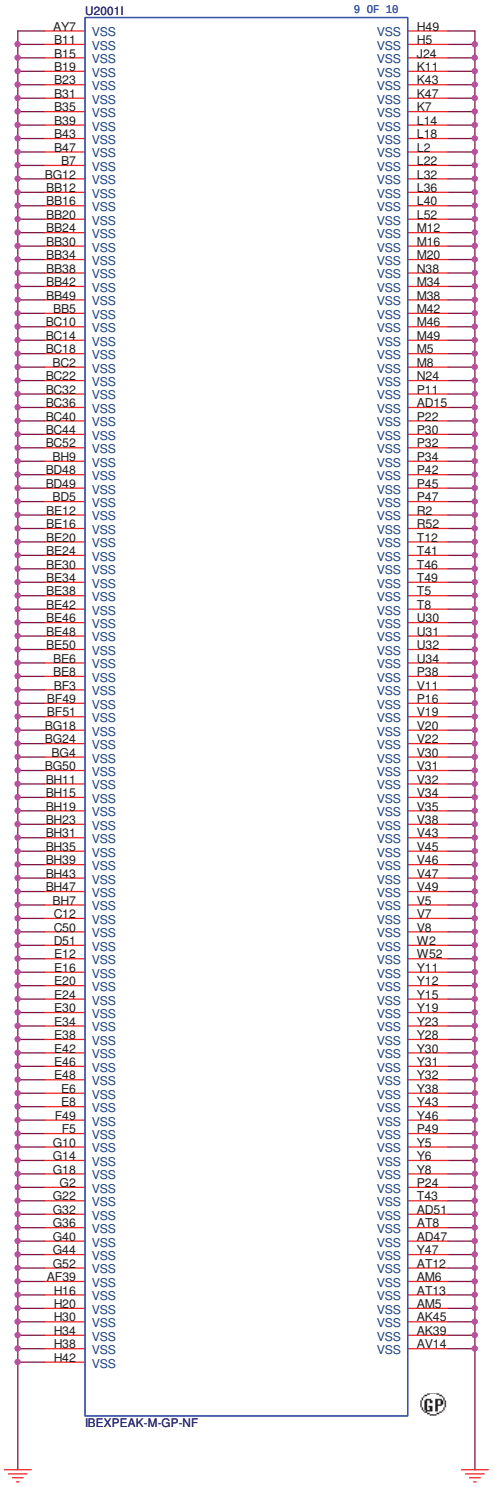
Title: PCH (POWER2)
Size: Document Number: Winery13 MB DIS Rev: A00
Date: Wednesday, January 13, 2010 Sheet 27 of 88

SSID = PCH





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Title		
PCH (VSS)		
Size	Document Number	Rev
	Winery13 MB DIS	A00
Date: Wednesday, January 13, 2010	Sheet 28 of 88	

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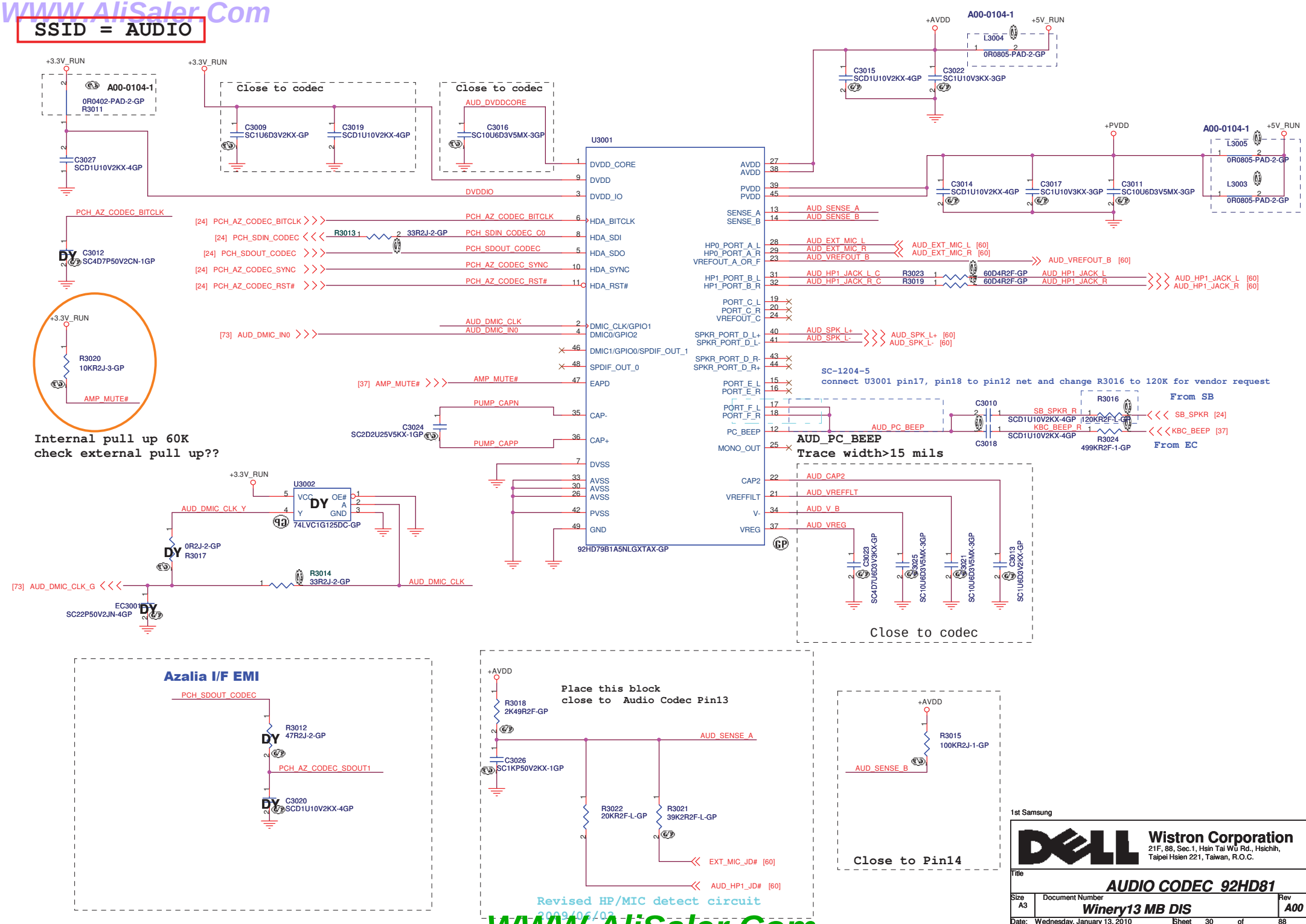
Title

(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date: Wednesday, January 13, 2010 Sheet 29 of 88

SSID = AUDIO



1st Samsung

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Title: AUDIO CODEC 92HD81

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 30 of 88

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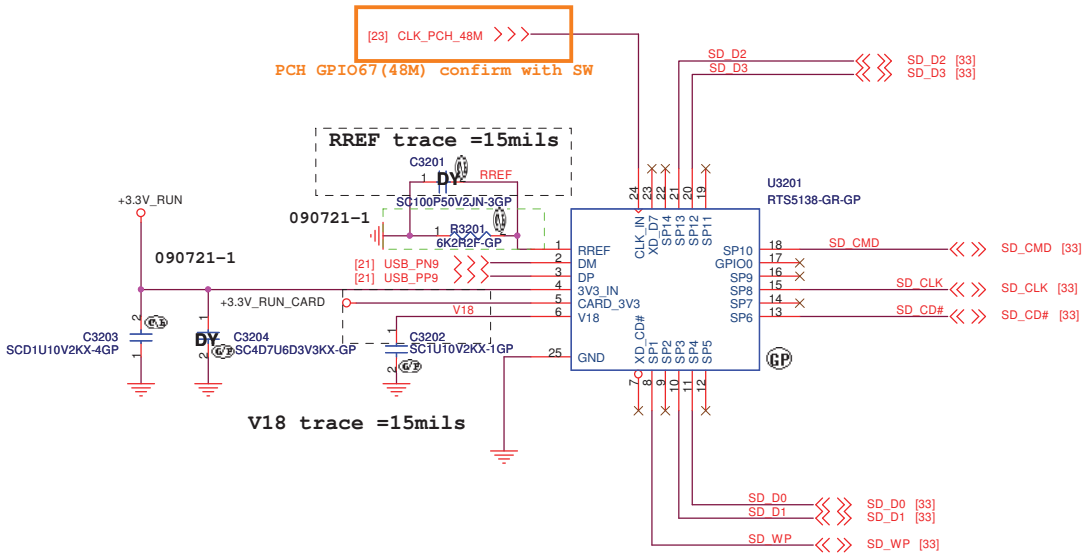
Title

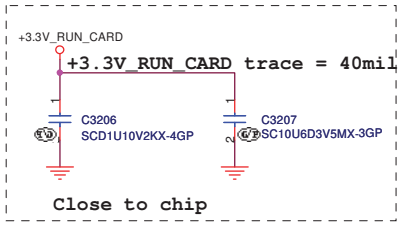
(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date: Wednesday, January 13, 2010 Sheet 31 of 88

SSID = SDIO





1st Samsung

DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

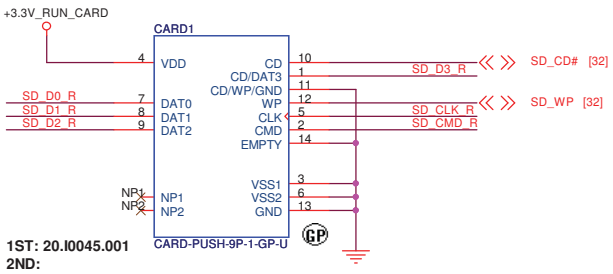
Title: *CardReader/RTS5138*

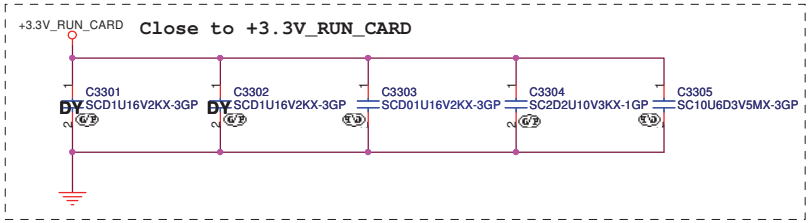
Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

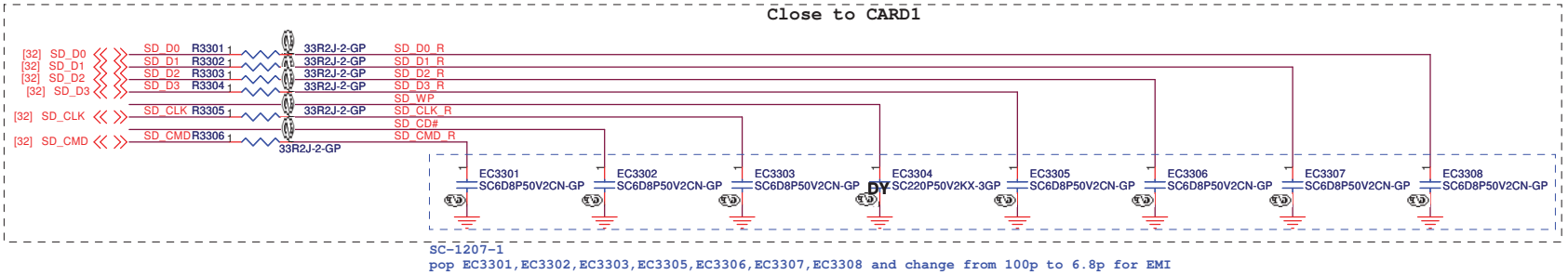
Date: Wednesday, January 13, 2010 | Sheet 32 of 88

SSID = SDIO

SD/MMC/MMC+ Card Reader







SSID = 1394

Remove 1394

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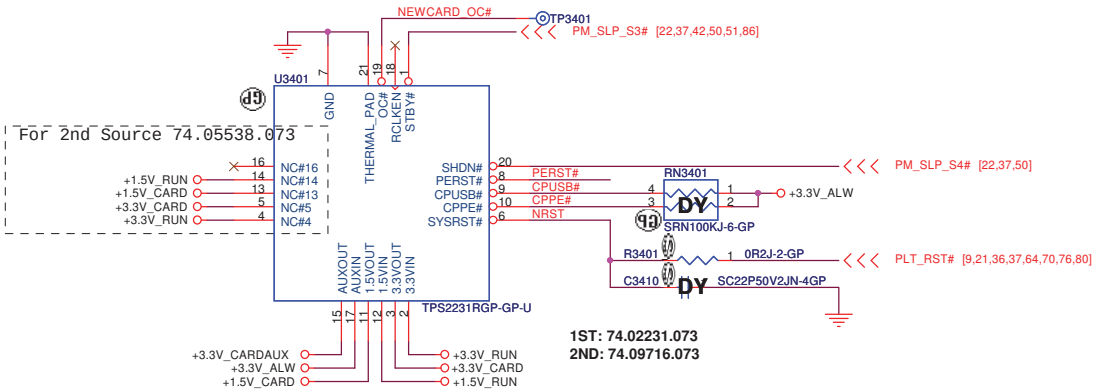
Title: CARD READER CONN

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 33 of 88

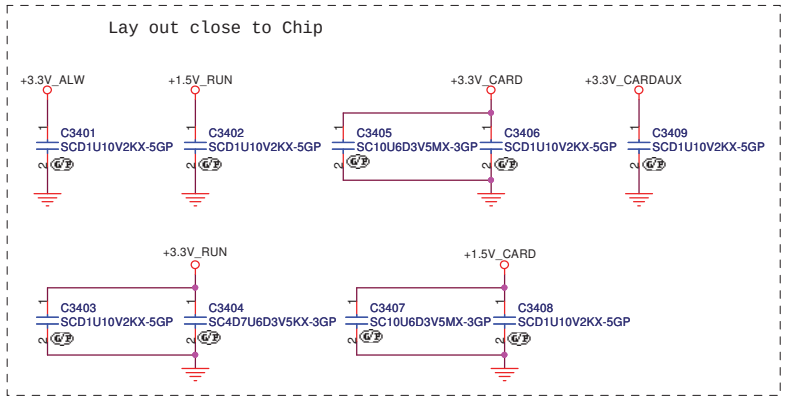
SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

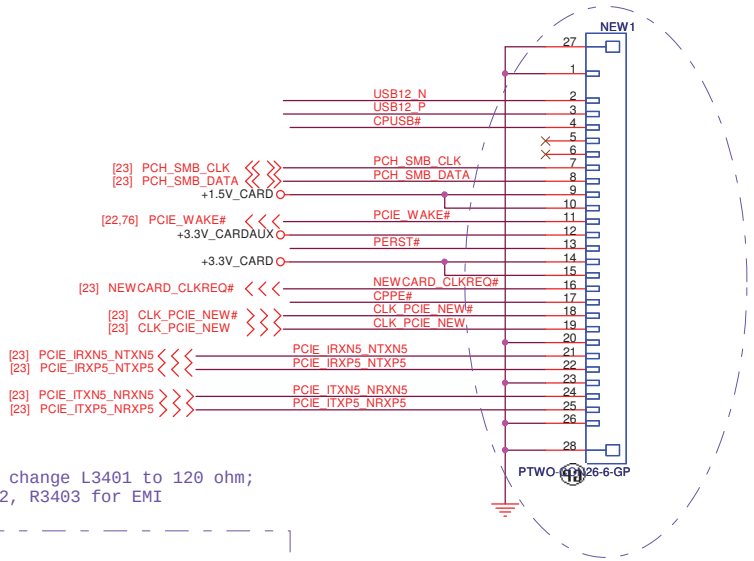


1ST: 74.02231.073
2ND: 74.09716.073

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

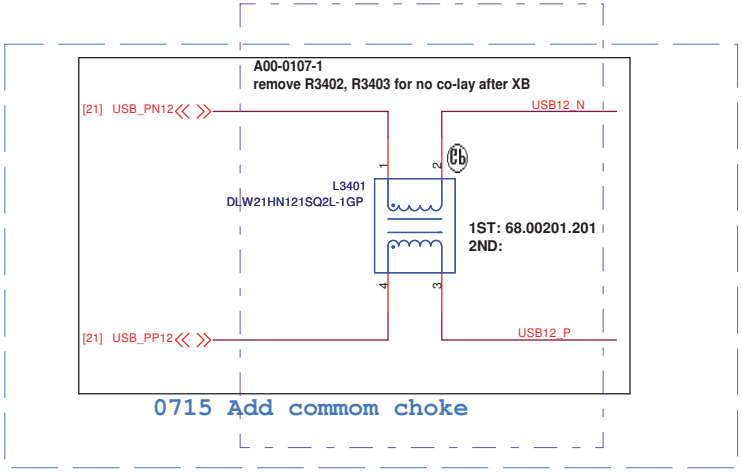


SB-26



1ST: 20.K0370.026
2ND: 20.K0315.026

SB-1021
pop and change L3401 to 120 ohm;
DY R3402, R3403 for EMI



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Title: ExpressCard
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 34 of 88

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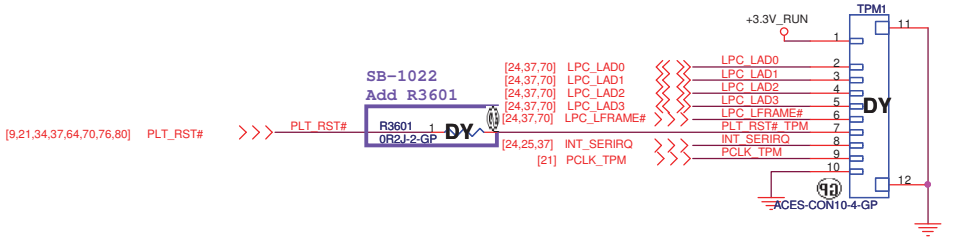
Title: (Reserve)

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 35 of 88

SSID = User.Interface

TPM board CONN



SC-1125-1
remove TPM AFTP

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Title: TPM		
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 36 of 88	

SSID = KBC

Put 0.1uf close to VCC-GND pin pair.

U3701A

MB VERSION

ID	VER1	VER0
SA	0	0
SB	0	1
SC	1	0
-1	1	1

KBC CLK EMI

Pull High : Discrete
internal Pull Low for UMA

Pull High : Switch Board
Pull Low : UnSwitch Board

C3710 need place near pin 44.

SC-1118-1
change power rail to KBC_PWR

SC-1125-2
add U3703 mux for panel backlight enable signal select

Add reset IC U3704 to prevent SPI ROM data lost

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Title: KBC Nuvoton NPCE781BA0DX

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 37 of 88

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Title: *(Reserve)*

Size: Custom | Document Number: *Winery13 MB DIS* | Rev: *A00*

Date: Wednesday, January 13, 2010 | Sheet 38 of 88

SSID = Thermal

+5V_RUN
25mil
C3910 SC4D7U6D3V5KX-3GP
C3909 SCD1U10V2KX-5GP

+3.3V_RUN
R3907 10KR2J-3-GP
SB-1023
EMC2102_FAN_TACH_1
EMC2102_FAN_TACH_1 [58]
EMC2102_FAN_DRIVE
EMC2102_FAN_DRIVE [58]
25mil
RN3901 SRN4K7J-8-GP
THERM_SCL [37,78]
THERM_SDA [37,78]

DW
07/10 Del
1. Not reserve S5 power source rail for EMC2102 ??

1. WWAN
1ST: 84.03904.P11
2ND: 84.03904.T11
Q3905 must be near WWAN
C3912 must be near Q3905
CH3904PT-GP Q3905
C3912 SC470P50V2JN-GP
C3914 SC470P50V2JN-GP
C3914 must be near EMC2102

+3.3V_RUN
R3908 49D9R2F-GP
EMC2102_VDD_3D3
C3905 SCD1U16V2KX-3GP

U3901 EMC2102
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#

EMC2102_DN1
EMC2102_DP1
VGA_THERMDC
VGA_THERMDA
T8_THERMDC
T8_THERMDA

TP_ALERT# TP3903 TPAD14-GP
CLK_32K
EMC2102_CLK_SEL
R3906 10KR2J-3-GP
TP_EM2102_RESET# TP3904 TPAD14-GP

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. GPU Sensor
[81] VGA_THERMDC
[81] VGA_THERMDA
C3906 SC470P50V2JN-GP
C3906 must be near EMC2102

DW
07/23 Removed
1.Removed SYSTEM Sensor Critical

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
R3903 10KR2J-3-GP
EMC2102_SHDN
R3916 0R2J-2-GP
EMC2102_FAN_mode
R3914 10KR2J-3-GP

EMC2102-DZK-GP
1ST: 74.02102.A73
2ND: 74.07922.0B3

RN3902 SRN10KJ-5-GP
EMC2102_PWROK
EMC2102_THERMTRIP#
+3.3V_RUN

KBC_PWR
R3910 10KR2J-3-GP
R3917 10KR2J-3-GP
SYS_SHDN#
SHDN
Q3903 2N7002A-7-GP
PURE_HW_SHUTDOWN# [37,42]
V_DEGREE
1ST: 84.2N702.E31
2ND: 84.2N702.D31

3. CPU Sensor
Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.
C3901 must be near Q3901
CH3904PT-GP Q3901
C3901 SC470P50V2JN-GP
C3903 SC470P50V2JN-GP
C3903 must be near EMC2102
1ST: 84.03904.P11
2ND: 84.03904.T11
3.HW T8 sensor (CPU)

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

+3.3V_RUN
C3902 SCD1U10V2KX-5GP
R3902 10KR2F-2-GP
TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)
T8 shutdown is set 86 deg-C.
SC-1204-1
C3904 SCD1U10V2KX-5GP
R3904 2K37R2F-GP

DW
07/28 Removed
1. Removed U3902 AND gate.

32K suspend clock output
1ST: 84.2N702.E31
2ND: 84.2N702.D31
Q3902 2N7002A-7-GP
[22] PCH_SUSCLK_2102
CLK_32K_R
R3913 10R2J-2-GP
CLK_32K
C3911 SC4D7P50V2CN-1GP
RUN_POWER_ON [42,52]

1st Samsung

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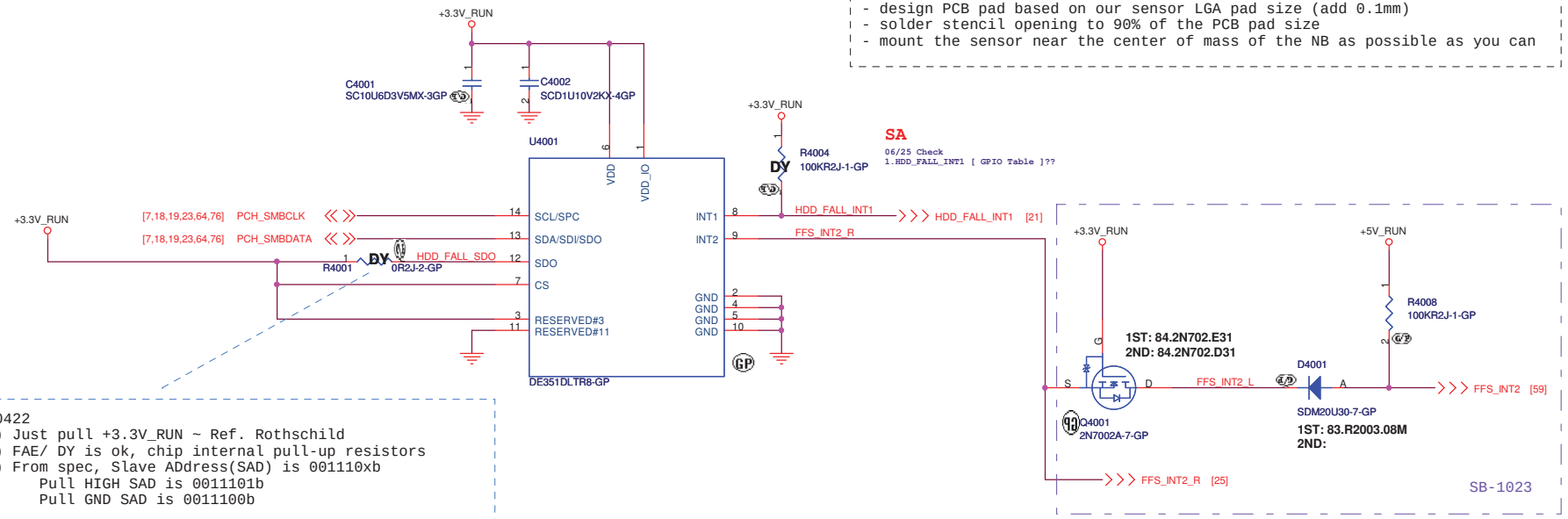
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 39 of 88

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title: Free Fall Sensor
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 40 of 88

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Title

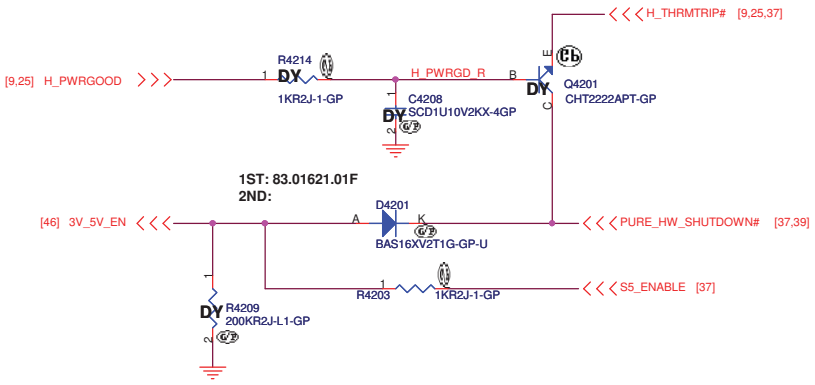
(Reserve)

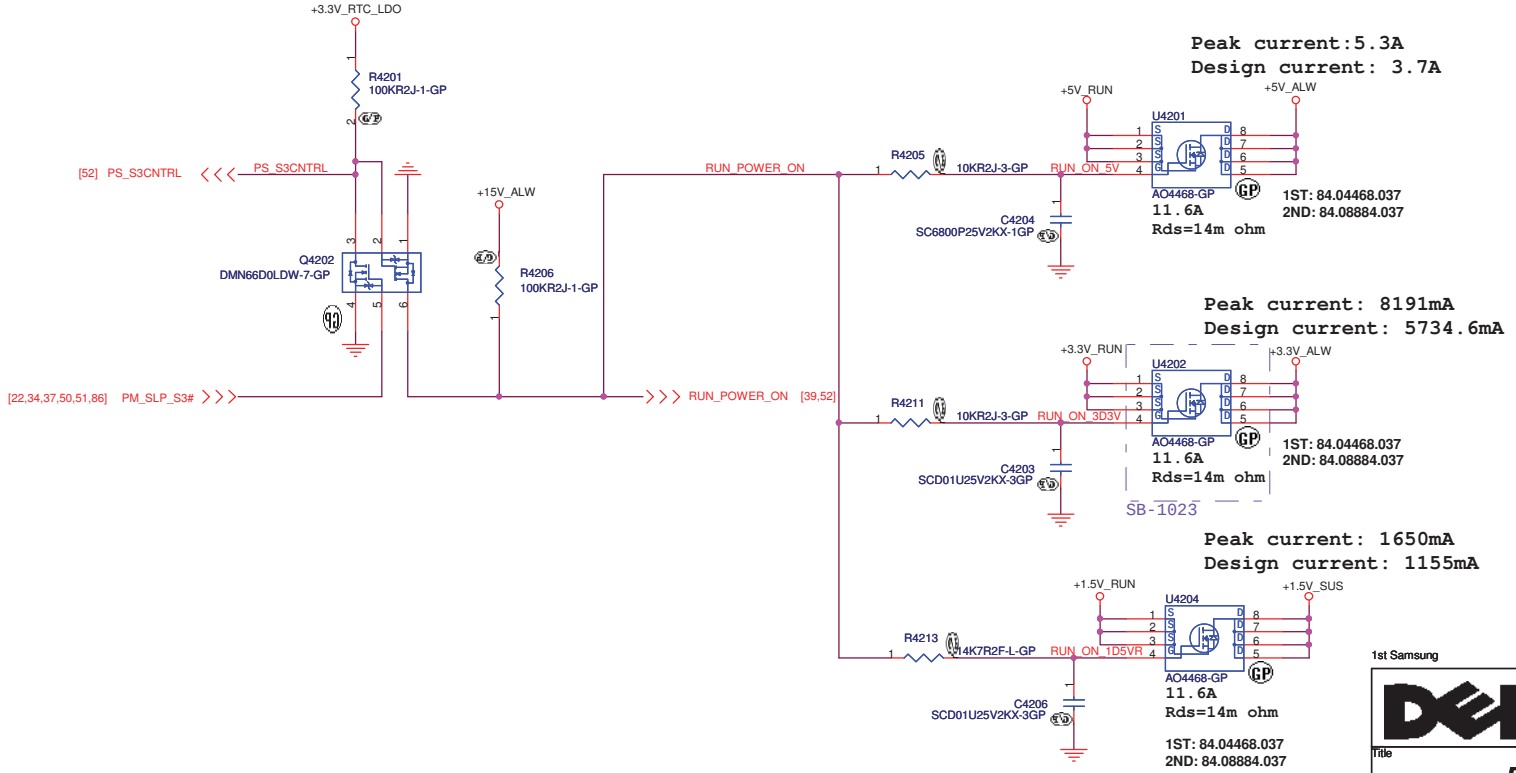
Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date: Wednesday, January 13, 2010 Sheet 41 of 88

SSID = Reset.Suspend

Remove +3.3V_DELAY power rail 2009/05/25





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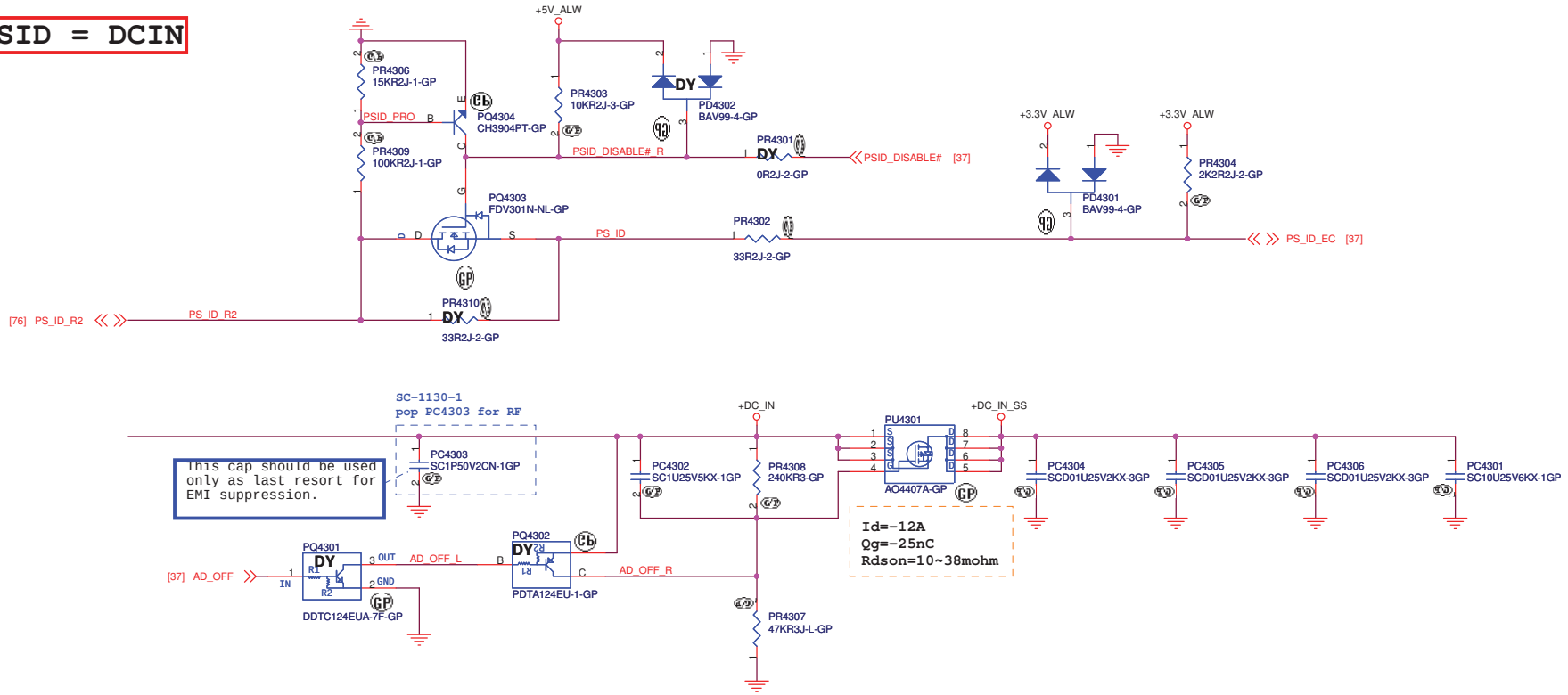
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 42 of 88

SSID = DCIN



1st Samsung

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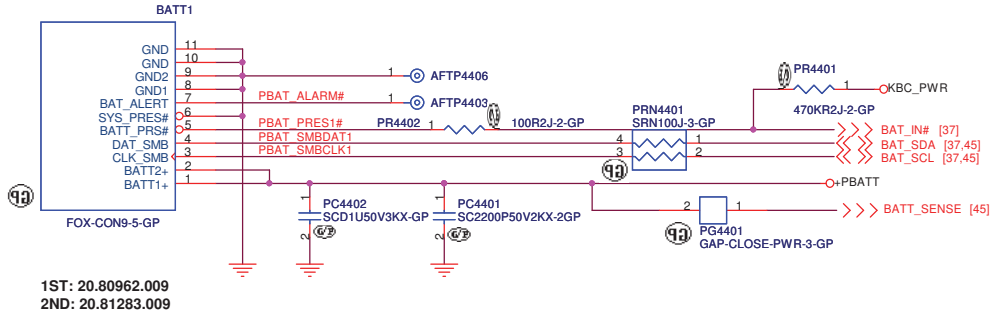
Taipei Hsien 221, Taiwan, R.O.C.

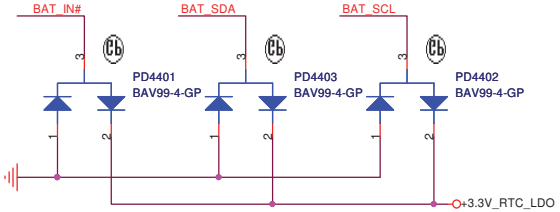
Title	DCIN	
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 43 of 88	

SSID = BATT

Batt Connecter



1ST: 20.80962.009
2ND: 20.81283.009

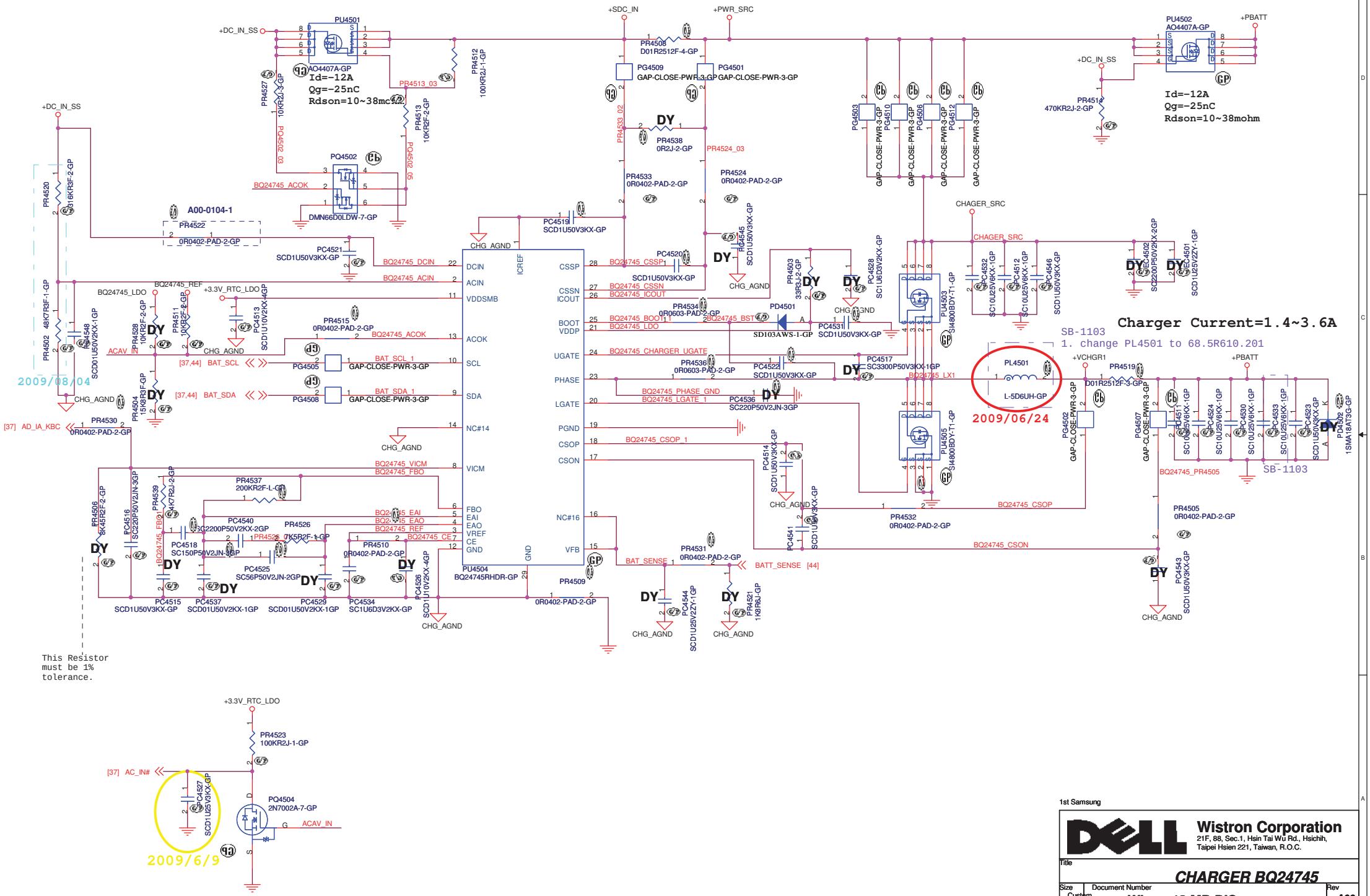


1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Batt Connecter	
Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 44 of 88	

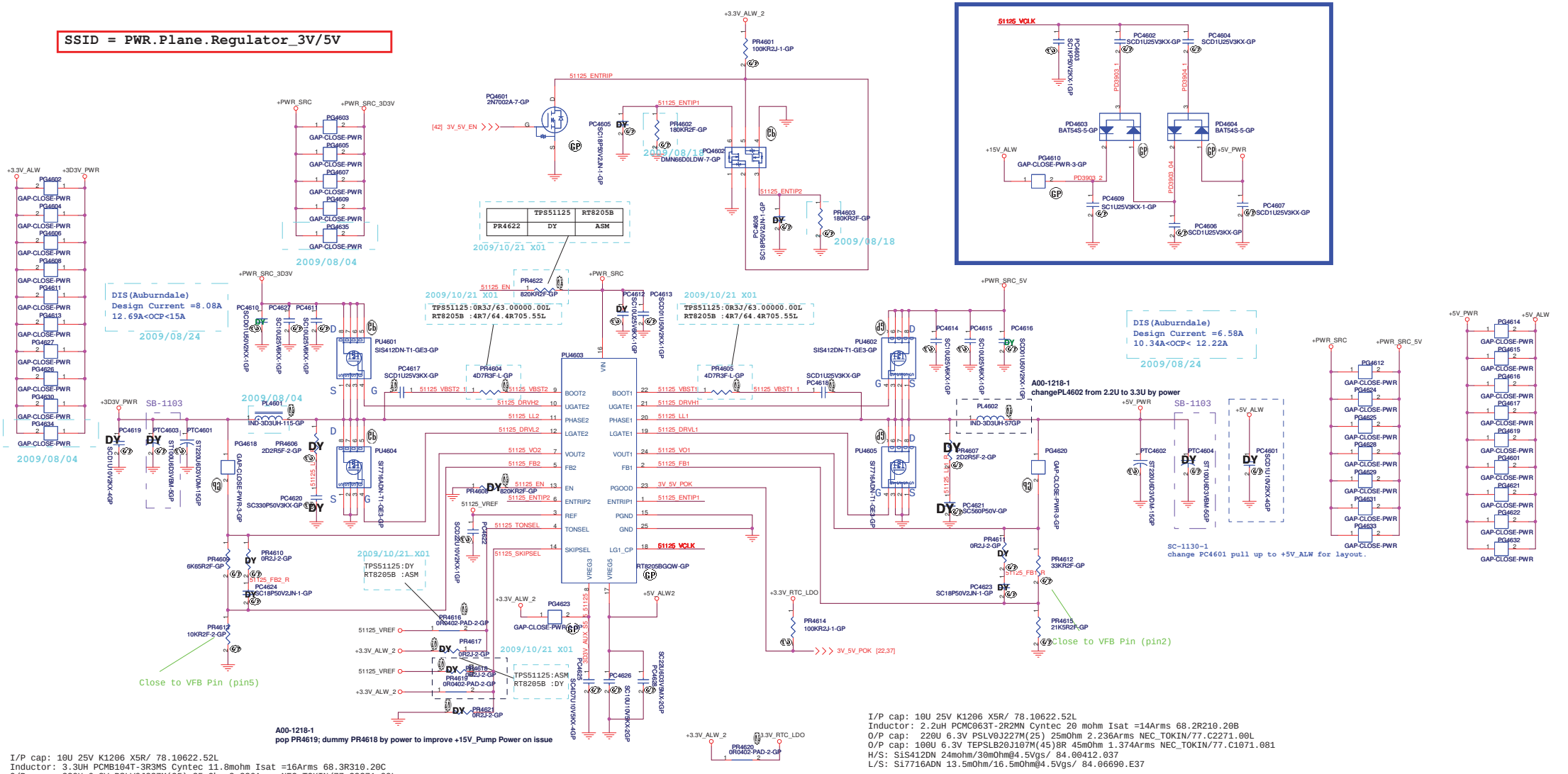
SSID = Charger



1st Samsung

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CHARGER BQ24745
Size: Custom	Document Number: Winery13 MB DIS
Rev	A00
Date: Wednesday, January 13, 2010	Sheet 45 of 88

SSID = PWR.Plane.Regulator_3V/5V



	TPS51125	RT8205B
PR4622	DY	ASM

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: SiS412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: Si7716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 46 of 88

SSID = PWR.Plane.Regulator_CPU Core

SC-1204-4
remove TC4701 for layout

NTC 470K close to H/S MOSFET of Phase1

NTC 10K close to Choke of Phase1

SB-1103
1. change PR4783 to 64.15015.6DL
2. change PR4796 to 64.20515.6DL
3. change PC4756 to 78.10421.2BL
4. change PC4757 to 78.47321.2FL

SC-1130-1
change PC4762 to 0603 size

2009/07/29

Intel support POC (power on current).

1st Samsung

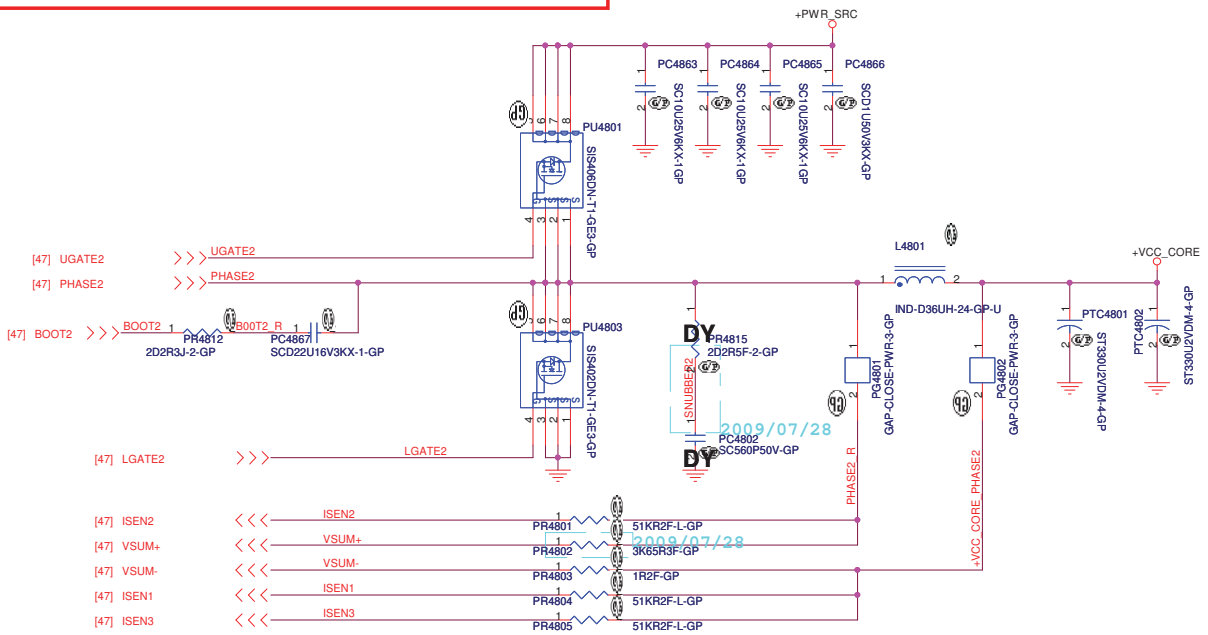
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE_1/2

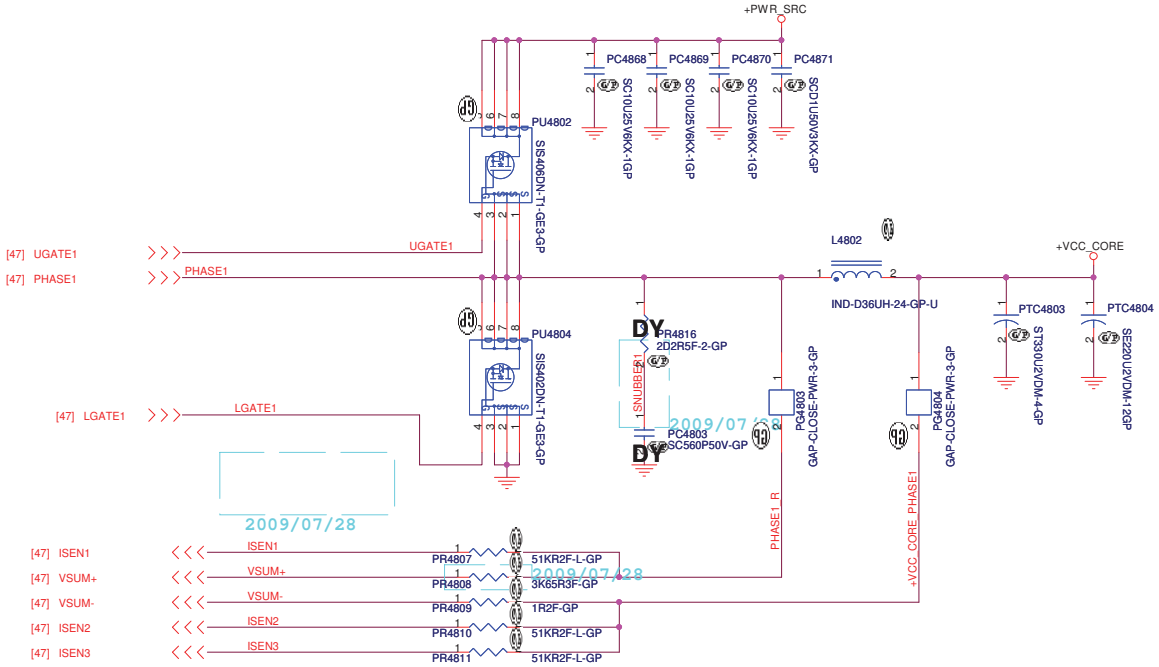
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 47 of 88

SSID = PWR.Plane.Regulator_CPU Core



DIS(Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SiR474DP/ POWERPAK-8/ 10mOhm/12mOhm @4.5Vgs/ 84.00474.037
L/S: Si7170DP/ POWERPAK-8/ 3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037
Freq=300KHz@PER PHASE

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

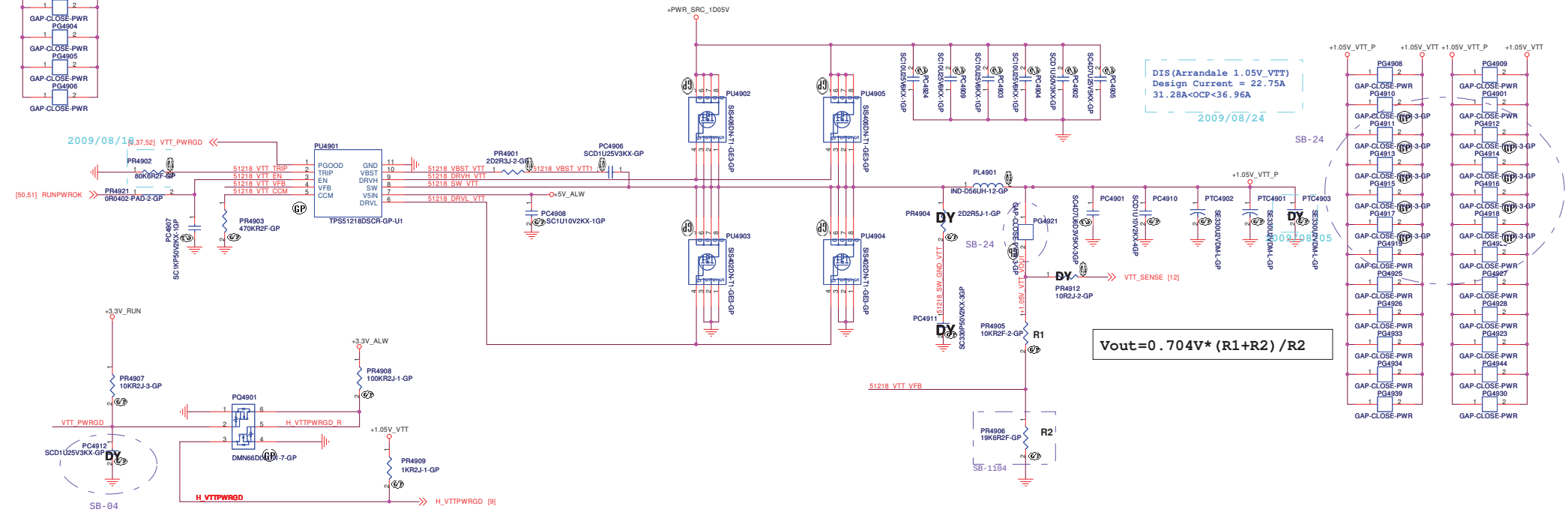
Title: ISL62883_CPU_CORE_2/2

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 48 of 88

SSID = PWR.Plane.Regulator_1D05V_VTT

TPS51218 for +1.05V_VTT



Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

1st Samsung

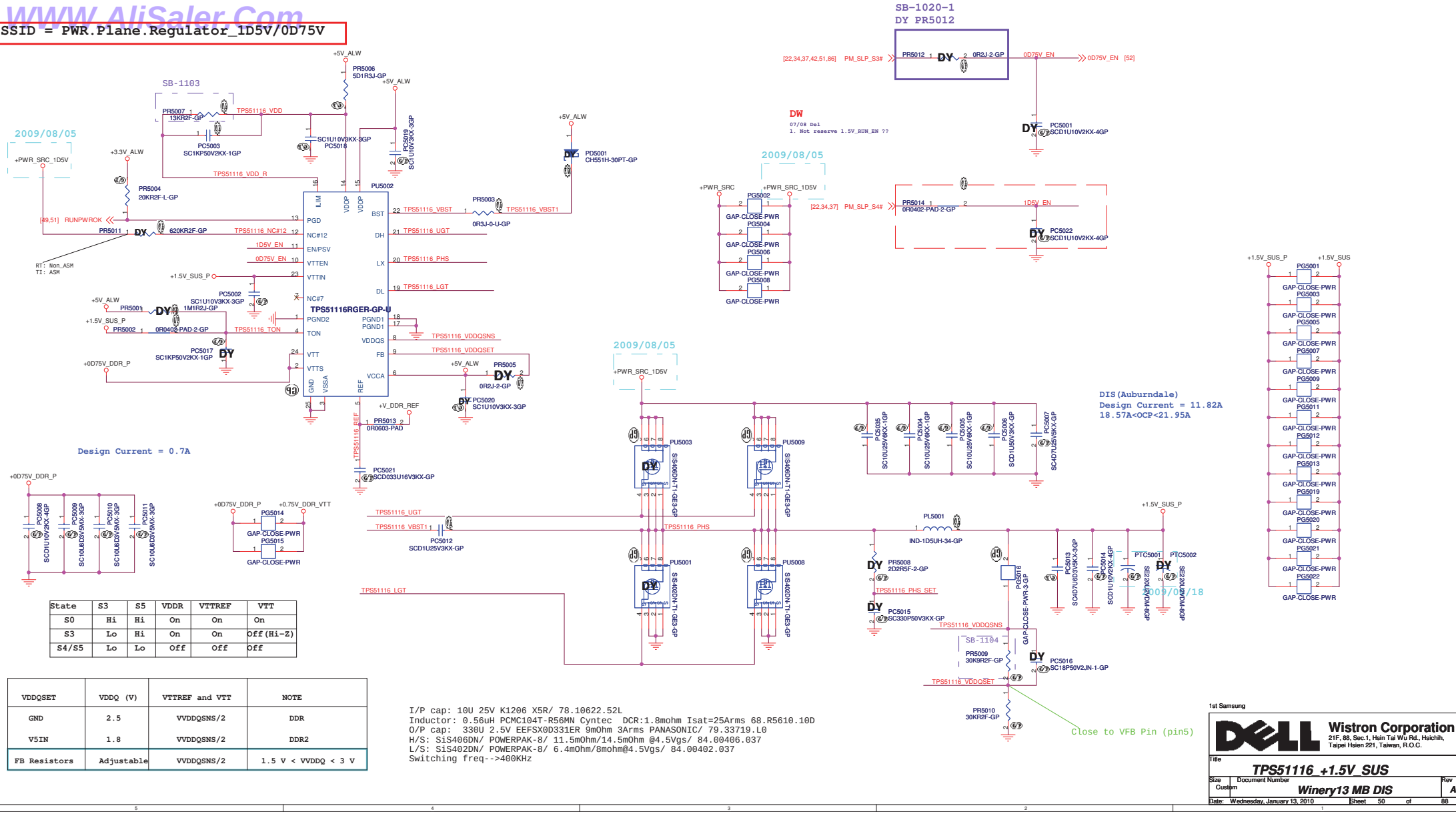
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 49 of 88

SSID = PWR.Plane.Regulator_1D5V/0D75V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
Switching freq-->400KHz

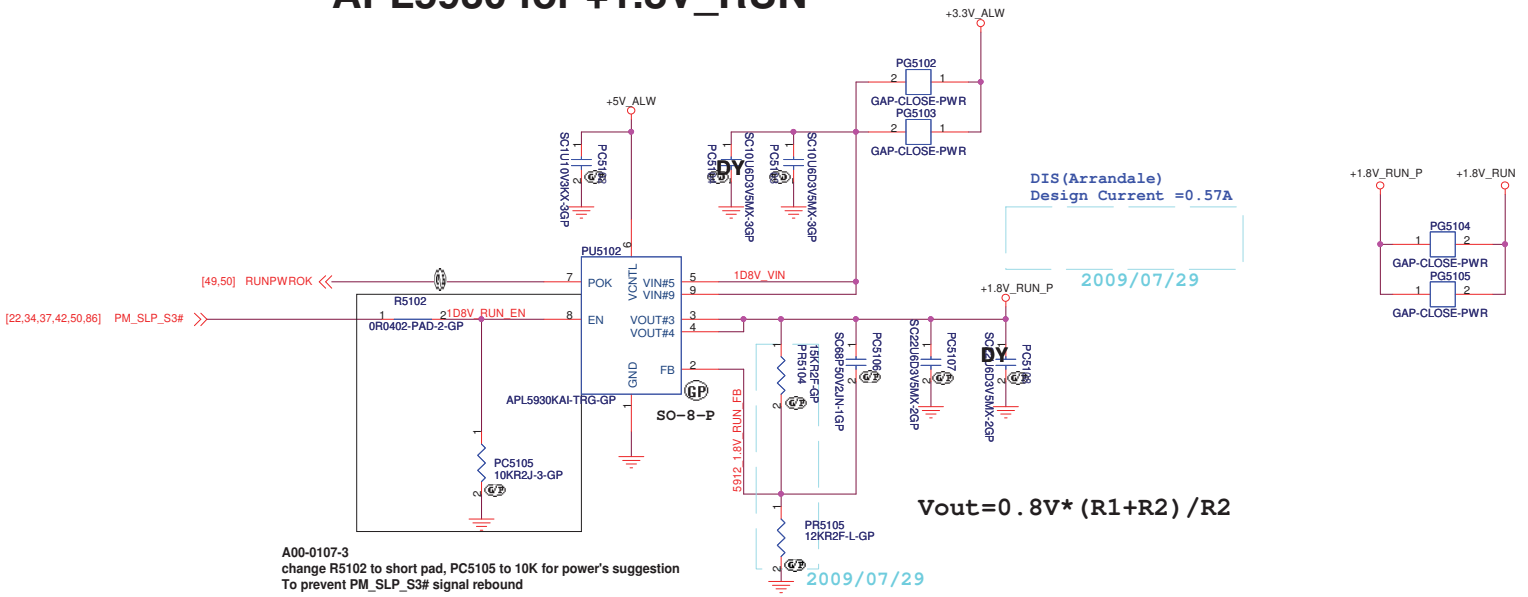
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

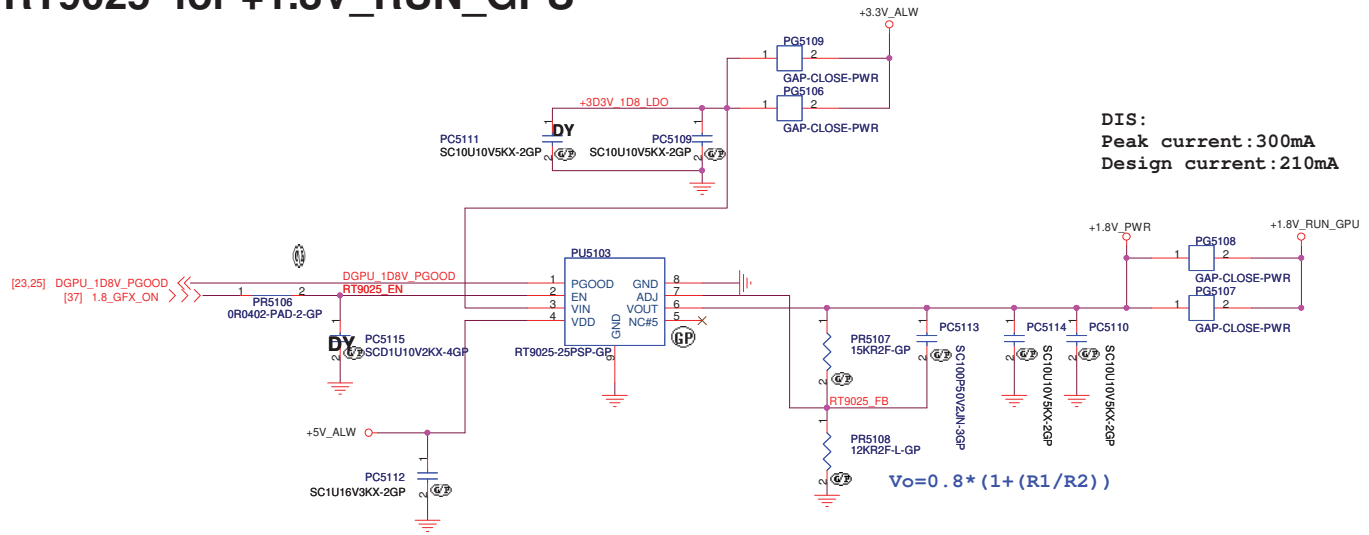
Title: TPS51116_+1.5V_SUS
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 50 of 88

SSID = PWR.Plane.Regulator_1D8V

APL5930 for +1.8V_RUN



RT9025 for +1.8V_RUN_GPU



1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

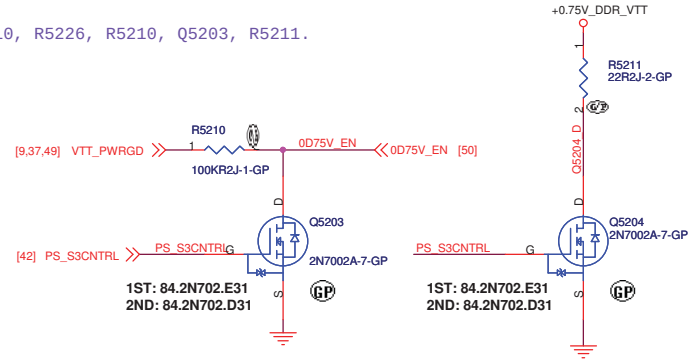
Title: APL5930/RT9205

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 51 of 88

SSID = PWR.Plane.Switch_1D5V CPU

SB-1020-1
DY R5215, R5222, R5223; POP R5221, C5210, R5226, R5210, Q5203, R5211.

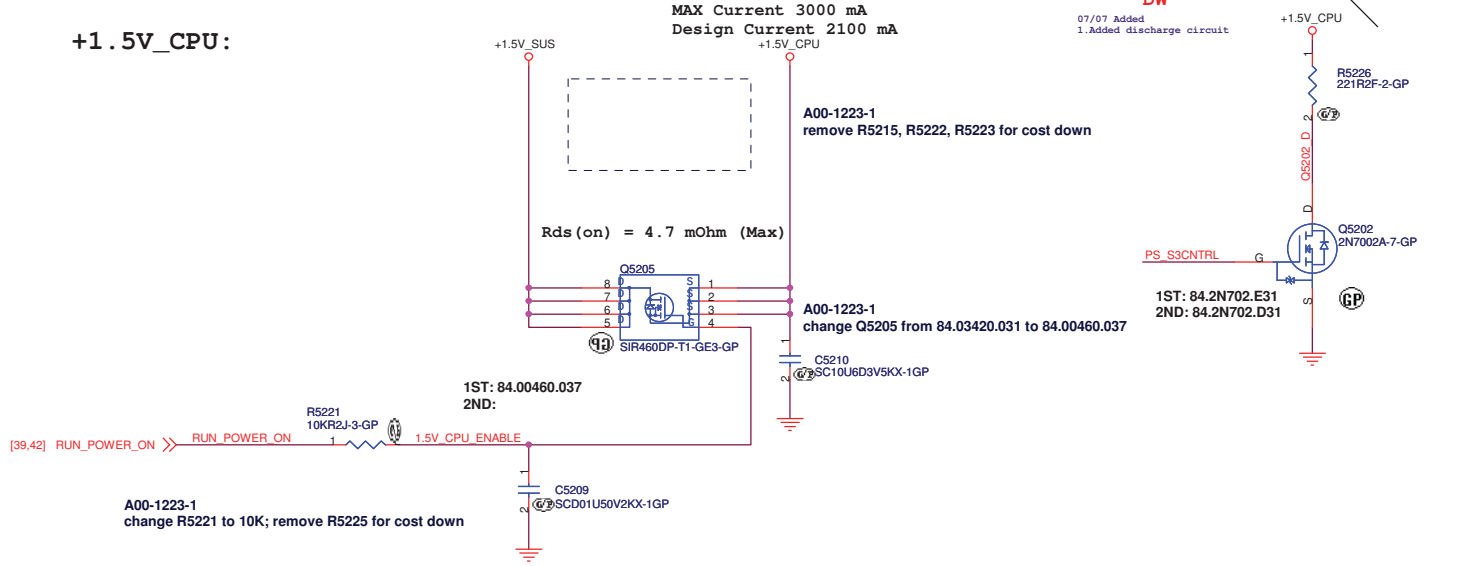


Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details
Revision 0.1

DW
07/07 Added
1.Added discharge circuit

+1.5V_CPU:

MAX Current 3000 mA
Design Current 2100 mA



DW
07/20 corrected
1. Removed C5288
2. RemovedQ5207,R5225,R5220 to save more part counts

1st Samsung

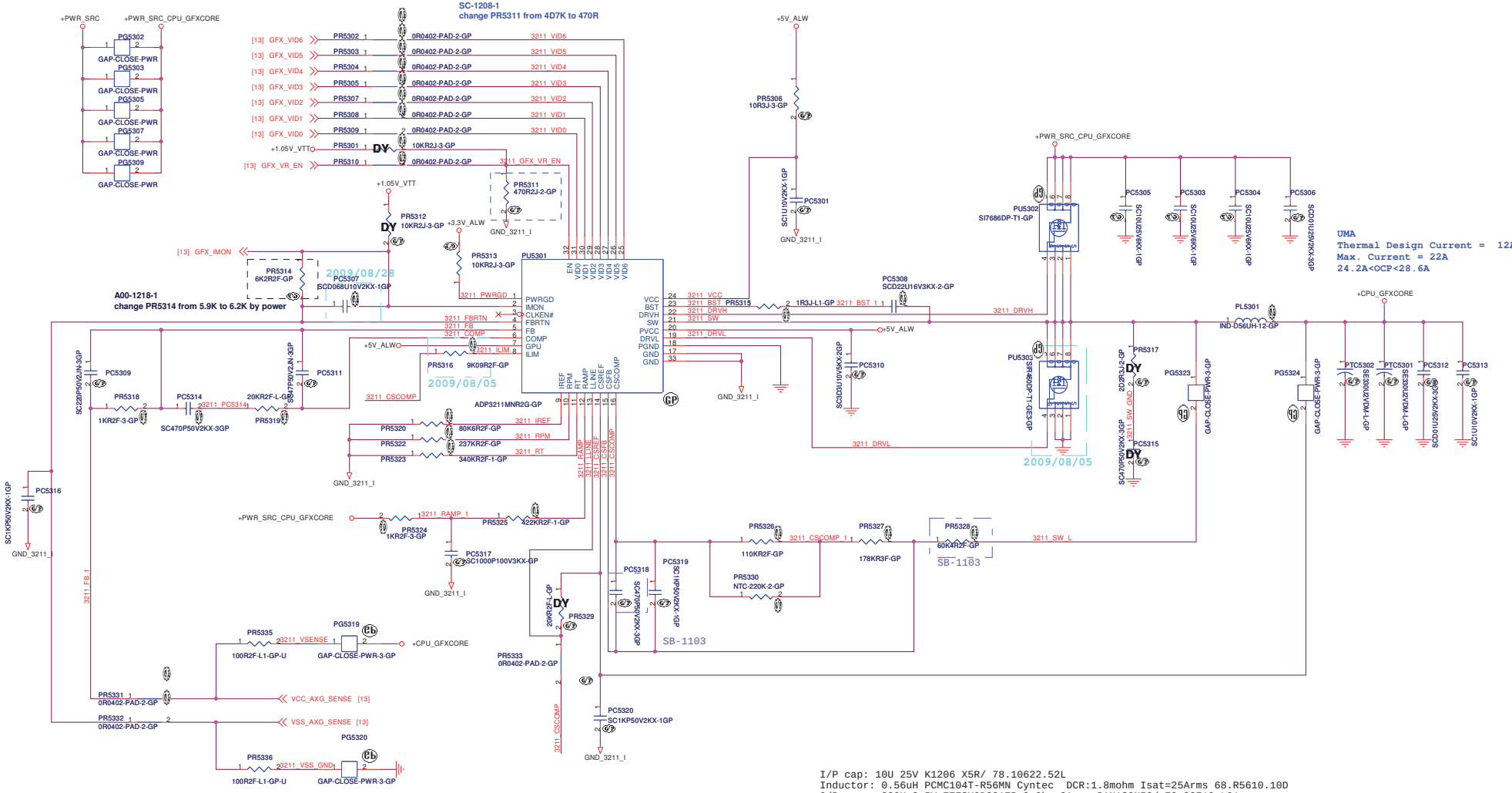
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1D5V

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

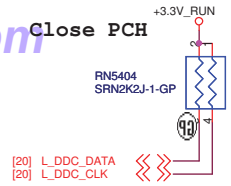
Date: Wednesday, January 13, 2010 | Sheet 52 of 88

SSID = CPU.GFX.Regulator

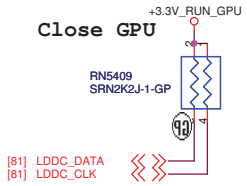


SSID = VIDEO

Close PCH

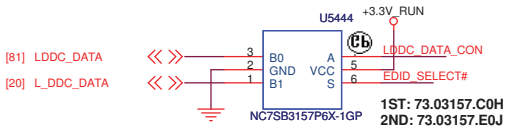


Close GPU



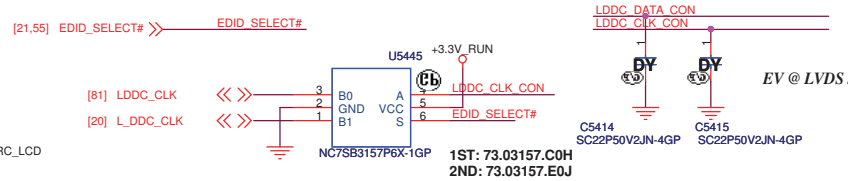
DW
07/07 Added
1.Added LVDS DDC CLK/DAT Pull Hi

UMA/DIS LVDS DDC CLK/DAT select circuit



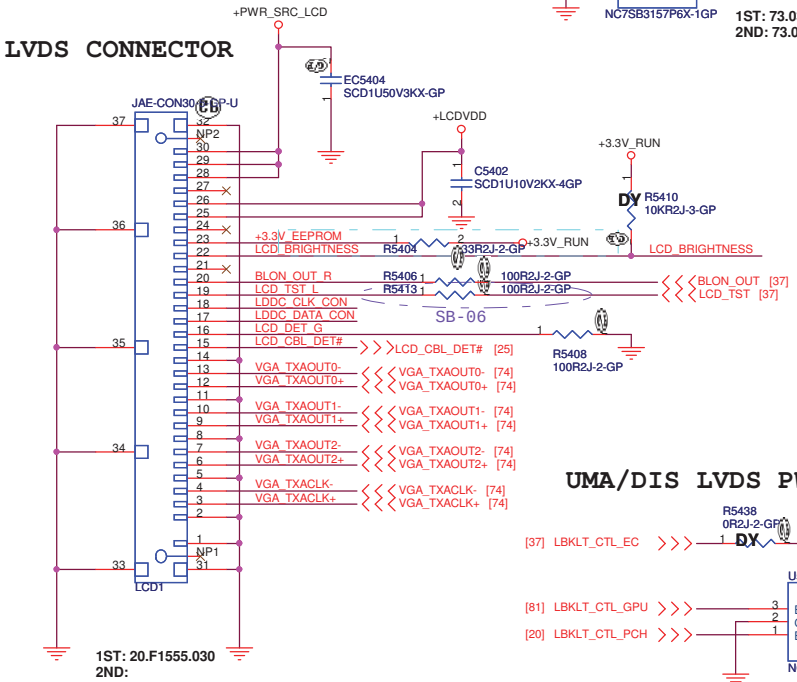
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

1ST: 73.03157.C0H
2ND: 73.03157.E0J



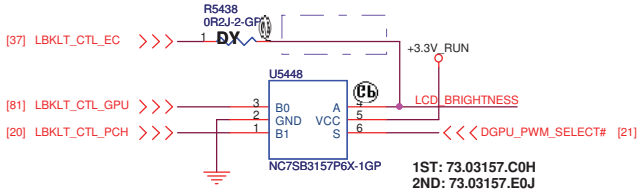
1ST: 73.03157.C0H
2ND: 73.03157.E0J

LVDS CONNECTOR



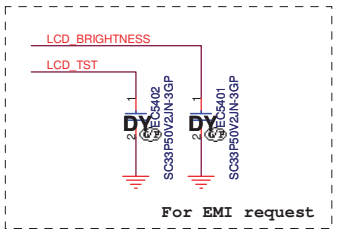
1ST: 20.F1555.030
2ND:

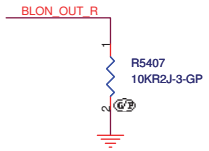
UMA/DIS LVDS PWM select circuit



1ST: 73.03157.C0H
2ND: 73.03157.E0J

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

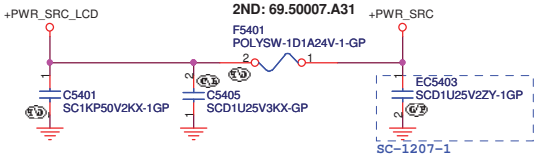




SSID = Inverter

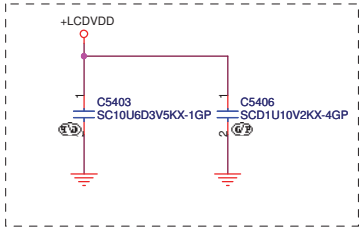
INVERTER POWER

1ST: 69.50007.A41
2ND: 69.50007.A31

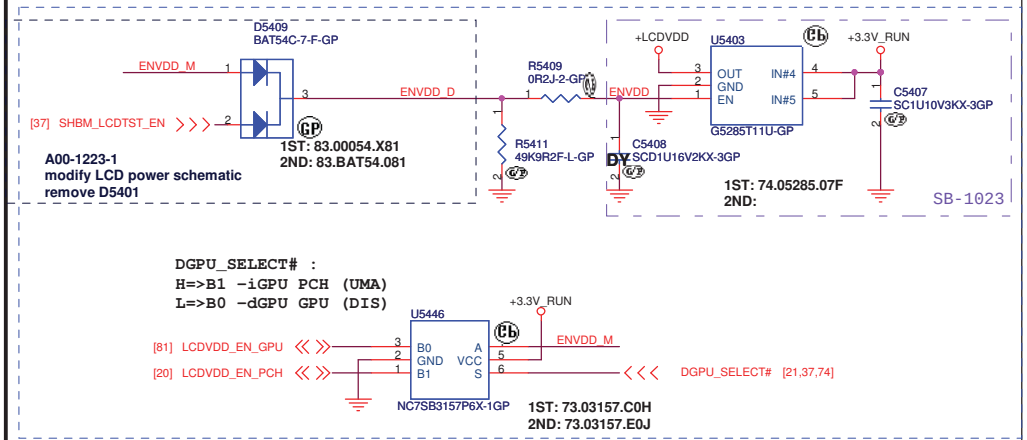


SSID = VIDEO

LCD POWER



SC-1125-2
add mux U5446 to select LCDVDD enable signal



DGPU_SELECT# :
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

1ST: 73.03157.C0H
2ND: 73.03157.E0J

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector
Size: Custom
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 54 of 88

SSID = VIDEO

A00-1218-1
change R5504, R5505, R5506 from 0R to 33R by EMI

A00-1218-1
change L5501, L5502, L5503 to 0R

[74] M_RED
[74] M_GREEN
[74] M_BLUE

R5504 M_RED_C 33R2J-2-GP
R5505 M_GREEN_C 33R2J-2-GP
R5506 M_BLUE_C 33R2J-2-GP

L5502 0R3J-0-U-GP CRT_R
L5501 0R3J-0-U-GP CRT_G
L5503 0R3J-0-U-GP CRT_B

R5502 150R2F-1-GP
R5501 150R2F-1-GP
R5503 150R2F-1-GP

C5508 SC8P250V2CC-GP
C5501 SC8P250V2CC-GP
C5506 SC8P250V2CC-GP

C5509 SC8P250V2CC-GP
C5507 SC8P250V2CC-GP
C5512 SC8P250V2CC-GP

CRT_R D5501 BAV99-4-GP +3.3V_RUN_GPU
CRT_G D5502 BAV99-4-GP +3.3V_RUN_GPU
CRT_B D5503 BAV99-4-GP +3.3V_RUN_GPU

Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

+5V_CRT_RUN
D5504 B0530WS-7-F-GP
+5V_RUN
C5510 SCD01U16V2KX-3GP

A00-0104-1
change CRT1 from 20.20431.015 to 20.20401.015

CRT1 VIDEO-15-127-GP-U
AFTP5502

CRT_R
CRT_G
CRT_B
+5V_CRT_RUN
DDC_DATA_CON
JVGA_HS [74]
JVGA_VS [74]
DDC_CLK_CON

1ST: 20.20401.015
2ND: 20.20479.015

C5502 SC33P50V2JN-3GP
C5504 SC33P50V2JN-3GP

AFTP5503 +5V_CRT_RUN
AFTP5501 DDC_DATA_CON
AFTP5509 DDC_CLK_CON
AFTP5507 CRT_R
AFTP5506 CRT_G
AFTP5508 CRT_B
AFTP5504 JVGA_HS
AFTP5505 JVGA_VS

DW
07/14 Change
1.Change CRT1 CONN PN from 20.20431.015 to 20.20401.015 base on ME emm files.

DW
07/07 Change
1.Change CRT DDC CLK/DAT Circuit

Close PCH
+3.3V_RUN
RN5510 SRN2K2J-1-GP
[20] GMCH_DDCDATA
[20] GMCH_DDCCLK

Close GPU
+3.3V_RUN_GPU
RN5511 SRN2K2J-1-GP
[81] CRT_DAT_DDC
[81] CRT_CLK_DDC

UMA/DIS CRT DDC CLK/DAT select circuit

U5542 +3.3V_RUN
[81] CRT_DAT_DDC
[20] GMCH_DDCDATA
B0 GND B1 VCC A S
DDC_DATA_CON2
EDID_SELECT#
NC7SB3157P6X-1GP

[21,54] EDID_SELECT#

U5543 +3.3V_RUN
[81] CRT_CLK_DDC
[20] GMCH_DDCCLK
B0 GND B1 VCC A S
DDC_CLK_CON2
EDID_SELECT#
NC7SB3157P6X-1GP

H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

+5V_CRT_RUN
RN5513 SRN2K2J-1-GP
DDC_DATA_CON
DDC_CLK_CON
C5519 SC22P50V2JN-4GP
C5520 SC10P50V2JN-4GP

A00-1218-1
change C5520 from 22p to 10p by EMI

5V @ CRT side

+3.3V_RUN
Q5517 DMN66D0LDW-7-GP
DDC_DATA_CON2
DDC_DATA_CON
DDC_CLK_CON2
DDC_CLK_CON

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: A3
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
Sheet 55 of 88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserve)

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 56 of 88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

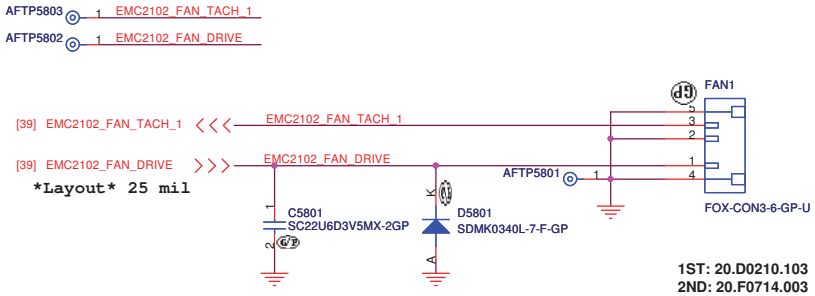
Title: HDMI Connector

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 57 of 88

SSID = Thermal

Fan Connector



1st Samsung

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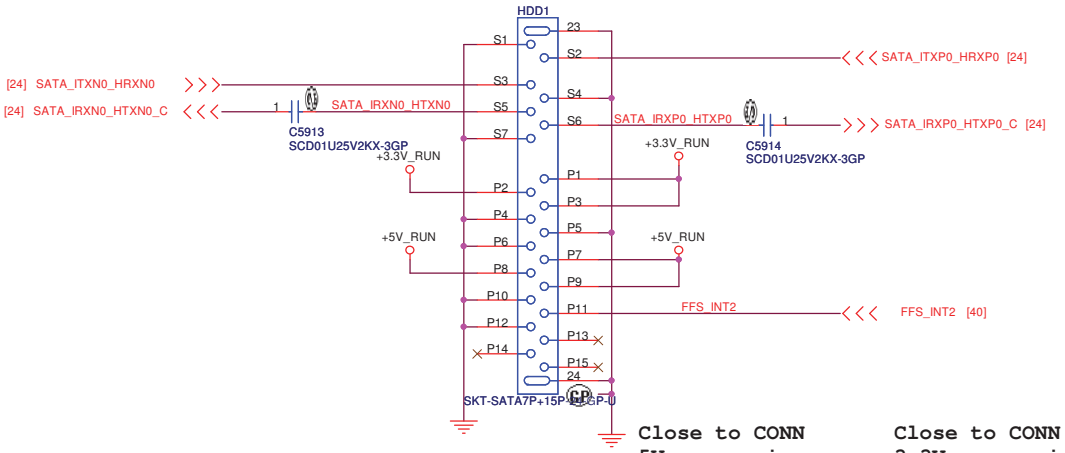
Taipei Hsien 221, Taiwan, R.O.C.

Title: FAN		
Size: A3	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 58 of 88	

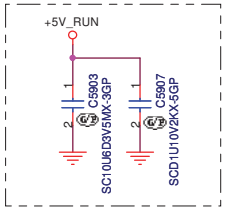
SSID = SATA

SATA HDD Connector

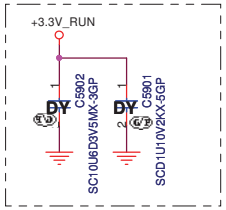


1ST: 22.10300.451
2ND:

Close to CONN
5V power pin



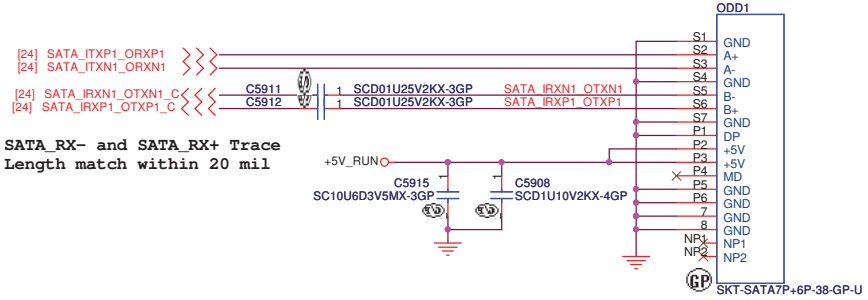
Close to CONN
3.3V power pin




```
SATA HDD Interface comment
*****************************
S1:GND
S2:RX+
S3:RX-
S4:GND
S5:TX-
S6:TX+
S7:GND
*****************************
P1------------ 3.3V
P2------------ 3.3V
P3------------ 3.3V
P4:GND
P5:GND / Dell Detected Pin
P6:GND
P7------------ 5V
P8------------ 5V
P9------------ 5V
P10--- GND
P11:Dell: FFS_INT for supported HDD
P12:GND
P13------------ 12V
P14------------ 12V
P15------------ 12V
*****************************
```

SSID = SATA

ODD Connector



SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

1ST: 62.10065.531
2ND: 62.10065.D21

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Title: HDD/ODD Connector

Size	Document Number	Rev
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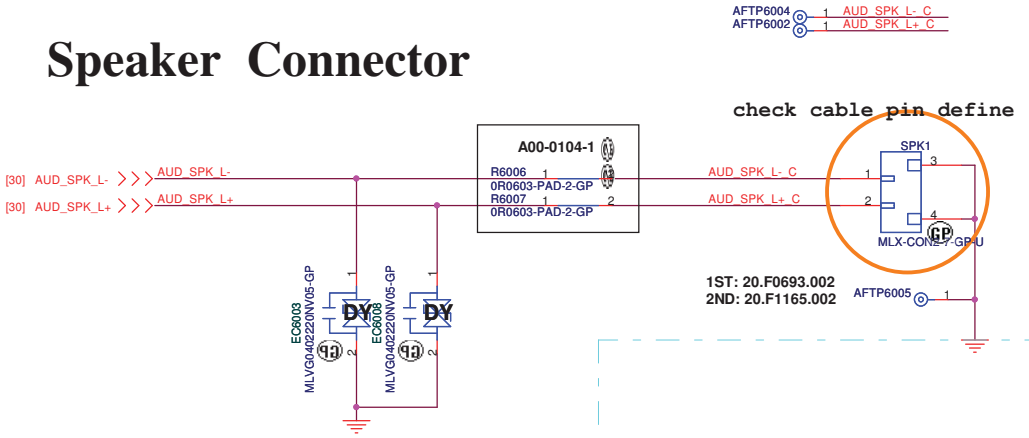
Date: Wednesday, January 13, 2010 Sheet 59 of 88

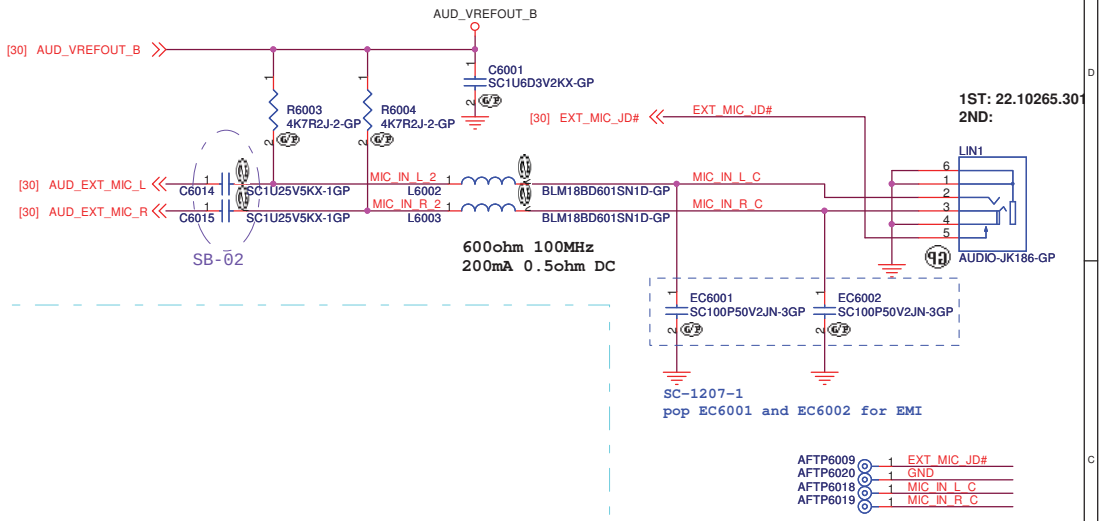
SSID = AUDIO

Speaker Connector



SSID = AUDIO

MIC IN

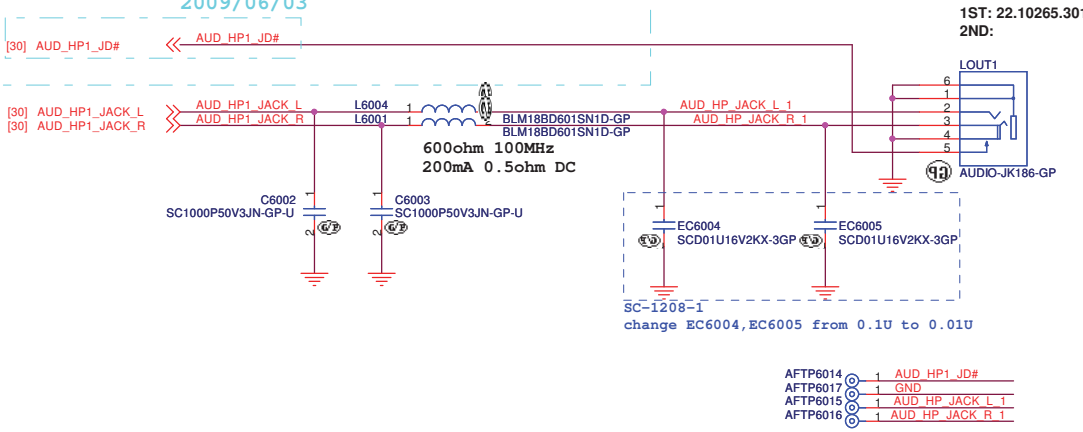


Delete Audio De-pop Circuit
2009/07/24

SSID = AUDIO

Head Phone

2009/06/03



Added HP circuit 2009/05/26

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Title: SPEAKER/MIC/AUDIO JACK

Size	Document Number	Rev
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Title

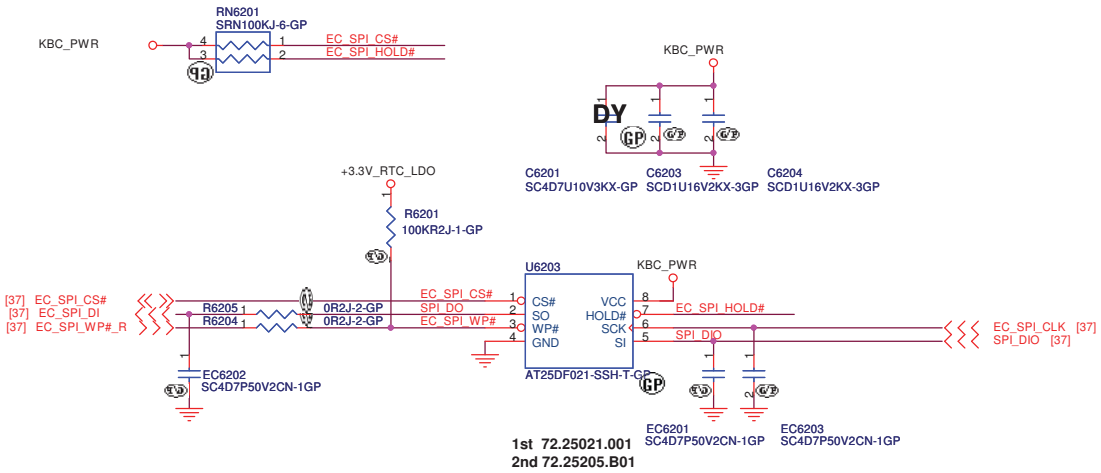
(Reserve)

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

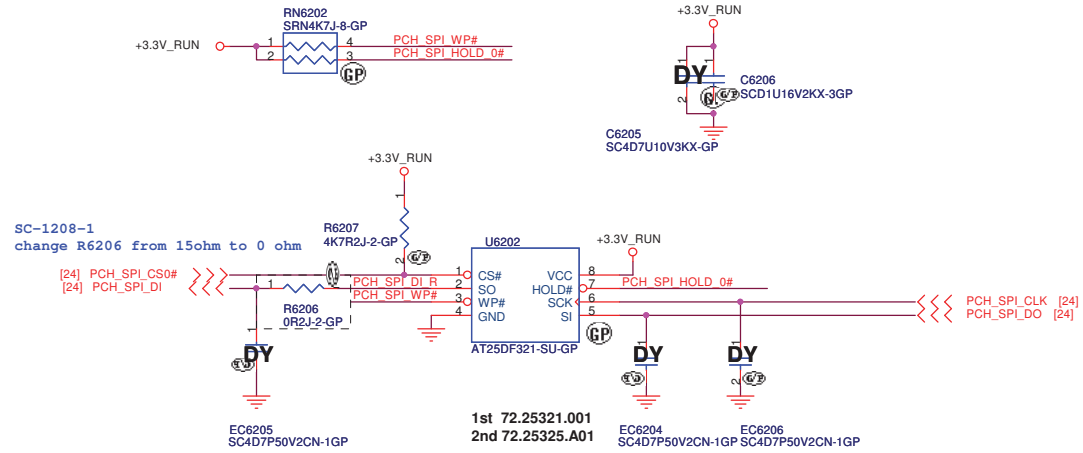
Date: Wednesday, January 13, 2010 Sheet 61 of 88

SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

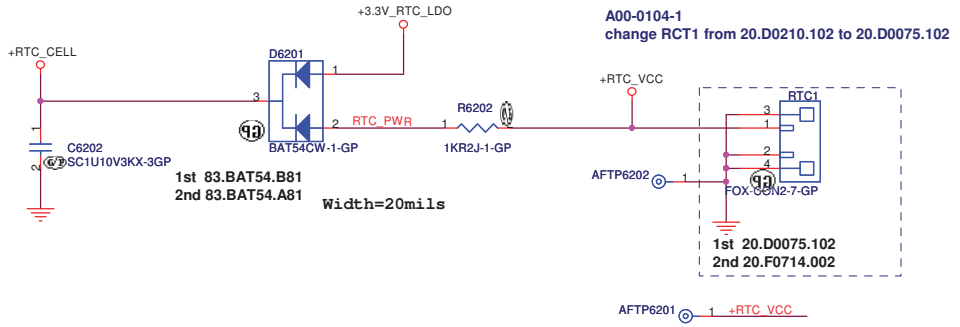


SPI FLASH ROM (32M bits) for PCH



SSID = RBATT

RTC Connector



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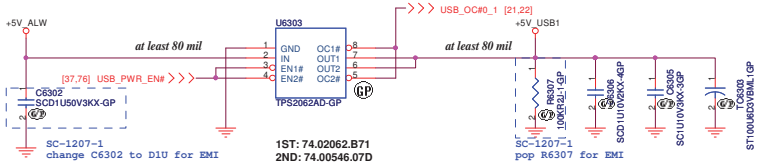
Title: EEPROM/RTC Connector

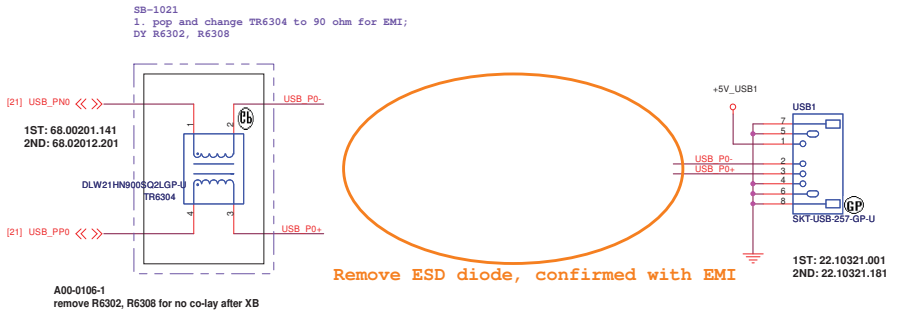
Size	Document Number	Rev
A3	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 62 of 88

SSID = USB

USB & ESATA Power SW

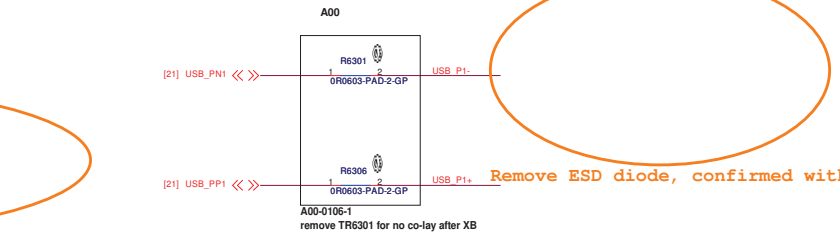


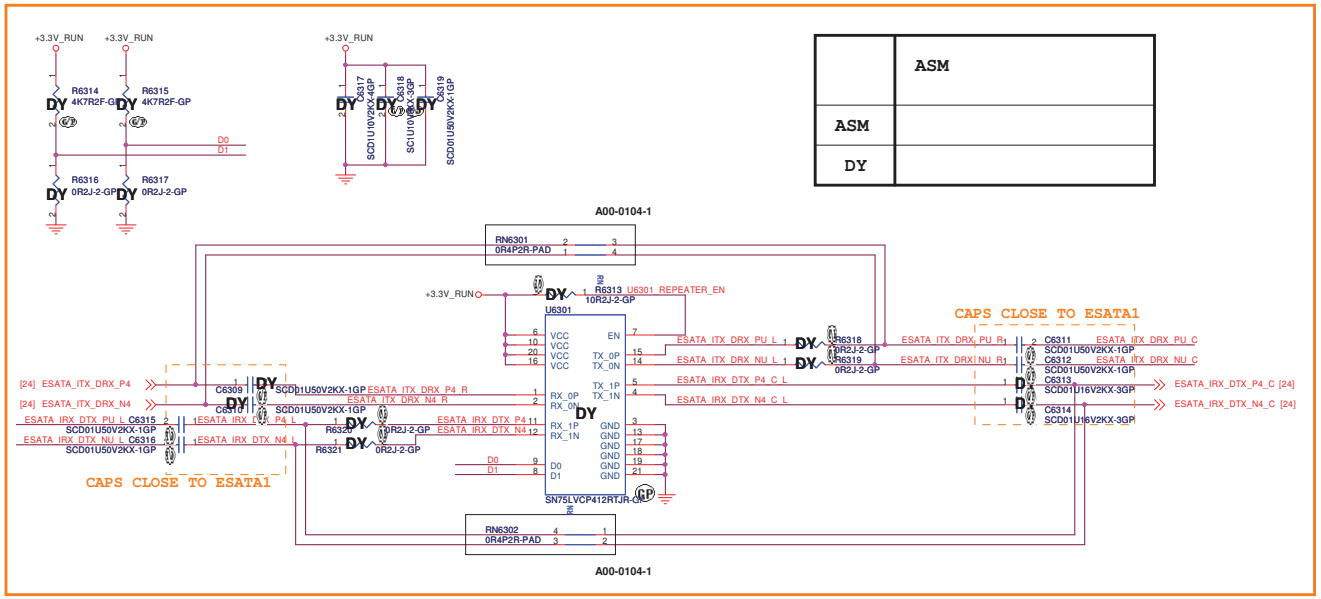


SSID = ESATA

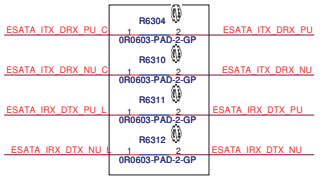
ESATA Power

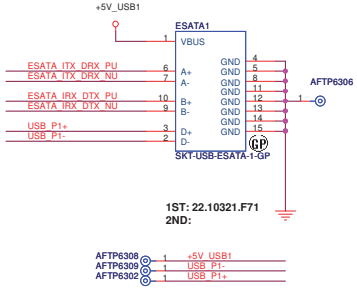
Share one power SW with USB port 1





	ASM
ASM	
DY	





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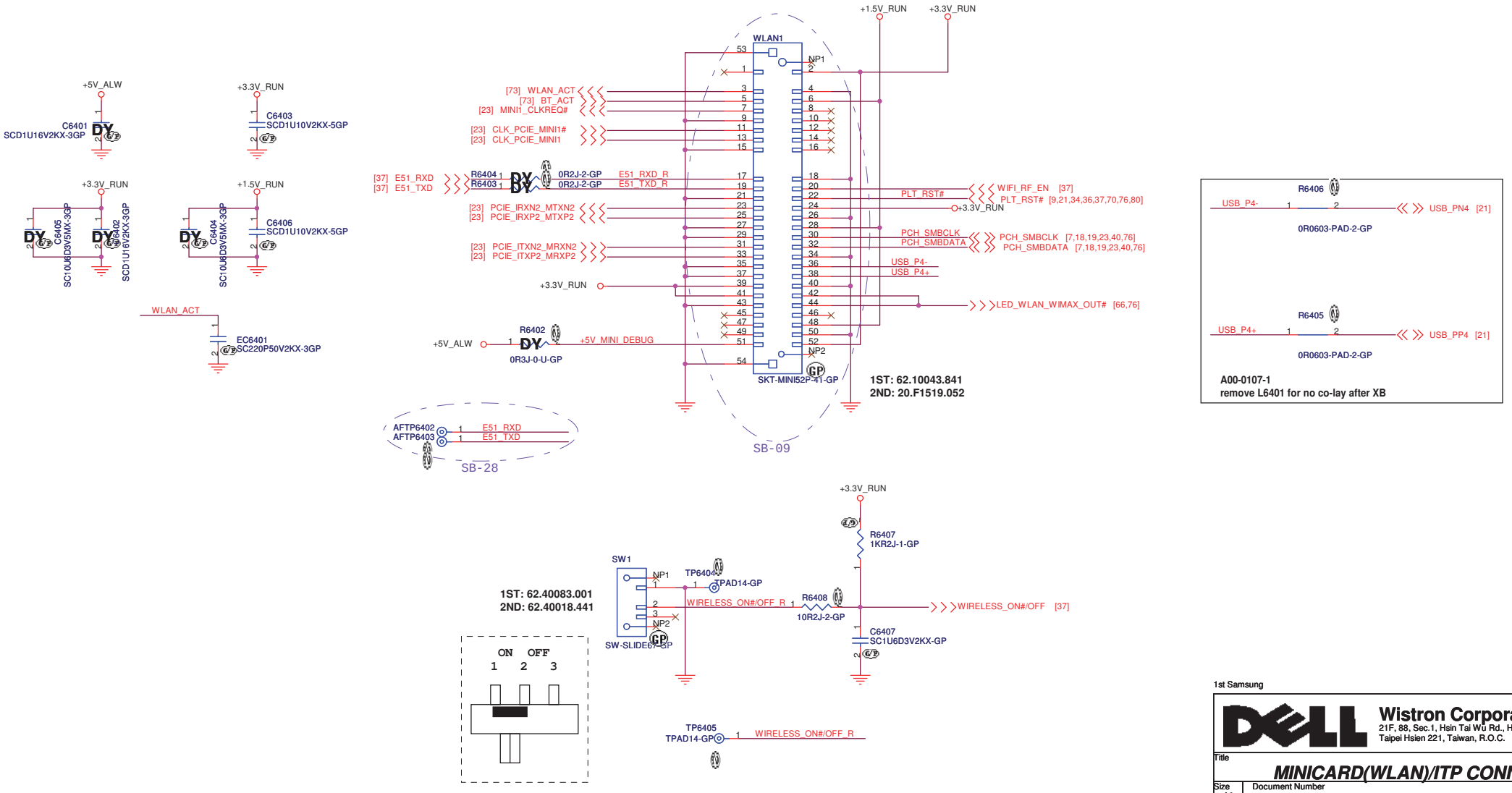
Title: USB/ESATA Port

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 63 of 88

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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Title: MINICARD(WLAN)/ITP CONN

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 64 of 88

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Title: WWAN Connector

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

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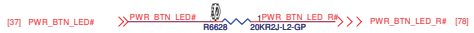
SSID = LED

For LED & Capacity board:

LED Type	Color	Power rail
BATTERY LED1	Amber(Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED

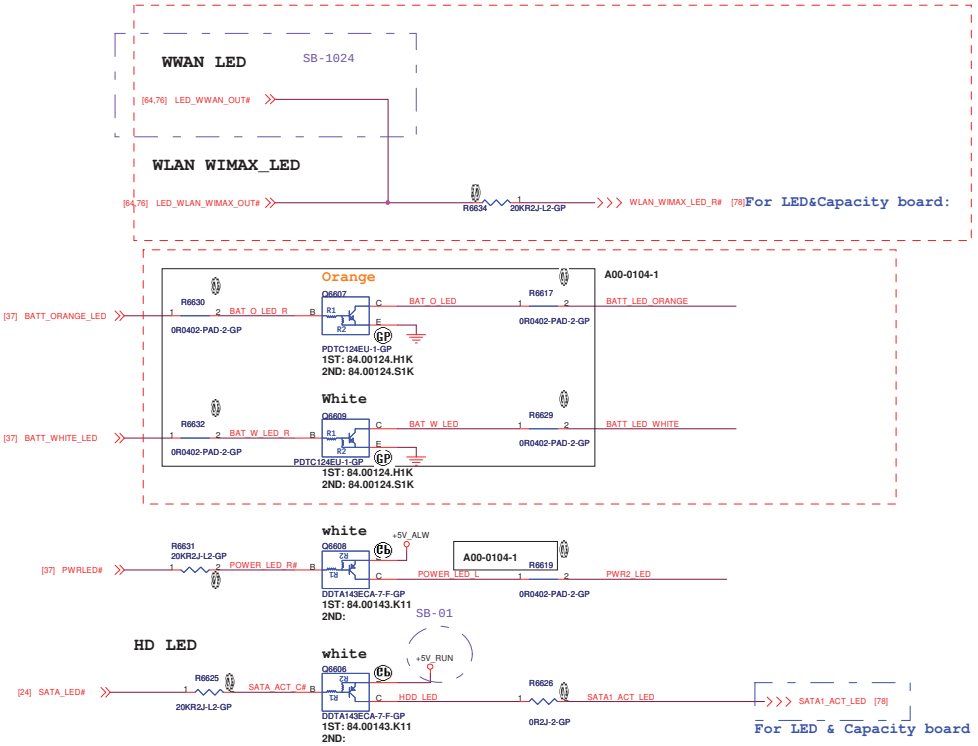


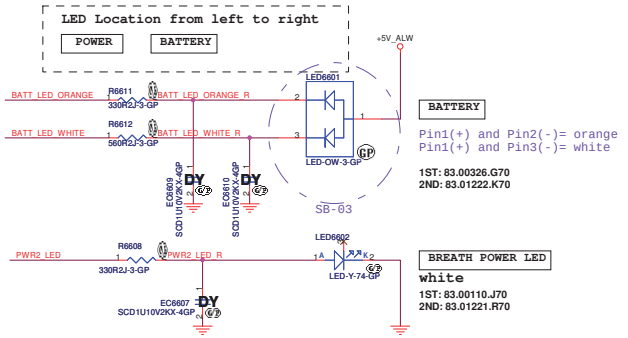
SCRLK LED

CAPS LED

NUM LED

Bluetooth LED





Remove HDD LED

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Title: LED

Size	Document Number	Rev
A2	Winery13 MB DIS	A00

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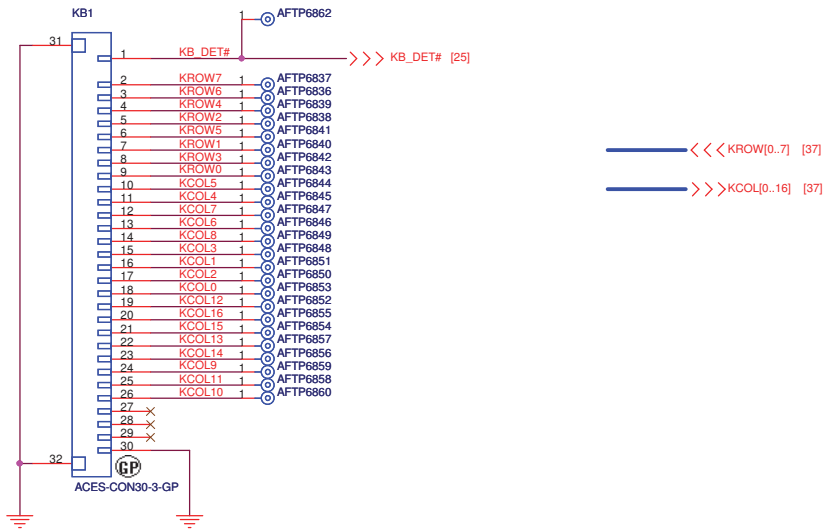
Title: *(Reserve)*

Size	Document Number	Rev
Custom	*Winery13 MB DIS*	*A00*

Date: Wednesday, January 13, 2010 Sheet 67 of 88

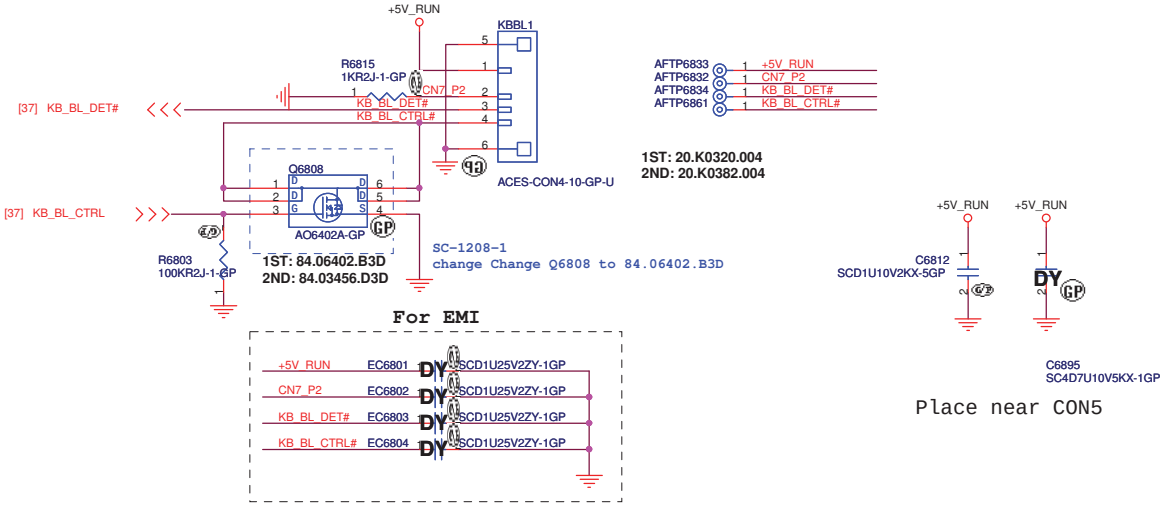
SSID = KBC

Internal KeyBoard Connector



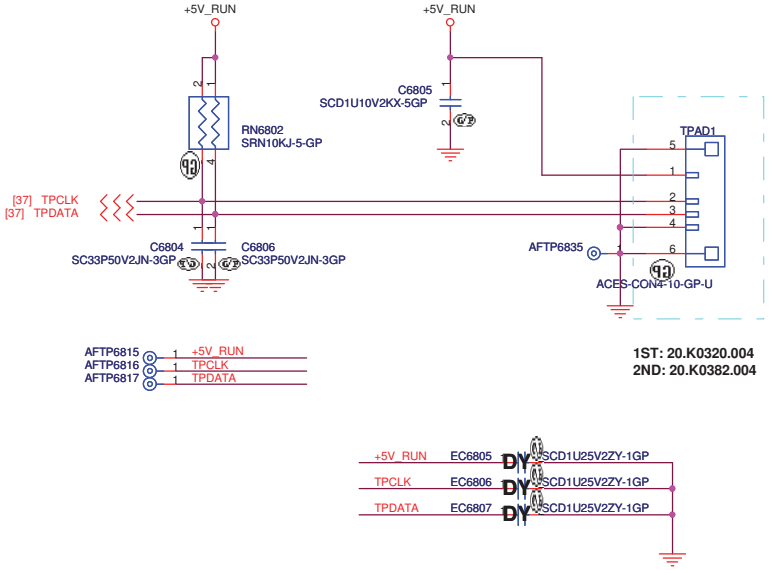
1ST: 20.K0421.030
2ND: 20.K0259.030

KB Backlight CONN



SSID = Touch.Pad

TouchPad Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title: Keyboard/Touch Pad
Size: Custom
Document Number: Winery13 MB DIS
Rev: A00
Date: Wednesday, January 13, 2010
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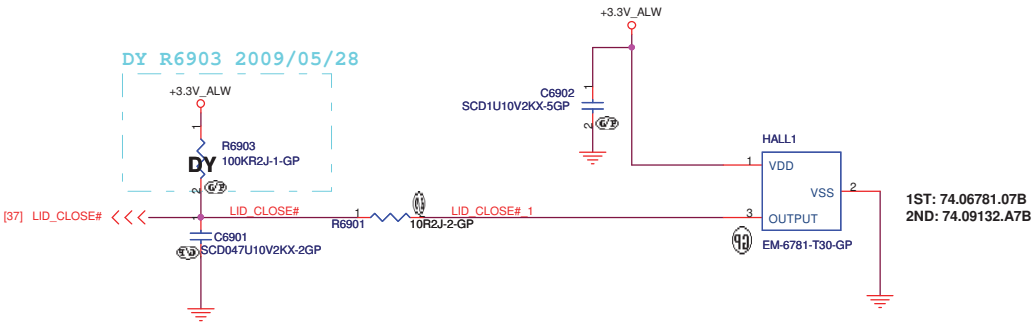
SSID = User.Interface

Hall Sensor Connector



1st Samsung

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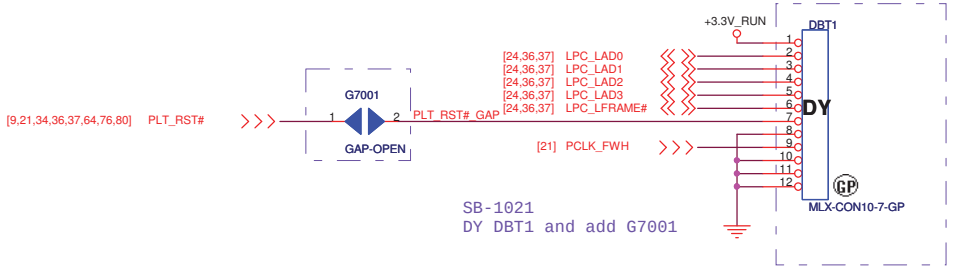
Title: Hall sensor

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 69 of 88

SSID = DEBUG PORT

GOLDEN FINGER FOR DEBUG BOARD



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Title: Debug port		
Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet 70 of 88	

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Title

(Reserve)

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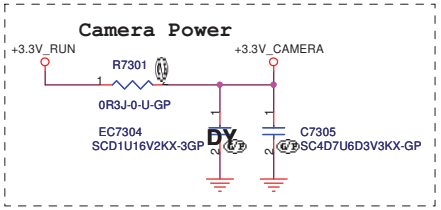
Title: Braidwood

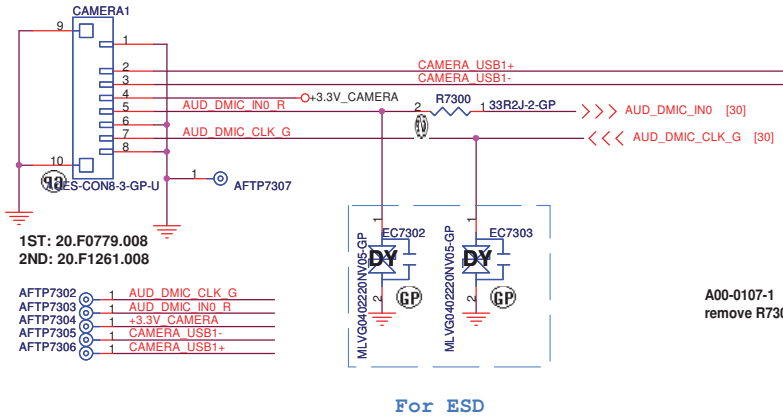
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

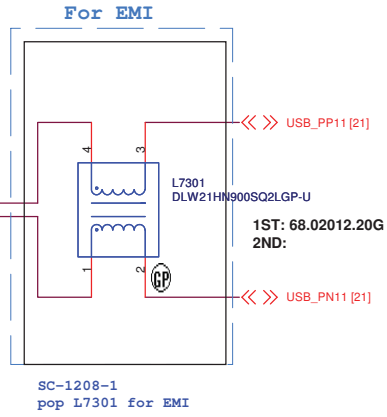
Date: Wednesday, January 13, 2010 | Sheet 72 of 88

SSID = User.Interface

Camera Connector



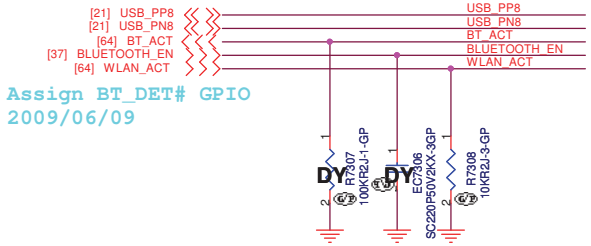


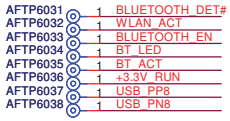


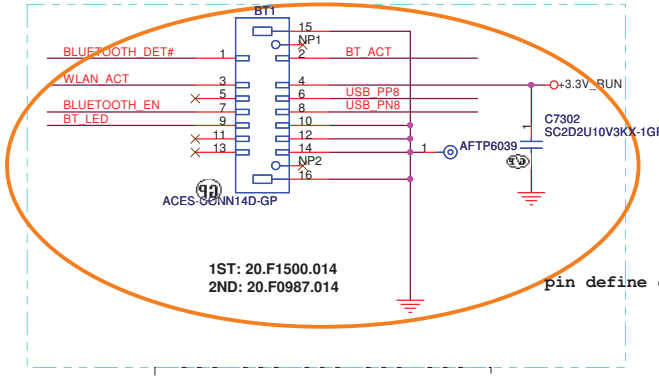
A00-0107-1
remove R7302, R7303 for no co-lay after XB

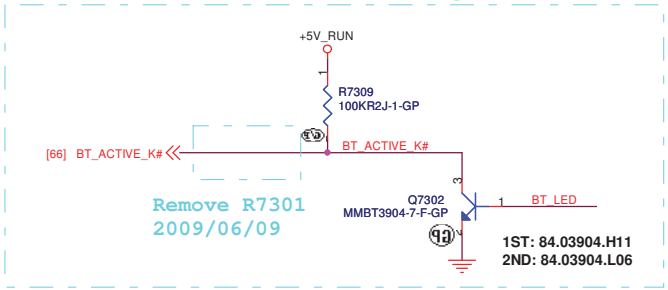
SSID = User.Interface

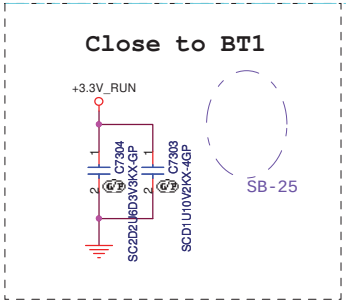
Bluetooth cable conn.











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Title: Camera CONN

Size	Document Number	Rev
A3	Winery13 MB DIS	A00

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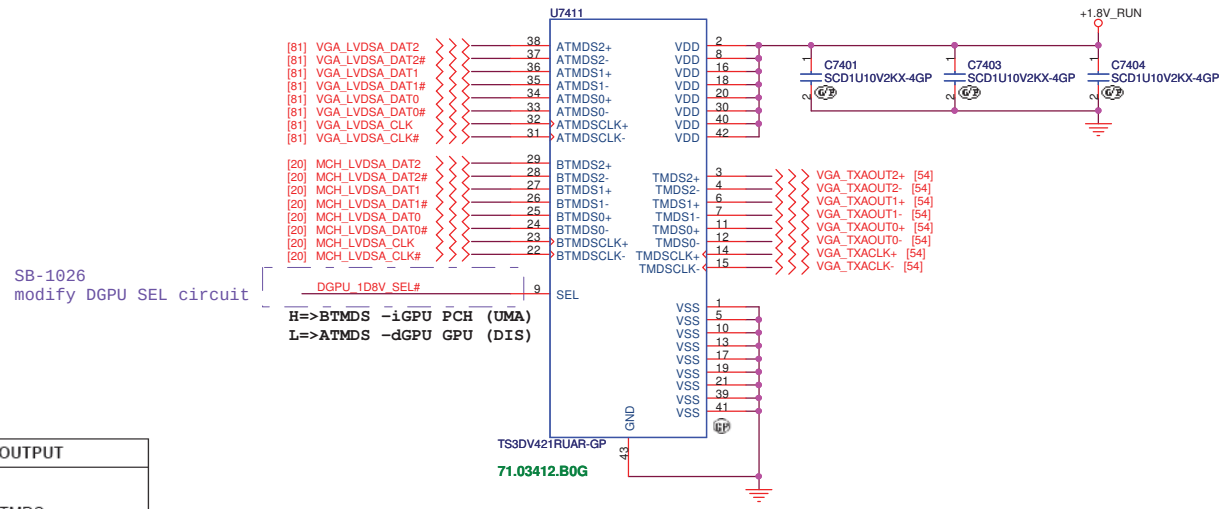
SSID = VIDEO

UMA/DIS LVDS signal select circuit

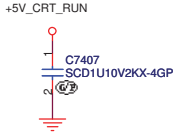


SB-1026
modify DGPU SEL circuit

H=>BTMDS -iGPU PCH (UMA)
L=>ATMDS -dGPU GPU (DIS)

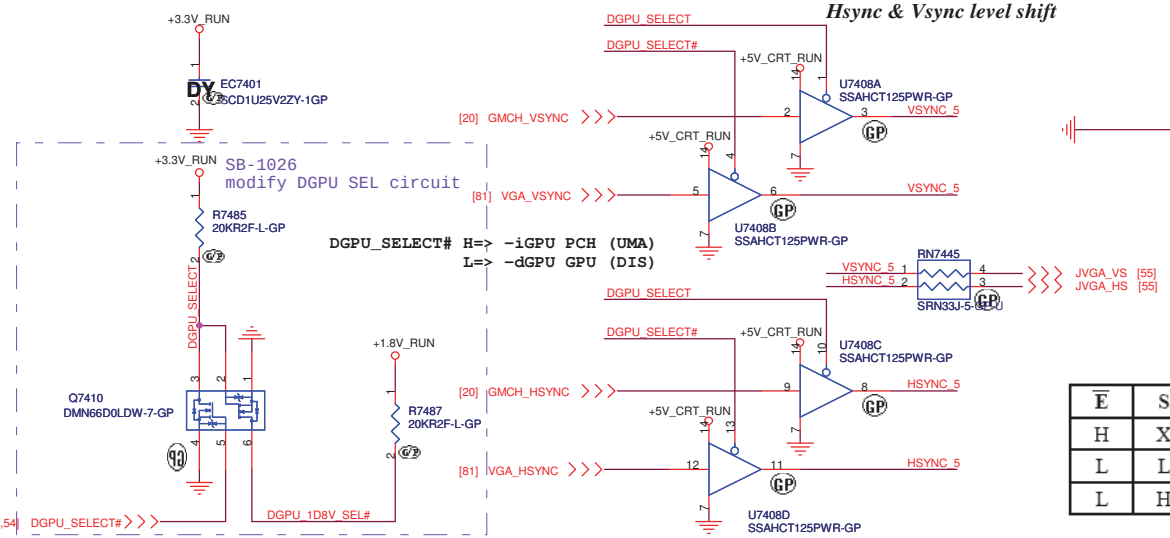
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

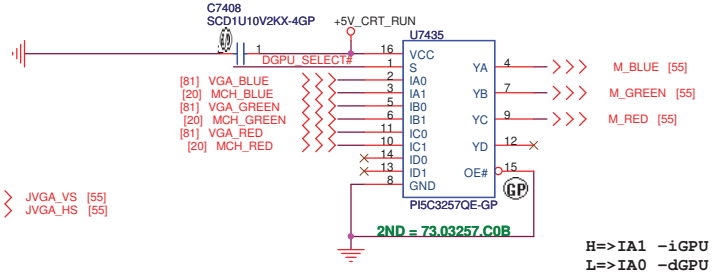


UMA/DIS CRT Hsync/Vsync select circuit

Hsync & Vsync level shift



UMA/DIS CRT signal select circuit



H=>IA1 -iGPU PCH (UMA)
L=>IA0 -dGPU GPU (DIS)

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: PX Swith-1
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 74 of 88

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Title: *(Reserve)*

Size: A3 | Document Number: *Winery13 MB DIS* | Rev: *A00*

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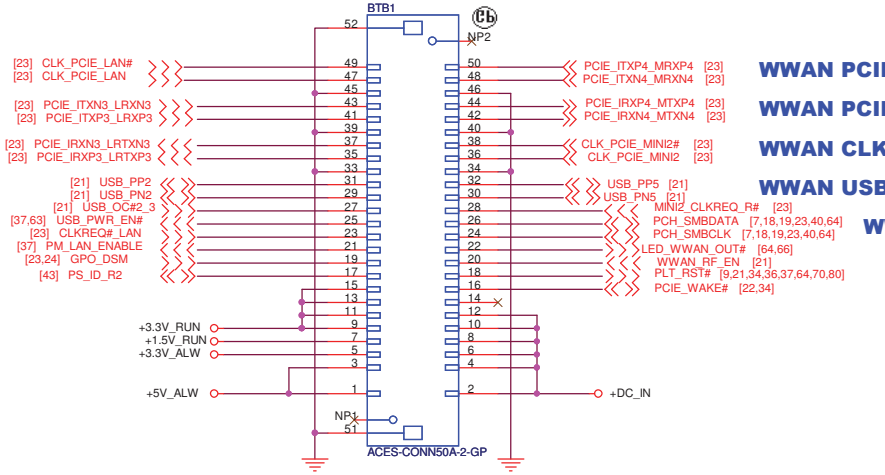
DC_IN baord CON

+DC_IN	:	19.5V/85W
+3.3V_RUN	:	3300mA
+5V_ALW	:	1000mA
+1.5V_RUN	:	500mA
+3.3V_ALW	:	58mA

Please reoute 300 mil at least.

LAN CLK
LAN PCIE
LAN PCIE
USB PORT2

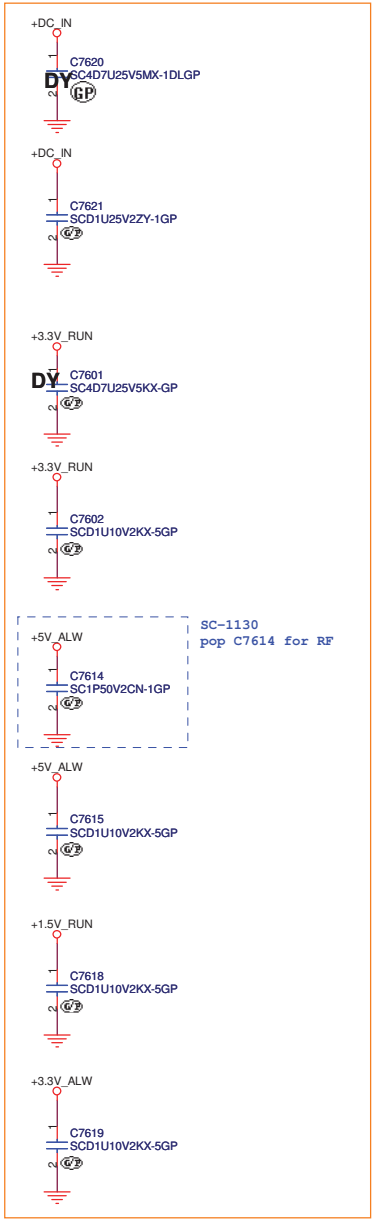


WWAN PCIE
WWAN PCIE
WWAN CLK
WWAN USB
WWAN SMBUS

Remove AFTP test point
Confirmed with AFTE.

1ST: 20.F1631.050
2ND:

Place near BTB1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC_IN Board BTB Connector
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 76 of 88

(Blank)

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio BD/IO BD CONN

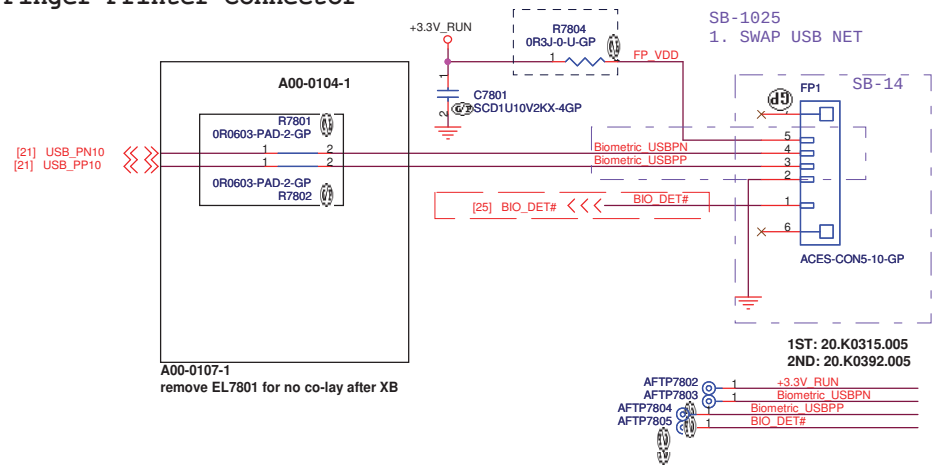
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 77 of 88

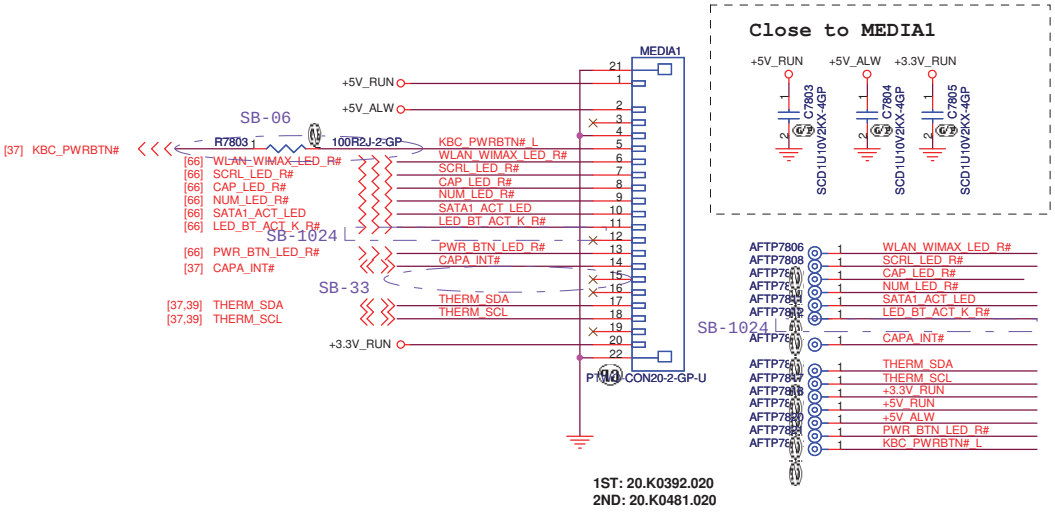
SSID = User.Interface

Finger Printer Connector

A00-1223-1
1. dummy FP1 pin6, pin7 for power pin short to GND when plug in cable issue
2. add damping resister R7804



LED&Capacity board CONN



1ST: 20.K0392.020
2ND: 20.K0481.020

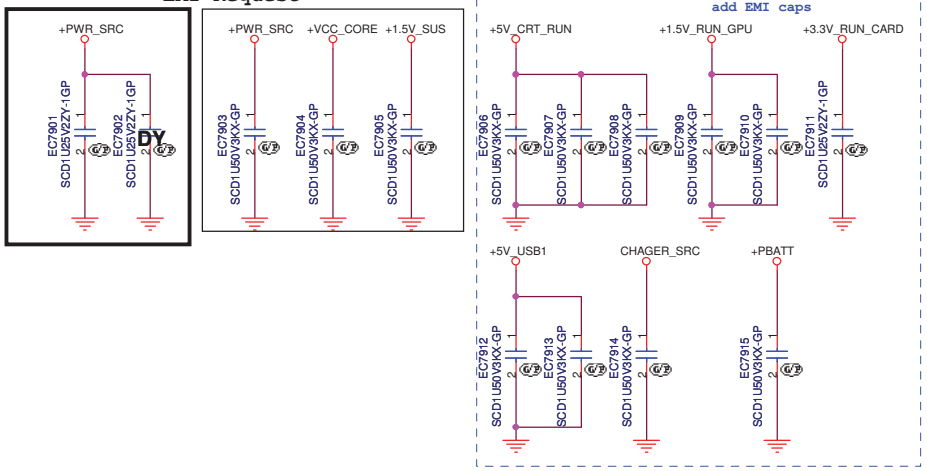
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

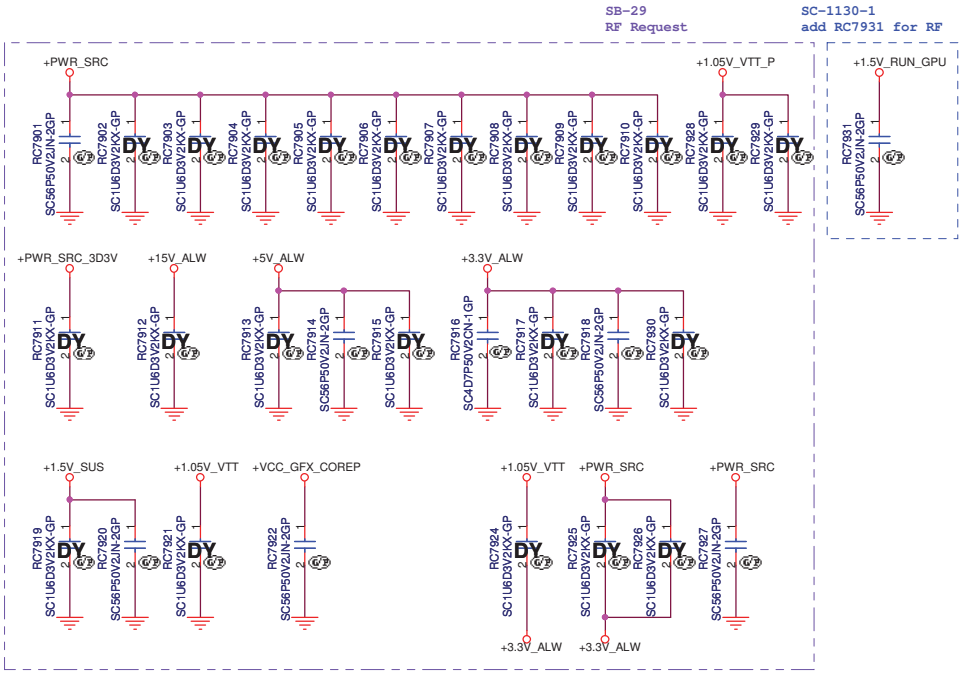
Title: Finger Printer/Felica/Capacity
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 78 of 88

SSID = EMI

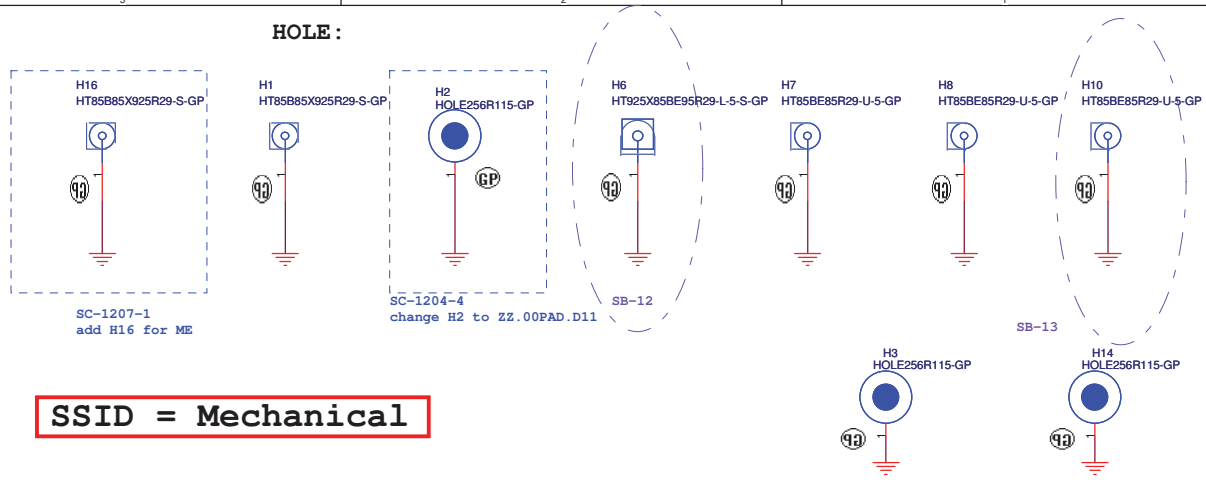
EMI Request



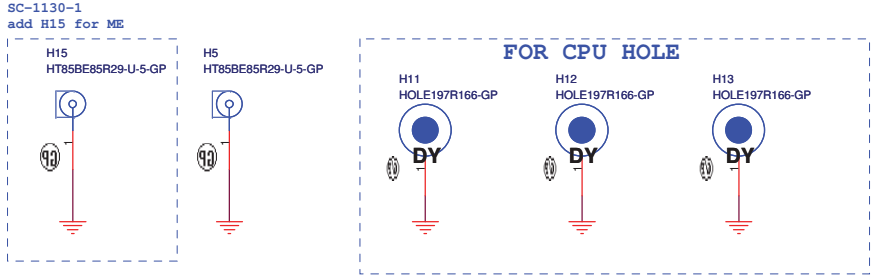
SSID = RF

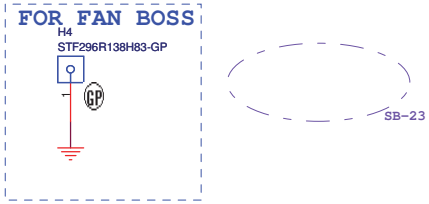


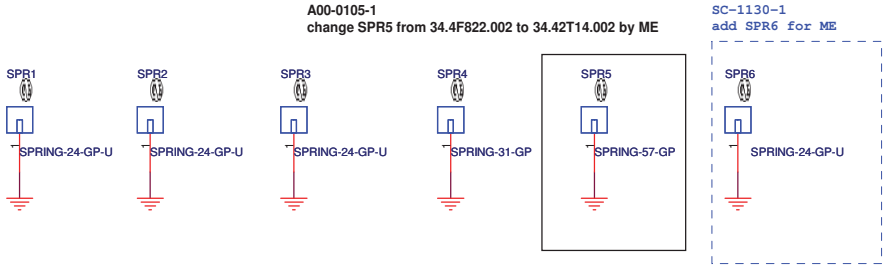
HOLE:



SSID = Mechanical







1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Miscellaneous Components***

Size: Custom | Document Number: ***Winery13 MB DIS*** | Rev: ***A00***

Date: Wednesday, January 13, 2010 | Sheet 79 of 88

SSID = VIDEO

PCIE_MTX_GRX_P[0..15] PCIE_MTX_GRX_P[0..15] [8]
PCIE_MTX_GRX_N[0..15] PCIE_MTX_GRX_N[0..15] [8]
PCIE_MRX_GTX_P[0..15] PCIE_MRX_GTX_P[0..15] [8]
PCIE_MRX_GTX_N[0..15] PCIE_MRX_GTX_N[0..15] [8]

U8001B 2 OF 7

PCIE_MTX_GRX_P0	AE12	PEX_RX0	AD10	PCIE_MRX_GTX_C_P0	C8033	SCD1U10V2KX-5GP PCIE_MRX_GTX_P0
PCIE_MTX_GRX_N0	AF12	PEX_RX0#	AD11	PCIE_MRX_GTX_C_N0	C8034	SCD1U10V2KX-5GP PCIE_MRX_GTX_N0
PCIE_MTX_GRX_P1	AG12	PEX_RX1	AD12	PCIE_MRX_GTX_C_P1	C8035	SCD1U10V2KX-5GP PCIE_MRX_GTX_P1
PCIE_MTX_GRX_N1	AG13	PEX_RX1#	AC12	PCIE_MRX_GTX_C_N1	C8036	SCD1U10V2KX-5GP PCIE_MRX_GTX_N1
PCIE_MTX_GRX_P2	AF13	PEX_RX2	AB11	PCIE_MRX_GTX_C_P2	C8037	SCD1U10V2KX-5GP PCIE_MRX_GTX_P2
PCIE_MTX_GRX_N2	AE13	PEX_RX2#	AB12	PCIE_MRX_GTX_C_N2	C8038	SCD1U10V2KX-5GP PCIE_MRX_GTX_N2
PCIE_MTX_GRX_P3	AE15	PEX_RX3	AD13	PCIE_MRX_GTX_C_P3	C8039	SCD1U10V2KX-5GP PCIE_MRX_GTX_P3
PCIE_MTX_GRX_N3	AF15	PEX_RX3#	AD14	PCIE_MRX_GTX_C_N3	C8040	SCD1U10V2KX-5GP PCIE_MRX_GTX_N3
PCIE_MTX_GRX_P4	AG15	PEX_RX4	AD15	PCIE_MRX_GTX_C_P4	C8042	SCD1U10V2KX-5GP PCIE_MRX_GTX_P4
PCIE_MTX_GRX_N4	AG16	PEX_RX4#	AC15	PCIE_MRX_GTX_C_N4	C8043	SCD1U10V2KX-5GP PCIE_MRX_GTX_N4
PCIE_MTX_GRX_P5	AF16	PEX_RX5	AB14	PCIE_MRX_GTX_C_P5	C8044	SCD1U10V2KX-5GP PCIE_MRX_GTX_P5
PCIE_MTX_GRX_N5	AE16	PEX_RX5#	AB15	PCIE_MRX_GTX_C_N5	C8045	SCD1U10V2KX-5GP PCIE_MRX_GTX_N5
PCIE_MTX_GRX_P6	AE18	PEX_RX6	AC16	PCIE_MRX_GTX_C_P6	C8047	SCD1U10V2KX-5GP PCIE_MRX_GTX_P6
PCIE_MTX_GRX_N6	AF18	PEX_RX6#	AD16	PCIE_MRX_GTX_C_N6	C8048	SCD1U10V2KX-5GP PCIE_MRX_GTX_N6
PCIE_MTX_GRX_P7	AG18	PEX_RX7	AD17	PCIE_MRX_GTX_C_P7	C8050	SCD1U10V2KX-5GP PCIE_MRX_GTX_P7
PCIE_MTX_GRX_N7	AG19	PEX_RX7#	AD18	PCIE_MRX_GTX_C_N7	C8051	SCD1U10V2KX-5GP PCIE_MRX_GTX_N7
PCIE_MTX_GRX_P8	AF19	PEX_RX8	AC18	PCIE_MRX_GTX_C_P8	C8052	SCD1U10V2KX-5GP PCIE_MRX_GTX_P8
PCIE_MTX_GRX_N8	AE19	PEX_RX8#	AB18	PCIE_MRX_GTX_C_N8	C8053	SCD1U10V2KX-5GP PCIE_MRX_GTX_N8
PCIE_MTX_GRX_P9	AE21	PEX_RX9	AB19	PCIE_MRX_GTX_C_P9	C8054	SCD1U10V2KX-5GP PCIE_MRX_GTX_P9
PCIE_MTX_GRX_N9	AF21	PEX_RX9#	AB20	PCIE_MRX_GTX_C_N9	C8055	SCD1U10V2KX-5GP PCIE_MRX_GTX_N9
PCIE_MTX_GRX_P10	AG21	PEX_RX10	AD19	PCIE_MRX_GTX_C_P10	C8056	SCD1U10V2KX-5GP PCIE_MRX_GTX_P10
PCIE_MTX_GRX_N10	AG22	PEX_RX10#	AD20	PCIE_MRX_GTX_C_N10	C8057	SCD1U10V2KX-5GP PCIE_MRX_GTX_N10
PCIE_MTX_GRX_P11	AF22	PEX_RX11	AD21	PCIE_MRX_GTX_C_P11	C8058	SCD1U10V2KX-5GP PCIE_MRX_GTX_P11
PCIE_MTX_GRX_N11	AE22	PEX_RX11#	AC21	PCIE_MRX_GTX_C_N11	C8077	SCD1U10V2KX-5GP PCIE_MRX_GTX_N11
PCIE_MTX_GRX_P12	AE24	PEX_RX12	AB21	PCIE_MRX_GTX_C_P12	C8078	SCD1U10V2KX-5GP PCIE_MRX_GTX_P12
PCIE_MTX_GRX_N12	AF24	PEX_RX12#	AB22	PCIE_MRX_GTX_C_N12	C8079	SCD1U10V2KX-5GP PCIE_MRX_GTX_N12
PCIE_MTX_GRX_P13	AG24	PEX_RX13	AC22	PCIE_MRX_GTX_C_P13	C8080	SCD1U10V2KX-5GP PCIE_MRX_GTX_P13
PCIE_MTX_GRX_N13	AF25	PEX_RX13#	AD22	PCIE_MRX_GTX_C_N13	C8081	SCD1U10V2KX-5GP PCIE_MRX_GTX_N13
PCIE_MTX_GRX_P14	AG25	PEX_RX14	AD23	PCIE_MRX_GTX_C_P14	C8082	SCD1U10V2KX-5GP PCIE_MRX_GTX_P14
PCIE_MTX_GRX_N14	AG26	PEX_RX14#	AD24	PCIE_MRX_GTX_C_N14	C8083	SCD1U10V2KX-5GP PCIE_MRX_GTX_N14
PCIE_MTX_GRX_P15	AE27	PEX_RX15	AE25	PCIE_MRX_GTX_C_P15	C8084	SCD1U10V2KX-5GP PCIE_MRX_GTX_P15
PCIE_MTX_GRX_N15	AE27	PEX_RX15#	AE26	PCIE_MRX_GTX_C_N15	C8085	SCD1U10V2KX-5GP PCIE_MRX_GTX_N15

+1.05V_GFX_PCIE

SC22U6D3V5MX-2GP C8069 SC1U6D3V5KX-1GP C8074 SC4D7U6D3V3KX-GP C8064 SC1U10V2KX-1GP C8067 SC1U6D3V2KX-GP C8068

Place near GPU

SCD1U16V2KX-3GP C8066 SCD1U16V2KX-3GP C8065

Place under GPU

Revised decoupling C 2009/05/28

AB13 AB16 AB17 AB7 AB8 AB9 AC13 AC7 AD6 AE6 AF6 AG6 PEX_IOVDDQ

PEX_IOVDD AC9 AD7 AD8 AE7 AF7 AG7

PEX_REFCLK AB10 CLK_PCIE_VGA CLK_PCIE_VGA [23]
PEX_REFCLK# AC10 CLK_PCIE_VGA# CLK_PCIE_VGA# [23]

PEX_TSTCLK_OUT AF10 PEX_TEST_PLL_CLK_OUT
PEX_TSTCLK_OUT# AE10 PEX_TEST_PLL_CLK_OUT# 200R2F-L-GP DY 1 R8002

PEX_CLKREQ# AE9 PEX_CLKREQ#
PEX_RST# AD9 PEX_RST#

PEX_SVDD_3V3 AG9 +3.3V_RUN_GPU
PEX_TERMP AG10 PEX_TERMP 1 R8001 2K49R2F-GP
PEX_PLLVDD AF9 +PEX_PLLVDD
PLLVDD K5 +GPU_PLLVDD

GT218-ES-S-A1-GP

Place under GPU

SCD1U16V2KX-3GP C8059 SCD1U16V2KX-3GP C8060

Place near GPU

+1.05V_GFX_PCIE

SC1U6D3V2KX-GP C8063 SC1U6D3V2KX-GP C8062 SC1U10V3KX-3GP C8061 SC4D7U6D3V3KX-GP C8073 SC10U6D3V5KX-1GP C8041 SC10U6D3V5KX-1GP

Revised decoupling C 2009/05/28

+3.3V_RUN_GPU

R8004 10KR2J-3-GP

Change R8004 resistor value 2009/06/05

2009/05/28

DW
07/10 NO STUFF
1. R8002 made NO STUFF

Remove 0.01u capacity C8039 2009/05/28

Place under GPU

SCD1U10V2KX-4GP C8049

Change power rail 2009/05/26

[25] DGPU_HOLD_RST#
[9,21,34,36,37,64,70,76] PLT_RST#

R8039 0R2J-2-GP DY C8086 SC1U6D3V2KX-GP

PLT_RST# RC

U8028 74LVC1G08GW-1-GP

+3.3V_RUN

PEX_RST#

R8017 100KR2J-1-GP

R8016 100KR2J-1-GP

DW
07/10 Change
1. Change U8028 from Operating voltage Range 5 to 3 V . Add
2.Added Pull-down resistors on GPU Reset [PEX_REST#] Pin

+PEX_PLLVDD PEX_PLLVDD = 120mA +1.05V_GFX_PCIE

L8011 IND-D1UH-20-GP 100NH 0603 DCR= 0.13 ohm

SCD1U16V2KX-3GP C8087 SC1U10V2KX-1GP C8070 SC4D7U6D3V3KX-GP C8046

NV suggestion. Place near GPU

Revised decoupling C 2009/05/28

Place under GPU

+GPU_PLLVDD (Pre pin)

SCD1U16V2KX-3GP C8071 SCD1U16V2KX-3GP C8072

Place near GPU SB-30

+1.05V_GFX_PCIE

L8005 BLM18SG121TN1D-GP

I SP_PLLVDD=45mA

SC1U10V2KX-1GP C8076 SC4D7U6D3V3KX-GP C8075

Revised decoupling C 2009/05/28

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 80 of 88

SSID = VIDEO

DW

07/05
1. LCD brightness control are separated by GPU,PCH,EC
2. LCD Power Enable control are separated by GPU,PCH,EC
3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
07/10 Not Reserve
1. Shorted LBKLT_CTL_GPU,LCDVDD_EN_GPU,PANEL_BKEN_GPU Not Reserve R8134,R8135,R8136.

U8001D

[54] LBKLT_CTL_GPU
[54] LCDVDD_EN_GPU
[37] PANEL_BKEN_GPU
[86] PWRCNTL_0
[86] PWRCNTL_1
[37] THERMTRIP_VGA#
[25] DEEPIDLE_WAKE_INT_R#

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO7 GPIO8 GPIO9 GPIO10 GPIO11 GPIO12 GPIO13 GPIO14 GPIO15 GPIO16 GPIO17 GPIO18 GPIO19

I2CA_SCL I2CA_SDA — CRT_CLK_DDC [55], CRT_DAT_DDC [55]
I2CB_SCL I2CB_SDA
I2CC_SCL I2CC_SDA — LDDC_CLK [54], LDDC_DATA [54]
I2CH_SCL I2CH_SDA
I2CS_SCL I2CS_SDA

JTAG_TDI JTAG_TDO JTAG_TMS JTAG_TRST# JTAG_TCK — TP_JTAG_TDI_GPU, TP_JTAG_TDO_GPU, TP_JTAG_TMS_GPU, JTAG_RST#_GPU, TP_JTAG_TCK_GPU, 1KR2J-1-GP, TP8102, TP8104, TP8101, TP8103, R8120

ROM_SO ROM_SI ROM_SCLK ROM_CS# — ROM_SO_GPU [83], ROM_SI_GPU [83], ROM_SCLK_GPU [83]

XTAL_IN XTAL_OUT — XTAL_IN, GPU_XTALOUT, 0R0402-PAD-2-GP, GPU_XTAL_IN, GPU_XTALOUT
XTAL_OUTBUFF XTAL_SSIN — XTALBUFF, XTAL_SSIN, R8124 10KR2J-3-GP, A00-0104-1

STRAP_CAL_PU_GND0 STRAP_CAL_PU_GND1 — R8133 40K2R2F-GP, R8126 40K2R2F-GP
MULTI_STRAP_REF0_GND MULTI_STRAP_REF1_GND

THERMDN THERMDP — VGA_THERMDC [39], VGA_THERMDA [39], C8102 SC2200P50V2KX-2GP
TESTMODE CEC SP_PLLVDD SPDIF — HDCP_TESTMODE, CEC, R8127 10KR2J-3-GP, R8107 10KR2J-3-GP, +3.3V_RUN_GPU, +SP_PLLVDD
BUFRST#

STRAP0 STRAP1 STRAP2 — [83] STRAP0, [83] STRAP1, [83] STRAP2

SC-1204-1
add EC8101,EC8102,EC8103 for EMI

[74] VGA_BLUE
[74] VGA_GREEN
[74] VGA_RED
EC8101 SC15P50V2JN-2-GP, EC8102 SC15P50V2JN-2-GP, EC8103 SC15P50V2JN-2-GP
R8116 150R2F-1-GP, R8118 150R2F-1-GP, R8119 150R2F-1-GP

DACA_BLUE DACA_GREEN DACA_RED
[74] VGA_VSYNC
[74] VGA_HSYNC
DACA_VSYNC DACA_HSYNC
DACA_RSET
+DACA_VDD
DACA_VREF
R8106 124R2F-1-GP, C8103 SCD1U10V2KX-2GP
DACB_BLUE DACB_GREEN DACB_RED
DACB_VSYNC DACB_HSYNC
DACB_RSET DACB_VDD DACB_VREF
DACB_VDD
R8111 10KR2F-2-GP

[83] STRAP0 [83] STRAP1 [83] STRAP2

GT218-ES-S-A1-GP

+3.3V_RUN_GPU
RN8112 SRN2K2J-1-GP
I2CB_SCL I2CB_SDA

Default X'tal

CLK GEN 27M select:

XTAL_IN R8123 DY 0R2J-2-GP CLK_VGA_27M [7]
XTAL_SSIN R8131 DY 0R2J-2-GP
R8132 10KR2J-3-GP DY
R8125 10KR2J-3-GP
Remove R8112, R8114 2009/06/09

VGA 27M	R8123	R8131	R8125	R8132
SS	DY	POP	DY	POP
NON-SS	POP	DY	POP	DY

Added CLK GEN 27M select circuit 2009/06/15
Added R8132 (DY) 2009/06/17

Main 82.30034.651
Second ?
X8101 XTAL-27MHZ-84-GP
GPU_XTAL_IN
GPU_XTALOUT
R8115 1MR2J-1-GP
C8135 SC15P50V2JN-2-GP
C8138 SC15P50V2JN-2-GP
SB-19

1st: HARMONY 82.30034.651
2nd: ITTI 82.30034.801
3rd: TXC 82.30034.681

+DACA_VDD = 120mA

Place near GPU
+3.3V_RUN_GPU
L8106 BLM18SG331TN1D-GP
C8153 SC4D7U6D3V2KX-2GP
C8154 SC1U6D3V2KX-2GP

Place under GPU
16mil
+DACA_VDD
C8144 SCD1U10V2KX-4GP
C8145 SCD1U10V2KX-4GP
C8118 SCD1U10V2KX-4GP
C8108 SC4700P50V2KX-1GP
C8107 SC470P50V2KX-3GP

Spec 300 ohm,
ESR<0.25 ohm

Revised decoupling C 2009/05/28

U8001C

[74] VGA_LVDSA_CLK
[74] VGA_LVDSA_CLK#
[74] VGA_LVDSA_DAT0
[74] VGA_LVDSA_DAT0#
[74] VGA_LVDSA_DAT1
[74] VGA_LVDSA_DAT1#
[74] VGA_LVDSA_DAT2
[74] VGA_LVDSA_DAT2#
IFPA_TXC IFPA_TXC# IFPA_TXD0 IFPA_TXD0# IFPA_TXD1 IFPA_TXD1# IFPA_TXD2 IFPA_TXD2# IFPA_TXD3 IFPA_TXD3#
+IFPAB_IOVDD — IFPA_IOVDD
+IFPAB_PLLVDD — IFPAB_PLLVDD
DY R8121 1KR2F-3-GP IFPAB_RSET 2009/05/28
IFPB_TXC IFPB_TXC# IFPB_TXD4 IFPB_TXD4# IFPB_TXD5 IFPB_TXD5# IFPB_TXD6 IFPB_TXD6# IFPB_TXD7 IFPB_TXD7#
+IFPAB_IOVDD — IFPB_IOVDD

DW30 LVDS only 1 chanel
Vendor confirm tie to +1.8V powe rail

DW30 not support HDMI
NV DG: pull-down 10K

IFPC_IOVDD R8135 1 10KR2J-3-GP
IFPC_PLLVDD R8134 10KR2J-3-GP
IFPC_L0 IFPC_L0# IFPC_L1 IFPC_L1# IFPC_L2 IFPC_L2# IFPC_L3 IFPC_L3#
IFPC_IOVDD IFPC_PLLVDD
IFPC_RSET
IFPC_AUX_I2CW_SCL IFPC_AUX_I2CW_SDA#

IFPD_L0 IFPD_L0# IFPD_L1 IFPD_L1# IFPD_L2 IFPD_L2# IFPD_L3 IFPD_L3#
IFPD_PLLVDD — IFPD_PLLVDD R8128 10KR2J-3-GP
IFPD_RSET
IFPD_AUX_I2CX_SCL IFPD_AUX_I2CX_SDA#
IFPDE_IOVDD — IFPDE_IOVDD R8129 10KR2J-3-GP
IFPE_L0 IFPE_L0# IFPE_L1 IFPE_L1# IFPE_L2 IFPE_L2# IFPE_L3 IFPE_L3#
IFPE_PLLVDD — IFPE_PLLVDD R8130 10KR2J-3-GP
IFPE_RSET
IFPE_AUX_I2CY_SCL IFPE_AUX_I2CY_SDA#

Unused IFP
Interfaces setting
2009/06/03

+IFPAB_IOVDD

+1.8V_RUN_GPU
L8107 BLM18PG181SN1D-GP
IFPAB_IOVDD = 300mA
C8126 SC4D7U6D3V2KX-4GP
C8149 SC1U6D3V2KX-GP
Place near GPU
Revised decoupling C 2009/05/28
Place under GPU near IFPA_IOVDD
C8150 SCD1U10V2KX-4GP
Place under GPU near IFPB_IOVDD
C8151 SCD1U10V2KX-4GP

+IFPAB_PLLVDD

Revised decoupling C 2009/05/28
Change power rail 2009/05/28
+1.05V_GFX_PCIE
L8108 BLM18PG181SN1D-GP
IFPAB_PLLVDD = 220mA
+IFPAB_PLLVDD
C8128 SC4D7U6D3V2KX-GP
C8152 SC1U6D3V2KX-GP
Place near GPU

SB-30
Place near GPU
+SP_PLLVDD
+1.05V_GFX_PCIE
L8110 BLM18SG121TN1D-GP
C8127 SC1U6D3V2KX-GP
C8130 SC4D7U6D3V2KX-GP
I SP_PLLVDD=45mA
Revised decoupling C 2009/05/28

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Title: VGA-LVDS/CRT/DP PORT
Size: A2 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 81 of 88

SSID = VIDEO

Revised decoupling C 2009/05/28

Place under GPU

+VCC_GFX_CORE

C8241 C8242 C8243 C8244 C8246 C8247 SCD01U16V2KX-3GP

C8248 C8249 C8250 C8234 SCD047U10V2KX-2GP SCD1U10V2KX-4GP

Place near GPU

C8240 SC4D7U6D3V3KX-GP

U8001F 6 OF 7

VDD DDR_VREF NC#J5 NC#D15 NC#C15 RFU_1 RFU_2 RFU_3 RFU_4 RFU_5 VDD33 VDD_SENSE VID_PLLVDD

GT218-ES-S-A1-GP

TPAD14-GP TP8203 TP_VDD_SENSE_E15

TPAD14-GP TP8205 TP_VDD_SENSE_W15

Place under GPU

C8229 C8230 C8232 SCD1U10V2KX-5GP

Place near GPU

+3.3V_RUN_GPU

C8211 SC1U6D3V2KX-GP C8231 SC4D7U6D3V3KX-GP

Revised decoupling C 2009/05/28

+GPU_PLLVDD

2009/05/28

"Remote Voltage Sensing" not used,reserve Test-Point.

U8001G 7 OF 7

GND GND_SENSE

GT218-ES-S-A1-GP

Change FBVDDQ power rail

2009/05/28

FBVDD/Q = 2.24A

+1.5V_RUN_GPU

U8001E 5 OF 7

FBVDDQ A13 B13 C13 D13 D14 E13 F13 F14 F15 F16 F17 F19 F22 H23 H26 J15 J16 J18 J19

GT218-ES-S-A1-GP

Place under GPU

C8209 C8222 C8235 C8251 C8252 C8253 SCD1U10V2KX-4GP

Place near GPU

C8219 SC1U10V3KX-3GP

Revised decoupling C 2009/05/28

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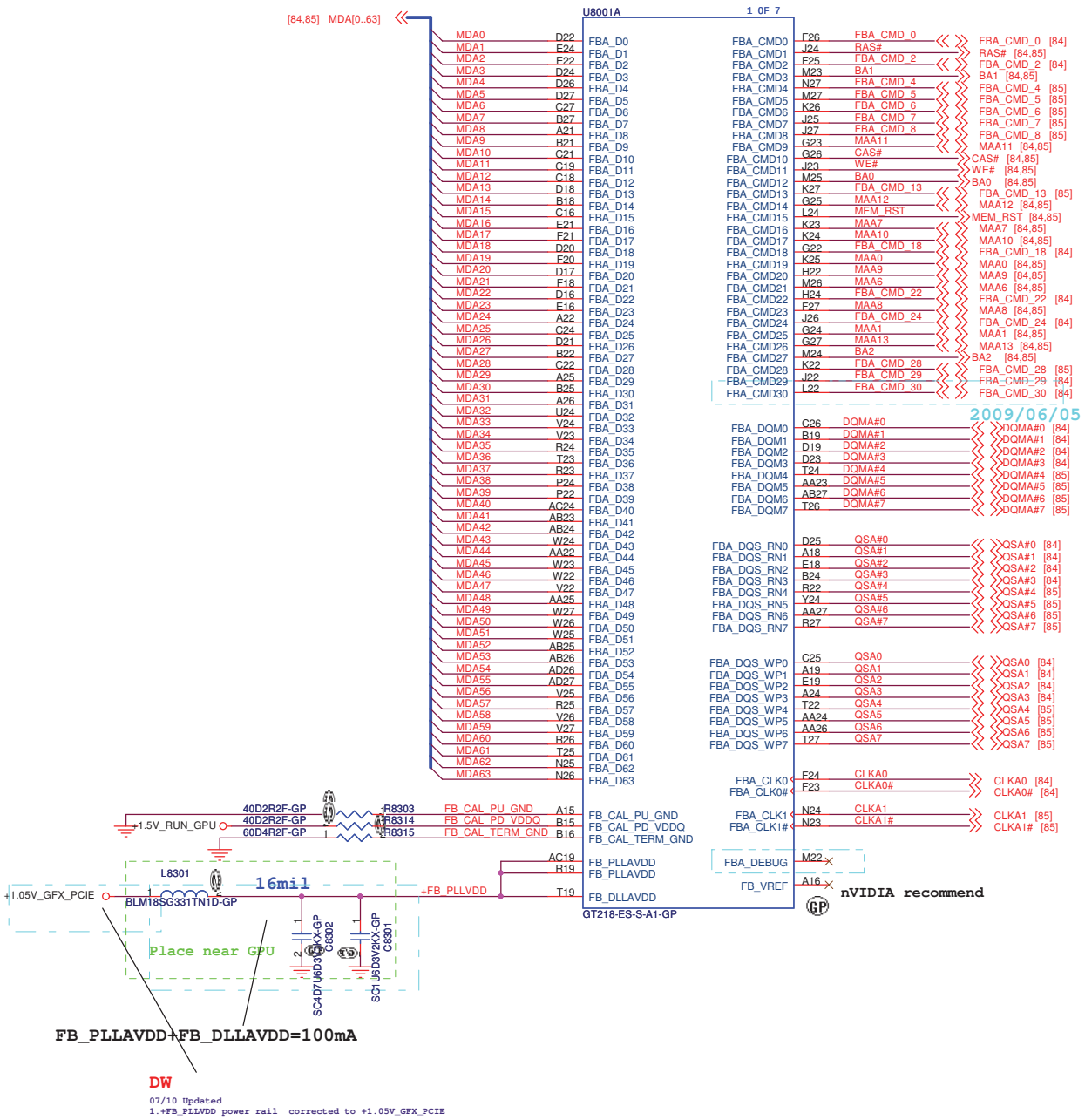
Title: VGA-POWER/GND(3/4)

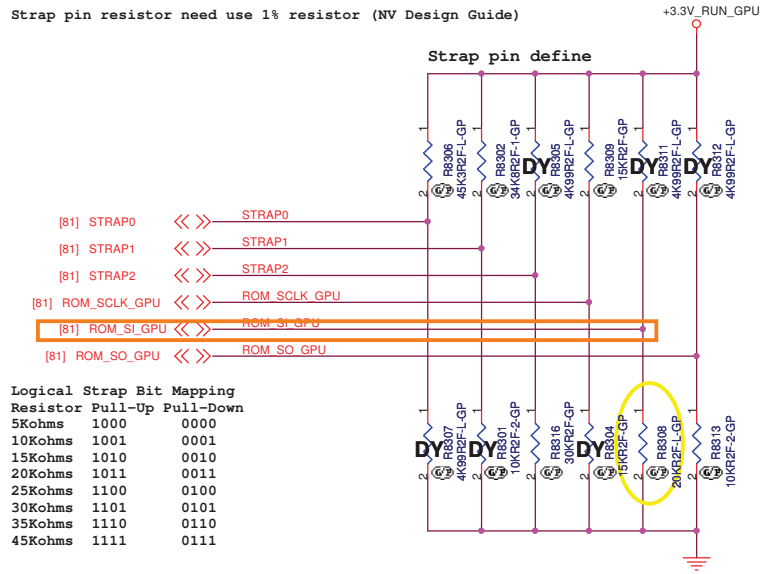
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 82 of 88

SSID = VIDEO



Strap pin resistor need use 1% resistor (NV Design Guide)



Logical Strap Bit Mapping

Resistor	Pull-Up	Pull-Down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

Strap0		Strap1		Strap2	
USER_BIT0	1	3GIO_PADCFG_LUT_ADR0	0	PCI_DEVID_0	1
USER_BIT1	1	3GIO_PADCFG_LUT_ADR1	1	PCI_DEVID_1	0
USER_BIT2	1	3GIO_PADCFG_LUT_ADR2	1	PCI_DEVID_2	1
USER_BIT3	1	3GIO_PADCFG_LUT_ADR3	1	PCI_DEVID_3	0
EDID is used		Reserved		N11M-GE1 GPU Device ID=0x0A75	

ROM_SI_GPU		ROM_SO_GPU		ROM_SCLK_GPU	
RAM_CFG0		VGA_DEVICE	1	PEX_PLL_EN_TERM	0
RAM_CFG1		SMB_ALT_ADDR	0	SLOT_CLK_CONFIG	1
RAM_CFG2		FB_0_BAR_SIZE	0	SUB_VENDOR	0
RAM_CFG3		XCLK_417	0	PCI_DEVID_4	1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)
If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K.

RAM_CFG[3:0]	Config	FB_BUS Width	Definitions
0000			
0001			
0010	64MX16	DDR3 64Bit	Hynix
0011	64MX16	DDR3 64Bit	Samsung
0100			Default
0101			
0110			
0111			

SUB_VENDOR		XCLK_417		PEX_PLL_EN_TERM	
0	No VBIOS ROM	0	277MHz(POR)	0	Disable (POR)
1	BIOS ROM present	1	Reserved	1	Enable

3GIO_PADCFG	USER[3:0]
0000	Desktop
1110	Notebook (POR)

1111 Use EDID to detect panel settings

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

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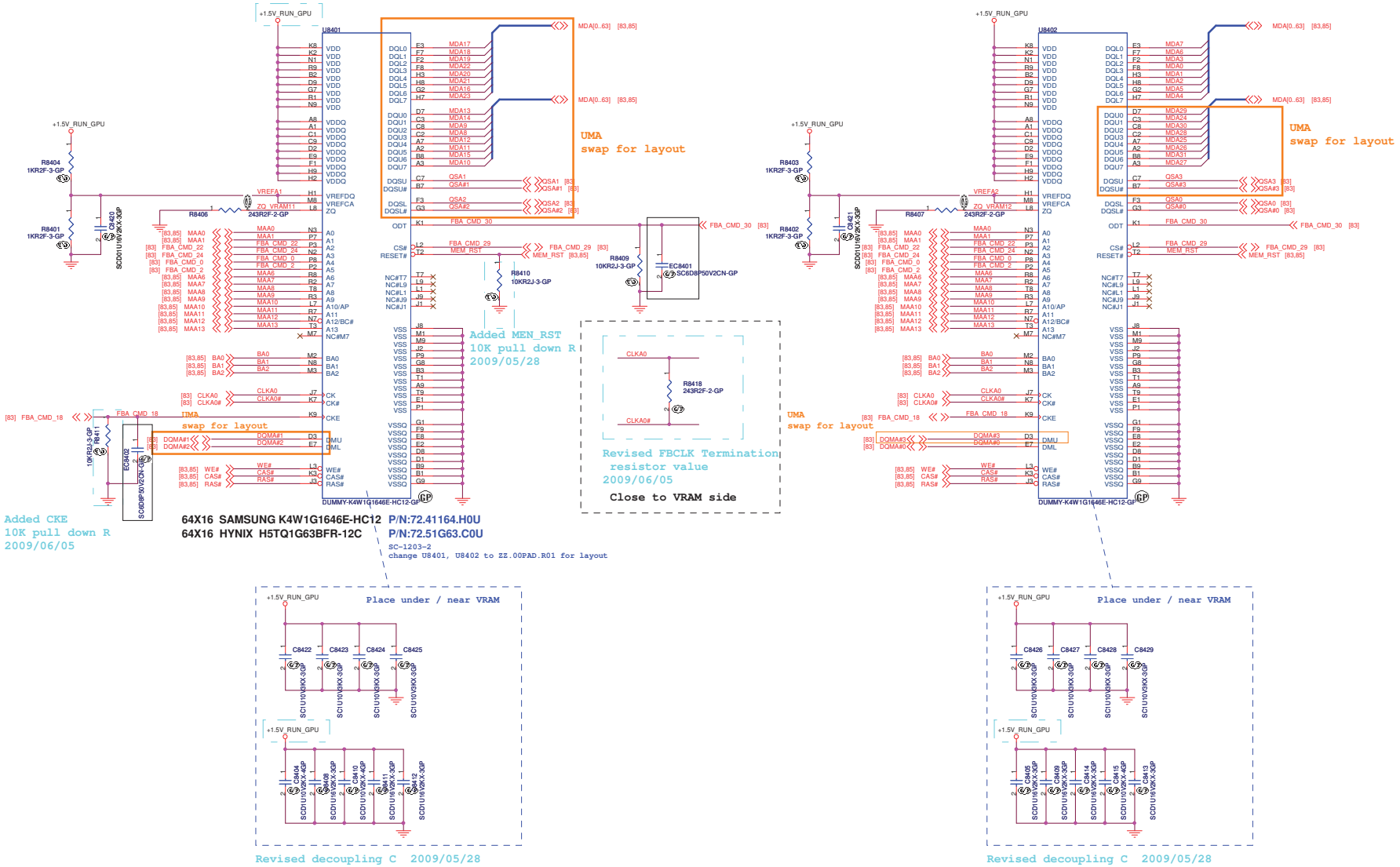
Title: VGA-MEMORY/STRAPS(4/4)
Size: A3 | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 83 of 88

SSID = VIDEO



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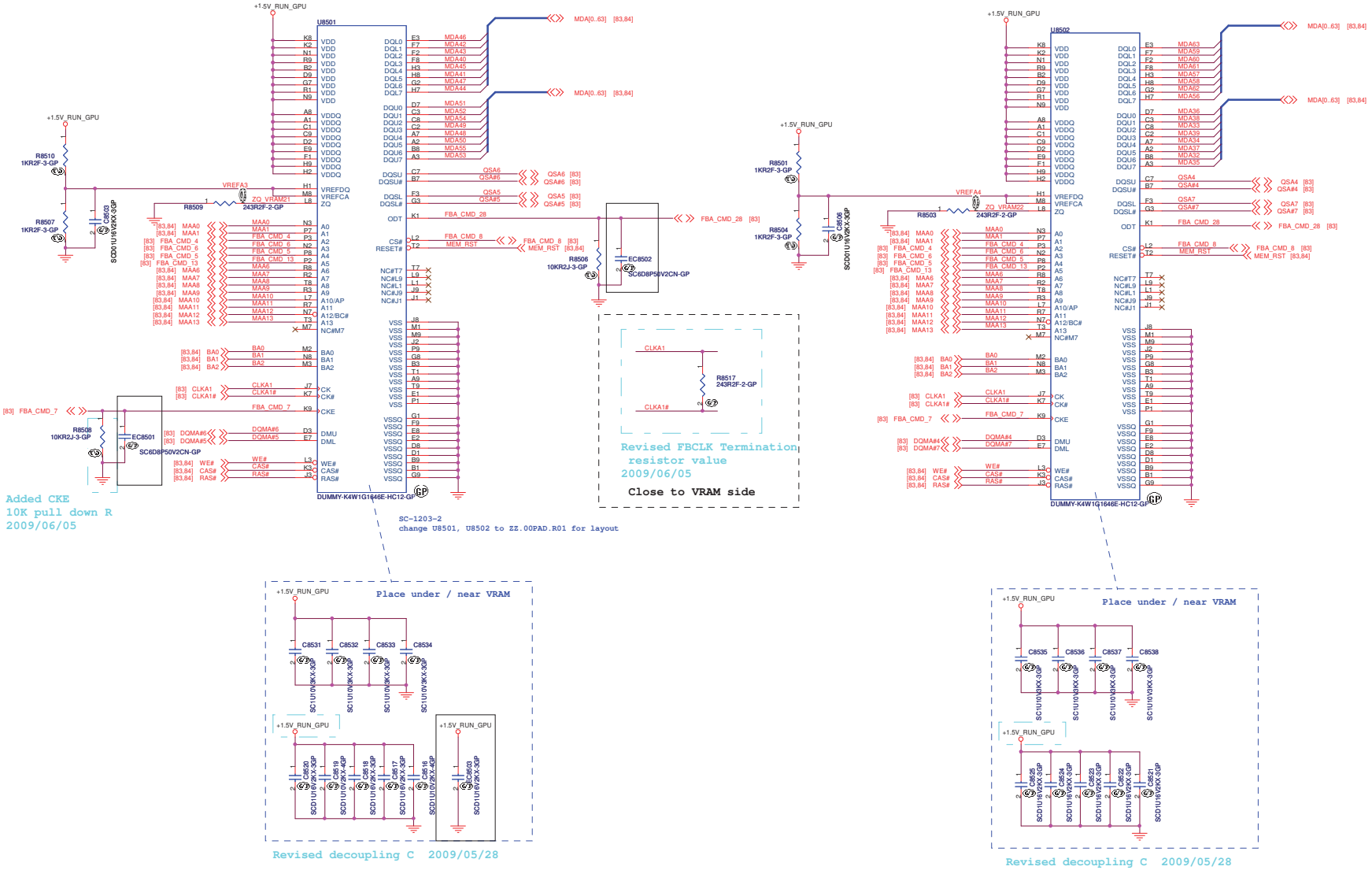
Title: VRAM(1/2)

Size	Document Number	Rev
A2	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 84 of 88

SSID = VIDEO



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Title: VRAM

Size	Document Number	Rev
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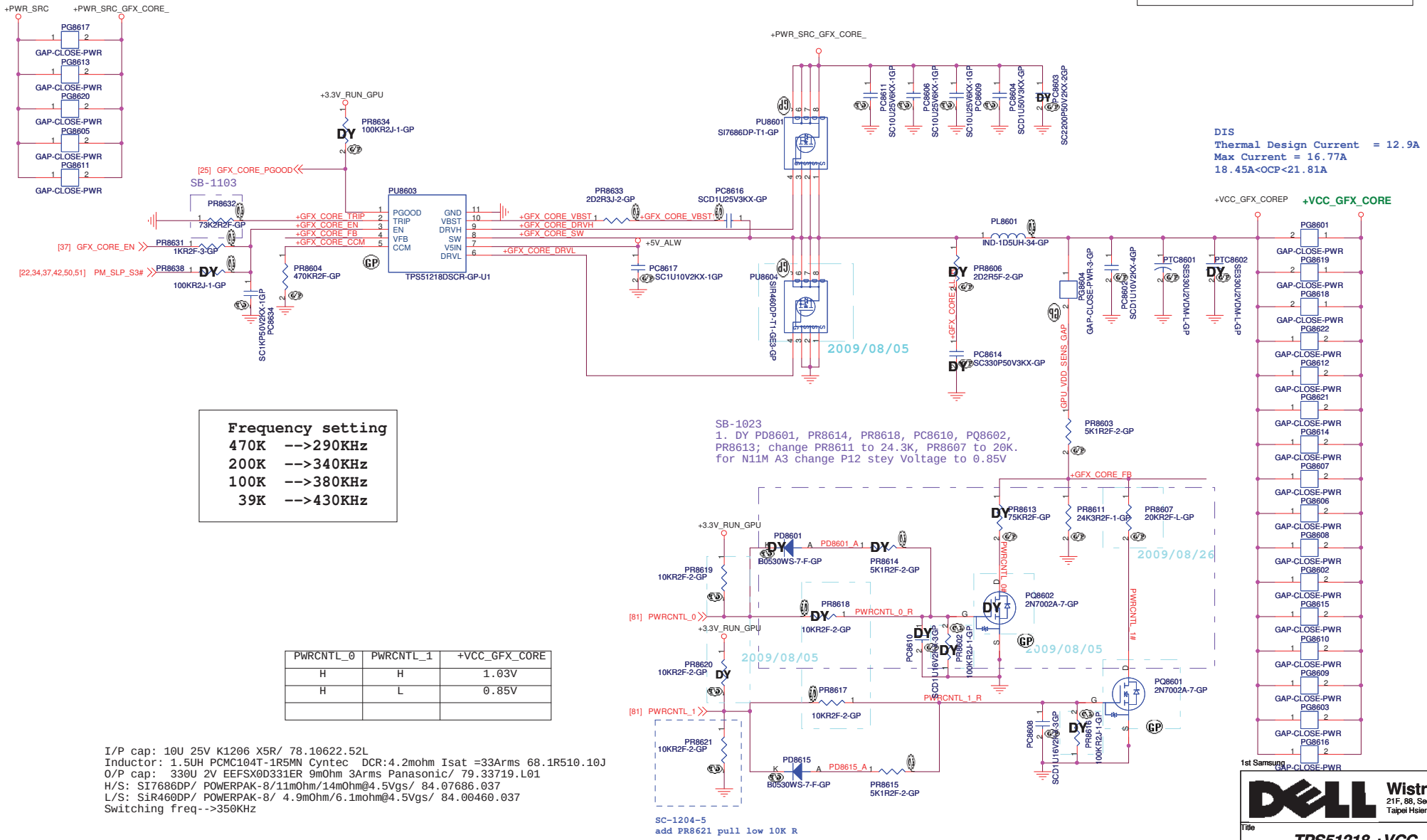
SSID = PWR.Plane.Regulator_GFX

Vout=0.704V*(R1+R2)/R2



DIS
Thermal Design Current = 12.9A
Max Current = 16.77A
18.45A<OCP<21.81A

SB-1023
1. DY PD8601, PR8614, PR8618, PC8610, PQ8602, PR8613; change PR8611 to 24.3K, PR8607 to 20K. for N11M A3 change P12 stey Voltage to 0.85V

Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.03V
H	L	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->350KHz

SC-1204-5
add PR8621 pull low 10K R

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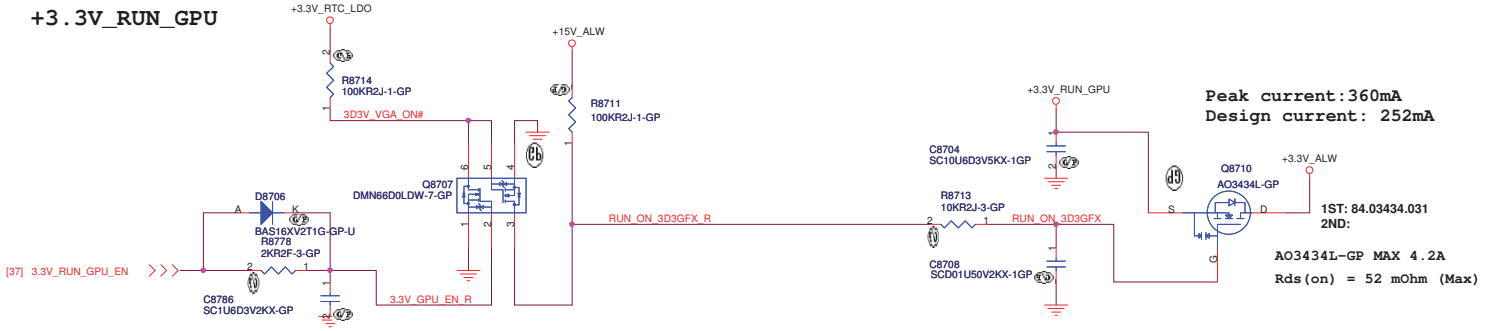
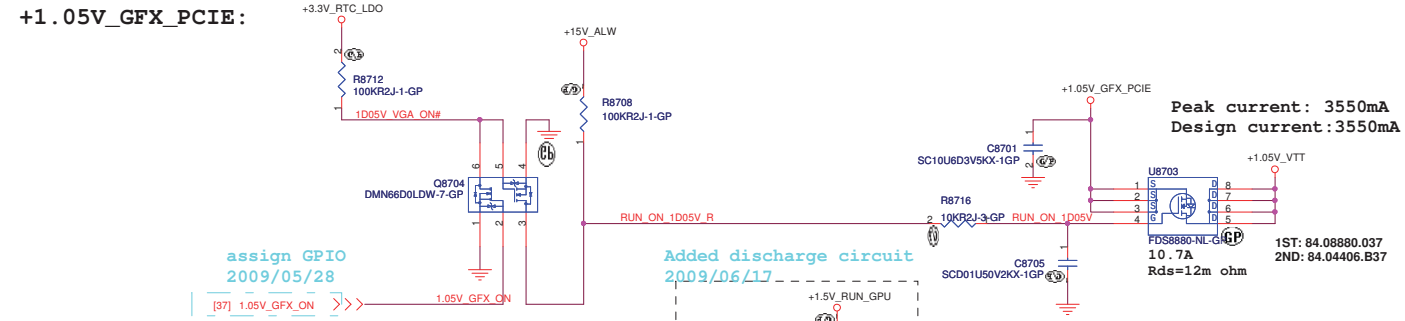
Title: TPS51218 +VCC_GFX_CORE
Size: Custom | Document Number: Winery13 MB DIS | Rev: A00
Date: Wednesday, January 13, 2010 | Sheet 86 of 88

SSID = VIDEO

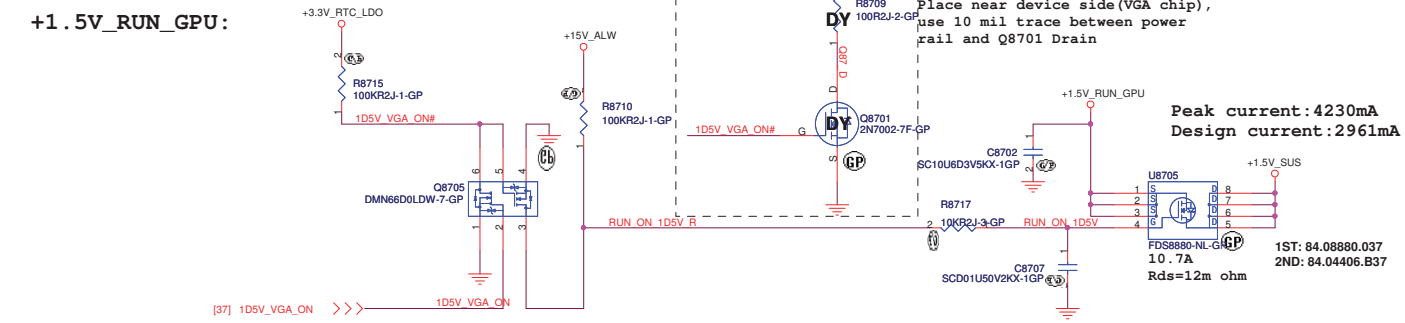
+3.3V_RUN_GPU



+1.05V_GFX_PCIE:



+1.5V_RUN_GPU:



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Title: LDO 1.8V

Size: Custom | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 87 of 88

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	66	2009/10/08	EE	HDD LED light in S5.	Change HDD LED power rail from +5V_ALW to +5V_RUN.	SB
02	60	2009/10/08	EE	External MIC NG.	Add caps C6014 C6015.	SB
03	66	2009/10/08	EE	Correct battery LED color.	Swap LED6601 pin2 & pin3.	SB
04	49	2009/10/08	EE	Improve VTT_PWRGD ramp up signal.	Dummy C4912.	SB
05	51	2009/10/08	EE	Fine tune +1.8V_RUN power on sequence behind +3.3V_RUN.	Change PR5102 from 2.2K to 3K and PC5105 from 4700pF to 1uF.	SB
06	54,78	2009/10/08	EE	For KBC ESD protect.	Add 100 ohm resistances R5413, R7803.	SB
07						
08	30	2009/10/08	EE		Change CODEC to 92HD79.	SB
09	64	2009/10/08	EE	By ME request	Change WLAN1 to 62.10043.841.	SB
10						
11	37	2009/10/09	EE	Change board ID.	Dummy R3708 and pop R3701.	SB
12	79	2009/10/12	ME	By ME request	Change H6 to ZZ.00PAD.F91	SB
13	79	2009/10/12	ME	By ME request	Change H10 to ZZ.00PAD.D41	SB
14	78	2009/10/12	ME	By ME request	Change FP1 to 20.K0315.005	SB
15	27	2009/10/12	EE	Follow Intel spec	Remove L2701, C2701, C2702; Add TP2701	SB
16	27	2009/10/12	EE	Follow Intel spec	Remove L2704, C2721, C2722; Add TP2702	SB
17	27	2009/10/12	EE	Cost down	Change L2702, L2703 to 68.10050.10Y	SB
18	24	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change C2402, C2403 to 12pF	SB
19	81	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change C8135, C8138 to 15pF	SB
20	26	2009/10/13	EE	Follow Intel spec	Remove L2602, C2616; Add TP2601	SB
21	26	2009/10/13	EE	Follow Intel spec	Remove L2601, C2606; Add TP2602	SB
22	37	2009/10/13	EE	Modify 10mW schematic		SB
23	79	2009/10/13	ME	By ME request	Remove H9 (BT BOSS)	SB
24	49	2009/10/13	EE	By PSE request	Change pg4910~pg4918 and pg4921 close gap to mask type	SB
25	73	2009/10/13	EE	Two AFTP for +3.3V_RUN	Remove AFTP6030	SB
26	34	2009/10/14	ME	By ME request	change NEW1 connector to 20.K0370.026	SB
27	79	2009/10/14	ME	By ME request	change SPR5 to 34.4F822.002	SB
28	64	2009/10/14	EE	By AFTE request	Add AFTP6402, AFTP6403	SB
29	79	2009/10/16	EE	By RF request	Add Cross Moat Caps	SB
30	80,81	2009/10/16	EE	Voltage Drop over 3%	change bead value to 120 ohm DCR 0.55 ohm	SB
31	22	2009/10/16	EE	RTC data loss	Added 3v/5v S5 power good to control resume reset sequence prevent RTC data loss	SB
32	25	2009/10/16	EE		Swapped Q2515 C,E Pin	SB
33	78	2009/10/16	EE		remove CAPA_RST# from capacity board	SB
34	37	2009/10/16	EE	By SW request	Added Switch Baord Detection circuit	SB

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Title: Change List(1/3)

Size: A3 | Document Number: Winery13 MB DIS | Rev: A00

Date: Wednesday, January 13, 2010 | Sheet 88 of 88

Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	37	2009/11/18	EE	Correct R3745 power rail to KBC_PWR	Change R3745 power rail to KBC_PWR	SC
02	36	2009/11/25	EE	TPM connector needn't AFTE test point	Remove TPM1 AFTP	SC
03	23	2009/11/25	EE	No support HDMI and eDP so needn't pop 25MHz Xtal of PCH.	C2313 pop 0 ohm if no use 25MHz XTAL	SC
04	37	2009/11/25	EE	Toggle VGA mode will flicker white screen in hybrid mode.	Add U3703 mux for panel backlight enable signal select	SC
05	54	2009/11/25	EE	Toggle VGA mode will flicker white screen in hybrid mode.	Add mux U5446 to select LCDVDD enable signal	SC
06	7	2009/11/30	RF	For solve WiMAX noise	Change C701 to 4.7pF for RF	SC
07	43	2009/11/30	RF	For solve WiMAX noise	Pop PC4303 for RF	SC
08	46	2009/11/30	RF	For solve WiMAX noise	Change PC4601 pull up to +5V_ALW for layout.	SC
09	47	2009/11/30	EE	For combine material item	Change PC4762 to 0603 size	SC
10	79	2009/11/30	ME	For one hand hold issue, ODD have noise	Add H15 for ME	SC
11	79	2009/11/30	RF	For solve WWAN noise	Add RC7931 for RF	SC
12	79	2009/11/30	RF	For solve WiMAX noise	Add SPR6 for RF	SC
13	55	2009/12/04	EMI	By EMI requirement	Change L5501,L5502,L5503 for EMI	SC
14	79	2009/12/04	EMI	By EMI requirement	Add EMI caps	SC
15	81	2009/12/04	EMI	By EMI requirement	Add EC8101,EC8102,EC8103 for EMI	SC
16	47	2009/12/04	ME	For cosmatic issue when insert 8 cell battery	Remove TC4701 for layout	SC
17	79	2009/12/04	ME	For cosmatic issue when insert 8 cell battery	Change H2 to ZZ.00PAD.D11	SC
18	30	2009/12/04	EE	Base on Application Note: IDT 92H81/79 AUX Mode as input of Diagnostic sound.	Connect U3001 pin17, pin18 to pin12 net and change R3016 to 120K for vendor request	SC
19	86	2009/12/04	EE	Set PWRCNTL_1 for default low.	Add PR8621 pull low 10K ohm	SC
20	12	2009/12/07	EMI	By EMI requirement	Pop C1243 and change size to 0603 for EMI	SC
21	33	2009/12/07	EMI	By EMI requirement	Pop C3301, EC3302, EC3303, EC3305, EC3306, EC3307, EC3308 and change from 100p to 6.8p for EMI	SC
22	54	2009/12/07	EMI	By EMI requirement	Pop EC5403 for EMI	SC
23	60	2009/12/07	EMI	By EMI requirement	Pop EC6001 and EC6002 for EMI	SC
24	63	2009/12/07	EMI	By EMI requirement	Pop R6307 for EMI	SC
25	79	2009/12/07	ME	For cosmatic issue when insert 8 cell battery	Add H16 for ME	SC
26	24	2009/12/08	EE	Base on EA teset result, change to 0 ohm.	Change R2413,R2414,R2415 from 15ohm to 0 ohm	SC
27	53	2009/12/08	EE	Base on ARD_Sightings_Report_18 #3622146	Change PR5311 from 4.7K to 470 ohm	SC
28	60	2009/12/08	EE	Audio AP LO THD+N fail	Change EC6004,EC6005 from 0.1U to 0.01U	SC
29	62	2009/12/08	EE	Base on EA teset result, change to 0 ohm.	Change R6206 from 15ohm to 0 ohm	SC
30	68	2009/12/08	EE	Change PCB Footprint	Change Q6808 to 84.06402.B3D	SC
31	73	2009/12/08	EMI	By EMI requirement	Pop L7301 for EMI	SC

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Title: Change List(2/3)

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	34	2010/01/07	EE	For no co-lay after XB	remove R3402, R3403	A00
02	37	2010/01/05	EE	Prevent SPI ROM data lost	Add reset IC U3704	A00
03	46	2009/12/18	EE	By POWER requirement	changePL4602 from 2.2U to 3.3U	A00
04	46	2009/12/18	EE	TO improve +15V_Pump Power on issue	pop PR4619; dummy PR4618	A00
05	51	2010/01/07	EE	To prevent PM_SLP_S3# signal rebound	change R5102 to short pad, PC5105 to 10K	A00
06	52	2009/12/23	EE	PREVNET MOS DEMAGE	Change C701 to 4.7pF for RF	A00
07	53	2009/12/18	EE	By POWER requirement	change PR5314 from 5.9K to 6.2K	A00
08	55	2009/12/18	EMI	By EMI requirement	change L5501, L5502, L5503 to 0R	A00
09	55	2009/12/18	EMI	By EMI requirement	change R5504, R5505, R5506 from 0R to 33R	A00
10	55	2009/12/18	EMI	By EMI requirement	change C5520 from 22p to 10p	A00
11	55	2010/01/04	ME	By ME requirement	change CRT1 from 20.20431.015 to 20.20401.015	A00
12	62	2010/01/04	ME	By ME requirement	change RCT1 from 20.D0210.102 to 20.D0075.102	A00
13	63	2010/01/06	EE	For no co-lay after XB	remove R6302, R6308,TR6301,TR6302, TR6303	A00
14	64	2010/01/07	EE	For no co-lay after XB	remove L6401	A00
15	73	2010/01/07	EE	For no co-lay after XB	remove R7302, R7303	A00
16	78	2009/12/23	EE	TO PREVENT power pin short to GND when plug in cable	dummy FP1 pin6, pin7	A00
17	78	2009/12/23	EE	add damping resister R7804	add R7804	A00
18	79	2010/01/05	ME	By ME requirement	change SPR5 from 34.4F822.002 to 34.42T14.002	A00

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Title: *Change List(3/3)*

Size: A3 | Document Number: *Winery13 MB DIS* | Rev: *A00*

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