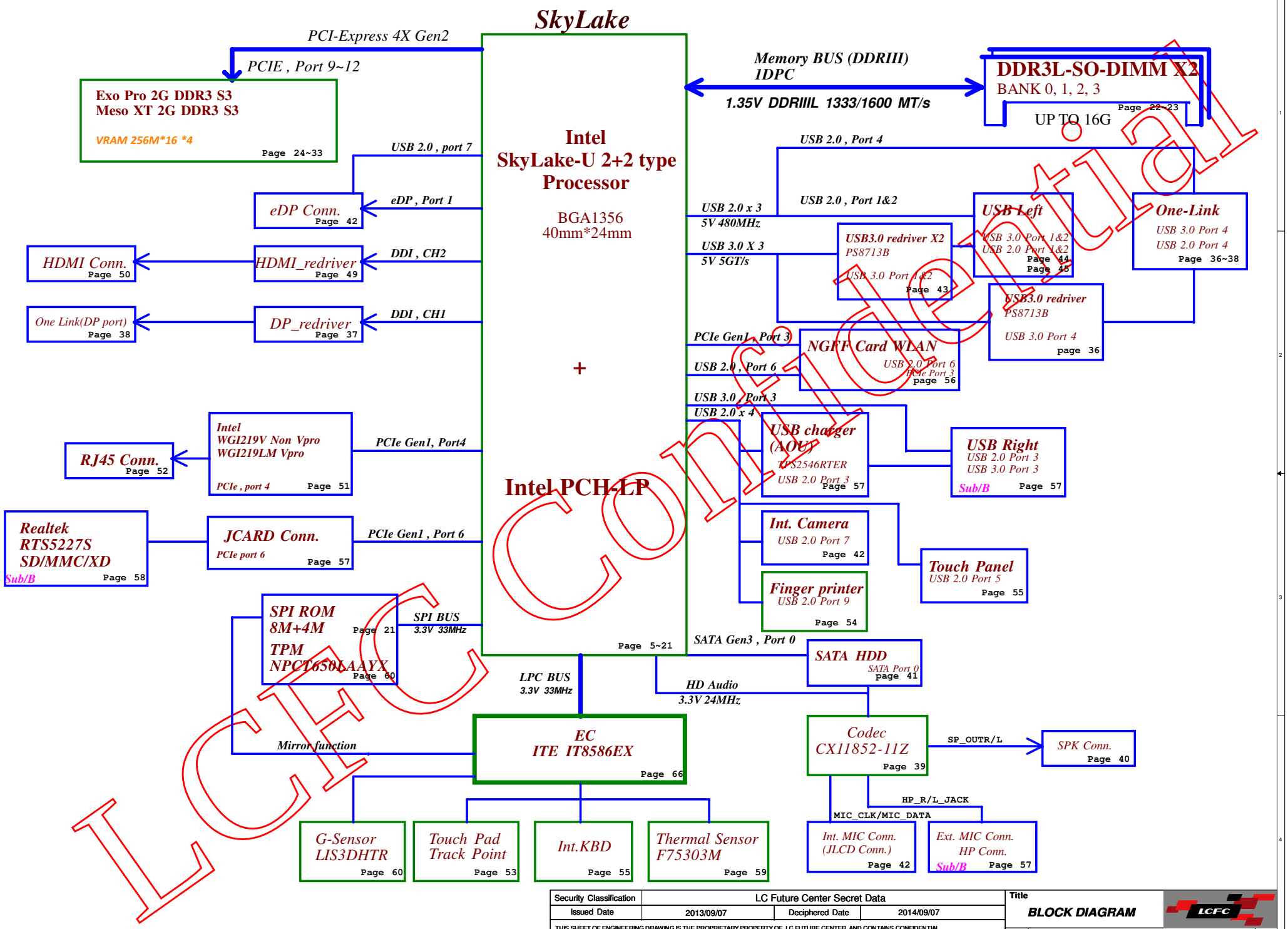

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+1VALW +1.8VALW +3VALW +5VALW	+1.35V	+5VS +3VS +0.675VS +VCC_CORE +VGA_CORE +3VS_VGA +1.8VS_VGA +1.35VS_VGA +1VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON	SUSP#
S0	HIGH	HIGH	HIGH	HIGH	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF

USB2 Port

Port	Device
1	On Board
2	On Board
3	SUB/B
4	ONE-Link DOCK
5	Touch Panel
6	BT
7	CMOS
8	FPR
9	X

USB3 Port

Port	Device
1	On Board
2	On Board
3	SUB/B
4	ONE-Link DOCK

PCIE Port

Port	Device
1	
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU

SATA Port

Port	Device
1	HDD
2	X
3	X
4	X

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Seccurity ROM	LAN PHY	G-Sensor
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3VALW_PCH	X	X	X	V +3VALW
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	V +3VS	X	X	X	V +5VS	V +3VS	X	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3VALW_PCH	X	X	X	X	X	X	X	X	V +3VALW	X

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: NOTE LIST

Size: Custom | Document Number: BE460_NM-A551 | Rev: 1.0

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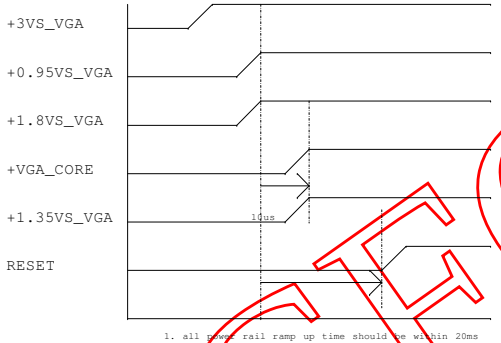
VGA and DDR3 Voltage Rails (JET TOPAZ GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	



	Device ID
JET-XT	0x6664
TOPAZ XT	0x6900

BOM Structure Table

BOM Structure	NOTE
EXO@	For GPU_EXO
MESO@	For GPU_MESO
DIS@	For GPU function
X76@	GPU VRAM Setting
TPM@	Trusted Platform Module(TPM)
DIMM1@	JDIMM1 function
DIMM2@	JDIMM2 function
UMA@	UMA SKU ID
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
MIRROR@	For mirror function
ME@	ME Connector
EMC@	For EMC function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
U31@	For U3 port1 redriver function
U32@	For U3 port2 redriver function
U33@	For U3 port3 redriver function
NU3R@	No U3 redriver function (All port)
RF@	For RF function
TS@	For Touch function

			RV104	RV105
Memory (GDDR3)				
Samsung	1G	SA22225SH30*4	PU 8.45K	PD 2K
	2G	SA000063F00*4	PU 3.4K	PD 10K
Hynix	1G	SA00005VS10*4	PU 4.53K	PD 2K
	2G	SA00005YL10*4	PU 4.75K	NC
Micron	1G	SA00005M100*4	NC	PD 4.75K
	2G	SA000060I00*4	PU 3.24K	PD 5.62K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: VGA NOTE

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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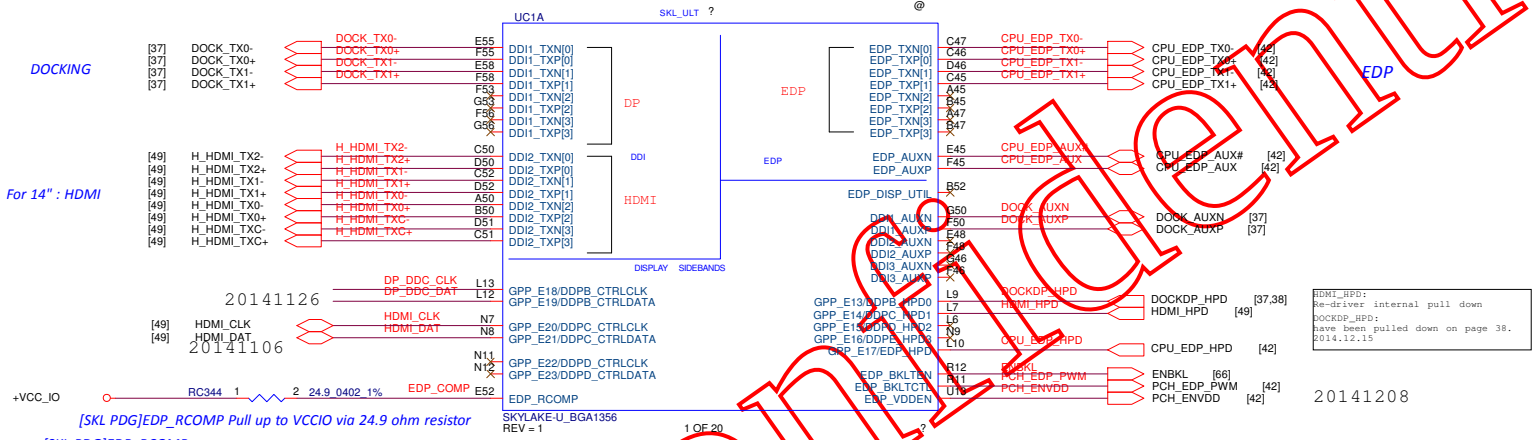
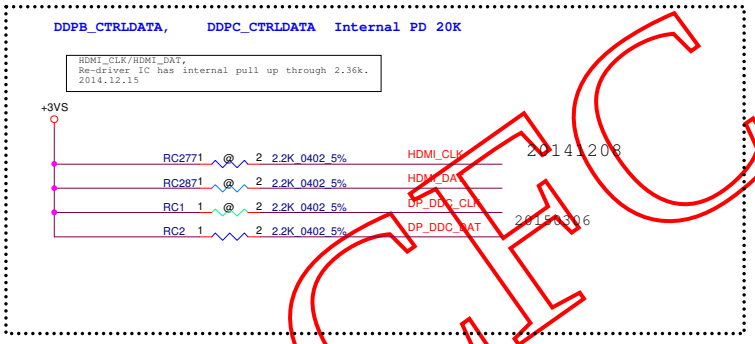
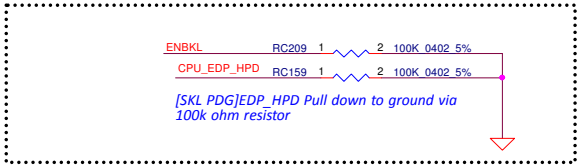


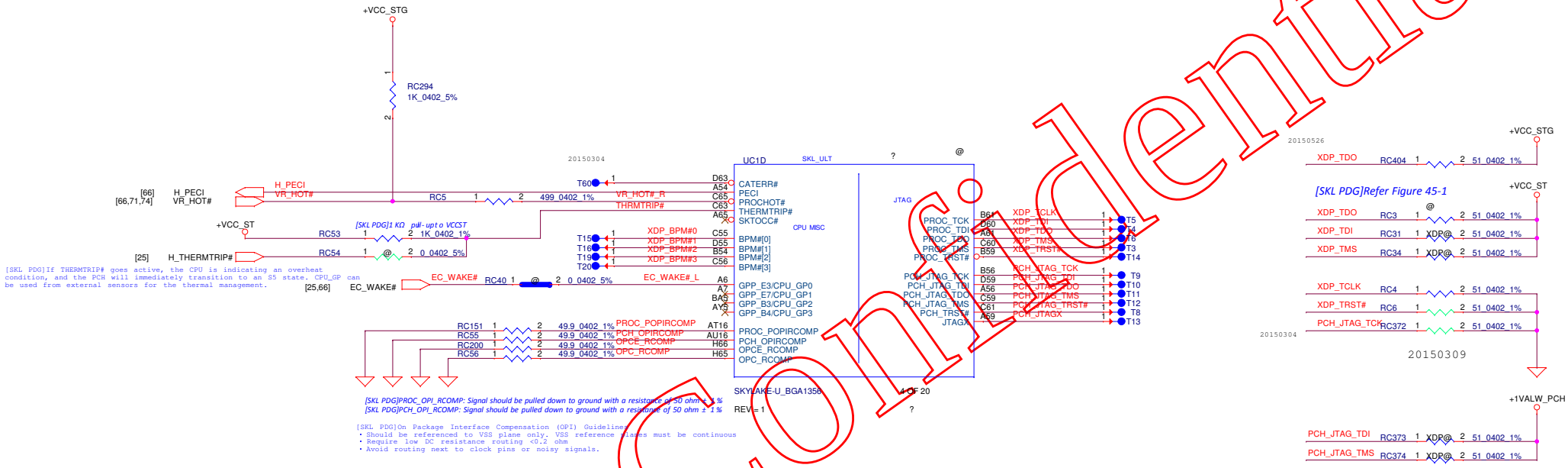




DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title	SKL(1/16):DDI/EDP		
Size	Document Number		Rev
Custom	BE460_NM-A551		1.0
Date:	Wednesday, August 05, 2015	Sheet	5 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(2/16):MISC/JTAG

Size: Custom	Document Number: BE460_NM-A551	Rev: 1.0
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[22] DDR_A_D[0..63]
[22] DDR_A_DQS#[0..7]
[22] DDR_A_DQS[0..7]
[22] DDR_A_MA[0..15]

20141201

UC1B

SKL_ULT

@

DDR_A_D0 AL71
DDR_A_D1 AL68
DDR_A_D2 AN68
DDR_A_D3 AN69
DDR_A_D4 AL70
DDR_A_D5 AL69
DDR_A_D6 AN70
DDR_A_D7 AN71
DDR_A_D8 AR70
DDR_A_D9 AR68
DDR_A_D10 AU71
DDR_A_D11 AU68
DDR_A_D12 AR71
DDR_A_D13 AR69
DDR_A_D14 AU70
DDR_A_D15 AU69
DDR_A_D16 BB65
DDR_A_D17 AW65
DDR_A_D18 AW63
DDR_A_D19 AY63
DDR_A_D20 BA65
DDR_A_D21 AY65
DDR_A_D22 BA63
DDR_A_D23 BB63
DDR_A_D24 BA61
DDR_A_D25 AW61
DDR_A_D26 BB59
DDR_A_D27 AW59
DDR_A_D28 BB61
DDR_A_D29 AY61
DDR_A_D30 BA59
DDR_A_D31 AY59
DDR_A_D32 AY39
DDR_A_D33 AW39
DDR_A_D34 AY37
DDR_A_D35 AW37
DDR_A_D36 BB39
DDR_A_D37 BA39
DDR_A_D38 BA37
DDR_A_D39 BB37
DDR_A_D40 AY35
DDR_A_D41 AW35
DDR_A_D42 AY33
DDR_A_D43 AW33
DDR_A_D44 BB35
DDR_A_D45 BA35
DDR_A_D46 BA33
DDR_A_D47 BB33
DDR_A_D48 AY31
DDR_A_D49 AW31
DDR_A_D50 AY29
DDR_A_D51 AW29
DDR_A_D52 BB31
DDR_A_D53 BA31
DDR_A_D54 BA29
DDR_A_D55 BB29
DDR_A_D56 AW27
DDR_A_D57 AW27
DDR_A_D58 AY25
DDR_A_D59 AW25
DDR_A_D60 BB27
DDR_A_D61 BA27
DDR_A_D62 BA25
DDR_A_D63 BB25

DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32]
DDR0_DQ[17]/DDR0_DQ[33]
DDR0_DQ[18]/DDR0_DQ[34]
DDR0_DQ[19]/DDR0_DQ[35]
DDR0_DQ[20]/DDR0_DQ[36]
DDR0_DQ[21]/DDR0_DQ[37]
DDR0_DQ[22]/DDR0_DQ[38]
DDR0_DQ[23]/DDR0_DQ[39]
DDR0_DQ[24]/DDR0_DQ[40]
DDR0_DQ[25]/DDR0_DQ[41]
DDR0_DQ[26]/DDR0_DQ[42]
DDR0_DQ[27]/DDR0_DQ[43]
DDR0_DQ[28]/DDR0_DQ[44]
DDR0_DQ[29]/DDR0_DQ[45]
DDR0_DQ[30]/DDR0_DQ[46]
DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0]
DDR0_DQ[33]/DDR1_DQ[1]
DDR0_DQ[34]/DDR1_DQ[2]
DDR0_DQ[35]/DDR1_DQ[3]
DDR0_DQ[36]/DDR1_DQ[4]
DDR0_DQ[37]/DDR1_DQ[5]
DDR0_DQ[38]/DDR1_DQ[6]
DDR0_DQ[39]/DDR1_DQ[7]
DDR0_DQ[40]/DDR1_DQ[8]
DDR0_DQ[41]/DDR1_DQ[9]
DDR0_DQ[42]/DDR1_DQ[10]
DDR0_DQ[43]/DDR1_DQ[11]
DDR0_DQ[44]/DDR1_DQ[12]
DDR0_DQ[45]/DDR1_DQ[13]
DDR0_DQ[46]/DDR1_DQ[14]
DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32]
DDR0_DQ[49]/DDR1_DQ[33]
DDR0_DQ[50]/DDR1_DQ[34]
DDR0_DQ[51]/DDR1_DQ[35]
DDR0_DQ[52]/DDR1_DQ[36]
DDR0_DQ[53]/DDR1_DQ[37]
DDR0_DQ[54]/DDR1_DQ[38]
DDR0_DQ[55]/DDR1_DQ[39]
DDR0_DQ[56]/DDR1_DQ[40]
DDR0_DQ[57]/DDR1_DQ[41]
DDR0_DQ[58]/DDR1_DQ[42]
DDR0_DQ[59]/DDR1_DQ[43]
DDR0_DQ[60]/DDR1_DQ[44]
DDR0_DQ[61]/DDR1_DQ[45]
DDR0_DQ[62]/DDR1_DQ[46]
DDR0_DQ[63]/DDR1_DQ[47]

DDR0_CKN[0] AU53 SA_CLK_DDR#0 → SA_CLK_DDR#0 [22]
DDR0_CKP[0] AT53 SA_CLK_DDR0 → SA_CLK_DDR0 [22]
DDR0_CKN[1] AU55 SA_CLK_DDR#1 → SA_CLK_DDR#1 [22]
DDR0_CKP[1] AT55 SA_CLK_DDR1 → SA_CLK_DDR1 [22]

DDR0_CKE[0] BA56 DDRA_CKE0_DIMMA → DDRA_CKE0_DIMMA [22]
DDR0_CKE[1] BB56 DDRA_CKE1_DIMMA → DDRA_CKE1_DIMMA [22]
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 DDRA_CS0_DIMMA# → DDRA_CS0_DIMMA# [22]
DDR0_CS#[1] AU43 DDRA_CS1_DIMMA# → DDRA_CS1_DIMMA# [22]
DDR0_ODT[0] AT45 DDRA_ODT0_DIMMA# → DDRA_ODT0_DIMMA# [22]
DDR0_ODT[1] AT43 DDRA_ODT1_DIMMA# → DDRA_ODT1_DIMMA# [22]

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 DDR_A_MA5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 DDR_A_MA9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 DDR_A_MA6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 DDR_A_MA8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AW52 DDR_A_MA7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AY55 DDR_A_BG2
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] AW54 DDR_A_MA12 → DDR_A_BS2 [22]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA54 DDR_A_MA11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 DDR_A_MA15
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 DDR_A_MA14

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 DDR_A_MA13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 DDR_A_CAS# → DDR_A_CAS# [22]
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 DDR_A_WE# → DDR_A_WE# [22]
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 DDR_A_RAS# → DDR_A_RAS# [22]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AV52 DDR_A_BS0 → DDR_A_BS0 [22]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 DDR_A_MA2
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 DDR_A_BS1 → DDR_A_BS1 [22]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 DDR_A_MA10
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 DDR_A_MA1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 DDR_A_MA0
DDR0_MA[3] BA50 DDR_A_MA3
DDR0_MA[4] BB52 DDR_A_MA4

DDR0_DQSN[0] AM70 DDR_A_DQS#0
DDR0_DQSP[0] AM69 DDR_A_DQS0
DDR0_DQSN[1] AT69 DDR_A_DQS#1
DDR0_DQSP[1] AT70 DDR_A_DQS1
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 DDR_A_DQS#2
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 DDR_A_DQS2
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 DDR_A_DQS#3
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 DDR_A_DQS3
DDR0_DQSN[4]/DDR1_DQSN[0] BA38 DDR_A_DQS#4
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 DDR_A_DQS4
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 DDR_A_DQS#5
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 DDR_A_DQS5
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 DDR_A_DQS#6
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 DDR_A_DQS6
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 DDR_A_DQS#7
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 DDR_A_DQS7

DDR0_ALERT# AW50 DDR0_ALERT# → 20141201
DDR0_PAR AT52

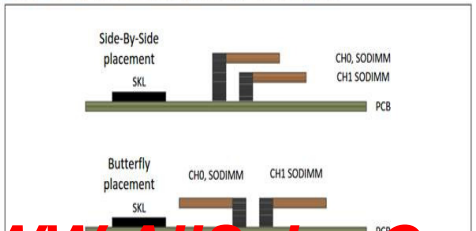
DDR_VREF_CA AY67 SM_DIMM_VREFCA → SM_DIMM_VREFCA [22]
DDR0_VREF_DQ AY68 SA_DIMM_VREFDQ → SA_DIMM_VREFDQ [22]
DDR1_VREF_DQ BA67 SB_DIMM_VREFDQ → SB_DIMM_VREFDQ [23]

DDR_VTT_CNTL AW67 DDR_PG_CTRL → DDR_PG_CTRL [22]

DDR CH - A

SKYLAKE-U_BGA1356
REV = 1
2 OF 20
?

Figure 4-14. SKL U DDR3L/-RS SODIMM T3/8L IL Placement Options



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Issued Date	2014/05/07	Deciphered Date	2015/05/07

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Title: SKL(3/16):DDR3L CH.A

Size: Custom | Document Number: BE460_NM-A551 | Rev: 1.0

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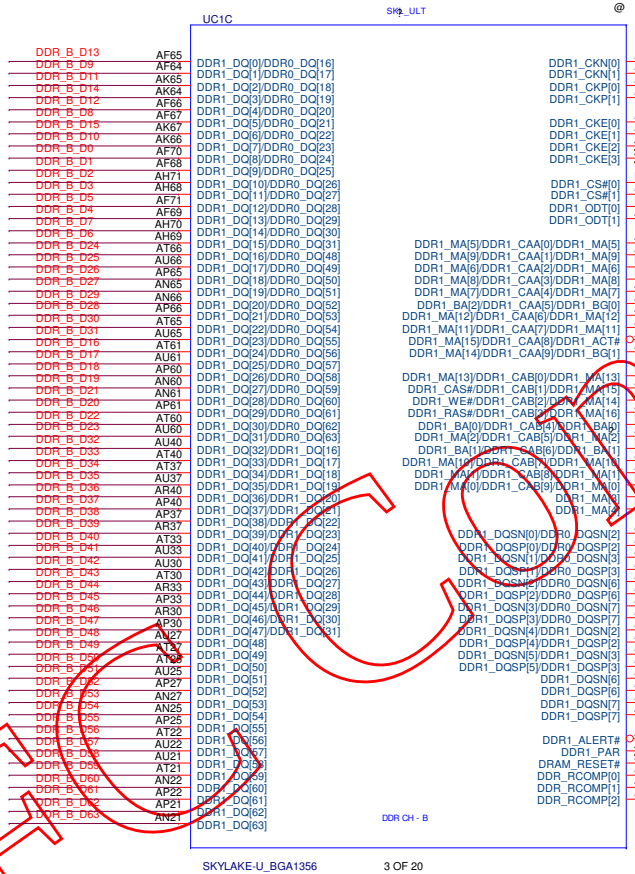

20141022

[SKL PDG]for DDR3L
DDR_RCOMP[0] Pull down 121 ohm resistor
DDR_RCOMP[1] Pull down 80.6 ohm resistor
DDR_RCOMP[2] Pull down 100 ohm resistor

[SKL PDG]DDR_RCOMP
1. Trace width=12~15 mils, Spacing=20mil, Max length=500mils
2. R close to MCP

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(4/16):DDR3L CH.B**

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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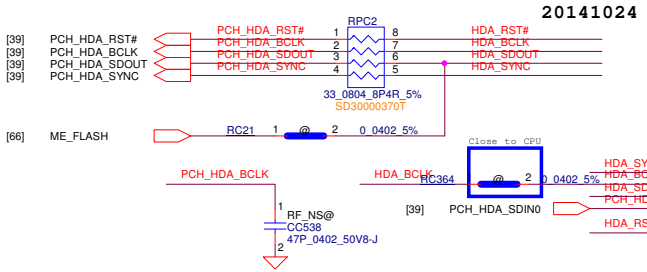
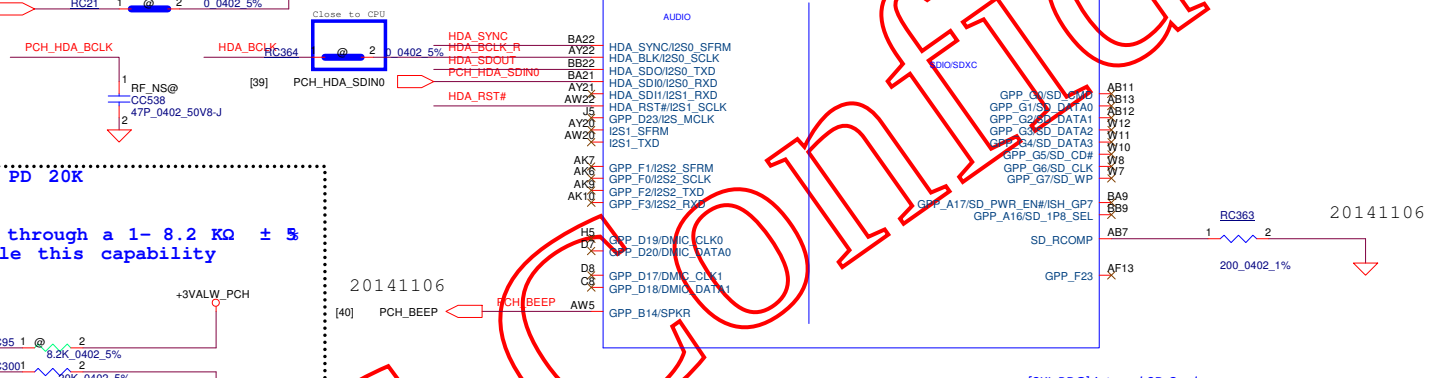
[SKL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in the flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.

20141024





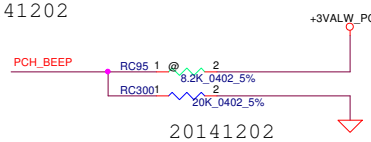
20141106

20141106

[SKL PDG] internal SD Card

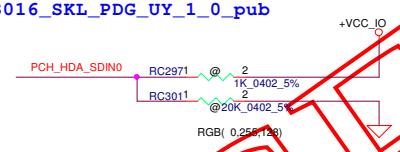
GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 1- 8.2 KΩ ± 5%
resistor to disable this capability

20141202



20141202

Processor Strapping
543016_543016_SKL_PDG_UY_1_0_pub
P780



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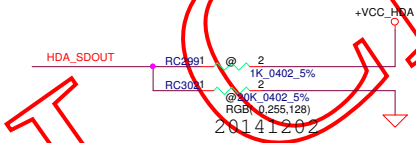
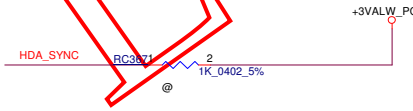


20141202

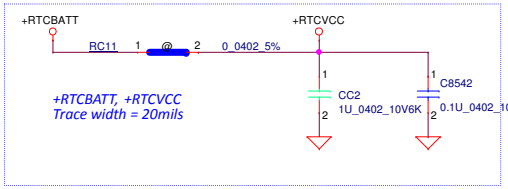


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

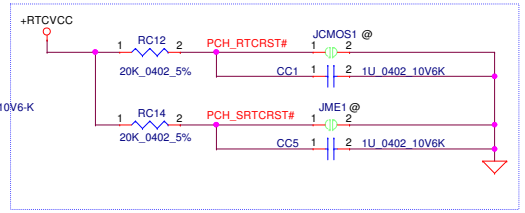
Title: **SKL(5/16):HDA/SDIO**

Size: Custom	Document Number: BE460_NM-A551	Rev: 1.0
Date: Wednesday, August 05, 2015	Sheet 9 of 83	

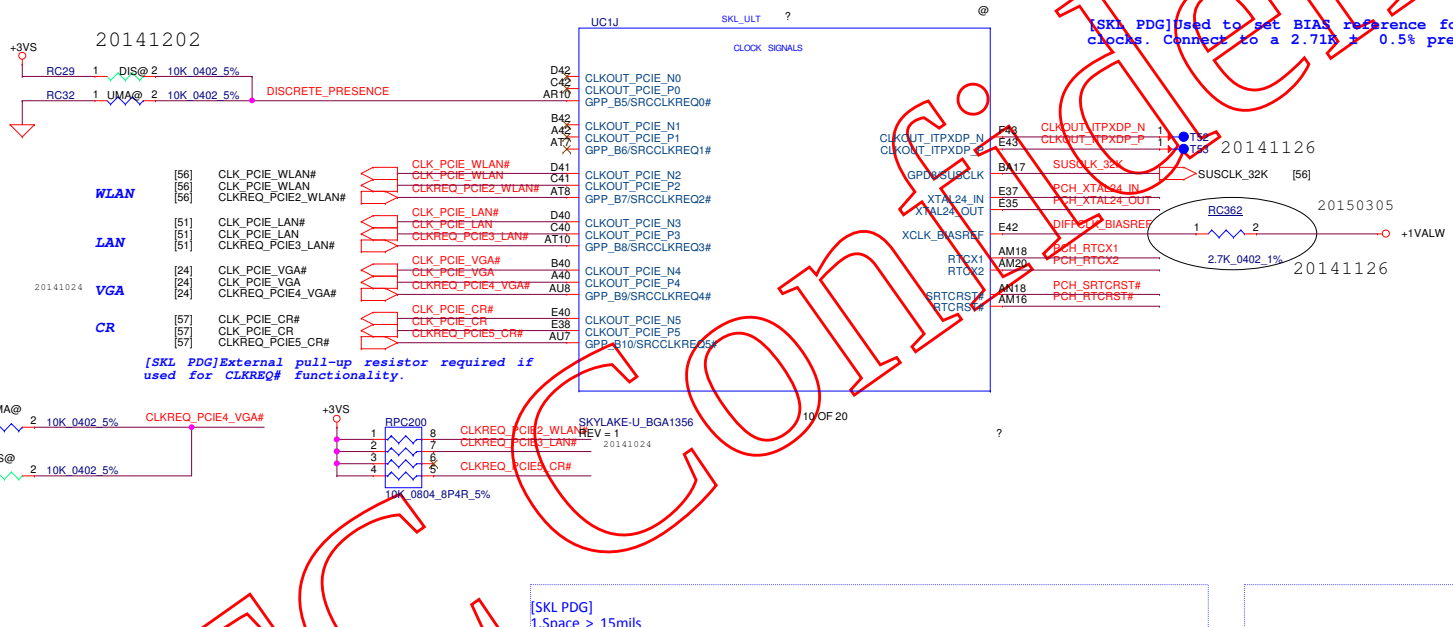
RTC External Circuit



JCMOS, JME Setting, Need Under DDR Door

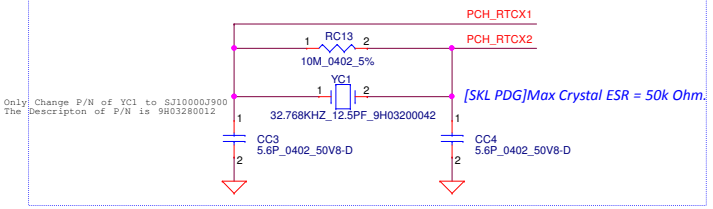


20141202

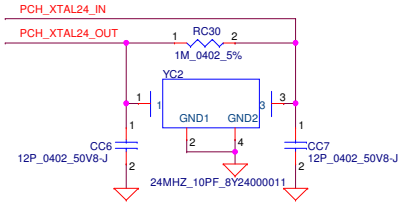


[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.

RTC Crystal



[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(6/16):CLOCK SIGNALS

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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Functional Strap Definitions

SPI0_MOSI

This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3VALW_PCH — SPI_SI — RC298 1 @ 2 8.2K_0402_5%

20141202

20150305

+3VALW_PCH — SPI_SO — RC308 1 @ 2 8.2K_0402_5%

20141202

20150305

GPP_C2; Internal PD 20K

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

+3VALW_PCH — GPP_C2 — RC306 1 2 1K_0402_5% — RC307 1 2 @20K_0402_5%

RGB(0,255,128)

GPP_C5; Internal PD 20K

*L: LPC
H: eSPI

+3VALW_PCH — GPP_C5 — RC83 2 @ 1 1K_0402_5% — RC84 2 1 20K_0402_5%

20141202

Close to CPU — RC365 1 @ 2 0_0402_5%

[21,60] SPI_CLK — SPI_SO — SPI_SI — SPI_IO2 — SPI_IO3 — SPI_CS0#_8MB — SPI_CS1#_4MB — SPI_CS2#_TPM

PCH_SPI_CLK — SPI_SO AV2 — SPI_SI AW3 — SPI_IO2 AV3 — SPI_IO3 AW2 — SPI_CS0#_8MB AU4 — SPI_CS1#_4MB AU3 — SPI_CS2#_TPM AU2 — AU1

UC1E — SKL_ULT

SPI - FLASH: SPI0_CLK, SPI0_MISO, SPI0_MOSI, SPI0_IO2, SPI0_IO3, SPI0_CS0#, SPI0_CS1#, SPI0_CS2#

SPI - TOUCH: GPP_D1/SPI1_CLK, GPP_D2/SPI1_MISO, GPP_D3/SPI1_MOSI, GPP_D21/SPI1_IO2, GPP_D22/SPI1_IO3, GPP_D0/SPI1_CS#

C LINK: CL_CLK, CL_DAT#, CL_RST#

SMBUS, SMLINK

GPP_C0/SMBCLK — R7 — PCH_SMB_CLK
GPP_C1/SMBDATA — R8 — PCH_SMB_DATA
GPP_C2/SMBALERT# — R10 — GPP_C2
GPP_B5/SML0CLK — R9 — PCH_SML0_CLK — PCH_SML0_CLK [51]
GPP_C4/SML0DATA — W2 — PCH_SML0_DAT — PCH_SML0_DAT [51]
GPP_C5/SML0ALERT# — W1 — GPP_C5
GPP_B6/SML1CLK — W3 — PCH_SML1CLK
GPP_C7/SML1DATA — V3 — PCH_SML1DATA
GPP_B23/SML1ALERT#/PCHHOT# — AM7 — GPP_B23

DIMM1, DIMM2, Security EEPROM, Click Pad

LAN

EC,dGPU,Thermal Sensor

[66] EC_SCI# — EC_SCI# M2

[56] CL_CLK_WLAN — G3
[56] CL_DATA_WLAN — G2
[56] CL_RST_WLAN# — G1

[66] KBRST# — KBRST# AW13

[60,66] SERIRQ — SERIRQ AY11

GPP_A0/RCIN#

GPP_A6/SERIRQ

SKYLAKE-U_BGA1356
REV = 1

5 OF 20

GPP_A1/LAD0/ESPI_IO0 — AY13 — LPC_AD0 [66]
GPP_A2/LAD1/ESPI_IO1 — BA13 — LPC_AD1 [66]
GPP_A3/LAD2/ESPI_IO2 — BB13 — LPC_AD2 [66]
GPP_A4/LAD3/ESPI_IO3 — AY12 — LPC_AD3 [66]
GPP_A5/FRAME#/ESPI_CS# — BA12 — LPC_FRAME# [66]
GPP_A14/SUS_STAT#/ESPI_RESET# — BA11 SUS_STAT#

RC47 1 @ 2 0_0402_5% 1 — T18

20141128

GPP_A9/CLKOUT_LPC0/ESPI_CLK — AW9 PCH_PCI_CLK_R
GPP_A10/CLKOUT_LPC1 — AY9
GPP_A8/CLKRUN# — AW11 CLKRUN#

RC24 1 EMC@ 2 22_0402_5% — CLK_PCI_EC [66]

RF_NS@ CC537 47P_0402_50V8-J

20141128

+3VS — RC52 1 2 8.2K_0402_5%

20141202

[SKL PDG]RCIN# Pull-up to Vcc3_3 with 10 Kohm resistor.

[SKL PDG]CLKRUN# Requires an 8.2 KΩ weak pull-up resistor to Vcc3_3

[SKL PDG]SERIRQ uses a 8.2 KΩ pull-up to +V3.3S power-rail.
[SKL CRB]SERIRQ uses a 10 KΩ pull-up to +V3.3S power-rail.

+3VS — RPC22 10K_0804_8P4R_5% — SERIRQ — EC_SCI# — KBRST#

+3VALW_PCH

PCH_SML0_CLK — RC92 1 2 499_0402_1%
PCH_SML0_DAT — RC93 1 2 499_0402_1%

PCH_SMB_CLK — RC375 1 2 4.7K_0402_5%
PCH_SMB_DATA — RC376 1 2 4.7K_0402_5%
PCH_SML1_CLK — RC377 1 2 2.2K_0402_1%
PCH_SML1_DAT — RC378 1 2 2.2K_0402_1%

GPP_B23 — RC101 2 1 1K_0402_5%

SB000013A00
2N7002KDWH_SOT363-6
QC1A

PCH_SMB_CLK — PM_SMB_CLK [21,22,23,53]

+3VS — RC106 1 2 4.7K_0402_5%

+3VS — RC107 1 2 4.7K_0402_5%

PCH_SMB_DATA — PM_SMB_DAT [21,22,23,53]

QC1B
2N7002KDWH_SOT363-6
SB000013A00

2N7002KDWH_SOT363-6
QC2A
SB000013A00

+3VS — PCH_SML1CLK — EC_SMB_CK3 [25,37,59,60,65]

PCH_SML1DATA — EC_SMB_DA3 [25,37,59,60,65]

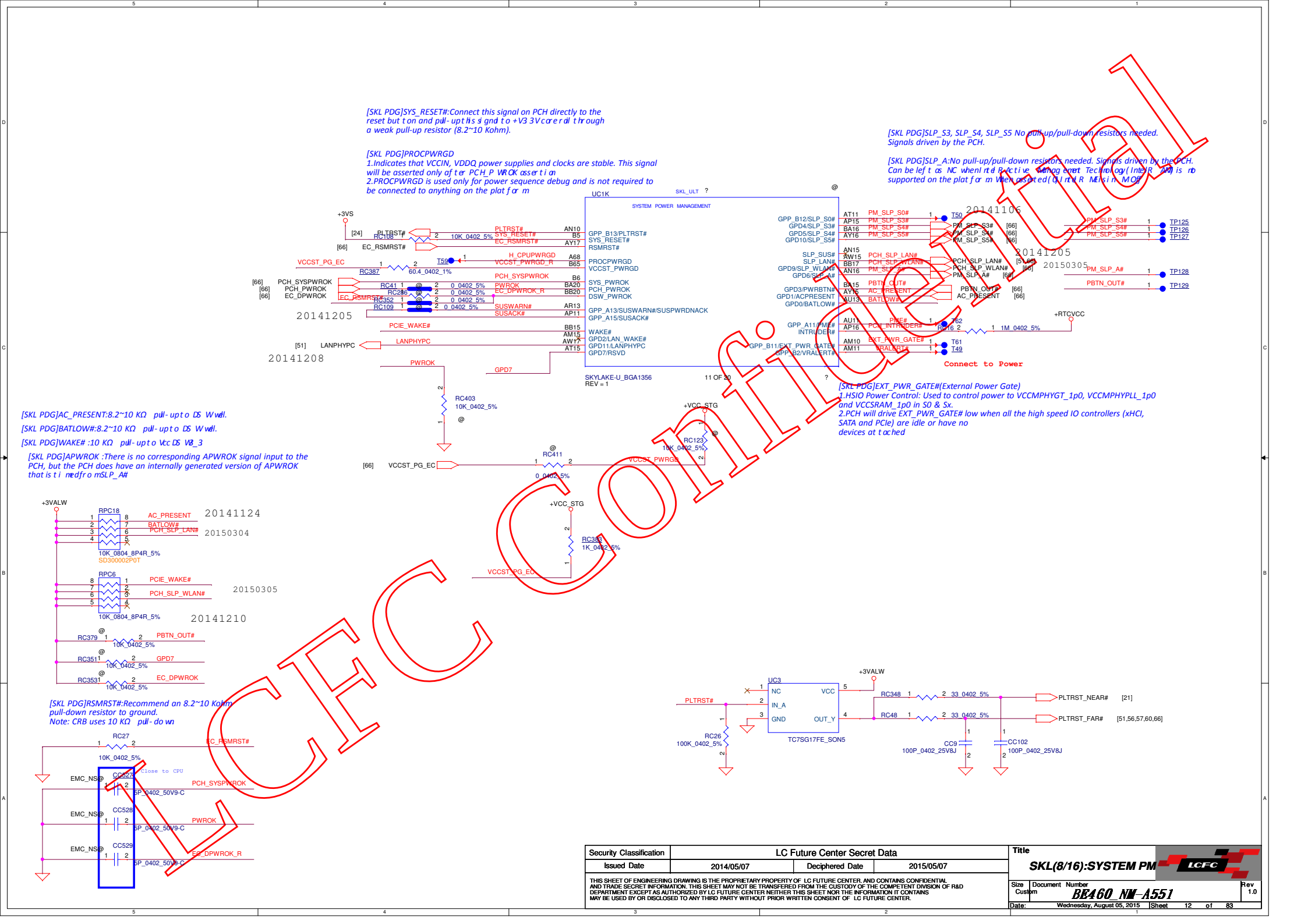
QC2B SB000013A00
2N7002KDWH_SOT363-6

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(7/16):LPC/SPI/SMBUS/CL

Size: C | Document Number: BB460_NM-A551 | Rev: 1.0

Date: Wednesday, August 05, 2015 | Sheet 11 of 83


[SKL PDG]SYS_RESET#:Connect this signal on PCH directly to the reset buffer on and pull-up this signal to +V3.3V core rail through a weak pull-up resistor (8.2~10 Kohm).
[SKL PDG]PROCPWRGD
1.Indicates that VCCIN, VDDQ power supplies and clocks are stable. This signal will be asserted only after PCH_PWROK assertion
2.PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform
[SKL PDG]SLP_S3, SLP_S4, SLP_S5 No pull-up/pull-down resistors needed. Signals driven by the PCH.
[SKL PDG]SLP_A:No pull-up/pull-down resistors needed. Signals driven by the PCH. Can be left as NC when Intel Rapid Active Cooling Event Technology (Intel RACE) is not supported on the platform or when asserted (Q-Intel RMS in MOF)
UC1K
SKL_ULT
SYSTEM POWER MANAGEMENT
SKYLAKE-U_BGA1356
REV = 1
11 OF 20
20141205
20141208
20141106
20150305
[SKL PDG]AC_PRESENT:8.2~10 KΩ pull-up to DSW rail.
[SKL PDG]BATLOW#:8.2~10 KΩ pull-up to DSW rail.
[SKL PDG]WAKE# :10 KΩ pull-up to VccDSW3_3
[SKL PDG]APWROK :There is no corresponding APWROK signal input to the PCH, but the PCH does have an internally generated version of APWROK that is timed from SLP_A#
[SKL PDG]EXT_PWR_GATE#(External Power Gate)
1.HSIO Power Control: Used to control power to VCCMPHYGT_1p0, VCCMPHYPLL_1p0 and VCCSRAM_1p0 in S0 & Sx.
2.PCH will drive EXT_PWR_GATE# low when all the high speed IO controllers (xHCI, SATA and PCIe) are idle or have no devices attached
Connect to Power
20141124
20150304
20150305
20141210
[SKL PDG]RSMRST#:Recommend an 8.2~10 Kohm pull-down resistor to ground.
Note: CRB uses 10 KΩ pull-down
Close to CPU
TC7SG17FE_SON5
LCFC Confidential
Security Classification
LC Future Center Secret Data
Issued Date
2014/05/07
Deciphered Date
2015/05/07
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Title
SKL(8/16):SYSTEM PM
Size
Custom
Document Number
BE460_NM-A551
Rev
1.0
Date:
Wednesday, August 05, 2015
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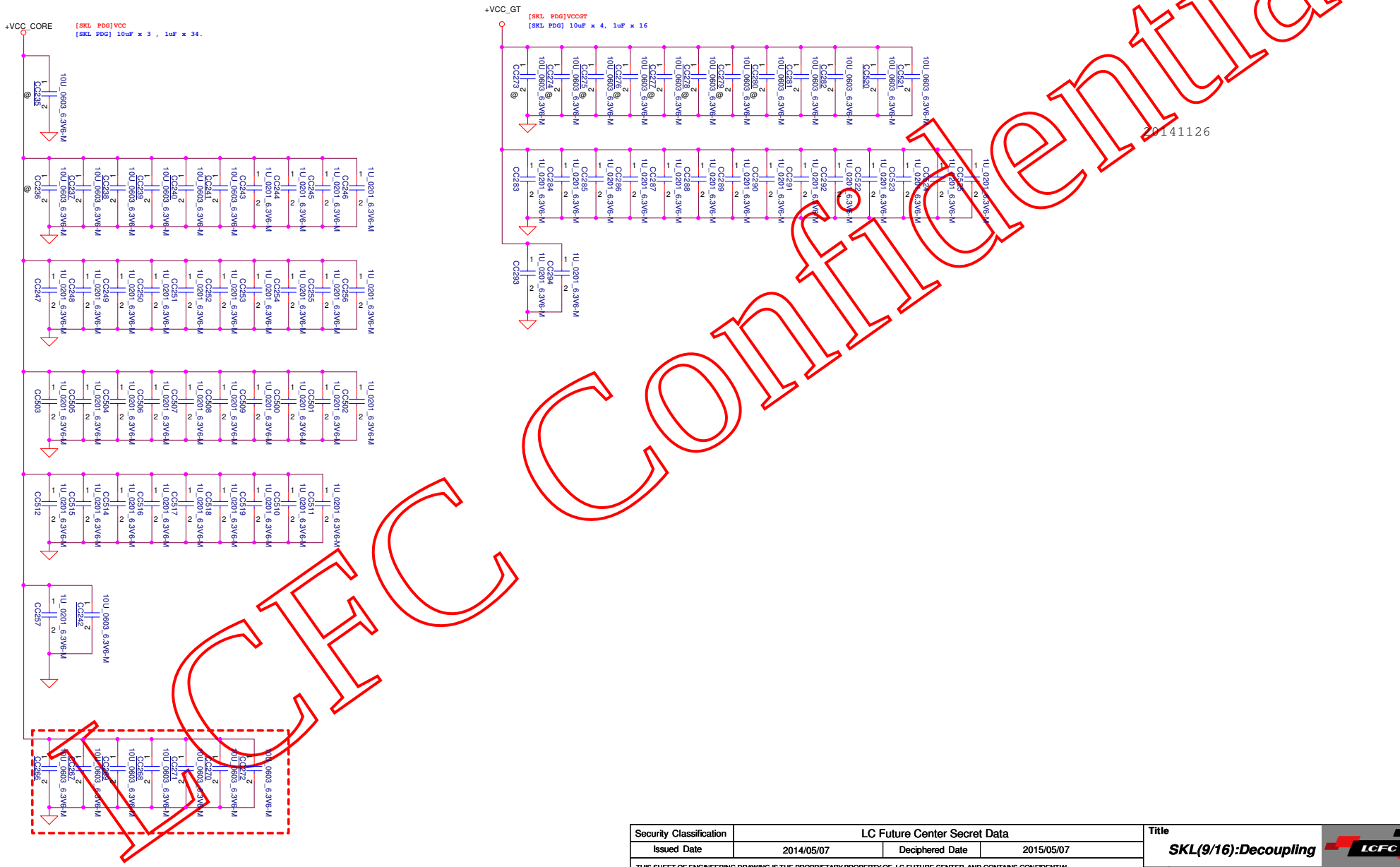
12
of
83

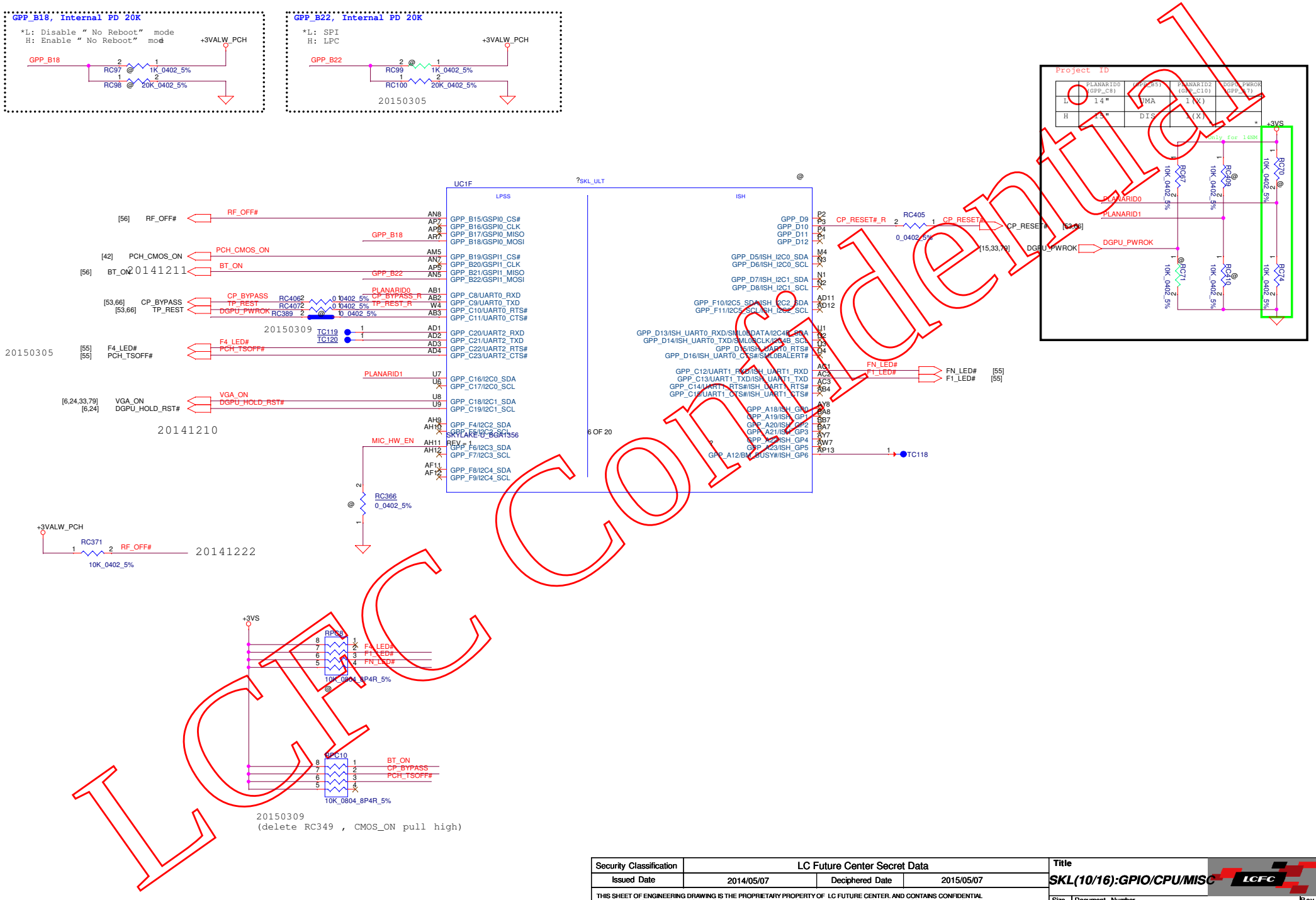


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(9/16):Decoupling

Size: Custom | Document Number: BE460_NM-A551 | Rev: 1.0

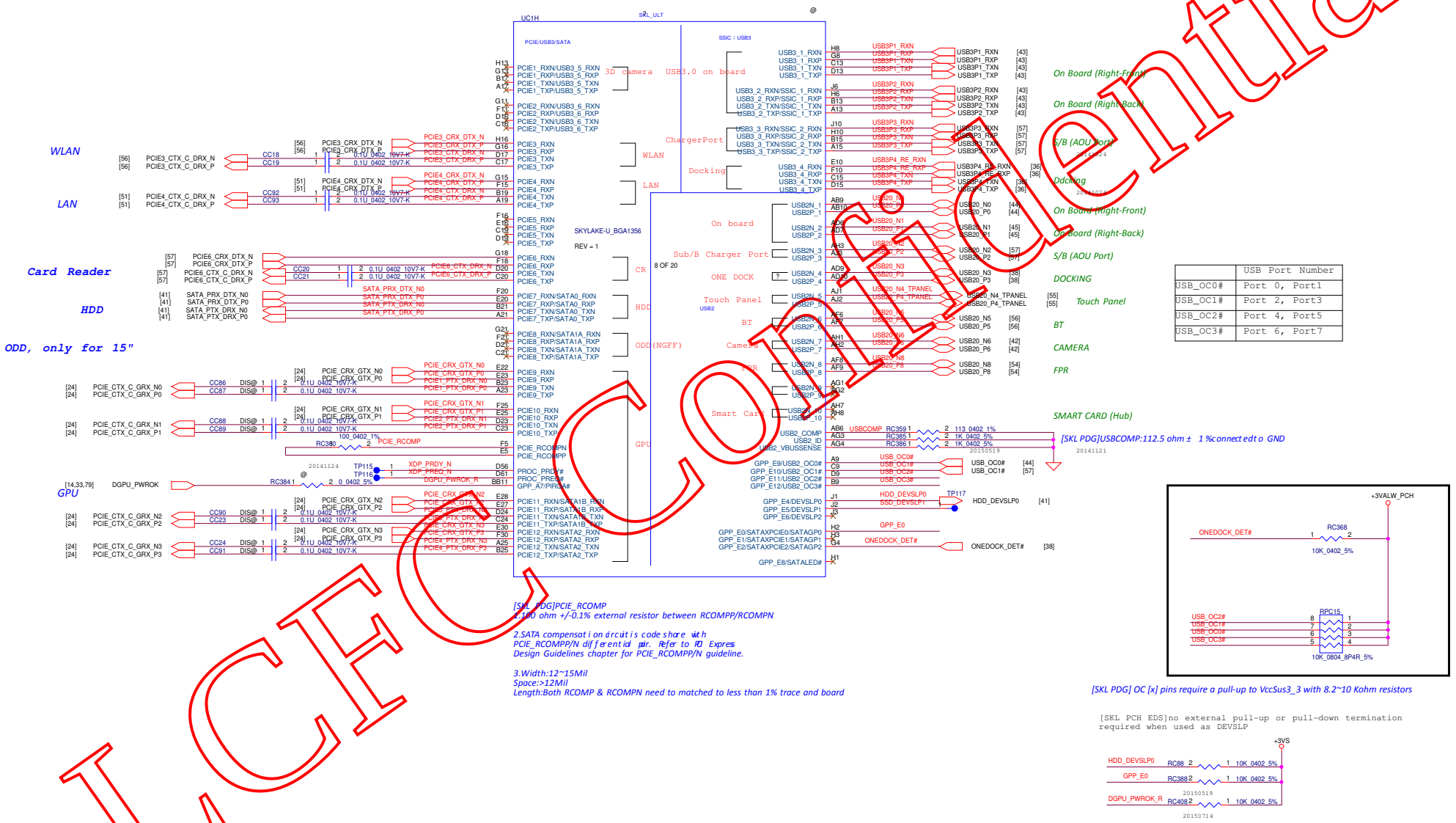
Date: Wednesday, August 05, 2015 | Sheet 13 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(10/16):GPIO/CPU/MISC

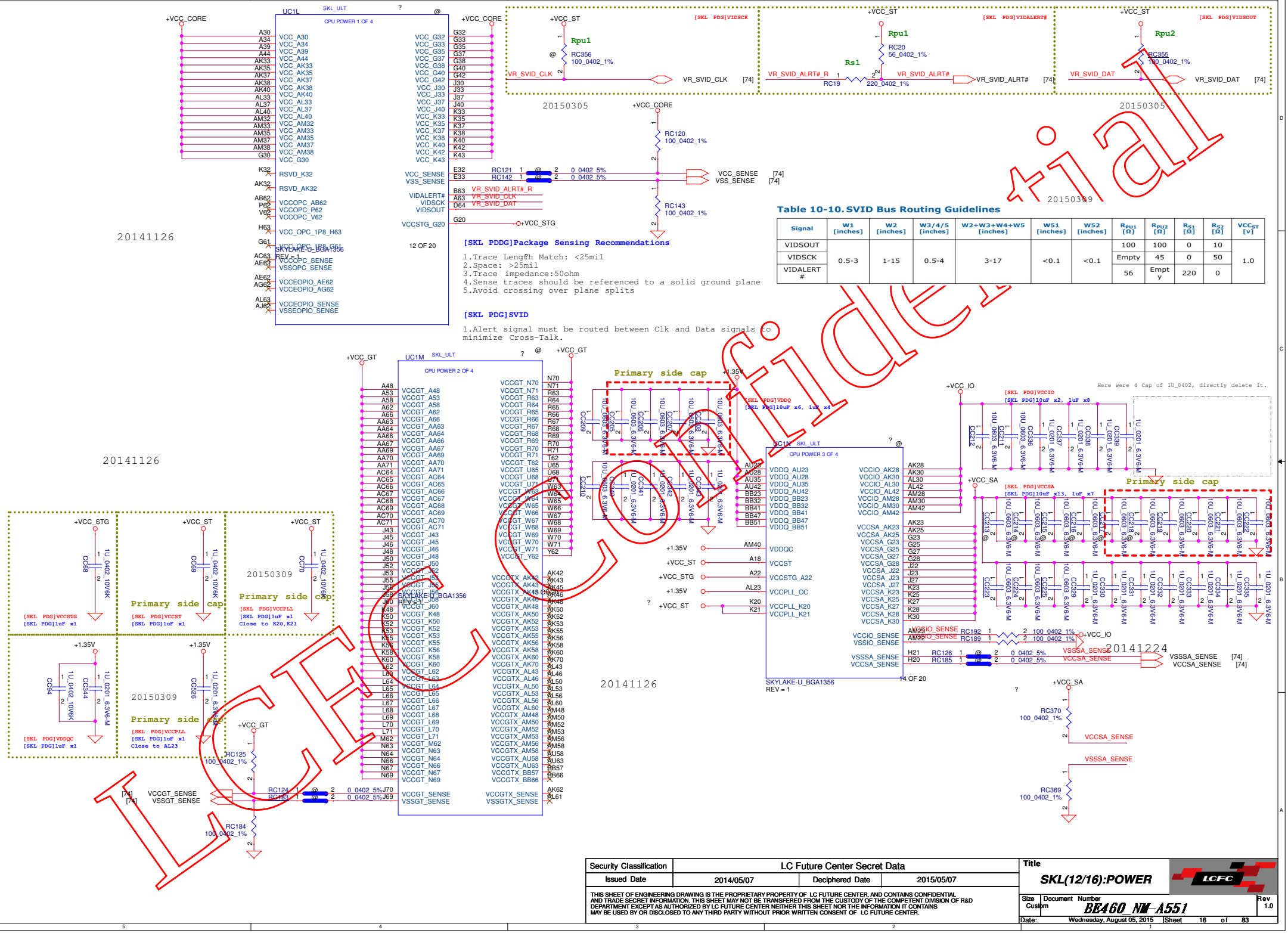
Size: Custom	Document Number: BE460_NM-A551	Rev: 1.0
Date: Wednesday, August 05, 2015	Sheet 14 of 83	



	USB Port Number
USB_OC0#	Port 0, Port1
USB_OC1#	Port 2, Port3
USB_OC2#	Port 4, Port5
USB_OC3#	Port 6, Port7

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title	SKL(11/16):PCIE/USB/SATA		
Size C	Document Number BR460_NM-A551		Rev 1.0
Date: Wednesday, August 05, 2015	Sheet 15 of 83		


UC1L SKL_ULT CPU POWER 1 OF 4
SKYLAKE-U_BGA1356 REV = 1
12 OF 20
20141126
[SKL PDDG]Package Sensing Recommendations
1.Trace Length Match: <25mil
2.Space: >25mil
3.Trace impedance:50ohm
4.Sense traces should be referenced to a solid ground plane
5.Avoid crossing over plane splits
[SKL PDDG]SVID
1.Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.
Table 10-10. SVID Bus Routing Guidelines
Signal | W1 [inches] | W2 [inches] | W3/4/5 [inches] | W2+W3+W4+W5 [inches] | W51 [inches] | W52 [inches] | RPU1 [Ω] | RPU2 [Ω] | RS1 [Ω] | RS2 [Ω] | VCCST [v]
VIDSOUT | 0.5-3 | 1-15 | 0.5-4 | 3-17 | <0.1 | <0.1 | 100 | 100 | 0 | 10 | 1.0
VIDSCK | | | | | | | Empty | 45 | 0 | 50 |
VIDALERT# | | | | | | | 56 | Empty | 220 | 0 |
Primary side cap
20150305
20150309
20141224
UC1M SKL_ULT CPU POWER 2 OF 4
UC1N SKL_ULT CPU POWER 3 OF 4
Here were 4 Cap of 1U_0402, directly delete it.
LC Future Center Secret Data
Security Classification
Issued Date 2014/05/07
Deciphered Date 2015/05/07
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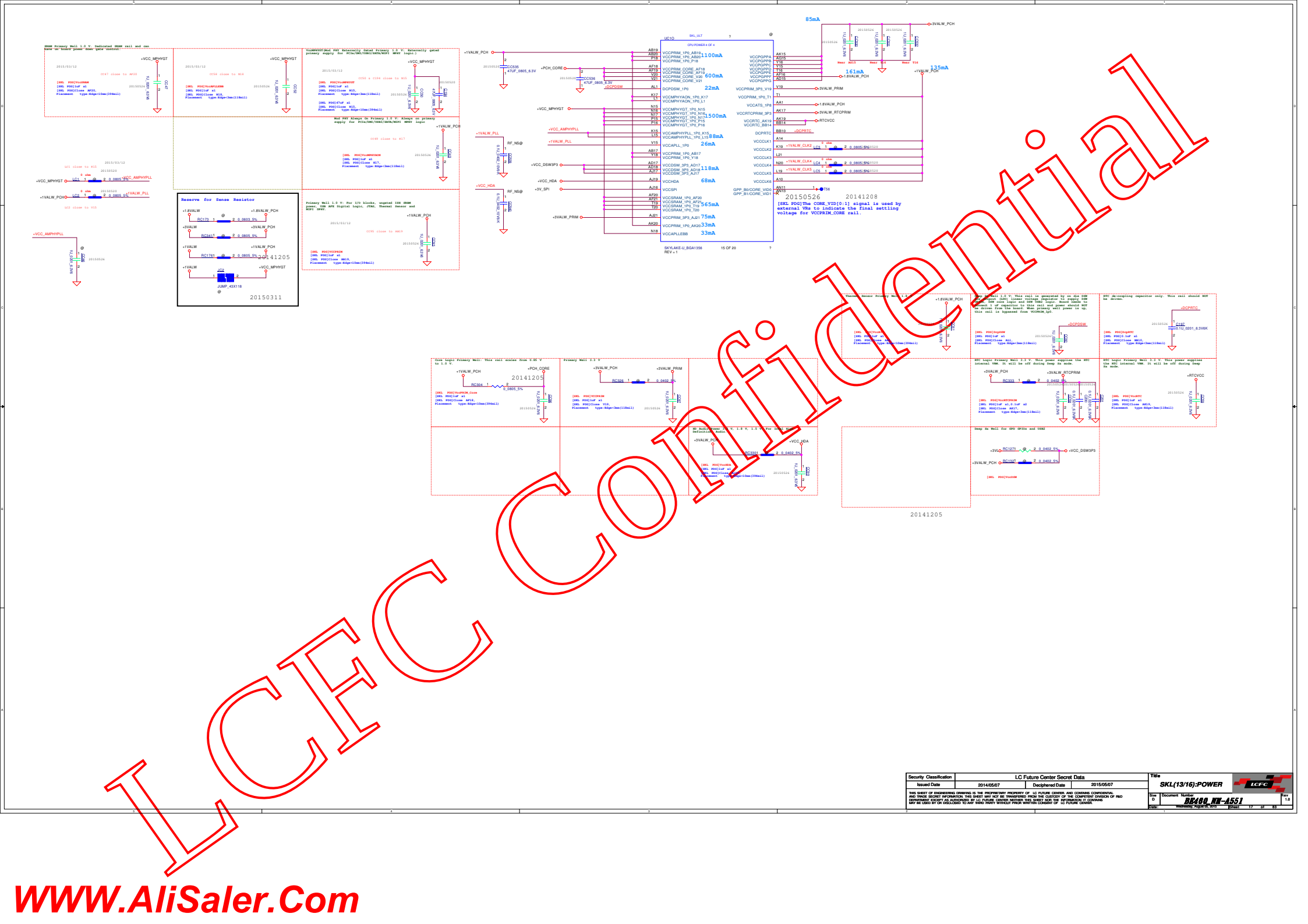
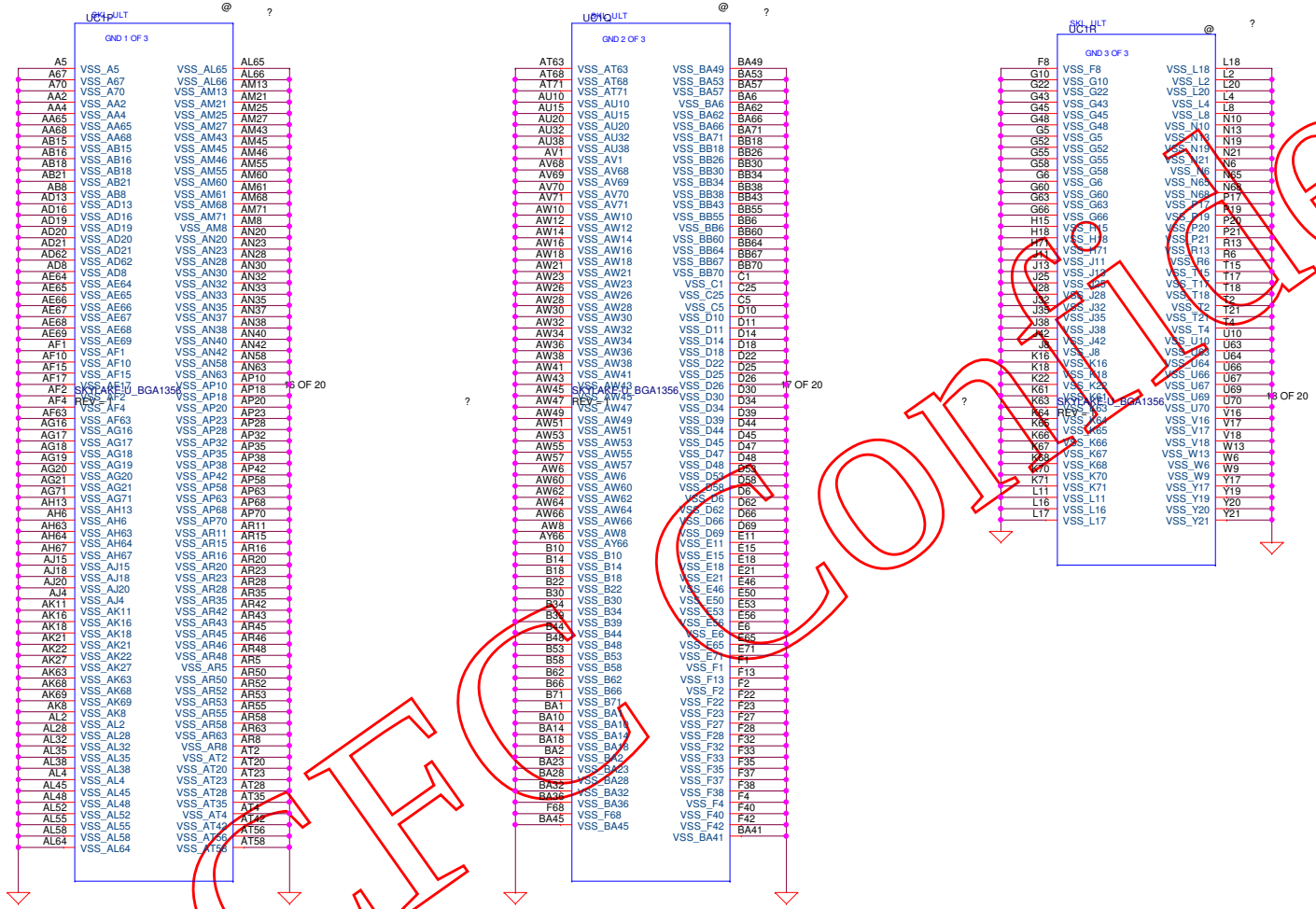
Title SKL(12/16):POWER
Size Custom
Document Number BE460_NM-A551
Rev 1.0
Date: Wednesday, August 05, 2015
Sheet 16 of 83



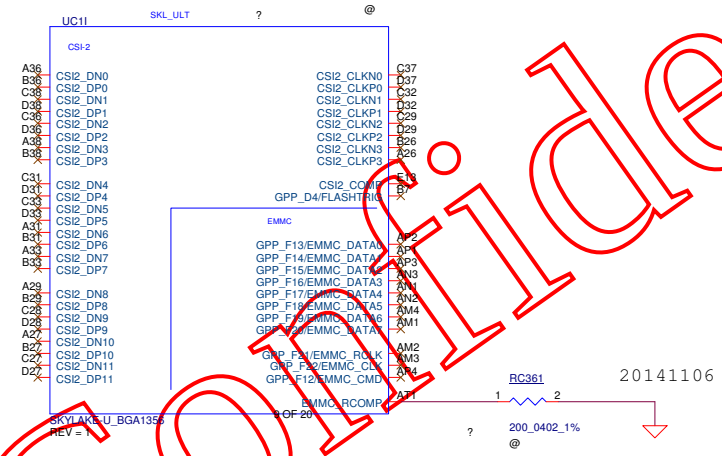


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(14/16):GND**

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

Date: Wednesday, August 05, 2015 Sheet 18 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(15/16):CSI-2/EMMC

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

Date: Wednesday, August 05, 2015 Sheet 19 of 83

[SKL EDS]

CFG0

+VCC_IO

CFG0 — RC105 2 @ 1 1K_0402_5% — RC201 2 @ 1 1K_0402_1%

L:Stall.
*H:(Default) Normal Operation; No stall.

CFG4

+VCC_IO

CFG4 — RC104 2 @ 1 1K_0402_5% — RC144 2 1 1K_0402_1%

*L: Embedded DisplayPort Enabled
H: Embedded DisplayPort Disabled

20150309
(Test point change to 12mil)

UC1S SKL_ULT ? @

RESERVED SIGNALS-1

TP36 CFG0 E68 — CFG[0]
TP38 CFG1 B67 — CFG[1]
TP40 CFG2 D65 — CFG[2]
TP41 CFG3 D67 — CFG[3]
TP42 CFG4 E70 — CFG[4]
TP44 CFG5 C68 — CFG[5]
TP46 CFG6 D68 — CFG[6]
TP47 CFG7 C67 — CFG[7]
TP48 CFG8 F71 — CFG[8]
TP50 CFG9 G69 — CFG[9]
TP52 CFG10 F70 — CFG[10]
TP53 CFG11 G68 — CFG[11]
TP55 CFG12 H70 — CFG[12]
TP56 CFG13 G71 — CFG[13]
TP57 CFG14 H69 — CFG[14]
TP58 CFG15 G70 — CFG[15]

TP61 CFG16 E63 — CFG[16]
TP63 CFG17 F63 — CFG[17]

TP62 CFG18 E66 — CFG[18]
TP65 CFG19 F66 — CFG[19]

[SKL CRB]

RC152 2 1 49.9_0402_1% — CFG_RCOMP E60 — CFG_RCOMP

+1VALW_PCH — RC354 2 1 1.5K_0402_5% — ITP_PMODE E8 — ITP_PMODE

[SKL PDG]Route HOOK[6] to Skylake ITP_PMODE. Termination: Resistor value from 1K ohm to 3K ohm pull up to PCH_V1.0A Rail.

TP24 AY2 — RSVD_AY2
TP26 AY1 — RSVD_AY1

SKYLAKE-U_BGA1356
REV = 1

TP74 D1 — RSVD_D1
TP30 D3 — RSVD_D3

TP86 K46 — RSVD_K46
TP85 K45 — RSVD_K45

TP88 AL25 — RSVD_AL25
TP87 AL27 — RSVD_AL27

TP90 C71 — RSVD_C71
TP89 B70 — RSVD_B70

TP32 F60 — RSVD_F60

TP91 A52 — RSVD_A52

TP92 BA70 — RSVD_TP_BA70
TP93 BA68 — RSVD_TP_BA68

TP94 J71 — RSVD_J71
TP95 J68 — RSVD_J68

F65 — VSS_F65
G65 — VSS_G65

TP96 F61 — RSVD_F61
TP97 E61 — RSVD_E61

RSVD_TP_BB68 BB68 — TP37
RSVD_TP_BB69 BB69 — TP39

RSVD_TP_AK13 AK13 — TP43
RSVD_TP_AK12 AK12 — TP45

RSVD_BB2 BB2 — TP49
RSVD_BA3 BA3 — TP51

TP5 AU5 — TP59
TP6 AT5 — TP60

RSVD_D5 D5 — TP22
RSVD_D4 D4 — TP23
RSVD_B2 B2 — TP25
RSVD_C2 C2 — TP27

RSVD_B3 B3 — TP64
RSVD_A3 A3 — TP66

RSVD_AW1 AW1 — TP29

RSVD_E1 E1 — TP31
RSVD_E2 E2 — TP32

RSVD_BA4 BA4 — TP34
RSVD_BB4 BB4 — TP35

RSVD_A4 A4 ? — TP67
RSVD_C4 C4 — TP68

TP4 BB5 — TP54

RSVD_A69 A69 — TP927
RSVD_B69 B69 — TP928

RSVD_AY3 AY3 — RC296 1 @ 2 0_0402_5% — TP929

RSVD_D71 D71 — TP930
RSVD_C70 C70

RSVD_C54 C54 — TP931
RSVD_D54 D54 — TP932

TP1 AY4 — TP933
TP2 BB3 — TP934

VSS_AY71 AY71 — RC295 1 @ 2 0_0402_5% — TP935
ZVM# AR56

RSVD_TP_AW71 AW71 — TP936
RSVD_TP_AW70 AW70 — TP937

MSM# AP56 — TP938
PROC_SELECT# C64

19 OF 20

[SKL CRB]

20141202

+VCC_ST

RC358 2 1 100K_0402_1% @

[SKL EDS]Zero Voltage Mode:VCCOPC is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:

ZVM# state	VCCOPC
0V	0V
1V	1V

[SKL EDS]Minimum Speed Mode: VCCEOPIO can be connected to OPC VR in this case VCCEOPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal .
In order to achieve better power/performance it is recommended to use a separate VR for VCCEOPIO in this case VCCEOPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEOPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the EOPIO interface as shown below:

ZVM# state	MSM# state	VCCEOPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted 1 : No Stall 0 : Stall
CFG4 : eDP Enable 1 : Disabled 0 : Enabled
CFG9 : SVID Bus Communication 1 : Enabled 0 : Disabled

UC1T SKL_ULT @ ?

SPARE

TP98 AW69 — RSVD_AW69
TP99 AW68 — RSVD_AW68
TP100 AU56 — RSVD_AU56
TP101 AW48 — RSVD_AW48
TP102 C7 — RSVD_C7
TP103 U12 — RSVD_U12
TP104 U11 — RSVD_U11
TP105 H11 — RSVD_H11

RSVD_F6 F6 — TP106
RSVD_E3 E3 — TP107
RSVD_C11 C11 — TP108
RSVD_B11 B11 — TP109
RSVD_B11 A11 — TP110
RSVD_A11 D12 — TP111
RSVD_D12 C12 — TP112
RSVD_C12 F52 — TP113
RSVD_F52

SKYLAKE-U_BGA1356
REV = 1

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Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(16/16):CFG/RESERVED

Size: Custom | Document Number: BE460_NM-A551 | Rev: 1.0

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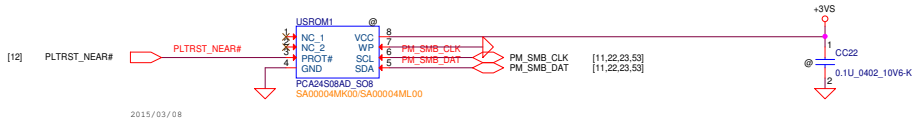
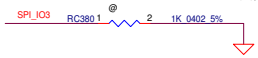
Security ROM

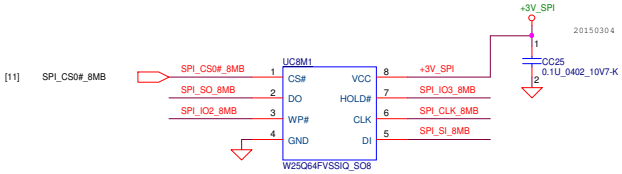


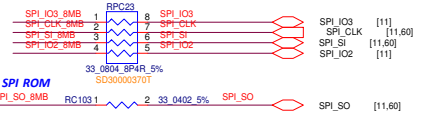
2015/03/08



[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM

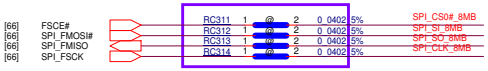
8MB(64Mb)





Near SPI ROM

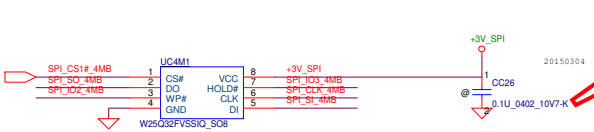
Mirror Code

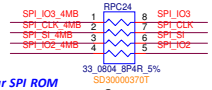


Close to SPI ROM (UC8M1).

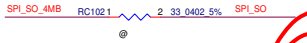
M3 Support + Intel LAN PHY / Wireless LAN Solut i on

4MB(32Mb) for VPRO SKU





Near SPI ROM



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	XXXX	
Size C	Document Number BR460_NM-A551	Rev 1.0
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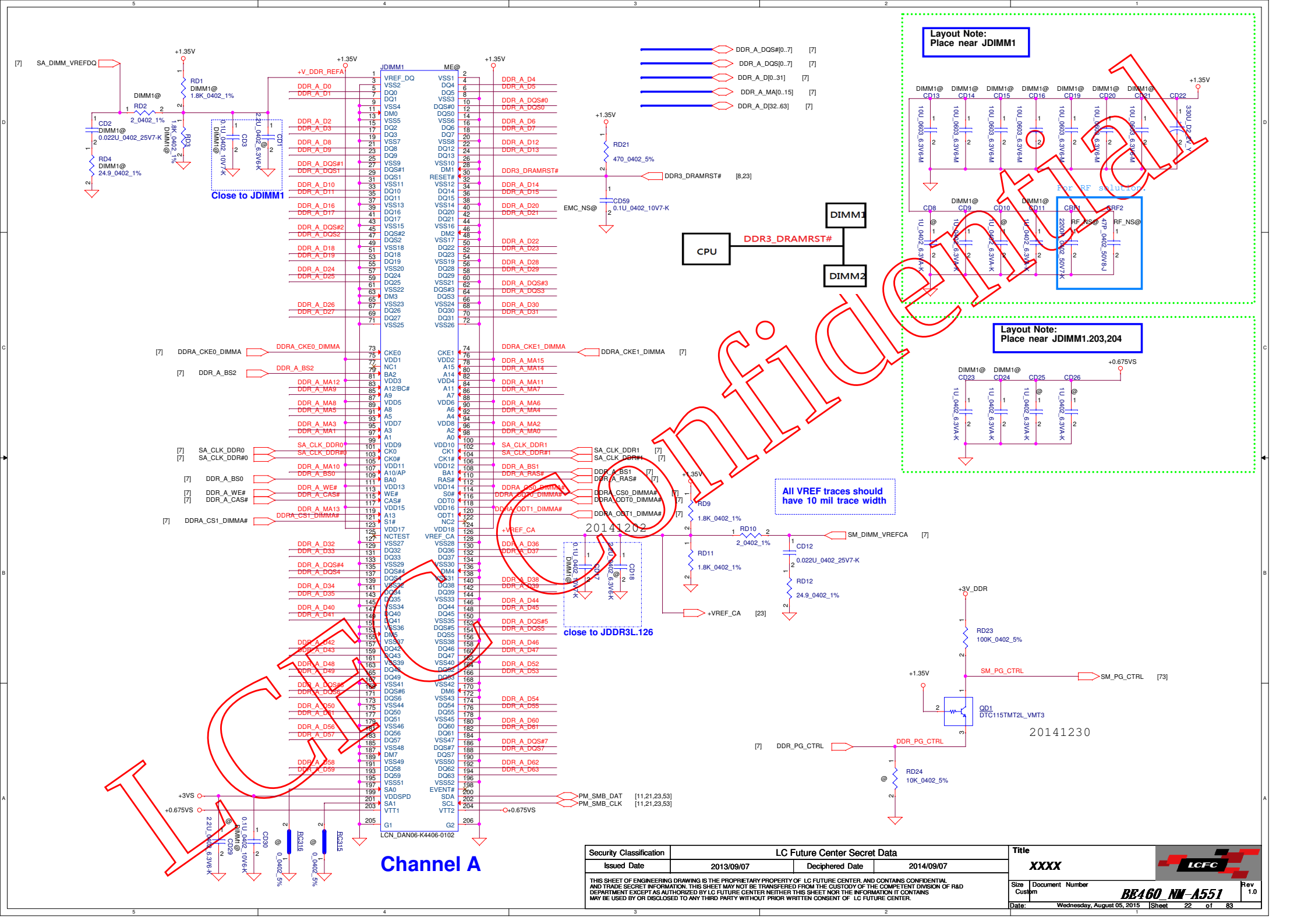

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: XXXX

LCFC

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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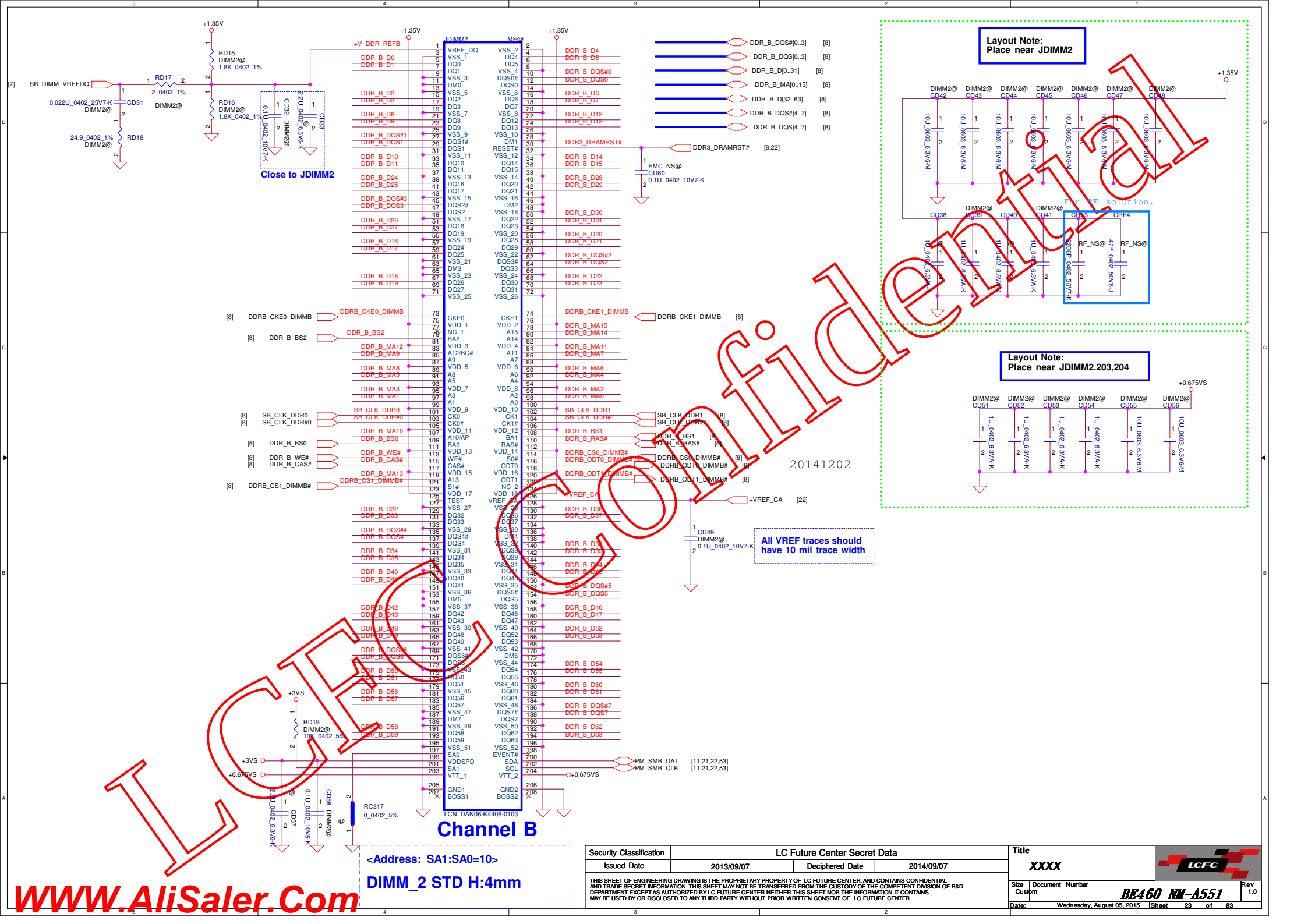

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

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Title: XXXX

Size	Document Number	Rev
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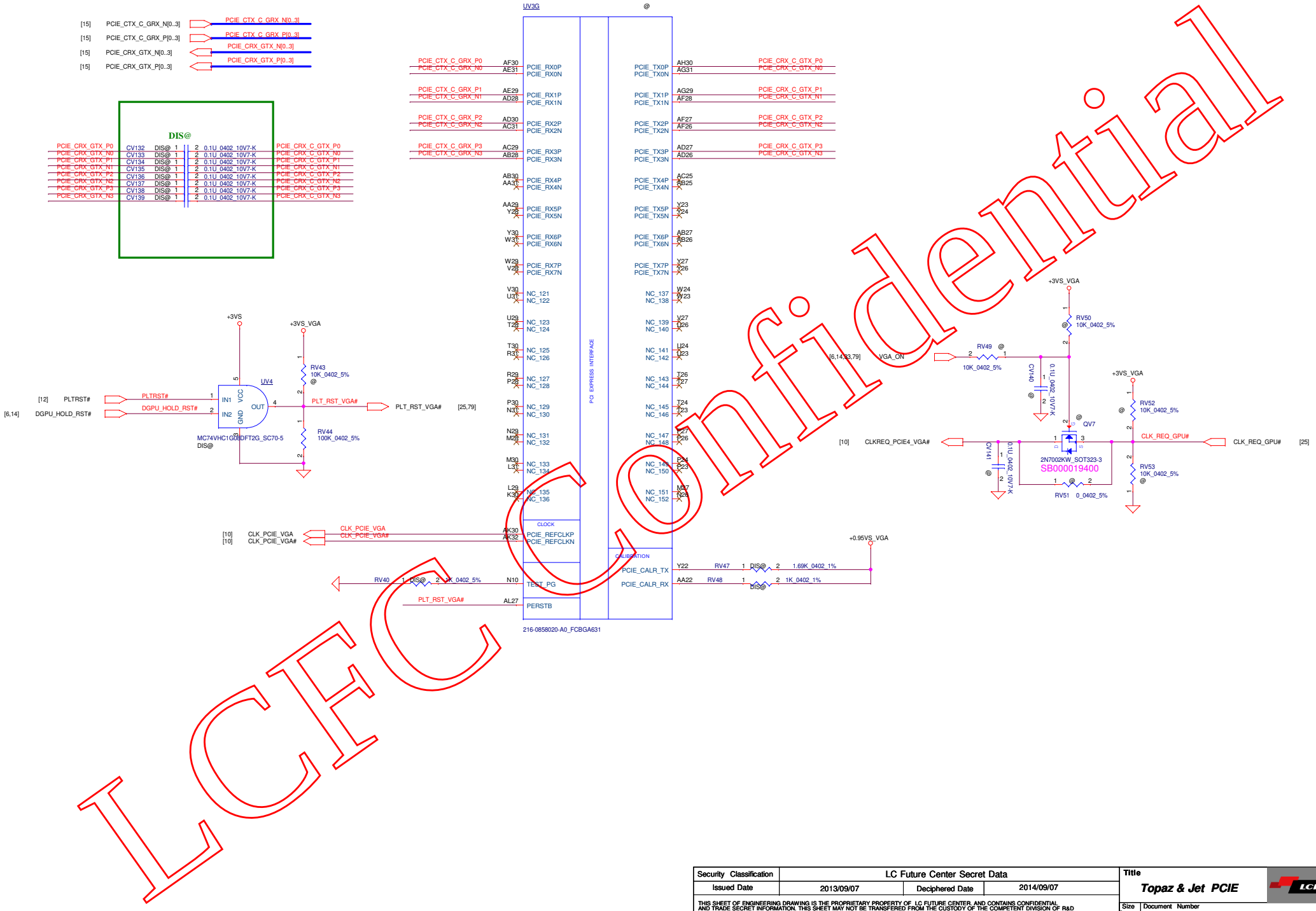

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: Topaz & Jet PCIE

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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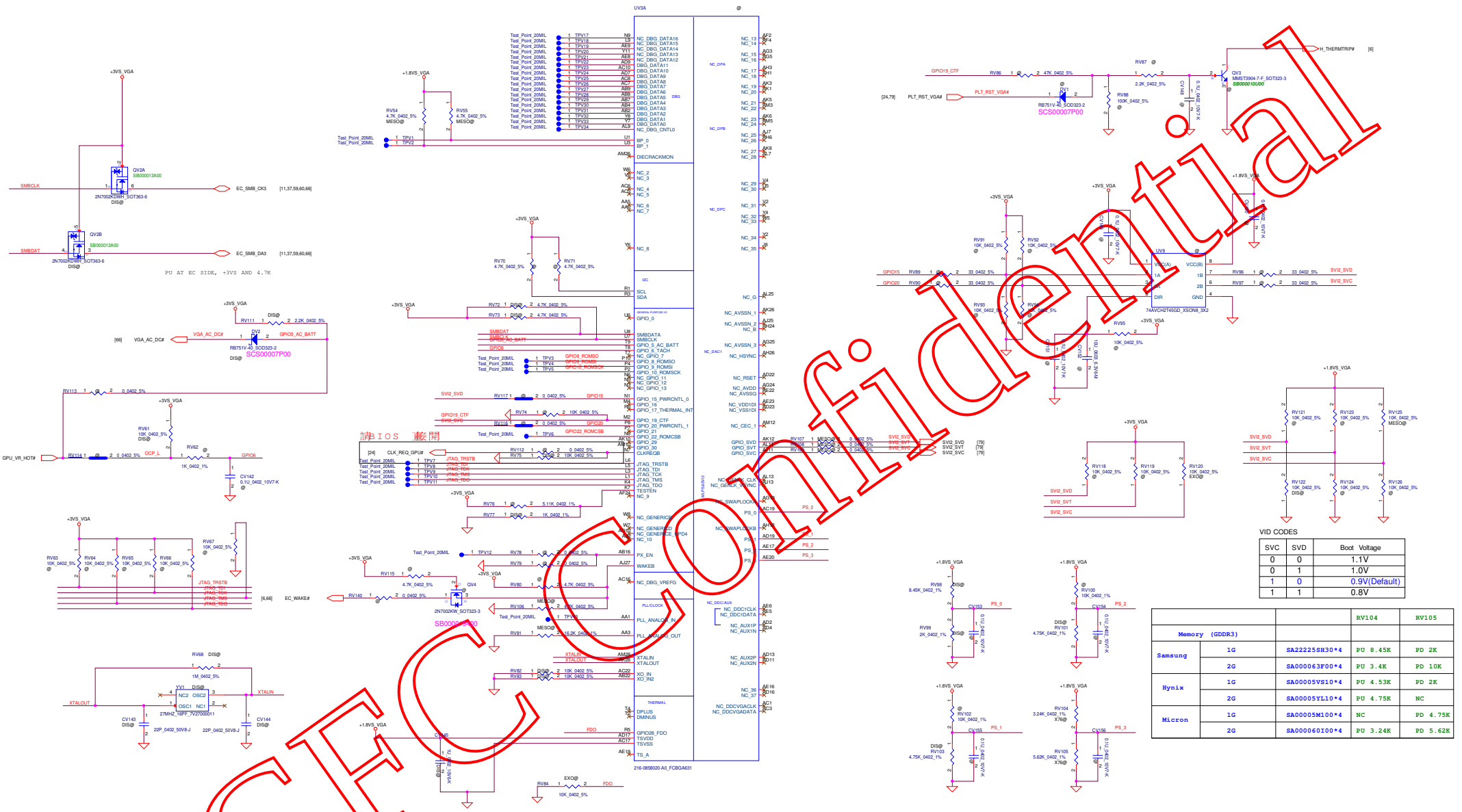

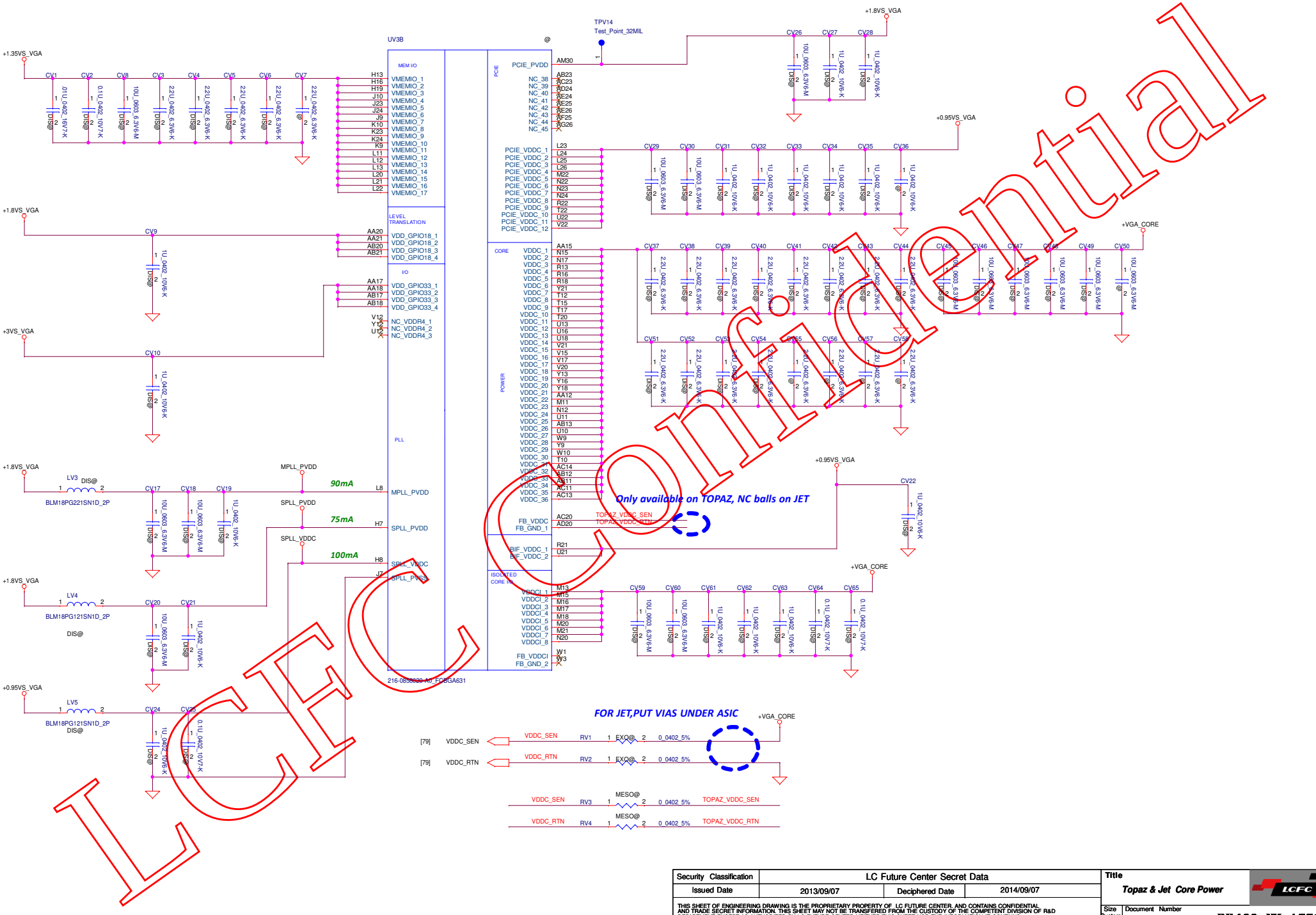

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	Topaz & Jet Core Power		
Size: Custom	Document Number: BE460_NM-A551		Rev: 1.0
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ASIC Ball	Topaz	Jet
U10,T10 AB13,W9 AB11,AB12 AC11,AC13 AC14,Y9,W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
J13,H16,H19,T10 J23,J24,J9,K10 K23,K24,K9,L11 L12,L13,L20,L21 L22	VMEMIO	VDDR1
AA17,AA18 AB17,AB18	VDD_GPIO33	VDDR3
AA20,AA21 AB20,AB21	VDD_GPIO18	VDD_CT

	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	1	1	0	0	0
PS2	0	0	0	0	0
PS3	1	1	?	?	?

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: Topaz & Jet DP Power/GND

Size	Document Number	Rev
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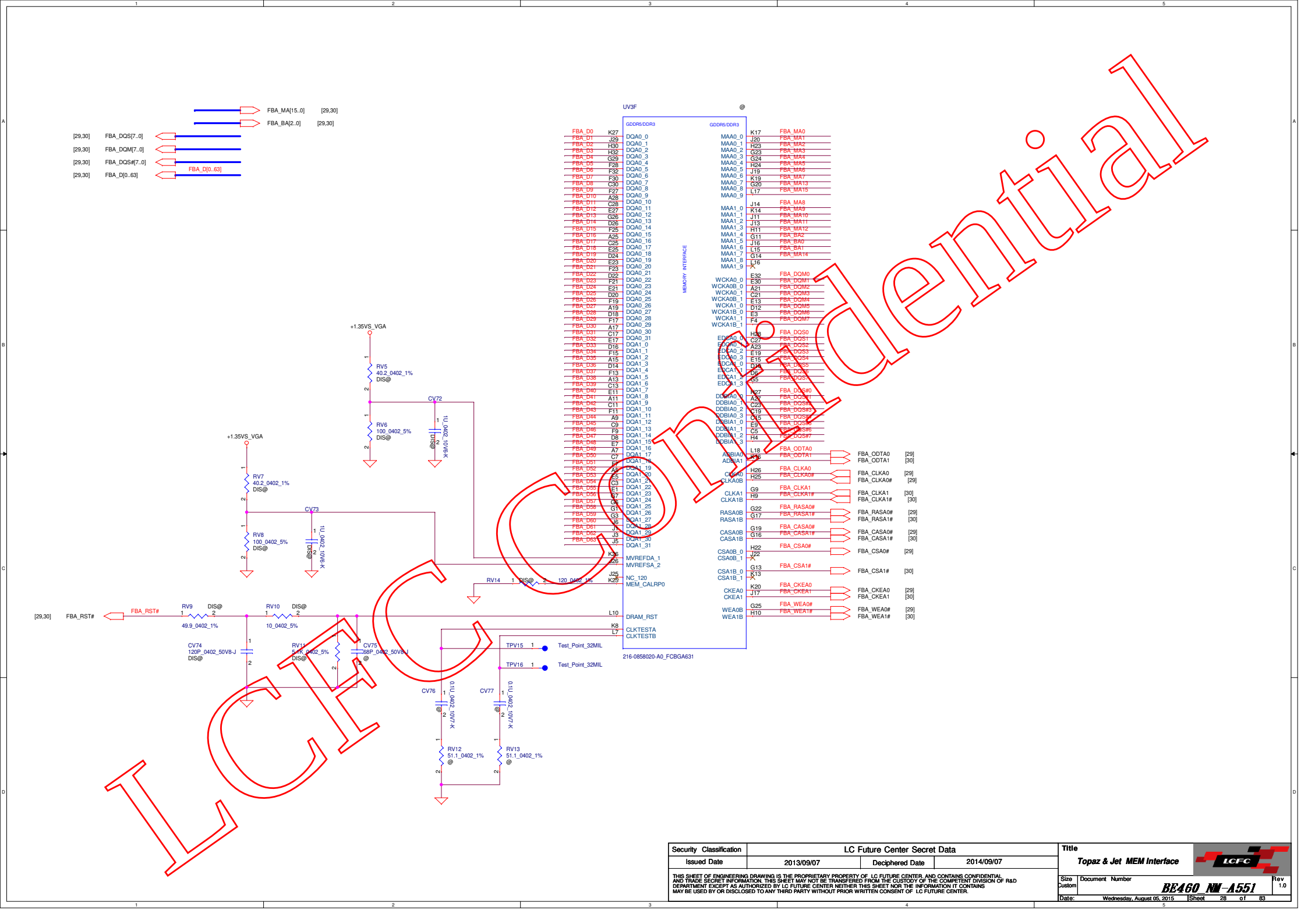

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: *Topaz & Jet MEM Interface*

Size	Document Number	Rev
Custom	BE460_MM-A551	1.0

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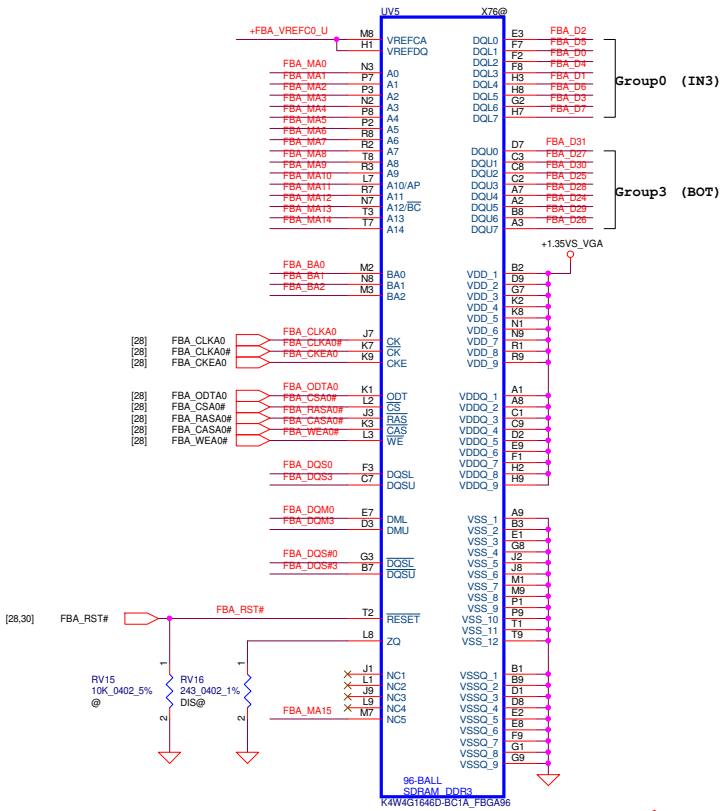
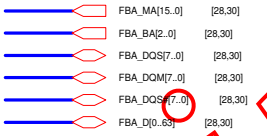
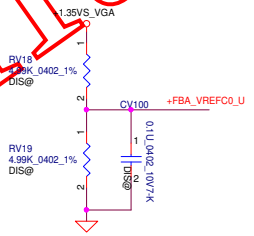
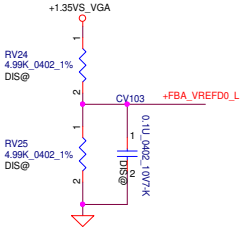
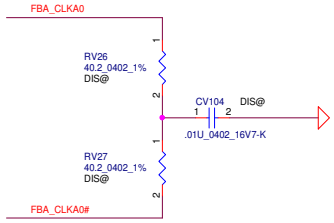
Memory Partition A - Lower 32 bits

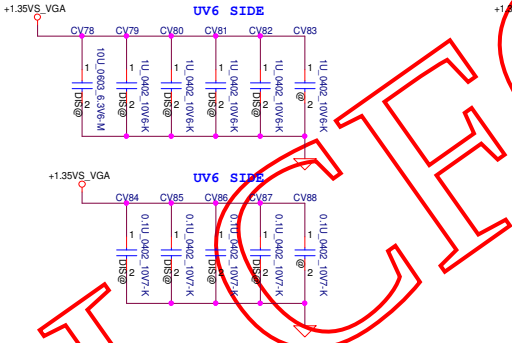


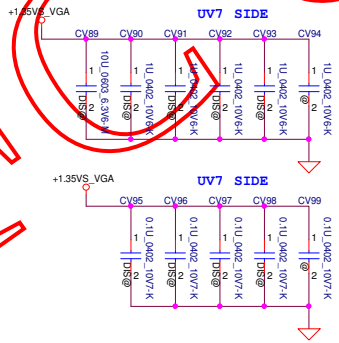












Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	Topaz & Jet DDR3 VRAM U		
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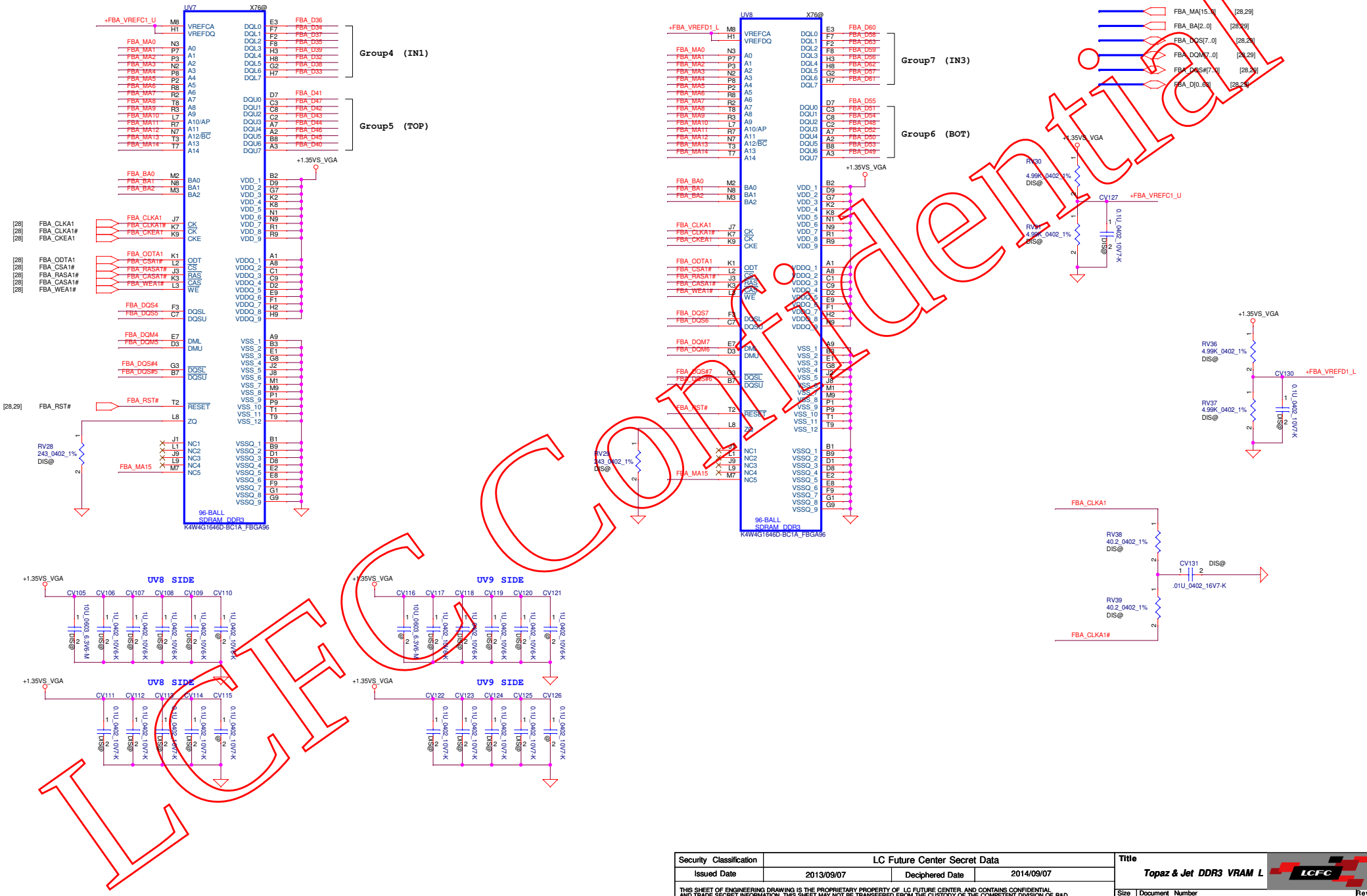
Memory Partition A - Upper 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	Topaz & Jet DDR3 VRAM L		
Size Custom	Document Number BE460_NM-A551		Rev 1.0
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Title: XXXX

Size	Document Number	Rev
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Title: XXXX

Size	Document Number	Rev
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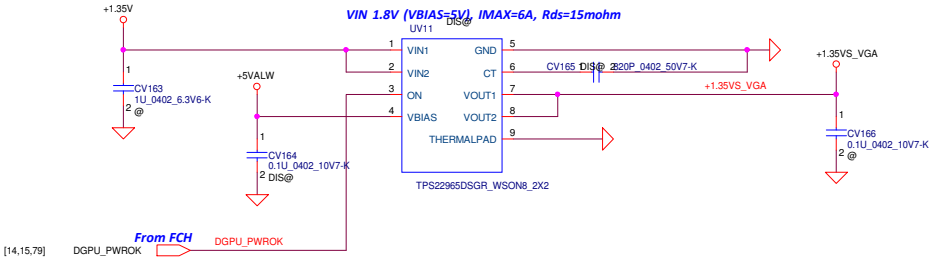
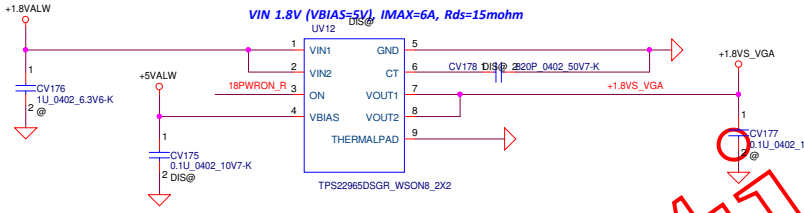
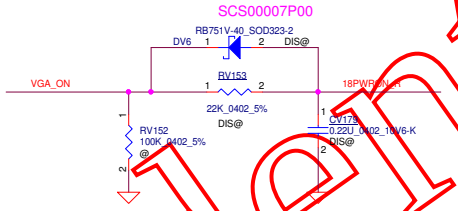
+1.35V to +1.35VS_VGA



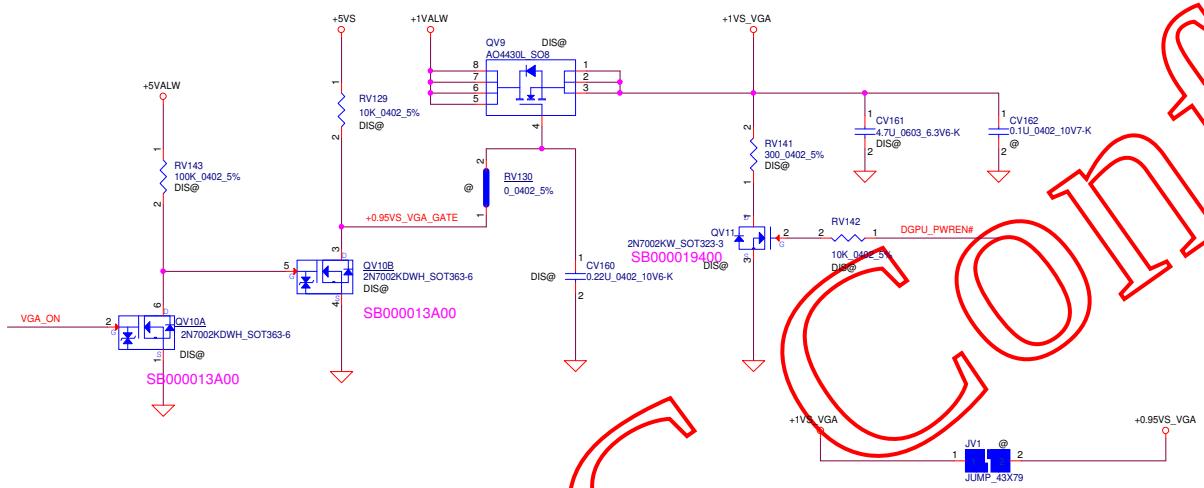
+1.8VALW to +1.8VS_VGA



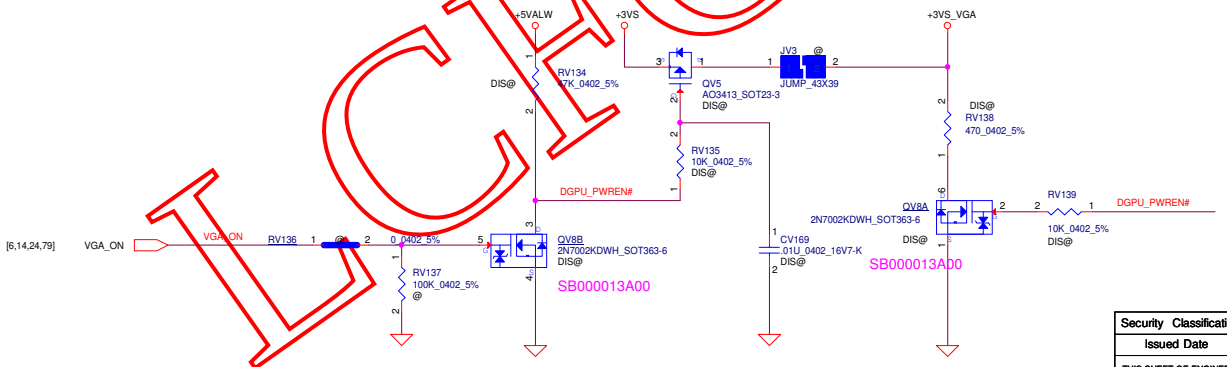
MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X



+1VALW to +1VS_VGA



+3VS to +3VS_VGA



PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled
PS_1[3]	N/A	0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)

Security Classification	LC Future Center Secret Data		
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Title: XXXX

Size	Document Number	Rev
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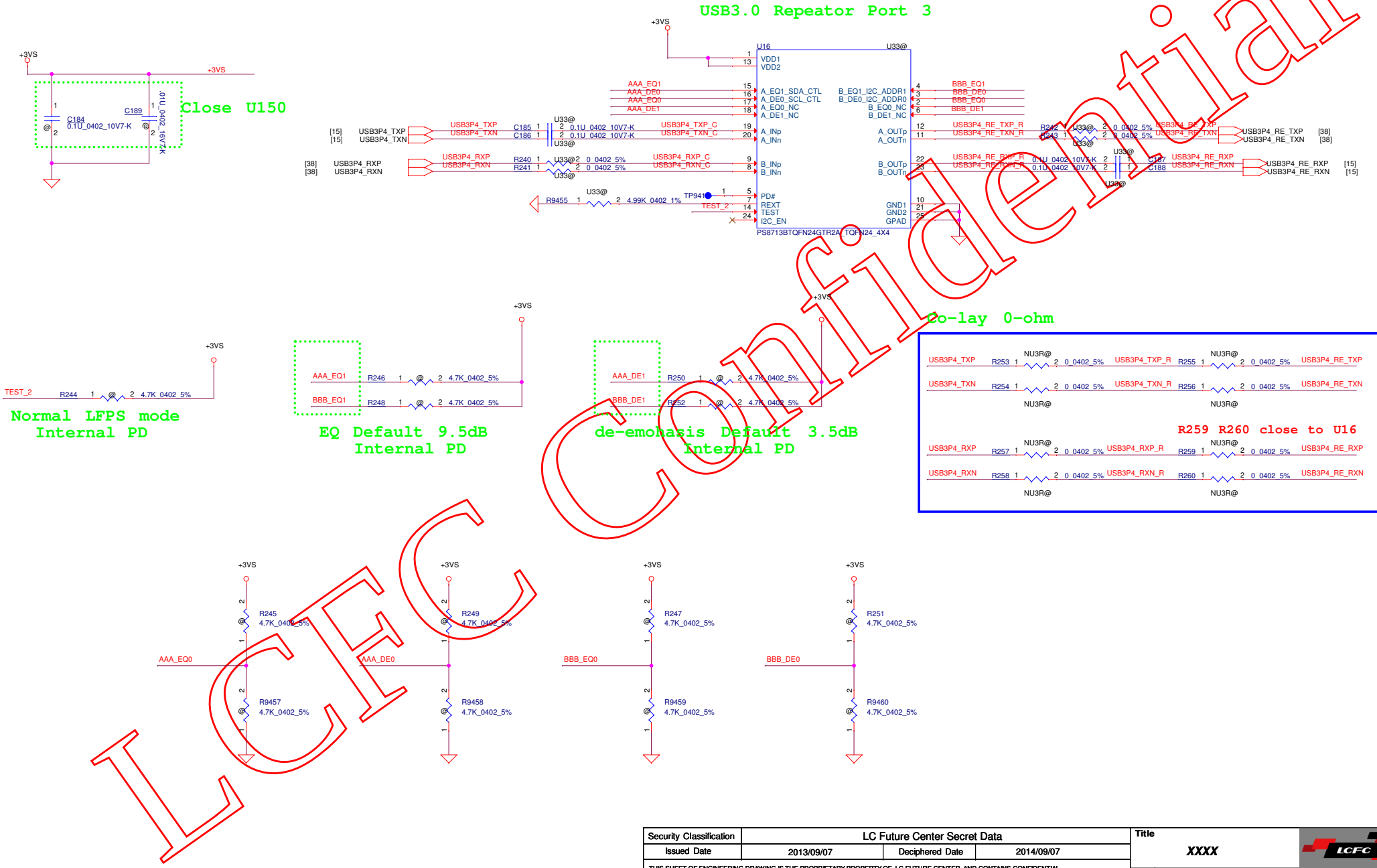

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	XXXX		
Size: Custom	Document Number: BE460_NM-A551		Rev: 1.0
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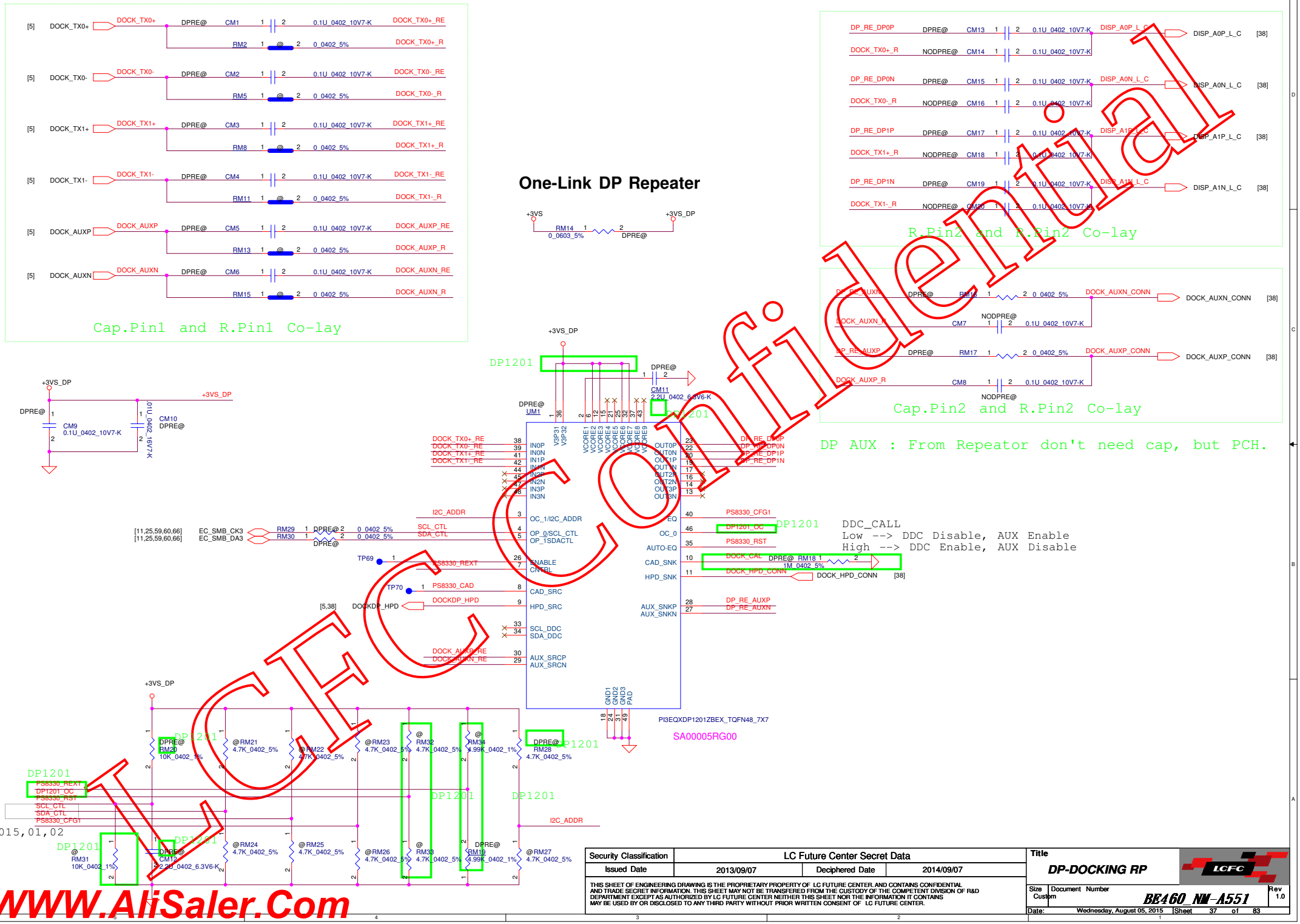

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

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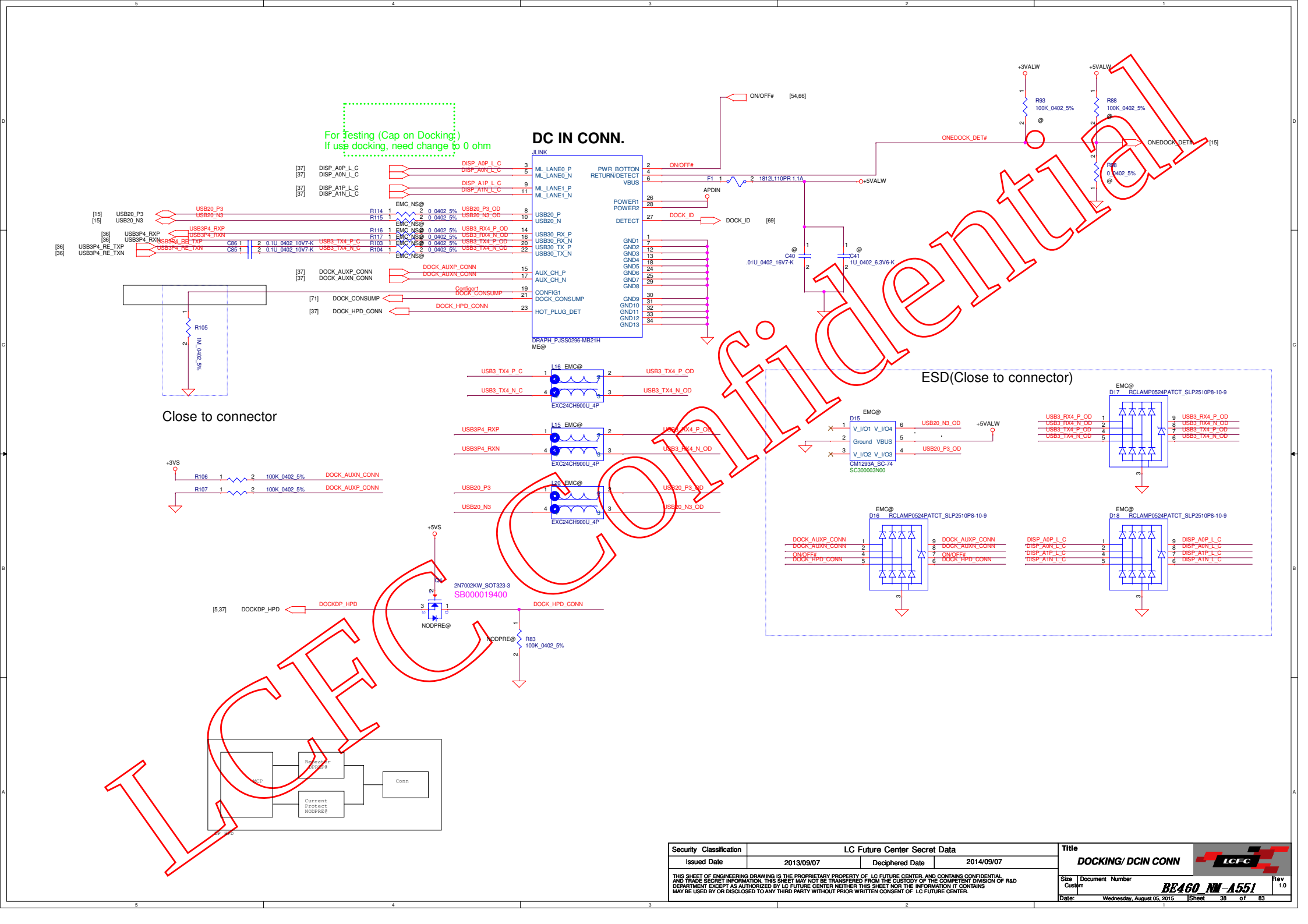
Title: DP-DOCKING RP

Size: Custom | Document Number: BE460_NM-A551 | Rev: 1.0

Date: Wednesday, August 05, 2015 | Sheet 37 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

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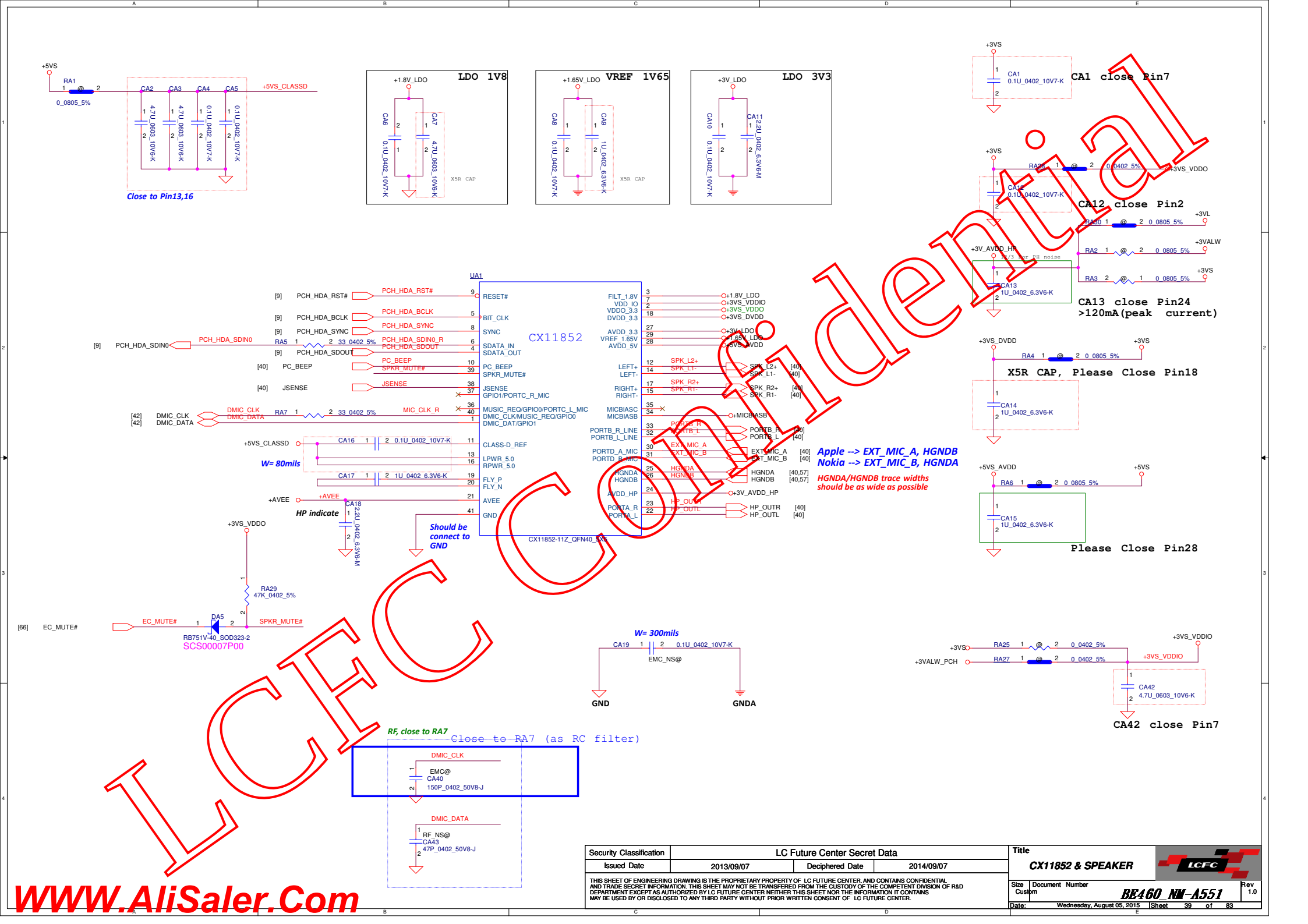
Title	DOCKING/ DCIN CONN		
Size	Document Number		Rev
Custom	BE460_NM-A551		1.0
Date:	Wednesday, August 05, 2015	Sheet	38 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	CX11852 & SPEAKER		
Size	Document Number		Rev
Custom	BE460_NM-A551		1.0
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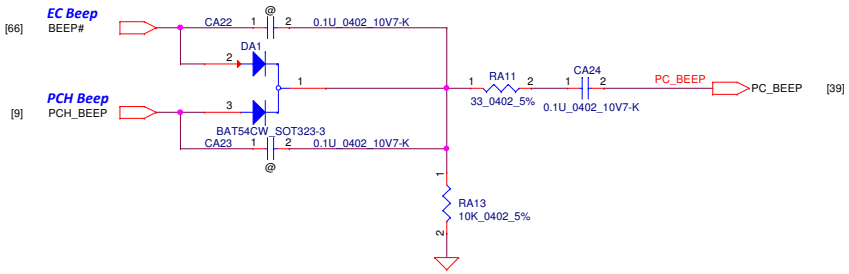
PC Beep



SPK CONN.

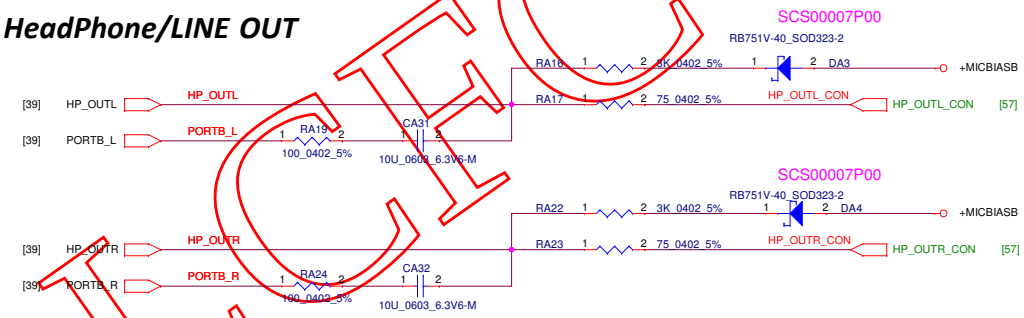
Speaker OUT

EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA

Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

HeadPhone/LINE OUT



CA31, CA32 change to 10U for Quality requirement

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: HP/MIC JACK

Size	Document Number	Rev
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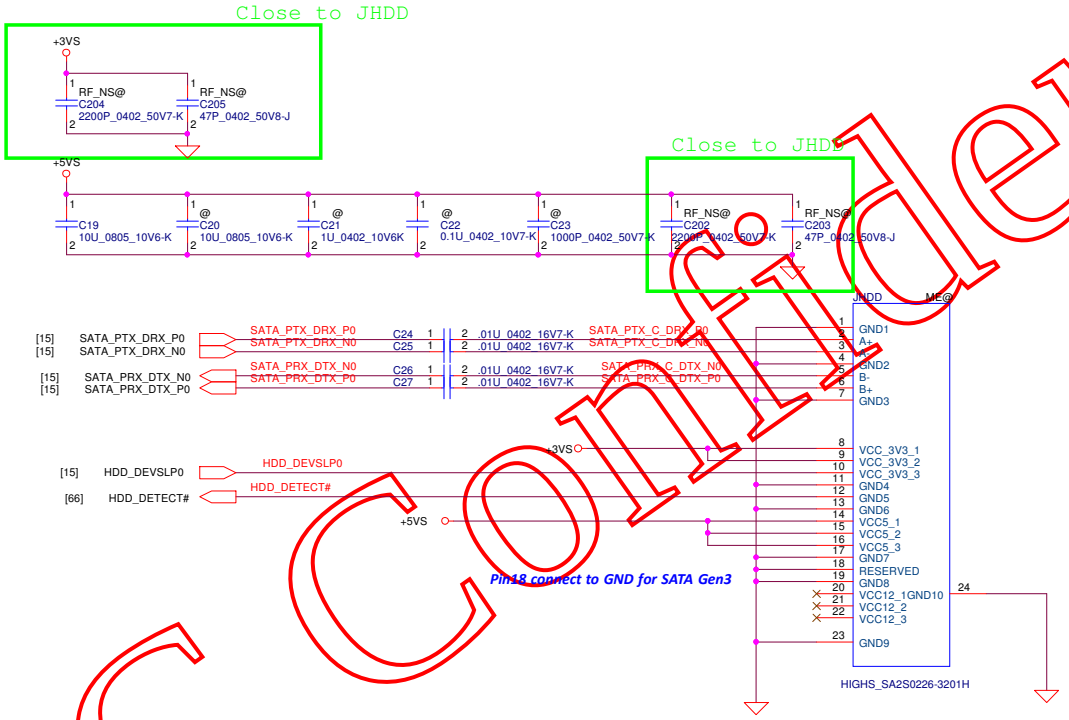
SATA HDD CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: SATA HDD/ODD

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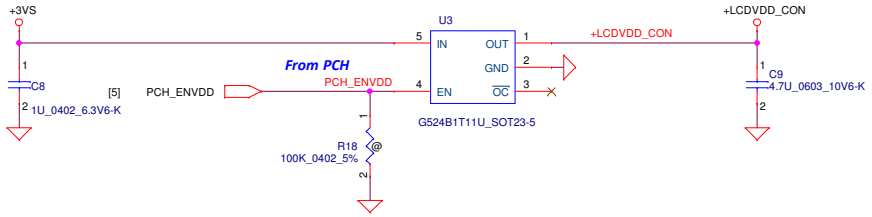
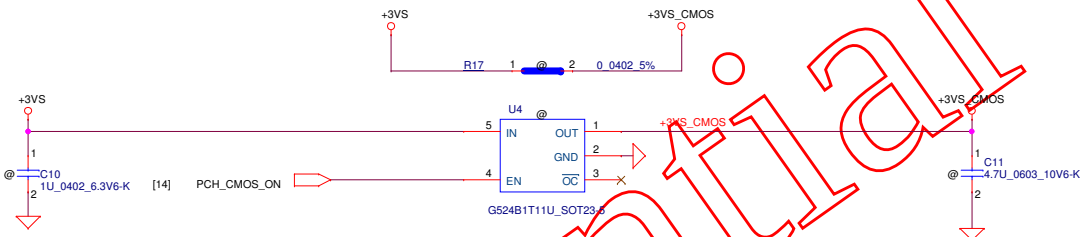
LCDVDD Circuit

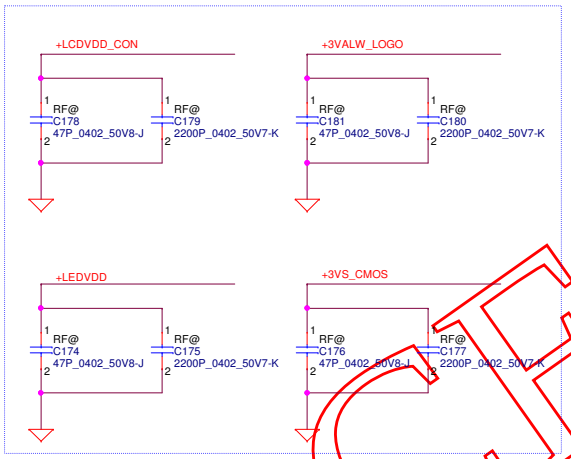


CMOS Camera

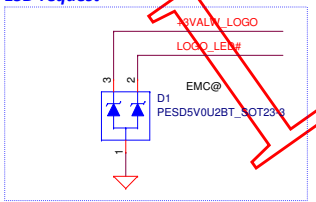
For A phase test



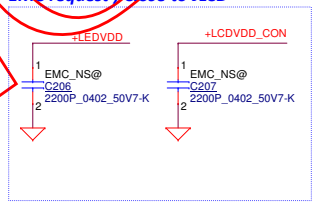
RF

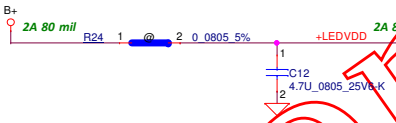


ESD request

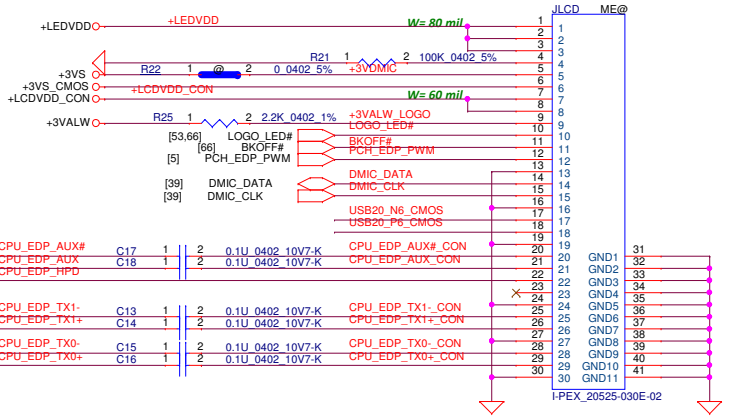


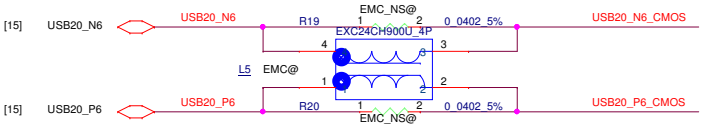
EMC request , Close to JLCD

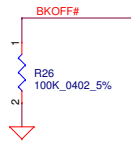




eDP CONN.







Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	eDP/CMOS		
Size	Document Number		Rev
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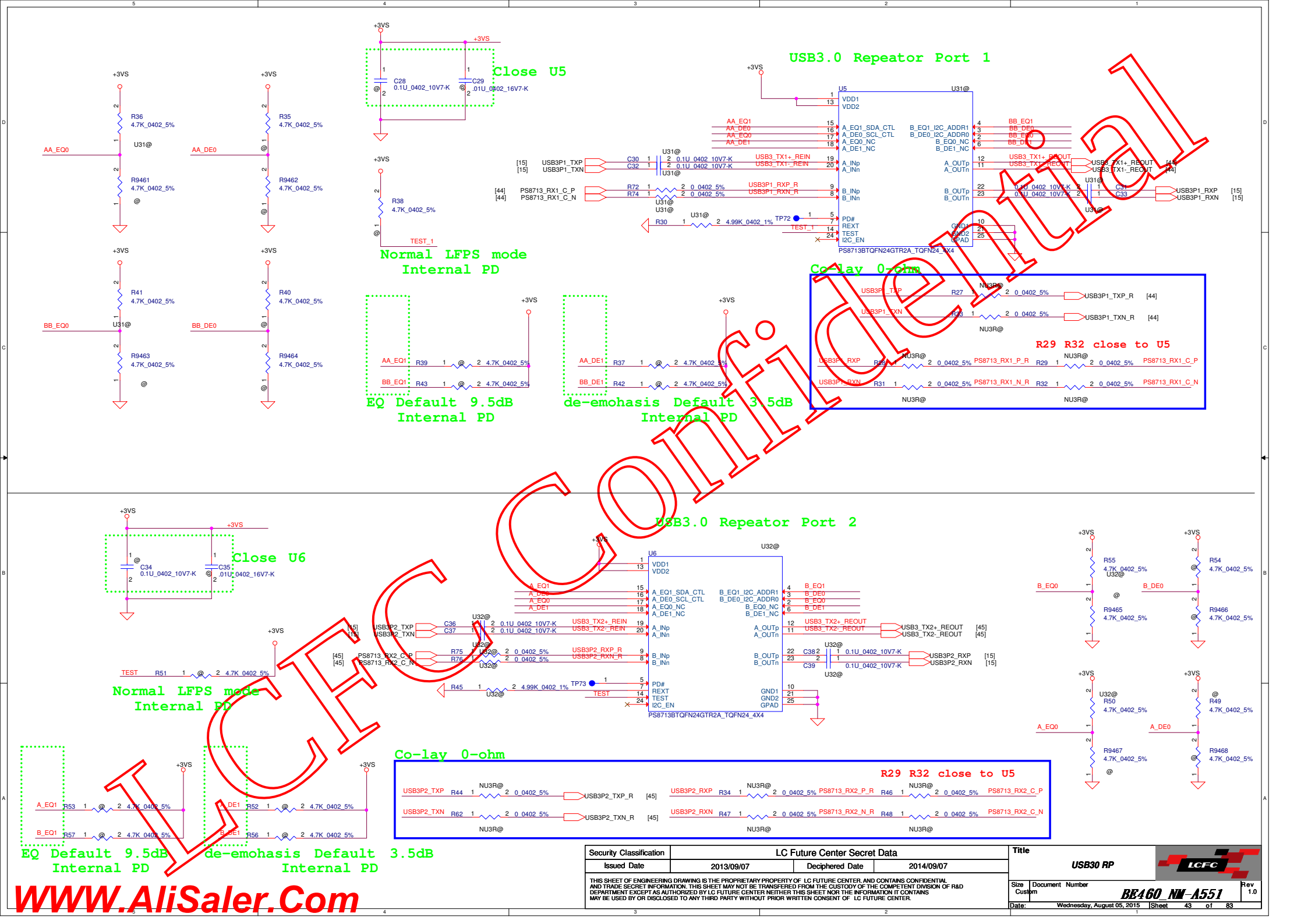

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

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Title: USB30 RP

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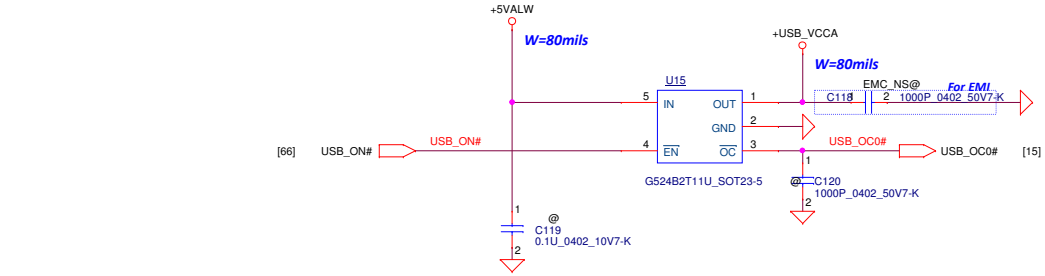
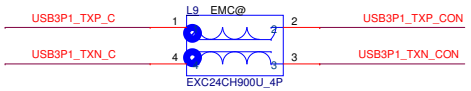
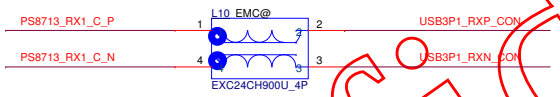
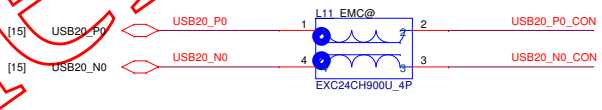
Broadwell Connector (USB+S&C)

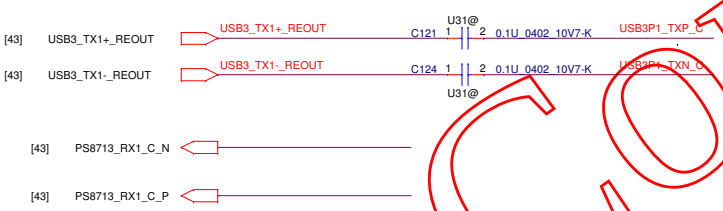
For 14" use(14" on board USB don't support S&C
,But 15" on board USB support S&C.S&C IC always on MB)

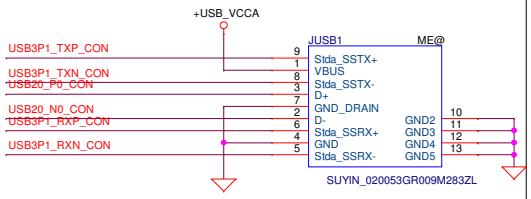


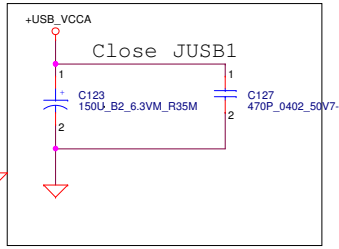




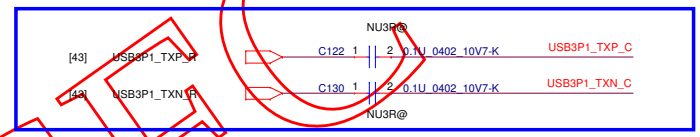


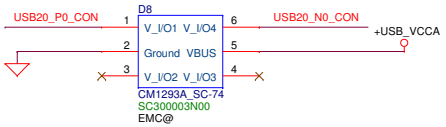


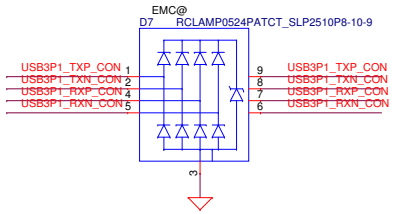




Co-lay 0-ohm







Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: USB3 PORT1

Size	Document Number	Rev
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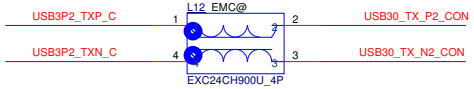
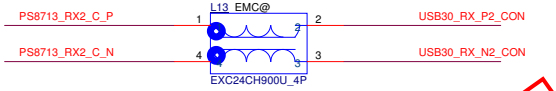
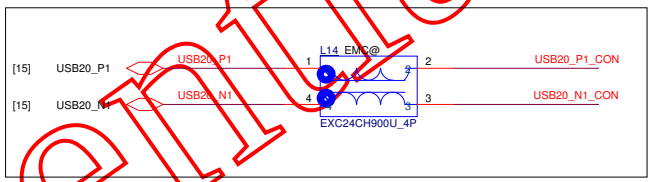
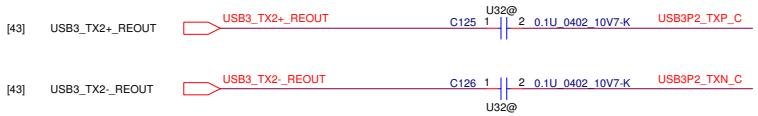
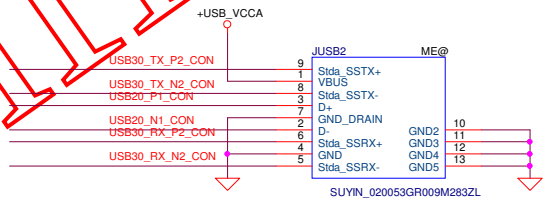


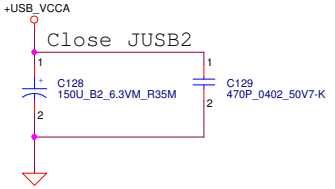


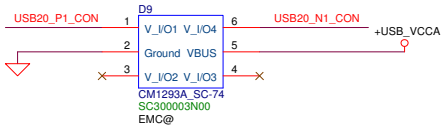
Co-layout L15 for EMI test

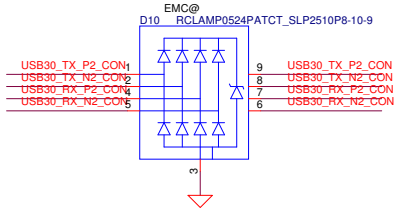




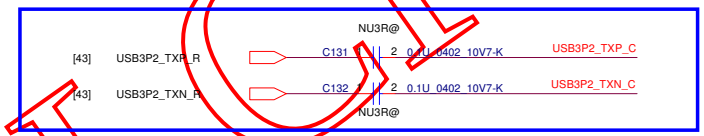








Co-lay 0-ohm



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: USB3 PORT2

Size	Document Number	Rev
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Title: XXXX

Size	Document Number	Rev
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Title: XXXX

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Title: XXXX

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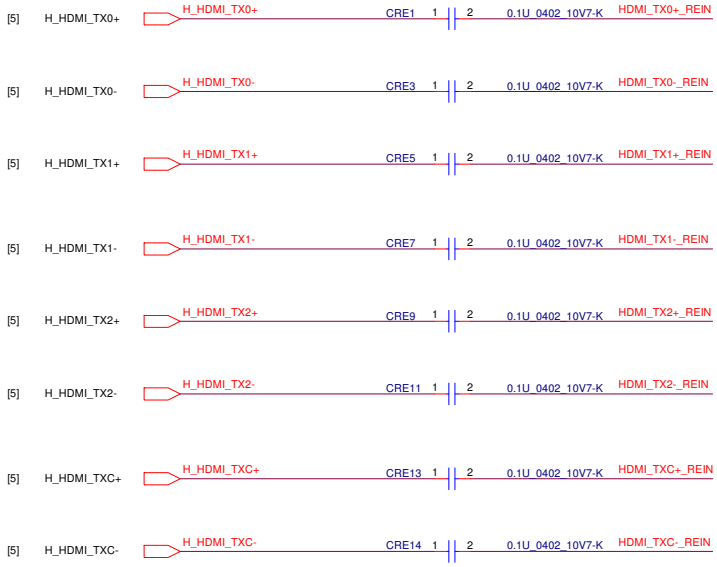
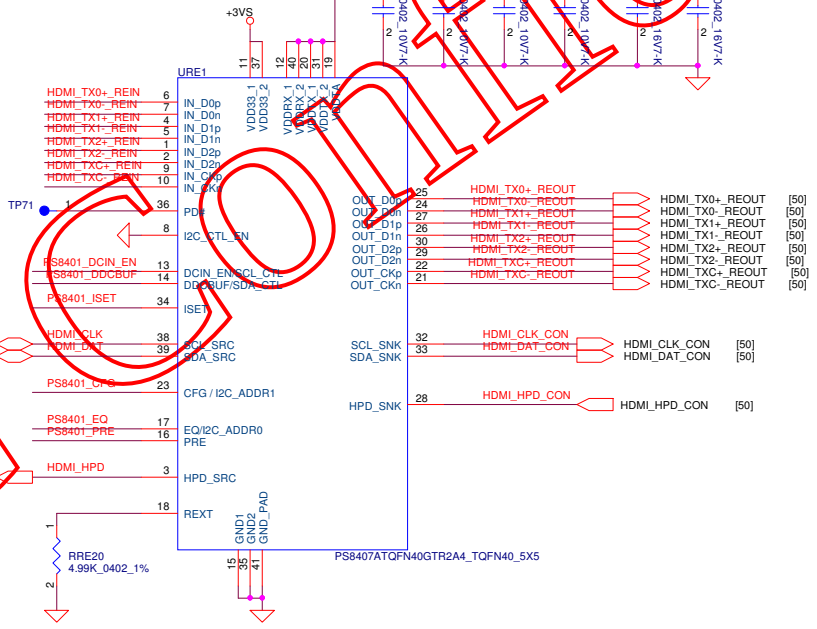
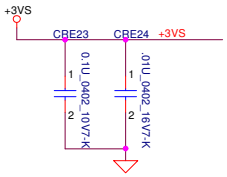
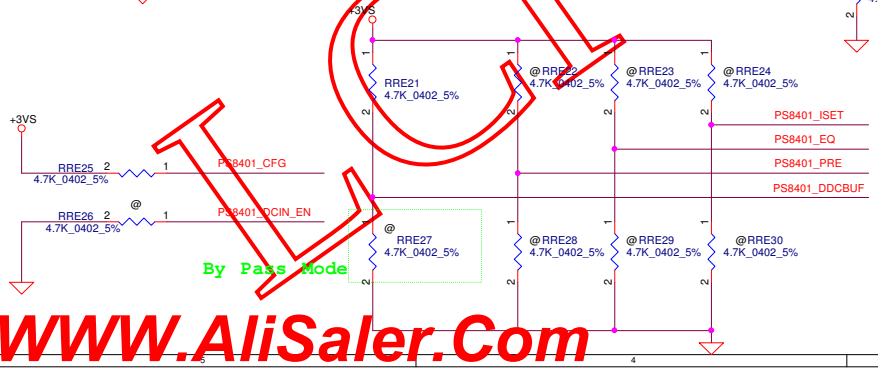
HDMI Repeater









Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	HDMI RP		
Size	Document Number		Rev
Custom	BE460_NM-A551		1.0
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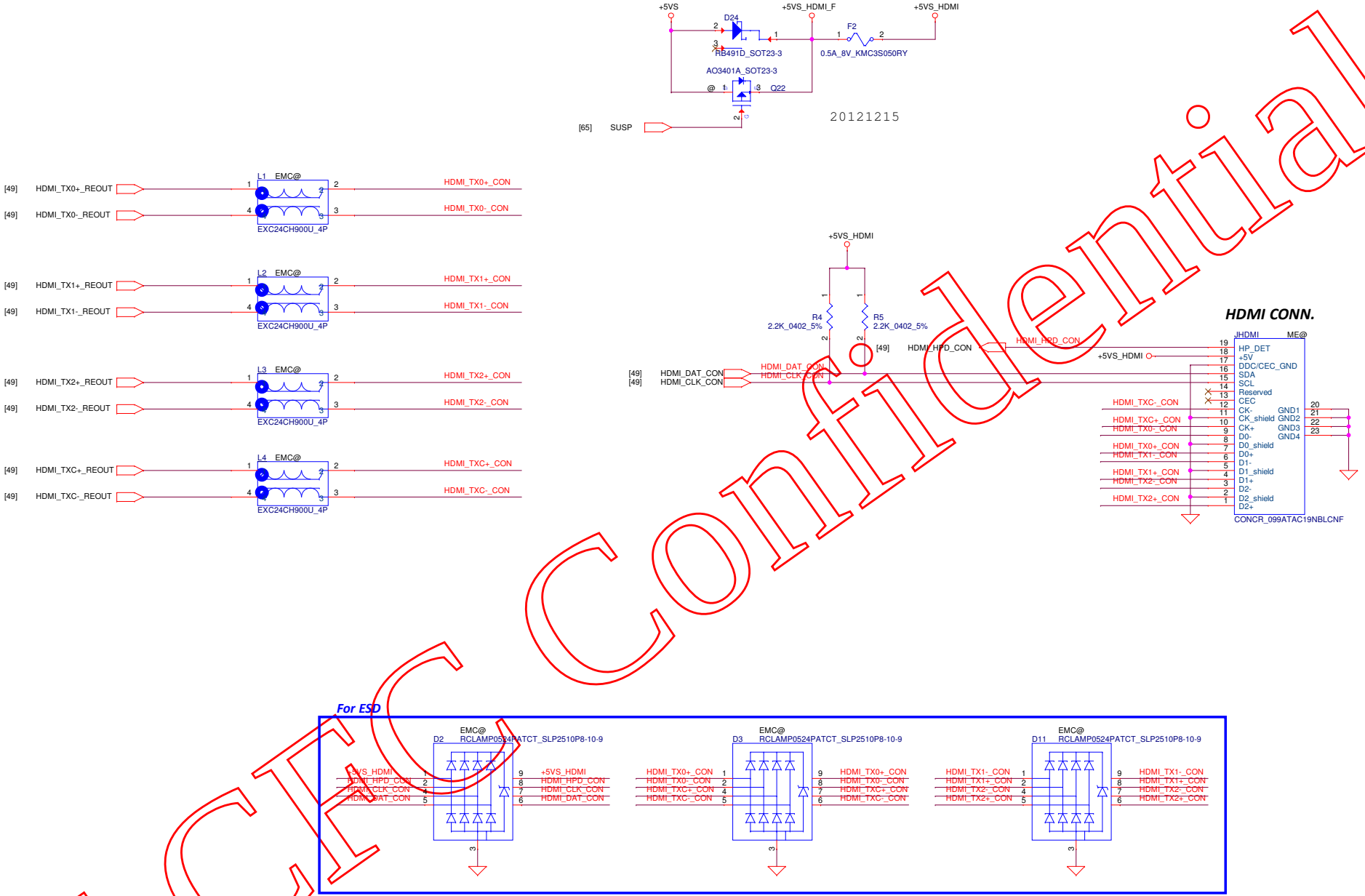

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **HDMI CONN.**

Size	Document Number	Rev
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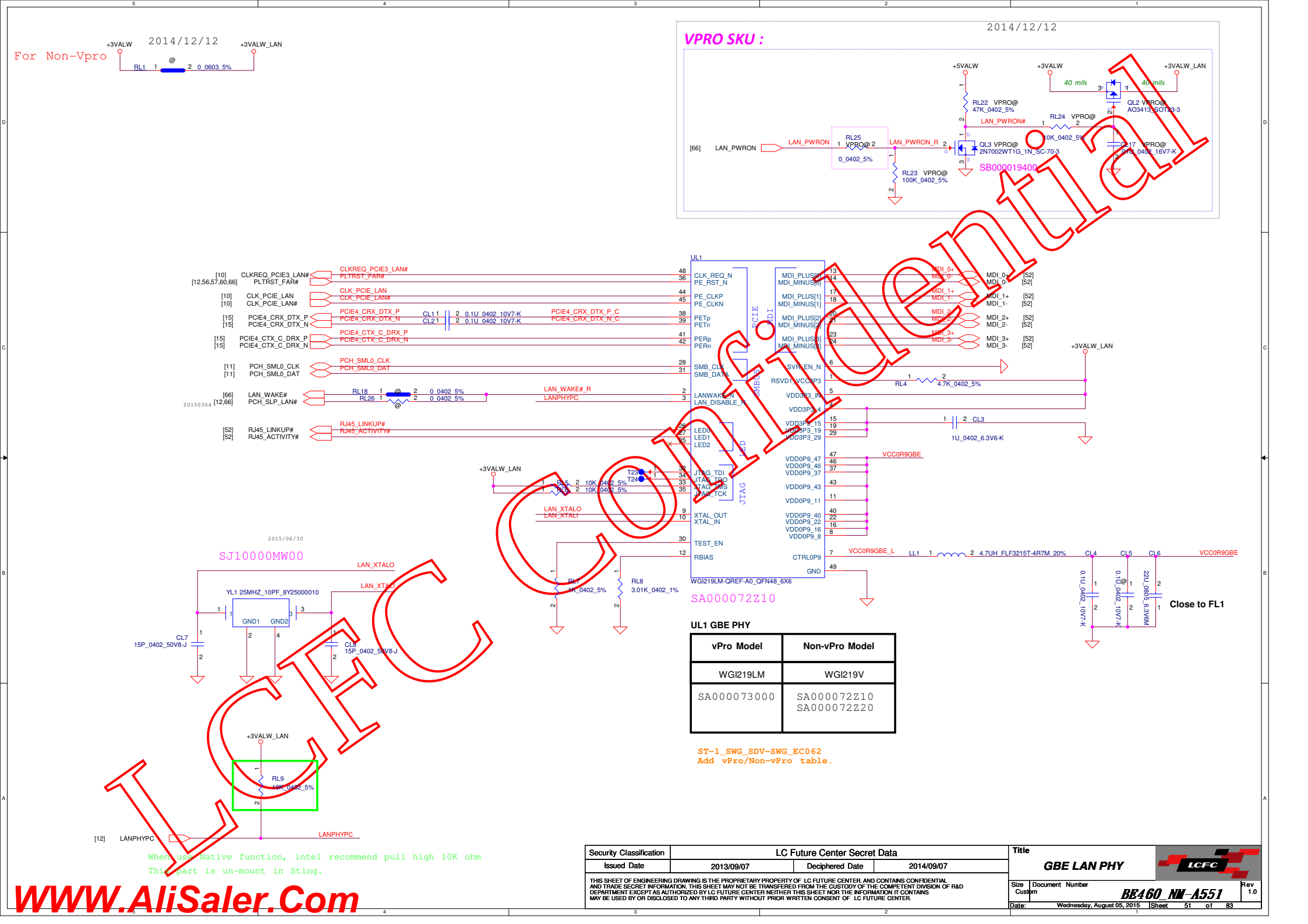

UL1 GBE PHY

vPro Model	Non-vPro Model
WGI219LM	WGI219V
SA000073000	SA000072Z10 SA000072Z20

ST-1_SWG_SDV-SWG_EC062
Add vPro/Non-vPro table.

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **GBE LAN PHY**

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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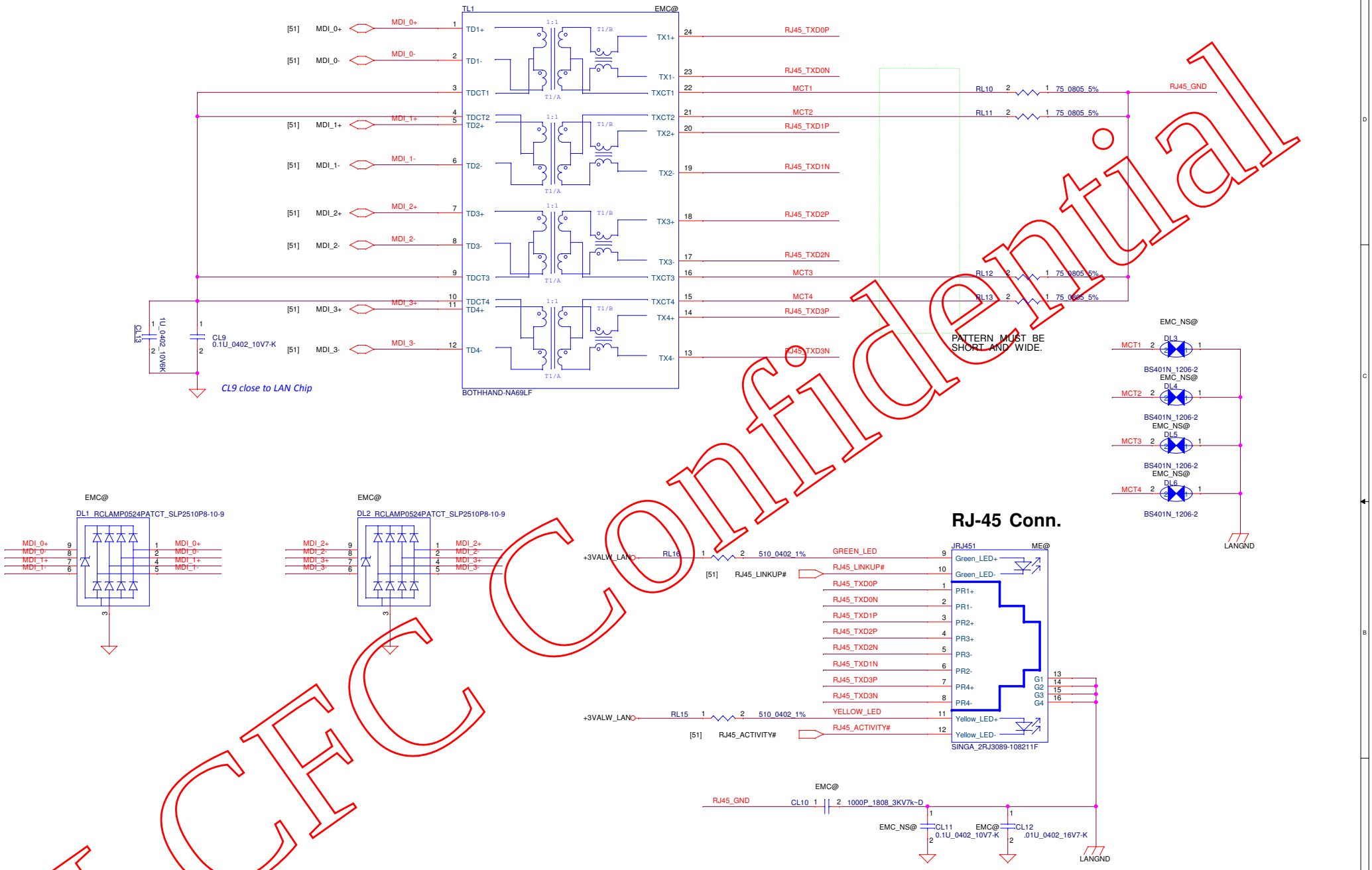

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	RJ45 CONN.		
Size	Document Number		Rev
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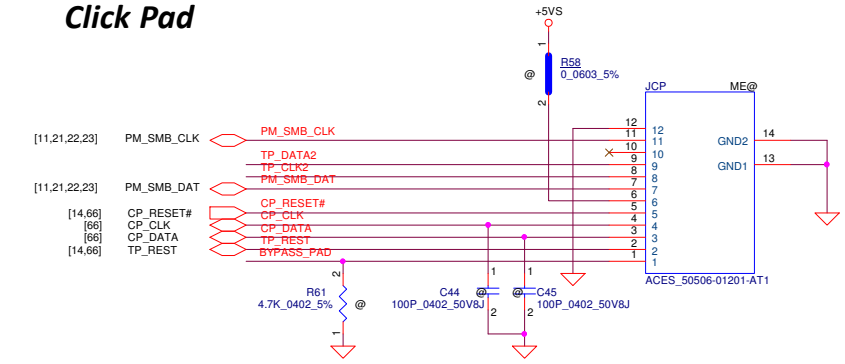
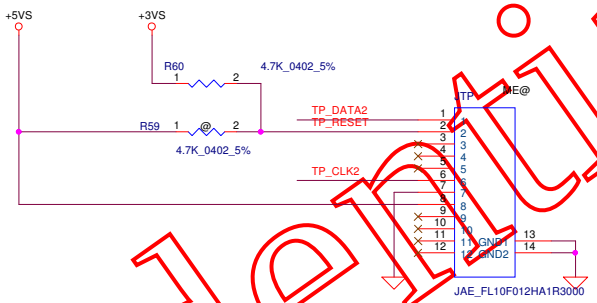
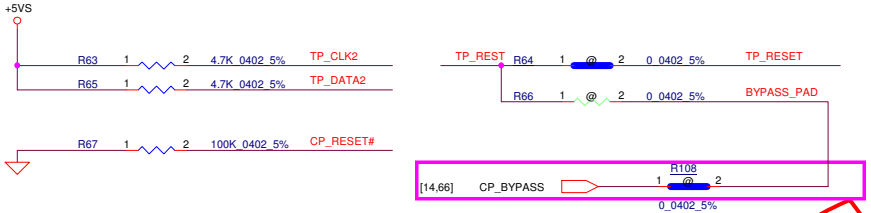
Click Pad

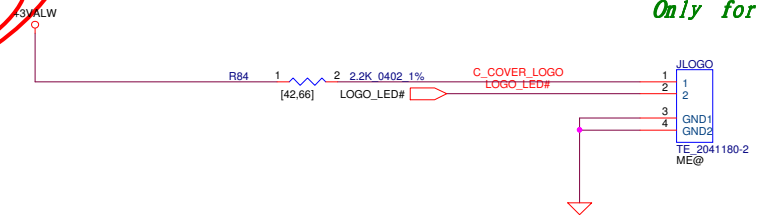


Track point





Only for Edge 14"



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: CP/TPOINTCONN.

Size	Document Number	Rev
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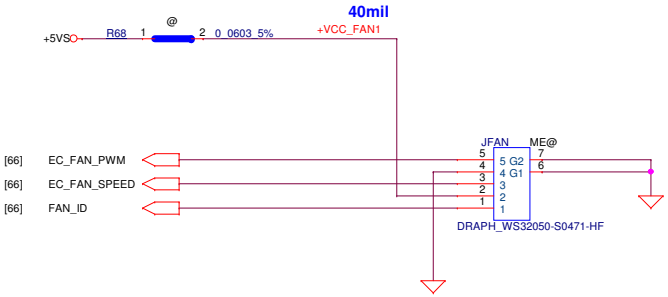
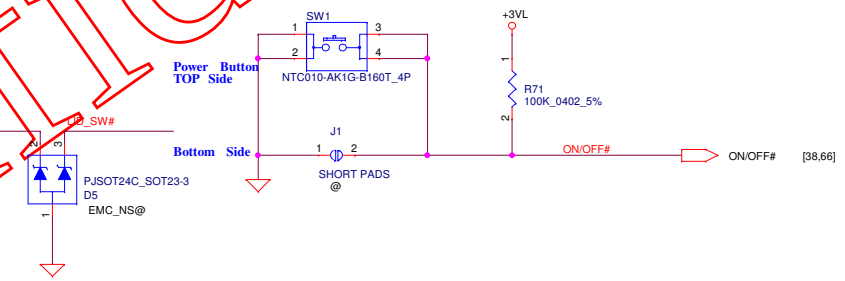
FAN CONN.



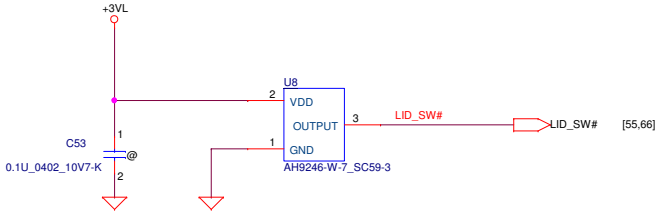
PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

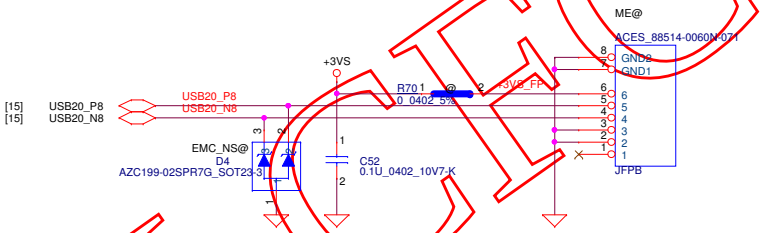
ON/OFF switch



Lid Switch



FingerPrint CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: PBTN/LID/FP/FAN CONN.

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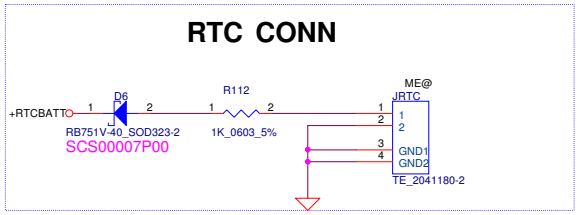
[66] KSI[0..7] KSI[0..7]

[66] KSO[0..17] KSO[0..17]

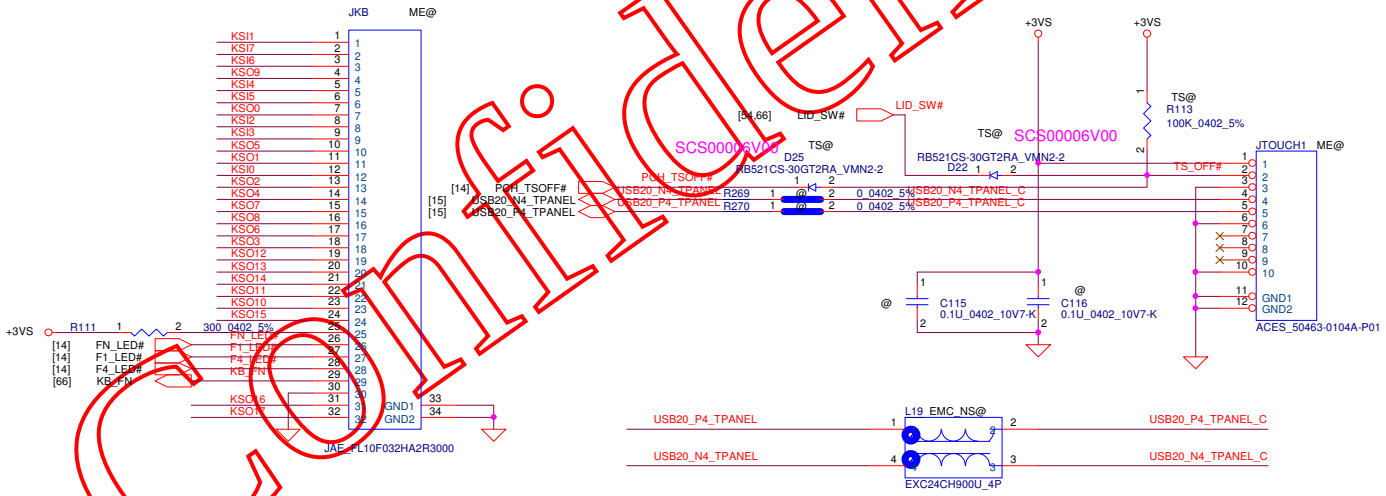
Key Board Signal From EC

KeyBoard CONN.(14")

RTC CONN



Touch Panel CONN. For 14"



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: KB/RTC/TOUCH PAN CONN.

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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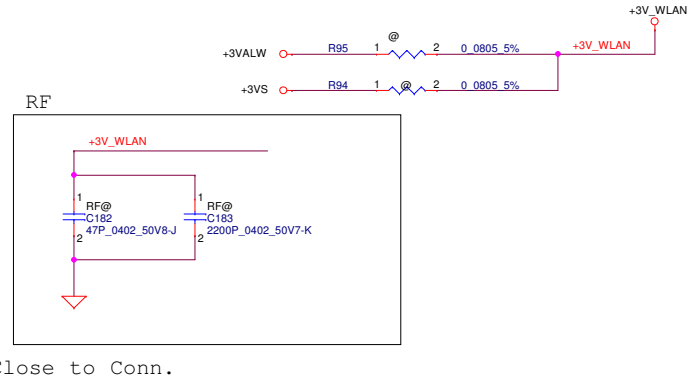
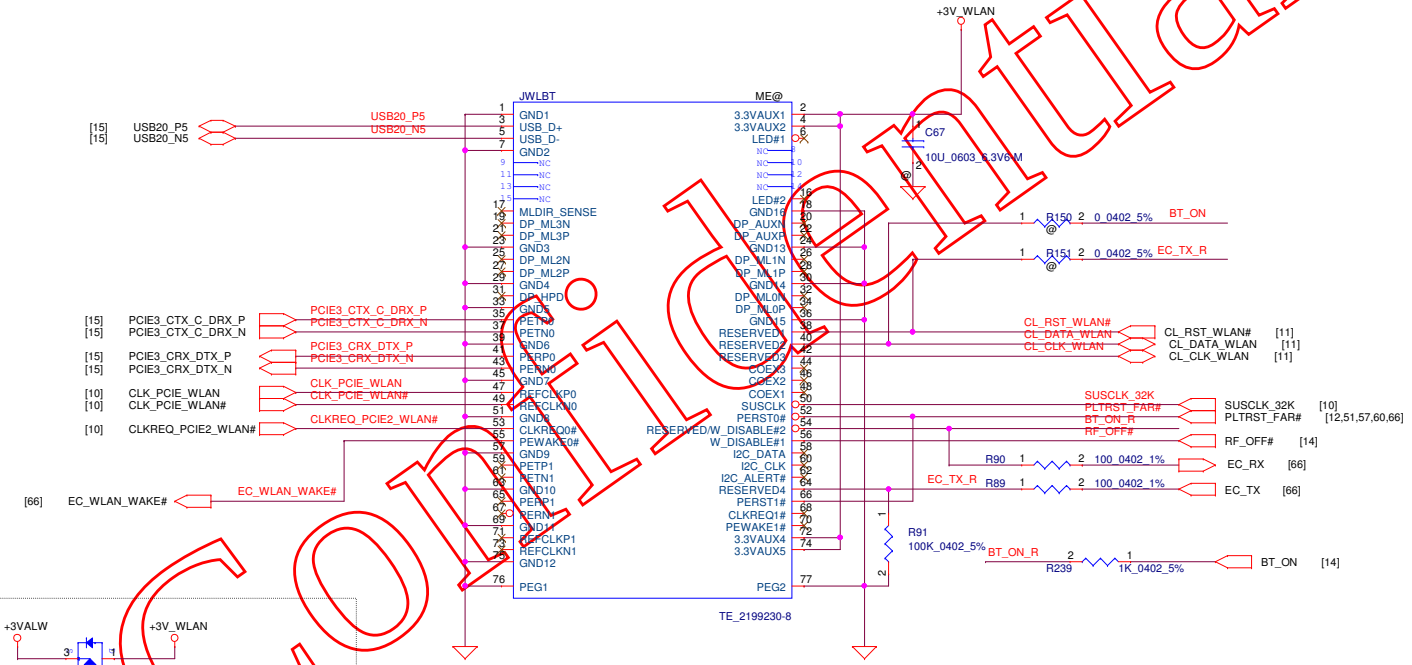
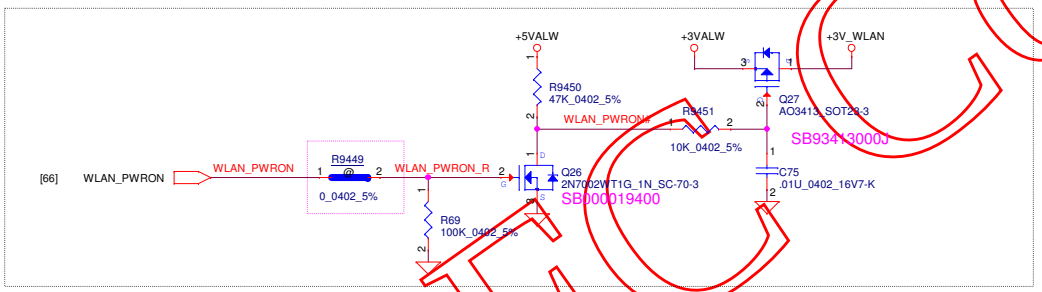
TYPE-A NGFF CCARD FOR WLAN

3.2H CONNECTOR







Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	WWAN/WLAN NGFF CONN.
Size	Custom
Document Number	BE460_NM-A551
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Date:	Wednesday, August 05, 2015
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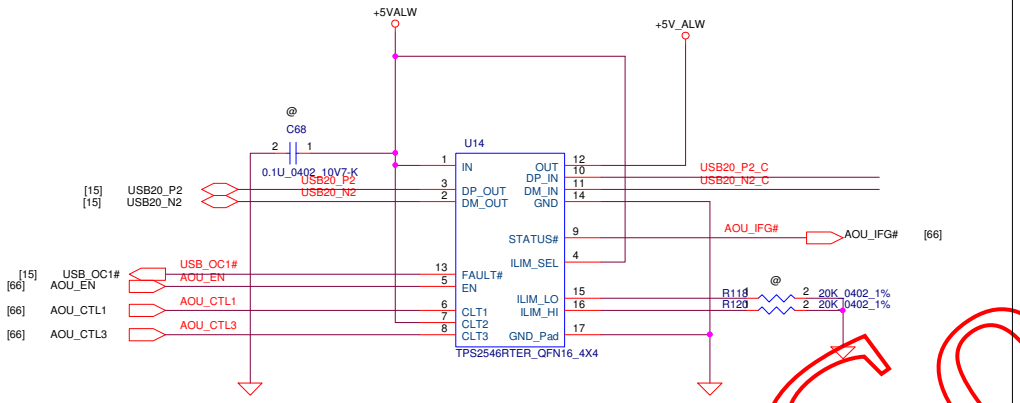
For 14"

CardReader Board : FFC

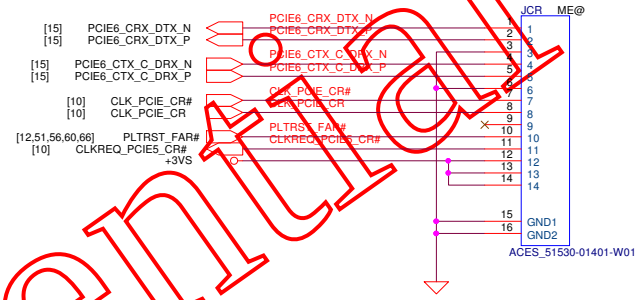
For 14" S&C IC on MB) S&C port on SUB/B

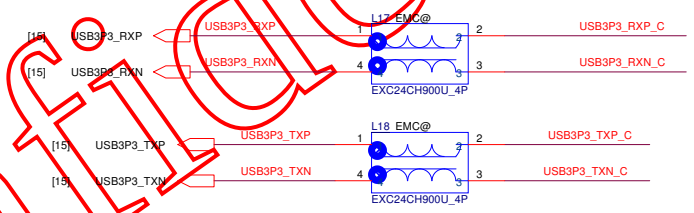


TI TPS2546

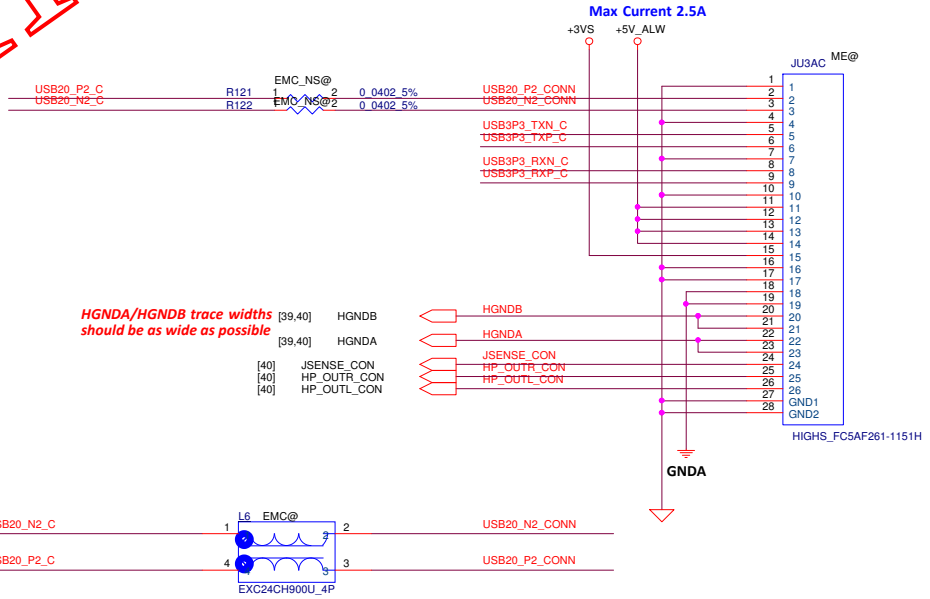
	CLT1	CLT2	CLT3	ILIM_SEL	MOD	
	0	0	0	X	DCH	OUT held low
*	1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
*	1	1	1	0	SDP2	Data Connected
*	1	1	0	X	SDP1	Data Connected
*	0	1	0	X	SDP1	Data Connected
	1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
	1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
*	0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
	0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

USB_OC5# to MCP
AOU_EN to EC
AOU_CTL1 to EC
AOU_CTL3 to EC
AOU_IFG# to EC





Max Current 2.5A



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **SUB CONN.**

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

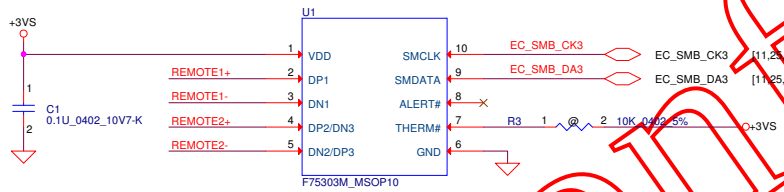
Title: XXXX

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

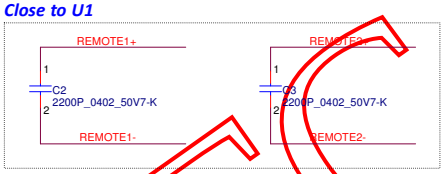
Date: Wednesday, August 05, 2015 Sheet 58 of 83

Thermal Sensor

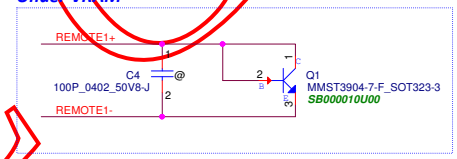
Thermal Sensor
placed near by VRAM



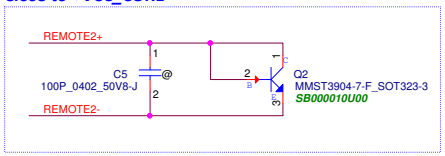
Close to U1



Under VRAM



Close to +VCC_CORE



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

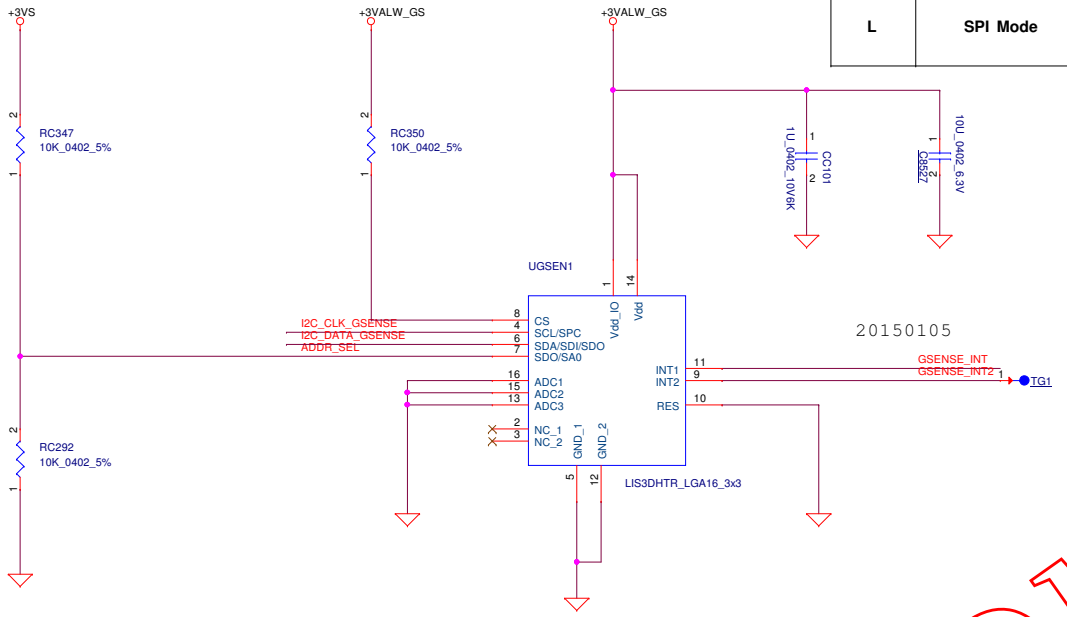
Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

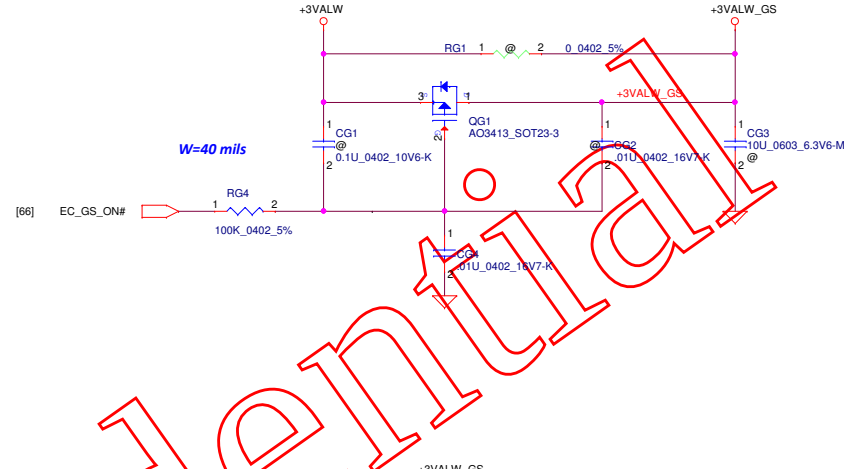
Title	THERMAL SENSOR	
Size: Custom	Document Number: BE460_NM-A551	Rev: 1.0
Date: Wednesday, August 05, 2015	Sheet 59 of 83	

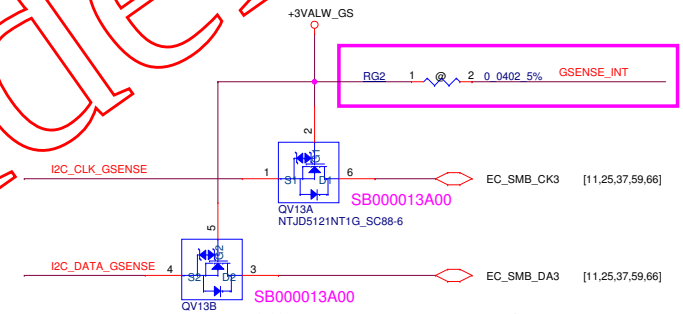
APS G-Sensor

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode

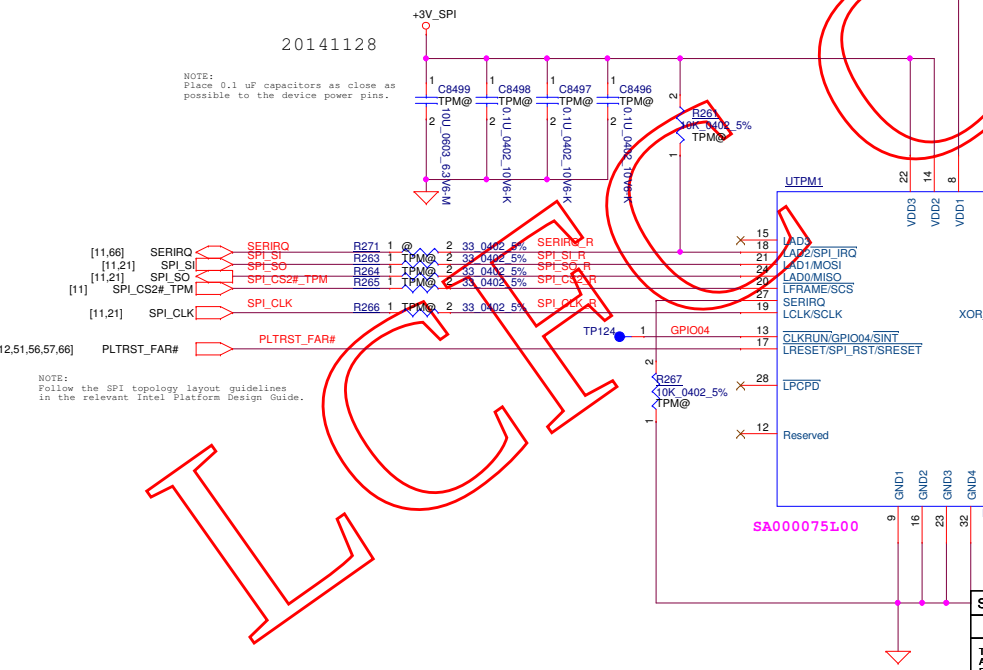




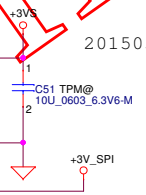


Only for UMA SKU

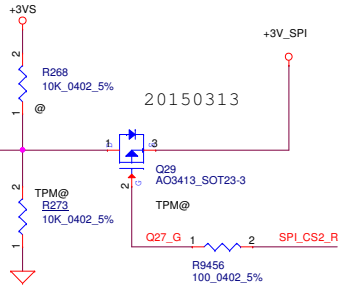
20141128



20150305



20150313



20150313

TABLE

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

	Q29	R268	R273	R9456
New silicon NPCT650LB0YX	X	O	X	X
Current silicon NPCT650LA0YX	O	X	O	O

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: G SENSOR/TPM

Size: Custom | Document Number: BE460_NM-A551 | Rev: 1.0

Date: Wednesday, August 05, 2015 | Sheet 60 of 83

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: RF

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

Date: Wednesday, August 05, 2015 Sheet 61 of 83

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title

XXXX

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

Date: Wednesday, August 05, 2015 Sheet 62 of 83

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: XXXX

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

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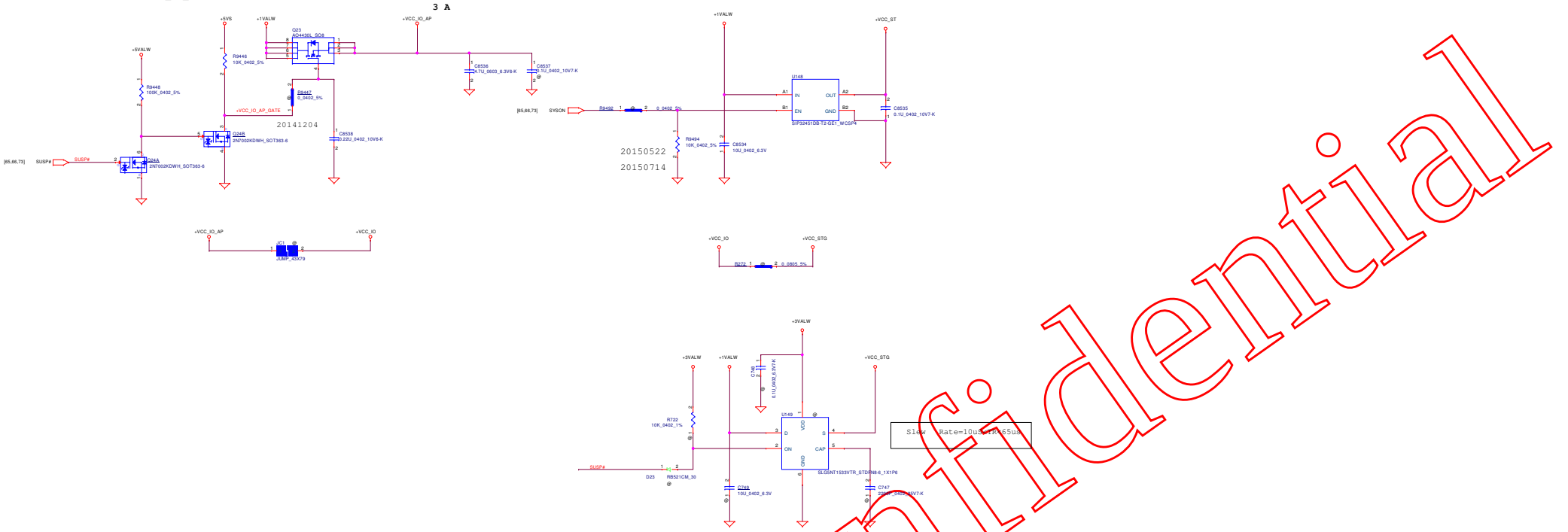
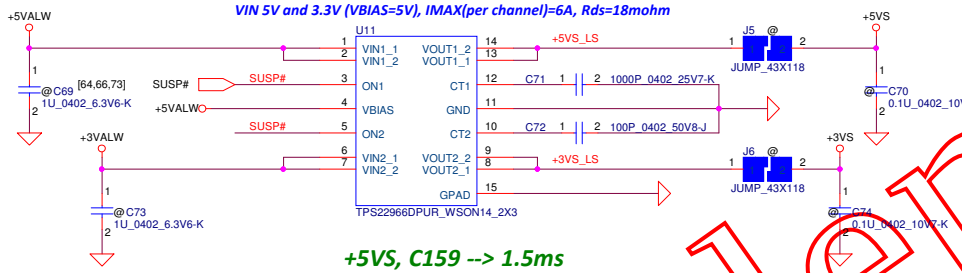
+1VALW to +VCC_IO_AP



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

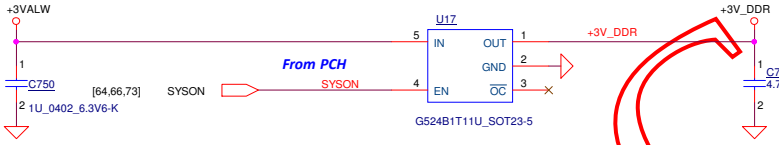
Title	XXXX		
Size D	Document Number	BM460_NM-A551	Rev 1.0
Date: Wednesday, August 06, 2014	Sheet 64 of 83		

Load Switch
+5VALW To +5VS
+3VALW To +3VS

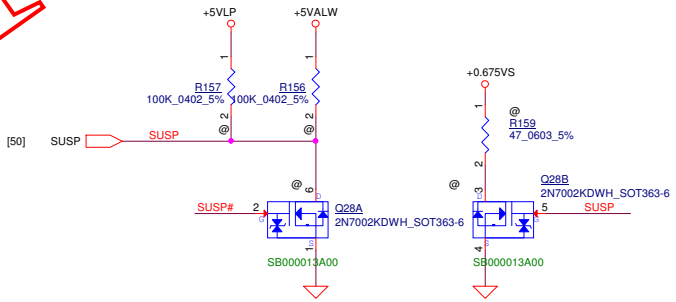


+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms

+3VALW to +3V_DDR

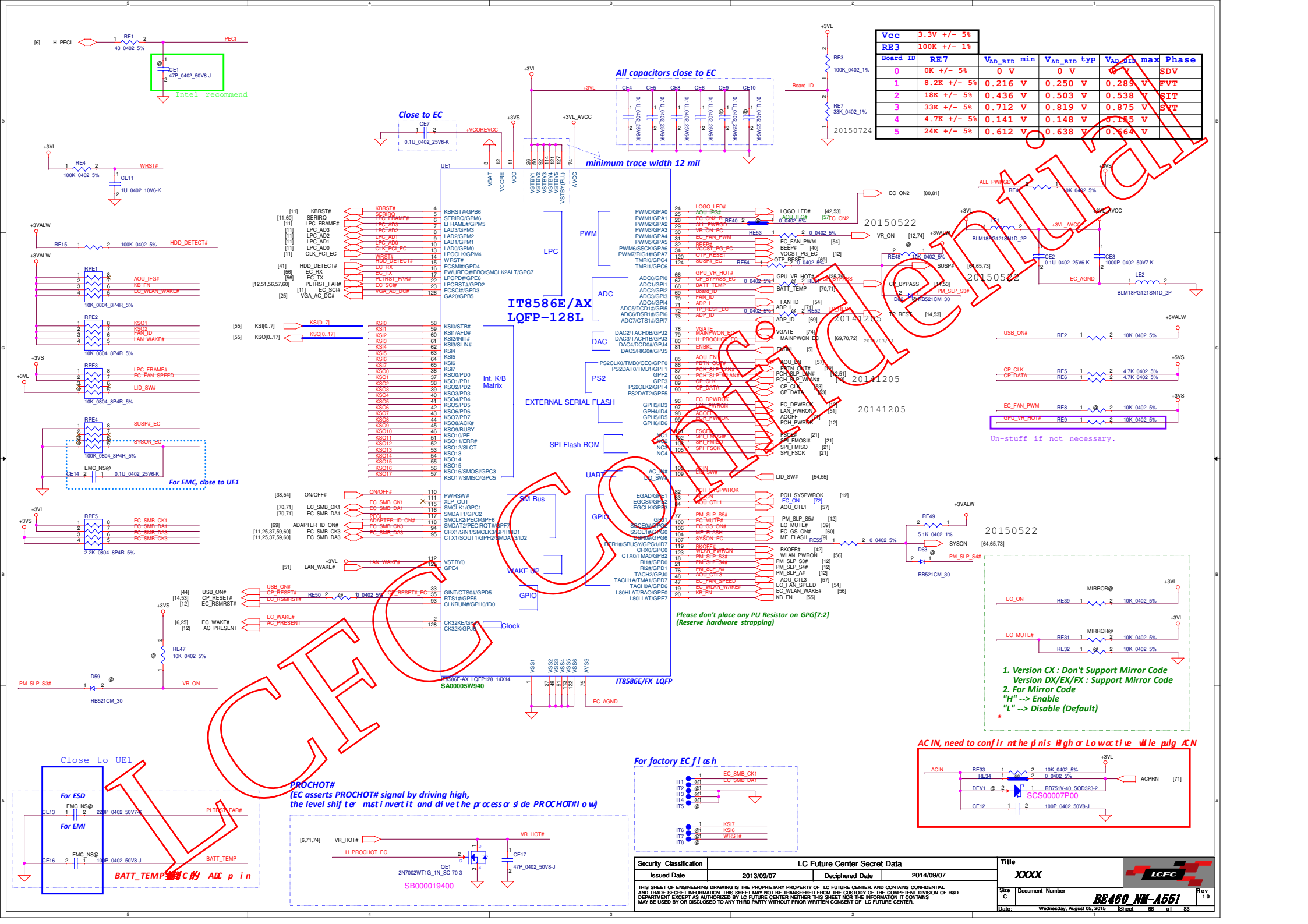


SUSP# to SUSP



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title	DC V TO VS/ V-PCH/VM		
Size: Custom	Document Number: BE460_NM-A551		Rev: 1.0
Date: Wednesday, August 05, 2015	Sheet 65 of 83		


Vcc 3.3V +/- 5%
RE3 100K +/- 1%
Board ID | RE7 | VAD_BID min | VAD_BID typ | VAD_BID max | Phase
0 | 0K +/- 5% | 0 V | 0 V | 0.2 V | SDV
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | FVT
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | SIT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | SVT
4 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V |
5 | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V |
20150724
All capacitors close to EC
Close to EC
minimum trace width 12 mil
IT8586E/AX
LQFP-128L
IT8586E-AX_LQFP128_14X14
SA00005W940
IT8586E/FX LQFP
PWM
ADC
DAC
PS2
LPC
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
Int. K/B Matrix
Please don't place any PU Resistor on GPG[7:2]
(Reserve hardware strapping)
For EMC, close to UE1
Un-stuff if not necessary.
1. Version CX : Don't Support Mirror Code
Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
*
ACIN, need to confirm the pin is High or Low active while pulg ACIN
PROCHOT#
(EC asserts PROCHOT# signal by driving high,
the level shifter must invert it and drive the processor side PROCHOT# low)
For factory EC flash
Close to UE1
For ESD
For EMI
BATT_TEMP
SB000019400
20150522
20141205
LCFC Confidential
Security Classification | LC Future Center Secret Data
Issued Date | 2013/09/07 | Deciphered Date | 2014/09/07
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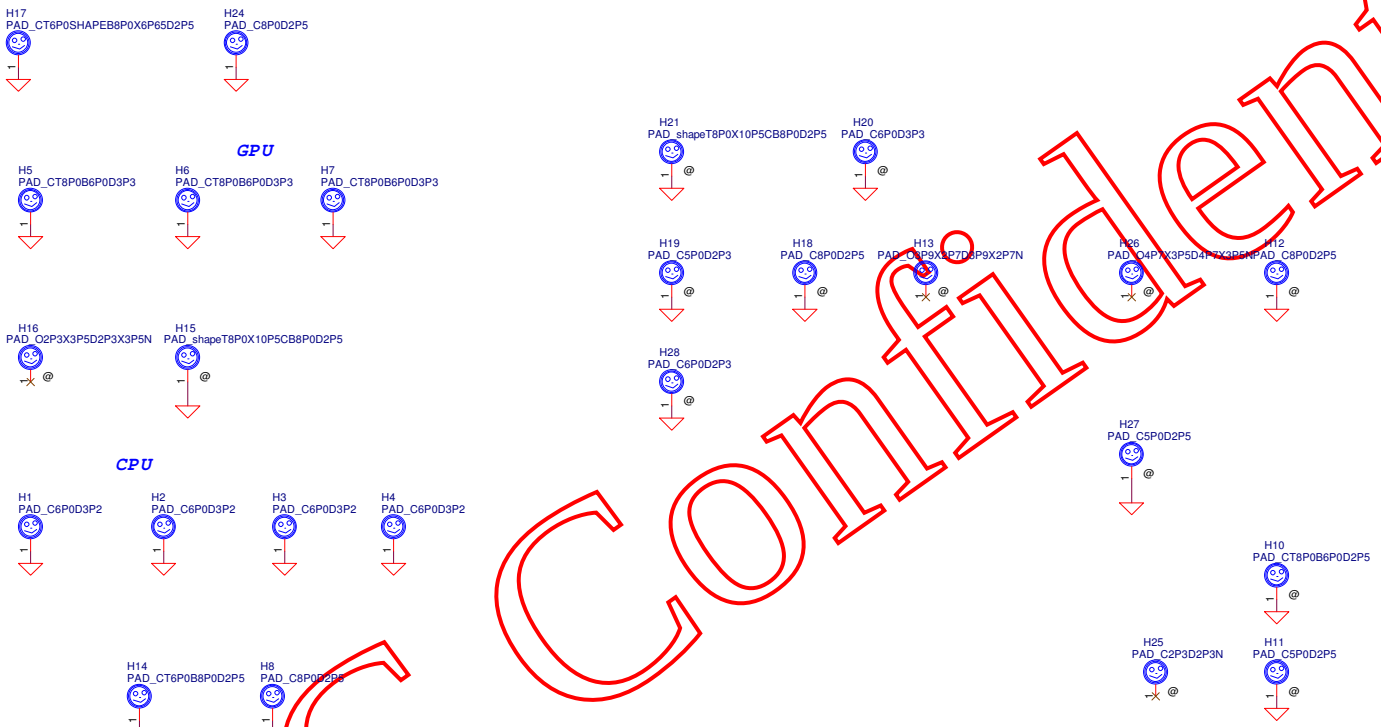
Title XXXX
Size C | Document Number BR460_MM-A551 | Rev 1.0
Date: Wednesday, August 05, 2015 | Sheet 66 of 83

Screw Hole



PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: PLM/SCREW HOLE

Size	Document Number	Rev
Custom	BE460_NM-A551	1.0

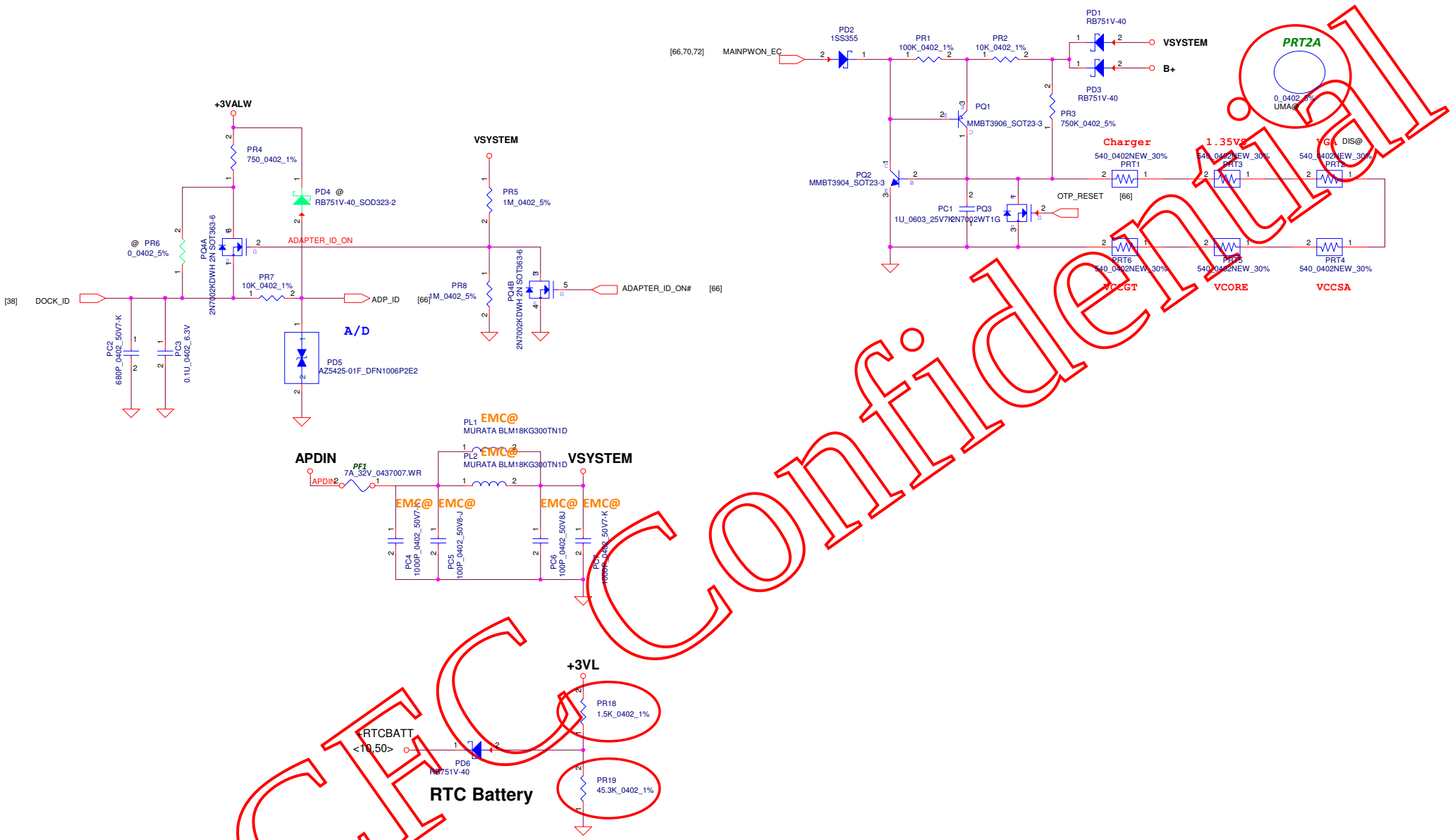
Date: Wednesday, August 05, 2015 Sheet 67 of 83

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: XXXX

Size	Document Number	Rev
C	BR460_NM-A551	1.0

Date: Wednesday, August 05, 2015 | Sheet 68 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: DCIN / Vin Detector

Size	Document Number	Rev
Custom	AIVL2_NM-A351	1.0

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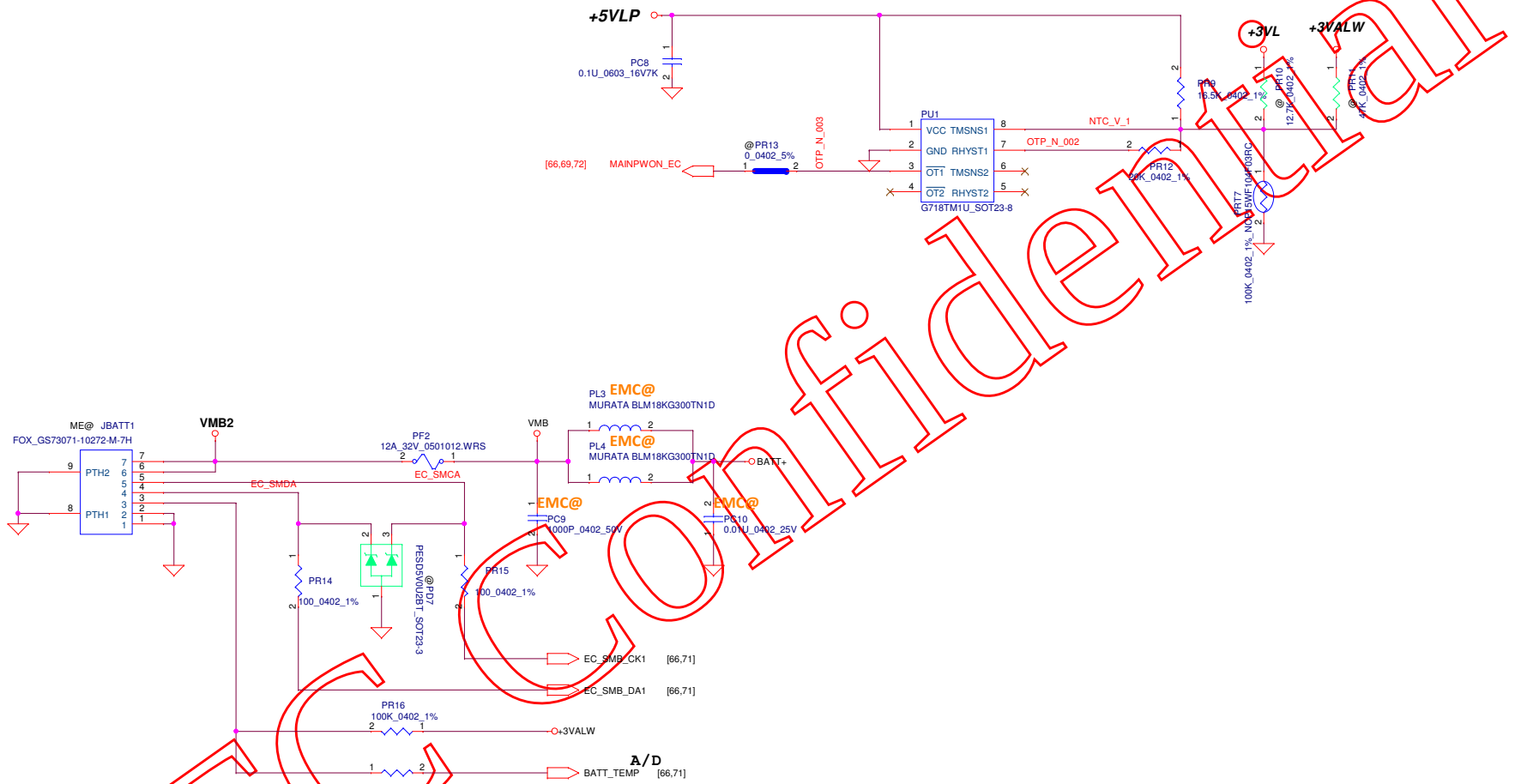
PRT7 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: BATTERY CONN/OTP

Size	Document Number	Rev
Custom	AIVL2_NM-A351	1.0

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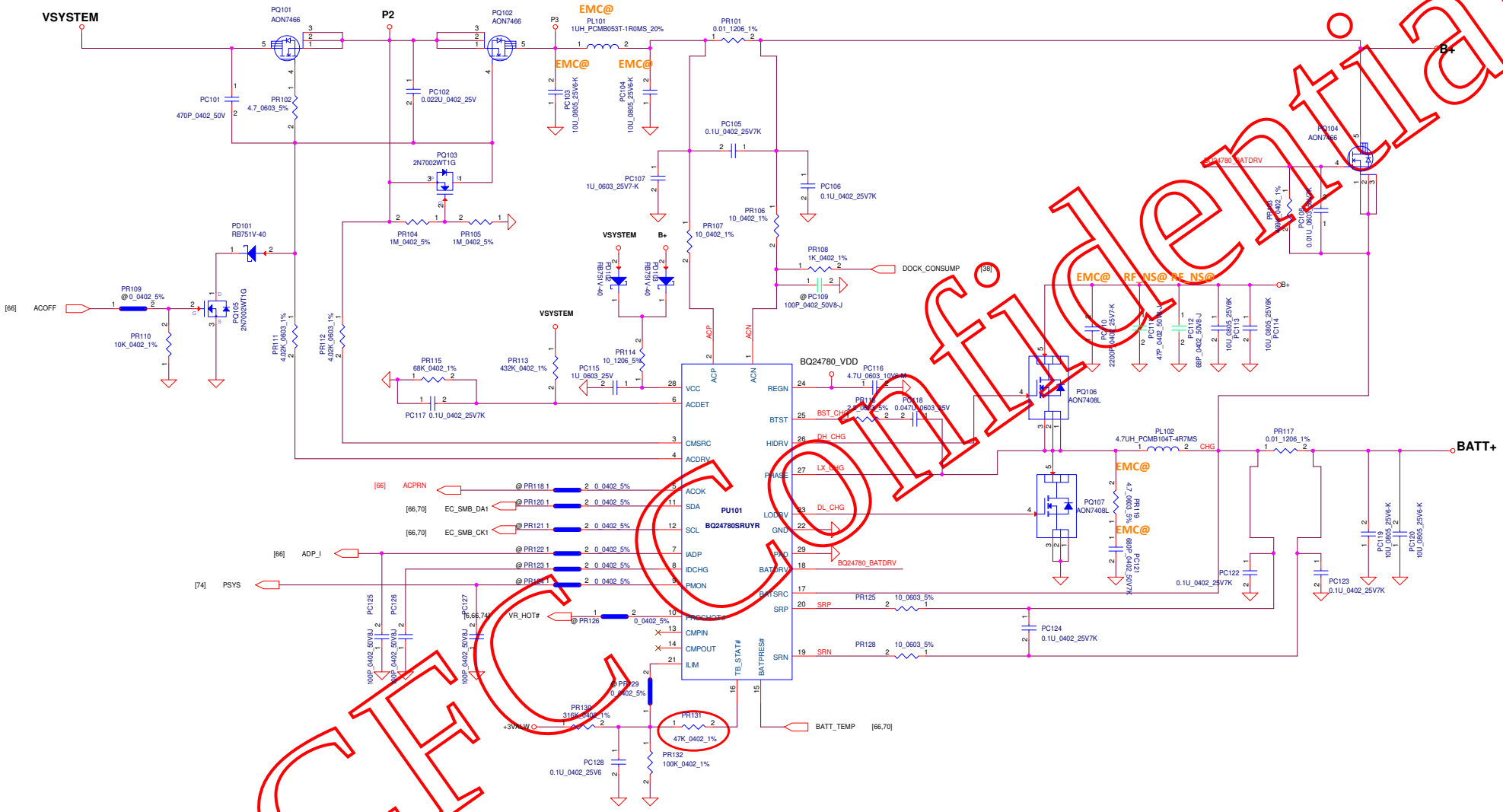
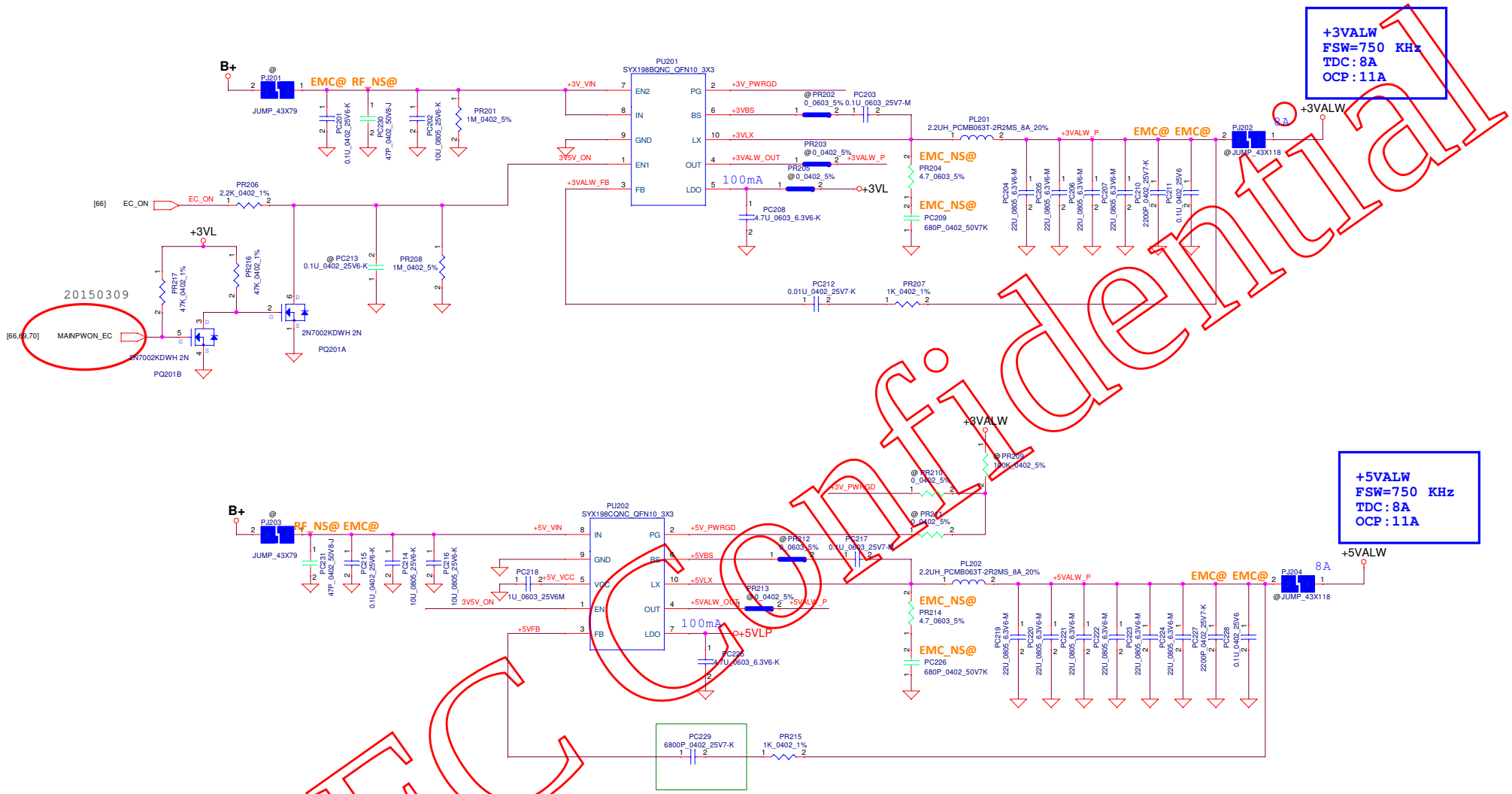


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	CHARGER		
Size	Document Number		Rev
C	AIVL2_NM-A351		1.0
Date:	Wednesday, August 05, 2015	Sheet	71 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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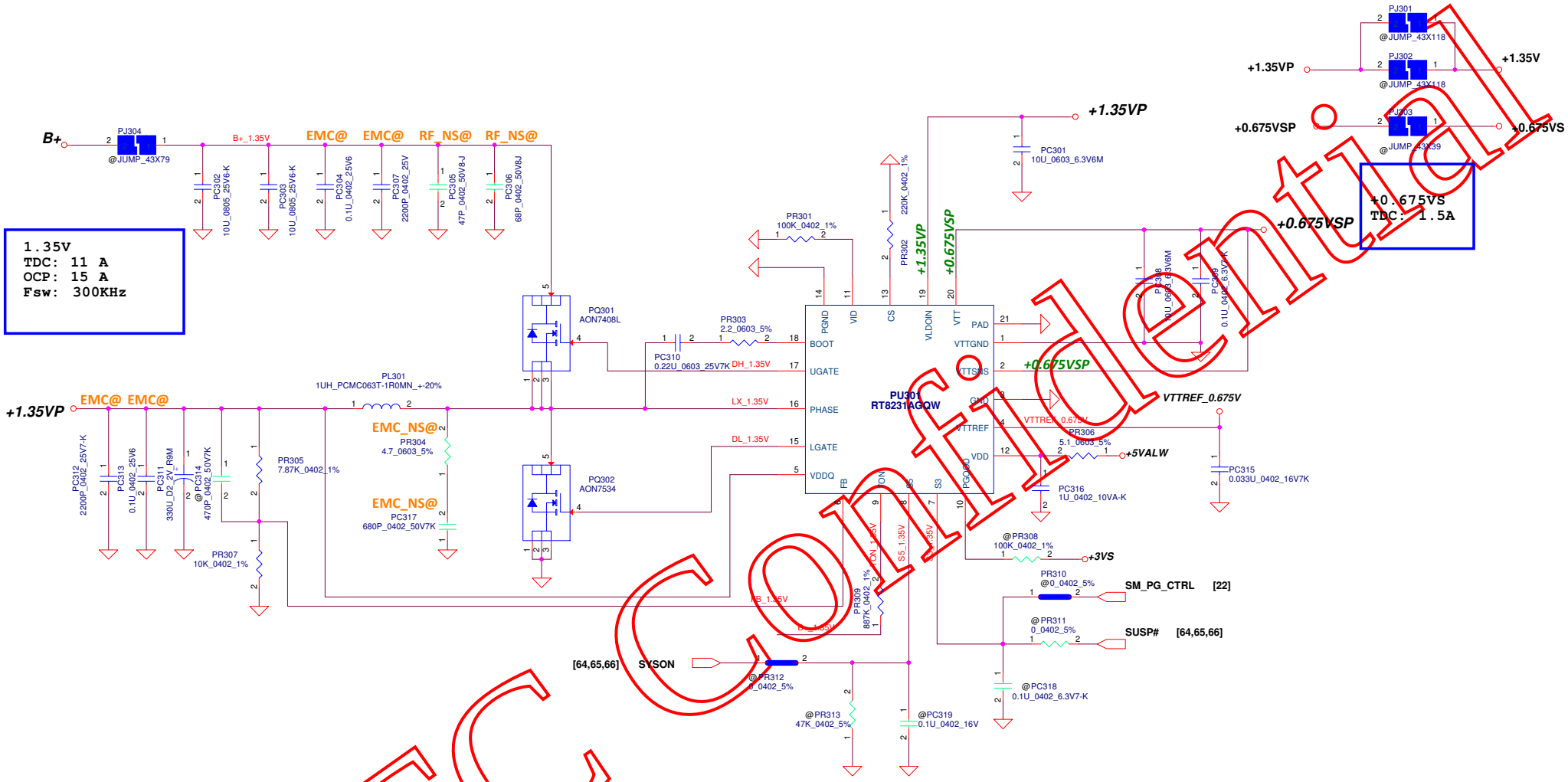
Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	AIVL2_MB-A351	1.0

Date: Wednesday, August 05, 2015 Sheet 72 of 83

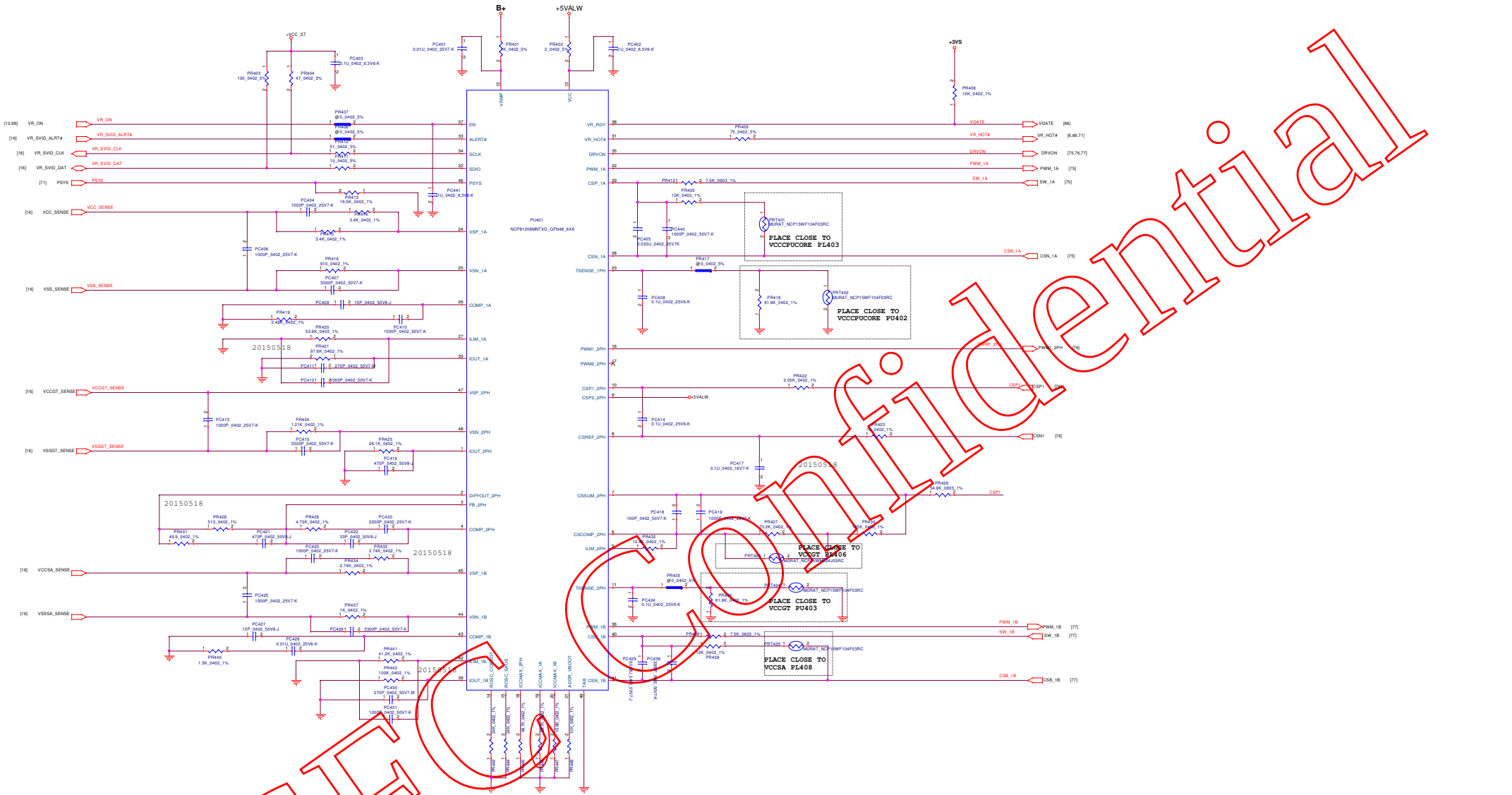


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.35V/+0.675VS

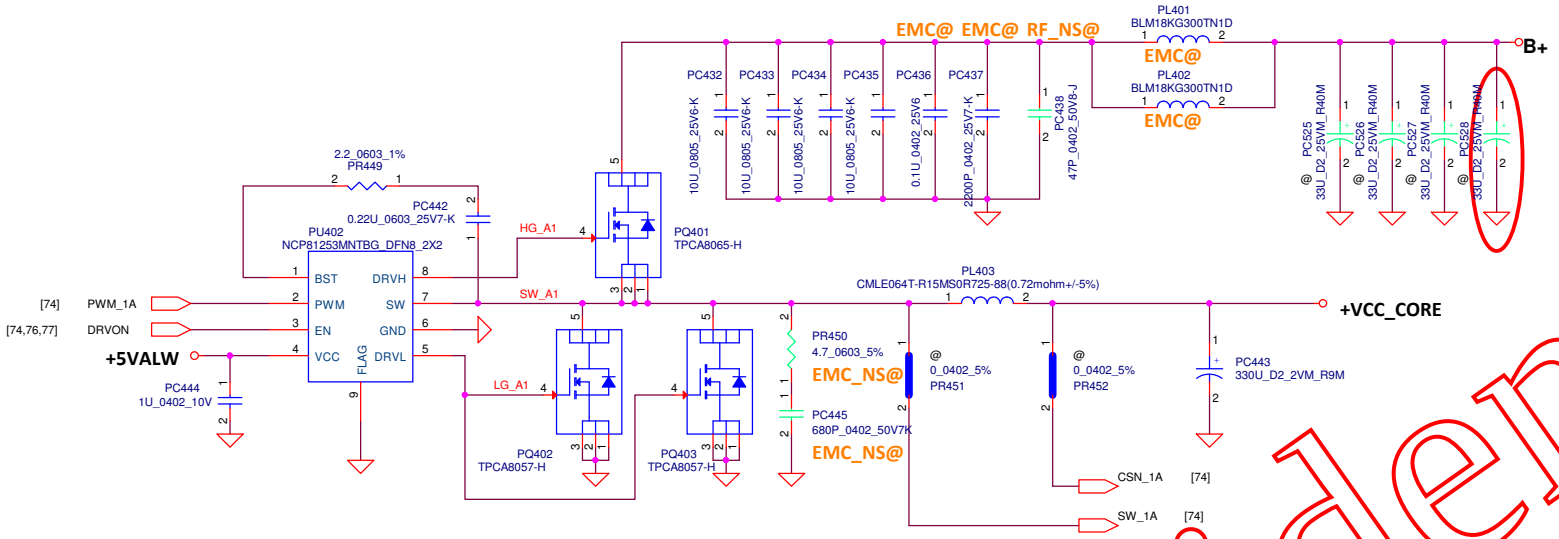
Size: Custom | Document Number: AIVL2_MM-A351 | Rev: 1.0

Date: Wednesday, August 05, 2015 | Sheet 73 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	IMVP8		
Size	Document Number		Rev
D	AIV8_NM-A351		1.0
Date:	Wednesday, August 06, 2014	Sheet	74 of 83

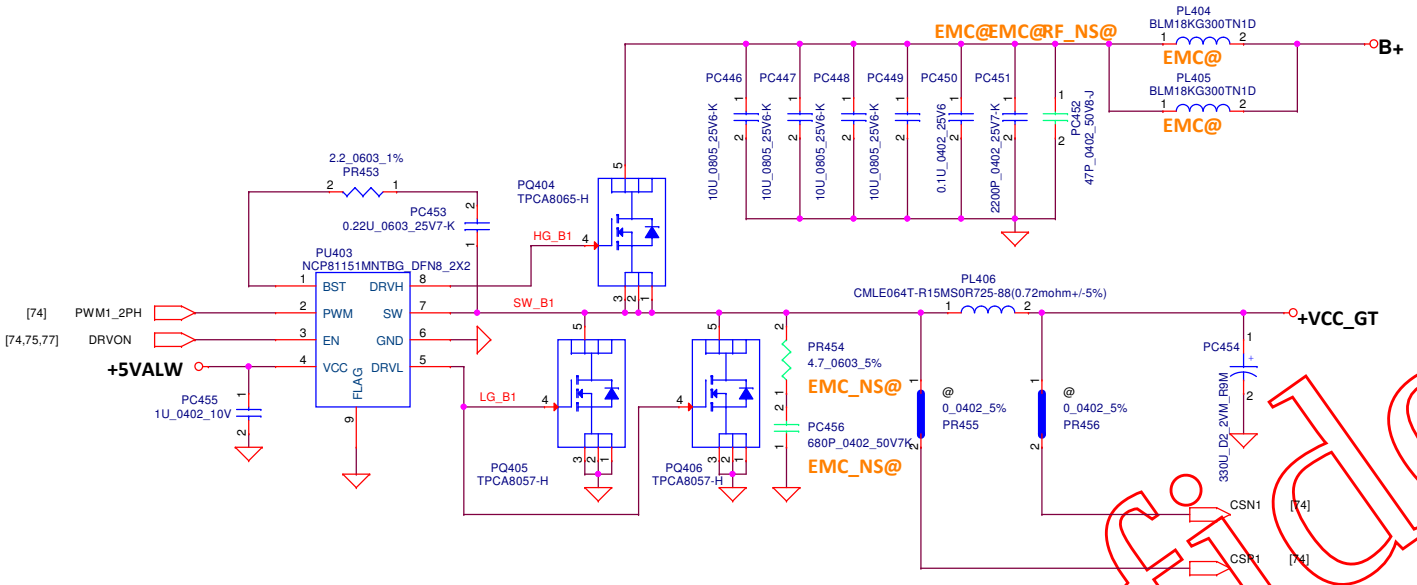


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_CORE

Size	Document Number	Rev
Custom	AIVL2_NM-A351	1.0

Date: Wednesday, August 05, 2015 Sheet 75 of 83

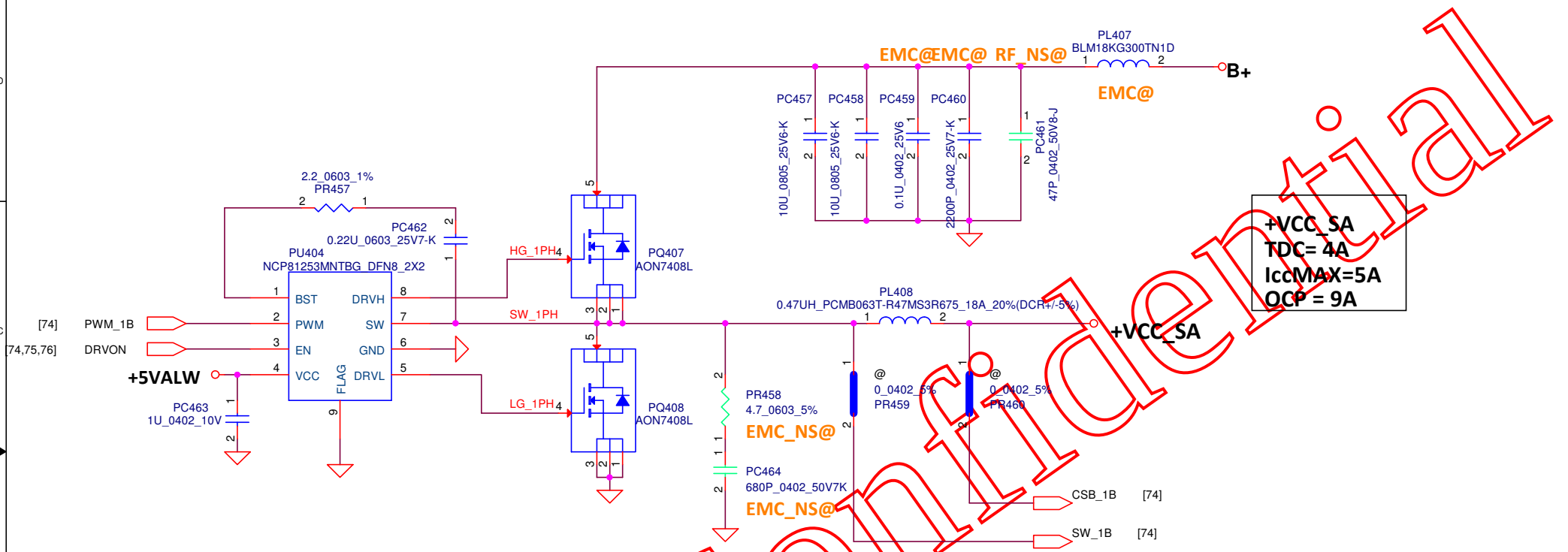


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_GT

Size	Document Number	Rev
Custom	AIVL2_NM-A351	1.0

Date: Wednesday, August 05, 2015 Sheet 76 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: VCCSA

Size	Document Number	Rev
Custom	AIVL2_NM-A351	1.0

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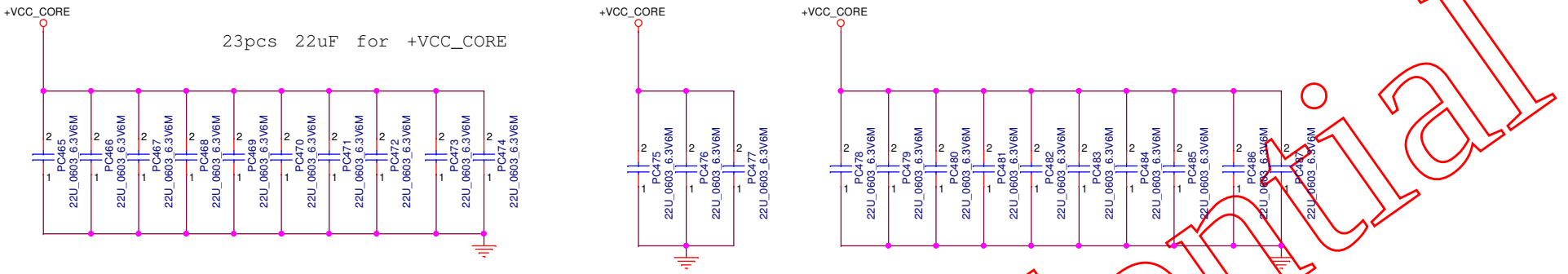
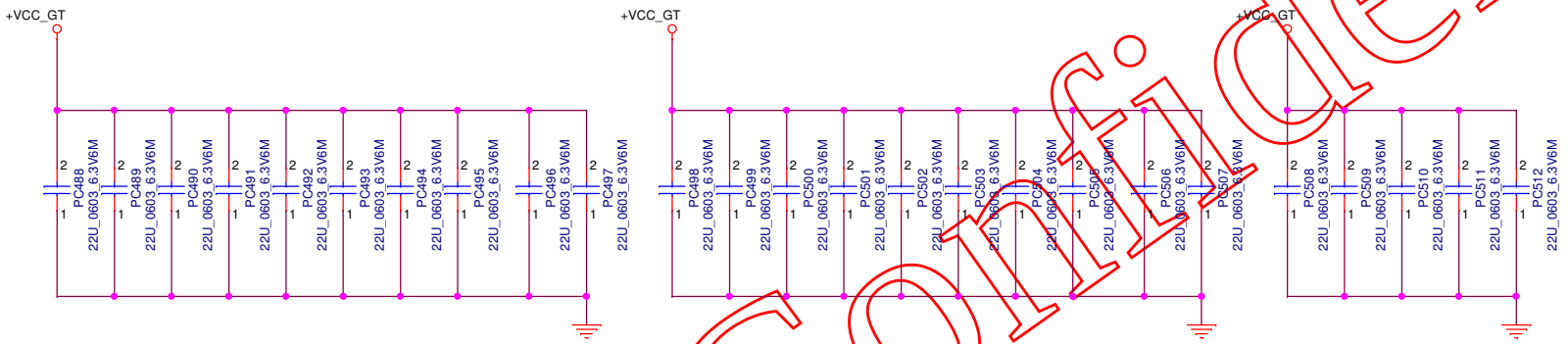
Based on PDDG rev 0.7 Table 5-1.

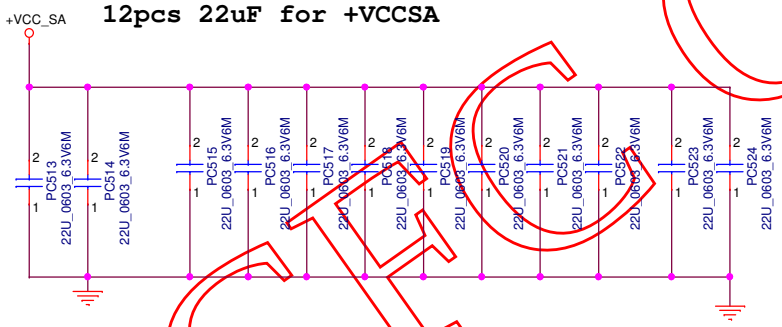
23pcs 22uF for +VCC_CORE



25pcs 22uF for +VCC_GT



12pcs 22uF for +VCCSA

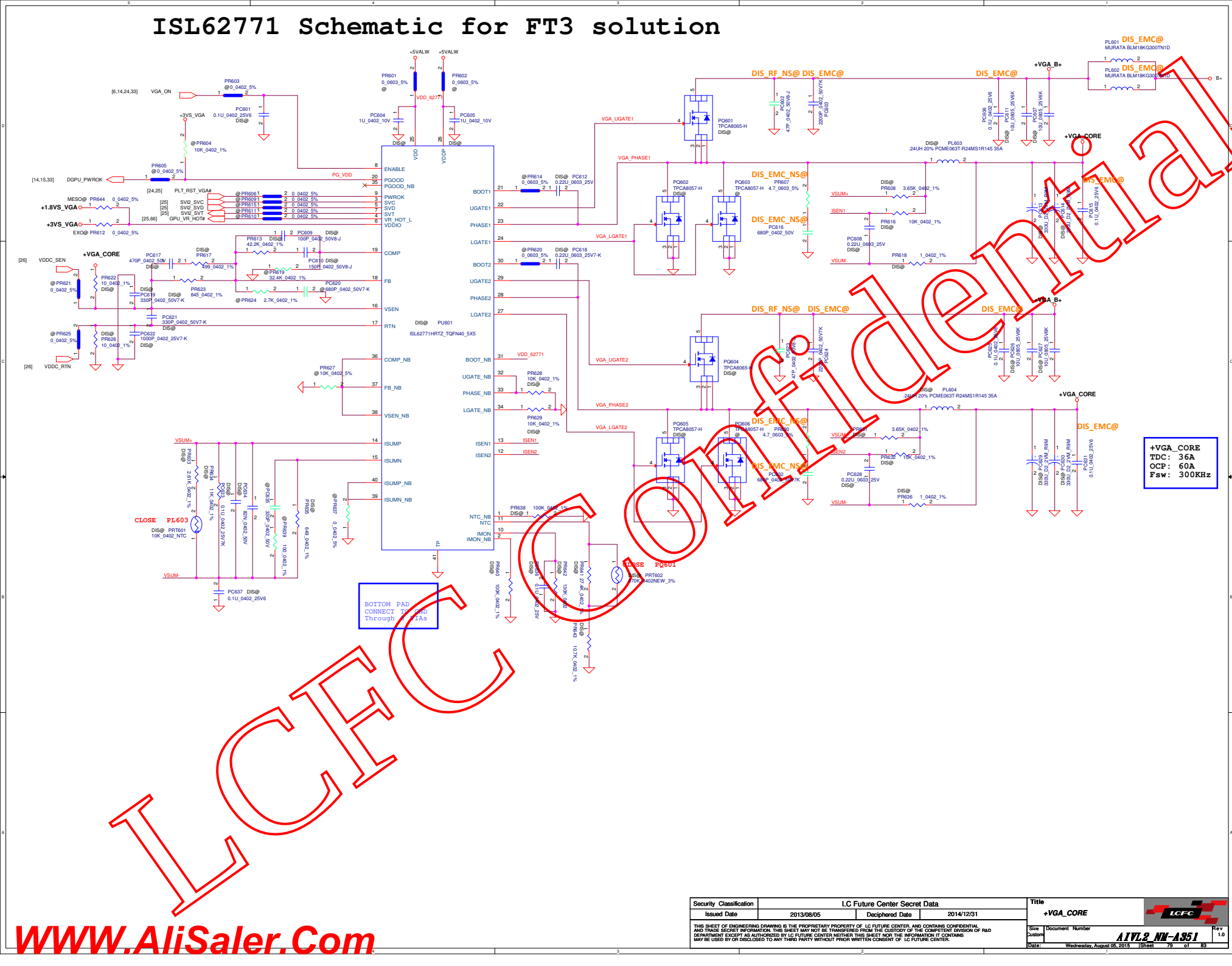


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

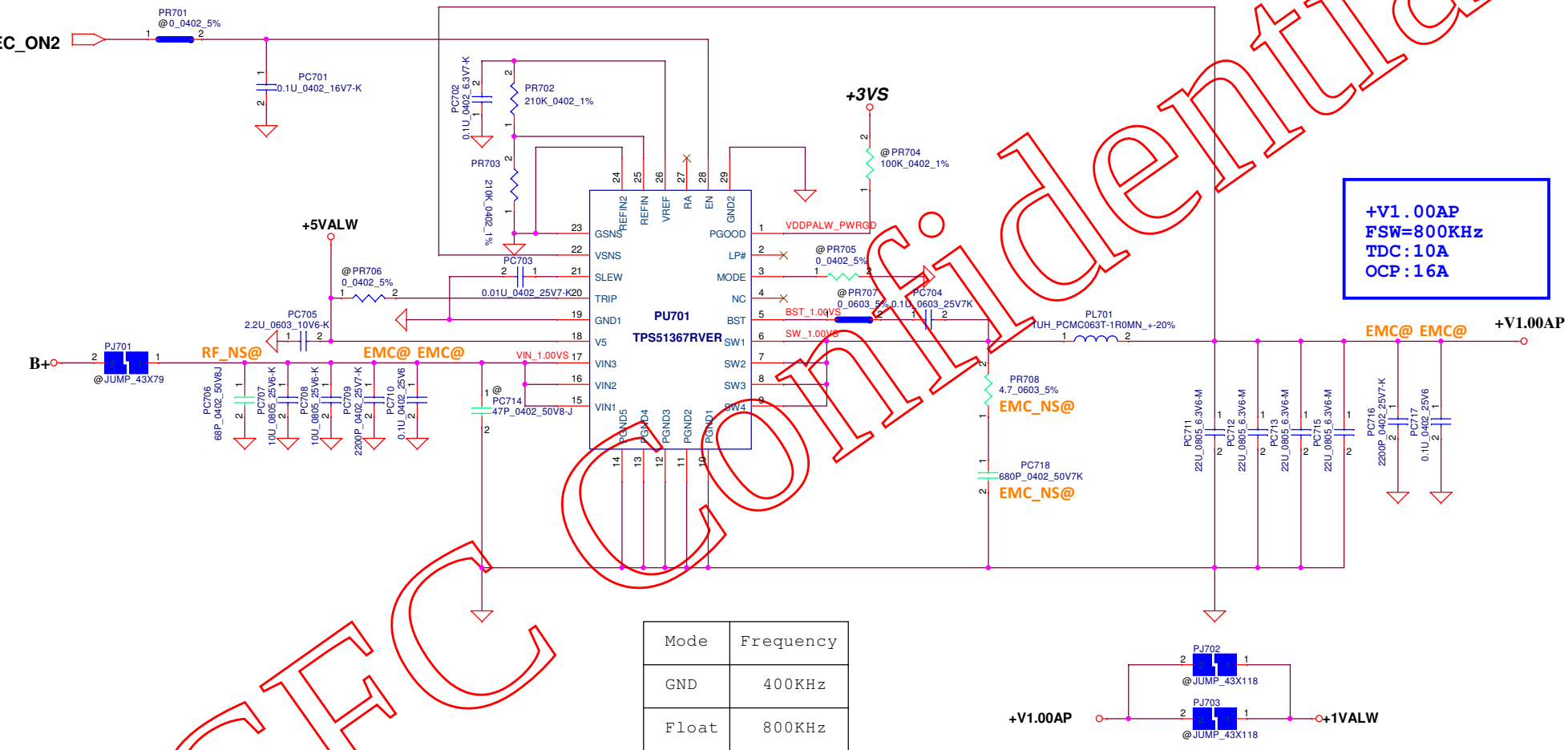
Size: B	Document Number: AIVL2_NM-A351	Rev: 1.0
Date: Wednesday, August 05, 2015	Sheet 78 of 83	

ISL62771 Schematic for FT3 solution



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

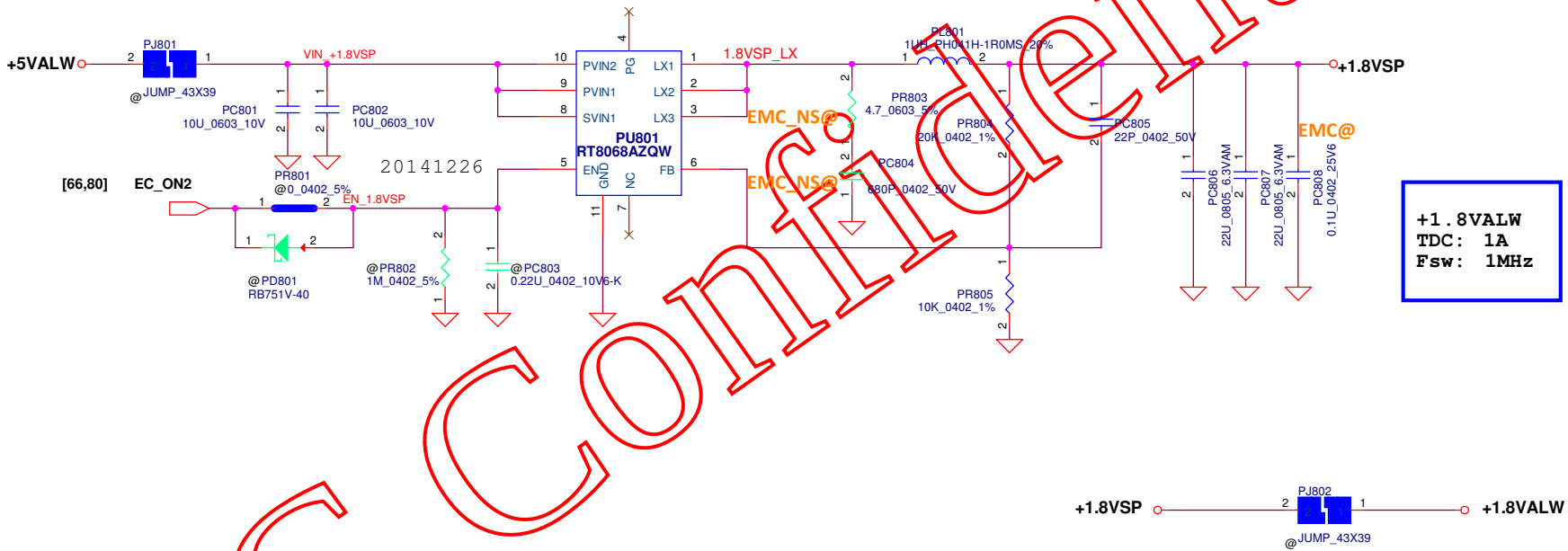
Title	+VGA_CORE		
Size: Custom	Document Number: AIVL2_MB-A351		Rev: 1.0
Date: Wednesday, August 05, 2015	Sheet 79 of 83		



Mode	Frequency
GND	400KHz
Float	800KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/08/01

Title	+V1.00A		
Size	Document Number		Rev
Custom	AIVL2_NM-A351		1.0
Date:	Wednesday, August 05, 2015	Sheet	80 of 83



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.8VS_VGA		
Size	Document Number		Rev
B	AIVE1_NM-A211		1.0
Date:	Wednesday, August 05, 2015	Sheet	81 of 83

HW PIR (Product Improve Record)

AIVE1 NM-AXXX SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1
GERBER-OUT DATE: 2013/10/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: XXXX

Size	Document Number	Rev
C	AITE1_NM-A221	1.0

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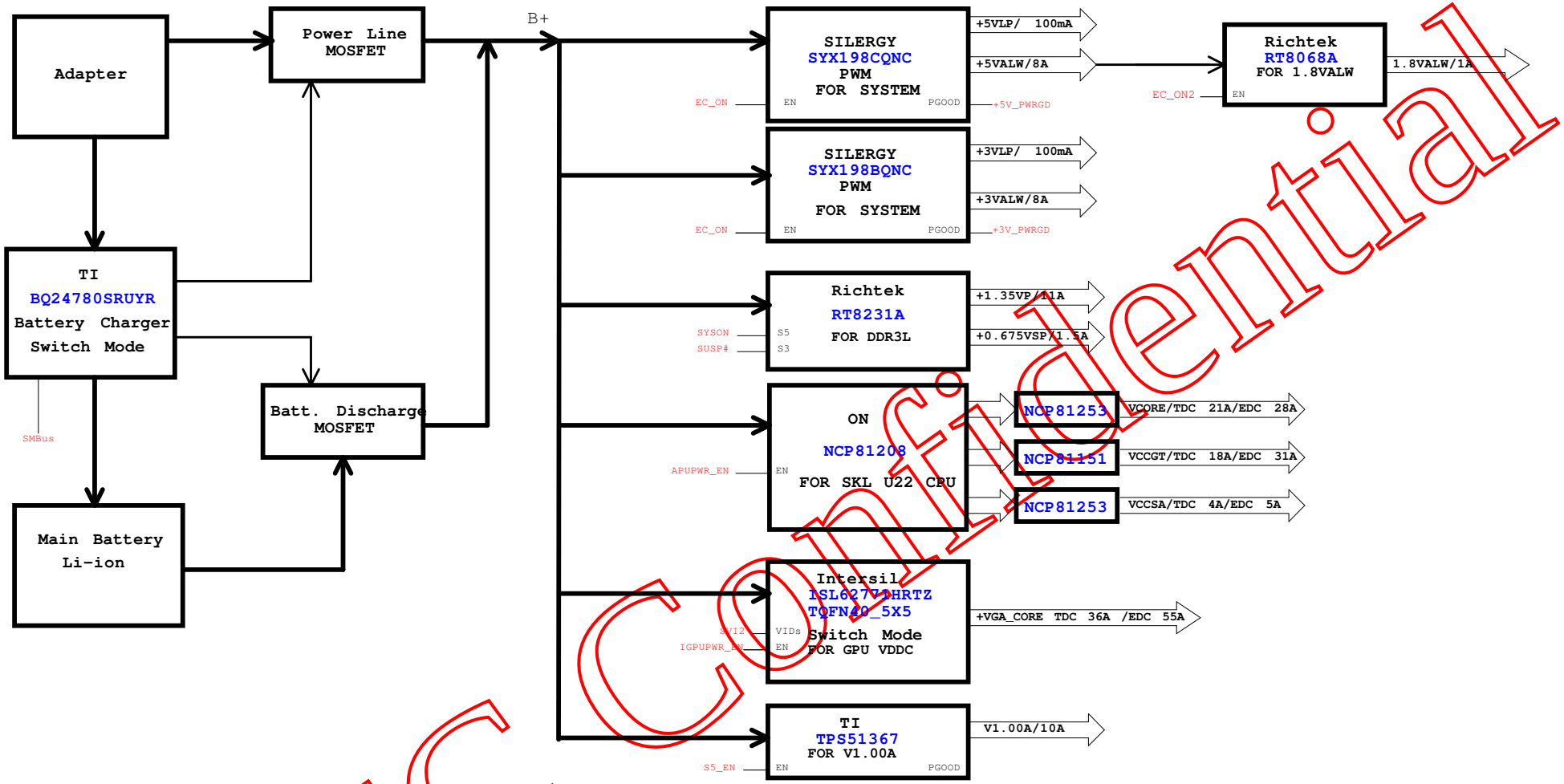

Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title: *Block Diagram*

Size	Document Number	Rev
Custom	AIVL2_NM-A351	1.0

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