LWG2-D Block Diagram
(Discrete)

Project code: 91.4Q801.001
PCB P/N : 55.4Q801.XXX
REVISION : 06210-2
(Hannstar, ACCL)

CLK GEN.
IDT CV125PA 3

Mobile CPU
Yonah 478
1.83G/2G/2.16G 4, 5

G792 19

HOST BUS 400/533/667MHz

DDR2 533 MHz 11,12
DDR2 533 MHz 11,12
533/667MHz
533/667MHz

Calistoga
Ver.:A3 :71.945PM.A0U / QK58
KI.94501.006 / SL8Z4
6,7,8,9,10

PCI Express x16
M56 Ver.: B24
M52 Ver.: A12
M54 Ver.: A12

ATI
M54P / M52P
42,43,44,45

VRAM x4
128/256M 47,48

TVO 14
LVDS
14"WSXGA LCD 13
RGB CRT
CRT 14

DMI I/F 100MHz

ICH7M
Ver. : B0, 71.ICH7M.A0U / QK65
KI.80101.017 / SL8YB
15,16,17,18

Codec
ALC883 28
AZALIA
29 MIC In
INT.MIC
29 INT.SPKR
Line Out 29

OP AMP G1432 29
OP AMP MAX4411 29

RJ11
MODEM MDC Card 21

PCI BUS

TI
PCI 7412
CARDBUS
1394
CardReader
24,25

PCMCIA I/F
PWR SW
TSP2220A 27
PCMCIA SLOT
Support TypeII 27

1394 CONN 26
MS/MMC/SD
3 in 1 26
Mini-PCI
802.11A/B/G 30

PCIEx1
Giga LAN
BCM5789/5787M 22
TXFM 23
RJ45 23
Mini Card*1
802.11A/B/G 26

BCM5787MKFBG-A1
BCM5789KFBG-C1
BCM4401EKFBG-B0

SPI I/F
BIOS
SST25LF080A 34

LPC BUS
KBC
Renesas
RE144B 30
LPC
DEBUG
CONN. 32
Touch Pad 31
INT. KB 31

USB
SATA
PATA

USB
3 PORT 21

Finger Print 20
HDD 20
CDROM 20
MINI USB 21
Blue-tooth

PCB STACKUP

TOP	
GND	
S	
S	
VCC	
S	
GND	
BOTTOM	

SYSTEM DC/DC
TPS51120 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
TPS51124 38

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 40

1D8V_S3	DDR_VREF_S0

APL5332KAC 40

3D3V_S0	2D5V_S0

APL5912-U 40

1D8V_S3	1D5V_S0

MAXIM CHARGER
MAX8725 39

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262 35, 36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 44A

ATI M54 DC/DC
FAN5234 49

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

APL5331KAC 43

1D8V_S0	1D2V_S0

<Variant Name>

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Wednesday, June 21, 2006 | Sheet 1 of 52

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

History

<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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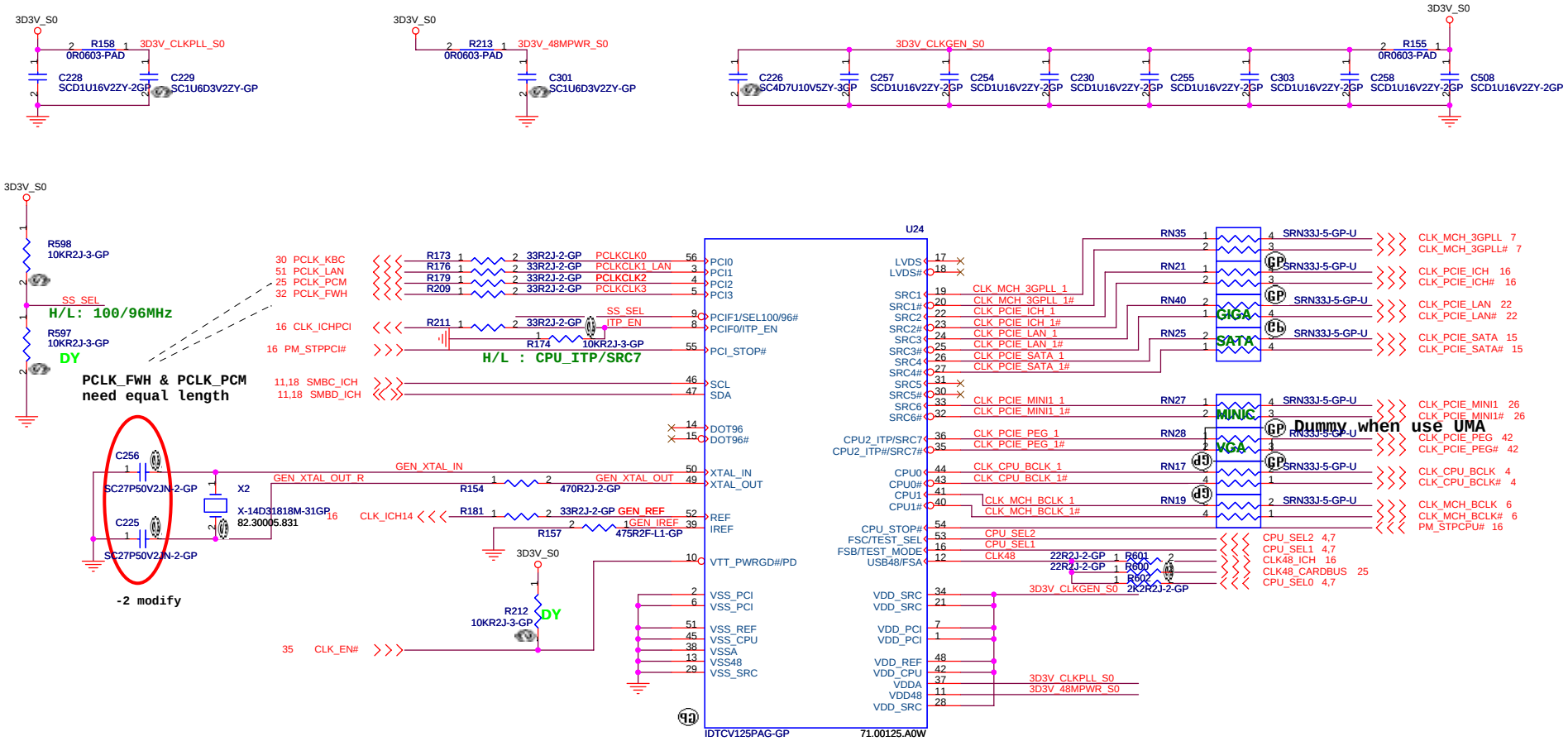
Title: Reference

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 2 of 52



SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

<Variant Name>

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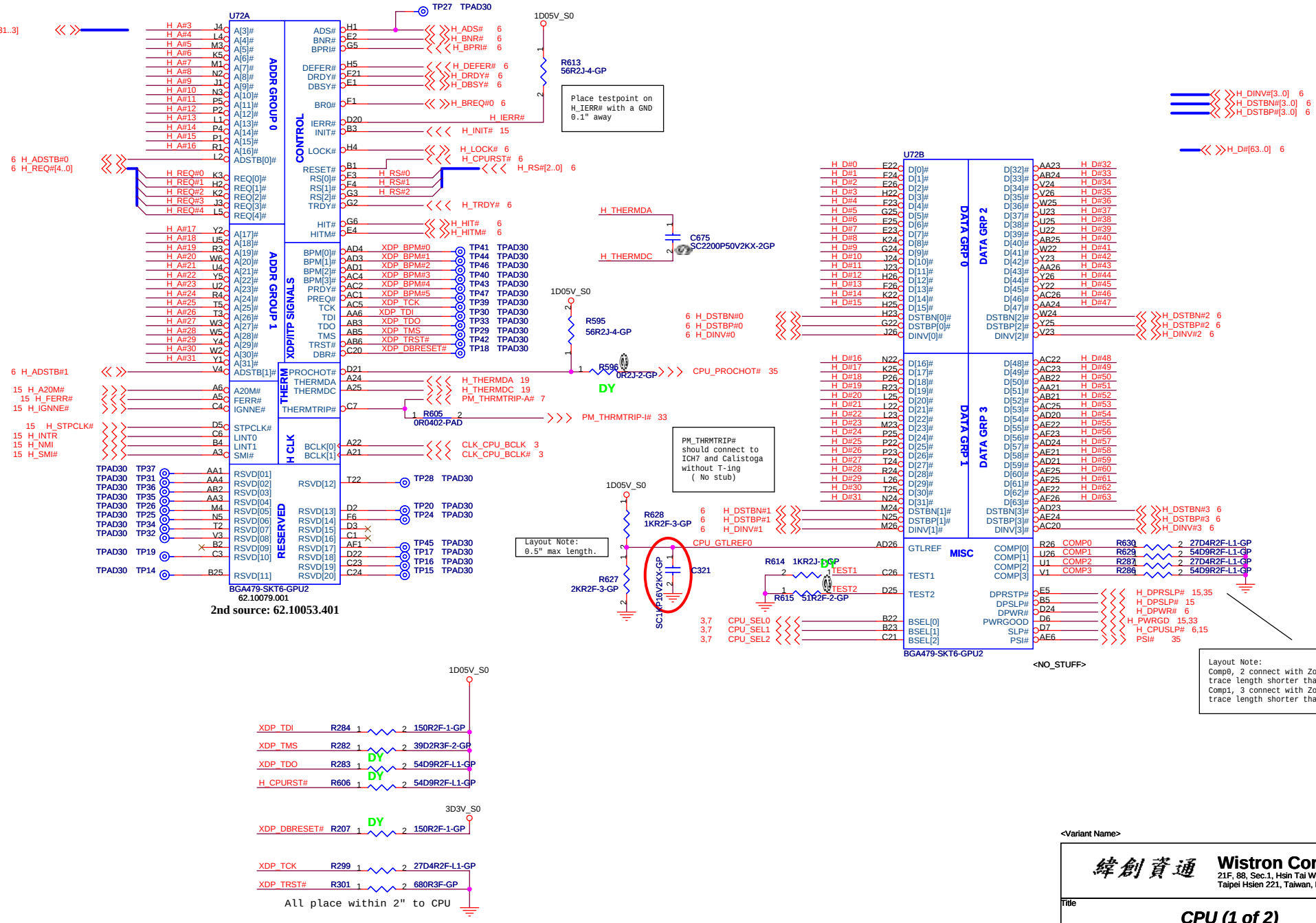
Title: Clock Generator IDT CVT125PAG

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 3 of 52



<Variant Name>

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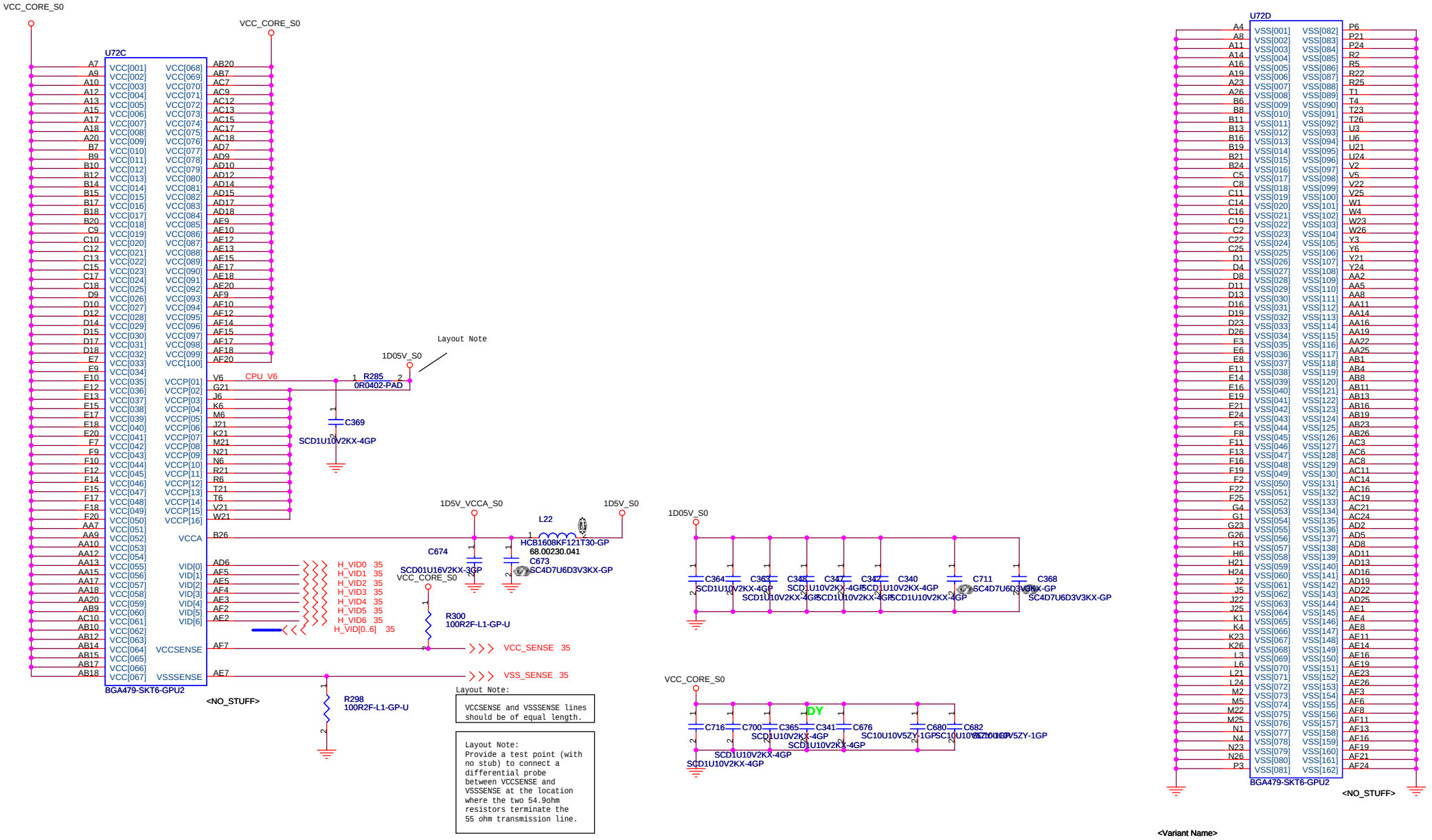
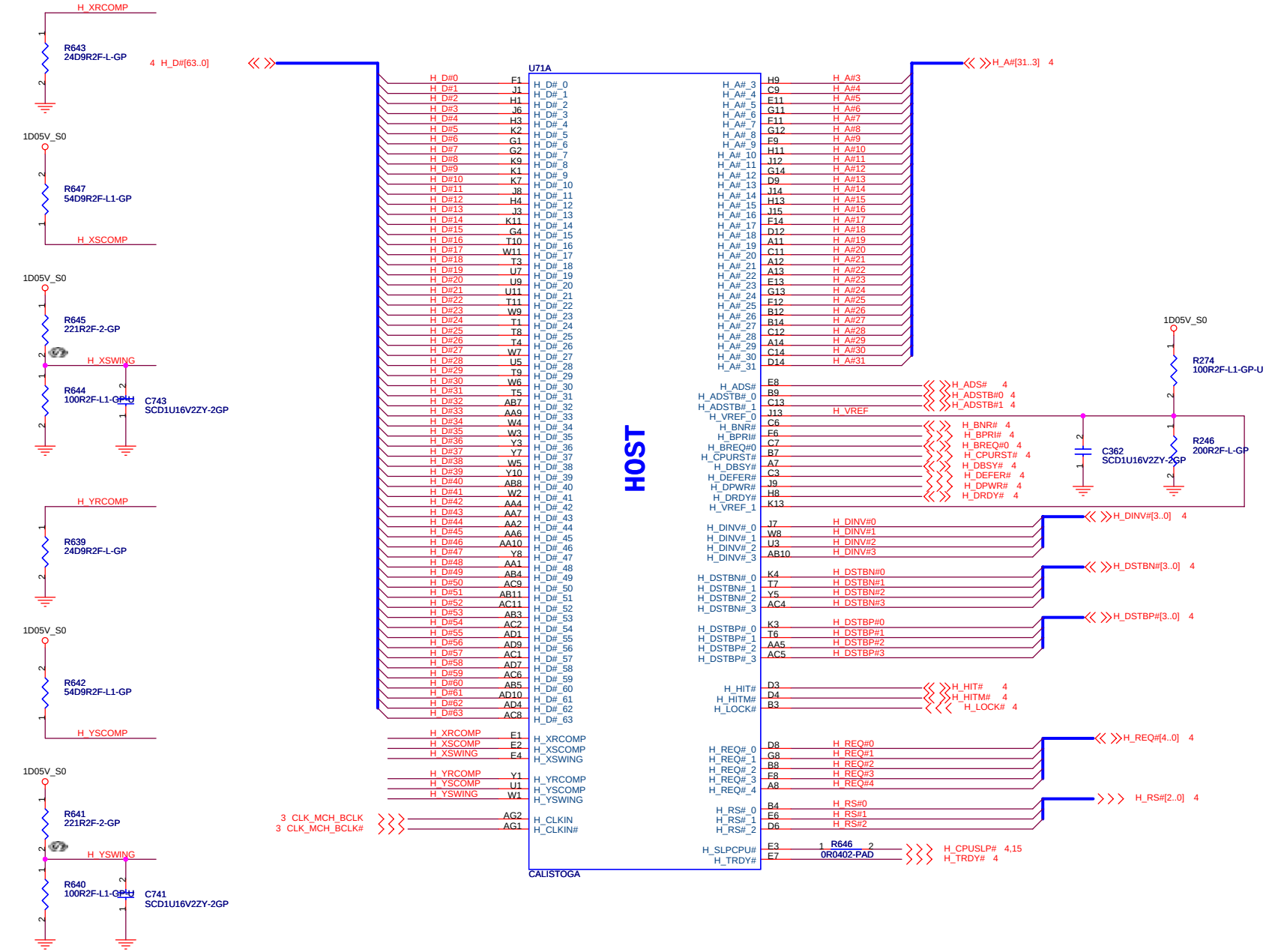
Title: CPU (1 of 2)
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Saturday, June 10, 2006 | Sheet 4 of 52





Place them near to the chip (< 0.5")

<Variant Name>

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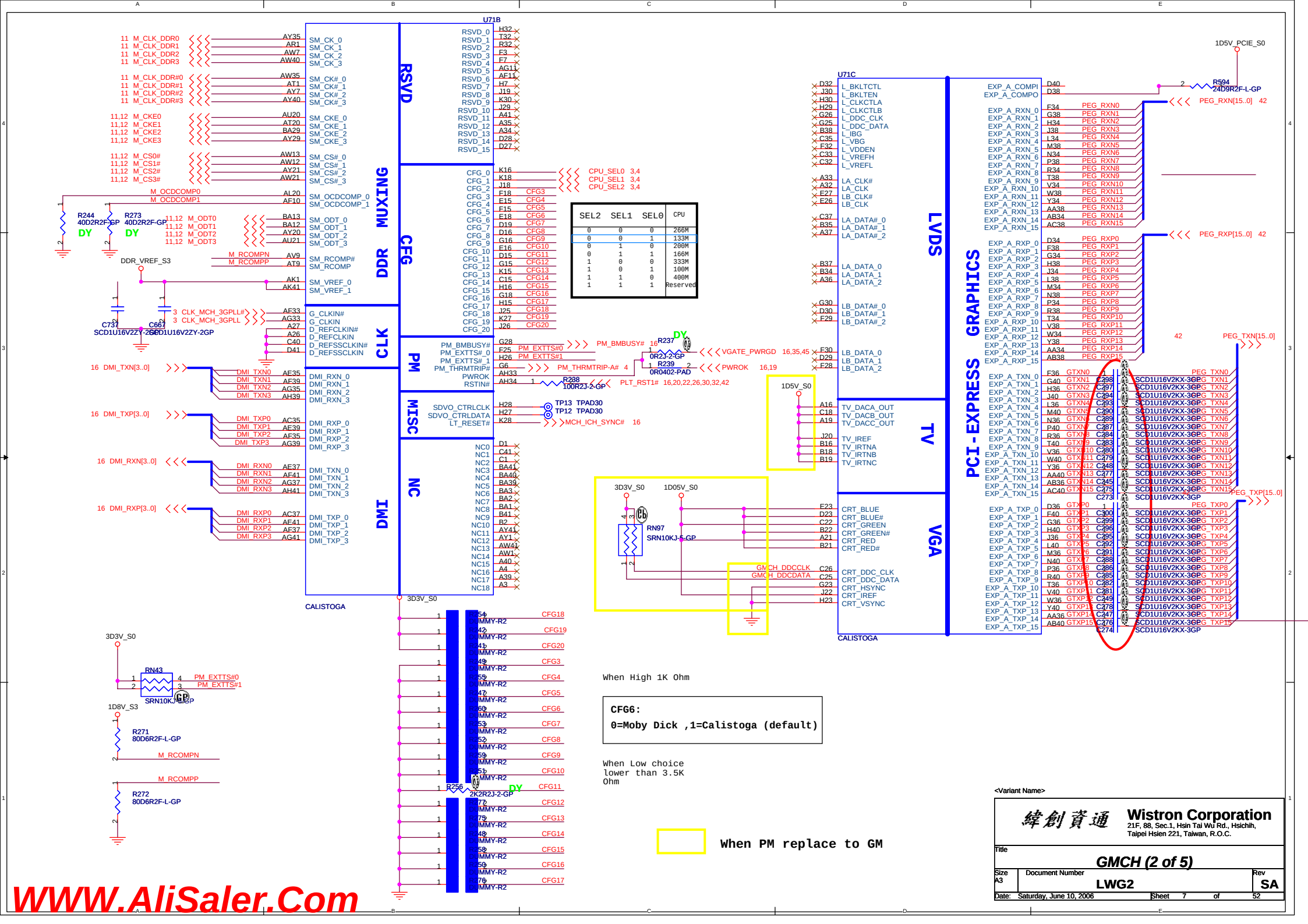
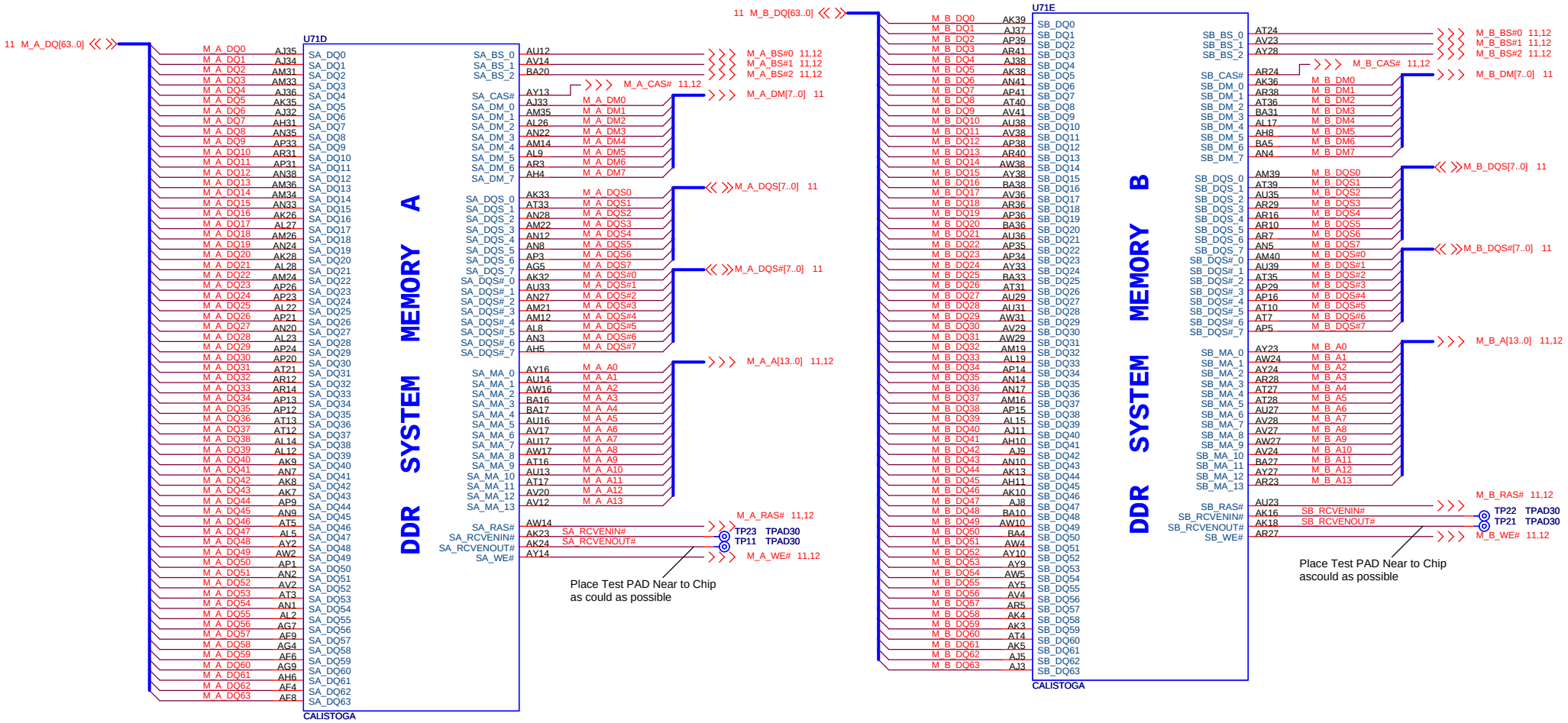
Title: ***GMCH (1 of 5)***

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 6 of 52





<Variant Name>

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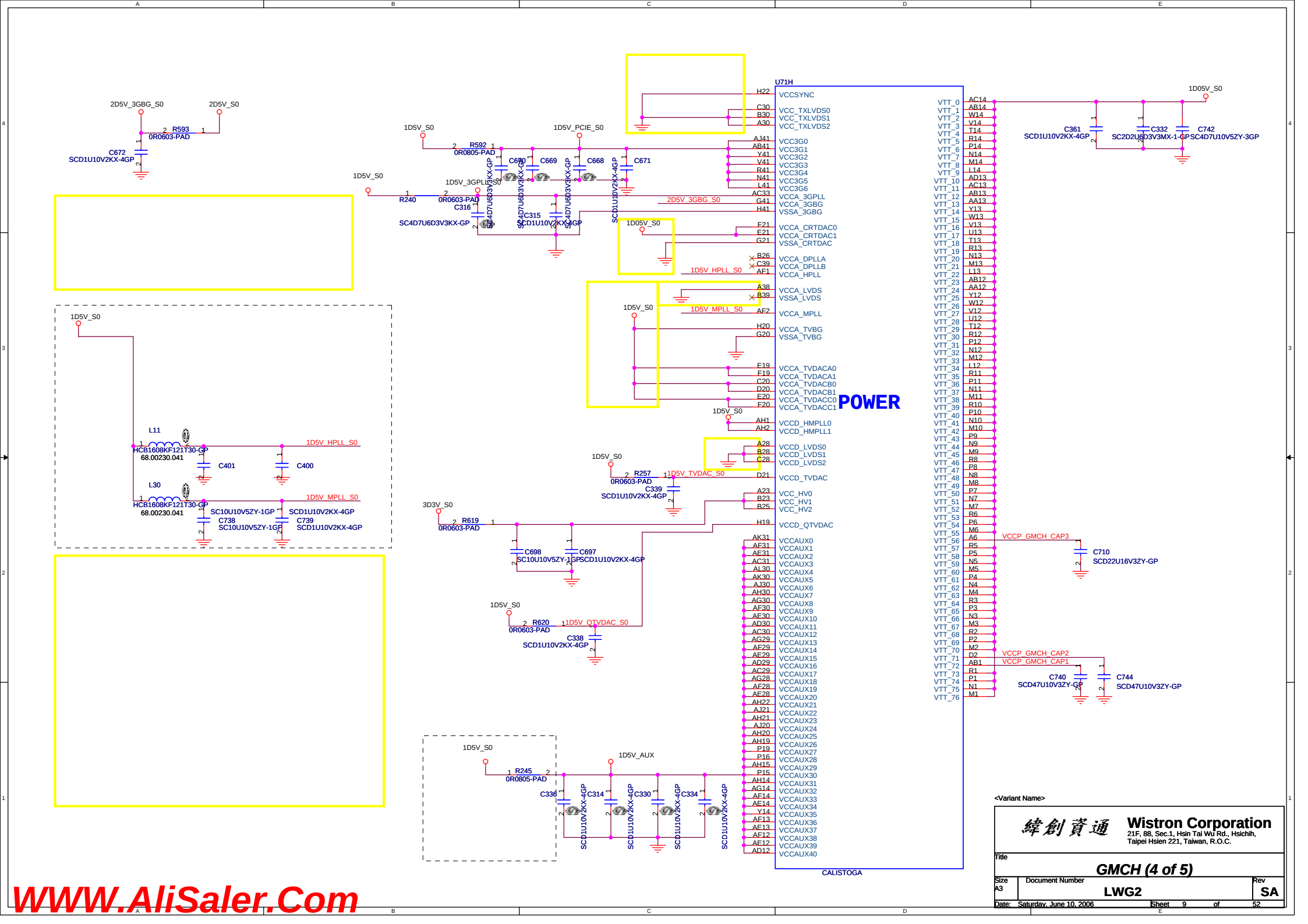
Title: GMCH (3 of 5)

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 8 of 52



<Variant Name>

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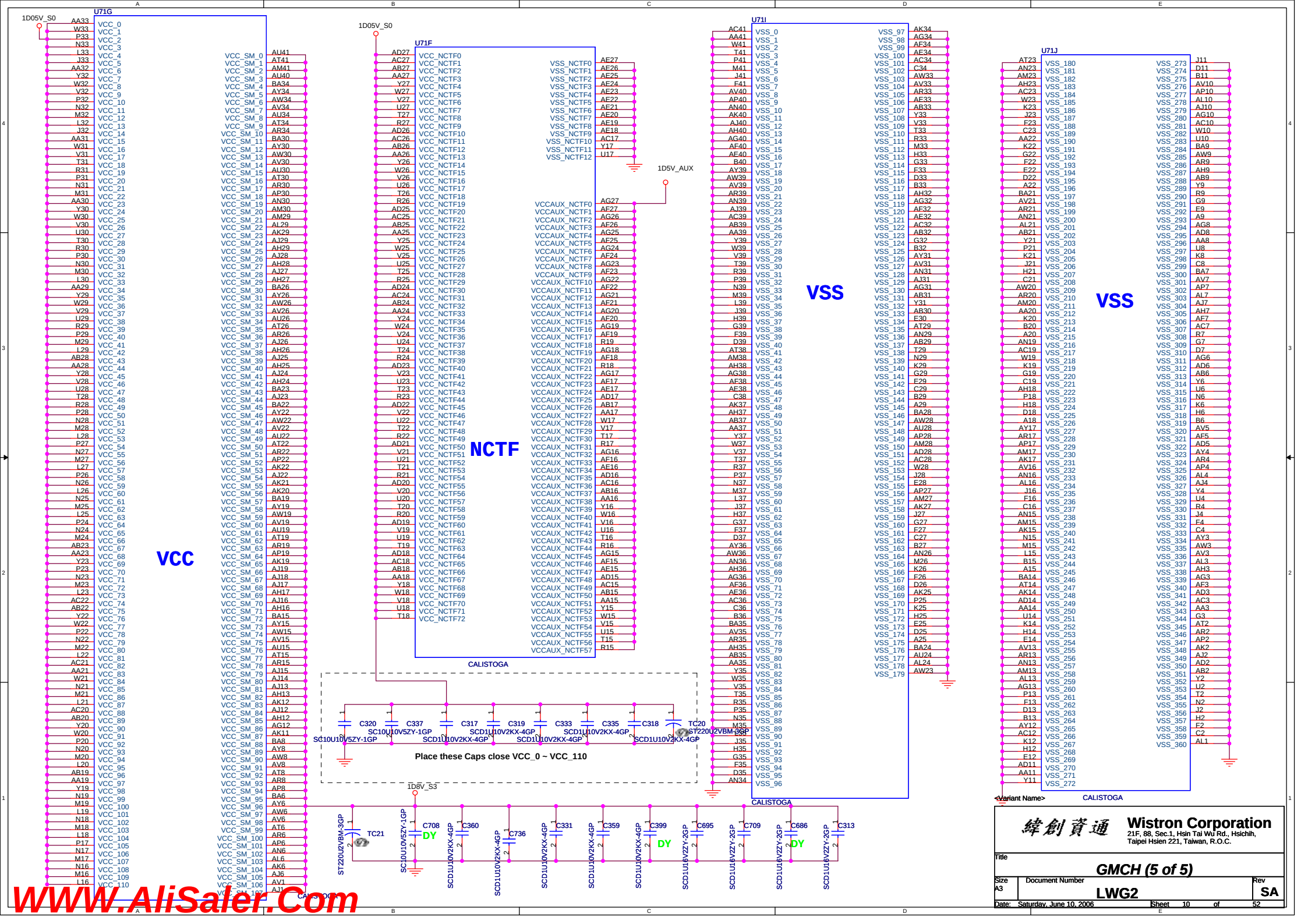
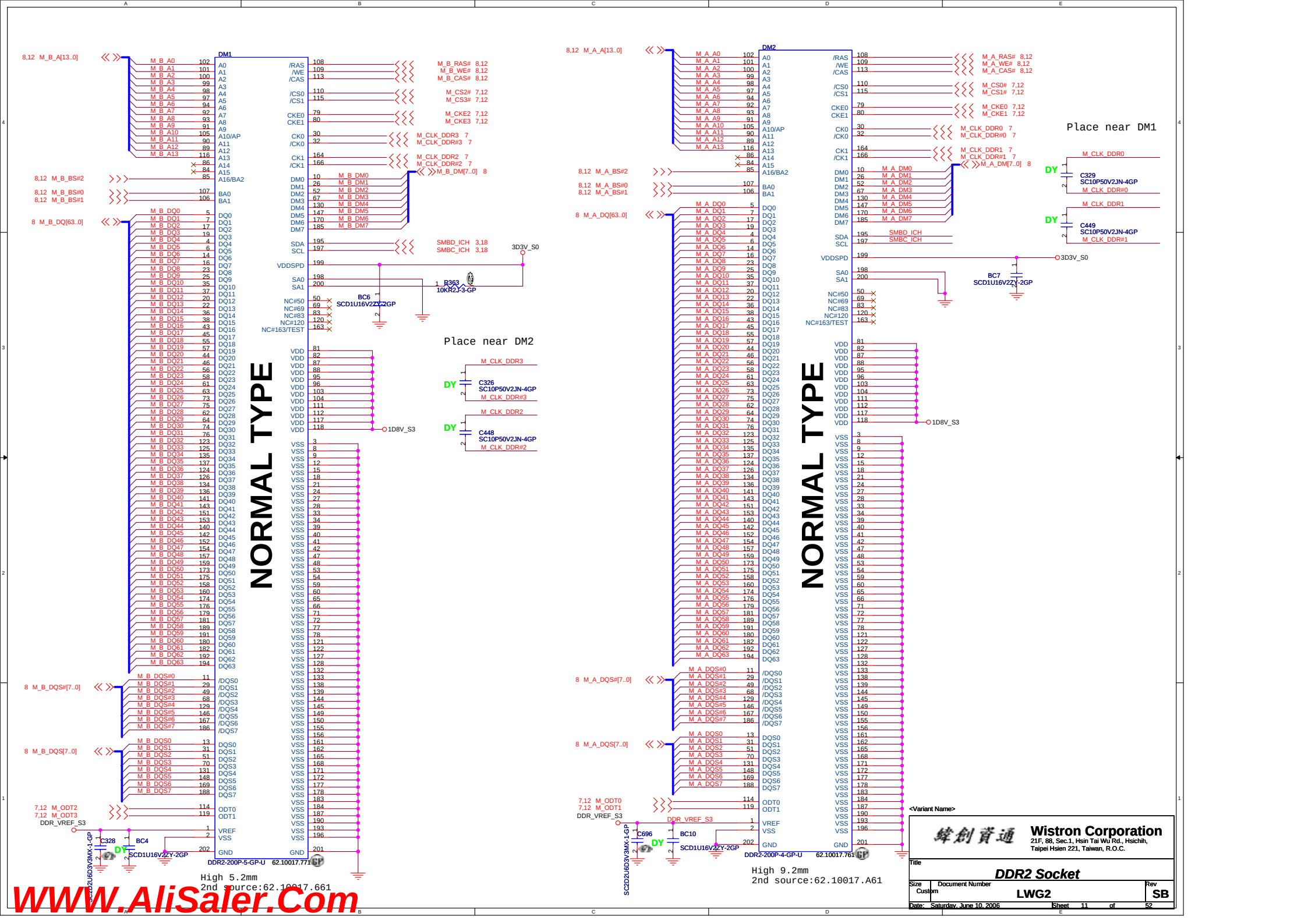
Title: ***GMCH (4 of 5)***

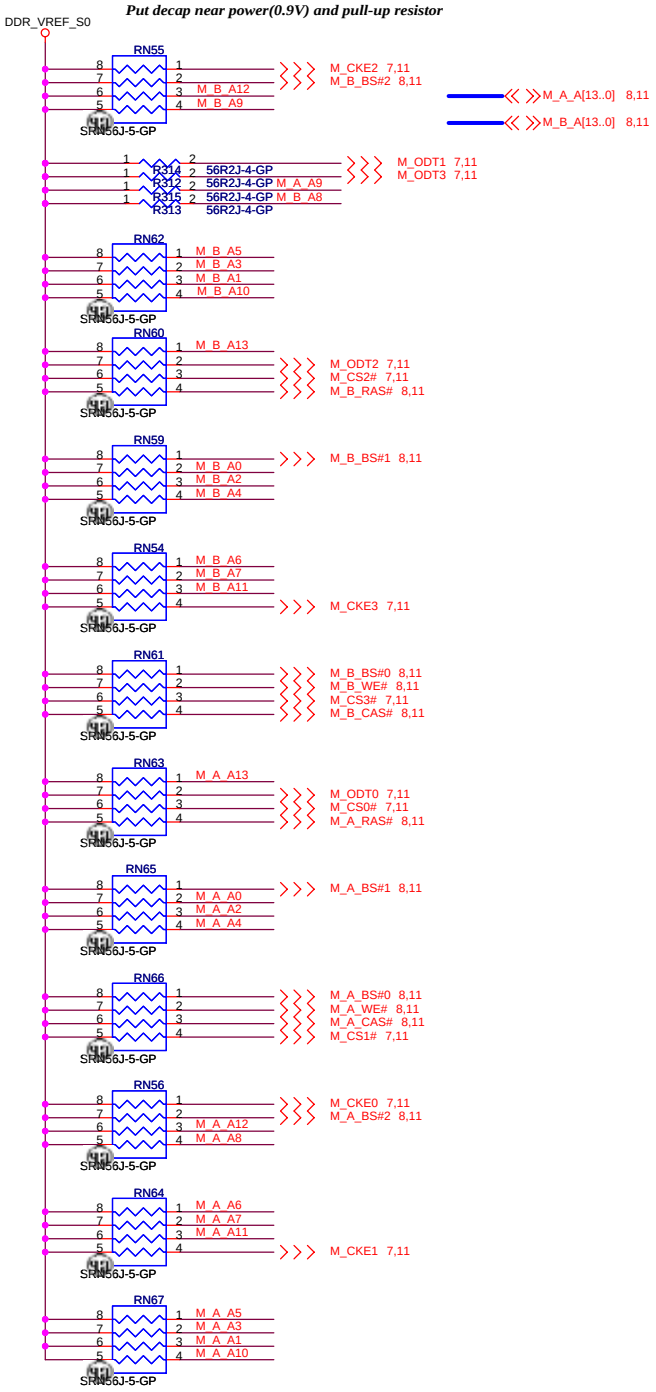
Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 9 of 52

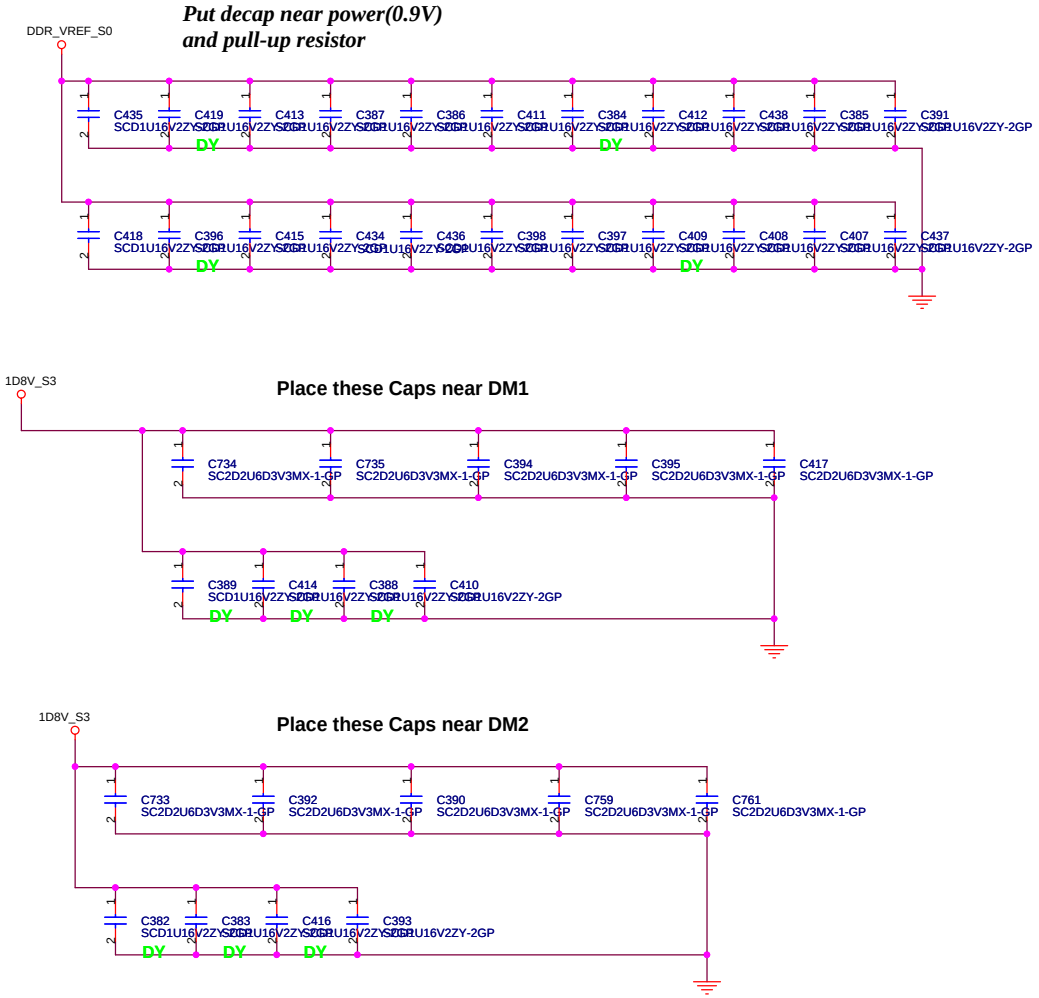




PARALLEL TERMINATION



Decoupling Capacitor



<Variant Name>

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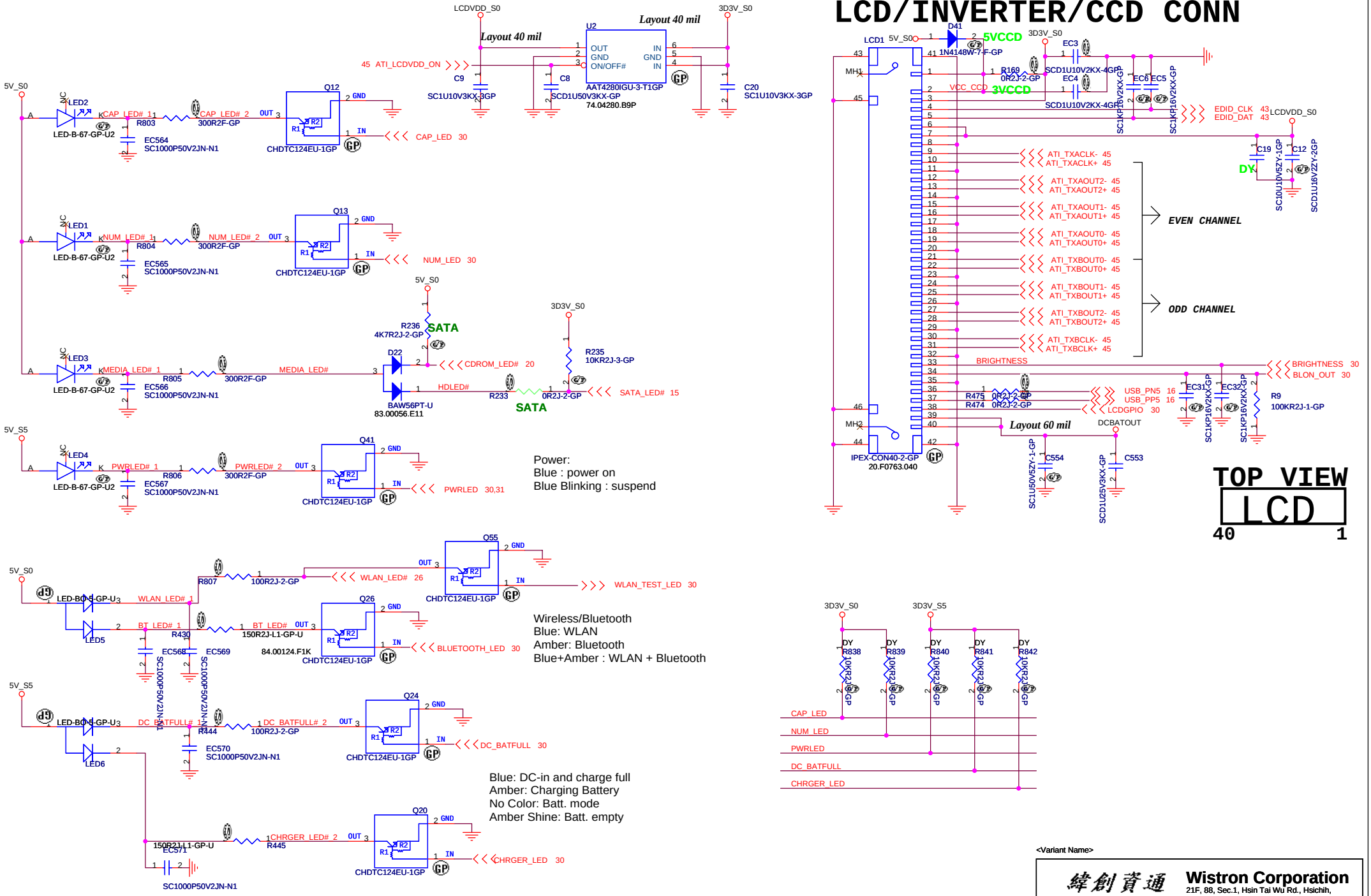
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 12 of 52

LCD/INVERTER/CCD CONN



Front panel

LED left side Right side

Power Battery Wireless Num Caps HDD

<Variant Name>

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Title: LCD / LAUNCH / LEDs

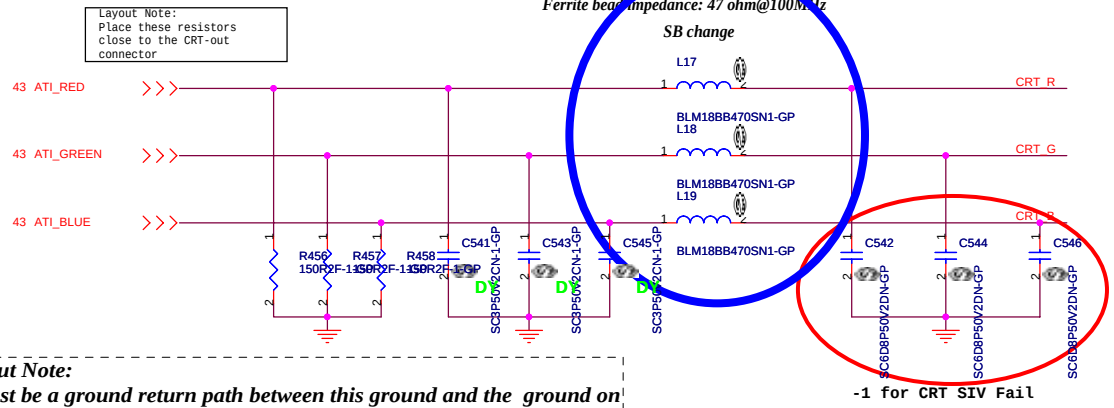
Size: Custom | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 13 of 52

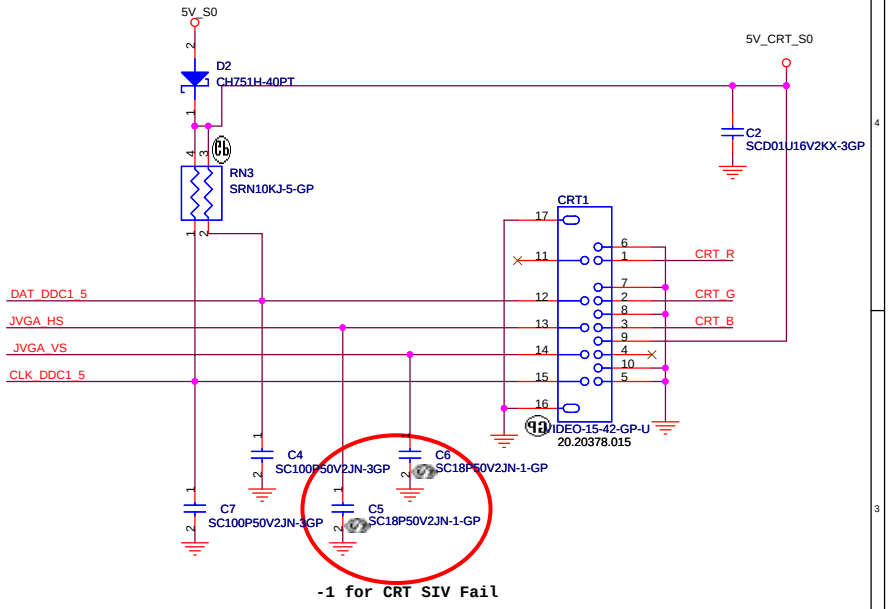
CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

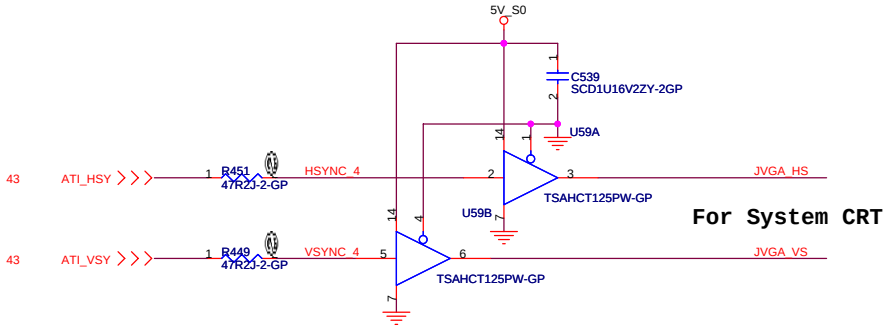
Ferrite bead impedance: 47 ohm@100MHz
SB change



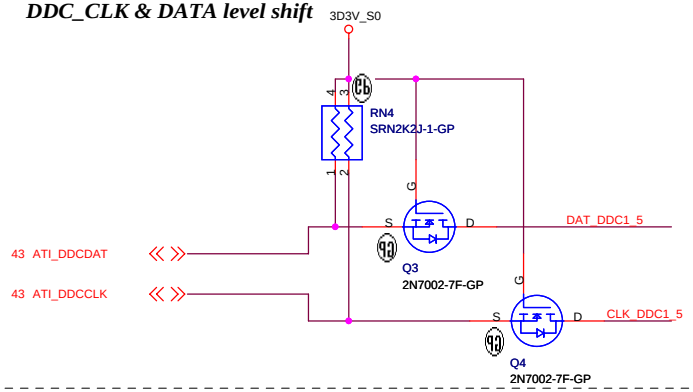
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



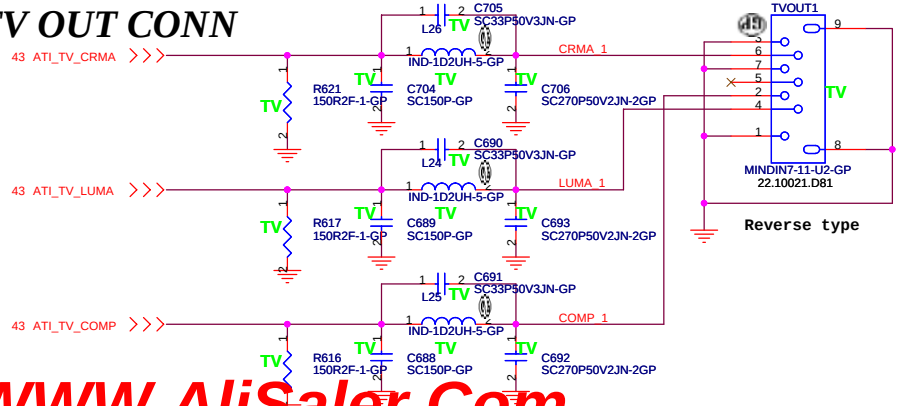
Hsync & Vsync level shift

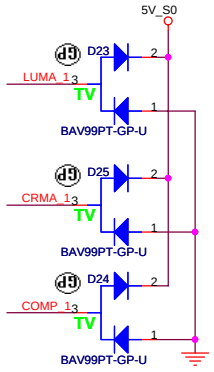


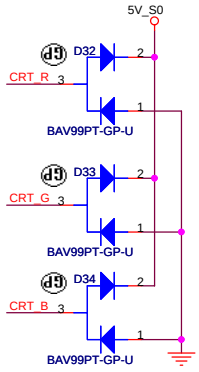
DDC_CLK & DATA level shift



TV OUT CONN







<Variant Name>

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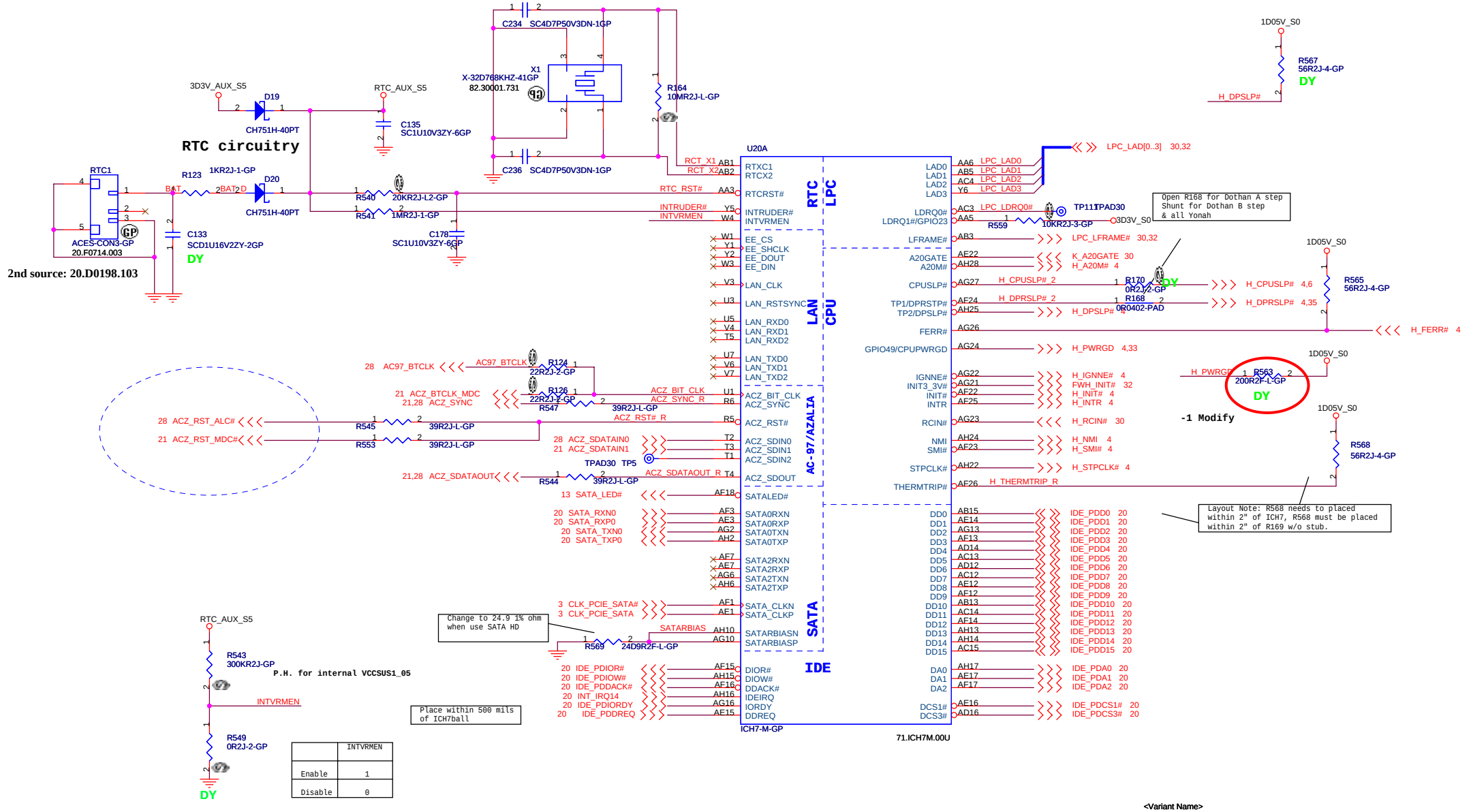
Title: ***CRT/TV Connector***

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 14 of 52



<Variant Name>

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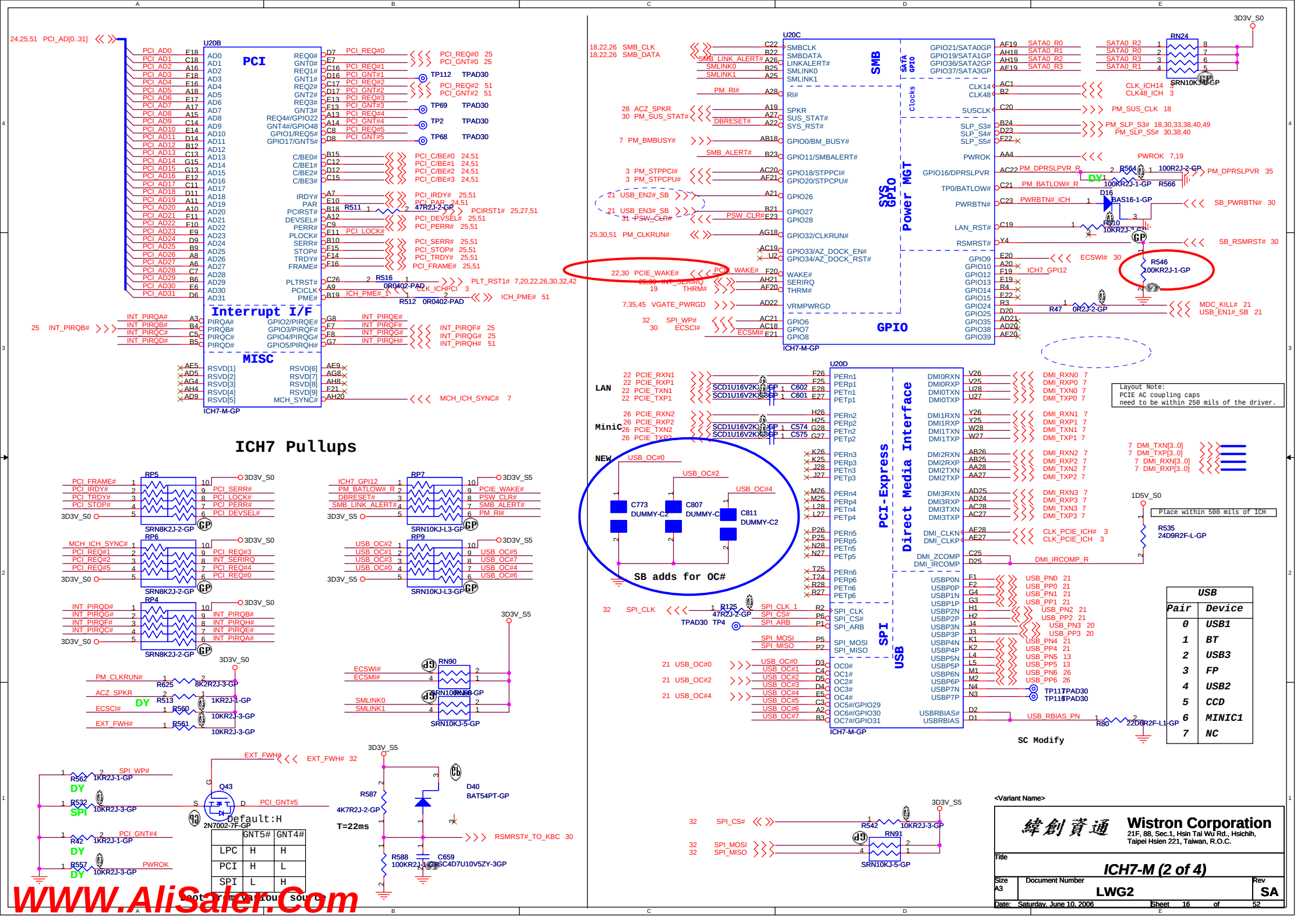
Title: ICH7-M (1 of 4)

Size	Document Number	Rev
A3	LWG2	SA

Date: Wednesday, June 21, 2006 Sheet 15 of 52


ICH7 Pullups
U20B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U20C
SMB
SYS GPIO
Power MGT
GPIO
ICH7-M-GP
U20D
PCI-Express
Direct Media Interface
USB
SPI
ICH7-M-GP
LAN
MiniC
NEW
SB adds for OC#
SC Modify
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB
Pair | Device
0 USB1
1 BT
2 USB3
3 FP
4 USB2
5 CCD
6 MINIC1
7 NC
Default:H
LPC H H
PCI H L
SPI L H
T=22ms
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
ICH7-M (2 of 4)
Size A3
Document Number LWG2
Rev SA
Date: Saturday, June 10, 2006
Sheet 16 of 52
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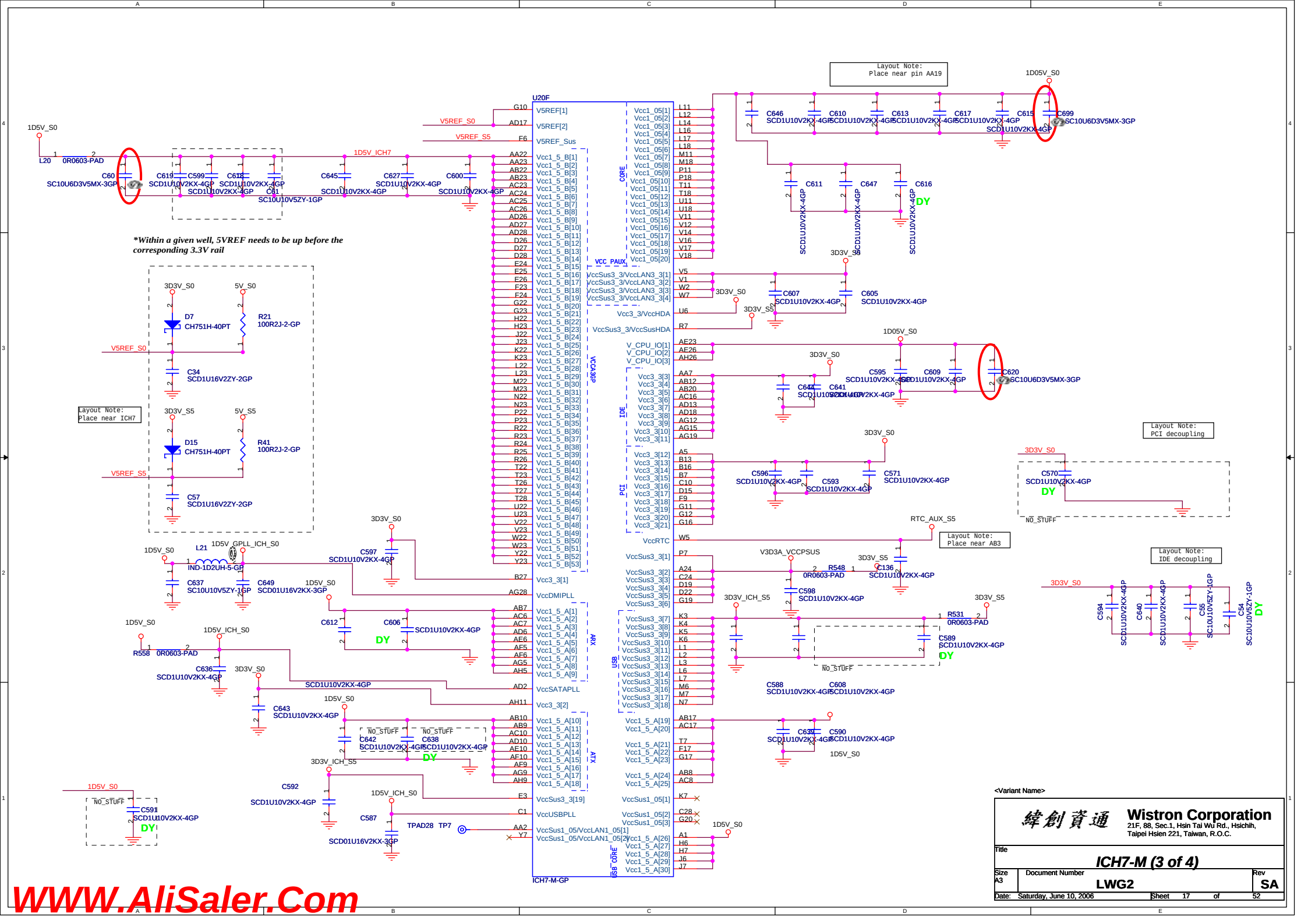
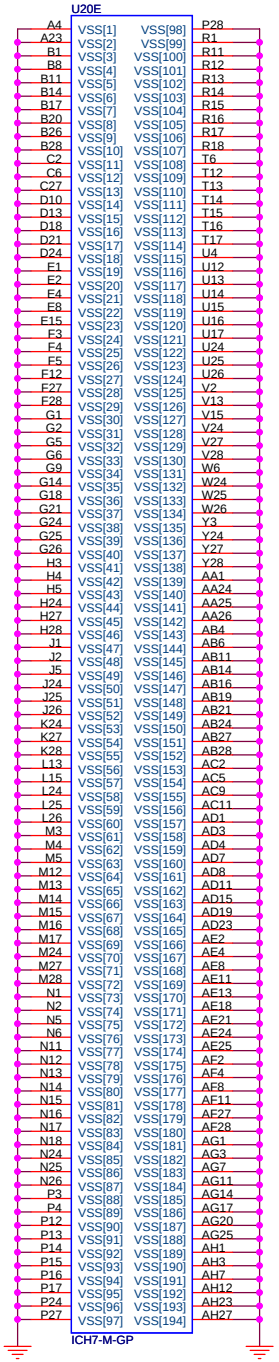
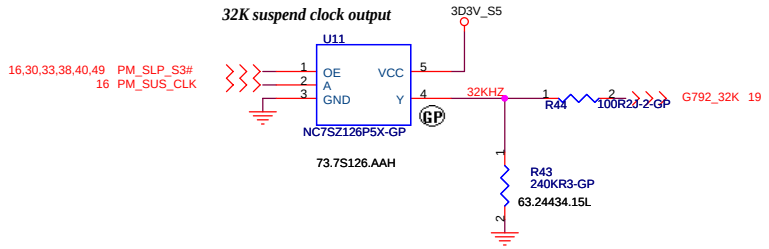
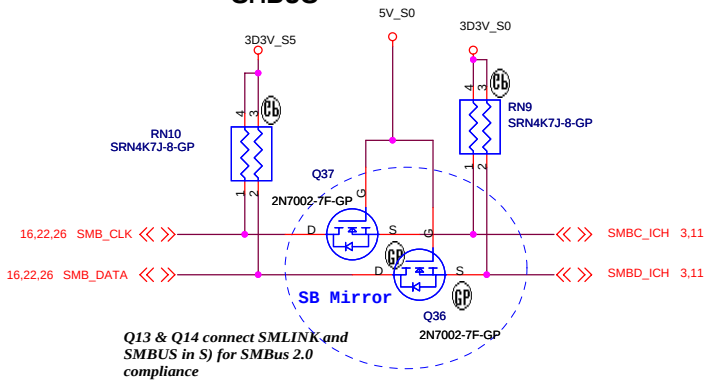

U20F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: PCI decoupling
Layout Note: Place near AB3
Layout Note: IDE decoupling
1D5V_S0
1D05V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
V5REF_S0
V5REF_S5
1D5V_ICH7
1D5V_GPLL_ICH_S0
1D5V_ICH_S0
3D3V_ICH_S5
V3D3A_VCCPSUS
RTC_AUX_S5
L20 0R0603-PAD
L21 IND-1D2UH-5-GP
D7 CH751H-40PT
D15 CH751H-40PT
R21 100R2J-2-GP
R41 100R2J-2-GP
R548 0R0603-PAD
R558 0R0603-PAD
R531 0R0603-PAD
C60 SC10U6D3V5MX-3GP
C81 SC10U10V5ZY-1GP
C34 SCD1U16V2ZY-2GP
C57 SCD1U16V2ZY-2GP
C637 SC10U10V5ZY-1GP
C649 SCD01U16V2KX-3GP
C699 SC10U6D3V5MX-3GP
C620 SC10U6D3V5MX-3GP
C54 SC10U10V5ZY-1GP
C55 SC10U10V5ZY-1GP
C587 SCD01U16V2KX-3GP
C592 SCD1U10V2KX-4GP
C591 SCD1U10V2KX-4GP
C597 SCD1U10V2KX-4GP
C612 SCD1U10V2KX-4GP
C606 SCD1U10V2KX-4GP
C643 SCD1U10V2KX-4GP
C642 SCD1U10V2KX-4GP
C638 SCD1U10V2KX-4GP
C646 SCD1U10V2KX-4GP
C610 SCD1U10V2KX-4GP
C613 SCD1U10V2KX-4GP
C617 SCD1U10V2KX-4GP
C615 SCD1U10V2KX-4GP
C611 SCD1U10V2KX-4GP
C647 SCD1U10V2KX-4GP
C616 SCD1U10V2KX-4GP
C607 SCD1U10V2KX-4GP
C605 SCD1U10V2KX-4GP
C595 SCD1U10V2KX-4GP
C609 SCD1U10V2KX-4GP
C644 SCD1U10V2KX-4GP
C641 SCD1U10V2KX-4GP
C596 SCD1U10V2KX-4GP
C593 SCD1U10V2KX-4GP
C571 SCD1U10V2KX-4GP
C570 SCD1U10V2KX-4GP
C136 SCD1U10V2KX-4GP
C598 SCD1U10V2KX-4GP
C589 SCD1U10V2KX-4GP
C588 SCD1U10V2KX-4GP
C608 SCD1U10V2KX-4GP
C633 SCD1U10V2KX-4GP
C590 SCD1U10V2KX-4GP
C594 SCD1U10V2KX-4GP
C640 SCD1U10V2KX-4GP
TPAD28 TP7
DY
N0_STUFF
CORE
VCC_PAUX
VCCA3GP
IDE
PCI
ARY
USB
ATX
USB CORE
WWW.AliSaler.Com
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number LWG2
Rev SA
Date: Saturday, June 10, 2006
Sheet 17 of 52



32K suspend clock output



SMBUS



Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

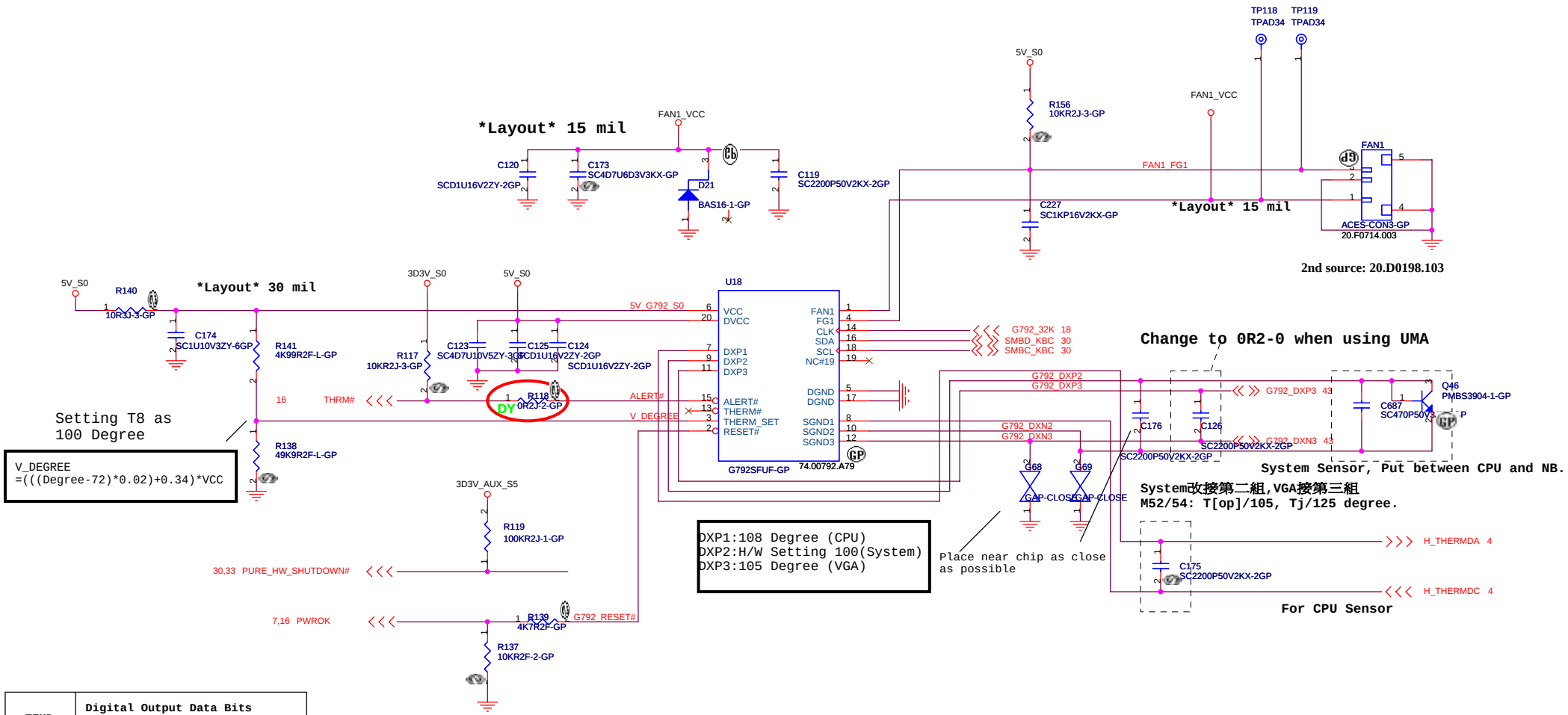
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

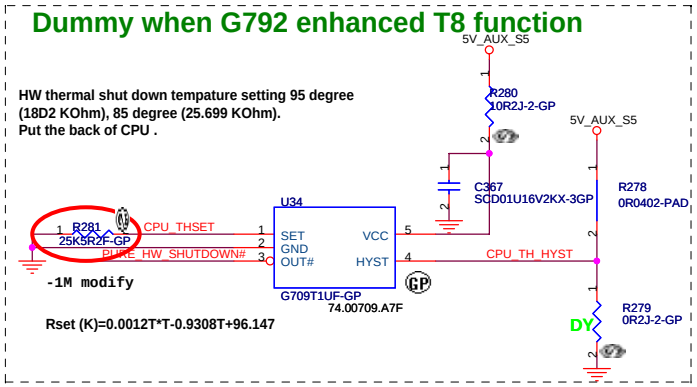
Title: *ICH7-M (4 of 4)*

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 18 of 52



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



Thermal Get Setting

		T6	T7
Sencor 0	CPU DTS	98	100
Sencor 1	G792-1 CPU	98	100
Sencor 2	G792-2 System	78	83
Sencor 3	G792-3 VGA	110	115

<Variant Name>

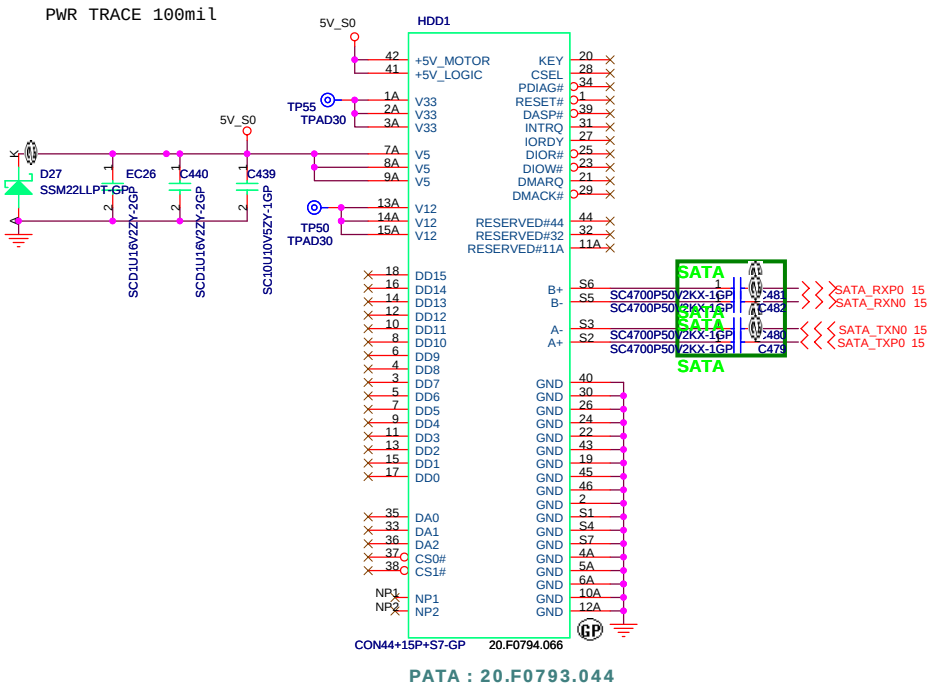
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

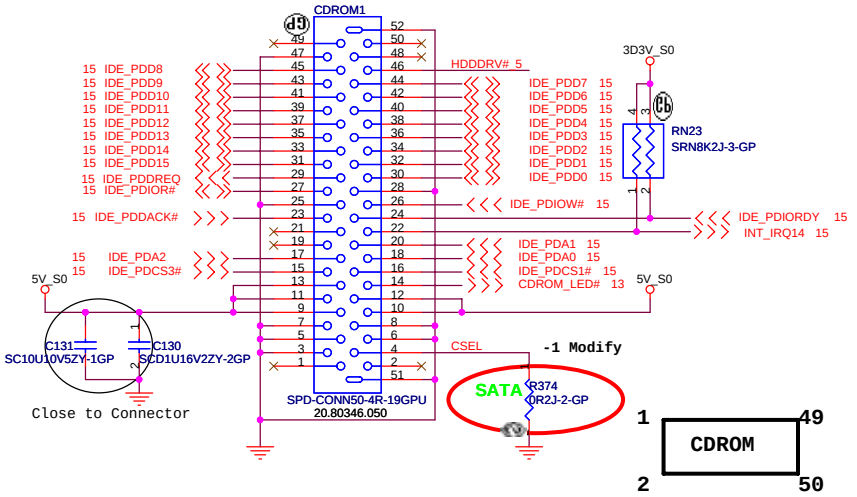
Size: Custom | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 19 of 52

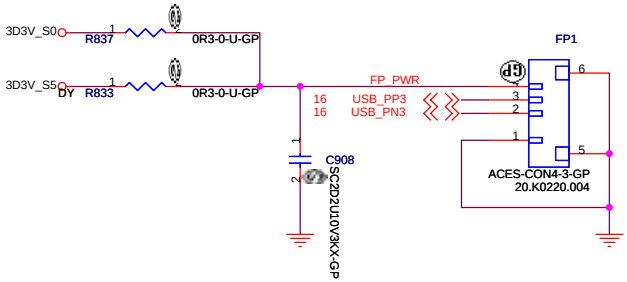
SATA Connector

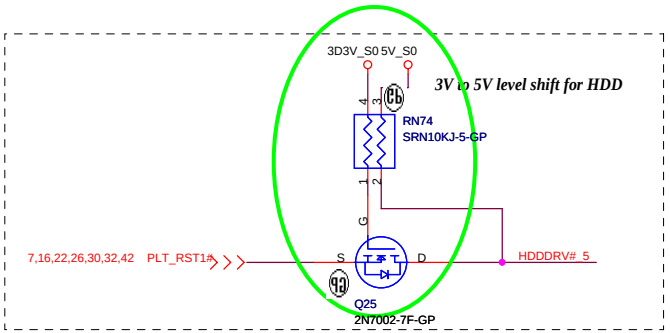


CDROM Connector



Finger Print





EC: N060446

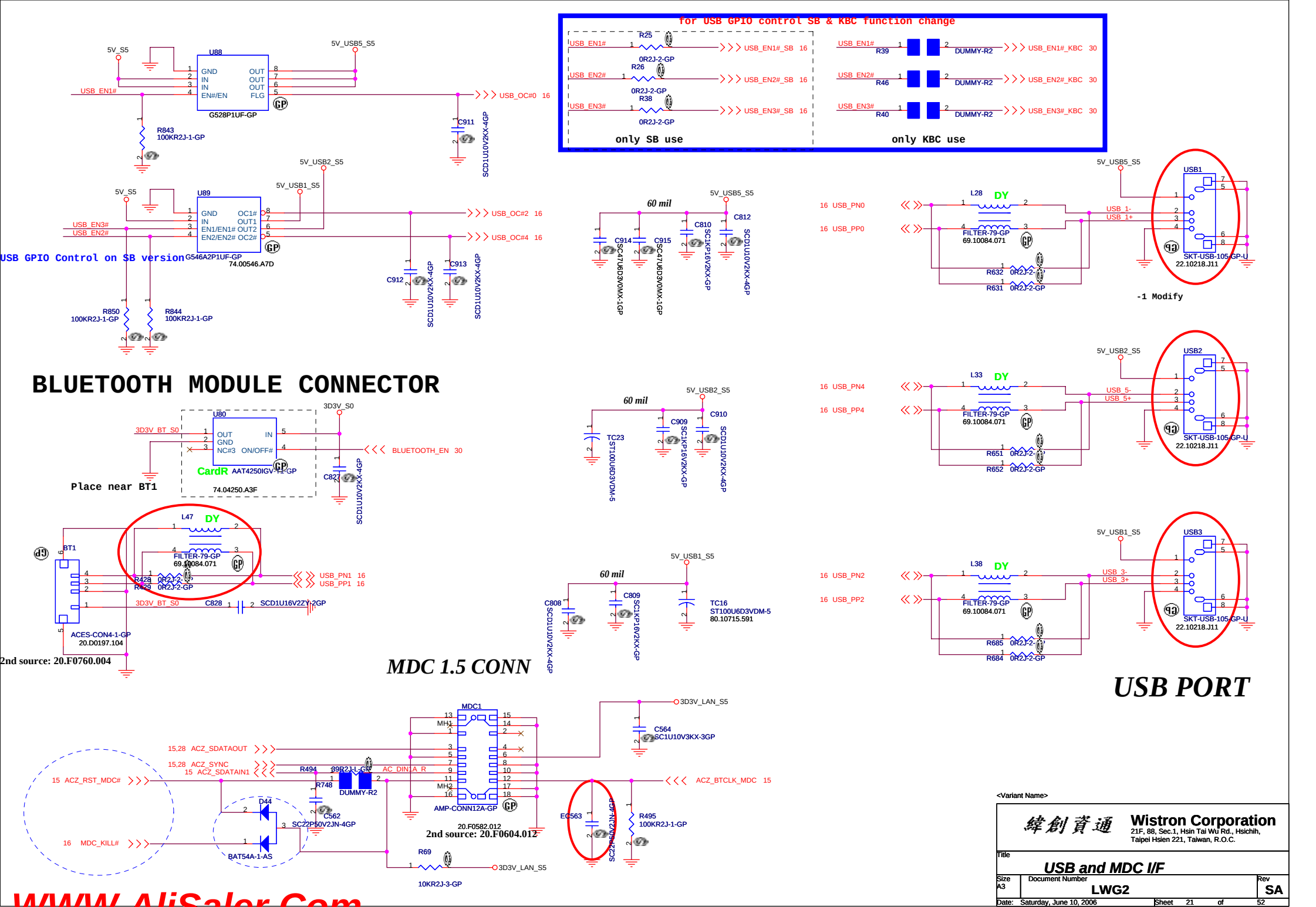
<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA HDD / ODD /FINGER PRINT

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 20 of 52


for USB GPIO control SB & KBC function change
only SB use
only KBC use
USB GPIO Control on SB version
BLUETOOTH MODULE CONNECTOR
Place near BT1
MDC 1.5 CONN
USB PORT
-1 Modify
2nd source: 20.F0760.004
2nd source: 20.F0604.012
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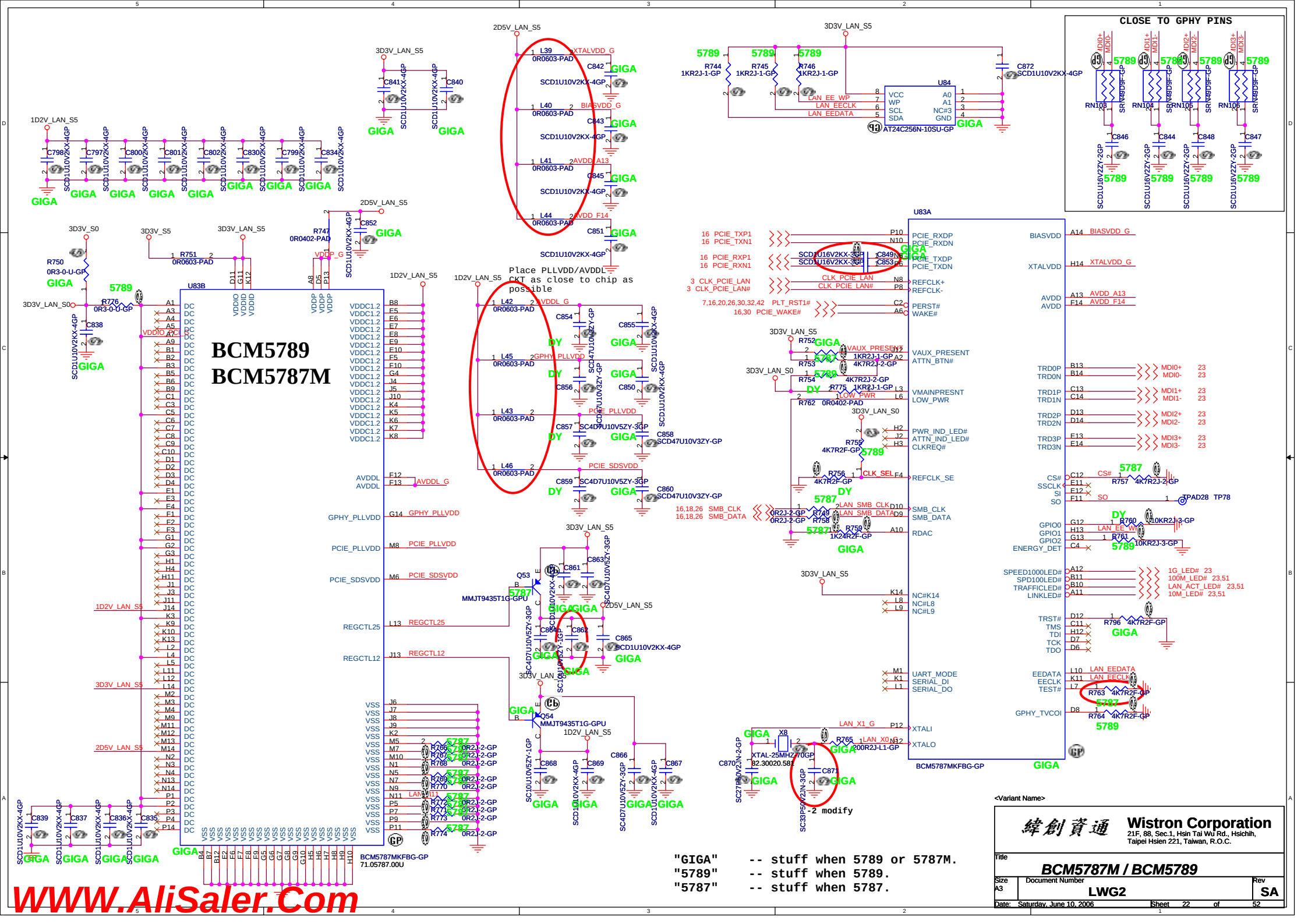
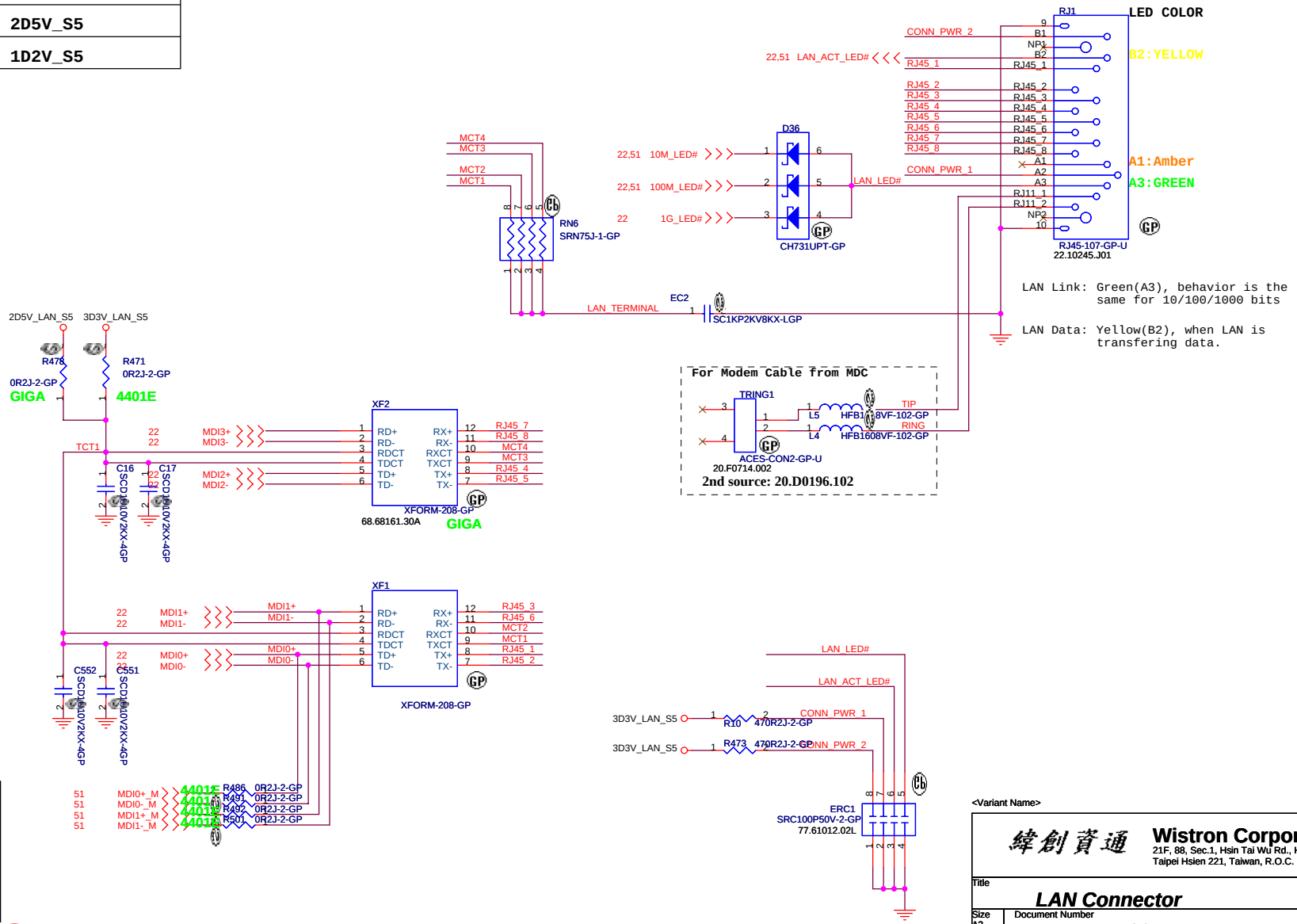
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
USB and MDC I/F
LWG2
SA
Saturday, June 10, 2006


BCM5789
BCM5787M
Place PLLVDD/AVDDL CKT as close to chip as possible
CLOSE TO GPHY PINS
BCM5787MKFBG-GP
71.05787.00U
BCM5787MKFBG-GP
-2 modify
"GIGA" -- stuff when 5789 or 5787M.
"5789" -- stuff when 5789.
"5787" -- stuff when 5787.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BCM5787M / BCM5789
LWG2
SA
Saturday, June 10, 2006
22
52
WWW.AliSaler.Com

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

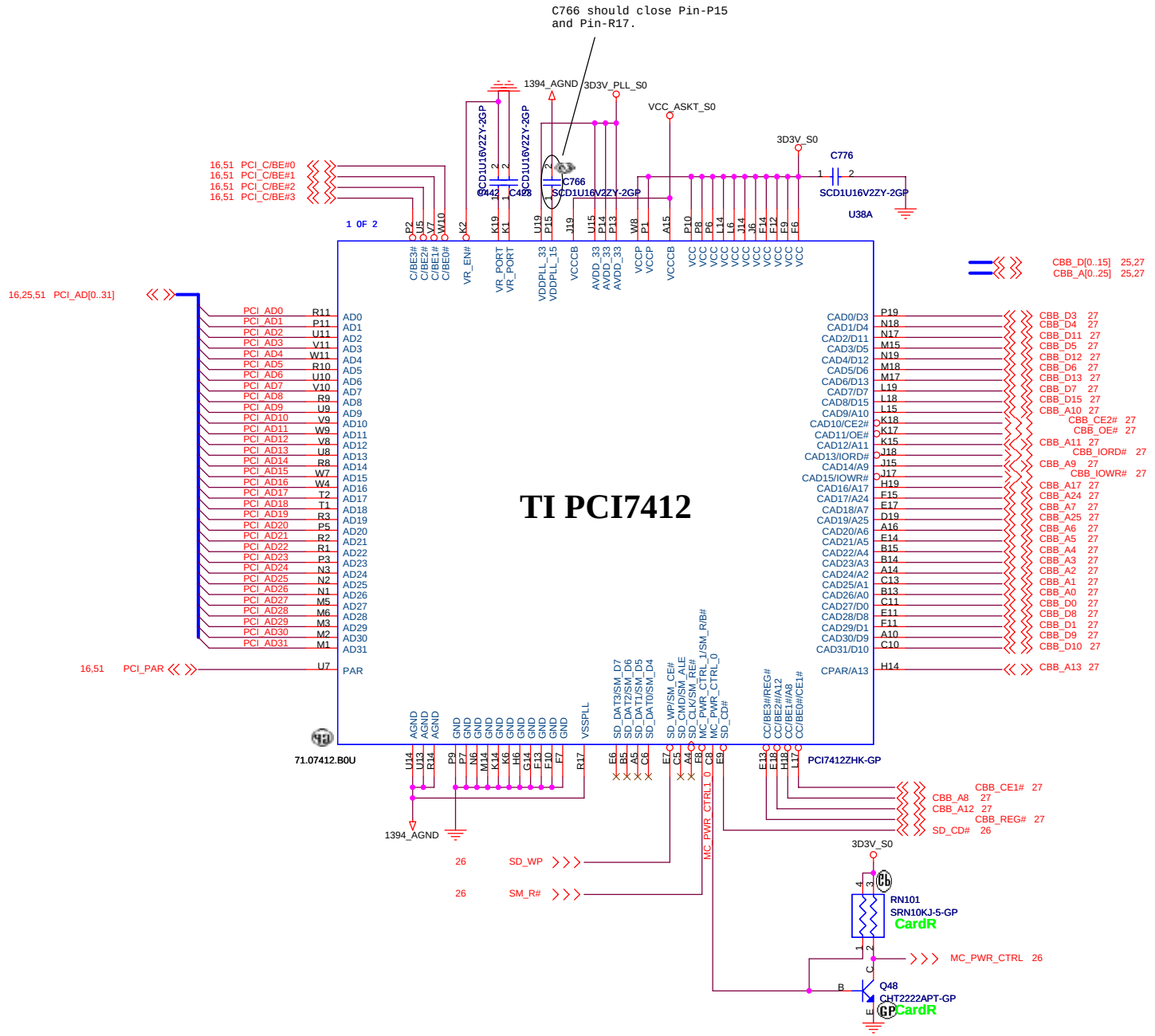
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Variant Name>

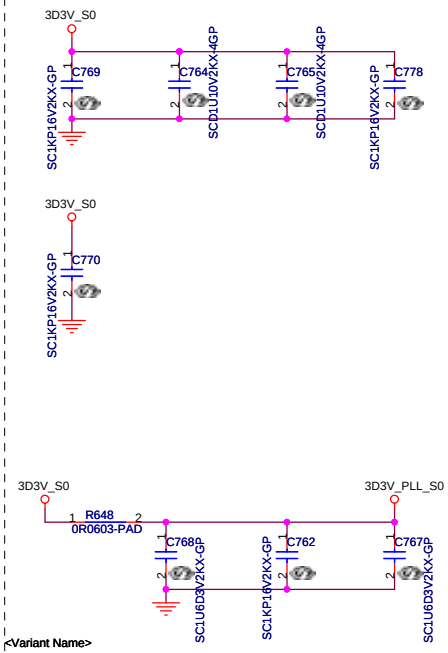
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector
Size: A3 | Document Number: LWG2 | Rev: SA
Date: Monday, June 12, 2006 | Sheet 23 of 52



* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible

Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible



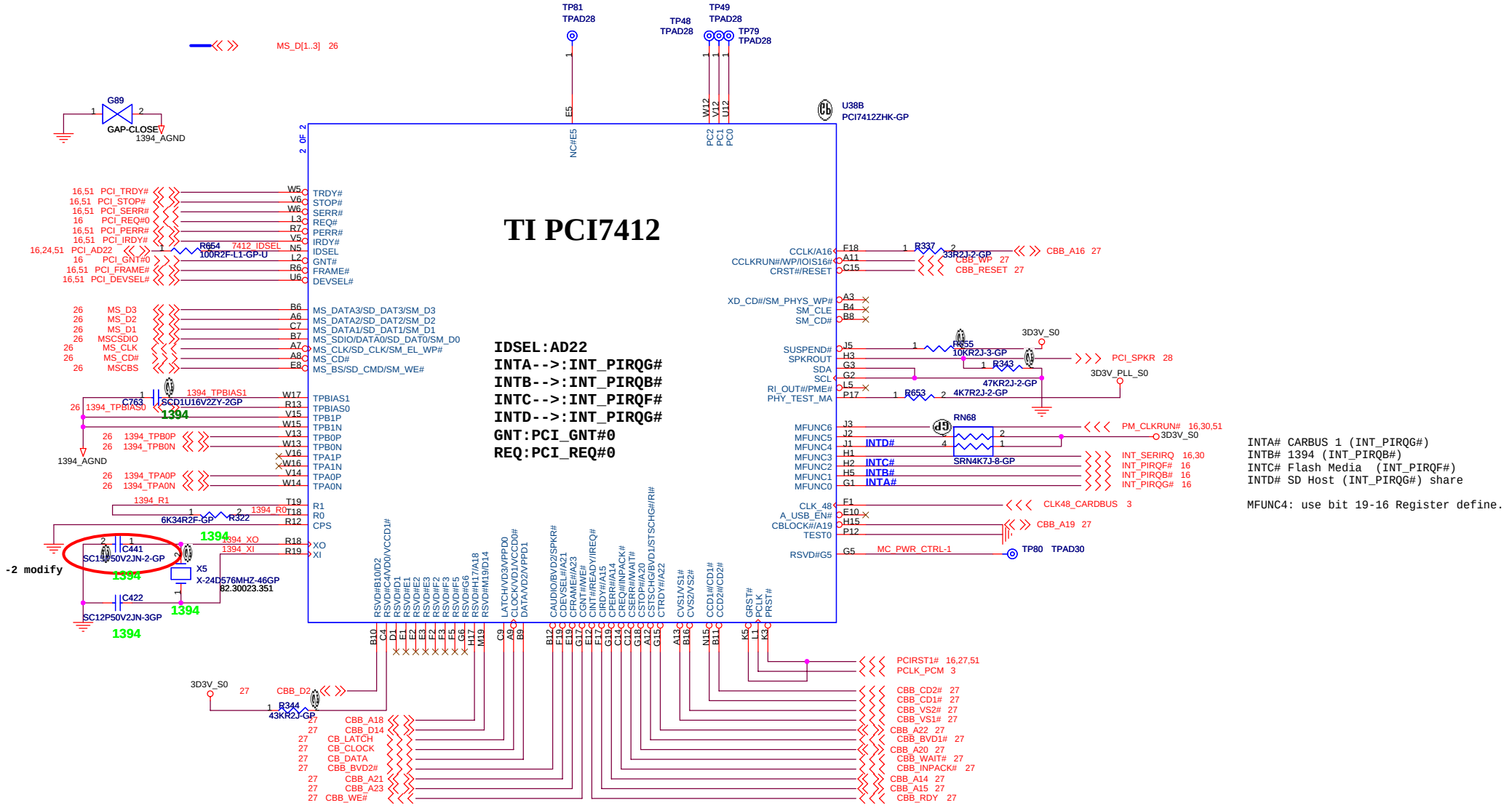
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TI PCI7412 (1 of 2)

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 24 of 52



INTA# CARBUS 1 (INT_PIRQG#)
INTB# 1394 (INT_PIRQB#)
INTC# Flash Media (INT_PIRQF#)
INTD# SD Host (INT_PIRQG#) share

MFUNC4: use bit 19-16 Register define.

<Variant Name>

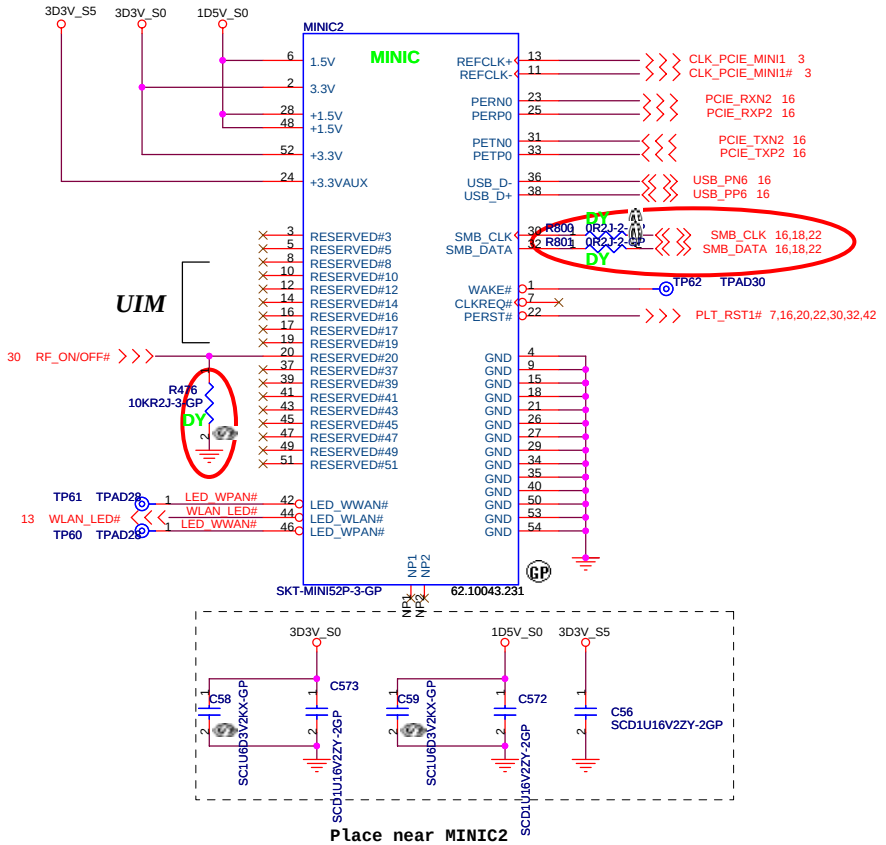
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI PCI7412 (2 of 2)**

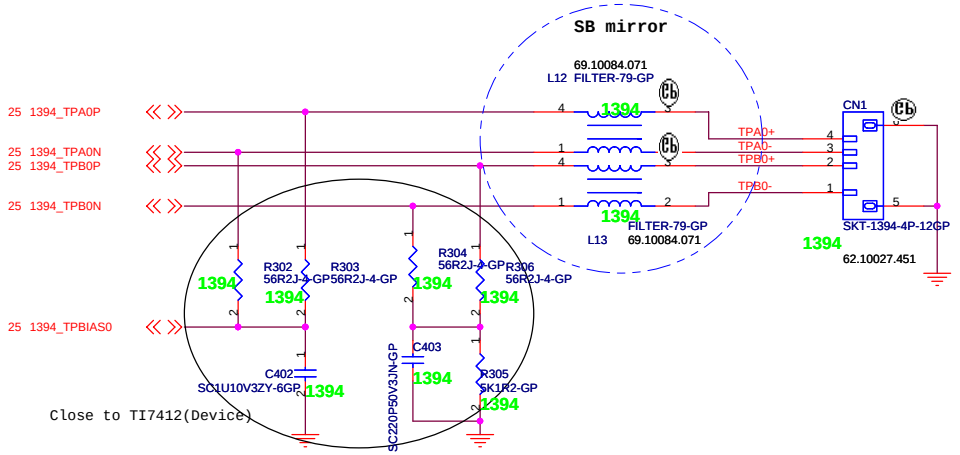
Size	Document Number	Rev
A3	LWG2	SA

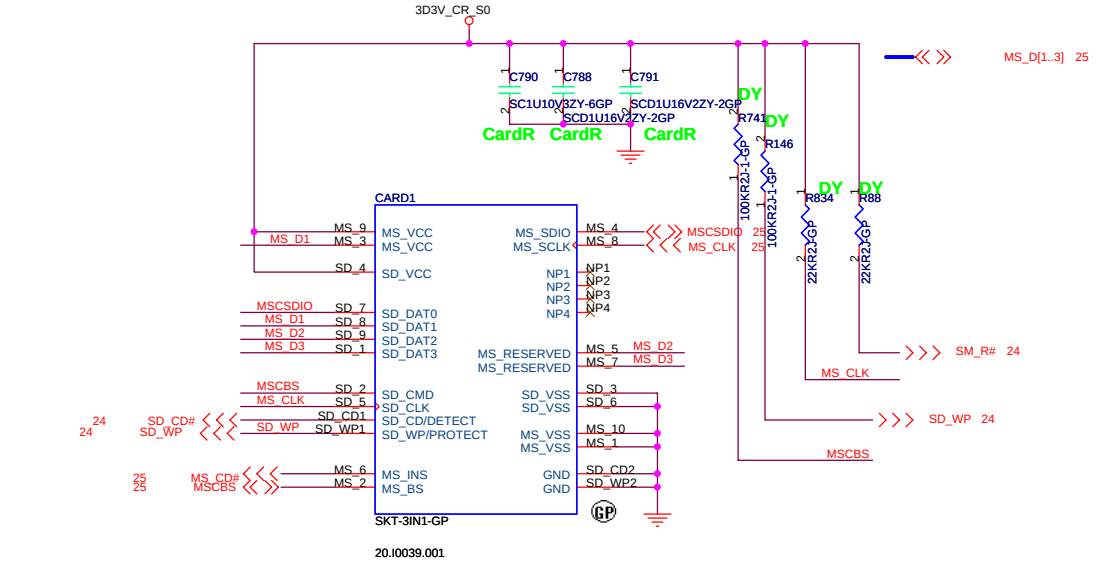
Date: Saturday, June 10, 2006 Sheet 25 of 52

Mini Card Connector



1394 Connector



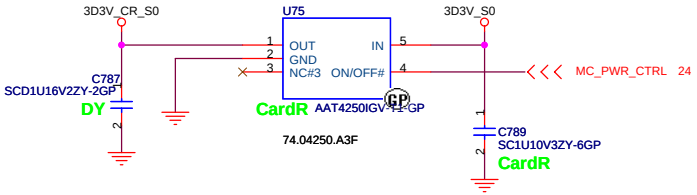


Bottom VIEW

1 36

Reader

POWER SWITCH



<Variant Name>

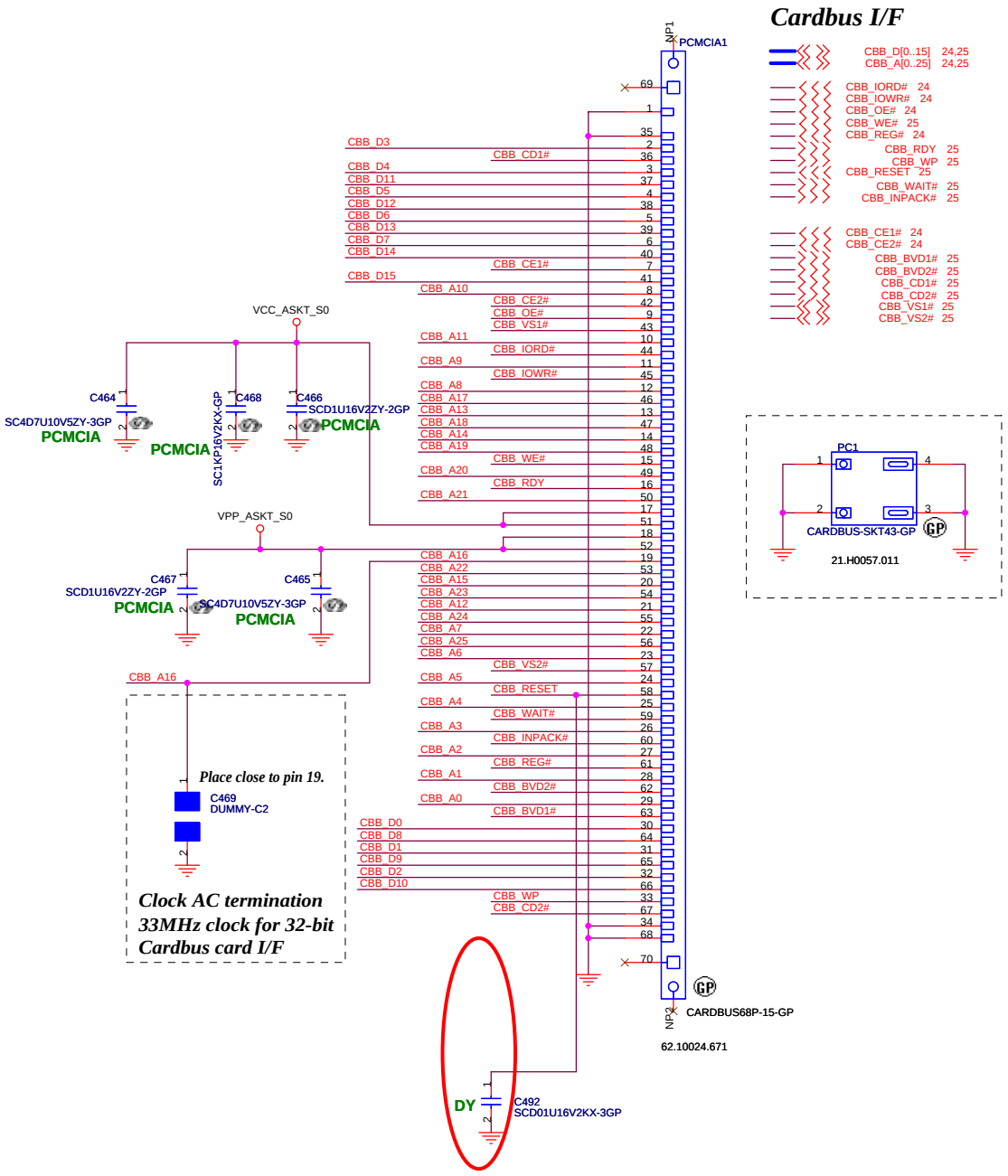
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / 1394

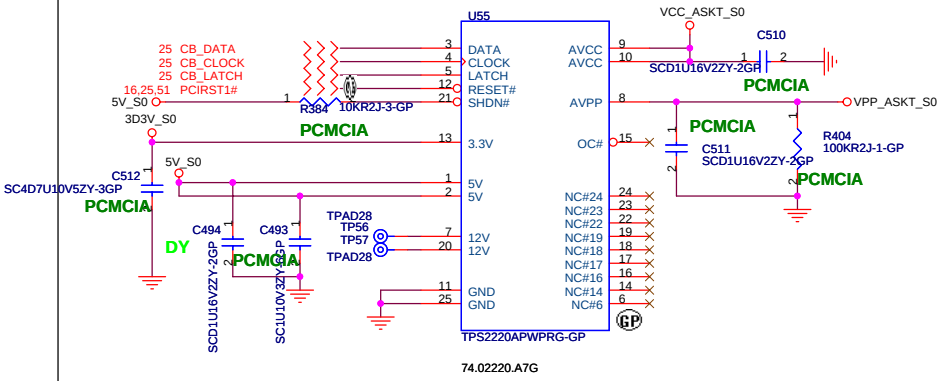
Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 26 of 52

PCMCIA Socket



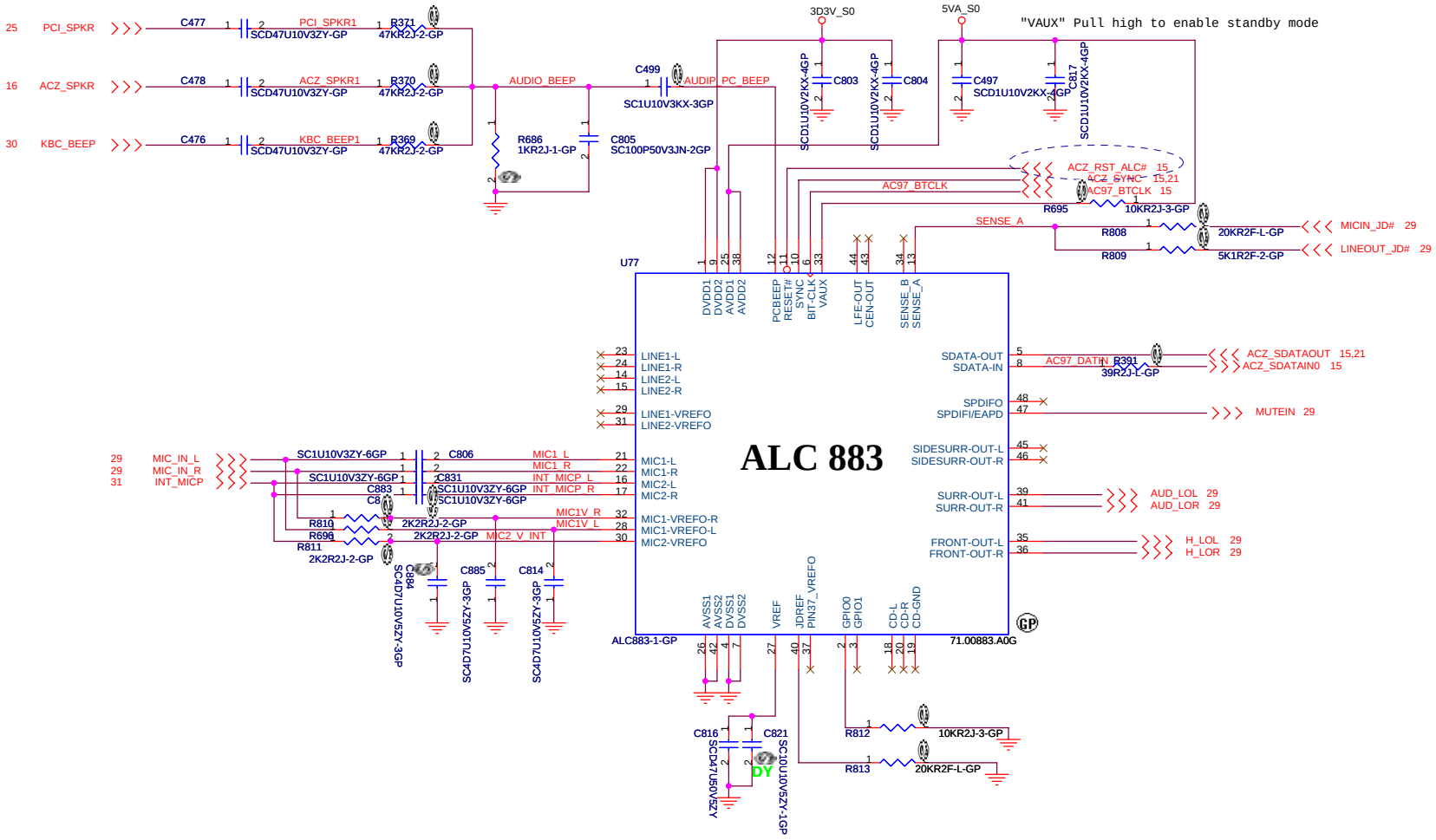
Power switch

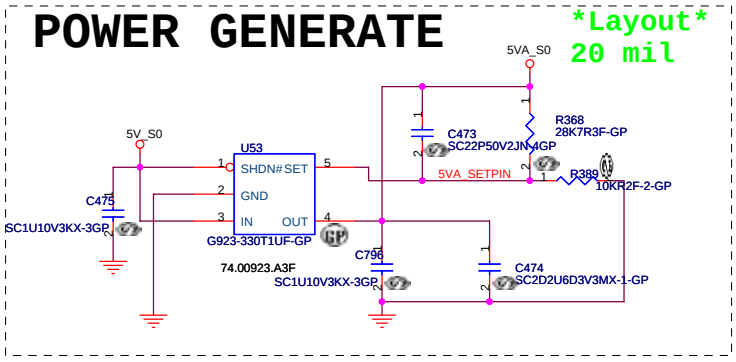


<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCIA	
Size A3	Document Number LWG2	Rev SA
Date: Saturday, June 10, 2006	Sheet 27 of 52	





1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	*Symbol*	*Location*	*Re-tasking*
35/36	*FRONT*	*AMP,Jack1*	AMP output, line input
39/41	*SURR*	*X*	X
43/44	*CEN/LEFT*	*X*	SURR-VREFO-L/R
45/46	*SIDESURR*	*X*	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	*LINE1*	*Jack 2*	Line input, line output
21/22	*MIC1*	*Jack 3*	Mic input, line output
14/15	*LINE2*	*X*	X
16/17	*MIC2*	*Int. Mic*	Mic input

<Variant Name>

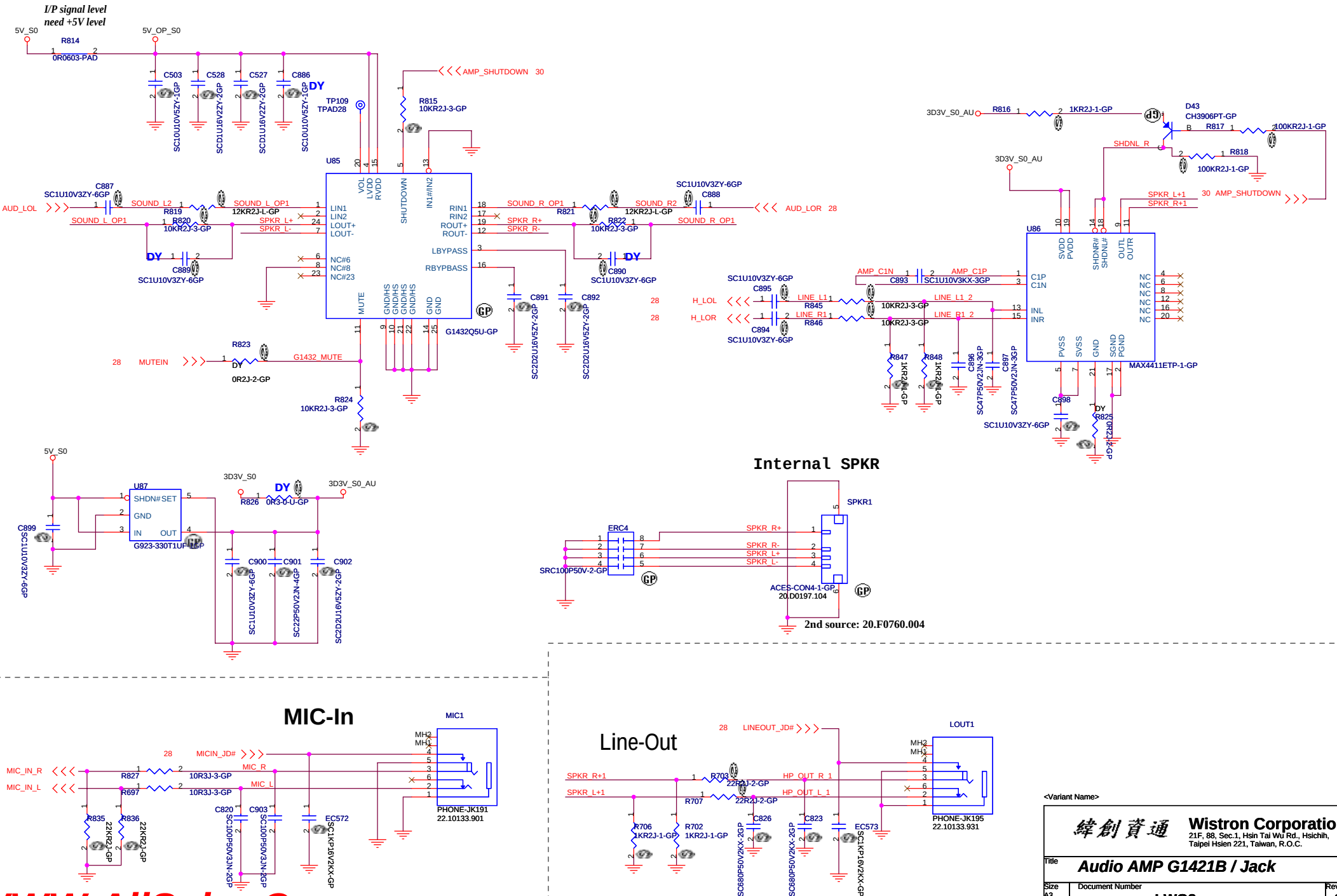
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Azalia codec ALC883**

Size: A3 | Document Number: LWG2 | Rev: SA

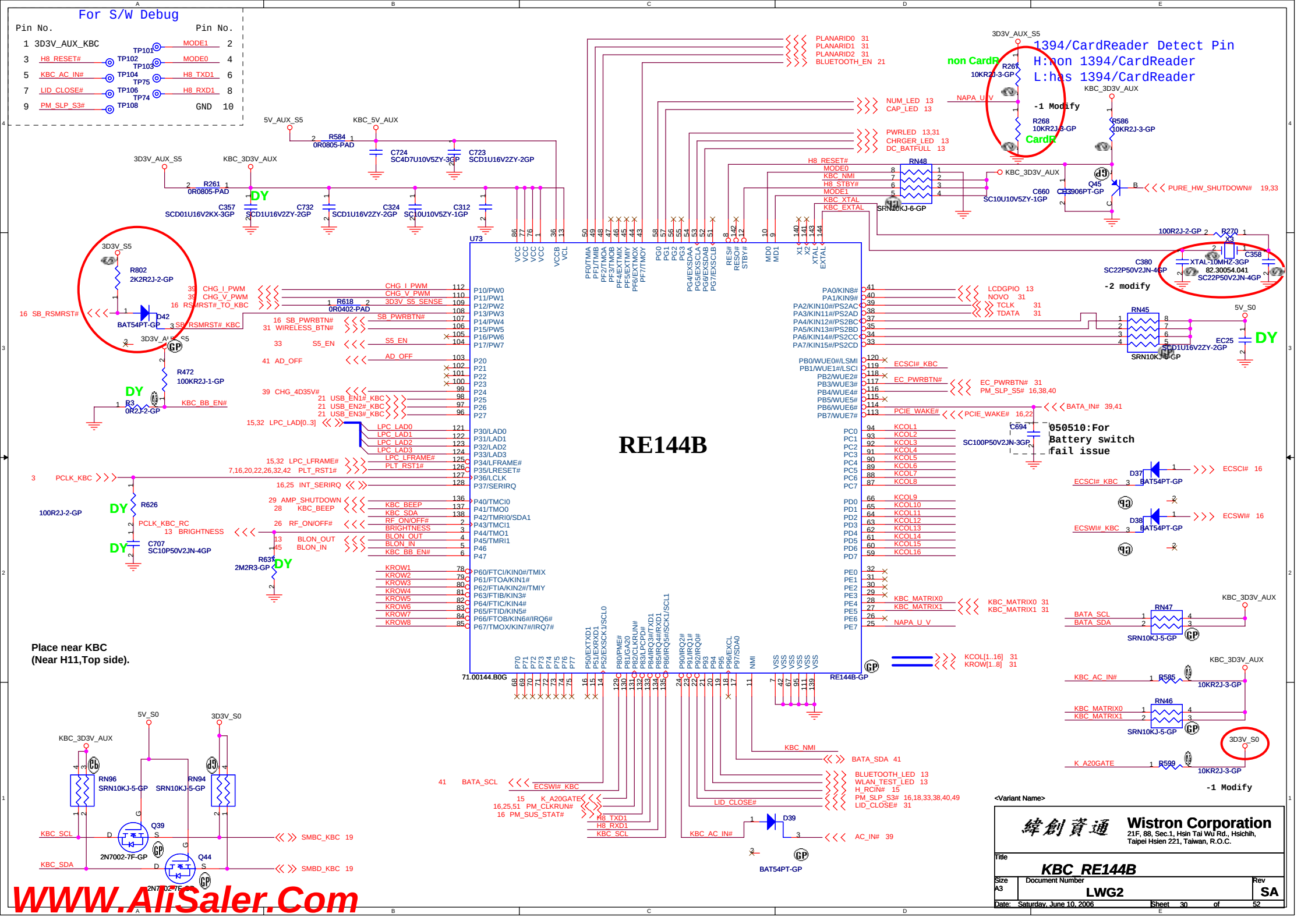
Date: Saturday, June 10, 2006 | Sheet 28 of 52

AUDIO OP AMPLIFIER



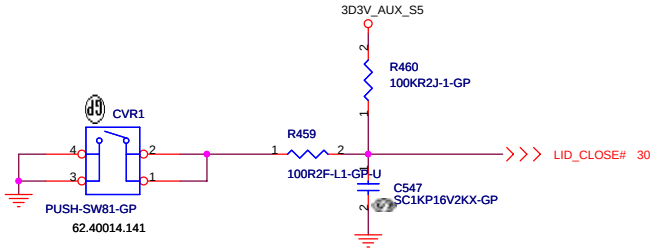
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Audio AMP G1421B / Jack	
Size A3	Document Number LWG2	Rev SA
Date: Saturday, June 10, 2006	Sheet 29 of 52	

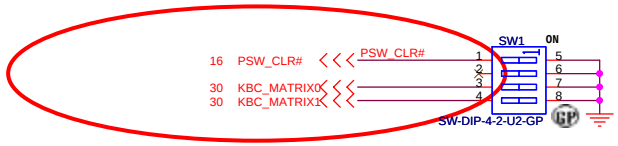

For S/W Debug
Pin No. Pin No.
1 3D3V_AUX_KBC
3 H8_RESET# TP102 MODE1 2
TP101 TP103
5 KBC_AC_IN# TP104 MODE0 4
TP75
7 LID_CLOSE# TP106 H8_TXD1 6
TP74
9 PM_SLP_S3# TP108 H8_RXD1 8
GND 10
RE144B
U73
71.00144.B0G
RE144B-GP
1394/CardReader Detect Pin
H:non 1394/CardReader
L:has 1394/CardReader
non CardR
CardR
-1 Modify
-2 modify
050510:For
Battery switch
fail issue
Place near KBC
(Near H11,Top side).
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_RE144B
LWG2
SA
Saturday, June 10, 2006
WWW.AliSaler.Com

Internal KeyBoard Connector

COVER SWITCH

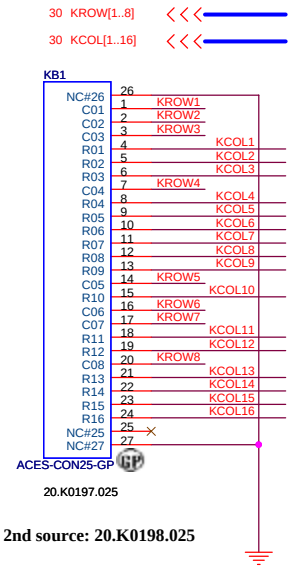


2nd source: 62.40010.151



Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

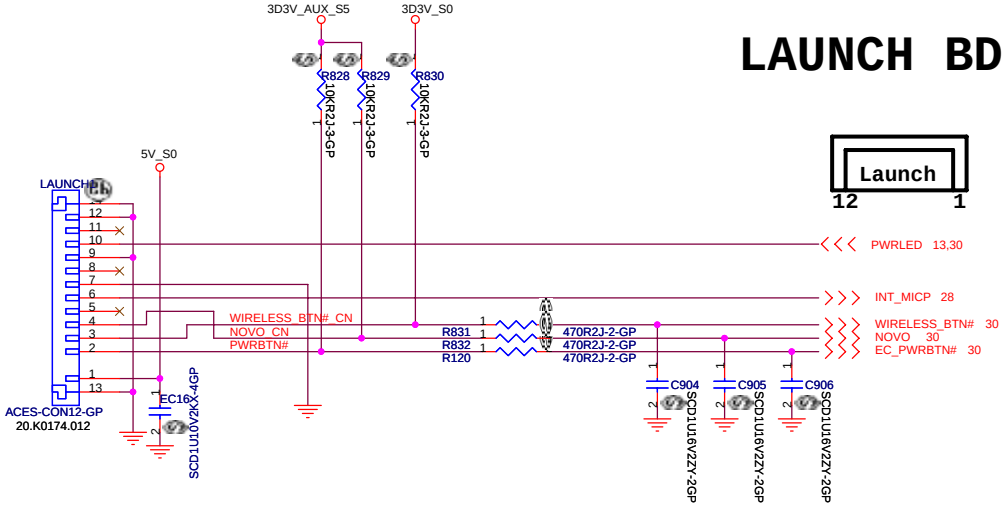


2nd source: 20.K0198.025

1 25

K/B

LAUNCH BD CONN

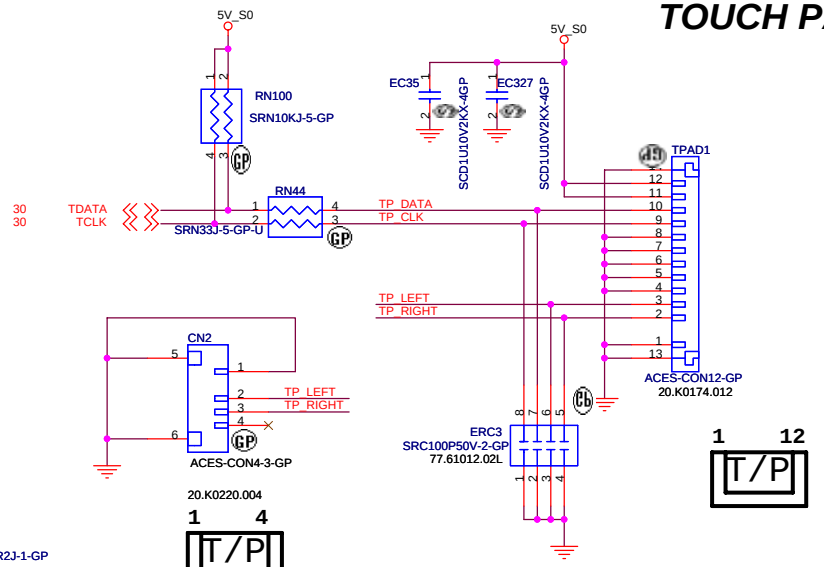


Launch

12 1

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

TOUCH PAD

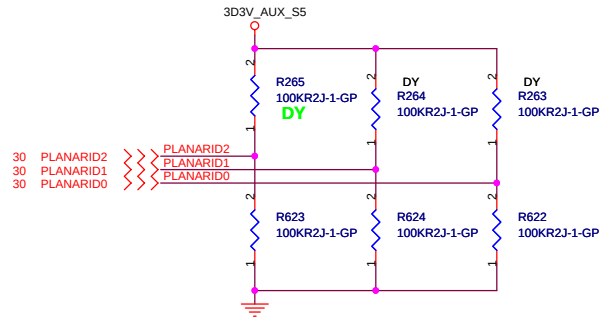


1 4

T/P

1 12

T/P



Planar
ID(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC,-1/-1m: 0,1,0
-2: 0,1,1

<Variant Name>

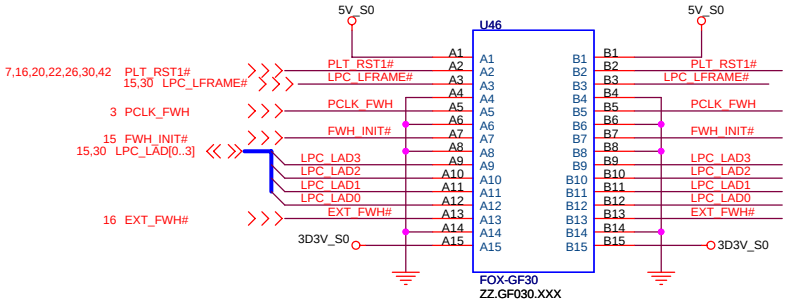
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KEYBOARD/TOUCHPAD**

Size	Document Number	Rev
A3	LWG2	SA

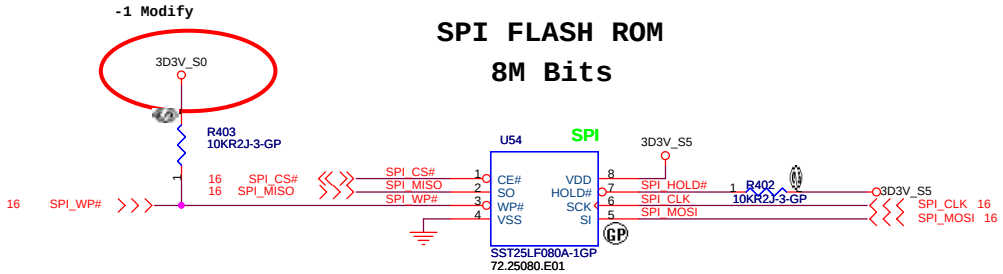
Date: Monday, June 12, 2006 Sheet 31 of 52

GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SPI FLASH ROM
8M Bits



SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

<Variant Name>

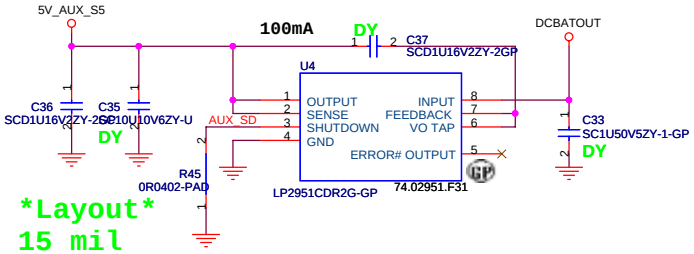
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

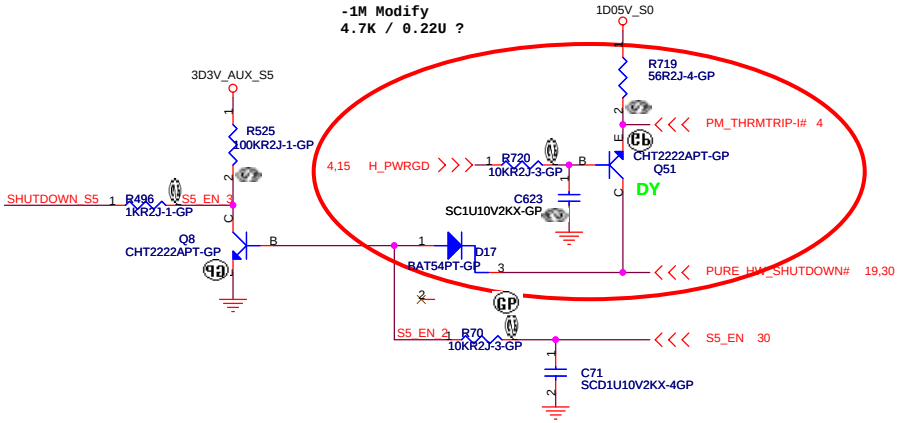
Title: ***BIOS : SPI***

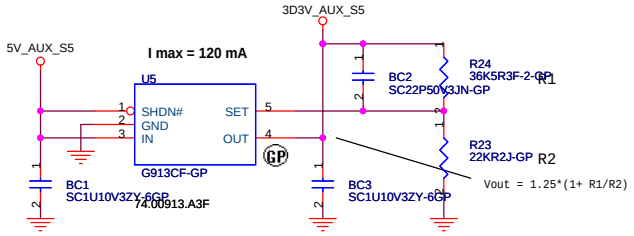
Size	Document Number	Rev
A3	LWG2	SA

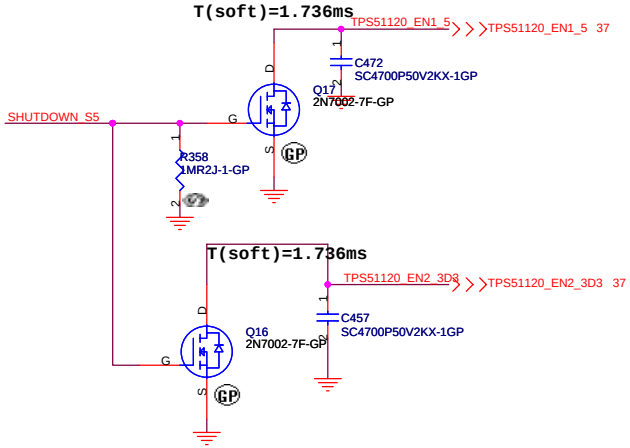
Date: Saturday, June 10, 2006 Sheet 32 of 52

Aux Power

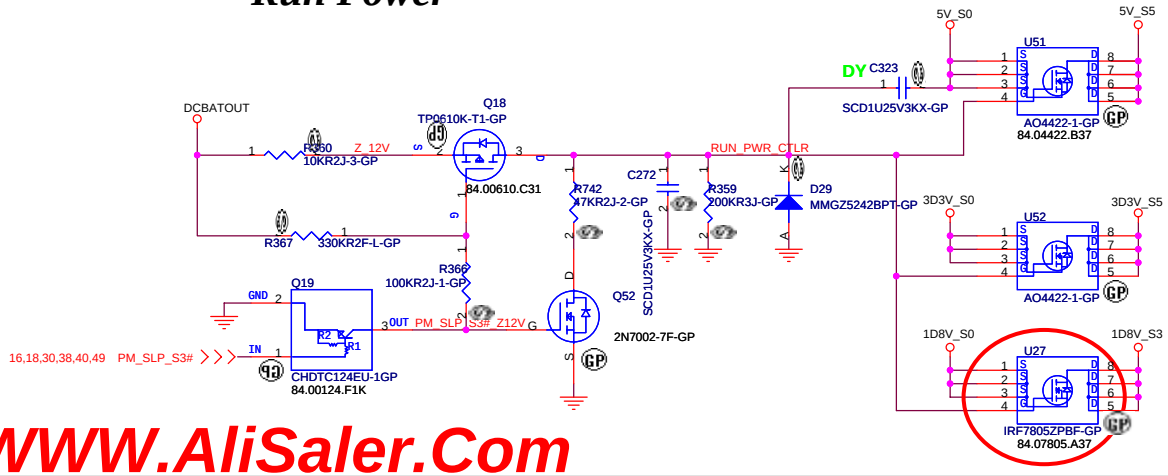


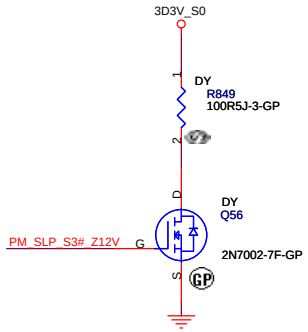






Run Power

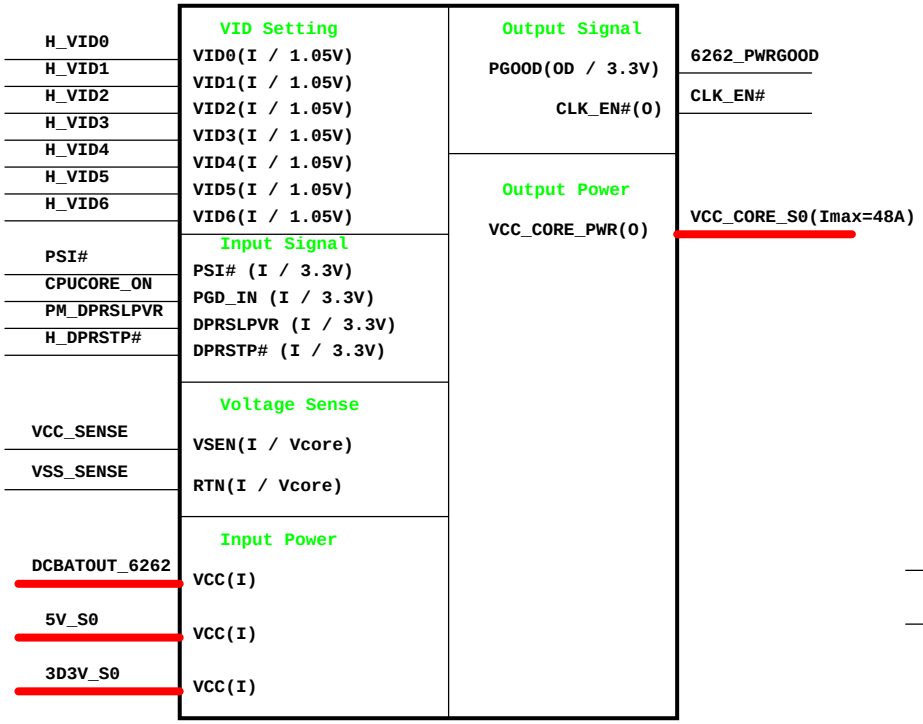




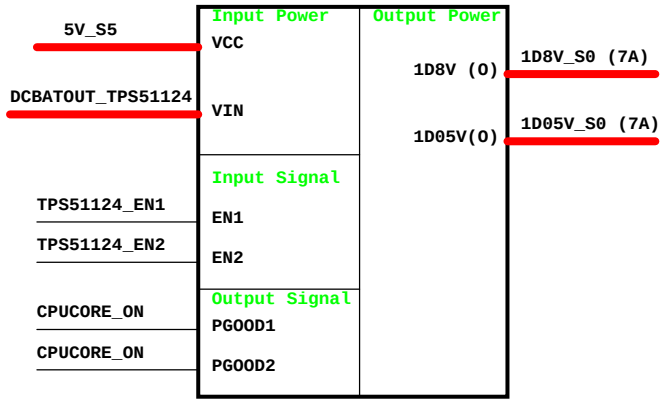
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN and AUX POWER		
Size: A3	Document Number: LWG2	Rev: SA
Date: Saturday, June 10, 2006	Sheet 33 of 52	

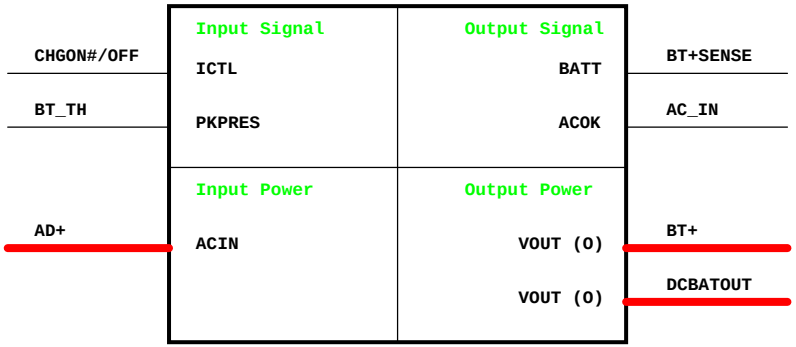
CPU_CORE
Intersil ISL6262



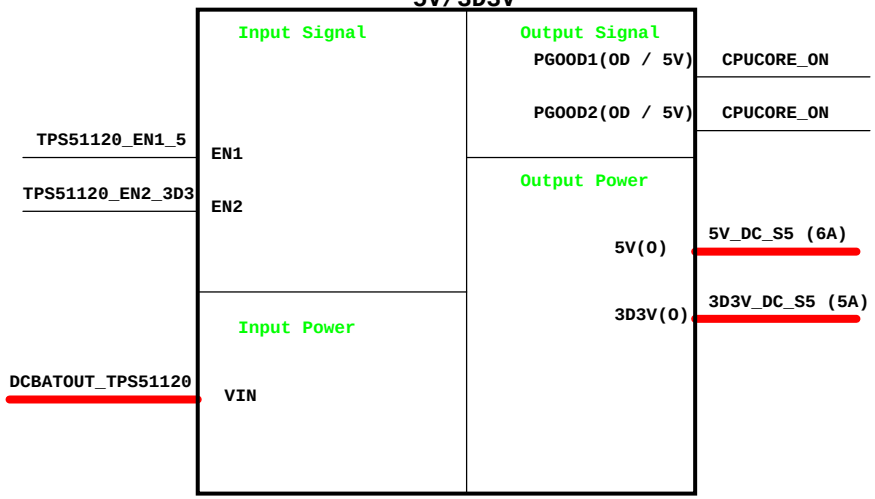
TPS51124
1D8V/1D05V



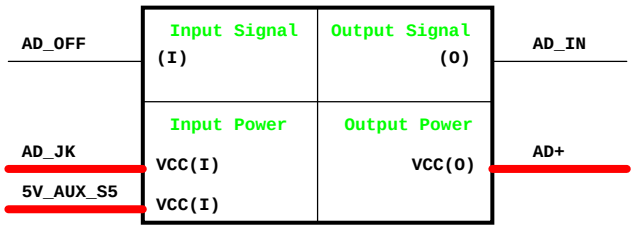
Charger Max8725



TPS51120
5V/3D3V



Adapter



<Variant Name>

緯創資通 **Wistron Corporation**
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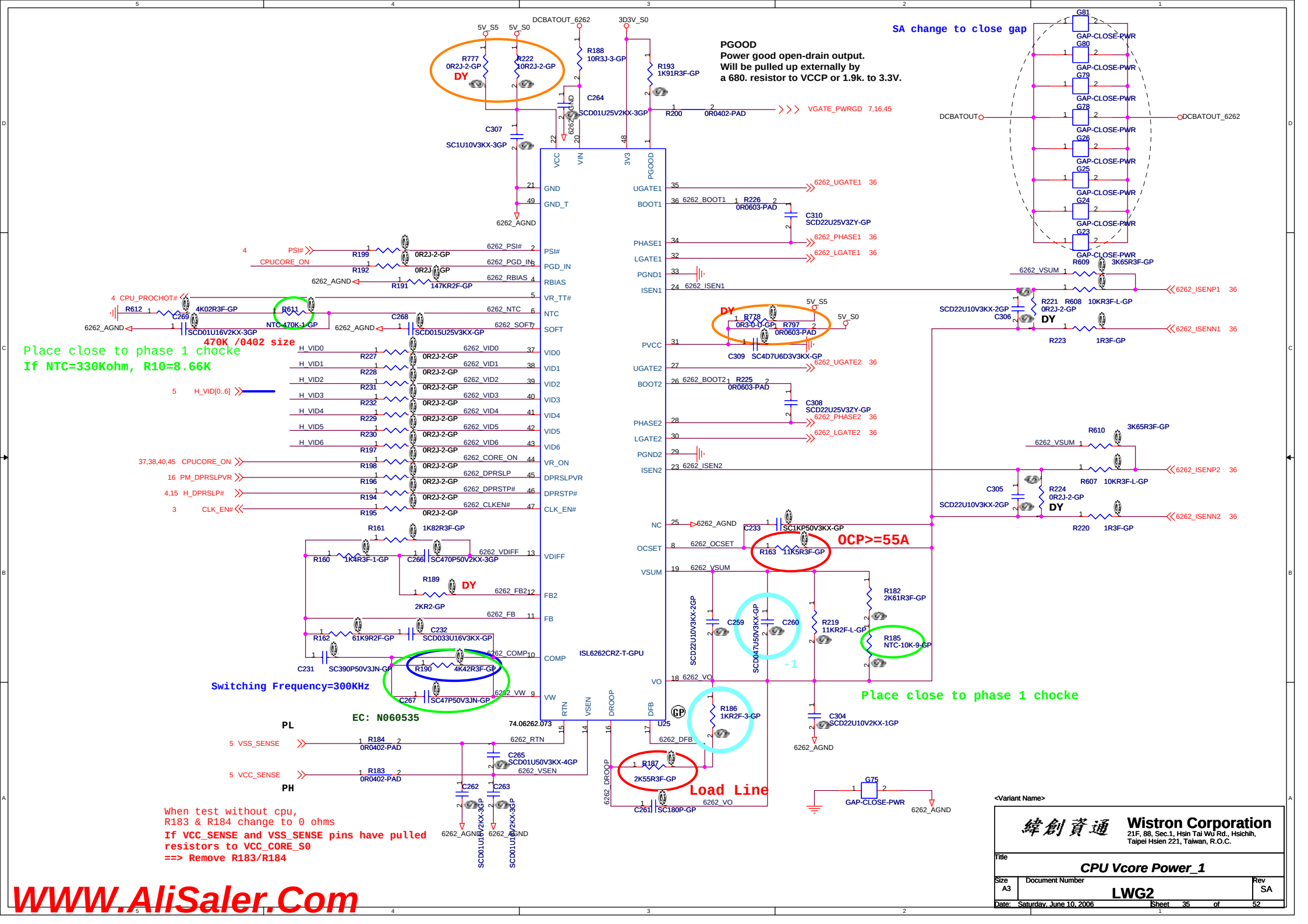
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 34 of 52



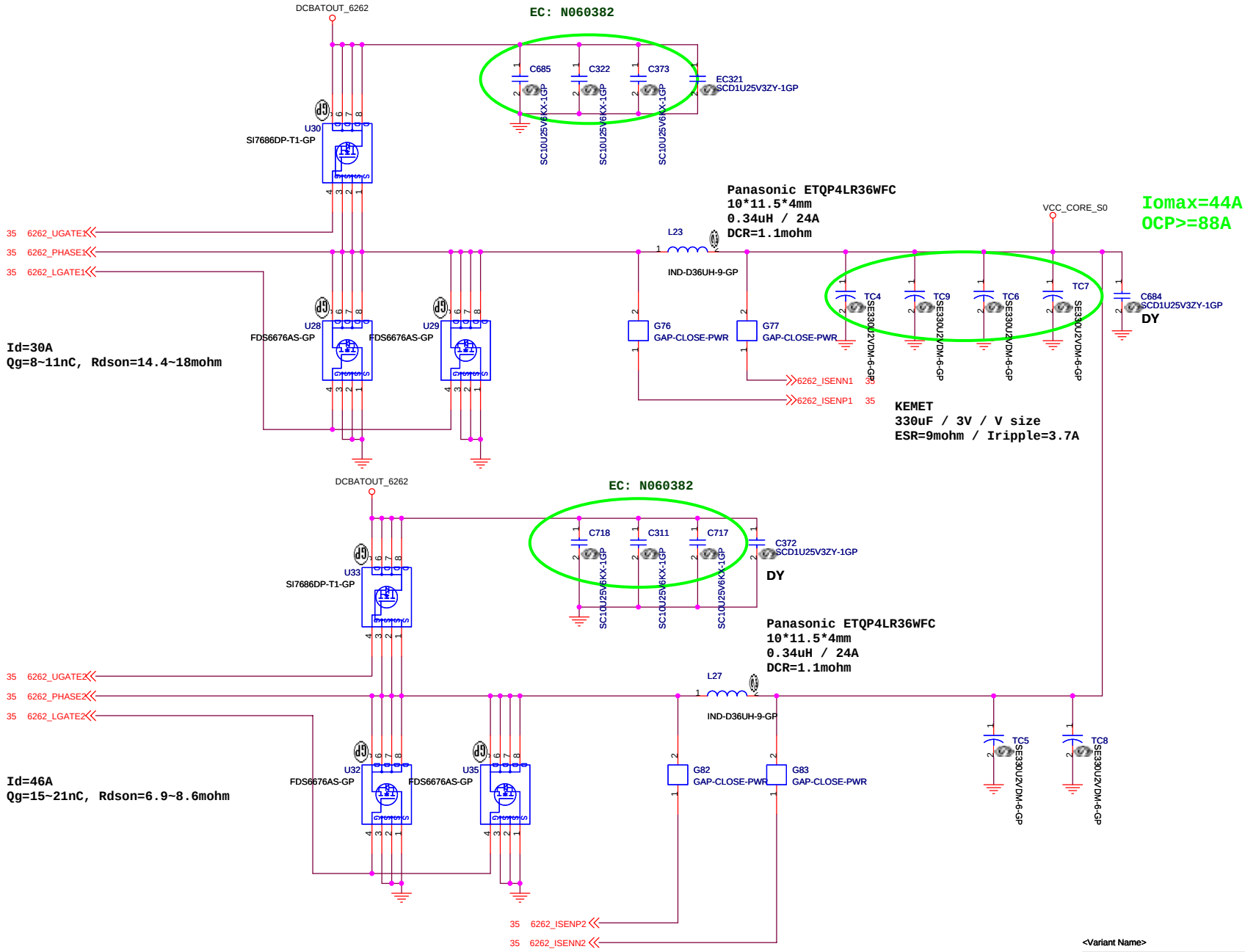
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 35 of 52

<Variant Name>



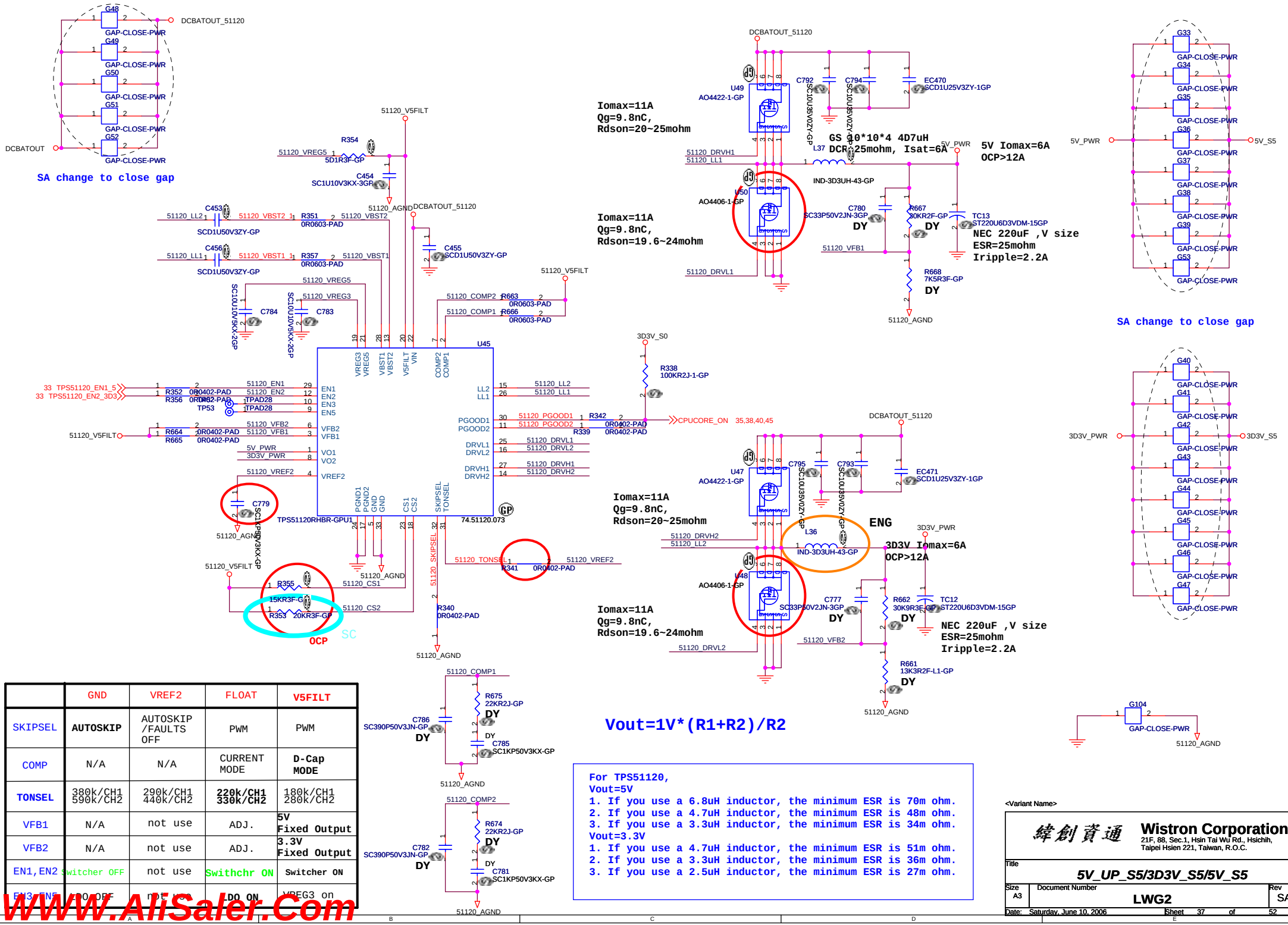
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_2

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 36 of 52



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

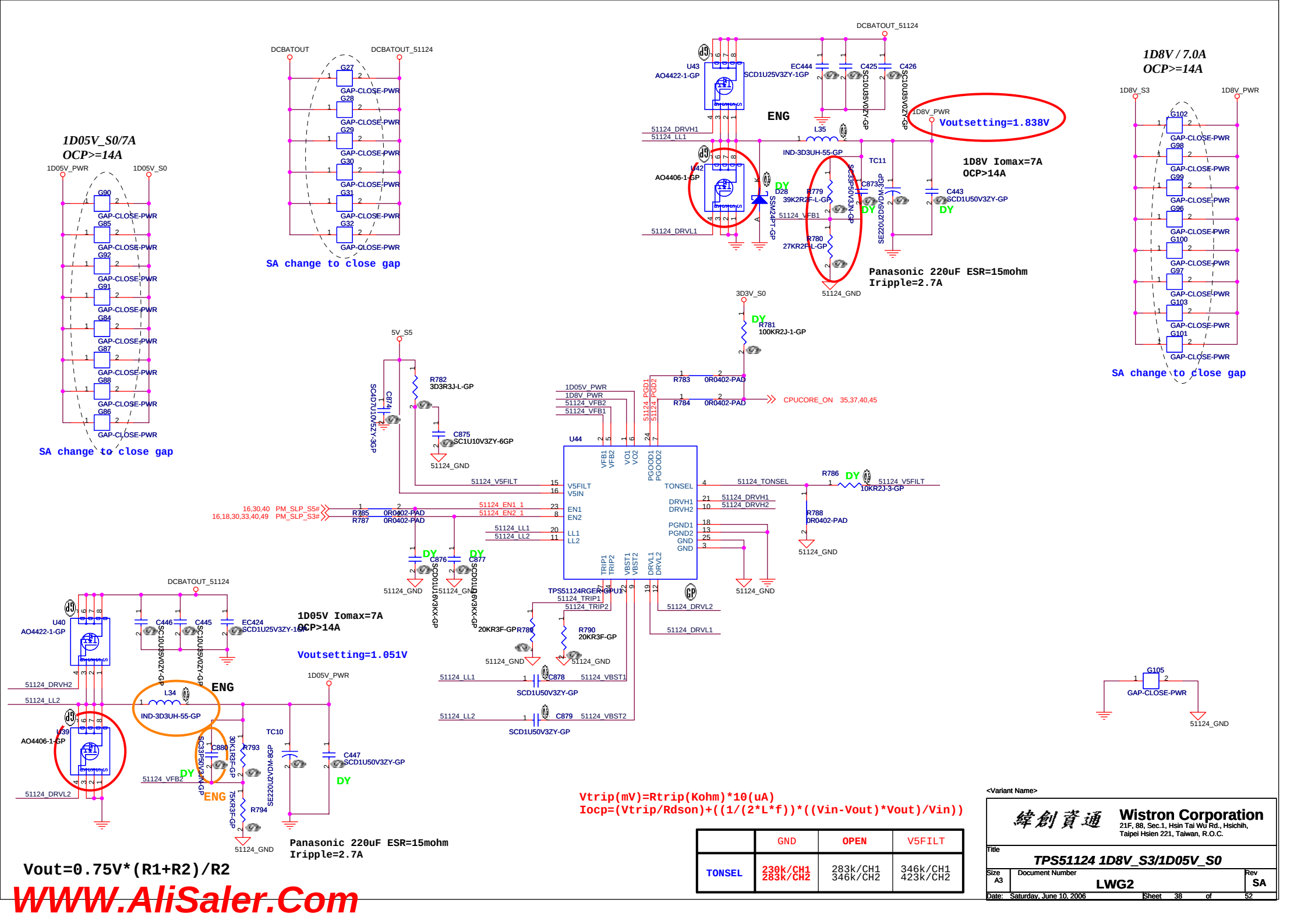
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V_UP_S5/3D3V_S5/5V_S5

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 37 of 52



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

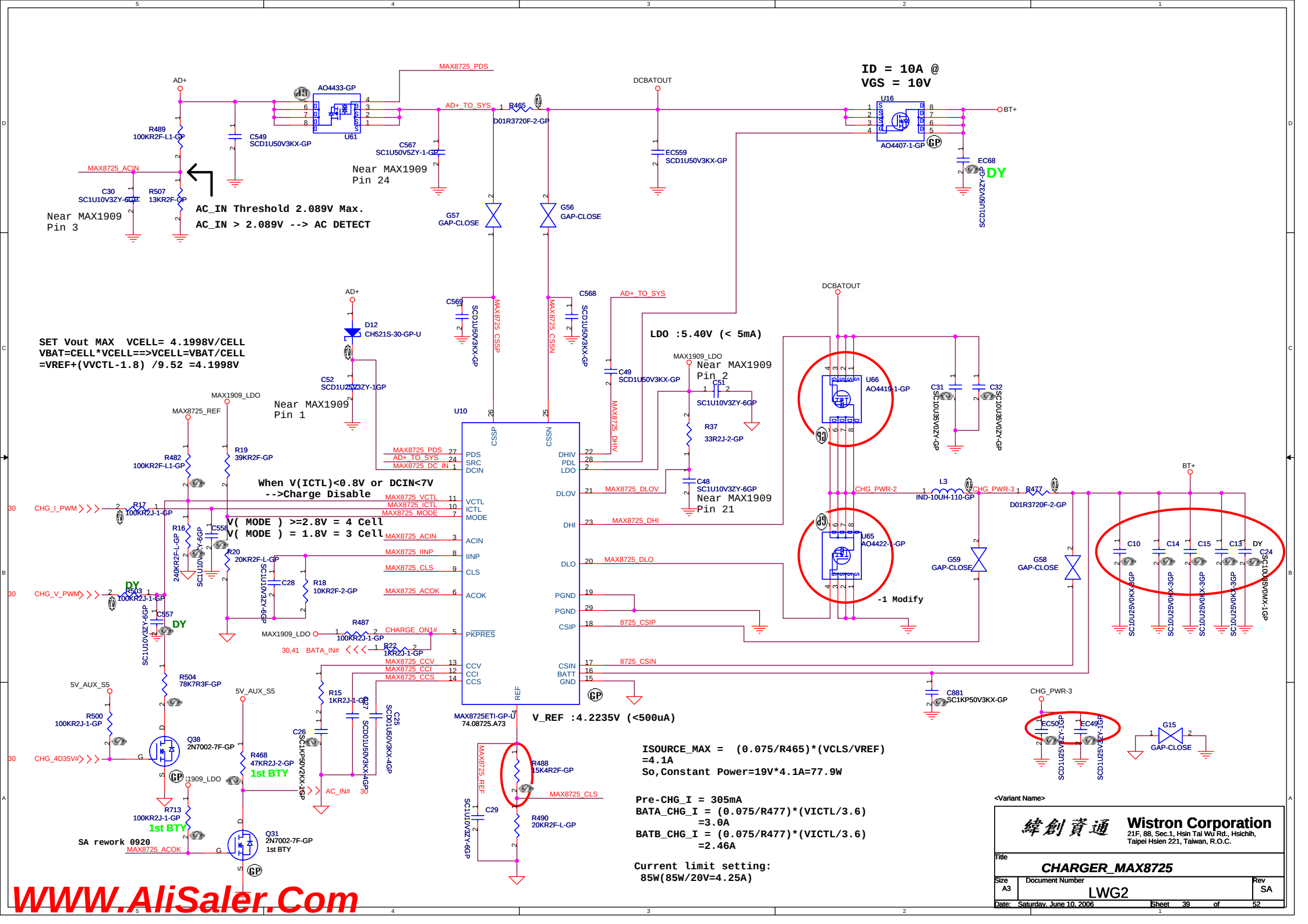
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

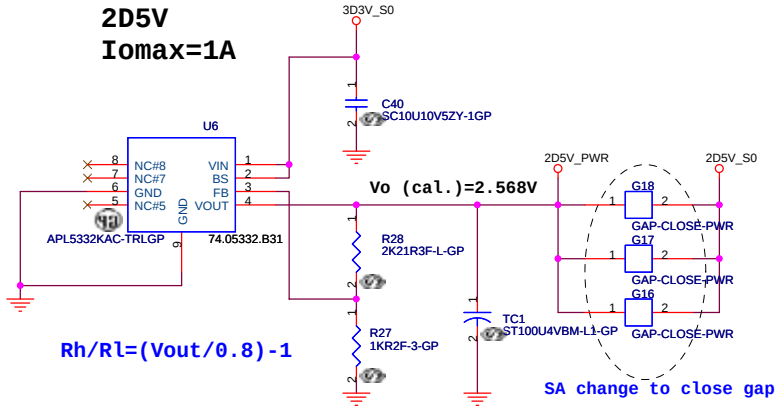
Title: TPS51124 1D8V_S3/1D05V_S0

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 38 of 52


ID = 10A @
VGS = 10V
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
Near MAX1909 Pin 3
Near MAX1909 Pin 24
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
LDO :5.40V (< 5mA)
Near MAX1909 Pin 1
Near MAX1909 Pin 2
Near MAX1909 Pin 21
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
-1 Modify
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/R465)*(VCLS/VREF)
=4.1A
So,Constant Power=19V*4.1A=77.9W
Pre-CHG_I = 305mA
BATA_CHG_I = (0.075/R477)*(VICTL/3.6)
=3.0A
BATB_CHG_I = (0.075/R477)*(VICTL/3.6)
=2.46A
Current limit setting:
85W(85W/20V=4.25A)
SA rework 0920
1st BTY
DY
AO4433-GP
AO4407-1-GP
D01R3720F-2-GP
CH521S-30-GP-U
AO4415-1-GP
AO4422-1-GP
IND-10UH-110-GP
MAX8725ETI-GP-U
74.08725.A73
2N7002-7F-GP
GAP-CLOSE
MAX8725_PDS
MAX8725_ACIN
MAX8725_REF
MAX1909_LDO
MAX8725_DLOV
MAX8725_DHI
MAX8725_DLO
MAX8725_CSIP
MAX8725_CSIN
MAX8725_VCTL
MAX8725_ICTL
MAX8725_MODE
MAX8725_IINP
MAX8725_CLS
MAX8725_ACOK
MAX8725_CCV
MAX8725_CCI
MAX8725_CCS
CHARGE_ON1#
CHG_I_PWM
CHG_V_PWM
CHG_4D35V#
AC_IN#
BATA_IN#
CHG_PWR-2
CHG_PWR-3
DCBATOUT
BT+
AD+
AD+_TO_SYS
MAX8725_DC_IN
MAX8725_CSSP
MAX8725_CSSN
MAX8725_DHIV
MAX8725_REF
5V_AUX_S5
U10
U16
U61
U65
U66
R489 100KR2F-L1-GP
R507 13KR2F-GP
R465
R37 33R2J-2-GP
R482 100KR2F-L1-GP
R19 39KR2F-GP
R17 100KR2J-1-GP
R16 240KR2F-L-GP
R20 20KR2F-L-GP
R18 10KR2F-2-GP
R503 100KR2J-1-GP
R504 78K7R3F-GP
R487 100KR2J-1-GP
R22 1KR2J-1-GP
R15 1KR2J-1-GP
R500 100KR2J-1-GP
R468 47KR2J-2-GP
R713 100KR2J-1-GP
R488 15K4R2F-GP
R490 20KR2F-L-GP
R477
C30 SC1U10V3ZY-6GP
C549 SCD1U50V3KX-GP
C567 SC1U50V5ZY-1-GP
C559 SCD1U50V3KX-GP
EC68 SCD1U50V3ZY-GP
C569 SCD1U50V3KX-GP
C568 SCD1U50V3KX-GP
C49 SCD1U50V3KX-GP
C51 SC1U10V3ZY-6GP
C48 SC1U10V3ZY-6GP
C52 SCD1U25V3ZY-1GP
C31 SC10U35V0ZY-GP
C32 SC10U35V0ZY-GP
C10 SC10U25V0KX-3GP
C14 SC10U25V0KX-3GP
C15 SC10U25V0KX-3GP
C13 SC10U25V0KX-3GP
C24 SC10U35V0MX-1GP
C558 SC1U10V3ZY-6GP
C28 SC1U10V3ZY-6GP
C557 SC1U10V3ZY-6GP
C27 SCD01U50V3KX-4GP
C25 SCD01U50V3KX-4GP
C26 SC1KP50V2KX-1GP
C29 SC1U10V3ZY-6GP
C881 SC1KP50V3KX-GP
EC50 SCD1U25V2ZY-1GP
EC49 SCD1U25V2ZY-1GP
G57 GAP-CLOSE
G56 GAP-CLOSE
G59 GAP-CLOSE
G58 GAP-CLOSE
G15 GAP-CLOSE
Q38 2N7002-7F-GP
Q31 2N7002-7F-GP
1st BTY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER_MAX8725
LWG2
SA
Saturday, June 10, 2006
39
52
WWW.AliSaler.Com

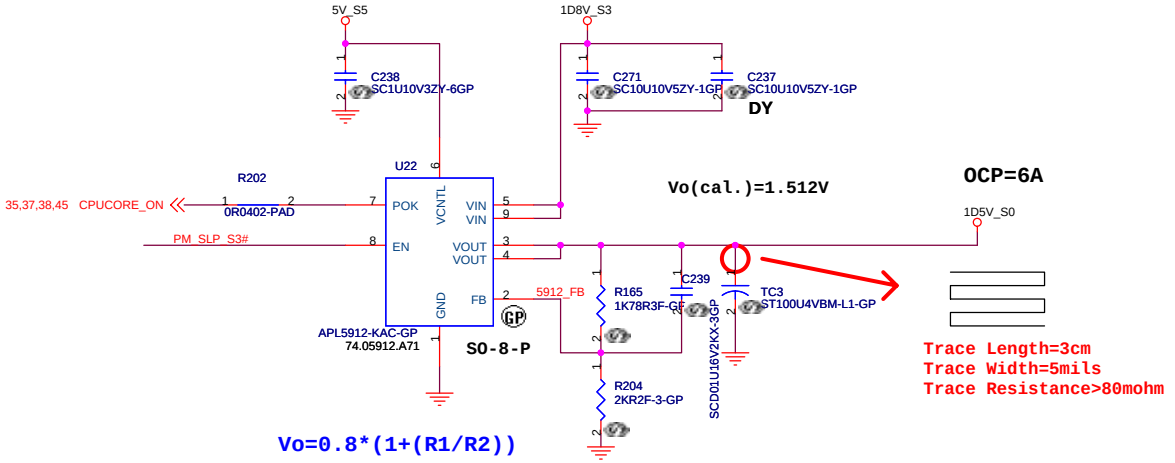
2D5V
Iomax=1A



Rh/Rl=(Vout/0.8)-1

SA change to close gap

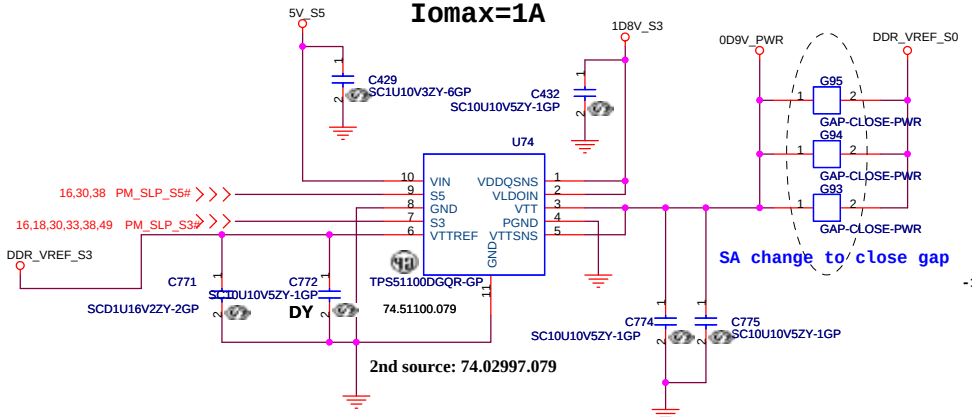
1D5V_S0
Iomax=4.0A



Vo=0.8*(1+(R1/R2))

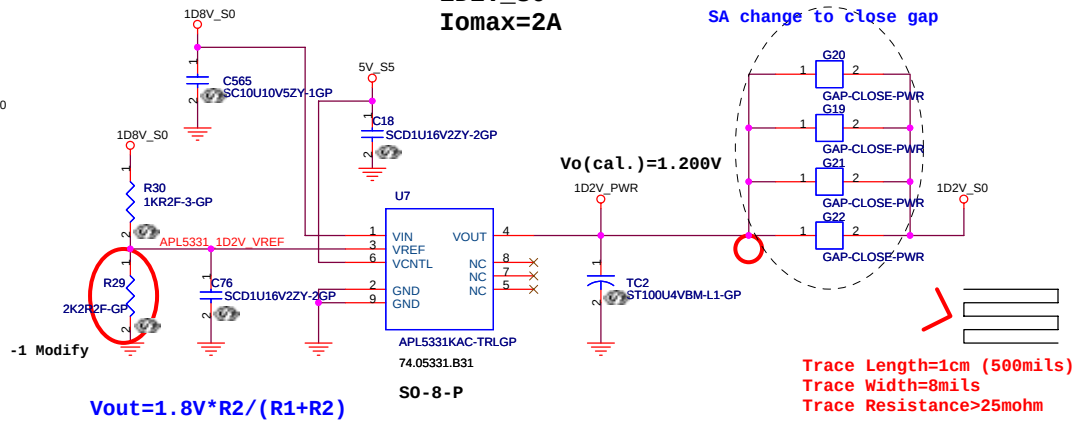
Trace Length=3cm
Trace Width=5mils
Trace Resistance>80mohm

0D9V
Iomax=1A



SA change to close gap

1D2V_S0
Iomax=2A



Vout=1.8V*R2/(R1+R2)

Trace Length=1cm (500mils)
Trace Width=8mils
Trace Resistance>25mohm

<Variant Name>

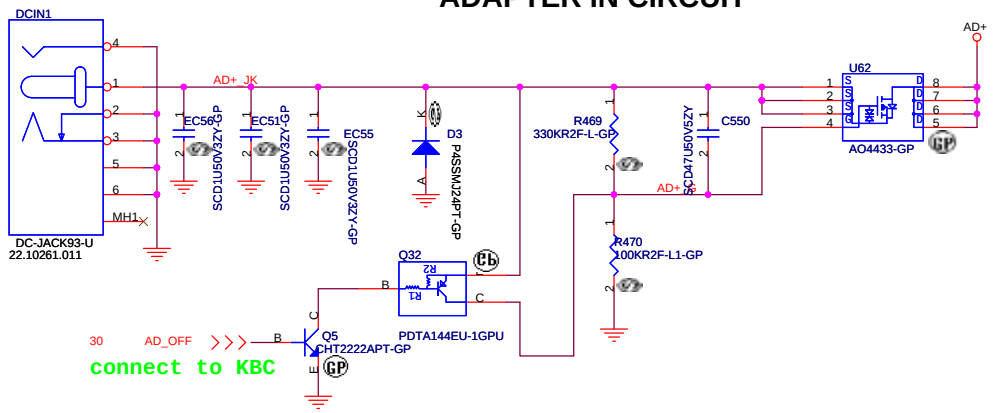
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D9V/1D2V/1D5V/2D5V

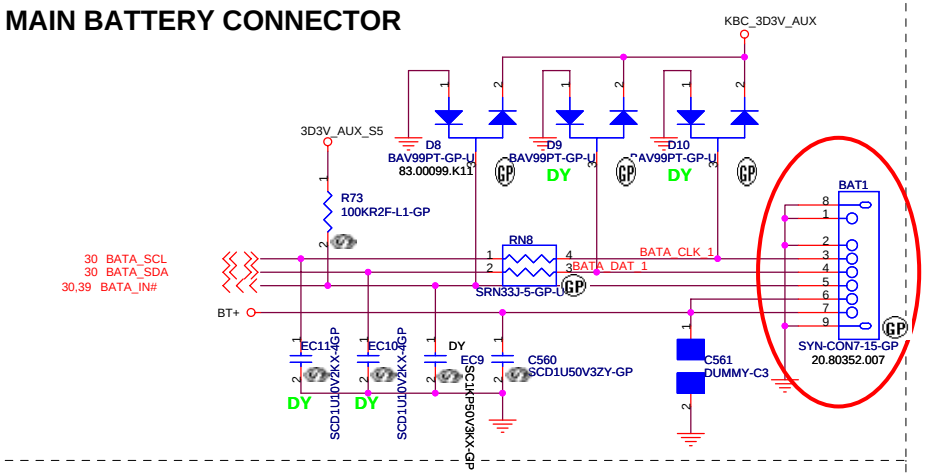
Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 40 of 52

ADAPTER IN CIRCUIT



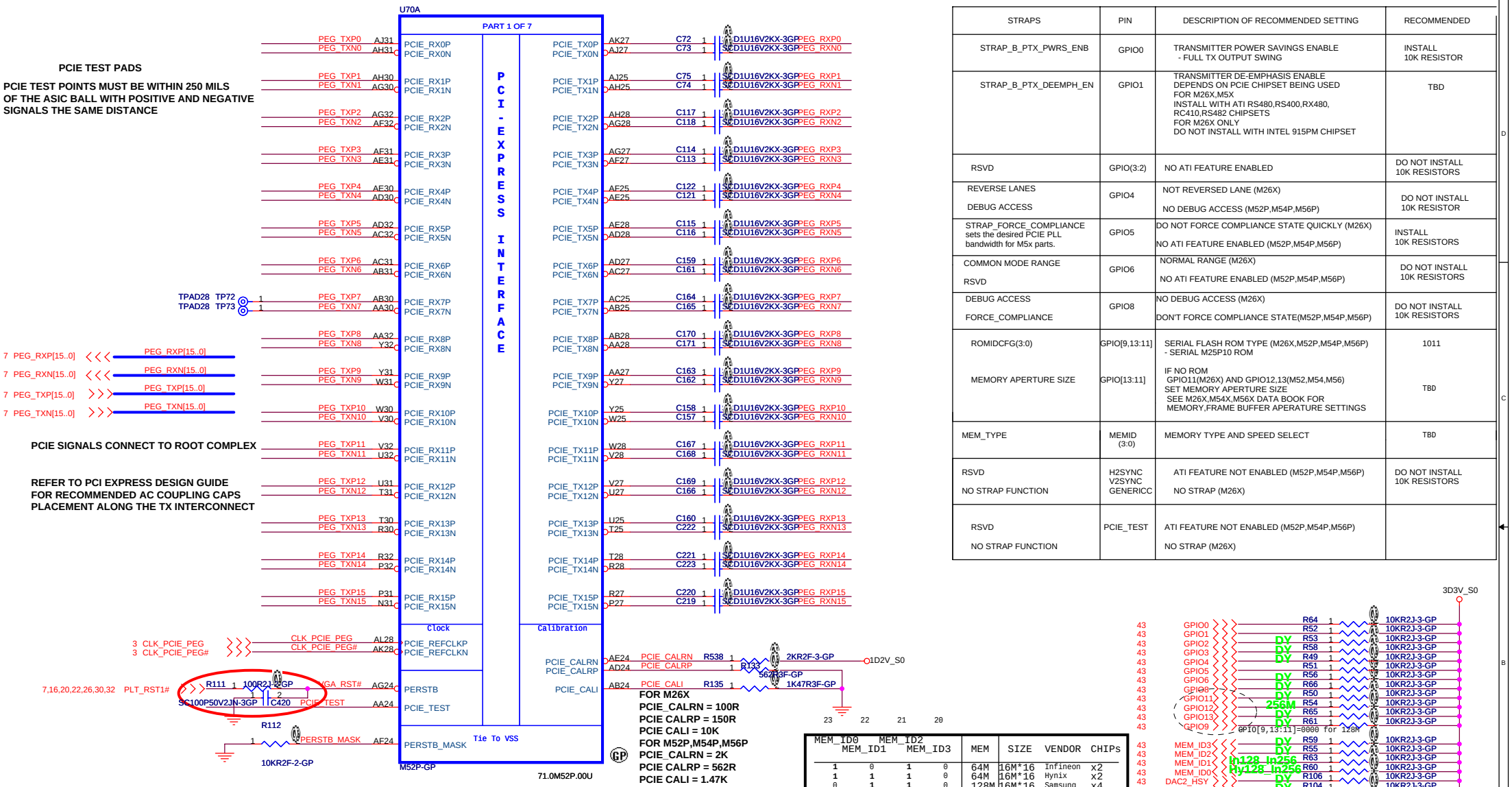
MAIN BATTERY CONNECTOR



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BATT CONN***	
Size A3	Document Number LWG2	Rev SA
Date: Saturday, June 10, 2006	Sheet 41 of 52	



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO[9,13:11] GPIO[13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	1011 TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPS
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

VGA THERMAL SENSOR

Place near GPU

IT IS REQUIRED TO DESIGN IN A THERMAL SENSOR
TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC

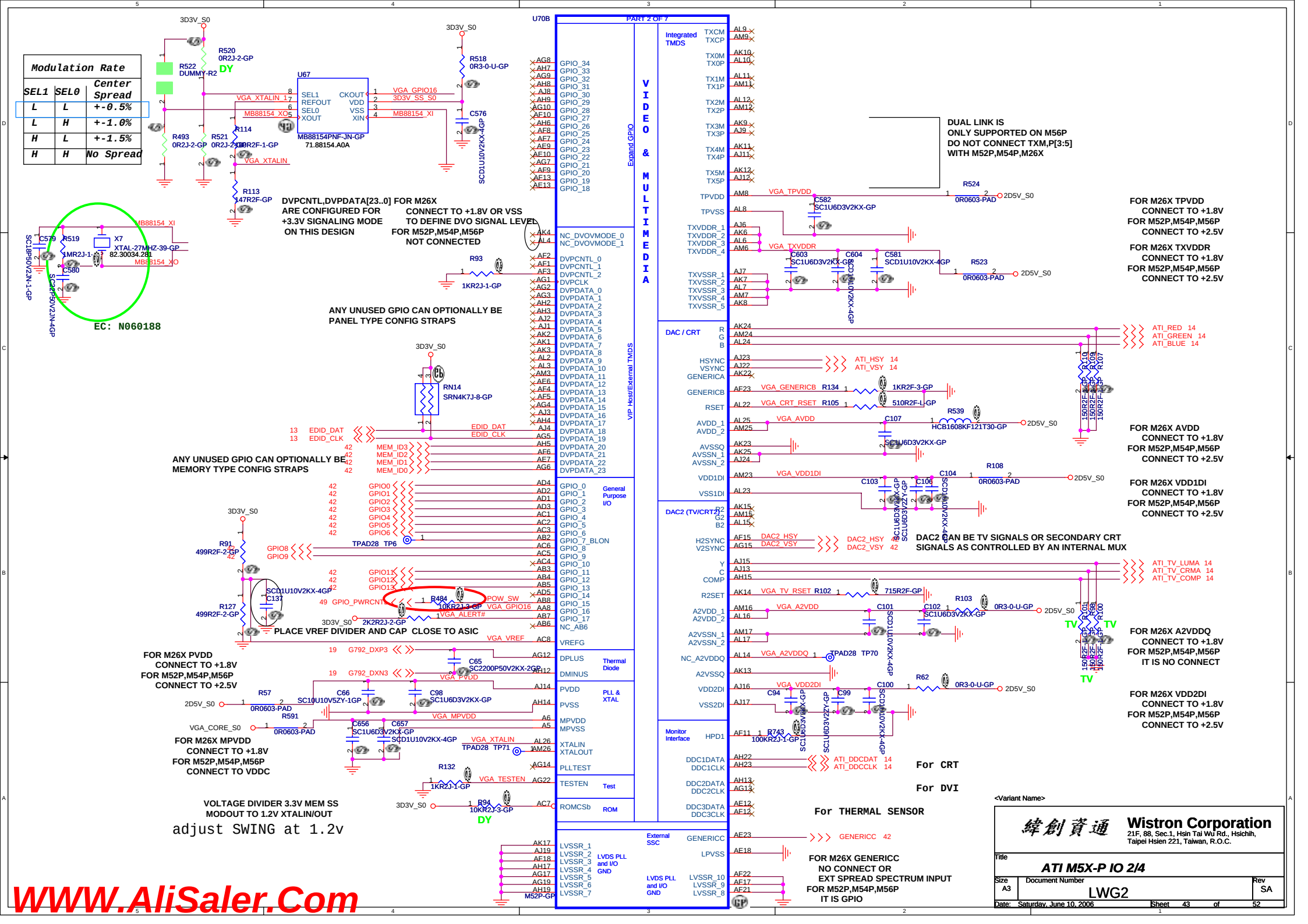
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P PCIE 1/4

Size: A3 | Document Number: LWG2 | Rev: SA

Date: Saturday, June 10, 2006 | Sheet 42 of 52


Modulation Rate
SEL1 SEL0 Center Spread
L L +-0.5%
L H +-1.0%
H L +-1.5%
H H No Spread
U70B
PART 2 OF 7
VIDEO & MULTIMEDIA
Expand GPIO
VIP Host/External TMDS
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
External SSC
LVDS PLL and I/O GND
DUAL LINK IS ONLY SUPPORTED ON M56P DO NOT CONNECT TXM,P[3:5] WITH M52P,M54P,M26X
DVPCNTL,DVPDATA[23..0] FOR M26X ARE CONFIGURED FOR +3.3V SIGNALING MODE ON THIS DESIGN
CONNECT TO +1.8V OR VSS TO DEFINE DVO SIGNAL LEVEL FOR M52P,M54P,M56P NOT CONNECTED
ANY UNUSED GPIO CAN OPTIONALLY BE PANEL TYPE CONFIG STRAPS
ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC
FOR M26X PVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X MPVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO VDDC
VOLTAGE DIVIDER 3.3V MEM SS MODOUT TO 1.2V XTALIN/OUT
adjust SWING at 1.2v
FOR M26X TPVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X TXVDDR CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X AVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X VDD1DI CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
DAC2 CAN BE TV SIGNALS OR SECONDARY CRT SIGNALS AS CONTROLLED BY AN INTERNAL MUX
FOR M26X A2VDDQ CONNECT TO +1.8V FOR M52P,M54P,M56P IT IS NO CONNECT
FOR M26X VDD2DI CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
For CRT
For DVI
For THERMAL SENSOR
FOR M26X GENERICC NO CONNECT OR EXT SPREAD SPECTRUM INPUT FOR M52P,M54P,M56P IT IS GPIO
EC: N060188
M52P-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI M5X-P IO 2/4
LWG2
Saturday, June 10, 2006
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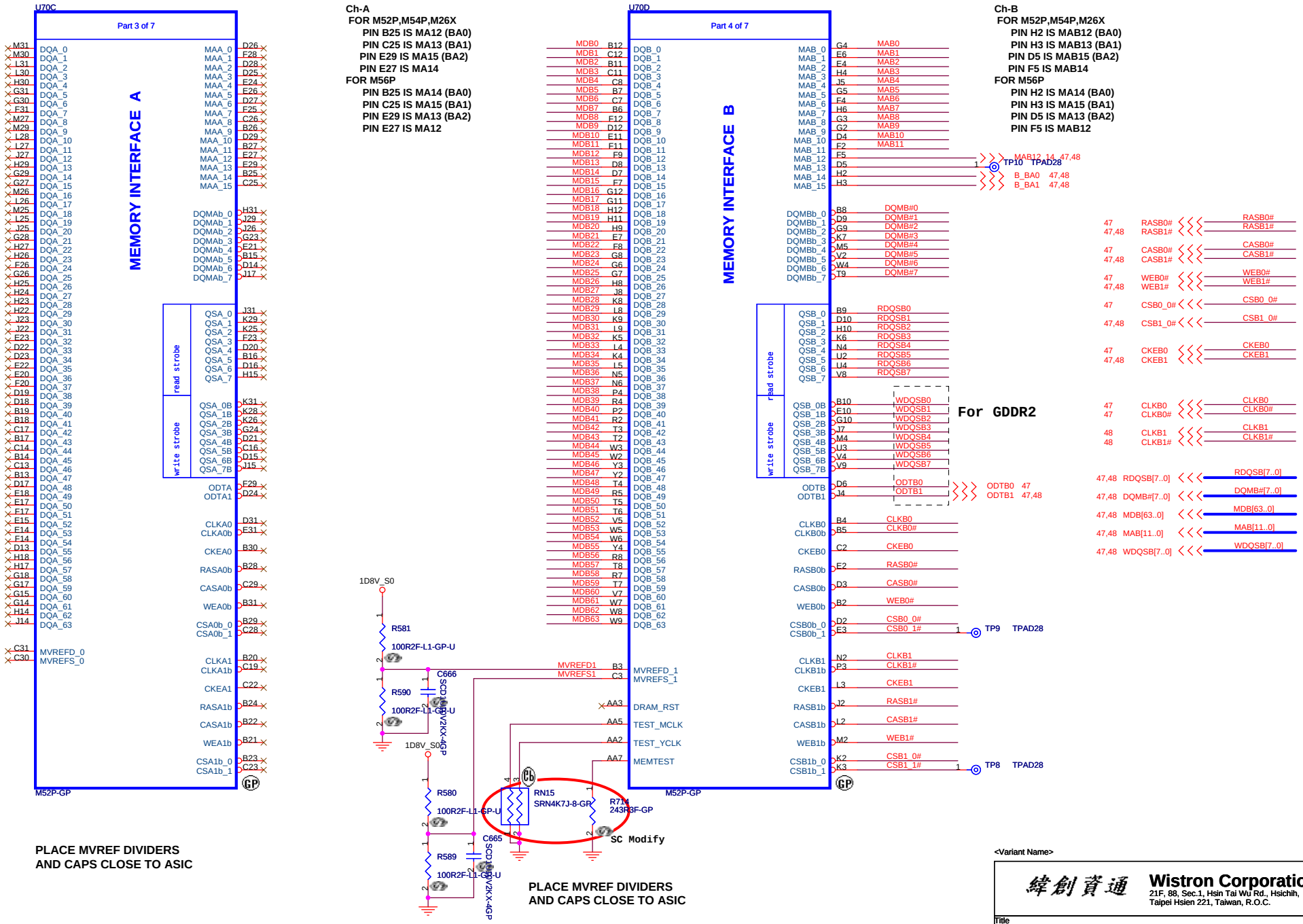

<Variant Name>

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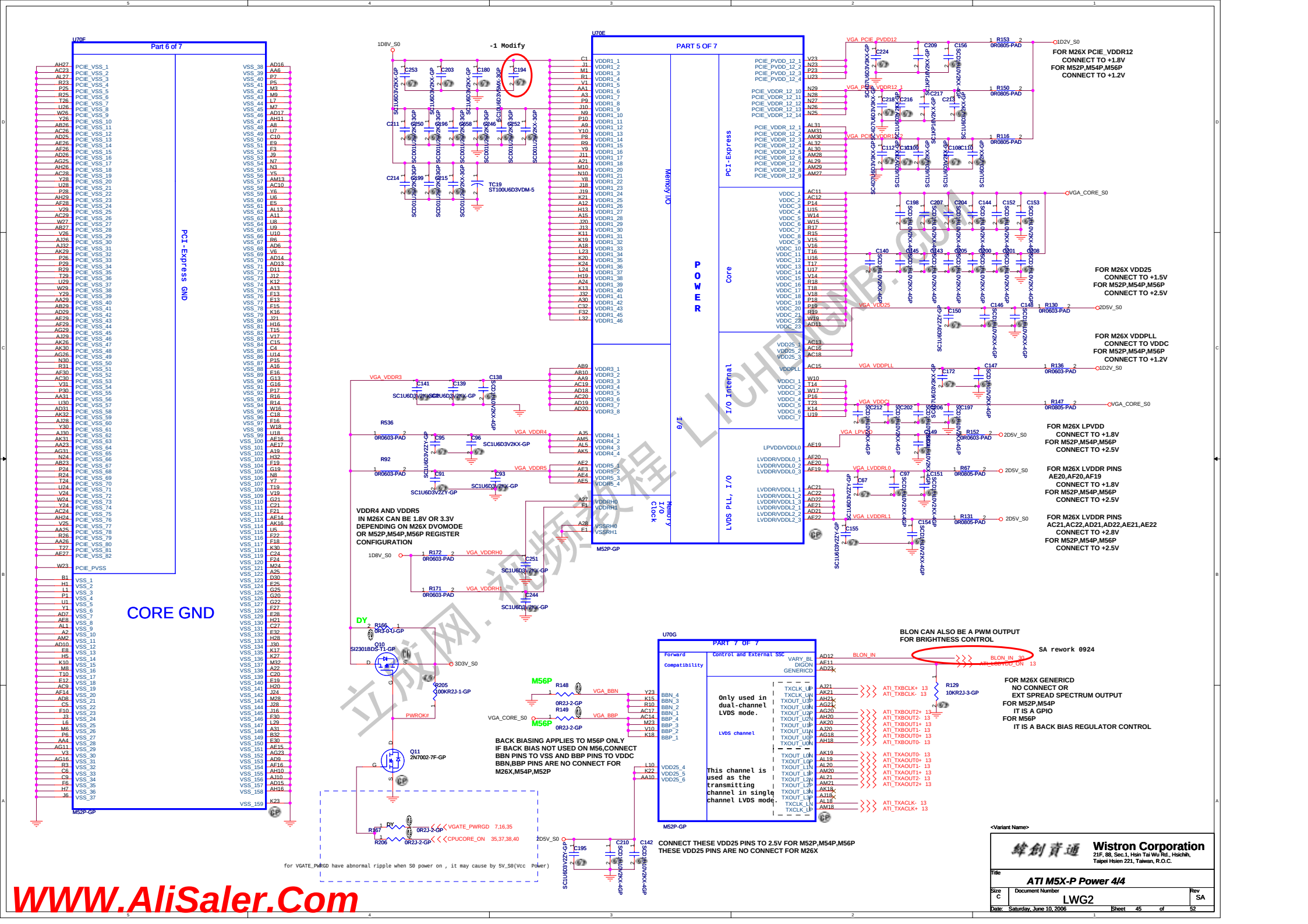
Taipei Hsien 221, Taiwan, R.O.C.

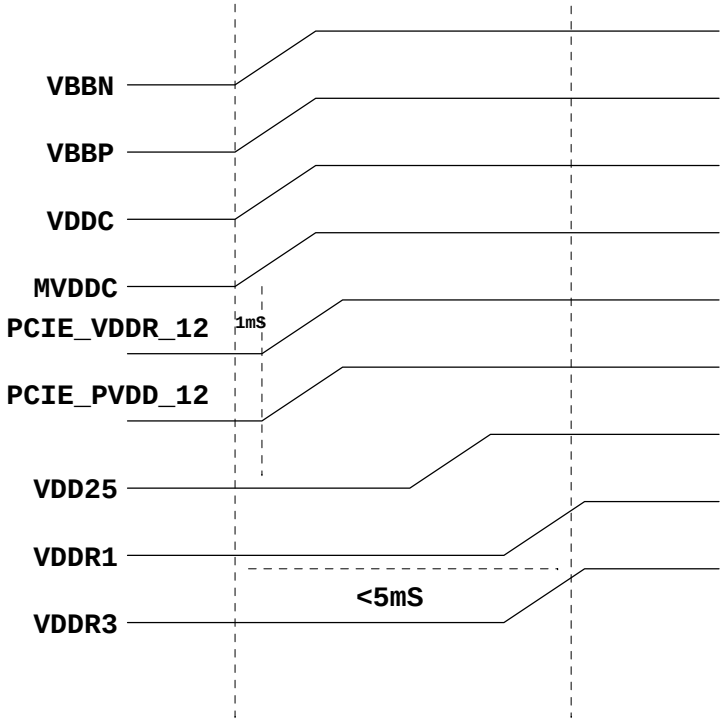
Title: **ATI M5X-P MEM 3/4**

Size	Document Number	Rev
A3	LWG2	SA

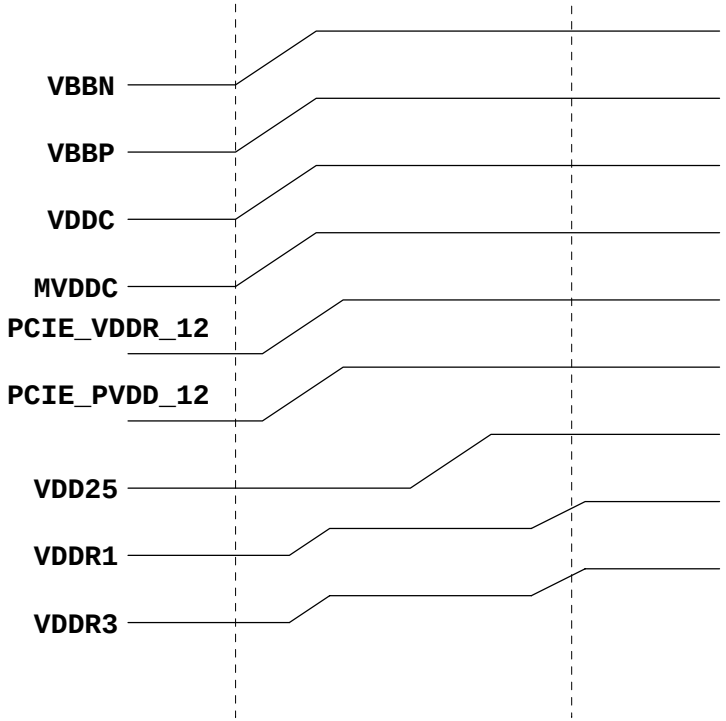
Date: Saturday, June 10, 2006 Sheet 44 of 52



Ideal Power Up Sequence



Real Power Up Sequence



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC22D1U16V5ZY	0.22uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

General Guidelines:

- **BBN and BBP must ramp up before or at the same time as VDDC but not after.**
- **VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).**
- **All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).**
- **VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.**
- **The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.**

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

<Variant Name>

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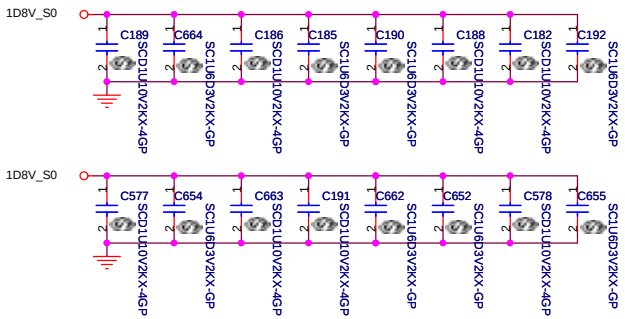
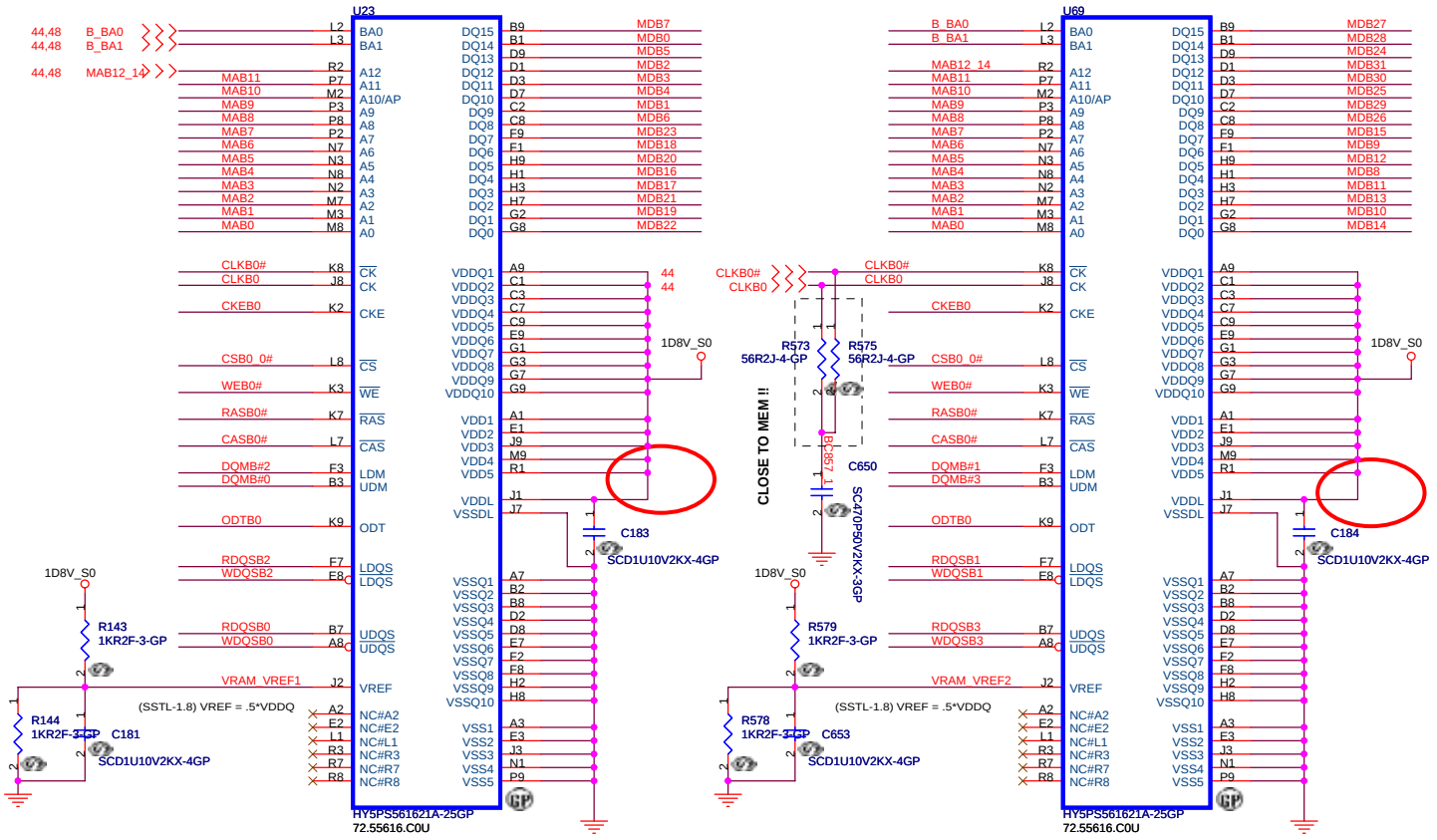
Title: ATI M5X-P POWER SEQUENCE

Size: A3 | Document Number: LWG2 | Rev: SA

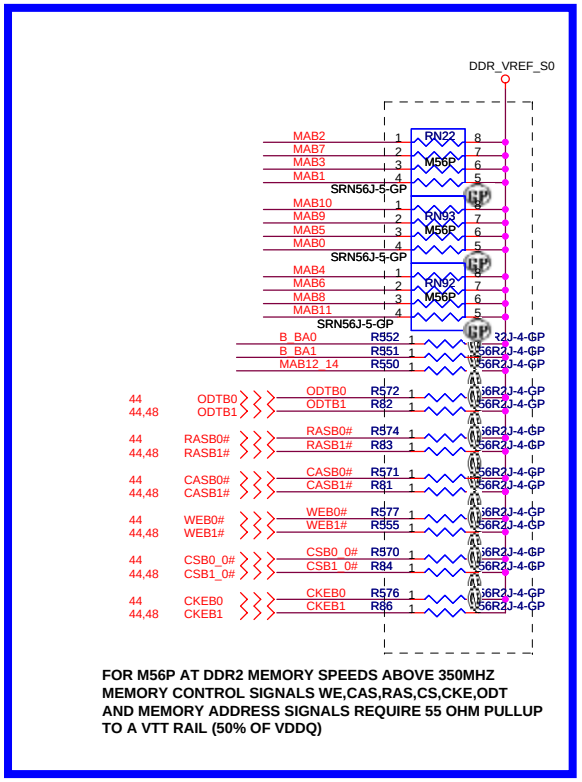
Date: Saturday, June 10, 2006 | Sheet 46 of 52

CHAN B DDR2 84BGA 32MX16 MEMORY

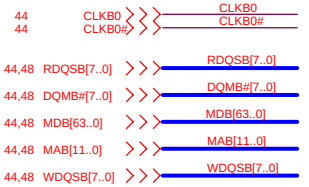




72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 350Mhz) Hynix-128M
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M*16, 350Mhz) Infineon-128M
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M*16, 400Mhz) Infineon-256M



FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)



<Variant Name>

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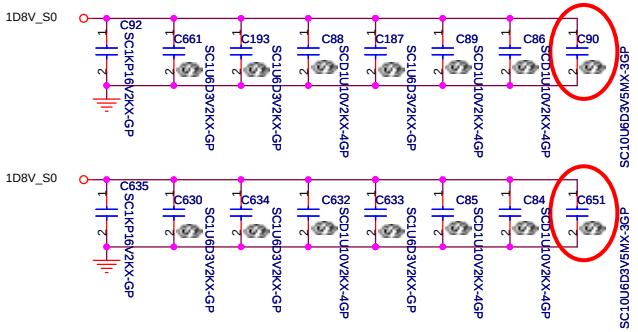
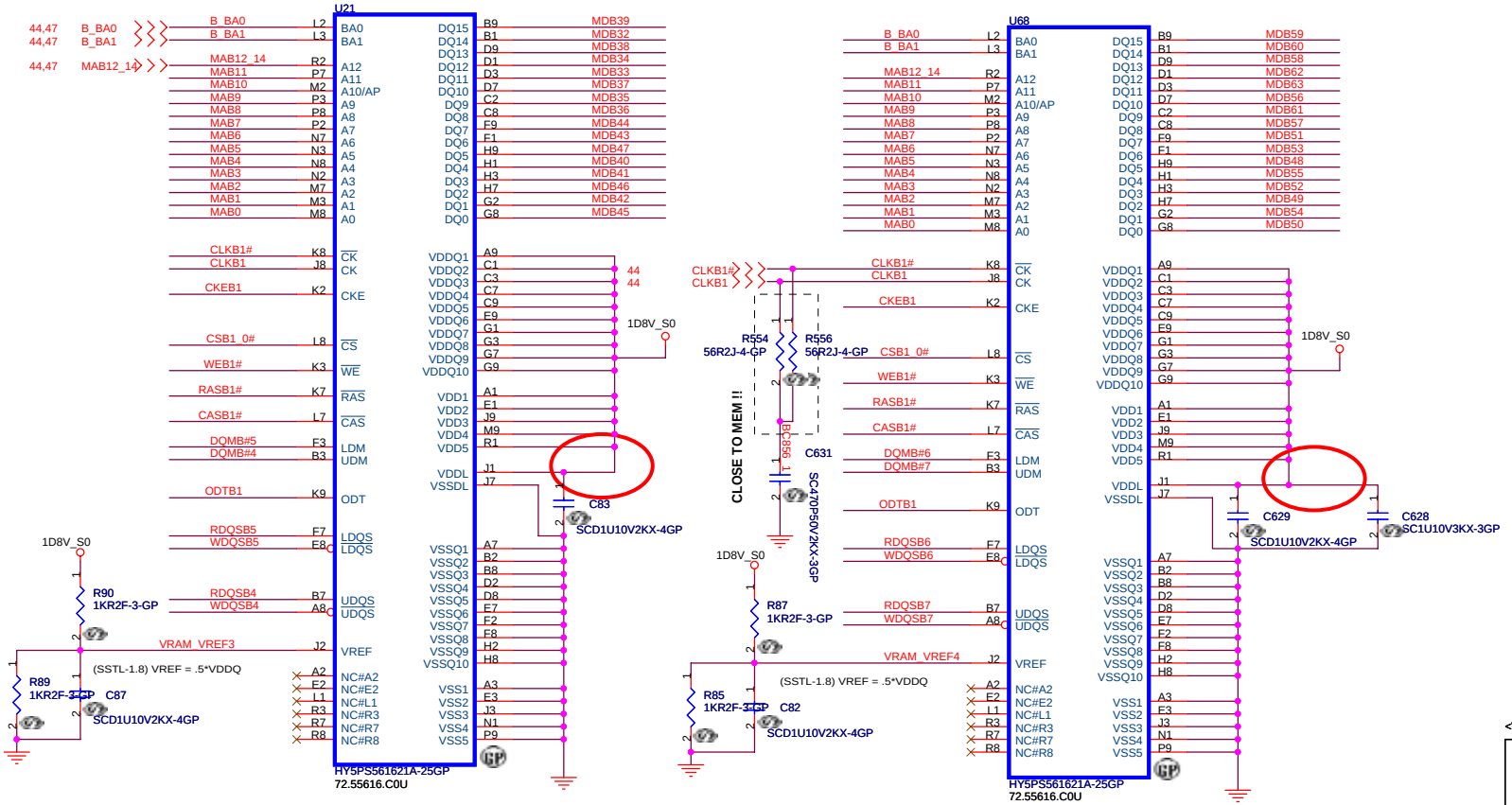
Title: ***VRAM 1/2***

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 47 of 52

-1 Modify





<Variant Name>

緯創資通 **Wistron Corporation**
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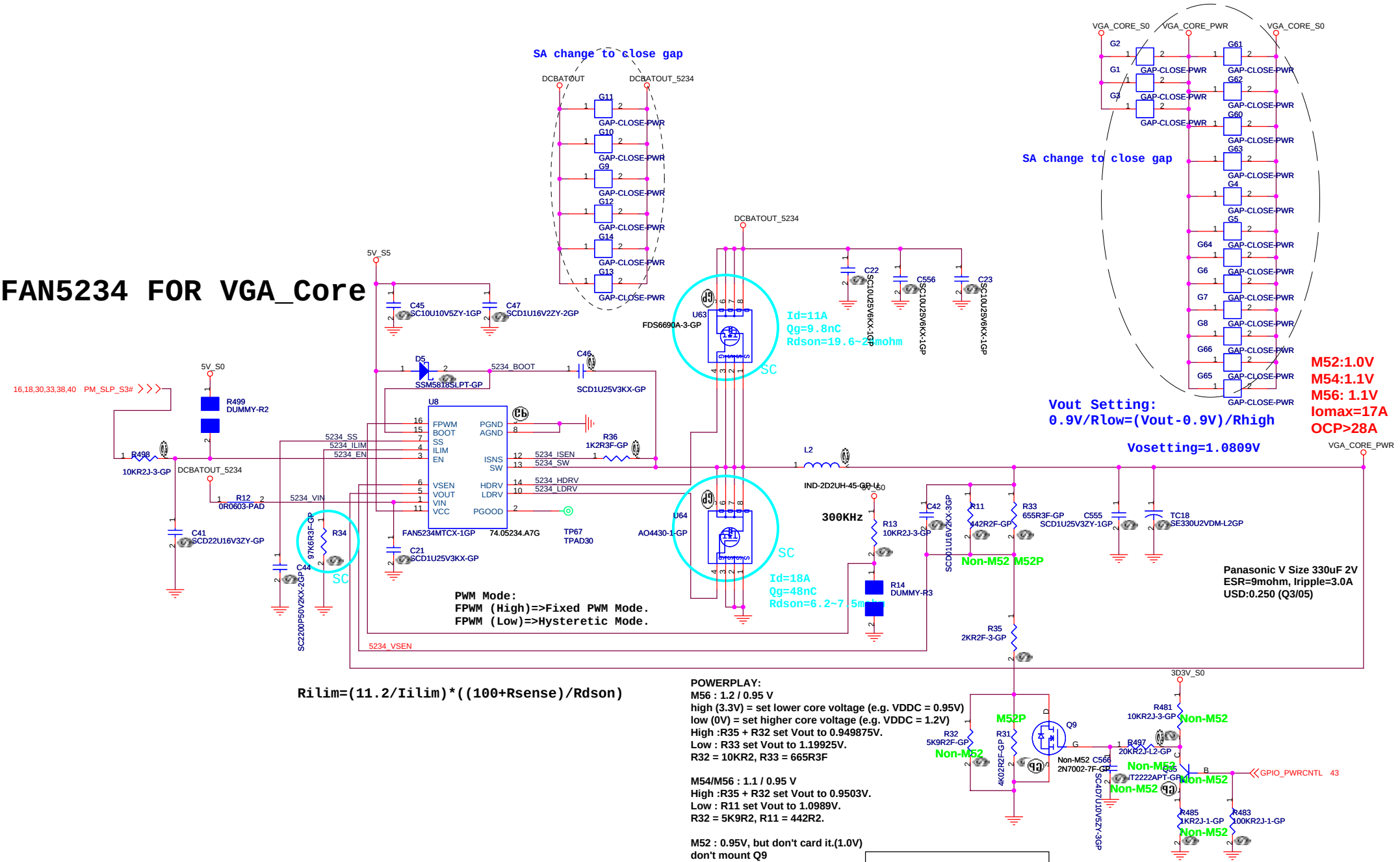
Title: **VRAM 2/2**

Size	Document Number	Rev
A3	LWG2	SA

Date: Saturday, June 10, 2006 Sheet 48 of 52

FAN5234 FOR VGA_Core



POWERPLAY:
M56 : 1.2 / 0.95 V
high (3.3V) = set lower core voltage (e.g. VDDC = 0.95V)
low (0V) = set higher core voltage (e.g. VDDC = 1.2V)
High :R35 + R32 set Vout to 0.949875V.
Low : R33 set Vout to 1.19925V.
R32 = 10KR2, R33 = 665R3F

M54/M56 : 1.1 / 0.95 V
High :R35 + R32 set Vout to 0.9503V.
Low : R11 set Vout to 1.0989V.
R32 = 5K9R2, R11 = 442R2.

M52 : 0.95V, but don't card it.(1.0V)
don't mount Q9
R35 + R31 set Vout to 0.9994V.
R31 = 4K02R2, R33 = 655R3.

ATI M5x VGA Core

VGA	Ver.	Normal	PowerPlay
M52	A12	1.0	0.95/1.0
M54	A12	1.1	0.95/0.95
M56		1.2	0.95
	B24	1.1	0.95/0.95

<Variant Name>

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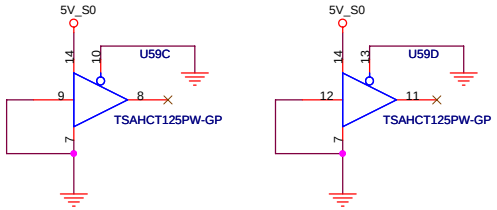
Taipei Hsien 221, Taiwan, R.O.C.

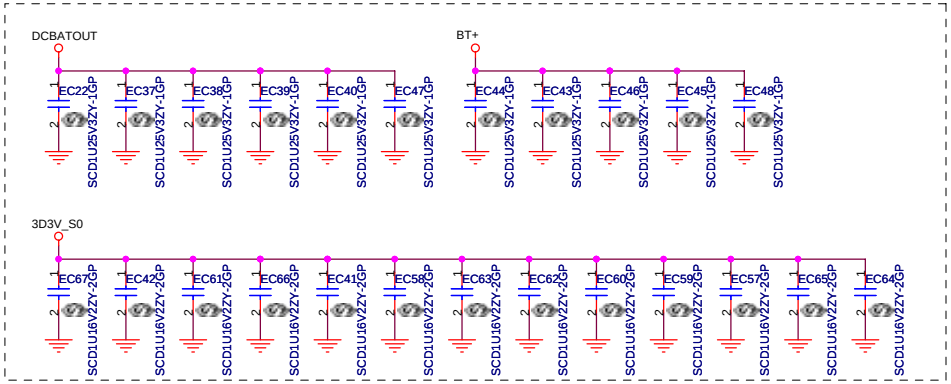
Title: **VGA CORE 1D1V**

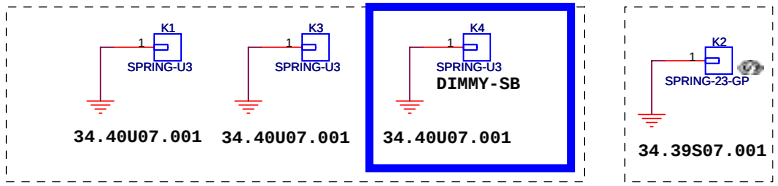
Size	Document Number	Rev
A3	LWG2	SA

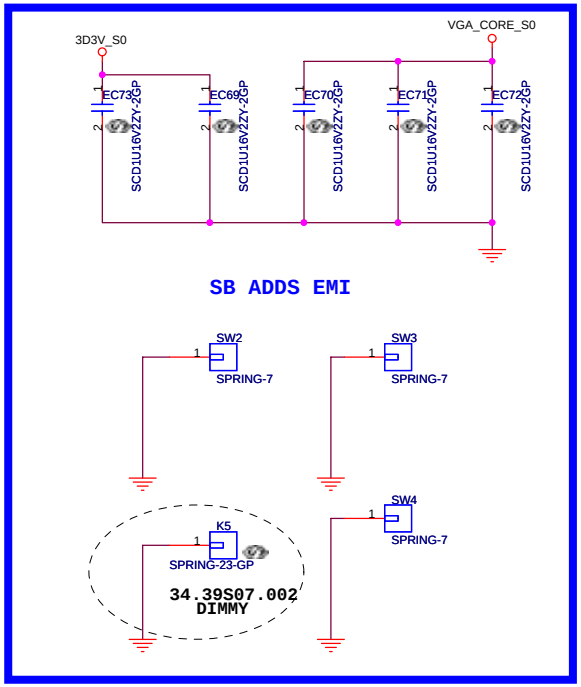
Date: Saturday, June 10, 2006 Sheet 49 of 52

EMI CAP

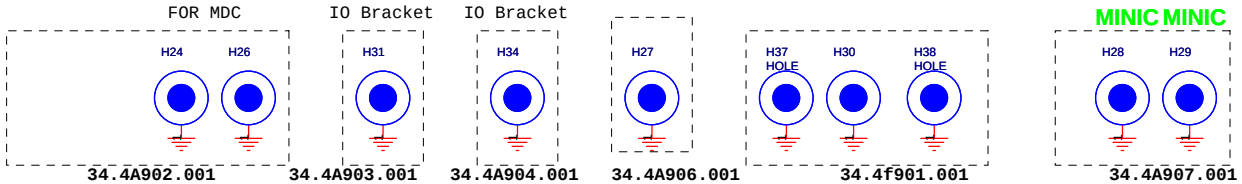


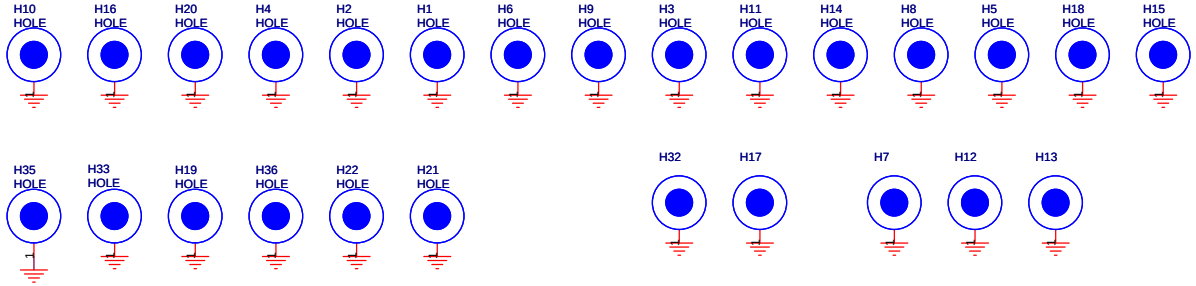






BOTTOM SIDE:





<Variant Name>

緯創資通 Wistron Corporation
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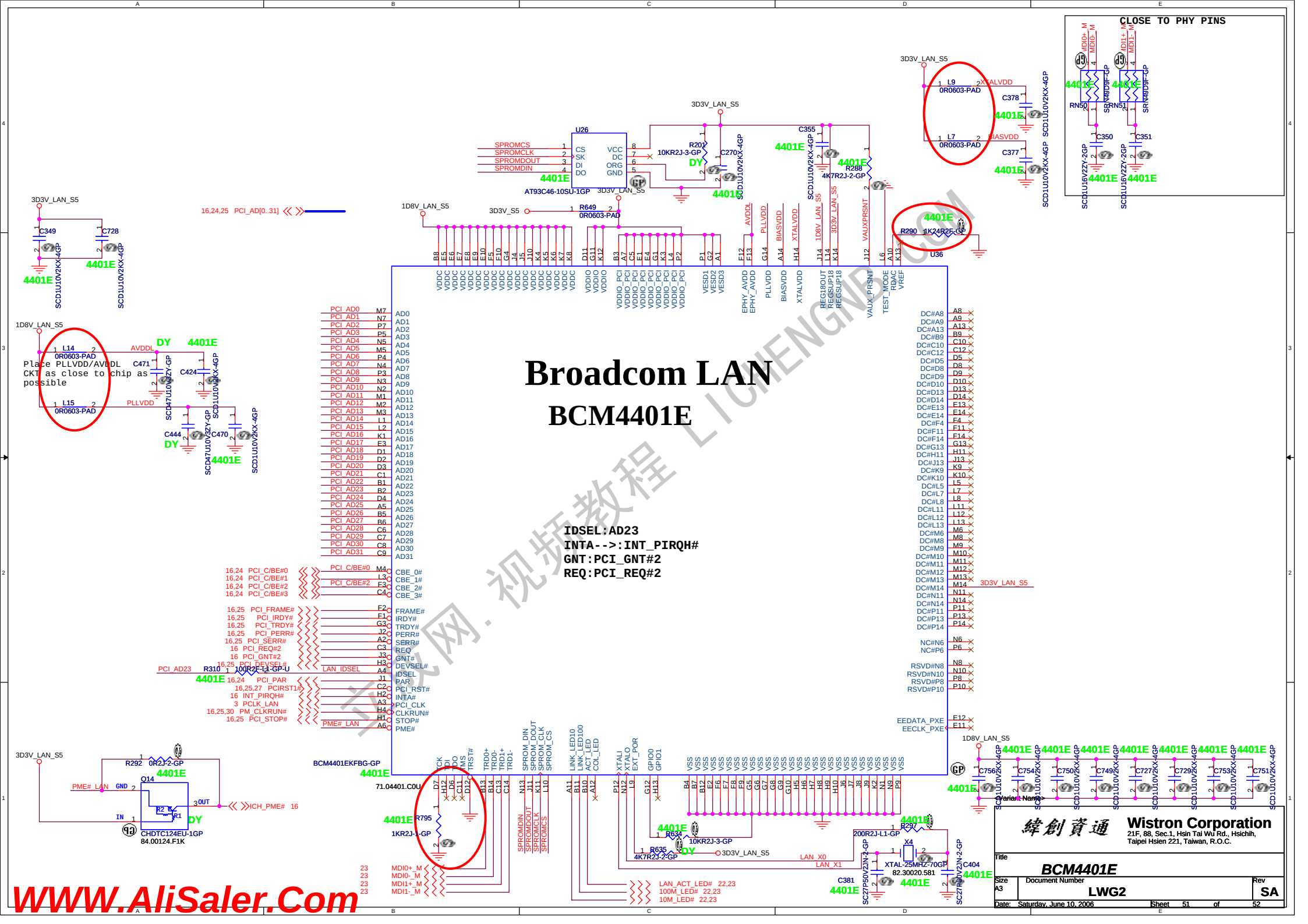
Title: SPRING & BOSS

Size	Document Number	Rev
A3	LWG2	SA

Date: Monday, June 12, 2006 Sheet 50 of 52


Broadcom LAN
BCM4401E
IDSEL:AD23
INTA-->:INT_PIRQH#
GNT:PCI_GNT#2
REQ:PCI_REQ#2
CLOSE TO PHY PINS
Place PLLVDD/AVDDL CKT as close to chip as possible
BCM4401EKFBG-GP
71.04401.C0U
AT93C46-10SU-1GP
Wistron Corporation
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BCM4401E
LWG2
SA
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51
52
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SA change to SB version change notes

1. Page 16 _ C773,C807,C811 for OC# cap -->Dimmy
3. Page 18 _ modify Q36/Q37 mirror
4. Page 50 _ Adds EMI Spring SW2,SW3, SW4 & K5 -- >34.49U26.001
5. Page 16 _ Adds R47 for MDC detect function -- > MDC_KILL# to SB GPIO24
6. Page 21 _ Adds R850,R844 for USB pull low
7. Page 21 _ Adds R25,R26,R38 for USB control to SB GPIO 25/26/27 pin (if use KBC GPIO then Dimmy)
8. Page 21 _ Adds R39,R40,R46 for USB control to KBC GPIO P-25/26/27 pin (if use SB GPIO then Dimmy)
9. Page 21 _ Add D44 for MDC_KILL#
10. Page 50 _ Adds EMI 5 pcs 0.1uF cap
11. Page 19 _ Adds TP118,TP119 tesr pad for test
12. Page 19 _ mirror L12,L13
13. Page 50 _ K4 Dimmy -- > BOM change
14. Page 14 _ L17,L18,L19 change to 47 Ohm -- >68.00084.271
15. Page 23 _ EC2 change to 78.1022N.24L
16. Page 15 _ adds R553 for ACZ_RST# signal to MDC & ALC883
    one signal ACZ_RST_ALC# to audio to page 28
    one signal ACZ_RST_MDC# to modem detect page 21
17. Page 21 _ adds R69 for D44 pull-hi-->63.10334.1DL
18. Page 35/37/38/40/49_Power Open Gap change to Power Close Gap
19. Page 31_ Wireless-BT & NOVO-BT pin change
20. Page 50_ K5 Dimmy

Title: <Title>		
Size: B	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, June 12, 2006	Sheet 52 of 52	