

Compal Confidential

Schematics Document

P4 uFCBGA/uFCPGA Northwood with SIS Core Logic

2001-5-30

REV:1.0A

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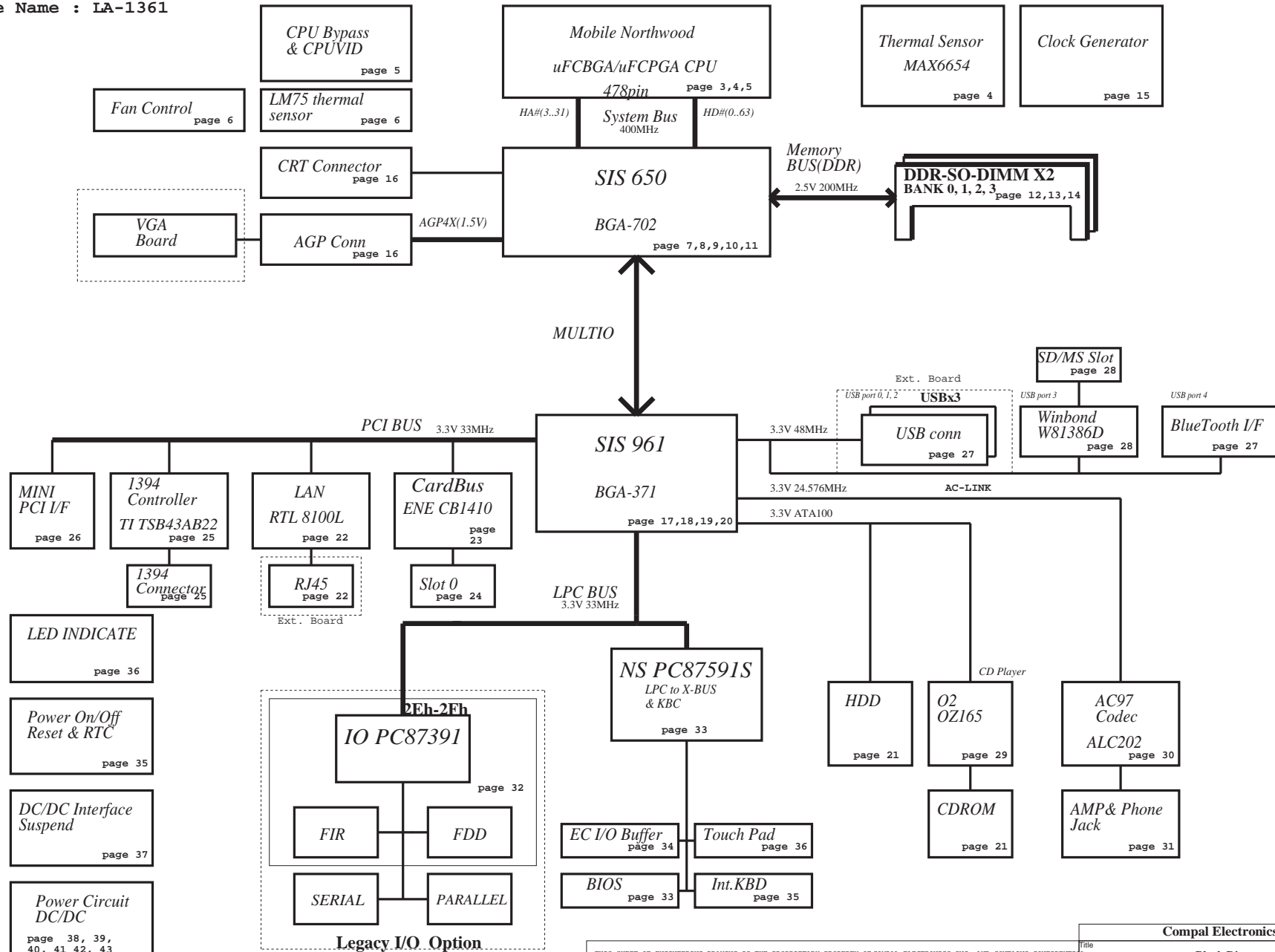
Compal Electronics, Inc.			
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Model Name :CT10

File Name : LA-1361

Block Diagram



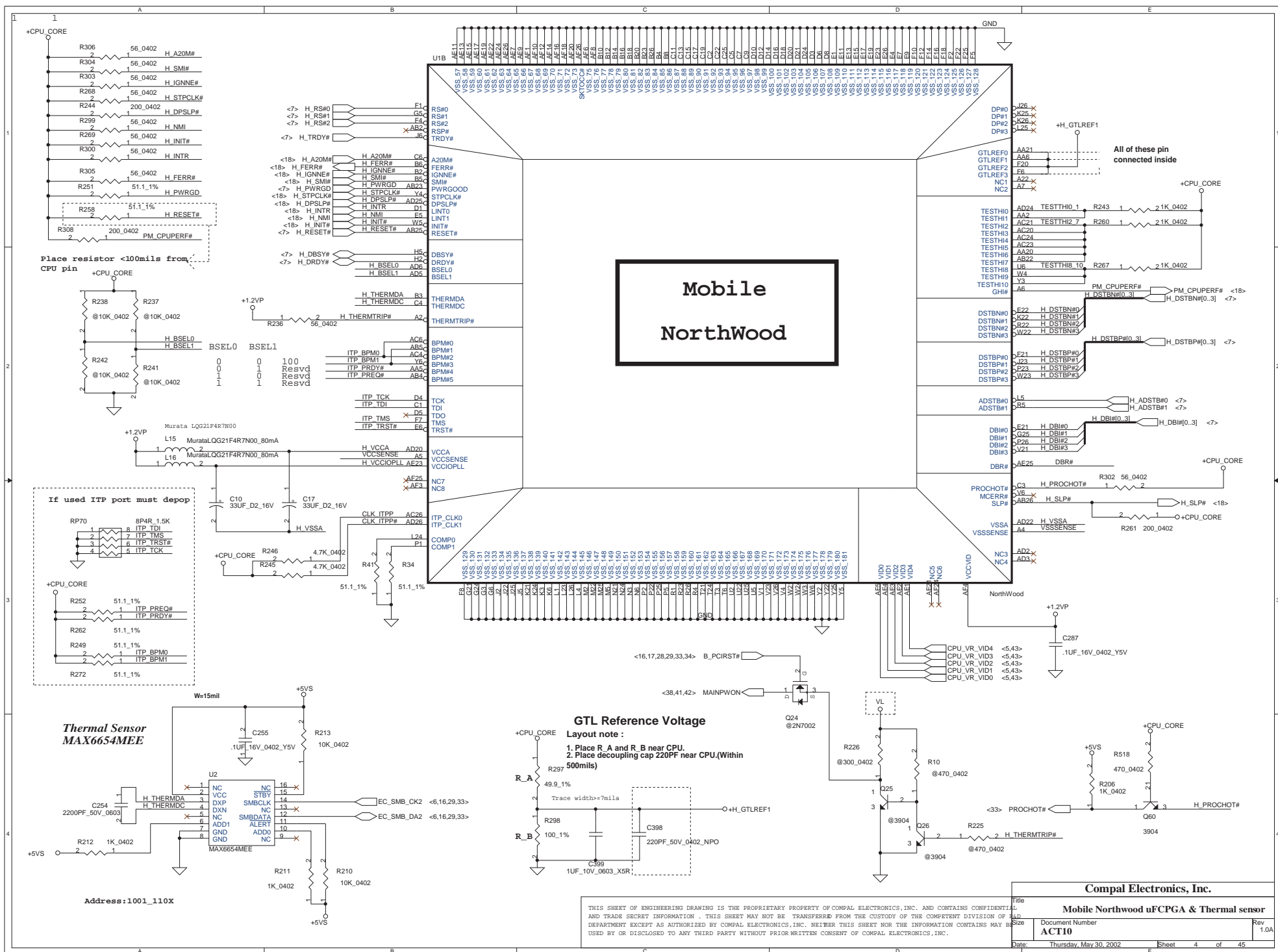
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Block Diagram			
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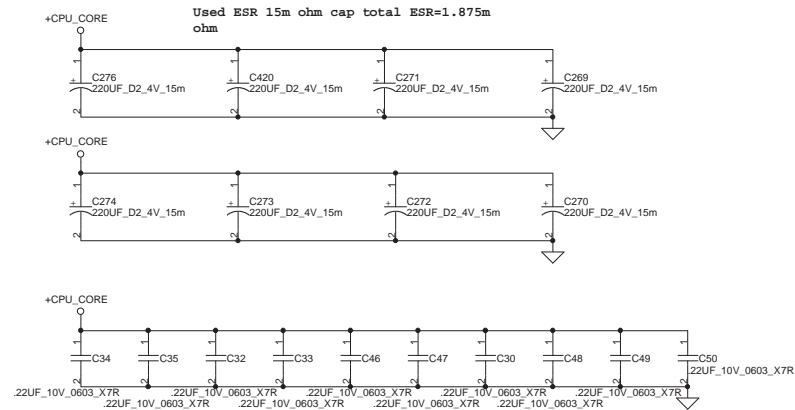
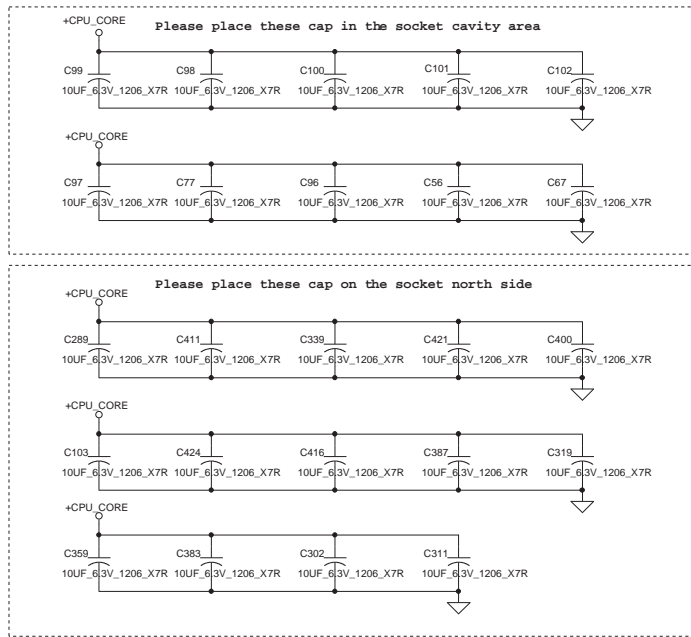


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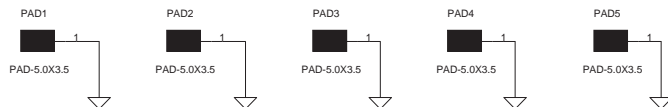
Place close to CPU. Use 2~3 vias per PAD.
Place .22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2~3 vias per PAD.

Layout note :

Place close to CPU power and ground pin as possible (<1inch)



EMI Clip PAD for CPU

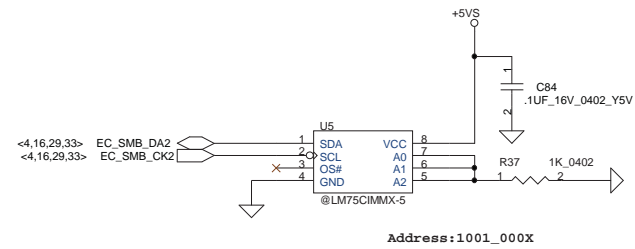
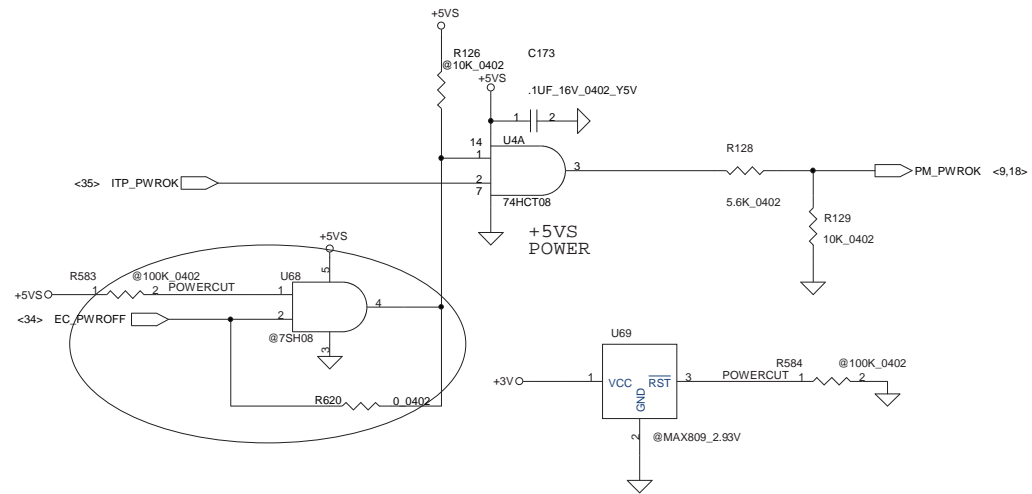


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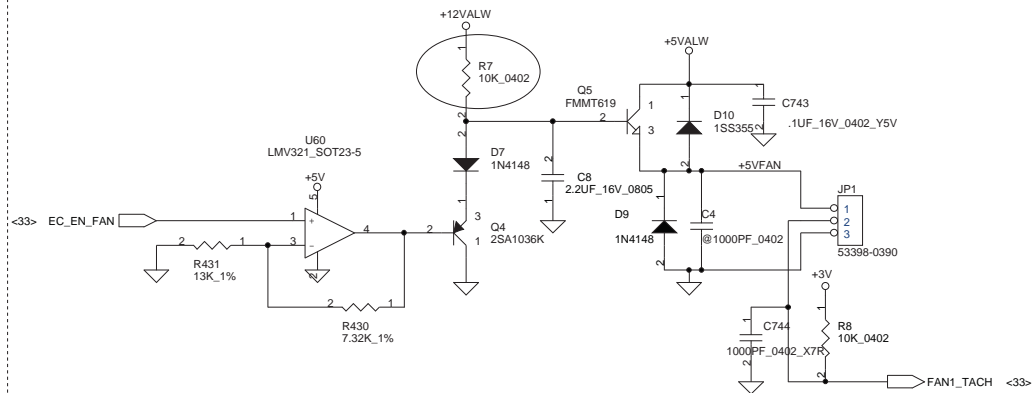
CPU Bypass & CPU VID

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Detect PCB Thermal

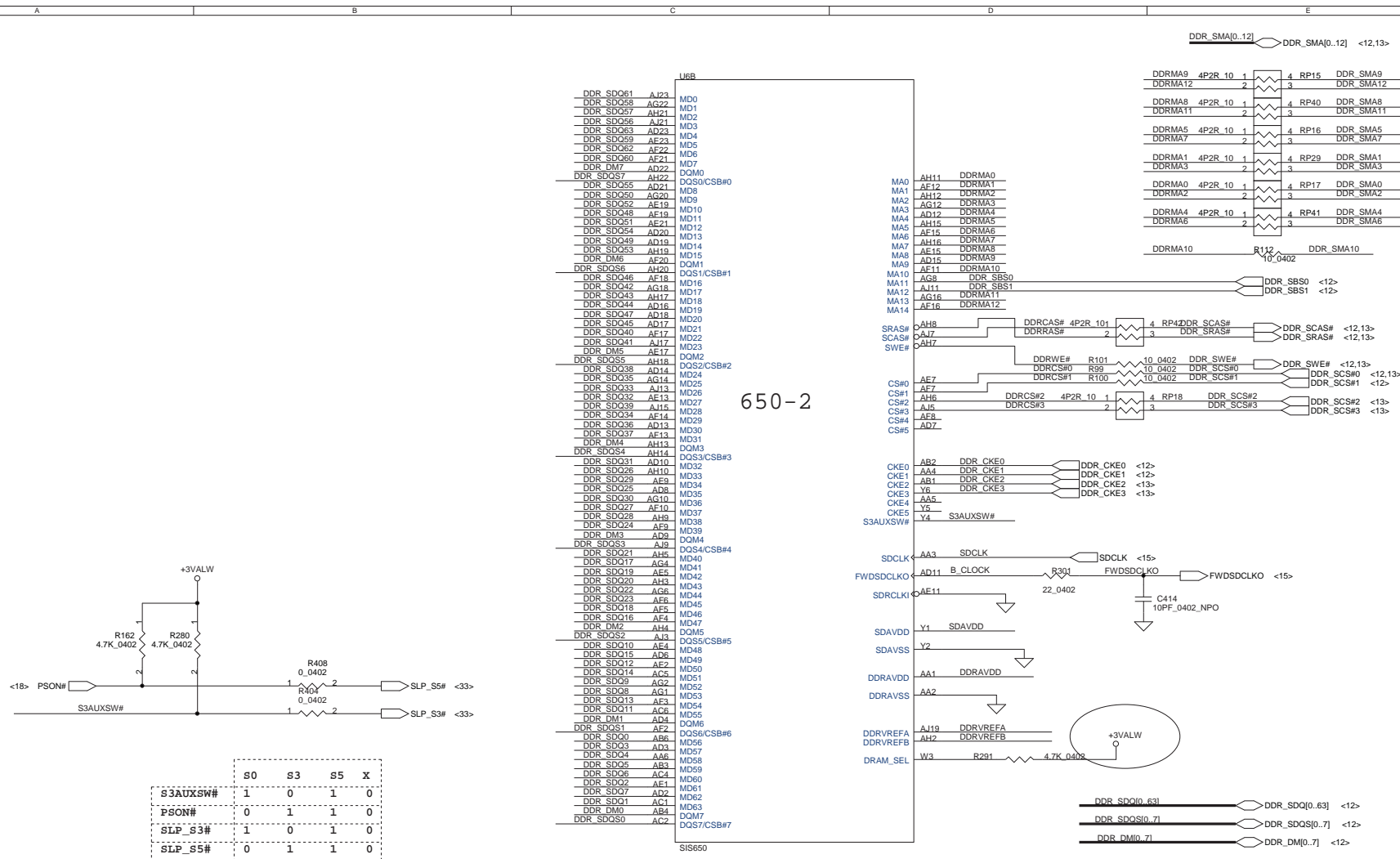
Fan1 Control circuit



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Title	LM75 Thermal sensor & Fan control		
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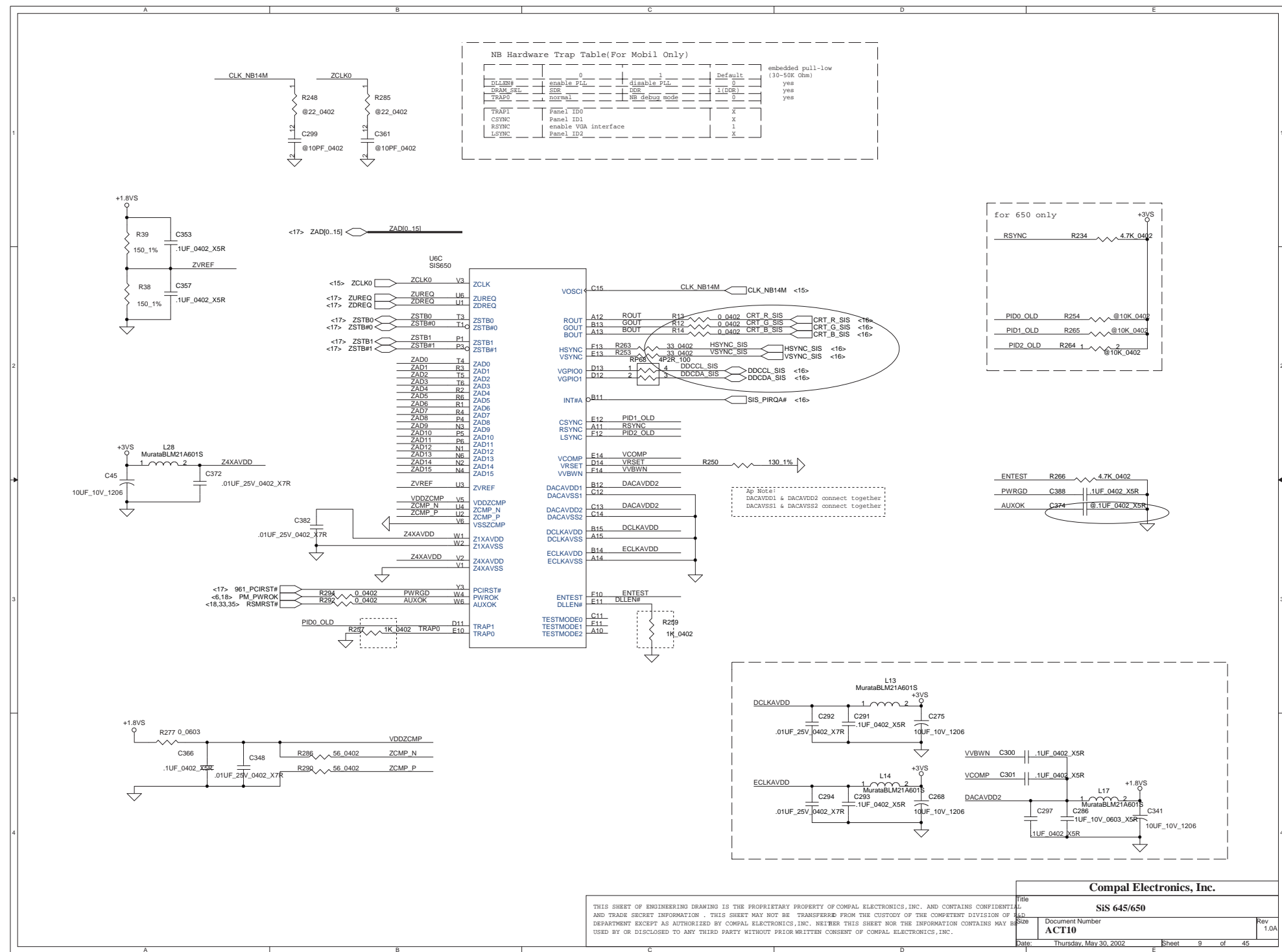




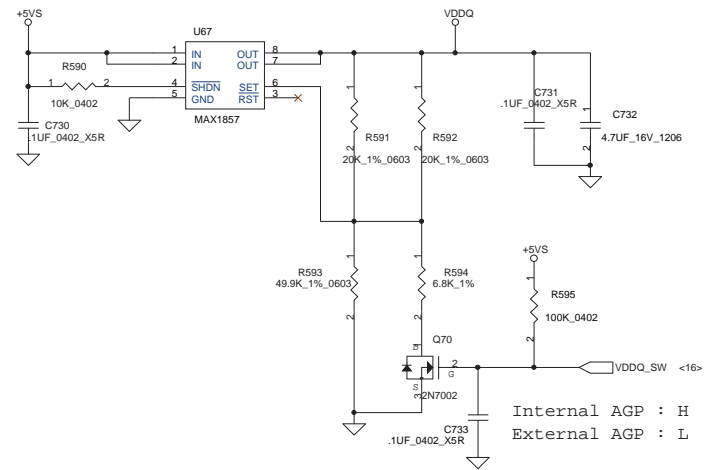
650-2

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SiS 645/650			
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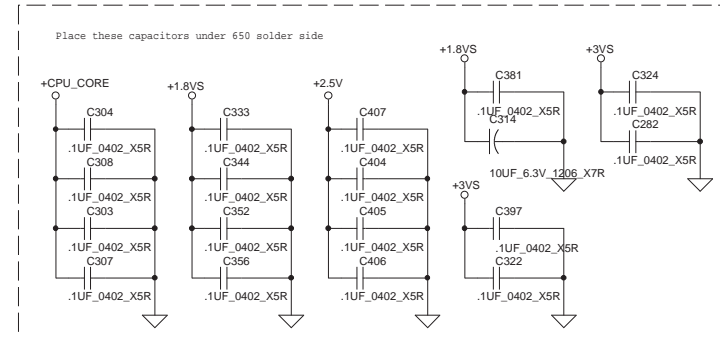
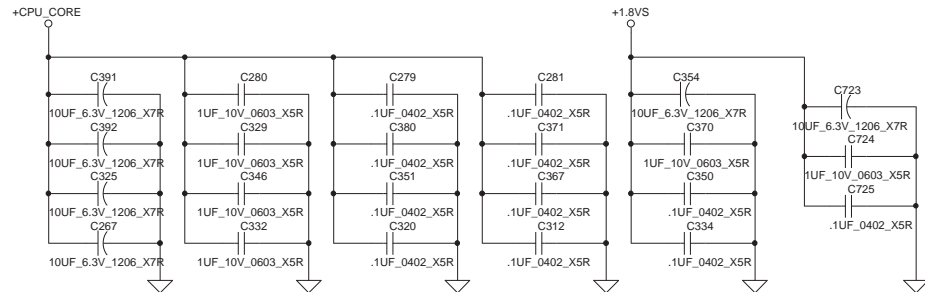
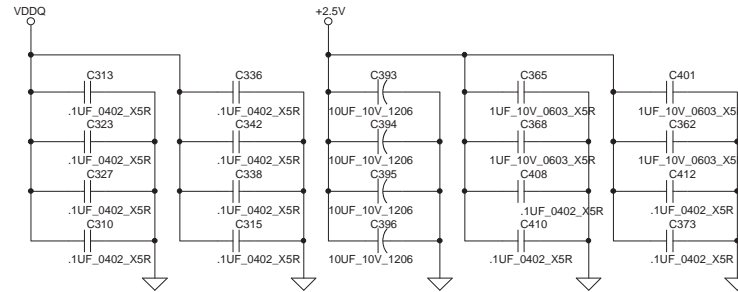
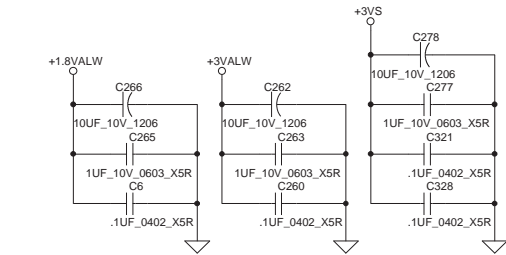
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Compal Electronics, Inc.			
Title		SiS 645/650	
Part Number	Document Number	Rev 1.0A	
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Layout note : Processor system bus
Distribute as close as possible
to Processor Quadrant.(between VTTFB and VSS pin)

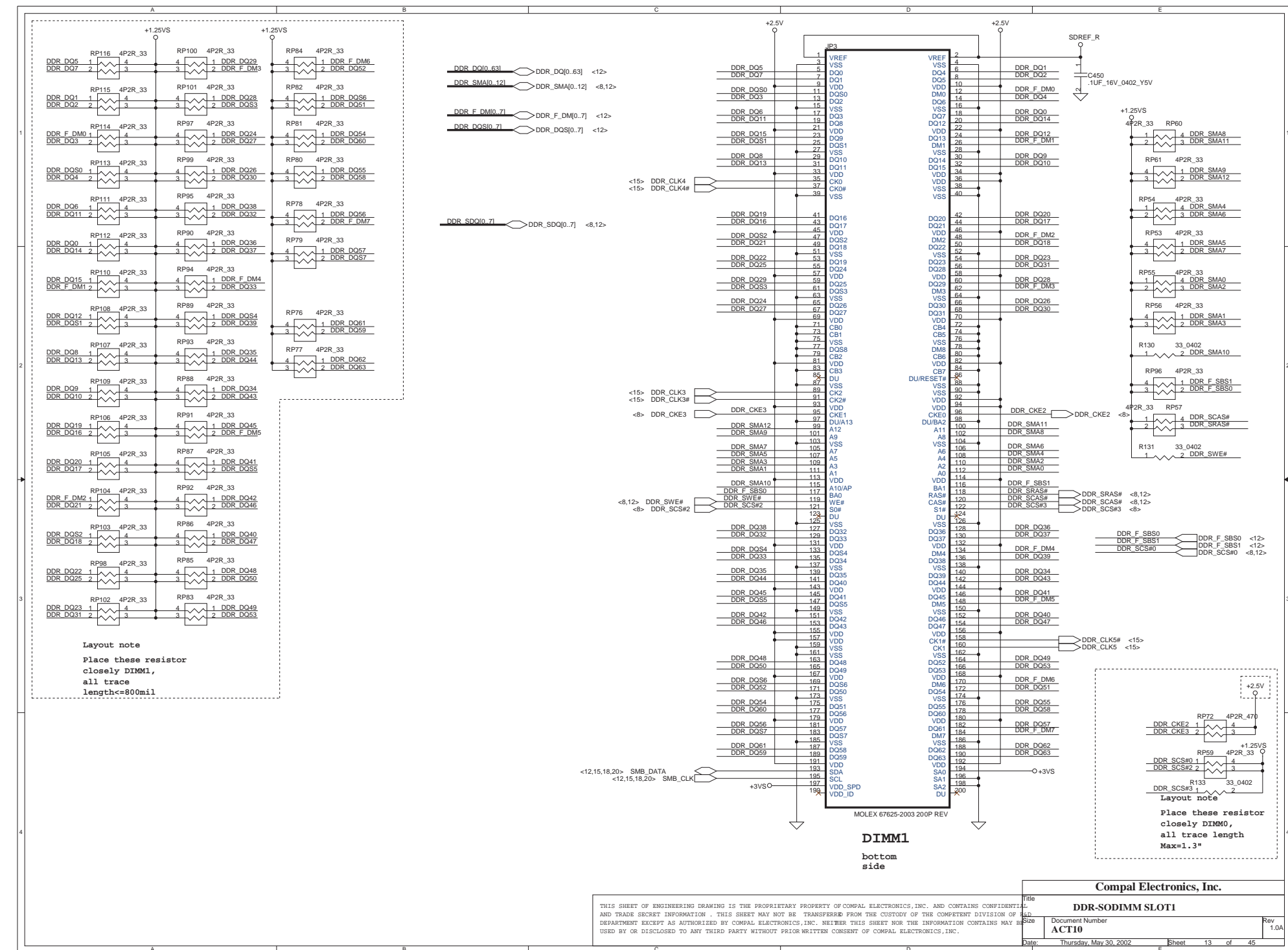
CHECK SiS 650 CAP.
IT NEED HOW MANY ESR



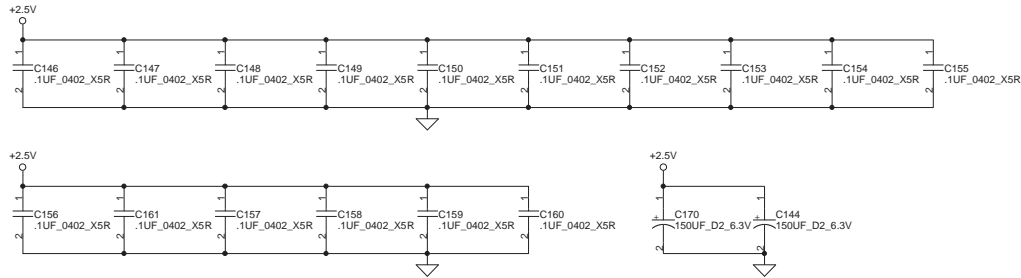
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Compal Electronics, Inc.			
Title	SIS 645/650 Decoupling		
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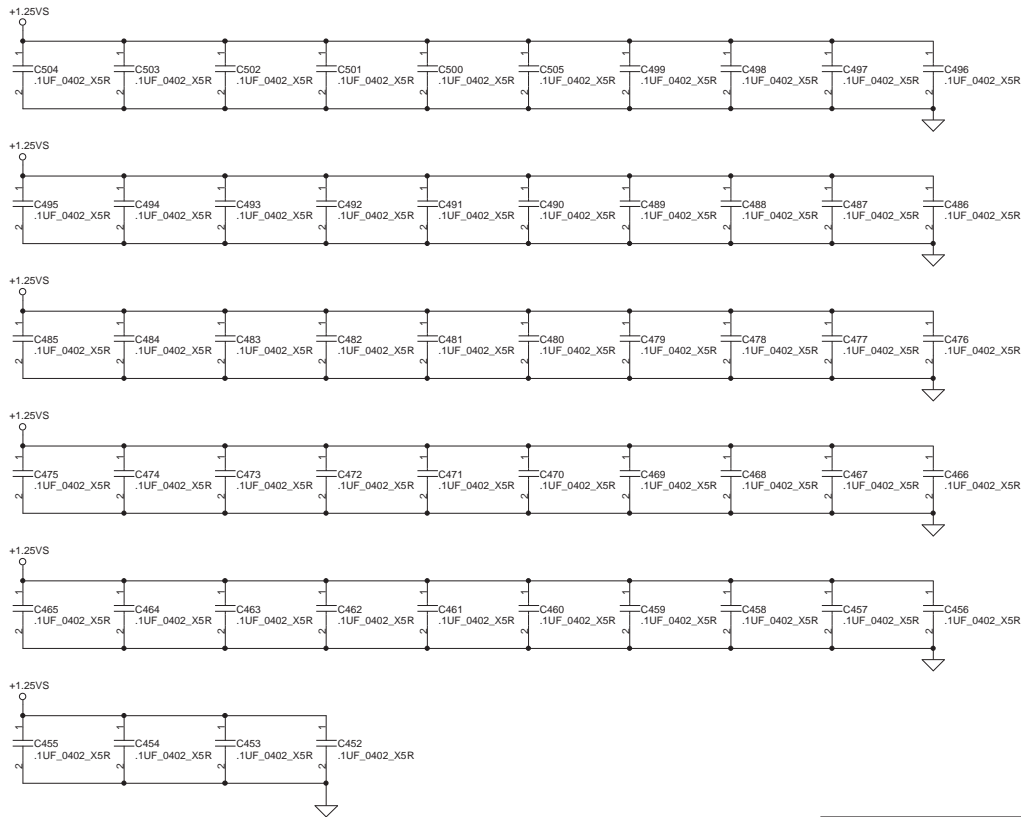




Layout note :
Distribute as close as possible
to DDR-SODIMM.



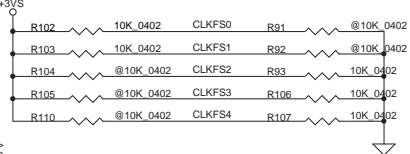
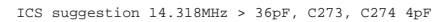
Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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Compal Electronics, Inc.			
DDR SODIMM Decoupling			
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(3 OPTIONS)
1: (ICS:ICS952001)
2: (Cypress:CY28342)
3: (Hitachi:HDTS403)



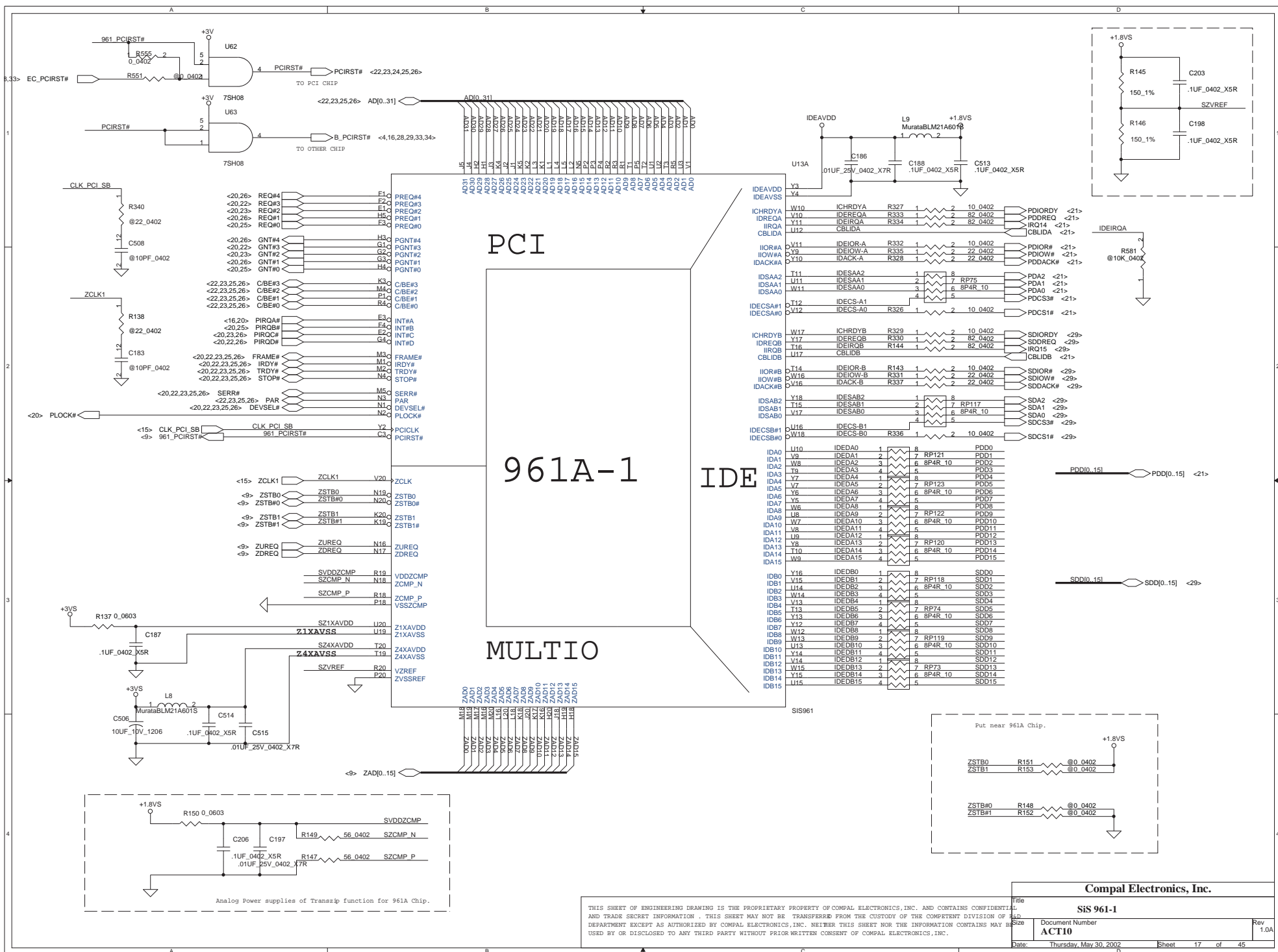
	FS4	FS3	FS2	FS1	FS0	CPU	DDR	ZCLK	AGP	PCI
1	1	0	0	0	0	100.0	133.0	80.0	66.7	33.3
1	1	0	0	0	1	100.0	100.0	80.0	66.7	33.3
0	0	1	1	1	1	100.0	133.3	80.0	66.7	33.3
* 0	0	0	0	1	1	100.0	133.3	66.7	66.7	33.3

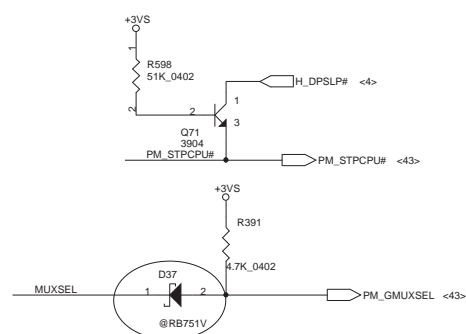
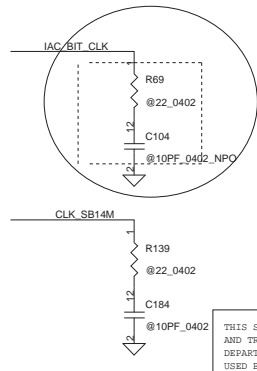
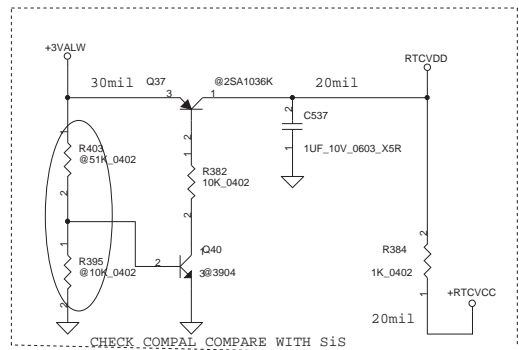
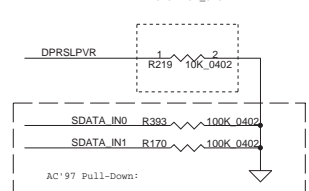
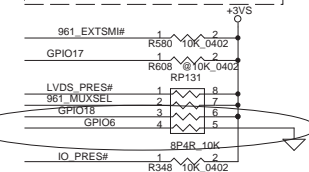
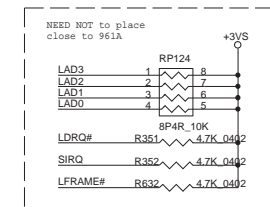
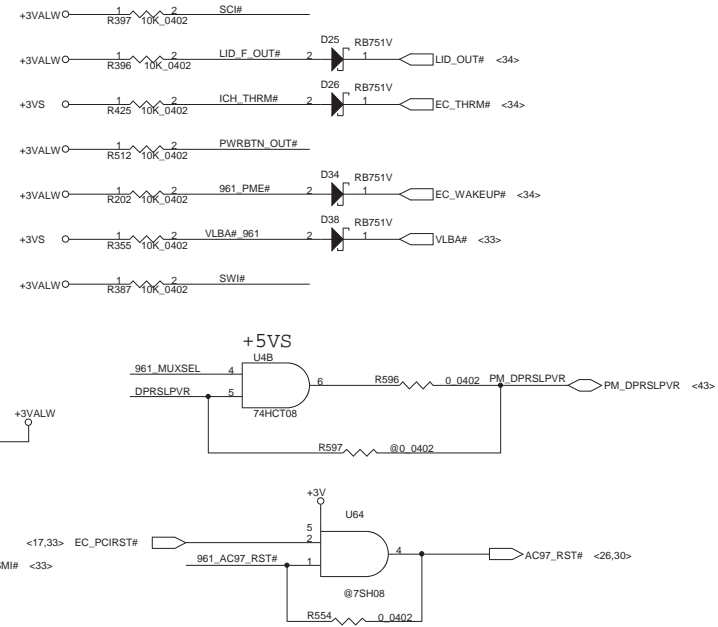
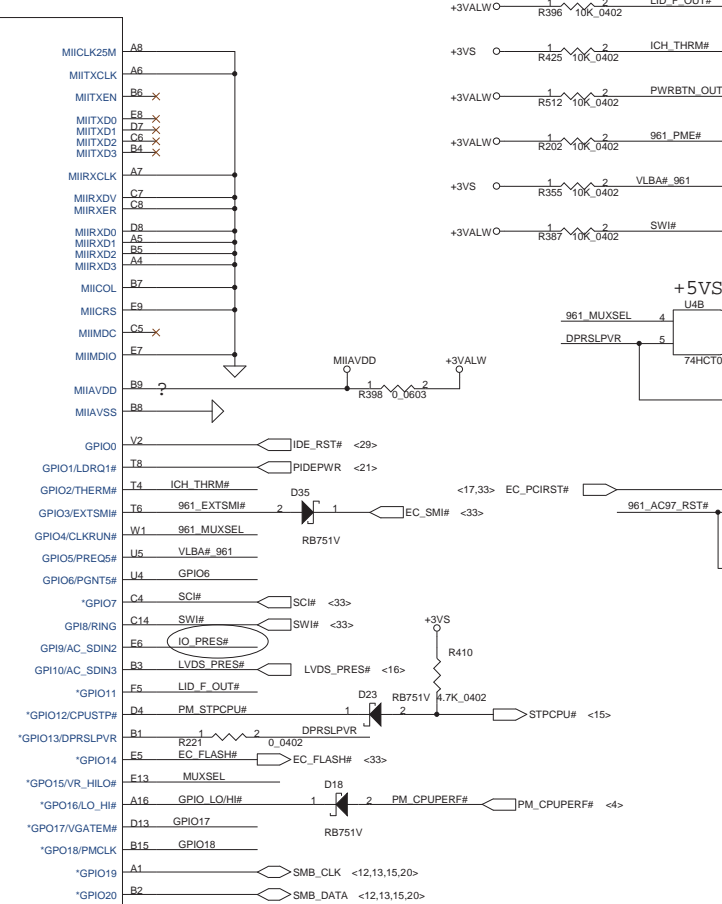
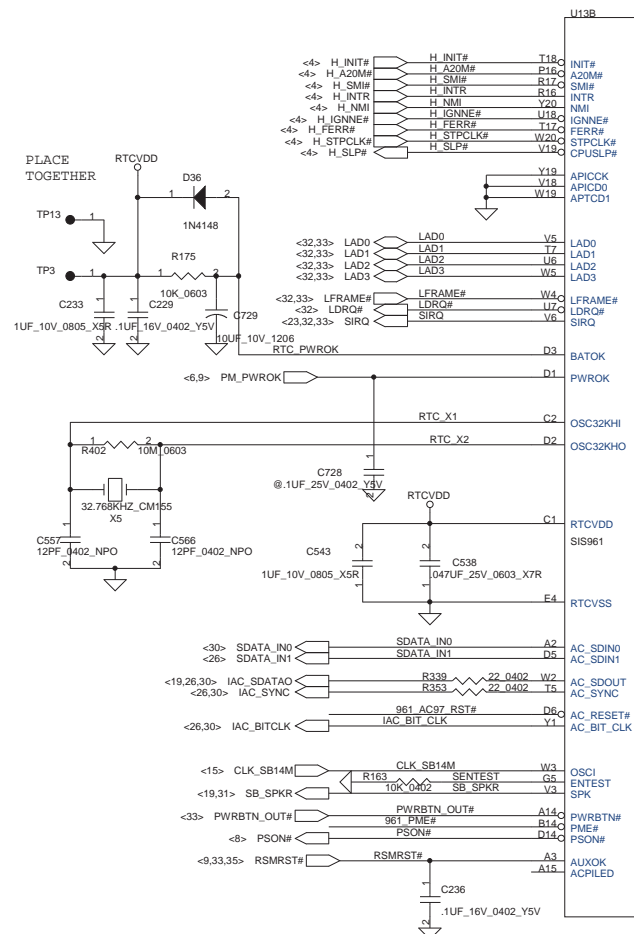
Clock Generator

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Clock Generator			
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Title			
SiS 961-2			
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FOR 961 USB PIN DEFINITION

Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
 Control 0 : port 1 UV1+ E14 UV1- D15 OC1# J16
 Control 0 : port 2 UV2+ E16 UV2- E15 OC2# H17
 HW TRIP PULL LOW 1K SOUTH BIRDGE DEBUG MODE

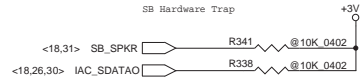
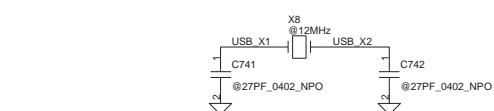
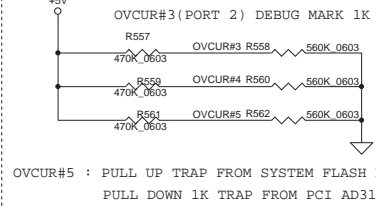
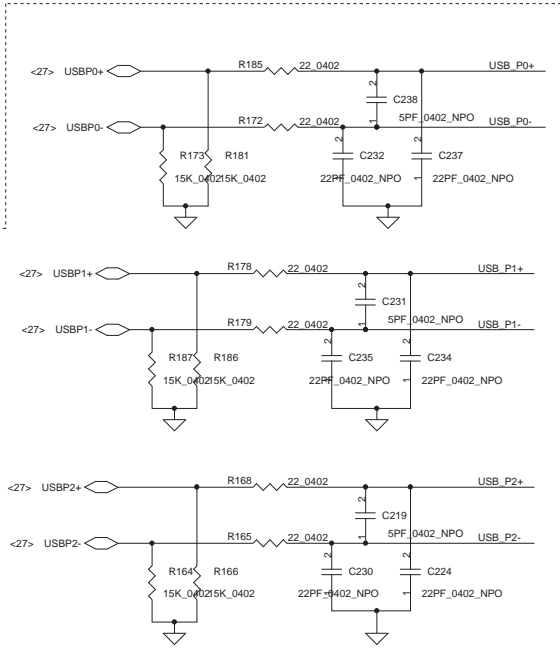
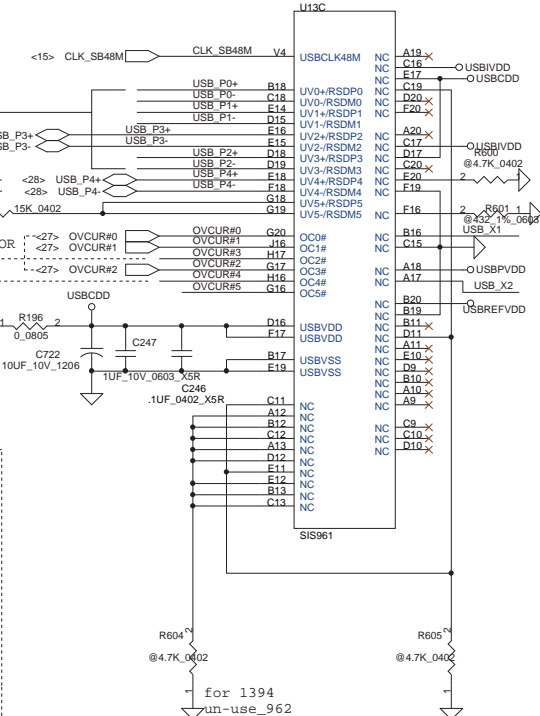
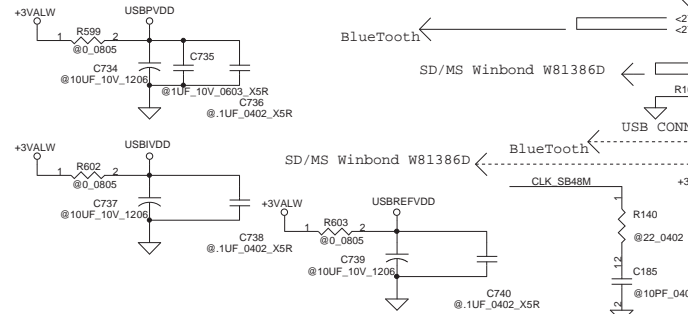
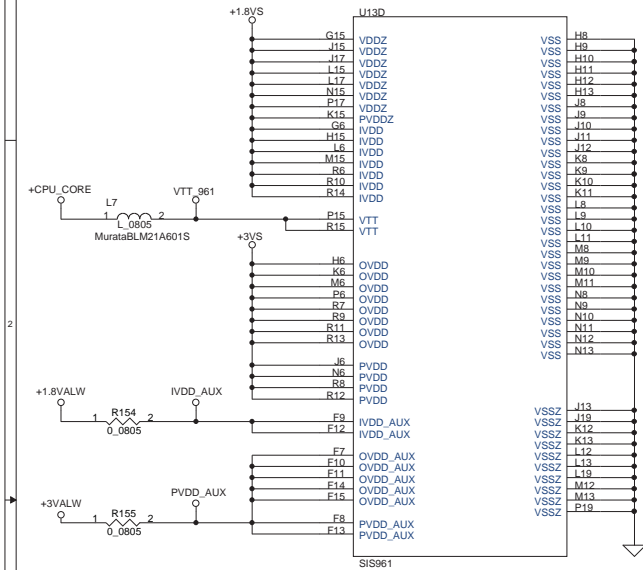
Control 1 : port 3 UV3+ D18 UV3- D19 OC3# G17
 Control 1 : port 4 UV4+ E18 UV4- F18 OC4# H16
 Control 1 : port 5 UV5+ G18 UV5- G19 OC5# G16
 HW TRIP PULL LOW 1K TRIP FROM PCI AD0..31
 PULL HIGH TRIP FROM FLASH ROM

FOR 962 USB PIN DEFINITION

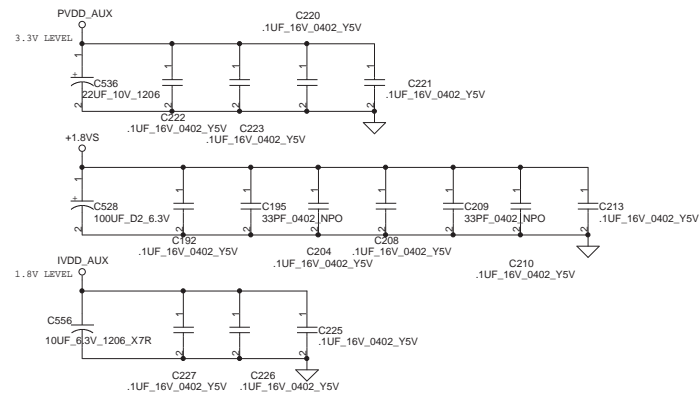
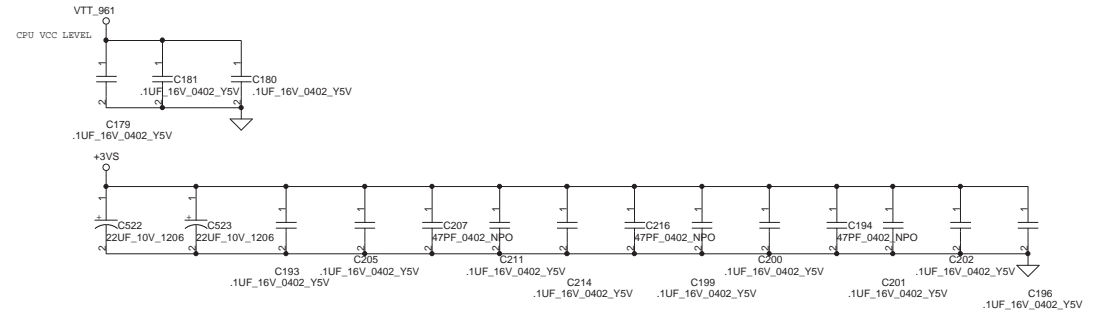
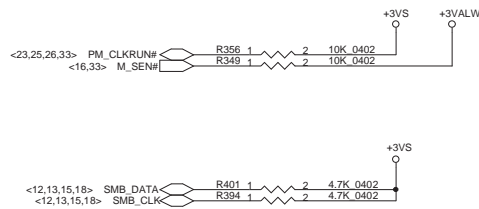
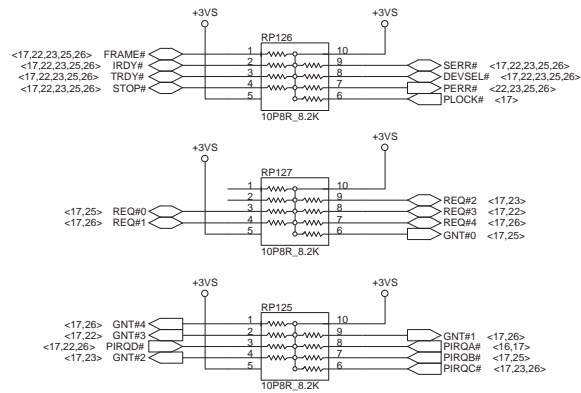
Control 0 : port 0 UV0+ B18 UV0- C18 OC0# G20
 Control 0 : port 3 UV3+ E18 UV3- F18 OC3# H16

Control 1 : port 1 UV1+ D18 UV1- D19 OC1# G17
 Control 1 : port 4 UV4+ E16 UV4- E15 OC4# H17

Control 2 : port 2 UV2+ E14 UV2- D15 OC2# J16
 Control 2 : port 5 UV5+ G18 UV5- G19 OC5# G16

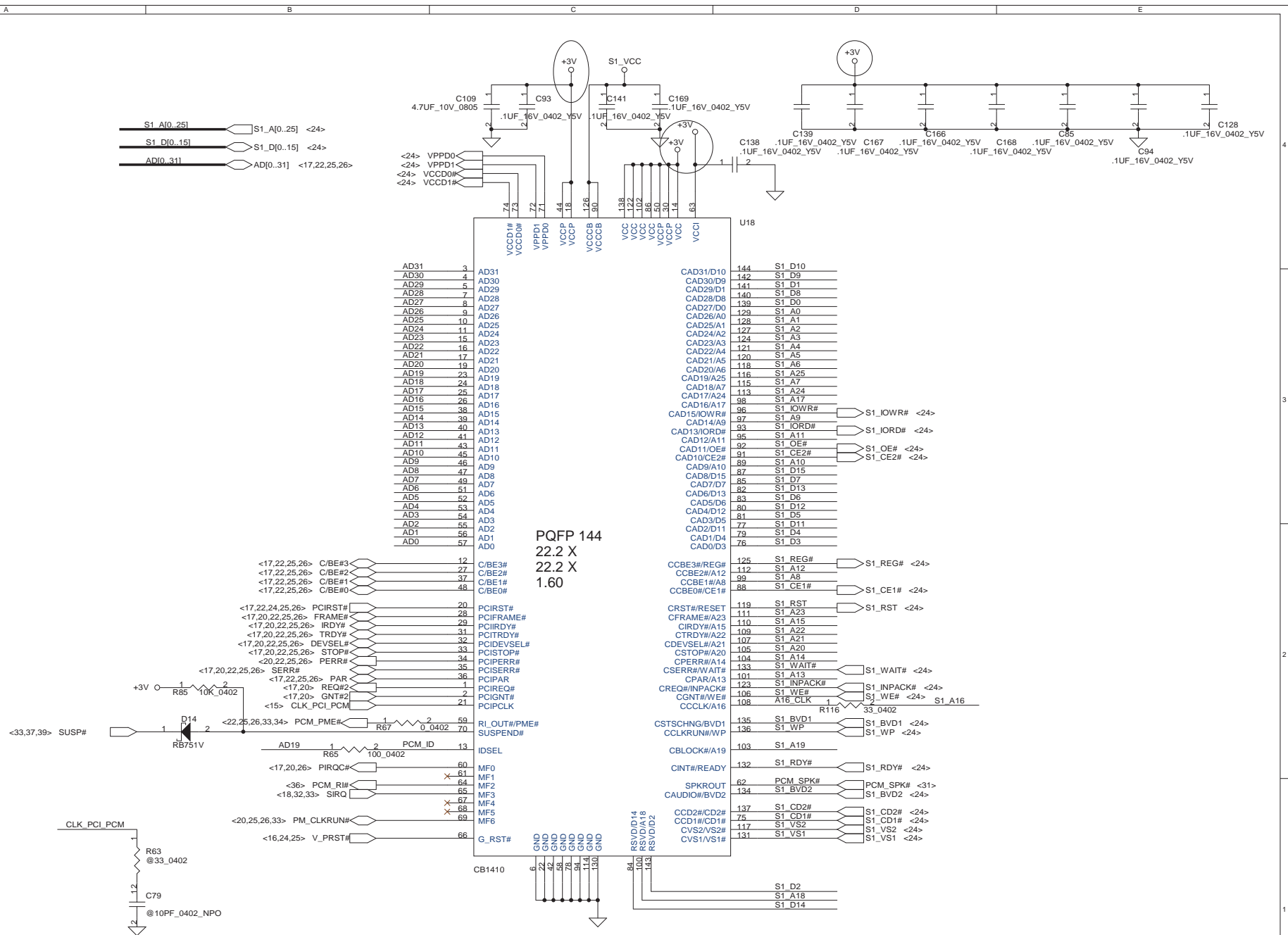


	0	1	Default
SPER (LPC addr mapping)	disable	enable	0
SDATO (RCLK PLL)	enable	disable	0
OC2 (SB debug mode)	enable	disable	1
OC5 (Trap mode)	PC7 AD	ROM	1

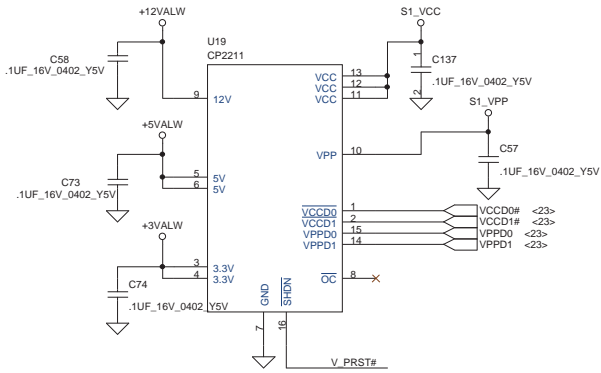


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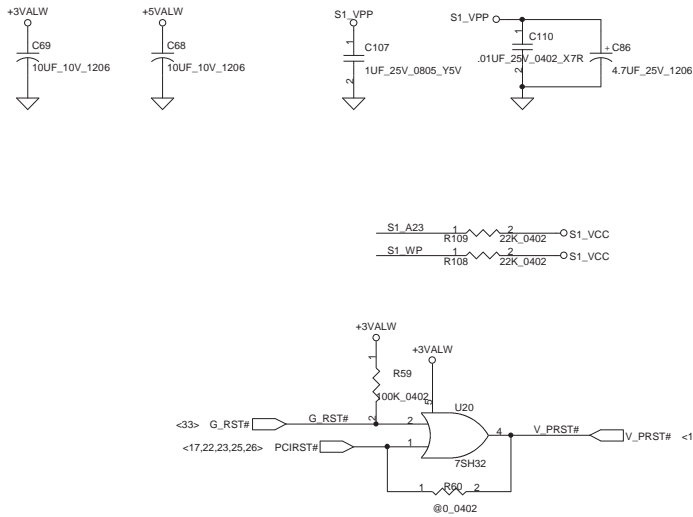
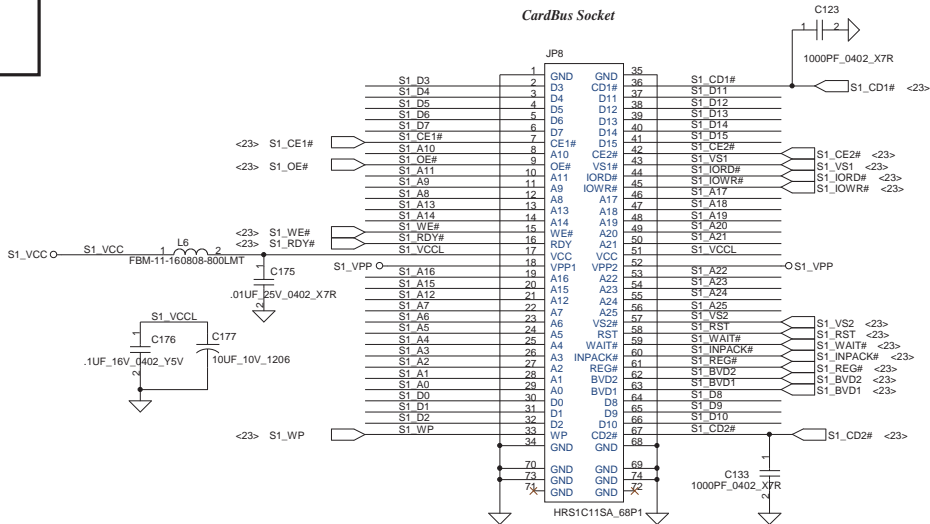
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PCMCIA Power Controller



CardBus Socket

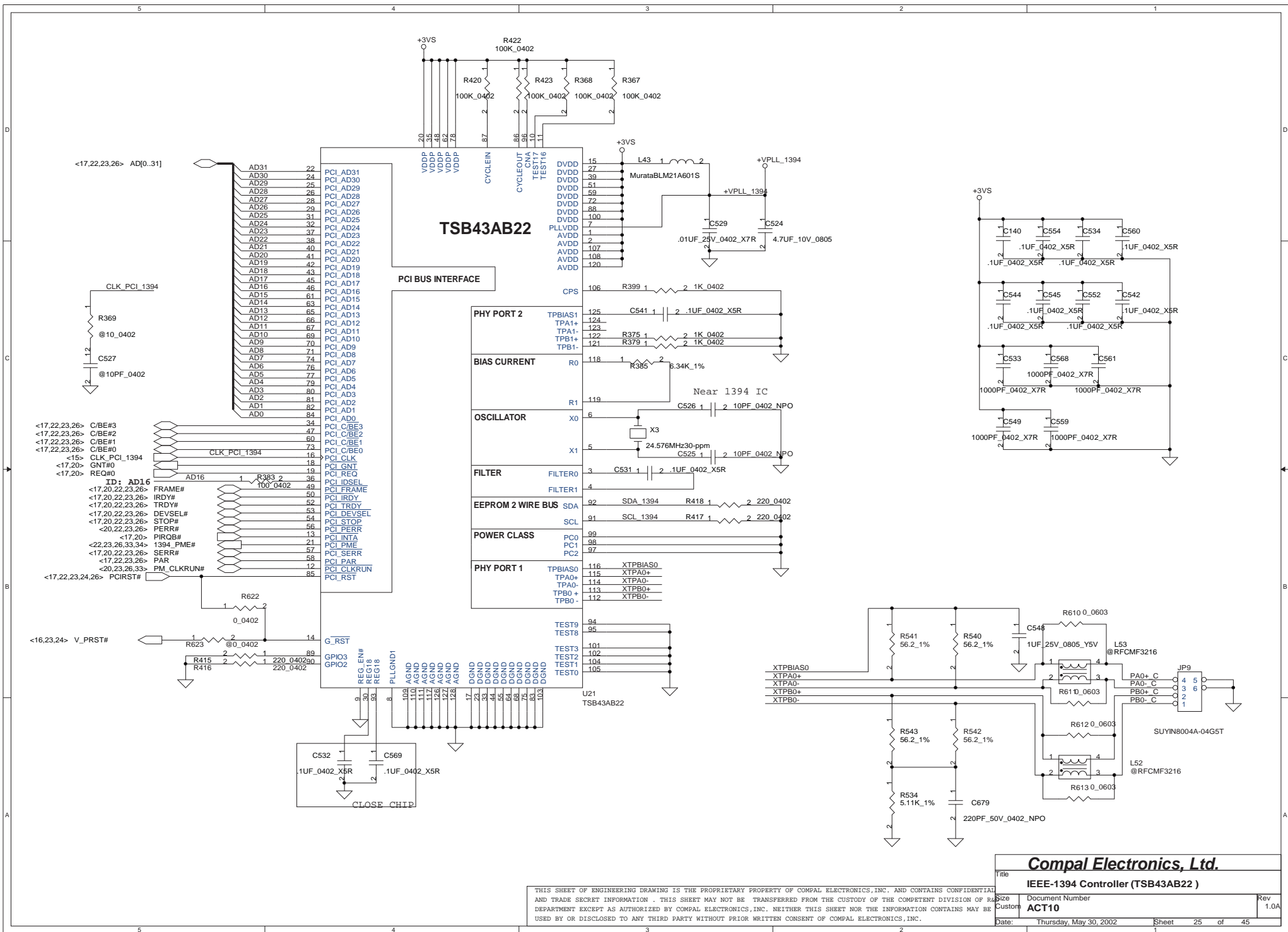


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CardBus Socket

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CardBus Socket			
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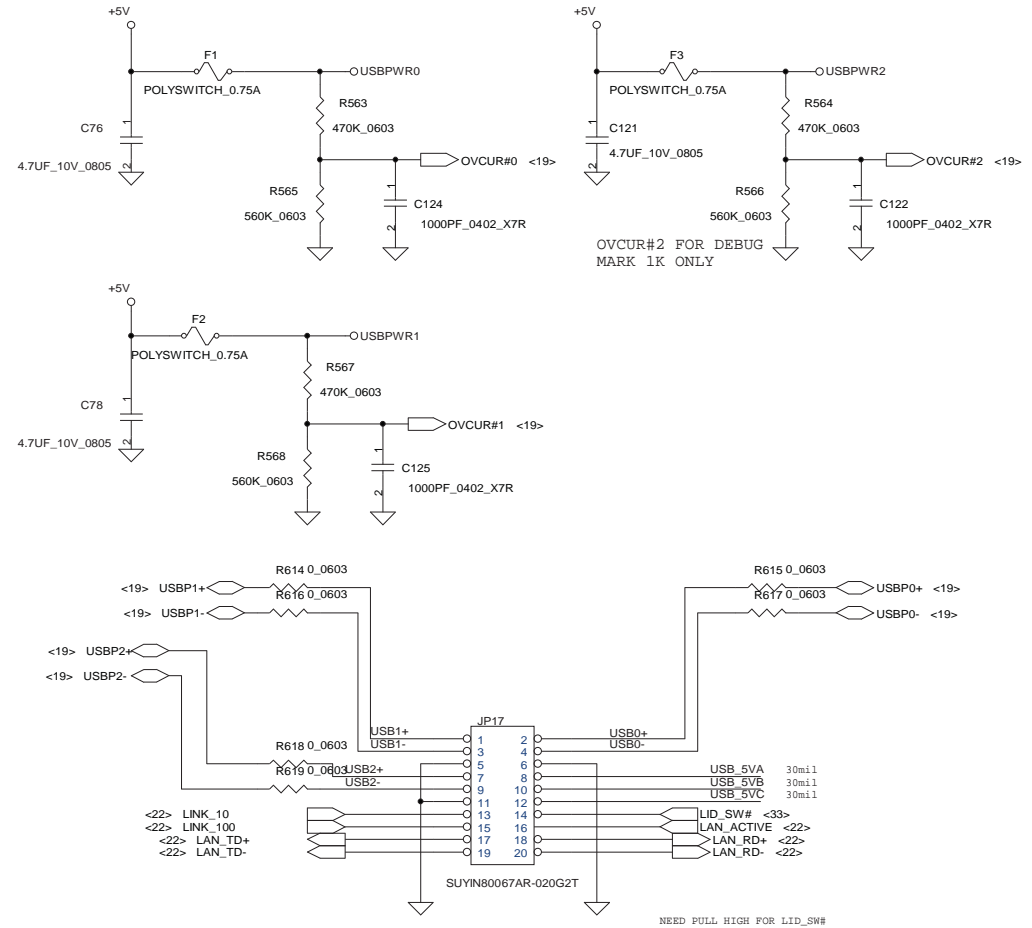
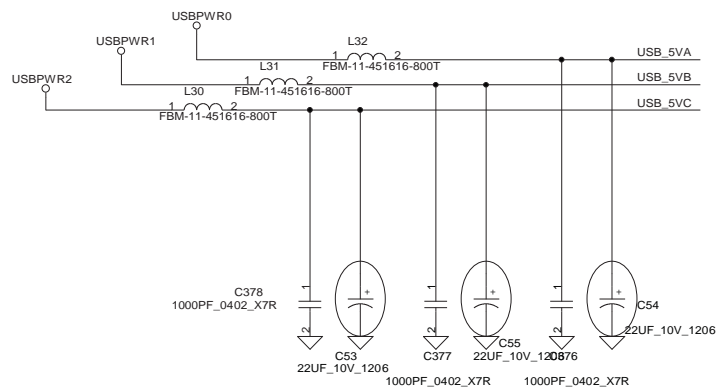
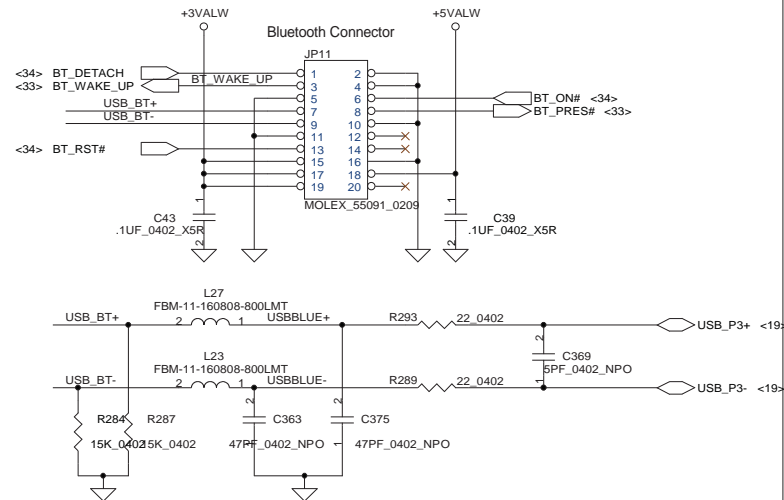
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IEEE-1394 Controller (TSB43AB22)

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Bluetooth Interface

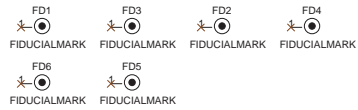


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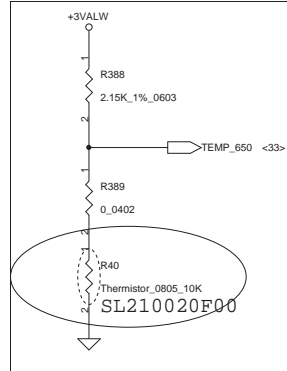
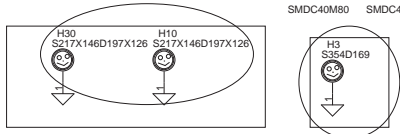
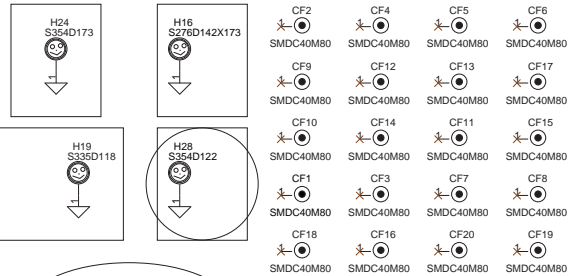
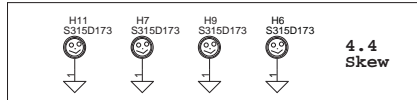
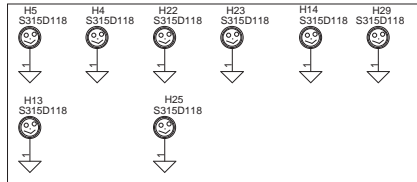
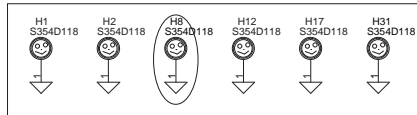
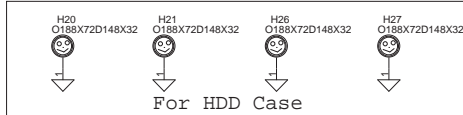
Compal Electronics, Ltd.			
Title			
USB & BlueTooth Connector			
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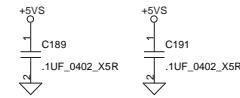
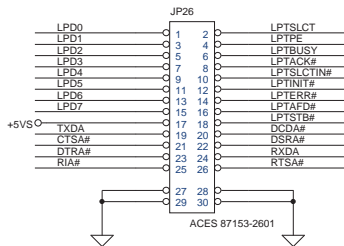
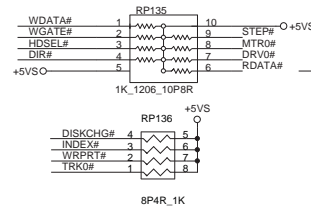
Fiducial Mark



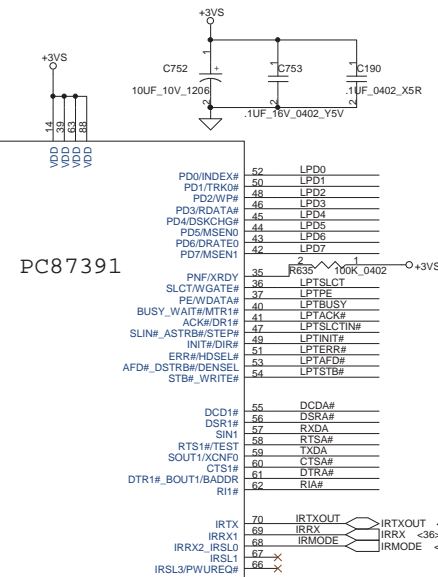
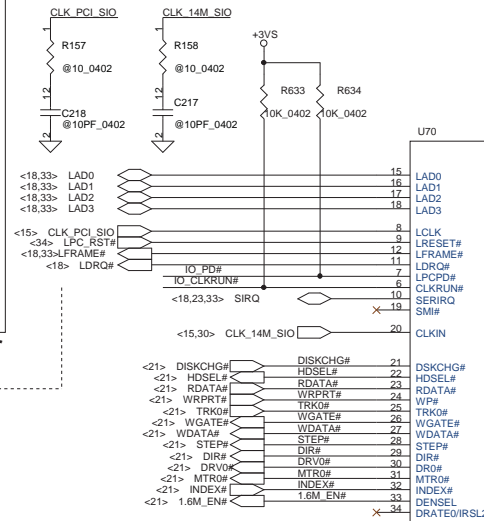
Screw Hole



The temperature sensing for SIS650



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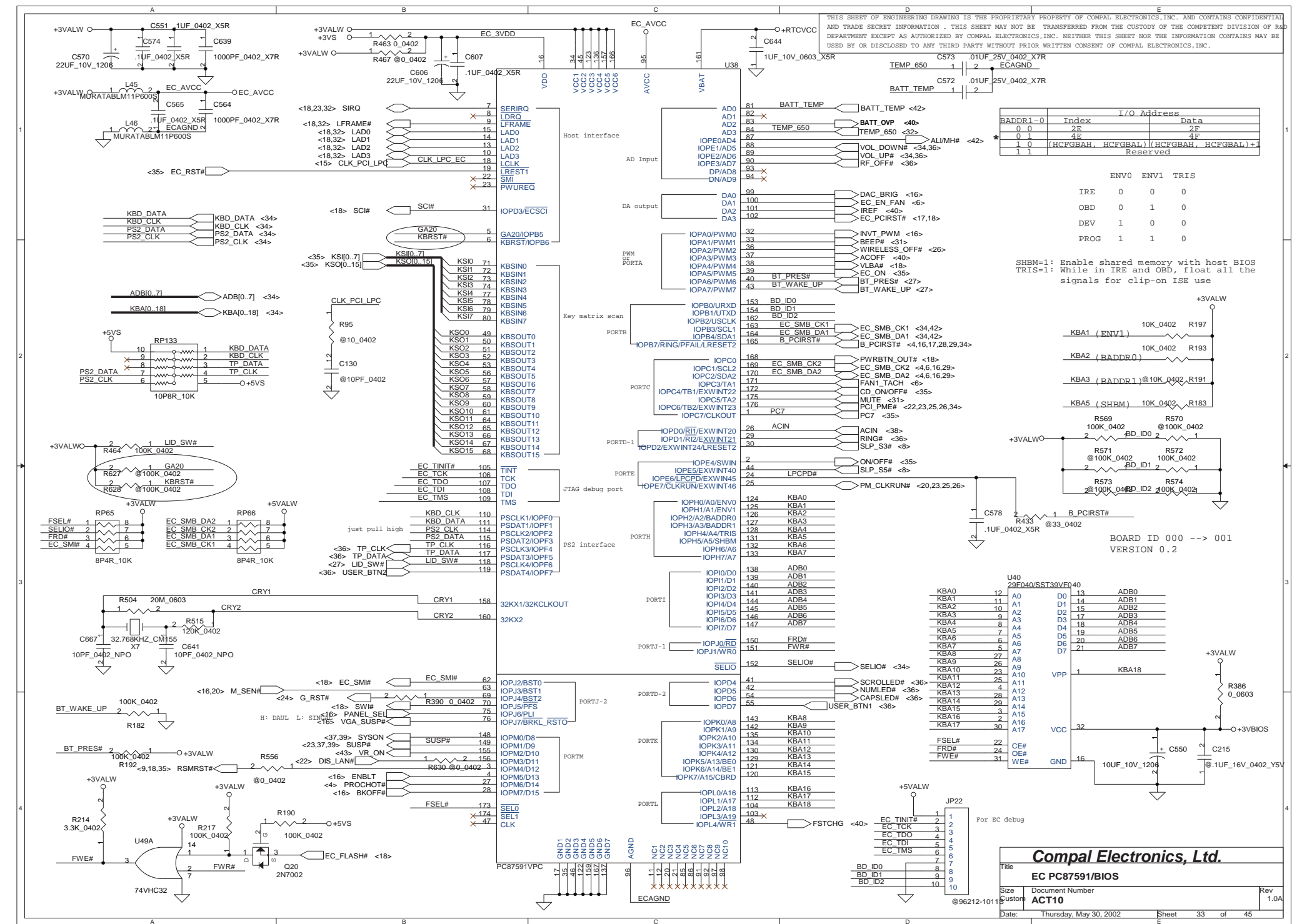


Signal	Pin #	Description
BADDR: DTRA#	61	BASE Address Selection "0": 2E-2F (Default) "1": 4E-4F

Compal Electronics, Inc.

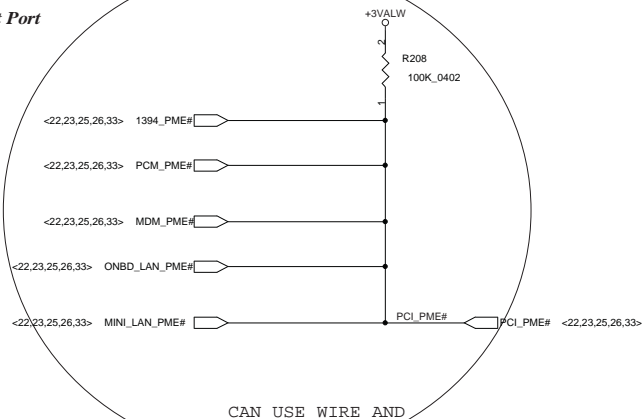
Skew Hole/SUPER IO

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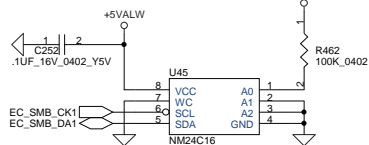


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<33> KBA[0..18] KBA[0..18]

Input Port

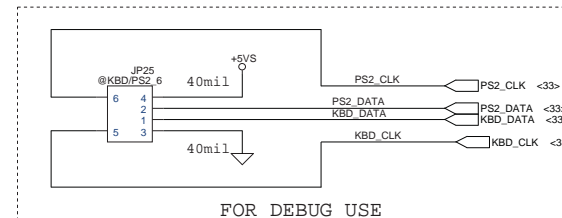
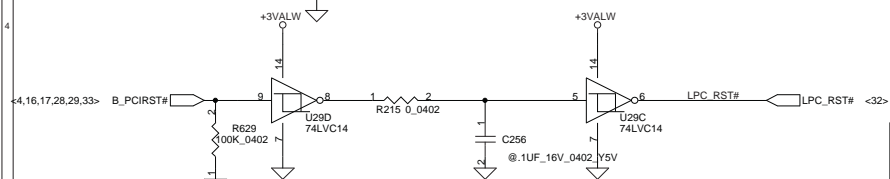
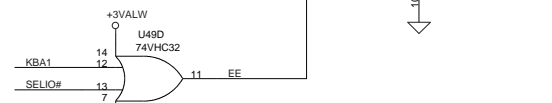
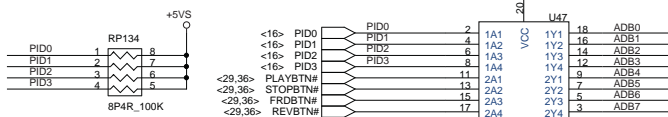


NM24C164 Address definition: 1 A2 A1# A0 B2 B1 B0 R/W#



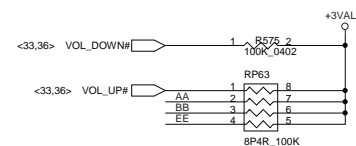
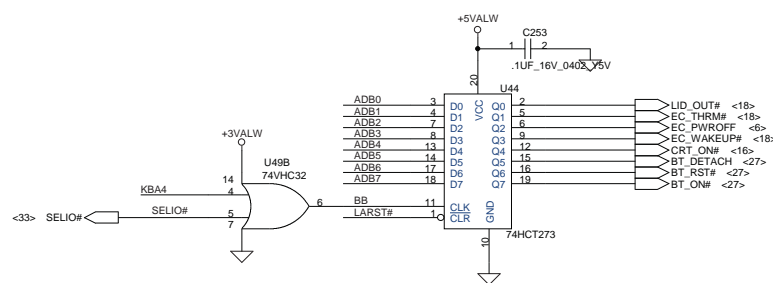
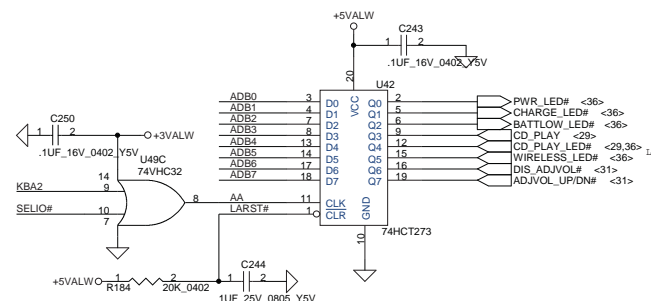
EC I2C Bus Address:

24C164: 1011xxxx R/W#
24C16: 1010xxxx R/W#



FOR DEBUG USE

Output Port



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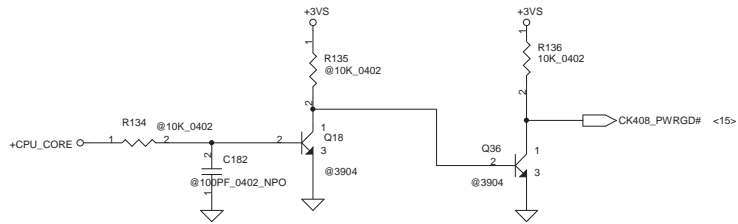
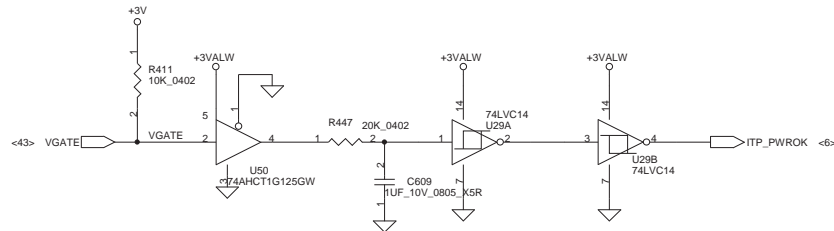
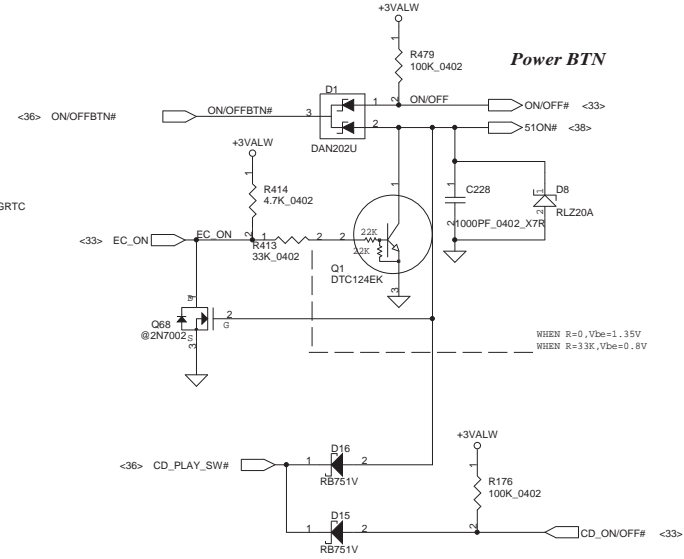
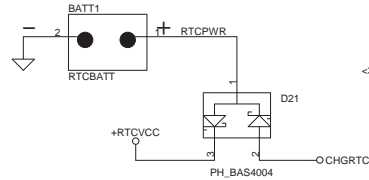
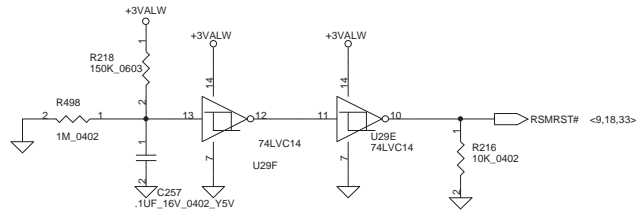
EC Extend I/O KB Comm. & BIOS

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Power ON Circuit

RTC Battery

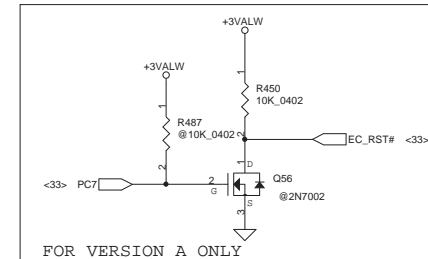
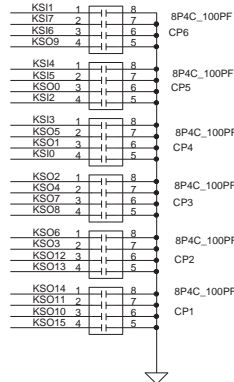
Power BTN



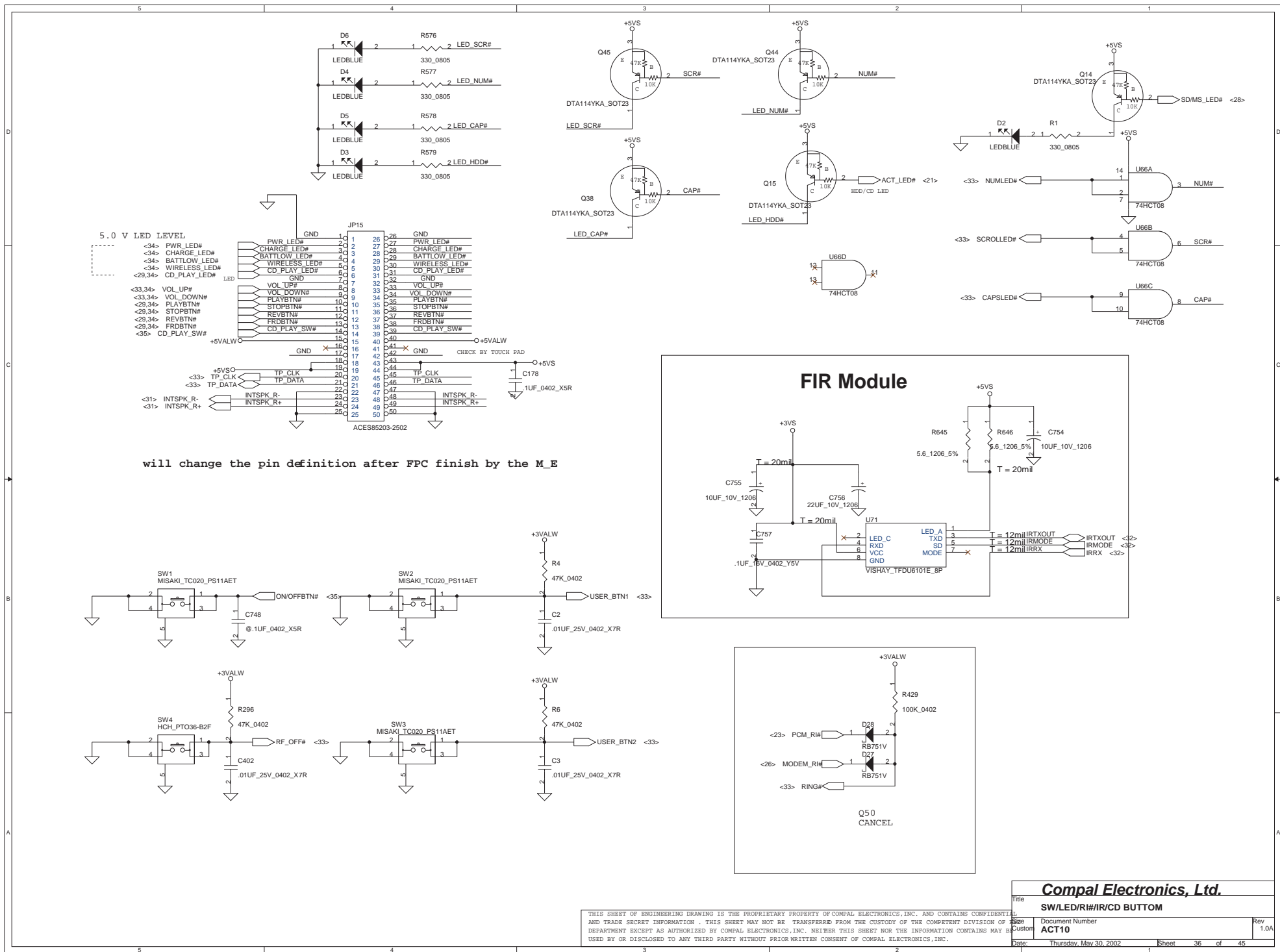
<33> KSO[0..15] KSO[0..15]
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INT_KBD CONN.

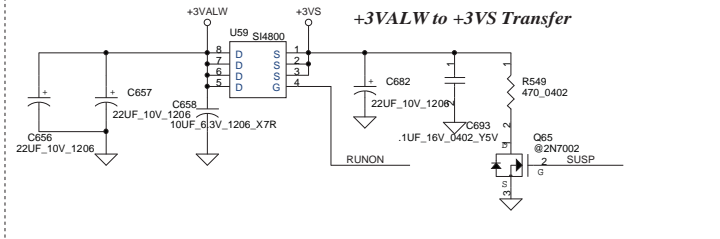
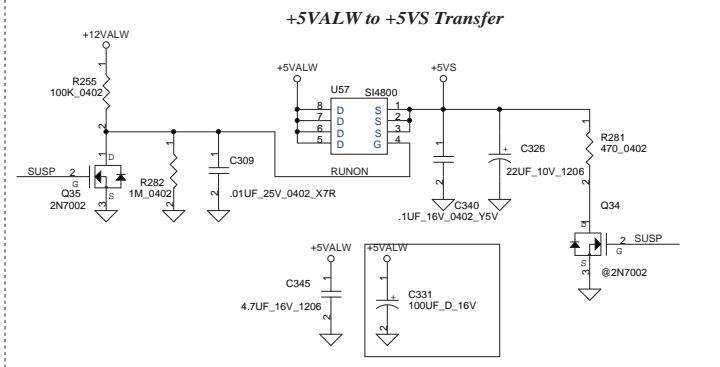
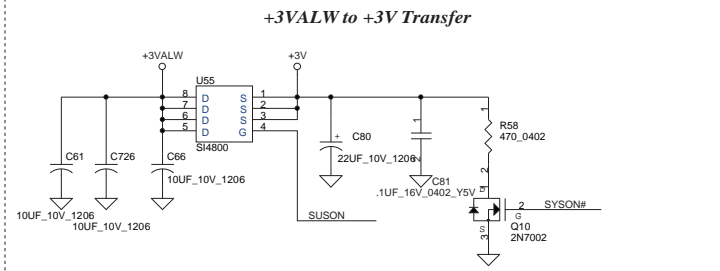
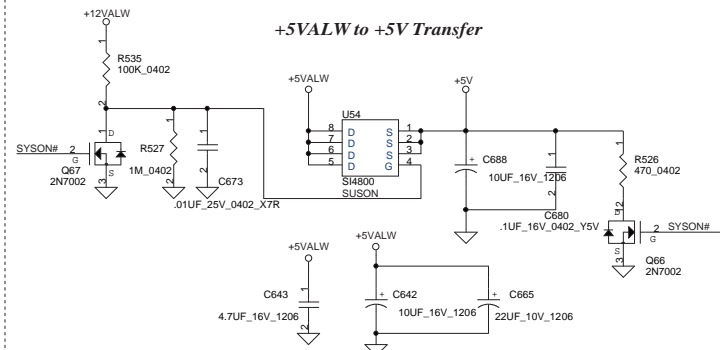
JP14			
KSI1	1	26	KSI1
KSI7	2	27	KSI7
KSI6	3	28	KSI6
KSO9	4	29	KSO9
KSI4	5	30	KSI4
KSI5	6	31	KSI5
KSO0	7	32	KSO0
KSI2	8	33	KSI2
KSI3	9	34	KSI3
KSO5	10	35	KSO5
KSO1	11	36	KSO1
KSI0	12	37	KSI0
KSO2	13	38	KSO2
KSO4	14	39	KSO4
KSO7	15	40	KSO7
KSO8	16	41	KSO8
KSO6	17	42	KSO6
KSO3	18	43	KSO3
KSO12	19	44	KSO12
KSO13	20	45	KSO13
KSO14	21	46	KSO14
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KSO15	24	49	KSO15
	25	50	

ACES85203-2502

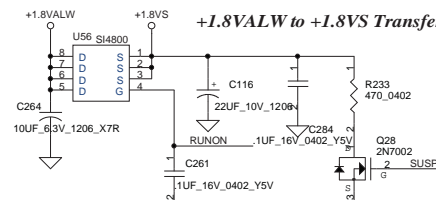


FOR VERSION A ONLY

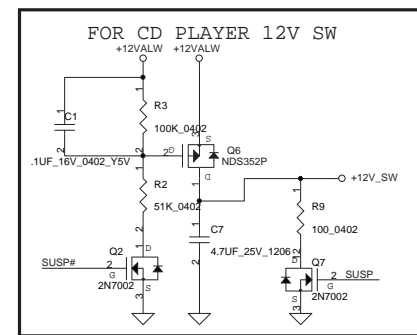
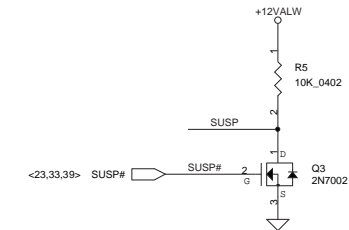
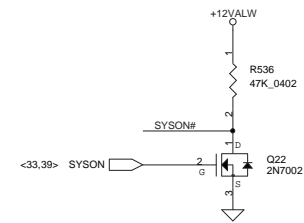
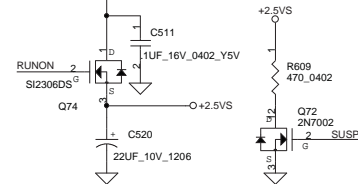




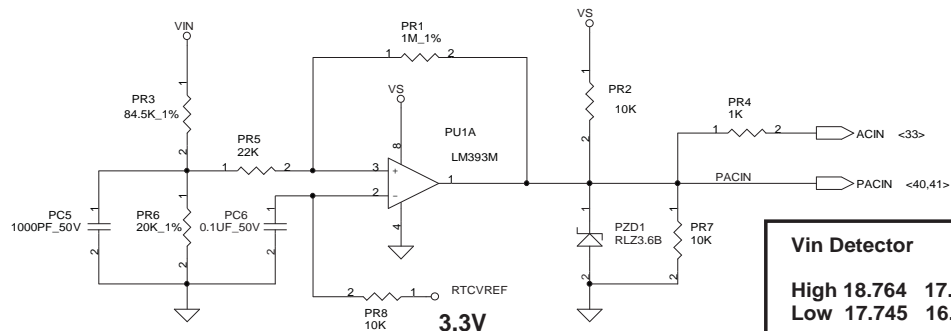
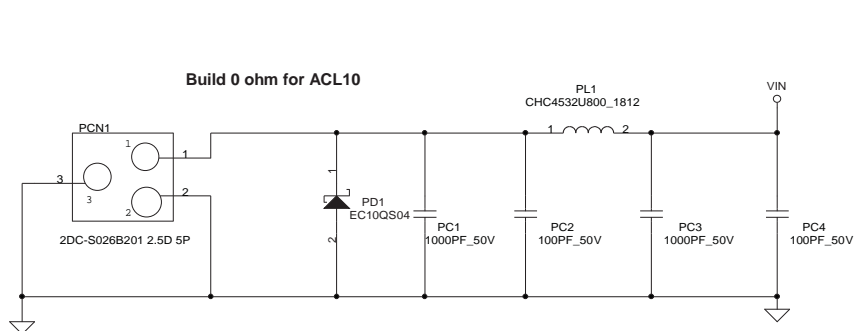
1.8VALW/+1.5VS Power direct provide



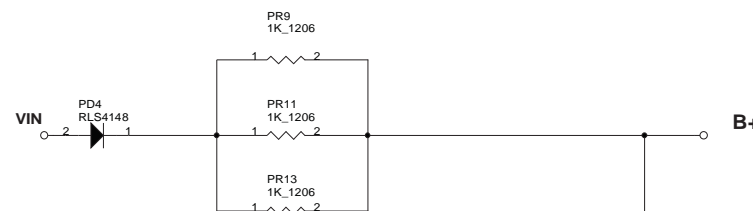
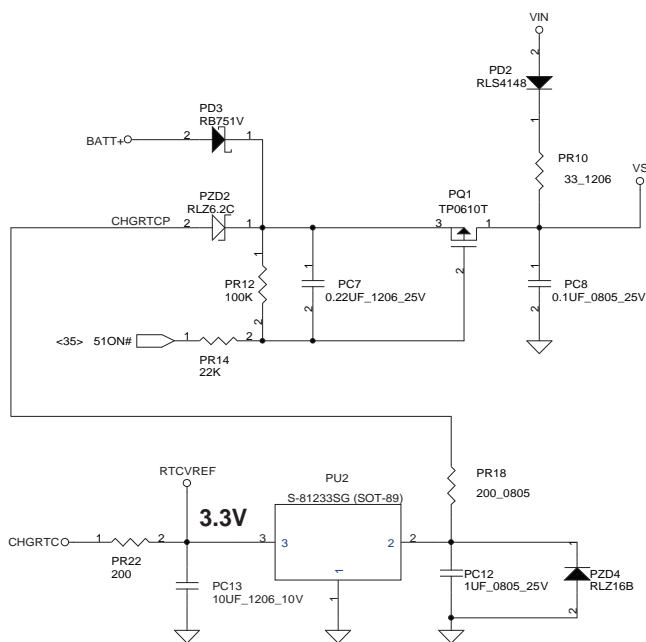
+2.5V to +2.5VS Transfer



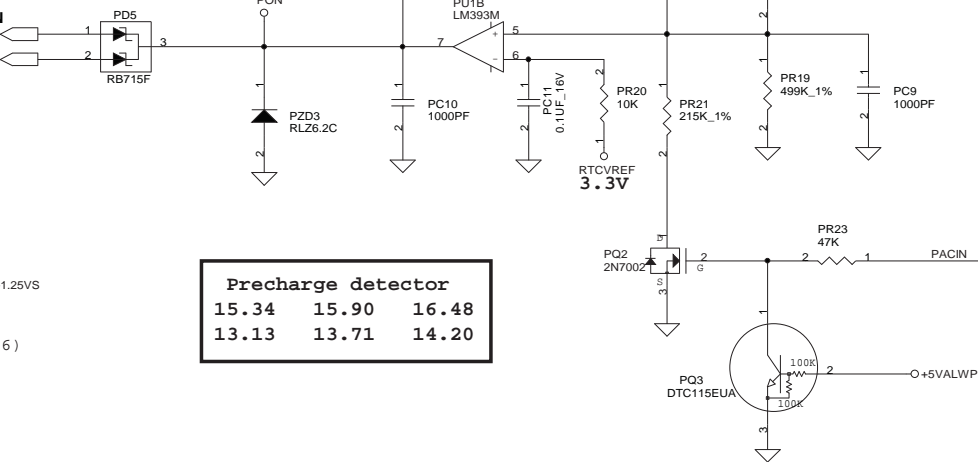
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Compal Electronics, Inc.			
DC/DC Circuit Interface			
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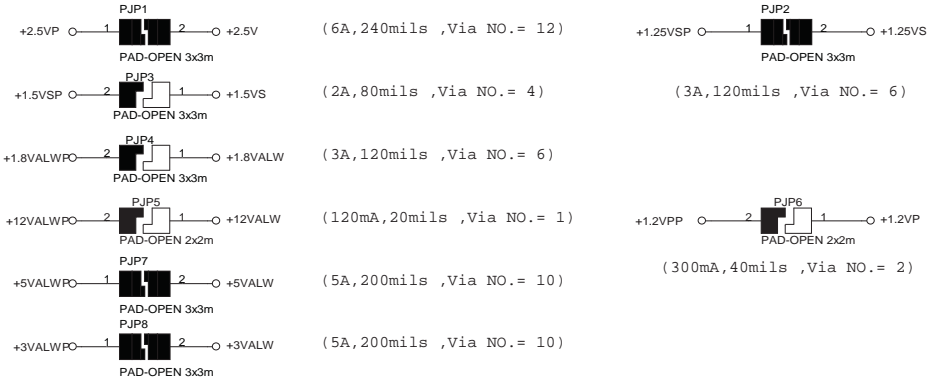
Vin Detector		
High	18.764	17.901
Low	17.745	16.038



<4,41,42> MAINPWON
<40> ACON

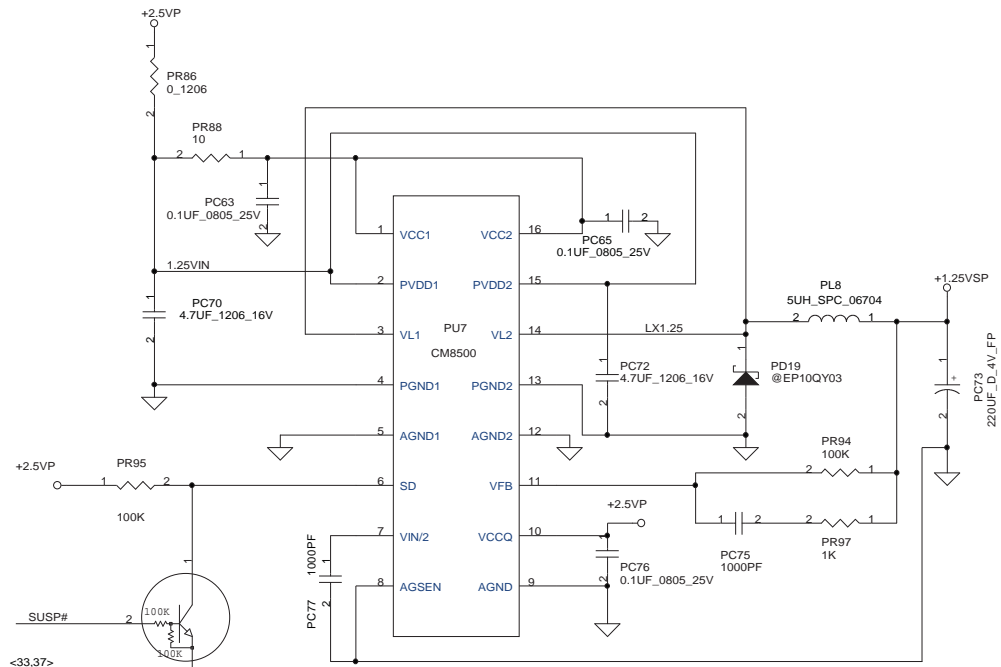
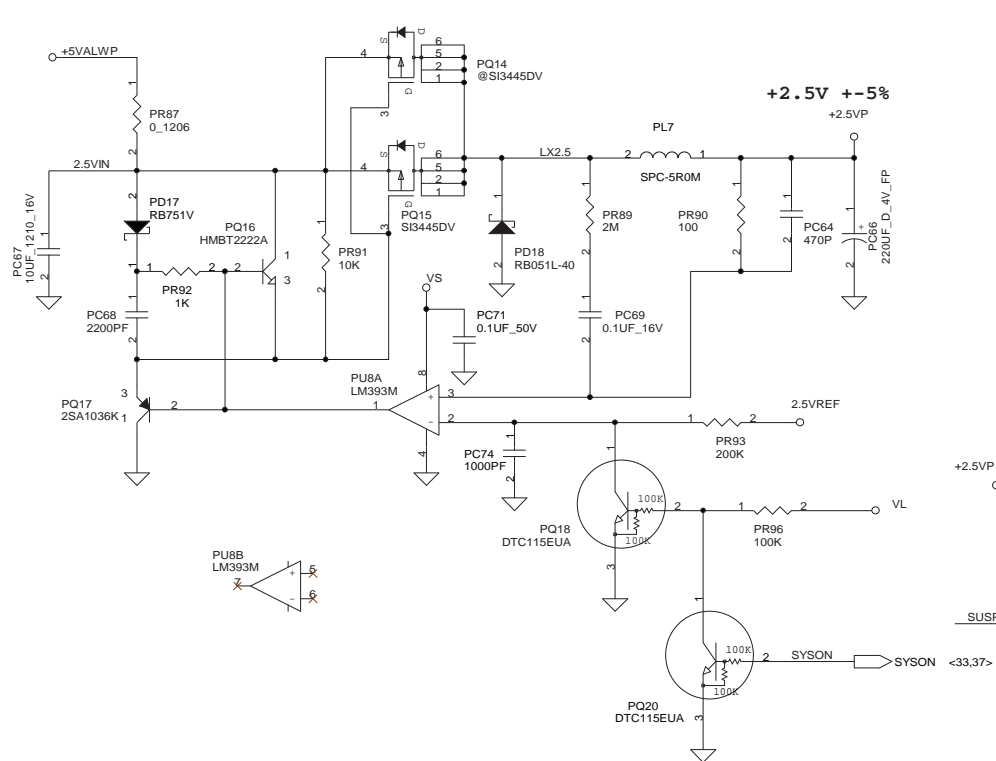


Precharge detector		
15.34	15.90	16.48
13.13	13.71	14.20

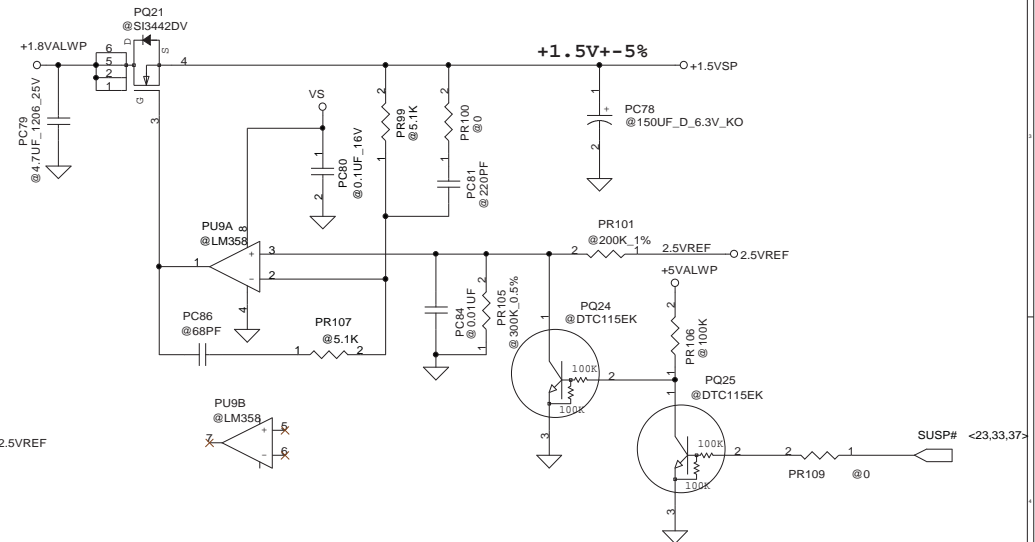
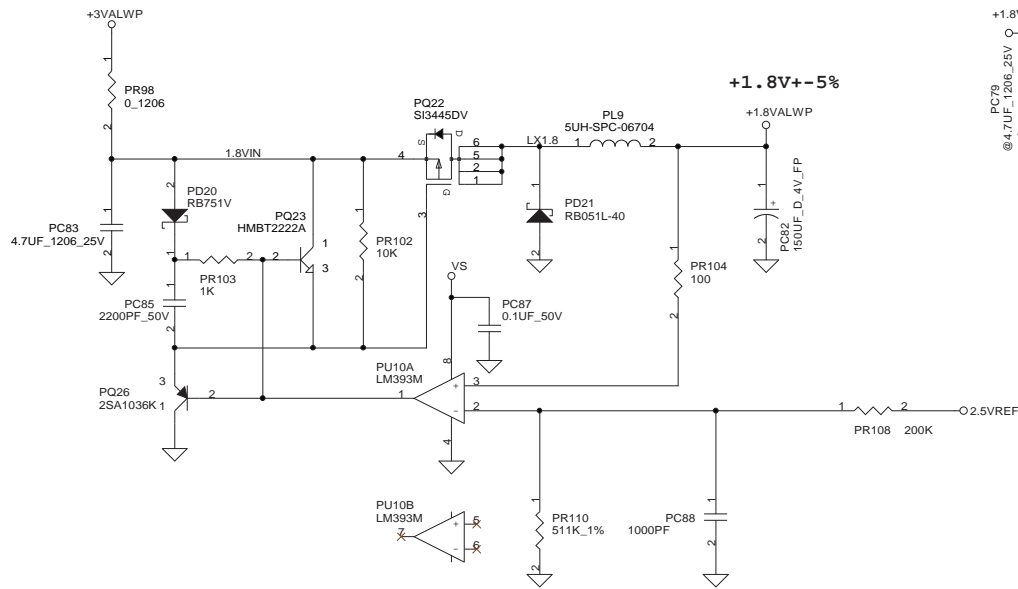


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COMPAL ELECTRONICS, INC		
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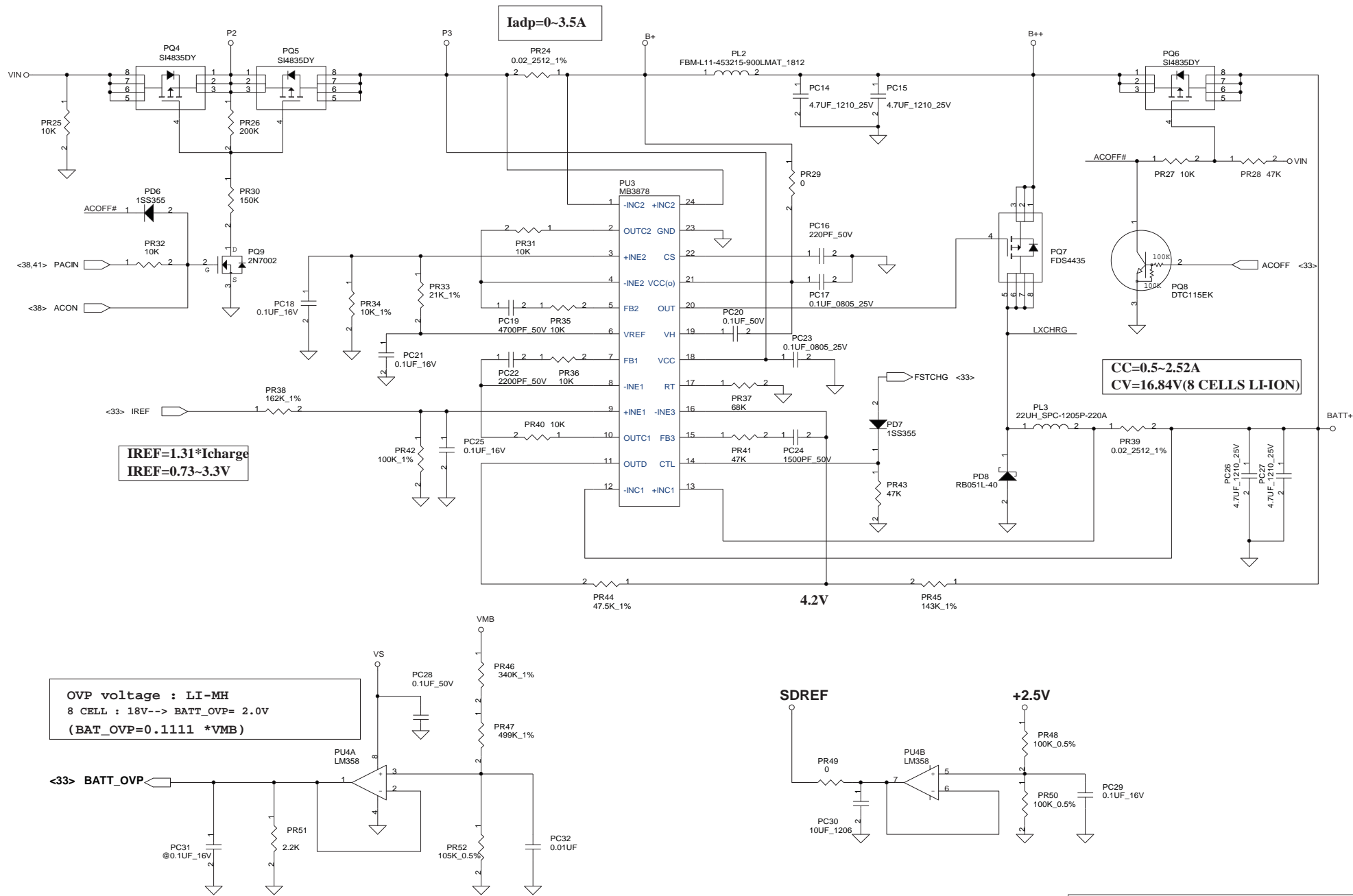


Layout : "Compensation network close to FB pin"



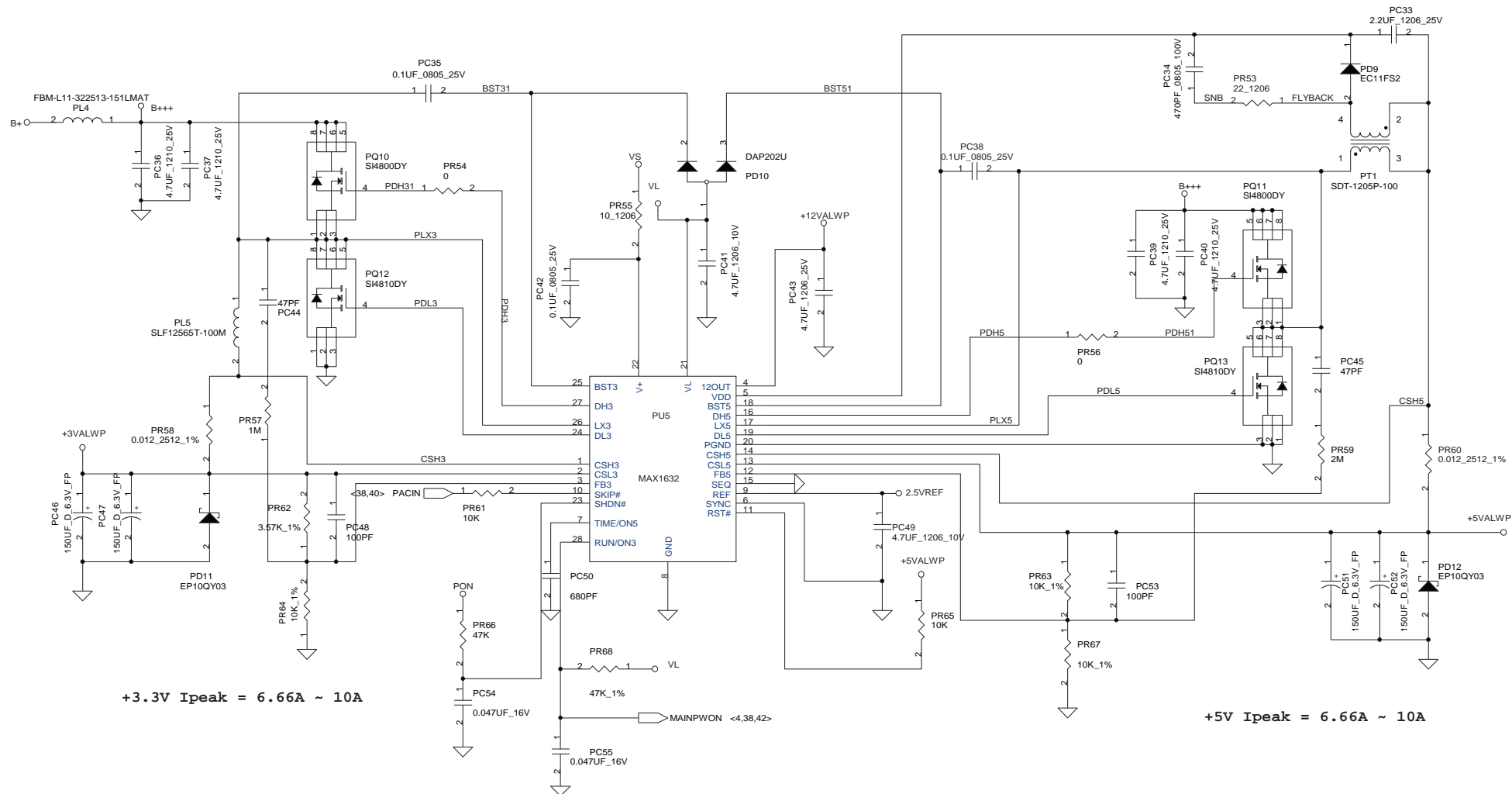
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COMPAL ELECTRONICS, INC			
Title	DDR /2.5V / 1.8V/1.25V		
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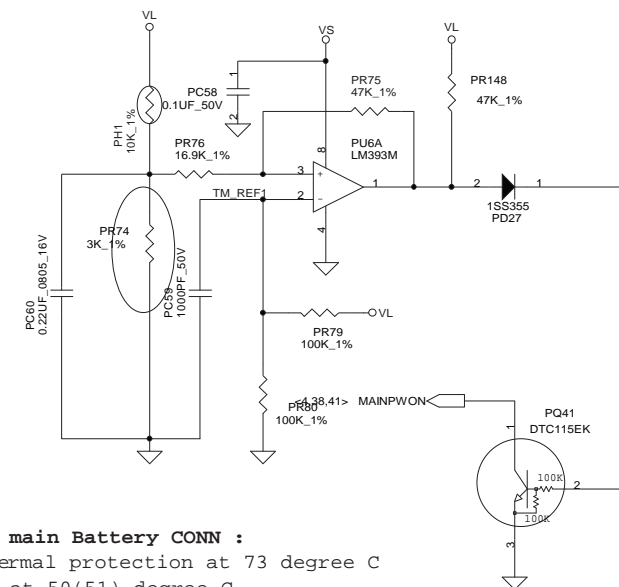
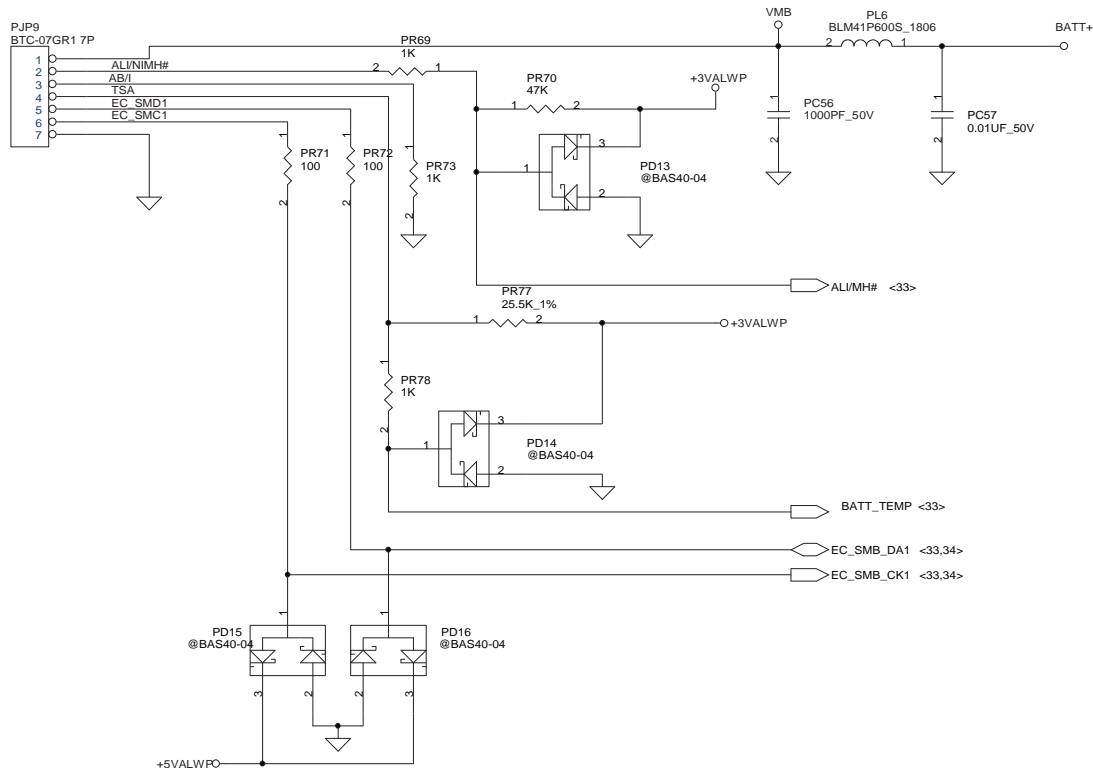
COMPAL ELECTRONICS, INC			
Title	CHARGER		
Size	Document Number	Rev	
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COMPAL ELECTRONICS, INC

Title
BATTERY CONN / OTP

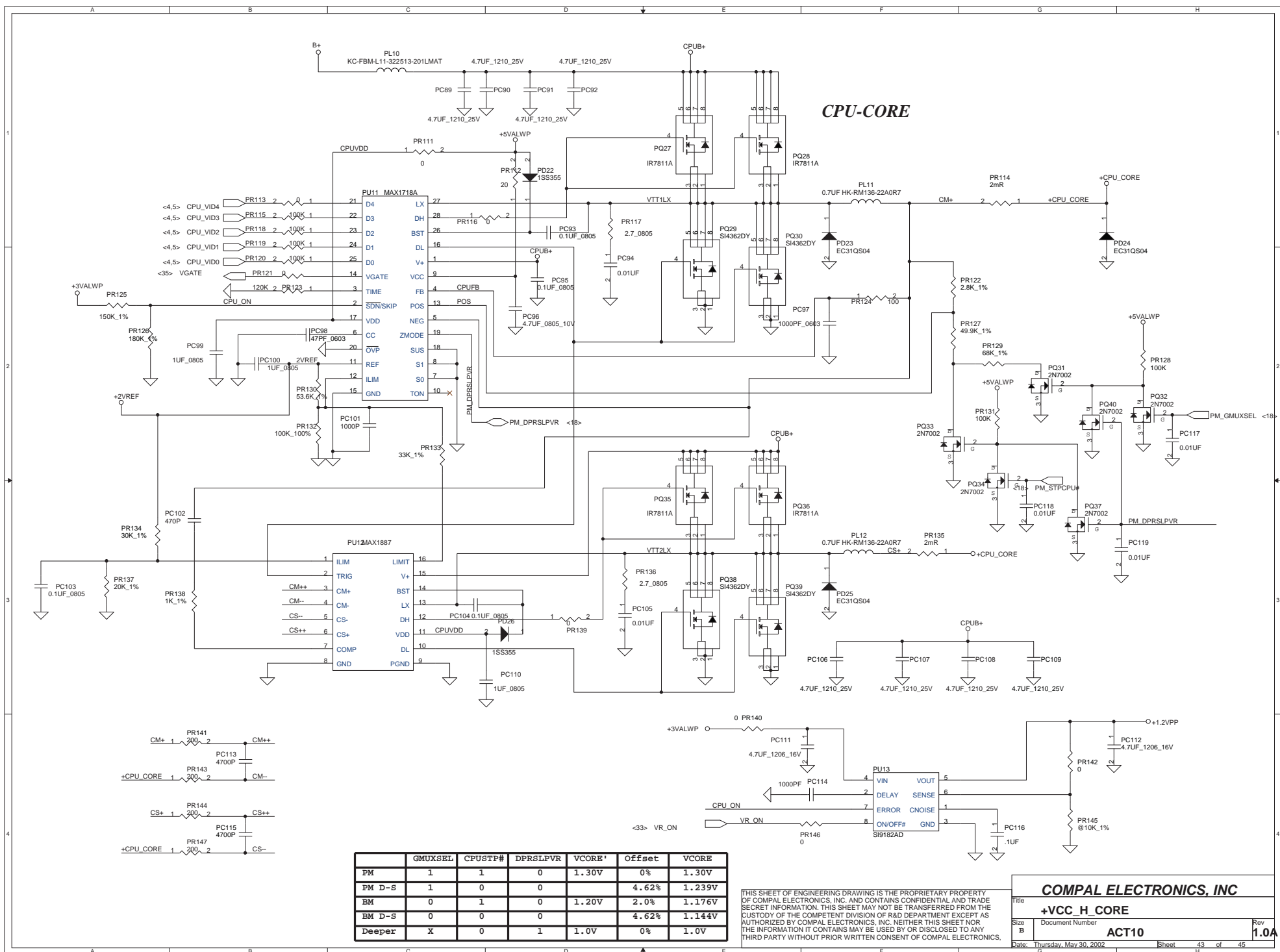
Size
B

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C

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A

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PCI MASTER :
1394 : REQ0#, GNT0#
MINI-PCI(Wireless Lan) : REQ1#, GNT1#
CARDBUS : REQ2#, GNT2#
LAN : REQ3#, GNT3#
MINI-PCI : REQ4#, GNT4#
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PCI MASTER :
1394 : REQ0#, GNT0#
MINI-PCI(Wireless Lan) : REQ1#, GNT1#
CARDBUS : REQ2#, GNT2#
LAN : REQ3#, GNT3#
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Compal Electronics, Inc.			
Title			
Note & Revision			
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