

# Compal Confidential

## NAWF2 M/B Schematics Document

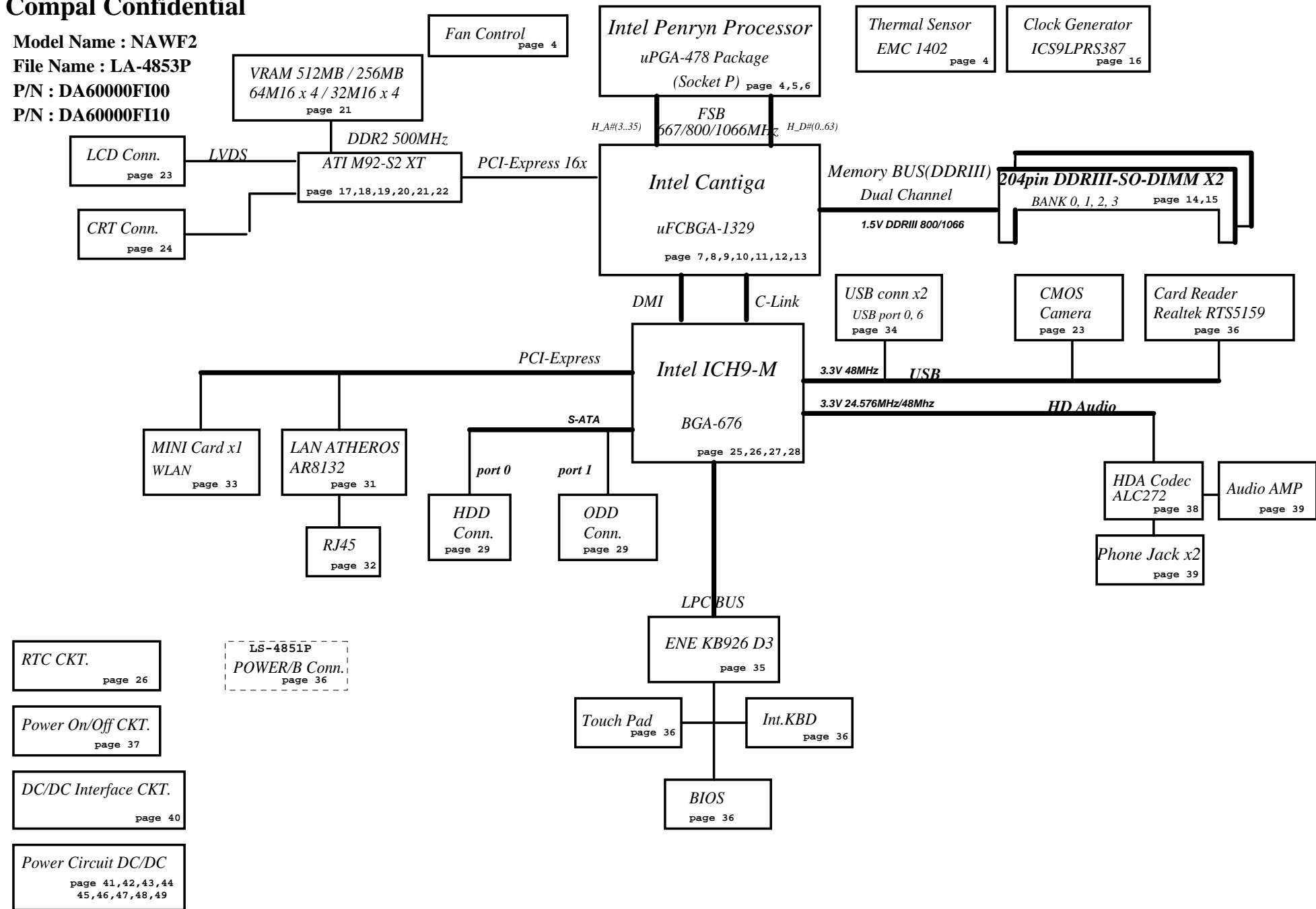
Intel Penryn Processor with Cantiga + DDRIII + ICH9M+M92-S2 XT

2009-09-17

REV:1.0

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**Model Name : NAWF2**  
**File Name : LA-4853P**  
**P/N : DA60000FI00**  
**P/N : DA60000FI10**



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for GMCH LVDS	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC 1402-1	1001 100X b
EEPROM(24C16/02)	1010 000X b	GMT G781-1	1001 101X b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4				
5				
6				
7				

BOARD ID Table

Board ID	PCB Revision
0	
1	0.1(PVT2)
2	1.0(Pre-MP)
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45	GM@
8132	8132@

PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

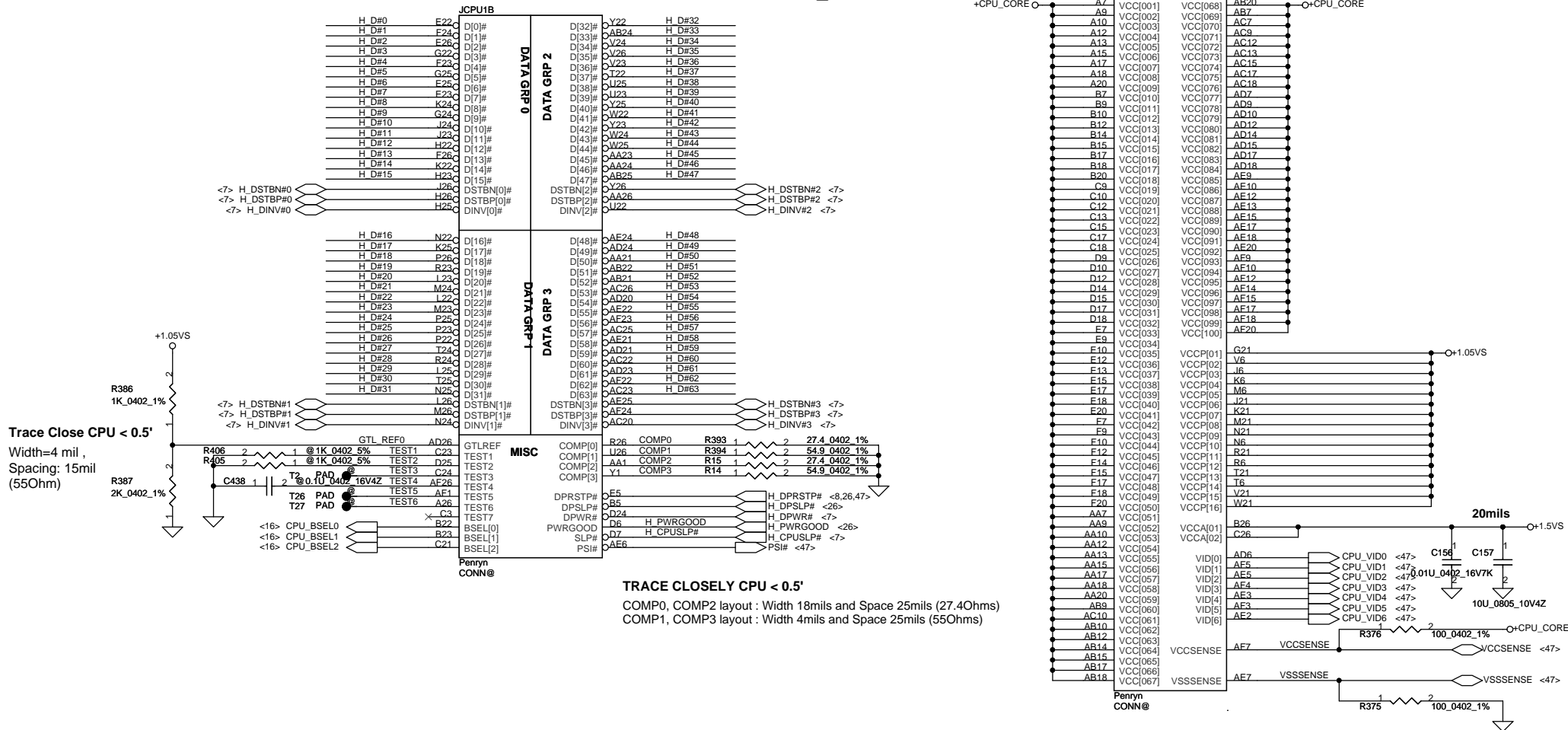
SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

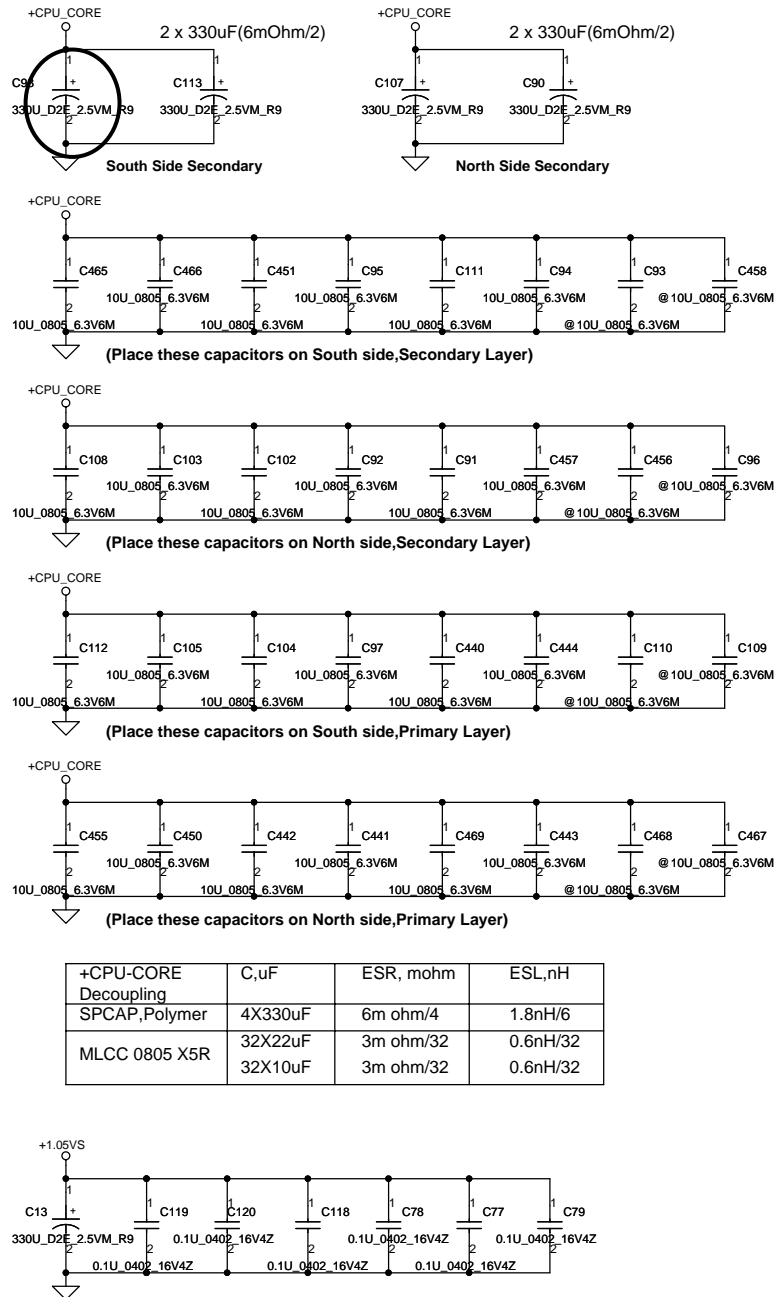
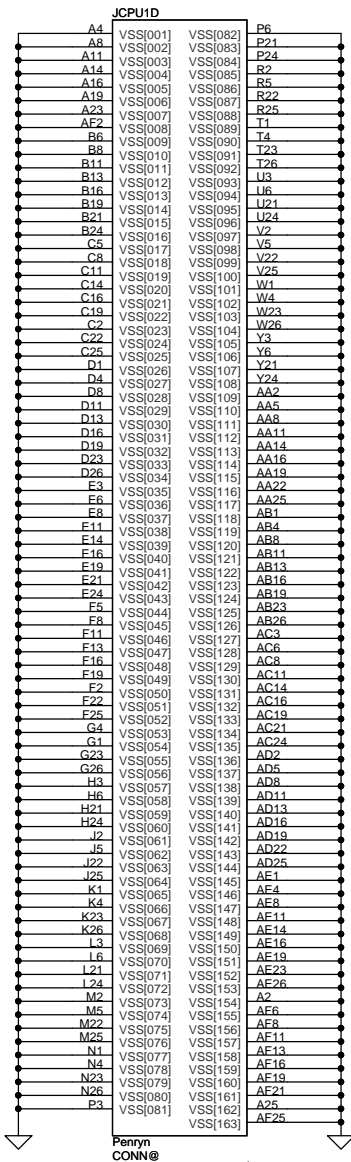
USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	
	UHCI2	Port2	
		Port3	CMOS Camera
	UHCI3	Port4	Card Reader
EHCI2		Port5	
		Port6	MB USB Conn.
	UHCI4	Port7	
		Port8	
	UHCI5	Port9	
		Port10	Wireless Card
	UHCI6	Port11	

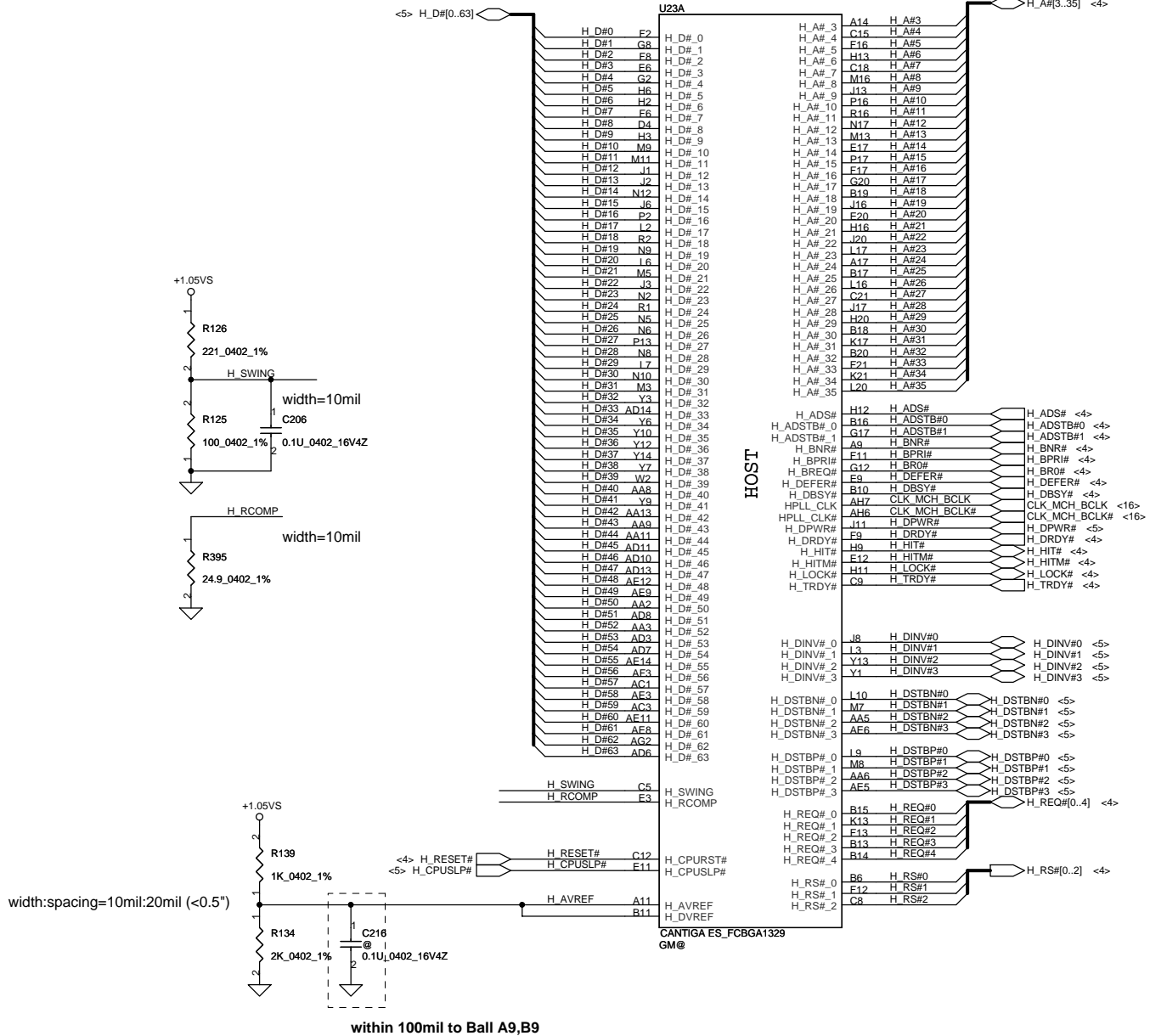




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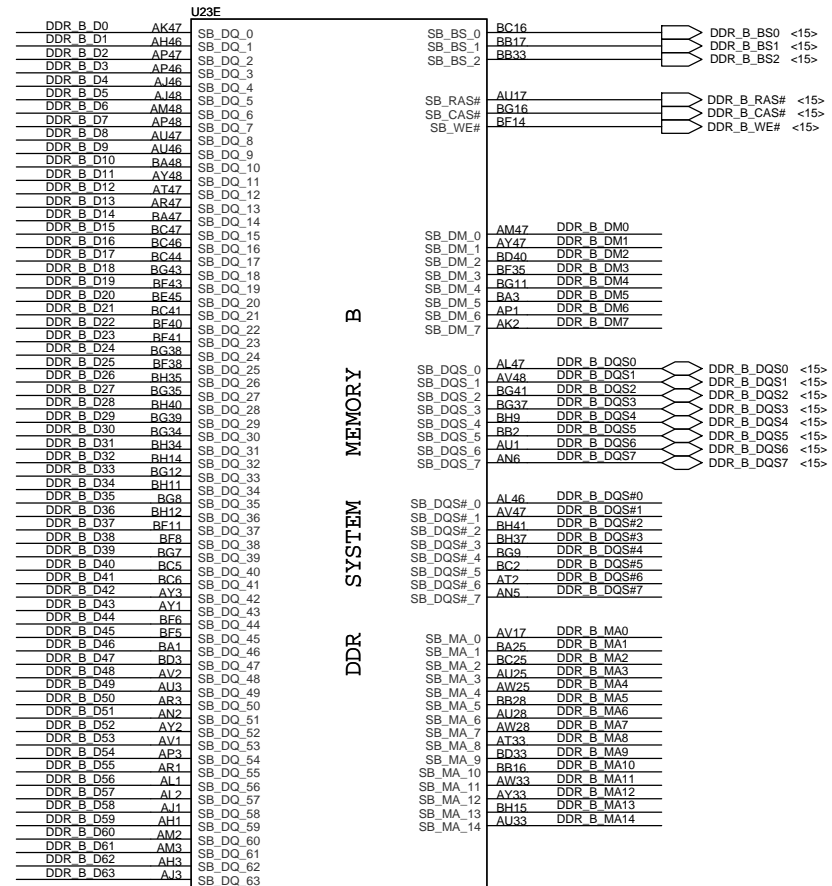
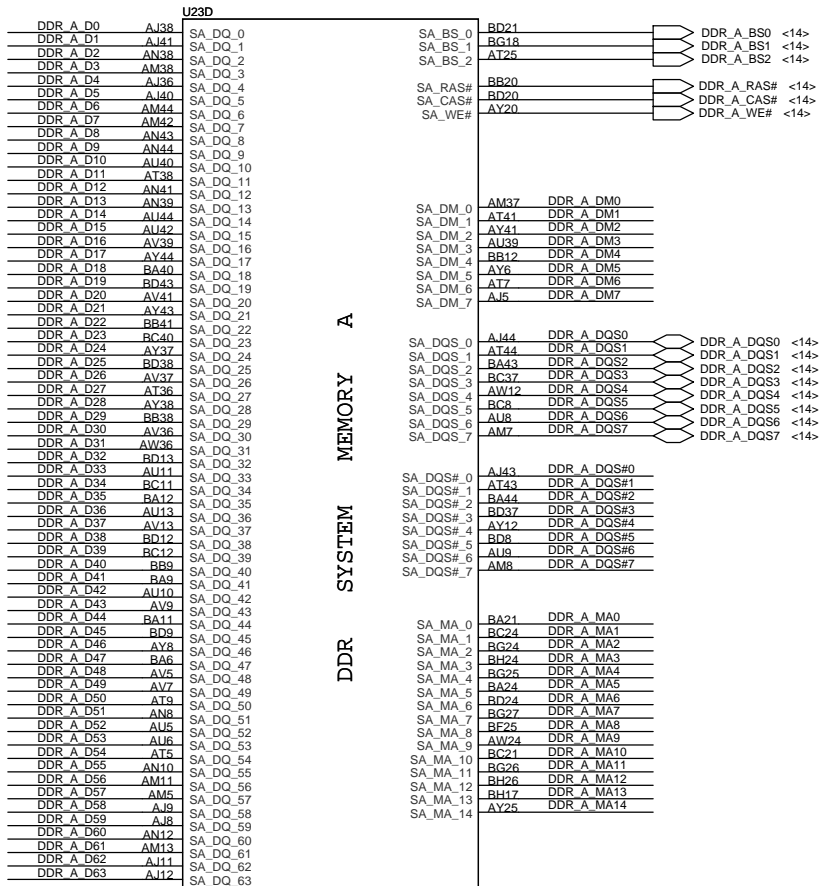
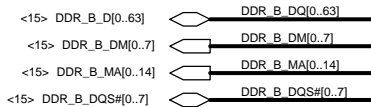
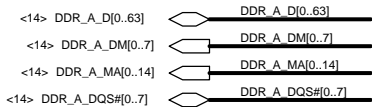
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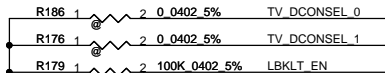


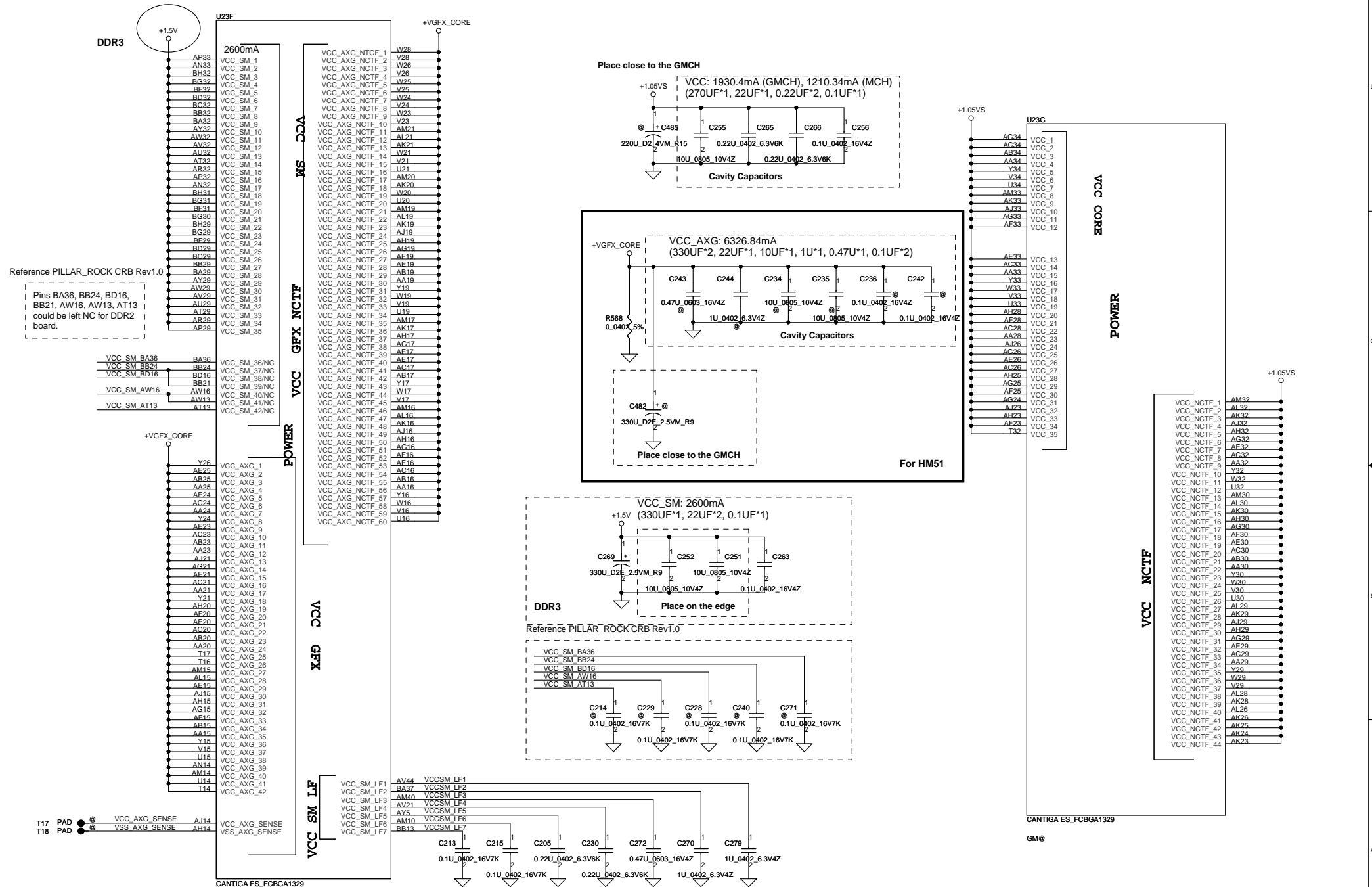
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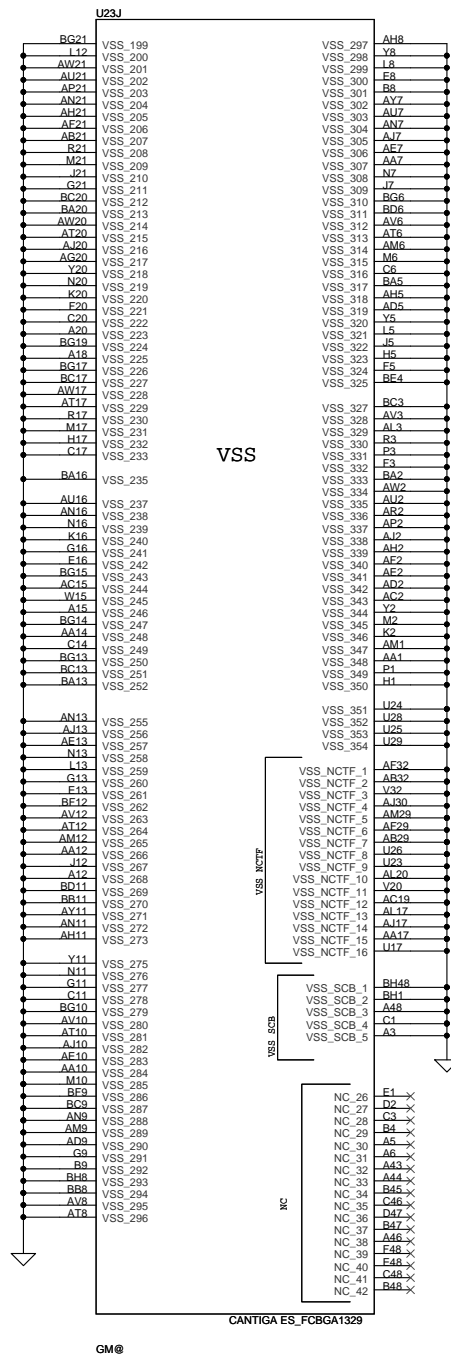
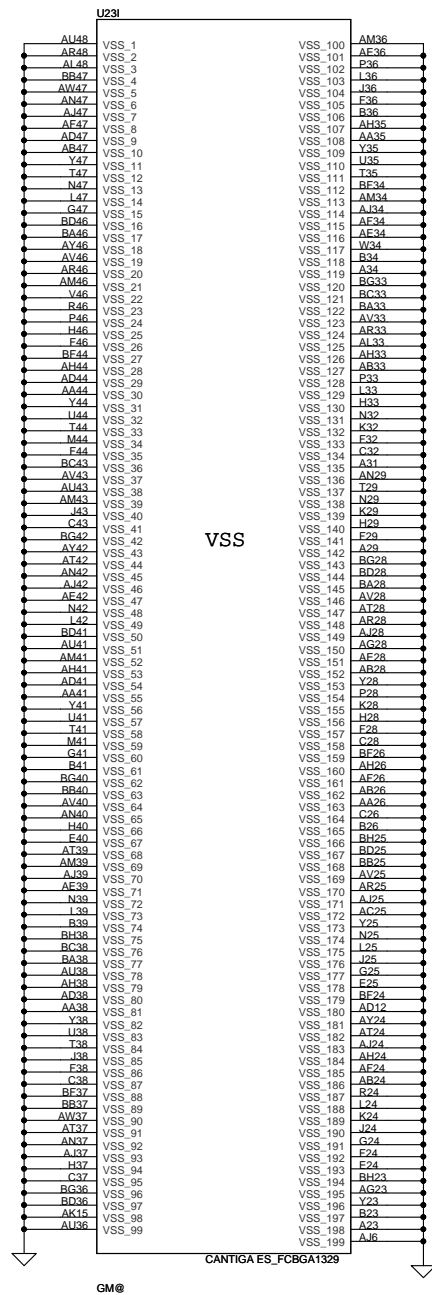




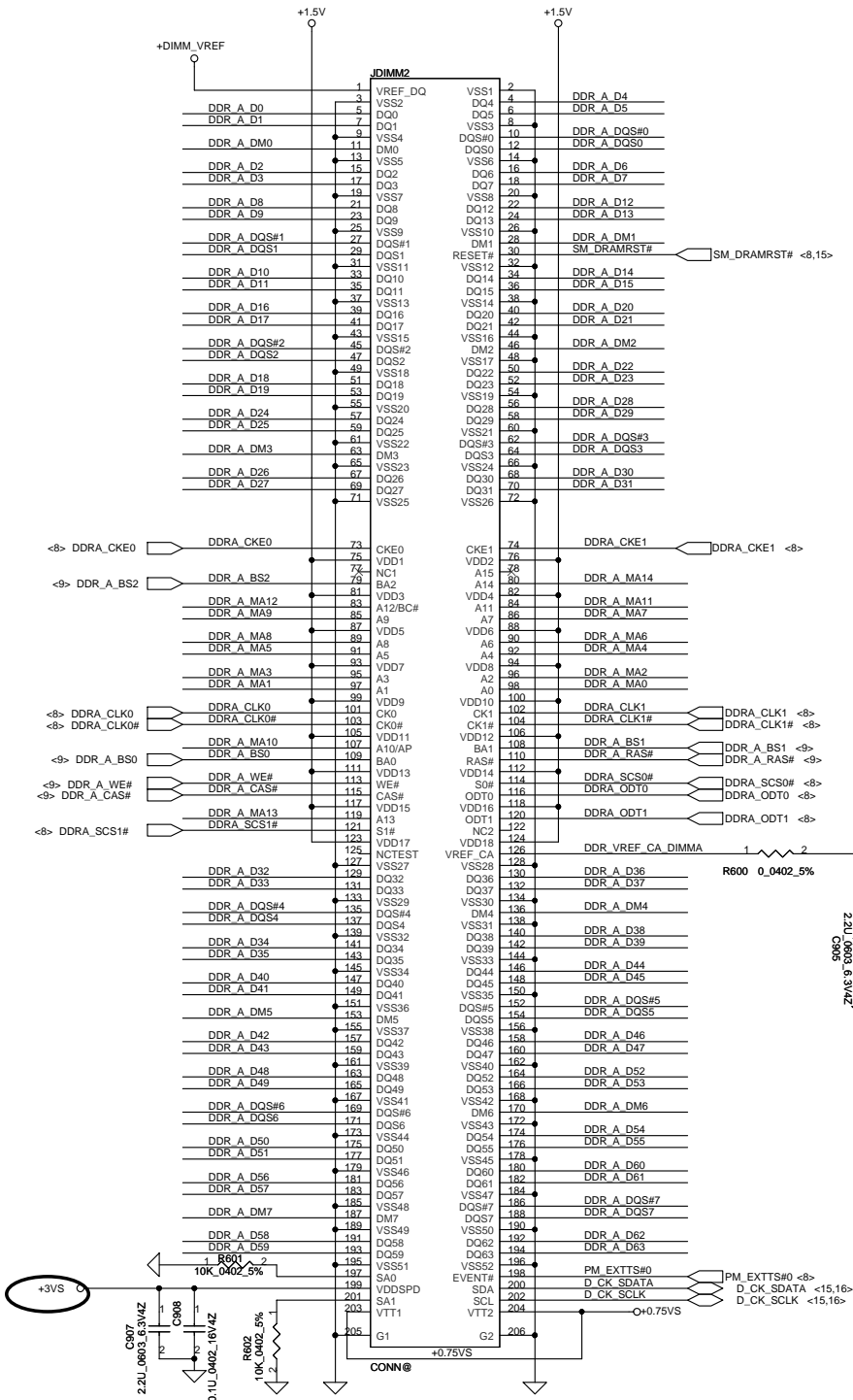








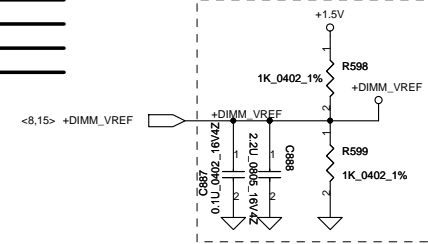
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DIMM0 REV H:5.2mm (BOT)

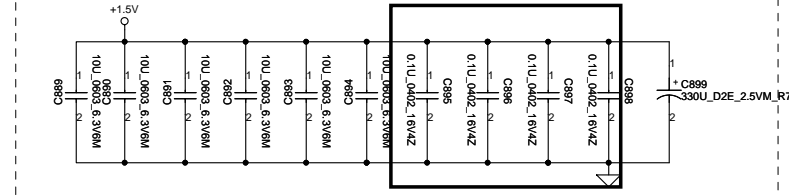
WWW.AliSaler.Com

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<8> DDR\_A\_MA[0..14]

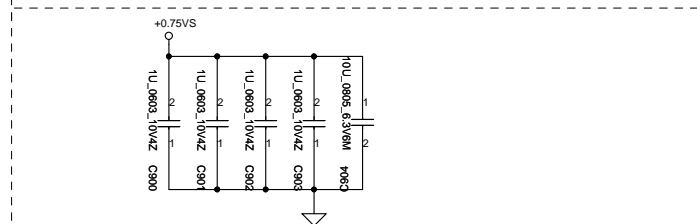


Layout Note:  
Place near JDIMM2

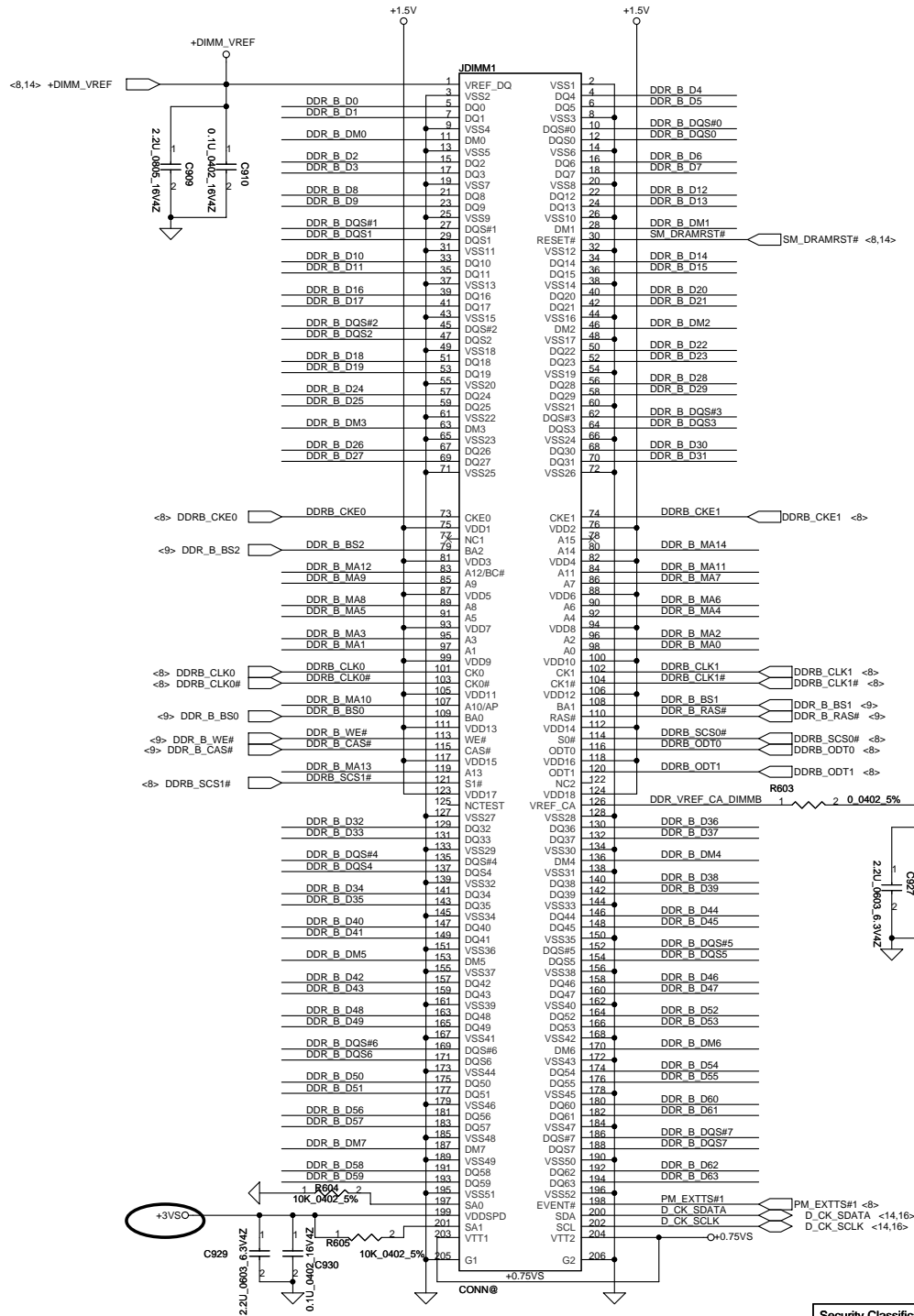
Layout Note: Place these 4 Caps near Command  
and Control signals of -DIMMA-



Layout Note:  
Place near JDIMM2.203 & JDIMM2.204



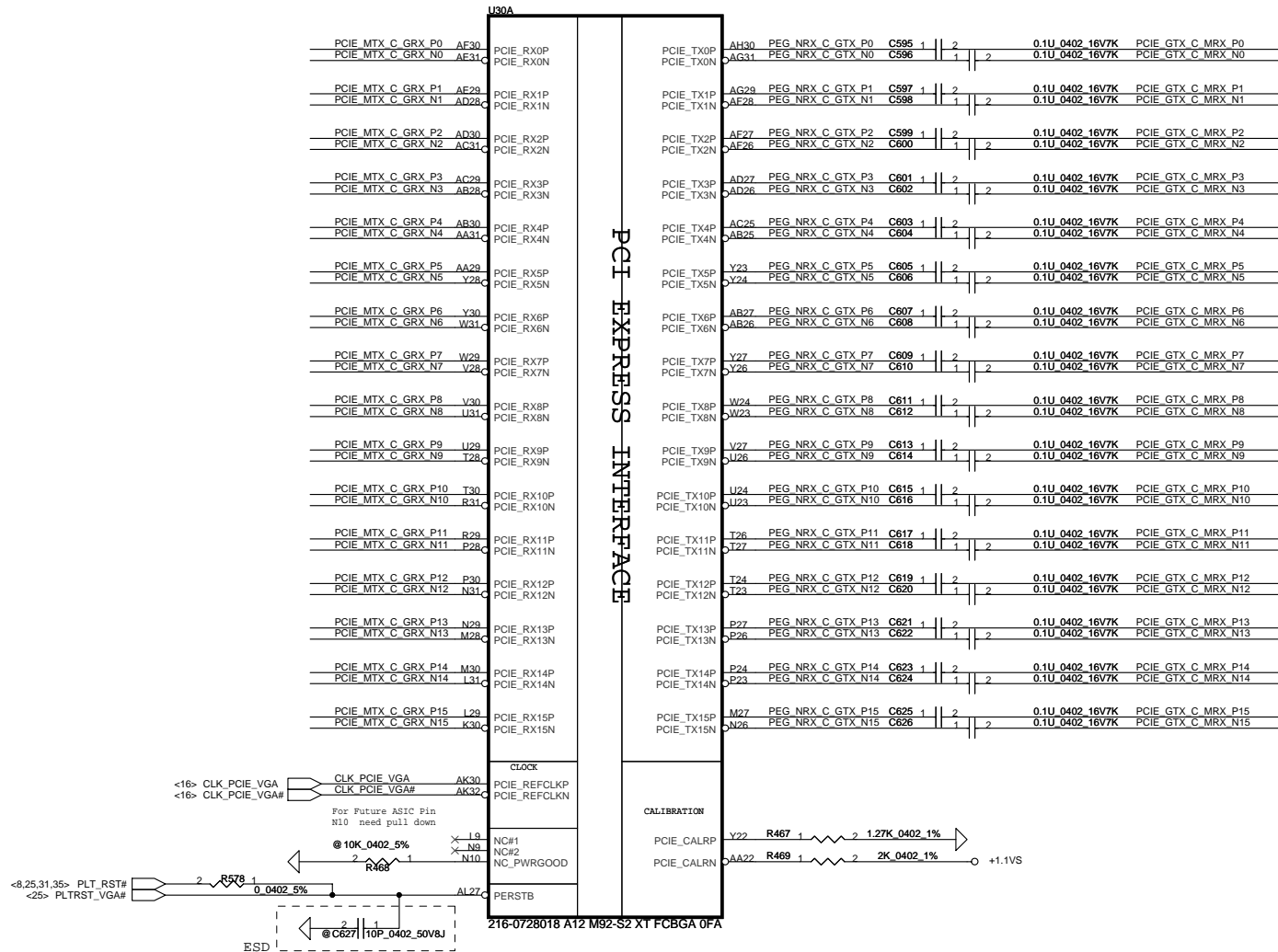
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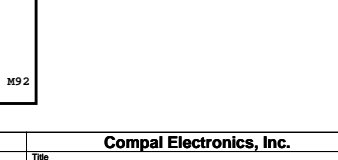
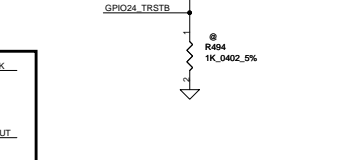
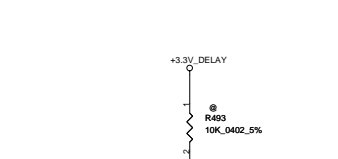
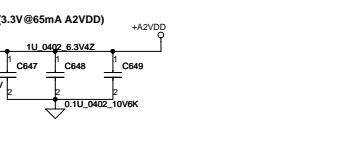
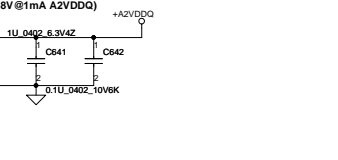
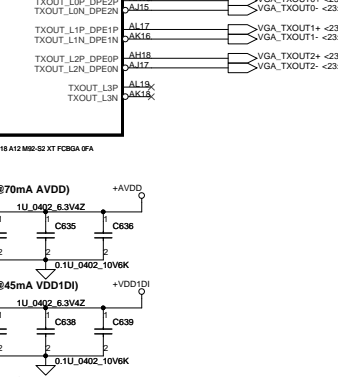
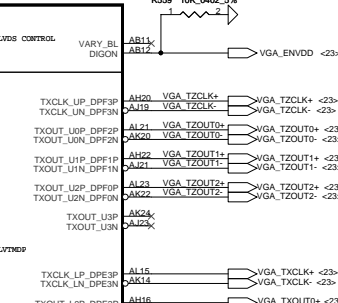
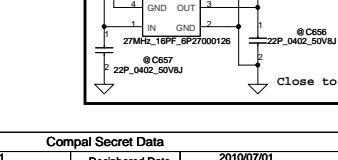
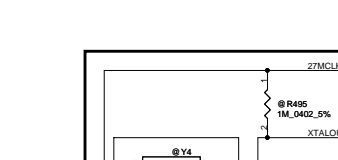
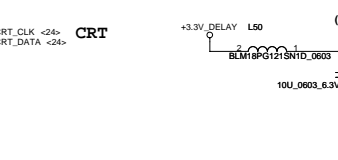
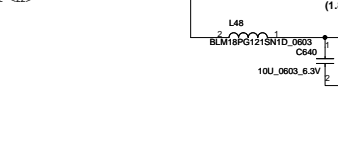
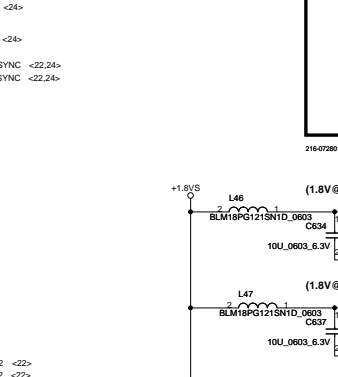
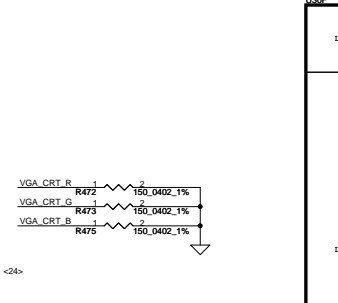
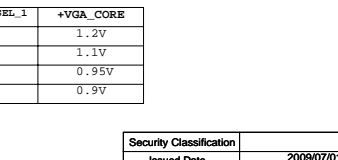
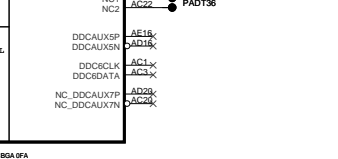
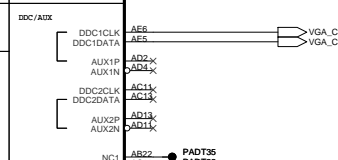
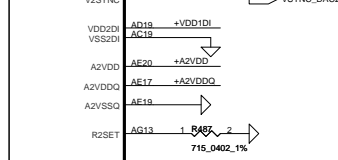
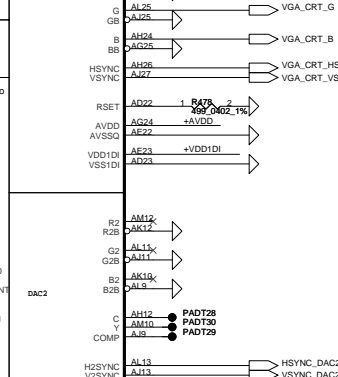
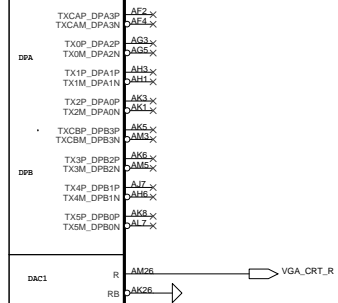
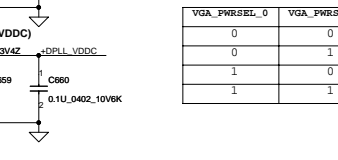
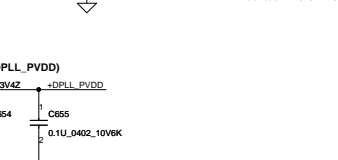
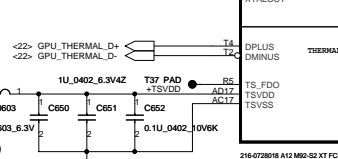
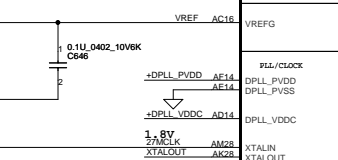
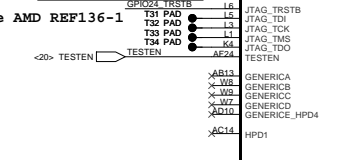
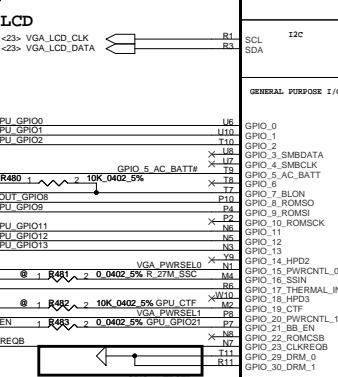
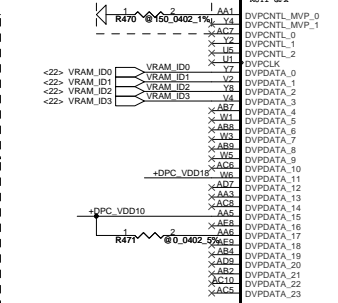
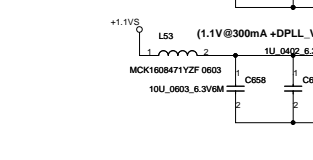
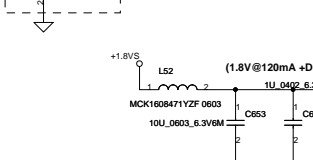
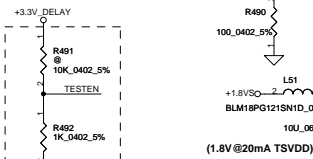
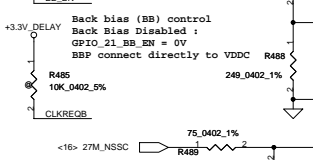
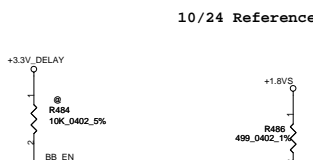
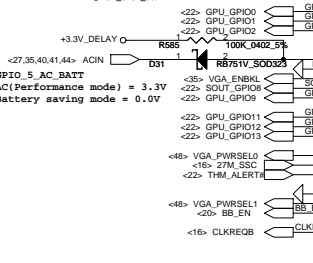




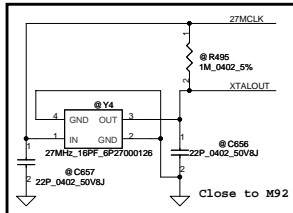
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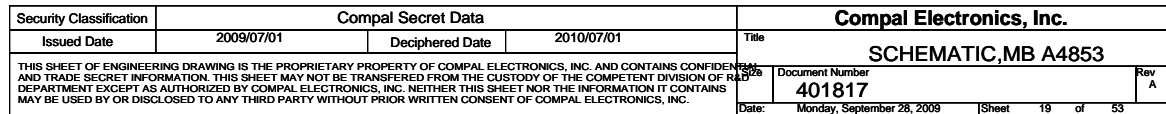
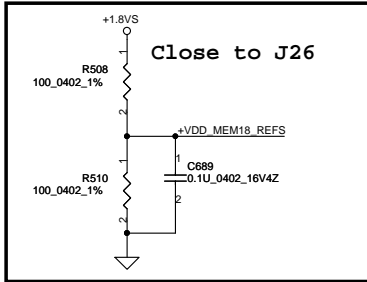


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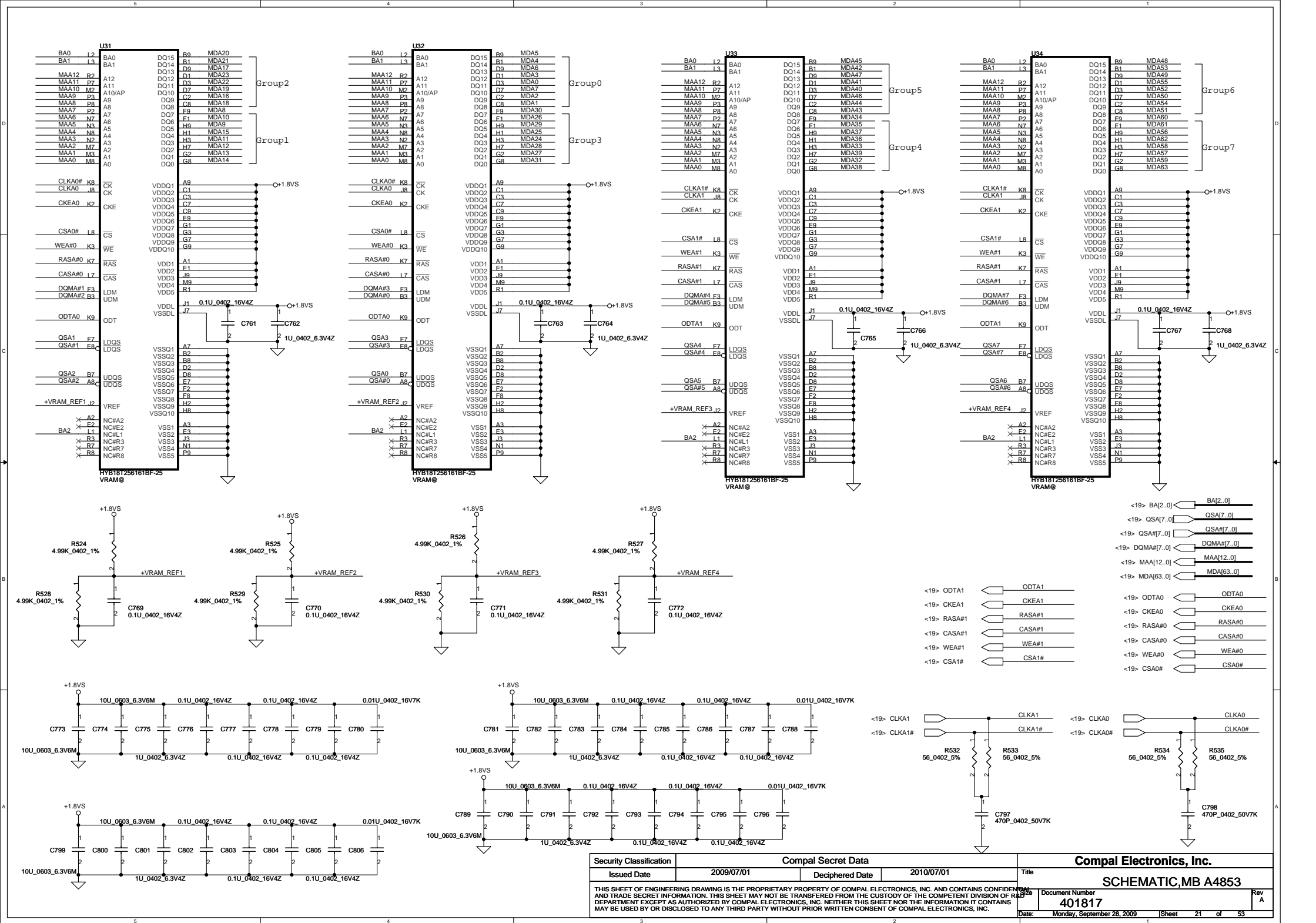


VGA_PWRSEL_0	VGA_PWRSEL_1	+VGA_CORE
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V

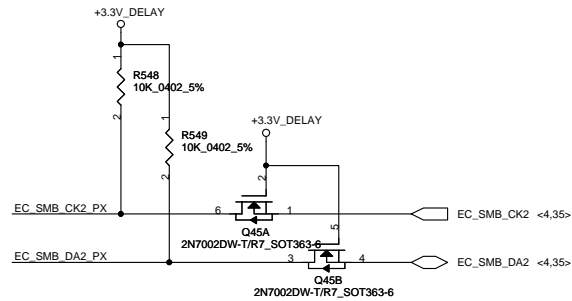
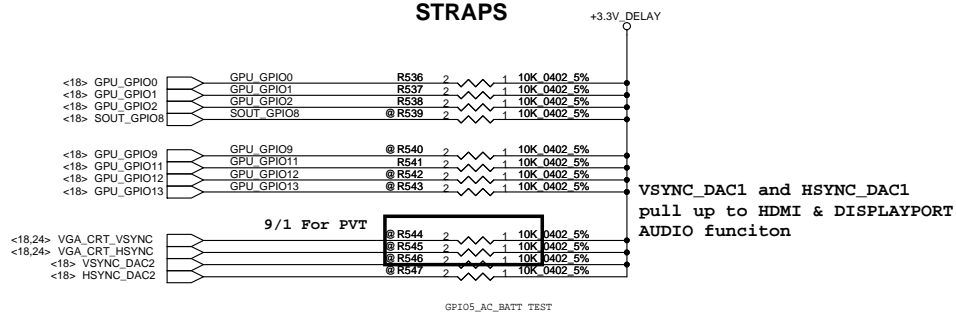




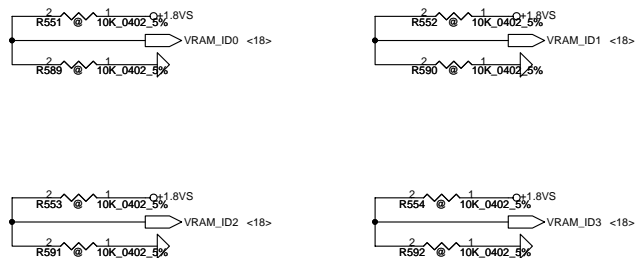
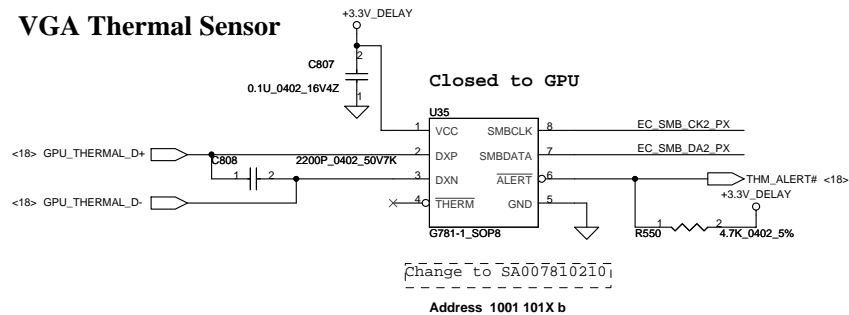




## STRAPS



## VGA Thermal Sensor



## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		1
ROMIDCFG2(0)	GPIO[13:11]	BIF_RX_PLL_CALIB_BP	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	ENABLE EXTERNAL BIOS ROM	0
SMS_EN_HARD	H2SYNC	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

## AMD RESERVED CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

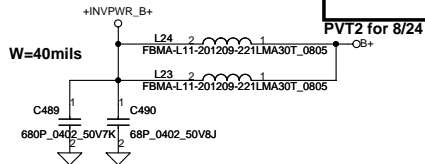
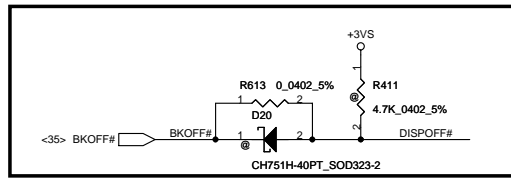
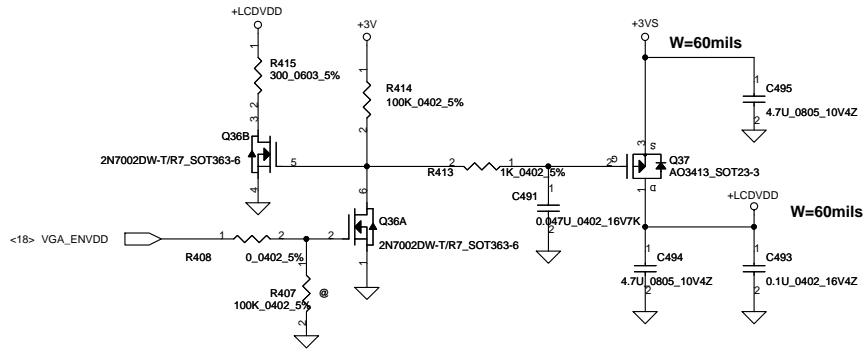
H2SYNC	GENERICC
<p><b>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
GPIO_28_TDO	GPIO21_BB_EN

```
VRAM_ID0=VRAM_ID0_0
VRAM_ID1=VRAM_ID1_1
VRAM_ID2=VRAM_ID2_2
VRAM_ID3=VRAM_ID3_3
```

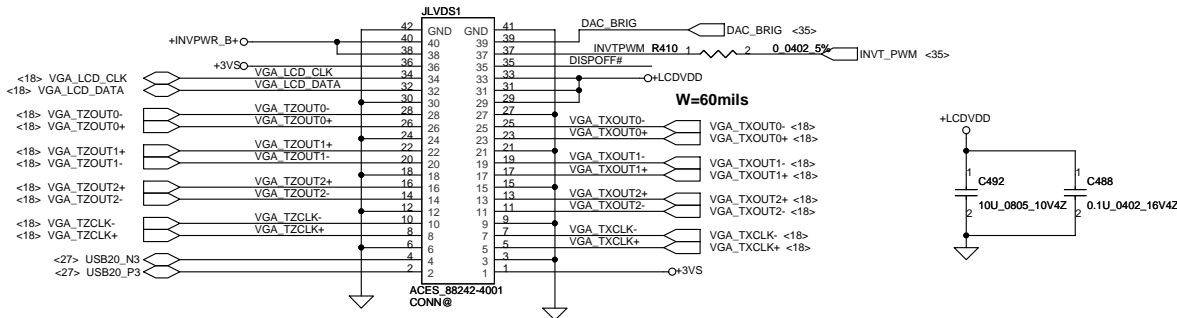
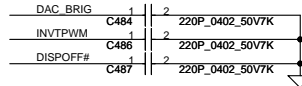
STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0	
VRAM_ID[3:0]	DVPDATA (3,2,1,0)	M92 S2-XT		256MB(x4)	Hynix 32Mx16 1.8V	SA00002DL10	1 0 0 0	
				512MB(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1	
				512MB(x4)	ATI 64Mx16 1.8V	SA00003LT10	0 0 1 0	
				512MB(x4)	Samsung 64Mx16 1.8V (E-die)	SA00003O10	0 1 0 0	

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## LCD POWER CIRCUIT

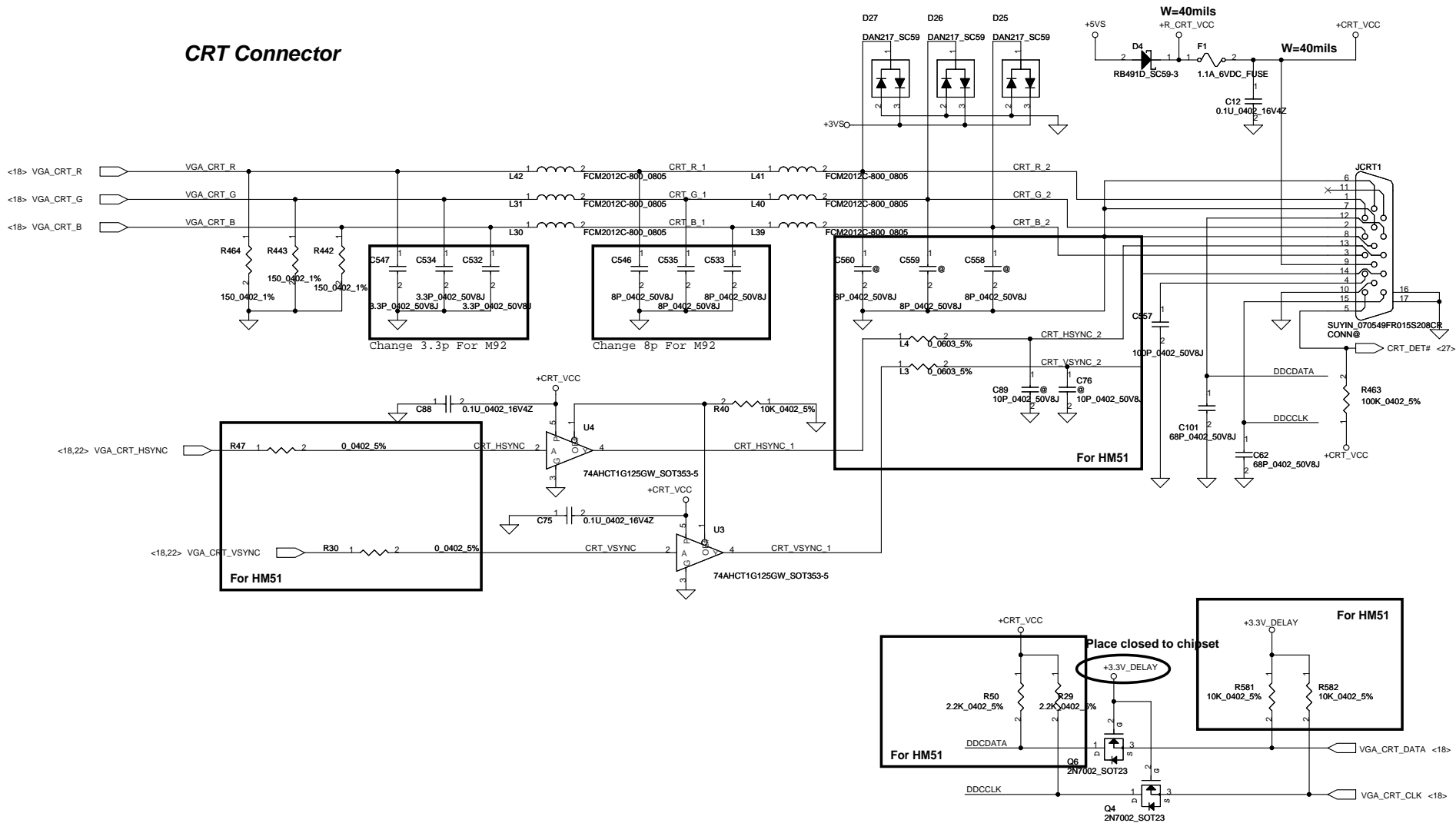


## LCD/PANEL BD. Conn.



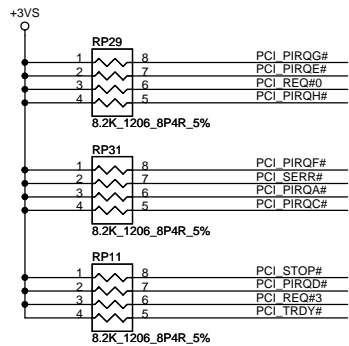
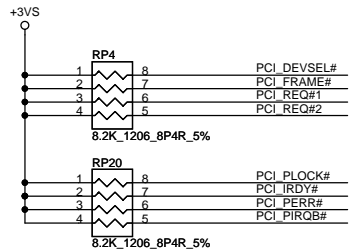
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## CRT Connector

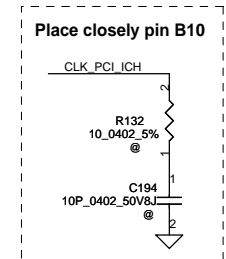
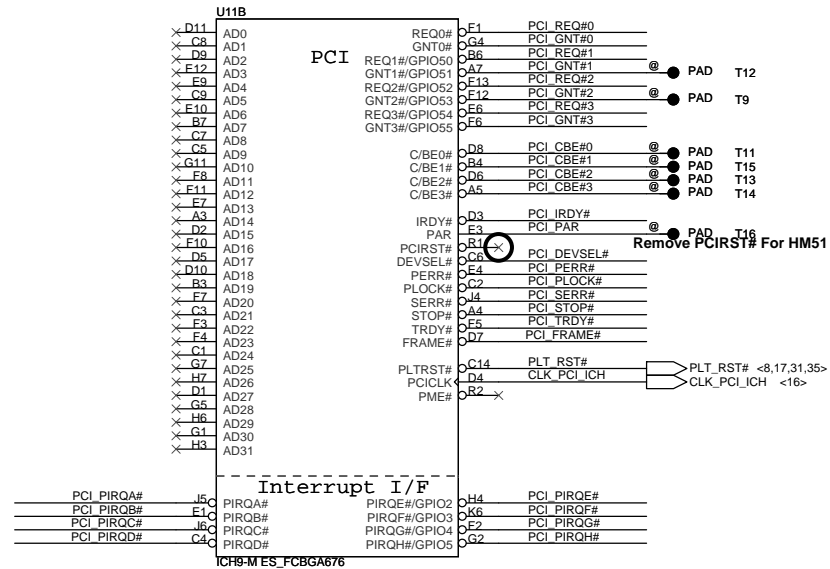


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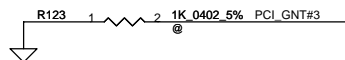




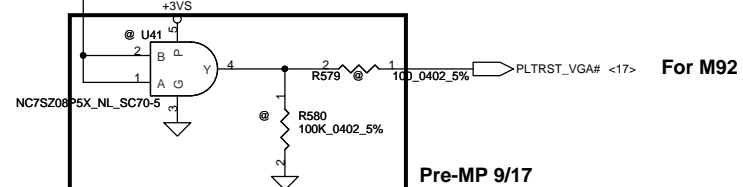
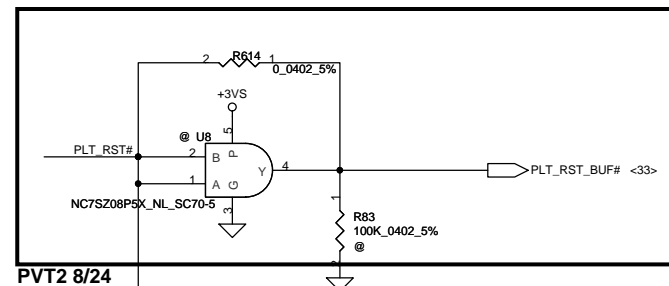
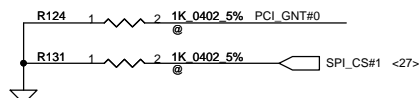
DMI for ESI-compatible operation	
PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)



A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

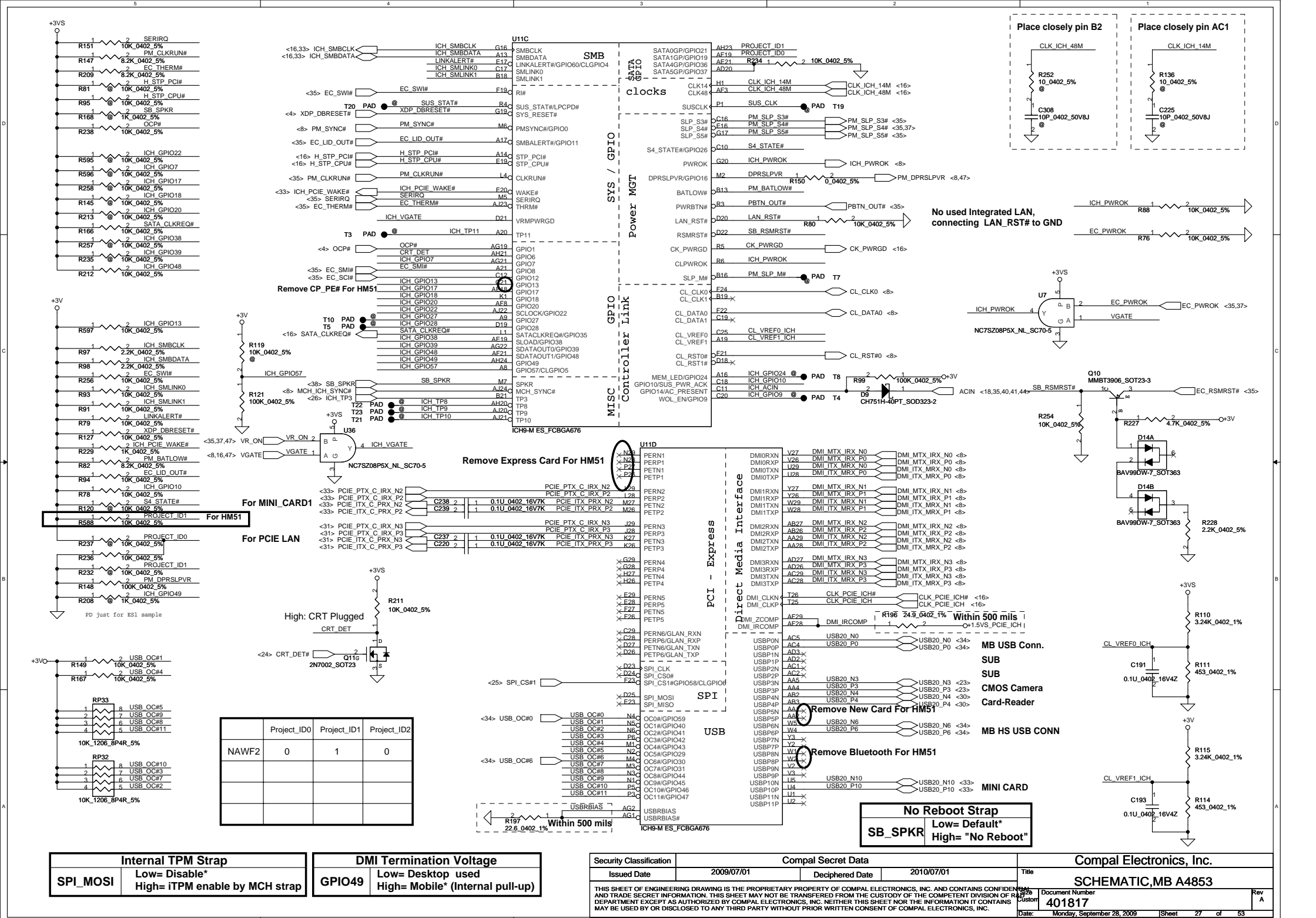


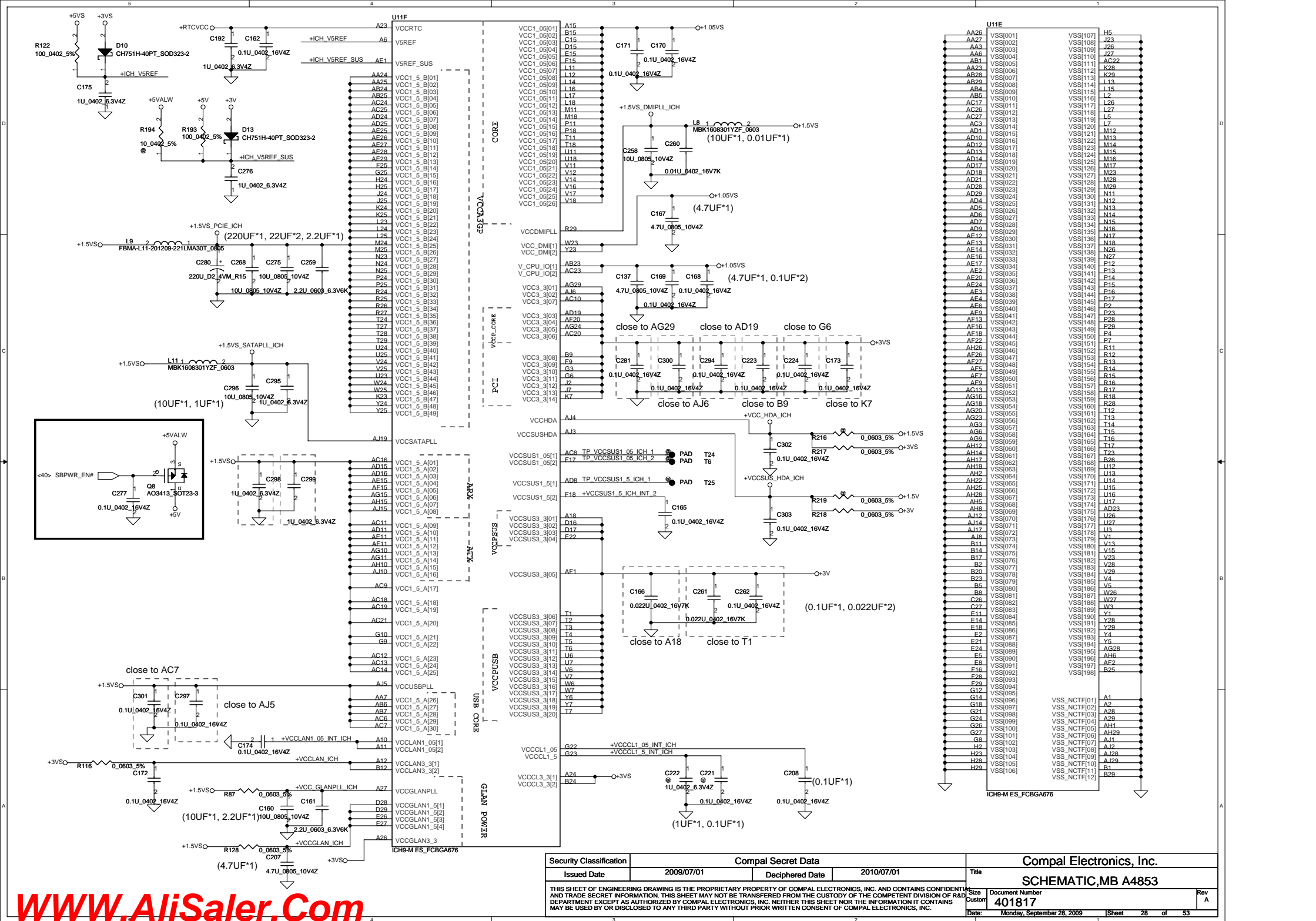
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

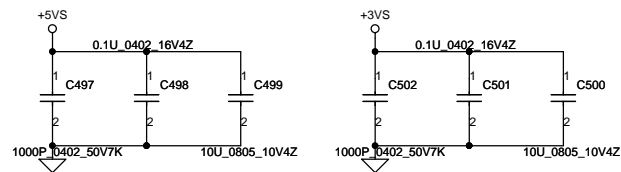


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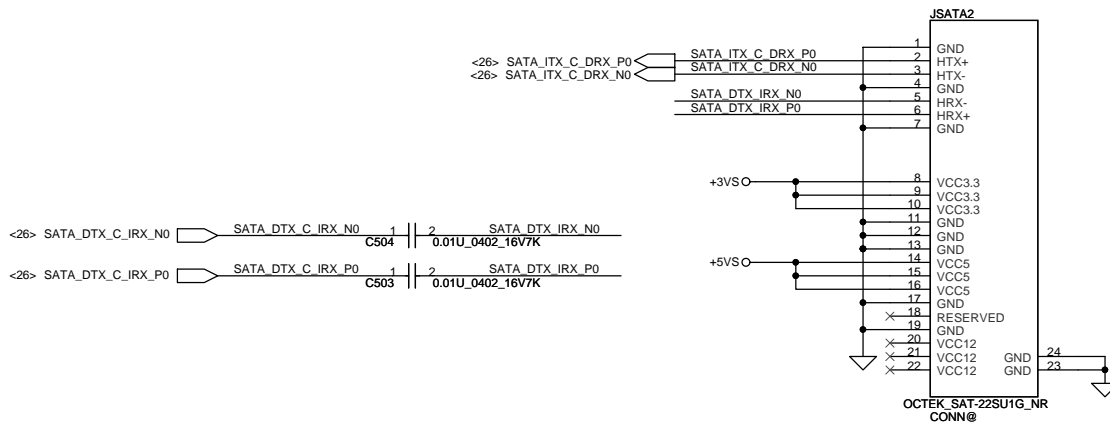




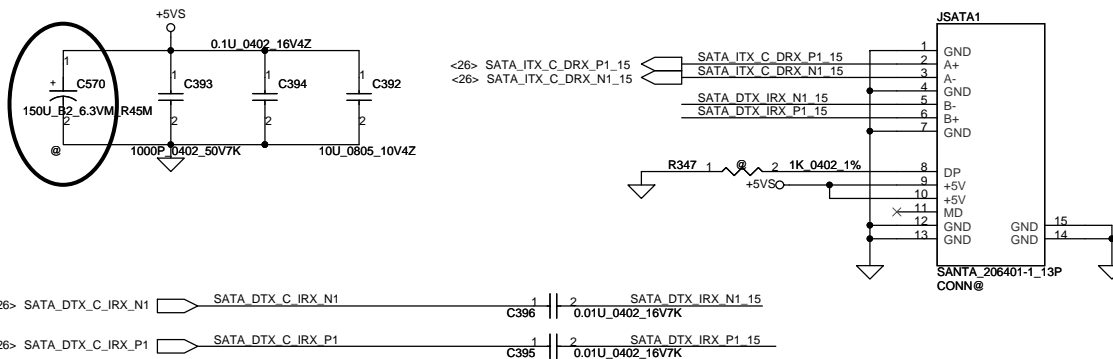




## SATA HDD Conn.

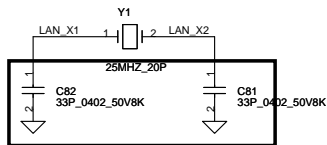
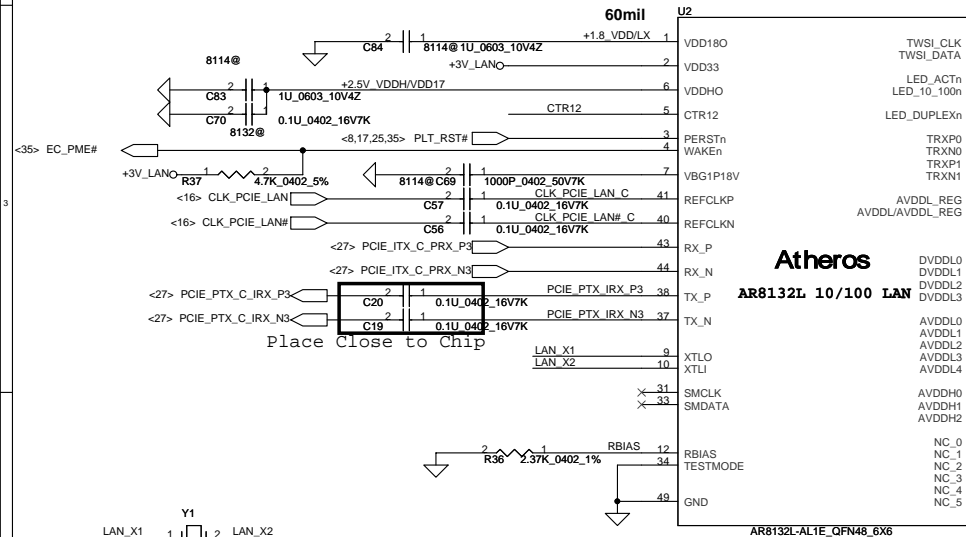
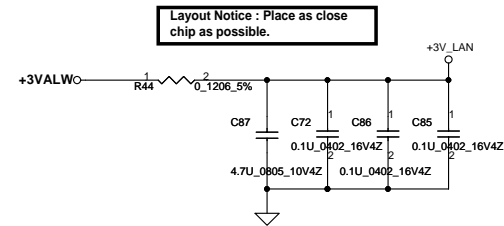
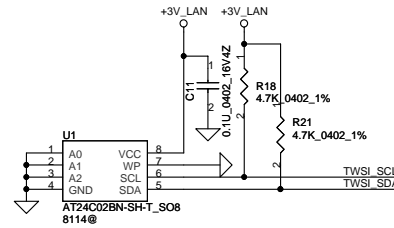
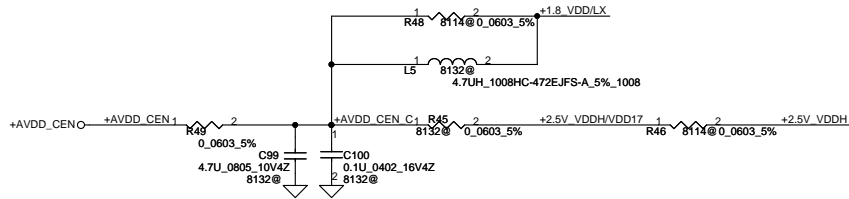


## SATA ODD Conn.

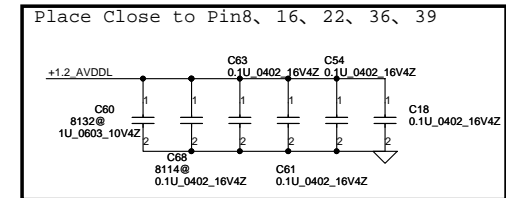
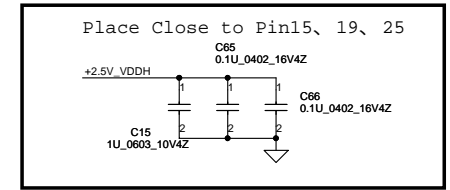
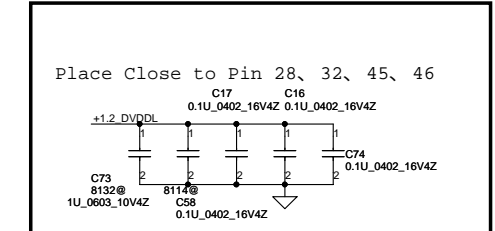
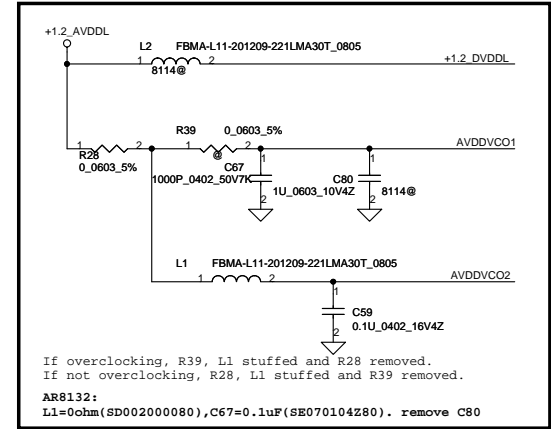
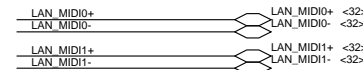
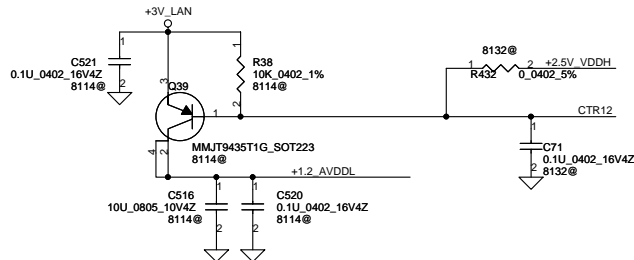


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Pre-MP 9/17

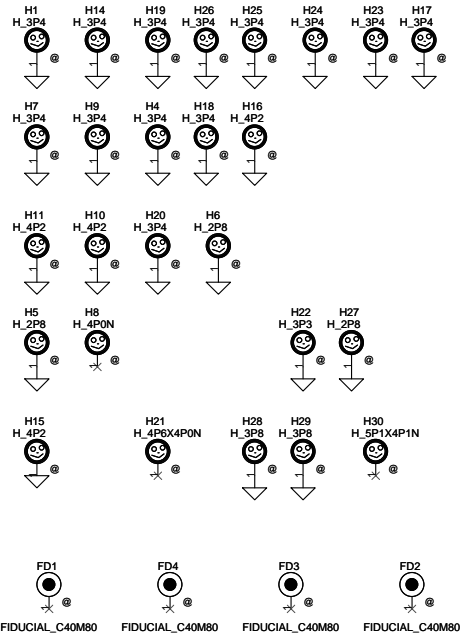


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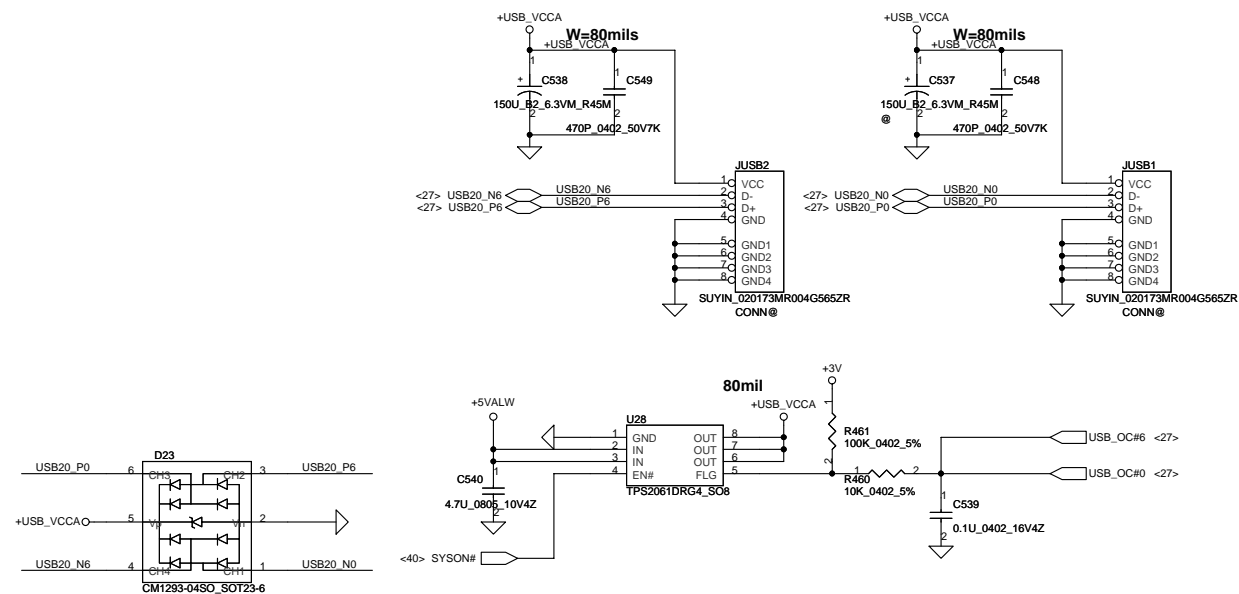


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

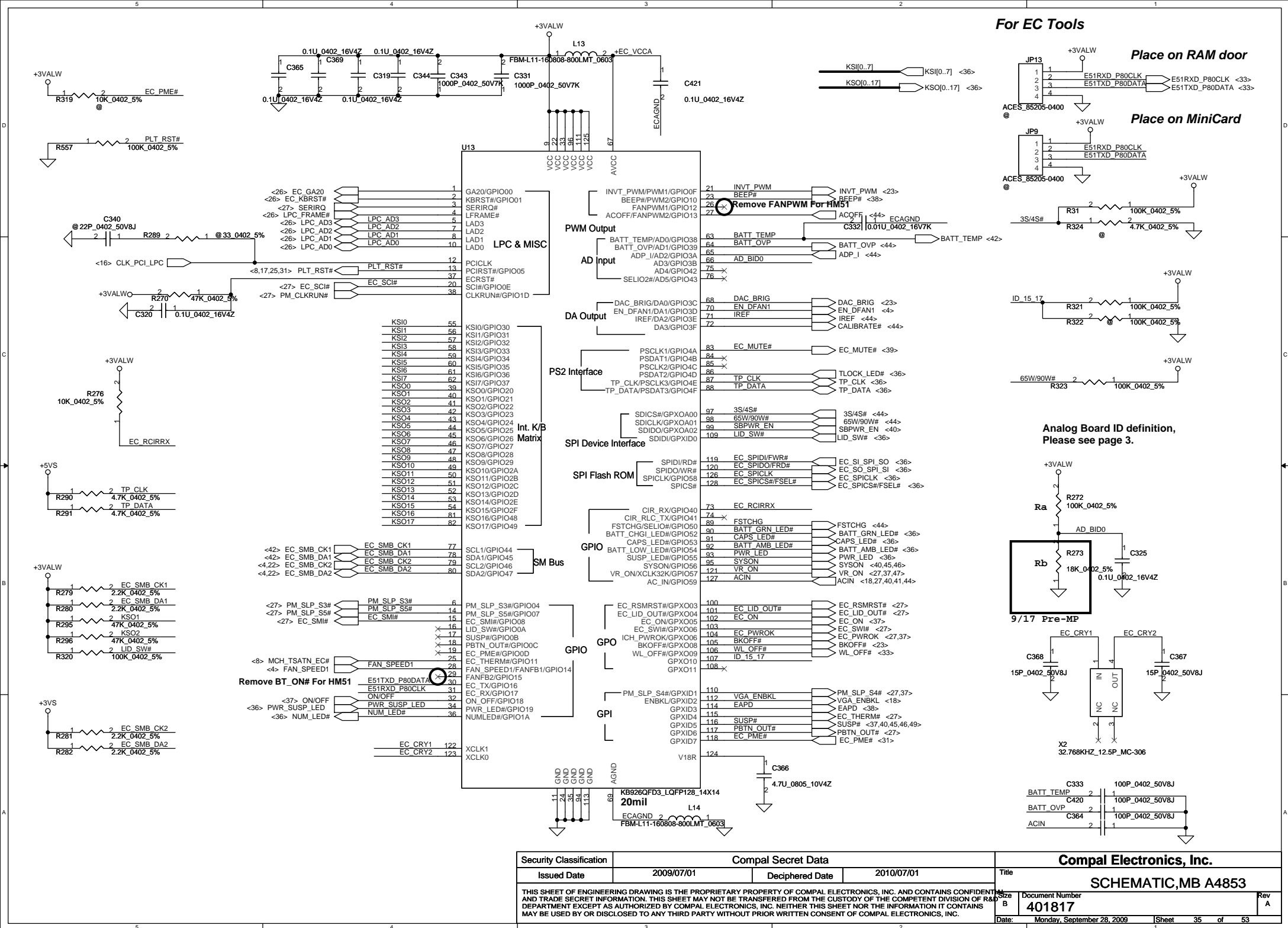


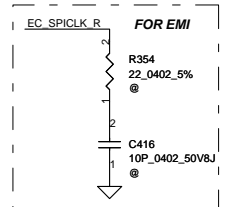
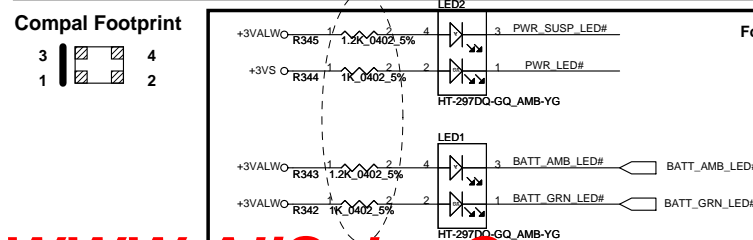
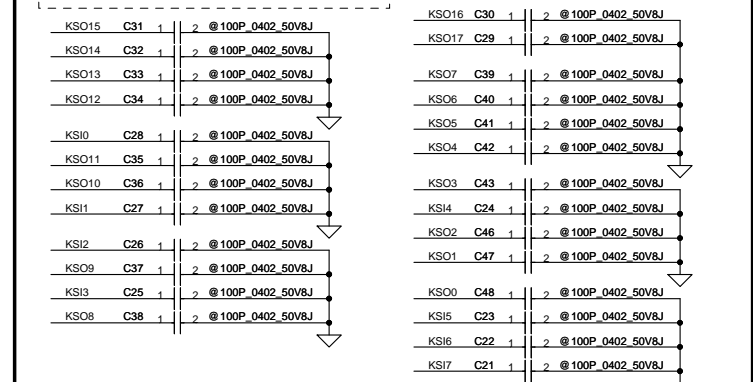
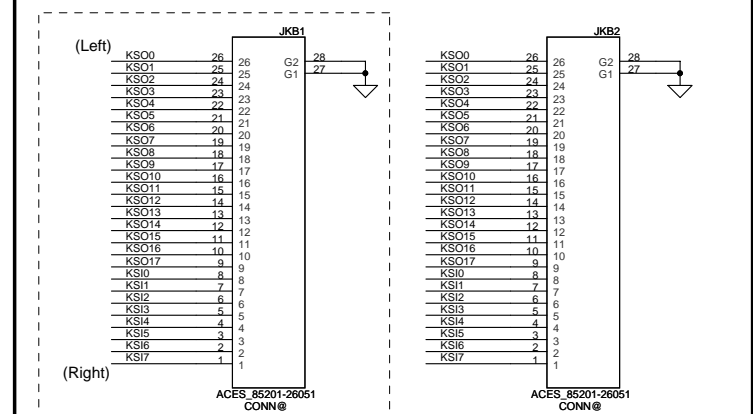
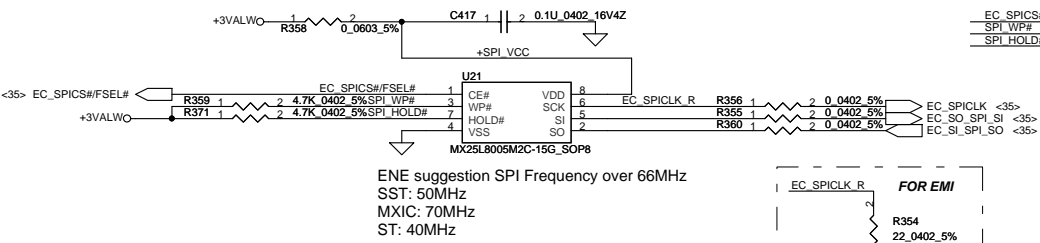
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# USB CONN.

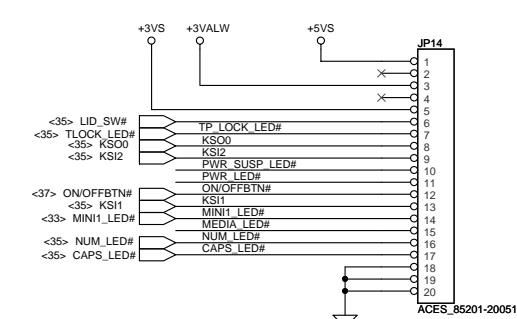


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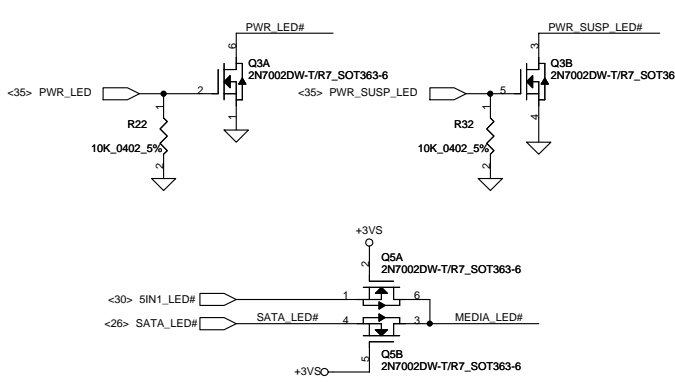




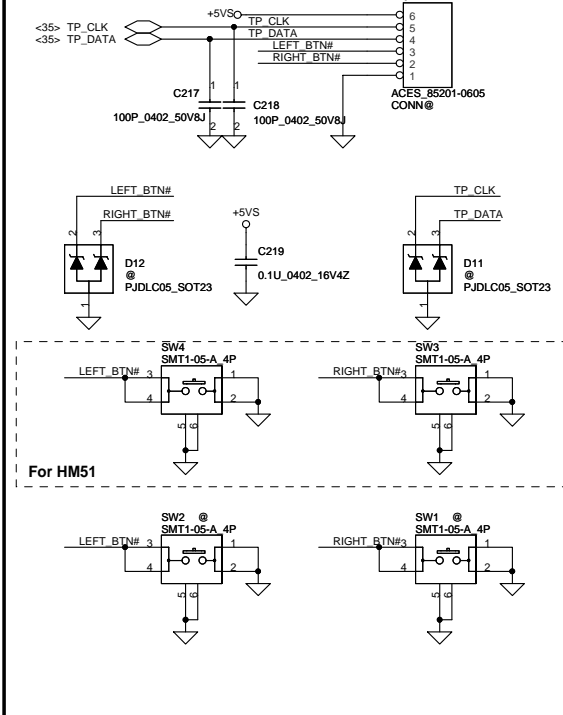
To POWER/B



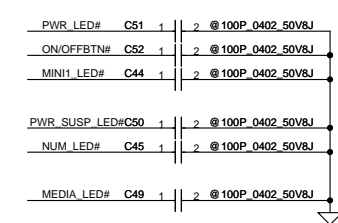
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KSI1	WL_BTN#
KSI2	TLOCK_BTN#
KSI3	
KSI4	
KSI5	



To TP/B Conn.

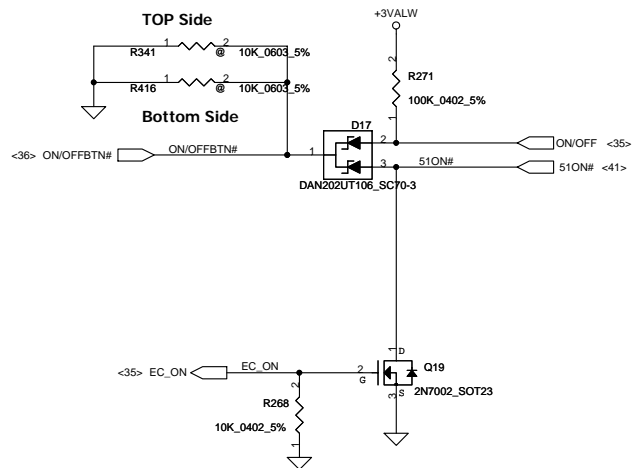


FOR EMI

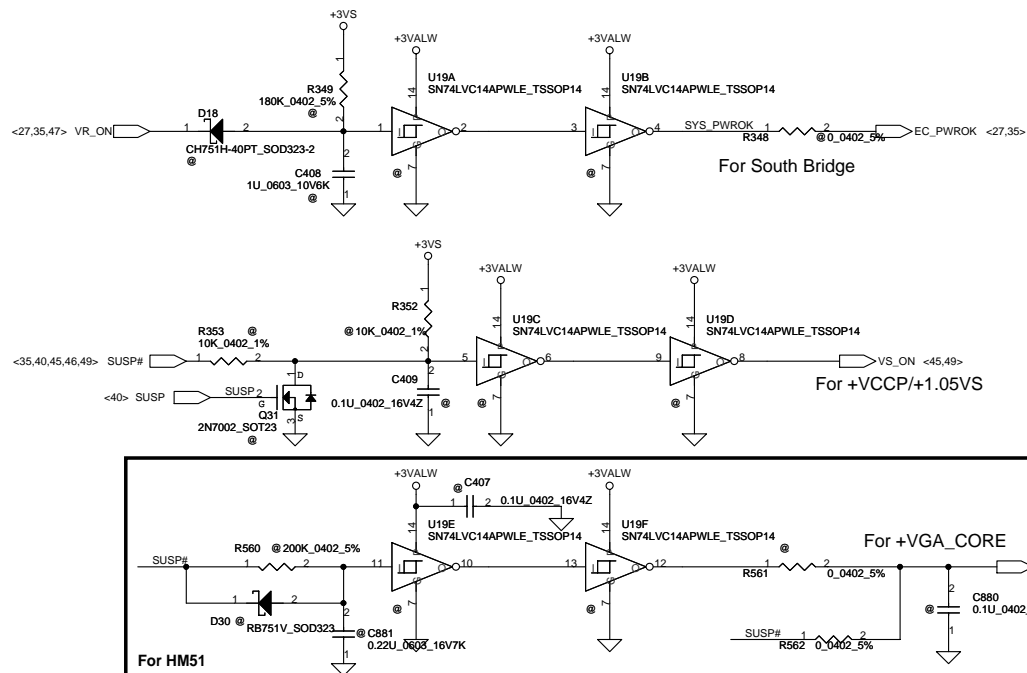


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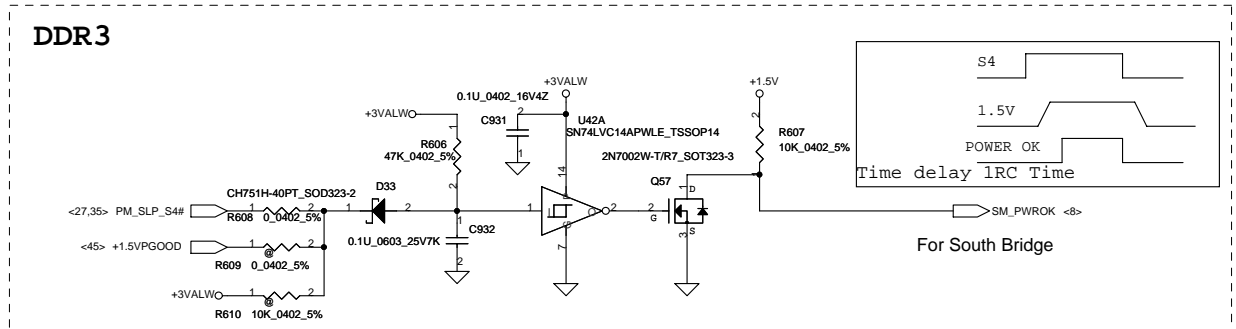
ON/OFF switch



### ***Power ON Circuit***

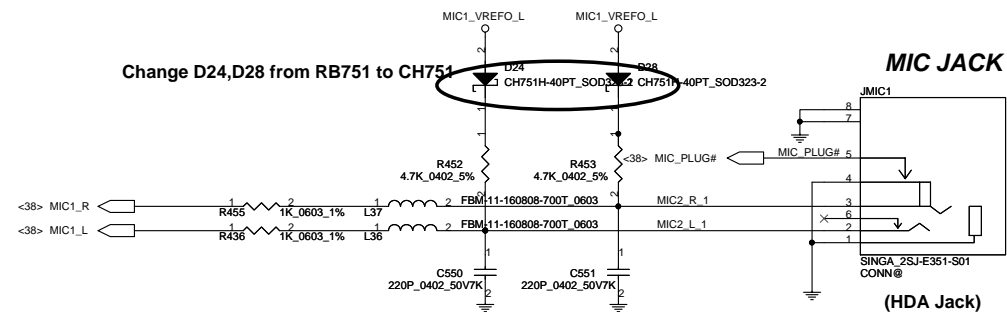
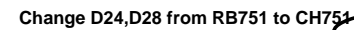


For HM51  
Pre-MP 9/17



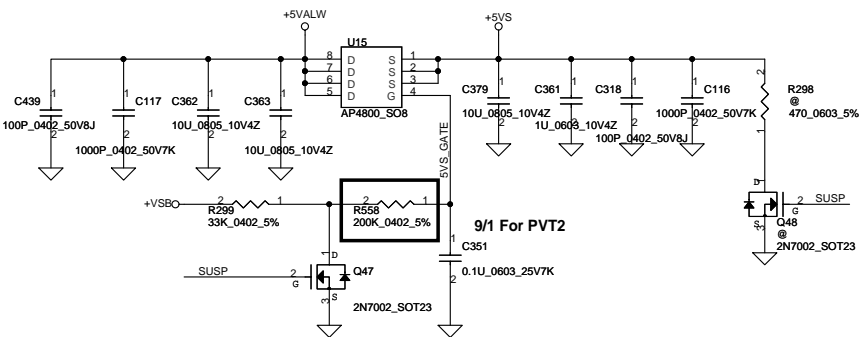
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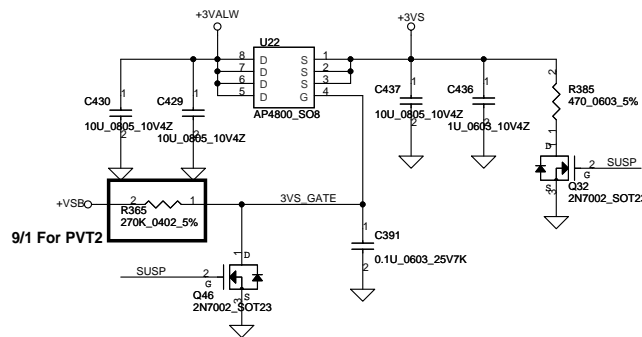


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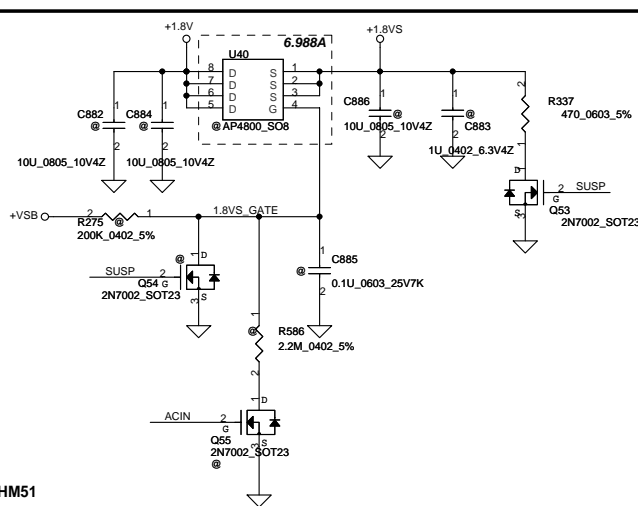
# **+5VALW TO +5VS**



# **+3VALW TO +3VS**

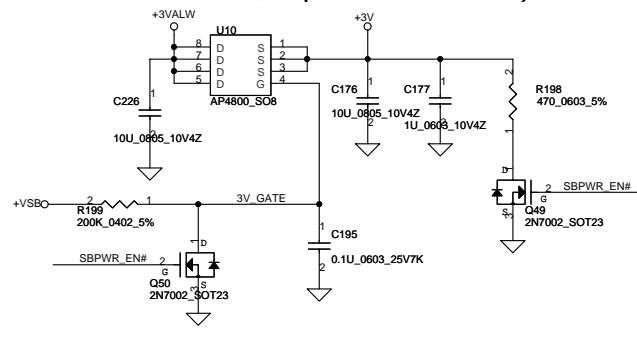


# **+1.8V to +1.8VS**

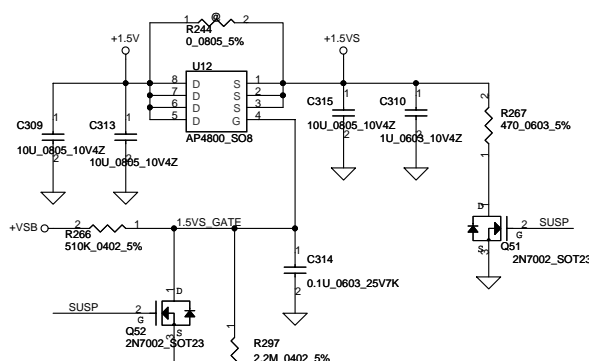


For HM51

# **+3VALW TO +3V\_SB(ICH8M AUX Power)**

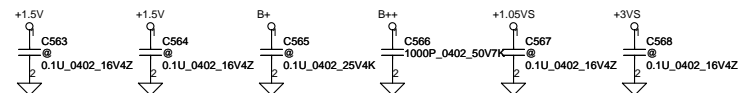


# **+1.5V to +1.5VS**

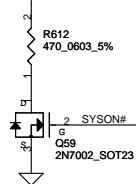


<18,27,35,41,44> ACIN

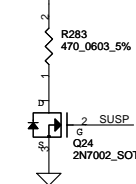
# **Reserve for EMI request**



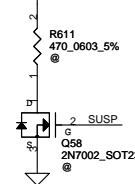
# **DDR3**



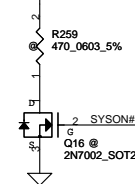
# **+1.05VS**



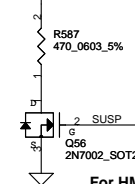
# **+0.75VS**



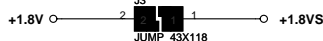
# **DDR3**



# **+1.1VS**

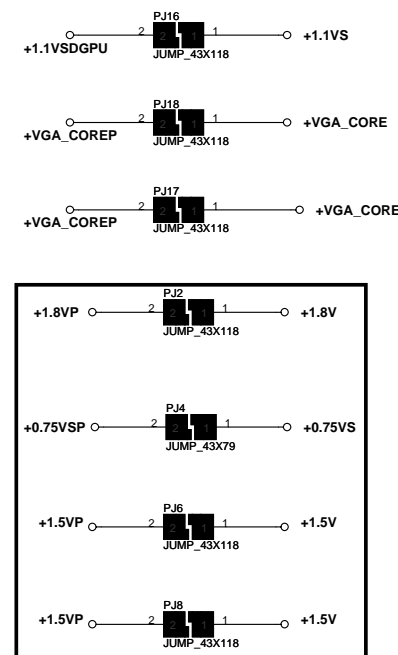
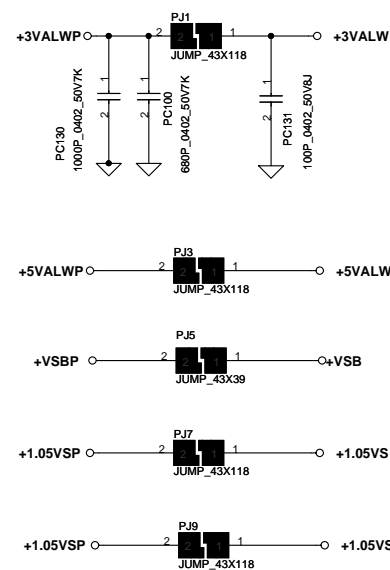
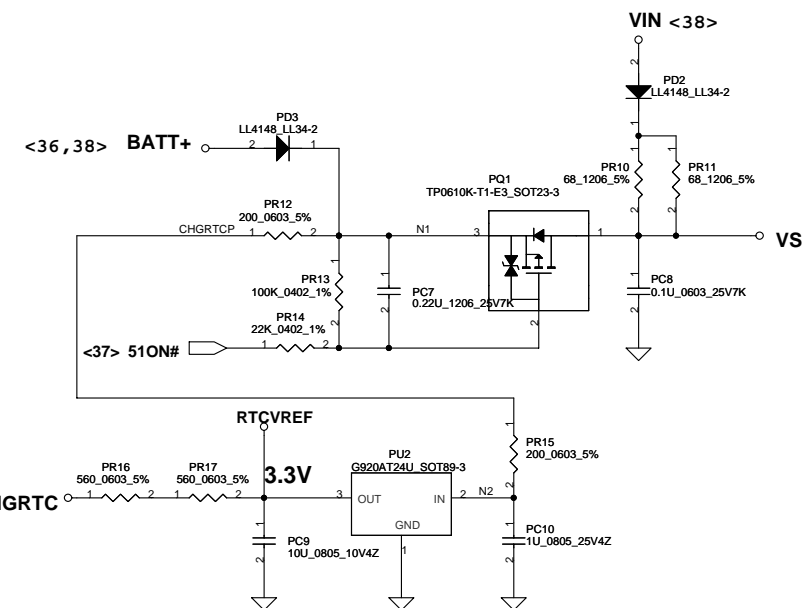
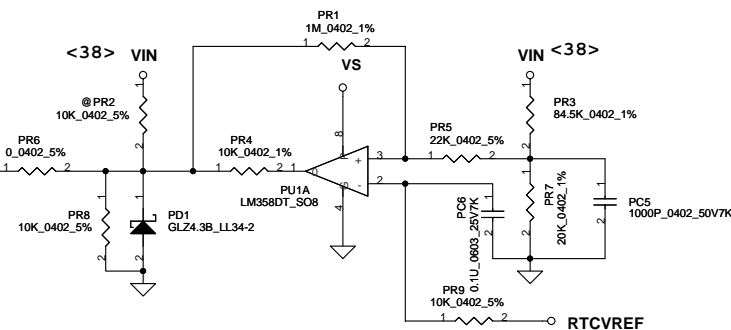


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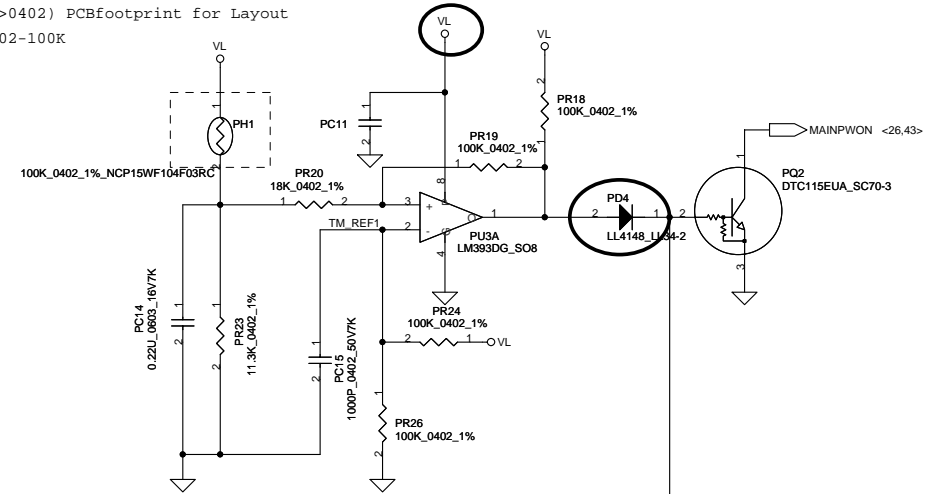




Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

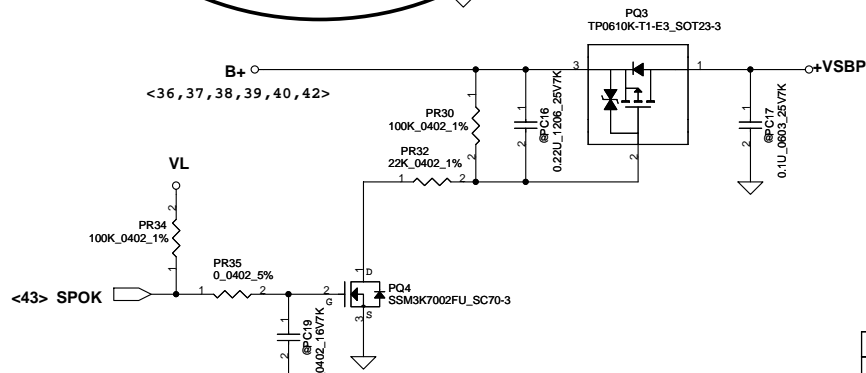
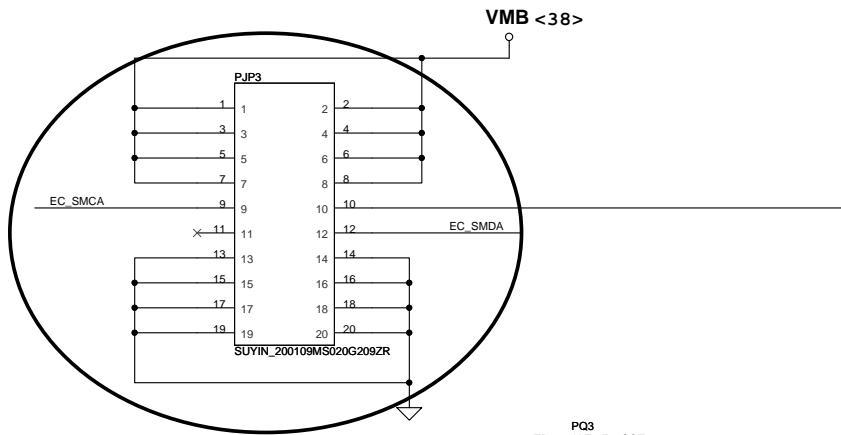
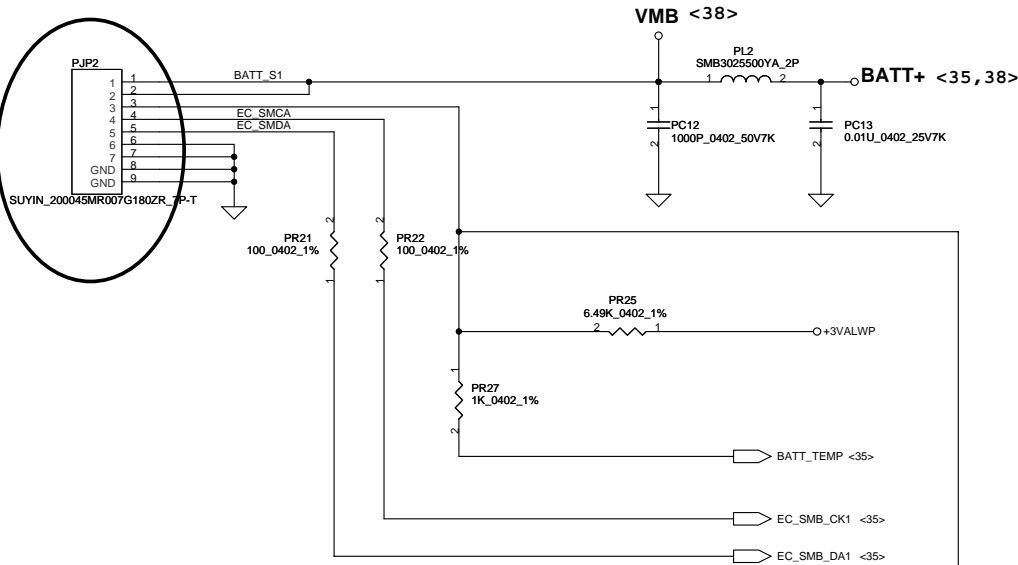
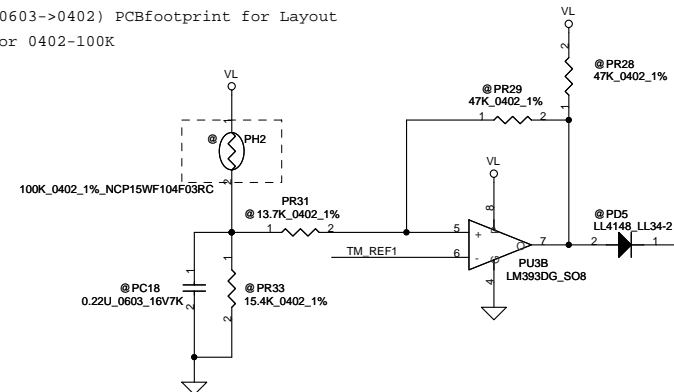
PH1 under CPU botten side :  
CPU thermal protection at 90 degree C  
Recovery at 70 degree C

2009\_08\_06 (0603->0402) PCBfootprint for Layout  
Change P/N for 0402-100K



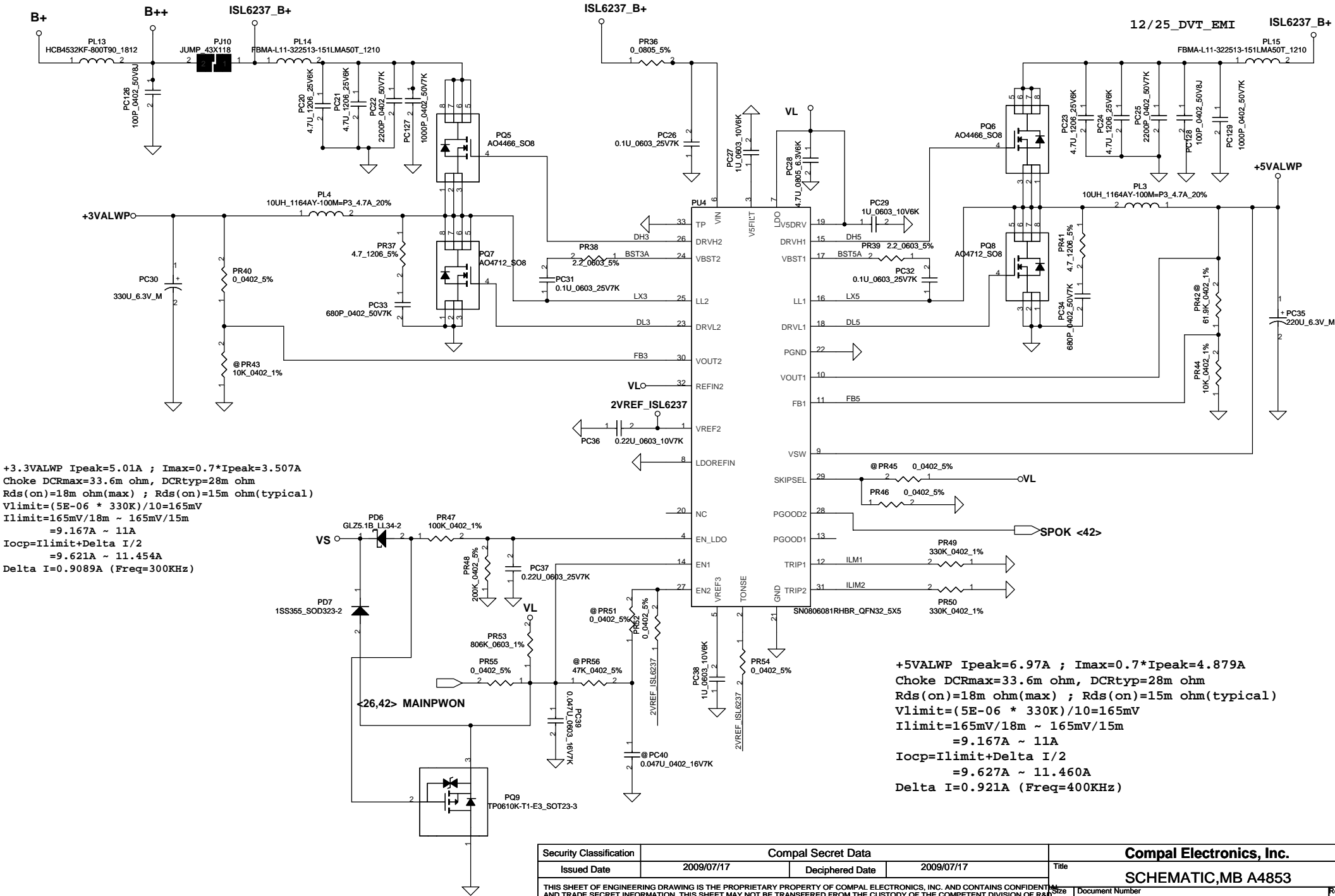
PH2 near main Battery CONN :  
BAT. thermal protection at 90 degree C  
Recovery at 70 degree C

2009\_08\_06 (0603->0402) PCBfootprint for Layout  
Change P/N for 0402-100K



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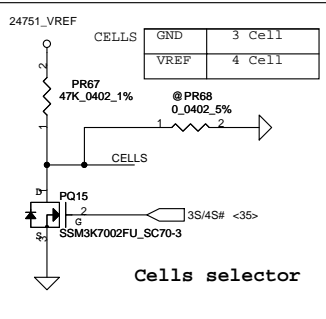
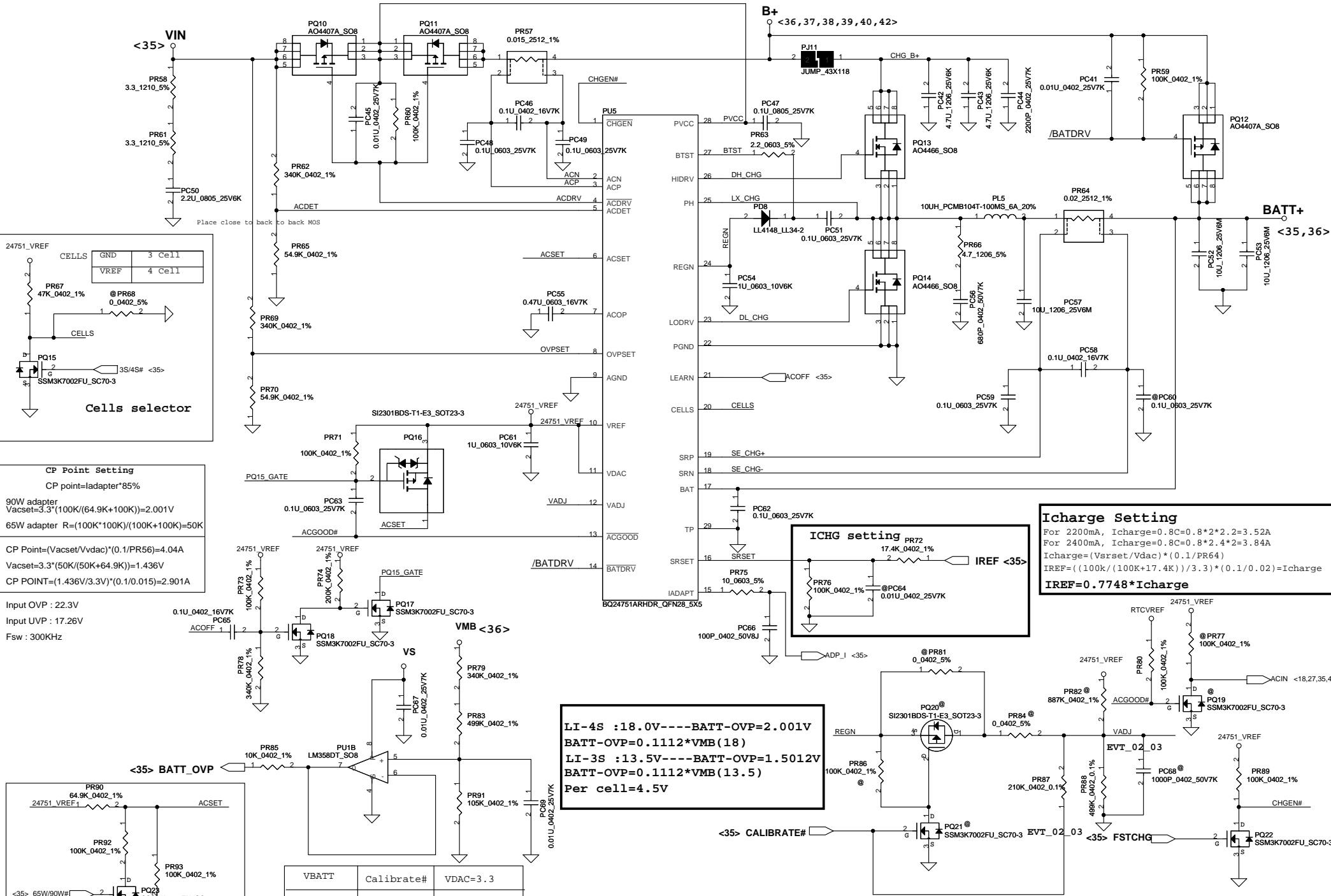
<36,37,38,39,40,42>



+3.3VALWP Ipeak=5.01A ; Imax=0.7\*Ipeak=3.507A  
Choke DCRmax=33.6m ohm, DCRtyp=28m ohm  
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
Vlimit=(5E-06 \* 330K)/10=165mV  
Ilimit=165mV/18m ~ 165mV/15m  
=9.167A ~ 11A  
Iocp=Ilimit+Delta I/2  
=9.621A ~ 11.454A  
Delta I=0.9089A (Freq=300KHz)

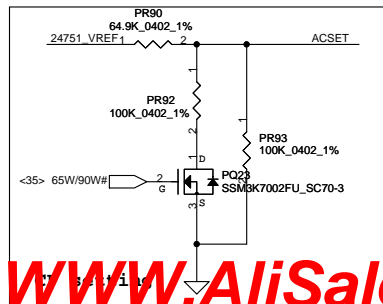
+5VALWP Ipeak=6.97A ; Imax=0.7\*Ipeak=4.879A  
Choke DCRmax=33.6m ohm, DCRtyp=28m ohm  
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)  
Vlimit=(5E-06 \* 330K)/10=165mV  
Ilimit=165mV/18m ~ 165mV/15m  
=9.167A ~ 11A  
Iocp=Ilimit+Delta I/2  
=9.627A ~ 11.460A  
Delta I=0.921A (Freq=400KHz)

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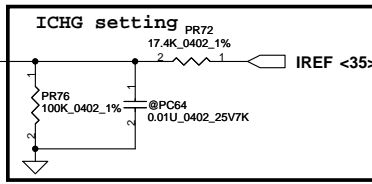
**CP Point Setting**  
CP point=ladapter\*85%  
90W adapter  
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$   
65W adapter  $R=(100K \cdot 100K)/(100K+100K)=50K$   
CP Point= $(V_{acset}/V_{dacc}) \cdot (0.1/PR56)=4.04A$   
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$   
CP POINT= $(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

Input OVP : 22.3V  
Input UVP : 17.26V  
Fsw : 300KHz



VBATT	Calibrate#	VDAC=3.3
4.0V	L=0	
4.2V	1.8755V	
4.3V	2.8132V	
4.5V	H=3.3	

**LI-4S : 18.0V---BATT-OVP=2.001V**  
**BATT-OVP=0.1112\*VMB(18)**  
**LI-3S : 13.5V---BATT-OVP=1.5012V**  
**BATT-OVP=0.1112\*VMB(13.5)**  
**Per cell=4.5V**



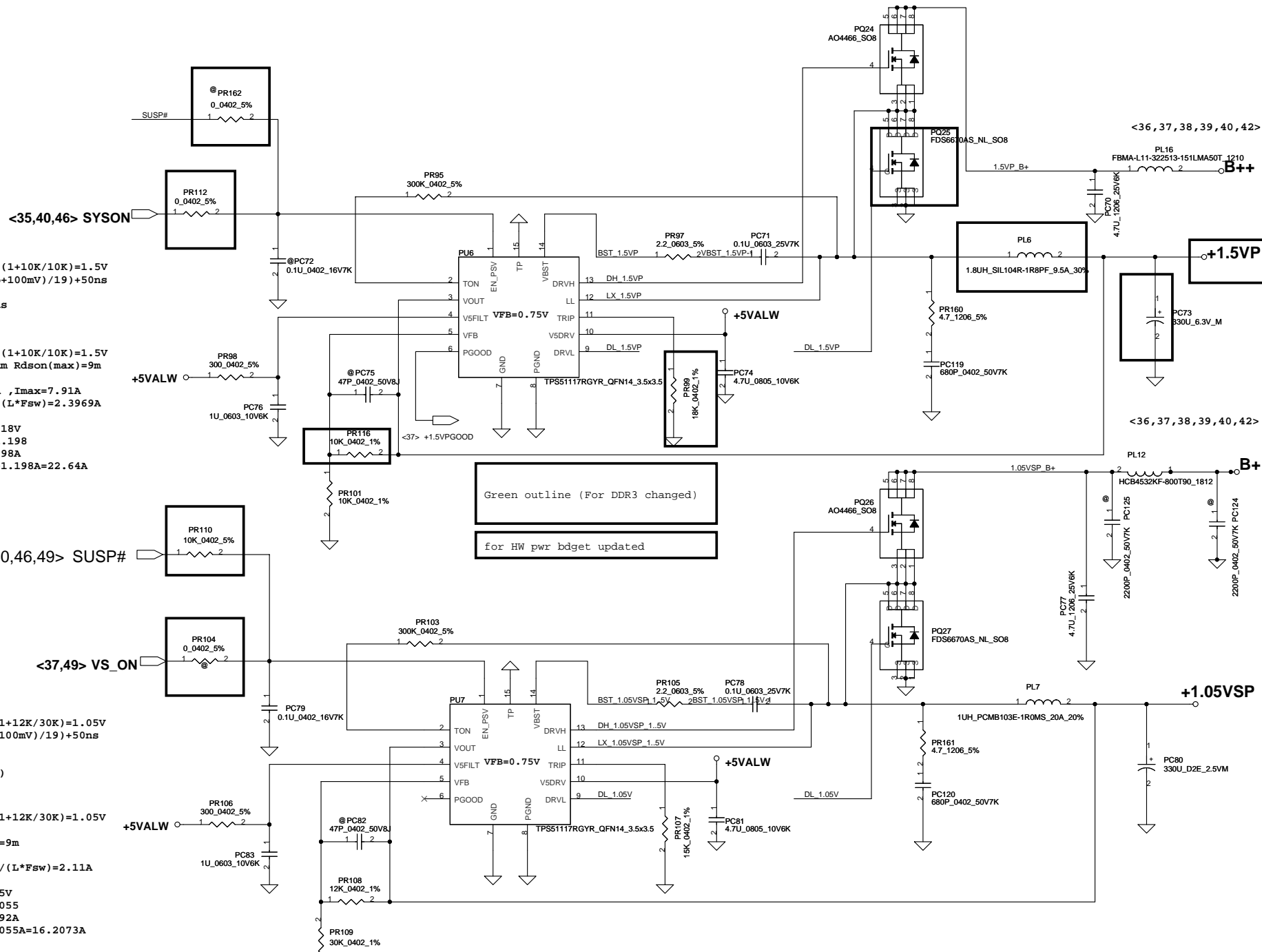
**Icharge Setting**  
For 2200mA,  $I_{charge}=0.8C=0.8 \cdot 2.2=3.52A$   
For 2400mA,  $I_{charge}=0.8C=0.8 \cdot 2.4=3.84A$   
 $I_{charge}=(V_{srset}/V_{dacc}) \cdot (0.1/PR64)$   
 $IREF=((100K/(100K+17.4K))/3.3) \cdot (0.1/0.02)=I_{charge}$   
**IREF=0.7748\*Icharge**

VFB=0.75V  
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Ton = 19 * e^{-12 * 143000 * ((2/3) * V_o + 100mV) / 19} + 50ns$   
 $= 2.645e-7 \text{ us}$   
 $=> V_o / V_{in} = D = Ton / Ts \Rightarrow Ts = 3.35us$   
 $Fsw = 262KHz$

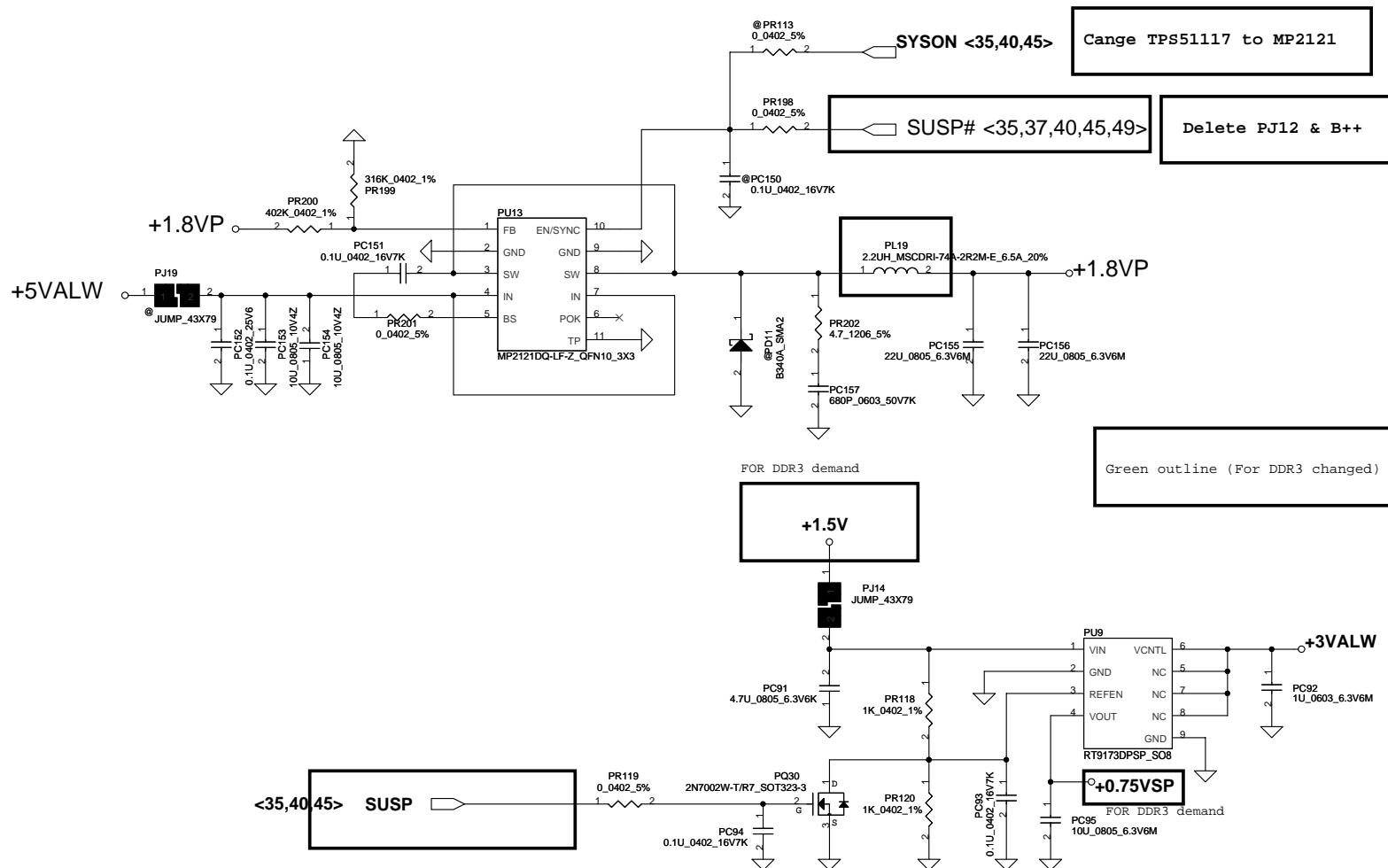
<Vo=1.5V> VFB=0.75V  
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$   
 $Fsw = 262KHz$  Cout ESR=15m ohm Rdson(max)=9m  
 $Rdson(min)=11.5m$   
 $I_{peak}=11.3A$ ,  $1.2I_{peak}=13.56A$ ,  $I_{max}=7.91A$   
 $\Delta I = ((19-1.5) * (1.5/19)) / (L * Fsw) = 2.3969A$   
 $=> 1/2 \Delta I = 1.198A$   
 $V_{trip} = R_{trip} * I_{0uA} = 18K * 10uA = 0.18V$   
 $I_{ocpmin} = V_{trip} / Rdsonmax * 1.2 + 1.198$   
 $= 0.075 / (0.018 * 1.3) + 1.198 = 13.98A$   
 $I_{ocpmax} = (0.075 / (0.015 * 1.1)) + 1.198A = 22.64A$   
 $I_{ocp} = 13.98 - 22.64A$

VFB=0.75V  
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$   
 $Ton = 19 * e^{-12 * 143000 * ((2/3) * V_o + 100mV) / 19} + 50ns$   
 $= 2.645e-7 \text{ us}$   
 $=> V_o / V_{in} = D = Ton / Ts \Rightarrow Ts = 3.35us$   
 $Fsw = 261KHz$  (by calculation tool)

<Vo=1.05V> VFB=0.75V  
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$   
 $Fsw = 261KHz$  Cout ESR=15m ohm  
 $Rdson(max.)=11.5m$   $Rdson(min)=9m$   
 $I_{peak}=9A$ ,  $I_{max}=I_{peak} * 0.7 = 6.3A$   
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * Fsw) = 2.11A$   
 $=> 1/2 \Delta I = 1.055A$   
 $V_{trip} = R_{trip} * I_{0uA} = 15K * 10uA = 0.15V$   
 $I_{ocpmin} = V_{trip} / Rdsonmax * 1.3 + 1.055$   
 $= 0.15 / (0.011 * 1.3) + 1.055 = 11.0892A$   
 $I_{ocpmax} = (0.15 / (0.009 * 1.1)) + 1.055A = 16.2073A$   
 $I_{ocp} = 11.0892A - 16.2073A$

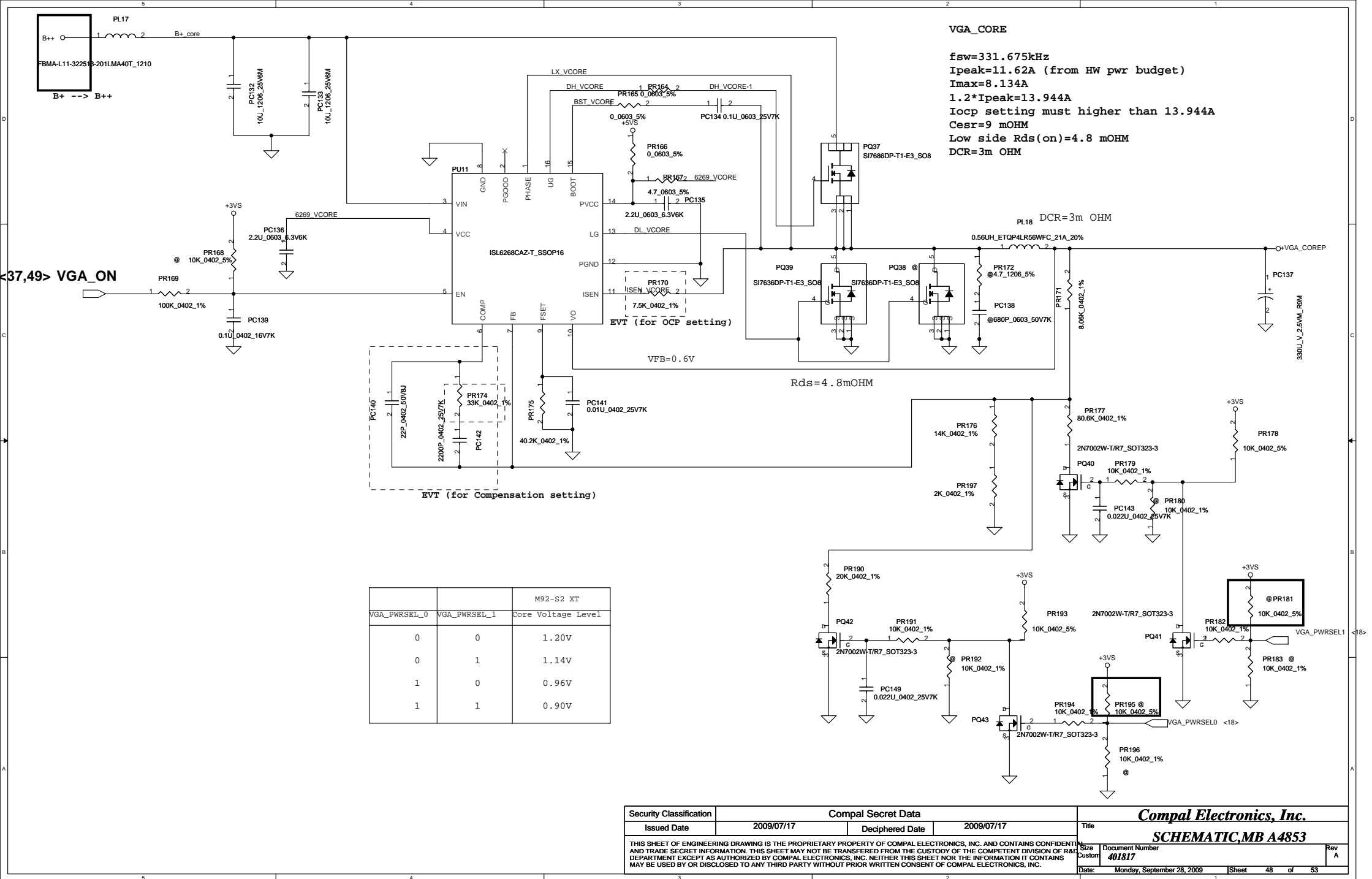


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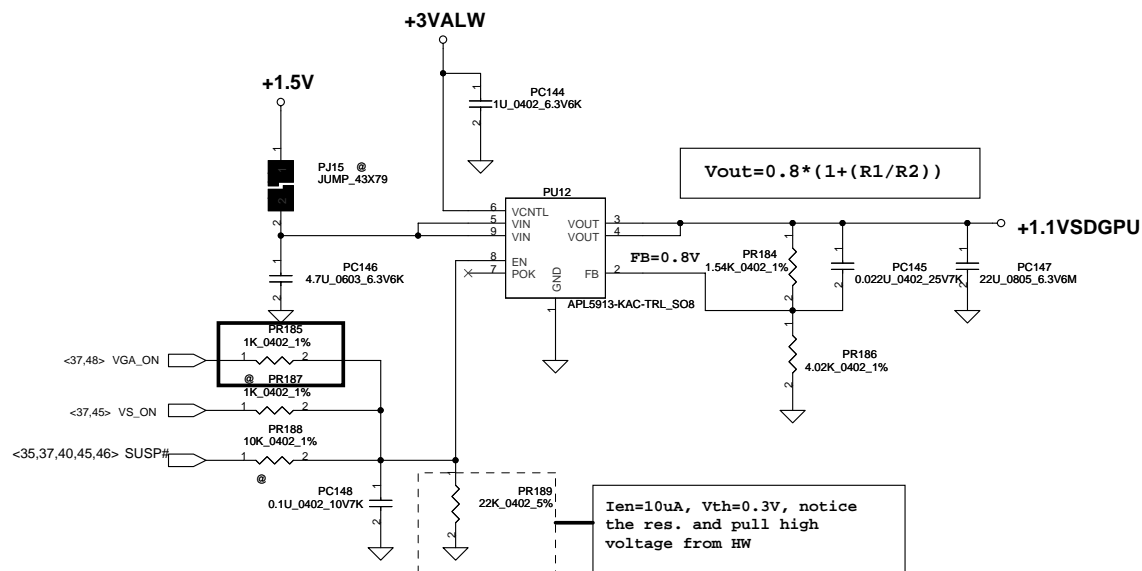


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## Version change list (P.I.R. List)

Page 1 of 3 of PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase	
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP  PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP  PR112: Reserve(@) 0_0402_5%	0.2		Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%	20081124	DVT	
				38				
				39				
				40	+1.05VSP  PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP  PR112: Reserve(@) 0_0402_5%			
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP  ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3		+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J  +1.5VP  ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT	
				35				
				40				
20	POWER Solution	+3VALWP/+5VALWP  RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT	
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8/21 For Change DDR3

- 1. P.40 Add R612, Q59 ; Unstuff R244 ; Remove R260, R253, Q13, Q14 ; stuff C309, C313, C315, C310, C314, R266, Q52, Q51, R267, U12 for +1.5V
- 2. P.40 Unstuff R611, Q58 for +0.75VS ; Add J3 for +1.8V ;
- 3. P.37 Unstuff R609, R610 ; Add R608, R606, R607, D33, U42, Q57 for DDR3
- 4. P.23 Unstuff R411, D20 ; Add R613 for BKOFF#
- 5. P.25 Unstuff U8, R83 ; Add R614 for PCI\_RST#

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- 1. P.22 Unstuff R544, R545 for No HDMI Audio Function
- 2. P.40 Change R558 120K ohm as 200K ohm ; Change R200K ohm as 270K ohm

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- 1. P.40 Unstuff C882, C883, C884, C885, C886, R275, Q54, U40 for 1.8VS
- 2. P.31 Change C81, C82 27pF as 33pF for Xtal 25MHz(TXC suggest value)
- 3. P.26 Change C163, C164 18pF as 15pF for Xtal 32.768kHz (TXC suggest value)
- 4. P.37 Unstuff C407, C880, C881, R560, D30
- 5. P.41 Unstuff R580, U41
- 6. P.35 Change R273 8.2k ohm as 18k ohm for Board ID

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