Cathedral Peak Block Diagram

Project code: 91.4J501.001
PCB P/N : 48.4J501.001
REVISION : 07261 - SB

CLK GEN.
ICS 9LPRS365BKLFT (71.09365.A03)
RTM 875N-606-LFT (71.00875.003)
3

Mobile CPU
Penryn 479
4, 5

THERMAL EMC2102
21

HOST BUS 667/800/1067MHz@1.05V

DDR2 DIMM1
667/800 MHz
12

DDR2 DIMM2
667/800 MHz
13

667/800MHz

667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

CRT 15

LCD 14

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
17,18,19,20

INT.MIC 29

Line In
29

Codec
ALC268
28

AZALIA

MIC In
29

29

OP AMP
APA2057 29

INT.SPKR

29

Line Out
(NO SPDIF)

RJ11

MODEM
MDC Card
23

PCIex1

LAN
Giga LAN
88E8071 25

TXFM 26

RJ45 26

PCIex1

New card 27

PWR SW
G577BR91U 27

PCIex1

Mini Card
Kedron a/b/g/n 27

LPC BUS

KBC
ENE3310
30

BIOS
Winbond
W25X80
8M Bits 31

LPC
DEBUG
CONN 31

Launch
Buttom
16

USB

Blue Tooth
(USB) 23

Camera
(USB) 14

Touch
Pad 30

INT.
KB 30

SATA

HDD SATA 22

ODD SATA 22

SATA

USB
2 Port 23

USB

CardReader
Realtek
RTS5158E 27

MS/MS Pro/xD
/MMC/SD
5 in 1 27

Daughter Board
LED Board
07950
16

Daughter Board
USB Board
2 Port + e-Key
07951
23

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
TPS51125 43

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
TPS51124 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44

1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44

1D8V_S3	1D5V_S0

CFXCORE DC/DC
ISL6263 35,36

INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC
ISL6266A 42

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER
BQ24750 47

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title: BLOCK DIAGRAM

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

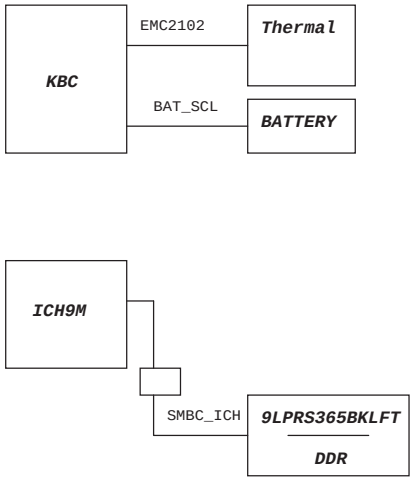
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	*NC*
LANE4	*NC*
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB4*
2	*USB2*
3	*NC*
4	*USB3*
5	*Bluetooth*
6	*NC*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	Card Reader
11	*NC*

SMBus



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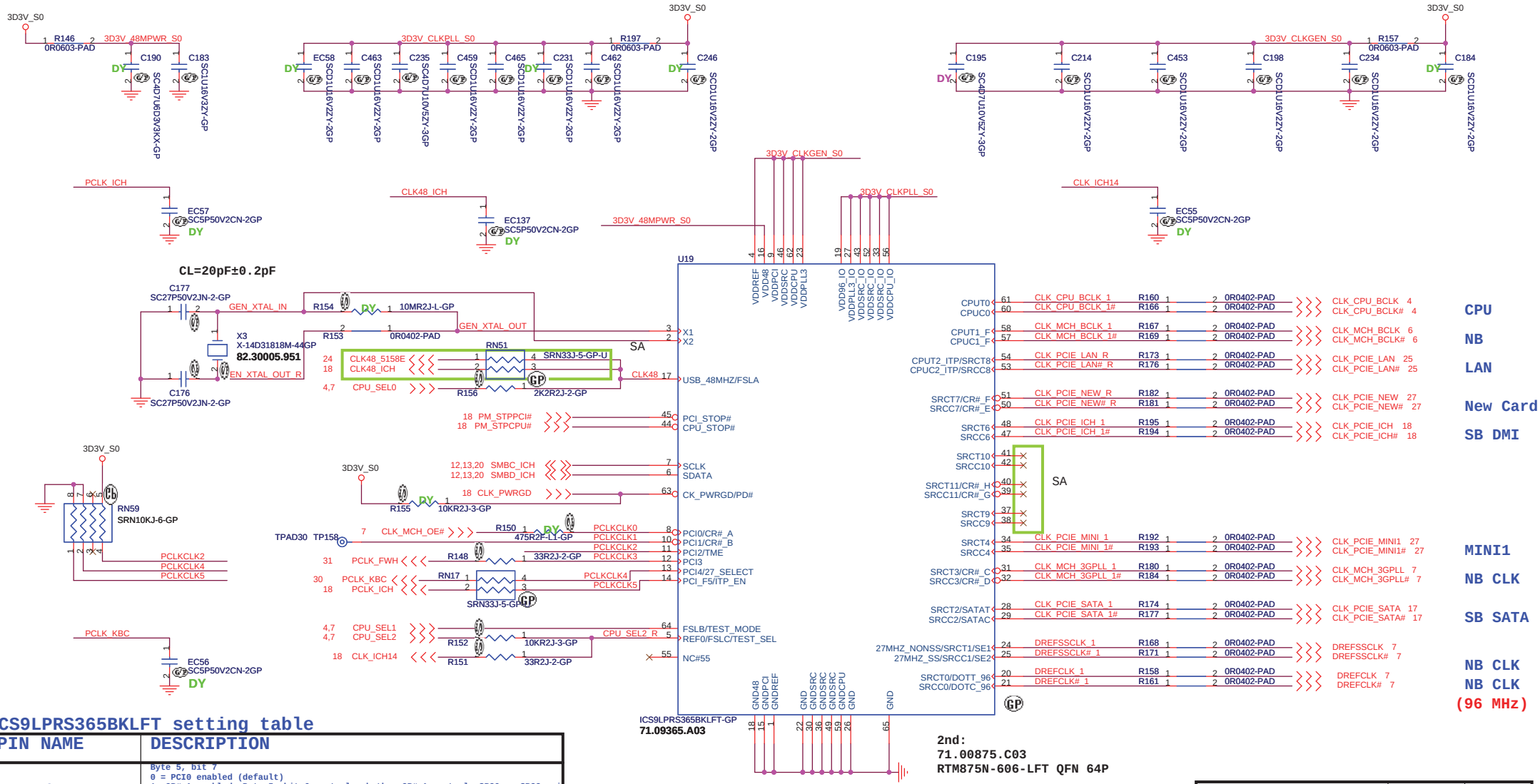

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title	Clock Generator	
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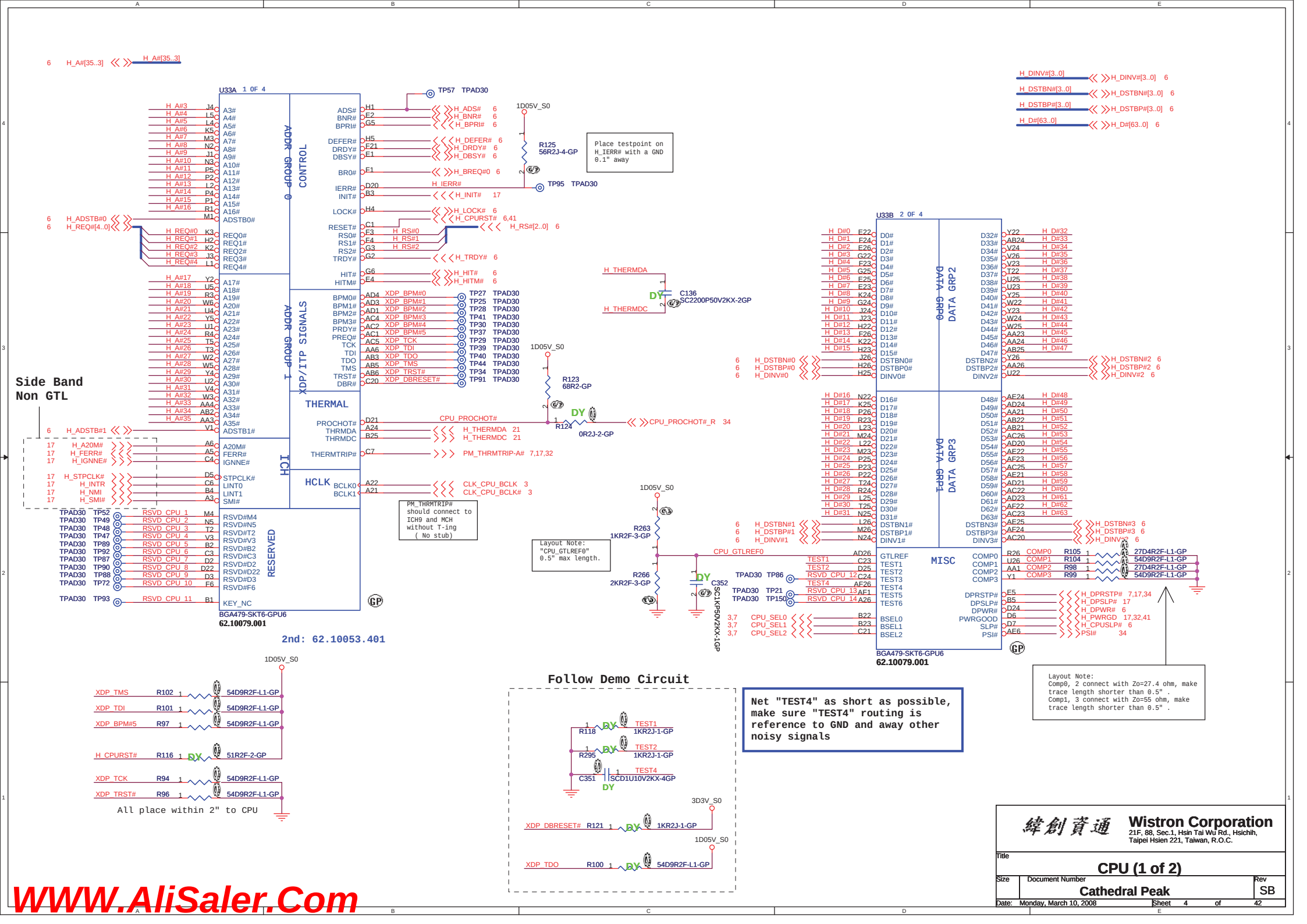
U33A 1 0F 4
U33B 2 0F 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
DATA GRP2
DATA GRP3
MISC
Side Band
Non GTL
BGA479-SKT6-GPU6
62.10079.001
2nd: 62.10053.401
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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CPU (1 of 2)
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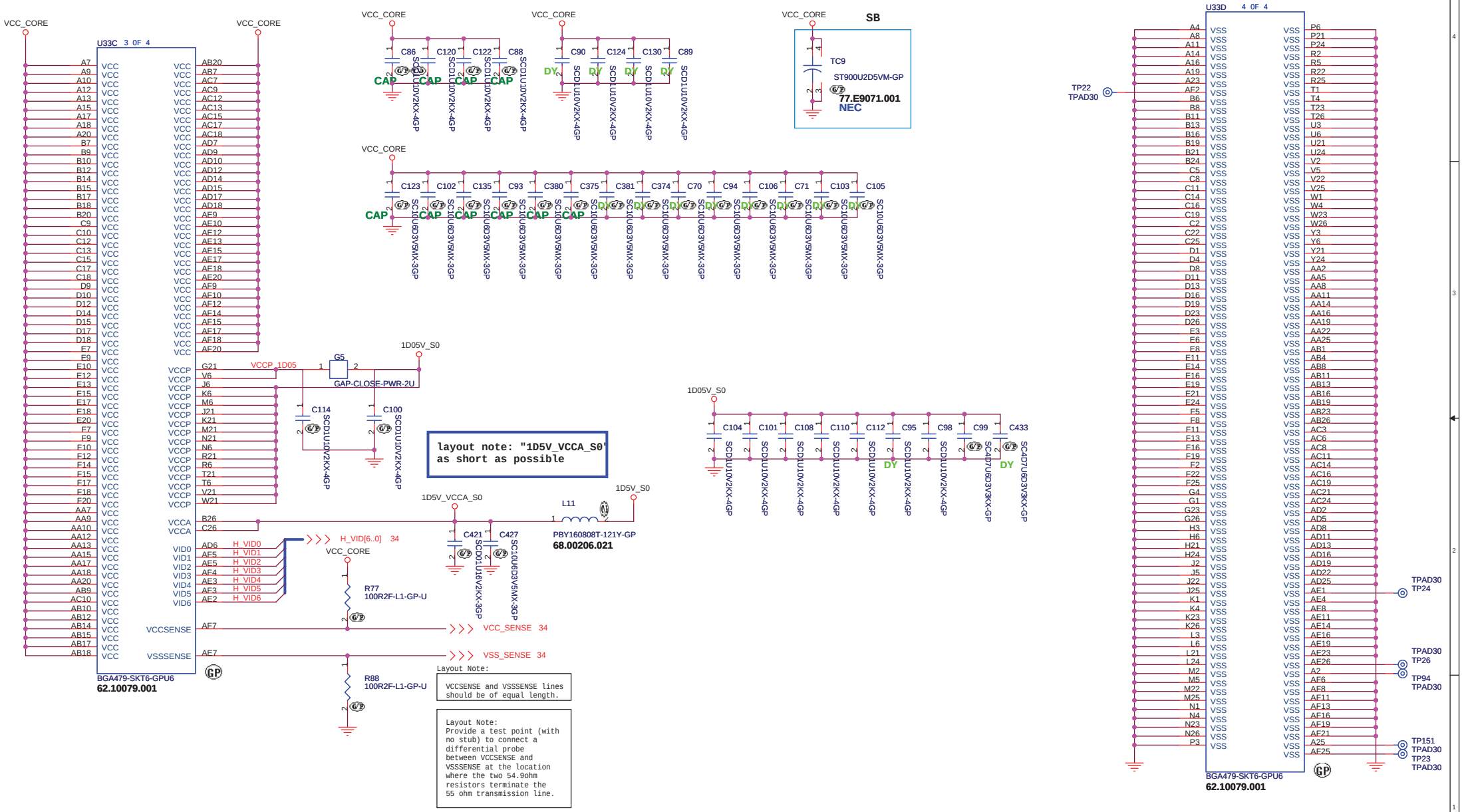

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Title	**CPU (2 of 2)**	
Size	Document Number: **Cathedral Peak**	Rev: SB
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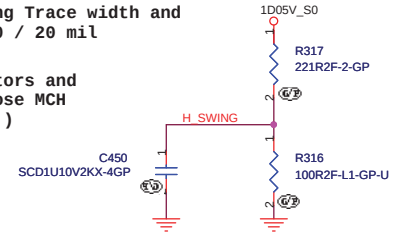
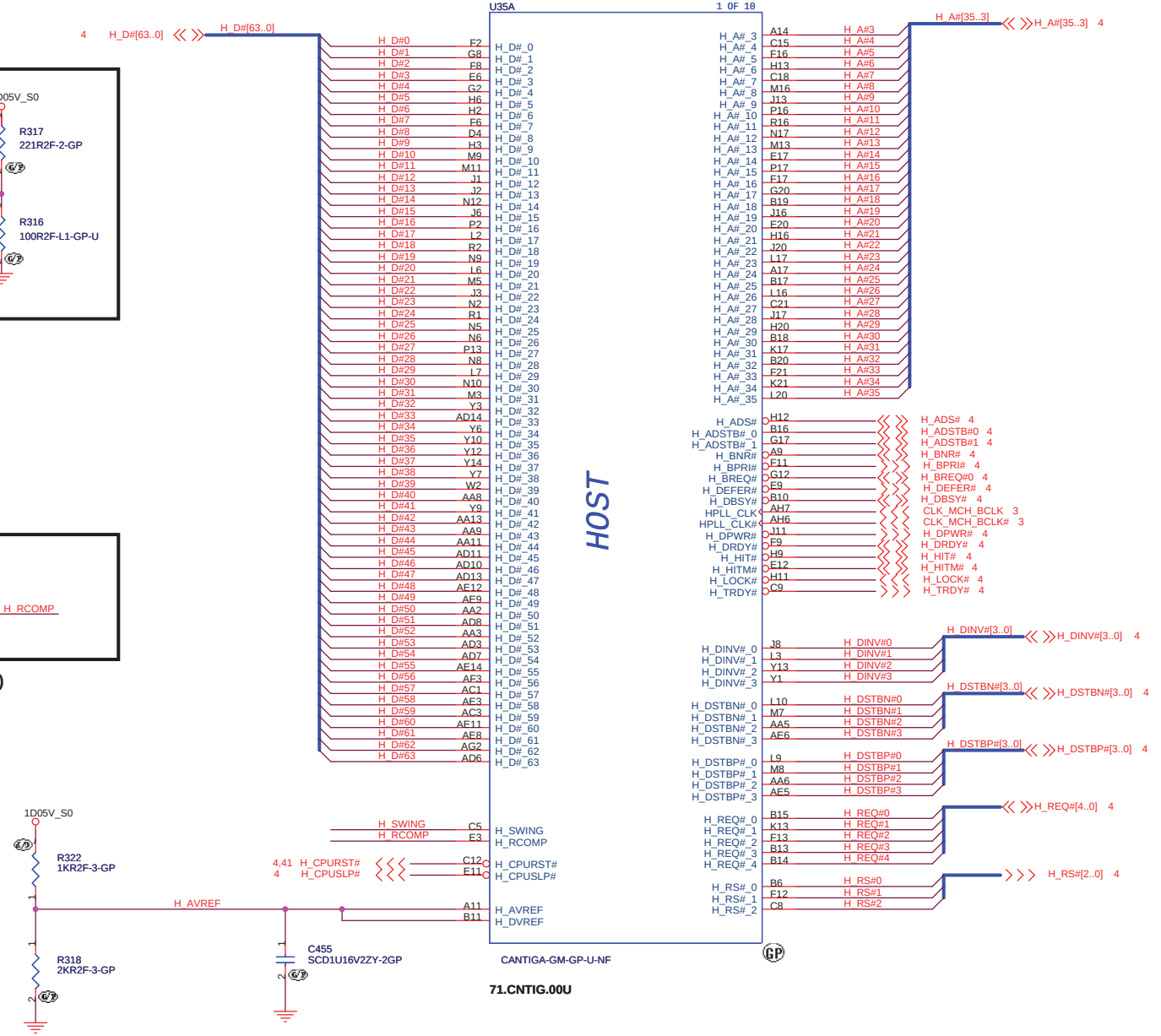
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

Size | Document Number: Cathedral Peak | Rev: SB

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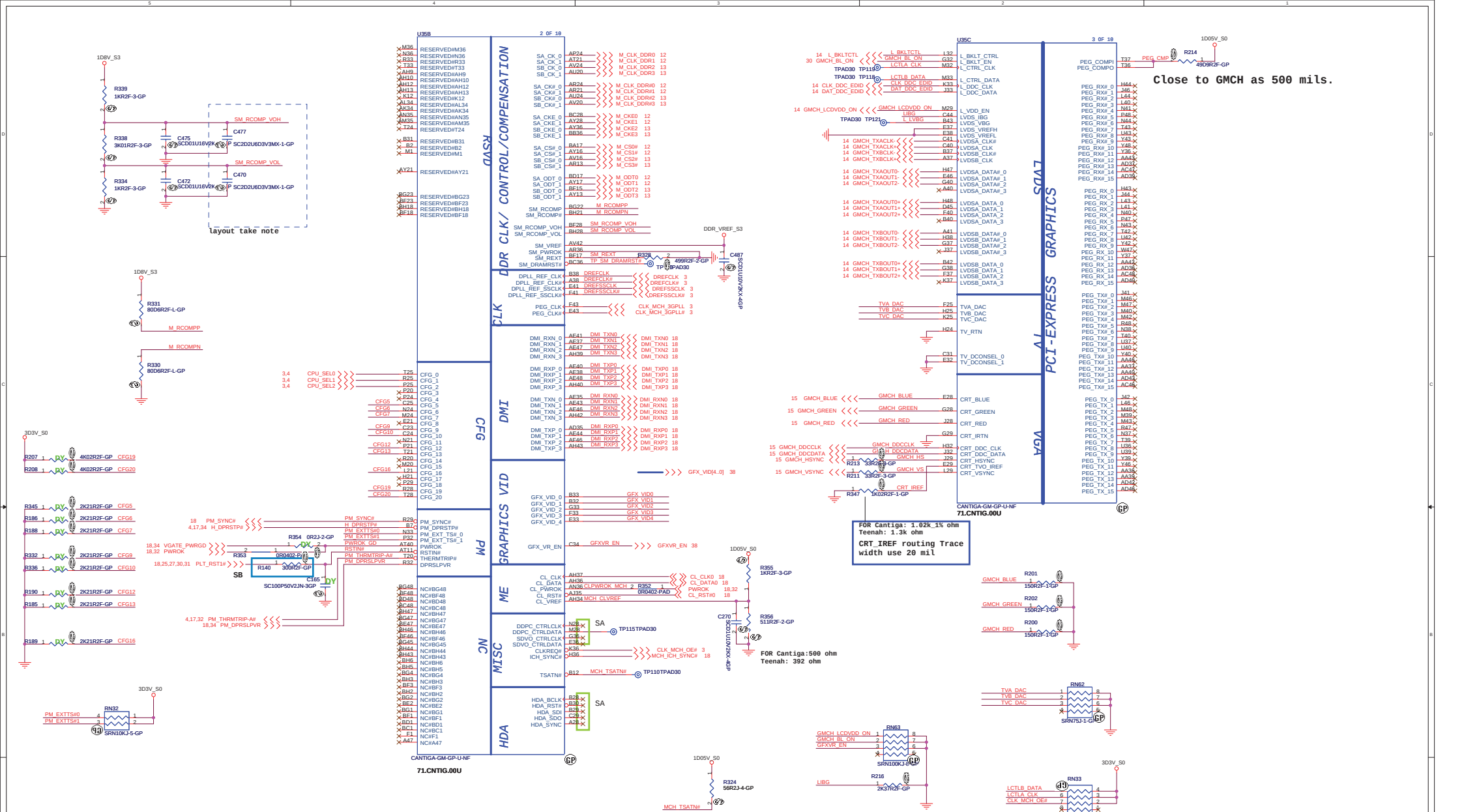

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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Title	Cantiga (2 of 6)	
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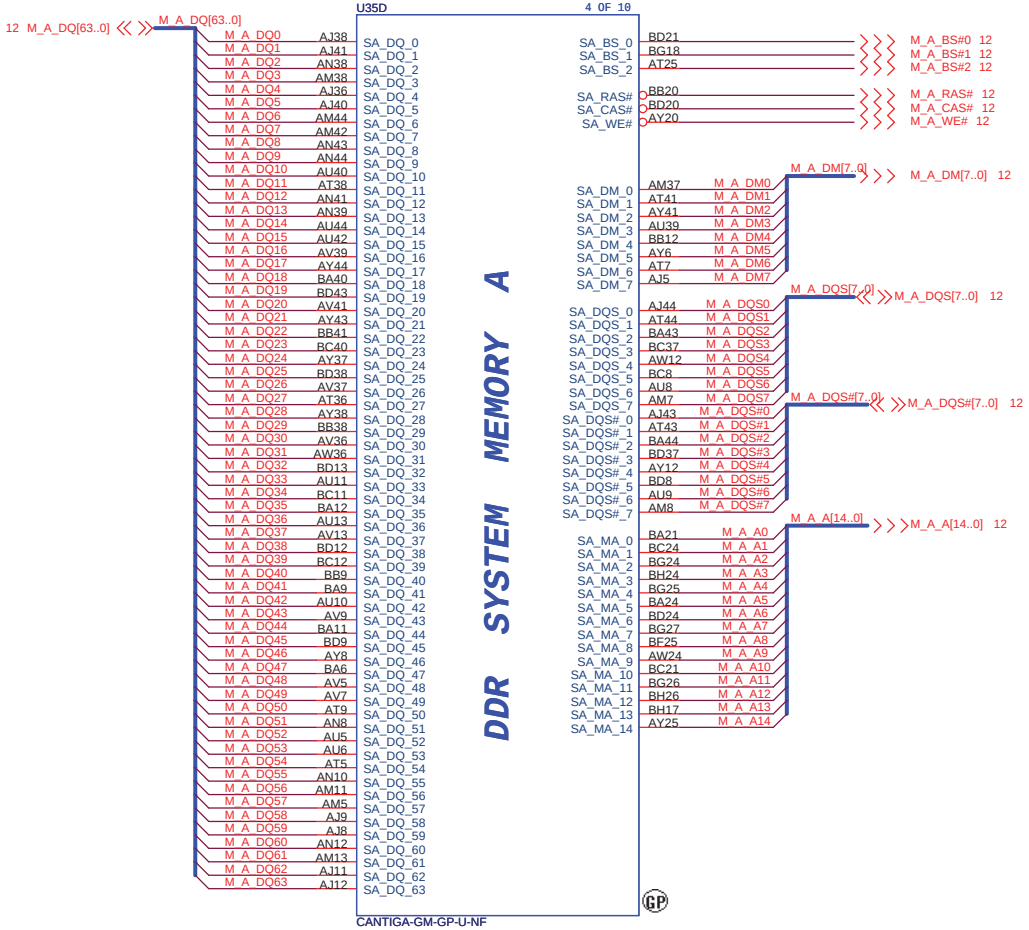

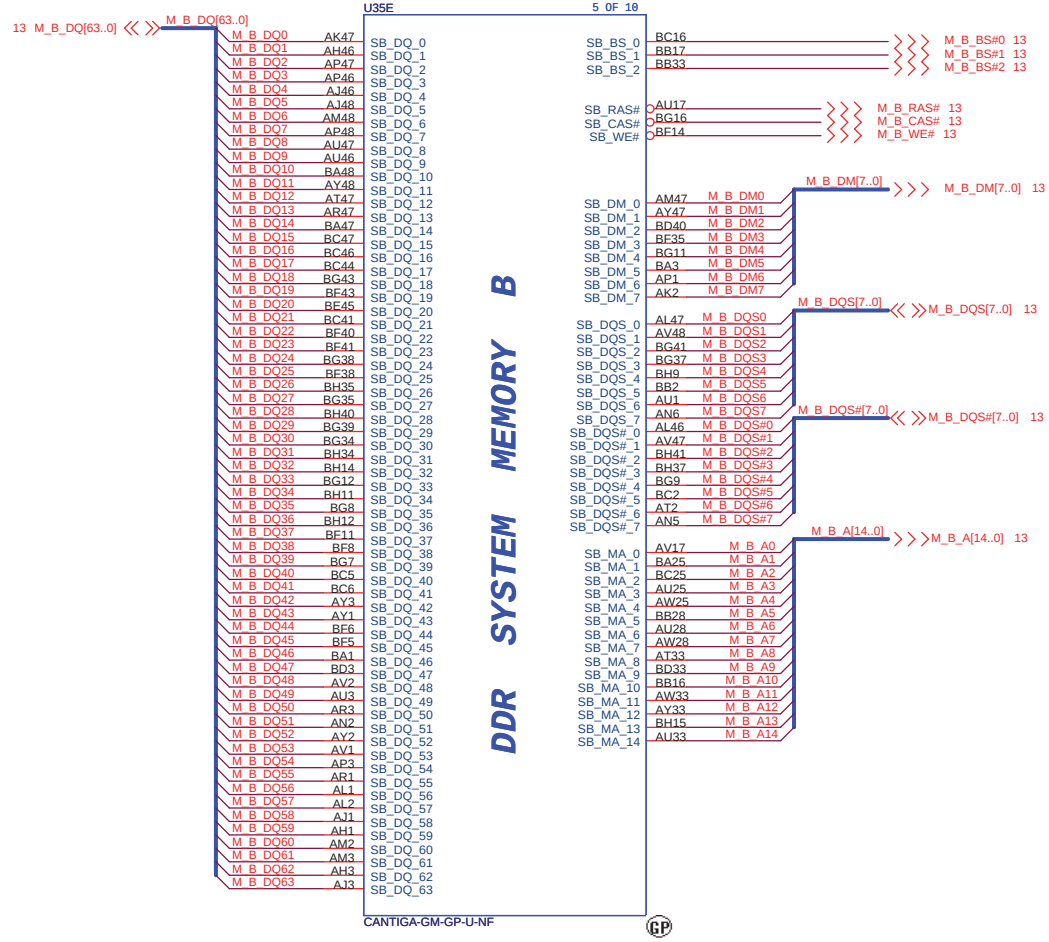

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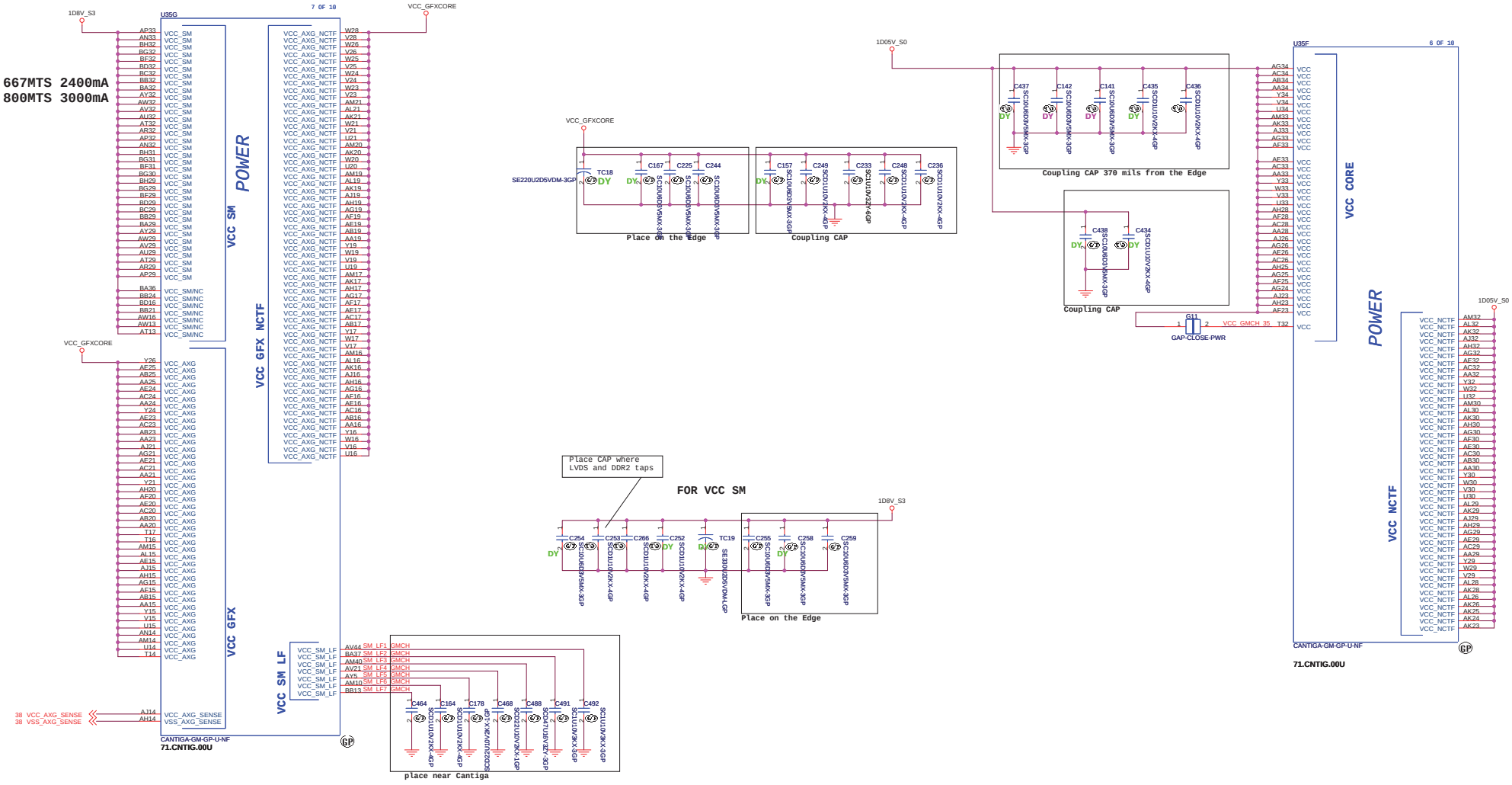
667MTS 2400mA
800MTS 3000mA



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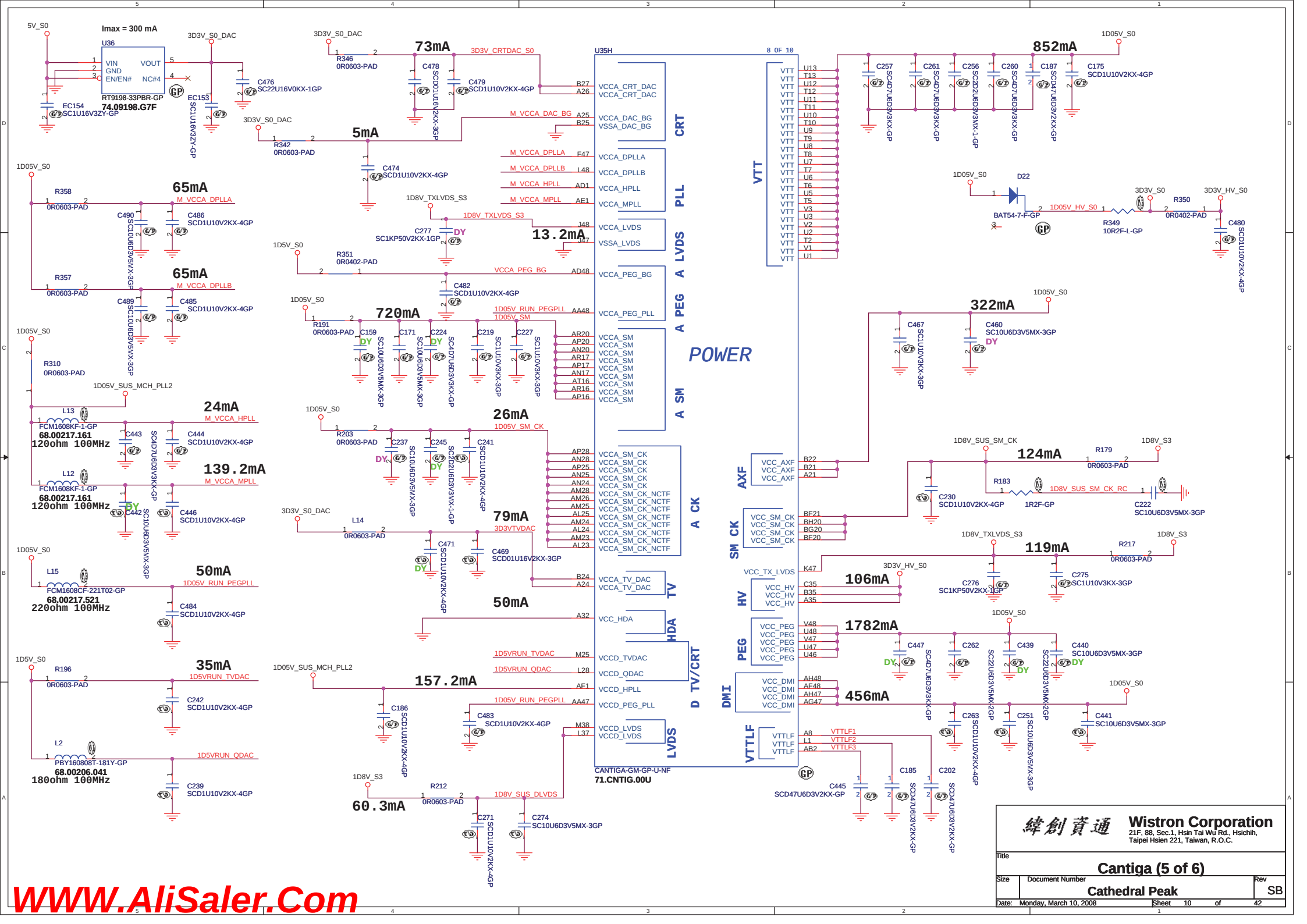
POWER
Imax = 300 mA
U36
RT9198-33PBR-GP
74.09198.G7F
73mA
5mA
65mA
65mA
720mA
13.2mA
852mA
322mA
24mA
139.2mA
26mA
79mA
124mA
119mA
50mA
106mA
1782mA
456mA
35mA
157.2mA
60.3mA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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Cantiga (5 of 6)
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Monday, March 10, 2008
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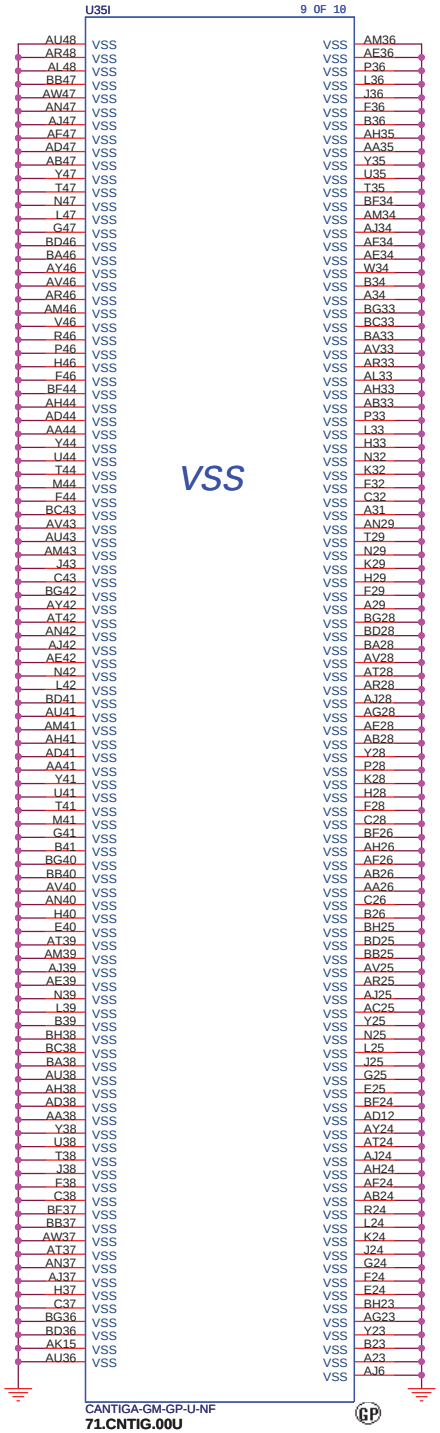

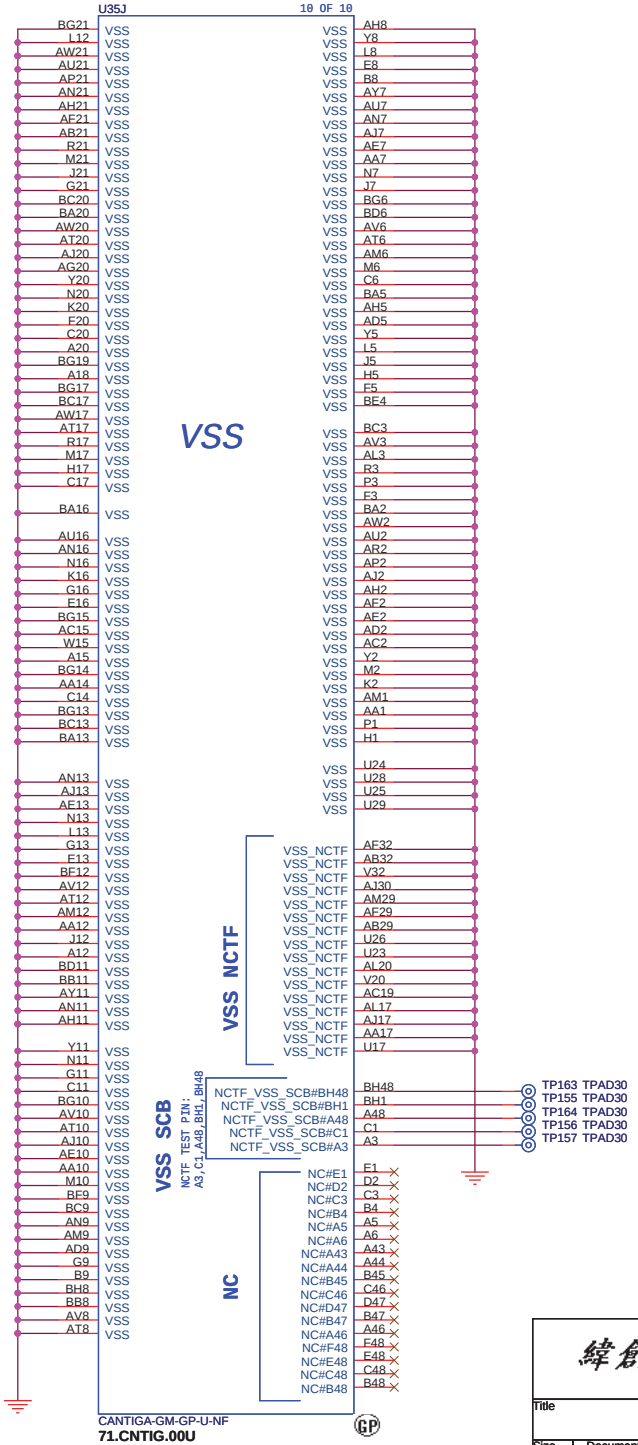

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Title: **Cantiga (6 of 6)**

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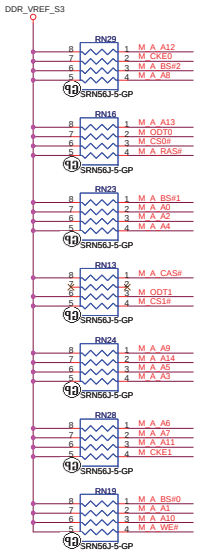
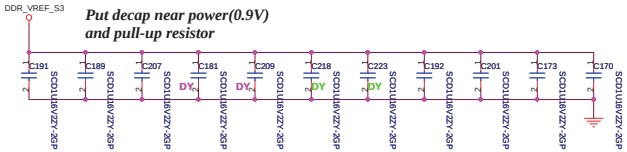
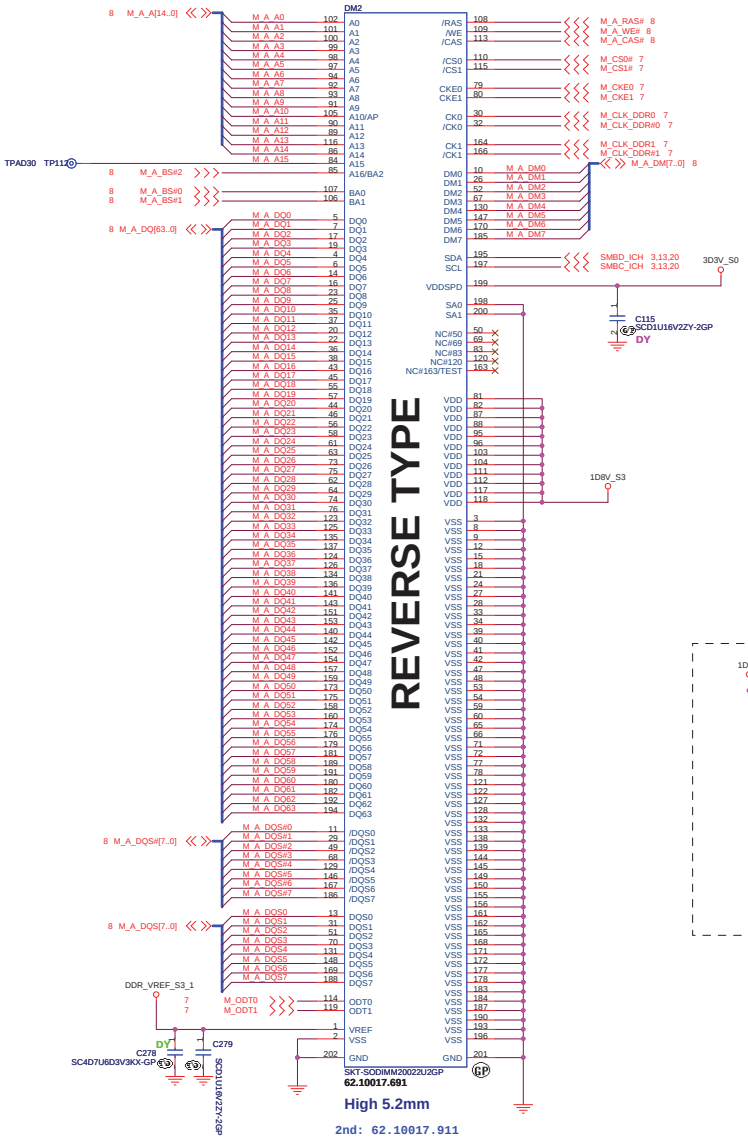
PARALLEL TERMINATION

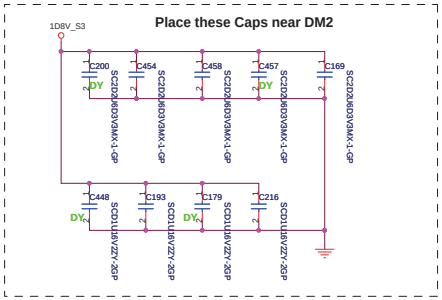
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







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Title	**DDR2 Socket 1 (DM2)**	
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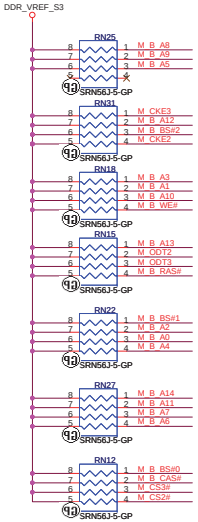
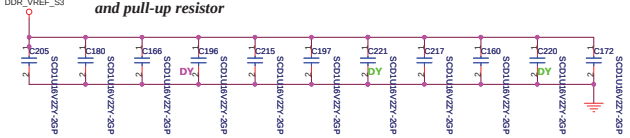
PARALLEL TERMINATION

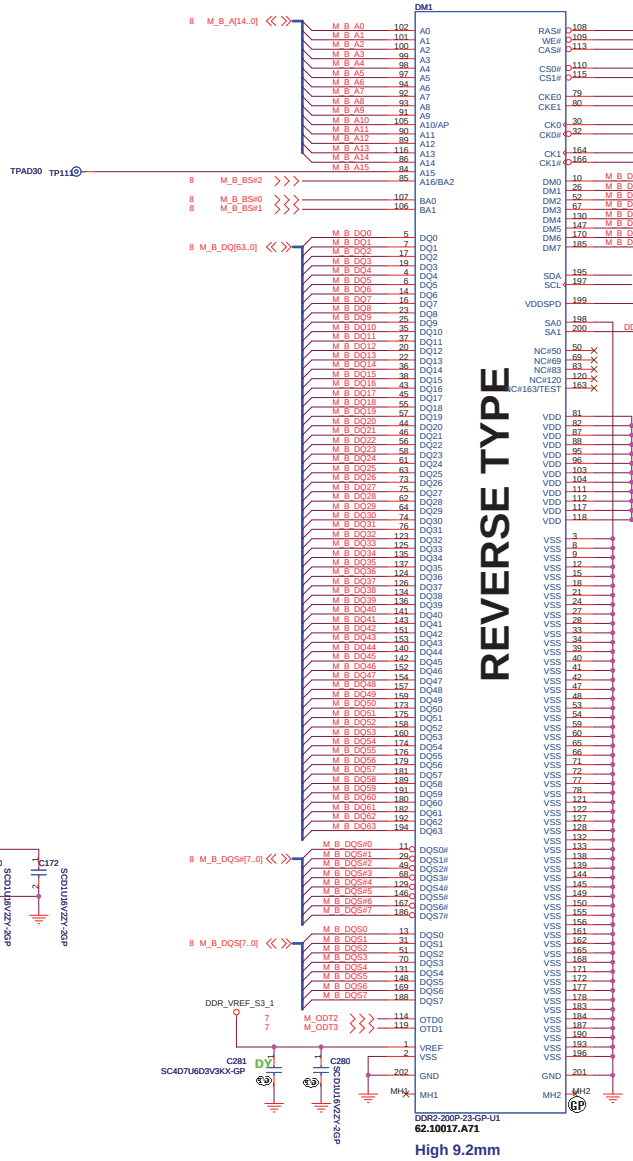
Put decap near power(0.9V) and pull-up resistor

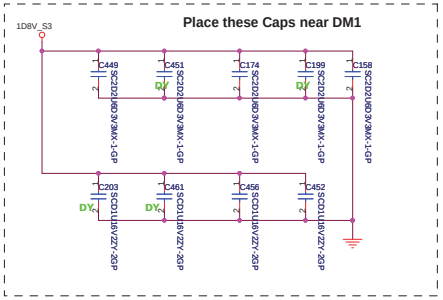


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor



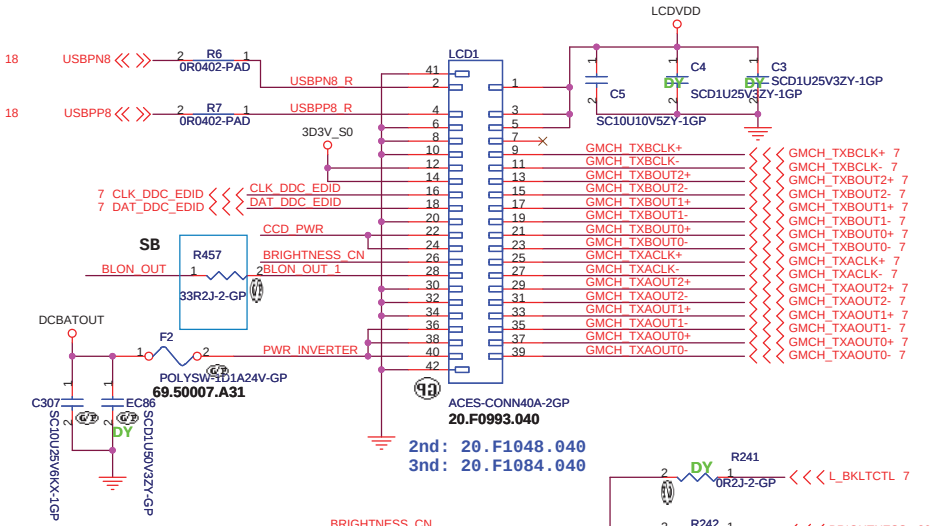


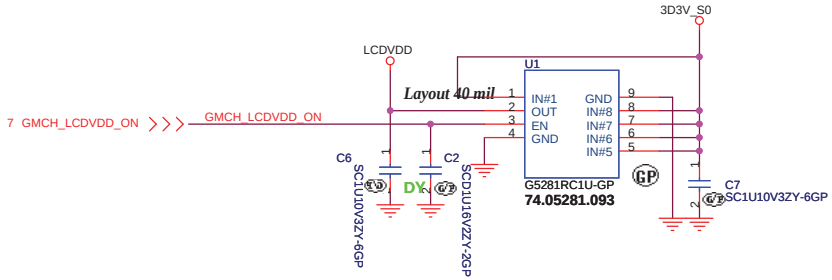


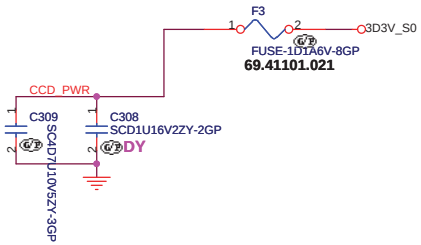
2nd: 62.10017.B51

緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DDR2 Socket 0 (DM1)			
Size	Document Number: Cathedral Peak	Rev: SB	
Date: Wednesday, March 12, 2008	Sheet 13 of 42		

LCD/INVERTER/CCD CONN



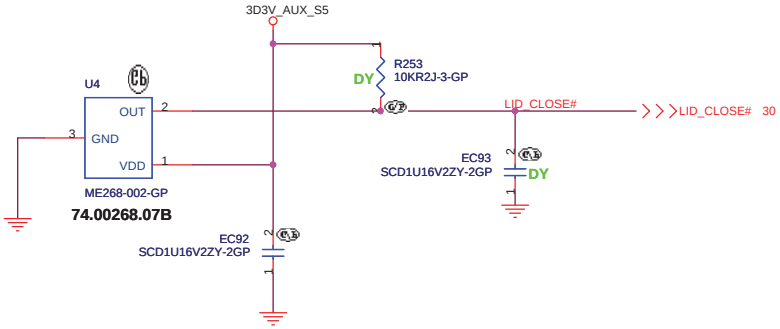




Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch



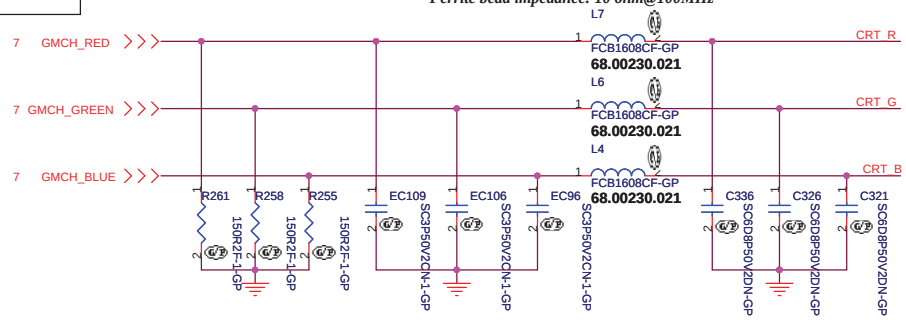
74.00268.A7B
74.00268.C7B

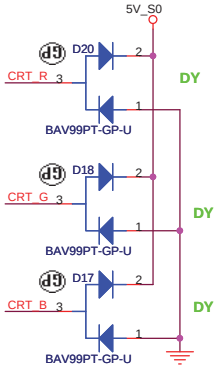
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN
Size | Document Number: Cathedral Peak | Rev: SB
Date: Monday, March 10, 2008 | Sheet 14 of 42

Layout Note:
Place these resistors close to the CRT-out connector

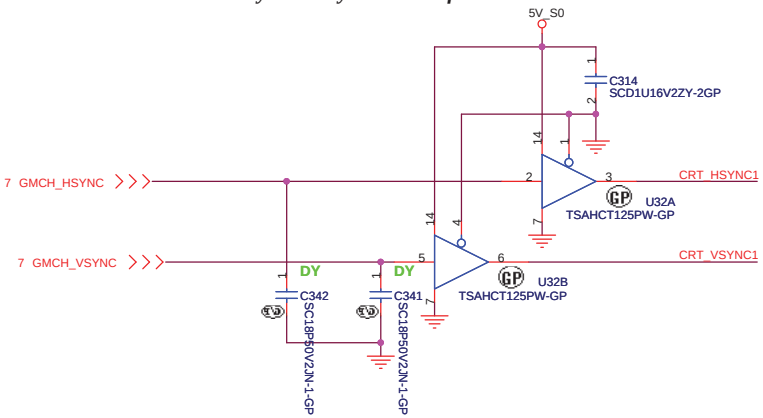
Ferrite bead impedance: 10 ohm@100MHz



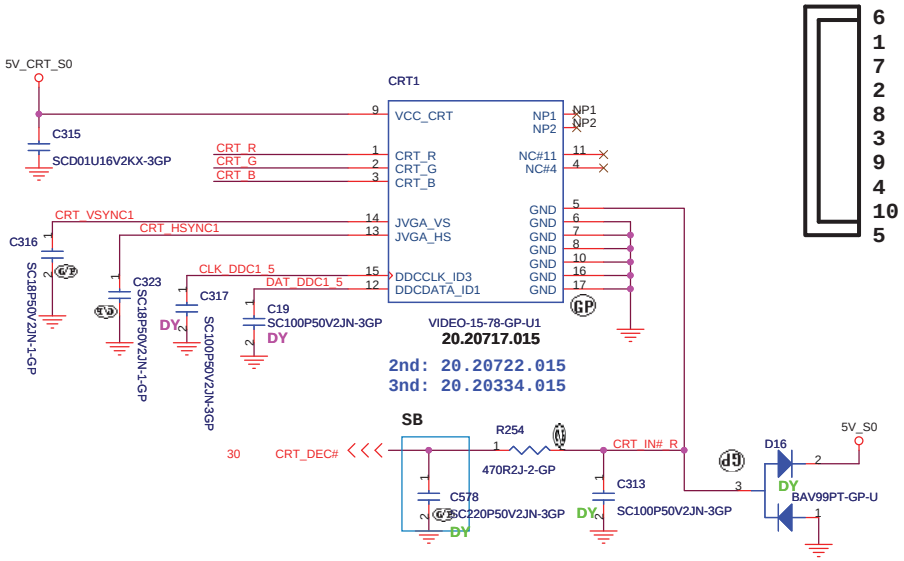


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

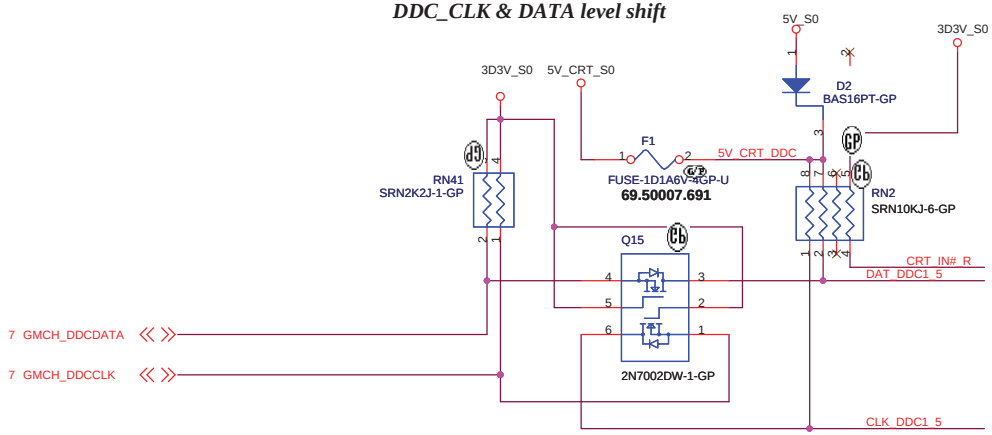
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



緯創資通 Wistron Corporation
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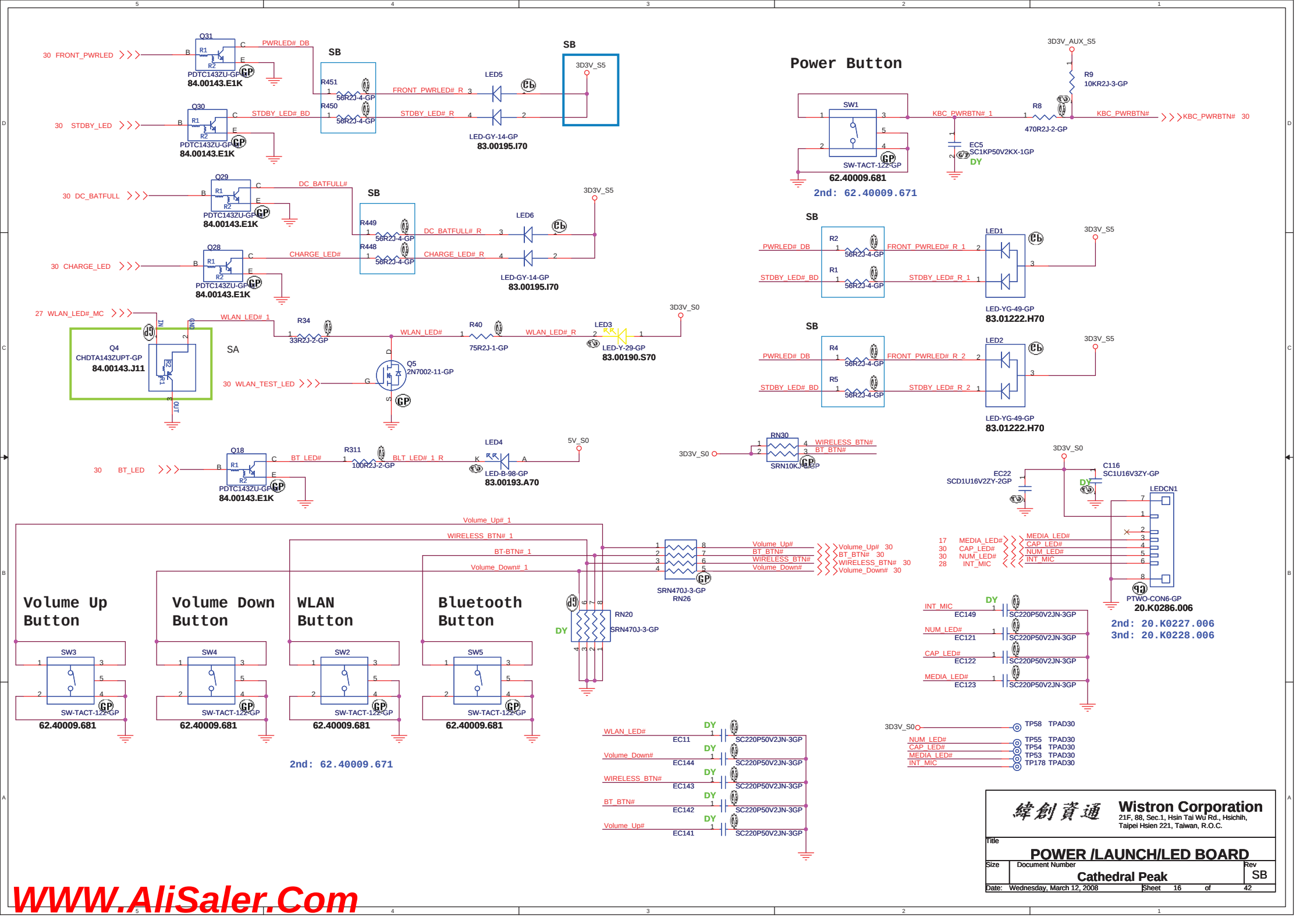
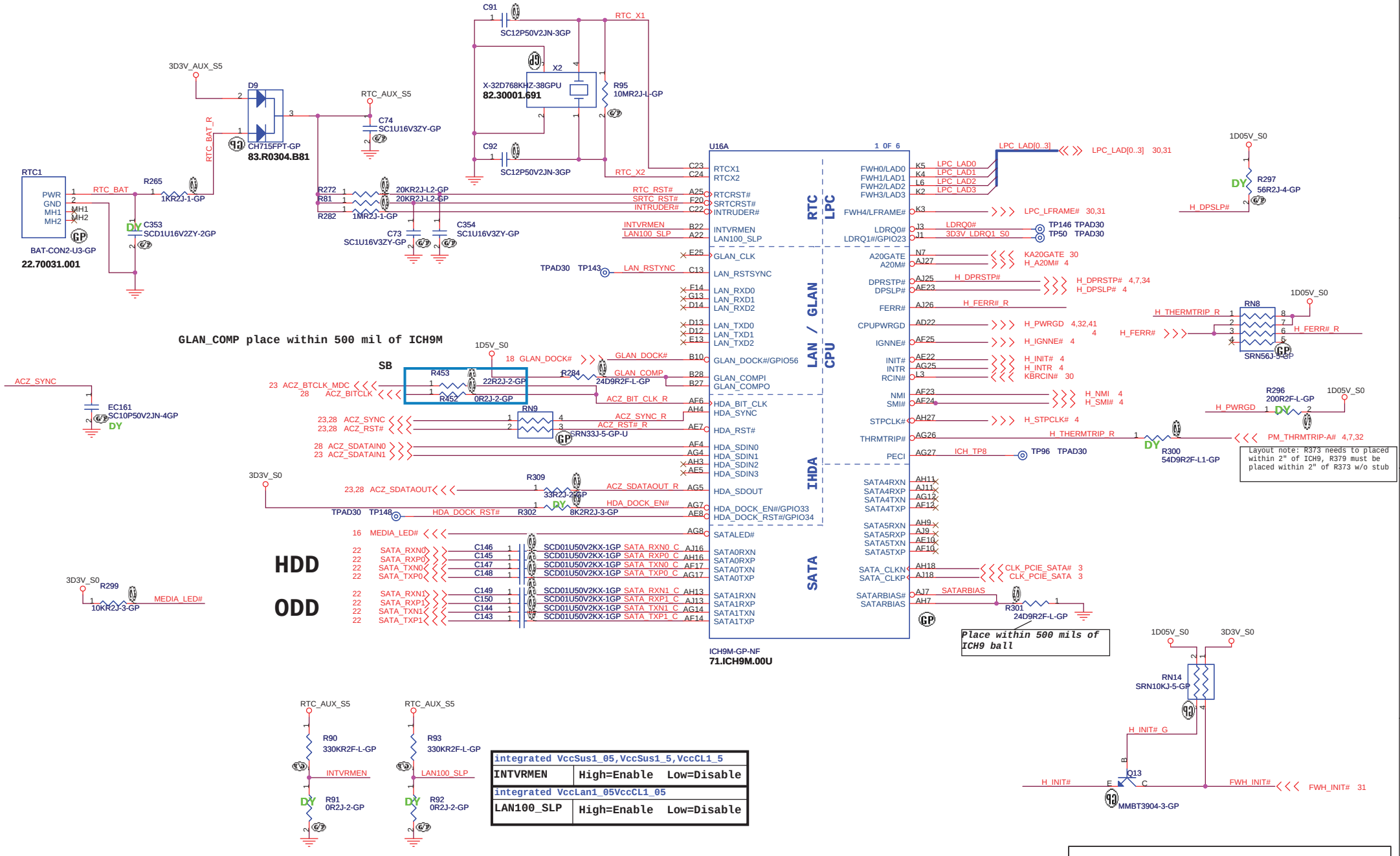
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size | Document Number: **Cathedral Peak** | Rev: SB

Date: Monday, March 10, 2008 | Sheet 15 of 42





Wistron Corporation	緯創資通
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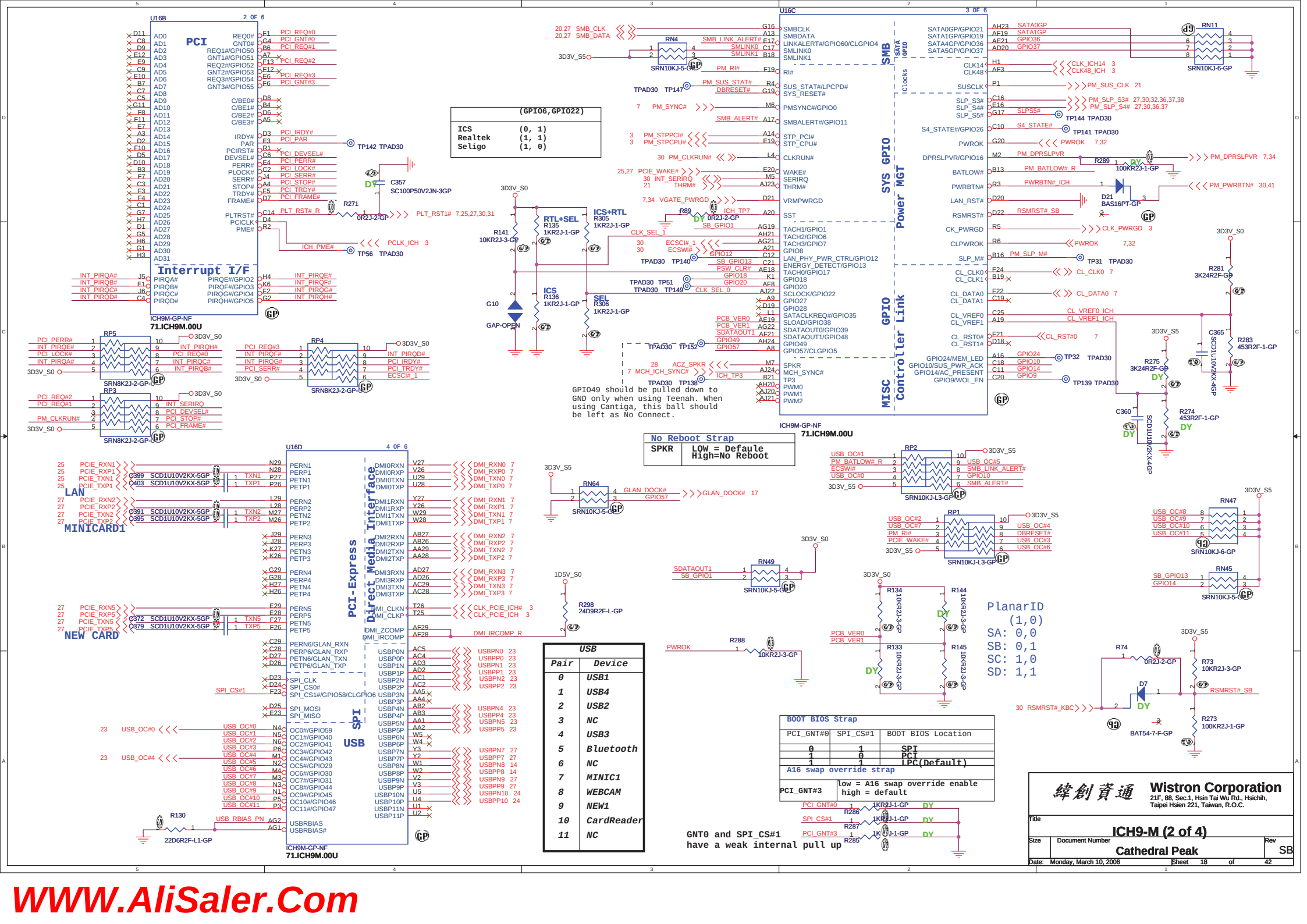
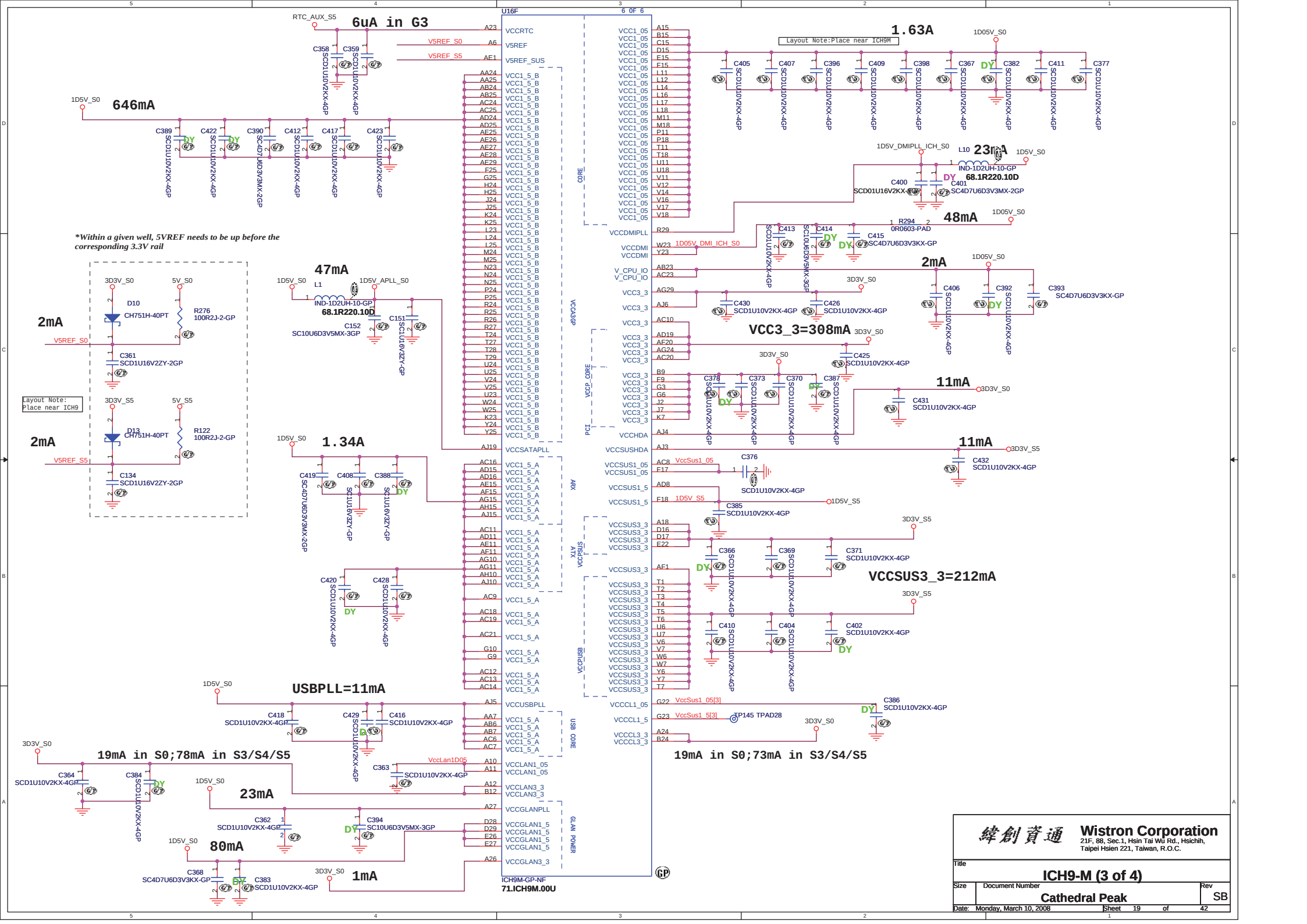
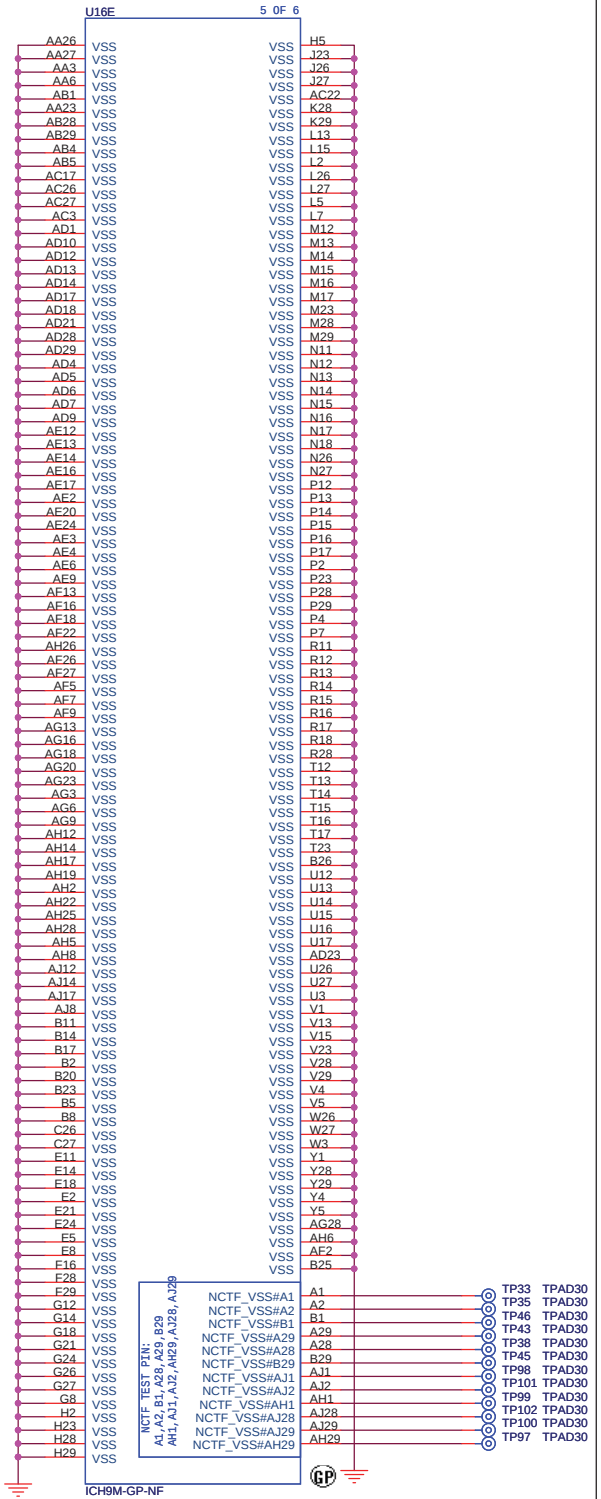
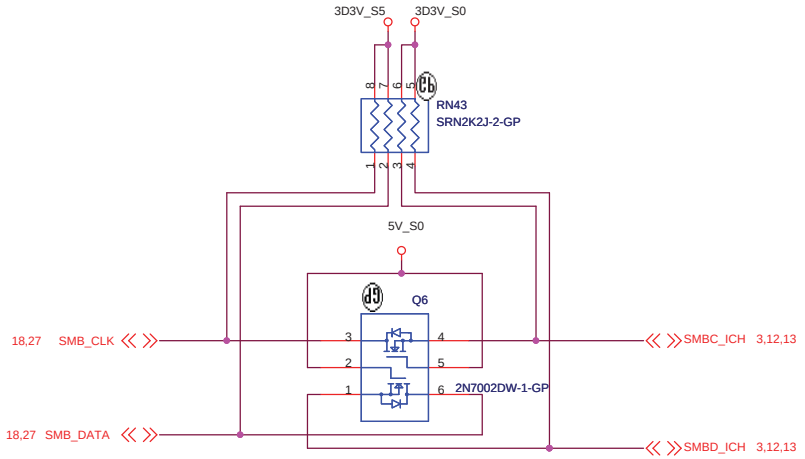
Title: ICH9-M (1 of 4)	
Size	Document Number: Cathedral Peak
Rev: SB	
Date: Monday, March 10, 2008	Sheet 17 of 42




U16F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
1.63A
Layout Note:Place near ICH9M
646mA
23mA
48mA
2mA
47mA
1.34A
VCC3_3=308mA
11mA
11mA
2mA
VCCSUS3_3=212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA in S0;73mA in S3/S4/S5
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH9
68.1R220.10D
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Cathedral Peak
SB
Monday, March 10, 2008
19
42





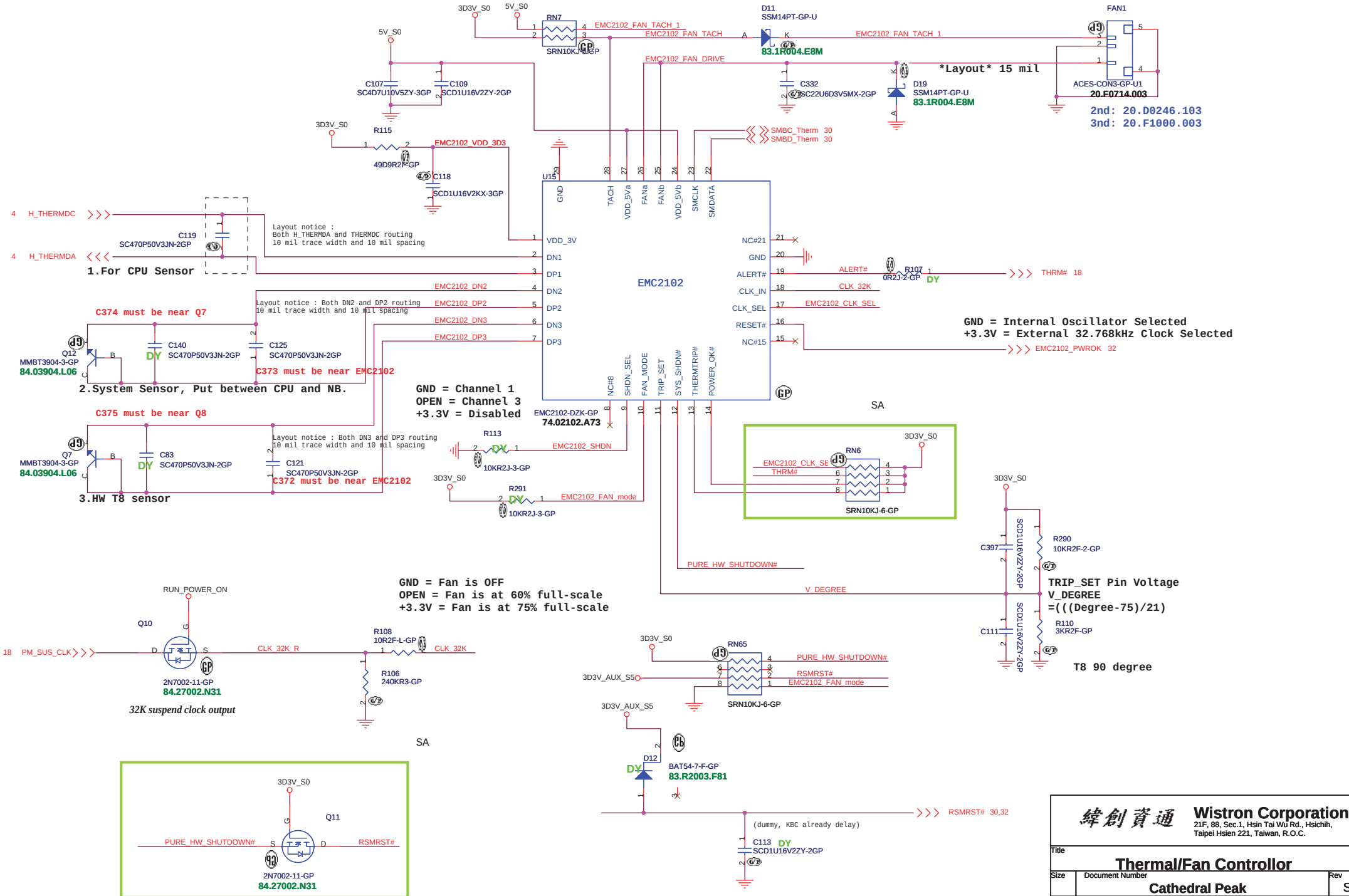
SMBUS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (4 of 4)**

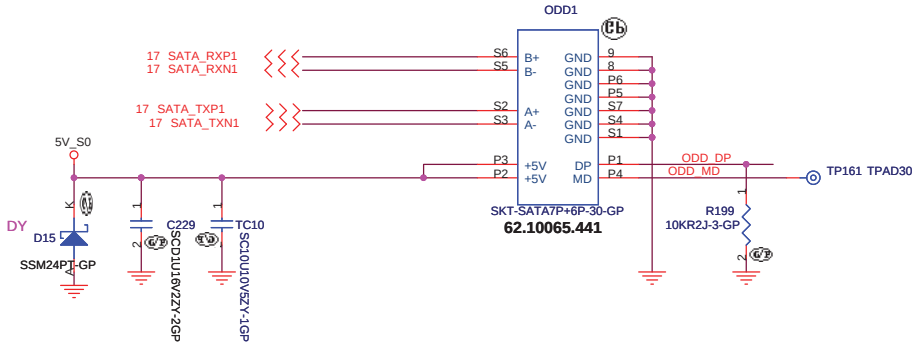
Size | Document Number: **Cathedral Peak** | Rev: SB

Date: Monday, March 10, 2008 | Sheet 20 of 42

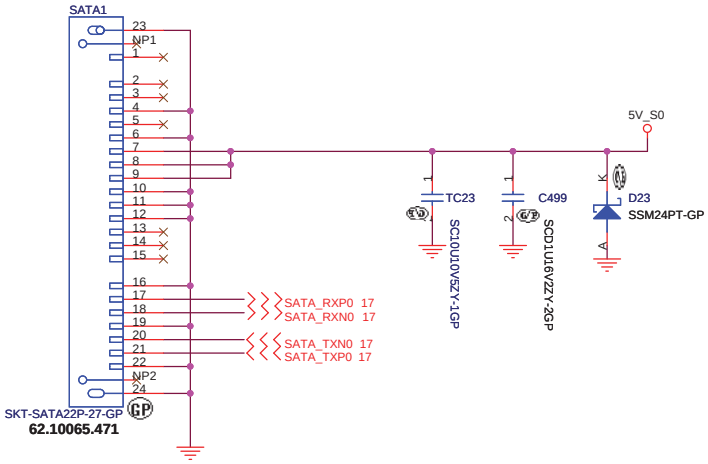


Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Thermal/Fan Controllor
Size	Document Number: Cathedral Peak
Rev	SB
Date: Tuesday, March 11, 2008	Sheet 21 of 42

SATA ODD Connector

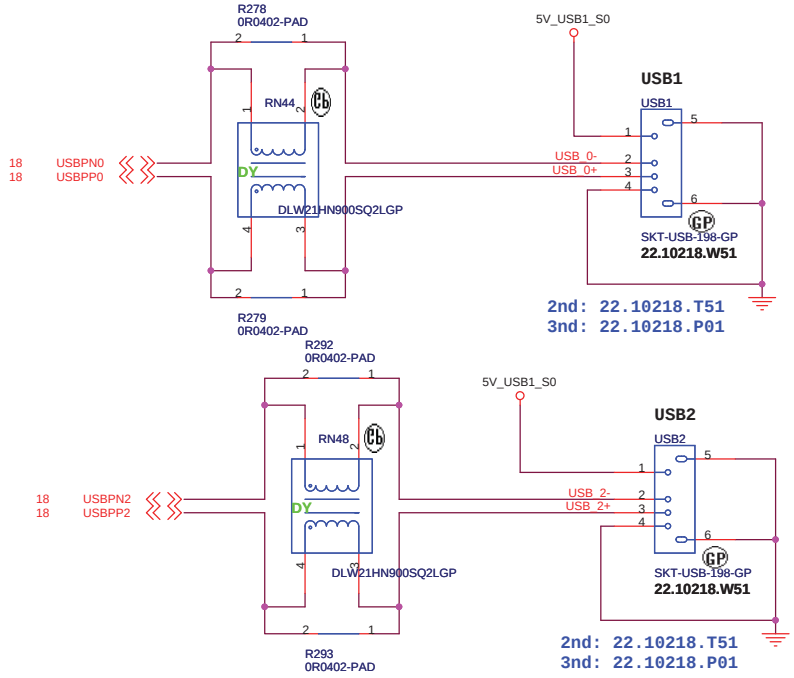


SATA Connector

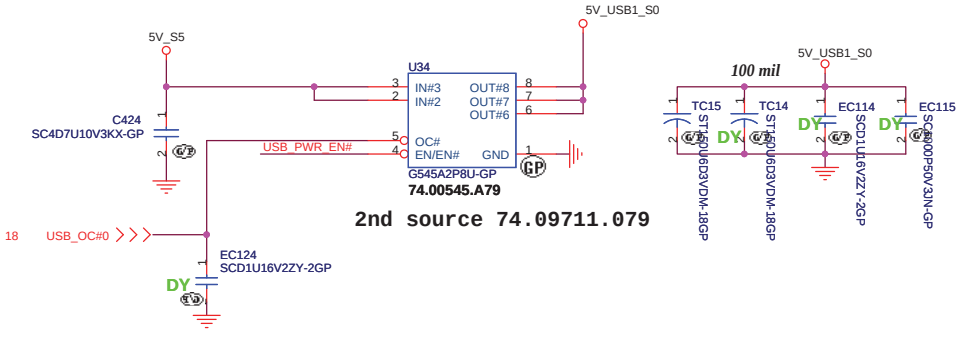


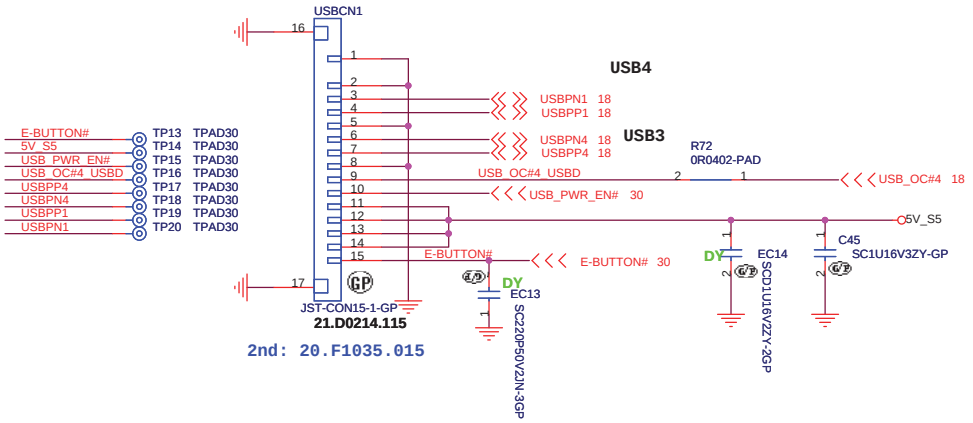
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD & CDROM		
Size	Document Number: Cathedral Peak	Rev: SB
Date: Tuesday, March 11, 2008	Sheet 22 of 42	

Co-Layout Common Mode Choke and 0 Ohm



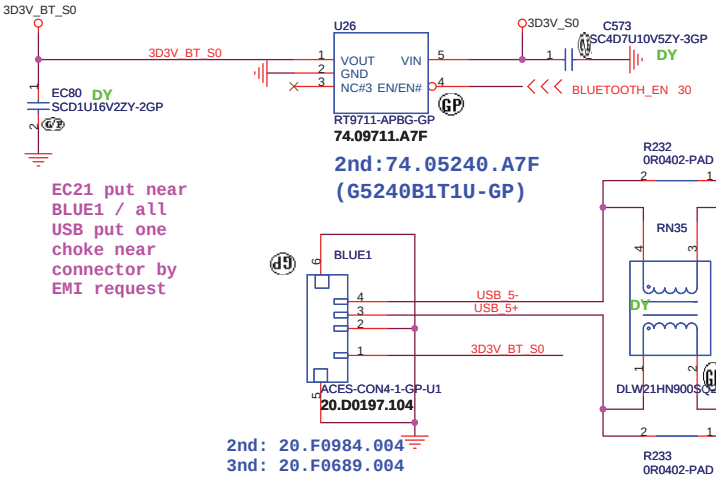
Co-Layout Common Mode Choke and 0 Ohm



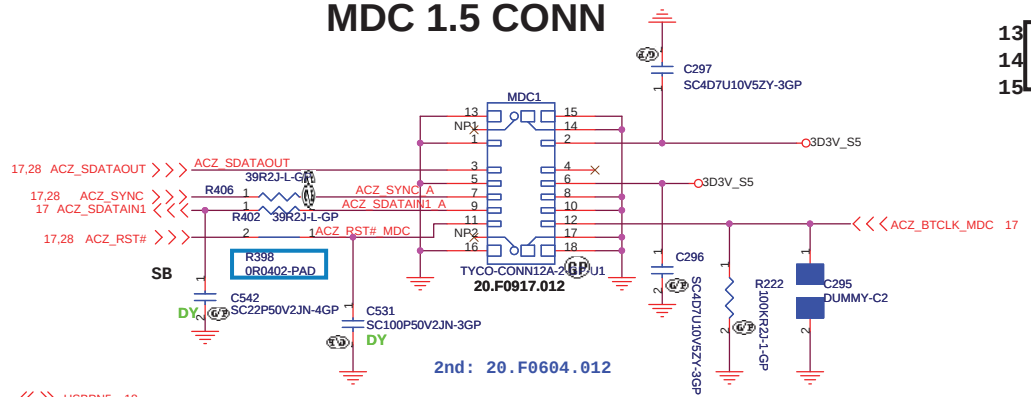


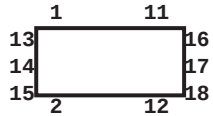
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



MDC 1.5 CONN



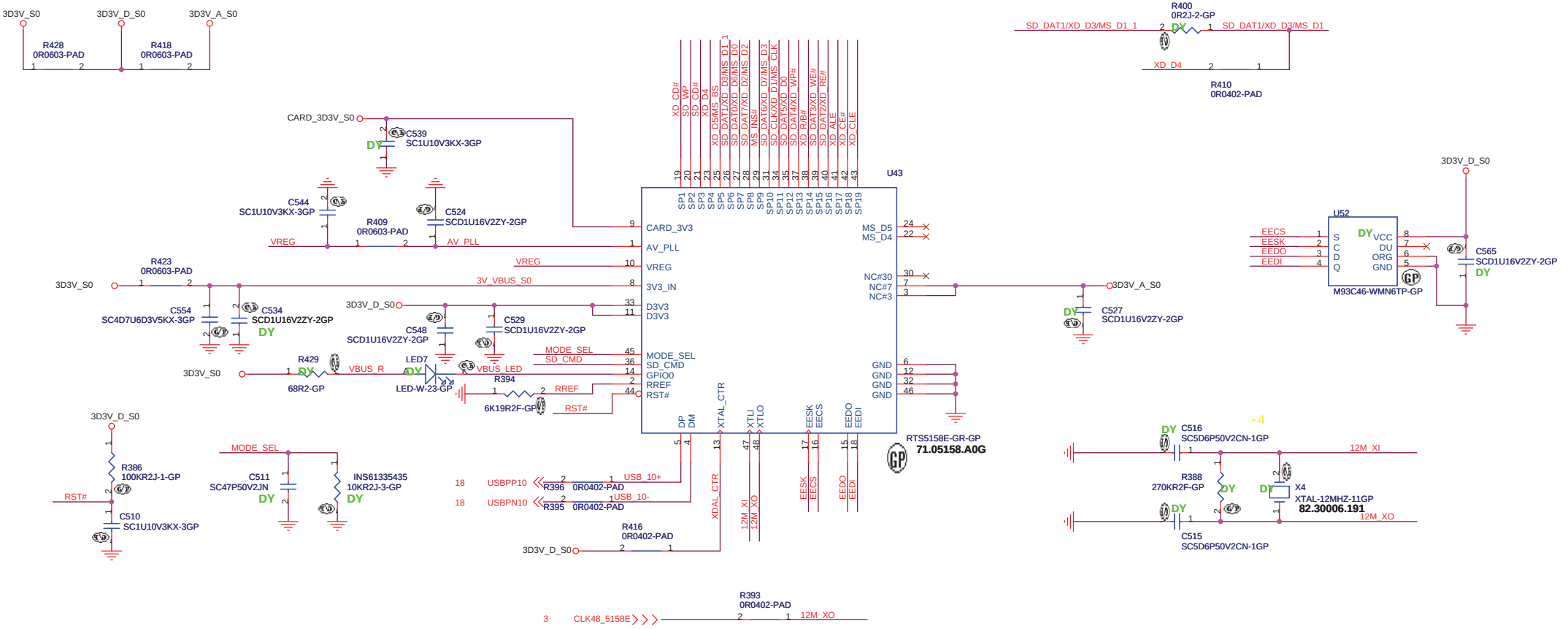


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

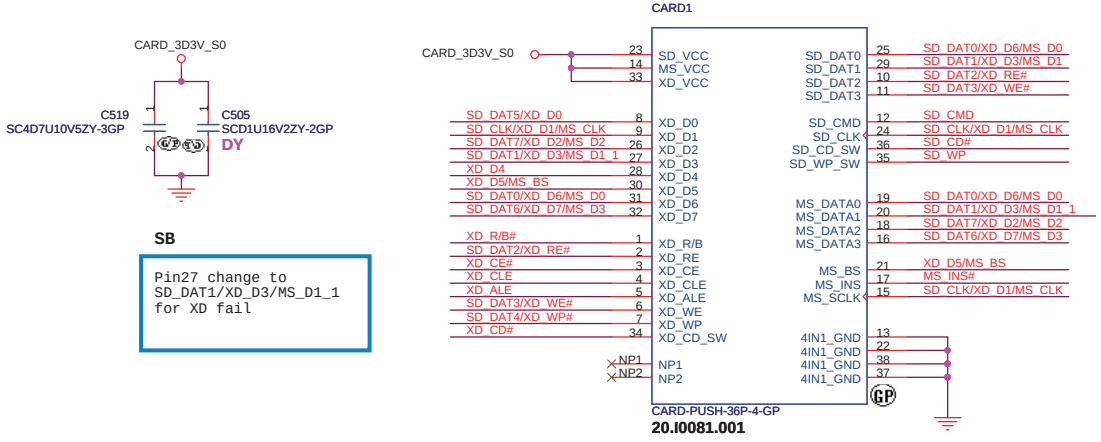
Title: USB/BLUETOOTH/MDC

Size | Document Number: Cathedral Peak | Rev: SB

Date: Monday, March 10, 2008 | Sheet 23 of 42



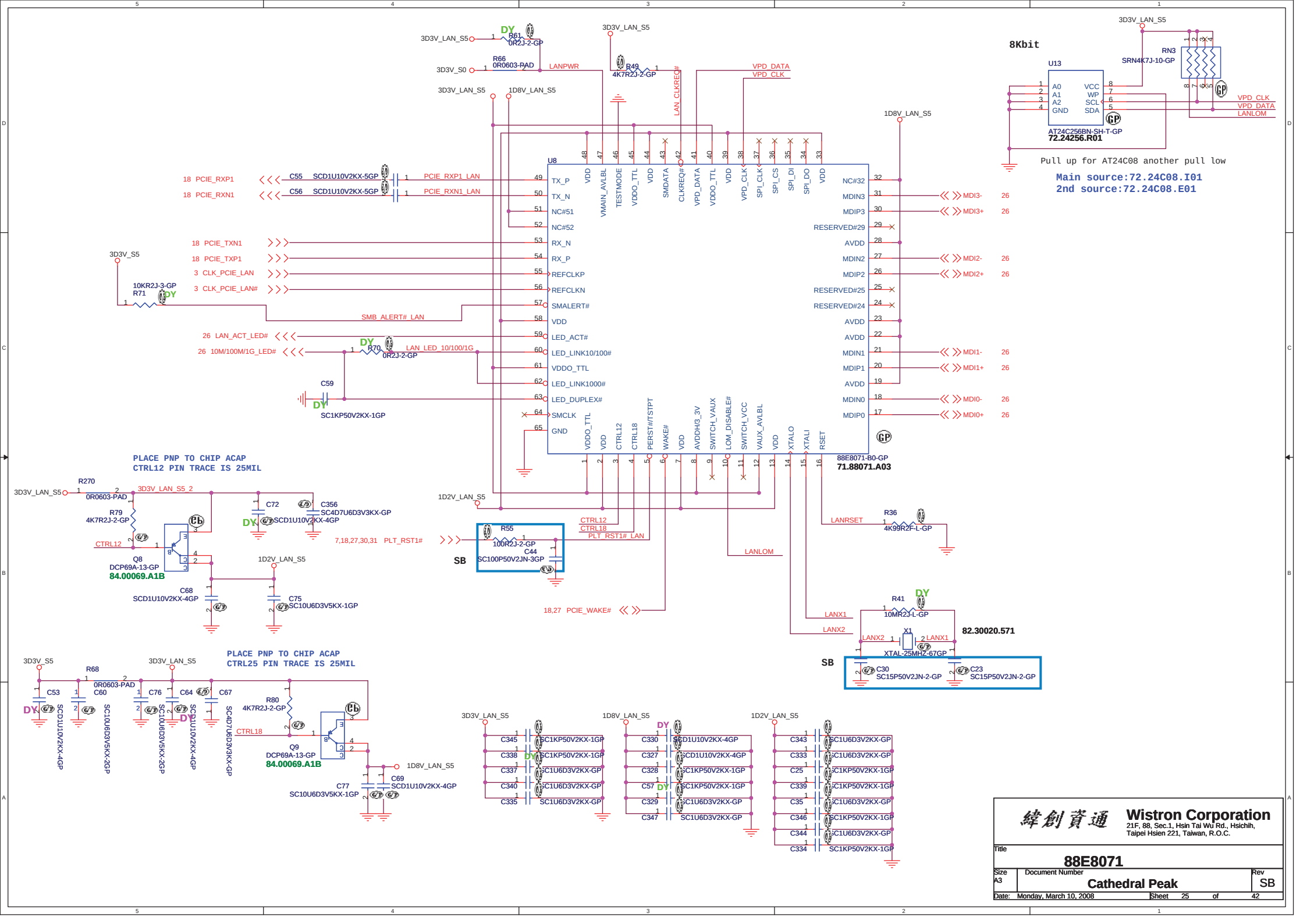
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



SB

Pin27 change to
SD_DAT1/XD_D3/MS_D1_1
for XD fail

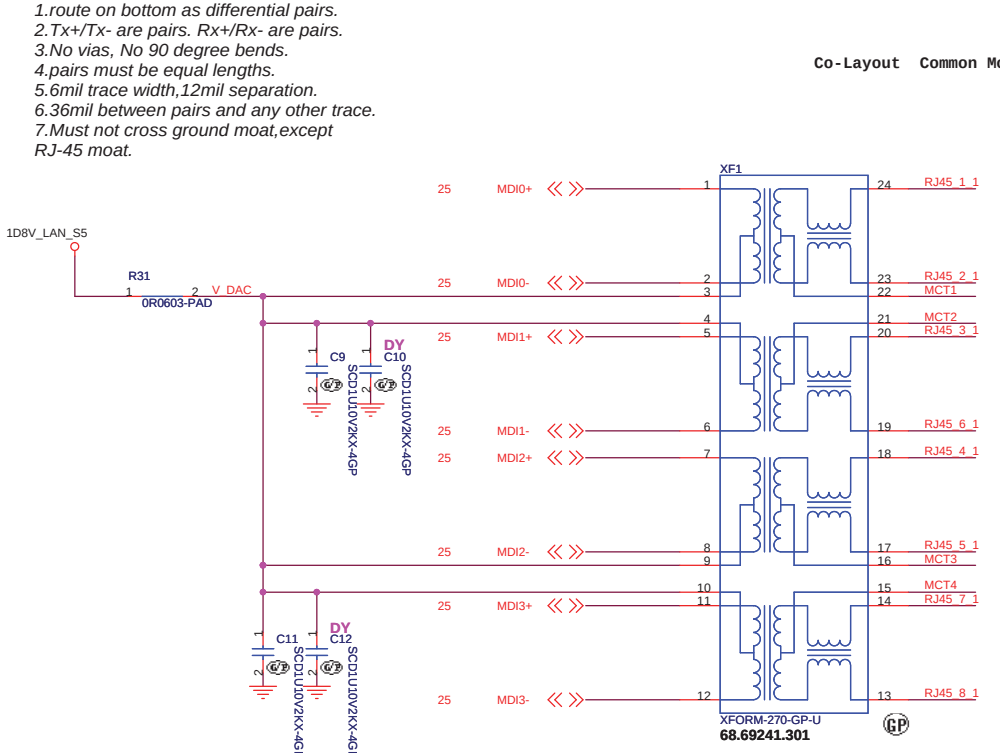
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CARDREADER- RTS5158E**	
Size	Document Number **Cathedral Peak**	Rev SB
Date: Monday, March 10, 2008	Sheet 24 of 42	

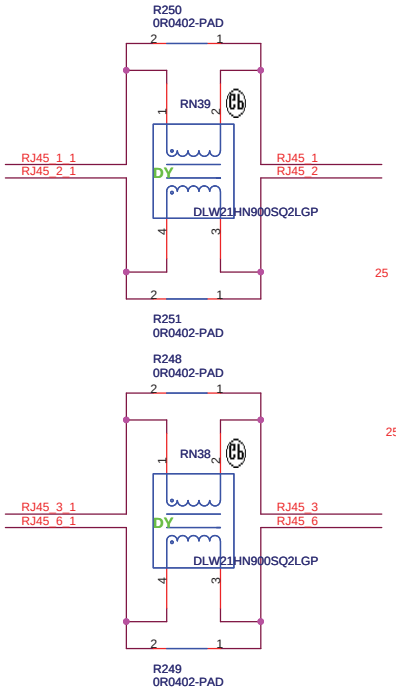

8Kbit
U13
AT24C256BN-SH-T-GP
72.24256.R01
Pull up for AT24C08 another pull low
Main source:72.24C08.I01
2nd source:72.24C08.E01
U8
88E8071-B0-GP
71.88071.A03
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
SB
82.30020.571
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
88E8071
Size A3
Document Number
Cathedral Peak
Rev SB
Date: Monday, March 10, 2008
Sheet 25 of 42

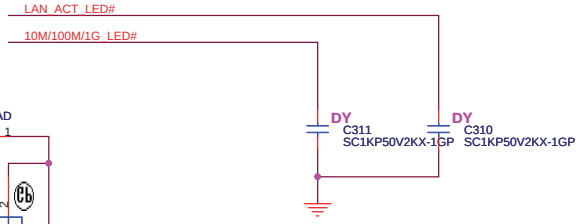
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

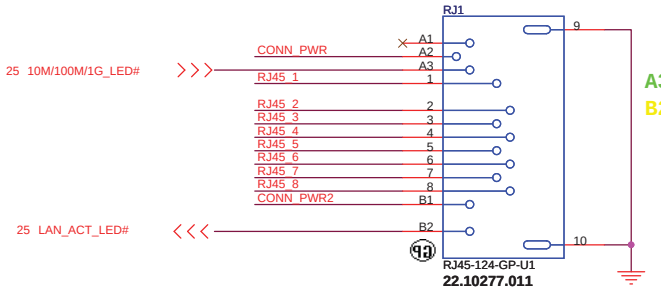
Co-Layout Common Mode Choke and 0 Ohm







LAN Connector



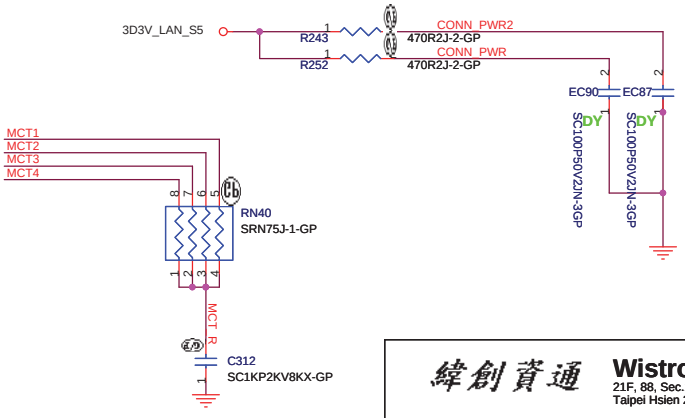
A3:GREEN
B2:Orange

2nd: 22.10277.061

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

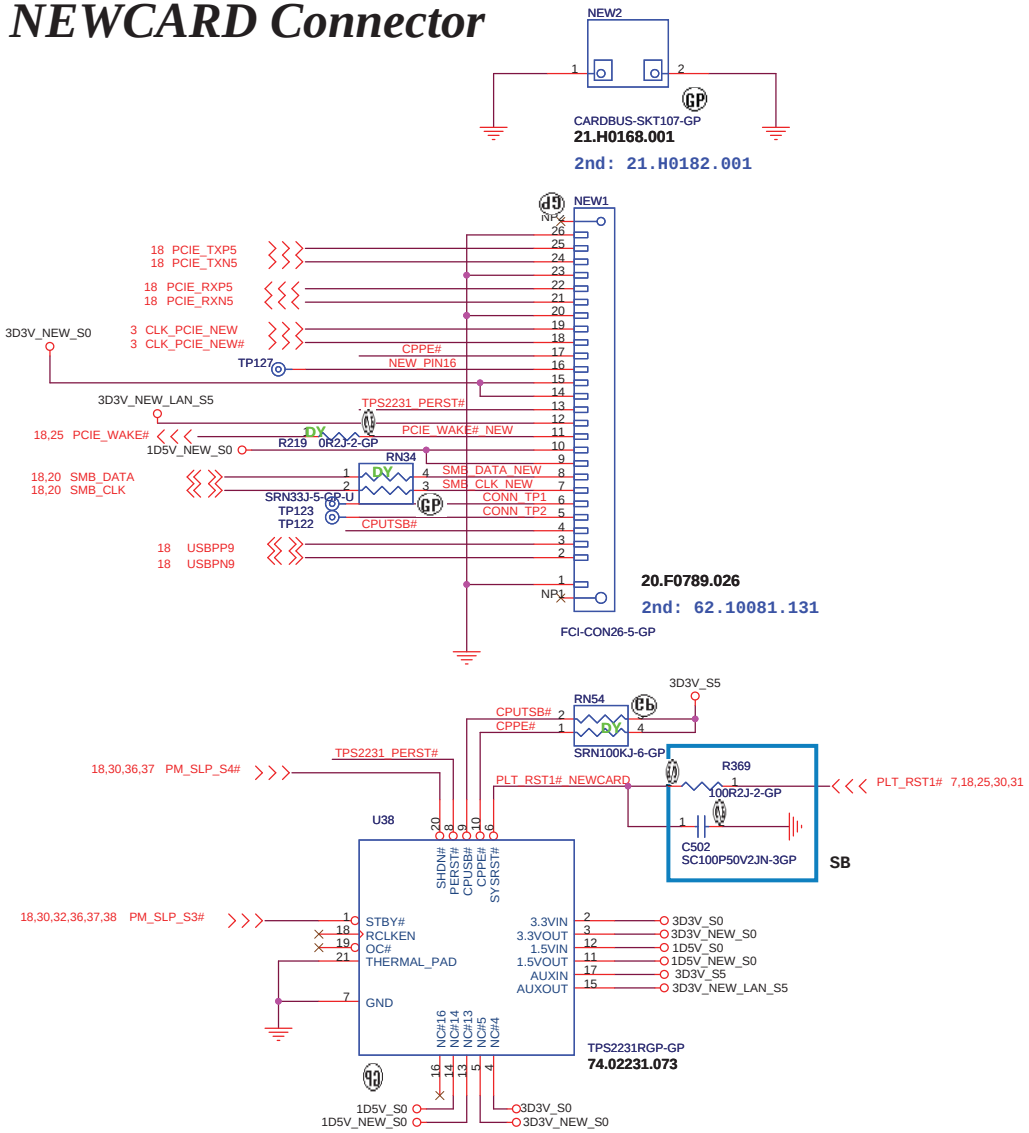
LAN Data: Yellow(B2), when LAN is transfering data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

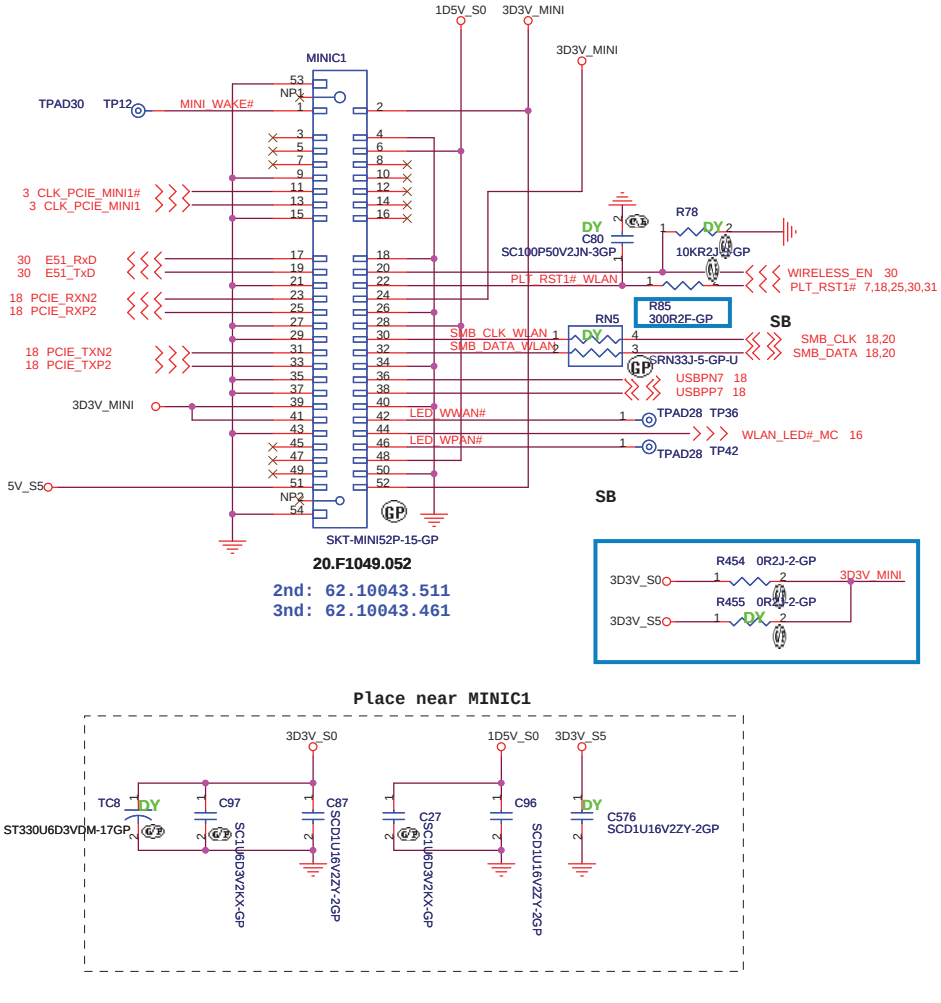


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LAN CONN		
Size: A3	Document Number: Cathedral Peak	Rev: SB
Date: Monday, March 10, 2008	Sheet 26 of 42	

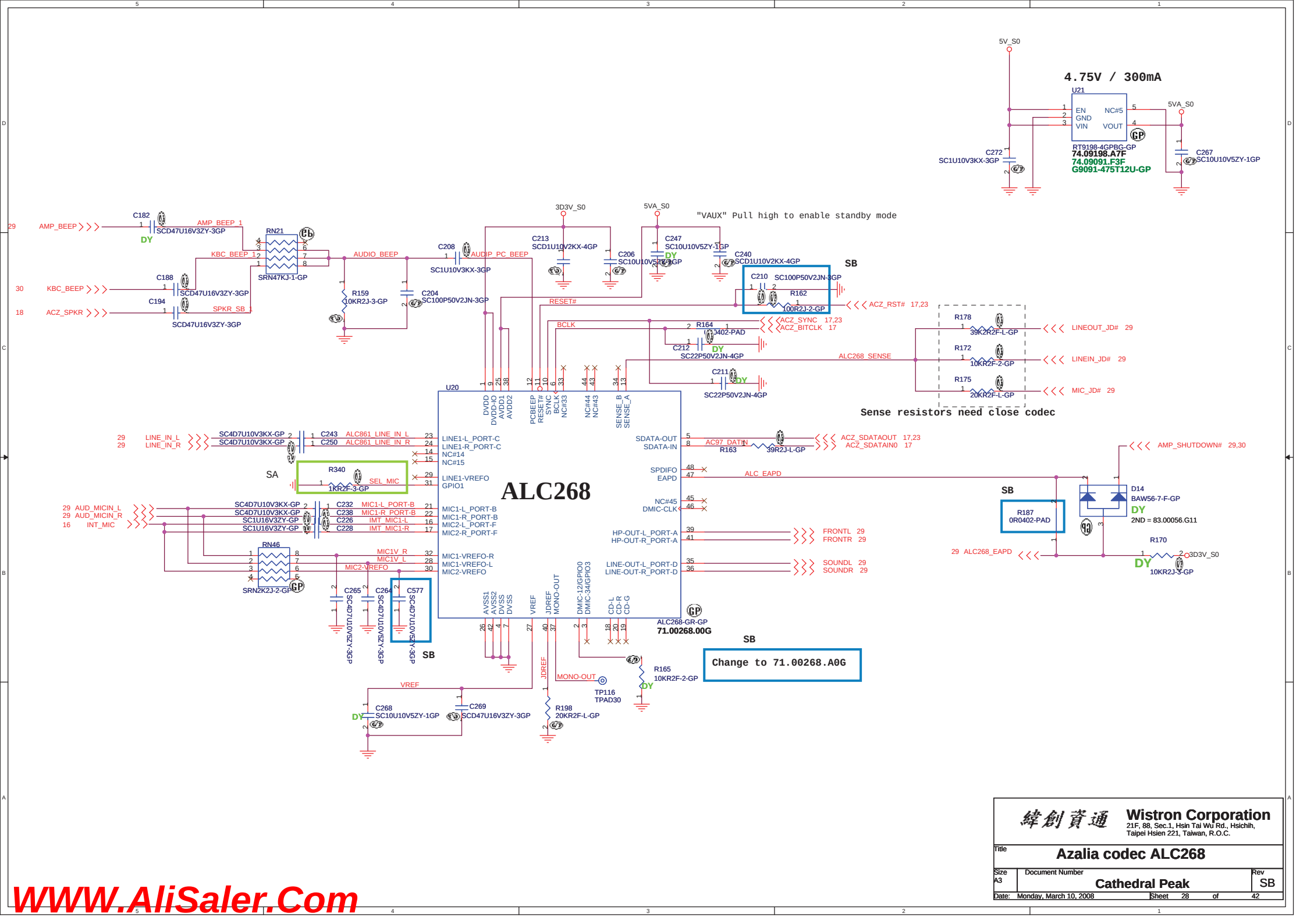
NEWCARD Connector



Mini Card Connector(WLAN)



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: NEW CARD/MINI CARD		
Size	Document Number: Cathedral Peak	Rev: SB
Date: Monday, March 10, 2008	Sheet 27 of 42	



AUDIO OP AMPLIFIER

SA

SB

Layout Note :
C218,C219,C220 near U110

5V_S0 3D3V_S0

C132 SC1U10V3KX-3GP R129 0R0402-PAD
28 SOUNDR INR_A

C133 SC1U10V3KX-3GP R127 0R0402-PAD
28 SOUNDL INL_A

C128 SC3D3U10V5ZY-1GP R128 40K2R2F-GP
28 FRONTR INR_H

C129 SC3D3U10V5ZY-1GP R126 40K2R2F-GP
28 FRONTL INL_H

R137 16KR2F-GP
SET
R138 30KR2F-GP

C138 SCD1U16V2ZY-2GP C137 SC1U6D3V5MX-3GP
C161 SC1U10V3KX-3GP

C168 SC2D2U6D3V3MX-1-GP
BIAS
C162 SCD1U16V2ZY-2GP

U18
VDD GND INR_A INR_H INL_A INL_H PGND LOUT+ LOUT- PVDD CVDD CP+ CGND CP-
GND BEEP AMP_EN# SET BIAS HP_EN PGND ROUT+ ROUT- PVDD HVDD HP_L HP_R HVSS CVSS
APA2057ARI-TRL-GP
74.02057.01G

INR_A INR_H INL_A INL_H
SPKR_L+ SPKR_L-
C139 SC1U10V3KX-3GP

R139 0R2J-2-GP DY
AMP_BEEP 28
SPK_EN# SET BIAS HP_EN
SPKR_R+ SPKR_R-
SPKR_L+1 SPKR_R+1
5V_S0 3D3V_S0
C153 SC1U10V3KX-3GP

HP_EN
R143 0R2J-2-GP DY
AMP_SHUTDOWN# 28,30
C163 SCD1U16V2ZY-2GP DY
R142 0R0402-PAD
ALC268_EAPD 28

R147 10KR2J-3-GP
SPK_EN#
Q14 2N7002-11-GP
G
AMP_SHUTDOWN# 28,30

Internal Speaker

SPKR_R+ SPKR_R- SPKR_L+ SPKR_L-
INTSPK1
ACES-CON4-1-GP-U2
20.D0197.104
EC1 EC2 EC3 EC4 SC100P50V2JN-3GP

SPKR_L- SPKR_L+ SPKR_R- SPKR_R+
TP1 TPAD30
TP2 TPAD30
TP3 TPAD30
TP4 TPAD30

2nd: 20.F0984.004
3nd: 20.F0689.004

LINE OUT

LOUT1
PHONE-JK235-GP-U2
22.10133.B21
2nd: 22.10251.511
3nd: 22.10147.151

SB
LINEOUT_JD# 28
SPKR_R_A1 SPKR_L_A1
RN68 SRN68J-5GP
SPKR_R+1 SPKR_L+1
EC152 SC1KP50V2KX-1GP
C466 SC680P50V2KX-2GP
C473 SC680P50V2KX-2GP
R329 1KR2J-1-GP
R335 1KR2J-1-GP

LINEOUT_JD# TP117 TPAD30
SPKR_R_A1 TP114 TPAD30
SPKR_L_A1 TP113 TPAD30
MIC_JD# TP109 TPAD30
AUD_MICIN_R TP160 TPAD30
AUD_MICIN_L TP159 TPAD30
LINEIN_JD# TP105 TPAD30
LINE_IN_R TP154 TPAD30
LINE_IN_L TP153 TPAD30

MIC IN

EC60 SC1KP50V2KX-1GP
MICIN1
28 MIC_JD#
28 AUD_MICIN_R
28 AUD_MICIN_L
RN66 SRN1KJ-7-GP
AUD_MIC_R AUD_MIC_L
R321 10KR2J-3-GP
R326 10KR2J-3-GP
EC140 EC145 SC1KP50V2KX-1GP
PHONE-JK233-GP-U2
22.10133.B01
2nd: 22.10251.491
3nd: 22.10147.131

LINE IN

EC52 SC1KP50V2KX-1GP
LINEIN1
28 LINEIN_JD#
28 LINE_IN_R
28 LINE_IN_L
RN67 SRN1KJ-7-GP
AUD_LINE_R AUD_LINE_L
R303 10KR2J-3-GP
R308 10KR2J-3-GP
EC127 EC128 SC1KP50V2KX-1GP
PHONE-JK234-GP-U2
22.10133.B11
2nd: 22.10251.501
3nd: 22.10147.141

Analog Int. Mic

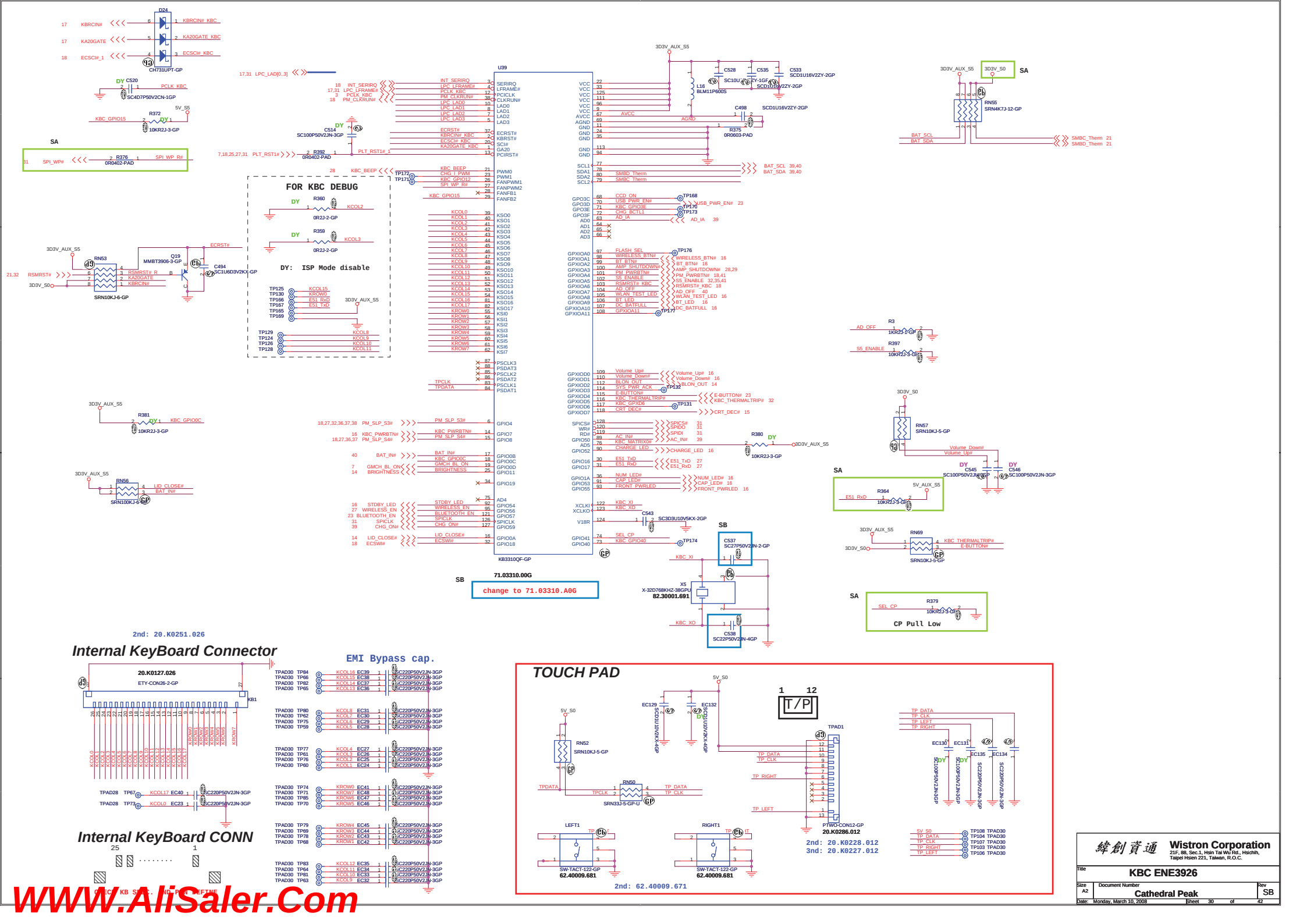
remove to LED Board

SB

For ESD

5V_S0 5V_S0
D28 1SS400PT DY
D27 1SS400PT DY
SPKR_L_A1
SPKR_R_A1
U55 SD05C-1-GP DY
U56 DY SD05C-1-GP

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AUDIO AMP AND JACK	
Size	Document Number: Cathedral Peak	Rev: SB
Date: Monday, March 10, 2008	Sheet 29 of 42	


FOR KBC DEBUG
DY: ISP Mode disable
SA
SB
71.03310.00G
change to 71.03310.A0G
CP Pull Low
2nd: 20.K0251.026
Internal KeyBoard Connector
20.K0127.026
ETY-CON26-2-GP
EMI Bypass cap.
Internal KeyBoard CONN
TOUCH PAD
T/P
PTWO-CON12-GP
20.K0286.012
2nd: 20.K0228.012
3nd: 20.K0227.012
2nd: 62.40009.671
SW-TACT-122-GP
62.40009.681
KB3310QF-GP
X5
X-32D768KHZ-38GPU
82.30001.691
U39
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ENE3926
Cathedral Peak
SB
Monday, March 10, 2008
30
42
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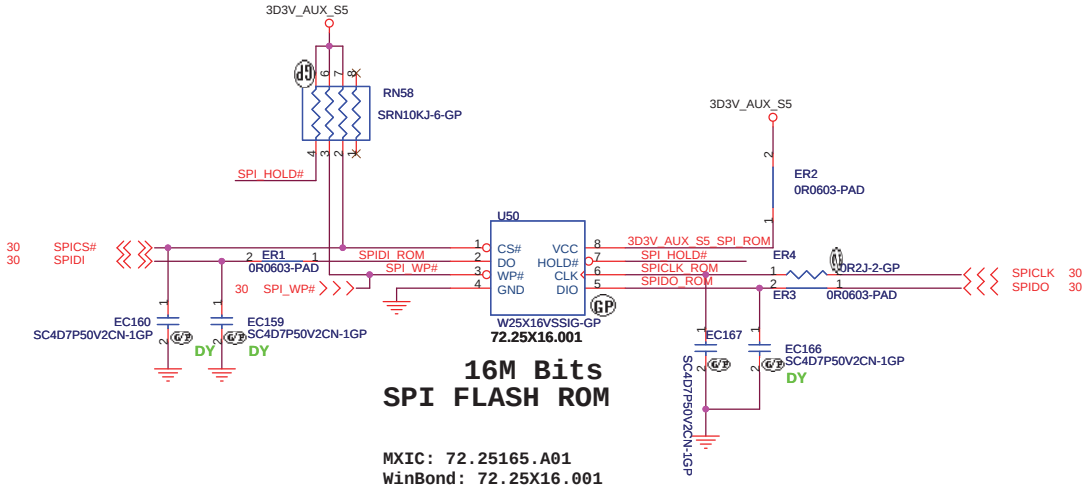


16M Bits SPI FLASH ROM

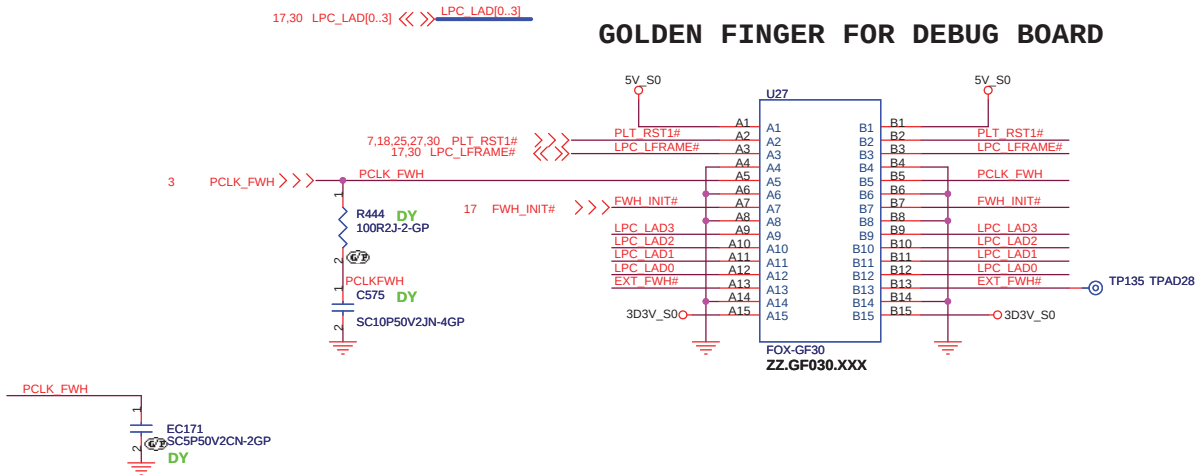
MXIC: 72.25165.A01
WinBond: 72.25X16.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



緯創資通 **Wistron Corporation**
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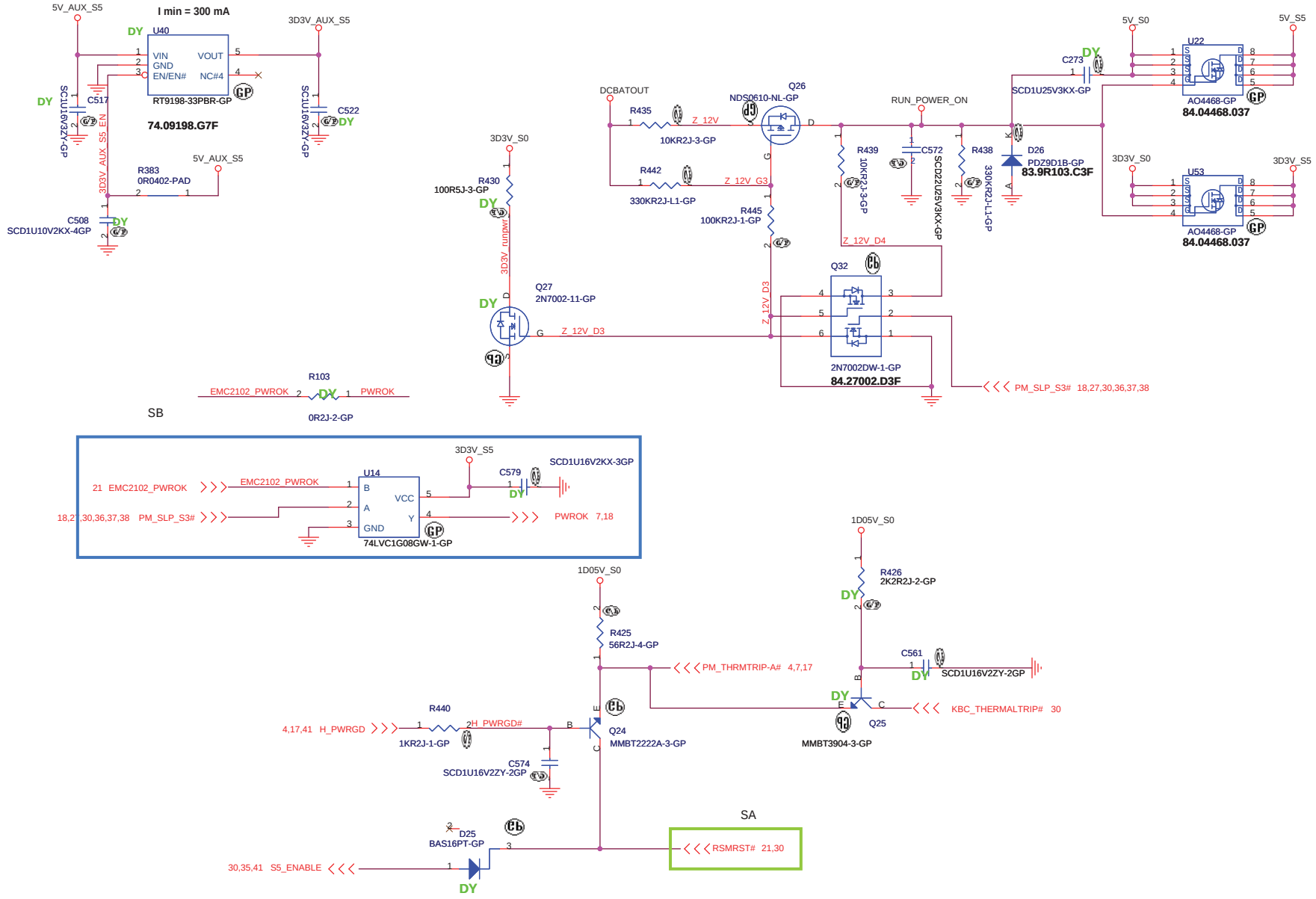
Taipei Hsien 221, Taiwan, R.O.C.

Title	**BIOS/GOLDEN FINGER**	
Size	Document Number: **Cathedral Peak**	Rev: SB
Date: Monday, March 10, 2008	Sheet 31 of 42	

Aux Power

3D3V_AUX_S5

Run Power

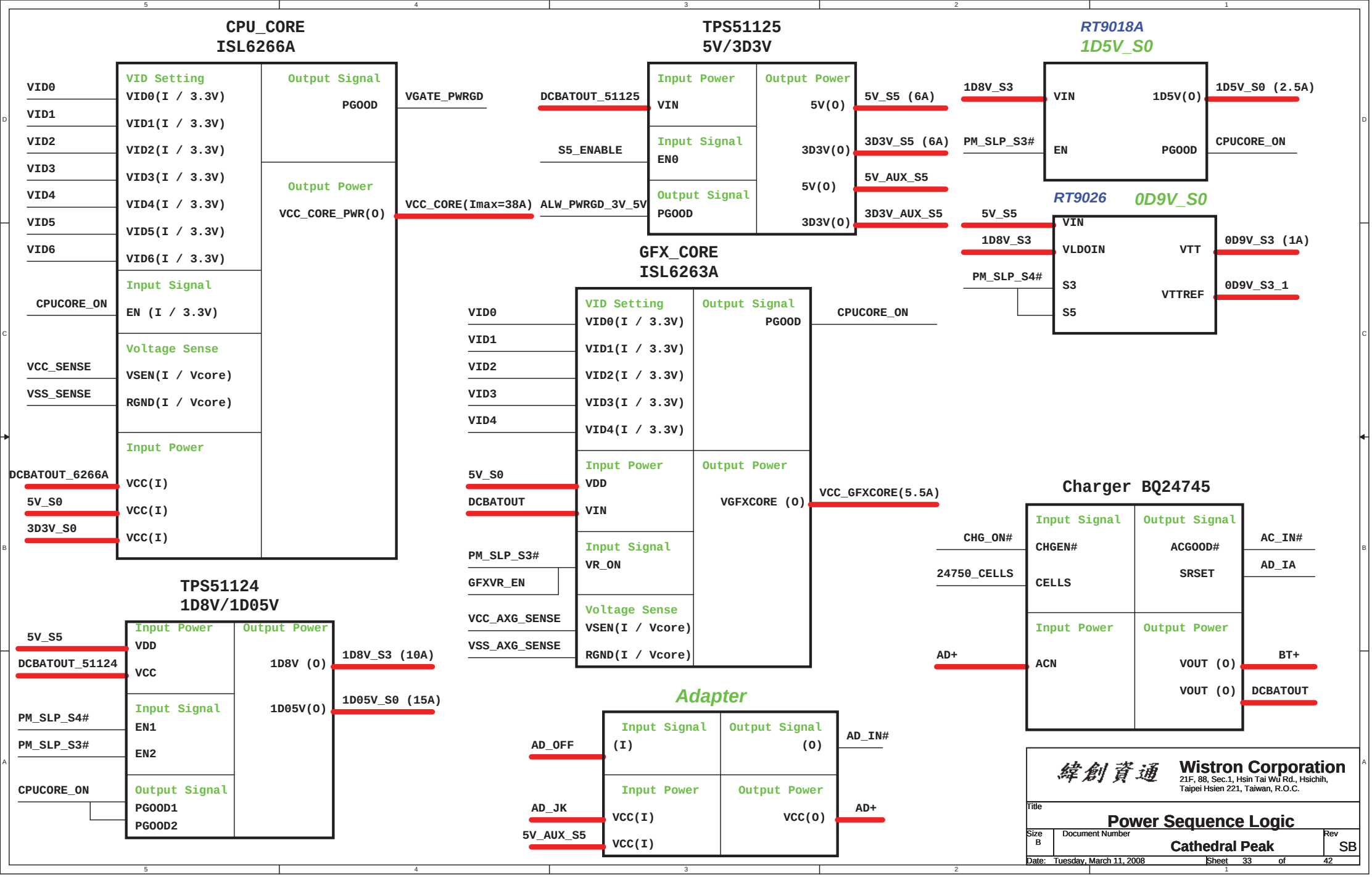


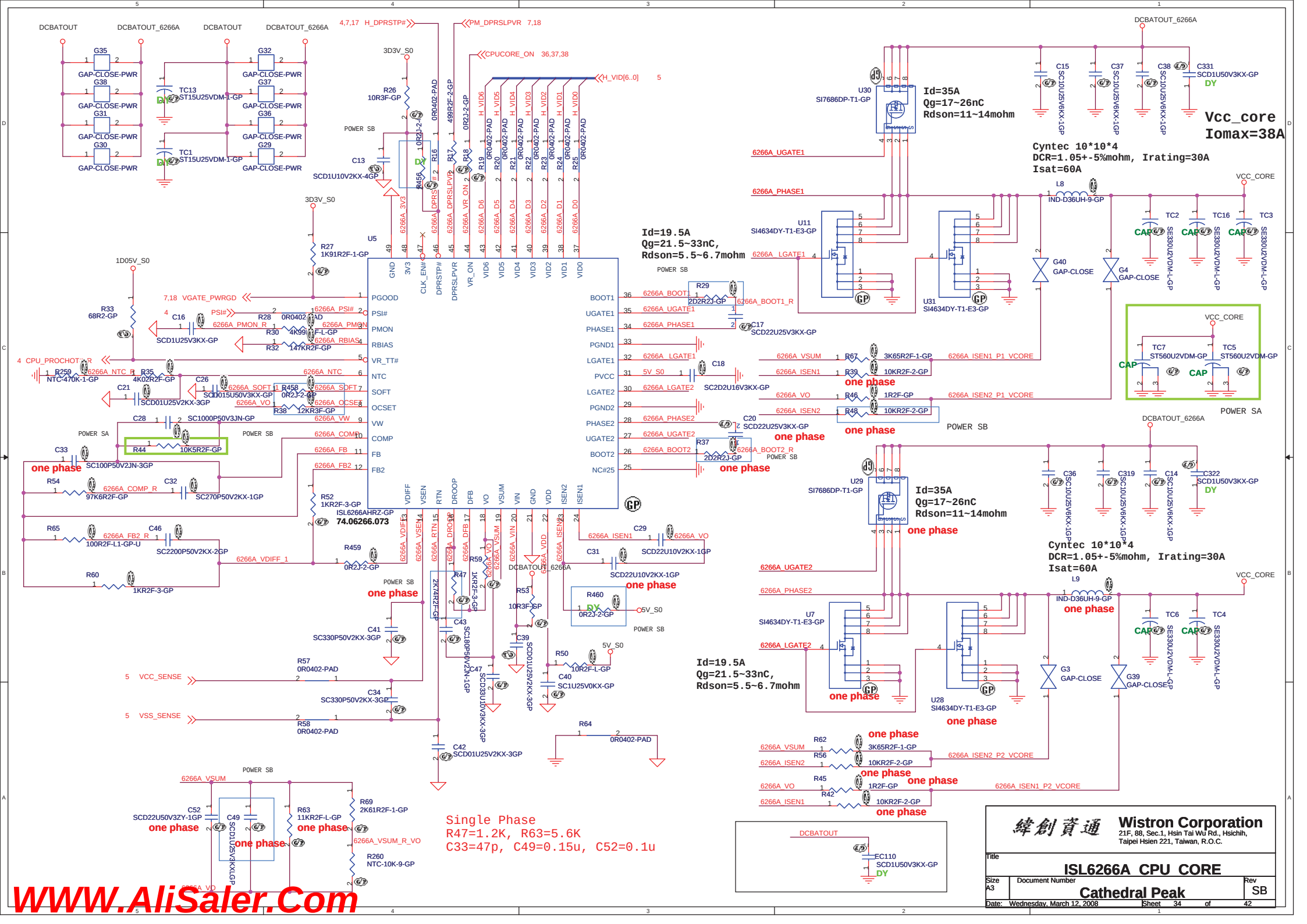
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size | Document Number: Cathedral Peak | Rev: SB

Date: Monday, March 17, 2008 | Sheet 32 of 42


CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
TPS51125
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D5V_S0
VIN
EN
1D5V(O)
PGOOD
1D8V_S3
PM_SLP_S3#
1D5V_S0 (2.5A)
CPUCORE_ON
RT9026
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S4#
0D9V_S3 (1A)
0D9V_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(5.5A)
Charger BQ24745
Input Signal
CHGEN#
CELLS
Input Power
ACN
Output Signal
ACGOOD#
SRSET
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
24750_CELLS
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D8V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D8V_S3 (10A)
1D05V_S0 (15A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
Cathedral Peak
Rev
SB
Date: Tuesday, March 11, 2008
Sheet 33 of 42


ISL6266AHRZ-GP
74.06266.073
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Vcc_core
Iomax=38A
Single Phase
R47=1.2K, R63=5.6K
C33=47p, C49=0.15u, C52=0.1u
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
Cathedral Peak
Wednesday, March 12, 2008
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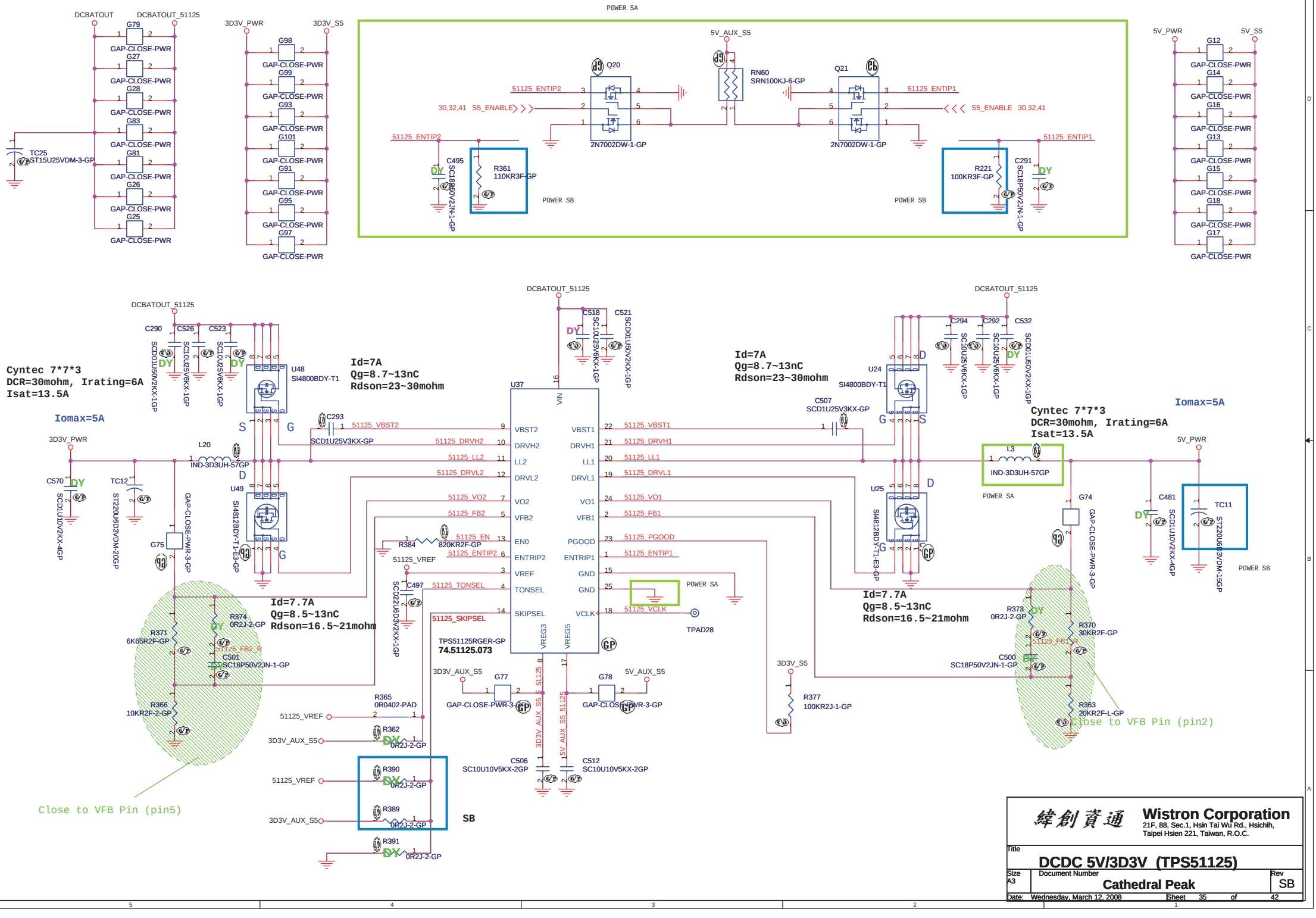

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC 5V/3D3V (TPS51125)**

Size	Document Number	Rev
A3	Cathedral Peak	SB

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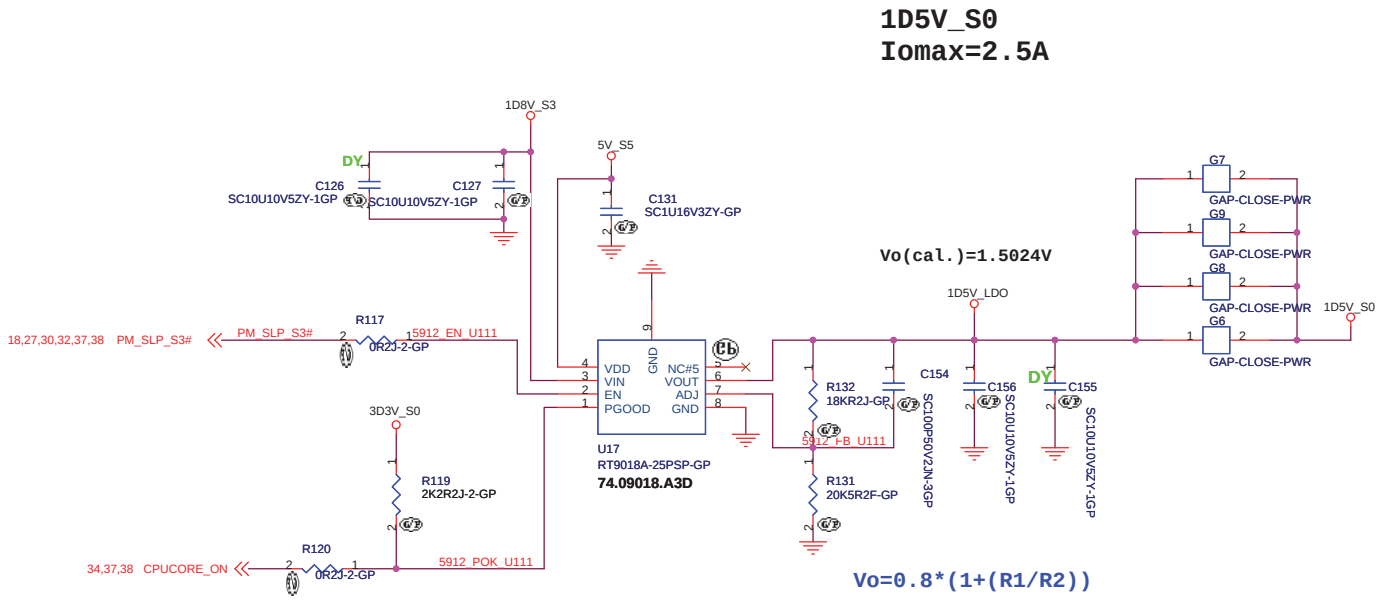
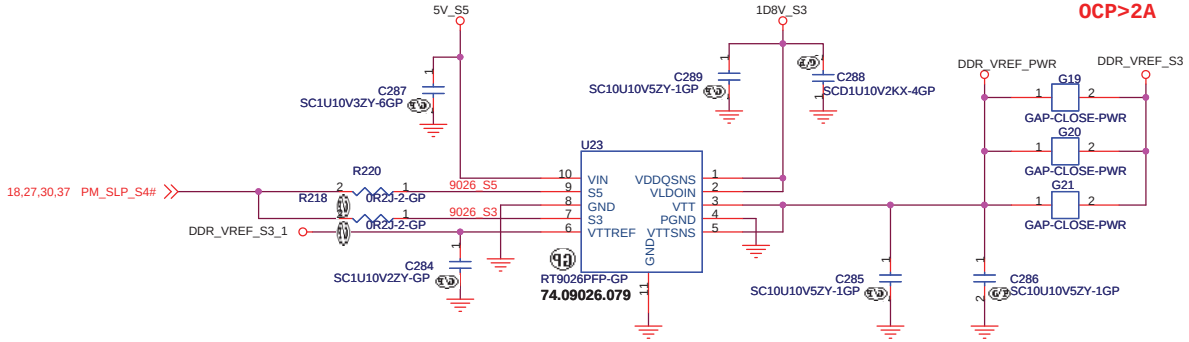
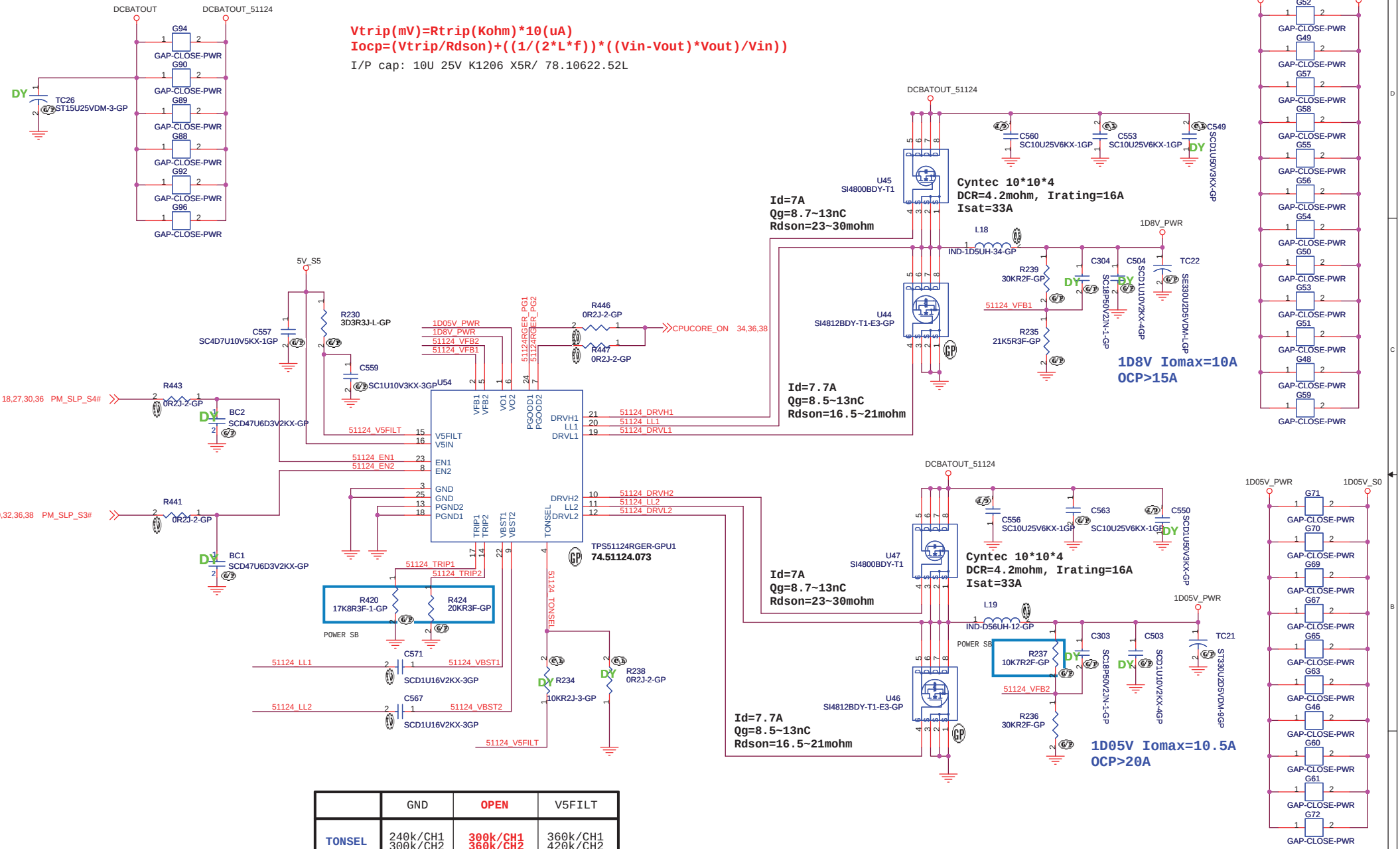




緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V & 0D9V		
Size: A3	Document Number: Cathedral Peak	Rev: SB
Date: Tuesday, March 11, 2008	Sheet 36 of 42	

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size	Document Number	Rev
A3	Cathedral Peak	SB

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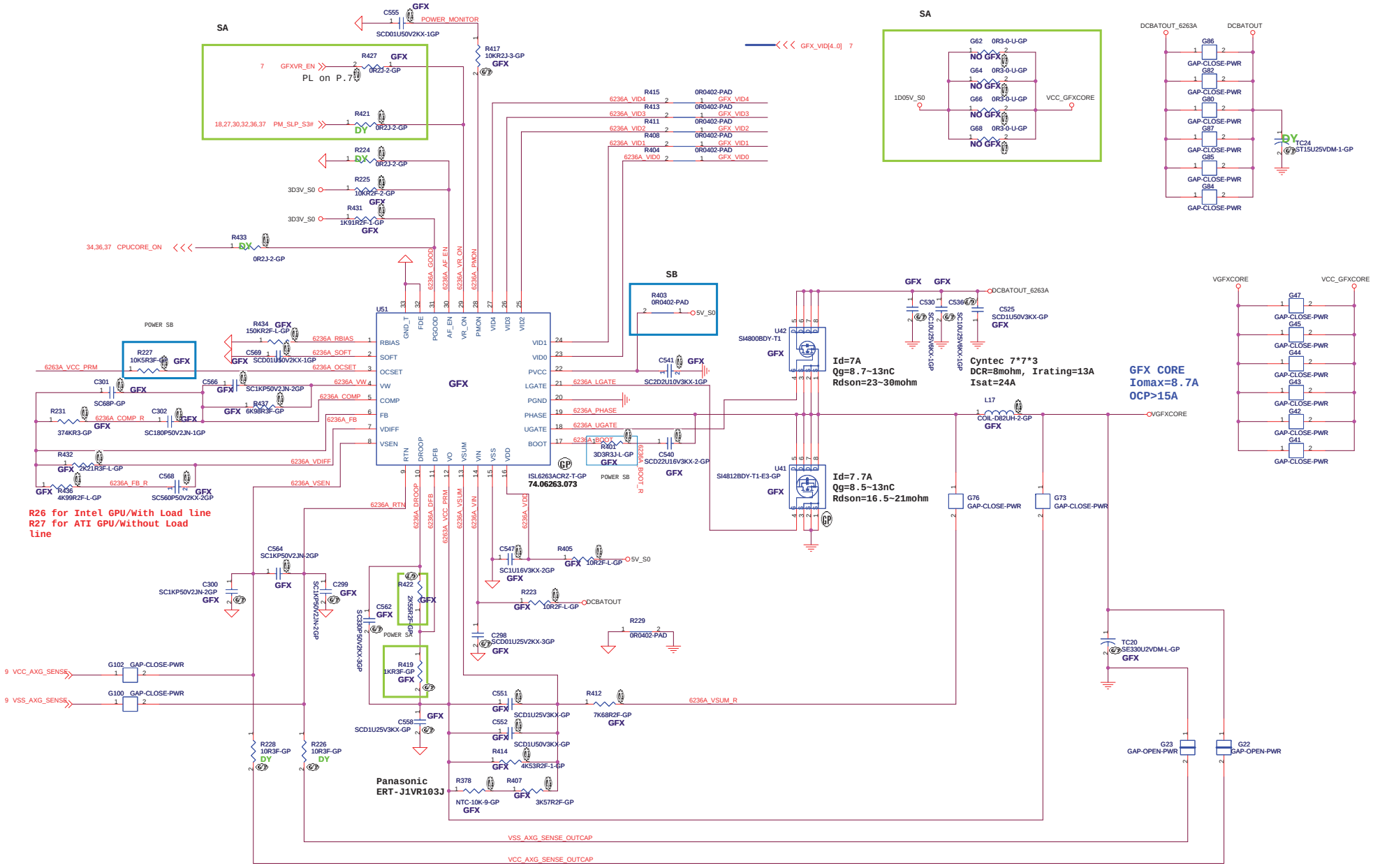

Eiger

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

Size	Document Number	Rev
C	Cathedral Peak	SB

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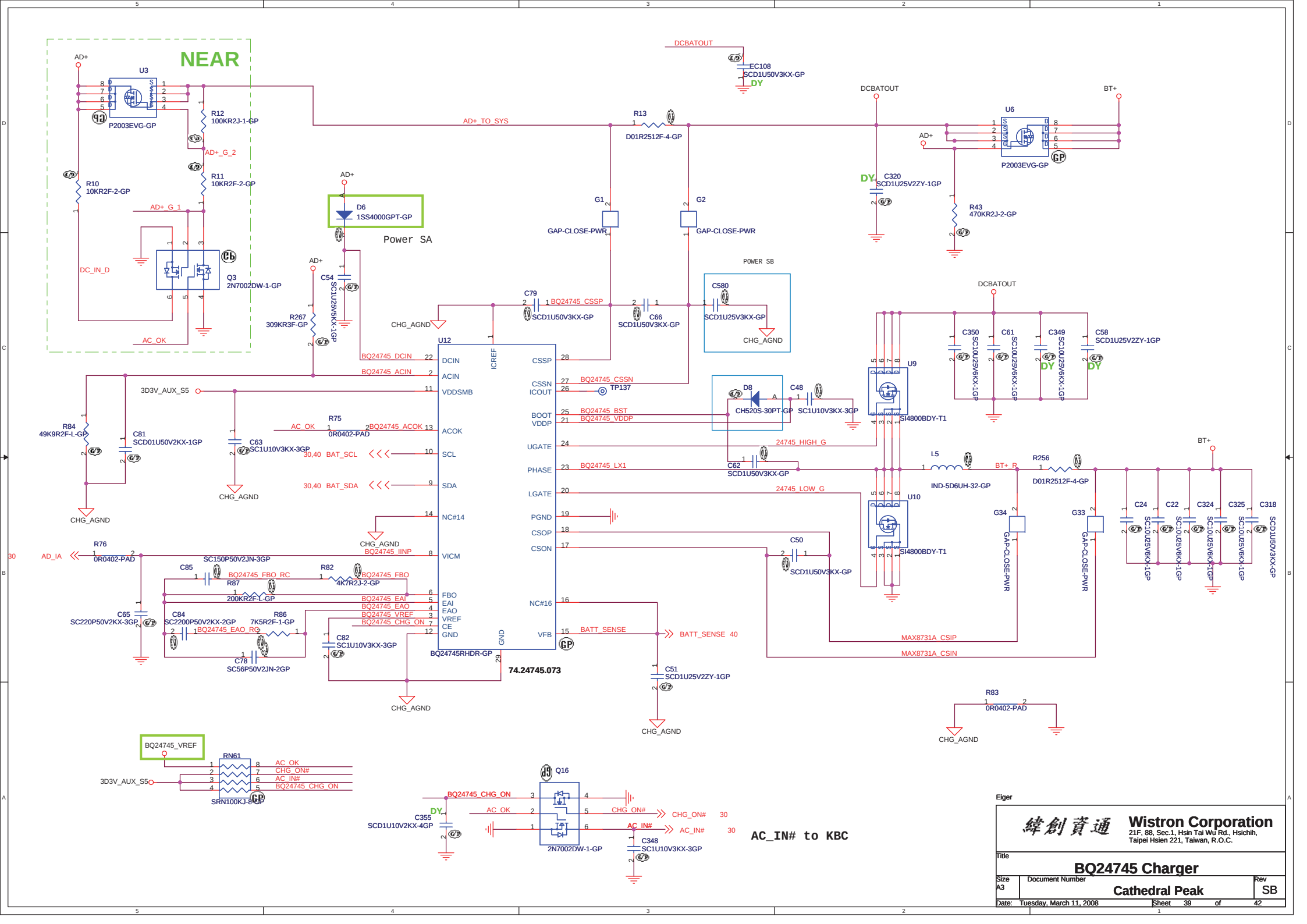

Elger

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

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A3	Cathedral Peak	SB

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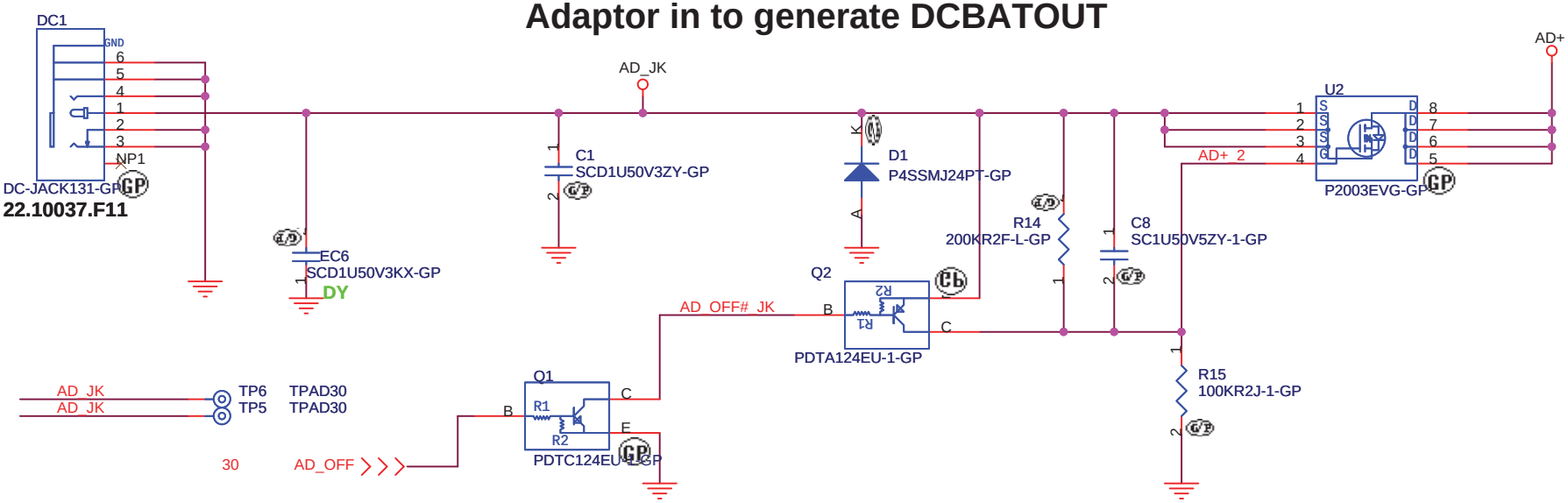
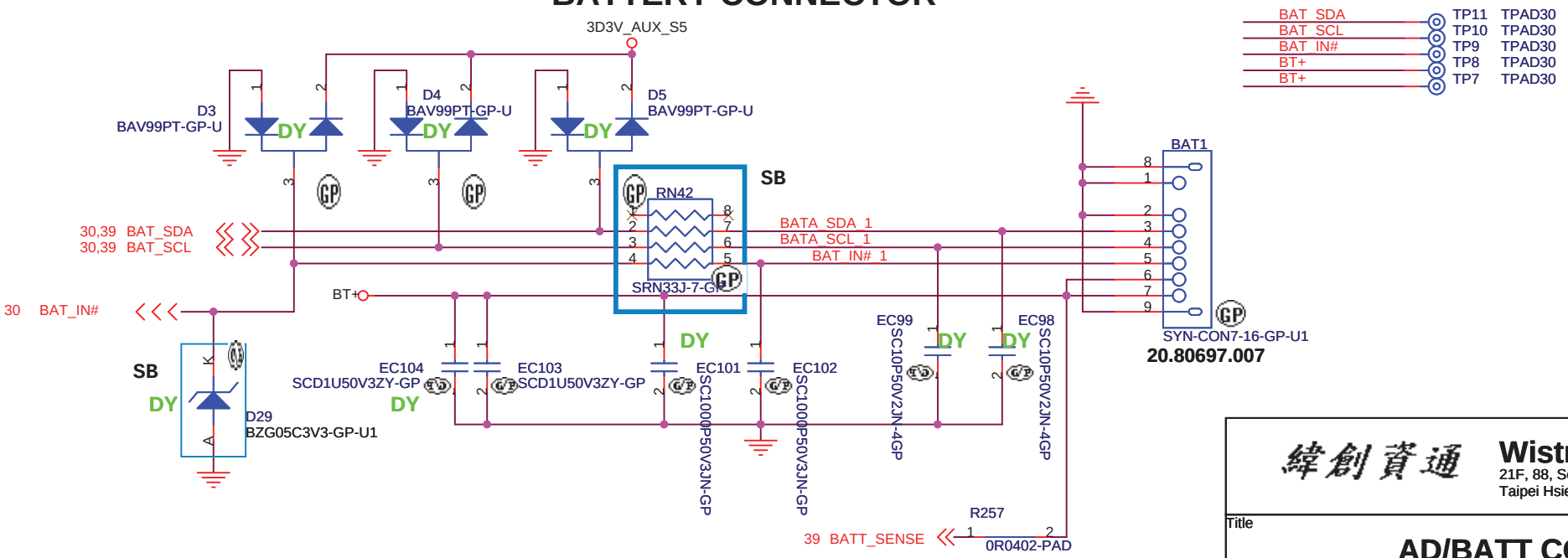
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size	Document Number	Rev
	Cathedral Peak	SB

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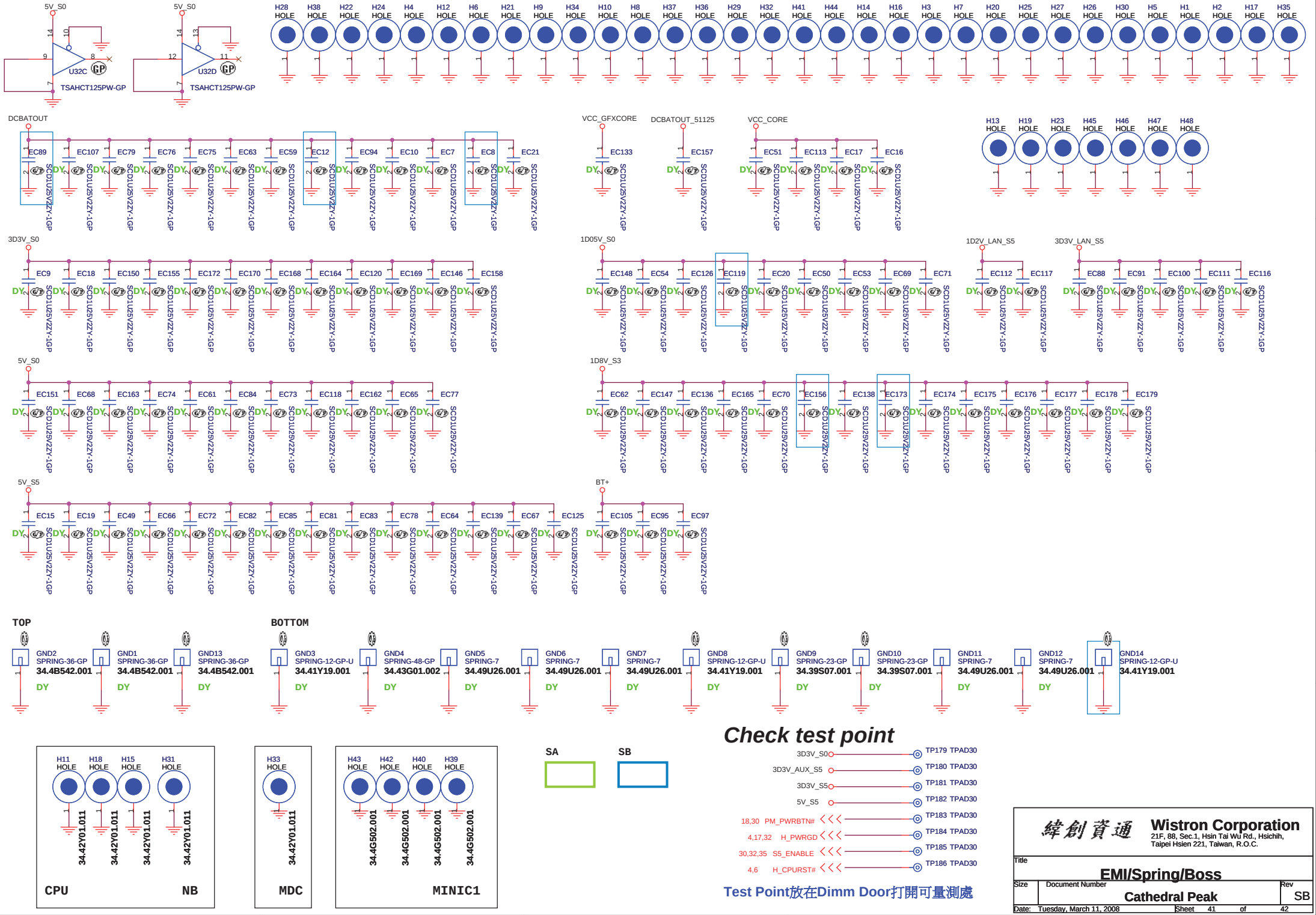
5V_S0
U32C
GP
TSAHCT125PW-GP
5V_S0
U32D
GP
TSAHCT125PW-GP
H28 HOLE
H38 HOLE
H22 HOLE
H24 HOLE
H4 HOLE
H12 HOLE
H6 HOLE
H21 HOLE
H9 HOLE
H34 HOLE
H10 HOLE
H8 HOLE
H37 HOLE
H36 HOLE
H29 HOLE
H32 HOLE
H41 HOLE
H44 HOLE
H14 HOLE
H16 HOLE
H3 HOLE
H7 HOLE
H20 HOLE
H25 HOLE
H27 HOLE
H26 HOLE
H30 HOLE
H5 HOLE
H1 HOLE
H2 HOLE
H17 HOLE
H35 HOLE
DCBATOUT
EC89 EC107 EC79 EC76 EC75 EC63 EC59 EC12 EC94 EC10 EC7 EC8 EC21
VCC_GFXCORE
EC133
DCBATOUT_51125
EC157
VCC_CORE
EC51 EC113 EC17 EC16
H13 HOLE
H19 HOLE
H23 HOLE
H45 HOLE
H46 HOLE
H47 HOLE
H48 HOLE
3D3V_S0
EC9 EC18 EC150 EC155 EC172 EC170 EC168 EC164 EC120 EC169 EC146 EC158
1D05V_S0
EC148 EC54 EC126 EC119 EC20 EC50 EC53 EC69 EC71
1D2V_LAN_S5
EC112 EC117
3D3V_LAN_S5
EC88 EC91 EC100 EC111 EC116
5V_S0
EC151 EC68 EC163 EC74 EC61 EC84 EC73 EC118 EC162 EC65 EC77
1D8V_S3
EC62 EC147 EC136 EC165 EC70 EC156 EC138 EC173 EC174 EC175 EC176 EC177 EC178 EC179
5V_S5
EC15 EC19 EC49 EC66 EC72 EC82 EC85 EC81 EC83 EC78 EC64 EC139 EC67 EC125
BT+
EC105 EC95 EC97
SCD1U25V2ZY-1GP
DY
TOP
GND2 SPRING-36-GP 34.4B542.001
GND1 SPRING-36-GP 34.4B542.001
GND13 SPRING-36-GP 34.4B542.001
BOTTOM
GND3 SPRING-12-GP-U 34.41Y19.001
GND4 SPRING-48-GP 34.43G01.002
GND5 SPRING-7 34.49U26.001
GND6 SPRING-7 34.49U26.001
GND7 SPRING-7 34.49U26.001
GND8 SPRING-12-GP-U 34.41Y19.001
GND9 SPRING-23-GP 34.39S07.001
GND10 SPRING-23-GP 34.39S07.001
GND11 SPRING-7 34.49U26.001
GND12 SPRING-7 34.49U26.001
GND14 SPRING-12-GP-U 34.41Y19.001
H11 HOLE
H18 HOLE
H15 HOLE
H31 HOLE
34.42Y01.011
CPU
NB
H33 HOLE
34.42Y01.011
MDC
H43 HOLE
H42 HOLE
H40 HOLE
H39 HOLE
34.4G502.001
MINIC1
SA
SB
Check test point
3D3V_S0 TP179 TPAD30
3D3V_AUX_S5 TP180 TPAD30
3D3V_S5 TP181 TPAD30
5V_S5 TP182 TPAD30
18,30 PM_PWRBTN# TP183 TPAD30
4,17,32 H_PWRGD TP184 TPAD30
30,32,35 S5_ENABLE TP185 TPAD30
4,6 H_CPURST# TP186 TPAD30
Test Point放在Dimm Door打開可量測處
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
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SB
Date: Tuesday, March 11, 2008
Sheet 41 of 42

SA to SB
1.No Power.
change KBC to BO (71.03310.A0G)
2.XD Card function fail
Cut CARD1 pin27. connect to R400 pin2
3.leakage
GFX power VDD connect to S0
4.Gain=8db.1.83W R137=16K.R138=30K
5.Int_MIC voice to small
add VREF C577=4.7U
6.Realtek Audio report
change R327=68 ohm.R333=68 ohm.merge to RN68
7.SIV reset
R140=300,R55=100.C44=100p,R398=0,R369=100.C502=100p,R85=300,R162=100.C210=100p,R392=0,
8.SIV Azalia
DY C542
BITCLK rise and fall time fail RN10 change to R453=22ohm(MDC).R452=0ohm(codec)
9.add MINICard power option for customer ask
R454.R455
10.interfere HDD
C390.C401.C419. change 0603 4.7U
11.power team
R38=12K.R47=2.74K .R361=110K.R221=100K.R237=10.7K .R424=20K.R420=17.8K .R227=10.5K
R48=10K.R29=2.2 .R37=2.2 .R401=3.3 .C49=0.1u.add R456.add C580.D8=83.R0203.08F .
TC11 change to 77.C2271.00L
TC9 change to 77.E9071.001 (power ripple)
add R458=1K.R459=1k.R460
12.Oscillation
C30=15p.C23=15P.C537=27p.C538=22p
13.audio S3.S4 resume bobo sound
R143 DY. R187 0ohm pad
14.AC mode have hight frequency noise
R390 DY.R389 0ohm pad
15.ESD issue
BAT_IN# series 33 ohm
RN42 change to 8p4r
add R457.D27.D28.D29.U55.U56.C578.R457.
16.noise
DY C523.TC25 change to 77.C1561.01L
20.LED brightness
R2.R1.R4.R5.R451.R450.R449.R448=56

EMI
1.EC23 ~~EC48.EC134.EC135.EC167.EC121.EC122.EC123.
2.EC89.EC12.EC8.EC119.EC156.EC173.
3.EC174~~~EC179.
4.GND13.GND14.

Merge
1.R313.R314.R315.R319.R320.R149. change to RN59
2.RN6.RN46. change to RN6
3.R341.R343.R344 change to RN46
4.R385 change to 100K merge R382 to RN56
5.RN53.RN56. change to RN53
6.Q20.Q21 change to Q21. Q21.Q23 change to Q21.
7.R367.R368 change to RN60
8.Q16.Q17 change to Q16
9.R262.R264.R268.R277 change to RN61
10.R205.R204.R206 change to RN62
11.RN33.R215 change to RN33
12.R209.R210.R348 change to RN63
13.R280=10K.merge R269 to RN64
14.R109.R112.R111.R290 change to RN65
15.R325.R323 change to RN66
16.R304.R307 change to RN67
17.U14 change to 73.01G08.L04 .add C579
18.R51.R399 vhange to RN69.

0 Ohm change to PAD
R427.R403.R415.R413.R411.R408.R404.R146.R197.R157.R153.R353.R352.R358.R357.R310.R196.R346.R342.R351.
R191.R203.L14.R212.R350.R179.R217.R6.R7.R242.R294.R278.R279.R292.R293.R232.R233.R410.R393.
R416.R250.R251.R248.R249.R246.R247.R244.R245.R129.R127.R376.ER2.R383.R28.R16.R19.R20.R21.
R22.R23.R24.R25.R57.R58.R365.R164.

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Change List	
Size	Document Number: Cathedral Peak	Rev: SB
Date: Wednesday, March 12, 2008	Sheet 42 of 42	