

VER : 3A
PWA: W028J
PWA: D178M
PWB: W026J

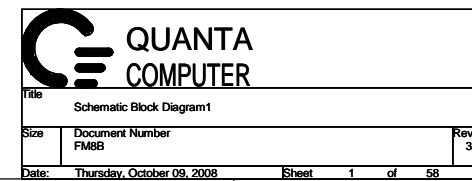



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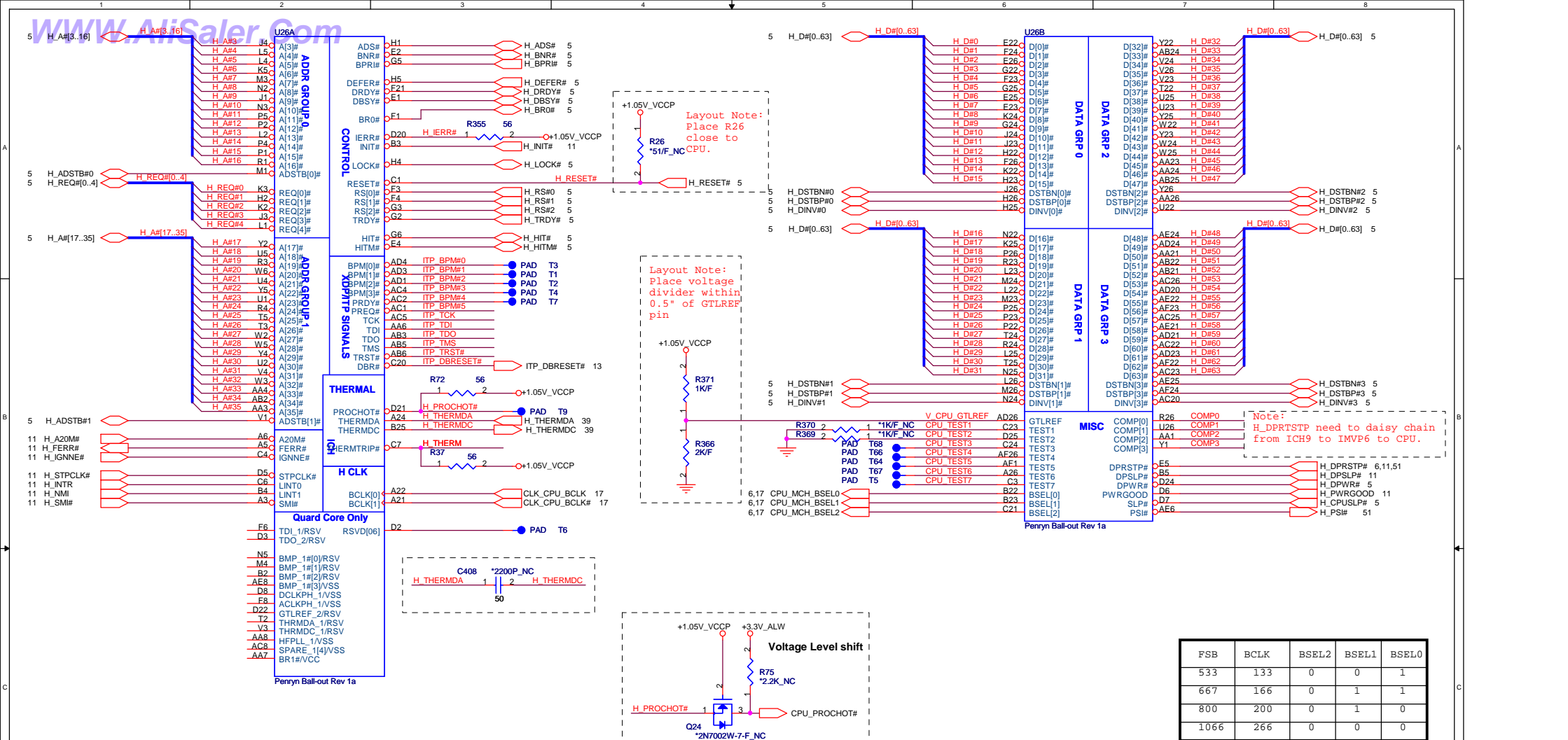
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Merom
5-10	Crestline
11-14	ICH9
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18	HDMI
26	LCD Conn. & SSP
27	CRT Conn
36	SATA Conn
28-30	CARD READER/Conn & 1394
30	Express Card & Card reader
33	Mini Card
31	SIO (ITE8512)
32	FLASH/RTC
35	USB
37	TP / KEYBOARD
38	SWITCH /LED
39	FAN & Thermal
40-41	Audio CODEC(ALC888)/Phone Jack
42-43	LOM / Switch
44	System Reset Circuit
46	Battery Selector & Charger
48	1.05VCCP / 1.5VRUN
49	DDR2_1.8VSUS, 0.9V
51	CPU_ISL6262(2phase)
52	MAX8744 (+5.5V,+3.3V)
53	RUN Power Switch
54	DCIN,Batt
55	PAD& SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Diagram

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,51,52	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	38,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,36,38,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,26,30,37,38,43,48,49,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,53	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,18,27,36,37,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,13,14,15,16,17,18,26,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	35,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,40,48,53	CALISTOGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+PBATT	+10V~+17V		MAIN BATTERY	CHG_PBATT	
+SBATT	+10V~+17V		SECOND BATTERY	CHG_SBATT	

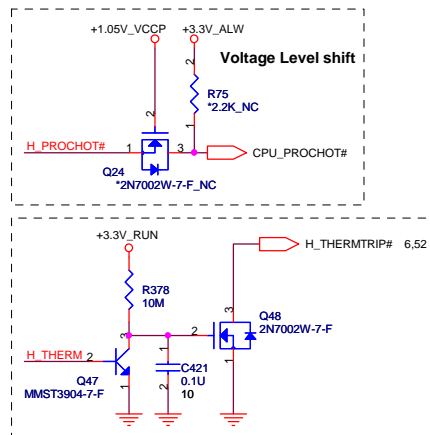
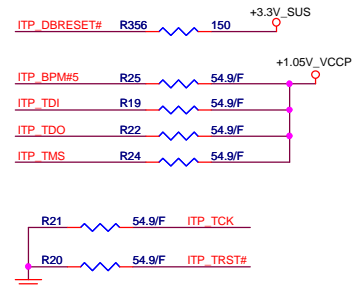
GND PLANE	PAGE	DESCRIPTION
8731AGND	46	
AGND_0.9V	49	
AGND_DC/DC	52	
AGND_DC2	48	
AGND_DDR	49	
AGND_ISL6260	51	
GND	ALL	

 QUANTA COMPUTER		
Title Index & Power Status		
Size	Document Number FM8B	Rev 3A
Date: Thursday, October 09, 2008	Sheet 2	of 58

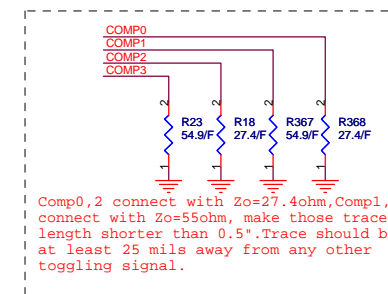
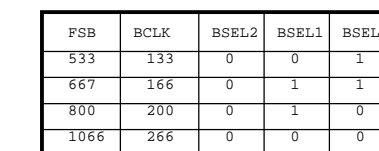


Populate ITP700Flex for bringup

Layout Note:
Place couple 0.1uF Decoupling
caps with in 0.1" ITP connector.



ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8



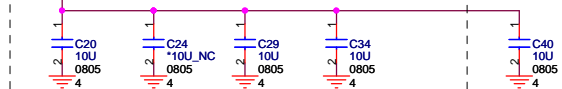
Title Merom Processor (HOST BUS)

Size	Document Number	Rev
	EMR	3A

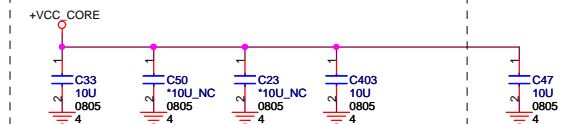
Date: Thursday, October 09, 2008

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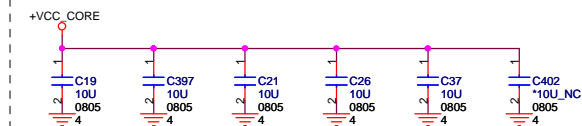
+VCC_CORE All use 10U 4V(+20%,X6S,0805)Pb-Free.



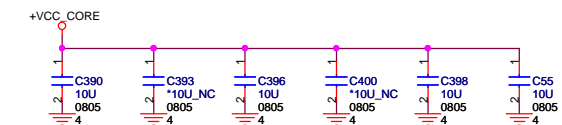
8 inside cavity, north side, secondary layer.



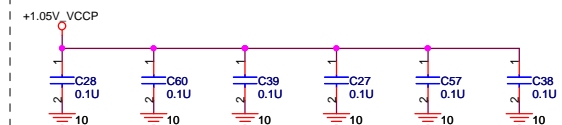
8 inside cavity, south side, secondary layer.



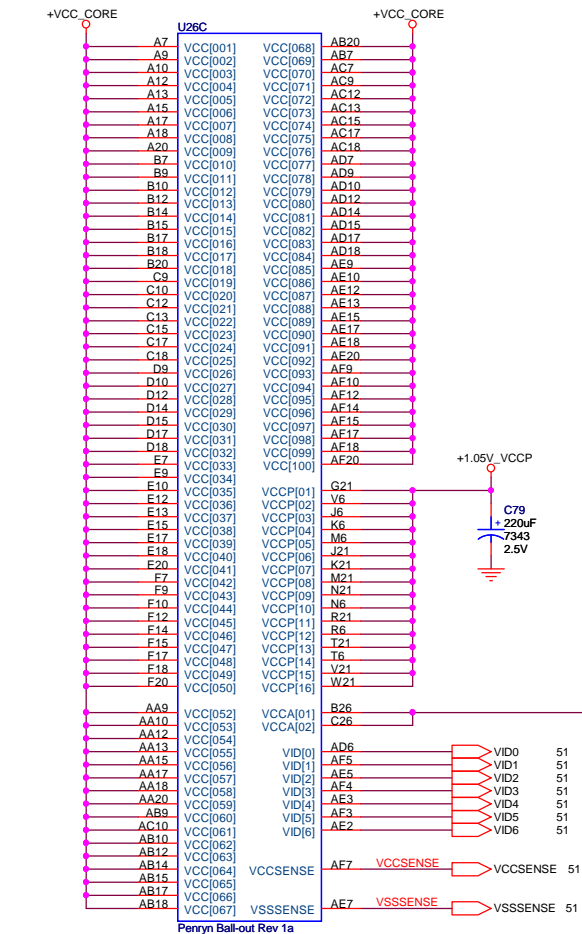
6 inside cavity, north side, primary layer.



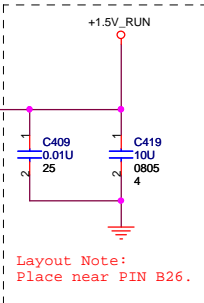
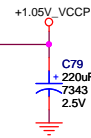
6 inside cavity, south side, primary layer.



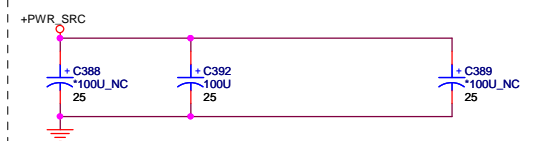
Layout out:
Place these inside socket cavity on North side secondary.



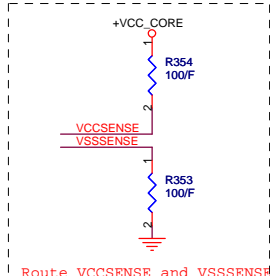
Penryn Ball-out Rev 1a



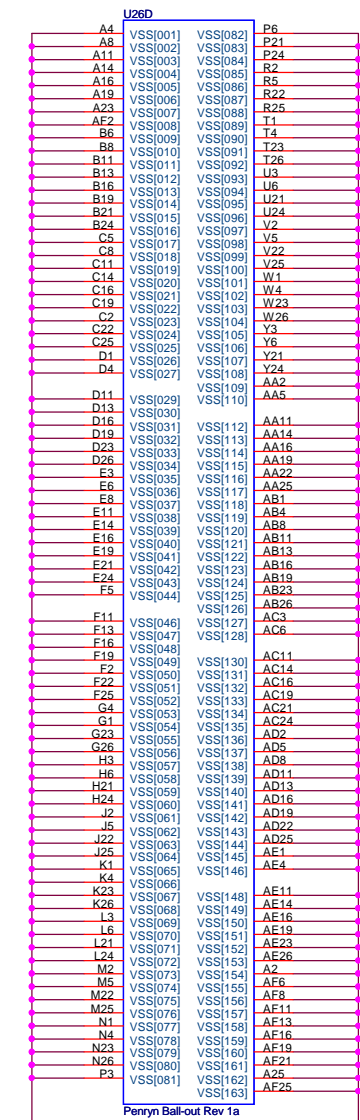
Layout Note:
Place near PIN B26.



Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.



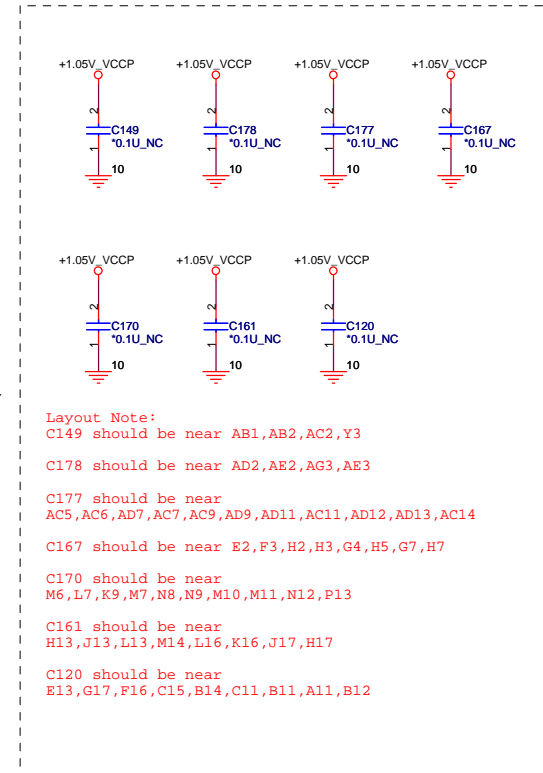
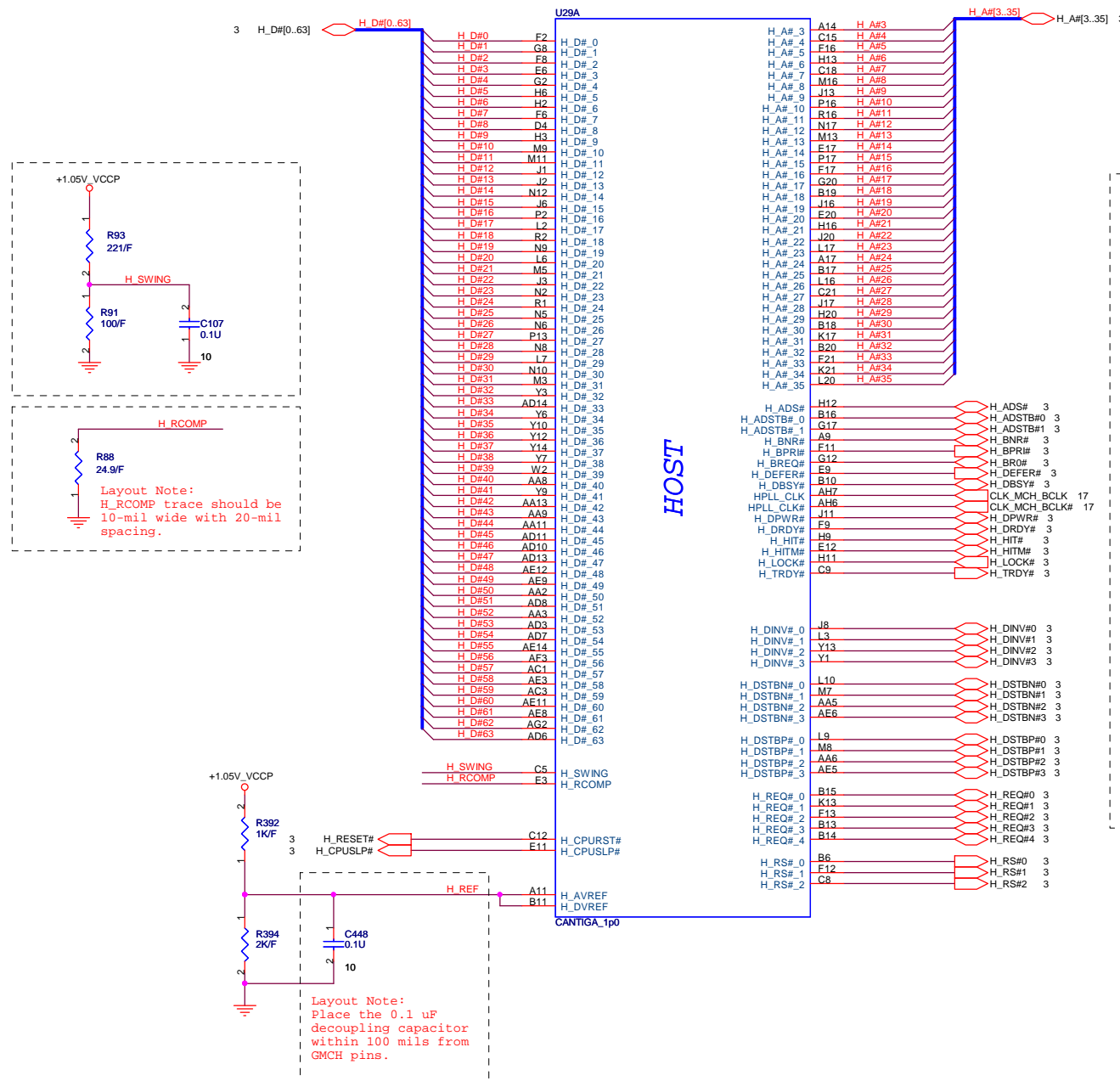
Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

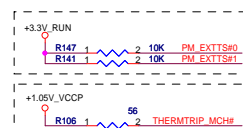
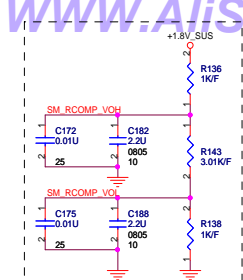


Penryn Ball-out Rev 1a

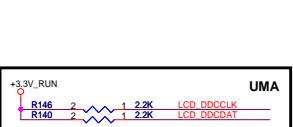
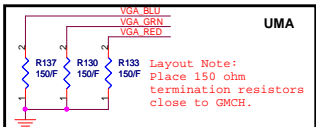
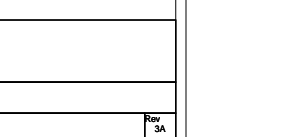
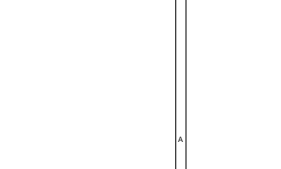
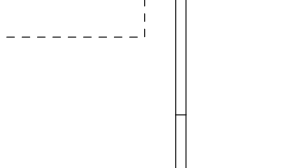
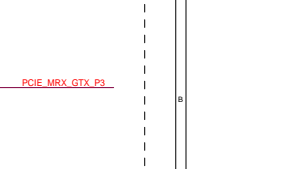
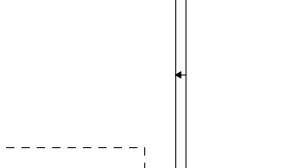
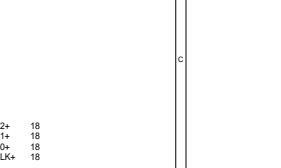
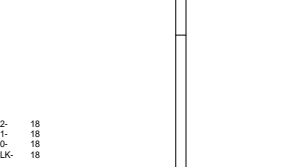
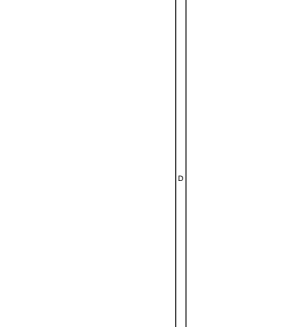
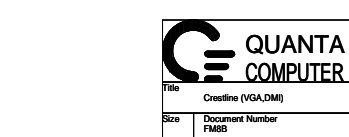
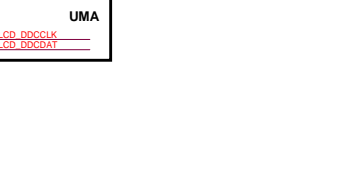
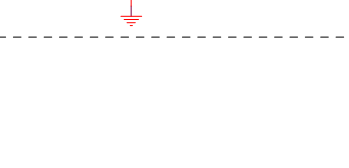
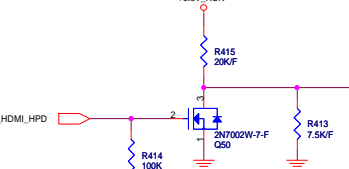
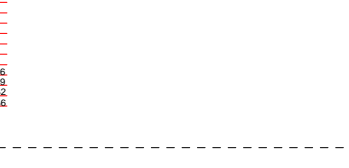
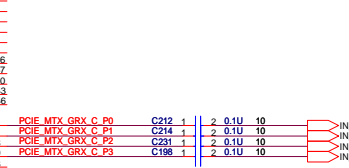
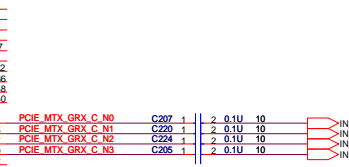
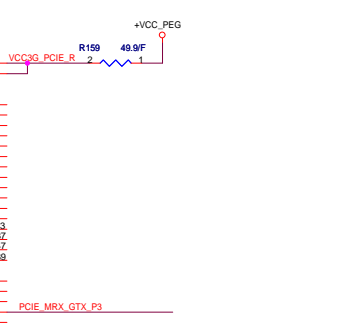
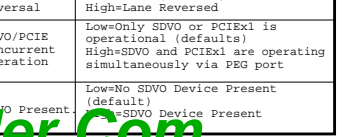
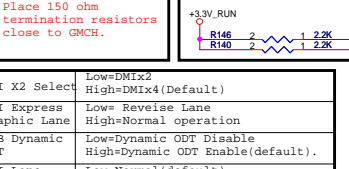
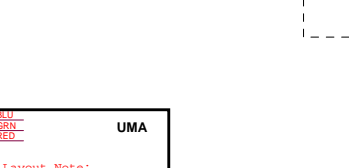
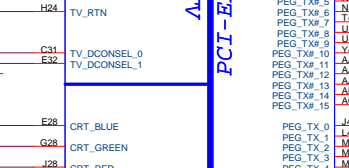
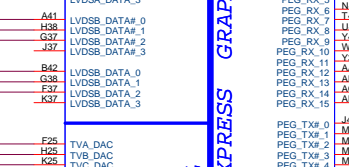
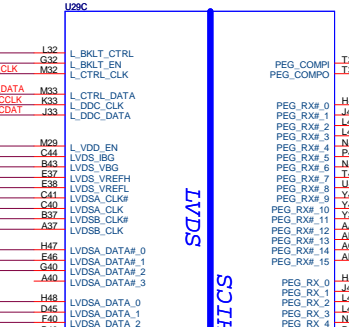
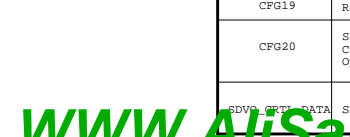
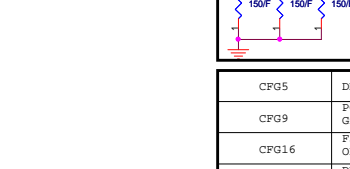
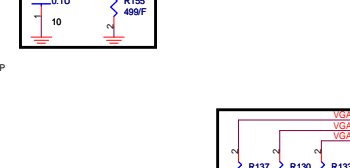
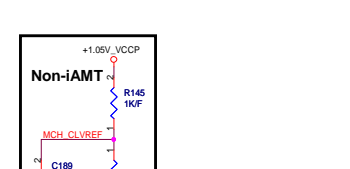
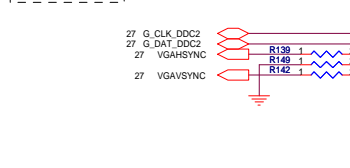
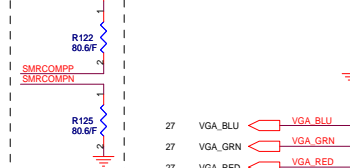
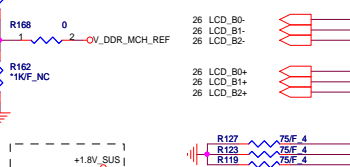
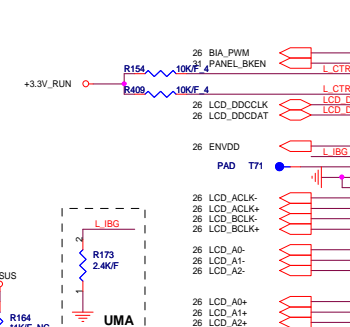
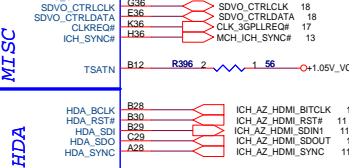
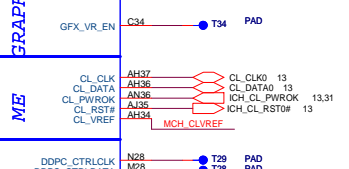
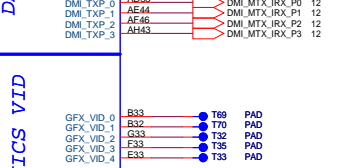
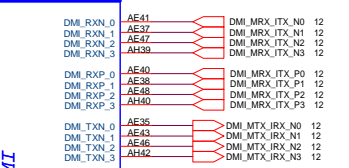
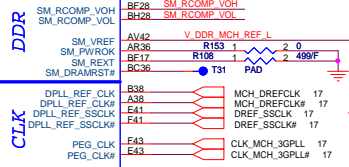
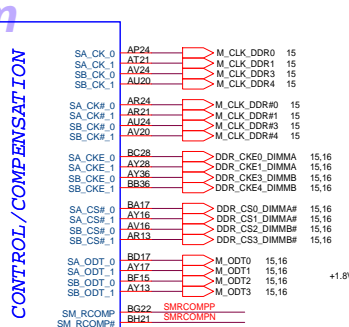
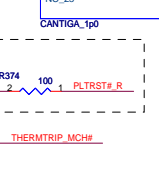
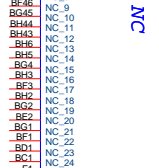
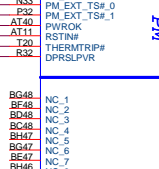
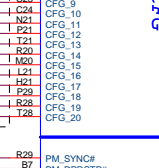
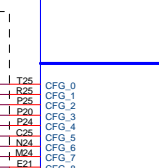
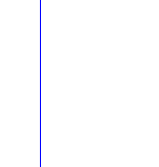
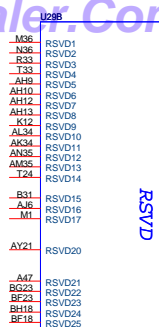
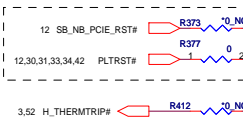
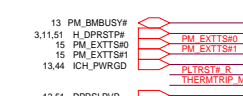
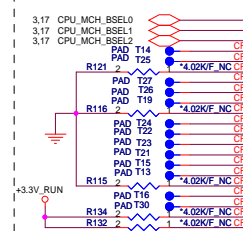


Title			Merom Processor (POWER)
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	FM8B	3A	
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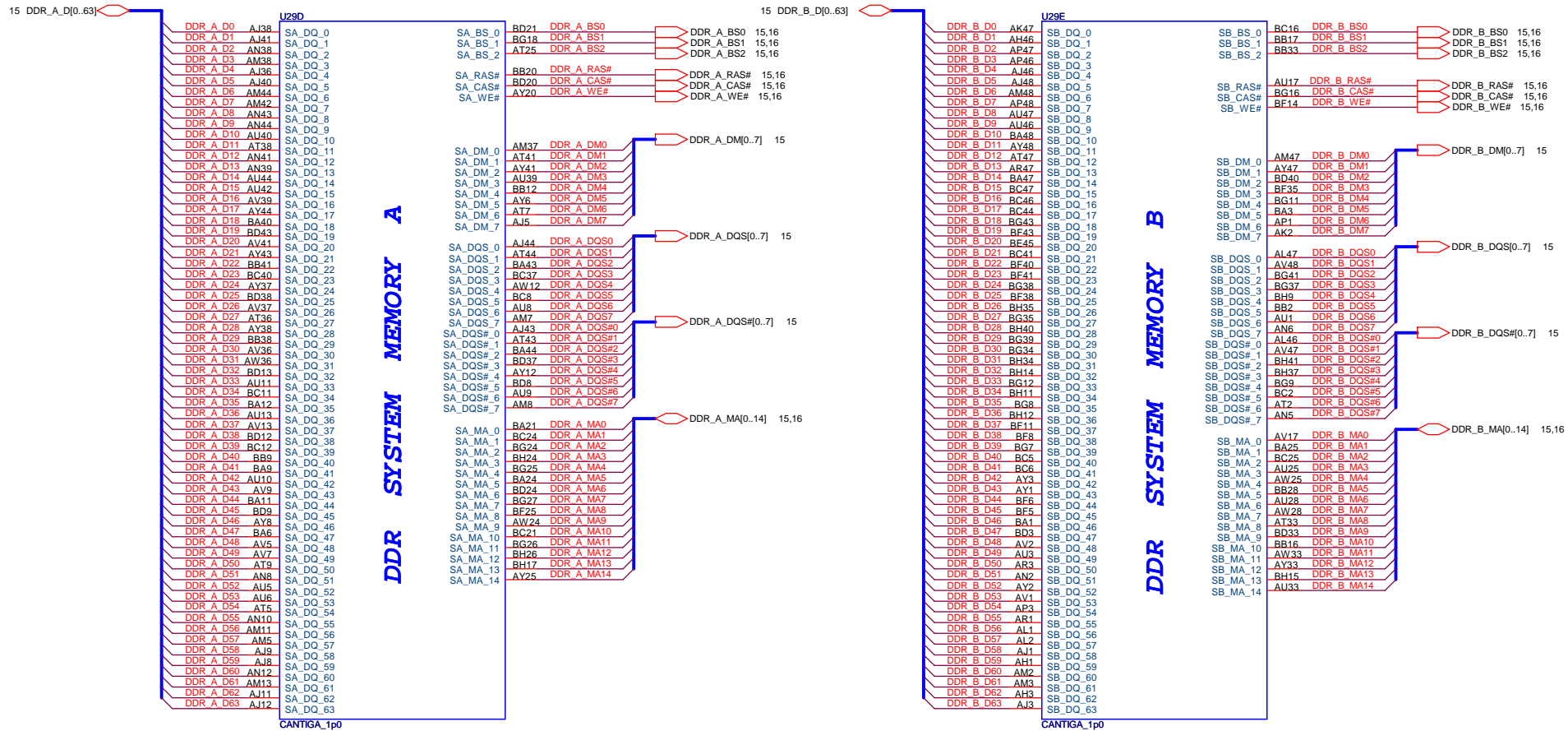
Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minimize stub.

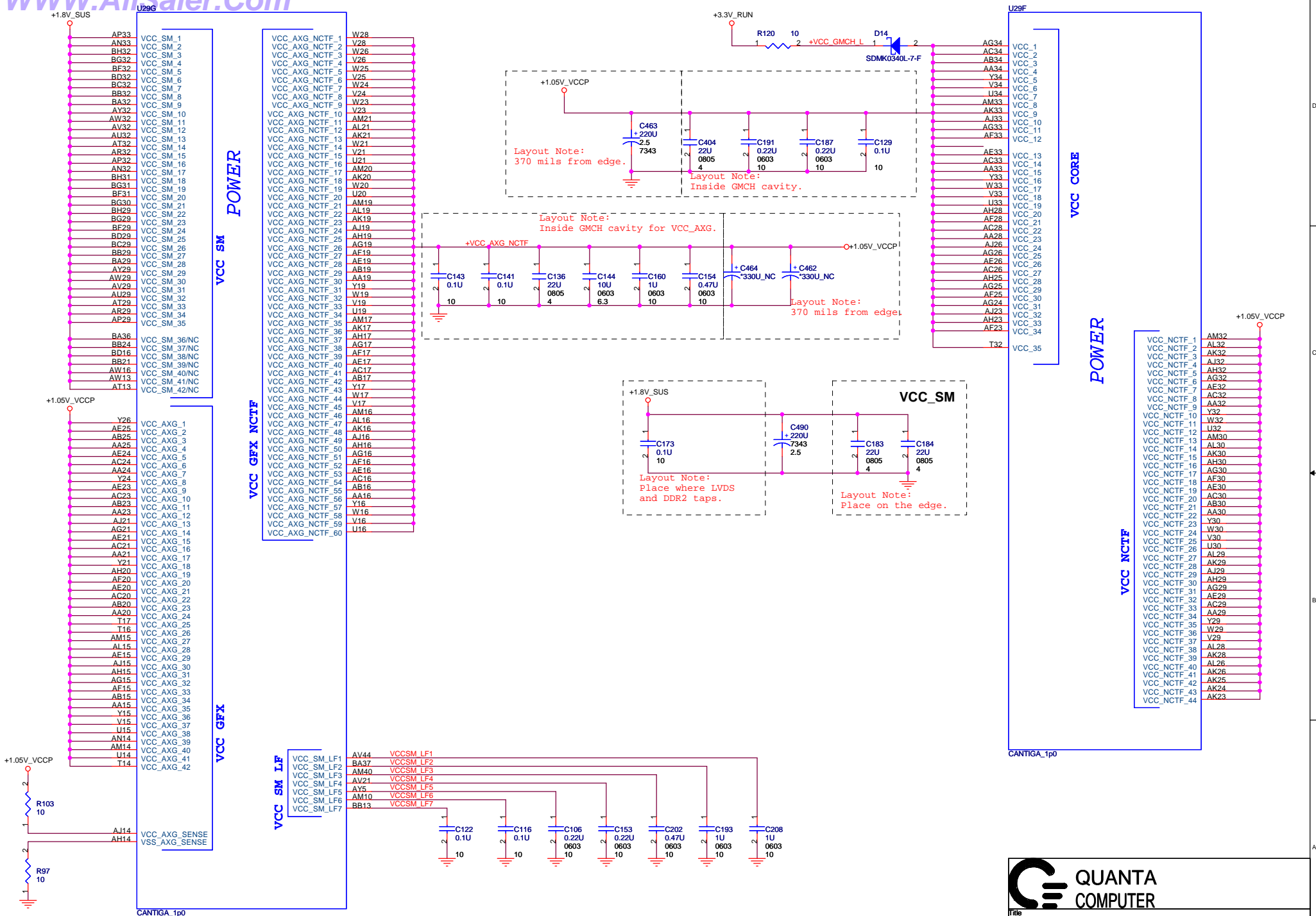


CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIE is operational (defaults) High=SDVO and PCIE are operating simultaneously via PEG port
	SDVO/PCIE Data Present	Low=No SDVO Device Present (default) High=SDVO Device Present

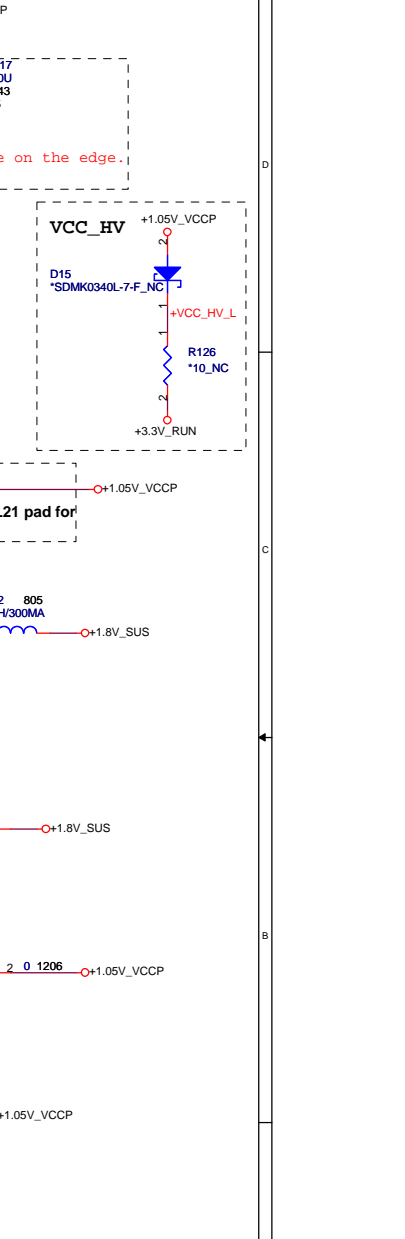
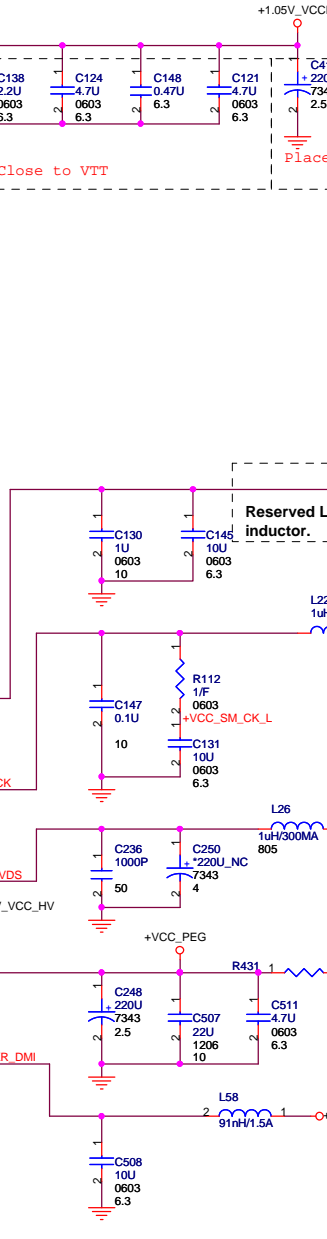
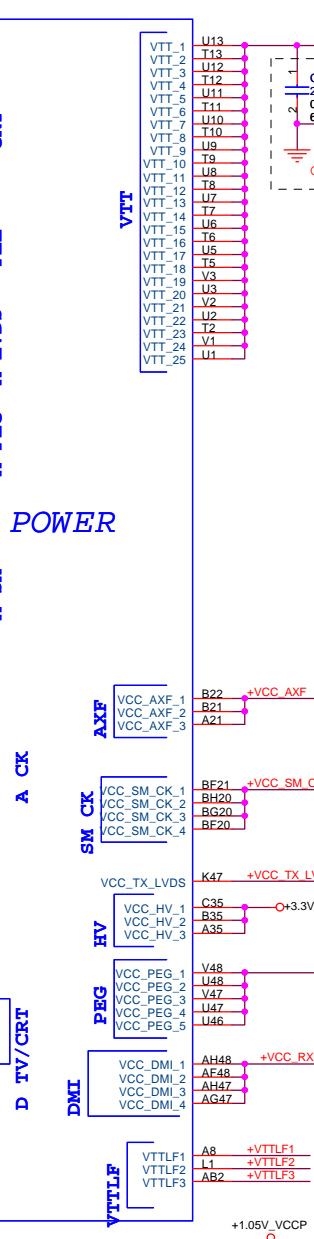
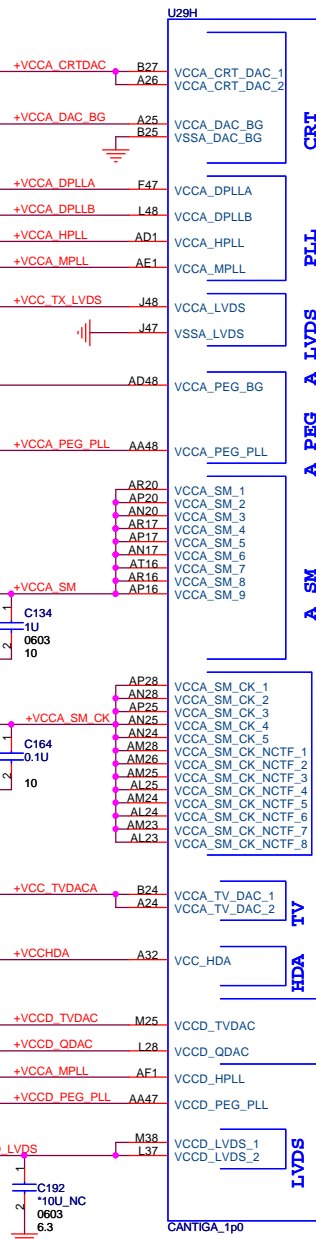
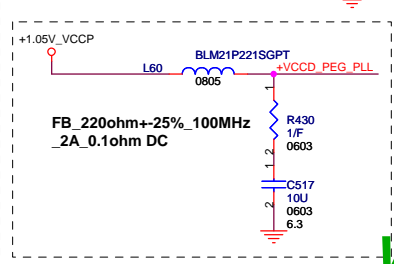
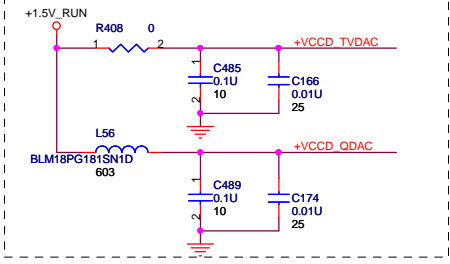
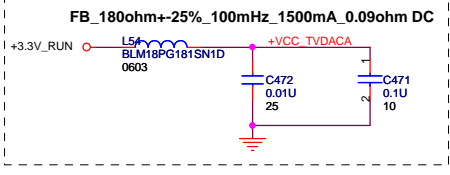
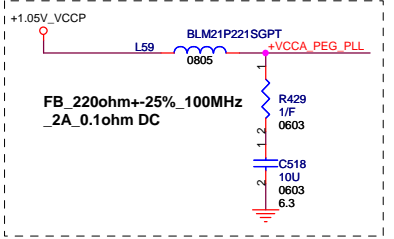
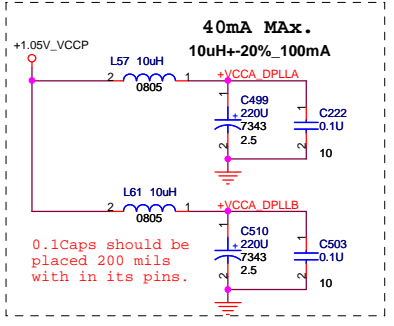
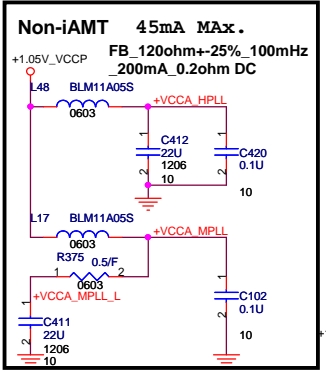
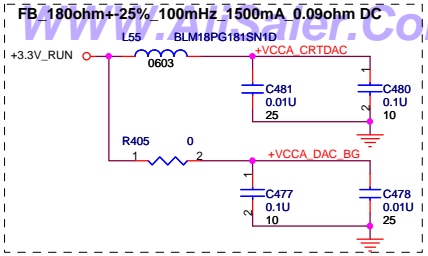


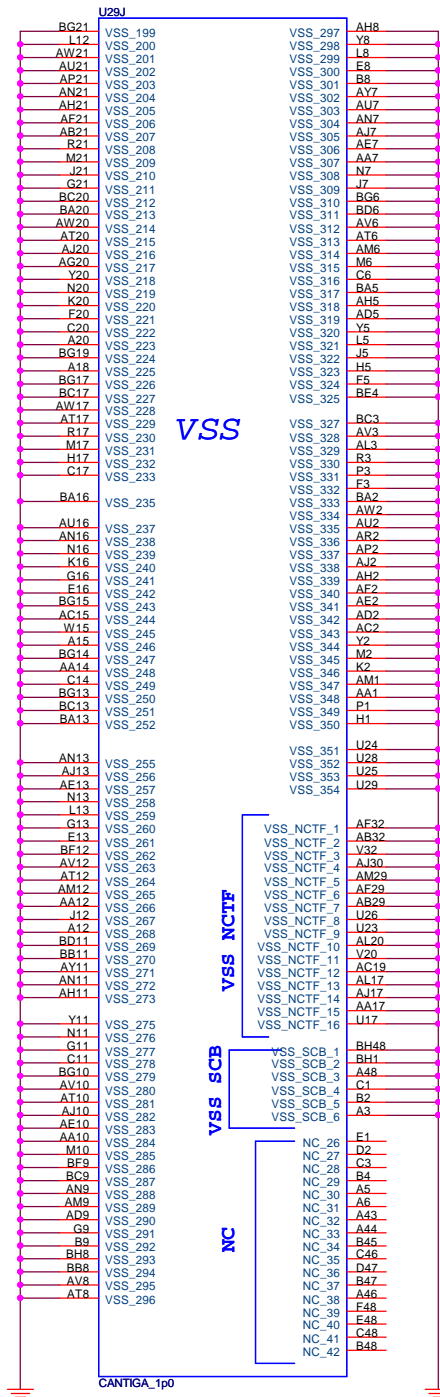
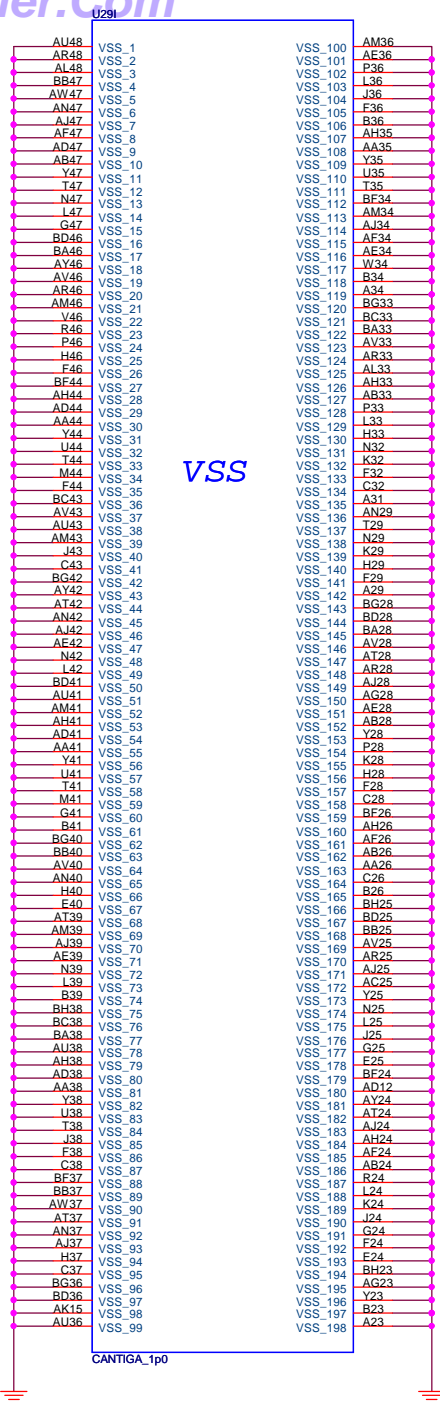
File	Crestline (VGA,DMI)	Rev	3A
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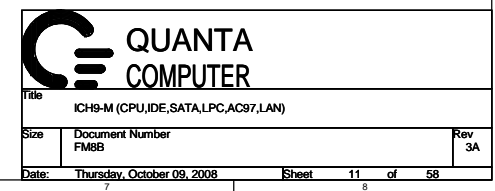


DIS: Please R103, R97 to 0 ohm.

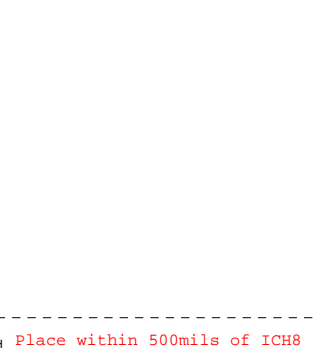
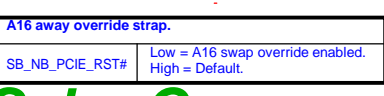
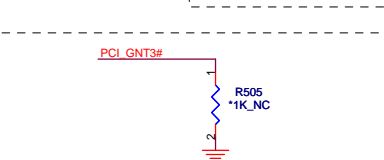
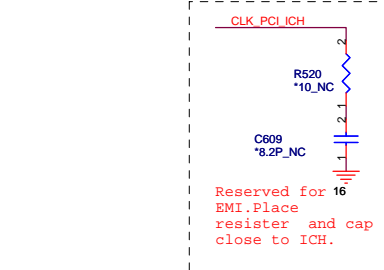
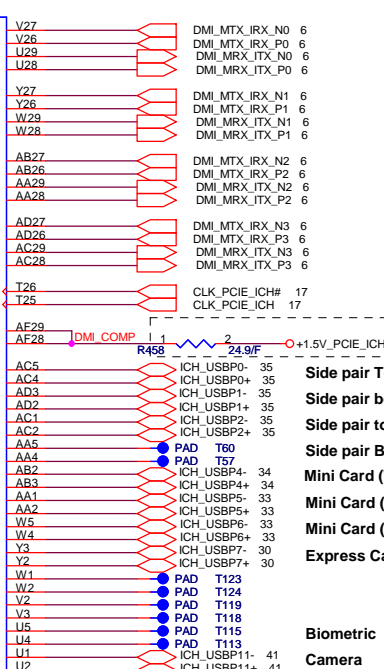
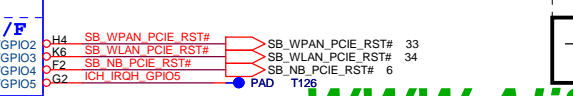
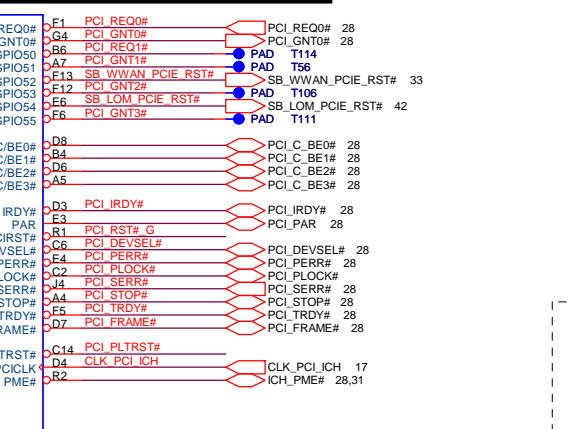
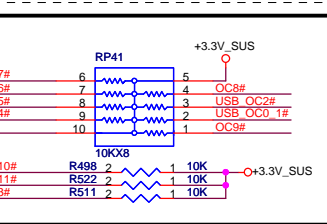
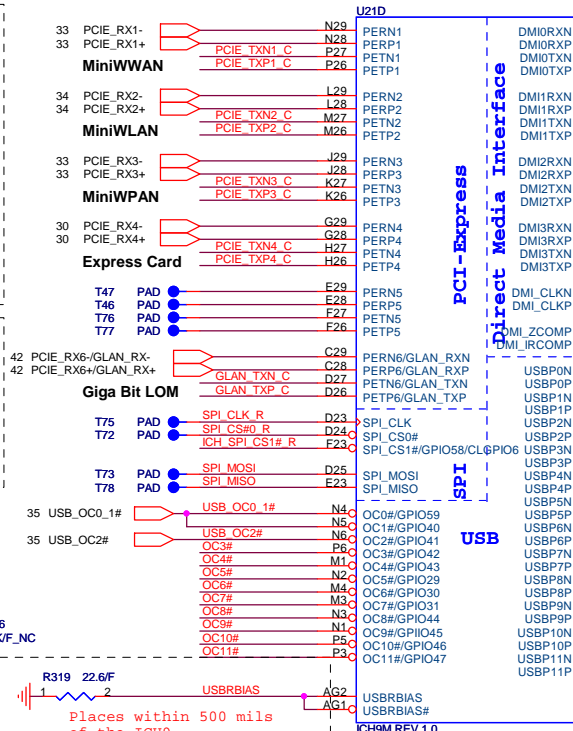
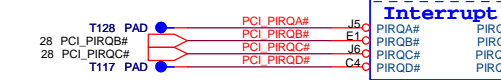
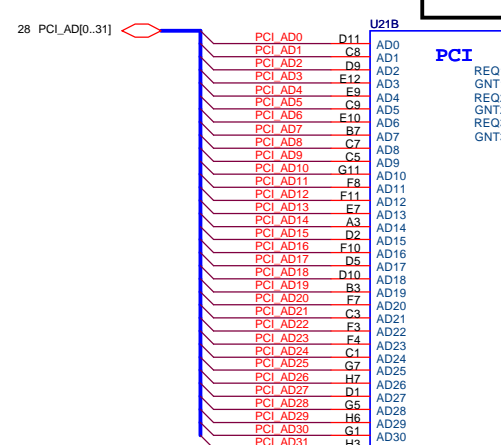
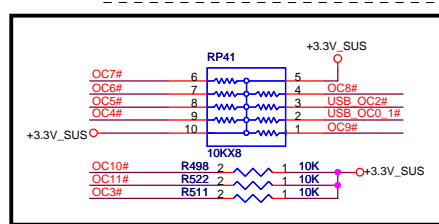
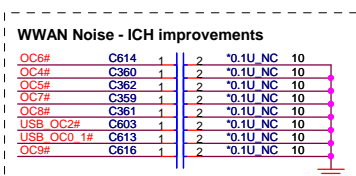
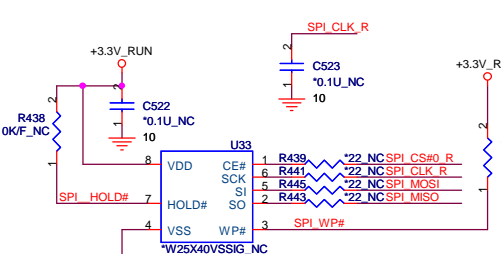
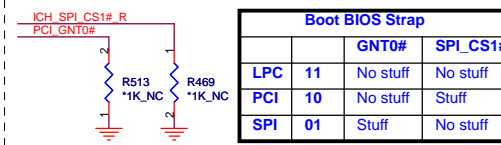
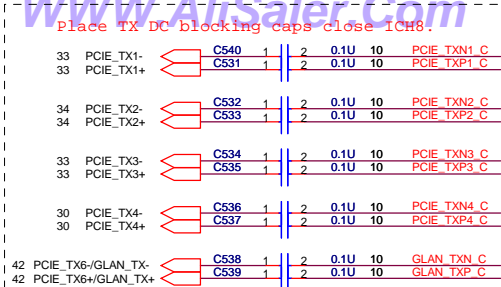


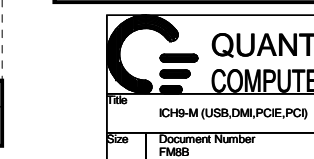
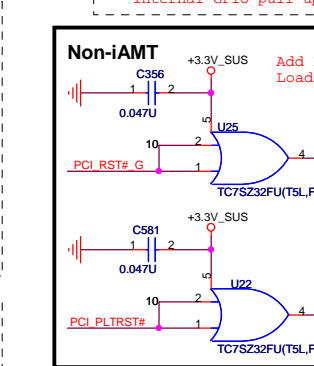
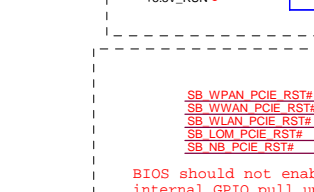
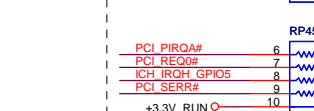
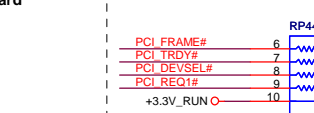
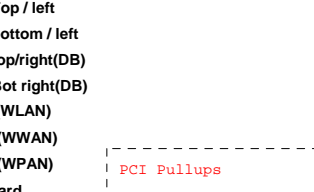


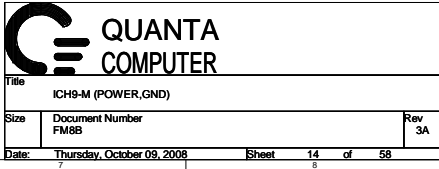
 QUANTA COMPUTER		
Title Crestline (VSS)		
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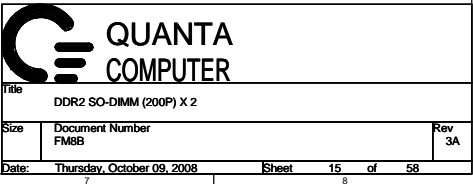


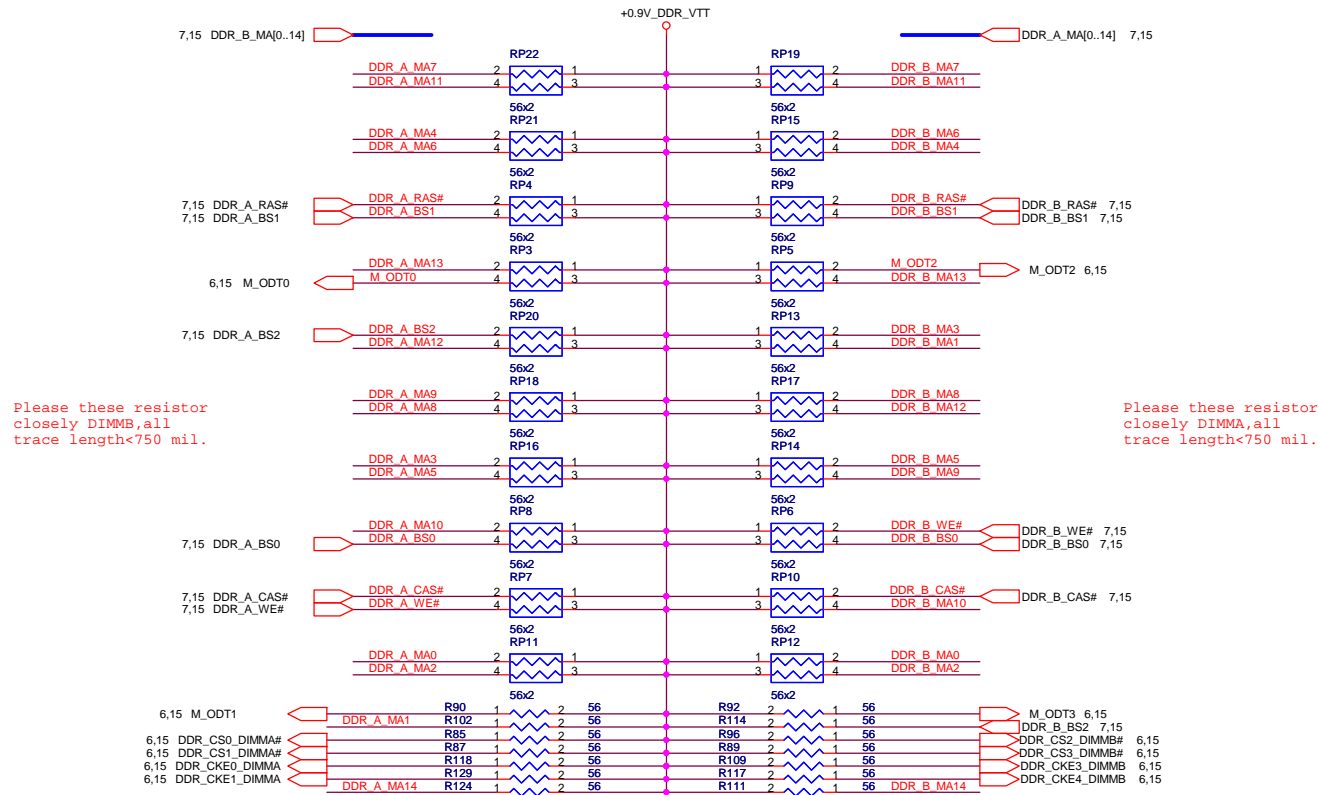
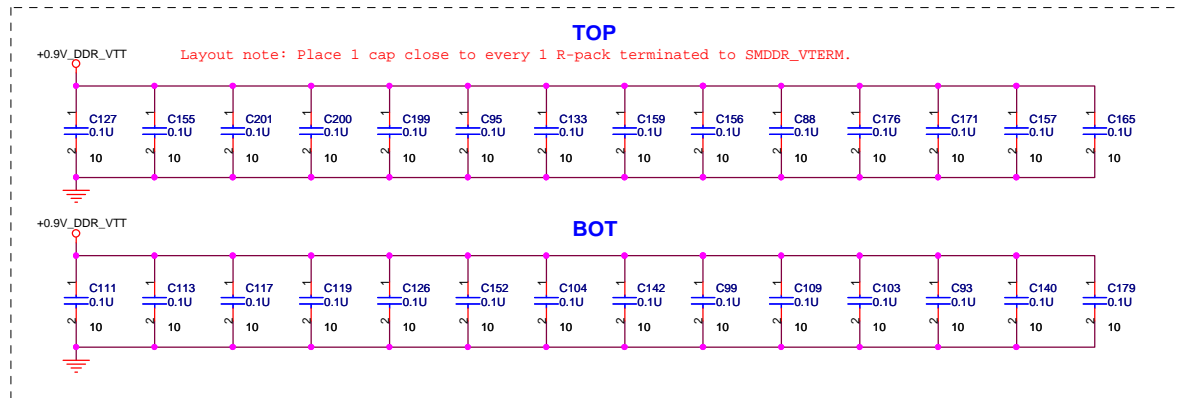
Place TX DC blocking caps close ICH8.





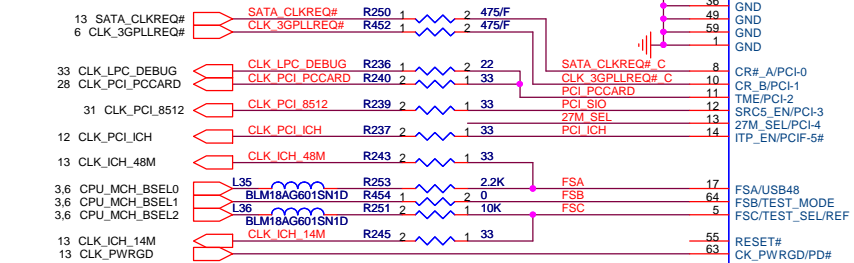
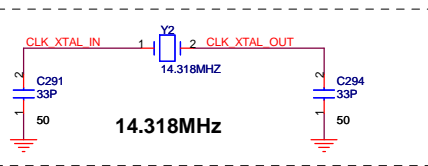
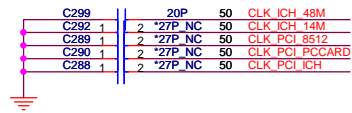


$$\begin{array}{l} 7] \quad 7 \\ 8] \quad 7 \\ \dots 7] \quad 7 \\ 0..7] \quad 7 \end{array}$$


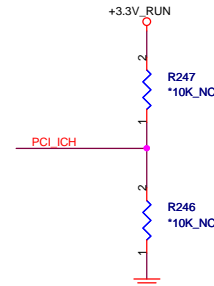
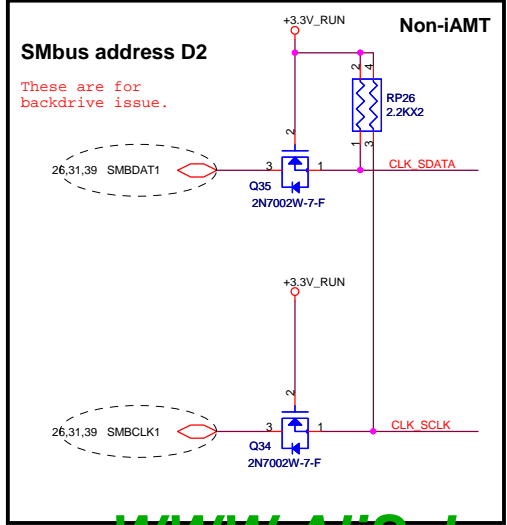
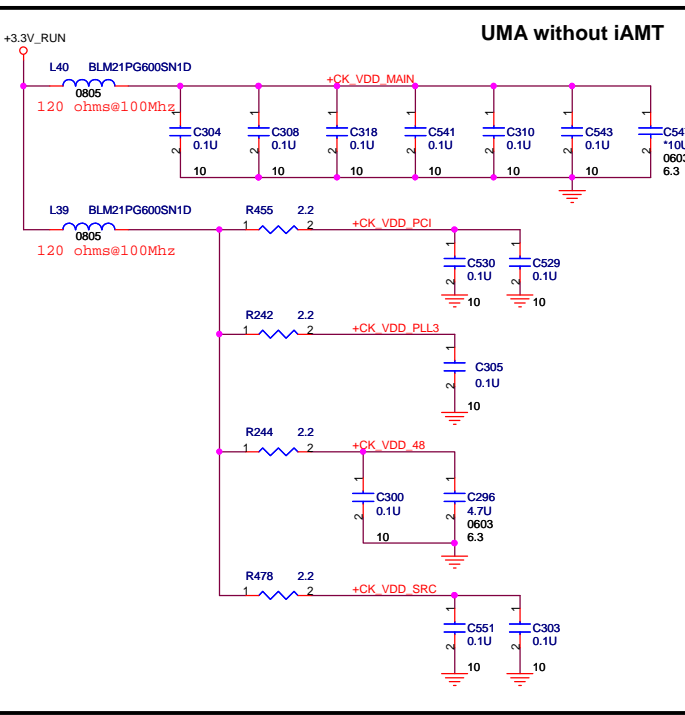
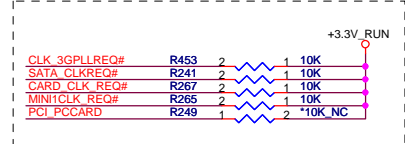
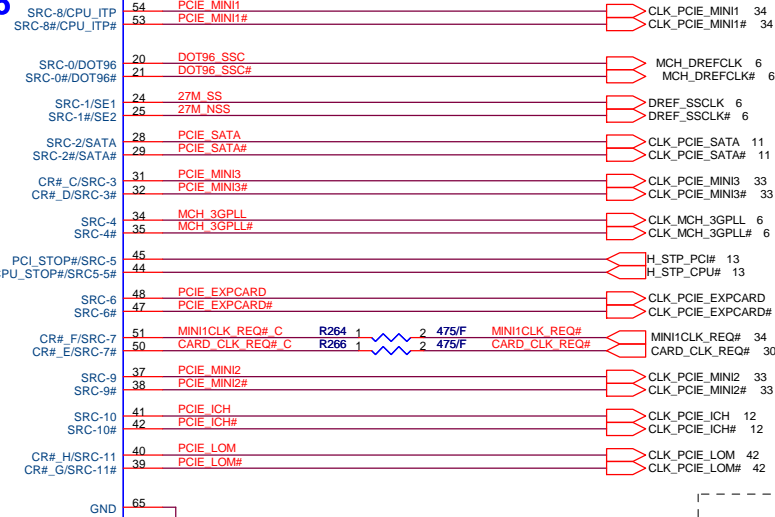


Title: DDR2 RES ARRAY		
Size: FMSB	Document Number: 16	Rev: 3A
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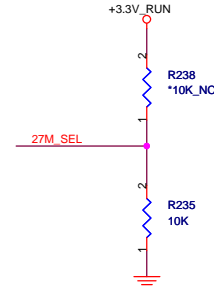
Add capacitor pads for improving WWAN.



CK505
QFN64



R246 POP: For Internal pull-low.
R235 POP: For internal pull-high.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL

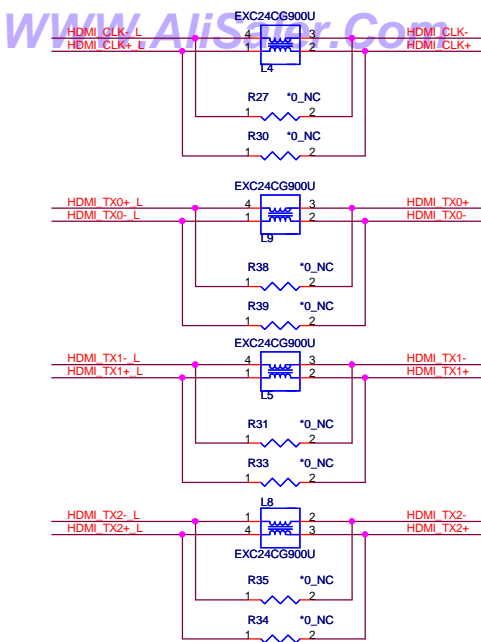
27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

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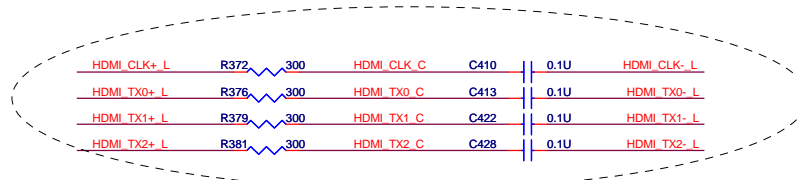
Title: CLOCK GENERATOR

Size: Document Number: FMBB Rev: 3A

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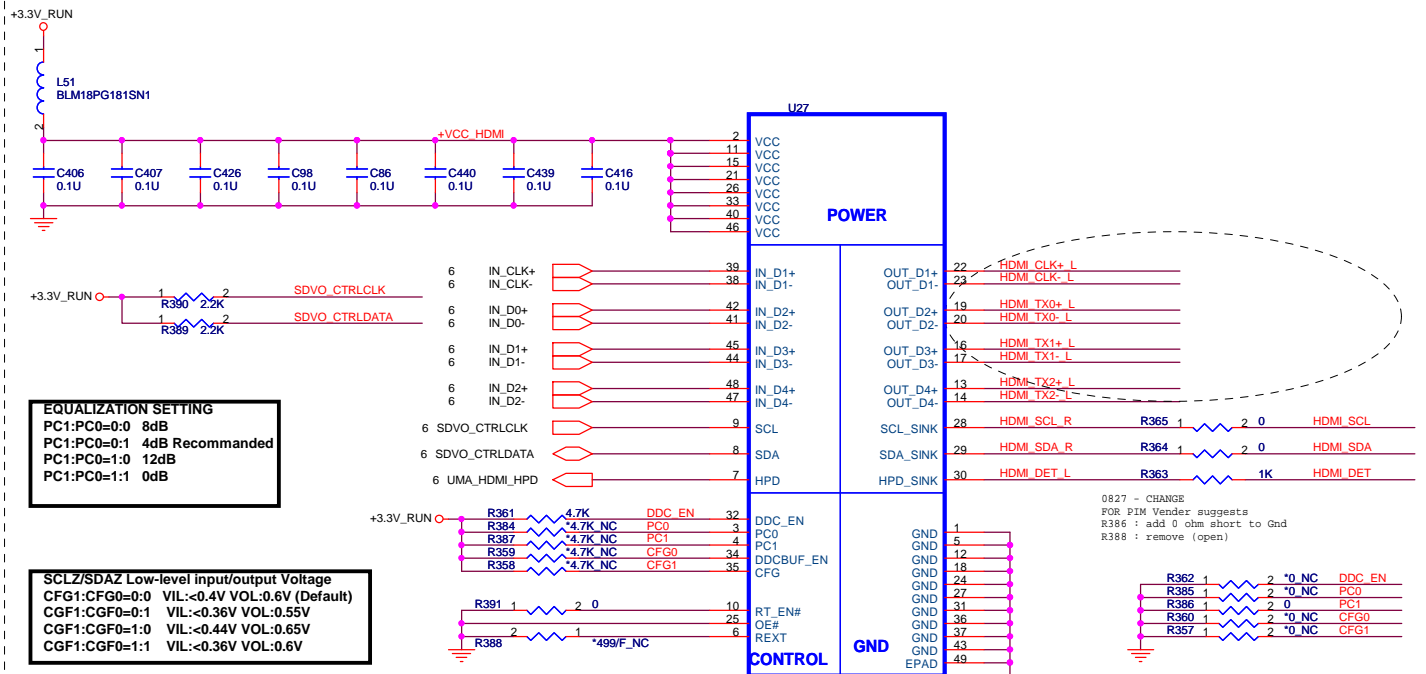
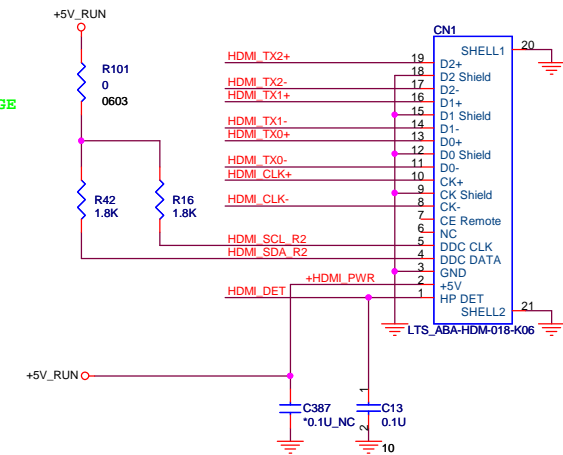


Reserve for EMI and close to HDMI CONN



HDMI Connector

07-24 - 23
FOR EA TEST HDMI CHANGE



EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V


PI3VDP411LSZDE

WWW.AliSaler.Com


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FLASH, RTC & KC		
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Title

Battery Selector


Size

Document Number
FM8B

Rev
3A

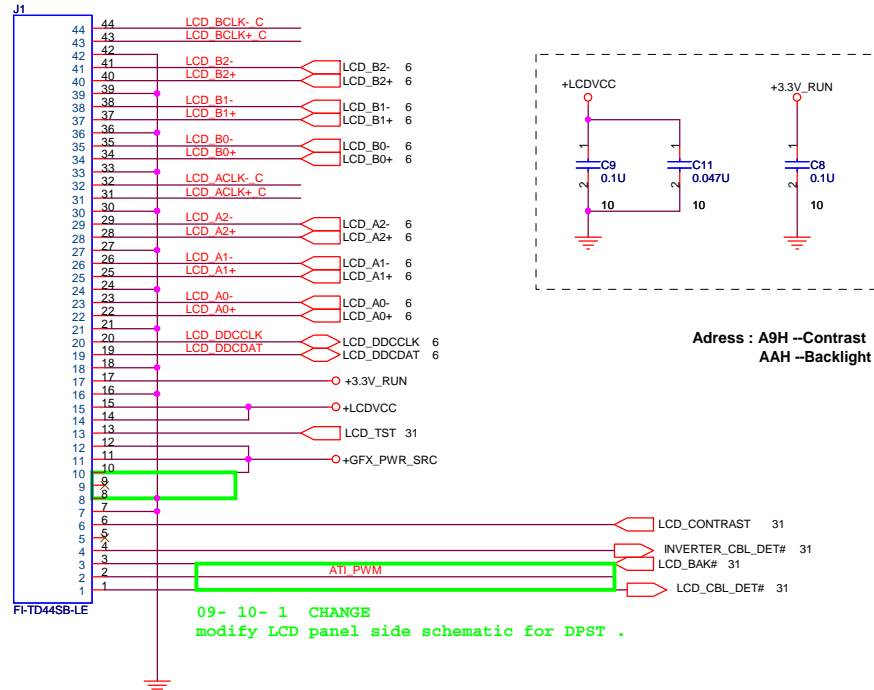
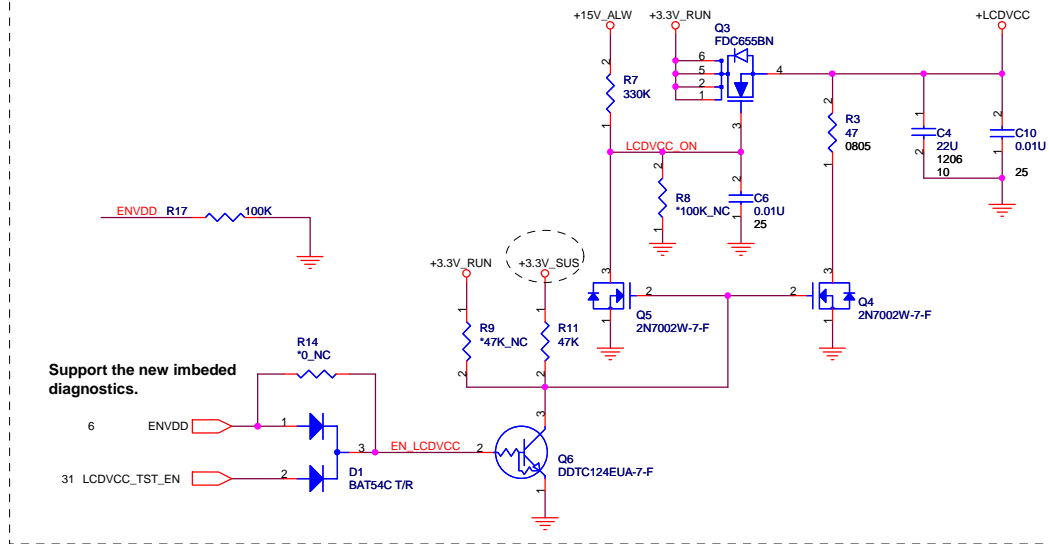
Date: Thursday, October 09, 2008

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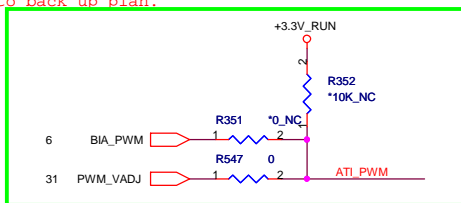
Title		
Docking Station CONN.		
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UMA

Populate R351 for DPST implementation only.

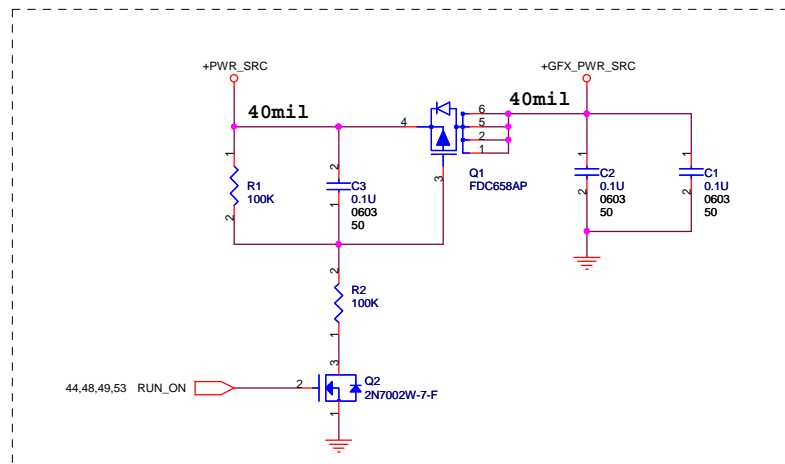
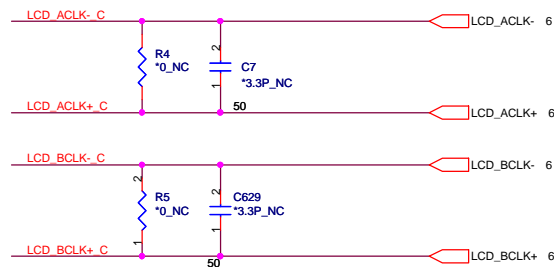
Populate R352 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.

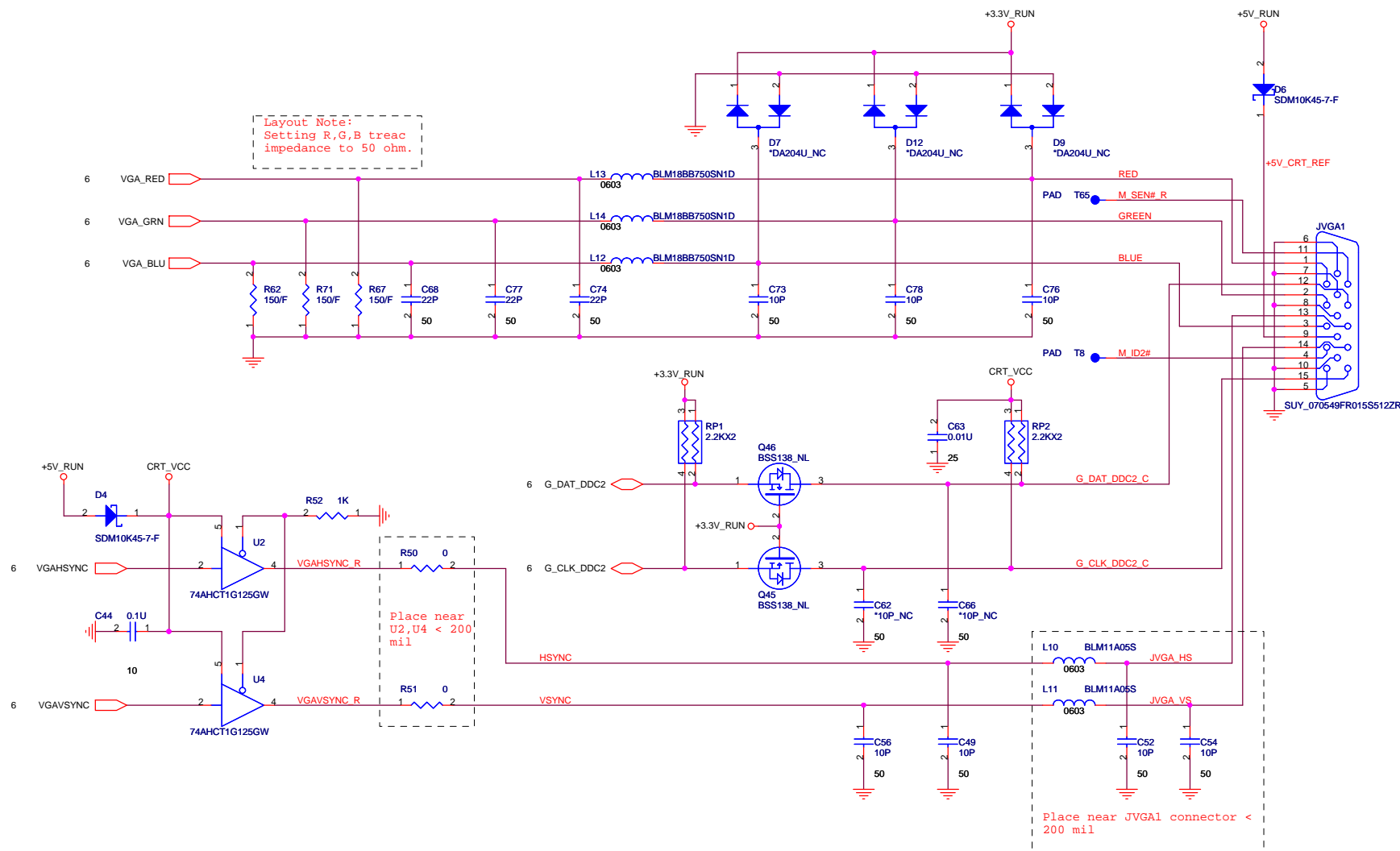


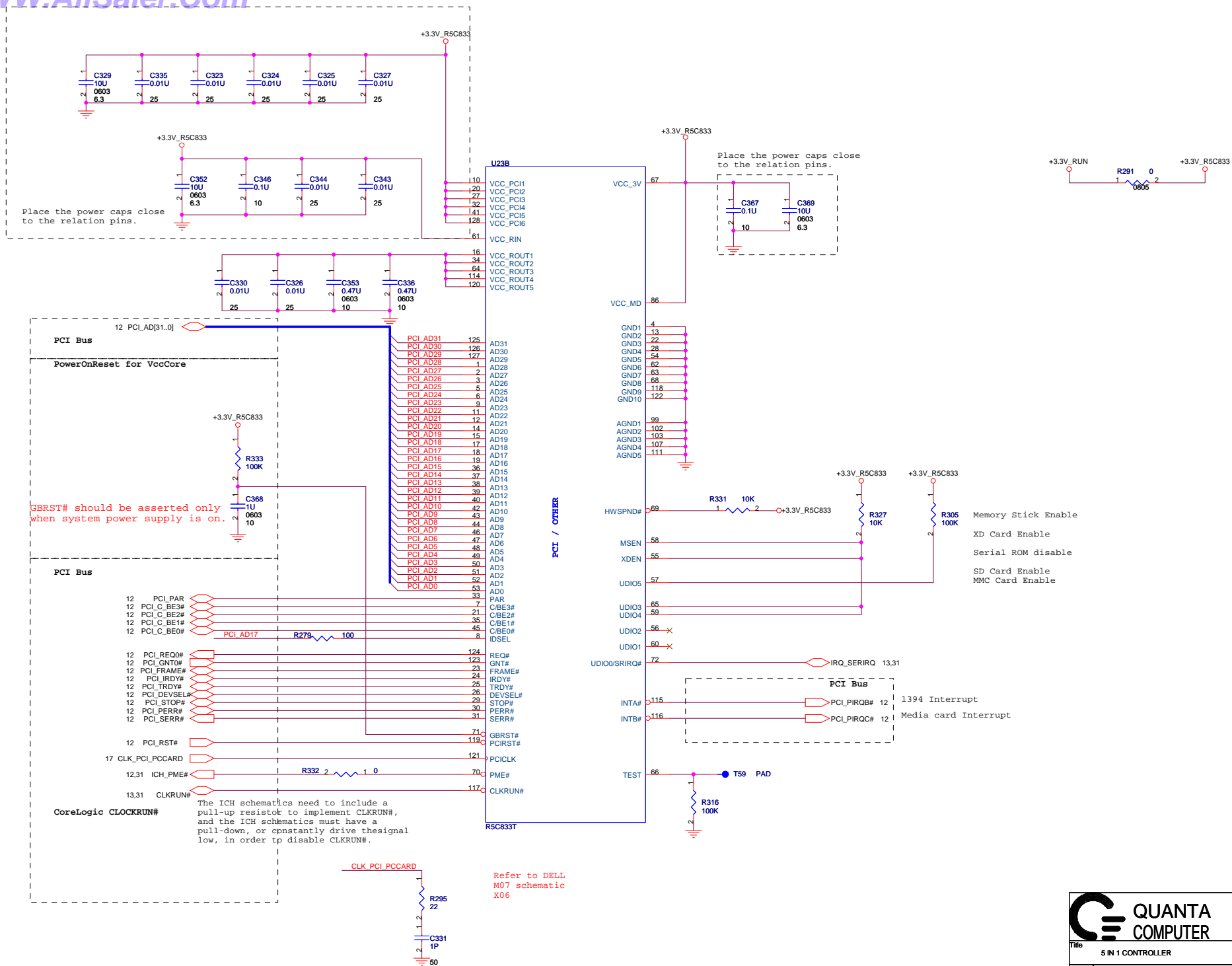
09- 10- 1 CHANGE modify LCD panel side schematic for DPST .

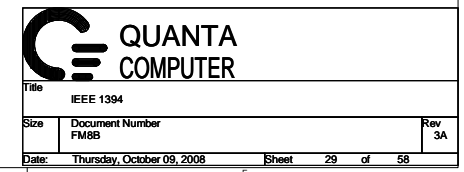
Shunt capacitors on LVDS for improving WWAN.

LCD B0-	C628	1	2	*3.3P	NC	50	LCD B0+
LCD B1-	C366	1	2	*3.3P	NC	50	LCD B1+
LCD B2-	C627	1	2	*3.3P	NC	50	LCD B2+
LCD A0-	C384	1	2	*3.3P	NC	50	LCD A0+
LCD A1-	C386	1	2	*3.3P	NC	50	LCD A1+
LCD A2-	C385	1	2	*3.3P	NC	50	LCD A2+

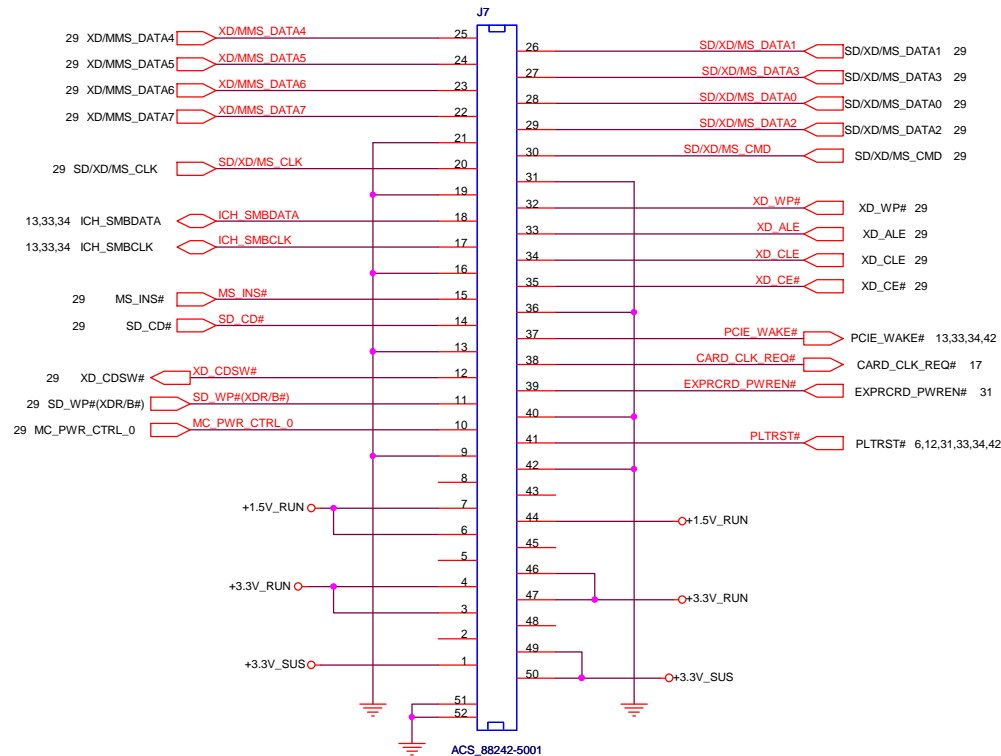




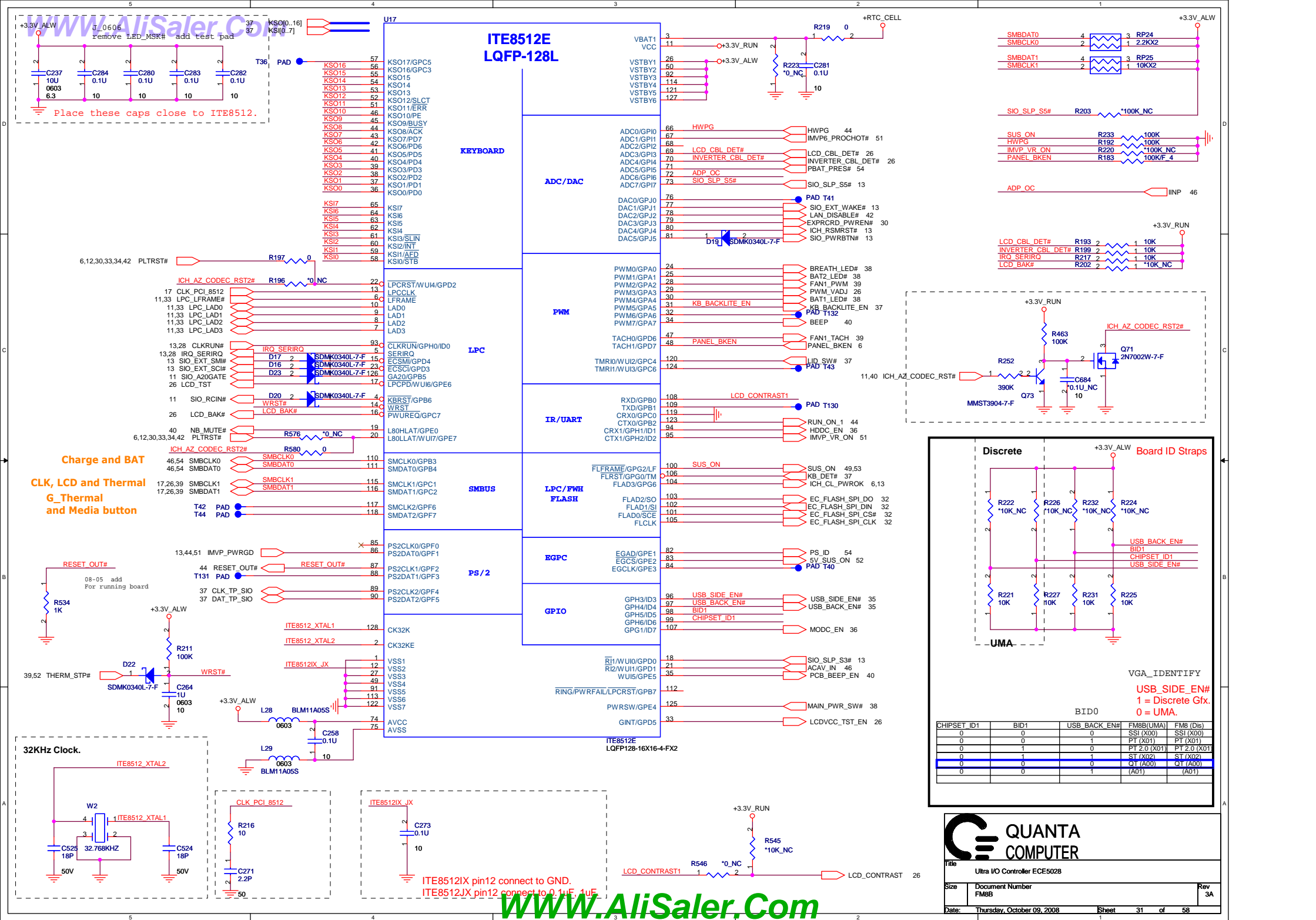


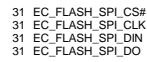


Express Card/CARD READER

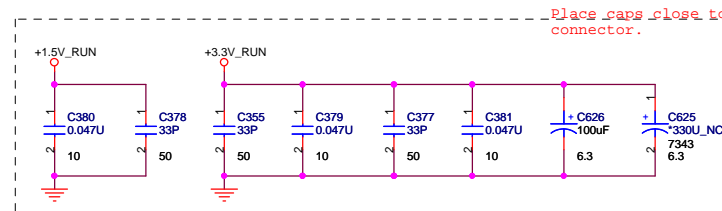
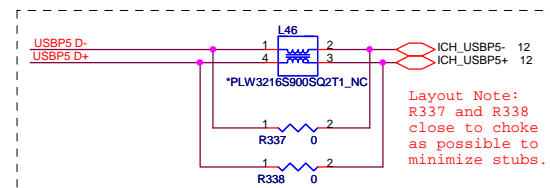
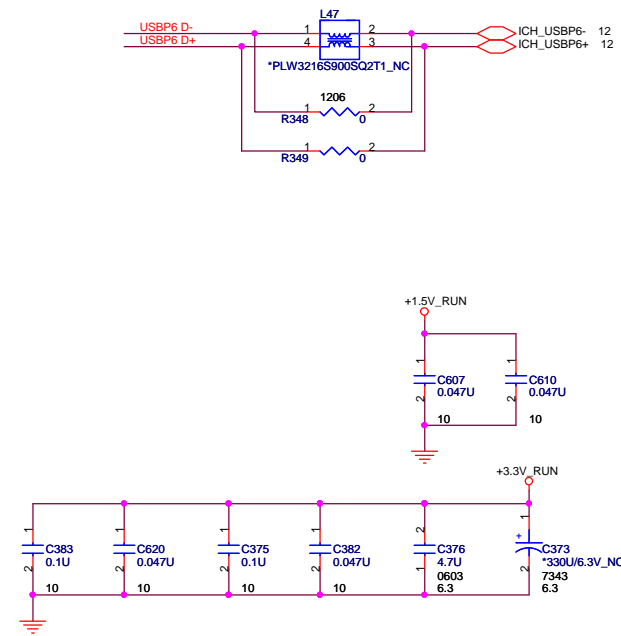


Title ExpressCard/SmartCard		
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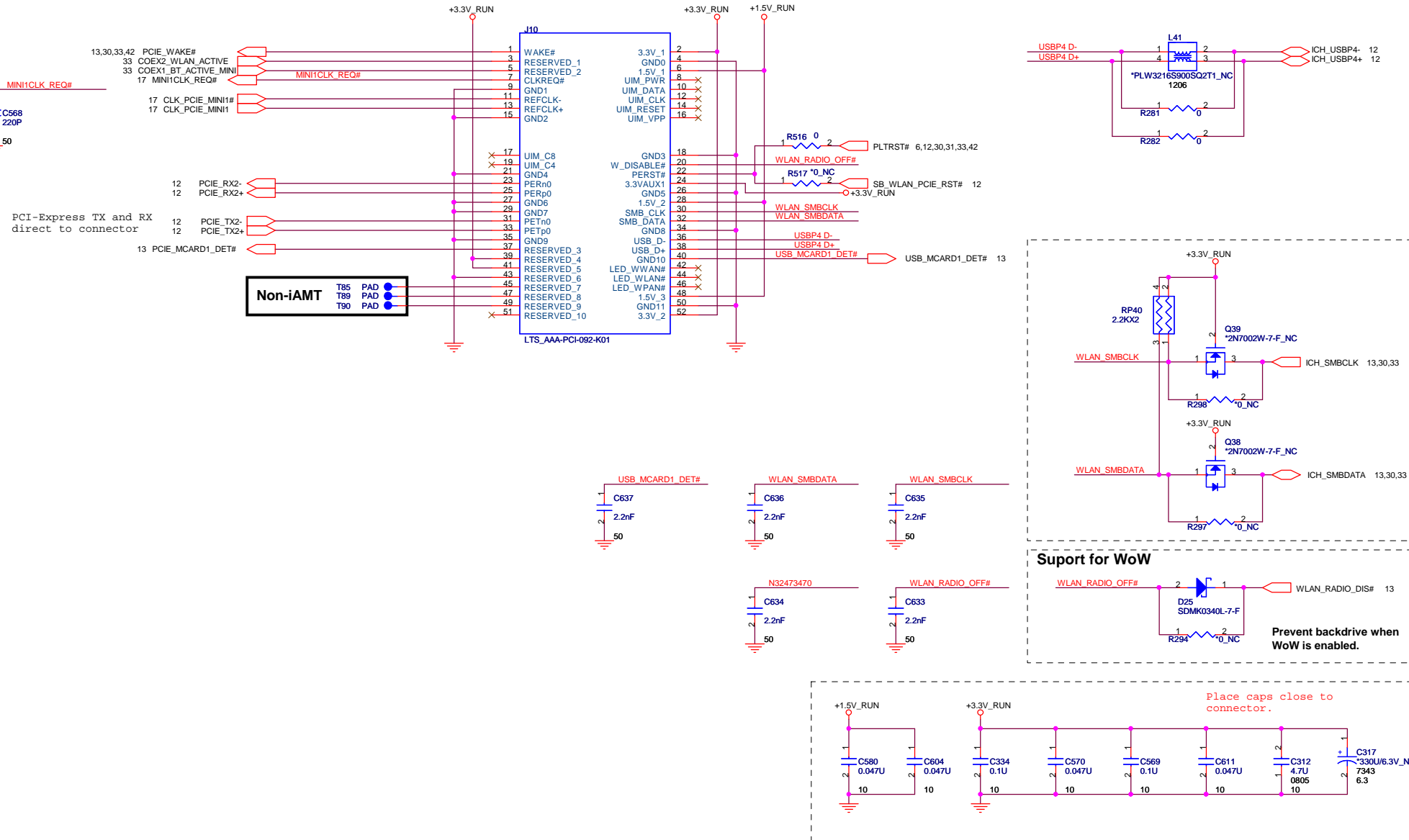
MiniCard WWAN connector



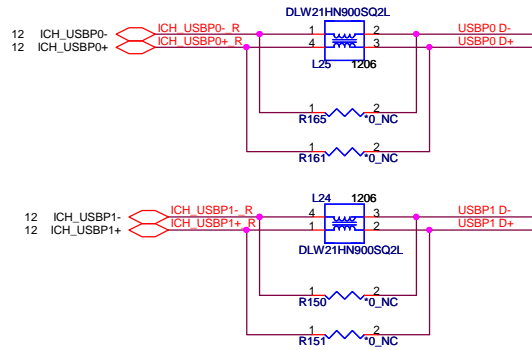
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MINI-PCI			
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MiniCard WLAN connector

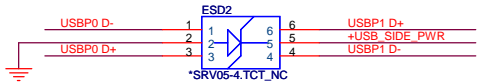


External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

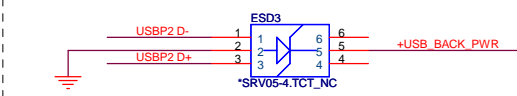
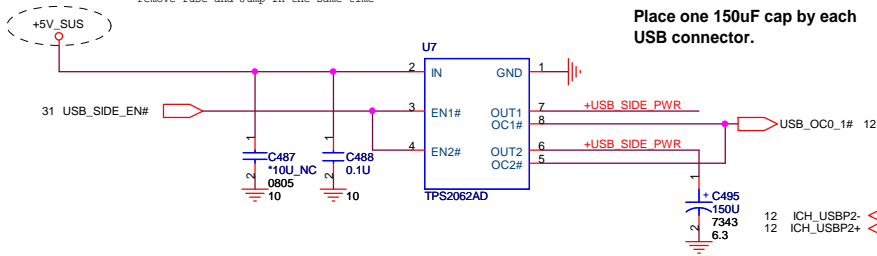


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

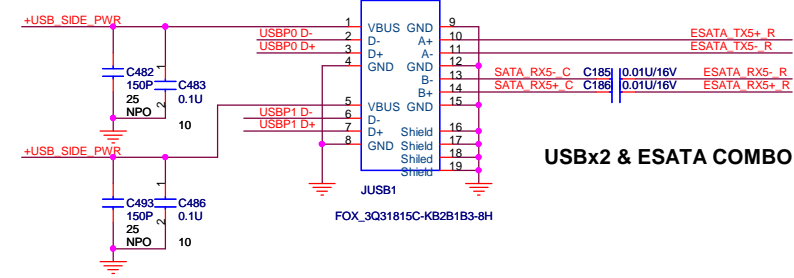
Place ESD diodes as close as USB connector.



08 - 06 Del
remove fuse and Jump in the same time

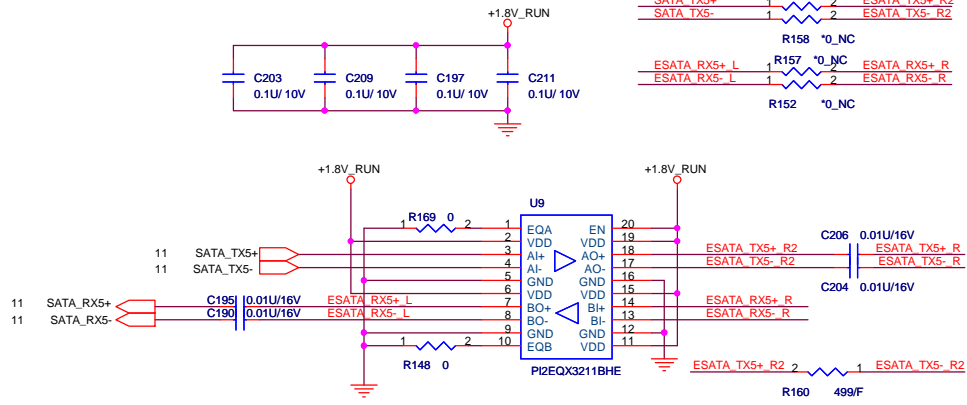


Side External USBX2

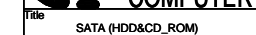


USBx2 & ESATA COMBO

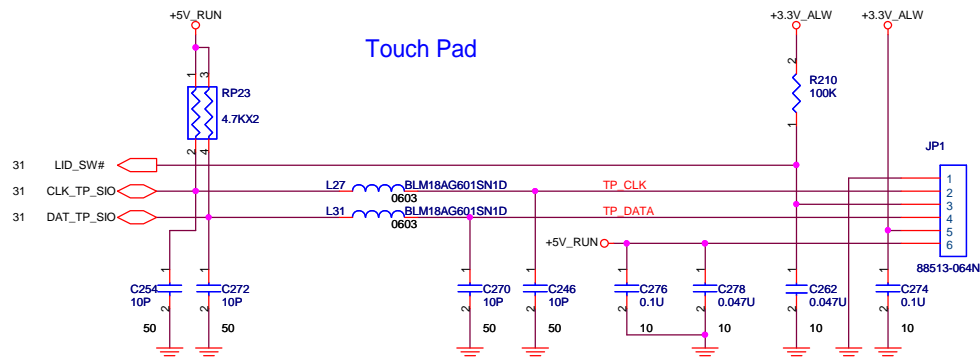
E-SATA Re-driver



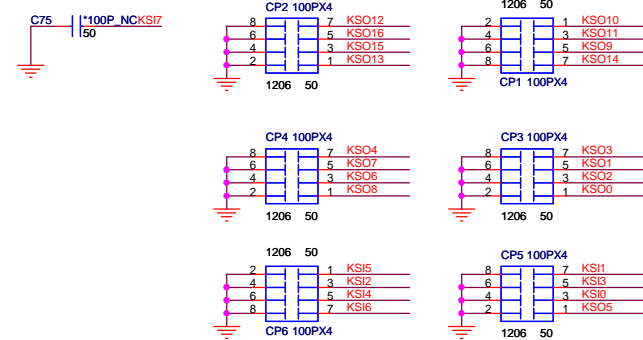
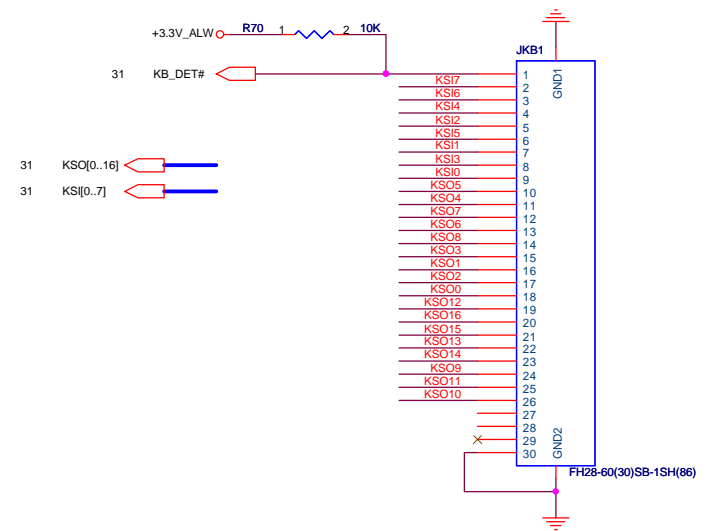
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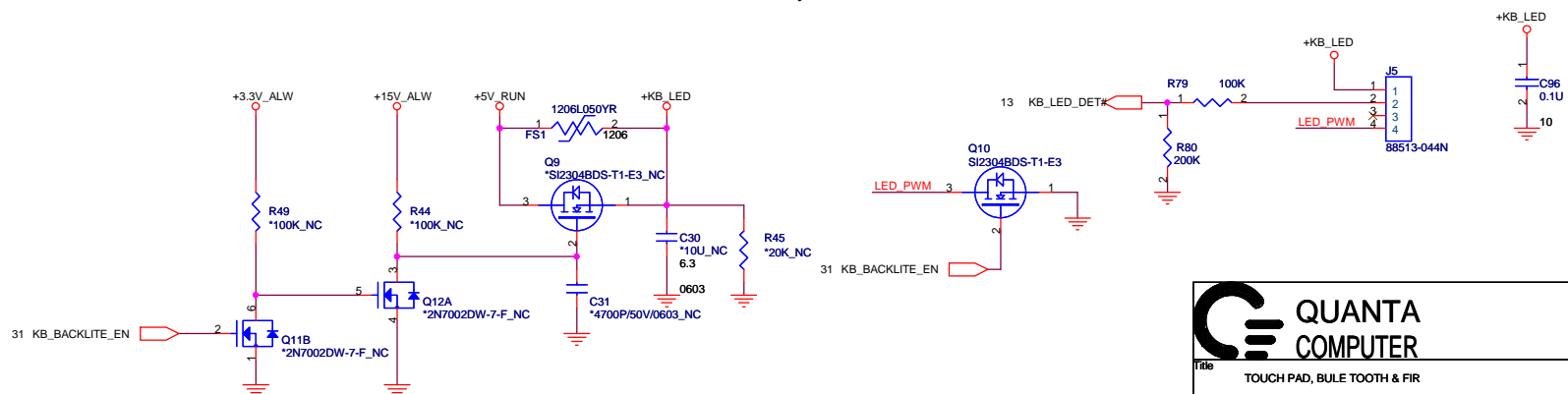


KEYBOARD CONNECTOR



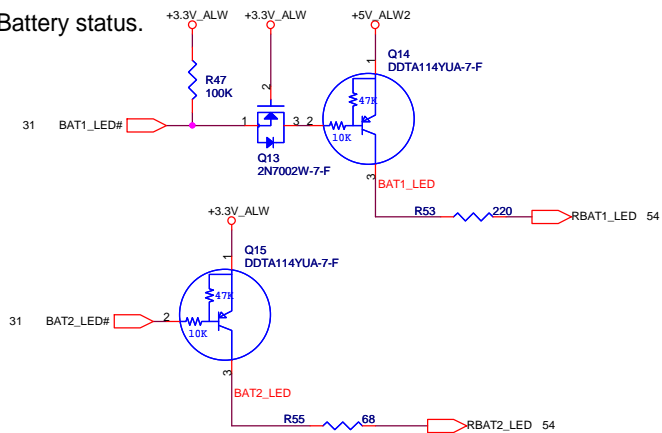
100P CAPS CLOSE TO JKB1

Key board Illumination

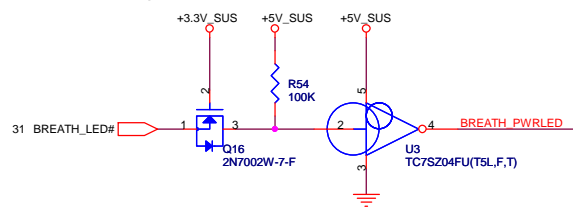


Title TOUCH PAD, BULE TOOTH & FIR		
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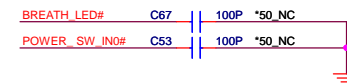
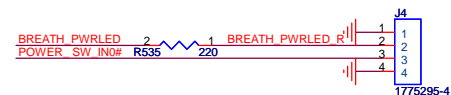
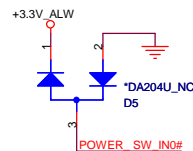
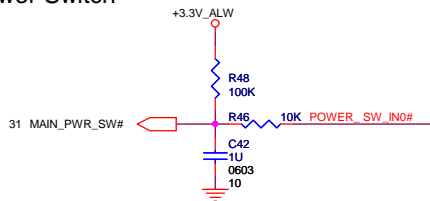
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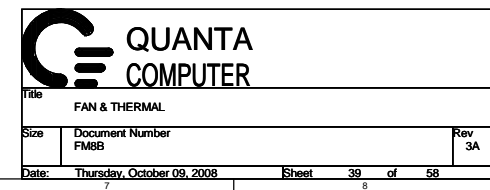


Power & Suspend.

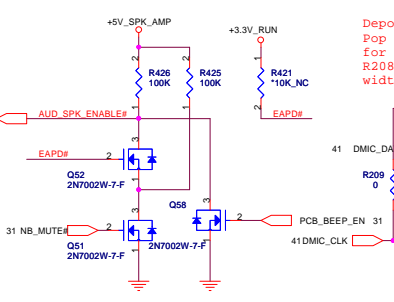
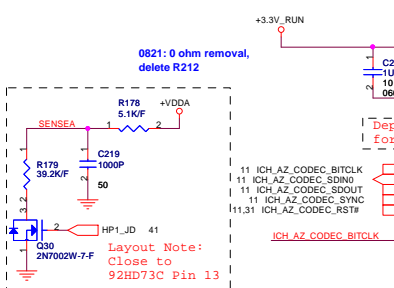
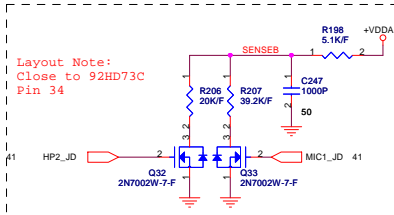
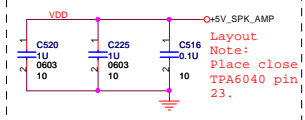
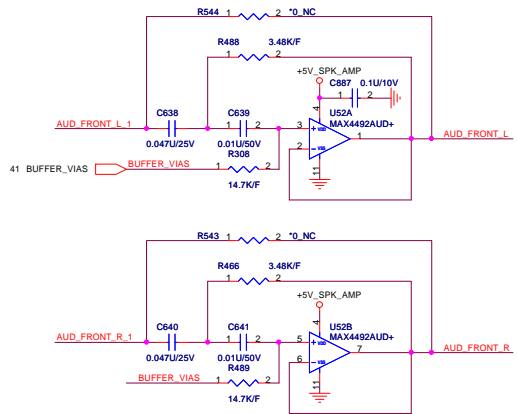
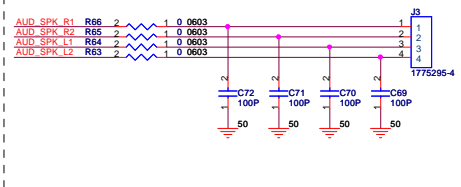
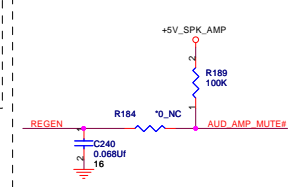
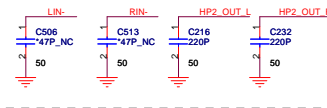


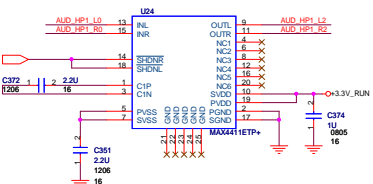
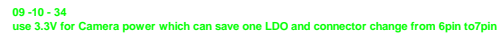
Power Switch



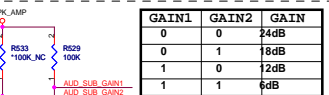


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

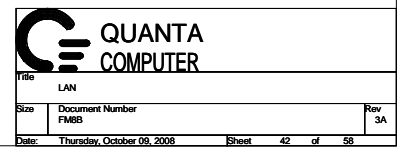




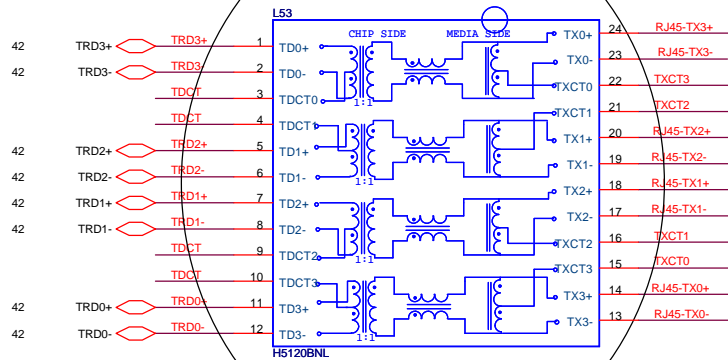
SYNC	Condition
VDD	Spread-spectrum mode with $f_S = 1200\text{kHz} \pm 70\text{kHz}$.
GND	Fixed-frequency mode with $f_S = 1100\text{kHz}$.
FLOAT	Fixed-frequency mode with $f_S = 1500\text{kHz}$.
Clocked	Fixed-frequency mode with $f_S = \text{external clock frequency}$.



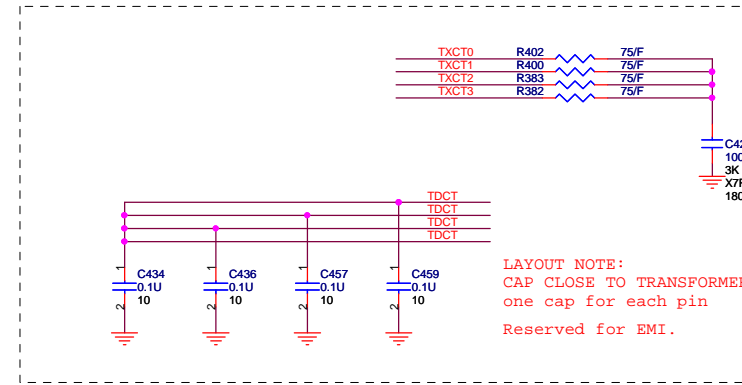
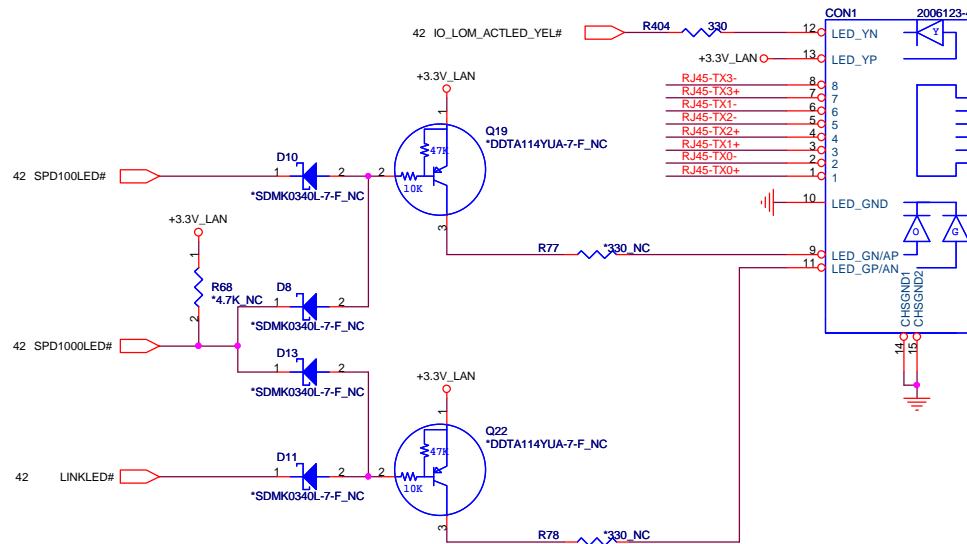
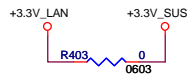
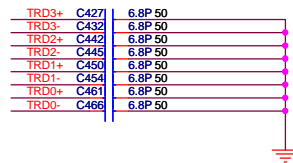
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB

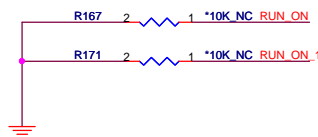
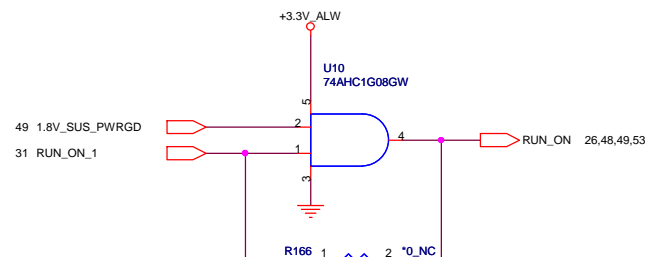
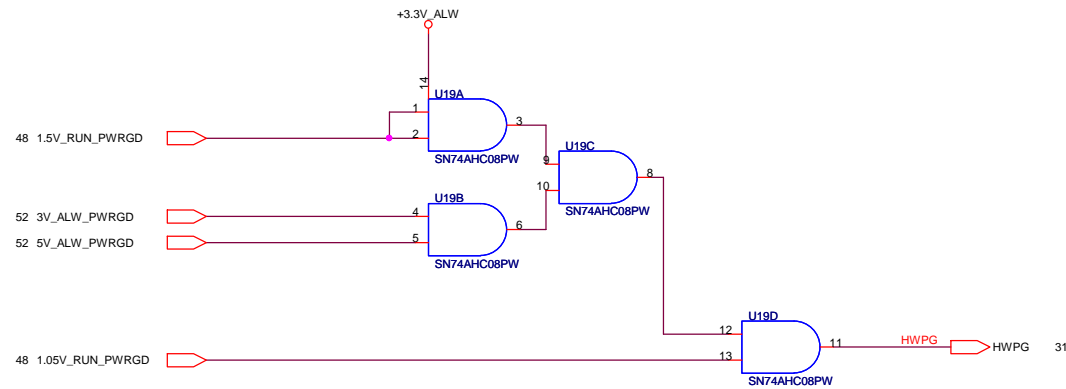
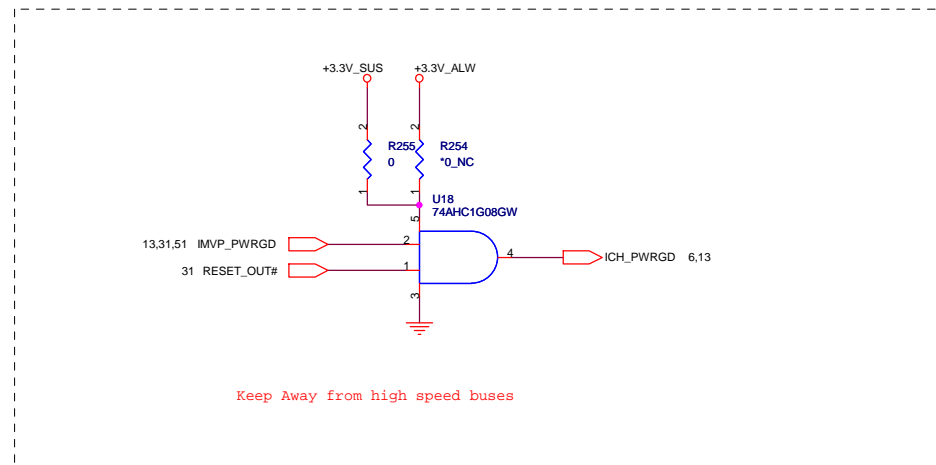



TRANSFORM




CHANGE FOR EA
FORM DTA CHANGE TO PLE H5120BNL



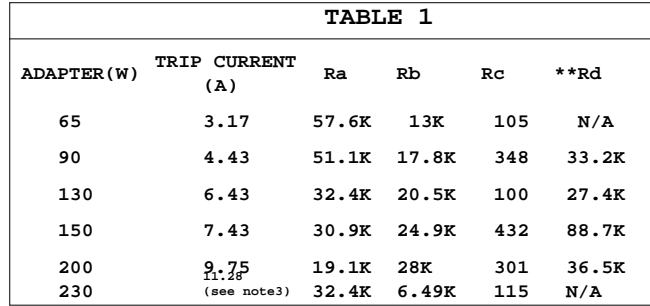


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Title: System Reset Circuit			
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COMPUTER

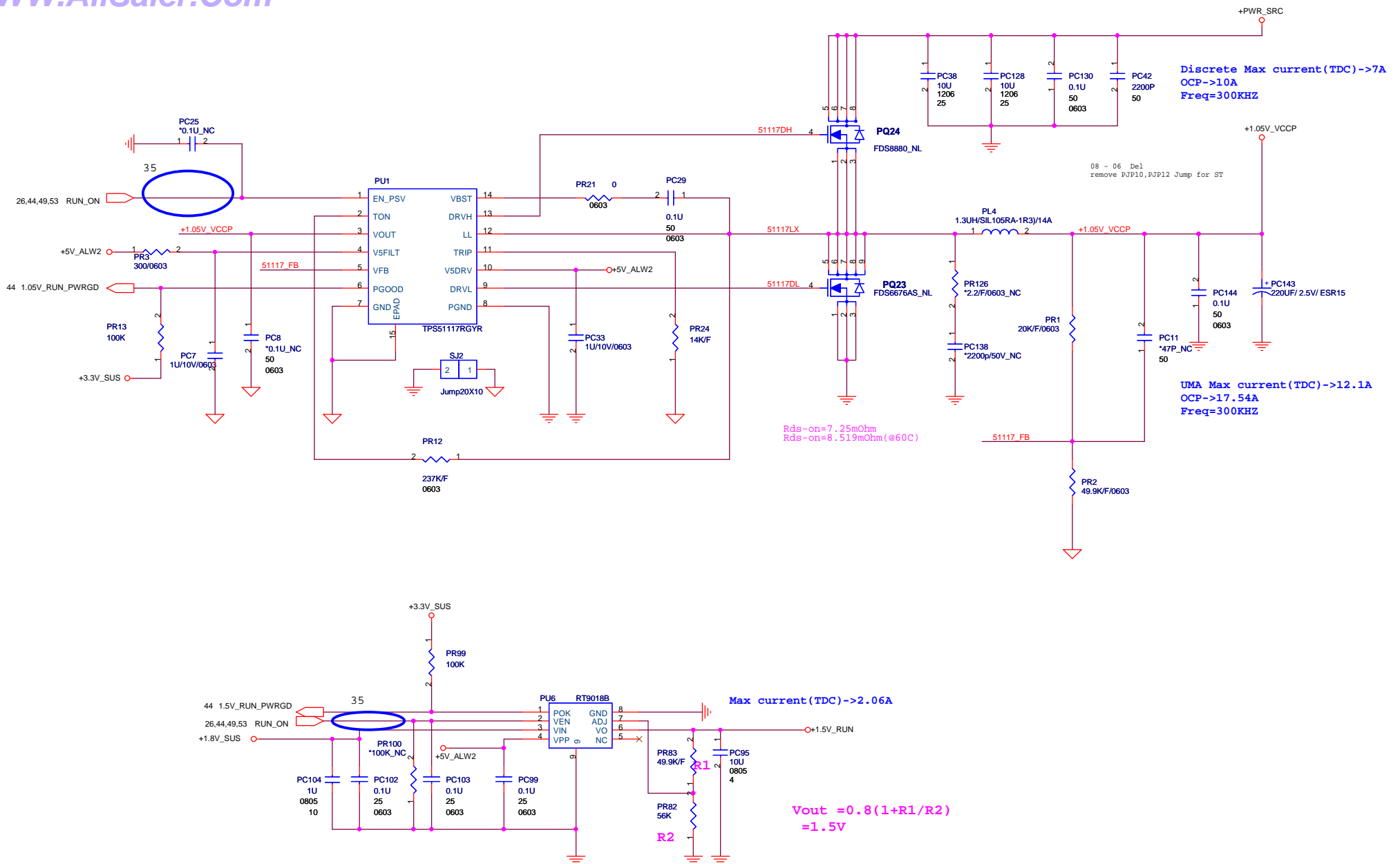
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Docking Q-SWITCH		
Size	Document Number	Rev
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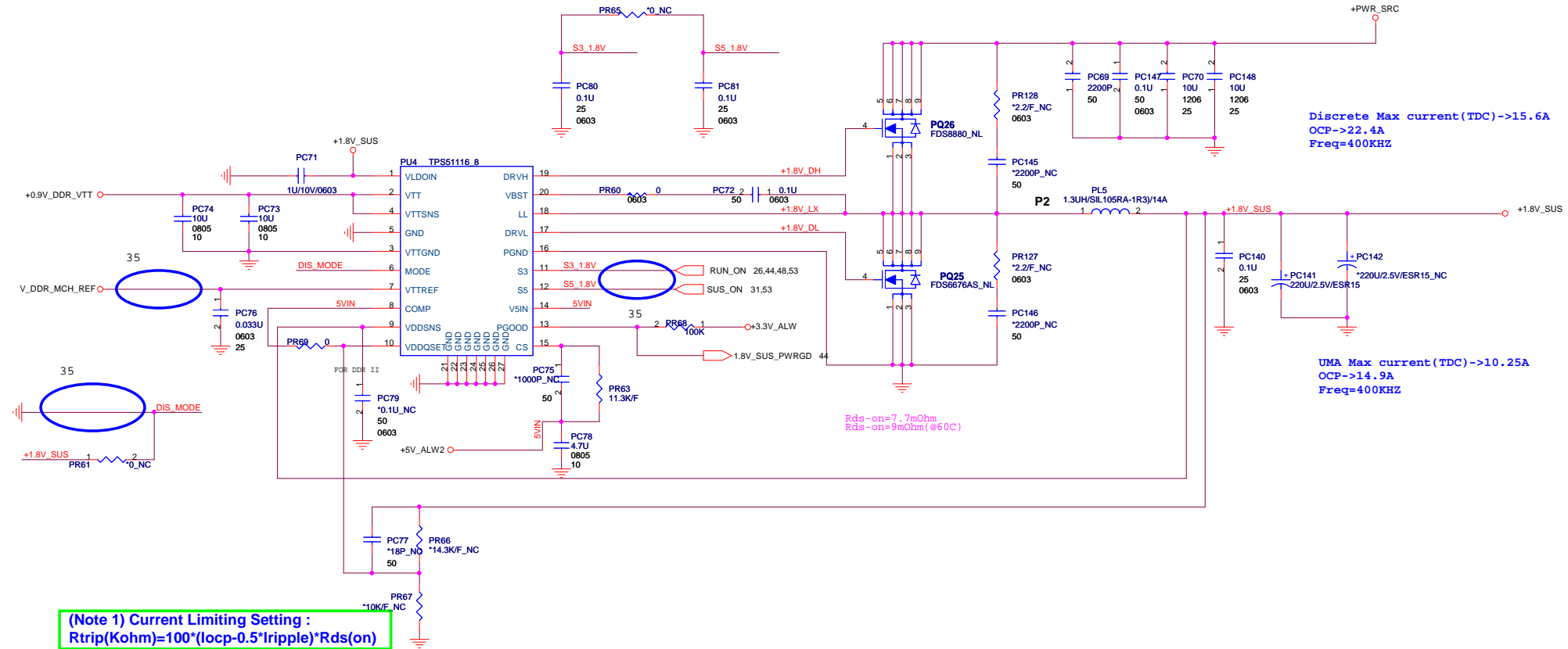


Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.


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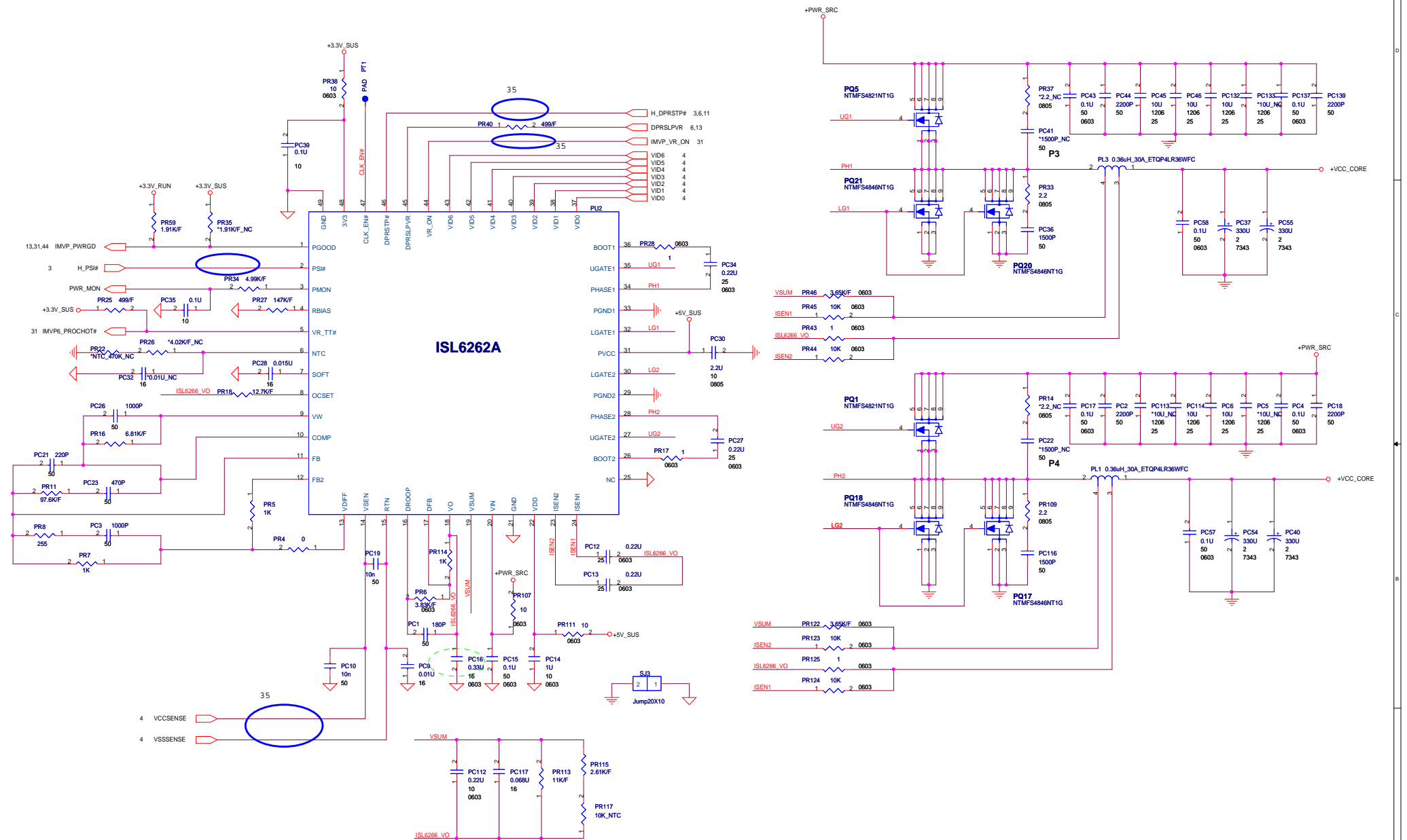
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Title			
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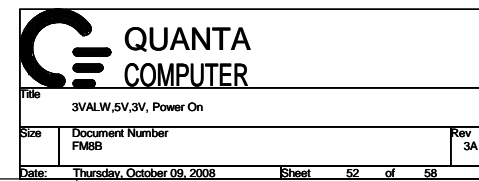


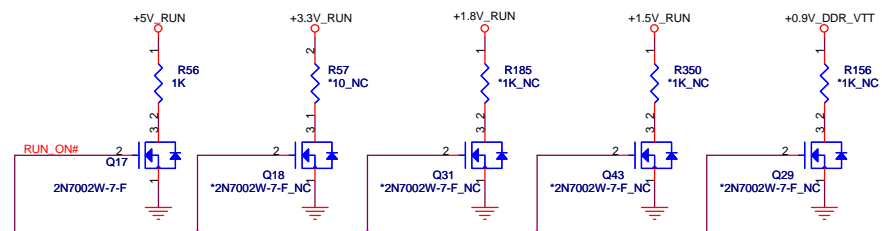


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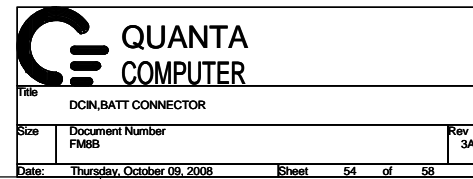
Title RUN POWER SW

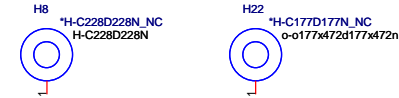
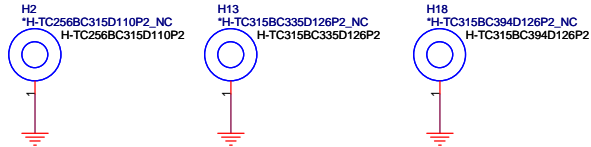
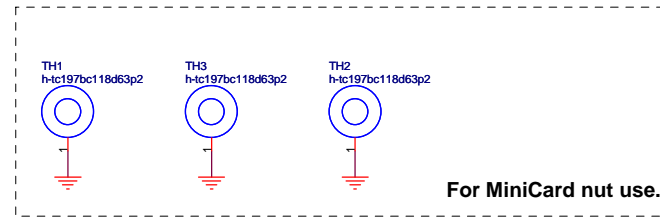
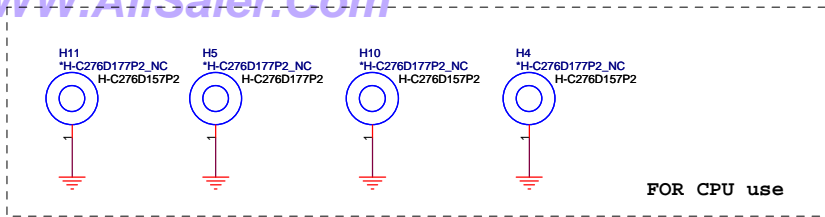
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Date: Thursday, October 09, 2008

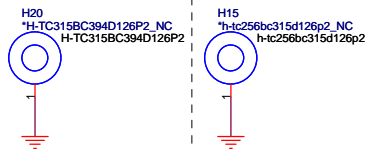
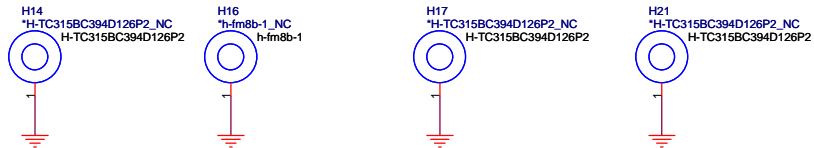
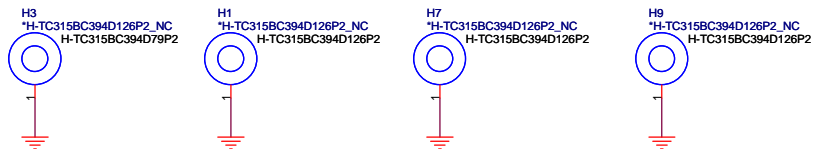
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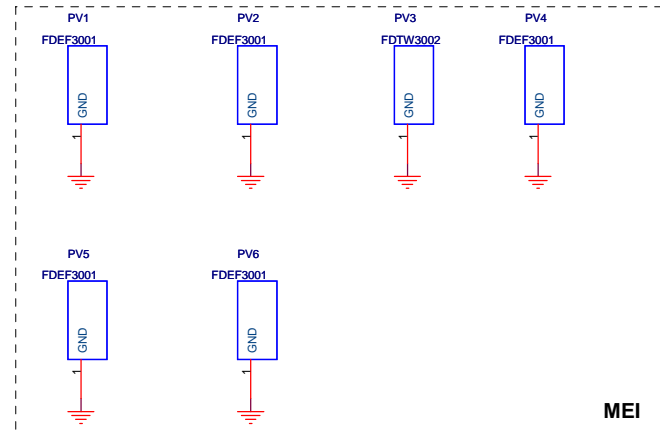





Non PTH




FOR 1394



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Stitching caps.

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COMPUTER

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EMI CAP		
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