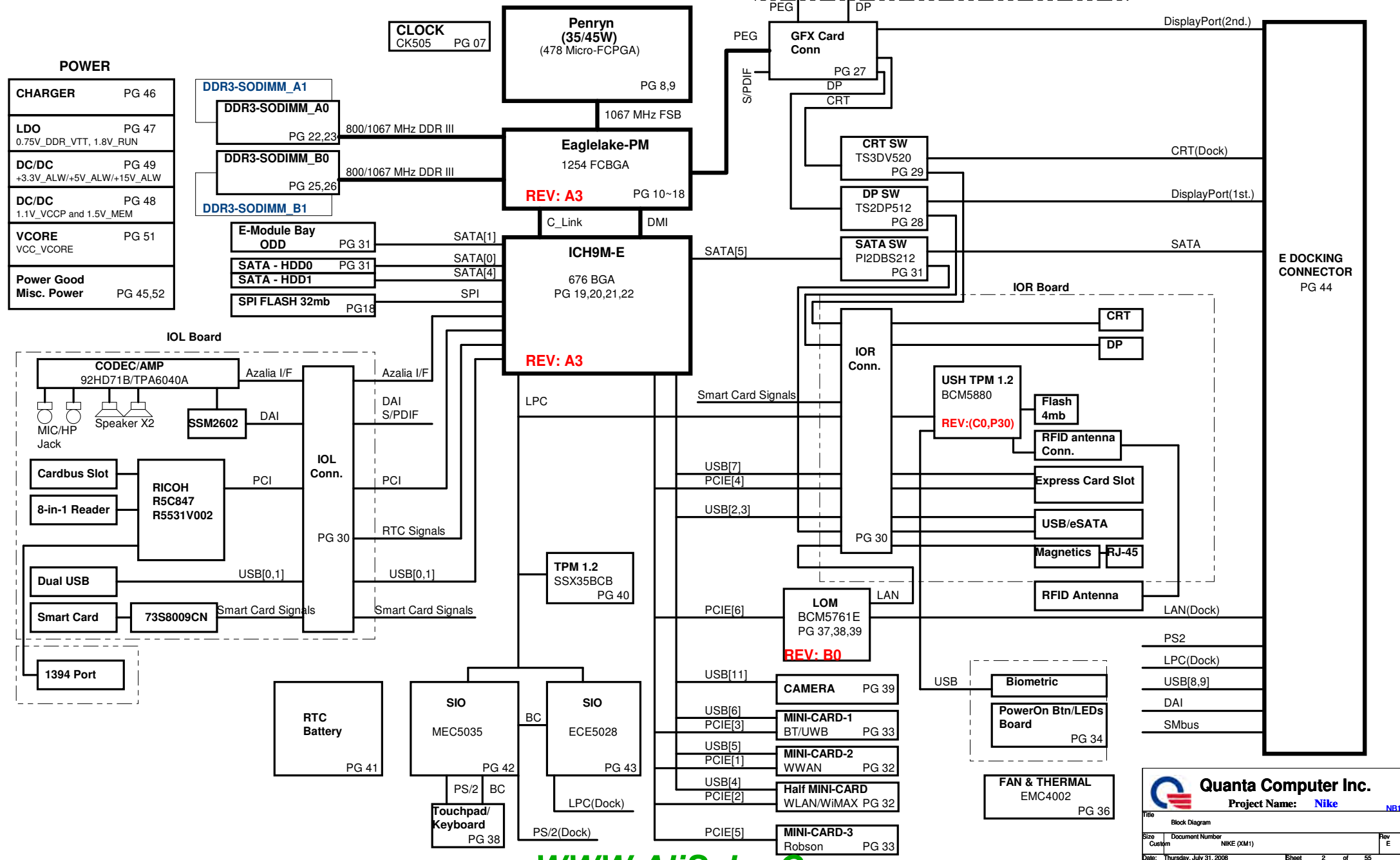


Quanta Project Name: XM1
Dell Project Name: Nike
A00(QT) Stage
BOARD REV : E
2008-07-25

**PWA XXX, PWB XXX,
SCHEM XXX.
Board Ver : E
Date:20080716**



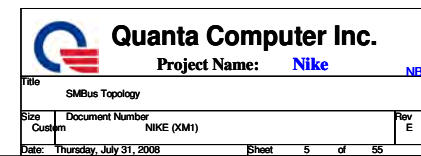
| INDEX | |
|-------|----------------------------|
| Pg# | Description |
| 01 | CoverPage |
| 02 | MB Block Diagram |
| 03 | Index |
| 04 | Config. |
| 05 | SMBus Topology |
| 06 | Power Sequence Diagram |
| 07 | Clock Generator |
| 08~09 | Penryn |
| 10~18 | Eaglelake |
| 19~22 | ICH9M |
| 23~26 | DDR3 |
| 27 | GFX CARD CONN. |
| 28 | DisplayPort SWITCH |
| 29 | CRT SWITCH |
| 30 | IOR and IOL connector. |
| 31 | SATA(HDD_ODD) eSATA SWITCH |
| 32 | MINI Card |
| 33 | MINI Card |
| 34 | TP PWR BUTTON |
| 35 | CCD SNIFFER LED. |
| 36 | THERMAL EMC4002 |
| 37~39 | BCM5761E_LOM |
| 40 | SSX35BCB (TPM for China) |
| 41 | RTC BATTERY |
| 42 | SIO_MEC5035 |
| 43 | SIO-ECE5028 |
| 44 | E-DOCKING CONNECTOR. |
| 45 | System Power Good. |
| 46 | Battery Charger. |
| 47 | 0.75V_DDR_VTT, 1.8V_RUN |
| 48 | 1.1V_VCCP and 1.5V_MEM |
| 49 | 5V_ALW, 3V_ALW |
| 50 | DCIN, Battery Connector |
| 51 | CPU_VCORE (ADP3207A) |
| 52 | Power Misc |
| 53 | Screw hole |

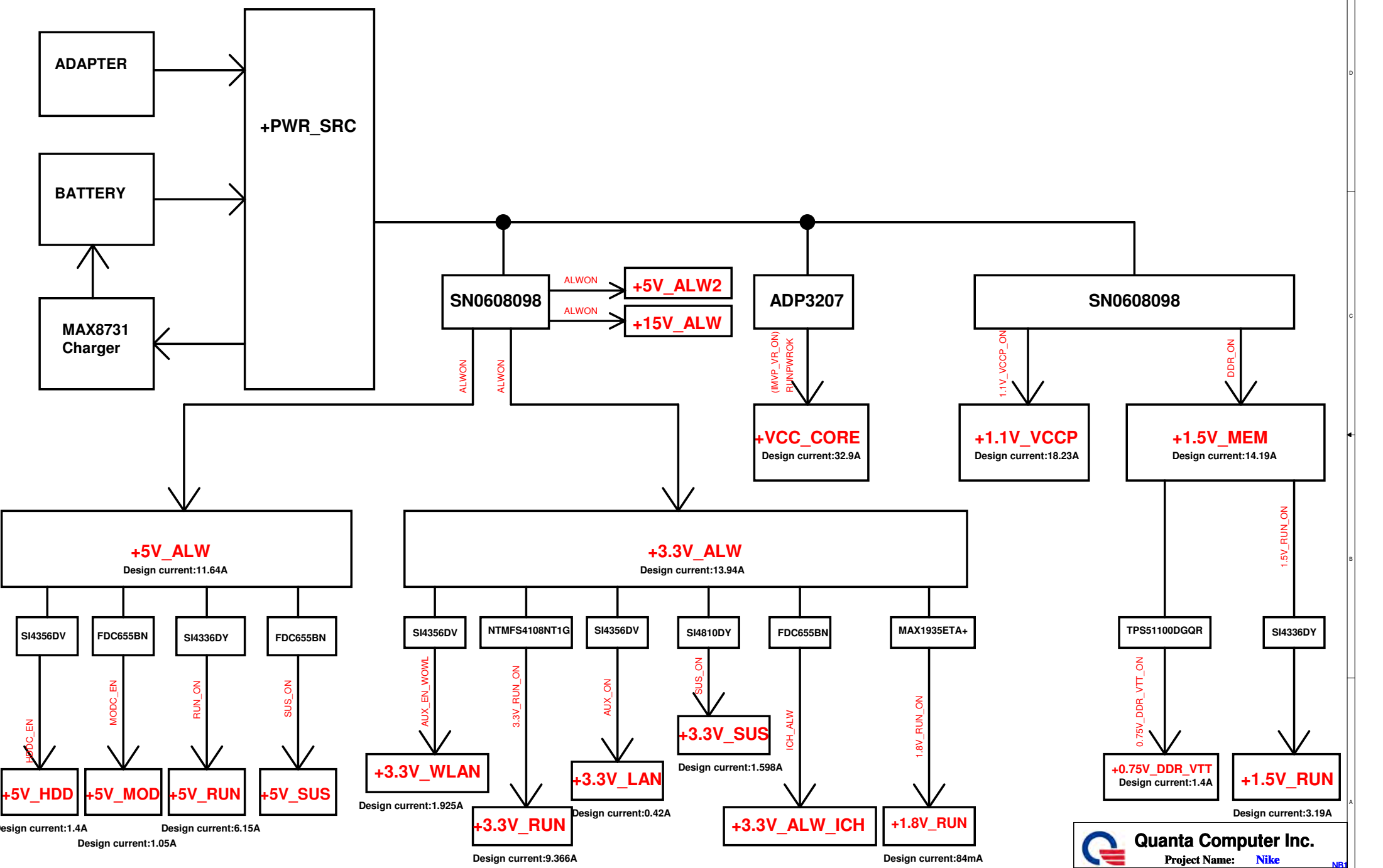
| Signal State | SLP S3# | SLP S4# | SLP S5# | SLP M# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|-----------------|------------|------------|------------|-----------|-----------------|------------|--------------|--------------|--------|
| S0 | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 | LOW | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 | LOW | LOW | HIGH | LOW | ON | OFF | OFF | OFF | OFF |
| S5 | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |


| Power Plane State | +15V_ALW +5V_ALW +3.3V_ALW_ICH +3.3V_RTC_LDO | +3.3V_SUS +1.5V_MEM | +5V_RUN +3.3V_RUN +1.5V_RUN +0.75V_DDR_VTT +1.1V_VCCP +VCC_CORE |
|-------------------------|---|------------------------|--|
| S0 | ON | ON | ON |
| S3 | ON | ON | OFF |
| S5 S4/AC | ON | OFF | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF |

| ICH9M-E | USB PORT# | DESTINATION |
|---------|-----------|--------------|
| | 0 | Left Top |
| | 1 | Left Bot |
| | 2 | Right Top |
| | 3 | Right Bot |
| | 4 | WLAN |
| | 5 | WWAN |
| | 6 | WPAN |
| | 7 | Express card |
| | 8 | DOCKING |
| | 9 | DOCKING |
| | 10 | USH |
| | 11 | Camera |

| ICH9M-E | PCI EXPRESS | DESTINATION |
|---------|-------------|--------------|
| | Lane 1 | WWAN |
| | Lane 2 | WLAN |
| | Lane 3 | BT/UWB |
| | Lane 4 | Express Card |
| | Lane 5 | Robson |
| | Lane 6 | Giga Bit LOM |



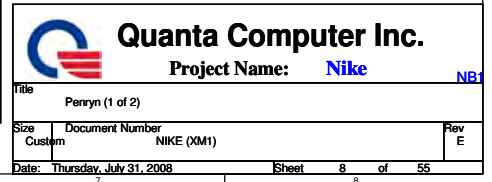




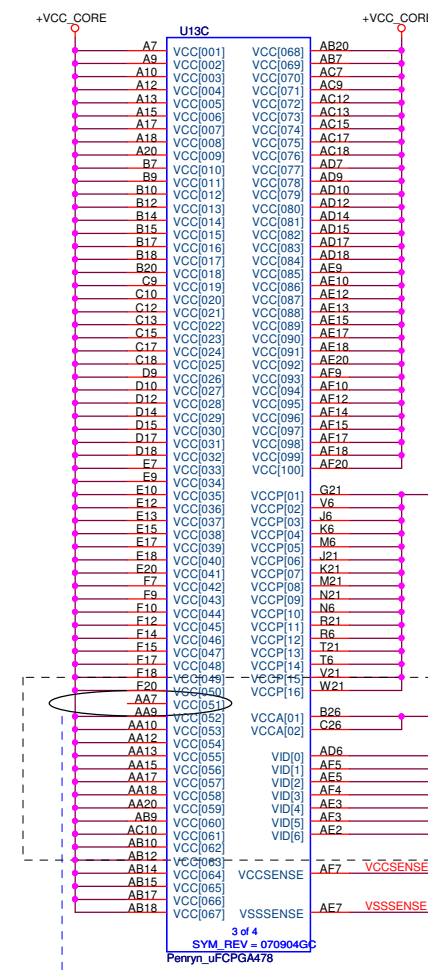
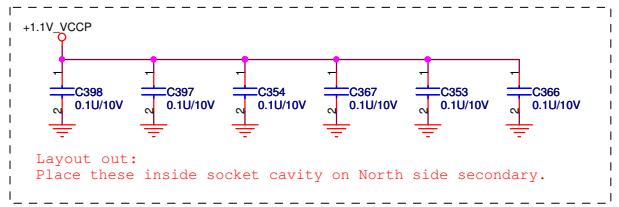
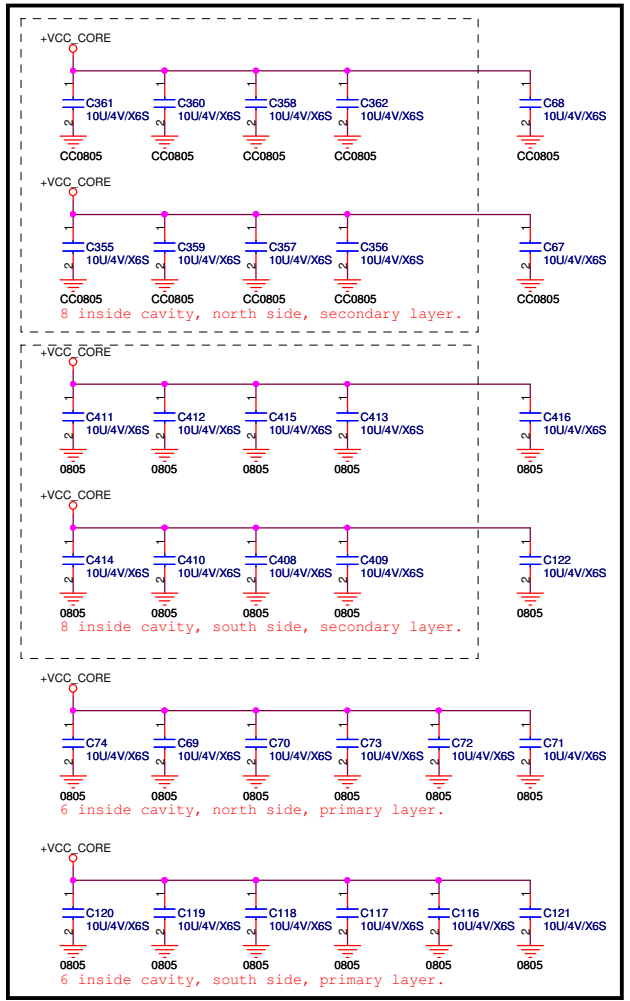
Quanta Computer Inc.

Project Name: Nike

| | | | |
|-------------------------------|-----------------|------------|-------|
| Title | | Screw hole | |
| Size | Document Number | Rev | |
| Custom | NIKE (XM1) | E | |
| Date: Thursday, July 31, 2008 | Sheet | 6 | of 55 |

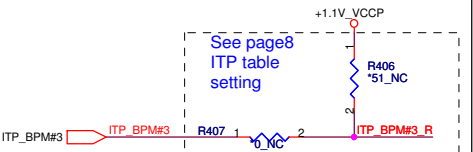
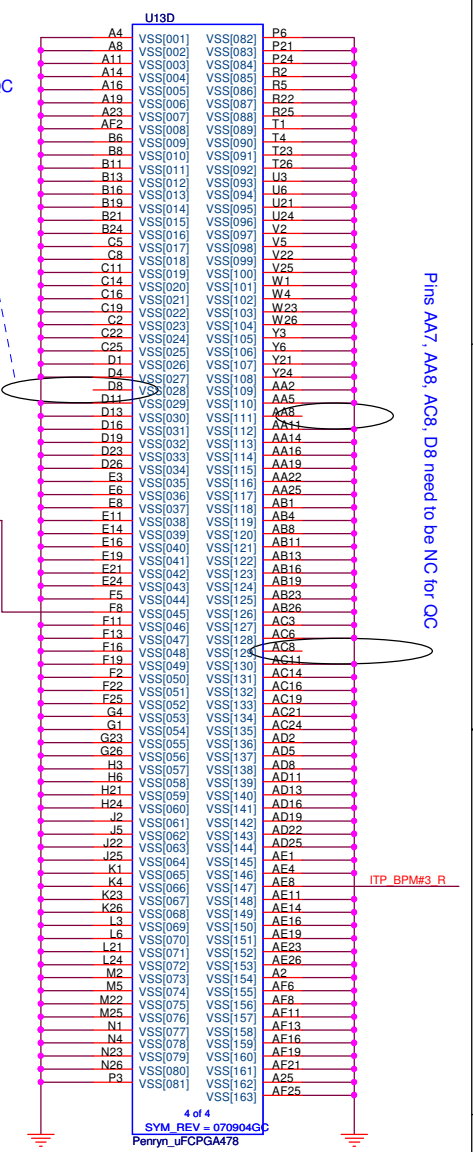
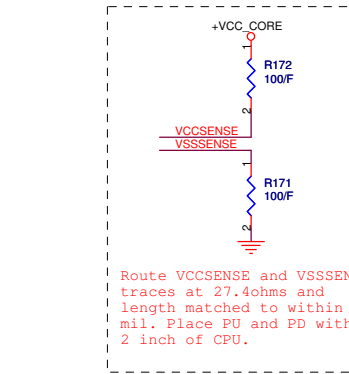
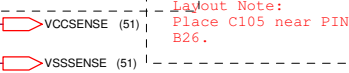
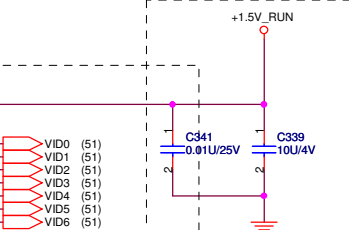
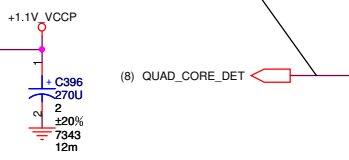


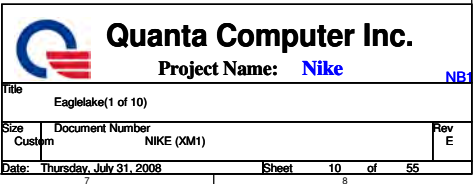
All use 22U 10V(+20%,X5R,1210)Pb-Free.

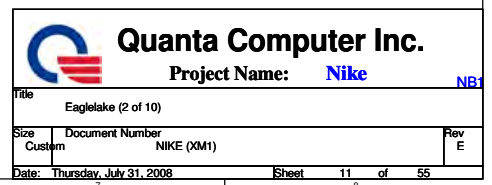


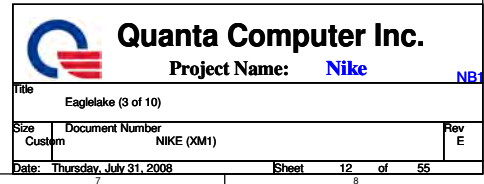
20080520 Intel update:
Penryn QC GTLREF_CONTROL pin.

| CPU | Pin F8 |
|-----------|------------------------------|
| Dual Core | GND |
| Quad Core | Internal pull 50 ohm to VCCP |

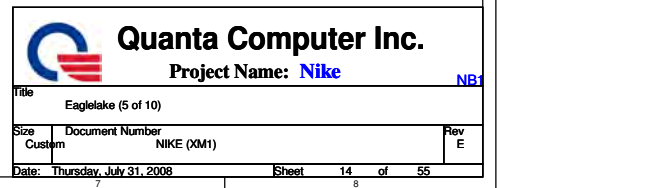


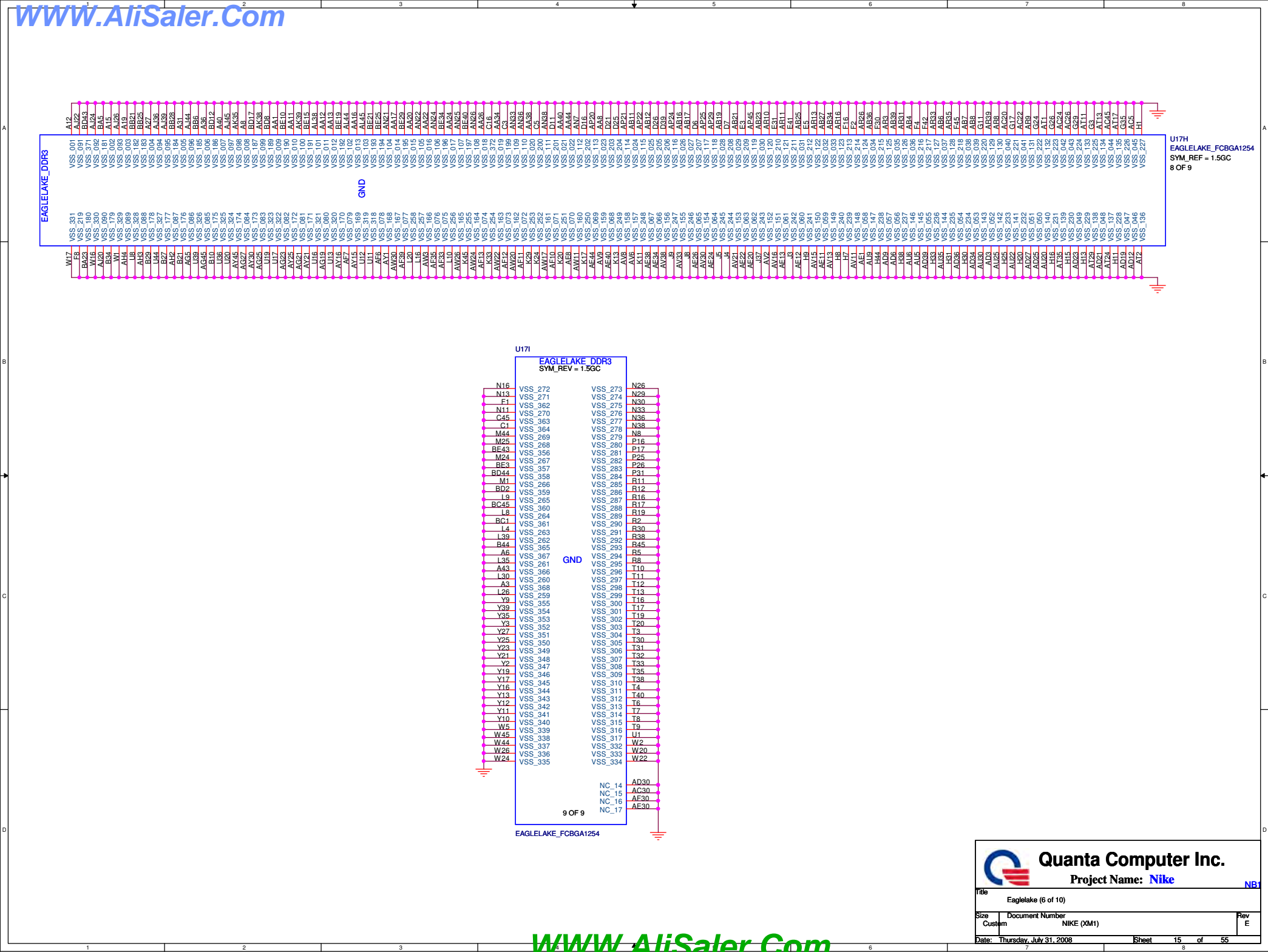















Quanta Computer Inc.

Project Name: Nike

Title

Eaglelake (6 of 10)

Size

Custom

Document Number

NIKE (XM1)

Rev

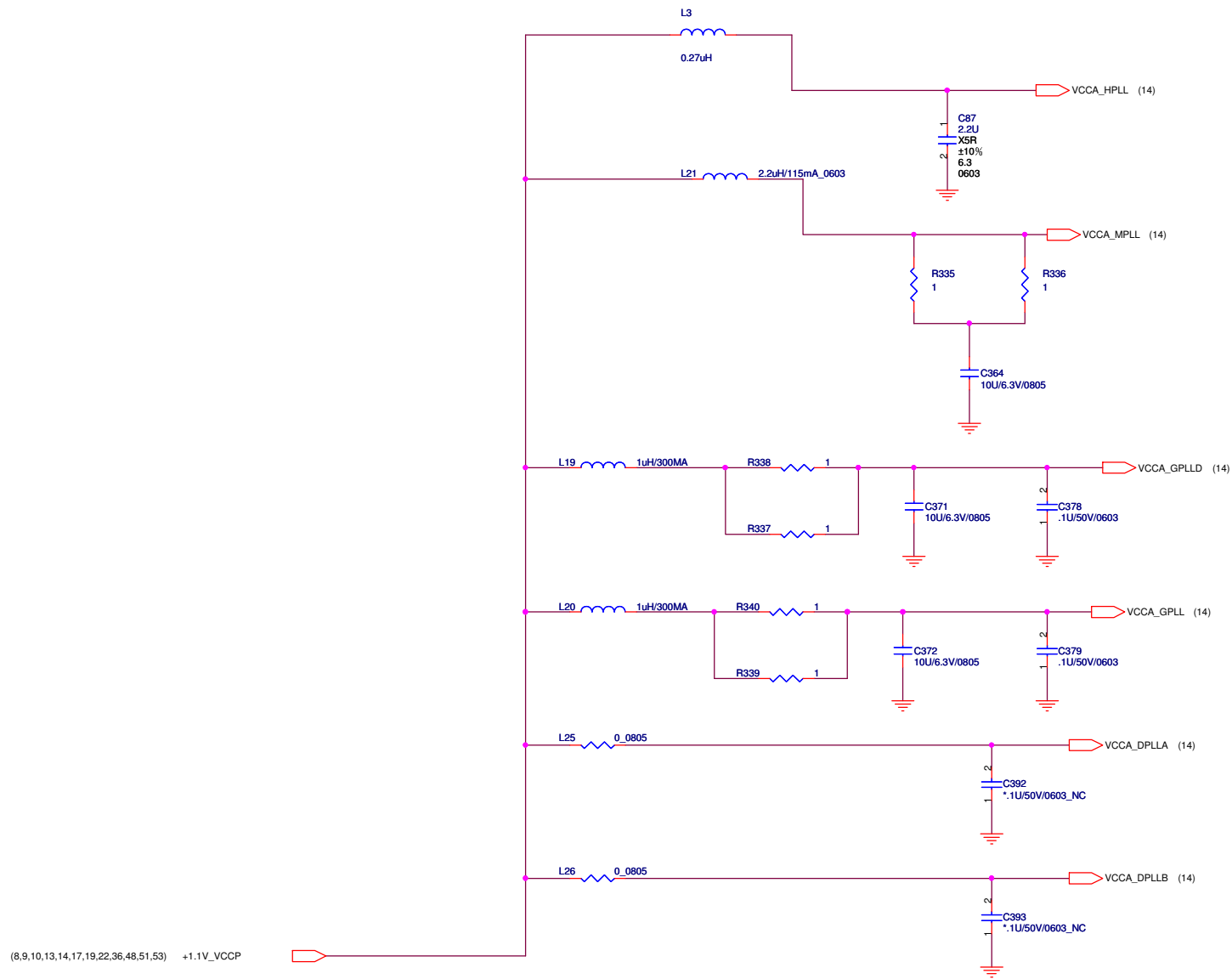
E


Date:

Thursday, July 31, 2008

Sheet

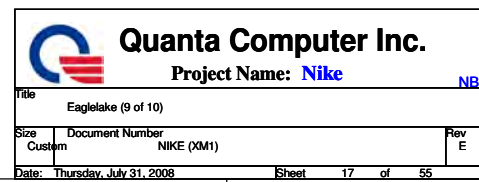
15 of 55

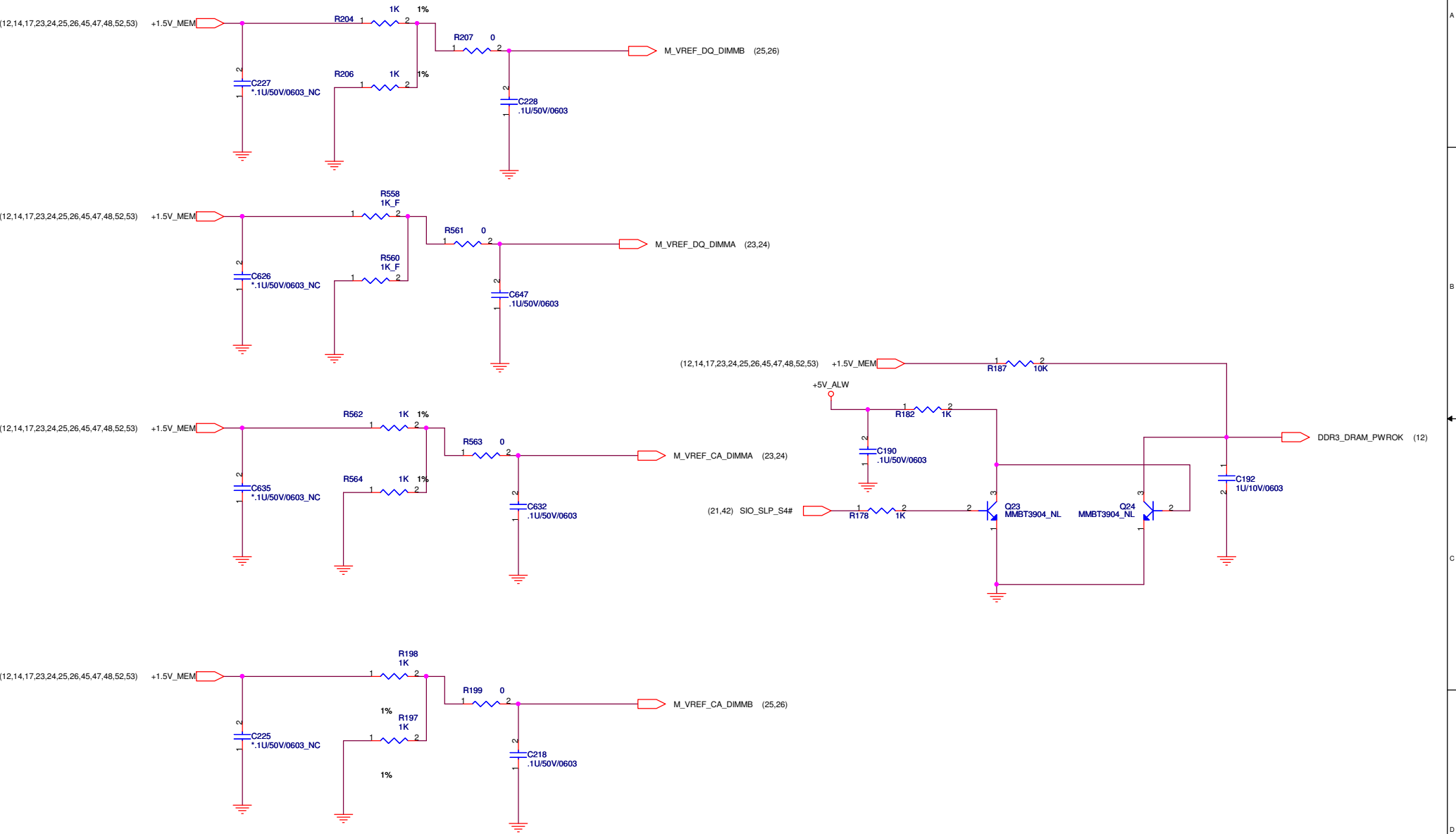





Quanta Computer Inc.
Project Name: **Nike**

| | | |
|-------------------------------|-------------------------------|----------------|
| Title Eaglelake (7 of 10) | | |
| Size Custom | Document Number NIKE (xM1) | Rev E |
| Date: Thursday, July 31, 2008 | | Sheet 16 of 55 |

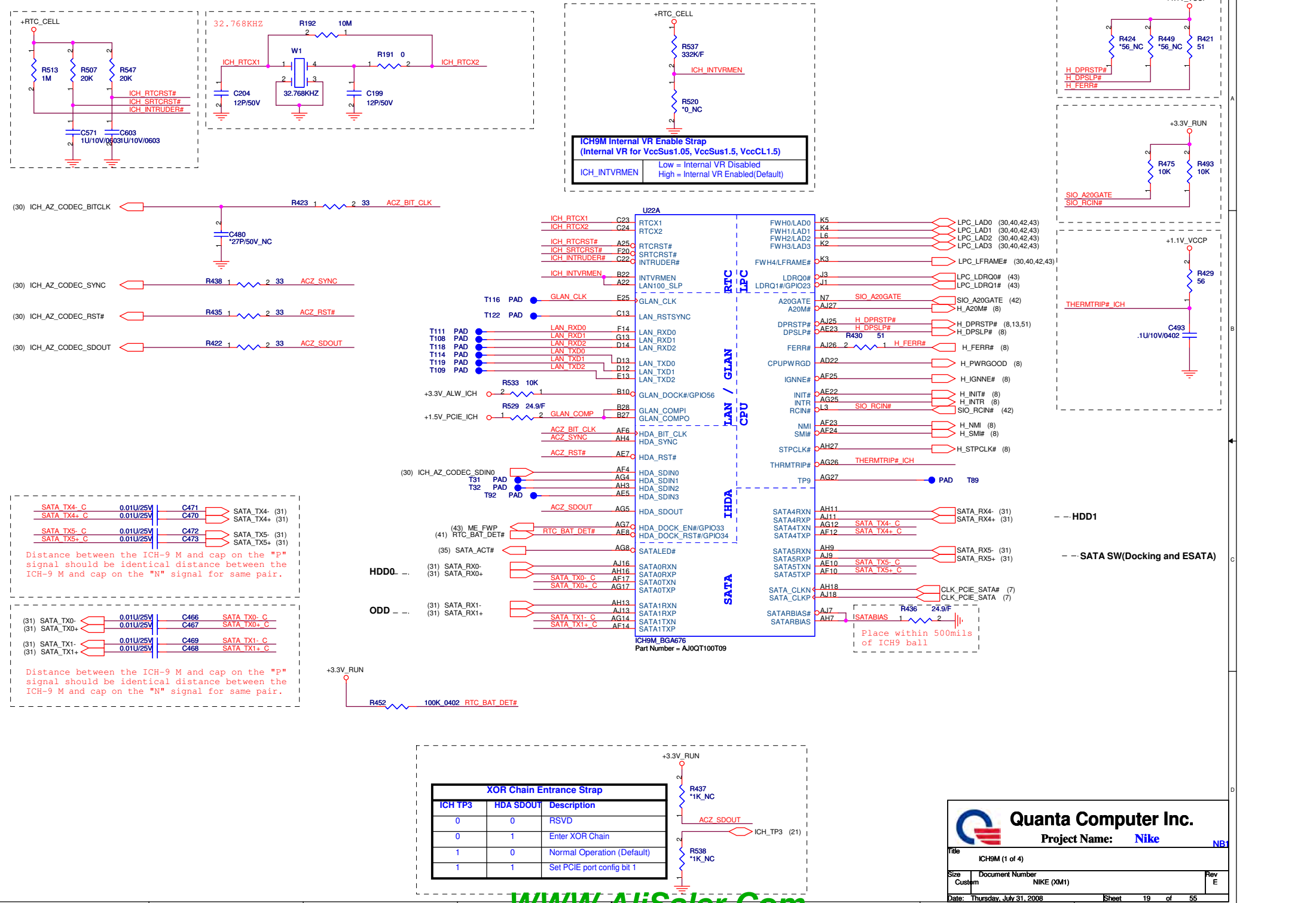




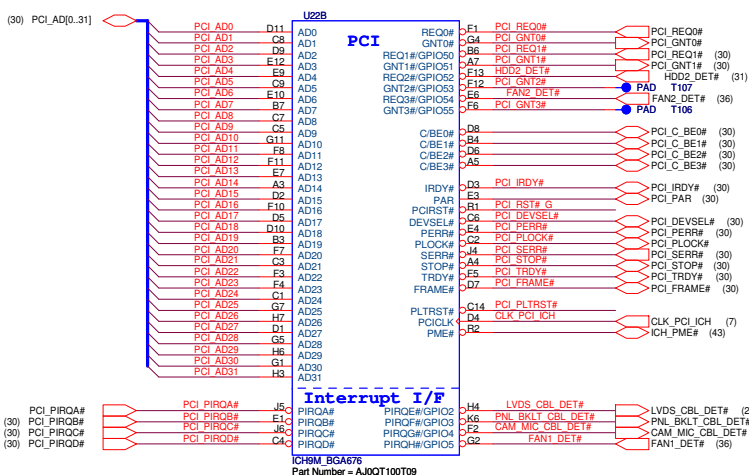
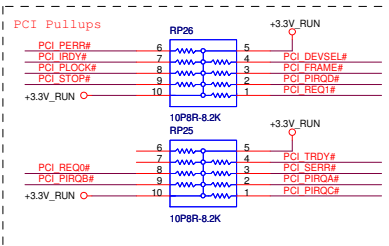
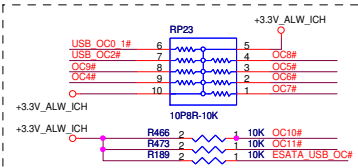


Quanta Computer Inc.
Project Name: **Nike**

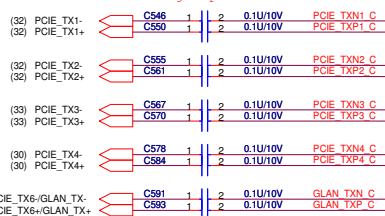
| | | |
|-------------------------------|-------------------------------|----------------|
| Title Eaglelake (10 of 10) | | |
| Size Custom | Document Number NIKE (XM1) | Rev E |
| Date: Thursday, July 31, 2008 | | Sheet 18 of 55 |



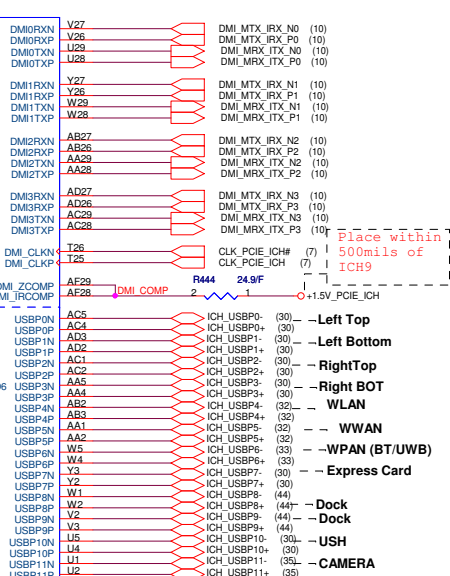
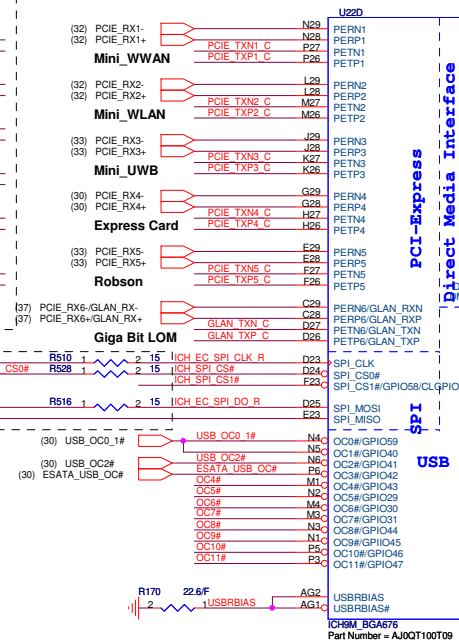
| | | | | | |
|----------------|------|---|---|-----------|----|
| OC6# | C559 | 1 | 2 | "0.1U/10V | NC |
| OC4# | C544 | 1 | 2 | "0.1U/10V | NC |
| OC5# | C554 | 1 | 2 | "0.1U/10V | NC |
| OC7# | C560 | 1 | 2 | "0.1U/10V | NC |
| OC8# | C553 | 1 | 2 | "0.1U/10V | NC |
| USB_OC2# | C545 | 1 | 2 | "0.1U/10V | NC |
| USB_OC0.1# | C552 | 1 | 2 | "0.1U/10V | NC |
| OC9# | C543 | 1 | 2 | "0.1U/10V | NC |
| OC10# | C534 | 1 | 2 | "0.1U/10V | NC |
| OC11# | C542 | 1 | 2 | "0.1U/10V | NC |
| ESATA_USB_OC1# | C197 | 1 | 2 | "0.1U/10V | NC |



Place TX DC blocking caps close ICH8.



Layout Note:
Place R528, R506 within
500 mils from ICH.



Non-IAMT

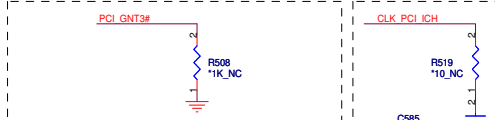
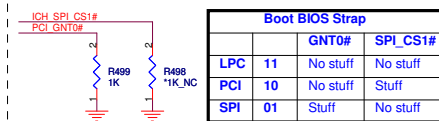
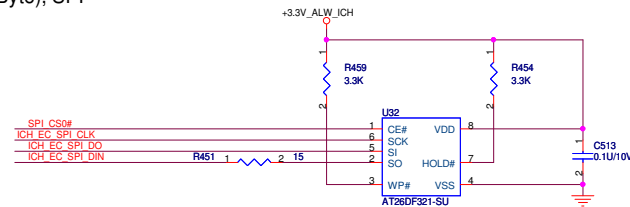
Add Buffers as needed for Loading and fanout concerns.

The diagrams show the following connections:

- Diagram 1:** PCI_RST# G (pin 1) and a 3.3V_ALW_ICH supply (pin 2) are connected to the inputs of buffer U20. The output (pin 4) is PCI_RST# (30,40).
- Diagram 2:** PCI_PLTRST# (pin 1) and a 3.3V_ALW_ICH supply (pin 2) are connected to the inputs of buffer U21. The output (pin 4) is PLTRST# (13,27,30).
- Diagram 3:** PCI_PLTRST# (pin 1) and a 3.3V_ALW_ICH supply (pin 2) are connected to the inputs of buffer U1. The output (pin 4) is PLTRST1# (37,42,43).
- Diagram 4:** PCI_PLTRST# (pin 1) and a 3.3V_ALW_ICH supply (pin 2) are connected to the inputs of buffer U12. The output (pin 4) is PLTRST2# (32,33).

PLTRST# for MCH, Express card, USH, Gfx.
PLTRST1# for 5035, 5028, 5761E.
PLTRST2# for WWAN/WLAN/WPAN/Robson.

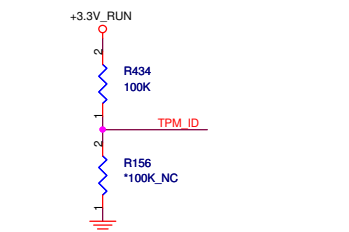
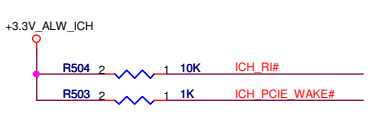
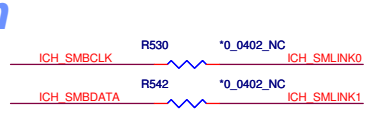
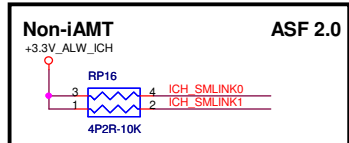
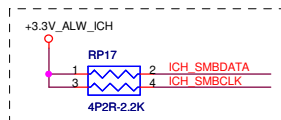
32Mbit (4M Byte), SPI



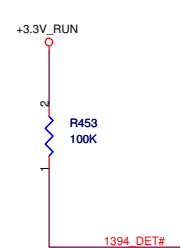
| | |
|---------------------------------|---|
| A16 away override strap. | |
| PCI_GNT3# | Low = A16 swap override enabled. High = Default. |

| | | | |
|------------------------------------|------|------|----------------|
| DOCK | REQ0 | GNT0 | PIRQA |
| Cardbus or Cardbus/1394 | REQ1 | GNT1 | PIRQD |
| 1394/MediaCard | REQ2 | GNT2 | PIRQC PIROD |

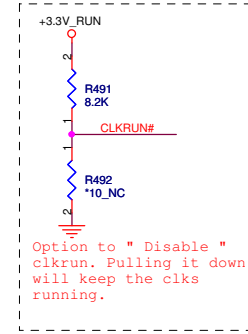
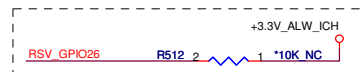
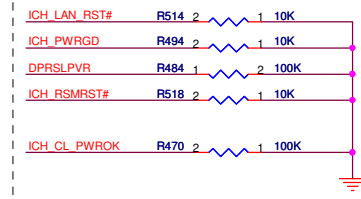
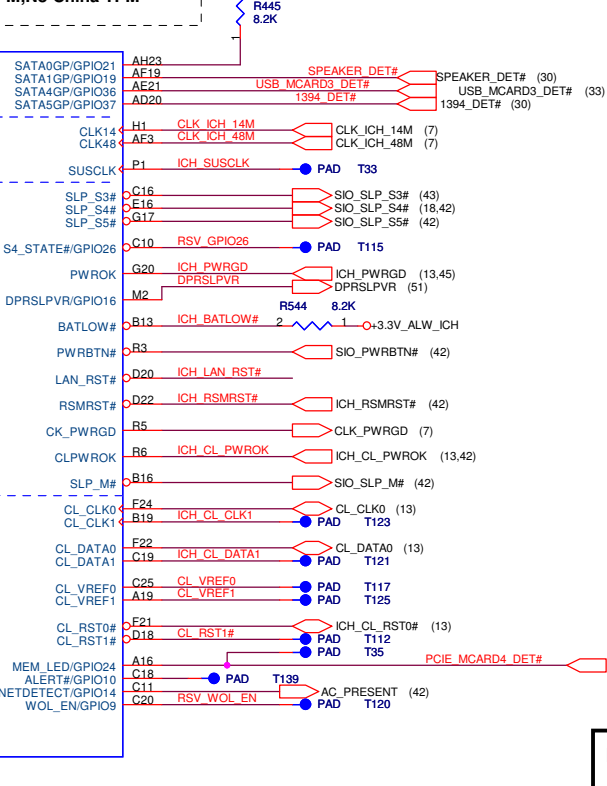
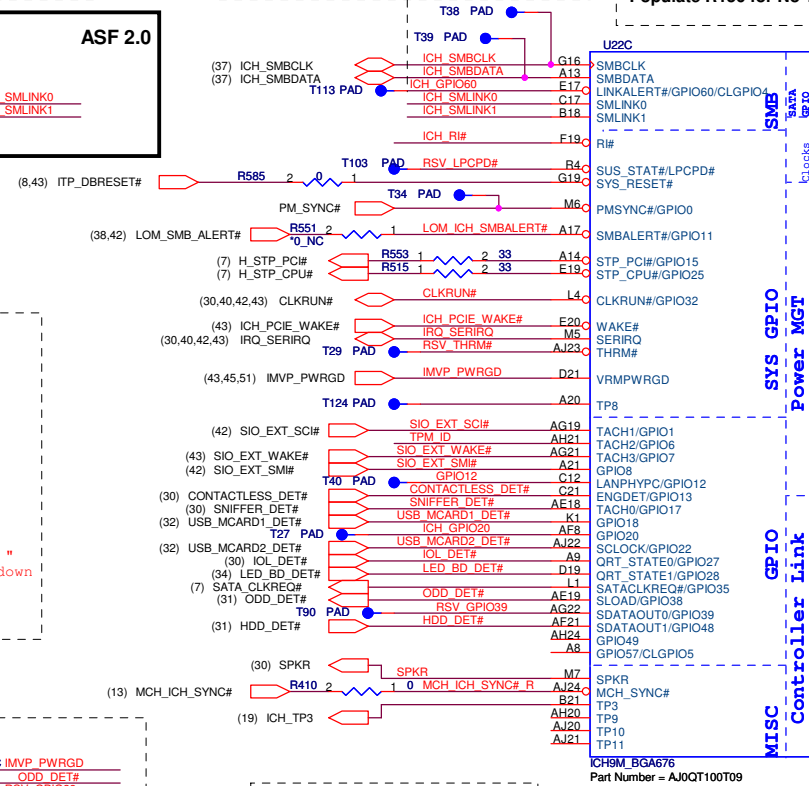
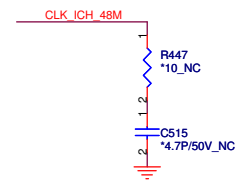
Reserved for
EMI. Place
resistor and cap
close to ICH.



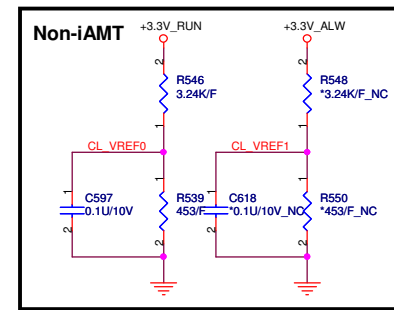
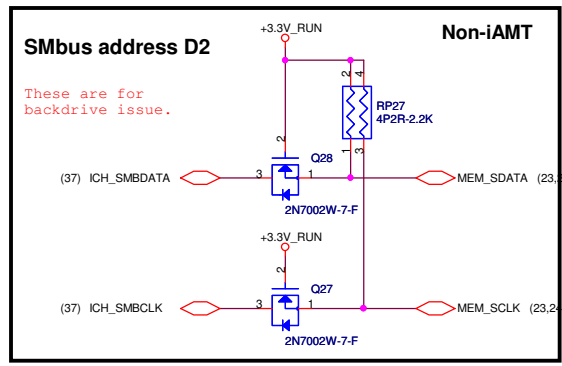
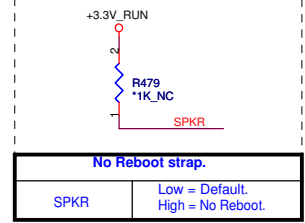
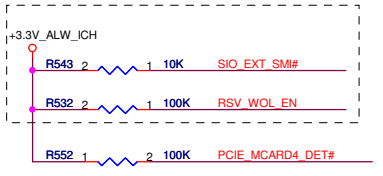
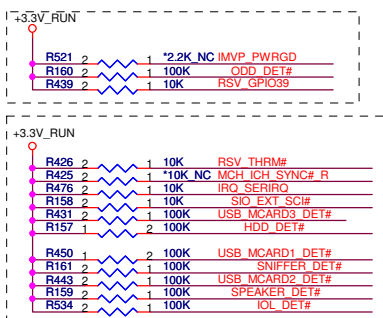
Populate R434 for USH TPM
Populate R156 for No TPM, No China TPM



Place these close to ICH9.

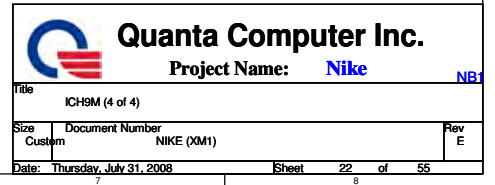


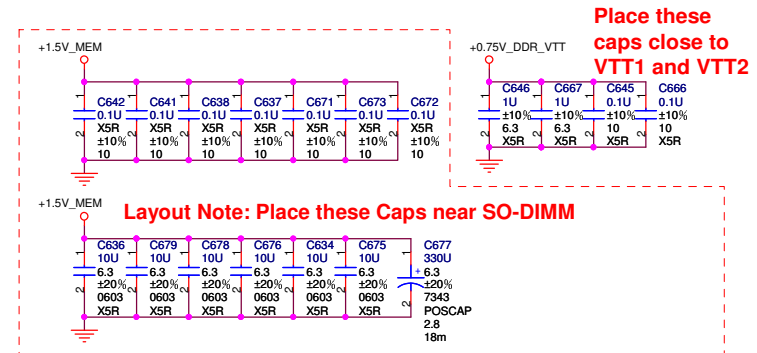
Option to "Disable" clkrun. Pulling it down will keep the clks running.




Quanta Computer Inc.
Project Name: Nike

| | | |
|-------------------------------|-----------------------------|--------|
| Title: ICH9M (3 of 4) | | Rev: E |
| Size: Custom | Document Number: NIKE (XM1) | |
| Date: Thursday, July 31, 2008 | Sheet: 21 of 55 | |

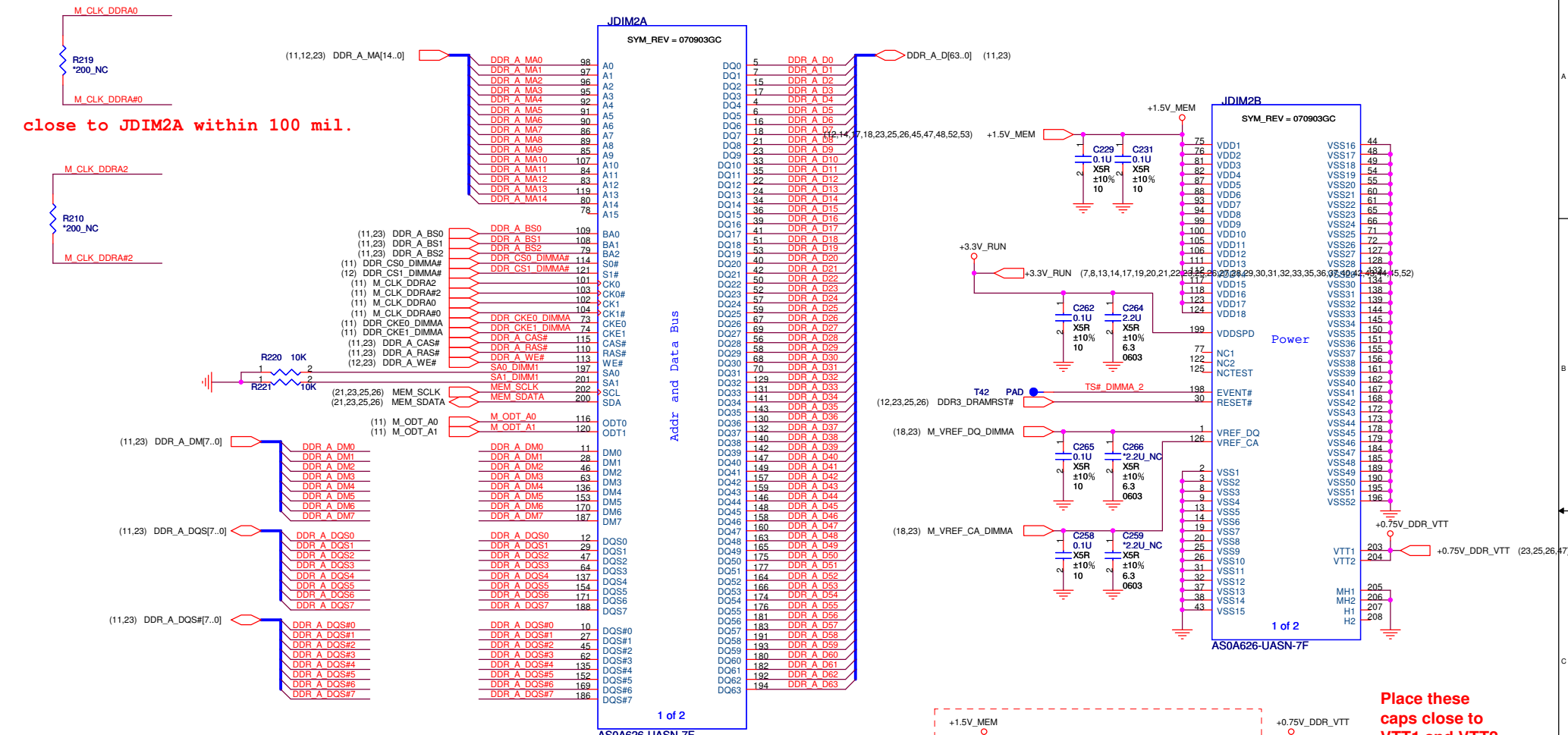




| | SA1 | SA0 | Note |
|------|-----|-----|------------------------|
| CHA0 | 0 | 0 | |
| CHA1 | 0 | 1 | Pull-High to +3.3V_RUN |
| CHB0 | 1 | 0 | |
| CHB1 | 1 | 1 | |

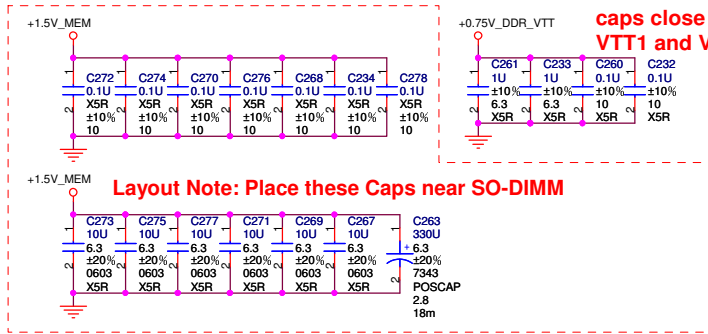
| | | | |
|---|--|-----------------|----------|
|  <div> <h1>Quanta Computer Inc.</h1> <p>Project Name: Nike</p> </div> | | NR | |
| Title | | | |
| DDR3 Channel A0 (1 of 5) | | | |
| Size | | Document Number | |
| Custom | | NIKE (XM1) | |
| Date: Thursday, July 31, 2008 | | Sheet | 23 of 55 |
| | | Rev | E |

CHA_DIMM0_TOP Layer



Select the Serial Presence Detect and Temp sensor base address.

| | SA1 | SA0 | Note |
|------|-----|-----|------------------------|
| CHA0 | 0 | 0 | |
| CHA1 | 0 | 1 | Pull-High to +3.3V_RUN |
| CHB0 | 1 | 0 | |
| CHB1 | 1 | 1 | |



Quanta Computer Inc.
Project Name: Nike

Title: DDR3 Channel A1 (2 of 5)

| | | |
|--------------|-----------------------------|--------|
| Size: Custom | Document Number: NIKE (XM1) | Rev: E |
|--------------|-----------------------------|--------|

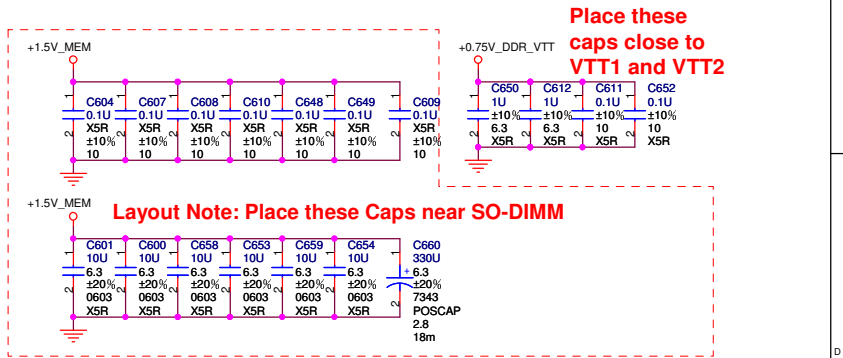
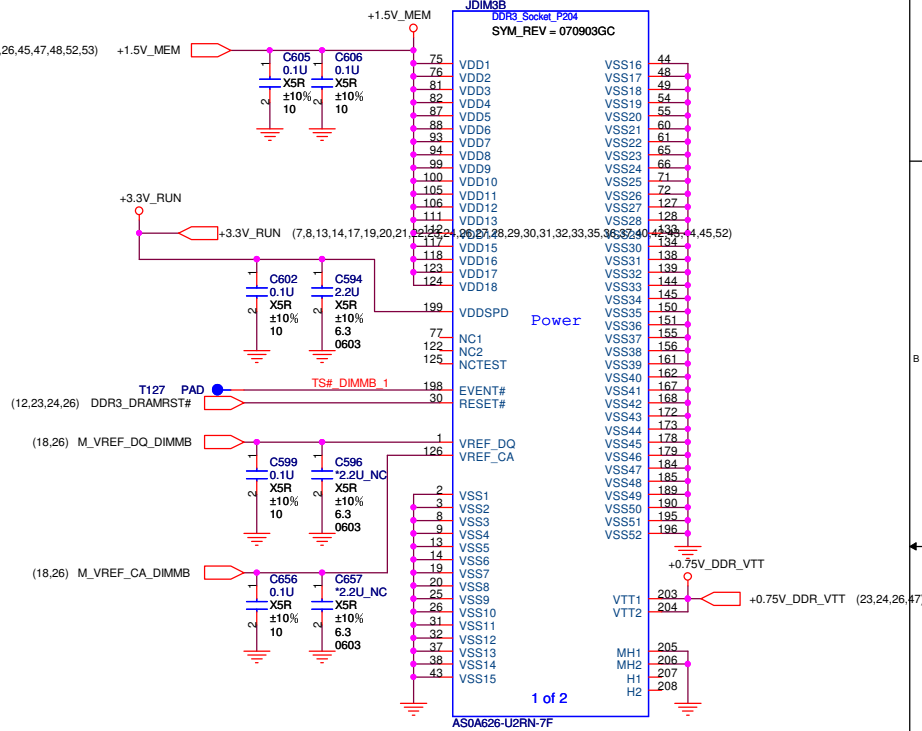
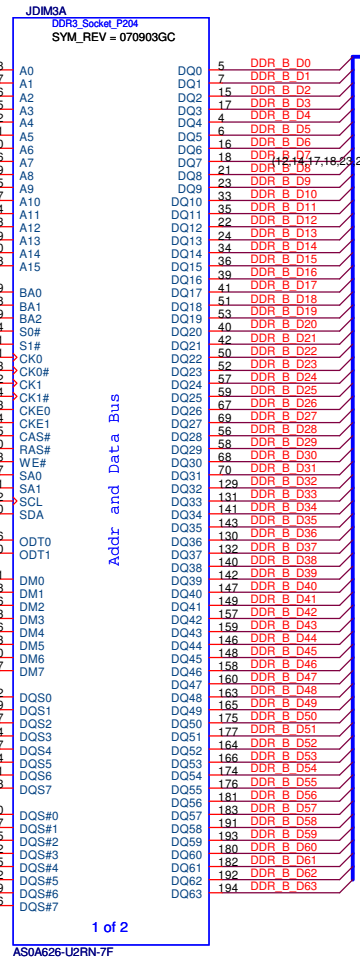
Date: Thursday, July 31, 2008 Sheet 24 of 55


close to JDIM4A within 100 mil.

close to JDIM4A within 100 mil.

Select the Serial Presence Detect and Temp sensor base address.

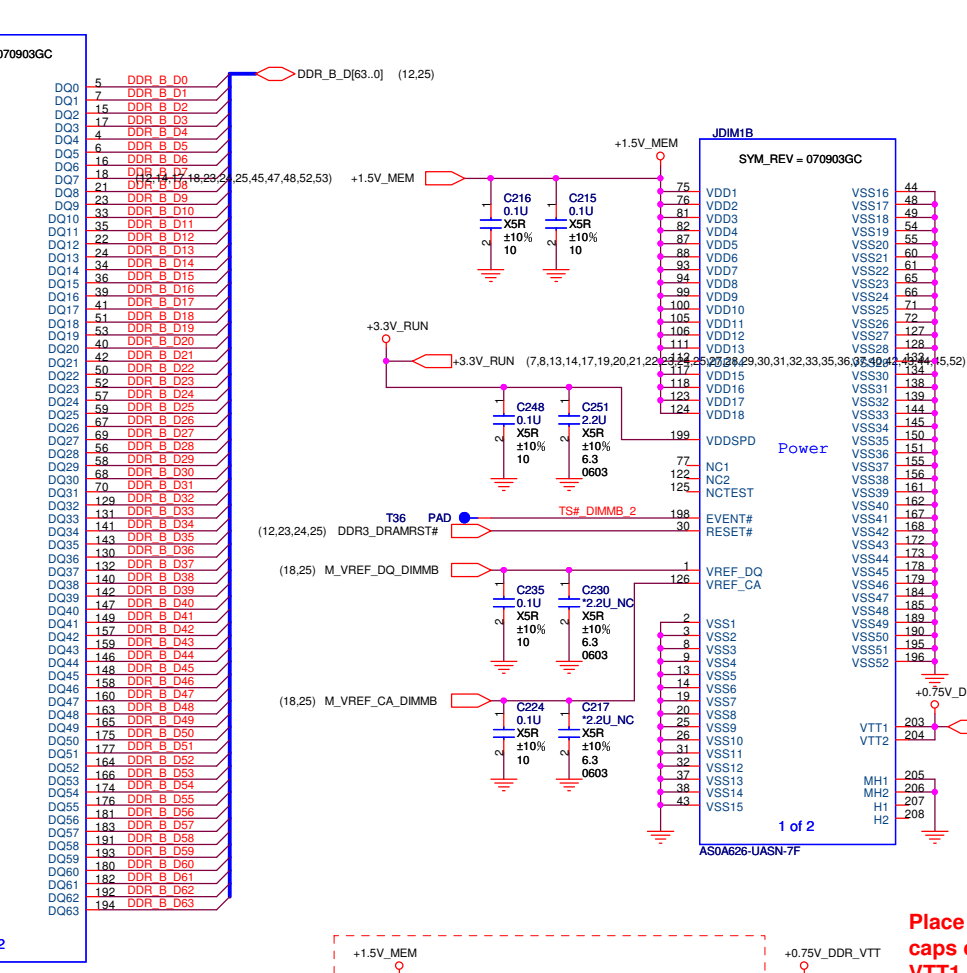
| | SA1 | SA0 | Note |
|------|-----|-----|------------------------|
| CHA0 | 0 | 0 | |
| CHA1 | 0 | 1 | Pull-High to +3.3V_RUN |
| CHB0 | 1 | 0 | |
| CHB1 | 1 | 1 | |



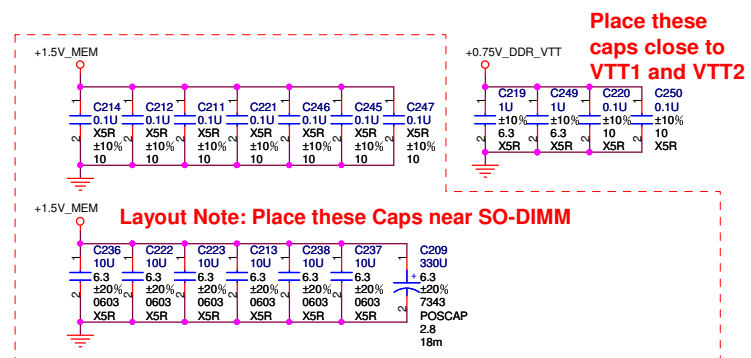



Quanta Computer Inc.
Project Name: **Nike**

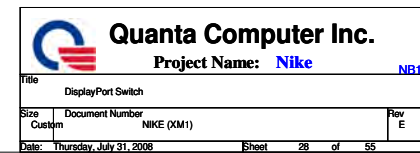
| | | |
|---------------------------------|-----------------------------|--------|
| Title: DDR3 Channel A0 (3 of 5) | | |
| Size: Custom | Document Number: NIKE (XM1) | Rev: E |
| Date: Thursday, July 31, 2008 | Sheet: 25 | of 55 |

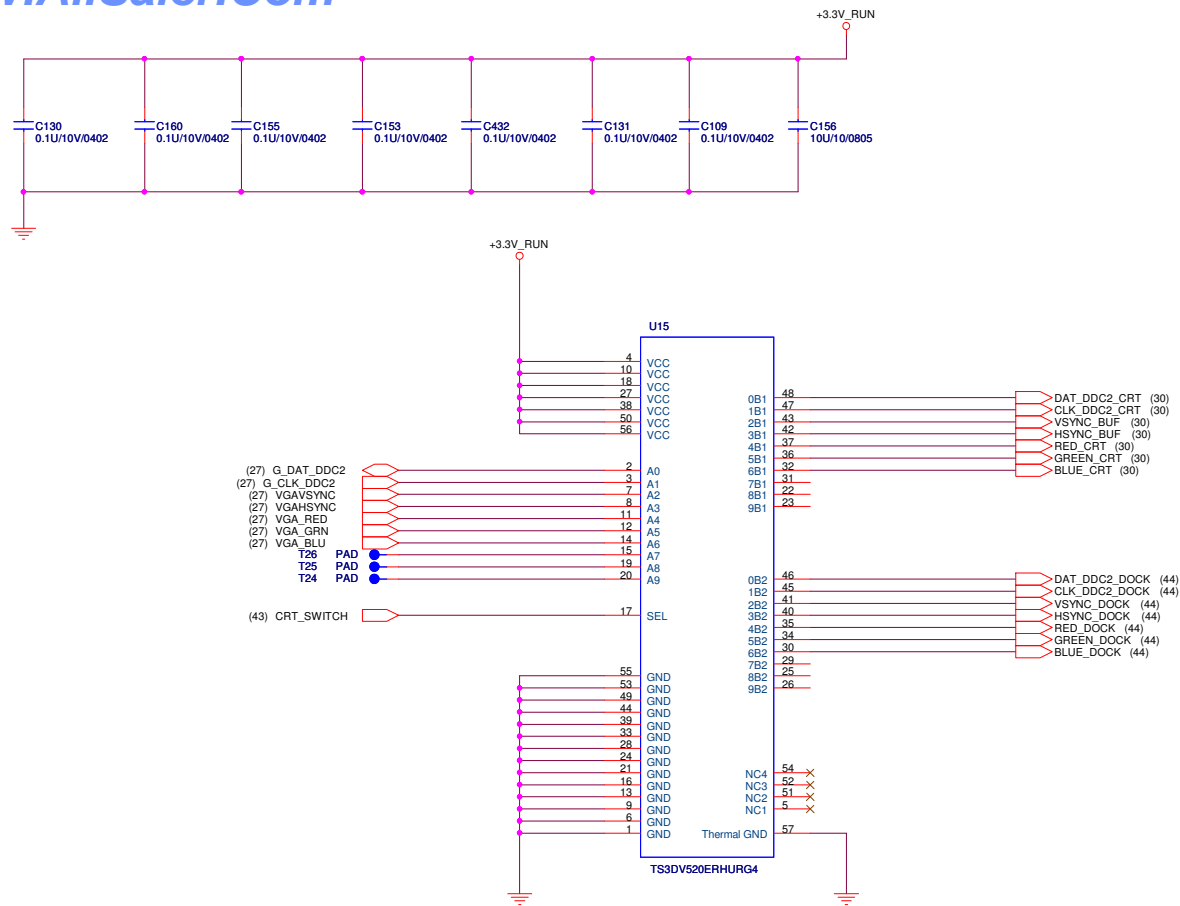


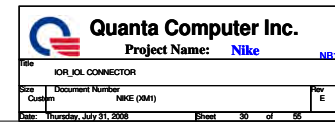
| | SA1 | SA0 | Note |
|------|-----|-----|------------------------|
| CHA0 | 0 | 0 | |
| CHA1 | 0 | 1 | Pull-High to +3.3V_RUN |
| CHB0 | 1 | 0 | |
| CHB1 | 1 | 1 | |




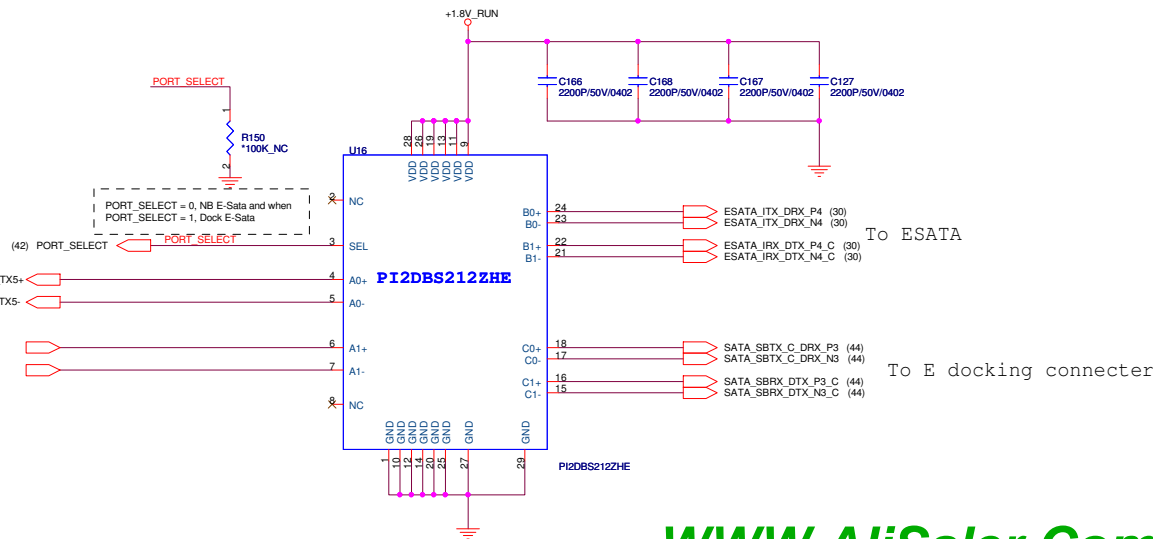
| | | | |
|--|--|--|-----------------------------|
|  <div> <h1>Quanta Computer Inc.</h1> <h2>Project Name: Nike</h2> </div> | | <div> <div>NR</div> <div>NR</div> </div> | |
| <div>Title</div> <div>DDR3 Channel A0 (4 of 5)</div> | | | |
| <div>Size</div> <div>Custom</div> | <div>Document Number</div> <div>NIKE (XM1)</div> | | <div>Rev</div> <div>E</div> |
| <div>Date: Thursday, July 31, 2008</div> | | <div>Sheet</div> <div>26</div> | <div>of</div> <div>55</div> |



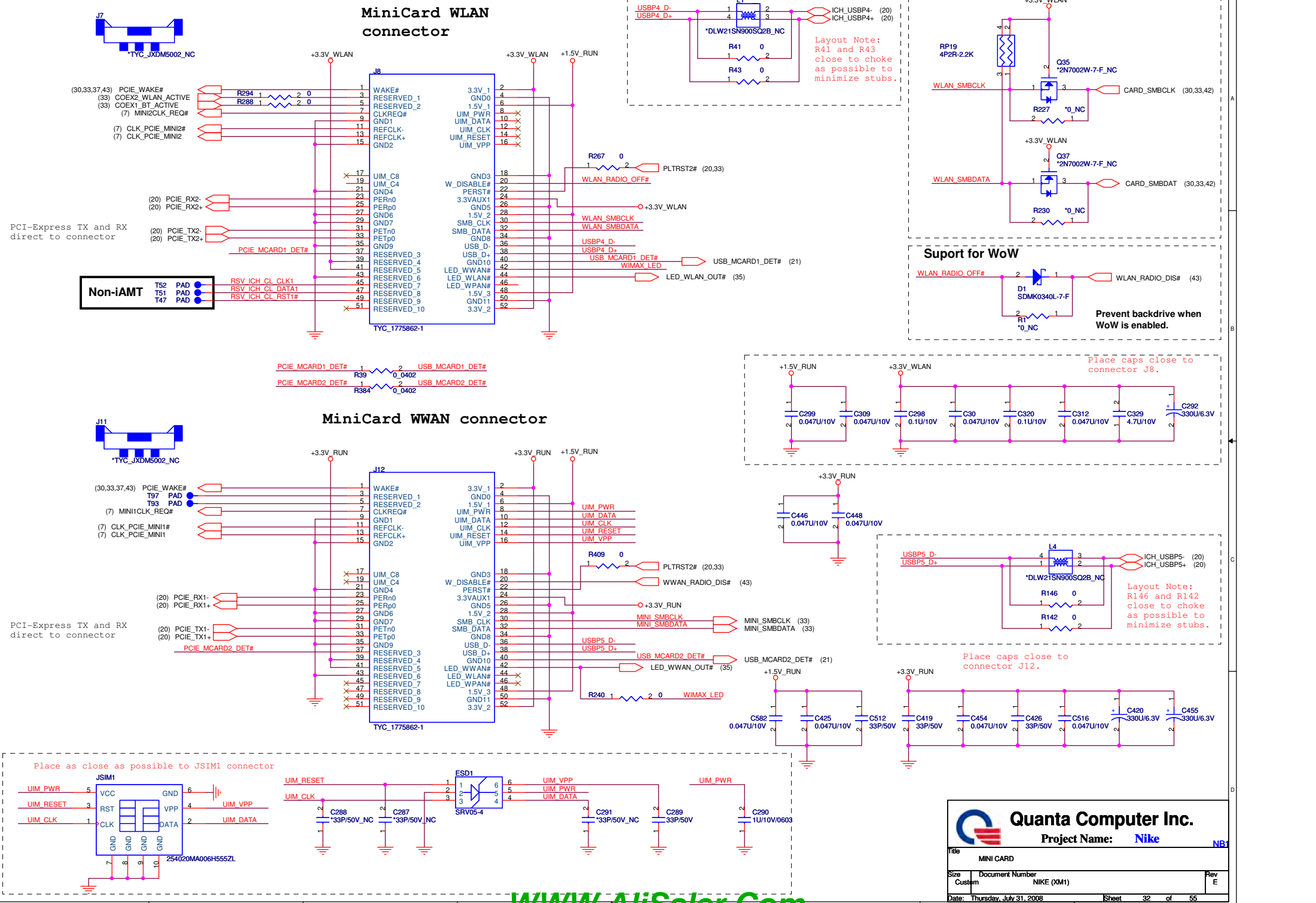


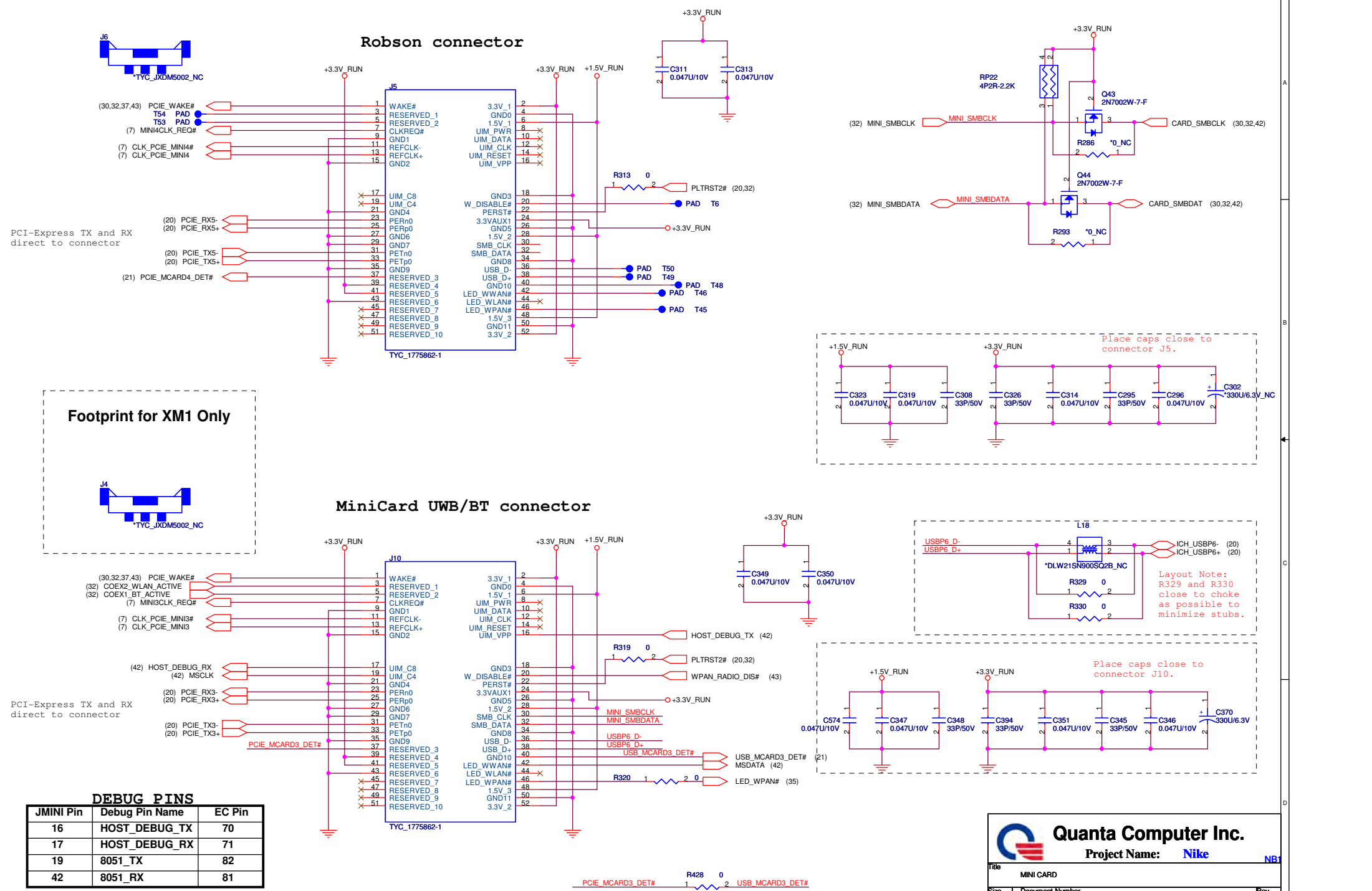



| | |
|---|------------------------------------|
|  <h1>Quanta Computer Inc.</h1> | |
| <p>Project Name: Nike</p> | |
| <p>Title: SATA (HDD_ODD) eSATA SWITCH</p> | |
| <p>Size: Custom</p> | <p>Document Number: NIKE (XM1)</p> |
| <p>Date: Thursday, July 31, 2008</p> | <p>Sheet 31 of 55</p> |
| <p>Rev: E</p> | |



To E docking connector

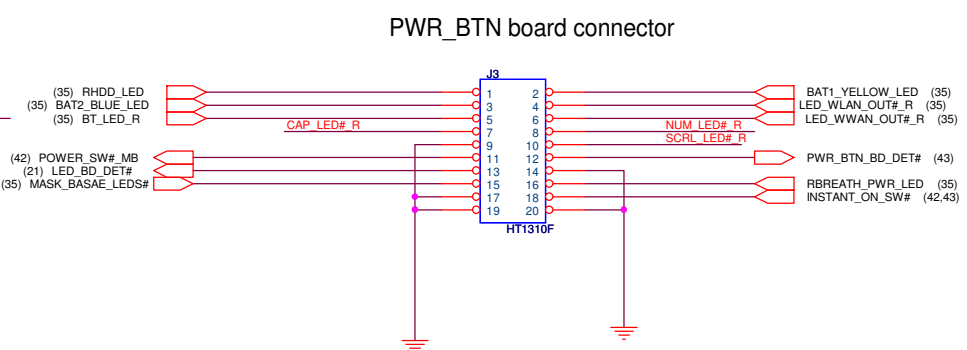
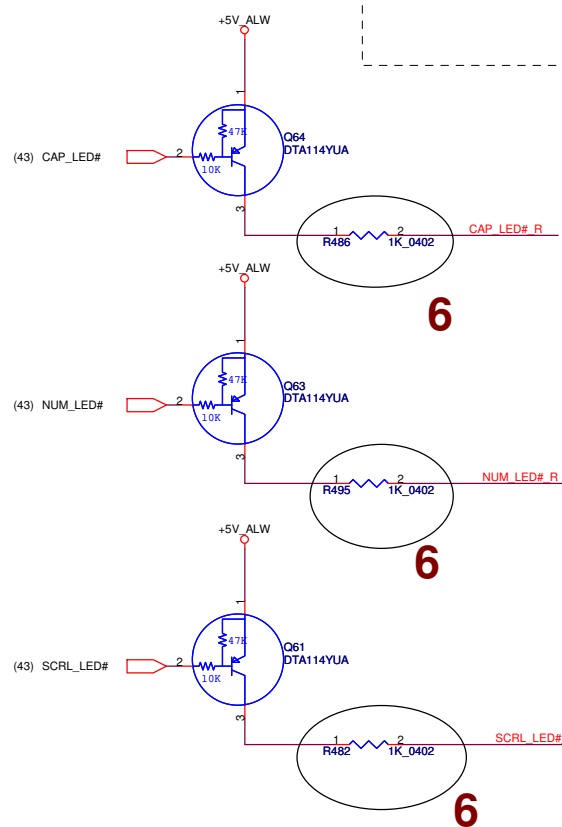
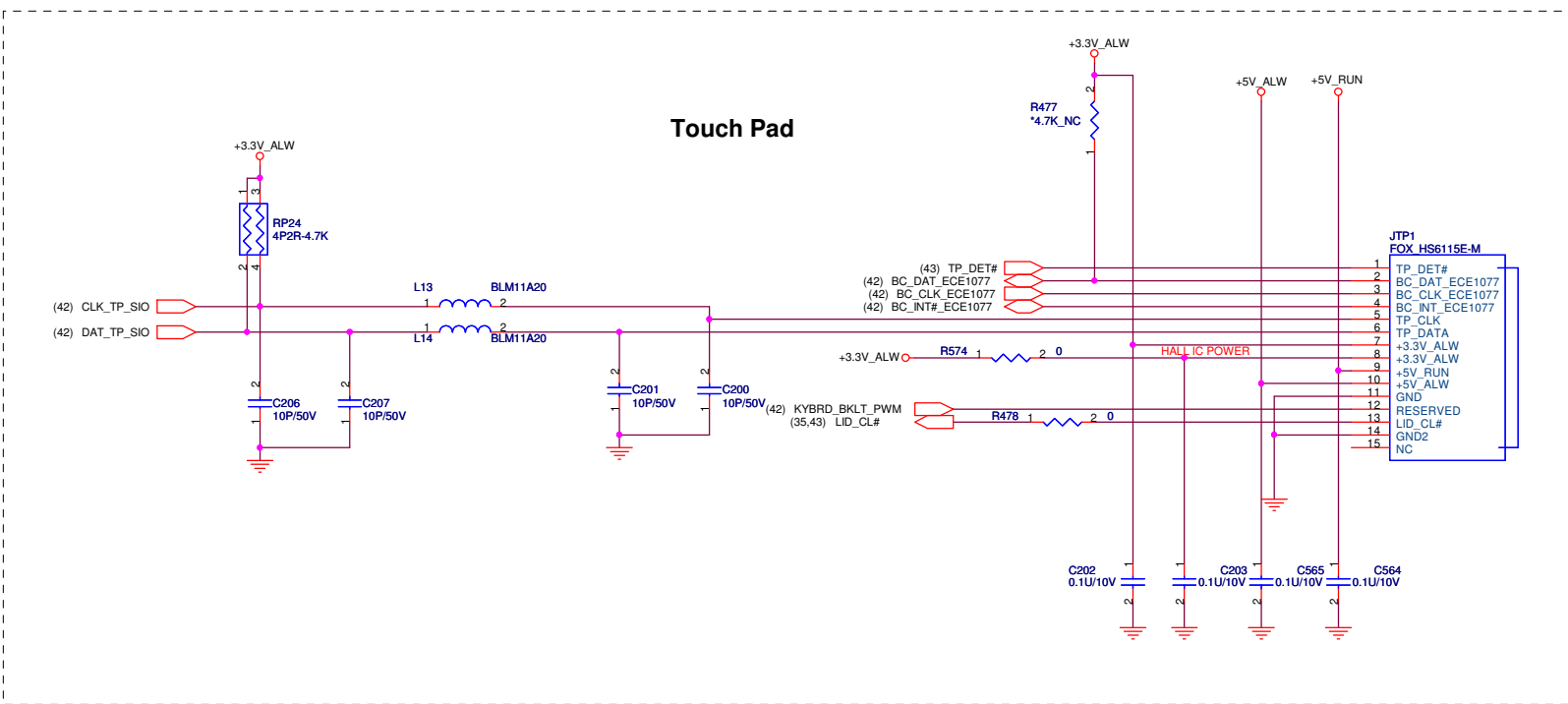






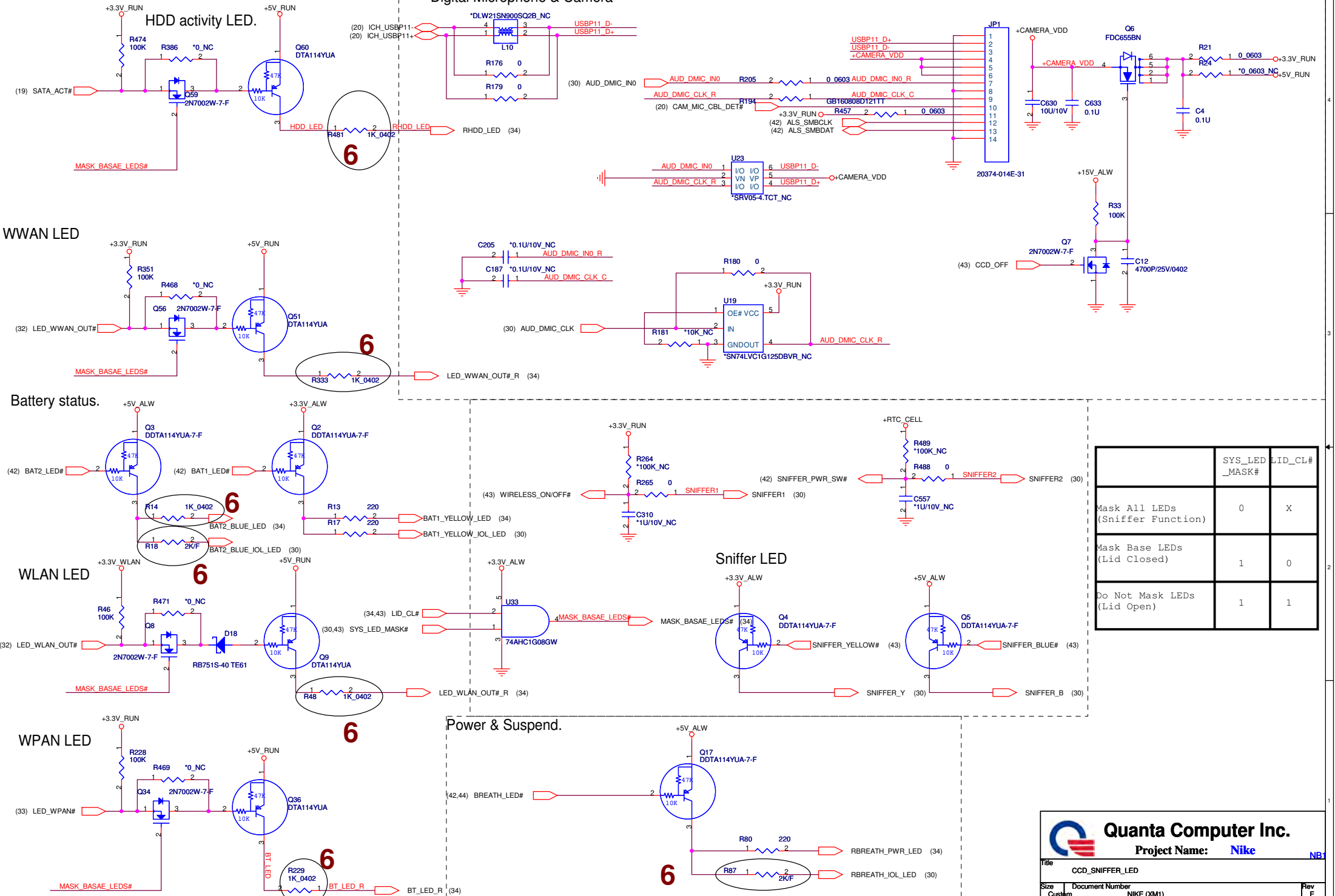
Quanta Computer Inc.
Project Name: **Nike**

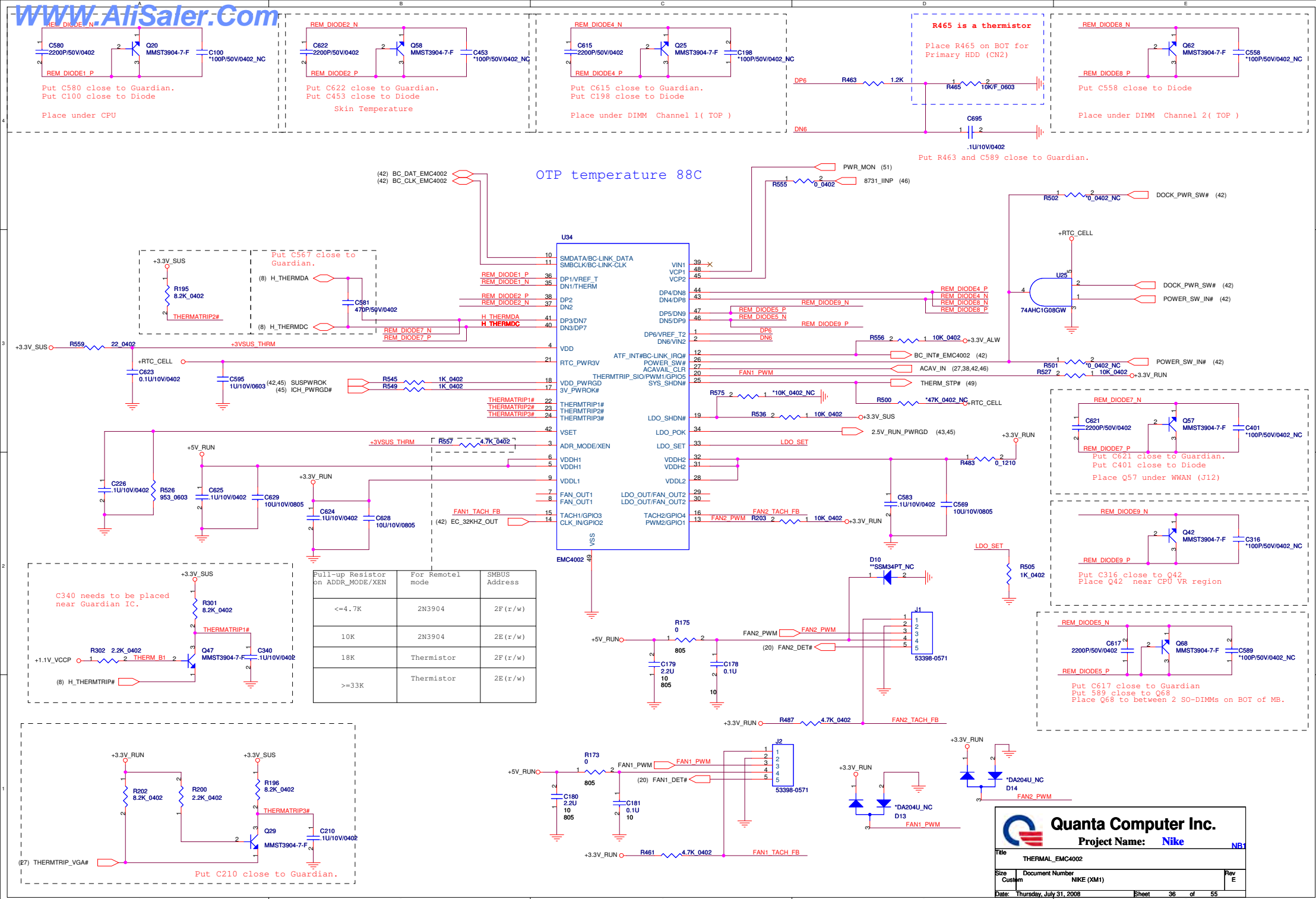
| | | |
|-------------------------------|-------------------------------|----------------|
| Title MINI CARD | | |
| Size Custom | Document Number NIKE (XM1) | Rev E |
| Date: Thursday, July 31, 2008 | | Sheet 33 of 55 |

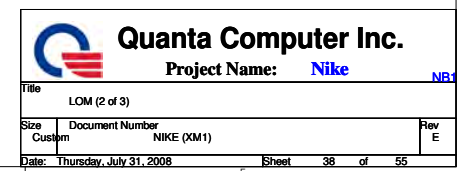


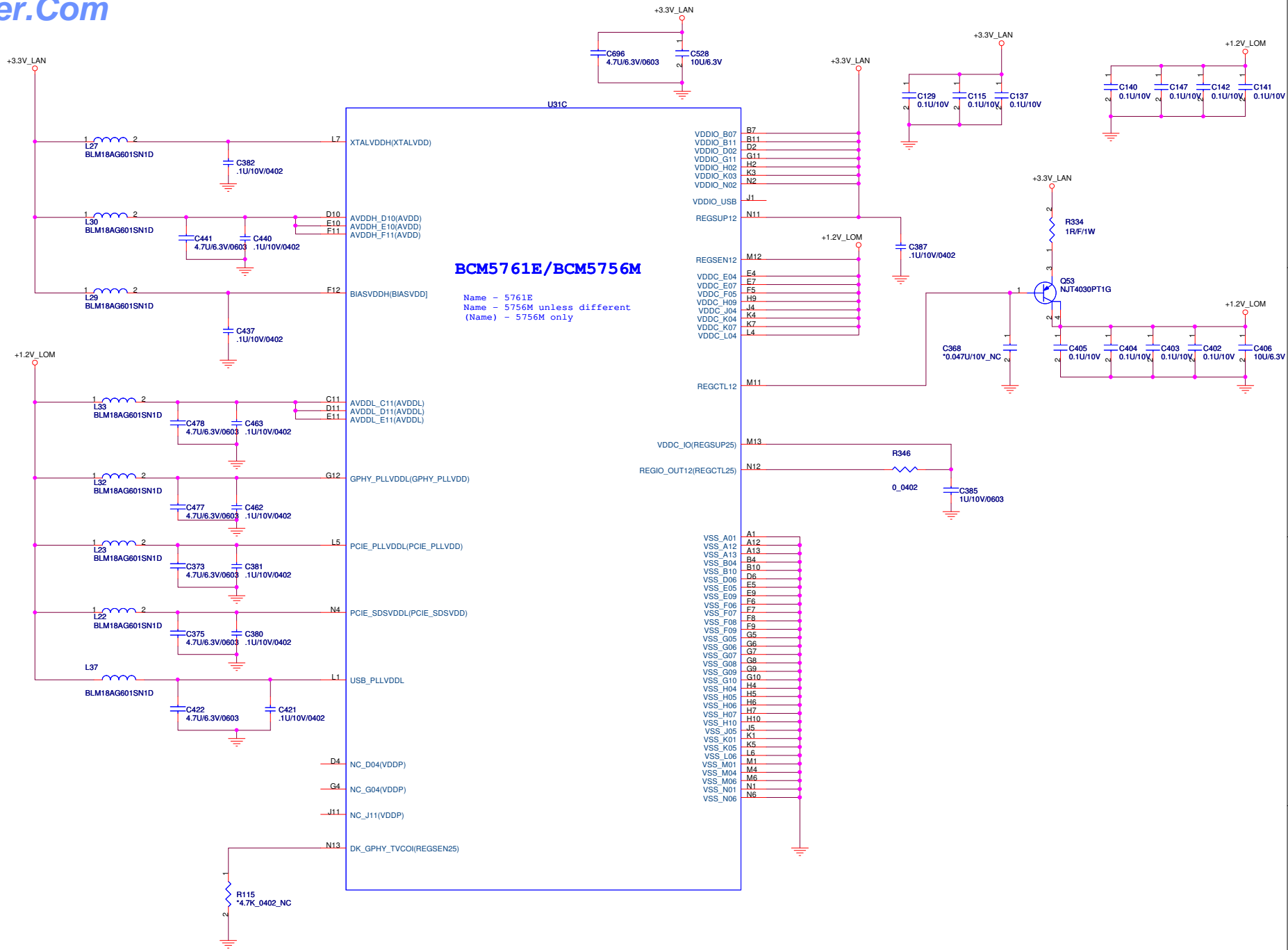
Quanta Computer Inc.
Project Name: **Nike**

| | | |
|--------|-------------------------|----------------|
| Title | | TP_PWR_BUTTON |
| Size | Document Number | NIKE (xM1) |
| Custom | | Rev E |
| Date: | Thursday, July 31, 2008 | Sheet 34 of 55 |









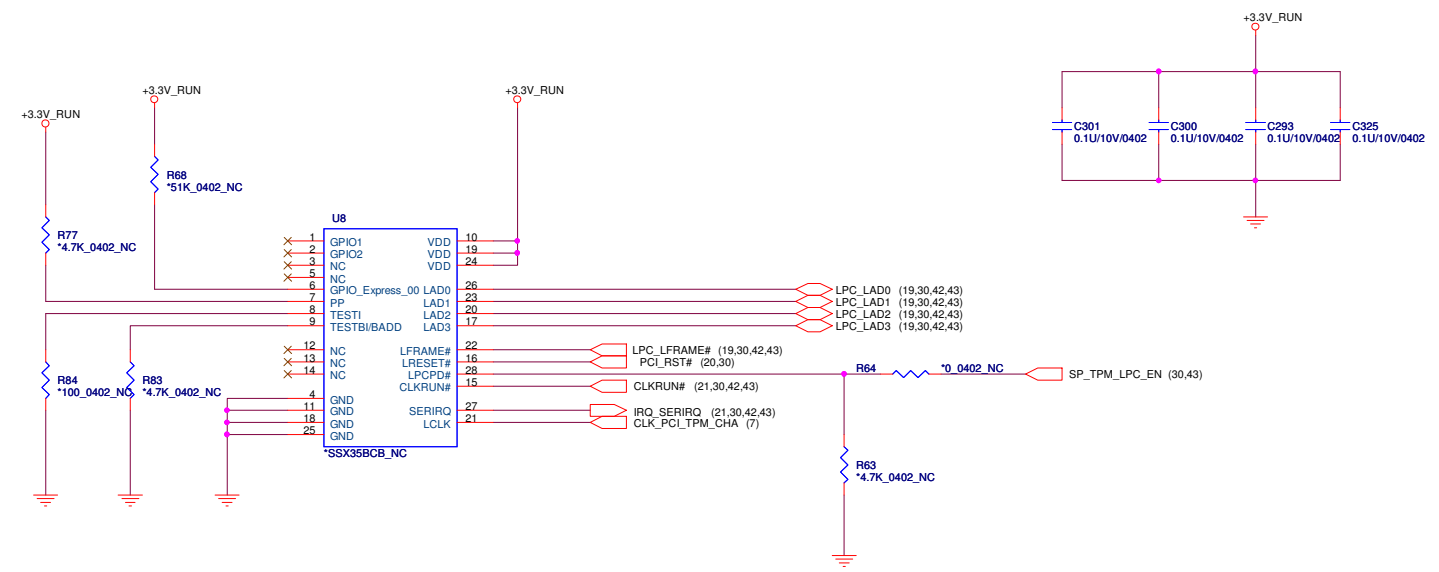



Table1

| BOM option scheme for USH TPM vs China TPM | | | | |
|--|--------------------|--------|--------|--|
| | | C0 USH | No TPM | |
| MB | MB, U8 | NC | NC | |
| | MB, R27 | NC | NC | |
| | MB, R63 | NC | NC | |
| | MB, R64 | NC | NC | |
| | R77, R68, R84, R83 | NC | NC | |
| | MB, R149 | POP | POP | |
| | MB, R151 | NC | NC | |
| | MB, R156 | NC | POP | |
| | MB, R434 | POP | NC | |



Quanta Computer Inc.

Project Name: Nike

MB

Title

TPM for CHINA

Size

Custom

Document Number

NIKE (XM1)

Rev

E

Date:

Thursday, July 31, 2008

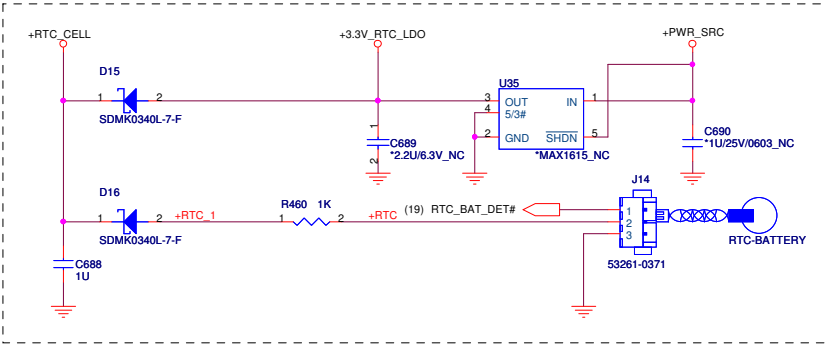
Sheet

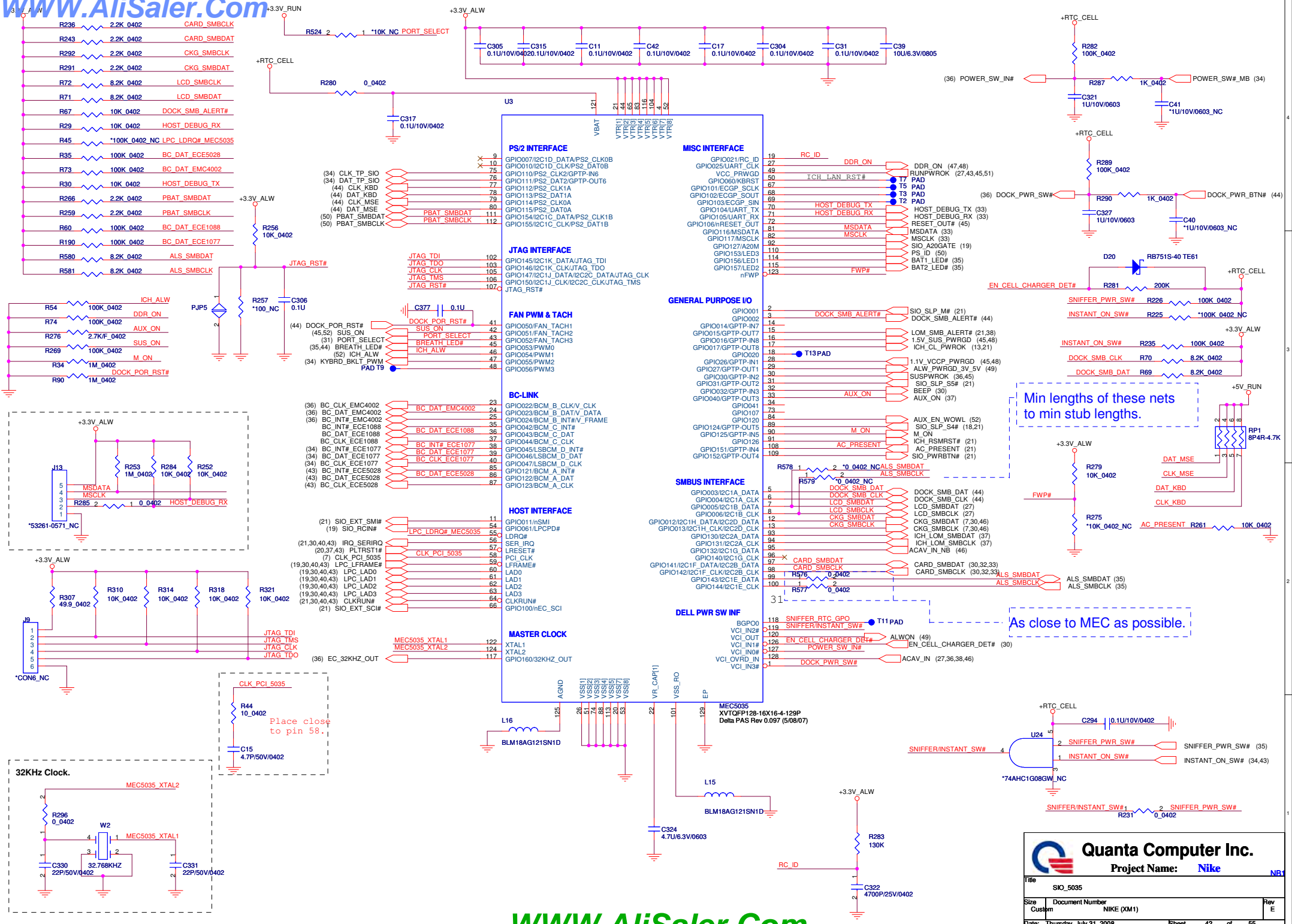
40


of

55

RTC BATTERY





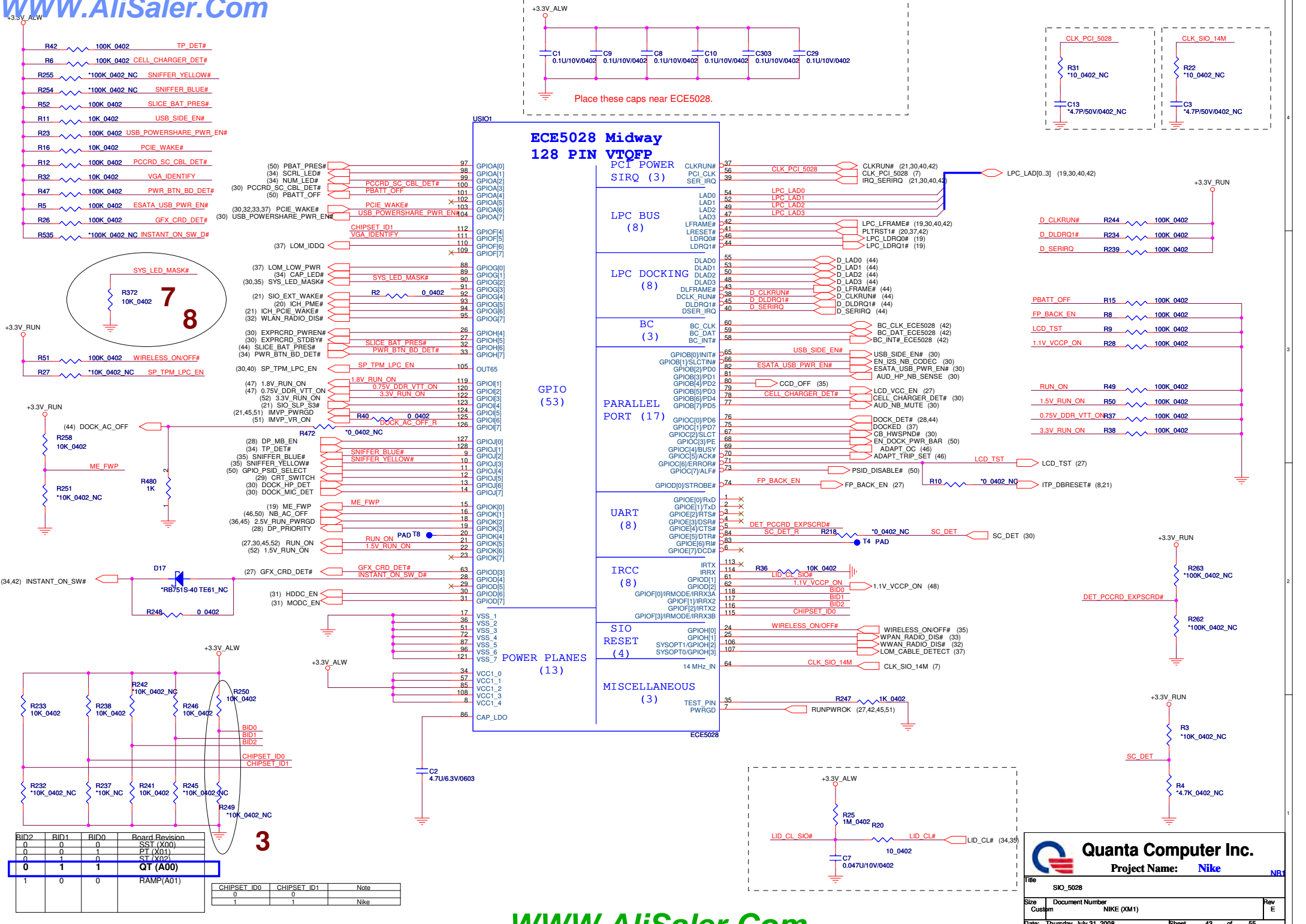


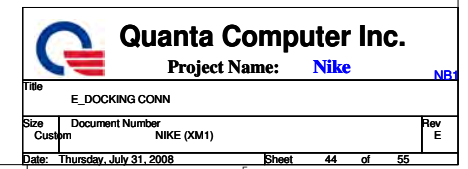
Quanta Computer Inc.

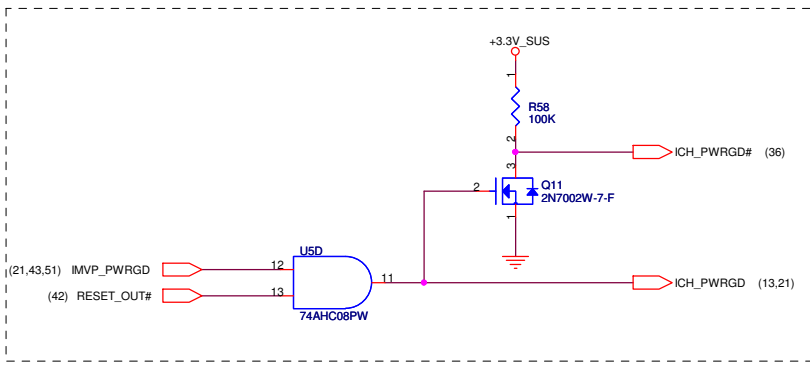
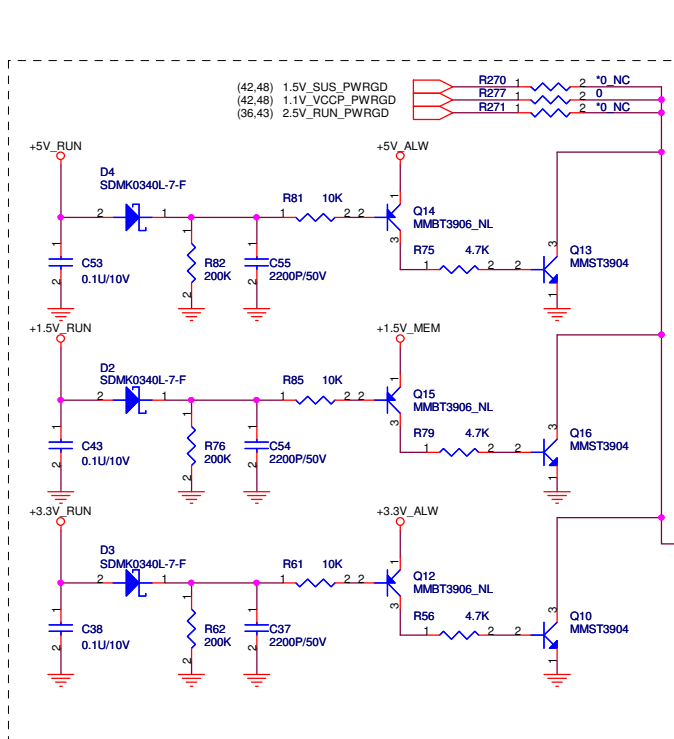
Project Name: Nike

Rev E

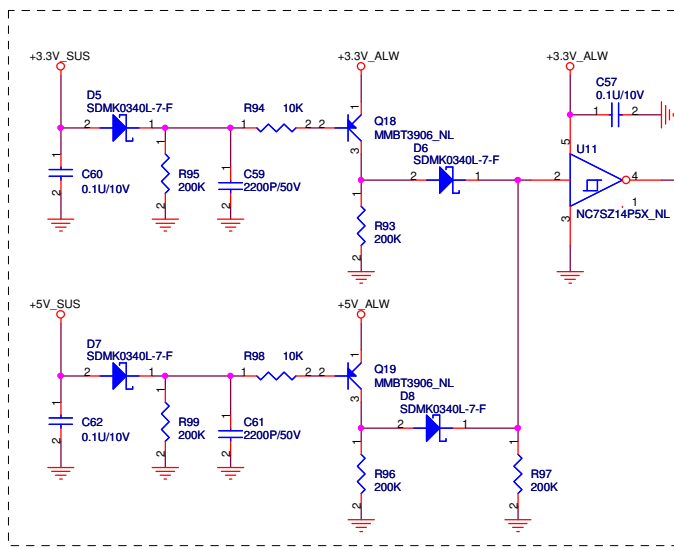
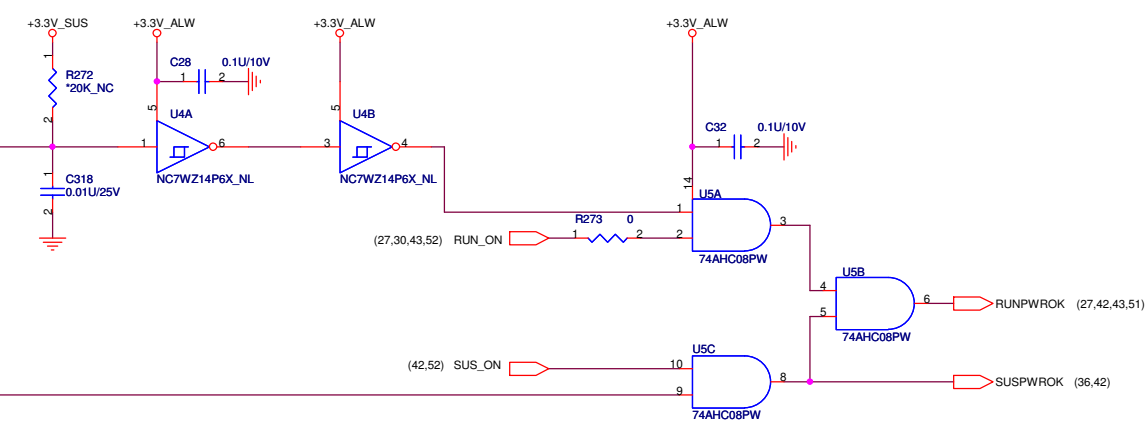
| | | | |
|-------|-------------------------|-----------------|------------|
| Title | SIO_5035 | Rev | E |
| Size | Custom | Document Number | NIKE (XM1) |
| Date | Thursday, July 31, 2008 | Sheet | 42 of 55 |








Keep Away from high speed buses

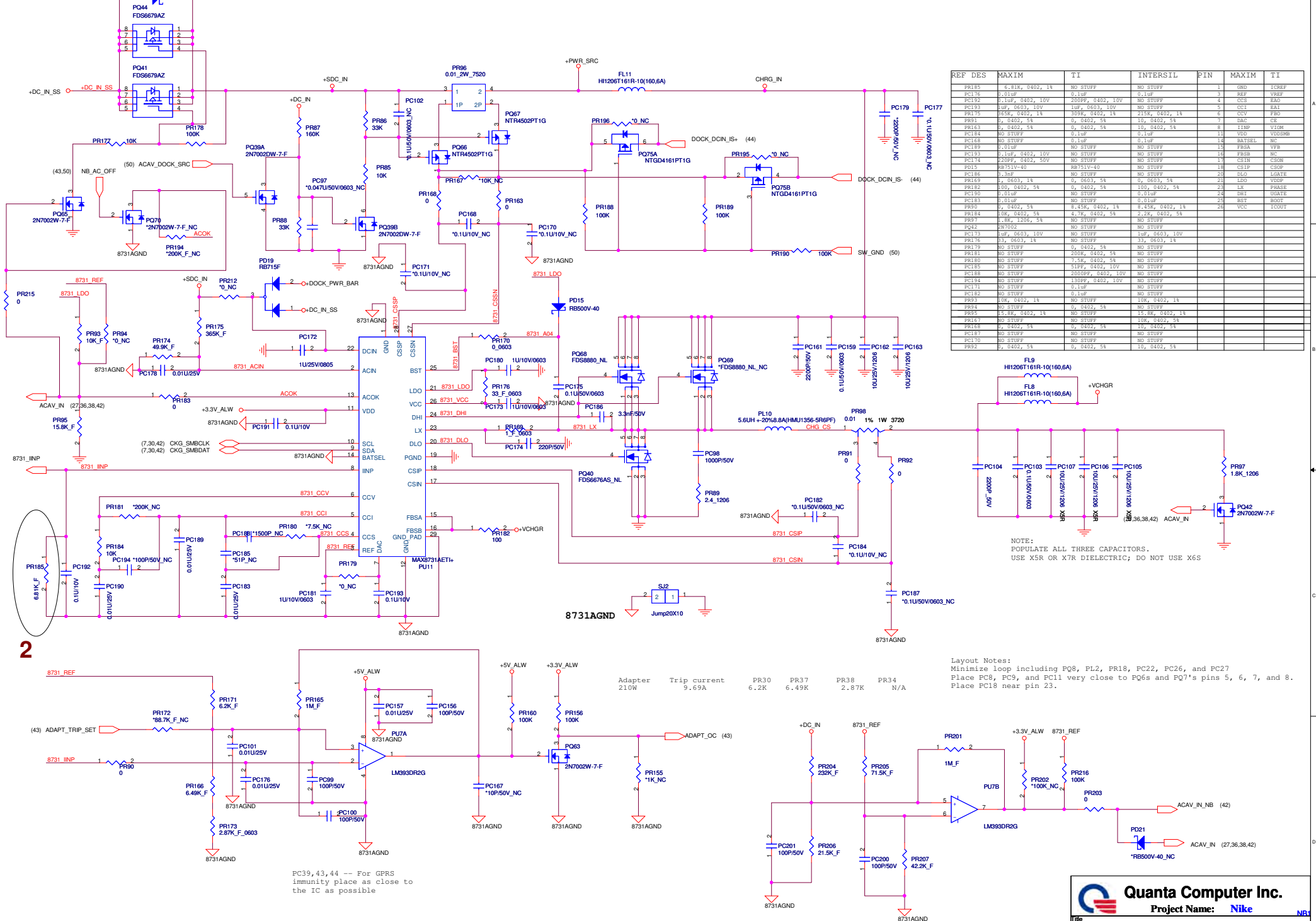




Quanta Computer Inc.

Project Name: Nike


| | | |
|-------------------------------|-------------------------------|-------------------|
| Title System Power Good | | |
| Size Custom | Document Number NIKE (XM1) | Rev E |
| Date: Thursday, July 31, 2008 | | Sheet 45 of 55 |



| REF | DES | MAXIM | TI | INTERSIL | PIN | MAXIM | TI |
|-------|------------------|------------------|-----------------|----------|--------|--------|----|
| PR185 | 6.81K, 0402, 1% | NO STUFF | NO STUFF | 1 | GND | ICREF | |
| PC176 | 0.1uF, 0402, 10V | 0.1uF | 0.1uF | 3 | REF | VREF | |
| PC193 | 1uF, 0603, 10V | 1uF, 0603, 10V | NO STUFF | 4 | CCS | EAG | |
| PR175 | 15K, 0402, 1% | 15K, 0402, 1% | 215K, 0402, 1% | 5 | CC1 | EAT | |
| PR191 | 0.0402, 5% | 0.0402, 5% | 10, 0402, 5% | 6 | CCV | FBO | |
| PR163 | 0.0402, 5% | 0.0402, 5% | 10, 0402, 5% | 8 | 11NP | VIOM | |
| PC184 | NO STUFF | 0.1uF | 0.1uF | 11 | VED | VEDRMB | |
| PC189 | NO STUFF | 0.1uF | 0.1uF | 14 | DATSEL | NC | |
| PC189 | 0.1uF | NO STUFF | NO STUFF | 15 | FRAA | VFB | |
| PC193 | 0.1uF, 0402, 10V | NO STUFF | NO STUFF | 16 | FBFB | NC | |
| PC174 | 220P, 0402, 50V | NO STUFF | NO STUFF | 17 | CS1B | CSGN | |
| PC15 | RB751V-40 | NO STUFF | NO STUFF | 18 | CS1P | CSOP | |
| PC186 | 3.3uF | NO STUFF | NO STUFF | 20 | DLO | LGATE | |
| PR189 | 0.0603, 1% | 0.0603, 5% | 0.0603, 5% | 21 | UDV | VDSR | |
| PR182 | 100, 0402, 5% | 0.0402, 5% | 100, 0402, 5% | 23 | LX | PHASE | |
| PC190 | 0.01uF | NO STUFF | 0.01uF | 24 | DRI | UGATE | |
| PC183 | 0.01uF | NO STUFF | 0.01uF | 25 | BS1 | BOOT | |
| PR190 | 0.0402, 5% | 8.45K, 0402, 1% | 8.45K, 0402, 1% | 26 | CC2 | ICOUT | |
| PR184 | 10K, 0402, 5% | 4.7K, 0402, 5% | 2.2K, 0402, 5% | | | | |
| PR191 | 2K, 1206, 5% | NO STUFF | NO STUFF | | | | |
| PQ42 | 2N7002 | NO STUFF | NO STUFF | | | | |
| PC173 | 1uF, 0603, 10V | NO STUFF | 1uF, 0603, 10V | | | | |
| PR176 | 15, 0603, 1% | NO STUFF | 15, 0603, 1% | | | | |
| PR179 | NO STUFF | 0.0402, 5% | NO STUFF | | | | |
| PR181 | NO STUFF | 200K, 0402, 5% | NO STUFF | | | | |
| PR180 | NO STUFF | 7.5K, 0402, 5% | NO STUFF | | | | |
| PC185 | NO STUFF | 100P, 0402, 10V | NO STUFF | | | | |
| PC188 | NO STUFF | 2000P, 0402, 10V | NO STUFF | | | | |
| PC154 | NO STUFF | 130P, 0402, 10V | NO STUFF | | | | |
| PC171 | NO STUFF | 0.1uF | NO STUFF | | | | |
| PC182 | NO STUFF | 0.1uF | NO STUFF | | | | |
| PR183 | 10K, 0402, 1% | NO STUFF | 10K, 0402, 1% | | | | |
| PR194 | NO STUFF | 0.0402, 5% | NO STUFF | | | | |
| PR195 | 15.8K, 0402, 1% | NO STUFF | 15.8K, 0402, 1% | | | | |
| PR188 | 0.0402, 5% | NO STUFF | 10, 0402, 5% | | | | |
| PC187 | NO STUFF | NO STUFF | NO STUFF | | | | |
| PC170 | NO STUFF | NO STUFF | NO STUFF | | | | |
| PR192 | 0.0402, 5% | NO STUFF | 10, 0402, 5% | | | | |

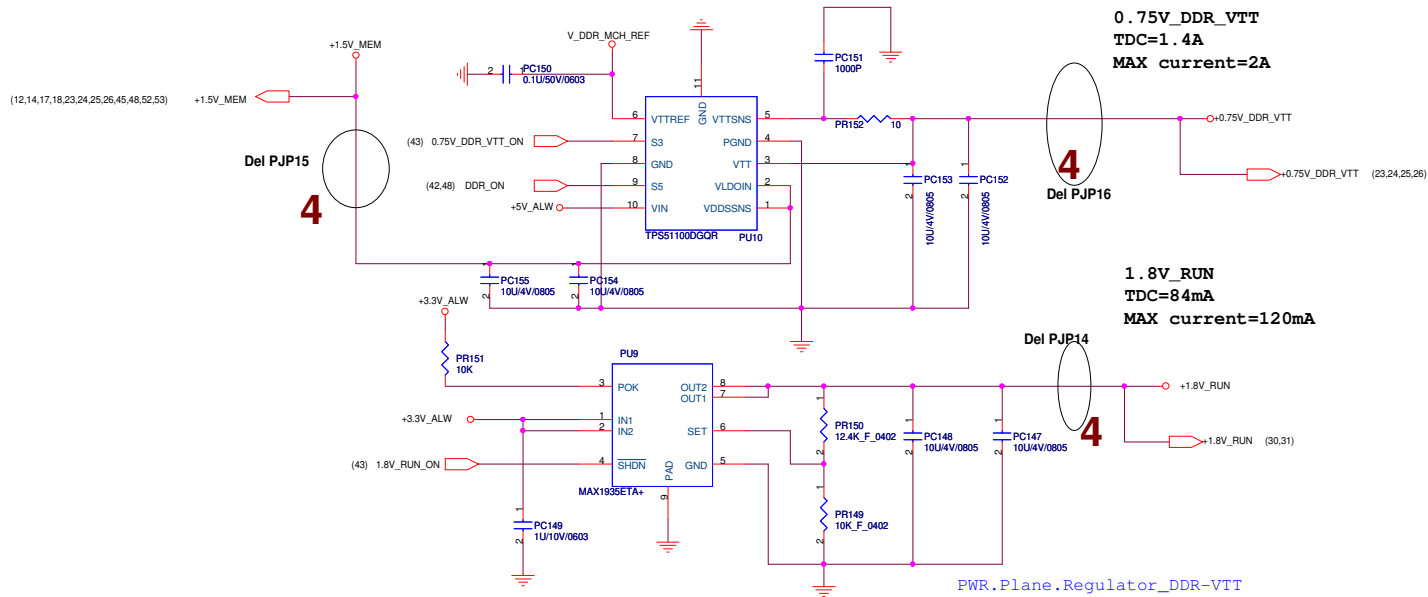
NOTE:
POPULATE ALL THREE CAPACITORS.
USE X5R OR X7R DIELECTRIC; DO NOT USE X6S

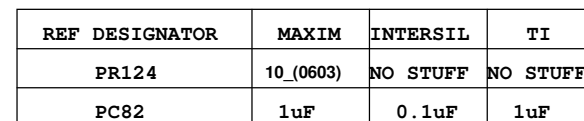
Layout Notes:
Minimize loop including PQ8, PL2, PR18, PC22, PC26, and PC27
Place PC8, PC9, and PC11 very close to PQ6 and PQ7's pins 5, 6, 7, and 8.
Place PC18 near pin 23.



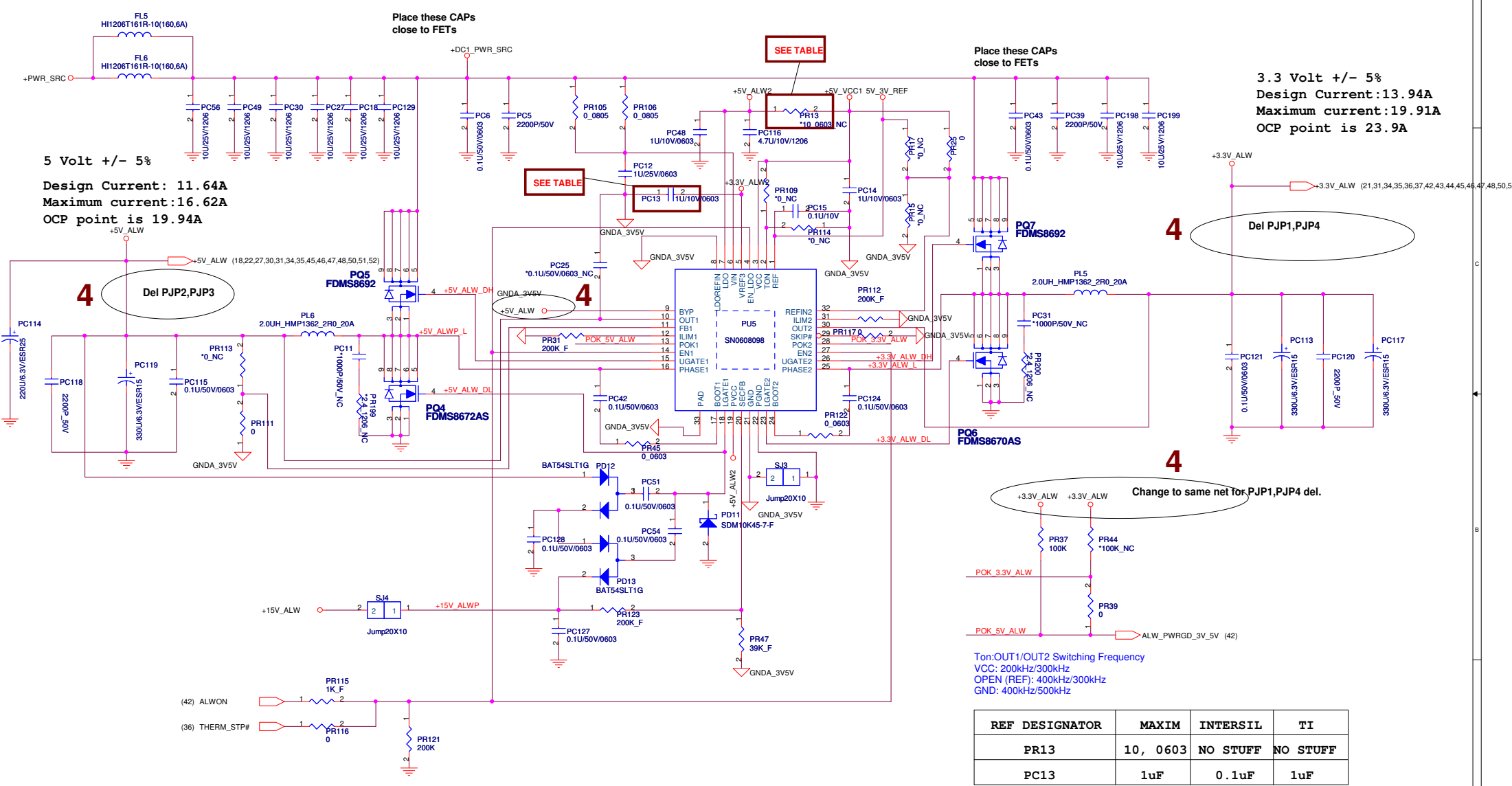
Quanta Computer Inc.
Project Name: **Nike**


| | | |
|-------------------------------|-----------------------------|--------|
| Title: Battery Charger | | Rev: E |
| Size: Custom | Document Number: NIKE (XM1) | |
| Date: Thursday, July 31, 2008 | Sheet: 46 of 55 | |





M'09
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+3.3V_ALW2/+15V_ALW





Quanta Computer Inc.

Project Name: Nike

Title

5V_ALW, 3V_ALW

Size

Custom

Document Number

NIKE (XM1)

Date

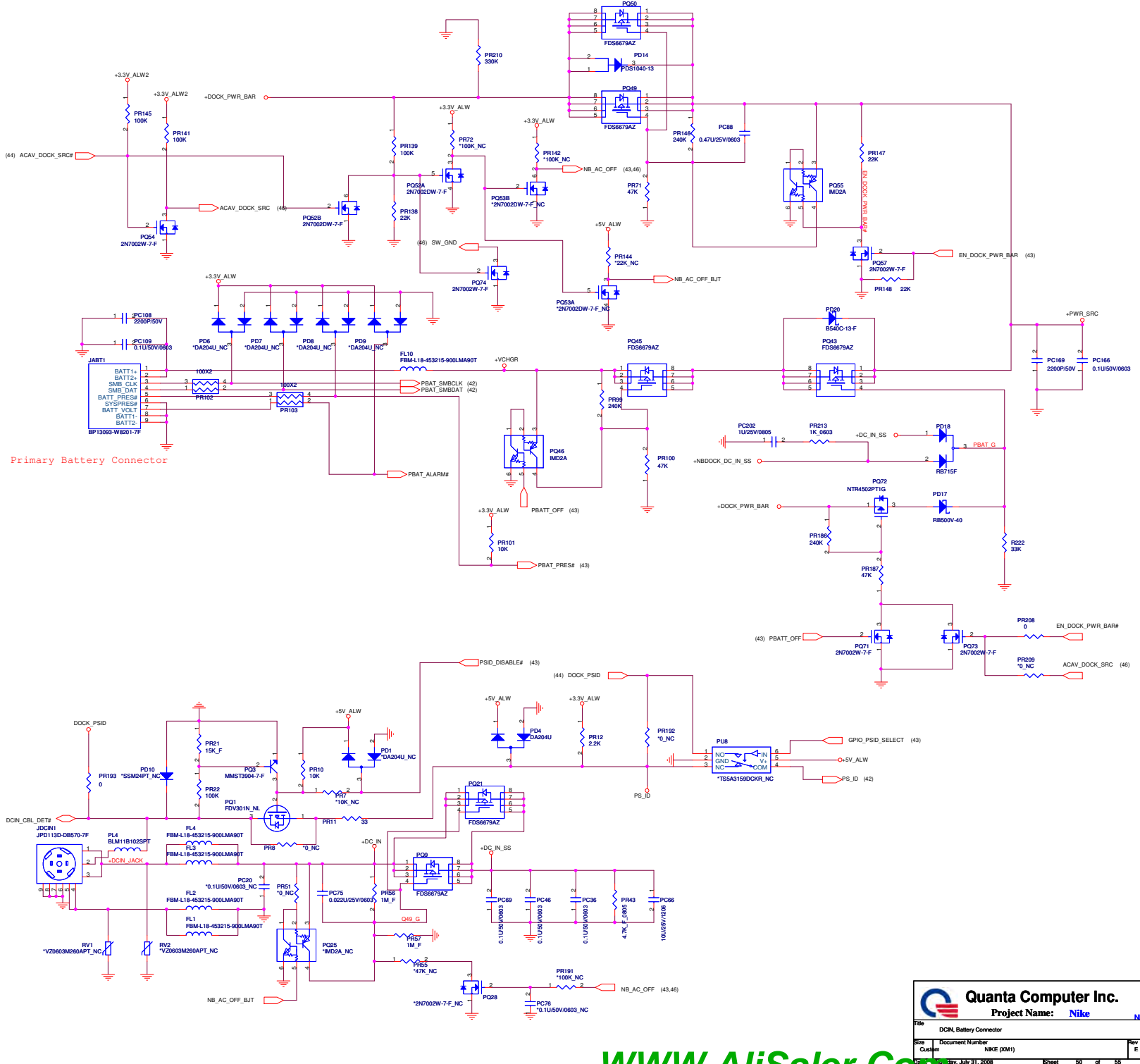
Thursday, July 31, 2008

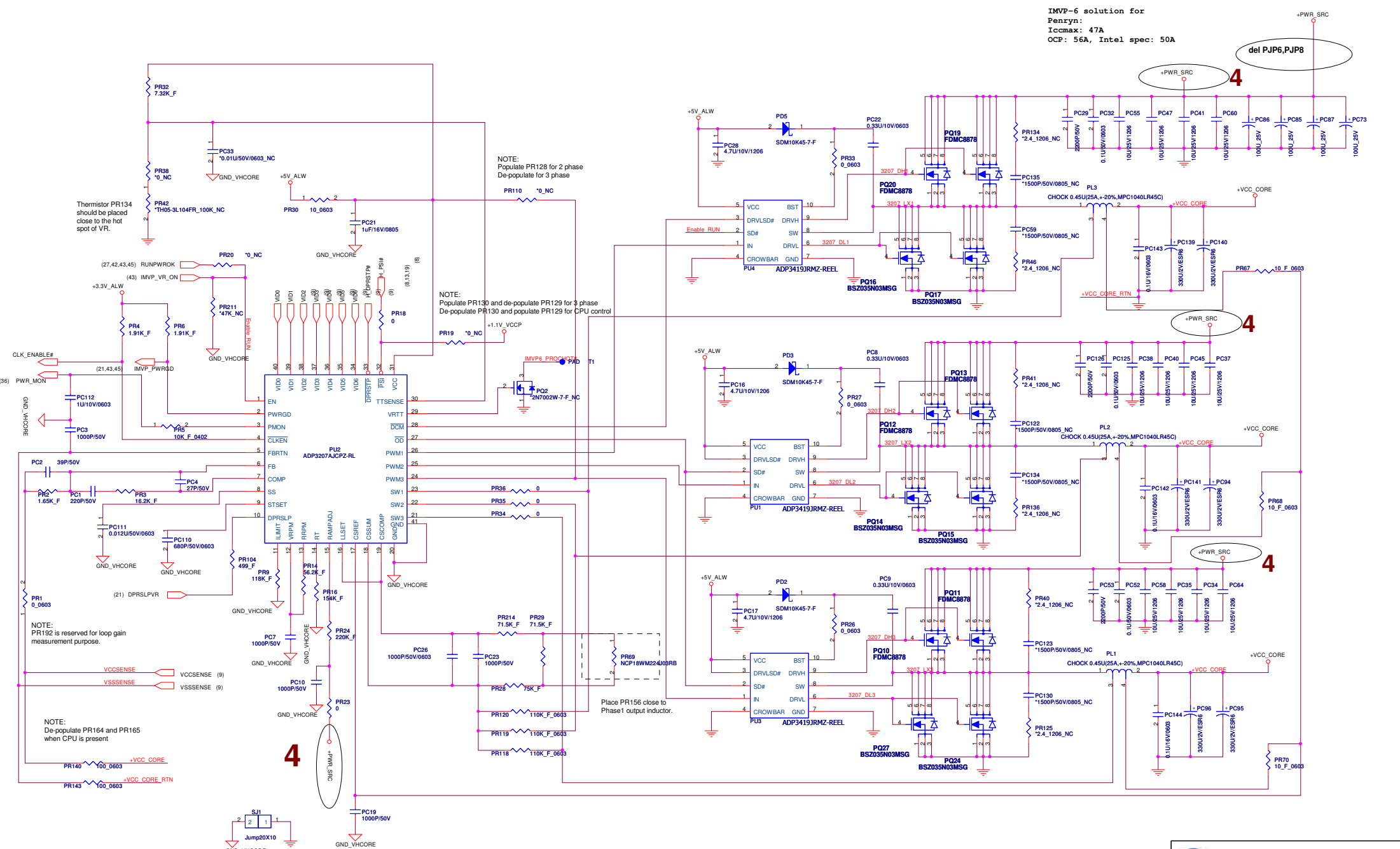
Sheet

49 of 55

Rev

E





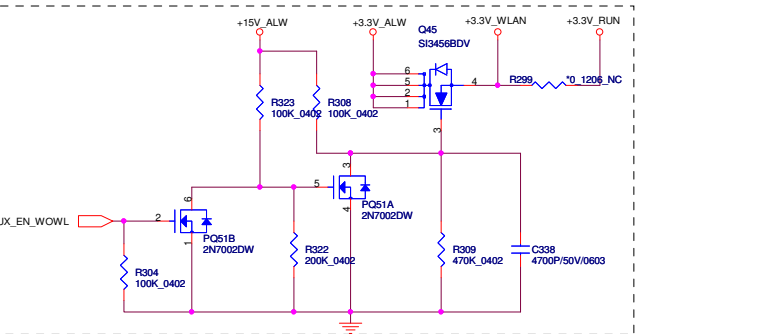
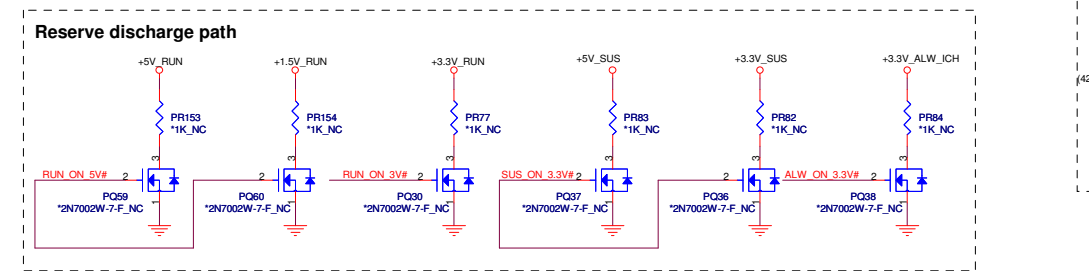
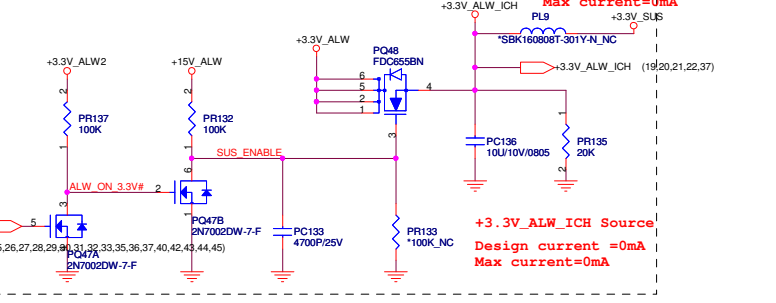
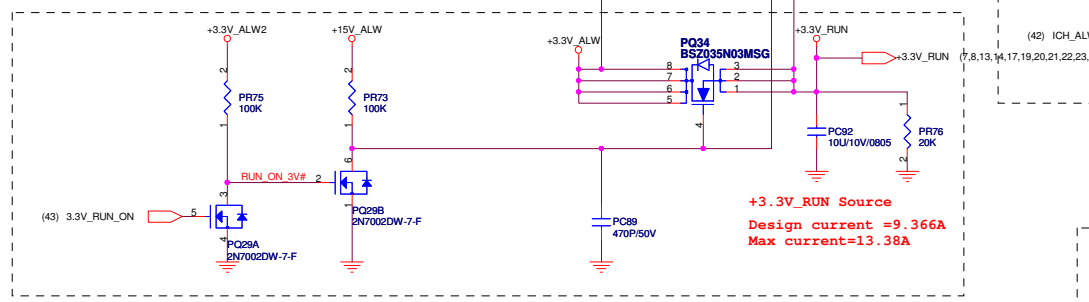
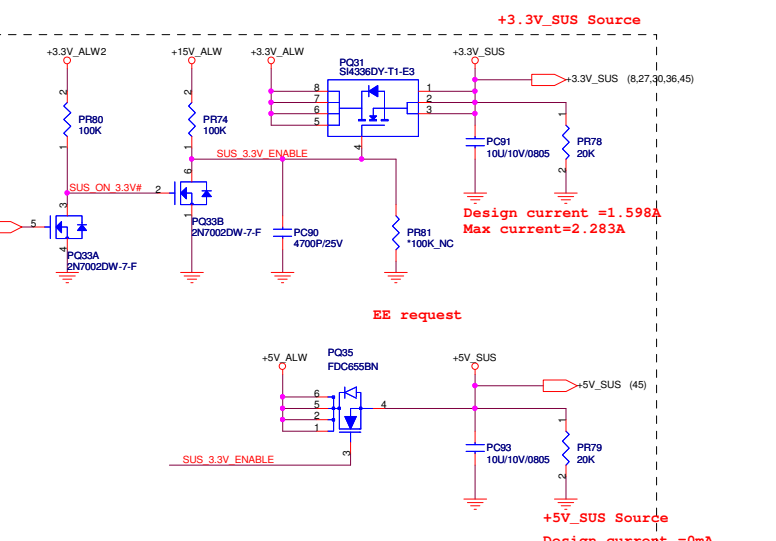
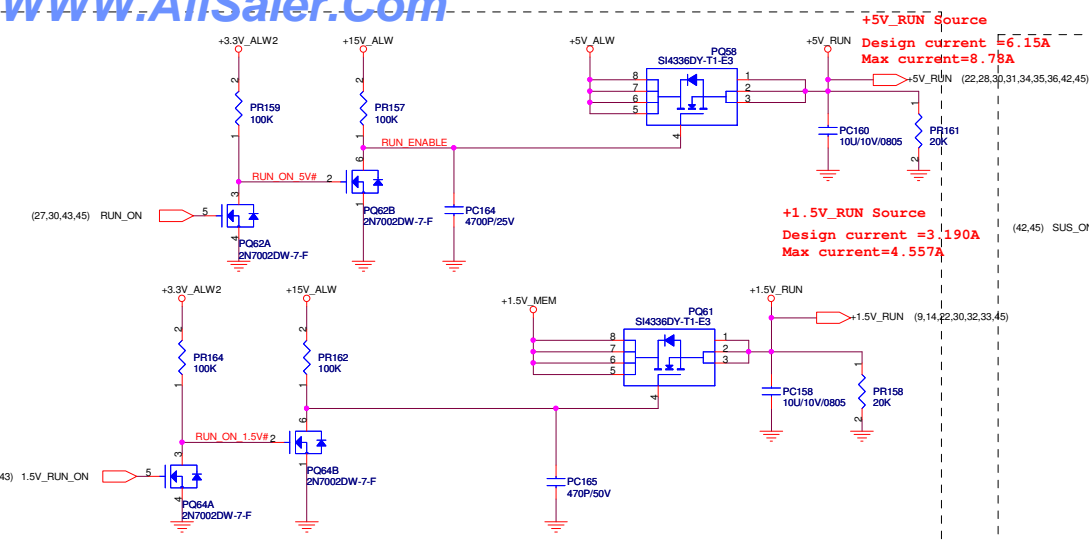
NOTE:
ADP3207A: PR141=10K, PC1=1uF (Pin 3 output Power Signal)
ADP3207:PR141=0, PC1=4.7nF (Pin 3 programs PWRGD Delay)

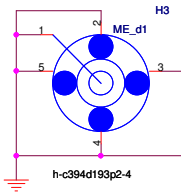
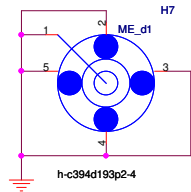
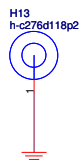
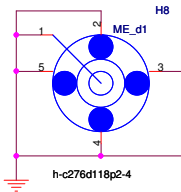
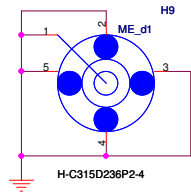
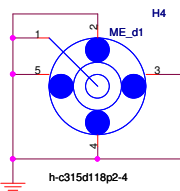
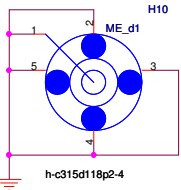
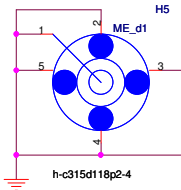
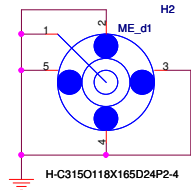
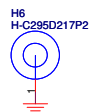
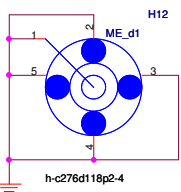
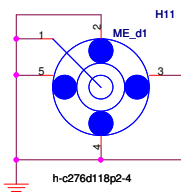
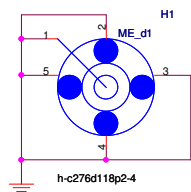
A

B

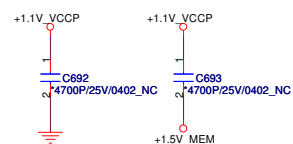
C

D





Stitching caps



EMI Clips

