Discrete/UMA Schematics Document

Sandy Bridge

Intel PCH

2011-01-19

REV : XXX

DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
MADISON:DIS MADISON platform installed
Colay :Manual modify BOM
MUX : PX

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Size A3	Document Number LZ57	Rev -1
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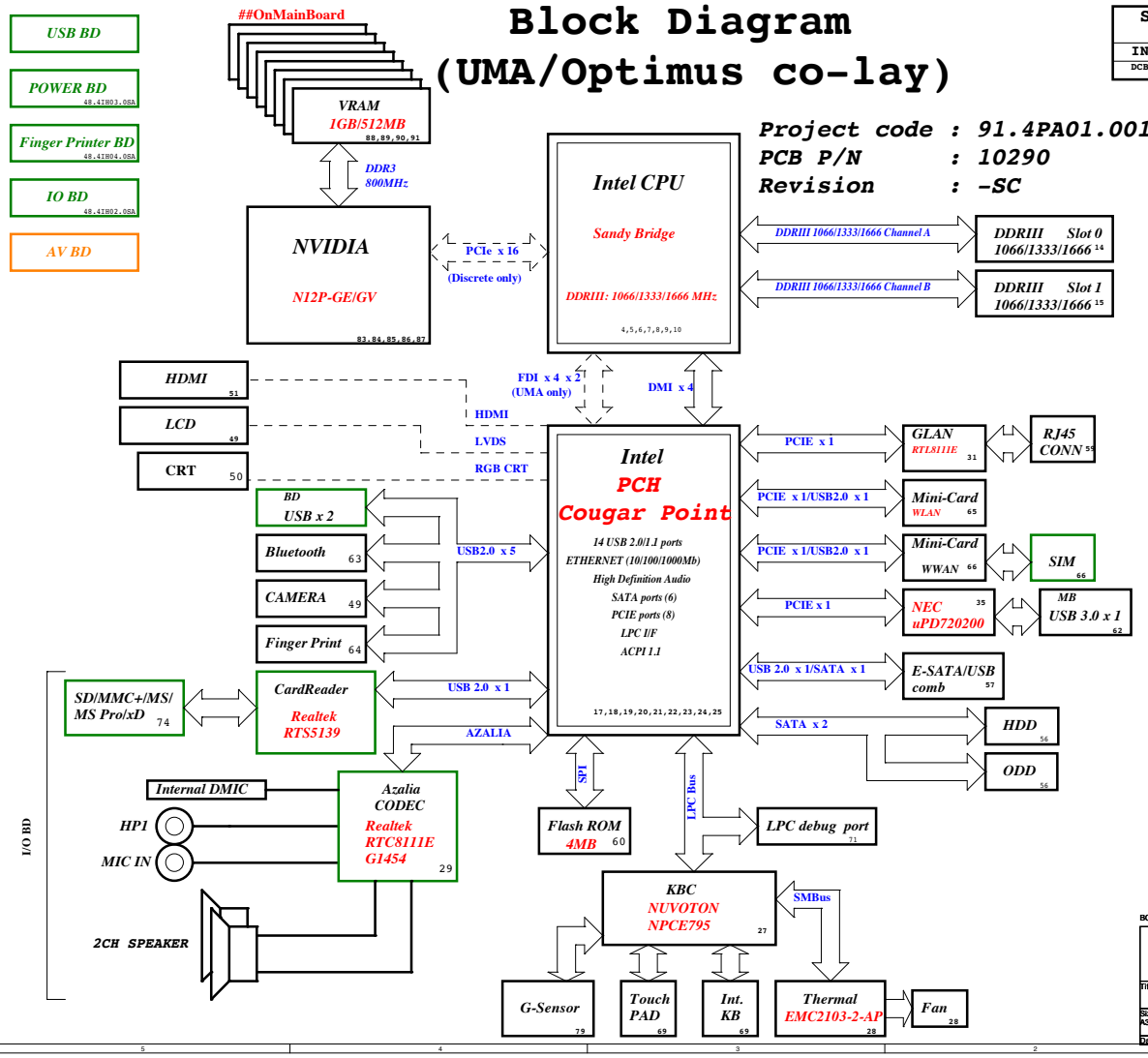
Block Diagram (UMA/Optimus co-lay)

Project code : 91.4PA01.001
PCB P/N : 10290
Revision : -SC



SYSTEM DC/DC RT8208B 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC NCP6131 42-44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6111CQHC 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183AQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6111C 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 DDR_VREF_S3

SYSTEM DC/DC NCP5911 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

LDO RT9025 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9091-180T11U 24,93	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D5V_S5 1D8V_VGA_S0

LDO RT9026 46	
INPUTS	OUTPUTS
5V_S5	0D75V_S0

PCB LAYER

L1:Top	L5:VCC
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Signal

BOM

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Title: Block Diagram

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ 18 kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-Up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Onboard LAN
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	USB Ext. port 3
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I2 C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex	Bus
EC SMBus 1 Battery CHARGER			BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP			SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI			PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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Title: Table of Content

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

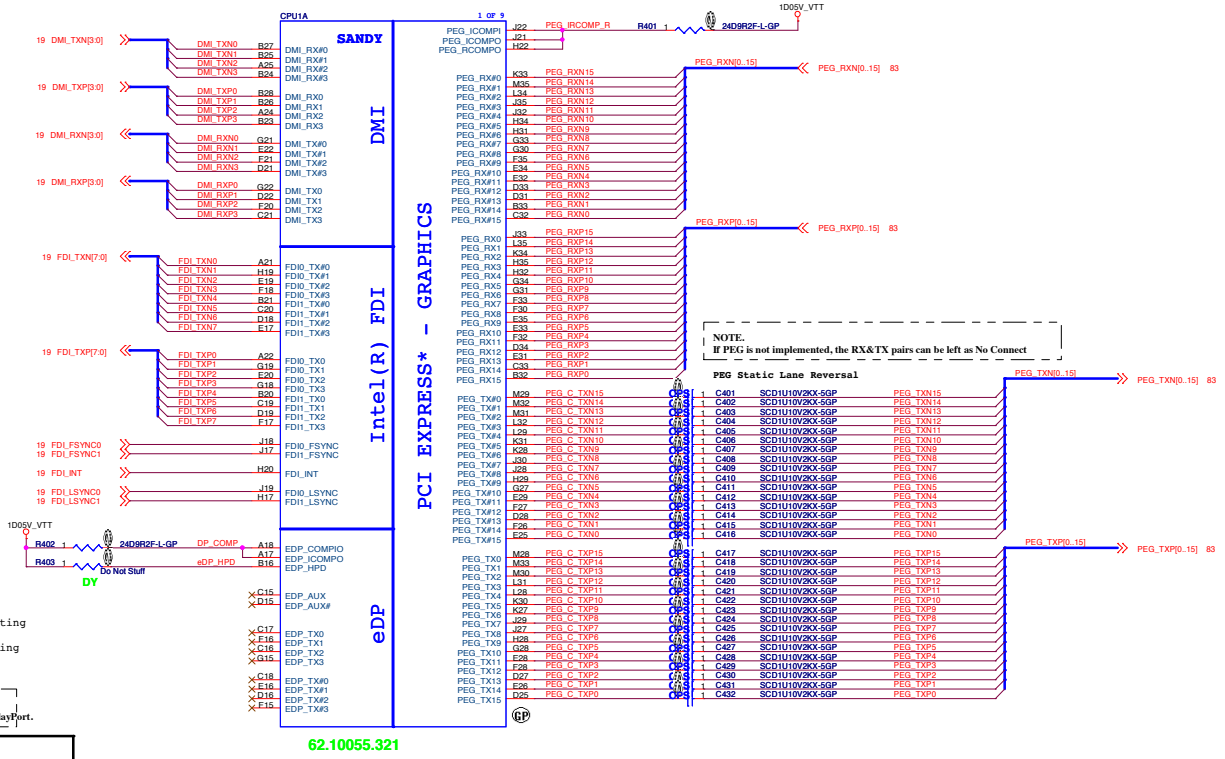
Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal



delete R404&RN 401 @20100630

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Title: CPU (PCIE/DMI/FDI)

Size: A3 | Document Number: LZ57 | Rev: -1

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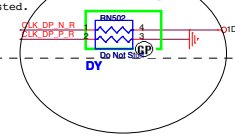
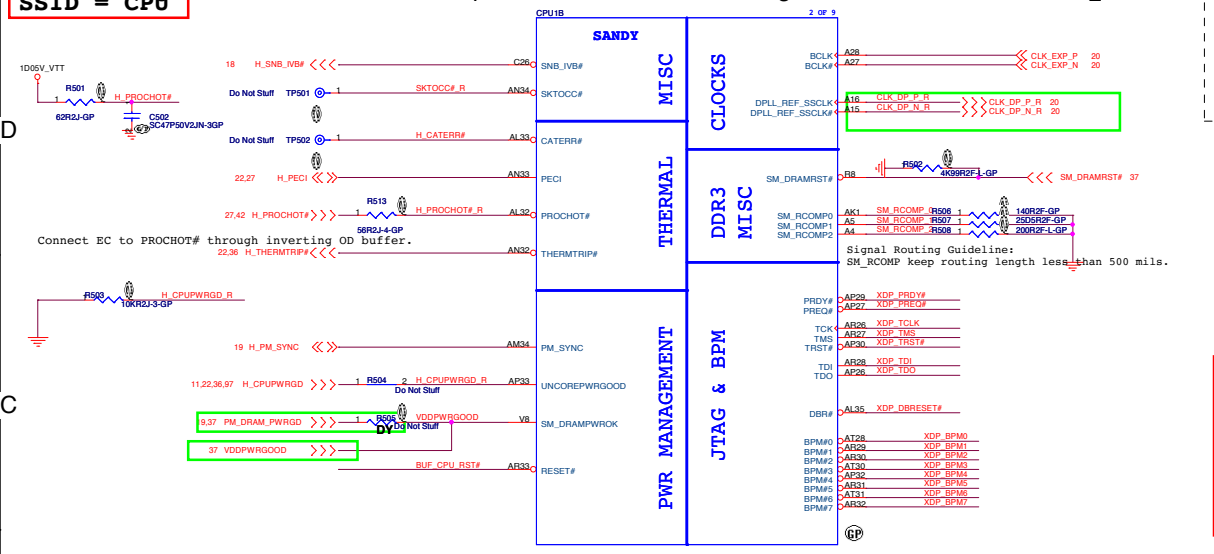
SSID = CPU

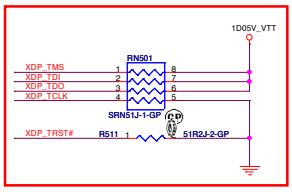
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

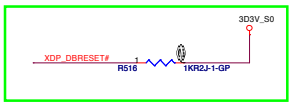


20100722 SA confirm.

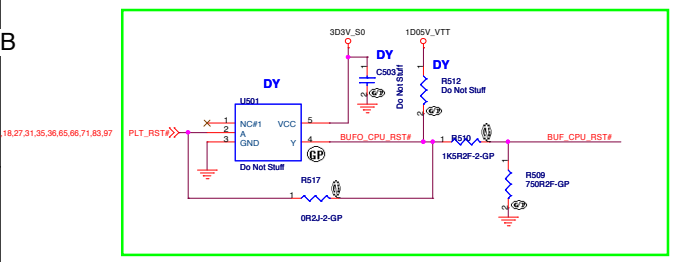


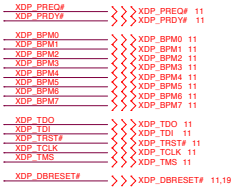
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.





20100722 follow Astro add buffer





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Title: CPU (THERMAL/CLOCK/PM)		
Size: A3	Document Number: LZ57	Rev: -1
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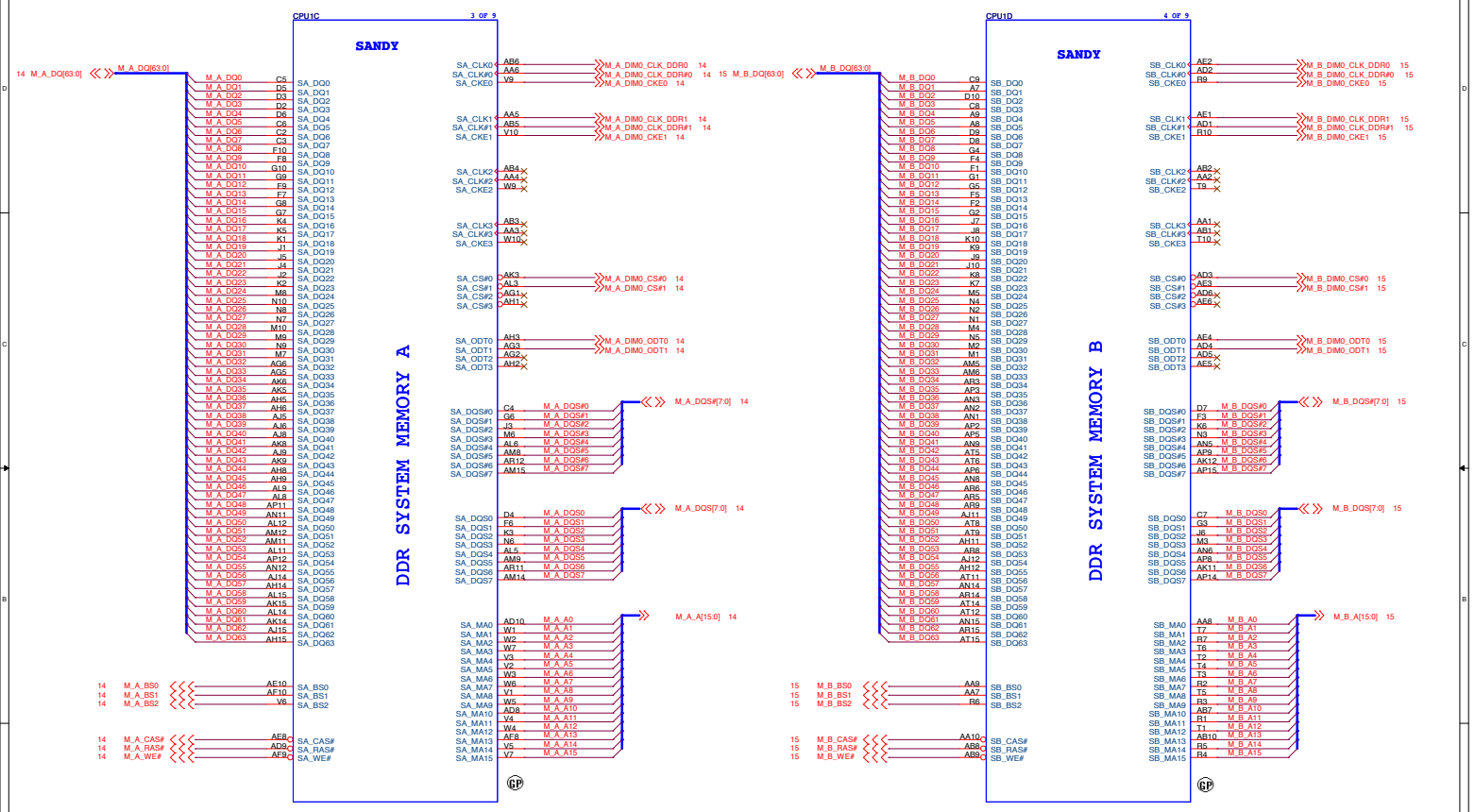
SSID = CPU



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Title	CPU (DDR)	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 6 of 102	

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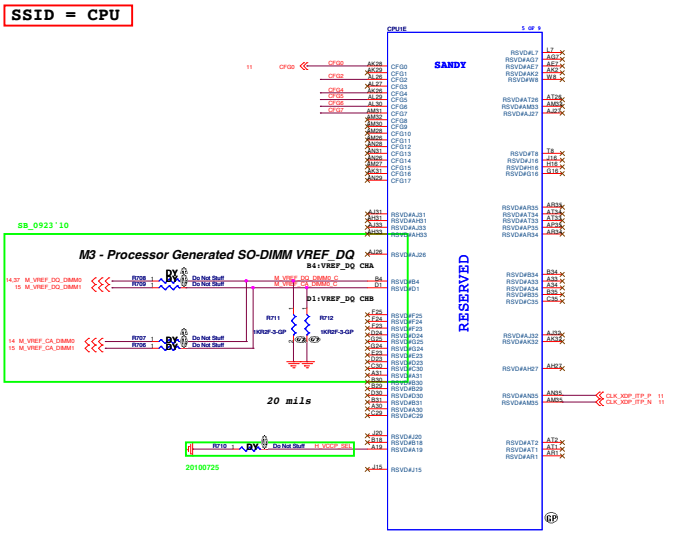
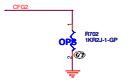
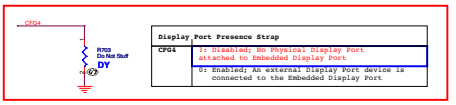
SSID = CPU

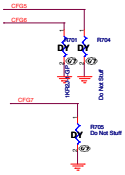




PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled , function 2 disabled 01: Reserved - (Device 1 function 1 disabled , function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

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File

CPU (RESERVED)

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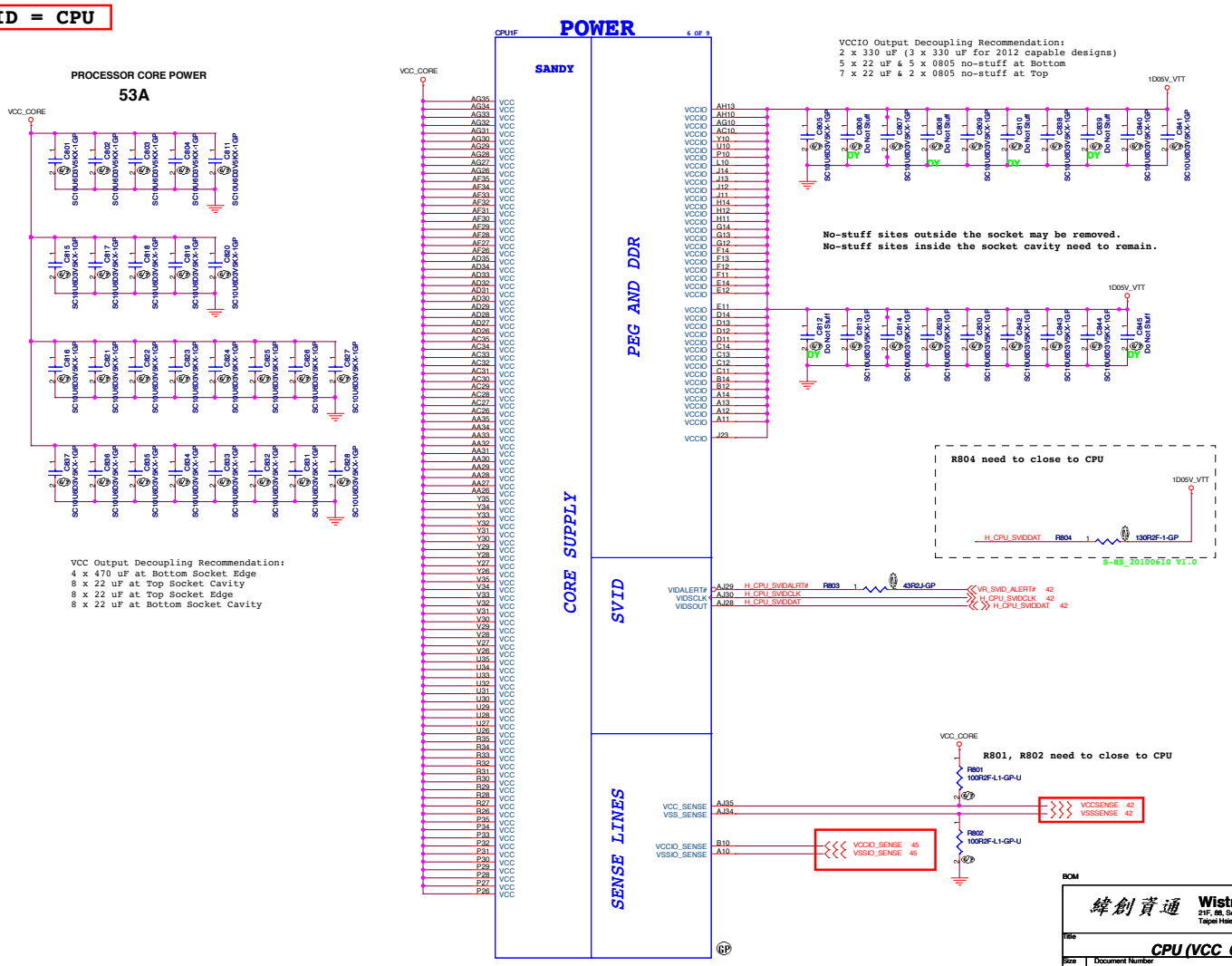
SSID = CPU



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Title	CPU (VCC_CORE)
Size / Custom	Document Number: LZ57
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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

POWER

CPU1G — 7 OF 9

SANDY GRAPHICS

SENSE LINES: VAXG_SENSE, VSSAXG_SENSE

VREF: SM_VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

VCC_GFXCORE

PROCESSOR VAXG: 24A

C301 Do Not Stuff, C302 SC1UB20V6KX-1GP, C303 Do Not Stuff, C304 SC1UB20V6KX-1GP, C305 SC1UB20V6KX-1GP, C306 SC1UB20V6KX-1GP, C307 SC1UB20V6KX-1GP, C308 SC1UB20V6KX-1GP, C318 SC1UB20V6KX-1GP, C319 SC1UB20V6KX-1GP, C320 SC1UB20V6KX-1GP, C321 SC1UB20V6KX-1GP

VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

SM_VREF AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

Close to CPU

VCC_GFXCORE — R906 100R2F-L1-GP-U — VCC_AXG_SENSE / VSS_AXG_SENSE — R907 100R2F-L1-GP-U

S-HR_20100609 V1.0

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

1D5V_DDR_S0

PROCESSOR VDDQ: 10A

C309 SC1UB20V6KX-1GP, C310 SC1UB20V6KX-1GP, C311 SC1UB20V6KX-1GP, C312 Do Not Stuff, C313 Do Not Stuff, C314 SC1UB20V6KX-1GP

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C316 Do Not Stuff, C315 SC1UB20V6KX-1GP, C317 SC1UB20V6KX-1GP, TC903 ST330U2VDM-4-GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0 — R902 100R2F-L1-GP-U — Notice:pull-high 100k or 10k

VCCSA_SENSE H23 — VCCSA_SENSE — VCCSA_SENSE 48

FC_C22 C22 — H_FC_C22 — H_FC_C22 48
VCCSA_VID1 C24 — VCCSA_SEL — VCCSA_SEL 48

RN901 SRN1KJ-7-GP

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

TC902 ST330U2VDM-4-GP, C823 SC1UB20V6KX-1GP, C822 SC1U10V6KX-1GP, C824 Do Not Stuff

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

20100721 standard schematic update

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Title: CPU (VCC_GFXCORE)

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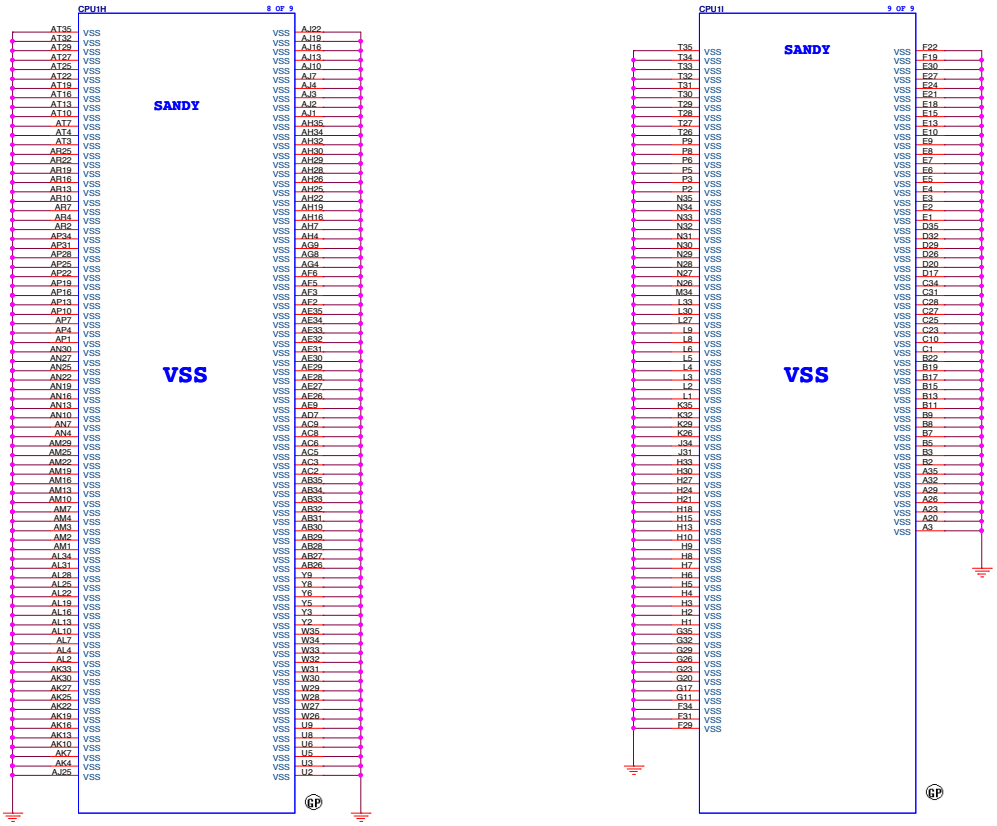
SSID = CPU



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Title	CPU (VSS)
Size A3	Document Number LZ57
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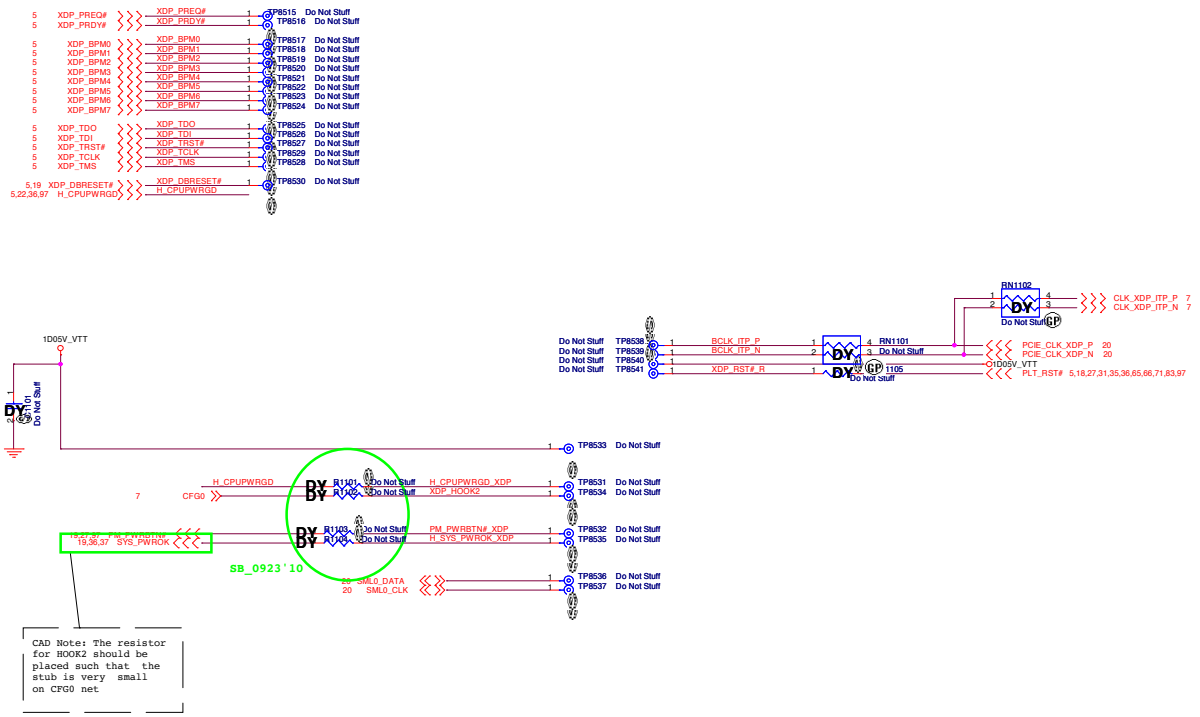

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Title	**XDP**	
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Title	***Reserved***
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Title	***Reserved***
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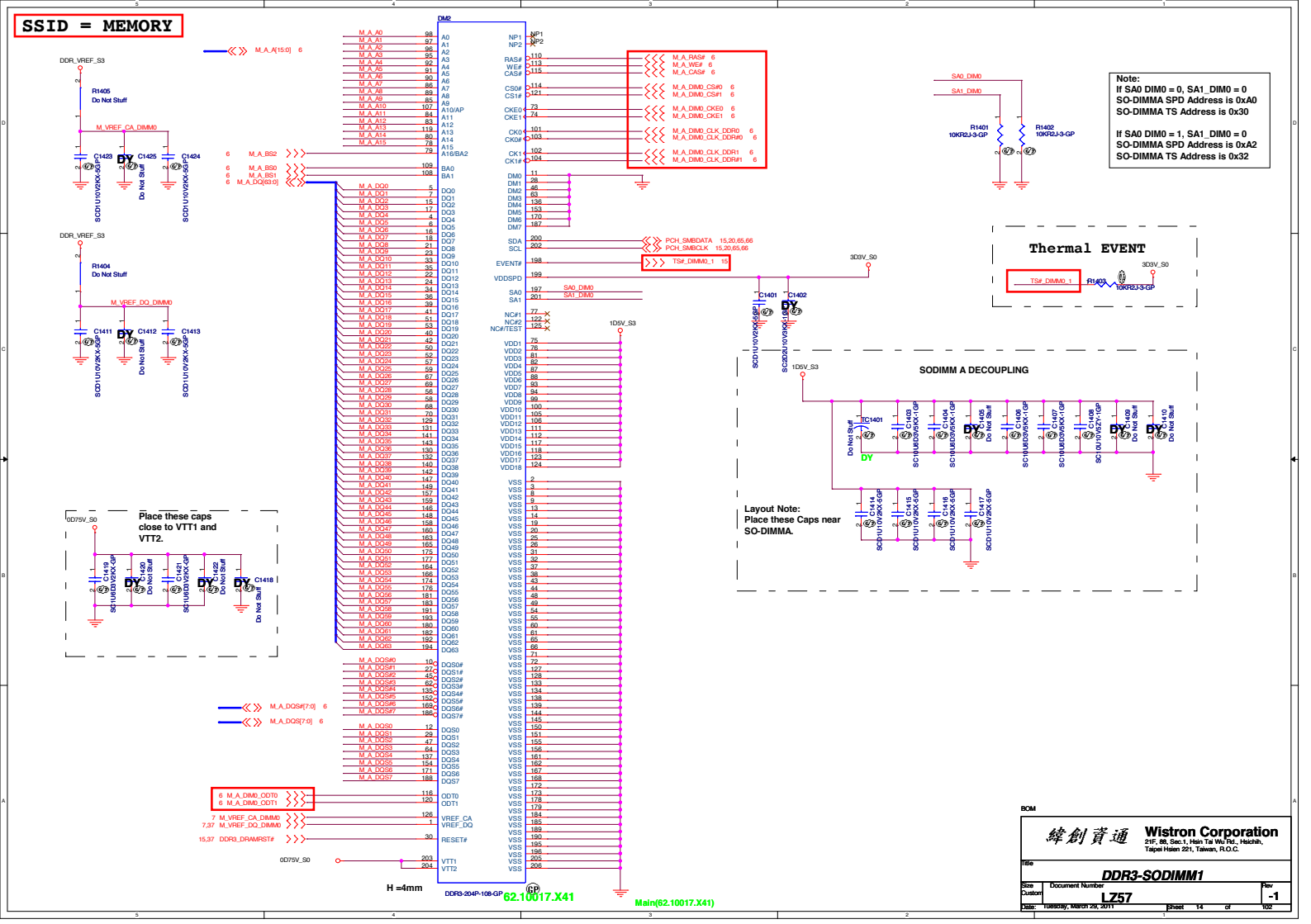

2nd = 62.10024.E01

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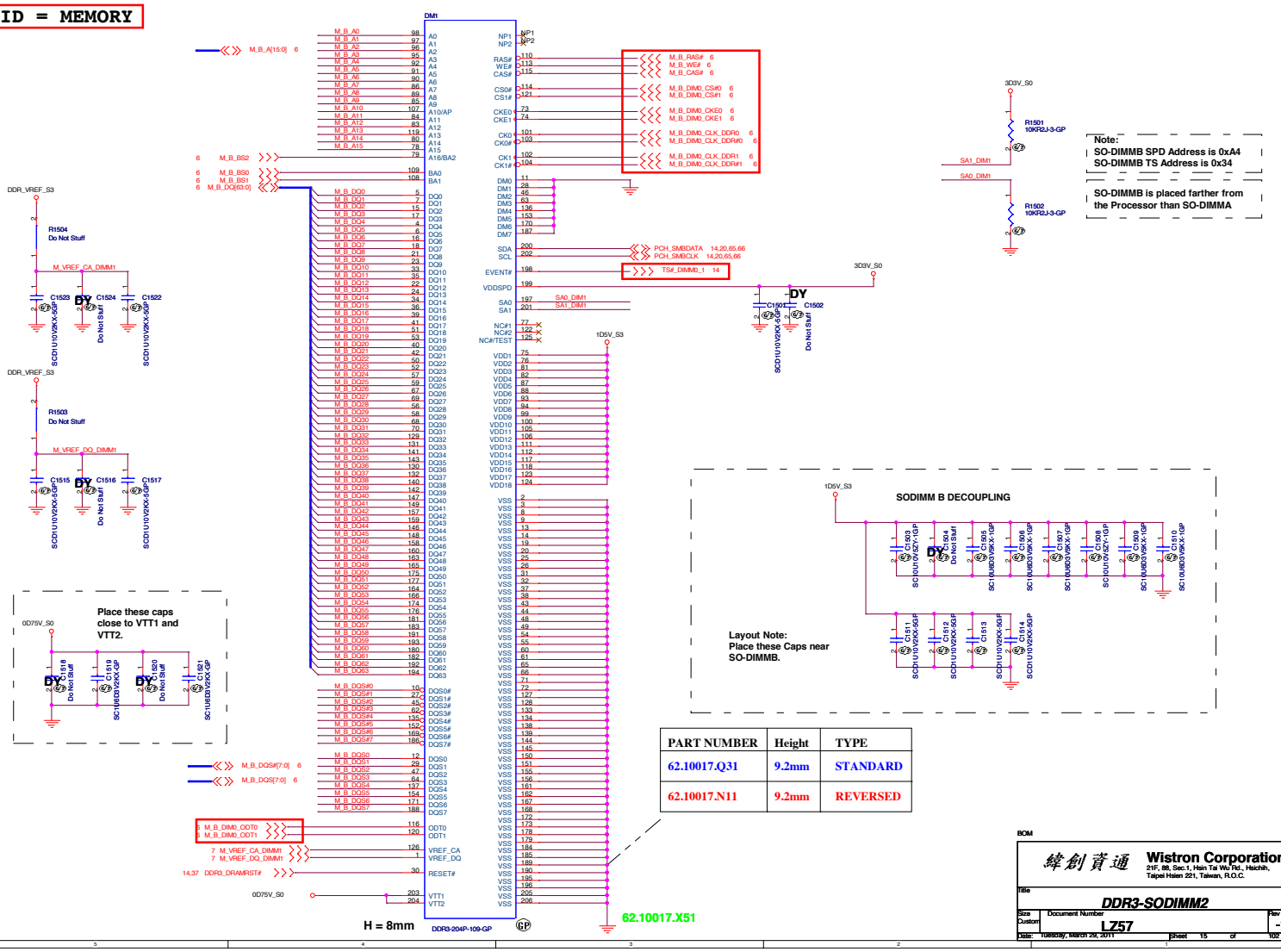
SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

PART NUMBER	Height	TYPE
62.10017.Q31	9.2mm	STANDARD
62.10017.N11	9.2mm	REVERSED

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 15 of 102

(Blanking)

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***DDR3-SODIMM2***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 16 of 102

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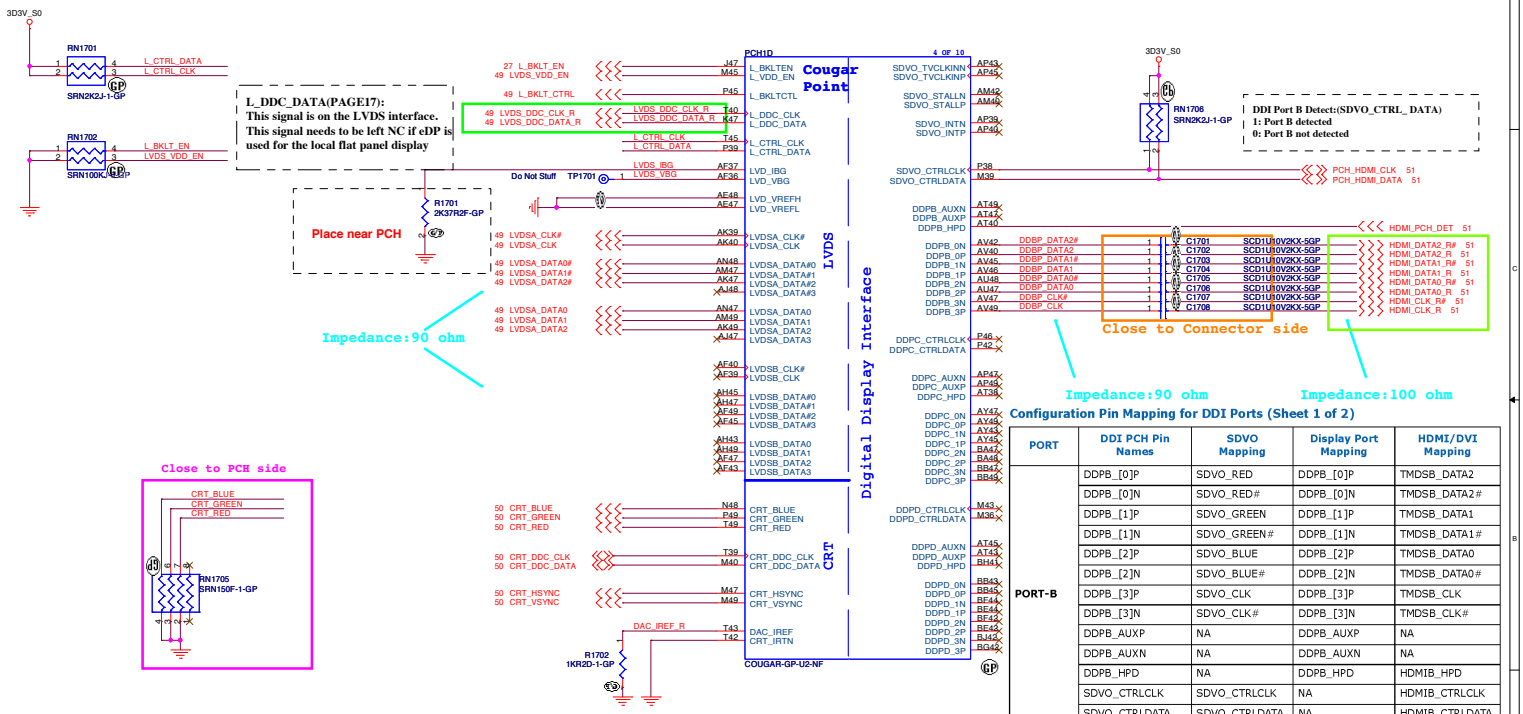

Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (LVDS/CRT/DDI)**

Size: A3 | Document Number: **LZ57** | Rev: **-1**

Date: Tuesday, March 29, 2011 | Sheet 17 of 102

SSID = PCH

20100725 Annie modify

CRB : 2.2K
CEKLT: 1K

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Danbury Technology:
Disabled when Low.
Enable when High.

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	X
1	USB Ext. port 1 (Left Side)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	E-SATA /USB Ext. port 4
9	USB Ext. port 2(CardReader BD)
10	USB Ext. port 3(RJ45_BD)
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SW programing USB_OC#12_13 for USB 9

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

KBC CLK EMI

20100629

-1_1209'10

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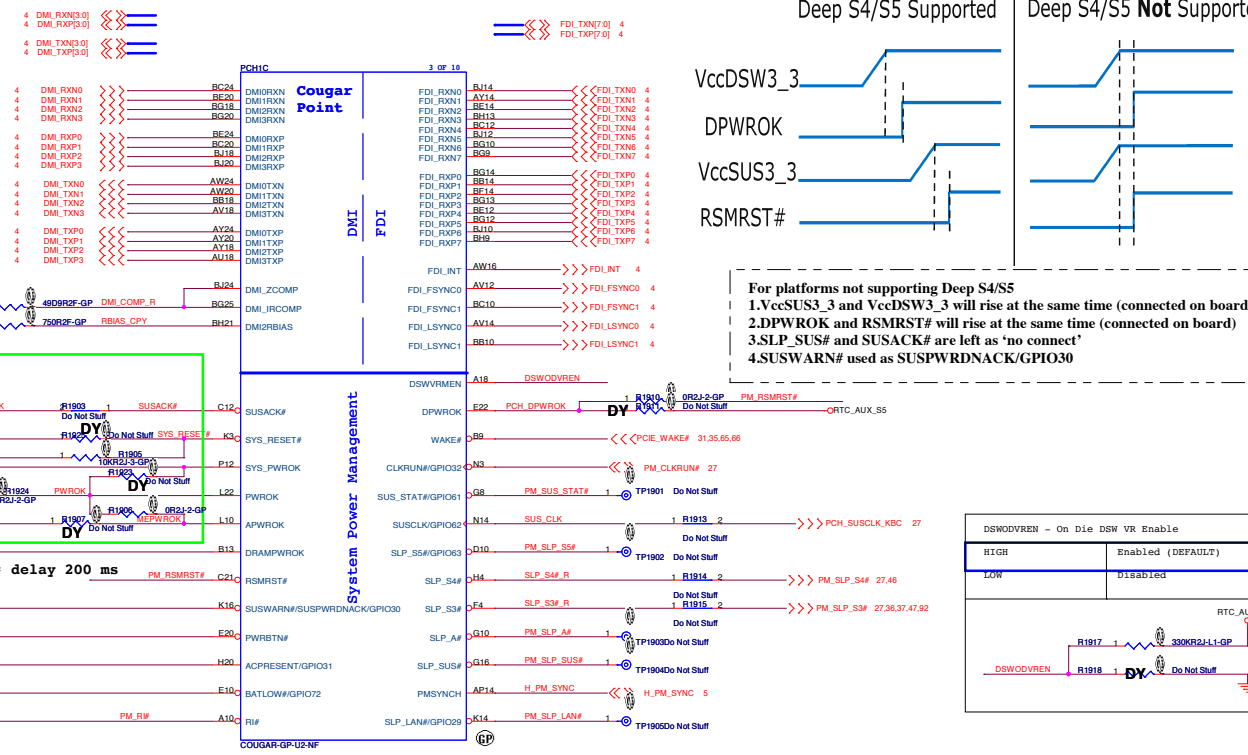
SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

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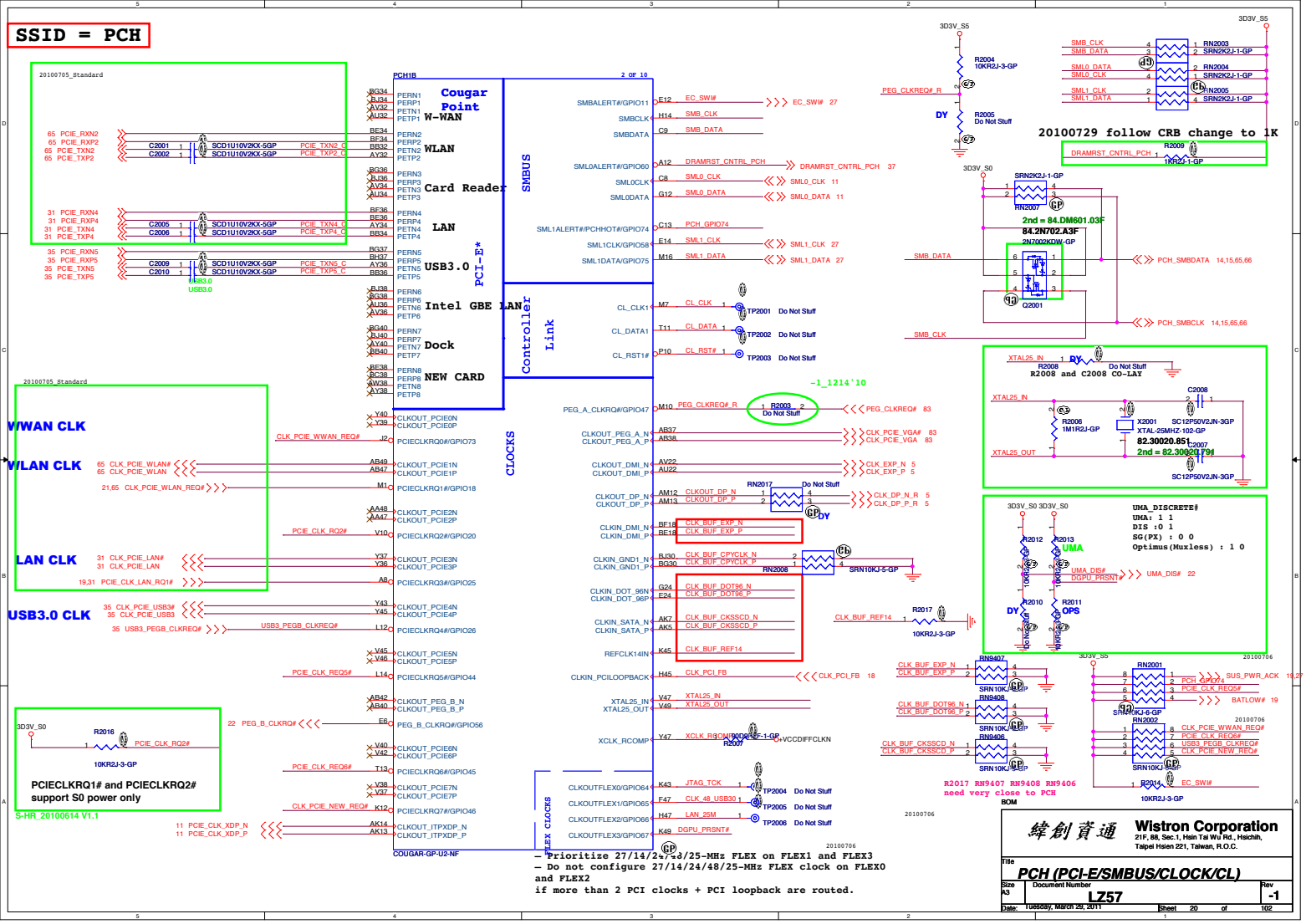
Title: PCH (DM I/FDI/PM)

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 19 of 102



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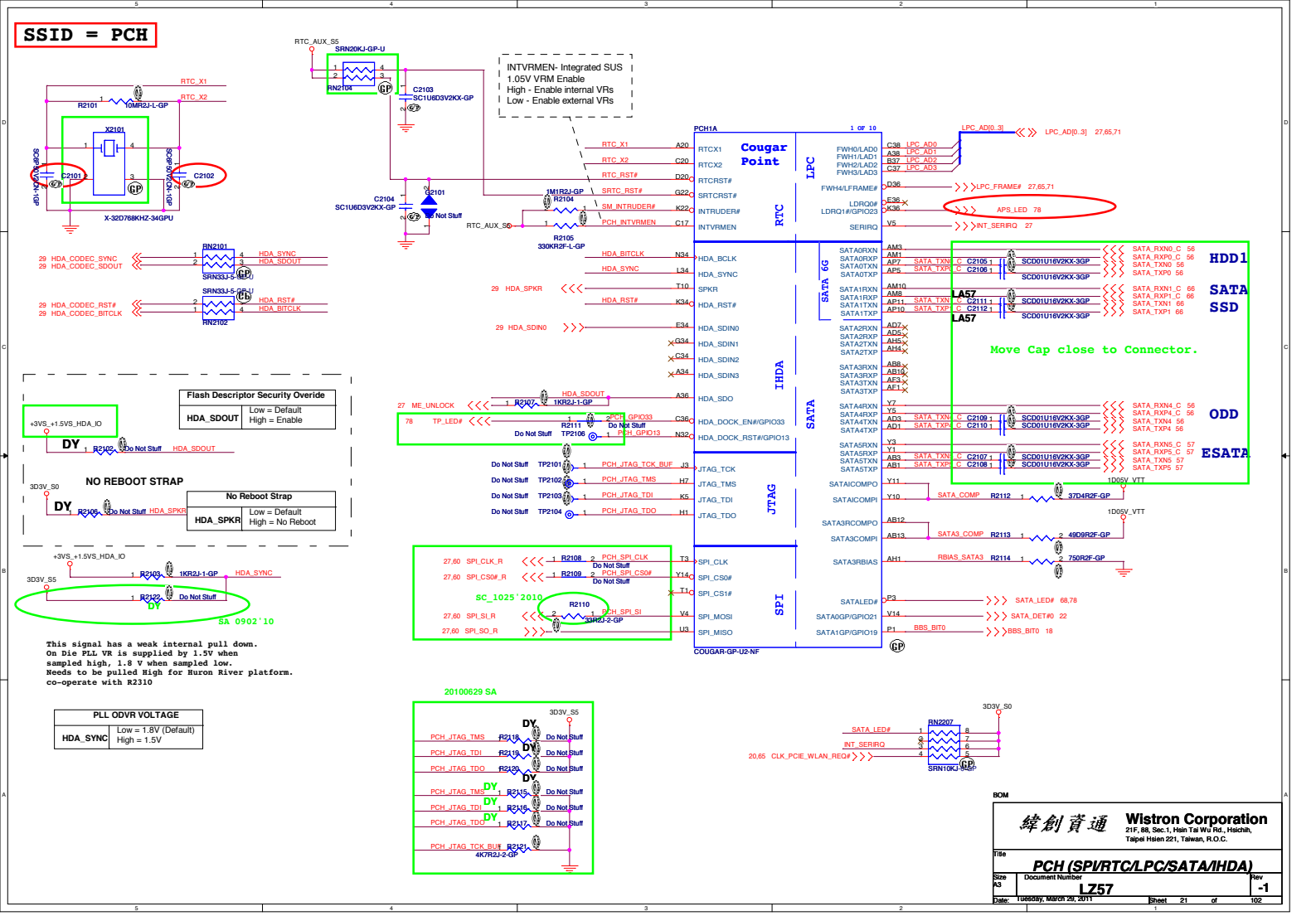
SSID = PCH


INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs
PCH1A
Cougar Point
1 OF 10
RTC
LPC
SATA 6G
IHDA
SATA
JTAG
SPI
COUGAR-GP-U2-NF
X-32D768KHZ-34GPU
SRN20KJ-GP-U
SRN33J-5-GP-U
SRN10KJ-GP
Flash Descriptor Security Overide
HDA_SDOUT
Low = Default
High = Enable
NO REBOOT STRAP
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
PLL ODVR VOLTAGE
HDA_SYNC
Low = 1.8V (Default)
High = 1.5V
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310
20100629 SA
SC_1025'2010
SA 0902'10
Move Cap close to Connector.
HDD1
SATA SSD
ODD
ESATA
LA57
APS_LED 78
INT_SERIRQ 27
LPC_FRAME# 27,65,71
LPC_AD[0..3] 27,65,71
SATA_LED# 68,78
SATA_DET#0 22
BBS_BIT0 18
CLK_PCIE_WLAN_REQ# 20,65
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size A3
Document Number LZ57
Rev -1
Date: Tuesday, March 29, 2011
Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

20100720 SW

20100725

20100729 follow Annie CRB

SB 0923'10

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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Title: PCH (GPIO/CPU)
Size: A3 | Document Number: LZ57 | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 22 of 102

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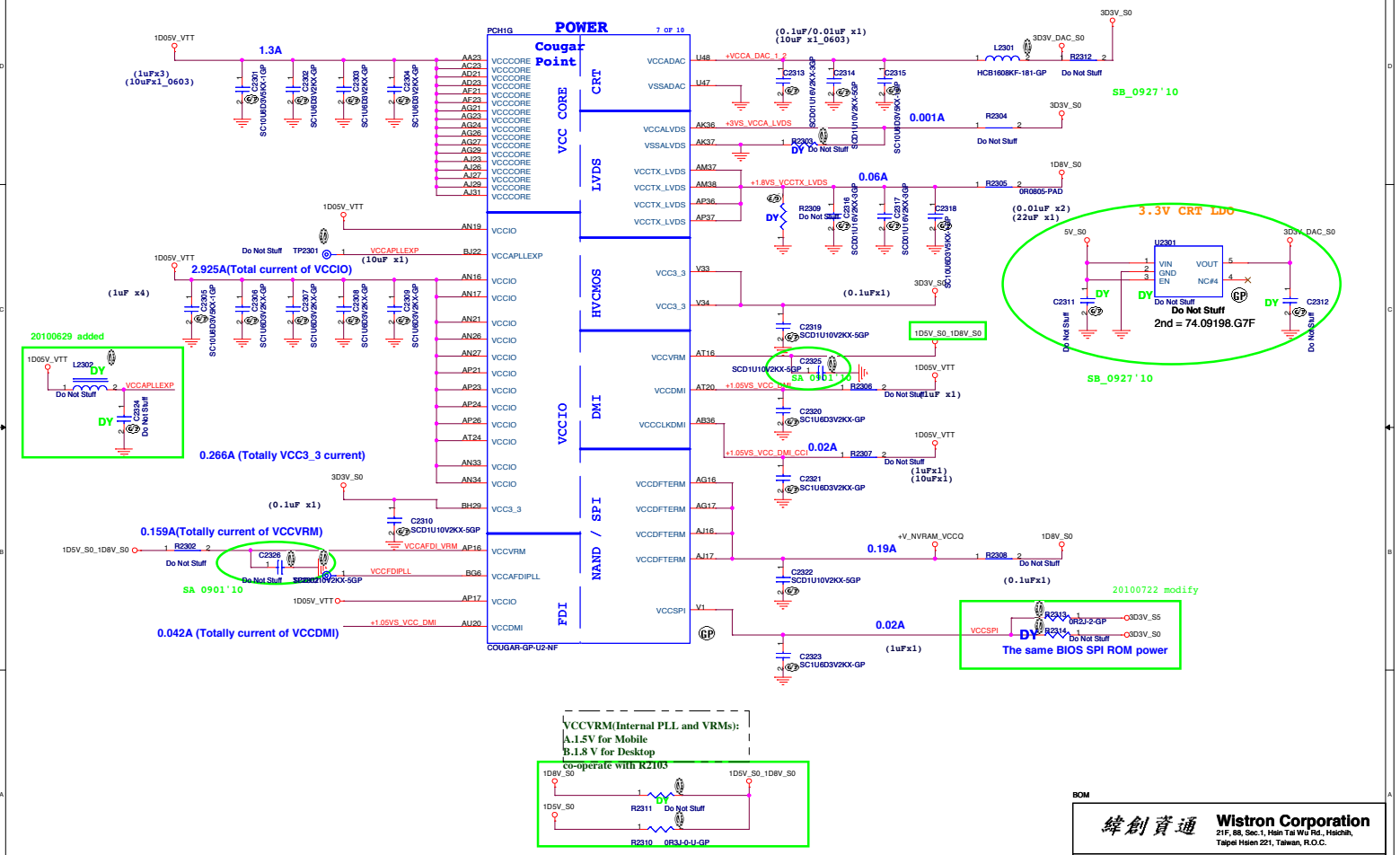
SSID = PCH 6A



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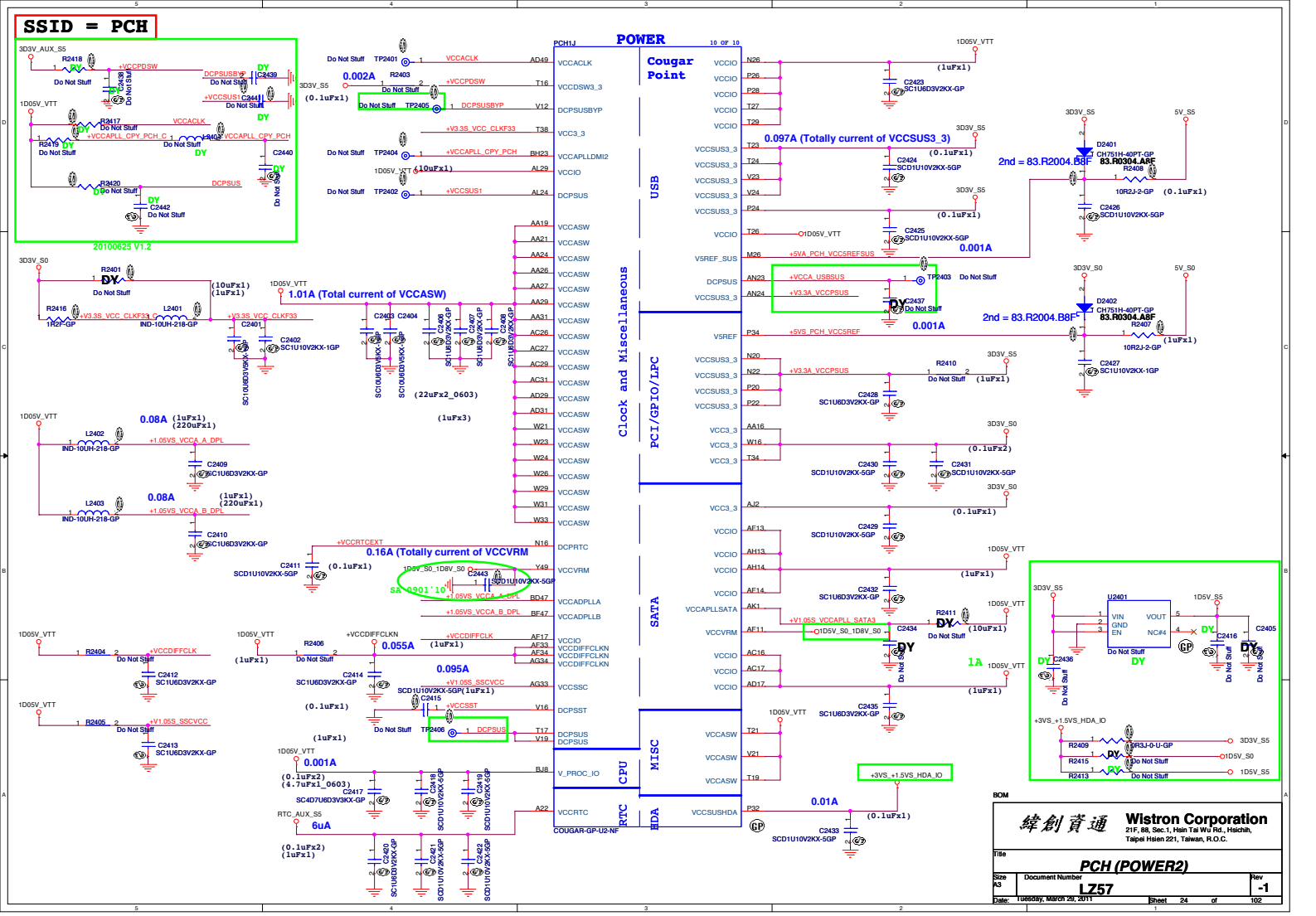
Title: **PCH (POWER1)**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 23 of 102



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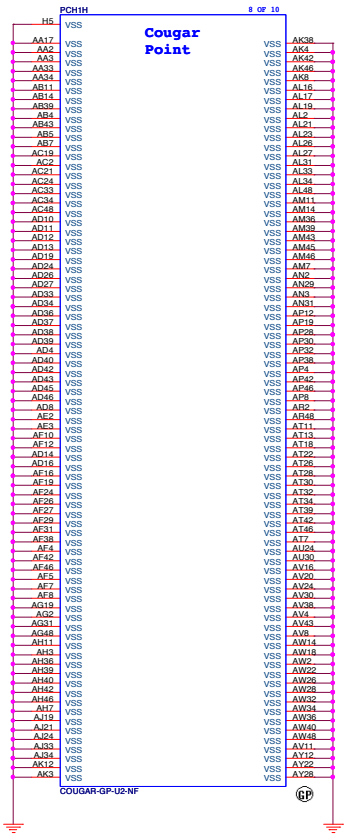
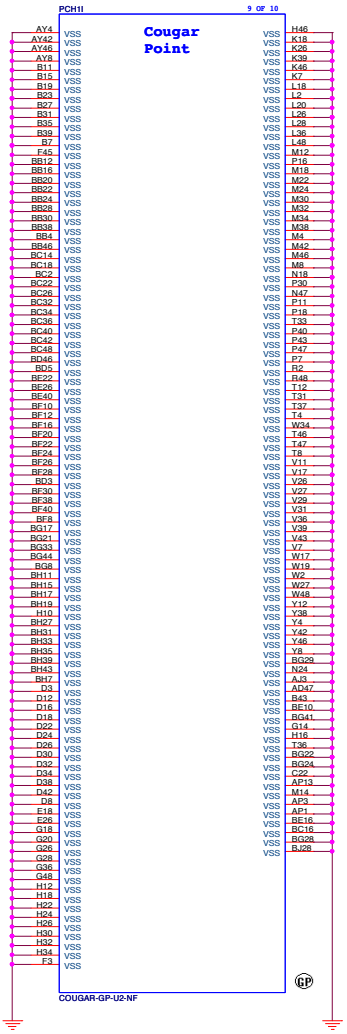
SSID = PCH





BOM

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Title	***PCH (VSS)***
Size A3 / Document Number	**LZ57**
Rev	**-1**
Date: Tuesday, March 29, 2011	Sheet 25 of 102

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Title	***Reserved***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 26 of 102

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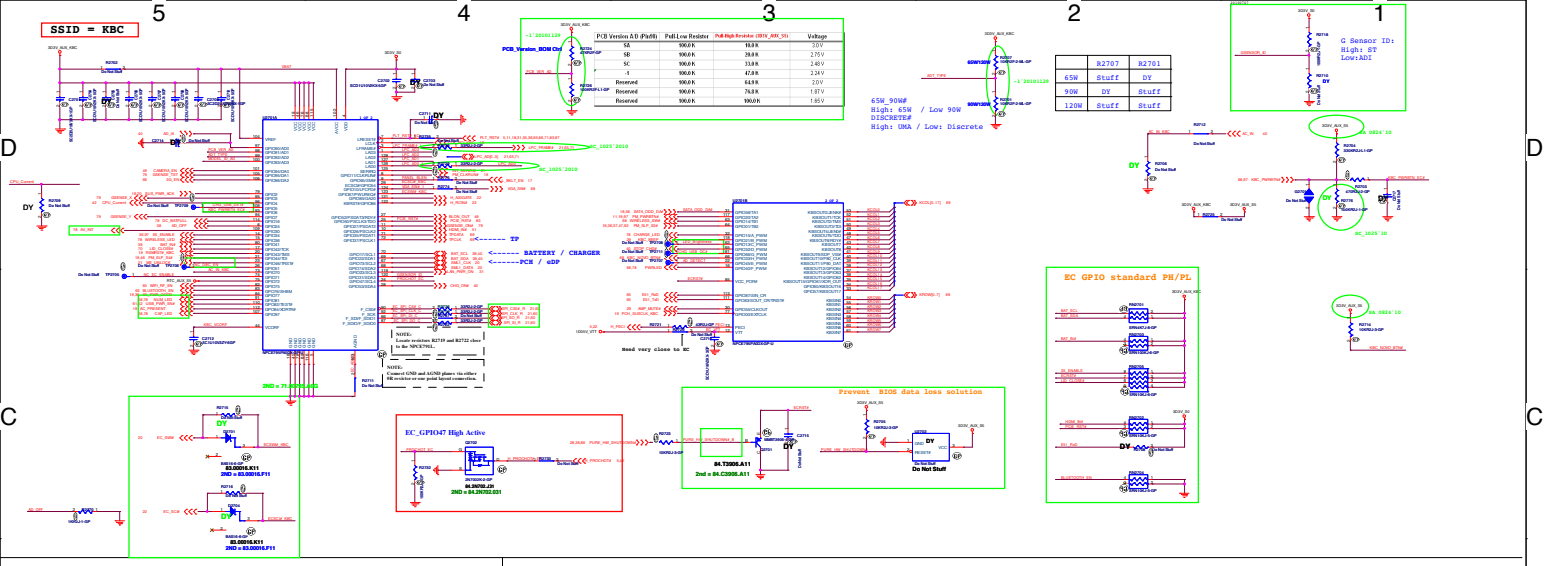


PCB Version A/D (Pin59)	Pull Low Resister	Pull High Resister (BTU_REV_S1)	Voltage
SA	100.0 K	10.0 K	3.0 V
SB	100.0 K	20.0 K	2.70 V
SC	100.0 K	33.0 K	2.48 V
1	100.0 K	47.0 K	2.24 V
Reserved	100.0 K	64.9 K	2.0 V
Reserved	100.0 K	76.8 K	1.87 V
Reserved	100.0 K	100.0 K	1.65 V

	R2707	R2701
65W	Stuff	DY
90W	DY	Stuff
120W	Stuff	Stuff

LILI Multi GPIO setting

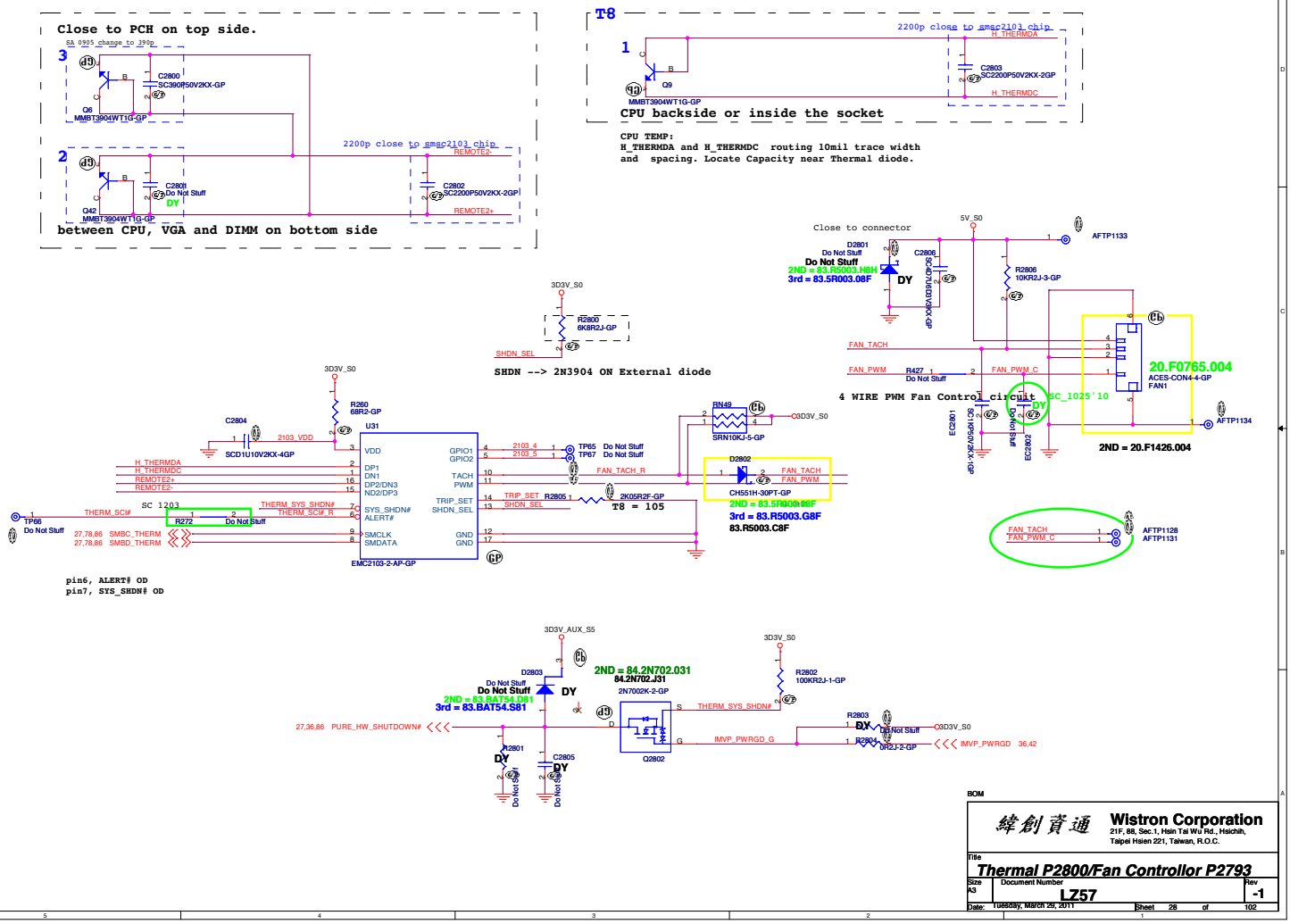
Model_ID_BOM Ctrl OPS: 84.14335.8DL

MODEL_ID_AD(Pin100)	Pull-Low Resister	Pull-High Resister	Voltage
V/B 57 UMA	100.0 K	64.9 K	2.001 V
V/B 57 OPTIMUS	100.0 K	76.8 K	1.867 V
E 57 UMA	100.0 K	100.0 K	1.650 V
E 57 OPTIMUS	100.0 K	143.0 K(64.14335.L0L)	1.32 V

緯創資通	Wistron Corporation
Title	KBC Nuvoton NPCE785
Size	A3
Document Number	L257
Rev	-1

SSID = Thermal

Thermal sensor



BOM

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Title	***Thermal P2800/Fan Controllor P2793***
Size A3 / Document Number	LZ57 / Rev -1
Date: Tuesday, March 29, 2011	Sheet 28 of 102

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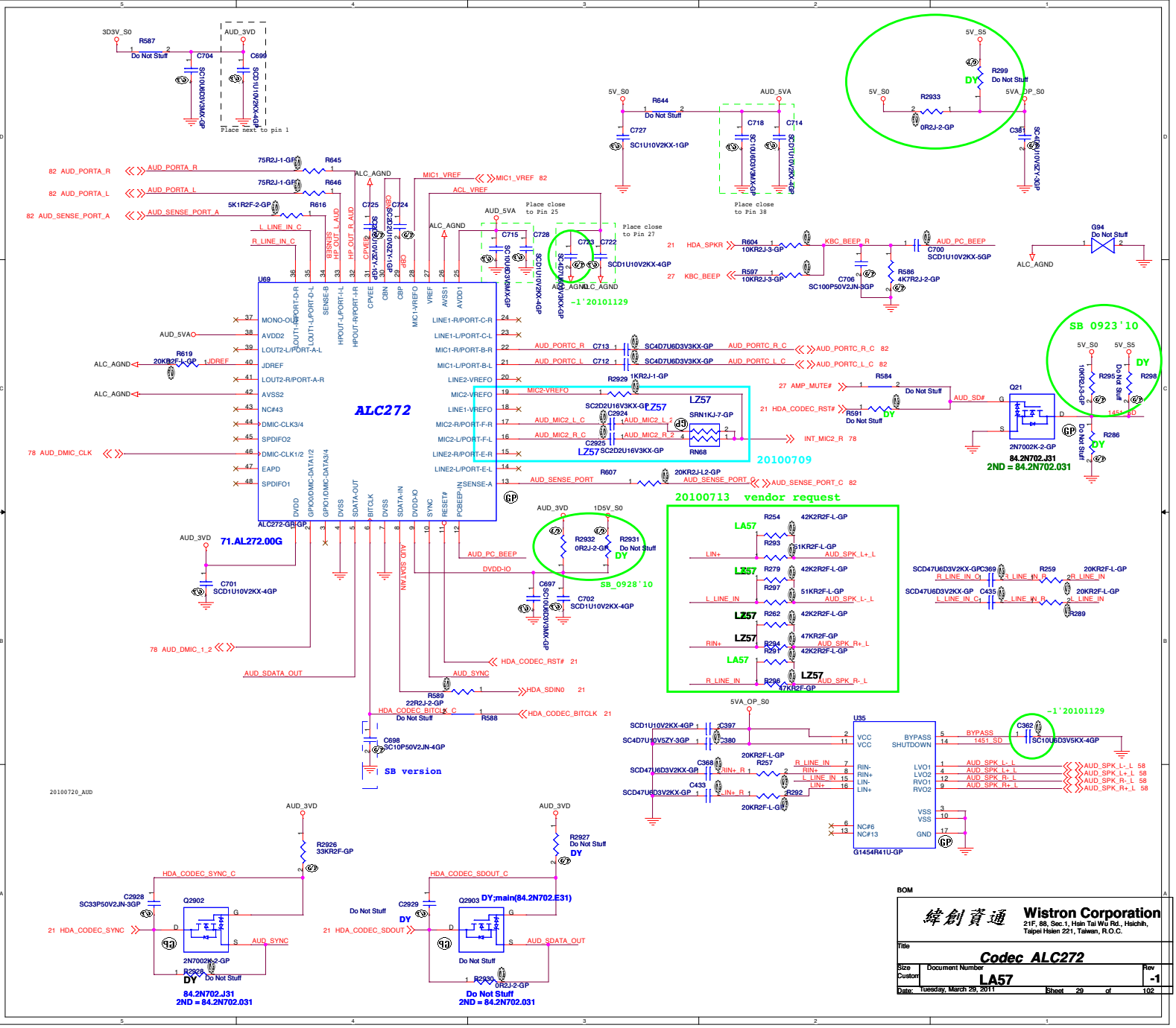

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Codec ALC272
Size / Custom	Document Number: LA57
Rev	-1
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Title	***reserved***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 30 of 102

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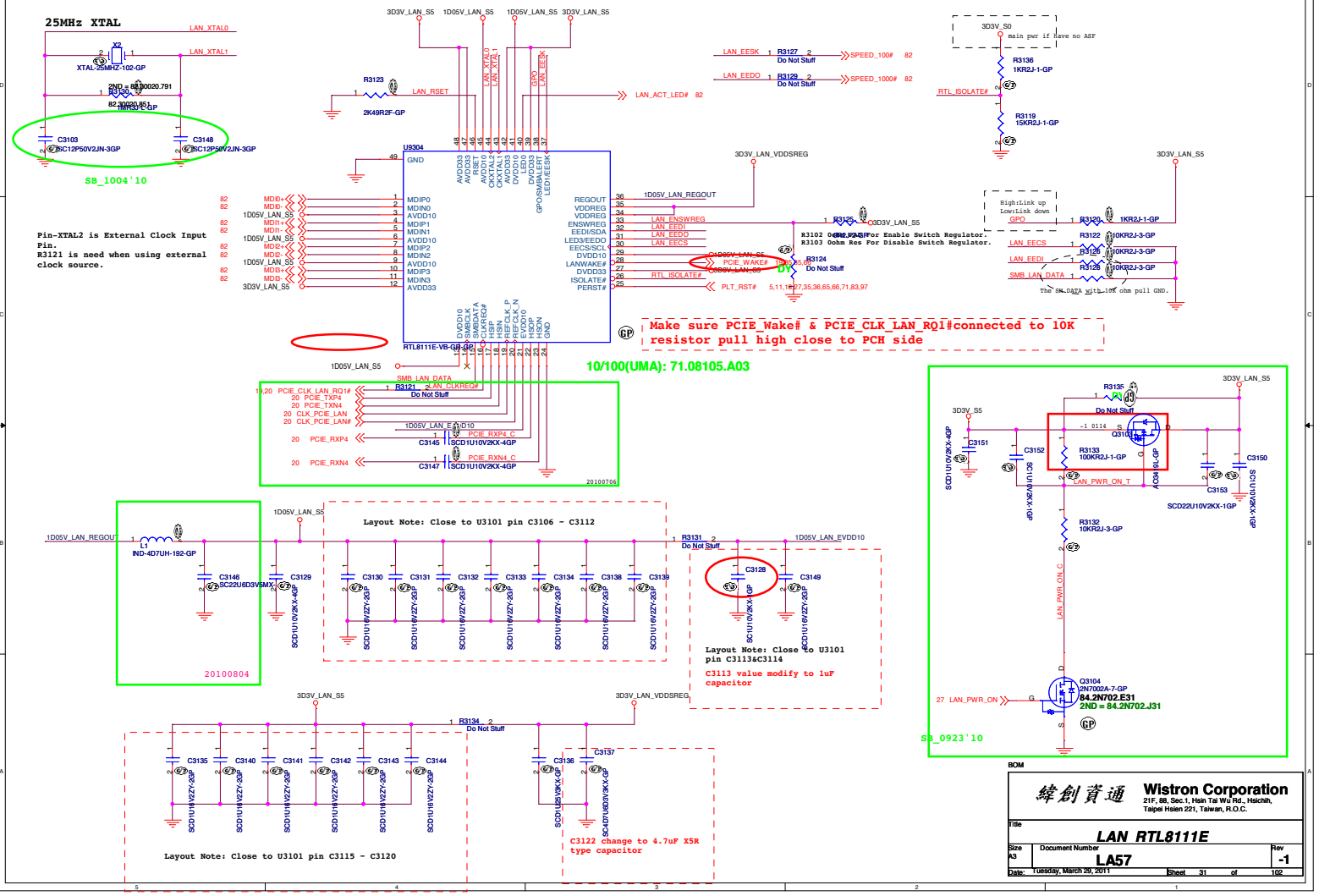

BOM

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Title	LAN RTL8111E	
Size A3	Document Number LA57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 31 of 102	

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RTS5159 (CARD READER)***
Size A3	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 32 of 102

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Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 33 of 102

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Title	***Reserved***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 34 of 102

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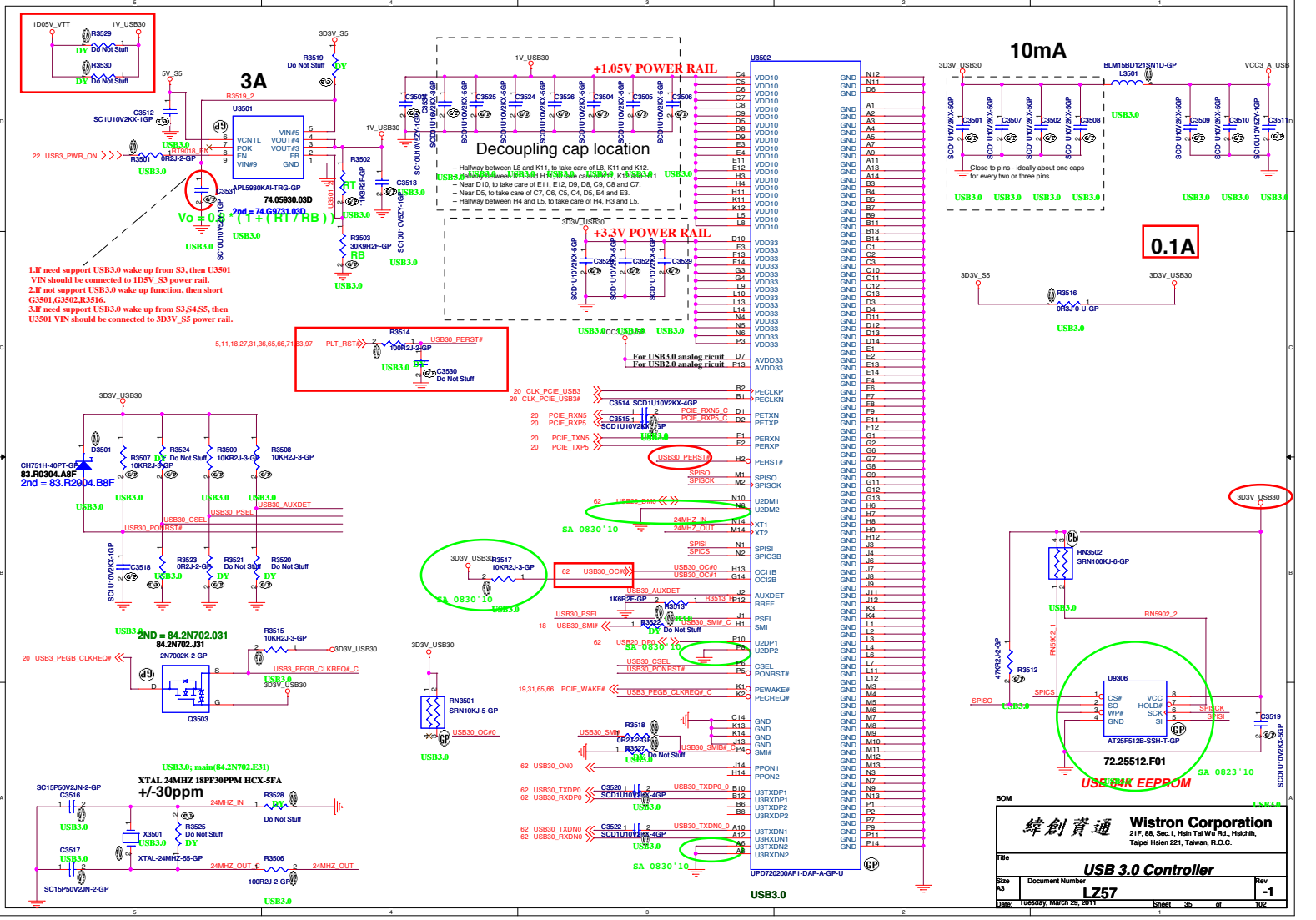
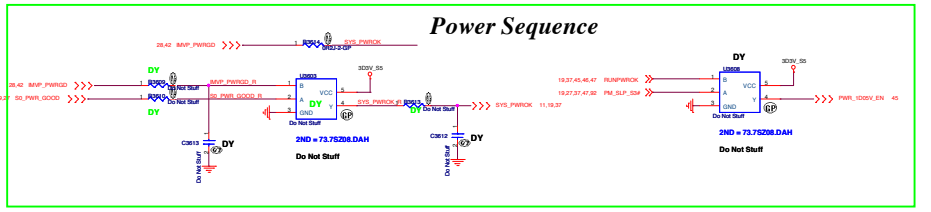
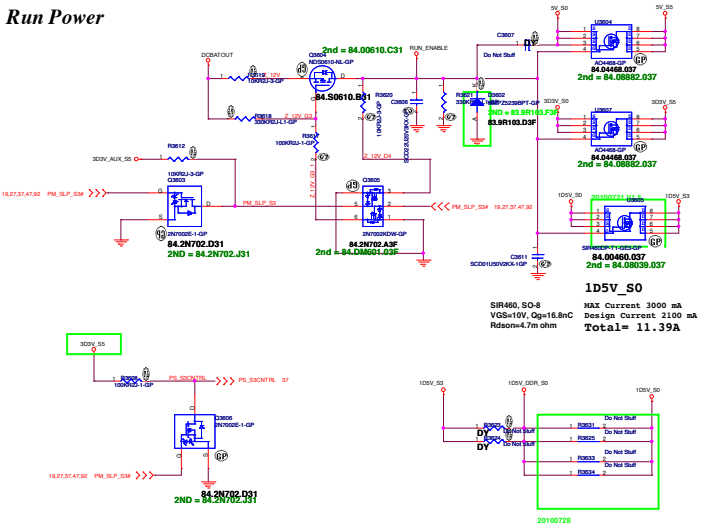
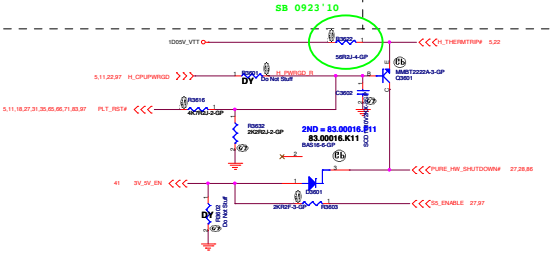

3A
10mA
0.1A
+1.05V POWER RAIL
+3.3V POWER RAIL
Decoupling cap location
-- Halfway between L8 and K11, to take care of L8, K11 and K12.
-- Halfway between K11 and H11, to take care of K11, K12 and H11.
-- Near D10, to take care of E11, E12, D9, D8, C9, C8 and C7.
-- Near D5, to take care of C7, C6, C5, C4, D5, E4 and E3.
-- Halfway between H4 and L5, to take care of H4, H3 and L5.
Close to pins - ideally about one caps for every two or three pins
1.If need support USB3.0 wake up from S3, then U3501 VIN should be connected to 1D5V_S3 power rail.
2.If not support USB3.0 wake up function, then short G3501,G3502,R3516.
3.If need support USB3.0 wake up from S3,S4,S5, then U3501 VIN should be connected to 3D3V_S5 power rail.
Vo = 0.8 * (1 + (RT / RB))
2nd = 74.G9731.03D
74.05930.03D
APL5930KAI-TRG-GP
2ND = 84.2N702.031
84.2N702.J31
2N7002K-2-GP
CH751H-40PT-GP
83.R0304.A8F
2nd = 83.R2004.B8F
XTAL 24MHZ 18PF30PPM HCX-5FA
+/-30ppm
USB3.0; main(84.2N702.E31)
USB3.0
For USB3.0 analog ricuit
For USB2.0 analog ricuit
U3502
UPD720200AF1-DAP-A-GP-U
U3501
U3306
AT25F512B-SSH-T-GP
72.25512.F01
USB 64K EEPROM
SA 0830'10
SA 0823'10
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
USB 3.0 Controller
Size A3
Document Number LZ57
Rev -1
Date: Tuesday, March 29, 2011
Sheet 35 of 102



SSID = Reset.Suspend



SB 0923'10



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Power Plane Enable
Size A2	Document Number LZ57
Rev -1	
Date: Tuesday, March 29, 2011	Sheet 36 of 50

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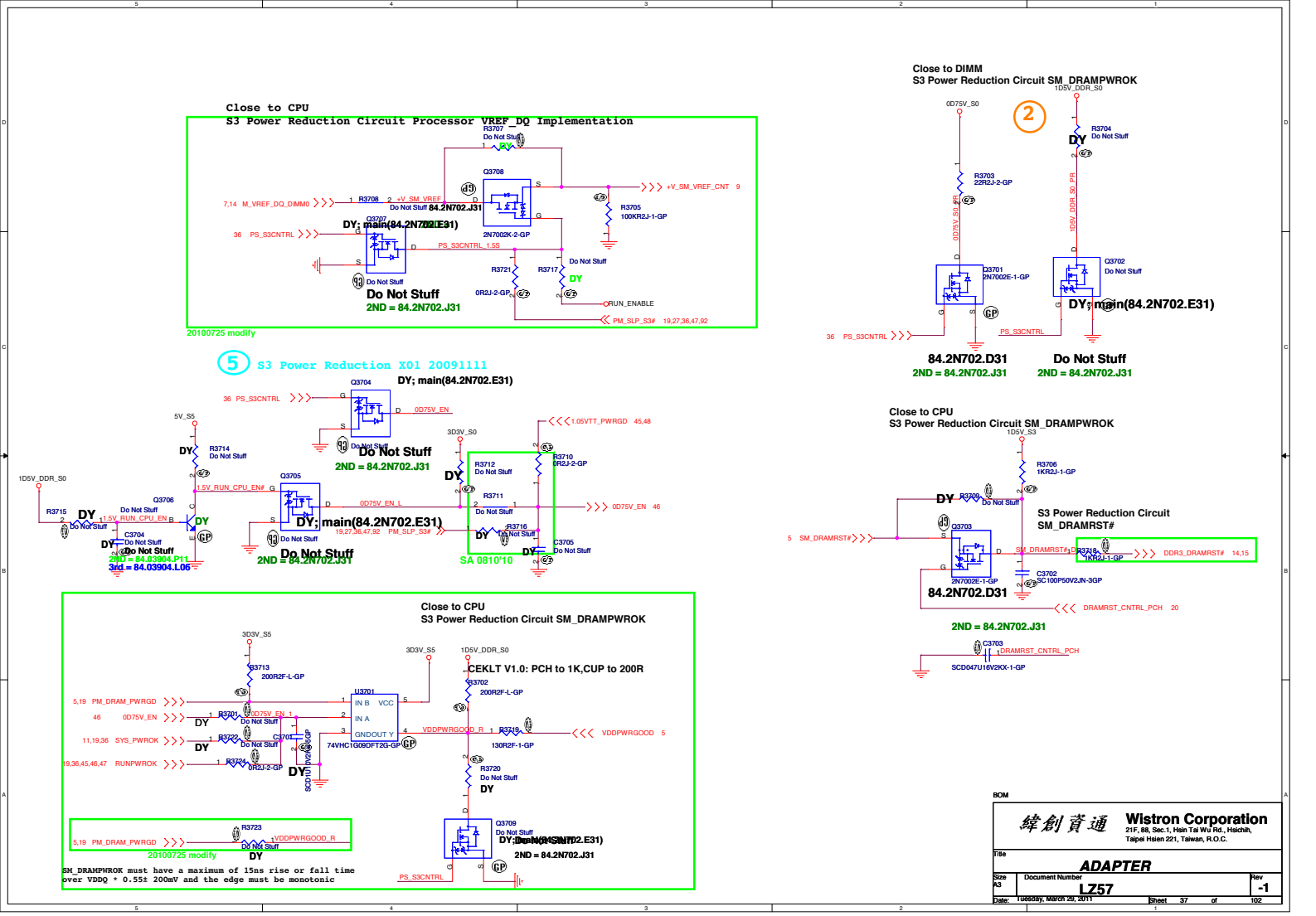
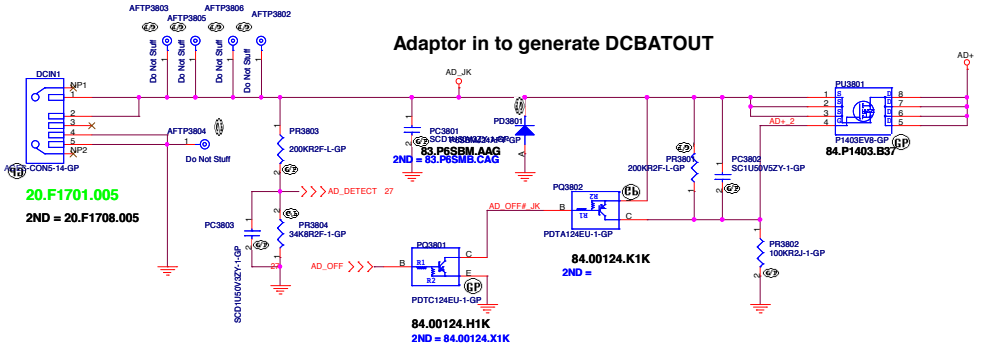


BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ADAPTER**
Size A3	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 37 of 102



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Title	***DCIN_JACK***
Size / Document Number	**LZ57**
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 38 of 102

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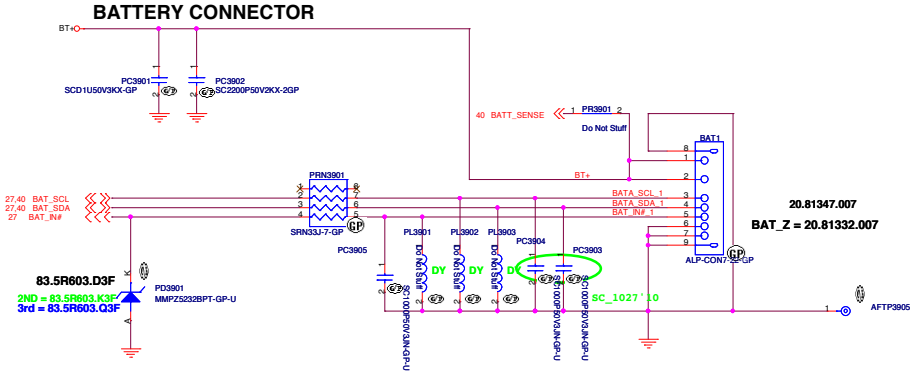
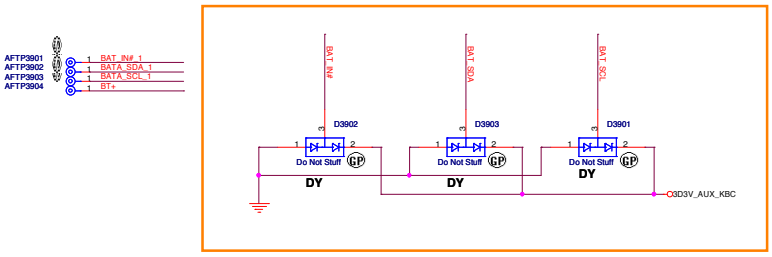
BATTERY CONNECTOR

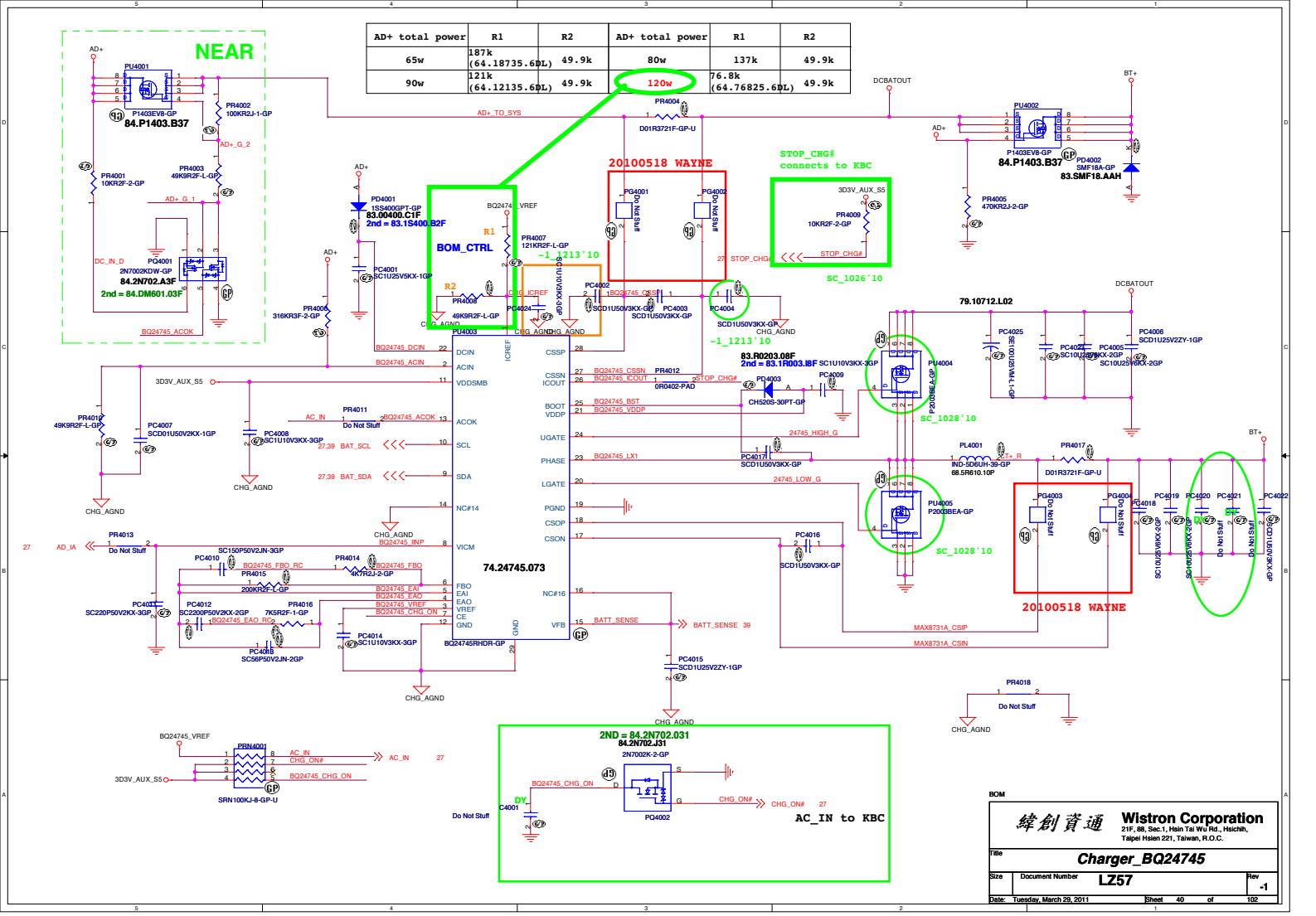




BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	BATT_CONN	
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k (64.18735.6DL)	49.9k	80w	137k	49.9k
90w	121k (64.12135.6DL)	49.9k	120w	76.8k (64.76825.6DL)	49.9k



BOM

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Title: Charger_BQ24745

Size | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 40 of 102

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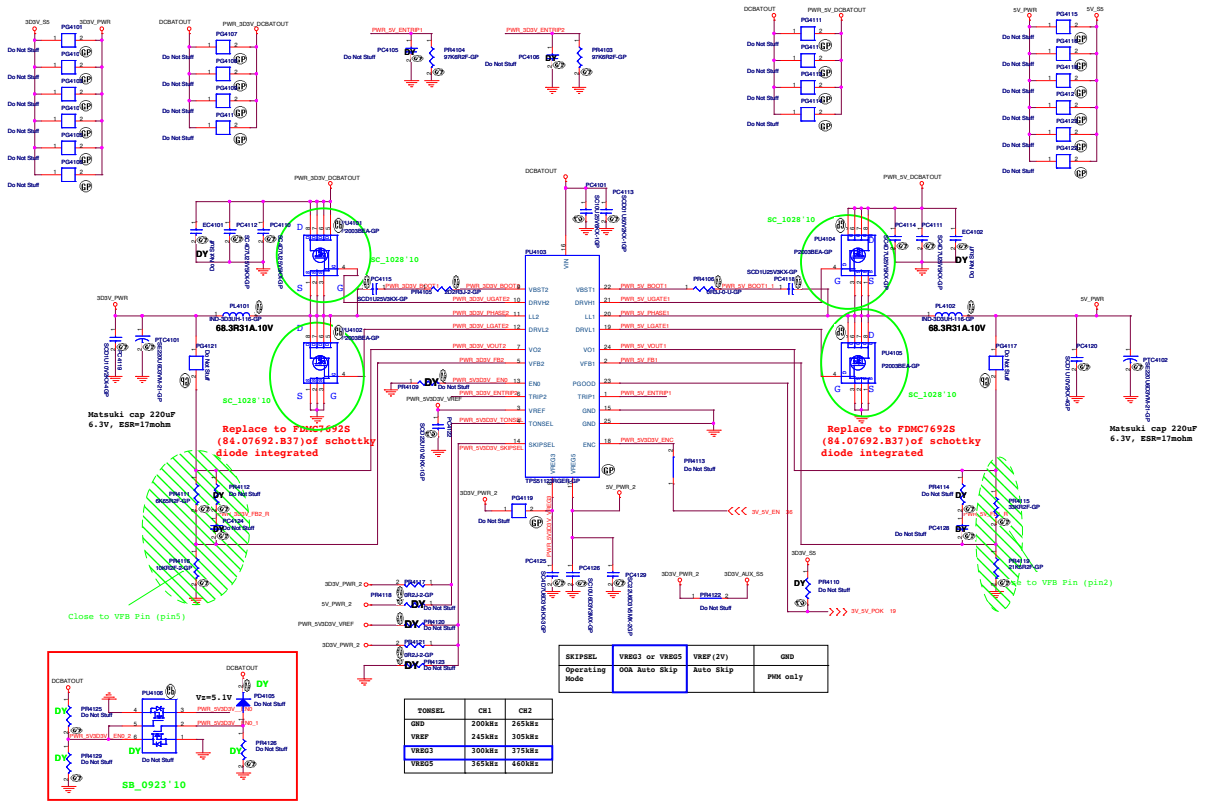
SSID = PWR.Plane.Regulator_5v3p3v



SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

BOM

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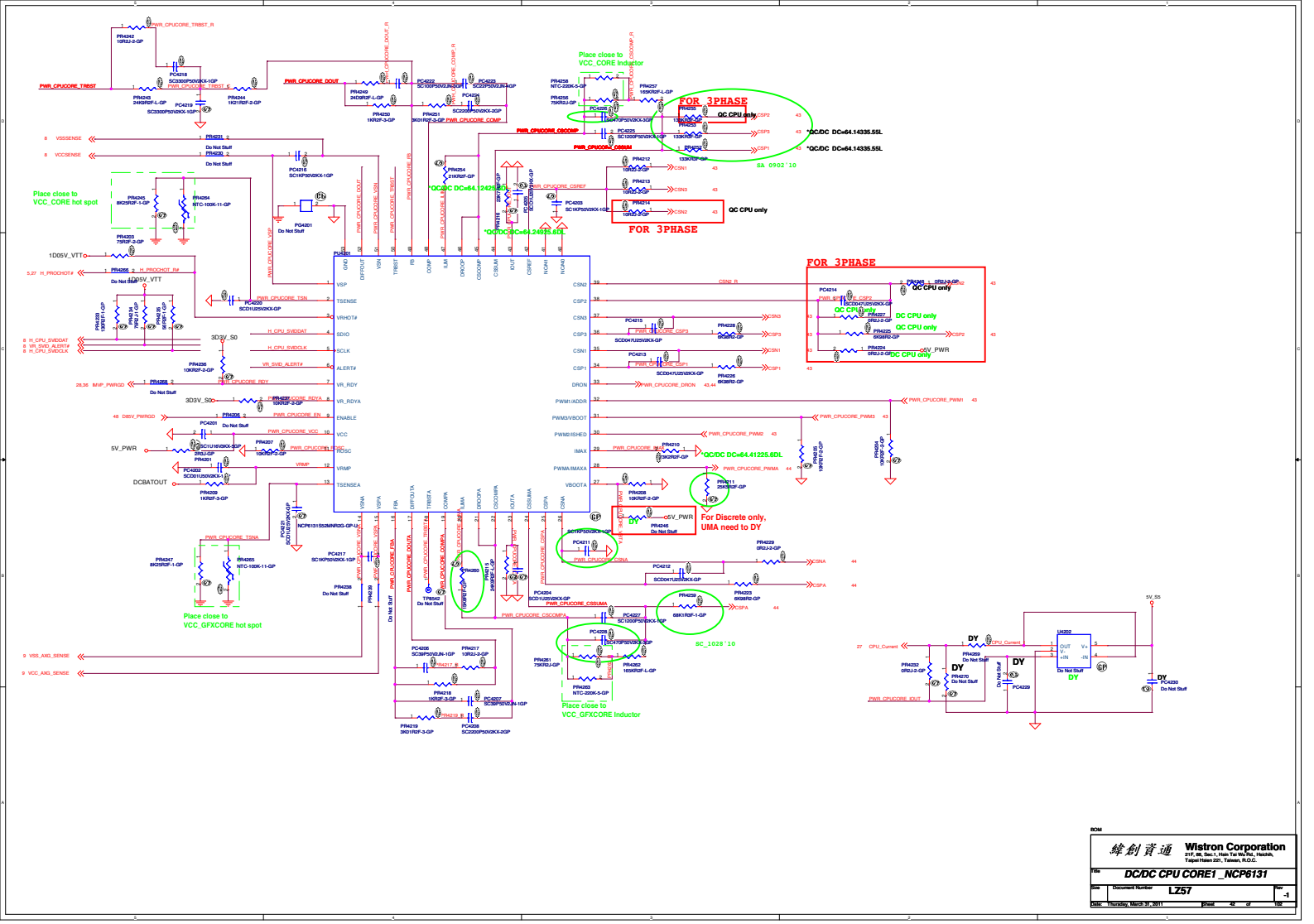
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DC/DC 3D3V5V

Size | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 41 of 102



BOM

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC CPU CORE1 _NCP6131		
Size	Document Number: LZ57	Rev: -1
Date: Thursday, March 31, 2011	Sheet 43 of 102	

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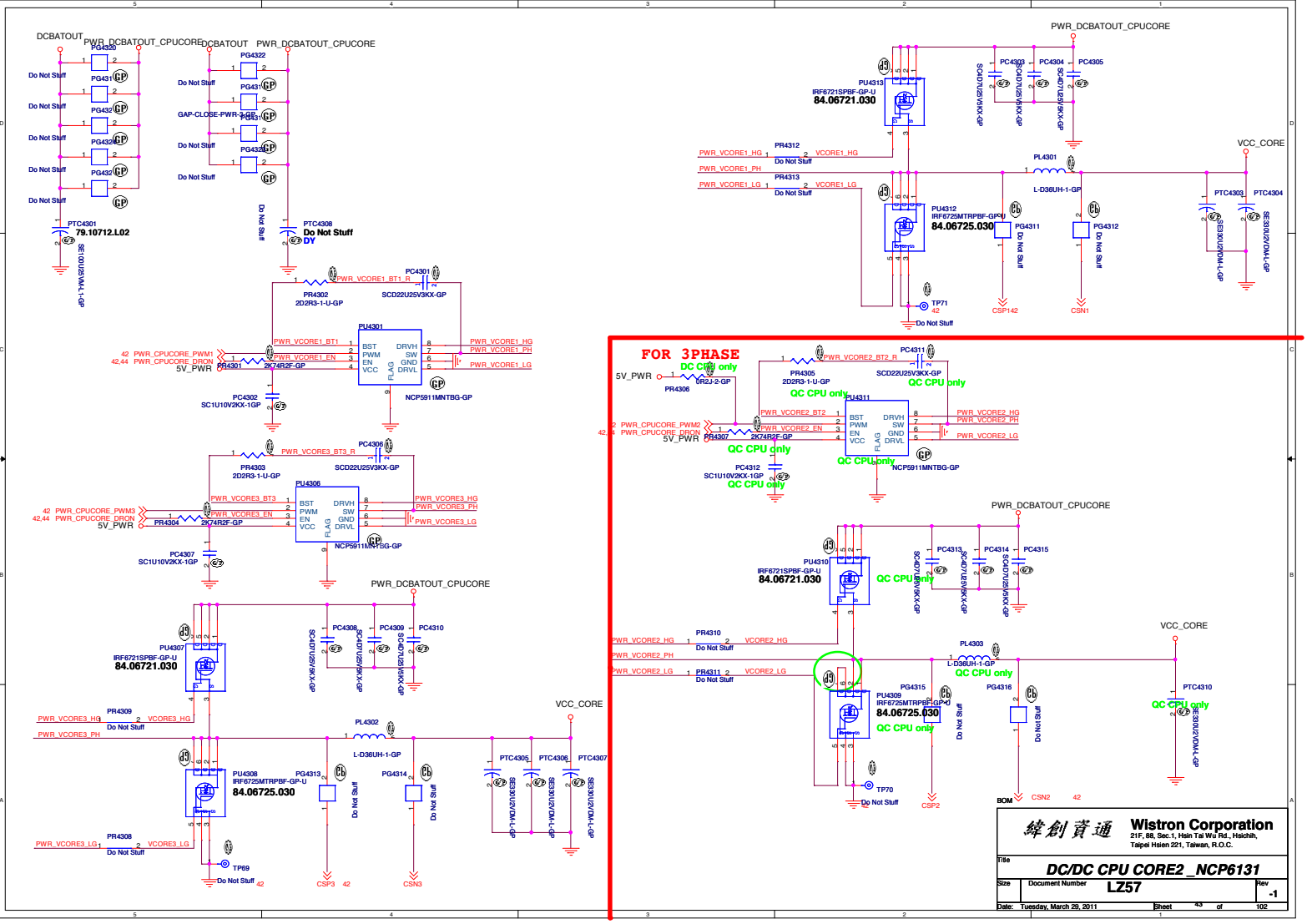
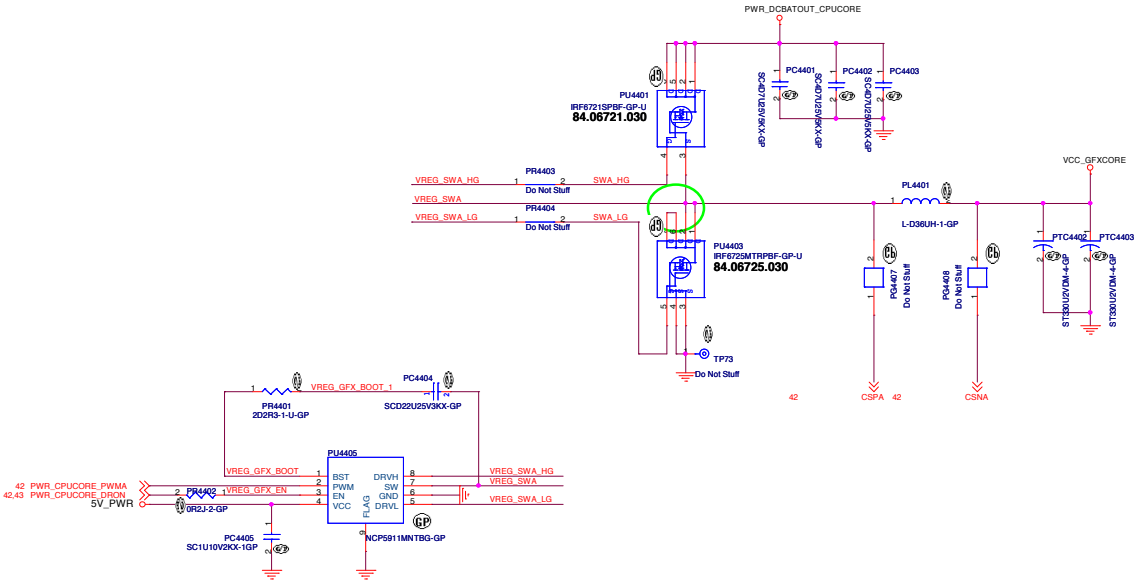

DCBATOUT
PWR_DCBATOUT_CPUCORE
PG4320
PG4321
PG4322
PG4323
PG4324
PG4325
PG4326
PG4327
PG4328
PG4329
GAP-CLOSE-PWR-3-GP
Do Not Stuff
PTC4301
79.10712.L02
SE100U25VM4-1-GP
PTC4308
DY
PC4301
SCD22U25V3KX-GP
PR4302
2D2R3-1-U-GP
PU4301
NCP5911MNTBG-GP
PWR_VCORE1_BT1
PWR_VCORE1_BT1_R
PWR_VCORE1_EN
PWR_VCORE1_HG
PWR_VCORE1_PH
PWR_VCORE1_LG
42 PWR_CPUCORE_PWM1
42,44 PWR_CPUCORE_DRON
5V_PWR
PR4301
2K74R2F-GP
PC4302
SC1U10V2KX-1GP
PC4306
PR4303
2D2R3-1-U-GP
PU4306
PWR_VCORE3_BT3
PWR_VCORE3_BT3_R
PWR_VCORE3_EN
PWR_VCORE3_HG
PWR_VCORE3_PH
PWR_VCORE3_LG
42 PWR_CPUCORE_PWM3
42,44 PWR_CPUCORE_DRON
PR4304
2K74R2F-GP
PC4307
SC1U10V2KX-1GP
PU4307
IRF6721SPBF-GP-U
84.06721.030
PC4308
PC4309
PC4310
SC4D7U25V5KX-GP
PR4309
VCORE3_HG
PR4308
VCORE3_LG
PU4308
IRF6725MTRPBF-GP-U
84.06725.030
PG4313
PG4314
PL4302
L-D36UH-1-GP
VCC_CORE
PTC4305
PTC4306
PTC4307
SE330U2VDM-1-GP
TP69
CSP3
CSN3
PU4313
IRF6721SPBF-GP-U
84.06721.030
PC4303
PC4304
PC4305
PR4312
VCORE1_HG
PR4313
VCORE1_LG
PL4301
L-D36UH-1-GP
PU4312
IRF6725MTRPBF-GP-U
84.06725.030
PG4311
PG4312
PTC4303
PTC4304
TP71
CSP142
CSN1
FOR 3PHASE
DC CPU only
QC CPU only
5V_PWR
PR4306
0R2J-2-GP
PR4305
2D2R3-1-U-GP
PC4311
SCD22U25V3KX-GP
PU4311
NCP5911MNTBG-GP
PWR_VCORE2_BT2
PWR_VCORE2_BT2_R
PWR_VCORE2_EN
PWR_VCORE2_HG
PWR_VCORE2_PH
PWR_VCORE2_LG
42 PWR_CPUCORE_PWM2
42,44 PWR_CPUCORE_DRON
PR4307
2K74R2F-GP
PC4312
SC1U10V2KX-1GP
PU4310
IRF6721SPBF-GP-U
84.06721.030
PC4313
PC4314
PC4315
PR4310
VCORE2_HG
PR4311
VCORE2_LG
PL4303
L-D36UH-1-GP
PU4309
IRF6725MTRPBF-GP-U
84.06725.030
PG4315
PG4316
PTC4310
SE330U2VDM-1-GP
TP70
CSP2
CSN2
BOM
42
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC CPU CORE2 _NCP6131
Size
Document Number
LZ57
Rev
-1
Date: Tuesday, March 29, 2011
Sheet 43 of 102



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DC/DC CPU CORE3 _NCP6131***	
Size	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 44 of 102	

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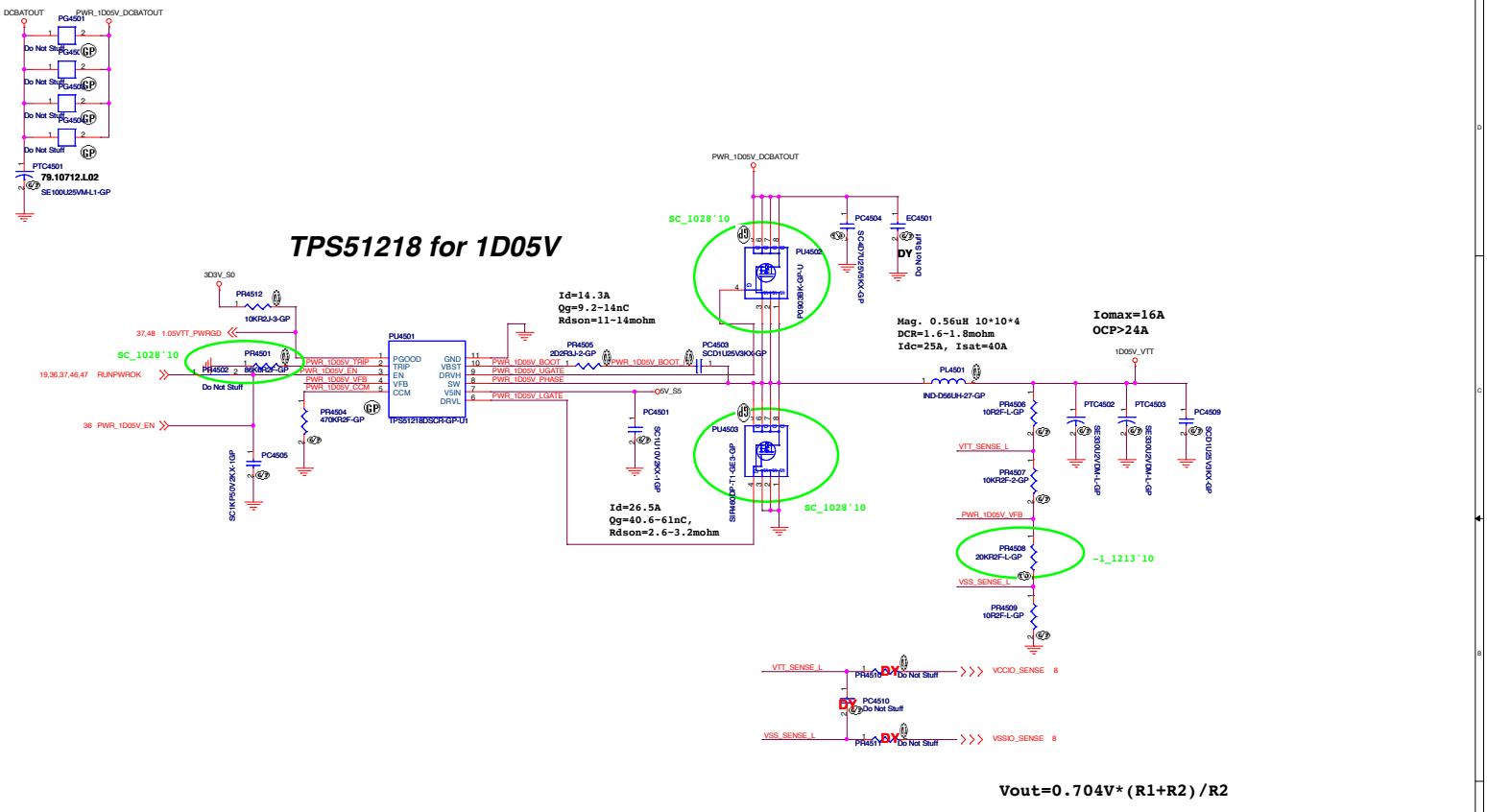
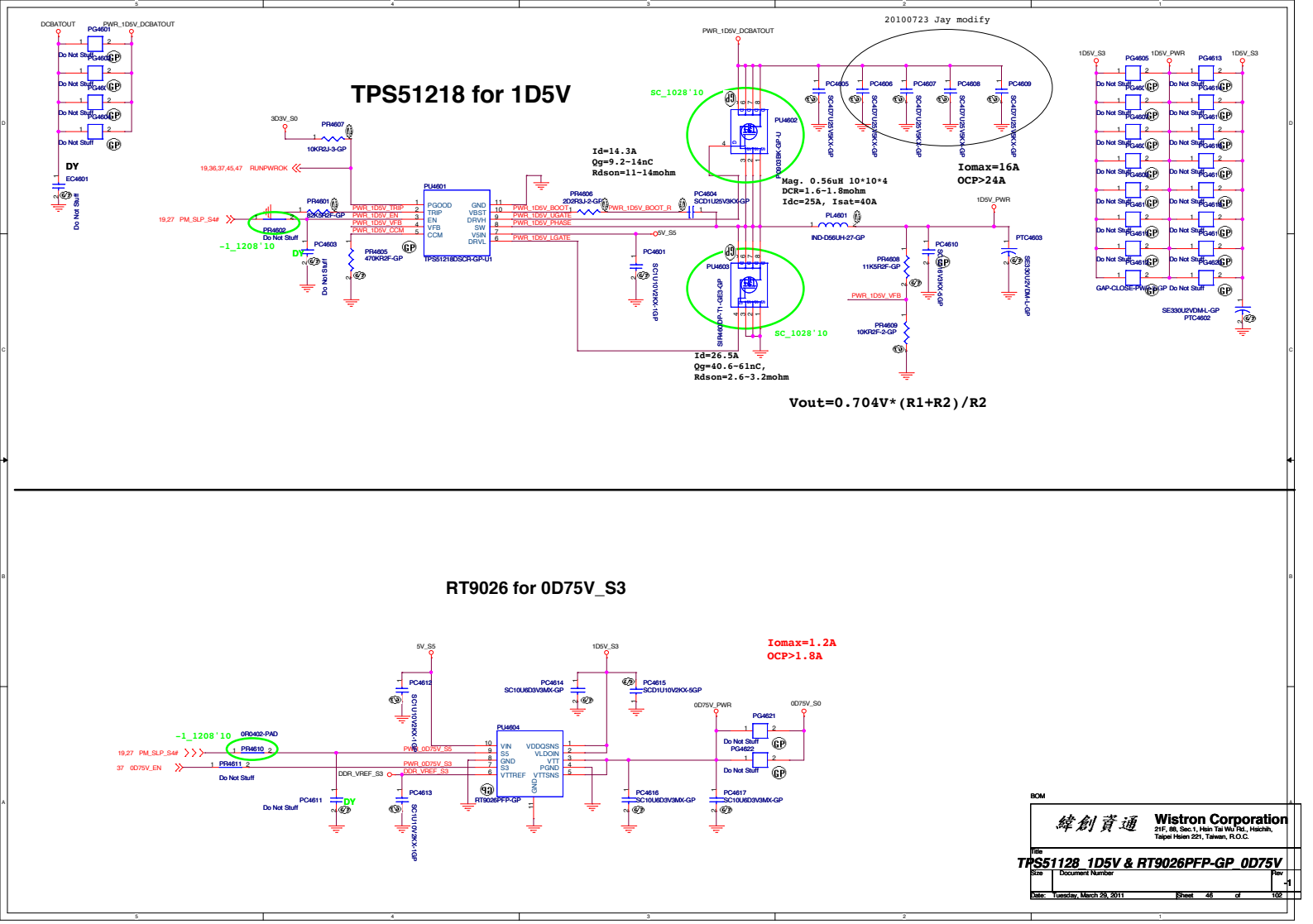


BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPS51218_1D05V***	
Size	Document Number	Rev -1
Date: Tuesday, March 29, 2011	Sheet 45 of 102	



BOM

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51128_1D5V & RT9026PFP-GP_0D75V

Size | Document Number | Rev -1

Date: Tuesday, March 29, 2011 | Sheet 46 of 102

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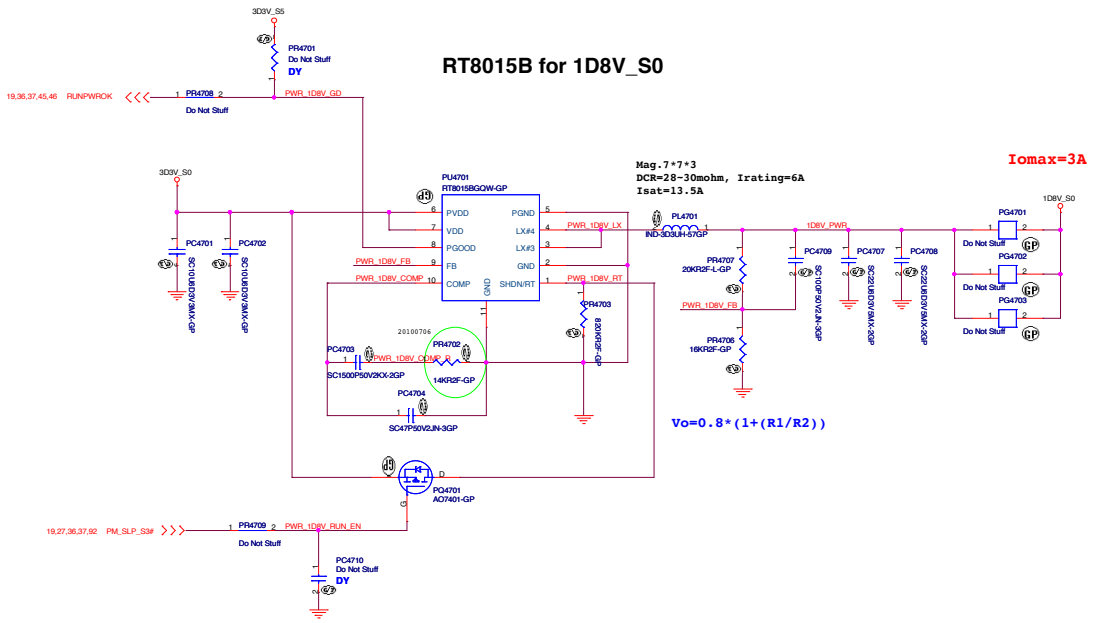
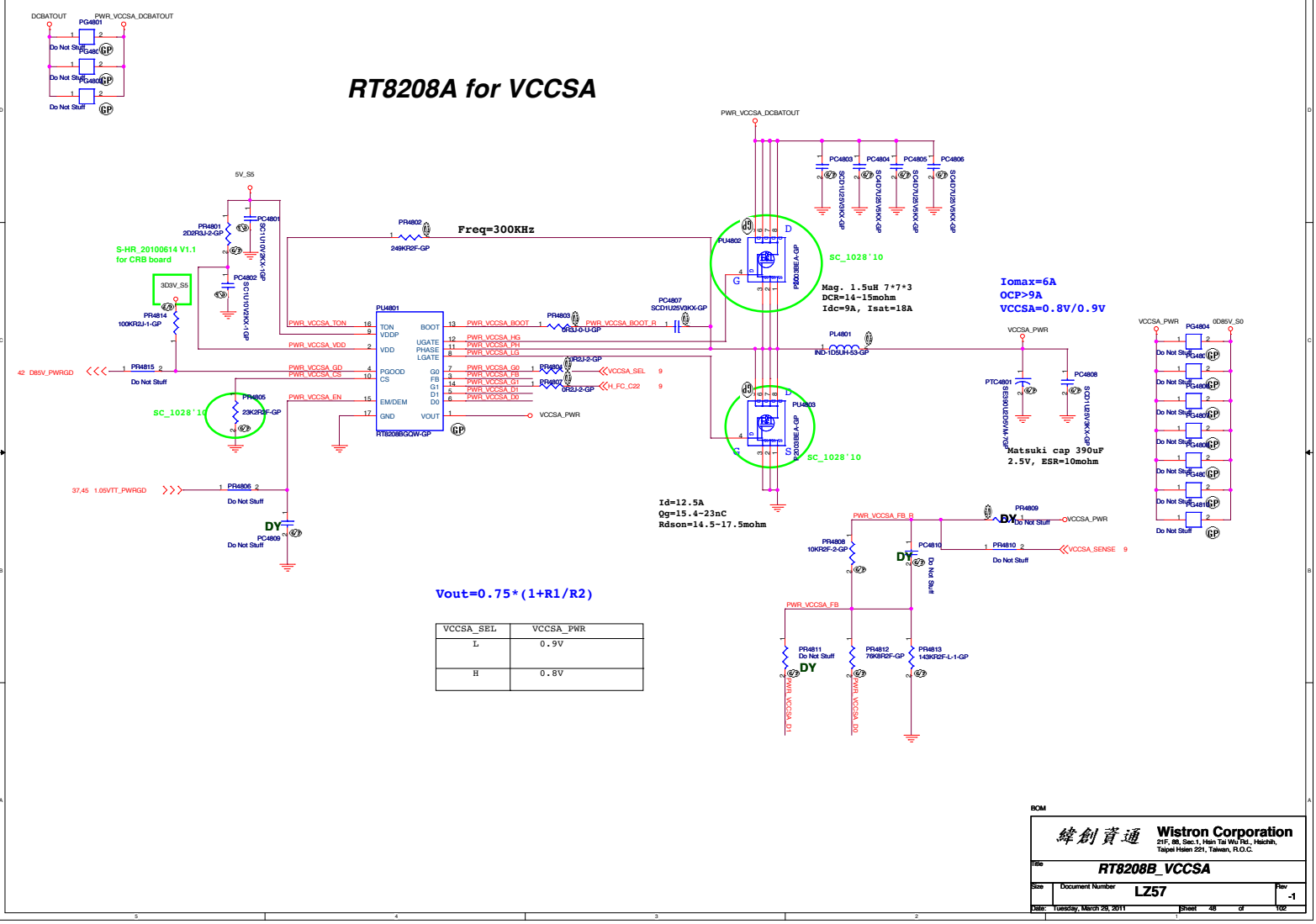
RT9025 for 1D8V_S0



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	1D8V_RT9025	
Size	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 47 of 102	

RT8208A for VCCSA



Vout=0.75*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_VCCSA

Size: | Document Number: LZ57 | Rev: -1

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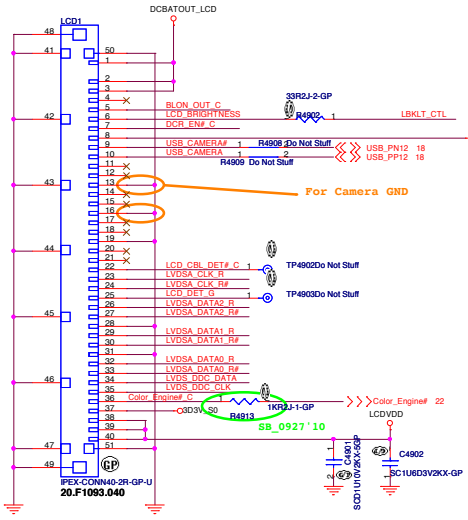
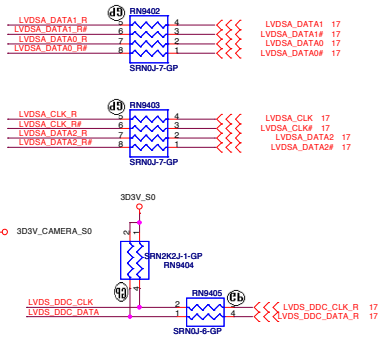
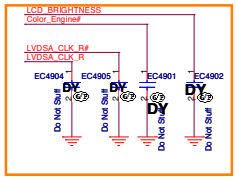
SSID = VIDEO

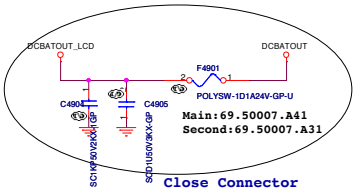
LVDS CONNECTOR

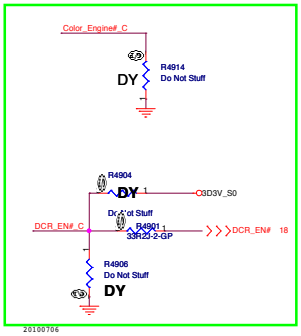




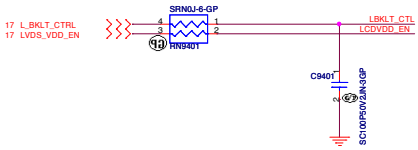
For EMI request
Close to LVDS connector



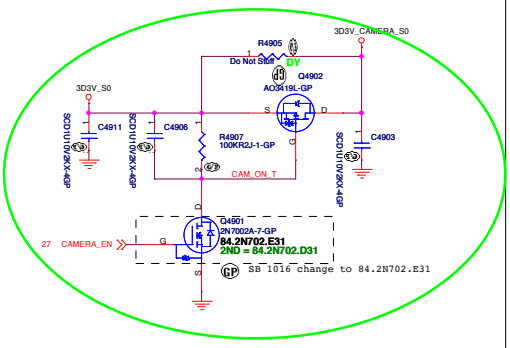




Panel BL brightness/Power En/BL En

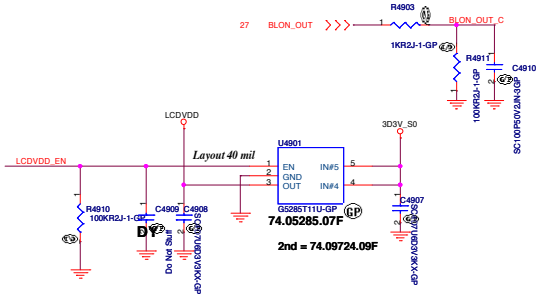


CAMERA POWER



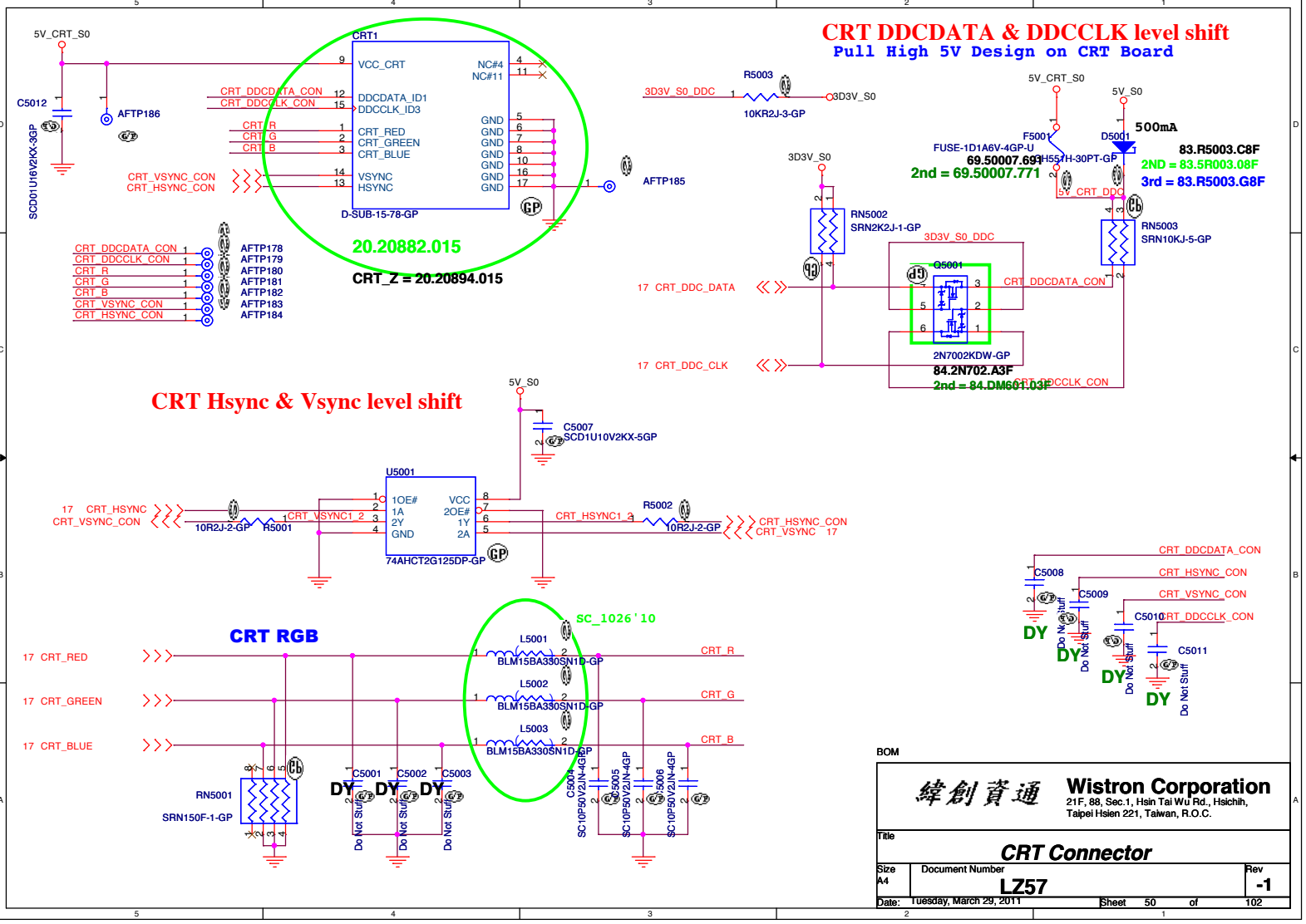
SB 0923'10

SSID = VIDEO



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LCD Connector
Size A3	Document Number LZ57 Rev -1
Date: Tuesday, March 29, 2011	Sheet 49 of 102



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CRT Connector	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 50 of 102	

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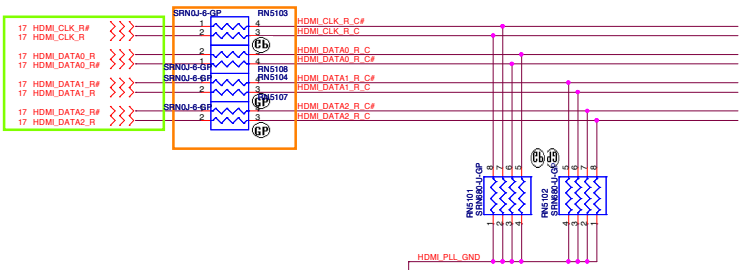
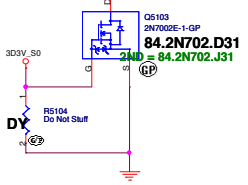
SSID = VIDEO

HDMI CONNECTOR

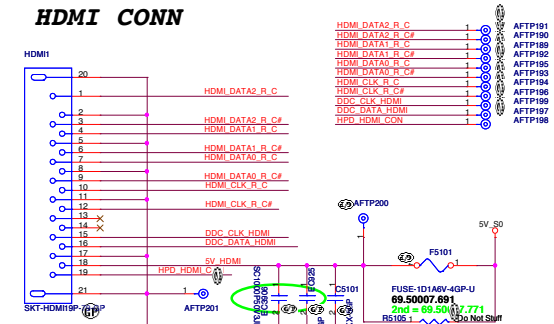
HDMI Passive Level Shifter

Close to HDMI Connector

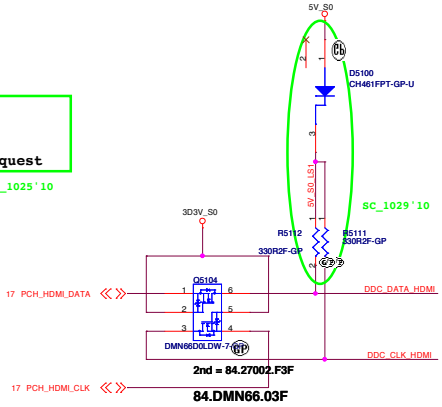




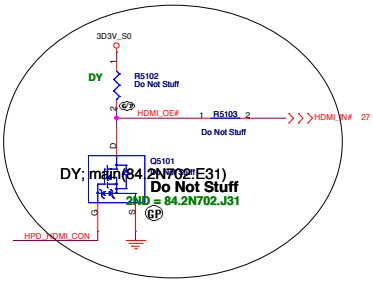
HDMI CONN



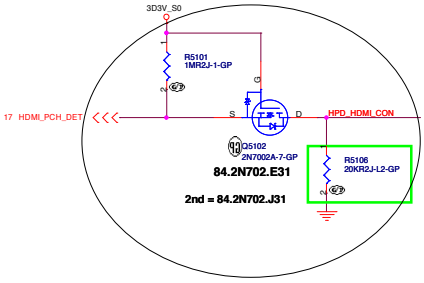
HDMI DDC Passive Level Shifter



20100727 modify, KBC isn't use.



20100727 follow intel design guide



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDMI Level Shifter/Connector	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 51 of 102	

(Blanking)

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	S-VIDEO	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 53 of 102	

(Blanking)

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Reserved	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 54 of 102	

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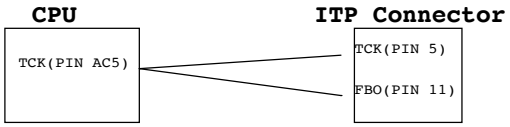
SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



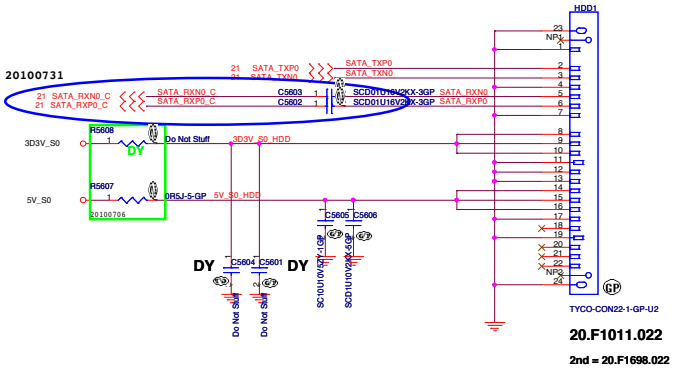
BOM

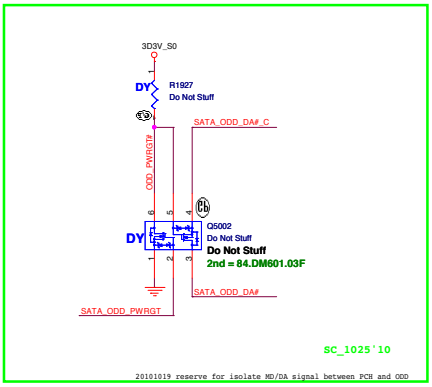
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ITP	
Size A4	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 55 of 102	

SSID = SATA

SATA HDD Connector



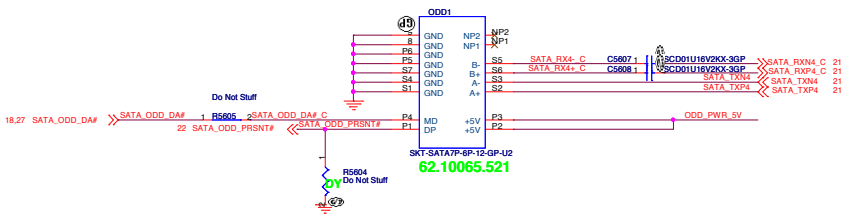


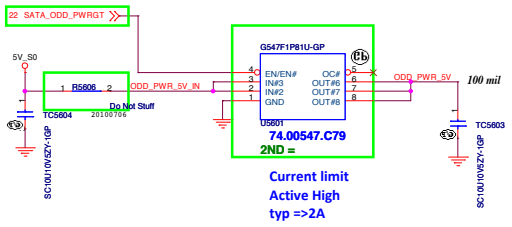
ODD Connector

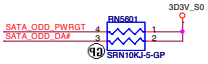
SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

SATA Zero Power ODD







SUPPORT ZERO SATA ODD

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	HDD/ODD	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 56 of 102	

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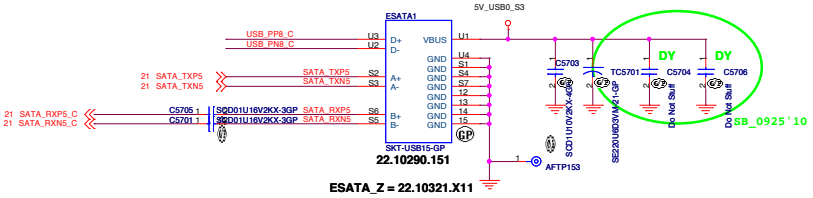
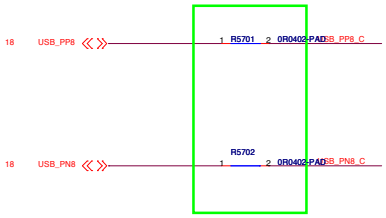
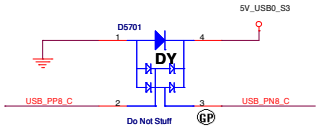
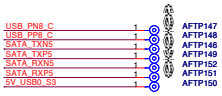


ESATA_Z = 22.10321.X11



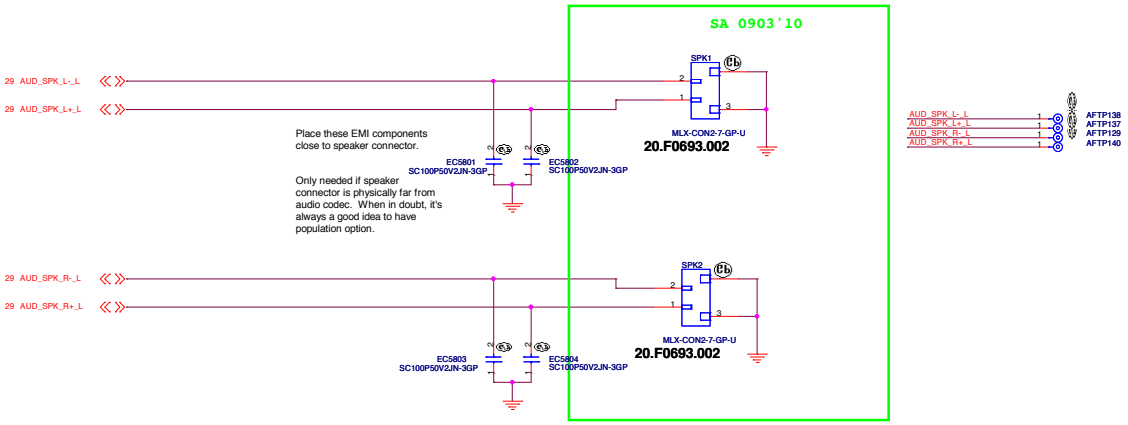




BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	E-SATA/USB	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 57 of 102	

INTERNAL STEREO SPEAKERS



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MIC/SPEAKER/AUDIO JACK***
Size A3	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 58 of 102

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Reserved

BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

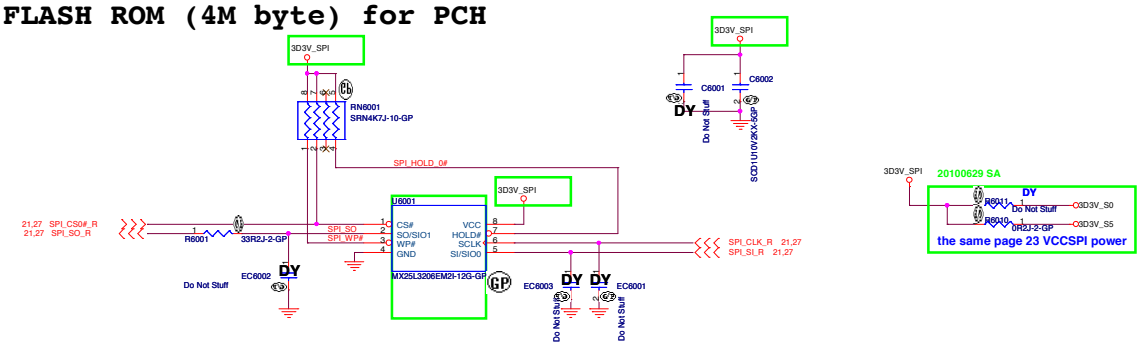
Title: Reserved

Size	Document Number	Rev
A3	LZ57	-1

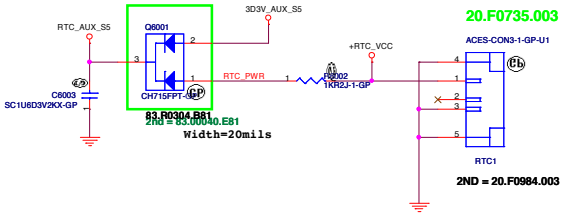
Date: Tuesday, March 29, 2011 Sheet 59 of 102

SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Flash/RTC	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 60 of 102	

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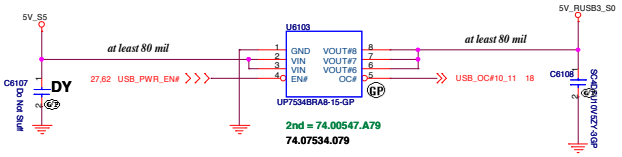
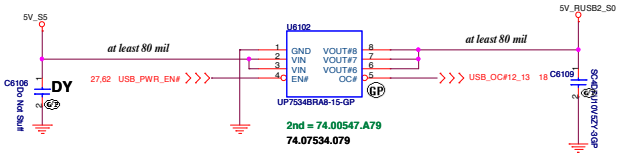
SSID = USB

RJ45_USB Board USB Power



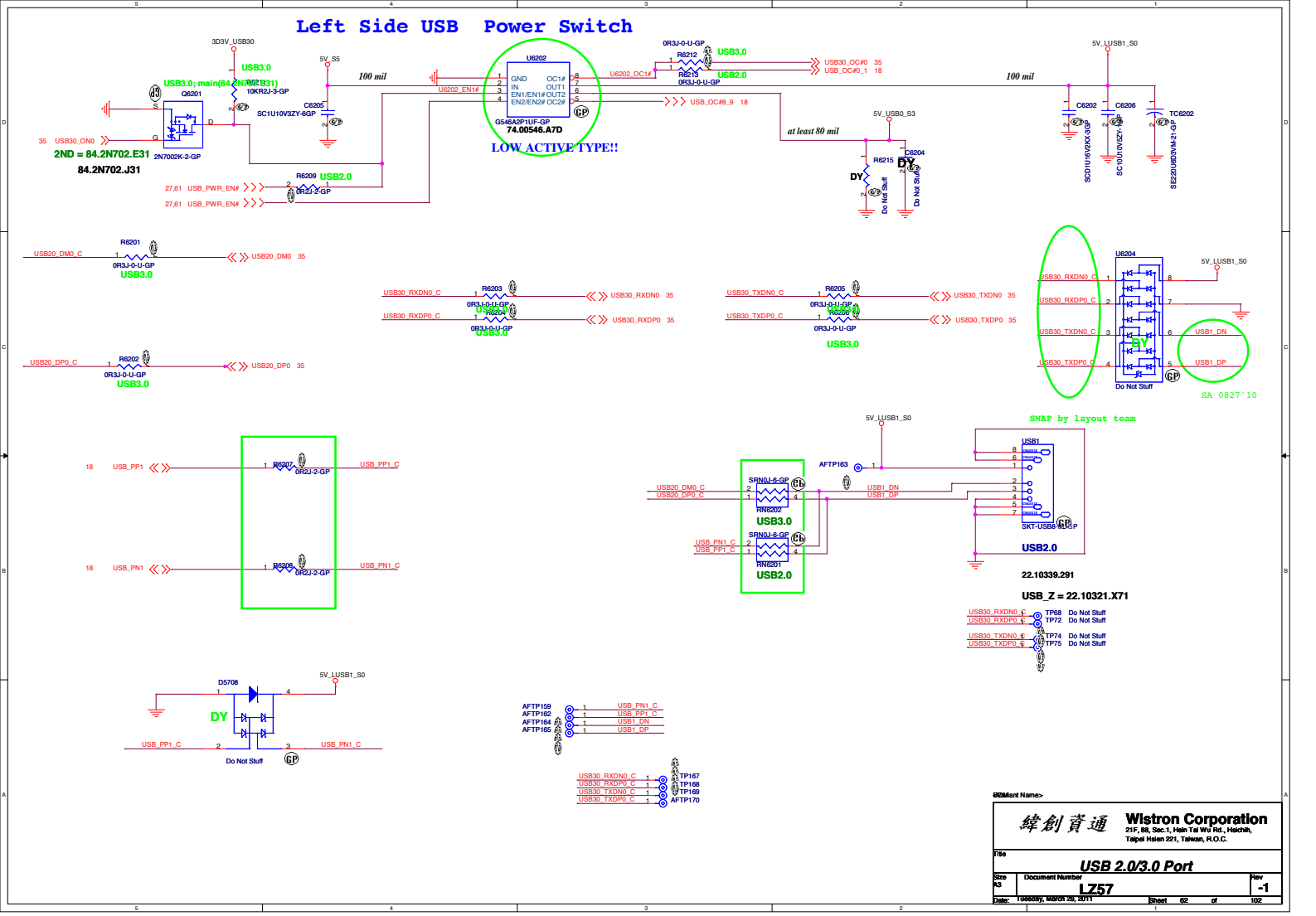
I/O Board USB Power



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	USB Power SW	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 61 of 102	

Left Side USB Power Switch



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: USB 2.0/3.0 Port			
Size: A3	Document Number: LZ57		Rev: -1
Date: Tuesday, March 29, 2011	Sheet 62 of 102		

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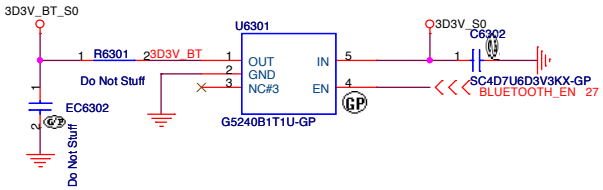
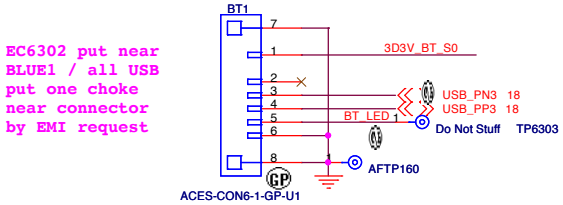
SSID = User.Interface

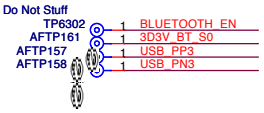
Bluetooth Module conn.

Bluetooth Module





EC6302 put near BLUE1 / all USB put one choke near connector by EMI request

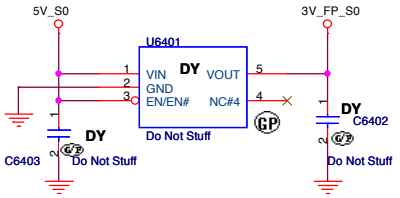


20.F0772.006

2ND = 20.F1804.006

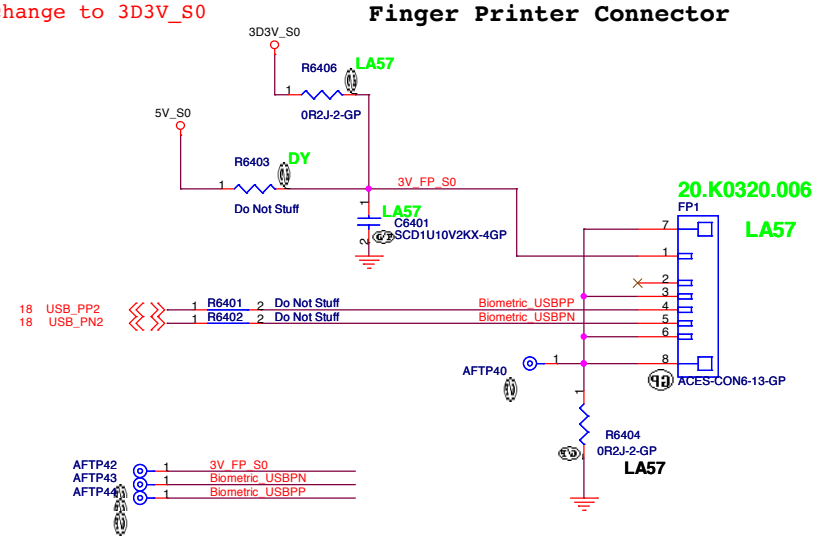
BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Bluetooth***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 63 of 102	



LA47 change to 3D3V_S0

Finger Printer Connector



BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 64 of 102

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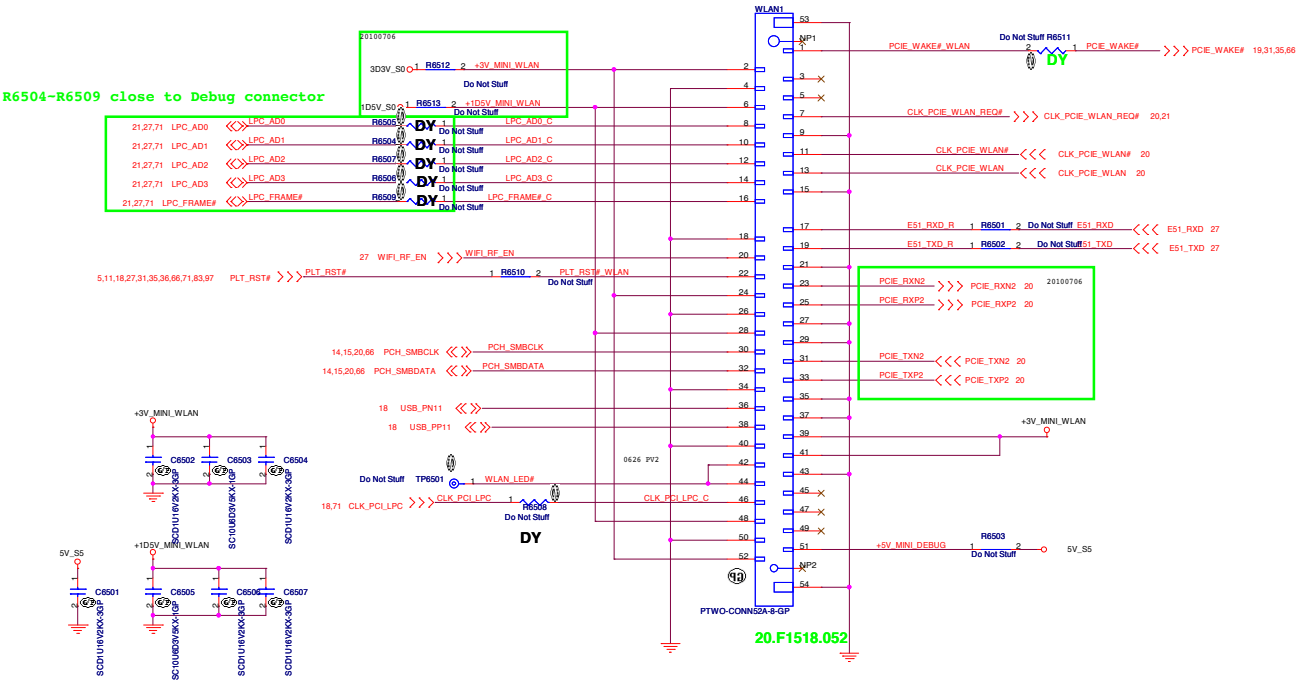
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

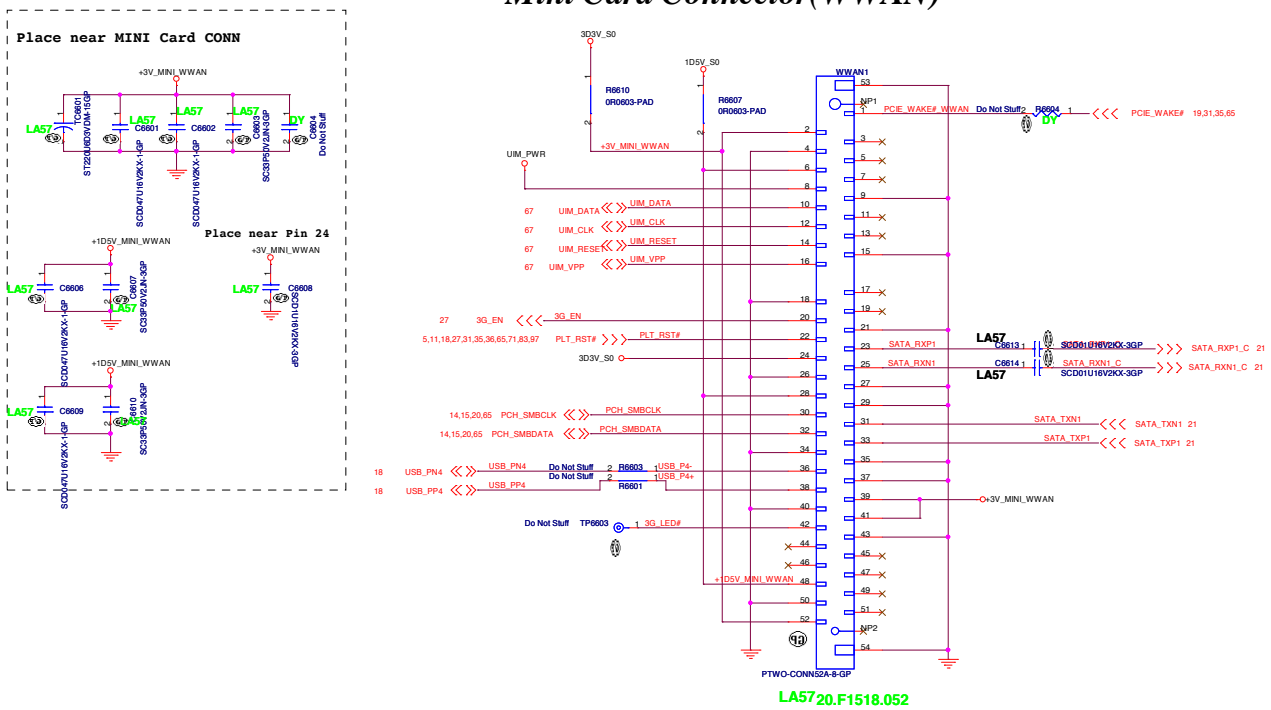


BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	MINICARD(WLAN)/TP CONN
Size A3	Document Number LZ57
Rev	-1
Date: Tuesday, March 29, 2011	Sheet 65 of 102

SSID = Wireless

Mini Card Connector(WWAN)



LA57 20.F1518.052

BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WWAN Connector	
Size A3	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 66 of 102	

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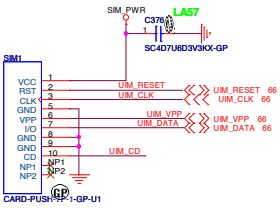
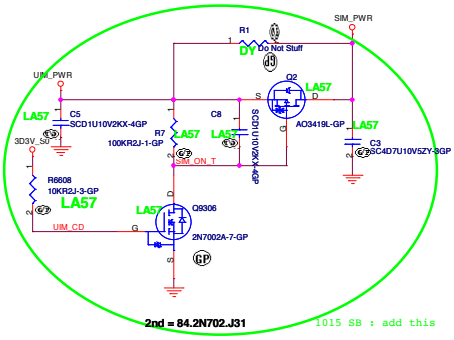


LA57

20.I0073.001



2nd = 84.2N702.J31

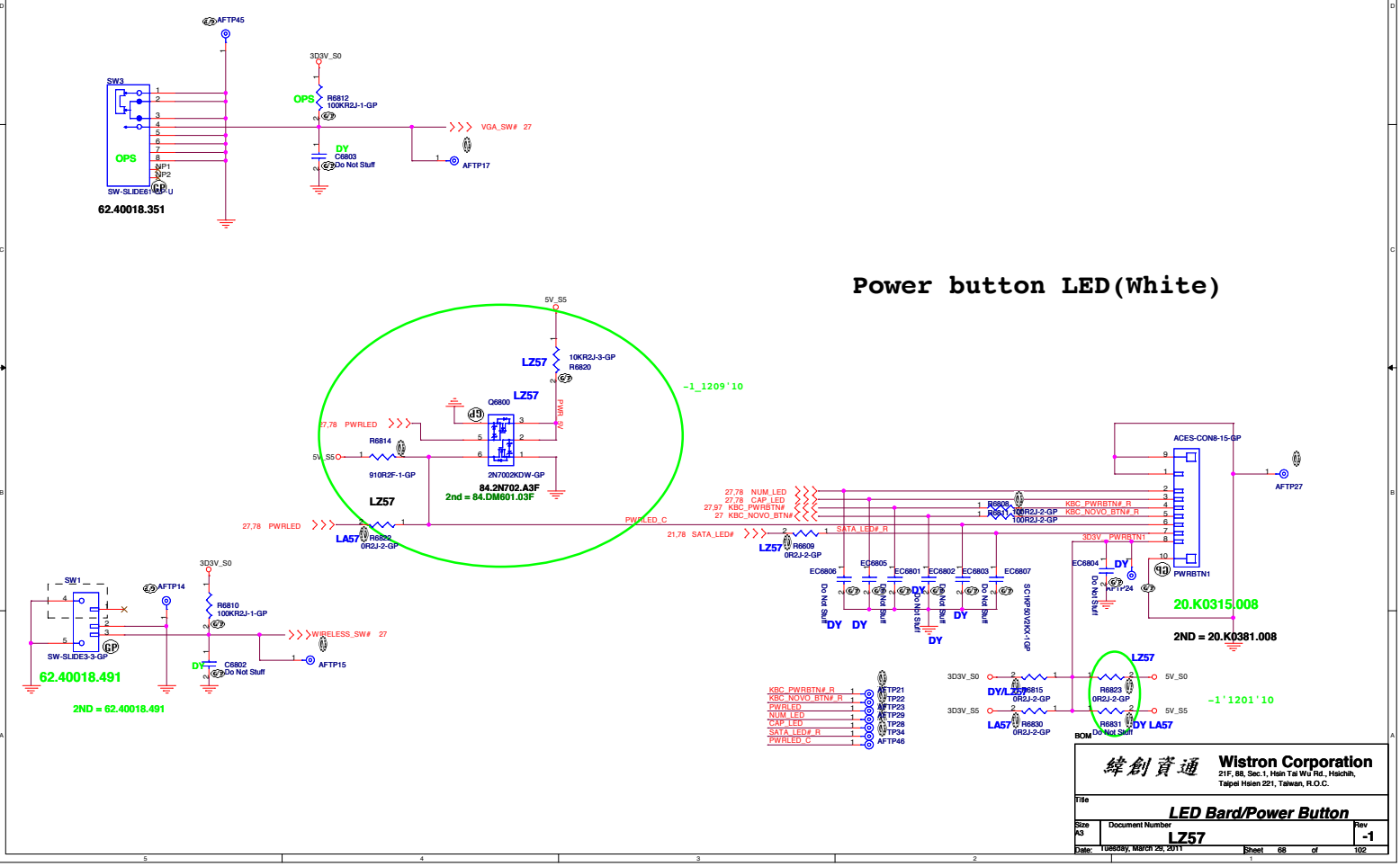
1015 SB : add this

84.2N702.E31

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***SIM CARD***	
Size A3	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 67 of 102	

SSID = User.Interface



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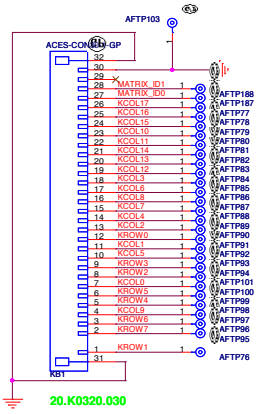
SSID = KBC

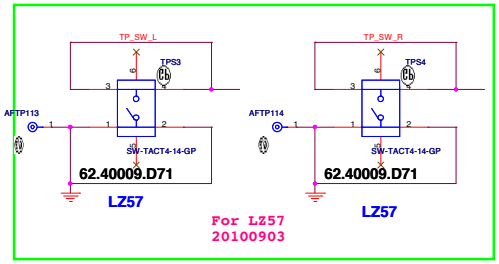
Internal KeyBoard Connector

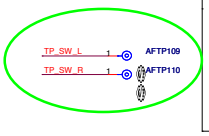


ID KEY MATRIX	SENSE			
	27	28	29	30
	ID0	ID1	ID2	GND
US	GND	GND	X	GND
GB	GND	X	X	GND
JP	X	GND	X	GND

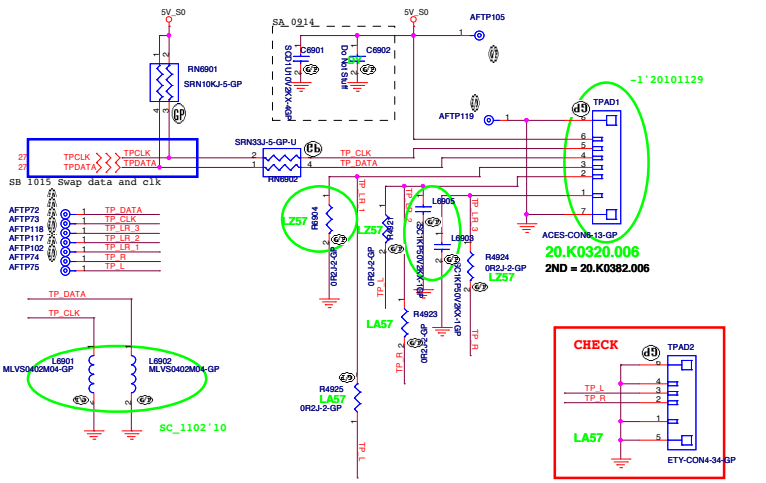
KROW[0..7] 27

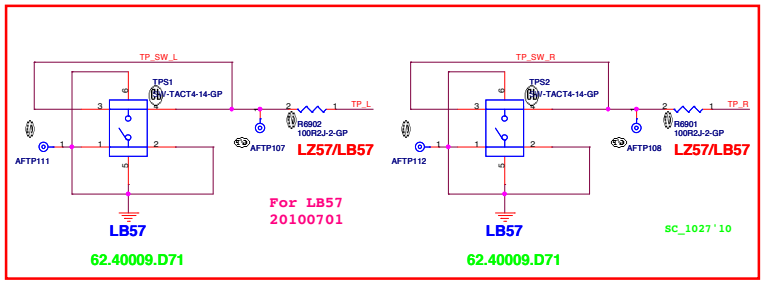
KCOL[0..17] 27





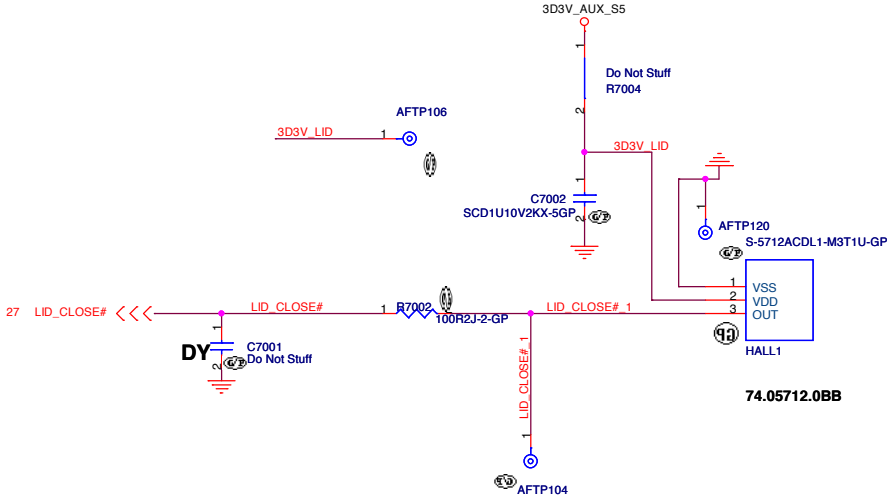
SSID = Touch.Pad





BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Key Board/Touch Pad
Size A3	Document Number LZ57 Rev -1
Date: Tuesday, March 29, 2011	Sheet 69 of 102



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Hall Sensor***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 70 of 102

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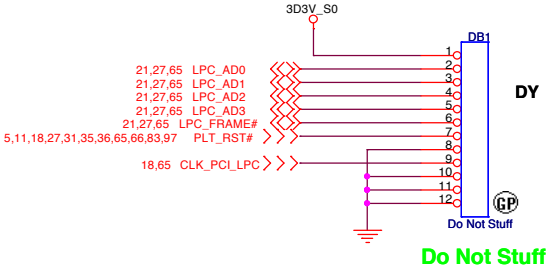

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Dubug connector***	
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 71 of 102	

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 72 of 102

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 73 of 102

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CARD Reader CONN***
Size A4	Document Number **LZ57**
Rev	**-1**
Date: Tuesday, March 29, 2011	Sheet 74 of 102

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***New Card***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 75 of 102

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 76 of 102

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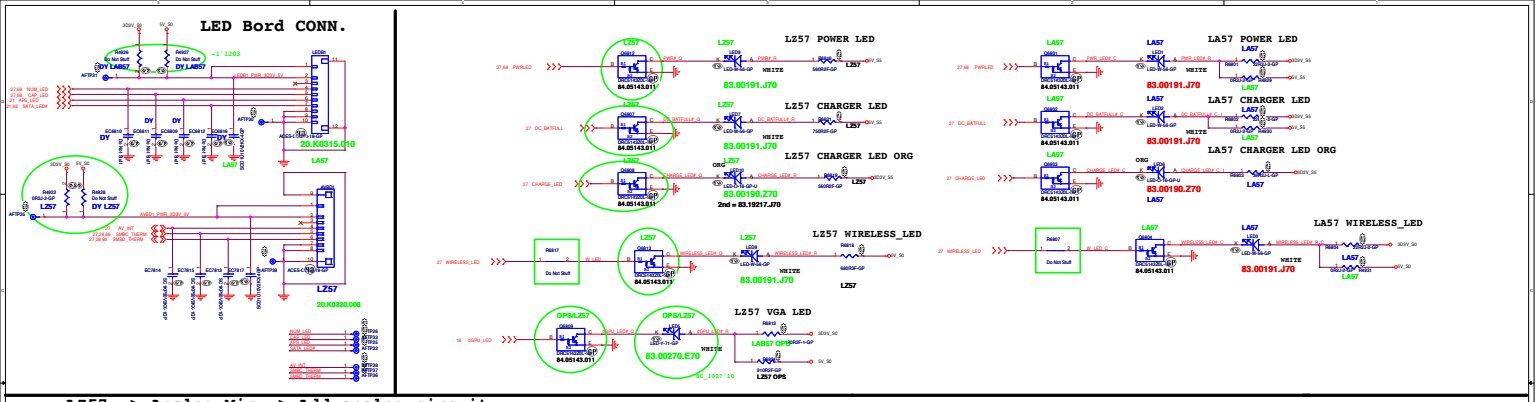
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

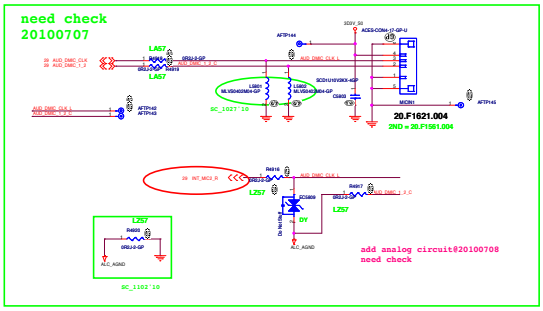
Title: *Reserved*

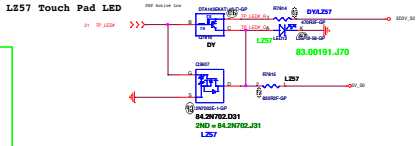
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 77 of 102



LZ57 => Analog Mic => Add analog circuit.
LA57 => Digital Mic





Wistron Corporation
LEDB/LED
LZ57

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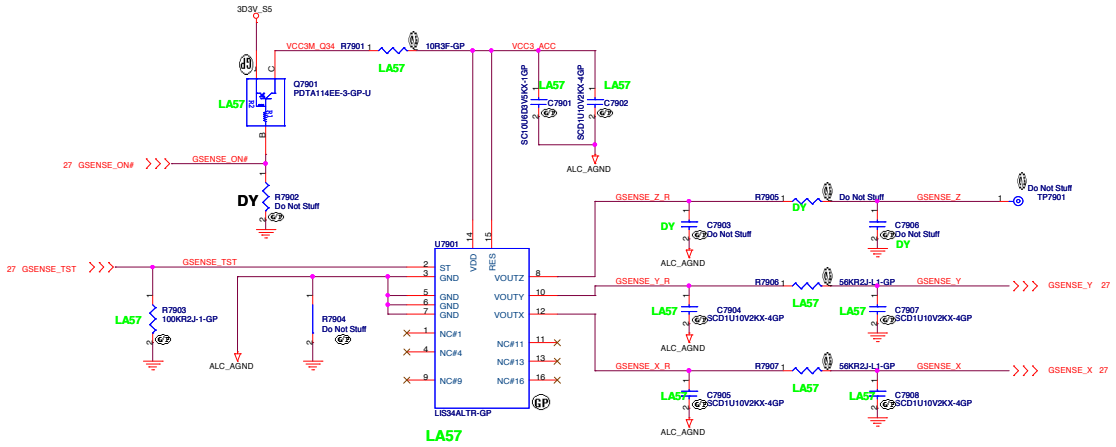
G-Sensor



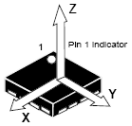
STMicro LIS34AL: 74.00034.0BZ
ADXL335 : 74.00335.0BZ

	ADXL322 LIS244AL LIS34AL	No Accel
R530	NO_ASM	ASM
R509	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

(1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.

(2) Avoid routing under DCDC switching area.



BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G-Sensor*

Size: Custom | Document Number: LZ57 | Rev: -1

Date: Tuesday, March 29, 2011 | Sheet 79 of 102

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Reserved***
Size A4	Document Number **LZ57** Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 80 of 102

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BOM

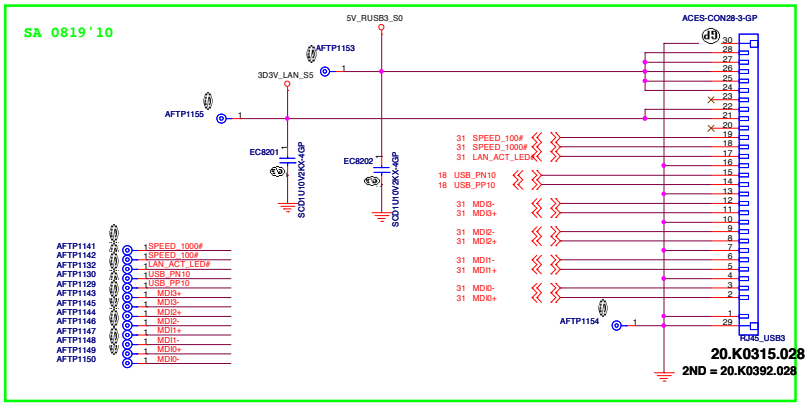
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

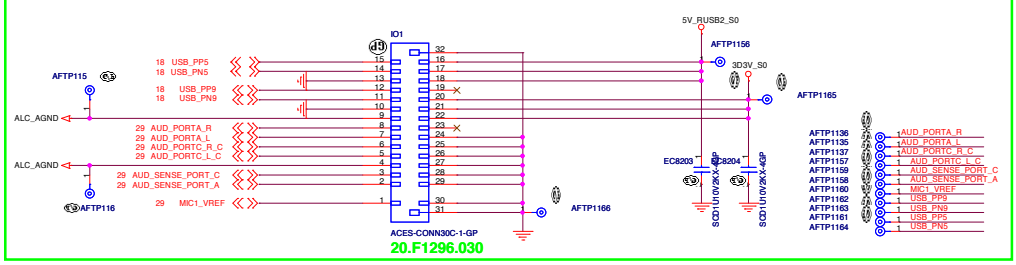
Size	Document Number	Rev
A4	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 81 of 102

RJ45_USB CONN.



Card Reader Board CONN.



BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***IO Board Connector***
Size A3	Document Number **LZ57** — Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 82 of 102

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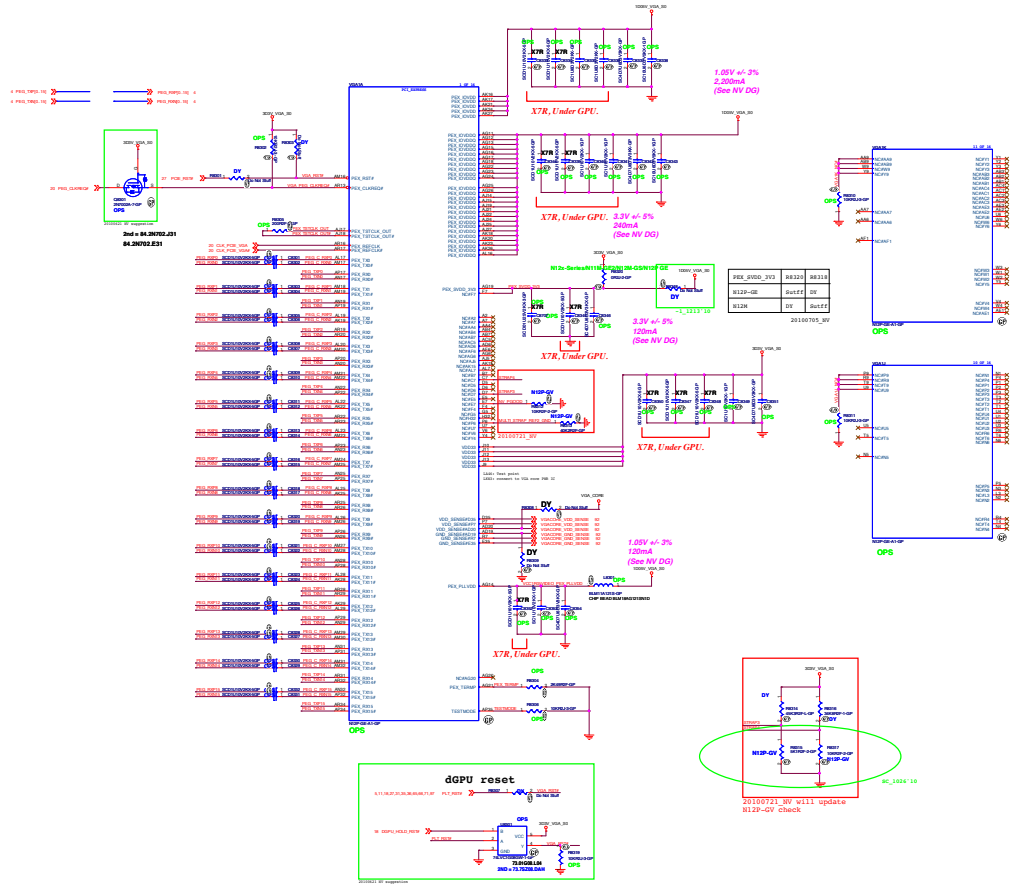
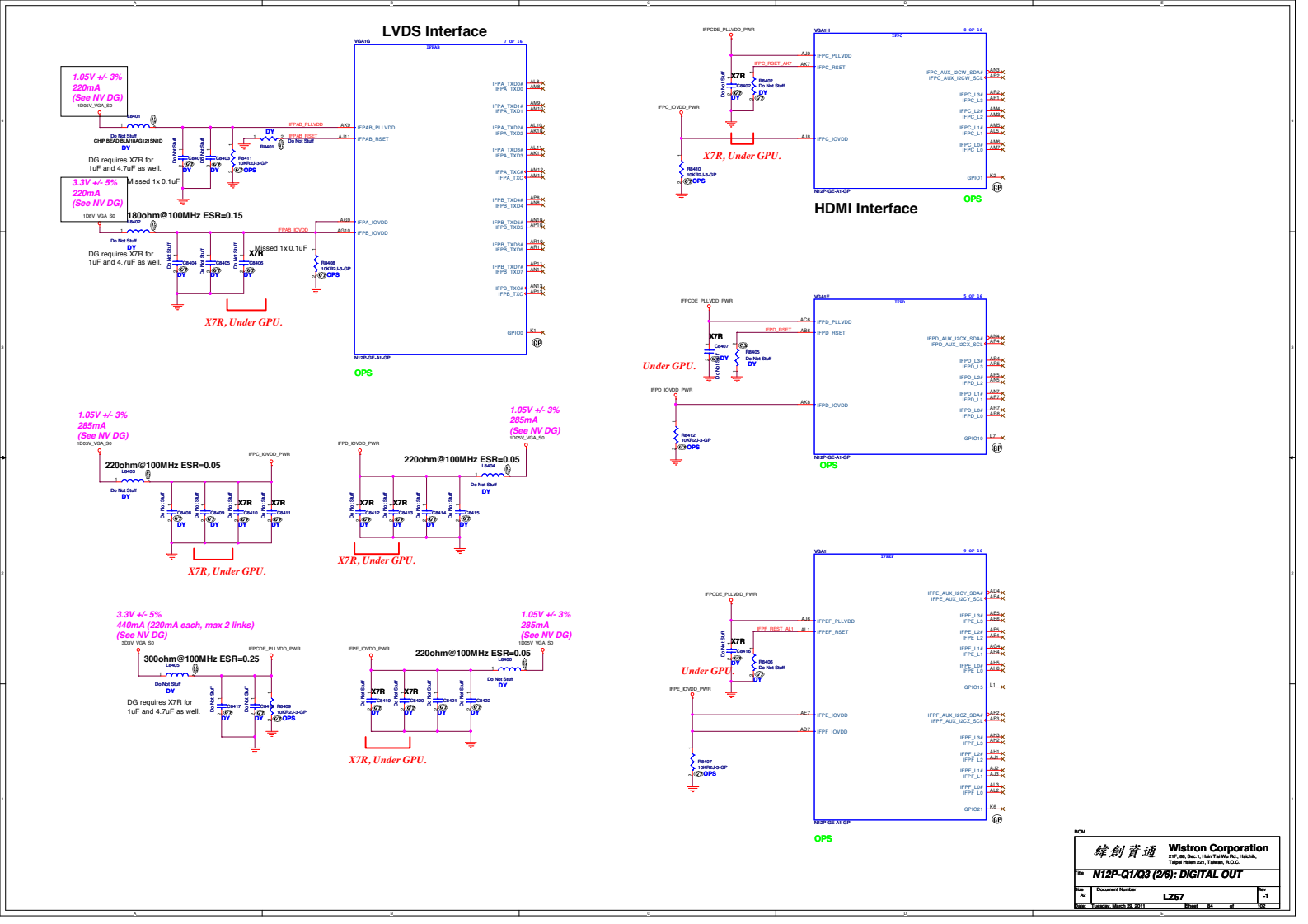


PEX_SVDD_3V3	R8325	R8318
N12P-GE	Suff	DY
N12N	DY	Suff

20100705_NV

Wistron Corporation			
Title	N12P-GE(1/6): PEG I/F		
Size	Document Number		Rev
D		LZ57	-1
Date: Monday, March 29, 2010	Sheet 03 of 47		



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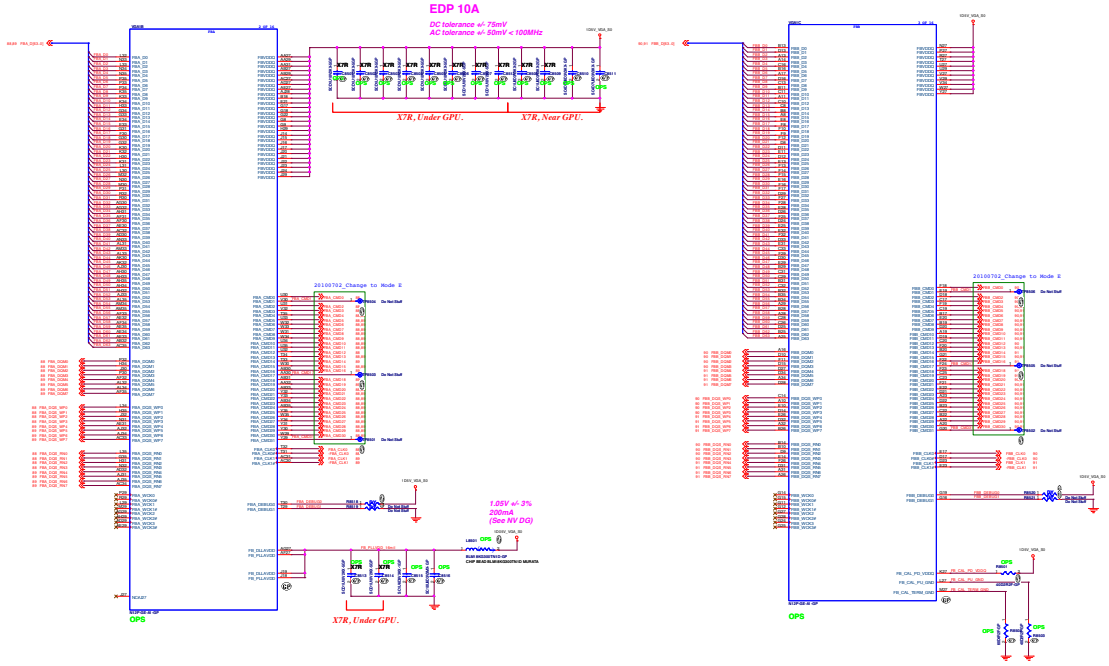
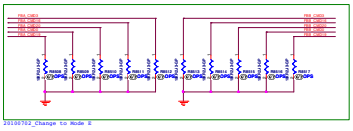
BOM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: N12P-Q1/Q3 (2/6): DIGITAL OUT
Size: A2
Document Number: LZ57
Rev: -1
Date: Tuesday, March 29, 2011
Sheet 84 of 102



FBCLK Termination place on VRAM side



FBCLK Termination place on VRAM side

緯創資通 Wistron Corporation	Title: N12P-Q1/Q3 (3/6): VRAM I/F
Size: A3	Document Number: L257
Date: Monday, March 01, 2010	Rev: 1

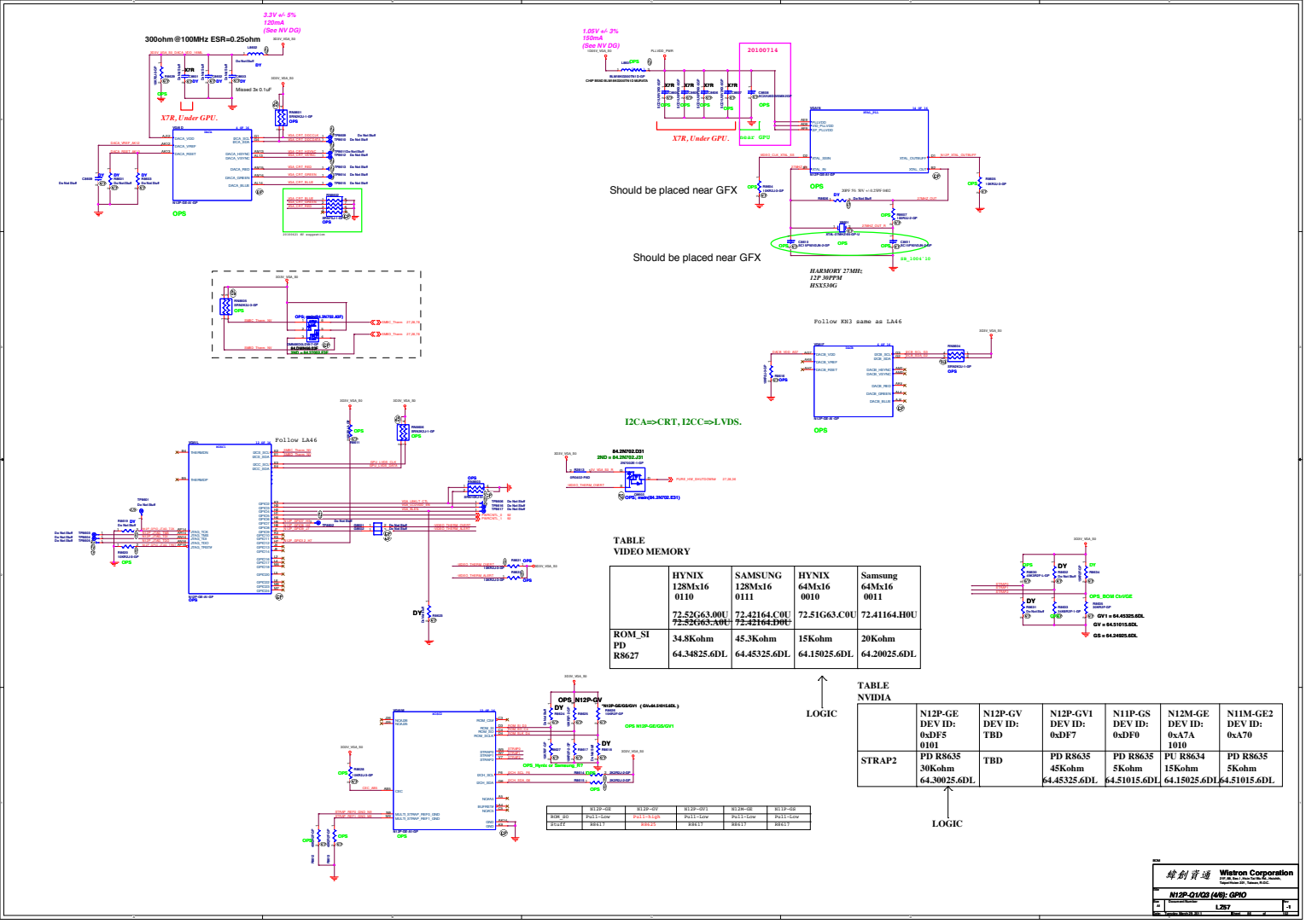


TABLE
VIDEO MEMORY

	HYNIX 128Mx16 0110 72.52G63.00U ~~72.52G63.A0U~~	SAMSUNG 128Mx16 0111 72.42164.C0U ~~72.42164.D0U~~	HYNIX 64Mx16 0010 72.51G63.C0U	Samsung 64Mx16 0011 72.41164.H0U
ROM_SI PD R8627	34.8Kohm 64.34825.6DL	45.3Kohm 64.45325.6DL	15Kohm 64.15025.6DL	20Kohm 64.20025.6DL

LOGIC

TABLE
NVIDIA

	N12P-GE DEV ID: 0xDF5 0101	N12P-GV DEV ID: TBD	N12P-GV1 DEV ID: 0xDF7	N11P-GS DEV ID: 0xDF0	N12M-GE DEV ID: 0xA7A 1010	N11M-GE2 DEV ID: 0xA70
STRAP2	PD R8635 30Kohm 64.30025.6DL	TBD	PD R8635 45Kohm 64.45325.6DL	PD R8635 5Kohm 64.51015.6DL	PU R8634 15Kohm 64.15025.6DL	PD R8635 5Kohm 64.51015.6DL

LOGIC

	N12P-GE	N12P-GV	N12P-GV1	N12M-GE	N11P-GS
ROM_SO	Pull-Low	Pull-High	Pull-Low	Pull-Low	Pull-Low
Stuff	R8617	R8625	R8617	R8617	R8617

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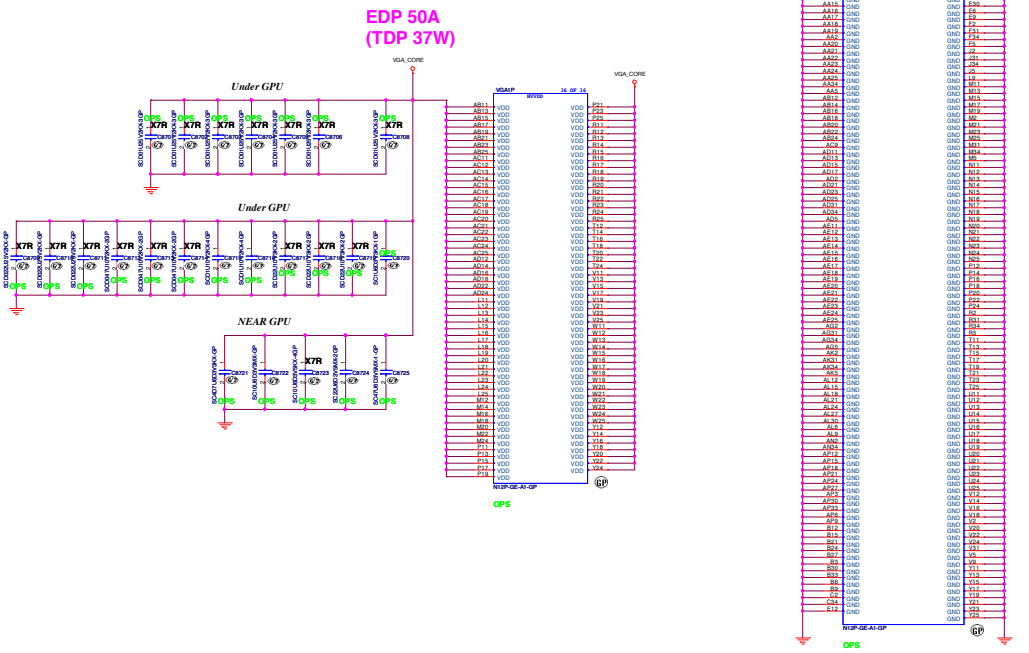
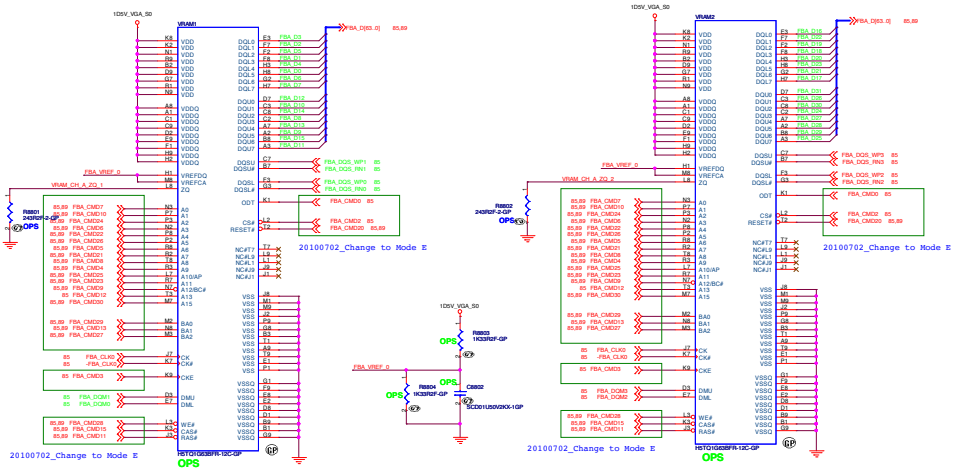
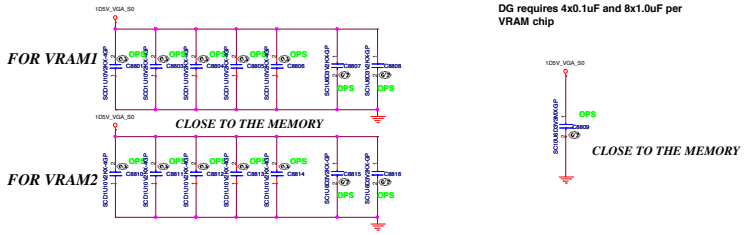


BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N12P-Q1/Q3 (5/6): POWER
Size: A0	Document Number: LZ57
Rev: -1	
Date: Tuesday, March 29, 2011	Sheet 87 of 100



FB CMD mapping Mode D-N12x



DG requires 4x0.1uF and 8x1.0uF per VRAM chip

VIDEO FRAME BUFFER PORT A

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*VRAM CHANNEL-A*	
Size A2	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 88 of 102	

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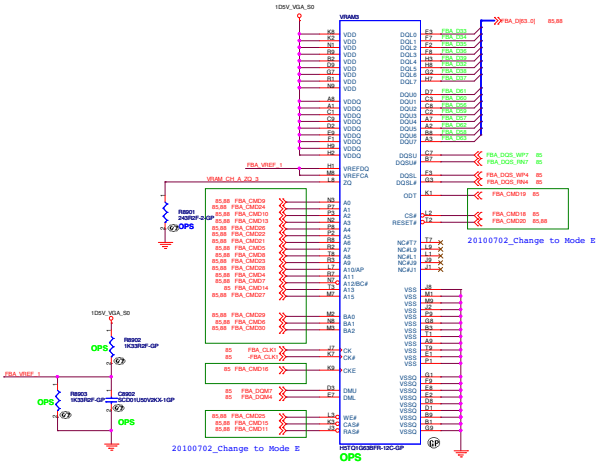
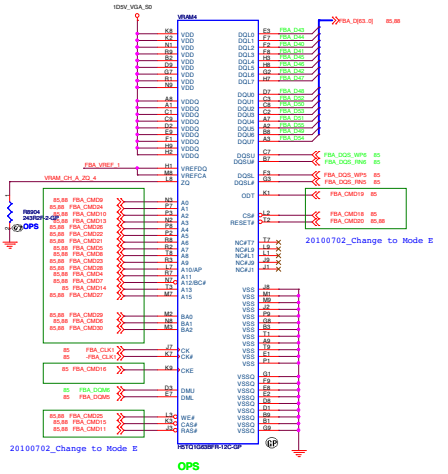
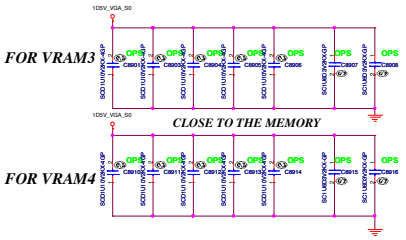




FB CMD mapping Mode D-N12x



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT A

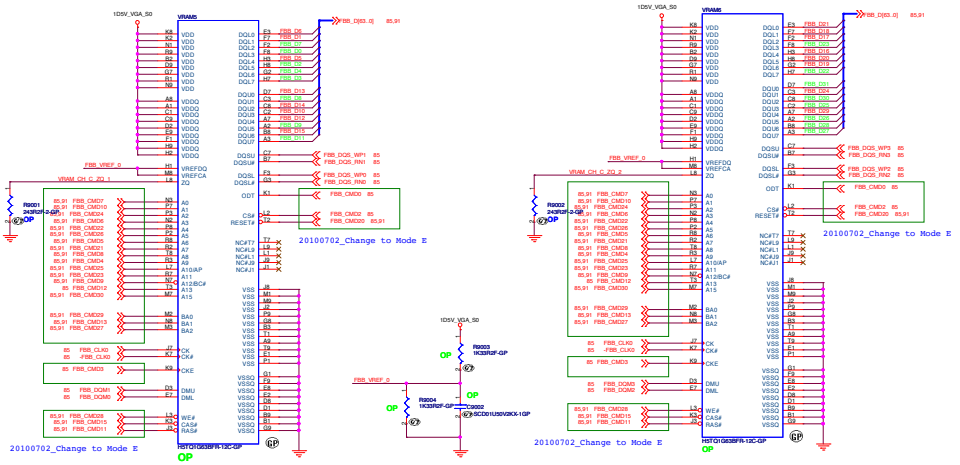
BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: **VRAM CHANNEL-A**

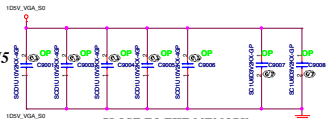
Size	Document Number	Rev
A2	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 89 of 102



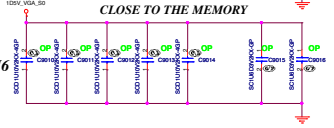
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

FOR VRAM5

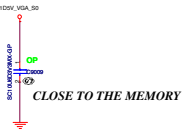


CLOSE TO THE MEMORY

FOR VRAM6



CLOSE TO THE MEMORY



CLOSE TO THE MEMORY

VIDEO FRAME BUFFER PORT C

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File	**VRAM CHANNEL-C**
Size: A0	Document Number: LZ57	Rev: -1
Date: Tuesday, March 29, 2011	Sheet 90 of 102

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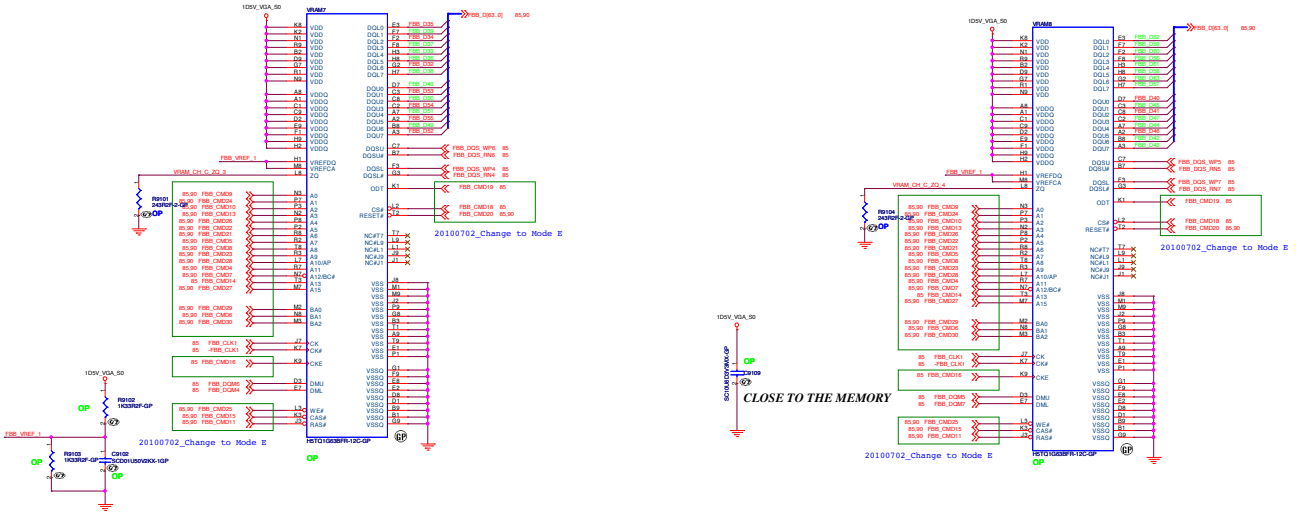
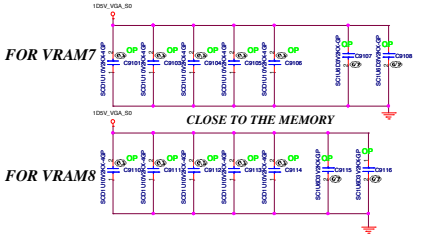


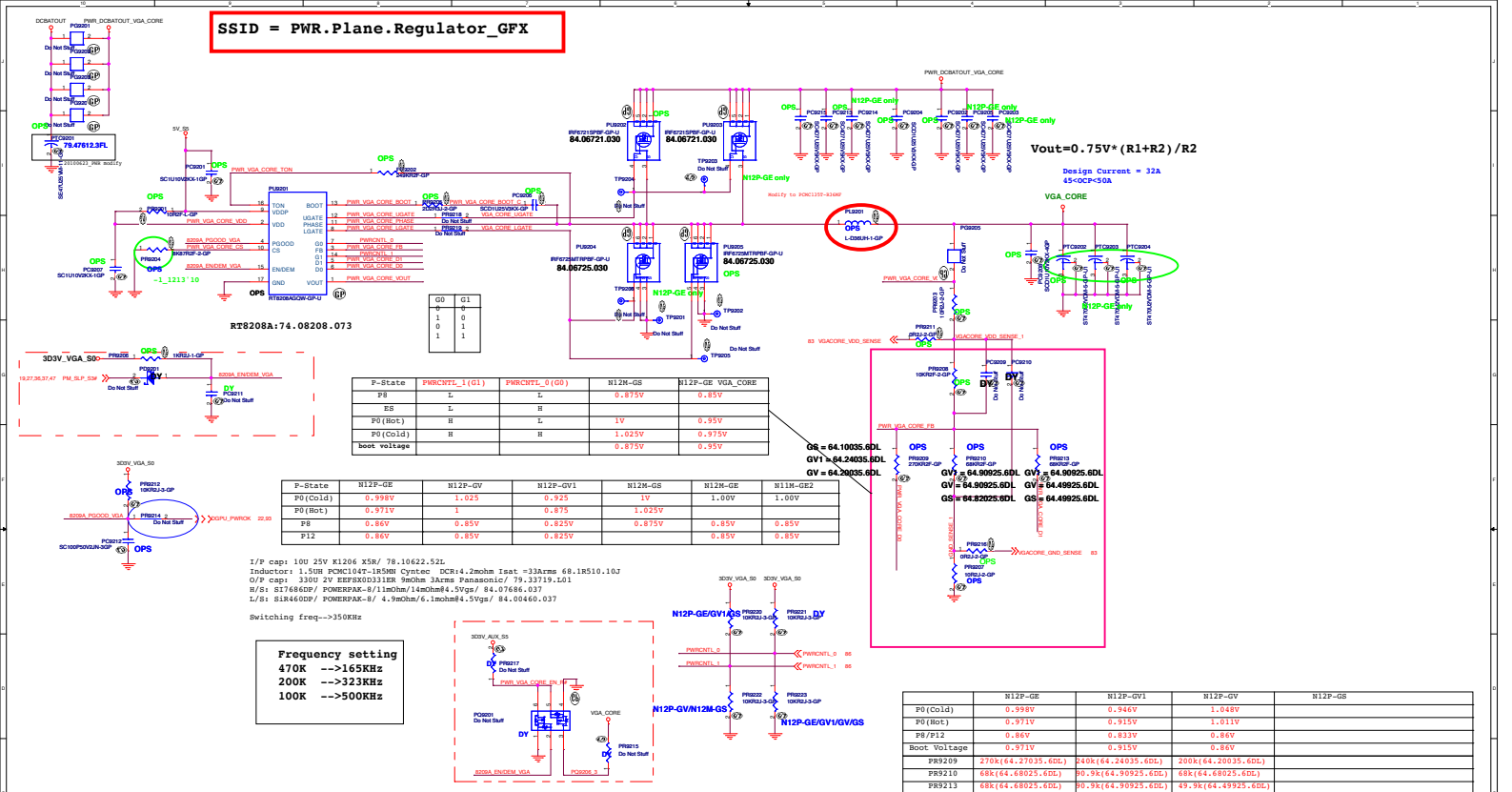


VIDEO FRAME BUFFER PORT C

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
File	***VRAM CHANNEL-C***
Size A2	Document Number: **LZ57** — Rev: -1
Date: Tuesday, March 29, 2011	Sheet 91 of 102

SSID = PWR.Plane.Regulator_GFX



P-State	PWRCNTL_1(G1)	PWRCNTL_0(G0)	N12M-GS	N12P-GE VGA_CORE
P8	L	L	0.875V	0.85V
ES	L	H		
P0(Hot)	H	L	1V	0.95V
P0(Cold)	H	H	1.025V	0.975V
boot voltage			0.875V	0.95V

P-State	N12P-GE	N12P-GV	N12P-GV1	N12M-GS	N12M-GE	N11M-GE2
P0(Cold)	0.998V	1.025	0.925	1V	1.00V	1.00V
P0(Hot)	0.971V	1	0.875	1.025V		
P8	0.86V	0.85V	0.825V	0.875V	0.85V	0.85V
P12	0.86V	0.85V	0.825V		0.85V	0.85V

GS = 64.10035.6DL
GV1 = 64.24035.6DL
GV = 64.20035.6DL

GV1 = 64.90925.6DL
GV = 64.90925.6DL
GS = 64.82025.6DL

GV1 = 64.90925.6DL
GV = 64.49925.6DL
GS = 64.49925.6DL

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: S1R460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

	N12P-GE	N12P-GV1	N12P-GV	N12P-GS
P0(Cold)	0.998V	0.946V	1.048V	
P0(Hot)	0.971V	0.915V	1.011V	
P8/P12	0.86V	0.833V	0.86V	
Boot Voltage	0.971V	0.915V	0.86V	
PR9209	270k(64.27035.6DL)	240k(64.24035.6DL)	200k(64.20035.6DL)	
PR9210	68k(64.68025.6DL)	90.9k(64.90925.6DL)	68k(64.68025.6DL)	
PR9213	68k(64.68025.6DL)	90.9k(64.90925.6DL)	49.9k(64.49925.6DL)	

BOM

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC/DC_VGA CORE_RT8208B**
Size: | Document Number: **LZ57** | Rev: -1
Date: Tuesday, March 29, 2011 | Sheet 92 of 102

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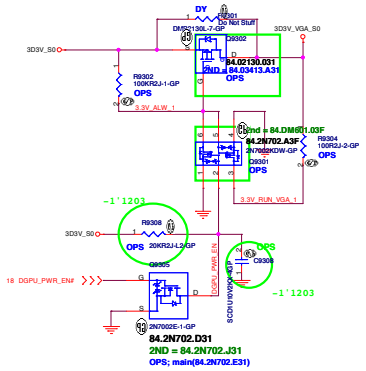
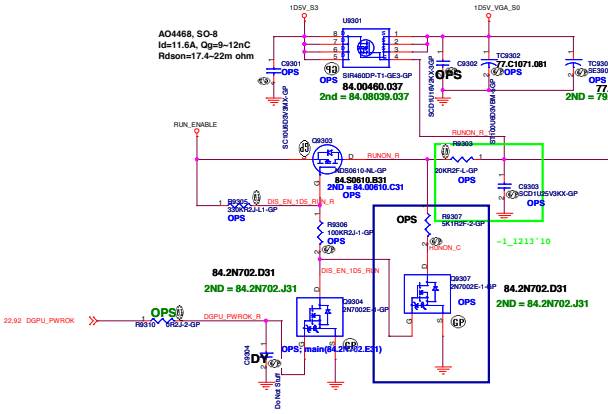
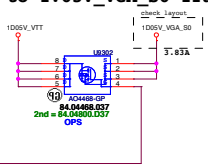
+3VS to 3.3V_DELAY Transfer



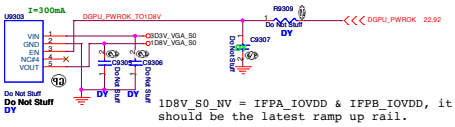
1D5V_VGA_S0



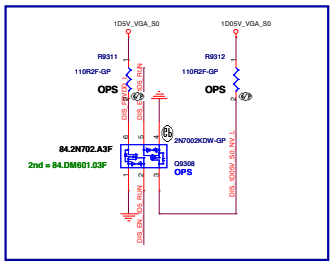
1.05V to 1.05V_VGA_S0 Transfer



+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 93 of 102	

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ROM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title:	LVDS_Switch
Size: A3 / Document Number:	LZ57 / Rev: -1
Date: Tuesday, March 26, 2013	Sheet 24 of 102

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BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Switch

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 95 of 102

BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***TOUCH PANEL***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 96 of 102

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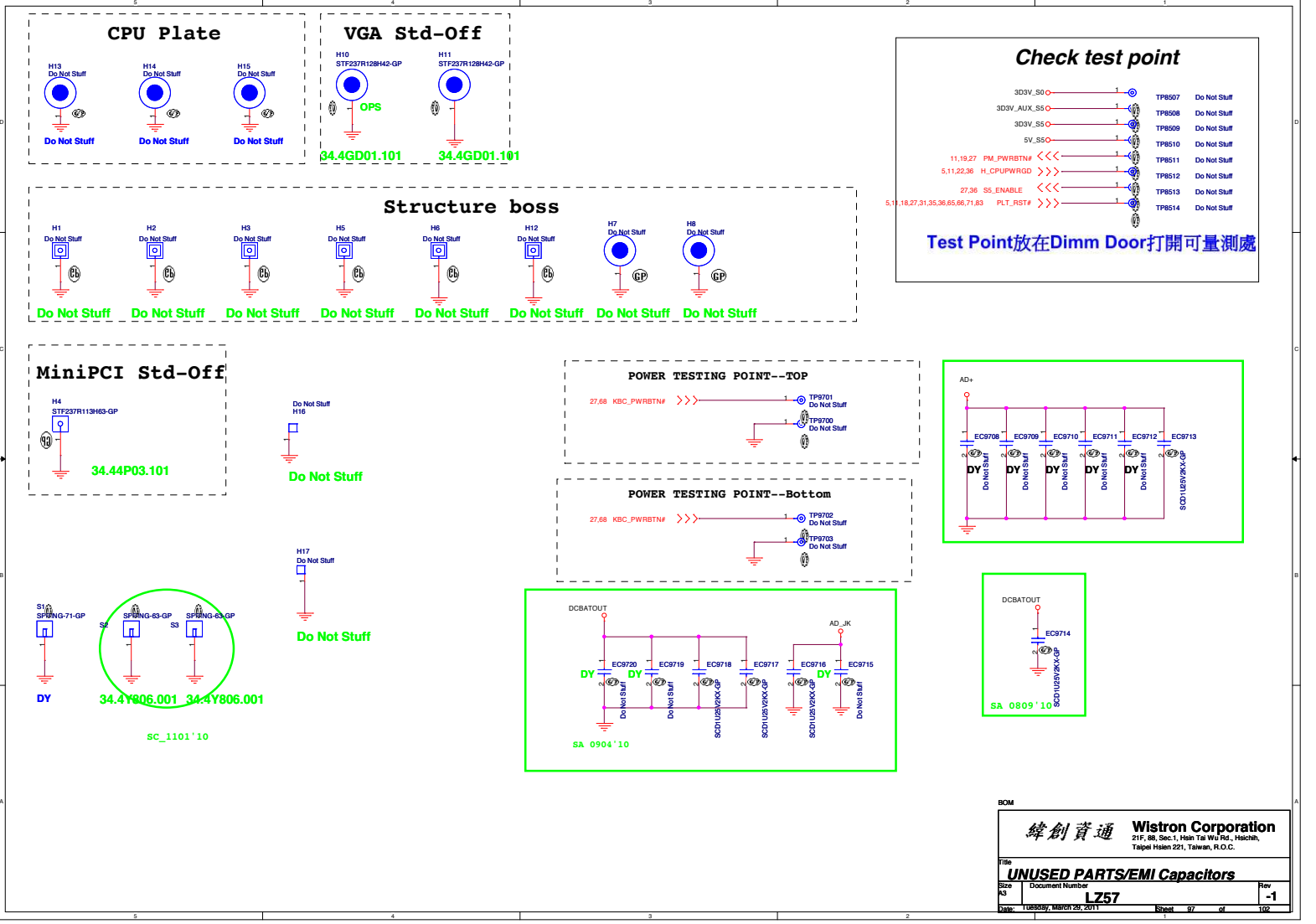

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 97 of 102

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BOM

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Change History***
Size A4	Document Number **LZ57**	Rev **-1**
Date: Tuesday, March 29, 2011	Sheet 98 of 102

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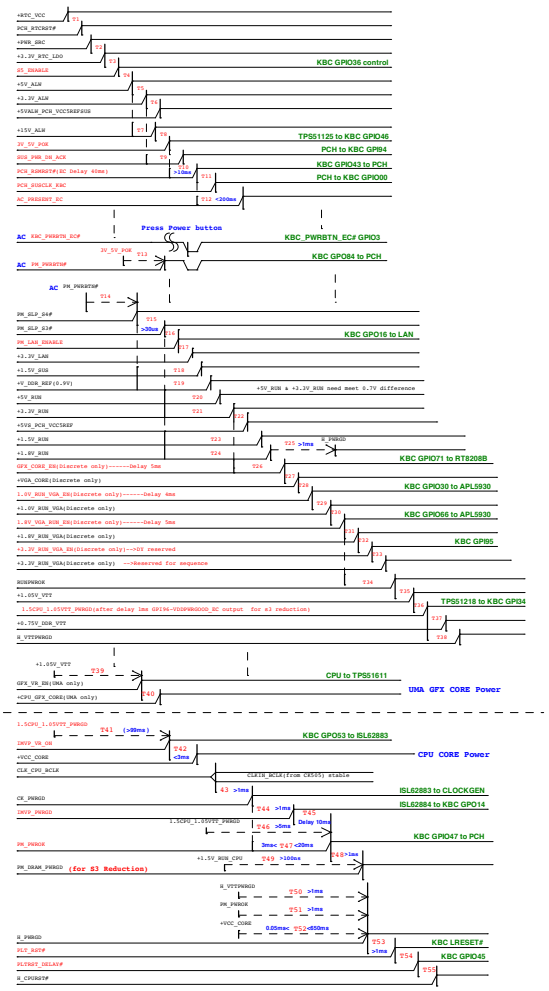
Intel-Power Up Sequence

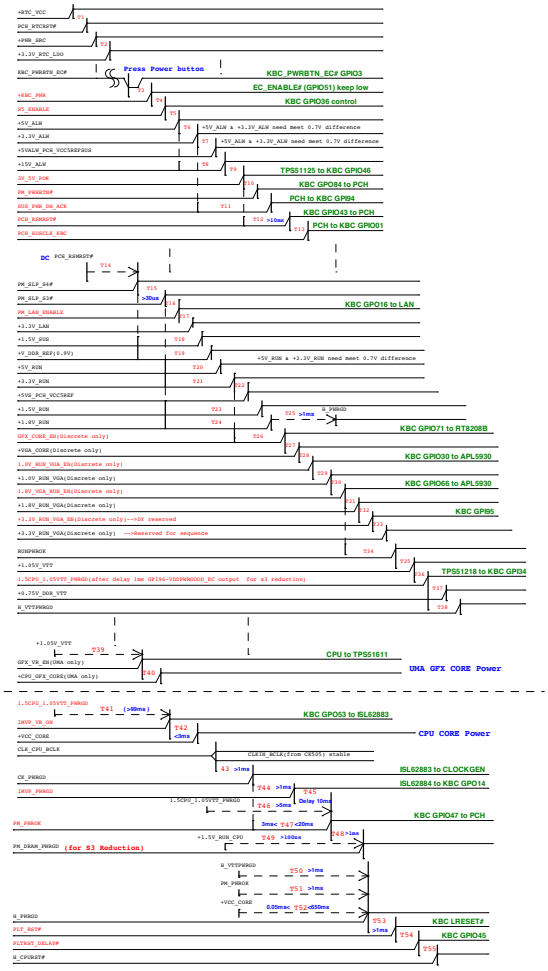
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO

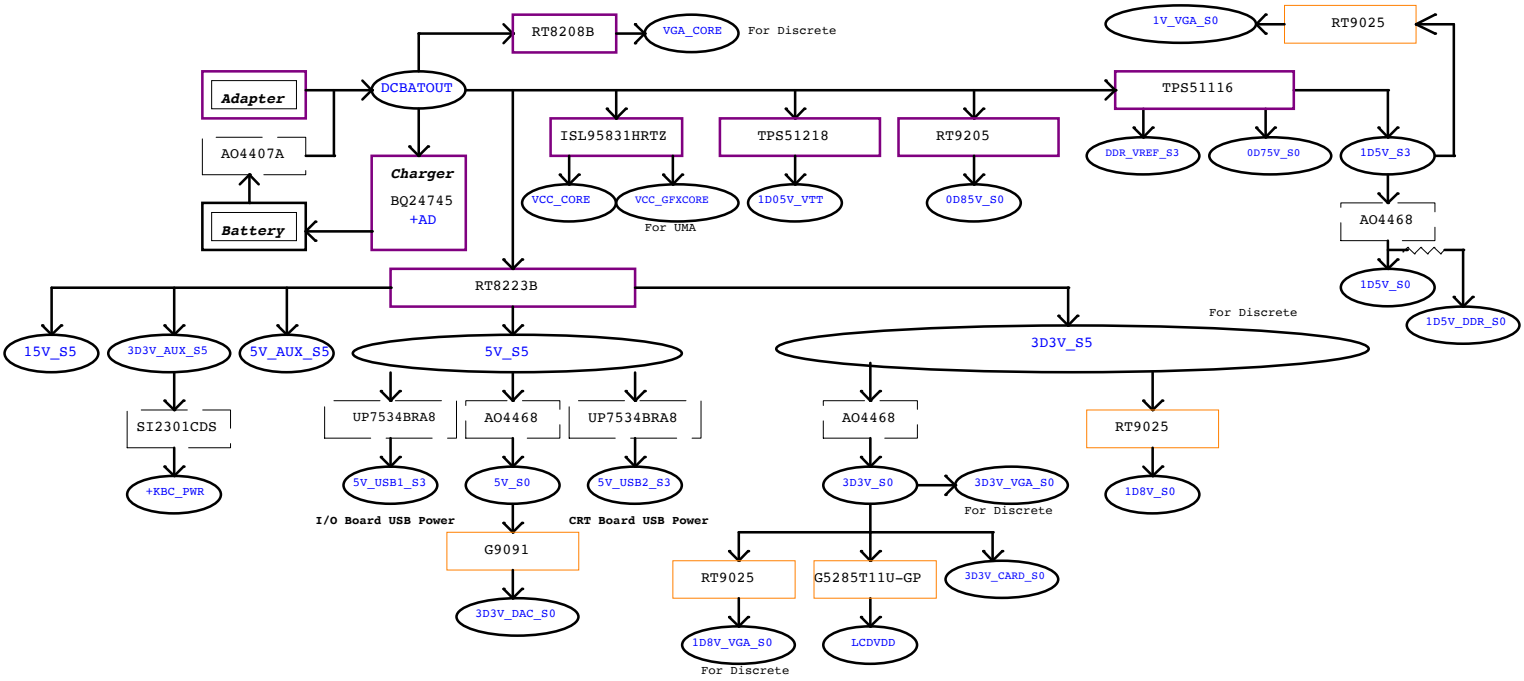


緯創資通 Wistron Corporation
22F,88 Sec.1,Hsin Tai Wu Rd.,Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Power Sequence

LJ57

-1



Power Shape

Regulator | LDO | Switch

BOM

緯創資通 **Wistron Corporation**
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	LZ57	-1

Date: Tuesday, March 29, 2011 Sheet 100 of 102

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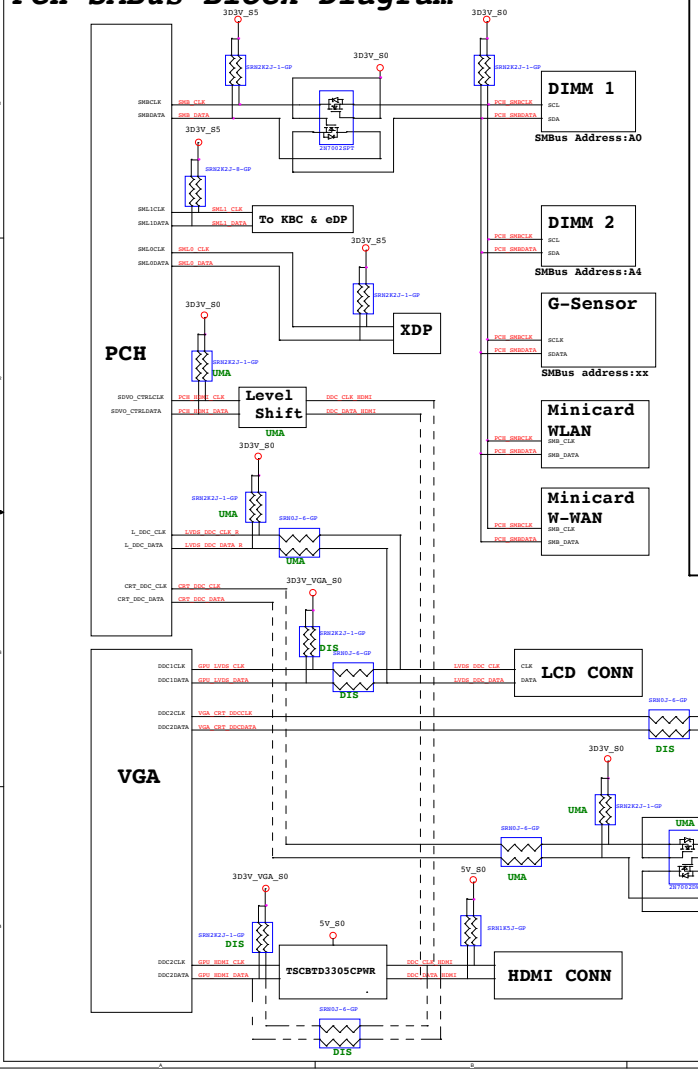
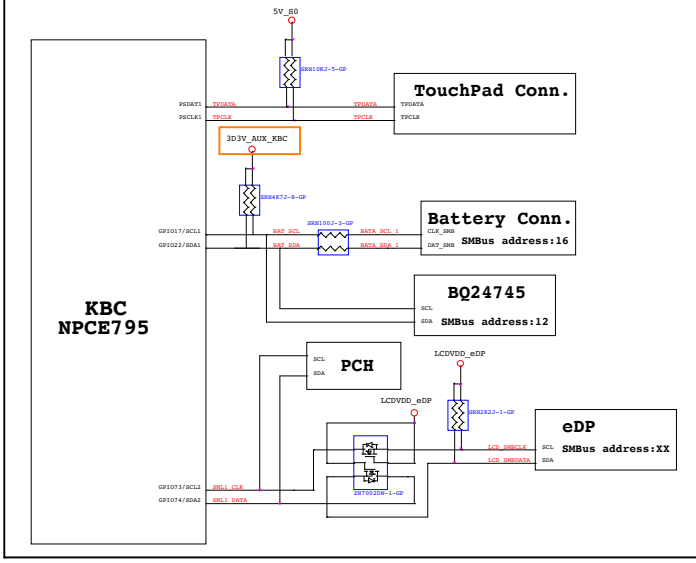
PCH SMBus Block Diagram



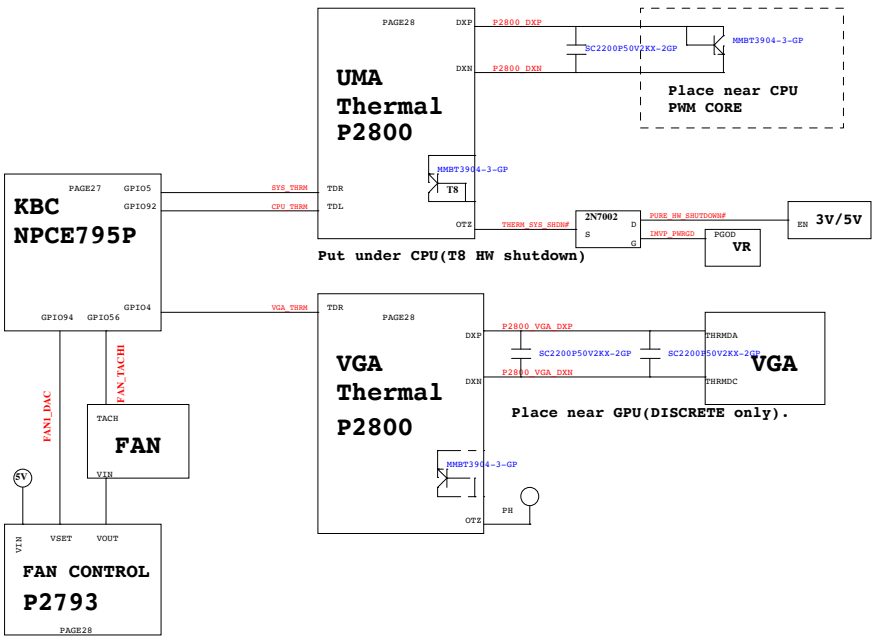
KBC SMBus Block Diagram



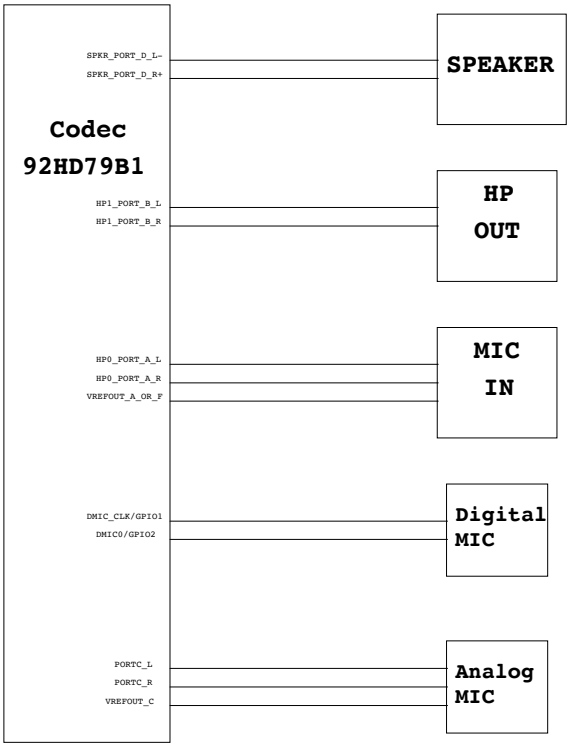
BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SMBUS Block Diagram	
Size	Document Number	Rev
A2	LZ57	-1
Date: Tuesday, March 30, 2010	Sheet 101 of 102	

Thermal Block Diagram



Audio Block Diagram



BOM

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Thermal/Audio Block Diagram	
Size Custom	Document Number LZ57	Rev -1
Date: Tuesday, March 29, 2011	Sheet 102 of 102	

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