MODEL:	REV:	CHANGE LIST:
ZL5 MotherBoard	1A	FIRST RELEASE
	2A	01. Page2 : Unstaff R202 for correct clock setting 02. Page3 : Delete JP2, Unstaff C561 and C559 ~ C562, C567 change P/N to CH6101M9A07 due to the height limitaion 03. Page5 : Change DDR MD terminator resistor array to 56ohm 4P2R type 04. Page9 : Change R20 to 6.2K, Unstaff C13 05. Page10 : Modify the CRT circuit due to the bad signal quality of CM2009 (Delete U1, Add D25, D28 ~ D32, Q35, Q36, R405, R404, R406, U31, U32) 06. Page11 : RN5, RN7, RN8, RN11, RN20, RN21 change P/N to CJ282084N01 07. Page12 : Modify the power good circuit (Delete D15, Add R402, R403) 08. Page16 : Modify the lan led circuit to fit to the right led color definition (R350, R353 change to pull high, Add D26, D27, CN3 change footprint) 09. Page17 : CN7, CN8 change footprint 10. Page19 : HOLE25 change to TOP layer 11. Page20 : Cancel the HOLD# ciruit (Unstaff R95, R111, D5, D7, Q17, Staff Q15, R99) 12. Page21 : SW2, SW3 change P/N to DHPPS11BD0 13. Page22 : Add PR123, PD16, PC149; PD13 change P/N to BC05FA20Z01; PU12 change P/N to AL001999W16 14. Page23 : PR63 change to 11K/F; PD15 change P/N to BC10QS04C01; Staff PC77 1000P 15. Page25 : PL8, PL9 change size to RC0805; PD8, PD9 change P/N to BC10QS04C01 16. Page26 : Unstaff PQ4; PR101, PR105 change P/N to CS31003B919; PU9 change P/N to AJ017720W06 17. Delete JP1, JP2 ~ JP6 18. U20 change P/N to AJ007600T25 19. L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L18, L24, L26, L27, L40, L43, L47, L48, L49, L50 change P/N to CX0QNT03004 20. PQ3, PQ4, PQ5, PQ6, PQ8, PQ9, PQ10, PQ12, PQ13, PQ14, PQ15, PQ16, PQ18, PQ24, PQ32, PQ33, PQ35, Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q11, Q26, Q27, Q34 change P/N to BAM70020074
	3A	01. Page2 : Staff R176 33ohm for 302ELV clock 02. Page4 : Staff C131, C175, C188, C189 03. Page9 : Staff R295(0ohm), R294 change P/N to CS00002JB03, Unstaff Y4, C31, C554 for 302ELV clock; Add C710 ~ C713, R407 ~ R410 for EMI reserved. 04. Page10 : D17 change p/n to BC05FA20Z01 to enlarge the current limit; L1 ~ L3 change p/n to CX808600101 for EMI 05. Page12 : C633, C634 change P/N to CH01806JB07 to adjust RTC accuracy; Add JP1 for RTC reset 06. Page15 : Add C709 07. Page17 : Unstaff CN8, CN10; Add C700 ~ C708 for EMI 08. Page19 : Delete HOLE18; Staff PAD4 for modem cable
	3B	01. Page17 : L36, R274, R279 change p/n to CX8HS121001; Staff R270, R273 100pF 02. Page18 : L54, L55 change p/n to CX8HS121001; Unstaff R260, R261, R265, R271, R278 03. Page19 : Staff PAD9(FDMK1004010) for EMI 04. Page22 : Unstaff PR112 for thermal shutdown working properly 05. Q2, Q3, Q4, Q5, Q6, Q8, Q9, Q11, Q18, Q26, Q27, Q34, Q35, Q36, PQ3, PQ4, PQ5, PQ6, PQ8, PQ9, PQ10, PQ12, PQ13, PQ14, PQ15, PQ16, PQ18, PQ24, PQ32, PQ33, PQ35 change p/n to BAN70020Z13

MODEL : ZL5 MB

PAGE	FROM	TO
1	3A	3B
2	3A	3B
3	3A	3B
4	3A	3B
5	3A	3B
6	3A	3B
7	3A	3B
8	3A	3B
9	3A	3B
10	3A	3B
11	3A	3B
12	3A	3B
13	3A	3B
14	3A	3B
15	3A	3B
16	3A	3B
17	3A	3B
18	3A	3B
19	3A	3B
20	3A	3B
21	3A	3B
22	3A	3B
23	3A	3B
24	3A	3B
25	3A	3B
26	3A	3B

Quanta Computer Inc.	PROJECT : ZL5	APPROVE BY: SAINT LIN	DRAWING BY:DILBERT YU	REV 3B
	MB ASSY'S P/N : 31ZL5MB0009	PROJECT LEADER: SAINT LIN	DOCUMENT NO:	DATE :2005/3/9

COVER SHEET 1 OF 1

ZL5
Block Diagram

CLK-GEN ICS 952801 — Page 2
- HOST 200MHz
- ZCLK 133MHz
- AGP 66MHz
- PCI 33MHz
- USB 48MHz
- REF 14.318MHz

3V/5V — Page 22
- 3V_ALWAYS
- 5VPCU
- 3V_S5
- 1.8V_S5
- 3VSUS
- 5VSUS
- +3V
- +5V
- 15V

2.5V/1.25V — Page 23
- 2.5VSUS
- 1.25VREF
- +2.5V
- DDR_VTT

1.2V/1.5V 1.8V — Page 24
- +1.2V_HT
- +1.5V
- +1.8V

CPU CORE — Page 25
- VCC_CORE

BATTERY CHARGER — Page 26

DDR SO-DIMM — Page 5
DDR 333

CPU AMD Athlon64, SMT uPGA754 — Page 3,4

Thermal — Thermal sensor & Fan

HyperTransport 16x16 1600MT/s

NB SIS M760GX (698 PIN BGA) — Page 6,7,8
- RGB → **CRT** 1x D-SUB 15-Pin — Page 10
- DVO → **LVDS Transmitter** SIS302ELV — Page 9 (INTA#)
  - LVDS → **LCD** 15" XGA/WXGA — Page 10

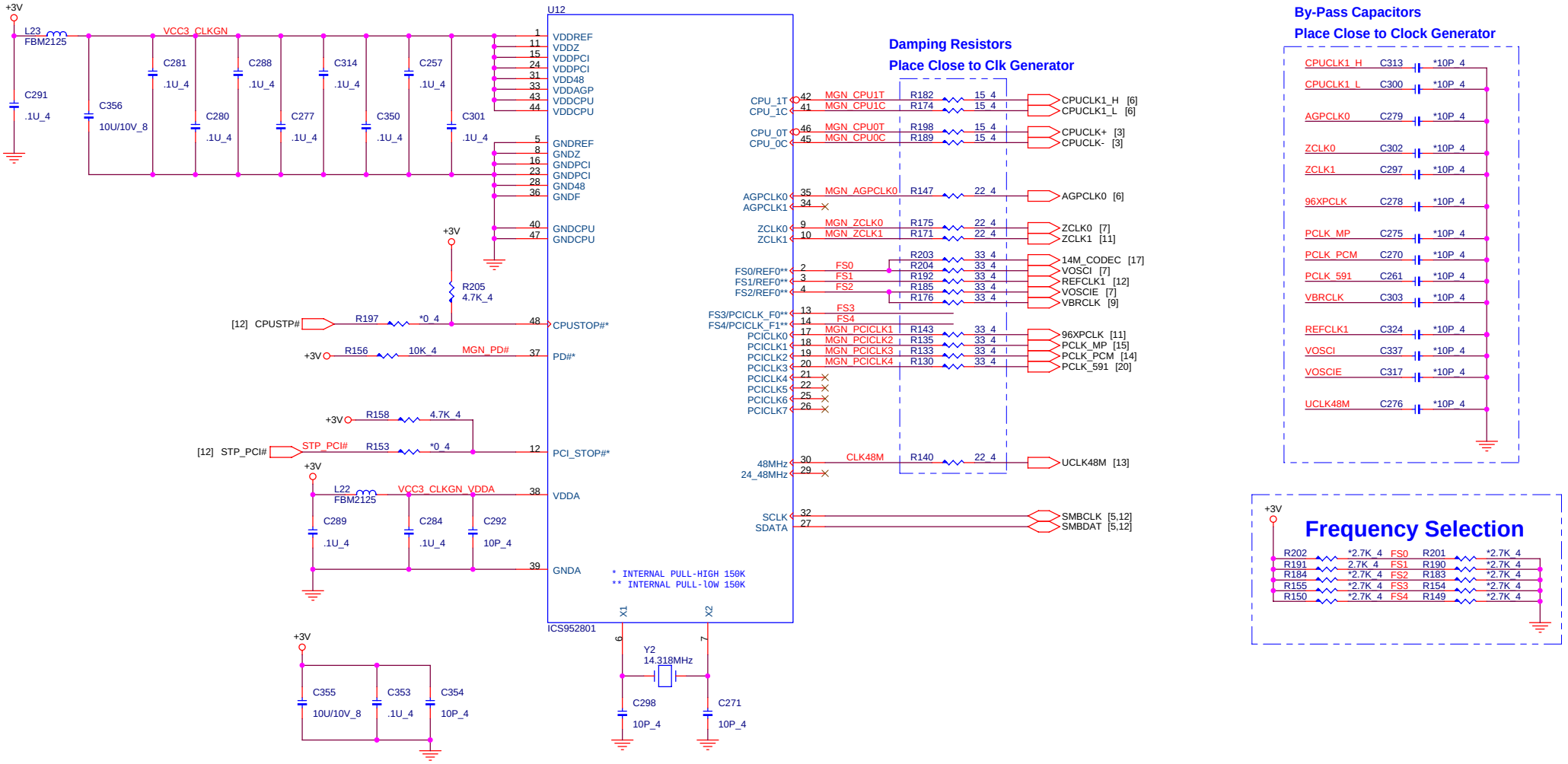
MuTIOL(1GB/s)

SB SIS 963L (371 PIN BGA) — Page 11,12,13
- ATA 66/100 → **HDD** Primary Master — Page 19
- ATA 66/100 → **ODD** Secondary Master — Page 19
- USB 2.0 → **USB** 3x connector — Page 15
- USB 2.0 → **MINI USB** (BLUETOOTH) — Page 15
- PCI 2.2 133MB/s (33MHZ) → **Mini PCI** WLAN 802.11A/G — Page 15 (REQ0#, GNT0# INTB#, INTC# IDSEL : AD22) → **Antenna**
- PCI 2.2 133MB/s (33MHZ) → **CardBus** TI PCI1410 — Page 14 (REQ1#, GNT1# INTD# IDSEL : AD17) → **PC Card** 1x type-I/II
- MII → **LAN PHY** RTL8201CP — Page 16 → **Transformer** — Page 16 → **RJ-45** — Page 16
- AC'97 2.1 → **MDC1.5** 56K MODEM — Page 17 → **RJ-11** — Page 16
- AC'97 2.1 → **AC97 Codec** ALC203 — Page 17
  - → **MIC-In Jack**
  - → **Line-In Jack**
  - → **AMP** MAX9755 — Page 18 → **HP-Out Jack**, **Int. Speaker**
- LPC → **EC** NS PC97551 — Page 20
  - **Int. Keyboard** 87-Key — Page 21
  - **Touch Pad** 6-Button — Page 21
  - → **BIOS** — Page 20

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	3B

Date: Thursday, March 10, 2005 Sheet 1 of 26



CLK Table for SiS M760 (Not For ICS ICS-952801)

SiS 755/M760 CLOCK									
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)	VCO (MHz)
0	0	0	0	0	200	66.66	66.66	33.33	400
0	0	0	0	1	200	100	66.66	33.33	400
0	0	0	1	0	200	133.33	66.66	33.33	400
0	0	0	1	1	200	166.66	66.66	33.33	1000
0	0	1	0	0	233	66.66	66.66	33.33	466
0	0	1	0	1	233	93.2	66.66	33.33	466
0	0	1	1	0	233	133.28	66.66	33.33	933
0	0	1	1	1	233	139.8	69.9	33.33	699
0	1	0	0	0	266	66.66	66.66	33.33	266
0	1	0	0	1	266	106.4	66.5	33.33	532
0	1	0	1	0	266	133	66.5	33.33	532
0	1	0	1	1	266	159.6	66.5	33.33	798
0	1	1	0	0	200	133	50	33.33	400
0	1	1	0	1	200	114	66.66	33.33	800
0	1	1	1	0	200	142	66.66	33.33	1000
0	1	1	1	1	200	160	66.66	33.33	800

SiS 755/M760 CLOCK								
(FS4)	(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	ZCLK (MHz)	AGPCLK (MHz)	PCI (MHz)
1	0	0	0	0	180	135	67.5	33.75
1	0	0	0	1	185	132.14	66.07	33.04
1	0	0	1	0	190	135.71	67.08	33.93
1	0	0	1	1	195	130	65	32.5
1	0	1	0	0	205	136.66	68.33	34.17
1	0	1	0	1	210	140	70	35
1	0	1	1	0	215	129	64.5	32.25
1	0	1	1	1	220	132	66	33
1	1	0	0	0	66.66	66.66	66.66	33.33
1	1	0	0	1	66.66	100	66.66	33.33
1	1	0	1	0	100	100	66.66	33.33
1	1	0	1	1	100	133.33	66.66	33.33
1	1	1	0	0	133	100	66.66	33.33
1	1	1	0	1	133	133.33	66.66	33.33
1	1	1	1	0	166	100	66.66	33.33
1	1	1	1	1	166	133.33	66.66	33.33

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	3B
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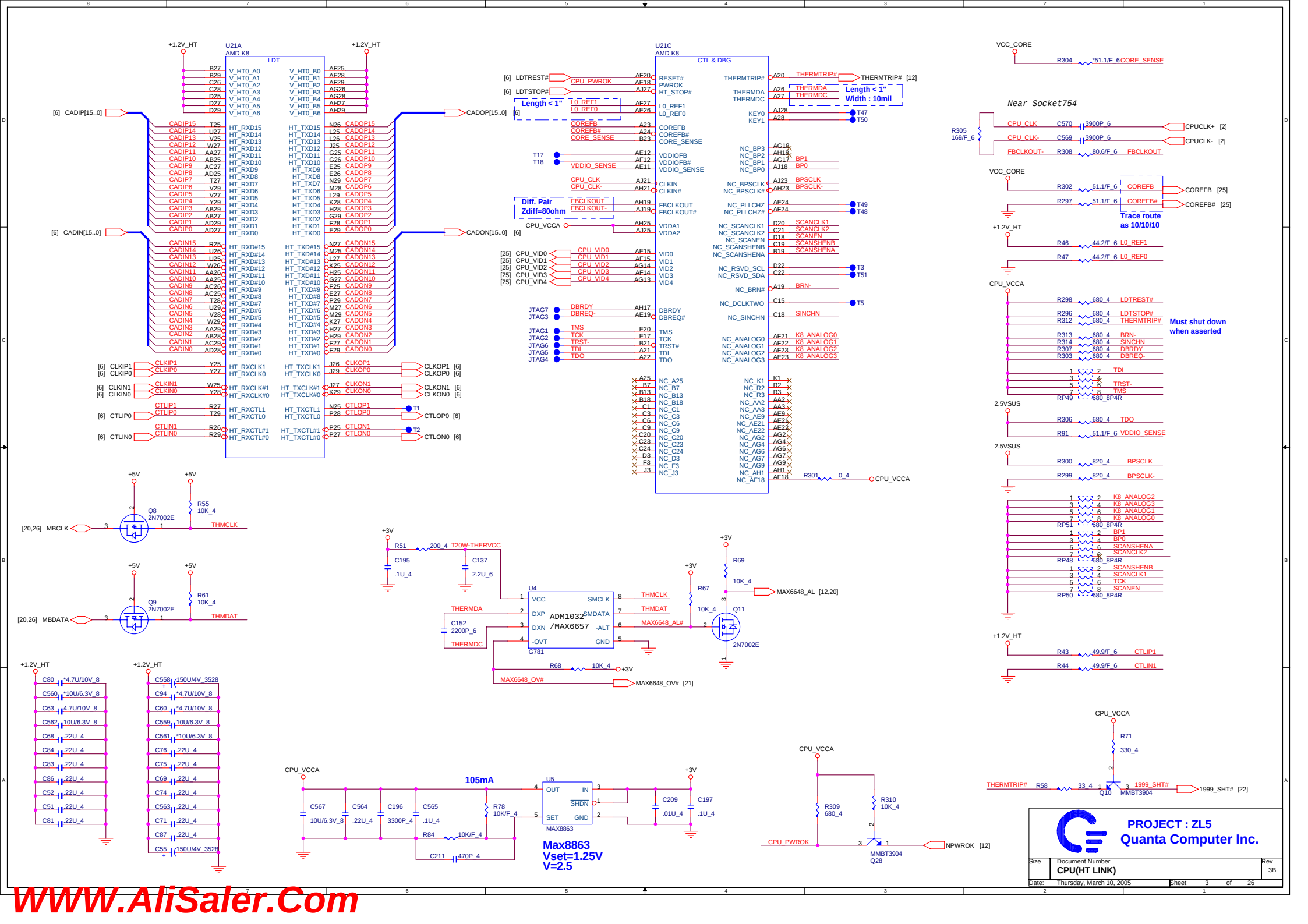
U21A
AMD K8
LDT
U21C
AMD K8
CTL & DBG
Near Socket754
Length < 1"
Width : 10mil
Length < 1"
Diff. Pair
Zdiff=80ohm
Trace route
as 10/10/10
Must shut down
when asserted
105mA
Max8863
Vset=1.25V
V=2.5
PROJECT : ZL5
Quanta Computer Inc.
CPU(HT LINK)
Thursday, March 10, 2005
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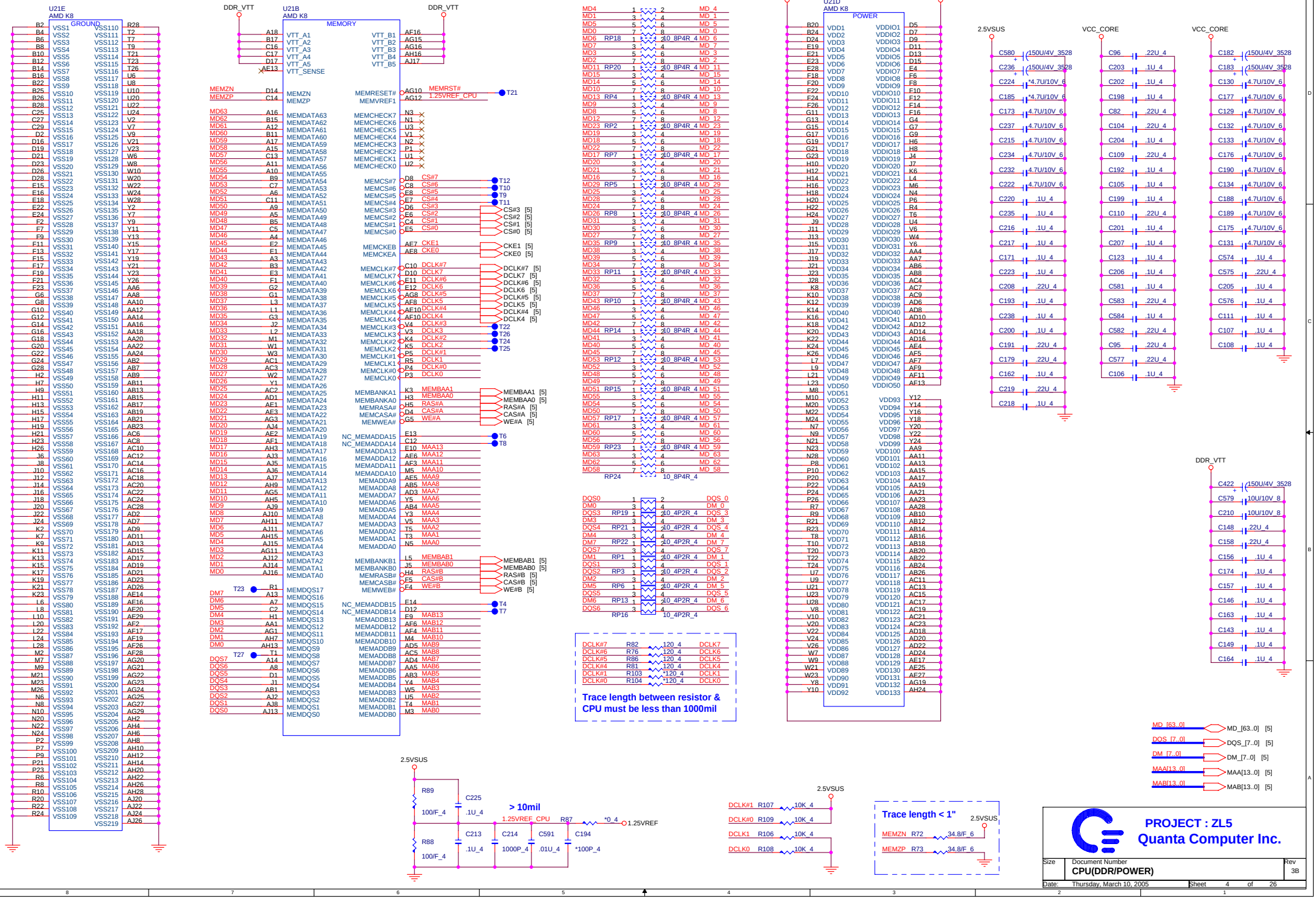
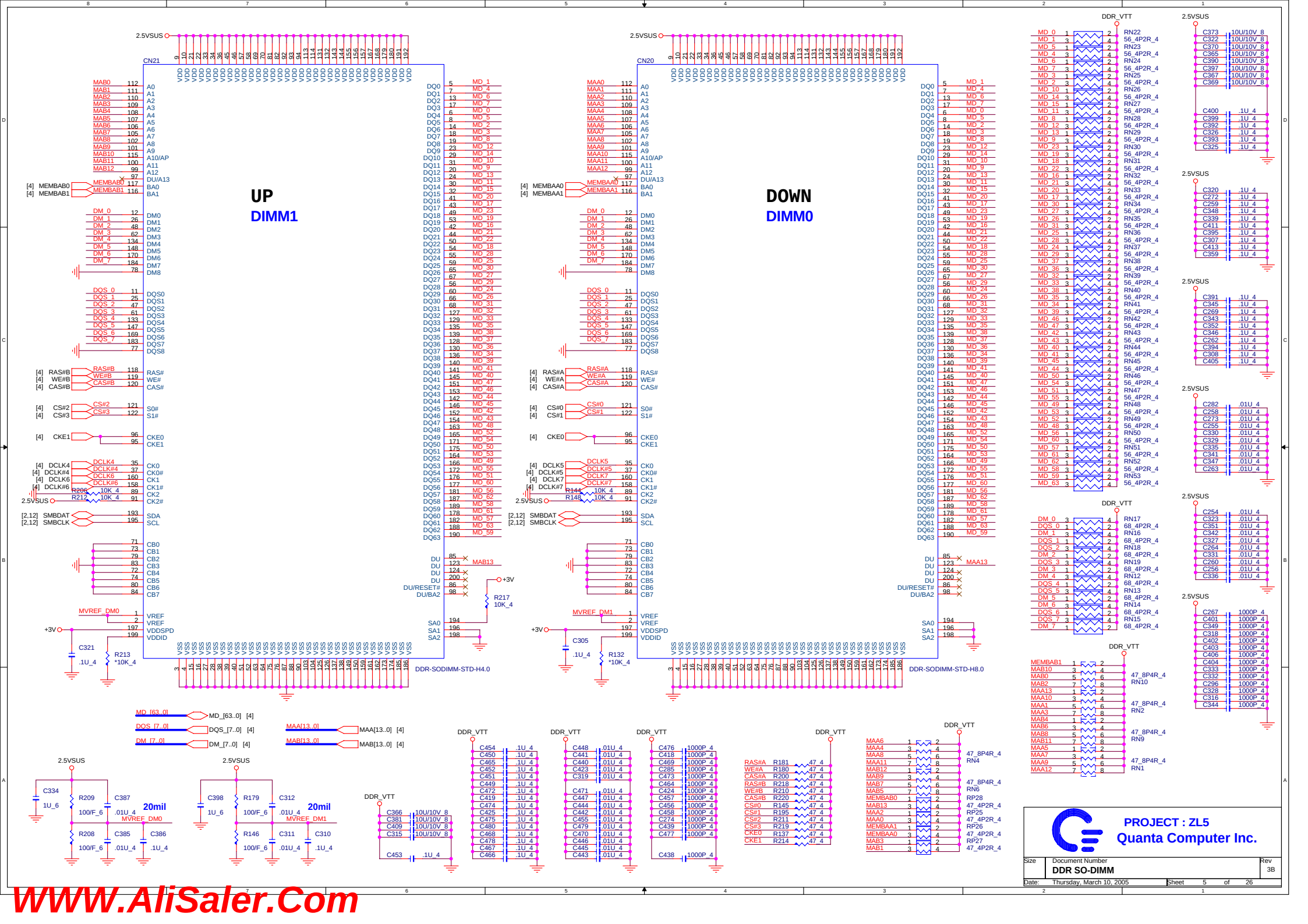
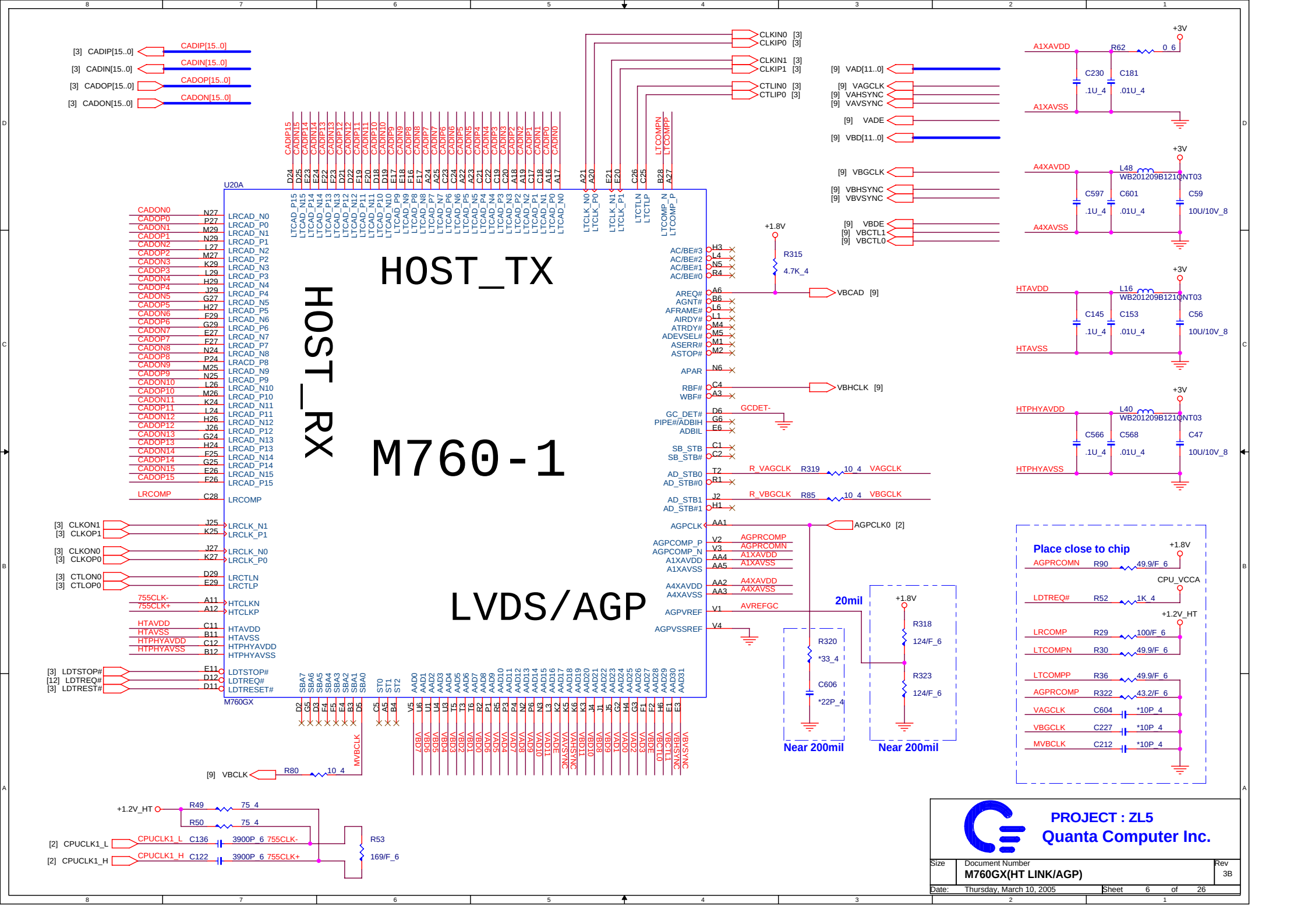
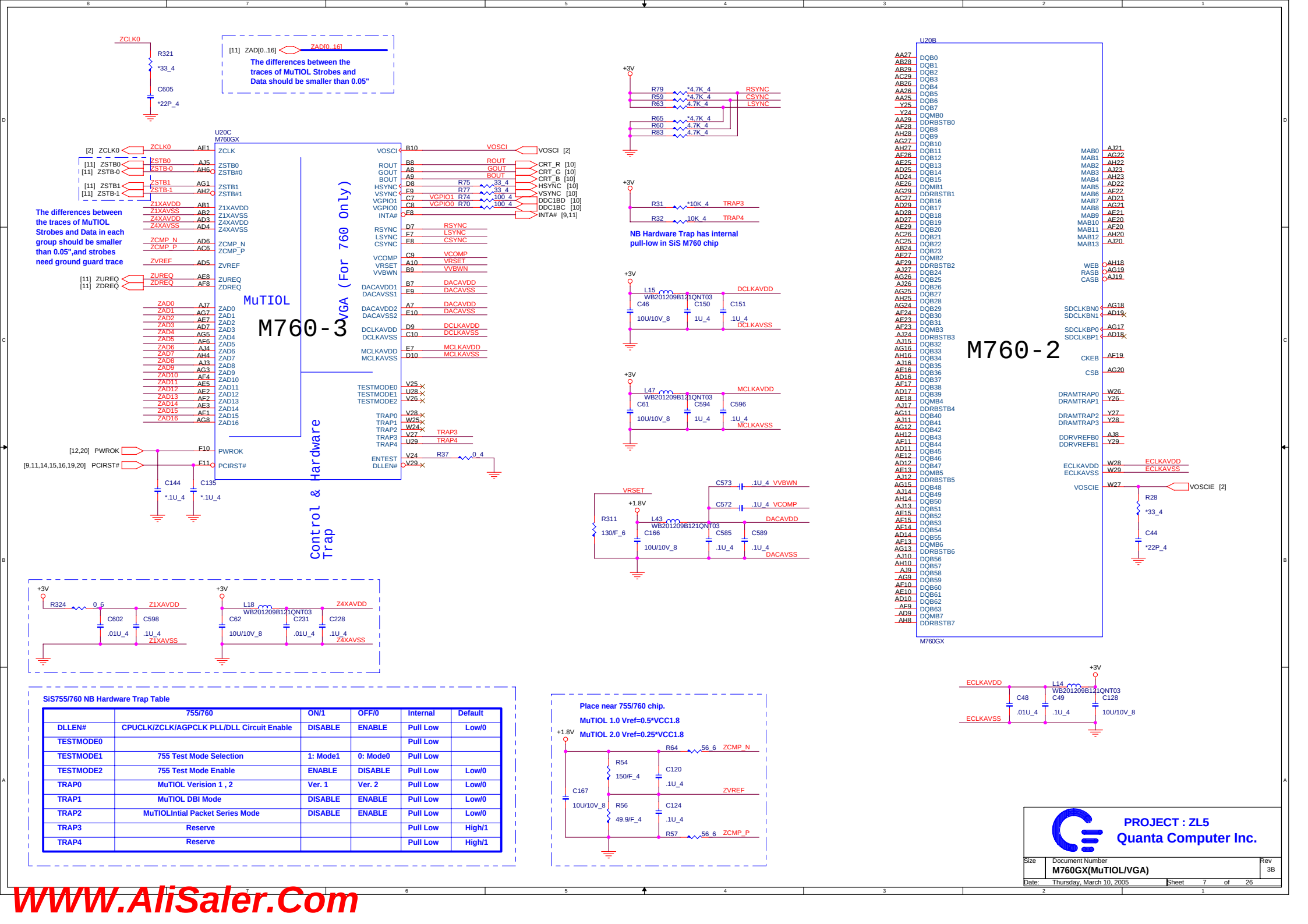
CPU DDR/POWER I/F






HOST_TX
HOST_RX
M760-1
LVDS/AGP
U20A
M760GX
[3] CADIP[15..0]
[3] CADIN[15..0]
[3] CADOP[15..0]
[3] CADON[15..0]
CADIP[15..0]
CADIN[15..0]
CADOP[15..0]
CADON[15..0]
CLKIN0 [3]
CLKIP0 [3]
CLKIN1 [3]
CLKIP1 [3]
CTLIN0 [3]
CTLIP0 [3]
[9] VAD[11..0]
[9] VAGCLK
[9] VAHSYNC
[9] VAVSYNC
[9] VADE
[9] VBD[11..0]
[9] VBGCLK
[9] VBHSYNC
[9] VBVSYNC
[9] VBDE
[9] VBCTL1
[9] VBCTL0
+3V
A1XAVDD
R62
0_6
C230
.1U_4
C181
.01U_4
A1XAVSS
A4XAVDD
L48
WB201209B121CNT03
C597
.1U_4
C601
.01U_4
C59
10U/10V_8
A4XAVSS
HTAVDD
L16
WB201209B121CNT03
C145
.1U_4
C153
.01U_4
C56
10U/10V_8
HTAVSS
HTPHYAVDD
L40
WB201209B121CNT03
C566
.1U_4
C568
.01U_4
C47
10U/10V_8
HTPHYAVSS
+1.8V
R315
4.7K_4
VBCAD [9]
VBHCLK [9]
GCDET-
R_VAGCLK
R319
10_4
VAGCLK
R_VBGCLK
R85
10_4
VBGCLK
AGPCLK0 [2]
AGPRCOMP
AGPRCOMN
A1XAVDD
A1XAVSS
A4XAVDD
A4XAVSS
AVREFGC
20mil
R320
*33_4
C606
*22P_4
R318
124/F_6
R323
124/F_6
Near 200mil
Near 200mil
Place close to chip
+1.8V
AGPRCOMN
R90
49.9/F_6
CPU_VCCA
LDTREQ#
R52
1K_4
+1.2V_HT
LRCOMP
R29
100/F_6
LTCOMPN
R30
49.9/F_6
LTCOMPP
R36
49.9/F_6
AGPRCOMP
R322
43.2/F_6
VAGCLK
C604
*10P_4
VBGCLK
C227
*10P_4
MVBCLK
C212
*10P_4
[9] VBCLK
R80
10_4
+1.2V_HT
R49
75_4
R50
75_4
[2] CPUCLK1_L
CPUCLK1_L
C136
3900P_6
755CLK-
[2] CPUCLK1_H
CPUCLK1_H
C122
3900P_6
755CLK+
R53
169/F_6
PROJECT : ZL5
Quanta Computer Inc.
Size
Document Number
M760GX(HT LINK/AGP)
Rev
3B
Date: Thursday, March 10, 2005
Sheet 6 of 26



	755/760	ON/1	OFF/0	Internal	Default
DLLEN#	CPUCLK/ZCLK/AGPCLK PLL/DLL Circuit Enable	DISABLE	ENABLE	Pull Low	Low/0
TESTMODE0				Pull Low	
TESTMODE1	755 Test Mode Selection	1: Mode1	0: Mode0	Pull Low	
TESTMODE2	755 Test Mode Enable	ENABLE	DISABLE	Pull Low	Low/0
TRAP0	MuTIOL Verision 1 , 2	Ver. 1	Ver. 2	Pull Low	Low/0
TRAP1	MuTIOL DBI Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP2	MuTIOLIntial Packet Series Mode	DISABLE	ENABLE	Pull Low	Low/0
TRAP3	Reserve			Pull Low	High/1
TRAP4	Reserve			Pull Low	High/1

If Support SiS M760LV IVDD=1.5V

M760-4

Power

M760-5

Power

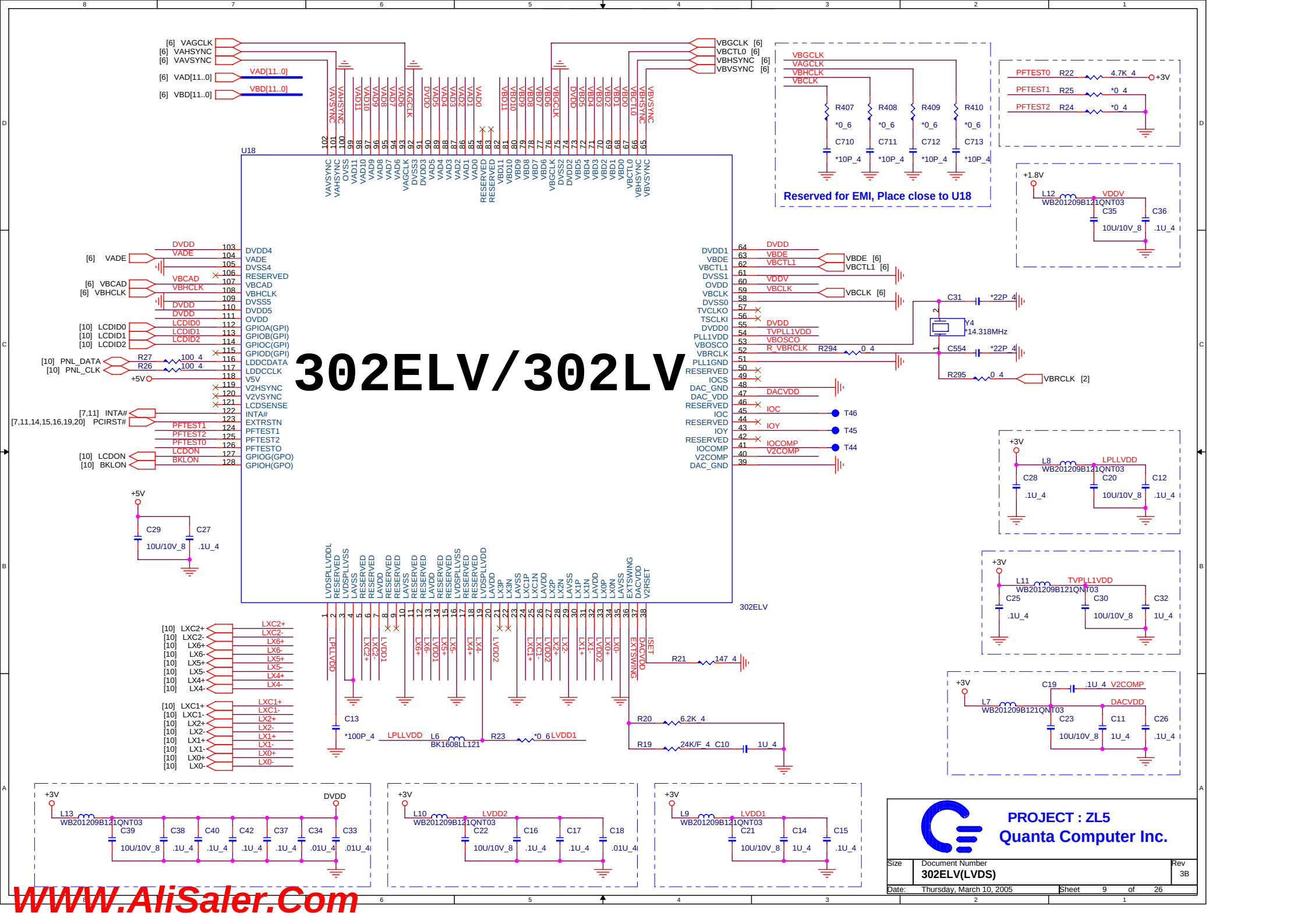
LAYOUT: Place HT bypass caps on topside near connected Lokar HT link.

Place these capacitors under 760 solder side.

PROJECT : ZL5

Quanta Computer Inc.

Size	Document Number	Rev
	M760GX(POWER)	3B
Date: Thursday, March 10, 2005	Sheet 8 of 26	


302ELV/302LV
U18
302ELV
Reserved for EMI, Place close to U18
PROJECT : ZL5
Quanta Computer Inc.
Size
Document Number
302ELV(LVDS)
Rev
3B
Date: Thursday, March 10, 2005
Sheet 9 of 26
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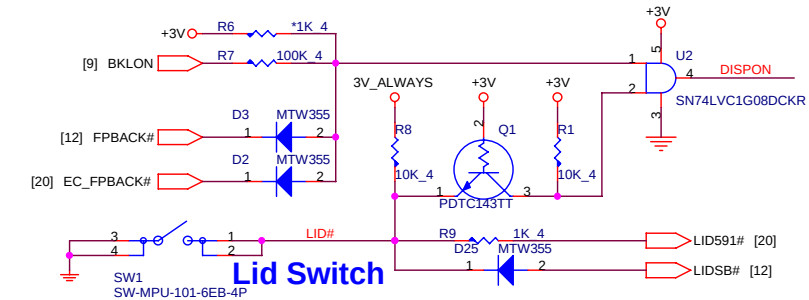
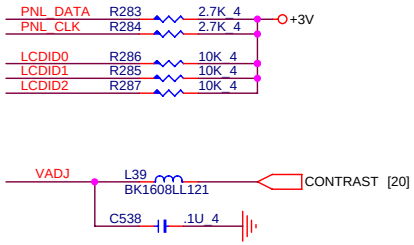
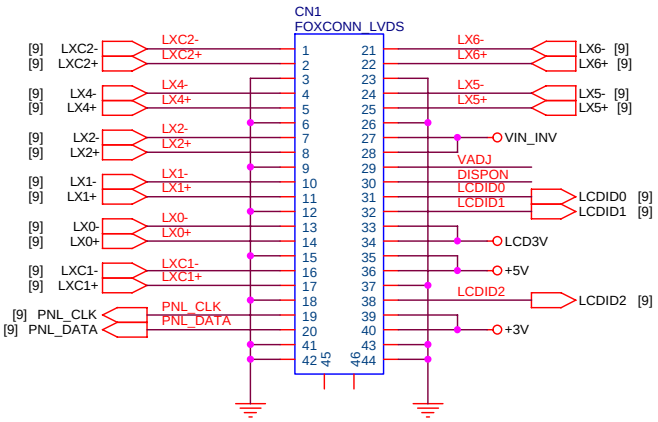
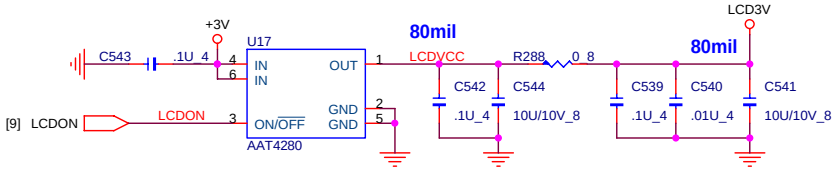
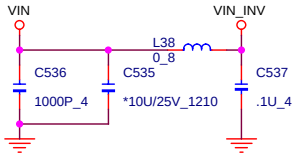
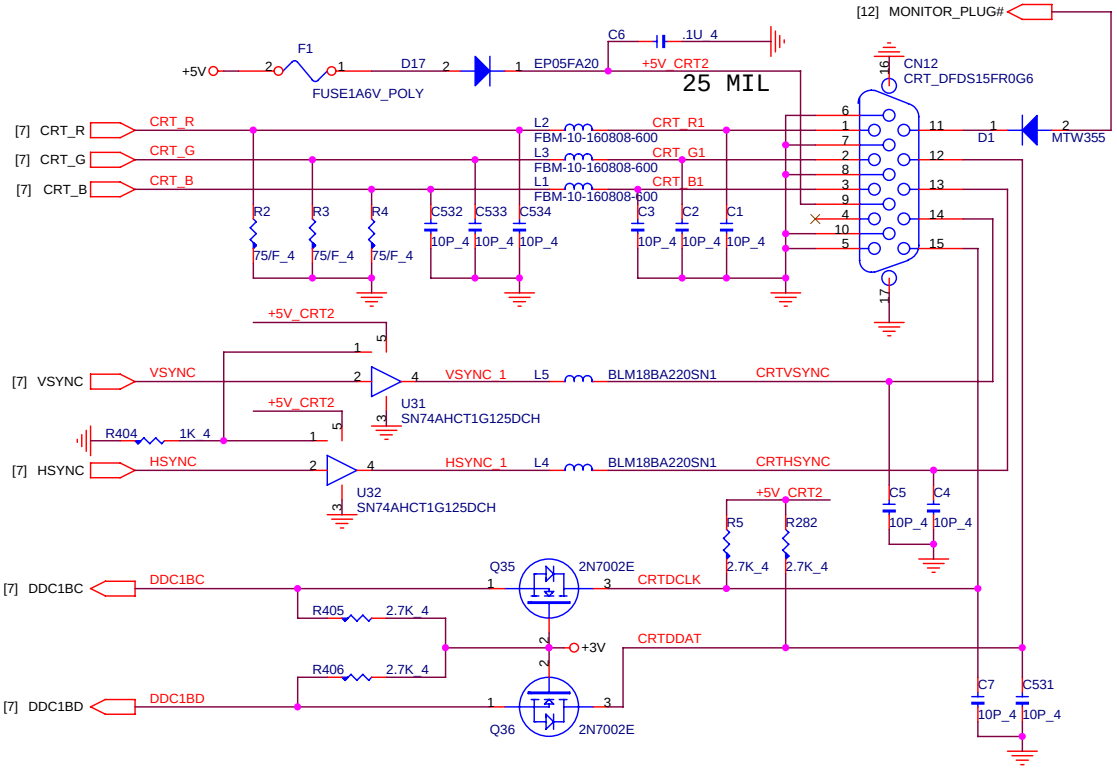


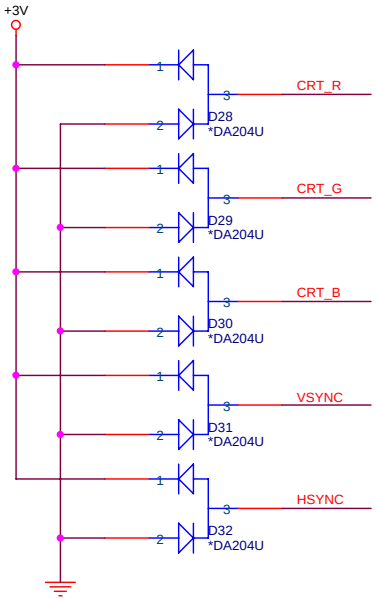






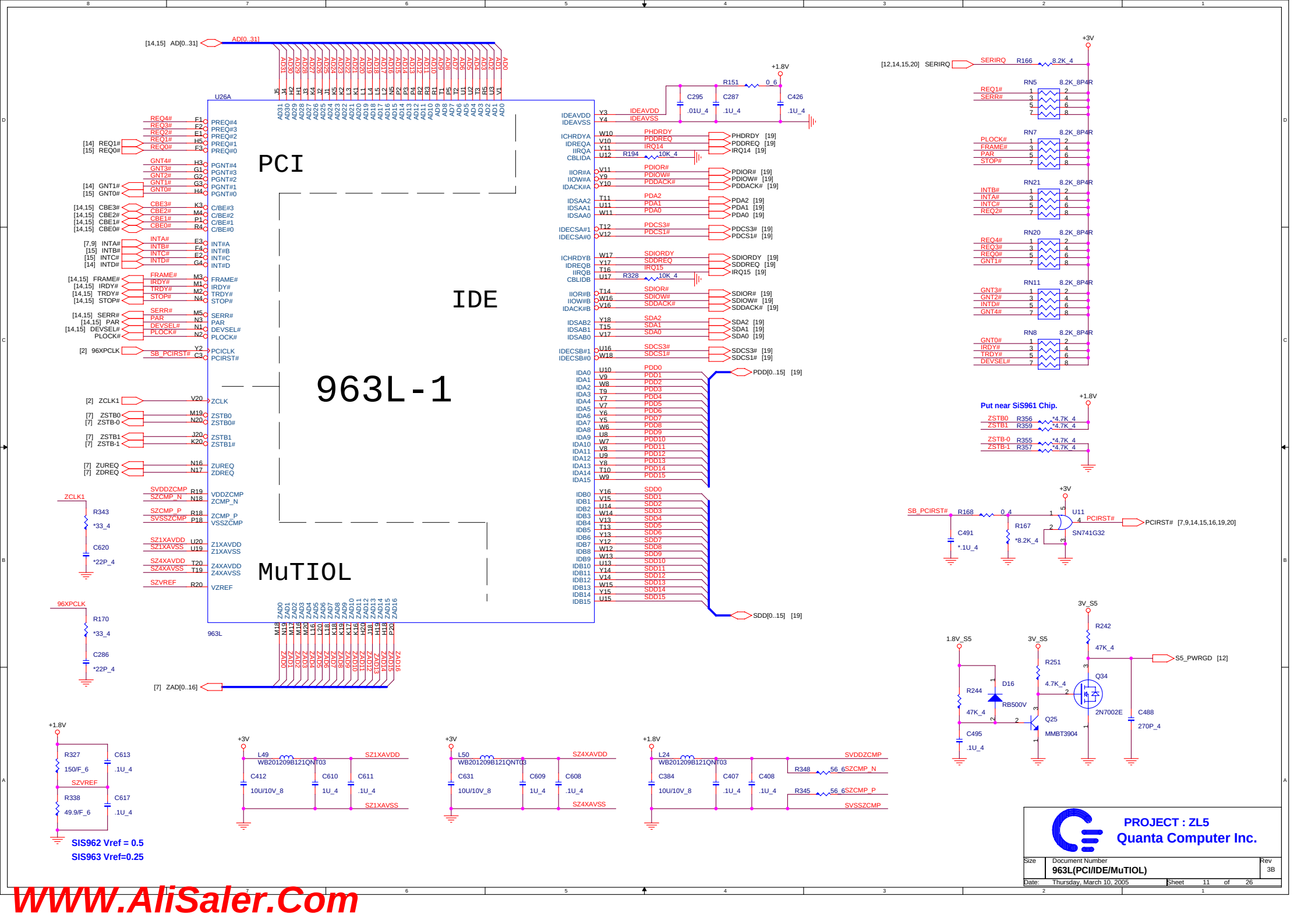


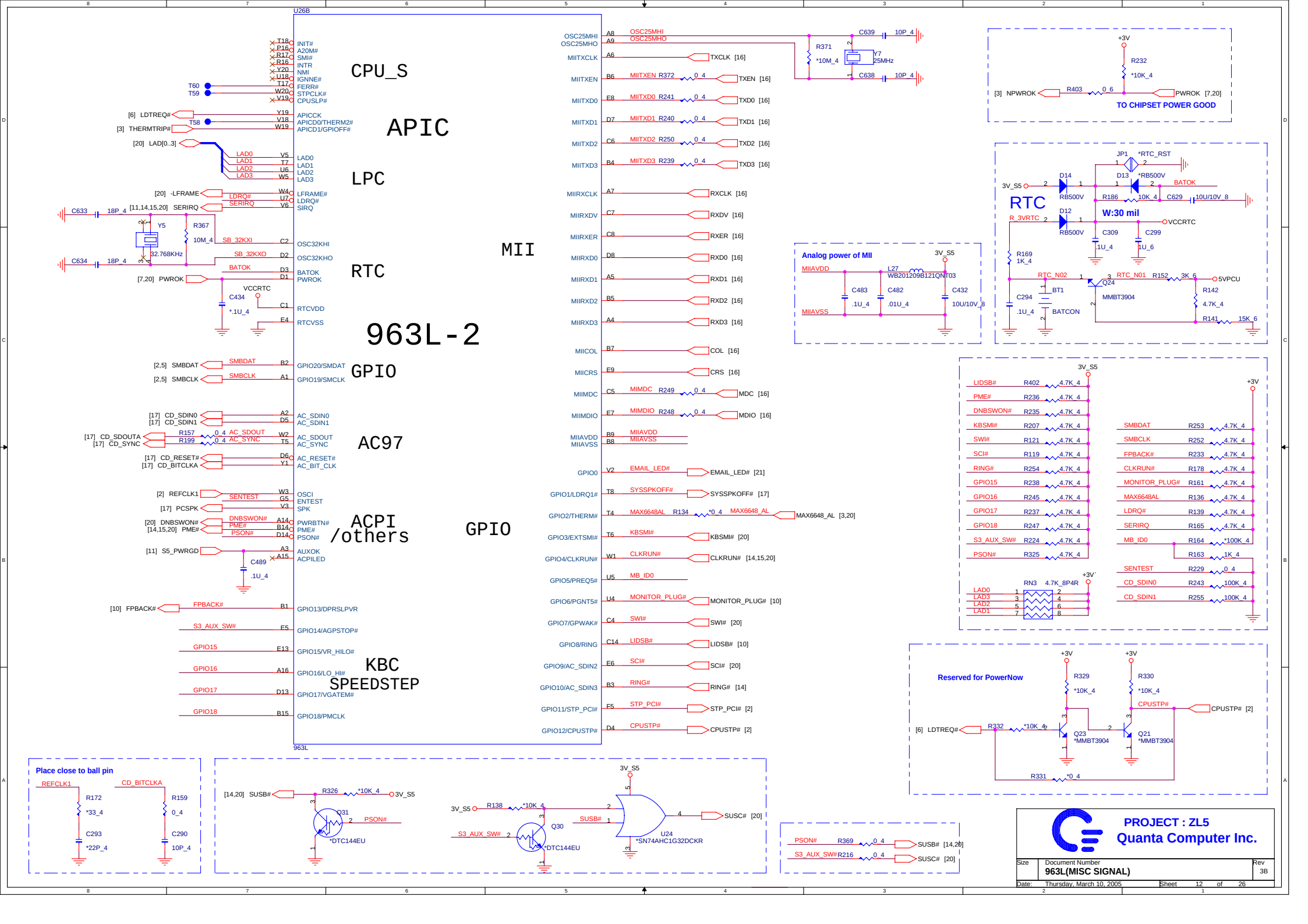


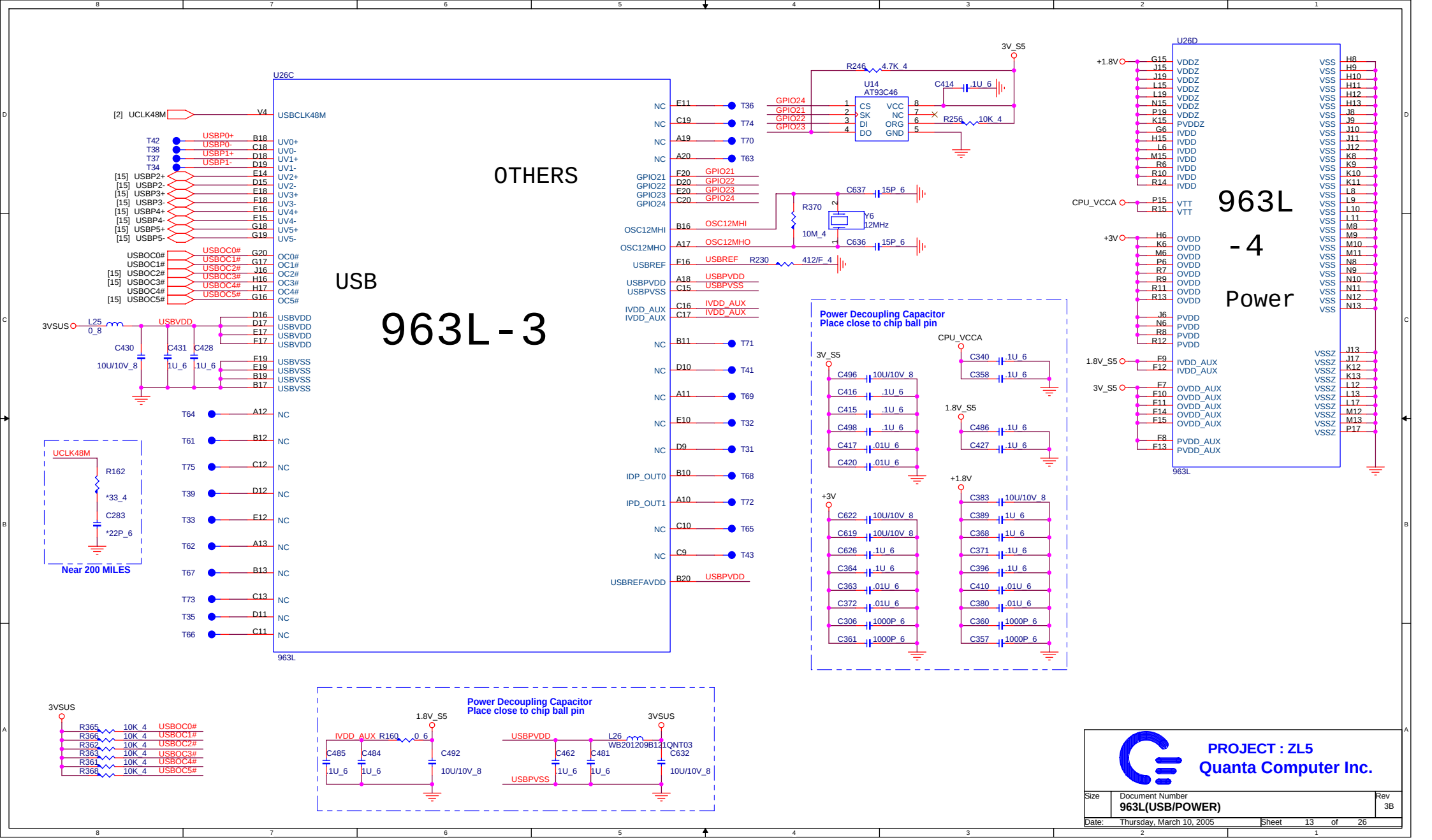


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS	3B
Date: Thursday, March 10, 2005	Sheet 10 of 26	




U26B
963L-2
CPU_S
APIC
LPC
RTC
MII
GPIO
AC97
ACPI /others
GPIO
KBC SPEEDSTEP
963L
INIT#
A20M#
SMI#
INTR
NMI
IGNNE#
FERR#
STPCLK#
CPUSLP#
APICCK
APICD0/THERM2#
APICD1/GPIOFF#
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ#
SIRQ
OSC32KHI
OSC32KHO
BATOK
PWROK
RTCVDD
RTCVSS
GPIO20/SMDAT
GPIO19/SMCLK
AC_SDIN0
AC_SDIN1
AC_SDOUT
AC_SYNC
AC_RESET#
AC_BIT_CLK
OSCI
ENTEST
SPK
PWRBTN#
PME#
PSON#
AUXOK
ACPILED
GPIO13/DPRSLPVR
GPIO14/AGPSTOP#
GPIO15/VR_HILO#
GPIO16/LO_HI#
GPIO17/VGATEM#
GPIO18/PMCLK
OSC25MHI
OSC25MHO
MIITXCLK
MIITXEN
MIITXD0
MIITXD1
MIITXD2
MIITXD3
MIIRXCLK
MIIRXDV
MIIRXER
MIIRXD0
MIIRXD1
MIIRXD2
MIIRXD3
MIICOL
MIICRS
MIIMDC
MIIMDIO
MIIAVDD
MIIAVSS
GPIO0
GPIO1/LDRQ1#
GPIO2/THERM#
GPIO3/EXTSMI#
GPIO4/CLKRUN#
GPIO5/PREQ5#
GPIO6/PGNT5#
GPIO7/GPWAK#
GPIO8/RING
GPIO9/AC_SDIN2
GPIO10/AC_SDIN3
GPIO11/STP_PCI#
GPIO12/CPUSTP#
TXCLK [16]
TXEN [16]
TXD0 [16]
TXD1 [16]
TXD2 [16]
TXD3 [16]
RXCLK [16]
RXDV [16]
RXER [16]
RXD0 [16]
RXD1 [16]
RXD2 [16]
RXD3 [16]
COL [16]
CRS [16]
MDC [16]
MDIO [16]
EMAIL_LED# [21]
SYSSPKOFF# [17]
MAX6648_AL [3,20]
KBSMI# [20]
CLKRUN# [14,15,20]
MONITOR_PLUG# [10]
SWI# [20]
LIDSB# [10]
SCI# [20]
RING# [14]
STP_PCI# [2]
CPUSTP# [2]
Analog power of MII
L27 WB201209B121QNT03
C483 .1U_4
C482 .01U_4
C432 10U/10V_8
RTC
W:30 mil
JP1 *RTC_RST
D14 RB500V
D13 *RB500V
D12 RB500V
BATOK
R186 10K_4
C629 10U/10V_8
C309 .1U_4
C299 1U_6
R169 1K_4
RTC_N02
RTC_N01
R152 3K_6
Q24 MMBT3904
R142 4.7K_4
R141 15K_6
C294 .1U_4
BT1 BATCON
TO CHIPSET POWER GOOD
R232 *10K_4
R403 0_6
Reserved for PowerNow
R329 *10K_4
R330 *10K_4
R332 *10K_4
Q23 *MMBT3904
Q21 *MMBT3904
R331 *0_4
Place close to ball pin
R172 *33_4
C293 *22P_4
R159 0_4
C290 10P_4
Q31 *DTC144EU
Q30 *DTC144EU
U24 *SN74AHC1G32DCKR
PROJECT : ZL5
Quanta Computer Inc.
963L(MISC SIGNAL)
Thursday, March 10, 2005
Sheet 12 of 26



ID Select : AD17
Interrupt Pin : INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#

U13
PCI1410A

U15
TPS2211A

CARDBUS SLOT

CN22

FOX_WZ21131-G2

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	PCMCIA(PCI1410)	3B

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ID Select : AD22
Interrupt Pin : INTB# , INTC#
Request Indicate : REQ0#
Grant Indicate : GNT0#

PCLK_MP R66 *22_4 C161 *10P_4

IDSEL_MP R48 150_4 AD22

[11,14] AD[0..31] AD[0..31]

MINI-PCI

CN17

[21] WIRELESS_LED
[20] RF_EN
D4 MTW355
[11] INTC#
[2] PCLK_MP
[11] REQ0#
[11,14] CBE3#
[11,14] CBE2#
[11,14] IRDY#
[12,14,20] CLKRUN#
[11,14] SERR#
R42 10K_4
[11,14] CBE1#

TIP	1	2	RING
LAN1	3	4	LAN2
LAN3	5	6	LAN4
LAN5	7	8	LAN6
LAN7	9	10	LAN8
LED_GP	11	12	LED_YP
LED_GN	13	14	LED_YN
NC1	15	16	NC2
-INTB	17	18	+5V
+3V	19	20	-INTA
R(IRQ3)	21	22	R(IRQ4)
GND	23	24	+3VAUX
PCICLK	25	26	-RST
GND	27	28	+3V
-REQ	29	30	-GNT
+3V	31	32	GND
AD31	33	34	-PME
AD29	35	36	(V)
GND	37	38	AD30
AD27	39	40	+3V
AD25	41	42	AD28
(V)	43	44	AD26
-CBE3	45	46	AD24
AD23	47	48	IDSEL
GND	49	50	GND
AD21	51	52	AD22
AD19	53	54	AD20
GND	55	56	PAR
AD17	57	58	AD18
-CBE2	59	60	AD16
-IRDY	61	62	GND
+3V	63	64	-FRAME
-CLKRUN	65	66	-TRDY
-SERR	67	68	-STOP
GND	69	70	+3V
-PERR	71	72	-DEVSEL
-CBE1	73	74	GND
AD14	75	76	AD15
GND	77	78	AD13
AD12	79	80	AD11
AD10	81	82	GND
GND	83	84	AD9
AD8	85	86	-CBE0
AD7	87	88	+3V
+3V	89	90	AD6
AD5	91	92	AD4
(V)	93	94	AD2
AD3	95	96	AD0
+5V	97	98	(V)
AD1	99	100	SERIRQ
GND	101	102	M66EN
SYNC	103	104	SDOUT
SDIN0	105	106	SDIN1
BITCLK	107	108	-RESET
-AC_PRIMARY	109	110	-MPCICACK
BEEP	111	112	AGND
AGND	113	114	+SPK
+MIC	115	116	-SPK
-MIC	117	118	AGND
AGND	119	120	NC4
-RI	121	122	+3VAUX
+5VA	123	124	3VSUS
GND	125	126	GND

MINIPCI_DGMC4000382

INTB# [11]
PCIRST# [7,9,11,14,16,19,20]
GNT0# [11]
PME# [12,14,20]
PAR [11,14]
FRAME# [11,14]
TRDY# [11,14]
STOP# [11,14]
DEVSEL# [11,14]
CBE0# [11,14]
SERIRQ [11,12,14,20]
SDIN1_MINI R33 *10K_4 3V_S5

VIN +5V
C221 .1U_6
C557 .1U_6
C50 .1U_6
C709 .1U_6

+3V: C186 .1U_4, C54 .1U_4, C53 .1U_4, C169 .1U_4
+5V: C41 .1U_4, C187 .1U_4
VIN: C642 *.01U_6, C683 *.01U_6, C684 *.1U_6, C641 *.1U_6, C640 *.1U_6, C682 *10U/25V_1210

[20] USBPWR_ON# R94 0_4 USBPWRON# R92 *0_4

U6 TPS2061DGNR: 5VSUS, USBPWRON#, USBPWR2, R100 0_4 USBOC2# [13], R96 *6.34K/F_6
U9 TPS2061DGNR: 5VSUS, USBPWRON#, USBPWR3, R124 0_4 USBOC3# [13], R122 *6.34K/F_6
U16 TPS2061DGNR: 5VSUS, USBPWRON#, USBPWR5, R267 0_4 USBOC5# [13], R268 *6.34K/F_6

USB2POWER: C240 47U/6.3V_1210, USBPWR2, L19 BK2125HS330, L17 DLW21HN900SQ2L, [13] USBP2-, [13] USBP2+, BUSBP2-, BUSBP2+, C226 *10P_4, C233 *10P_4, CN18 USB_DFHD04MR671

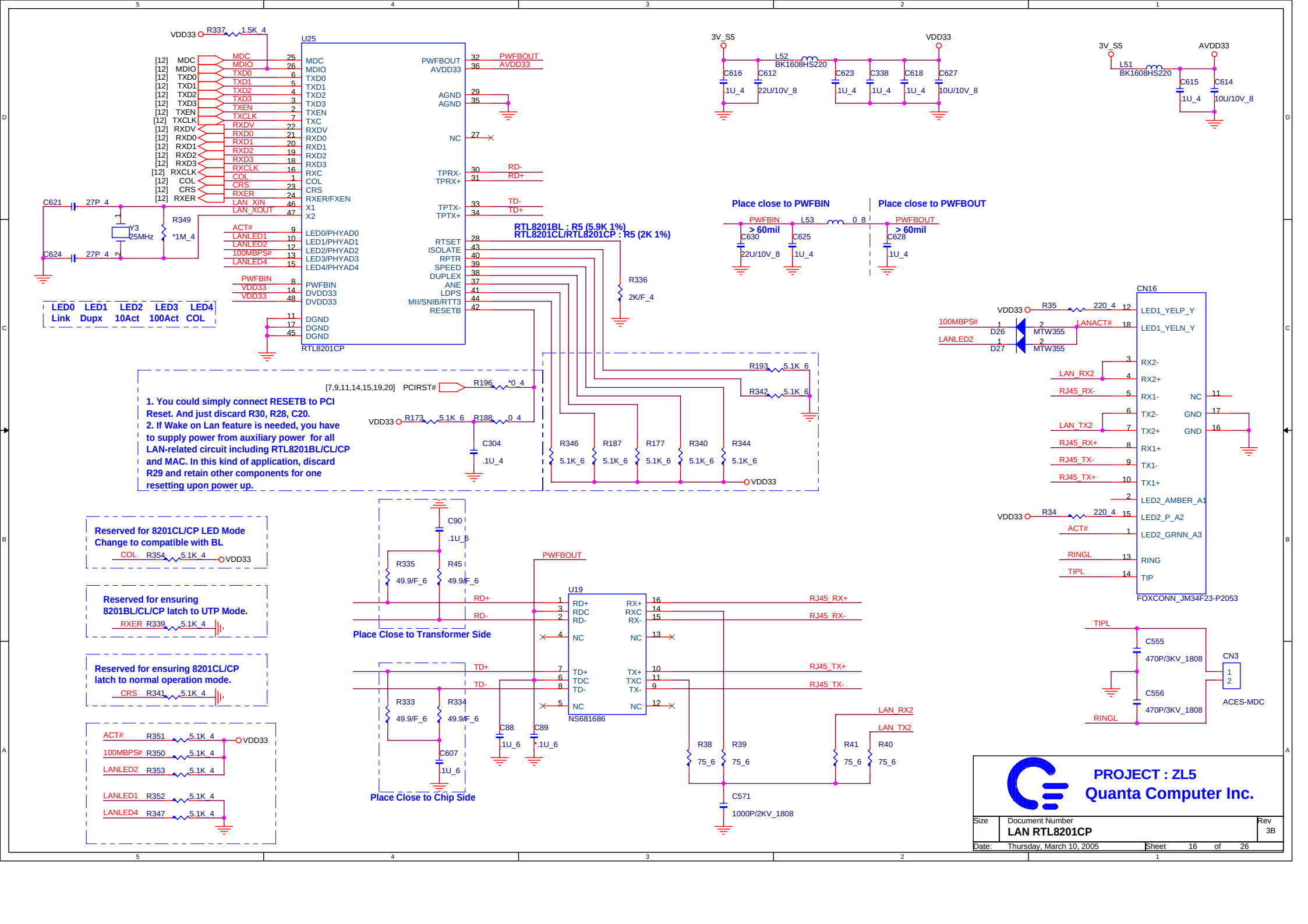
USB3POWER: C251 47U/6.3V_1210, USBPWR3, L21 BK2125HS330, L20 DLW21HN900SQ2L, [13] USBP3-, [13] USBP3+, BUSBP3-, BUSBP3+, C243 *10P_4, C246 *10P_4, CN19 USB_DFHD04MR671

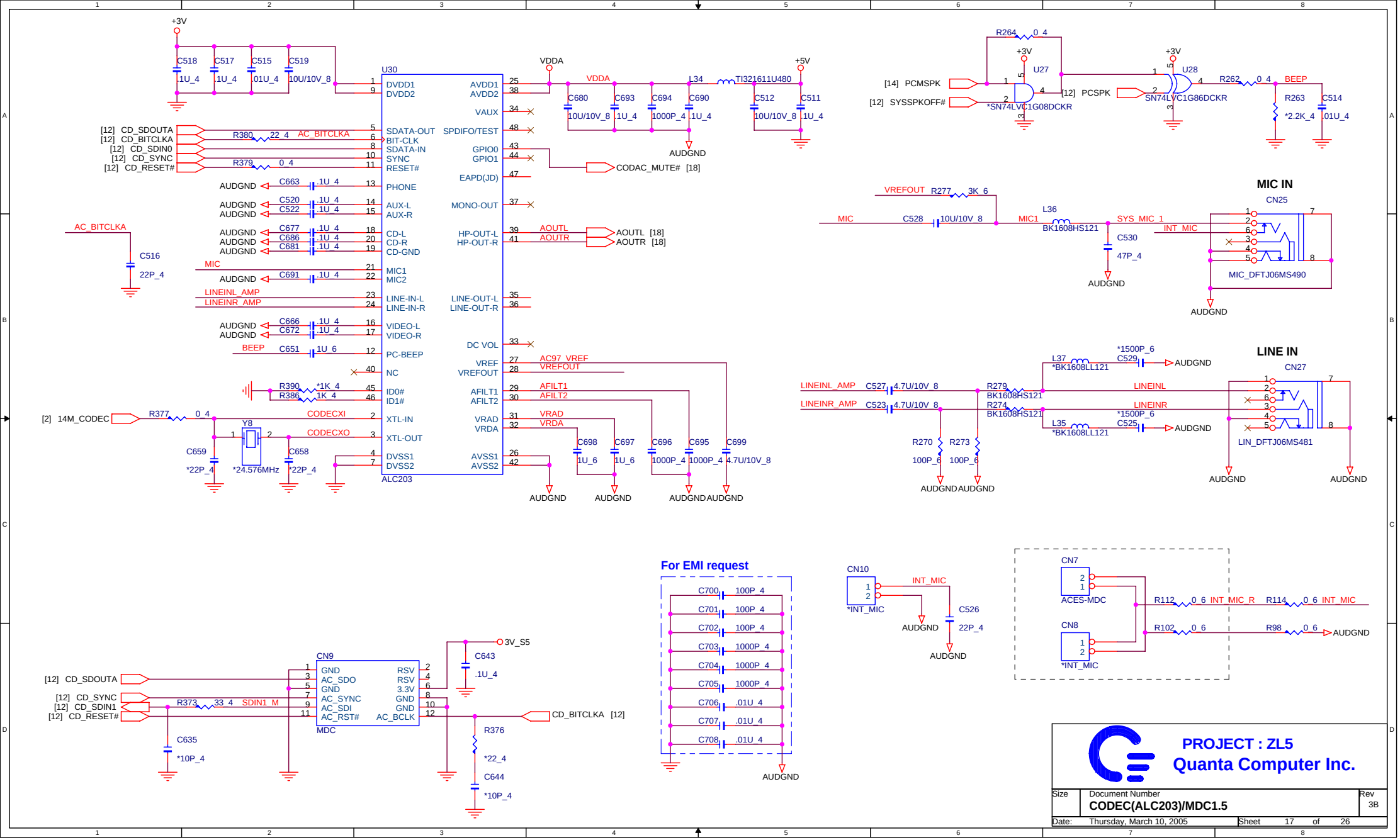
USB5POWER: C521 47U/6.3V_1210, USBPWR5, L32 BK2125HS330, L33 DLW21HN900SQ2L, [13] USBP5-, [13] USBP5+, BUSBP5-, BUSBP5+, C678 *10P_4, C679 *10P_4, CN24 USB_DFHD04MR671

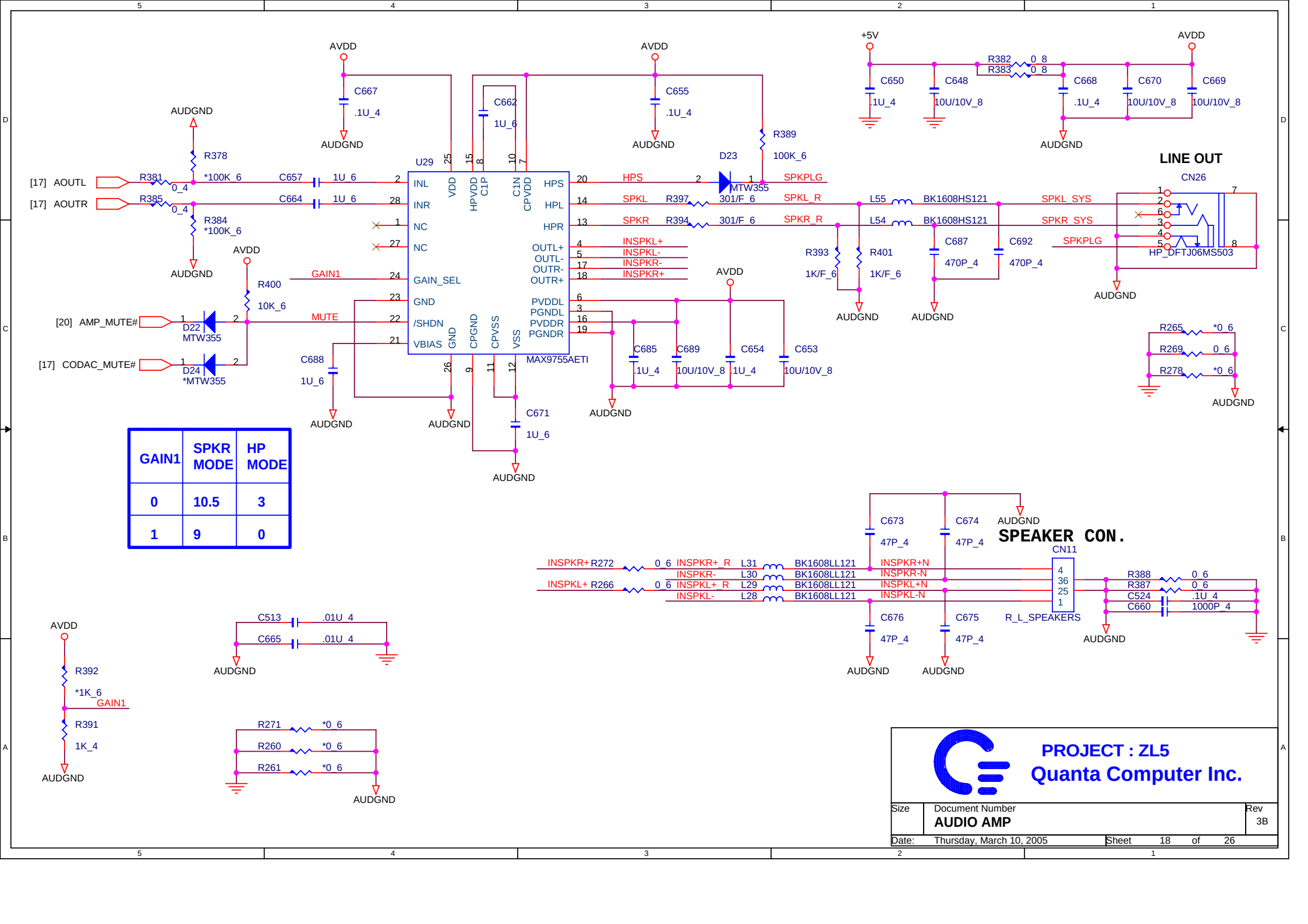
BT_POWERON# [20]
Q29 AO3403
3VSUS
C590 10U/10V_8
L42 BK2125HS330
BT_POWER
L41 DLW21HN900SQ2L
[13] USBP4+
[13] USBP4-
BUSBP4+
BUSBP4-
C587 *10P_4
C588 *10P_4
[21] BT_LED
C586 .01U_4
CN5 PTWO_MINIUSB

PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI/USB	3B
Date: Thursday, March 10, 2005	Sheet 15 of 26	


U25
RTL8201CP
RTL8201BL : R5 (5.9K 1%)
RTL8201CL/RTL8201CP : R5 (2K 1%)
LED0 LED1 LED2 LED3 LED4
Link Dupx 10Act 100Act COL
1. You could simply connect RESETB to PCI Reset. And just discard R30, R28, C20.
2. If Wake on Lan feature is needed, you have to supply power from auxiliary power for all LAN-related circuit including RTL8201BL/CL/CP and MAC. In this kind of application, discard R29 and retain other components for one resetting upon power up.
Reserved for 8201CL/CP LED Mode Change to compatible with BL
Reserved for ensuring 8201BL/CL/CP latch to UTP Mode.
Reserved for ensuring 8201CL/CP latch to normal operation mode.
Place Close to Transformer Side
Place Close to Chip Side
Place close to PWFBIN
Place close to PWFBOUT
U19
NS681686
CN16
FOXCONN_JM34F23-P2053
CN3
ACES-MDC
PROJECT : ZL5
Quanta Computer Inc.
LAN RTL8201CP
Thursday, March 10, 2005
Sheet 16 of 26



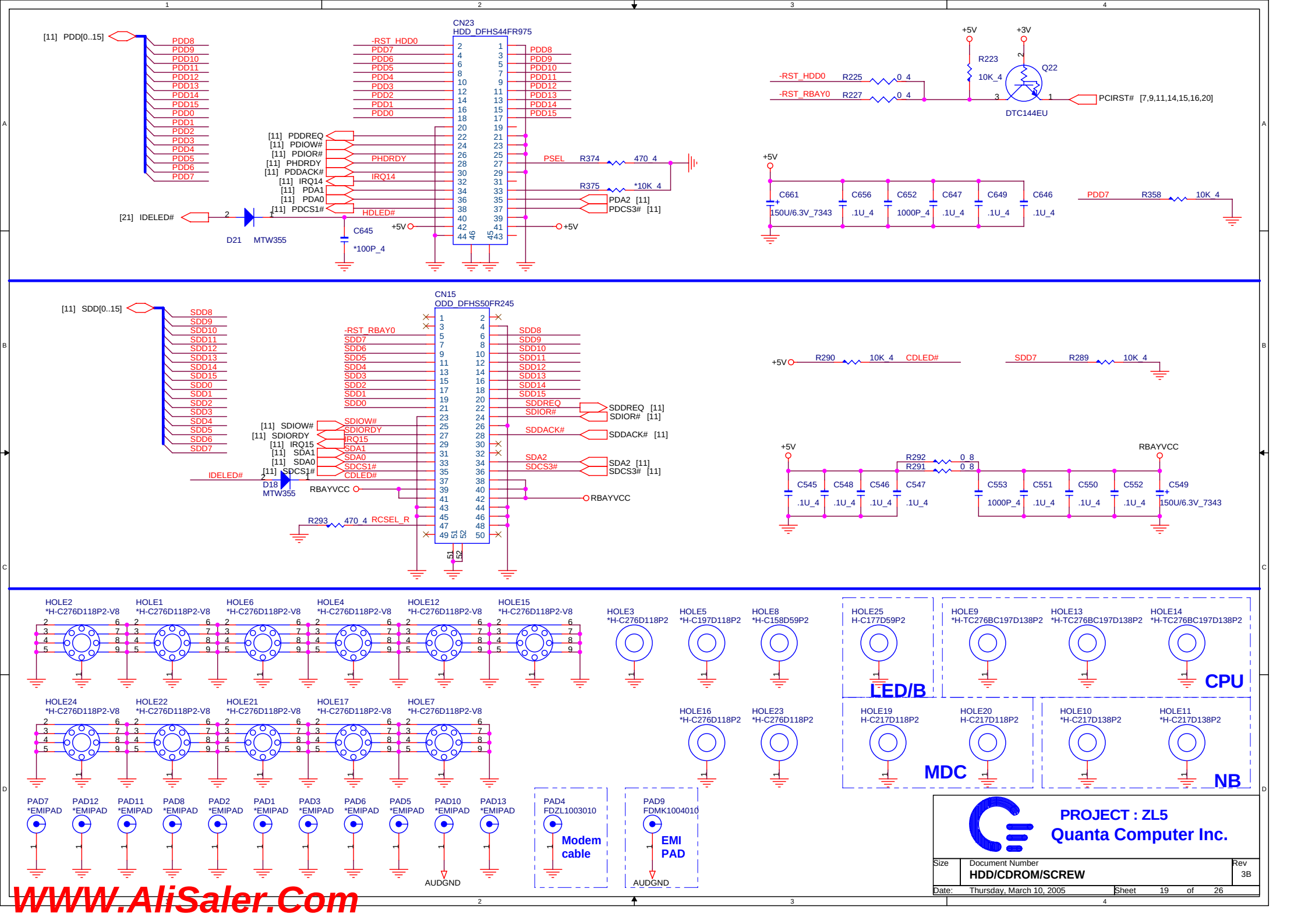


GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

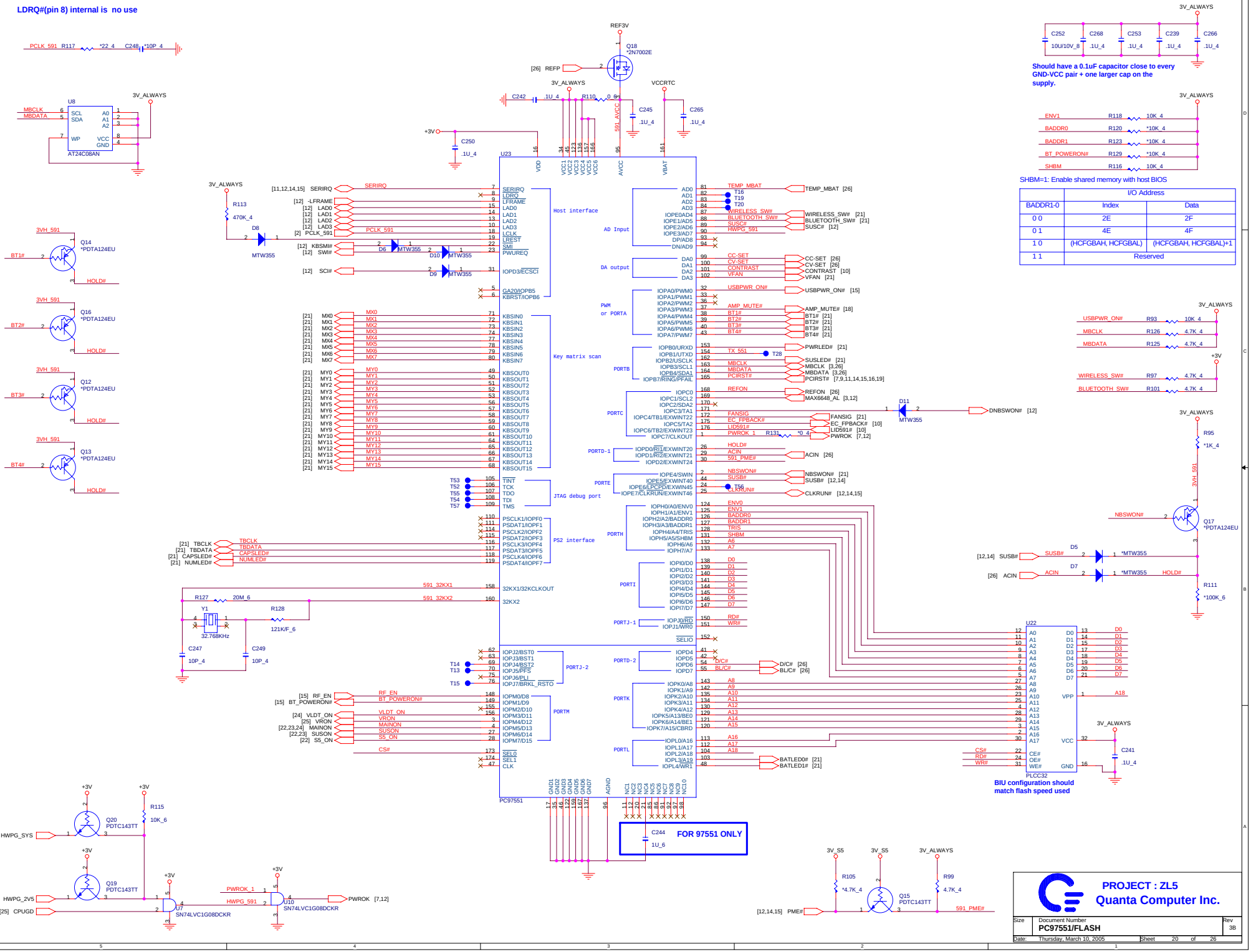
PROJECT : ZL5

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP	3B
Date: Thursday, March 10, 2005	Sheet 18 of 26	



LDRQ#(pin 8) internal is no use



PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	PC97551/FLASH	3B

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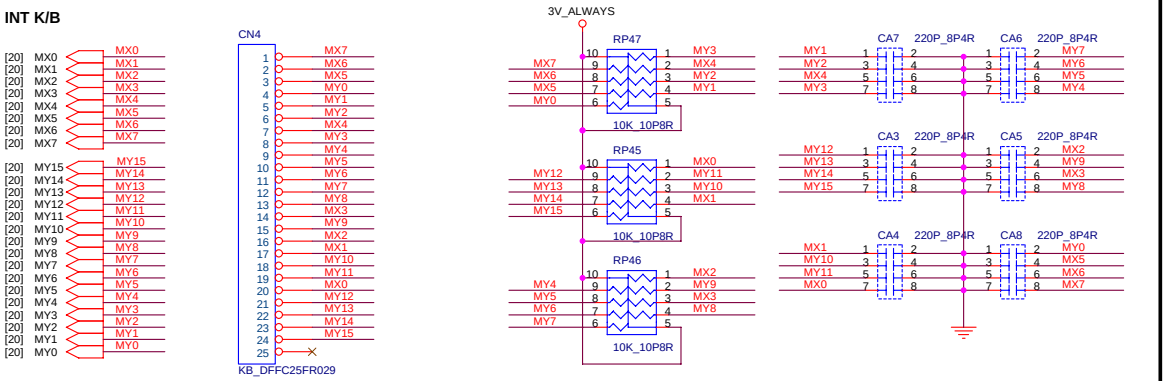
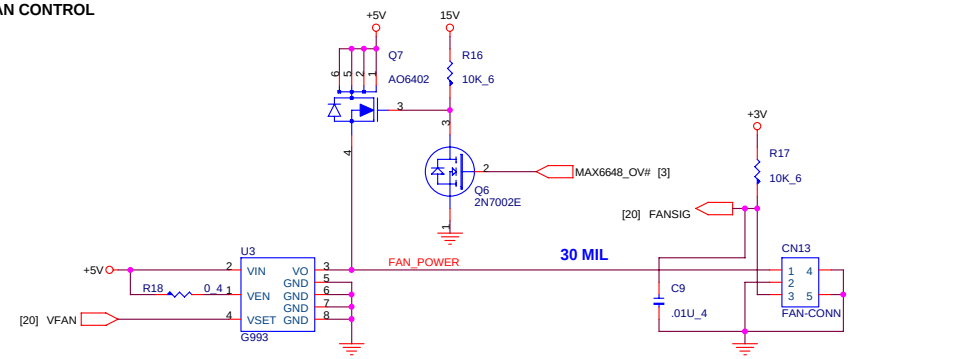
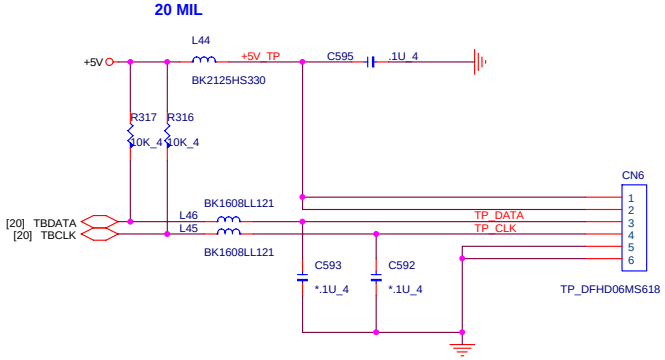
INT K/B

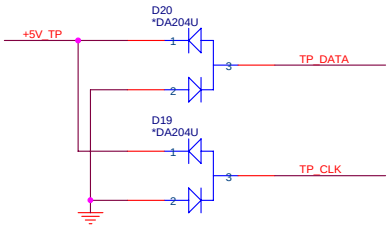


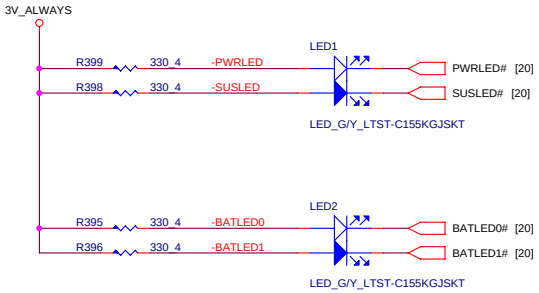
FAN CONTROL

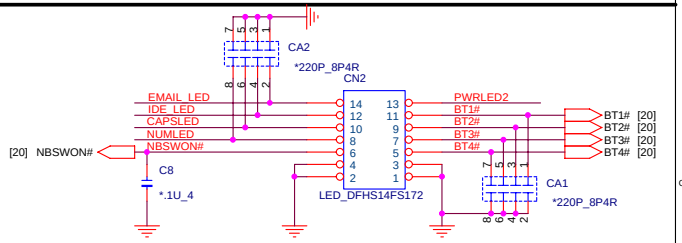


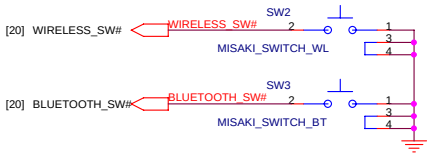
TOUCH PAD

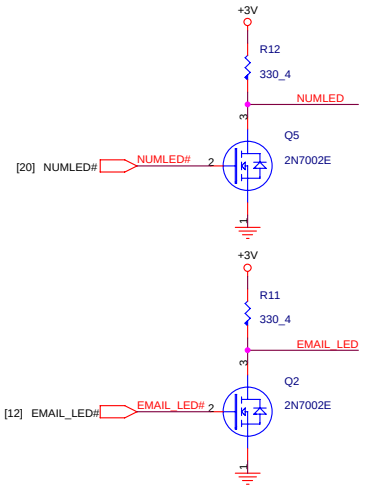


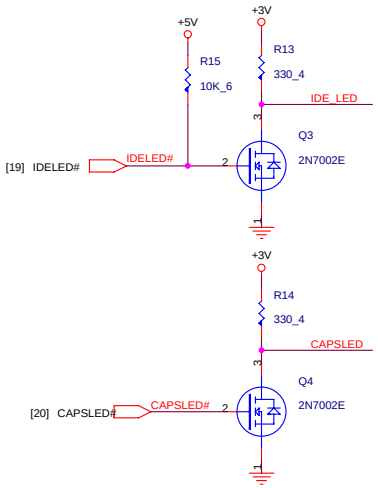


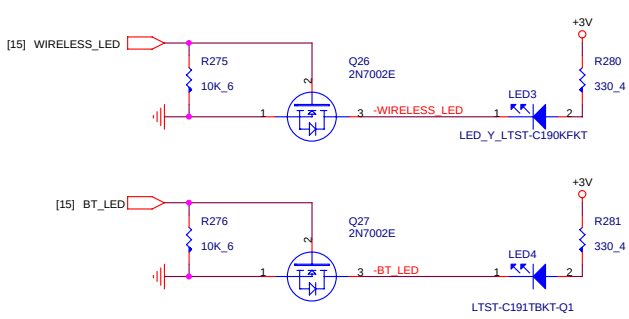






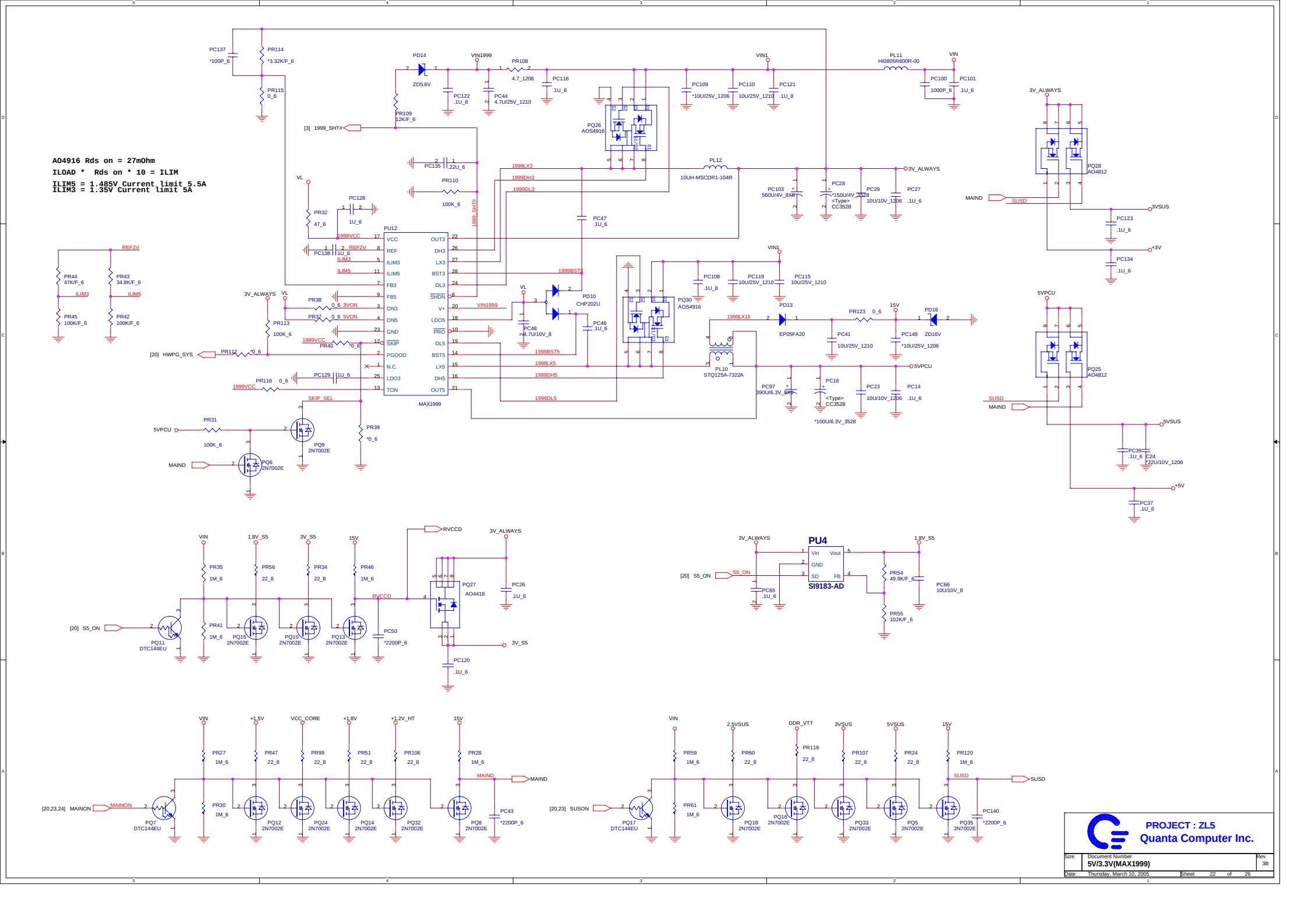


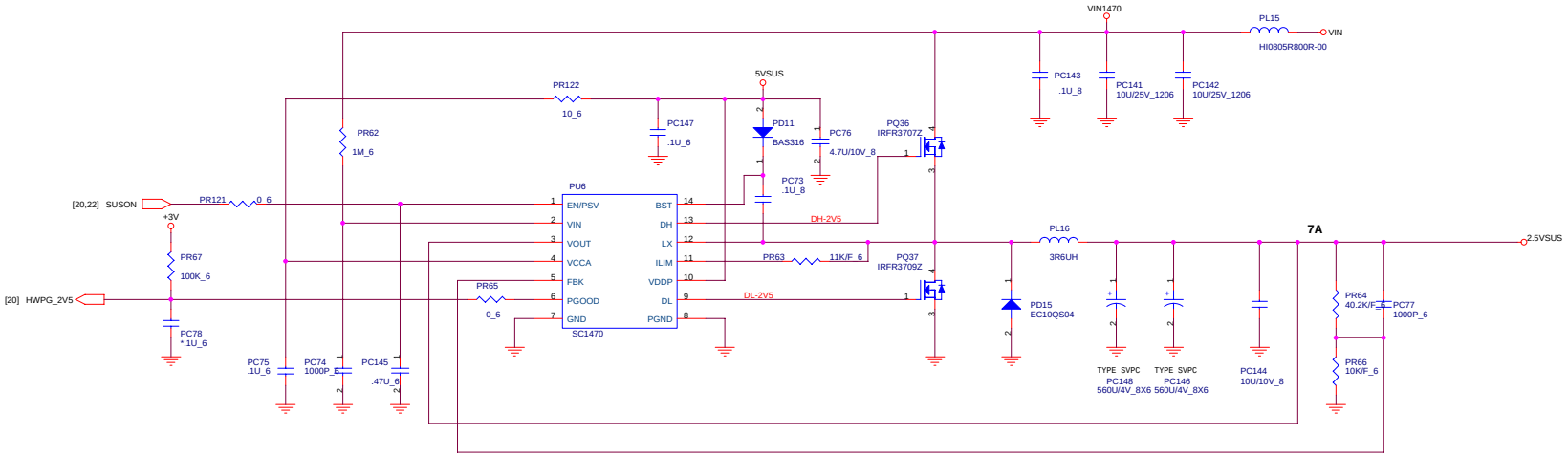


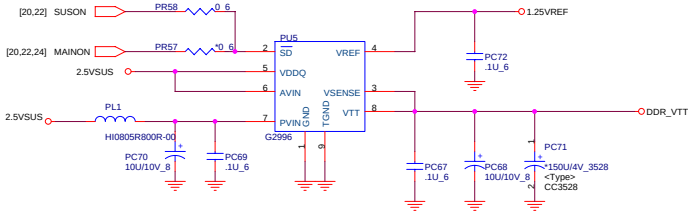


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	TP/FAN/SWITCH/LED/KB	3B
Date: Thursday, March 10, 2005	Sheet 21 of 26	

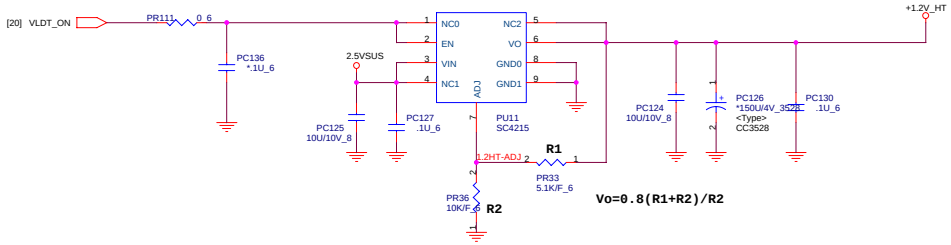

AO4916 Rds on = 27mOhm
ILOAD * Rds on * 10 = ILIM
ILIM5 = 1.485V Current limit 5.5A
ILIM3 = 1.35V Current limit 5A
MAX1999
PU4
SI9183-AD
PROJECT : ZL5
Quanta Computer Inc.
5V/3.3V(MAX1999)
Thursday, March 10, 2005

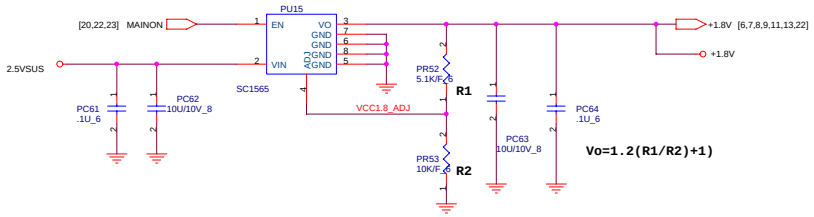


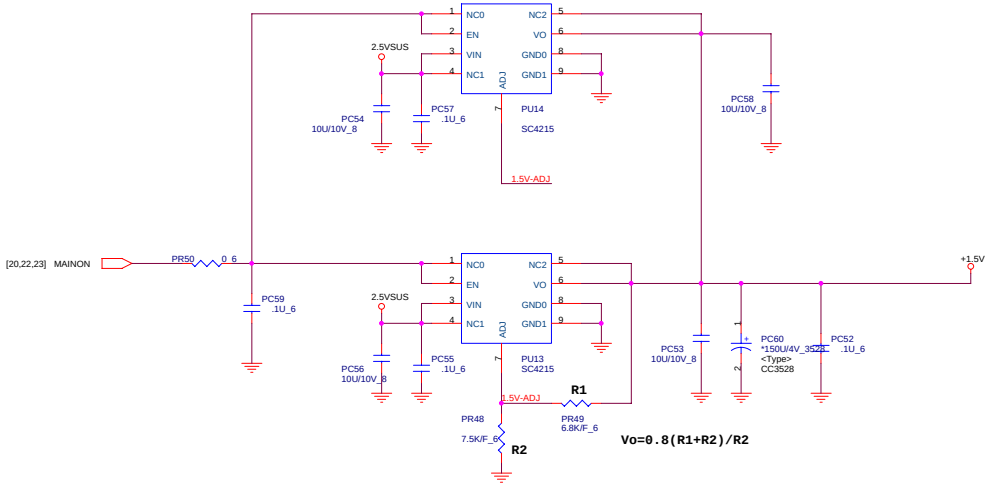


PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	2.5VSUS/+1.25TERM	3B
Date: Thursday, March 10, 2005	Sheet 23 of 26	



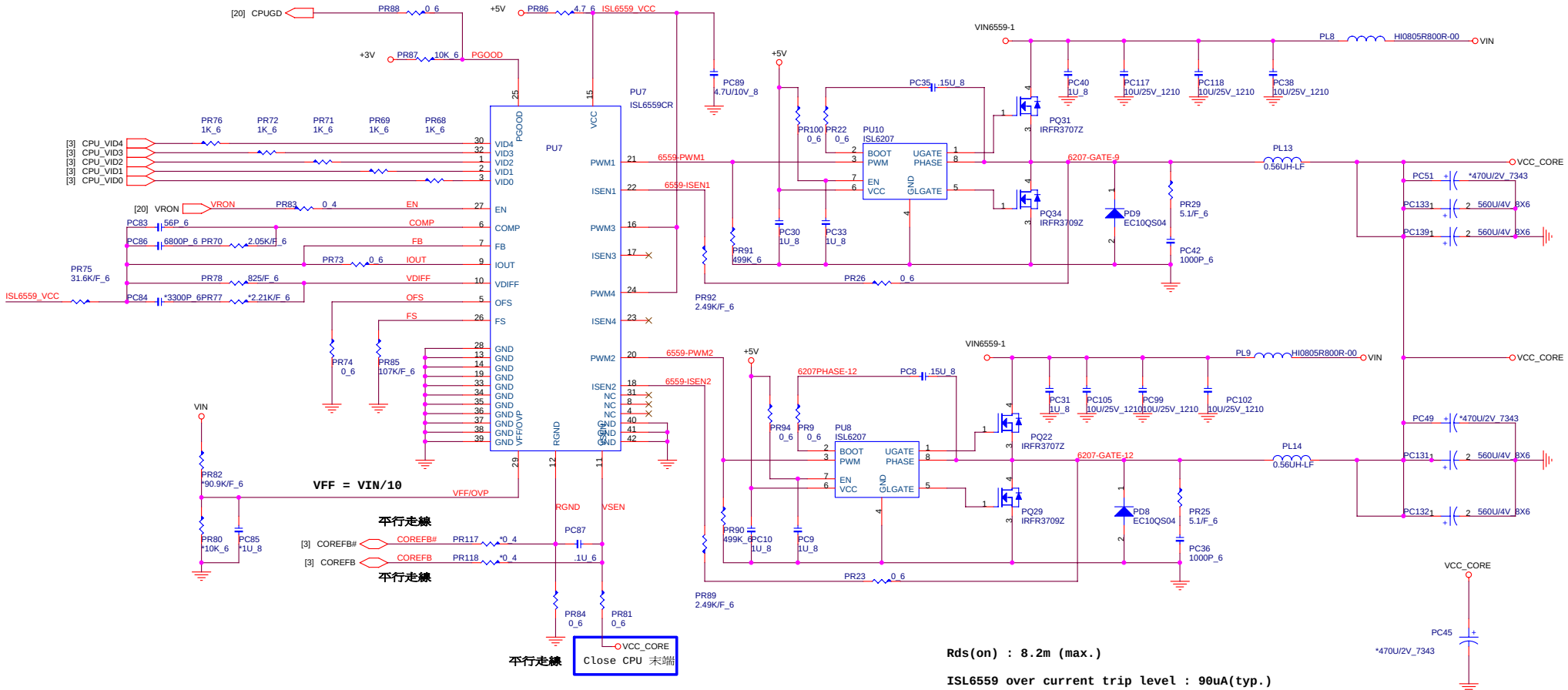




PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	+1.5V/+1.8V/+1.2V	3B
Date: Thursday, March 10, 2005	Sheet 24 of 25	

Vcore

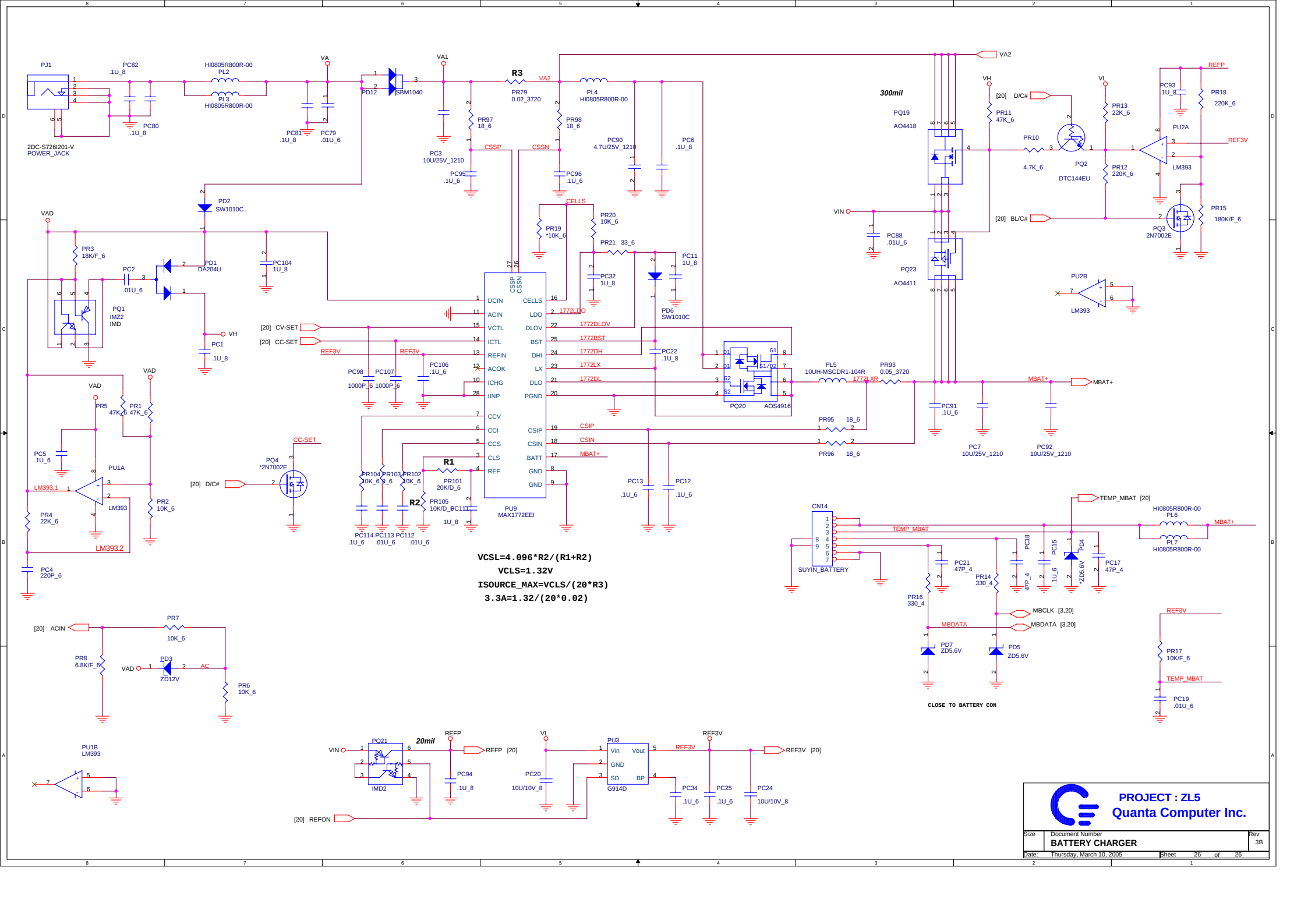


Rds(on) : 8.2m (max.)

ISL6559 over current trip level : 90uA(typ.)
Full load Isen current : 90uA/1.5 ~ 60uA
AMD LPM 35W current 28A

Rds(on) * Io(phase) = Rsen * Isen
8.2m*1.3*(28A/2) = Rsen*60uA
Rsen = 2.48K ~ 2.49K
OCP : 28A*1.5 = 42A

PROJECT : ZL5		
Quanta Computer Inc.		
Size	Document Number	Rev
	CPU CORE	3B
Date: Thursday, March 10, 2005	Sheet 25 of 26	



PROJECT : ZL5
Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY CHARGER	3B
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