JE40 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

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JE40 HR Block Diagram (Discrete/UMA/co-lay)

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1

##OnMainBoard

VRAM
2GB/1GB/512MB
88,89,90,91

DDR3
800MHz

Nvidia N12P
83.84,85,86,87

PCIe x 16
(Discrete only)

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 14
DDRIII Slot 1 1066/1333 15

Discreet/UMA/PX Co-lay

FDIx4x2
(UMA only)

DMIx4

HDMI 51
LCD 49
CRT 50

HDMI
LVDS(Dual Channel)
RGB CRT
Level shifter 57

Intel
PCH
Cougar Point

14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1

17,18,19,20,21,22,23,24,25,26

PCIE x 1
USB x 2
USB3.0
uPD720200
75

PCIE x 1
USB x 1
Mini-Card
802.11a/b/g
65

PCIE x 1
1000 NIC
BCM57780A1
31

RJ45 CONN 59

SD/MMC+/MS/
MS Pro/xD

PCIE x 1,USB x 1
Mini-Card
WWAN 66
SIM 66

USB 2.0 x 1
Right Side:
USB x 1

Left Side:
USB x 1
Bluetooth 63
CAMERA 49
64

USB2.0 x 4

AZALIA

Azalia
CODEC
ALC271X
29

Internal Analog MIC
HP1
MIC IN
2CH SPEAKER

SPI
Flash ROM
4MB 60

LPC Bus
LPC debug port 71

SATA x 2
HDD 56
ODD 56

KBC
NUVOTON
NPCE795P
27

SMBus
Touch PAD 69
Int. KB 69
Thermal
ENE P2800
ENE P2793 28
Fan 28

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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SSID = CPU

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

JE40 delete eDP function

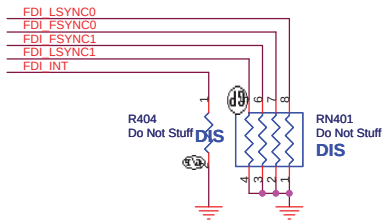
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.



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Title: CPU (PCIE/DMI/FDI)
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SSID = CPU

CPU1B
SANDY

2 OF 9

SANDY

MISC
- 18 H_SNB_IVB# → C26 SNB_IVB#
- JE40 modify AN34 SKTOCC#

THERMAL
- JE40 modify AL33 CATERR#
- 22,27 H_PECI AN33 PECI
- 27,42 H_PROCHOT# → R513 56R2J-4-GP → H_PROCHOT# R AL32 PROCHOT#
- 22,36 H_THERMTRIP# AN32 THERMTRIP#

PWR MANAGEMENT
- 19 H_PM_SYNC AM34 PM_SYNC
- R503 10KR2J-3-GP
- 22,36,97 H_CPUPWRGD AP33 UNCOREPWRGOOD
- 19,37 PM_DRAM_PWRGD → R505 DX Do Not Stuff V8 SM_DRAMPWROK
- 37 VDDPWRGOOD
- BUF_CPU_RST# AR33 RESET#

CLOCKS
- BCLK A28 CLK_EXP_P 20
- BCLK# A27 CLK_EXP_N 20
- DPLL_REF_SSCLK A16 CLK_DP_P_R
- DPLL_REF_SSCLK# A15 CLK_DP_N_R
- RN502 Do Not Stuff DIS
- JE40 modify 1D05V_VTT

DDR3 MISC
- SM_DRAMRST# R8 R502 4K99R2F-L-GP SM_DRAMRST# 37
- SM_RCOMP0 AK1 SM_RCOMP_0 R506 140R2F-GP
- SM_RCOMP1 A5 SM_RCOMP_1 R507 25D5R2F-GP
- SM_RCOMP2 A4 SM_RCOMP_2 R508 200R2F-L-GP

JTAG & BPM
- PRDY# AP29
- PREQ# AP27
- JE40 modify
- TCK AR26
- TMS AR27
- TRST# AP30 XDP_TRST#
- TDI AR28
- TDO AP26 XDP_TDO
- DBR# AL35 XDP_DBRESET#
- BPM#0 AT28
- BPM#1 AR29
- BPM#2 AR30
- BPM#3 AT30
- BPM#4 AP32
- BPM#5 AR31
- BPM#6 AT31
- BPM#7 AR32
- JE40 modify

1D05V_VTT
- R501 62R2J-GP
- H_PROCHOT#
- C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf

Connect EC to PROCHOT# through inverting OD buffer.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

1D05V_VTT
- RN501 SRN51J-GP
- XDP_TDO
- XDP_TRST#

3D3V_S0
- RN503 SRN1K5J-1-GP
- XDP_DBRESET#
- 18,27,31,36,65,66,71,82,97 PLT_RST# → BUF_CPU_RST#

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Title	**CPU (THERMAL/CLOCK/PM)**
Size: Custom	Document Number: **JE40-HR** Rev: **-1**
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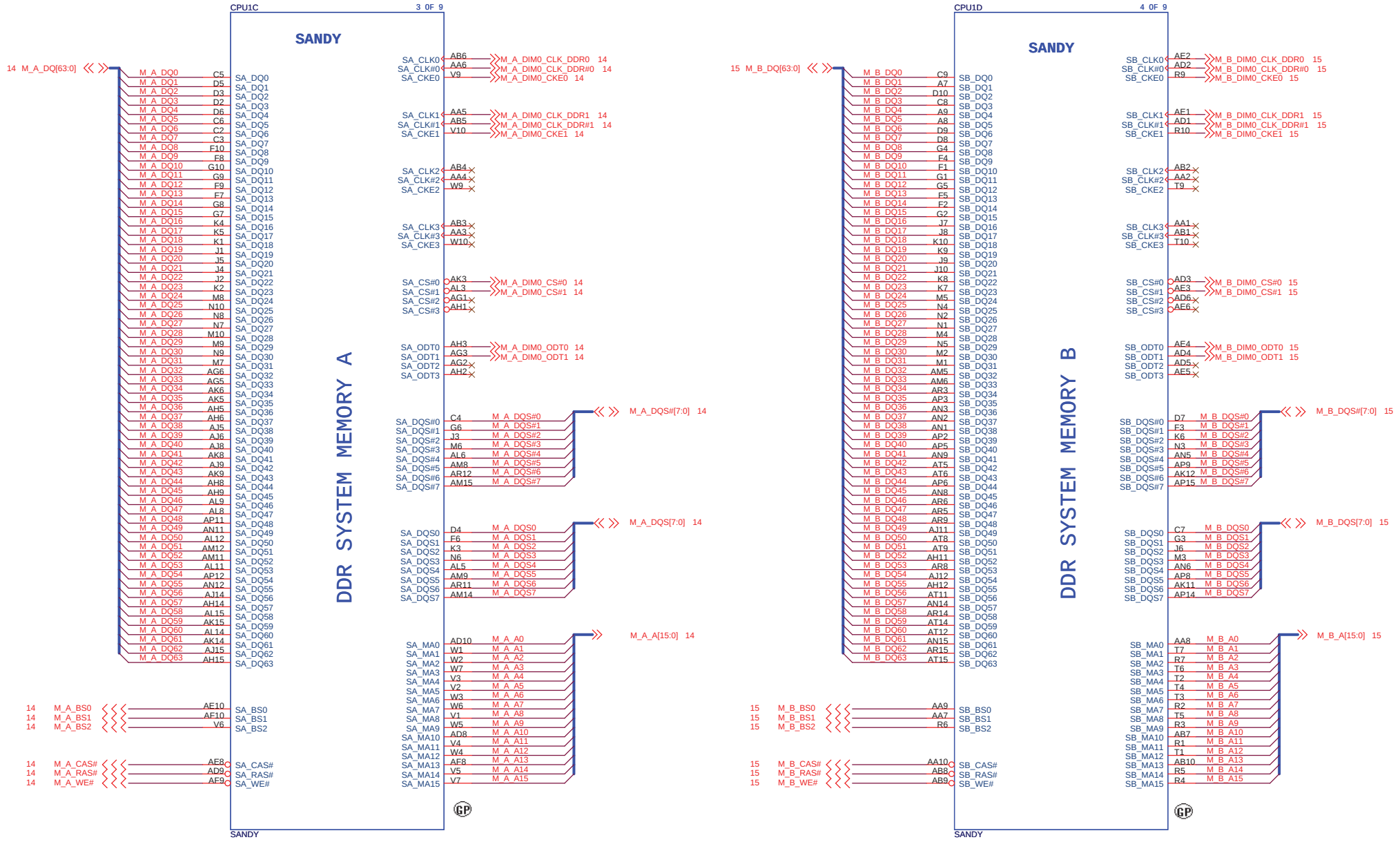
SSID = CPU



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Title: CPU (DDR)

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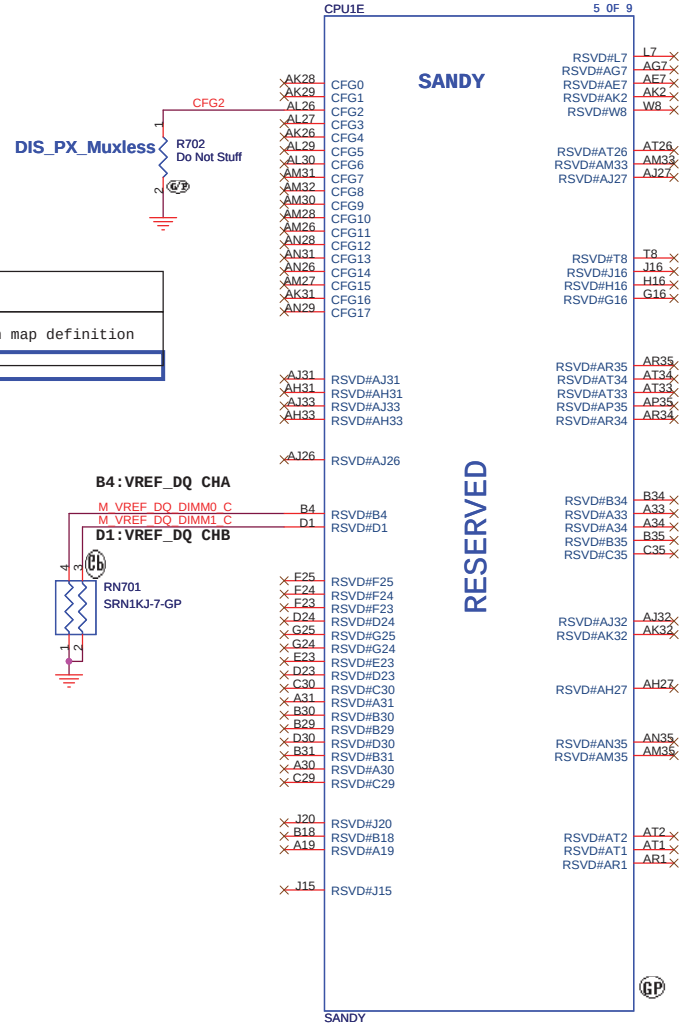
SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

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Title	***CPU (RESERVED)***
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SSID = CPU

POWER

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff
C802 Do Not Stuff
C803 Do Not Stuff
C804 Do Not Stuff
C811 Do Not Stuff
C820 Do Not Stuff
C819 Do Not Stuff
C818 Do Not Stuff
C817 Do Not Stuff
C815 Do Not Stuff
C816 SC10U6D3V5KX-1GP
C821 Do Not Stuff
C822 SC10U6D3V5KX-1GP
C823 SC10U6D3V5KX-1GP
C824 SC10U6D3V5KX-1GP
C825 SC10U6D3V5KX-1GP
C826 SC10U6D3V5KX-1GP
C827 SC10U6D3V5KX-1GP
C837 SC10U6D3V5KX-1GP
C836 SC10U6D3V5KX-1GP
C835 SC10U6D3V5KX-1GP
C834 SC10U6D3V5KX-1GP
C833 SC10U6D3V5KX-1GP
C832 Do Not Stuff
C831 Do Not Stuff
C828 SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

CPU1F

SANDY

6 OF 9

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VCC_CORE

VCC: AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

1D05V_VTT

VCCIO: AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 F14 F12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

C805 SC10U6D3V5KX-1GP
C806 SC10U6D3V5KX-1GP
C807 SC10U6D3V5KX-1GP
C809 SC10U6D3V5KX-1GP
C810 SC10U6D3V5KX-1GP
C838 SC10U6D3V5KX-1GP
C839 SC10U6D3V5KX-1GP
C840 SC10U6D3V5KX-1GP
C841 SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

C812 SC10U6D3V5KX-1GP
C813 SC10U6D3V5KX-1GP
C814 SC10U6D3V5KX-1GP
C829 SC10U6D3V5KX-1GP
C830 SC10U6D3V5KX-1GP
C842 Do Not Stuff
C843 Do Not Stuff
C844 SC10U6D3V5KX-1GP
C845 SC10U6D3V5KX-1GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 43R2J-GP VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT

H_CPU_SVIDDAT R804 130R2F-1-GP

VCC_CORE

R801,R802 close to CPU

R801 100R2F-L1-GP-U
R802 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE 42

VCCIO_SENSE B10 VCCIO_SENSE 45
VSSIO_SENSE A10 VSSIO_SENSE 45

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Title: CPU (VCC_CORE)

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — 7 OF 9 — SANDY

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff, C902 SC10U6D3V5KX-1GP, C903 SC10U6D3V5KX-1GP, C904 SC10U6D3V5KX-1GP, C905 SC10U6D3V5KX-1GP, C906 Do Not Stuff — DY — UMA_PX_Muxless

C907 Do Not Stuff, C908 SC10U6D3V5KX-1GP, C918 Do Not Stuff, C919 SC10U6D3V5KX-1GP, C920 SC10U6D3V5KX-1GP, C921 SC10U6D3V5KX-1GP — DY — UMA_PX_Muxless

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

VCC_GFXCORE

R903 Do Not Stuff — DIS, R904 Do Not Stuff — DIS, R905 Do Not Stuff — DIS, R901 Do Not Stuff — DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

SENSE LINES

VAXG_SENSE — AK35
VSSAXG_SENSE — AK34
→ VCC_AXG_SENSE 42
→ VSS_AXG_SENSE 42

VCC_GFXCORE
R906 100R2F-L1-GP-U — VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF — AL1 → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AE7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1

C909 Do Not Stuff — DY, C910 SC10U6D3V5KX-1GP, C911 SC10U6D3V5KX-1GP, C912 SC10U6D3V5KX-1GP, C913 SC10U6D3V5KX-1GP, C914 Do Not Stuff — DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

C916 Do Not Stuff — DY, C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
R902 10R2J-2-GP — **R902 need be close to pin H23.**
VCCSA_SENSE — H23 → VCCUSA_SENSE
TP901 Do Not Stuff

MISC

FC_C22 — C22
VCCSA_VID1 — C24
H_FC_C22 → VCCSA_SEL 48

RN901 SRN1KJ-7-GP

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6, A6, A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

SANDY

HR UMA

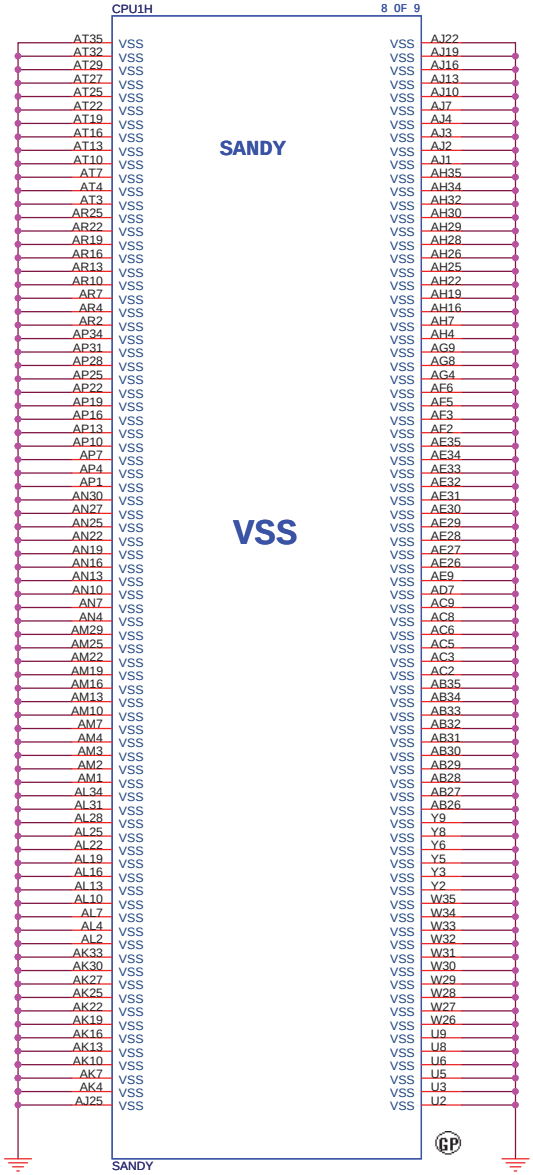
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

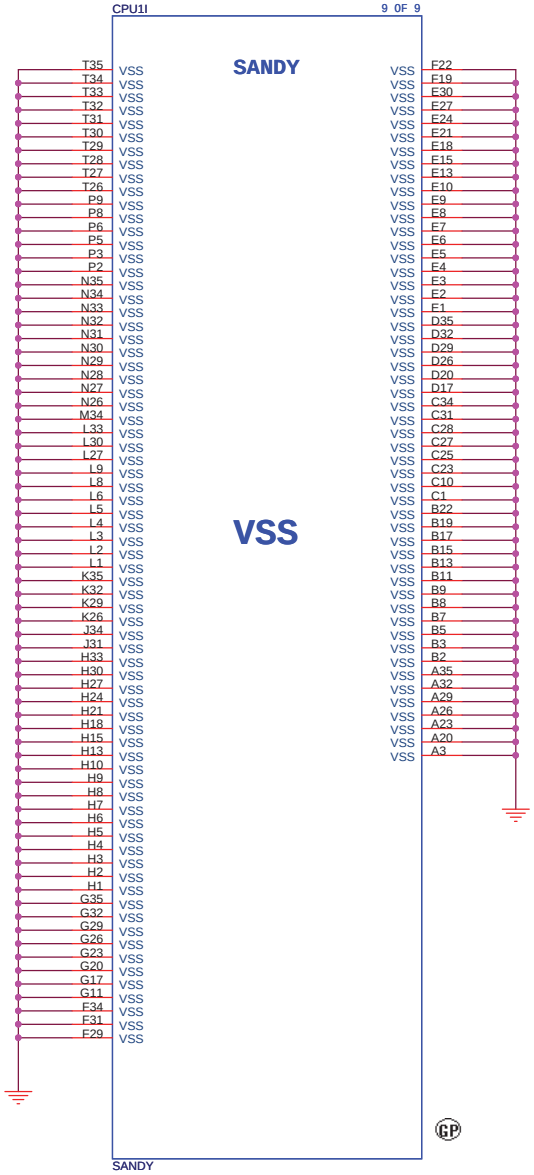
Title: **CPU (VCC_GFXCORE)**

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 — Sheet 9 of 102

SSID = CPU





HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (VSS)		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 10 of 102	

JE40 delete XDP function

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***XDP***

Size: A3 | Document Number: **JE40-HR** | Rev: **-1**

Date: Thursday, December 02, 2010 | Sheet 11 of 102

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 12 of 102

(Blanking)

HR UMA

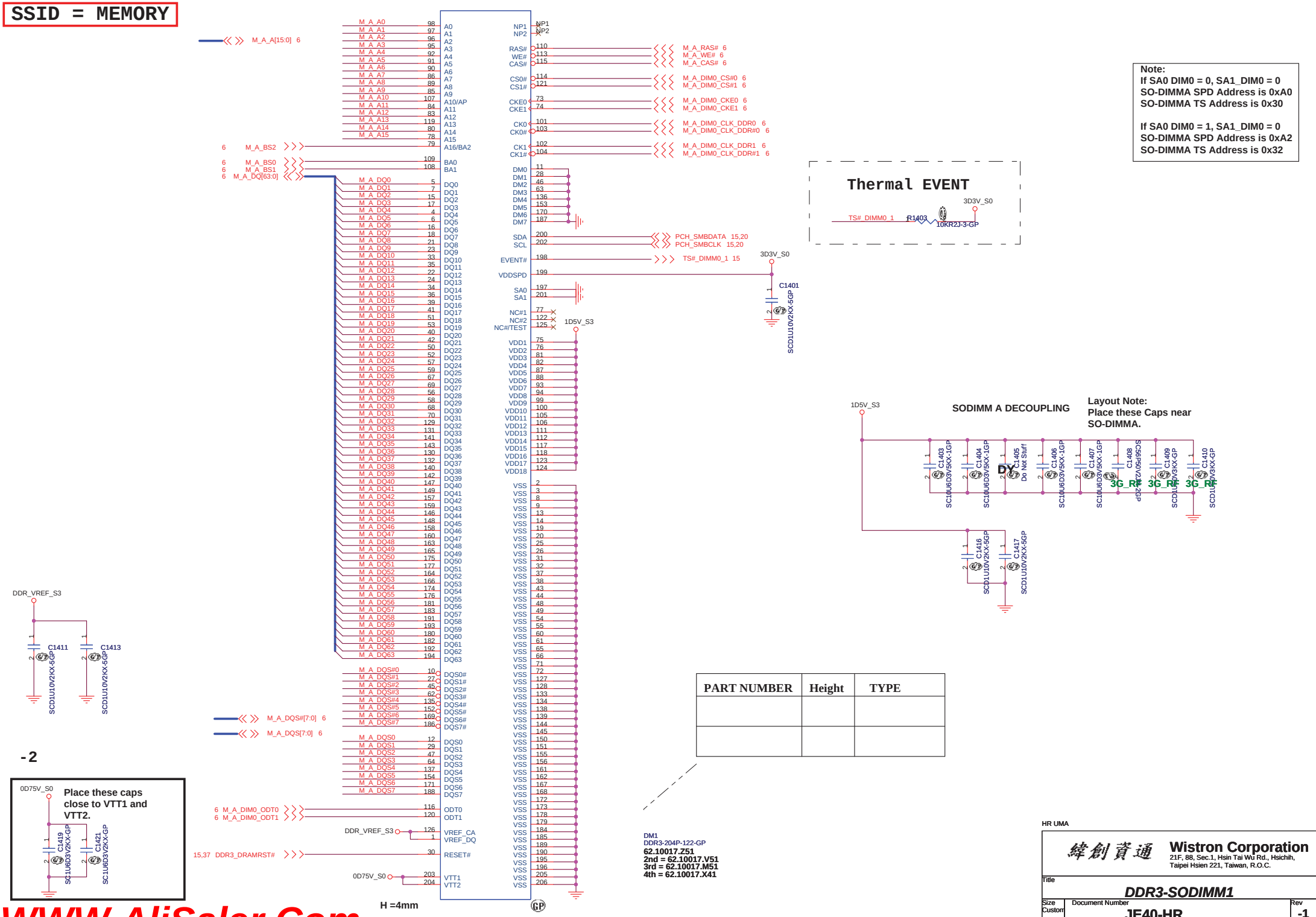
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 13 of 102

SSID = MEMORY



Thermal EVENT

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

SODIMM A DECOUPLING

Layout Note:
Place these Caps near SO-DIMMA.

PART NUMBER	Height	TYPE

DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41

Place these caps close to VTT1 and VTT2.

-2

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

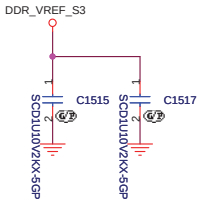
Size	Document Number	Rev
Custom	JE40-HR	-1

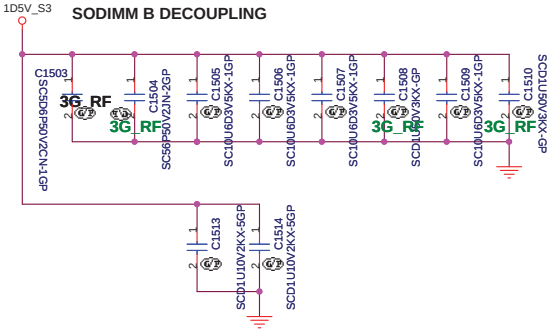
Date: Thursday, December 02, 2010 Sheet 14 of 102

SSID = MEMORY

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

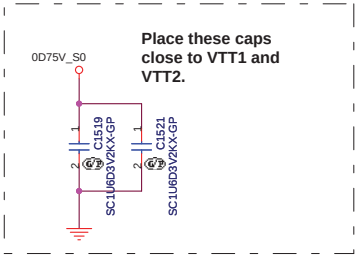
SO-DIMMB is placed farther from the Processor than SO-DIMMA





Layout Note:
Place these Caps near SO-DIMMB.

-2



H = 8mm

DM2
DDR3-204P-126-GP
62.10024.D41

2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 15 of 102

(Blanking)

HR UMA

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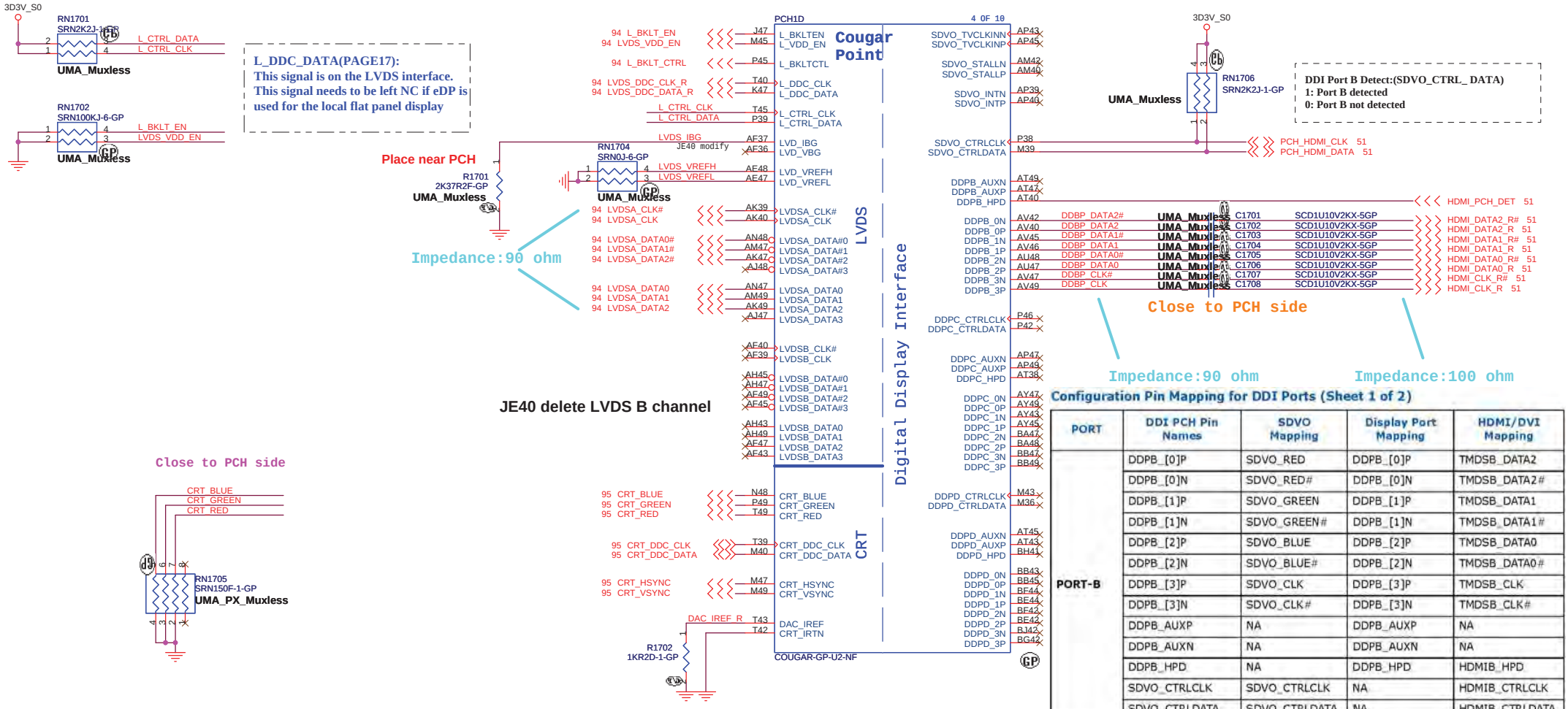
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 17 of 102

SSID = PCH

RN1801
SRN8K2J-2-GP-U

INT_PIRQH#	1	10	3D3V_S0
INT_PIRQB#	2	9	INT_PIRQD#
INT_PIRQF#	3	8	INT_PIRQE#
INT_PIRQA#	4	7	INT_PIRQC#
3D3V_S0	5	6	USB30_SMI#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

PCH1E — 5 OF 10

Cougar Point

RSVD: TP1–TP20 (BG26, BJ26, BH25, BJ16, BG16, AH38, AH37, AK43, AK45, C18, N30, H3, AH12, AM4, AM5, Y13, K24, L24, AB46, AB45)

NVRAM: RSVD (AY7, AV7, AU3, BG4, AT10, BC8, AU2, AT4, AT3, AT1, AY3, AT5, AV3, AV1, BB1, BA3, BB5, BB3, BB7, BE8, BD4, BF6, AV5, AY1, AV10, AT8, AY5, BA2, AT12, BF3)

RN1803
SRN10KJ-5-GP

DGPU_HOLD_RST# 2
DGPU_PWR_EN# 1

RSVD: TP21–TP40 (B21, M20, AY16, BG46, BE28, BC30, BE32, BJ32, BC28, BE30, BF32, BG32, AV26, BB26, AU28, AY30, AU26, AY26, AV28, AW30)

DMI & FDI Termination Voltage

NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

1D8V_S0
R1808 2K2R2J-2-GP
NV_CLE 1
R1809 1KR2J-1-GP
H_SNB_IVB# 5

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB: USBP0N/P … USBP13N/P

USBP0N/P	C24, A24	USB_PN0 66, USB_PP0 66
USBP1N/P	C25, B25	USB_PN1 61, USB_PP1 61
USBP2N/P	C26, A26	JE40 delete FP function
USBP3N/P	K28, H28	USB_PN3 63, USB_PP3 63
USBP4N/P	E28, D28	USB_PN4 66, USB_PP4 66
USBP5N/P	C28, A28	USB_PN5 32, USB_PP5 32
USBP6N/P	C29, B29	
USBP7N/P	N28, M28	
USBP8N/P	L30, K30	USB_PN8 82, USB_PP8 82
USBP9N/P	G30, E30	USB_PN9 61, USB_PP9 61
USBP10N/P	C30, A30	JE40 delete eDP function
USBP11N/P	L32, K32	USB_PN11 65, USB_PP11 65
USBP12N/P	G32, E32	USB_PN12 49, USB_PP12 49
USBP13N/P	C32, A32	JE40 delete New Card function

SB add USB port 5

JE40 co-lay USB2.0

USBRBIAS# C33 — USB_RBIAS — R1811 22D6R2F-L1-GP
USBRBIAS B33

PCI: PIRQA#/PIRQB#/PIRQC#/PIRQD# (K40, K38, H38, G38); REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54 (C46, C44, E40); GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55 (D47, E42, F46); PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5 (G42, G40, C42, D44); PME# (K10); PLTRST# (C6)

INT_PIRQA#, INT_PIRQB#, INT_PIRQC#, INT_PIRQD#

Do Not Stuff TP1806 — 83 DGPU_HOLD_RST# — DGPU_SELECT#
93 DGPU_PWR_EN#
Do Not Stuff TP1804 — DGPU_PWM_SELECT#

R1813 Do Not Stuff
56 SATA_ODD_DA#
82 USB30_SMI#
INT_PIRQE#, INT_PIRQF#, INT_PIRQH#

JE40 modify 07/16

5,27,31,36,65,66,71,82,97 PLT_RST#

71 CLK_PCI_LPC
20 CLK_PCI_FB
27 CLK_PCI_KBC
R1804, R1805, R1806 — 22R2J-2-GP
CLK_PCI_LPC_R, CLK_PCI_FB_R, CLK_PCI_KBC_R

CLKOUT_PCI0 (H49), CLKOUT_PCI1 (H43), CLKOUT_PCI2 (J48), CLKOUT_PCI3 (K42), CLKOUT_PCI4 (H40)

EC1803 DY Do Not Stuff
EC1802 DY Do Not Stuff
EC1801 DY Do Not Stuff

KBC CLK EMI

OC0#/GPIO59, OC1#/GPIO40, OC2#/GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO9, OC6#/GPIO10, OC7#/GPIO14 (A14, K20, B17, C16, L16, A16, D14, C14)

3D3V_S5
R1820 10KR2J-3-GP

COUGAR-GP-U2-NF

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

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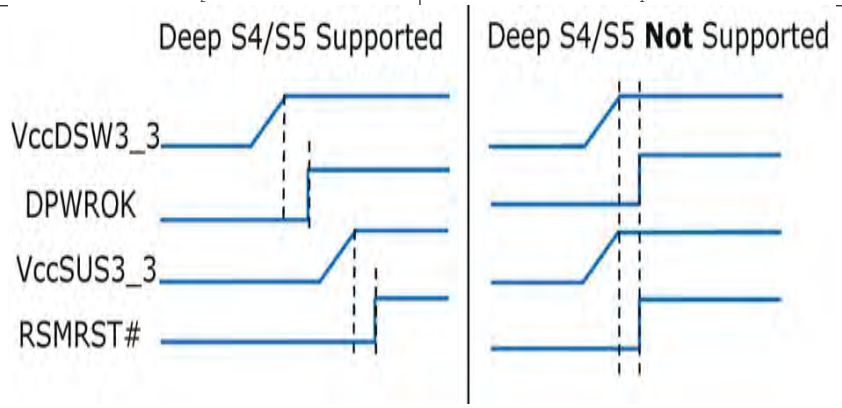
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 18 of 102

SSID = PCH



Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — Cougar Point — 3 OF 10

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

COUGAR-GP-U2-NF

1D05V_VTT
R1901 49D9R2F-GP DMI_COMP_R → DMI_ZCOMP
R1902 750R2F-GP RBIAS_CPY → DMI2RBIAS

R1926 Do Not Stuff DY — SYS_PWROK
R1904 100KR2J-1-GP — PWROK
0628 Modify: Change R1904 to 100K 0402 from 10K and default stuff.

JE40 modify SUS_PWR_ACK → SUSACK#
3D3V_S0 — R1905 10KR2J-3-GP — SYS_RESET#
36 SYS_PWROK → SYS_PWROK
27,42 S0_PWR_GOOD — R1924 Do Not Stuff JE40 modify — PWROK
PWROK, APWROK

5,37 PM_DRAM_PWRGD → DRAMPWROK
PM_RSMRST# → RSMRST#
27 SUS_PWR_ACK → SUSWARN#/SUSPWRDNACK/GPIO30
27,97 PM_PWRBTN# → PWRBTN#
27 AC_PRESENT → ACPRESENT/GPIO31
BATLOW# → BATLOW#/GPIO72
PM_RI# → RI#

DSWODVREN → A18
DPWROK → E22 PCH_DPWROK — R1910 Do Not Stuff DY — R1911 Do Not Stuff — PM_RSMRST# — RTC_AUX_S5
WAKE# → B9 PCIE_WAKE# 31,65,66,82
CLKRUN#/GPIO32 → N3 PM_CLKRUN# 27
SUSCLK/GPIO62 → N14 PCH_SUSCLK_KBC 27
SLP_S4# → H4 PM_SLP_S4# 27,46
SLP_S3# → F4 PM_SLP_S3# 27,36,37,47,92
PMSYNCH → AP14 H_PM_SYNC 5

FDI_INT → AW16 FDI_INT 4
FDI_FSYNC0 → AV12 FDI_FSYNC0 4
FDI_FSYNC1 → BC10 FDI_FSYNC1 4
FDI_LSYNC0 → AV14 FDI_LSYNC0 4
FDI_LSYNC1 → BB10 FDI_LSYNC1 4

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

JE40 modify 07/16

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

RTC_AUX_S5 — R1917 330KR2J-L1-GP — DSWODVREN — R1918 DY Do Not Stuff

R1919 8K2R2J-3-GP — 3D3V_S0 — PM_CLKRUN#

3D3V_S5 — RN1901 SRN10KJ-6-GP: BATLOW#, PM_RI#, AC_PRESENT, SUS_PWR_ACK
R1921 10KR2J-3-GP — PCIE_WAKE#

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor

R1908 100KR2J-1-GP — PM_RSMRST#

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

3D3V_AUX_S5 — R1909 100KR2J-1-GP
R1916 10KR2J-3-GP — 3V_5V_POK_#
Q1901 2N7002KDW-GP
R1912 1KR2J-1-GP — PM_RSMRST# — RSMRST#_KBC 27
3V_5V_POK 41

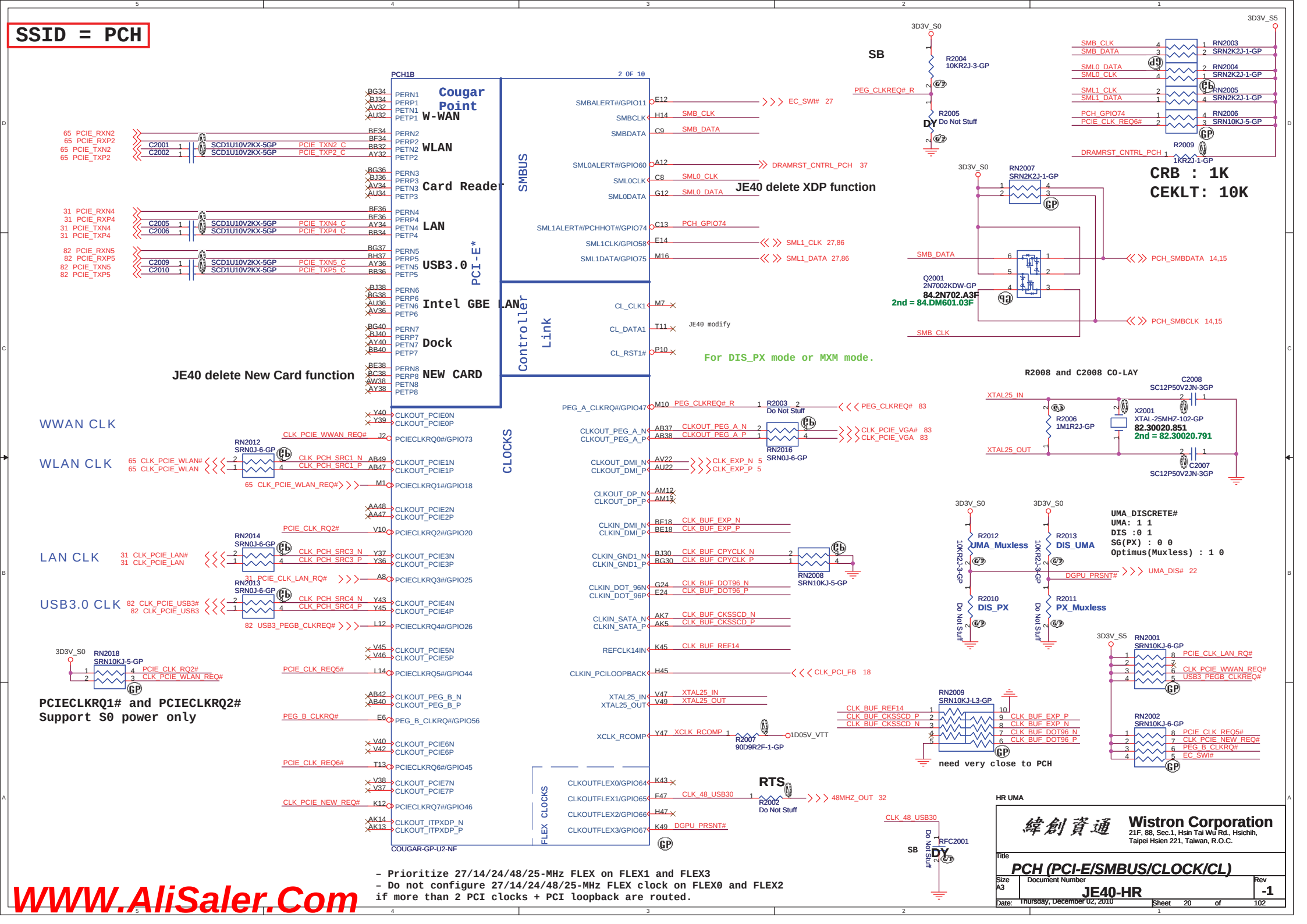
84.2N702.A3F
2nd = 84.DM601.03F

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**
Size: A3 | Document Number: **JE40-HR** | Rev: **-1**
Date: Thursday, December 02, 2010 | Sheet 19 of 102

SSID = PCH



- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

SSID = PCH

RTC_X1
RTC_X2
R2101 1 10MR2J-L-GP
X2101
X-32D768KHZ-34GPU
82.30001.661
2nd = 82.30001.B21
C2101 SC5P50V2CN-2GP
C2102 SC5P50V2CN-2GP

SB SEIKO suggest modify to 5P
EPSON suggest modifyg to 6P

RTC_AUX_S5
RN2104 SRN20KJ-GP-U
C2103 SC1U6D3V2KX-GP
C2104 SC1U6D3V2KX-GP
G2101 Do Not Stuff

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

RTC Reset

RTC_AUX_S5 — R2105 330KR2F-L-GP — INTVRMEN
1M1R2J-GP R2104

-1M
R2122 33R2J-2-GP DY
R2123 33R2J-2-GP
29 HDA_CODEC_SYNC
29 HDA_CODEC_SDOUT
HDA_SYNC
HDA_SDOUT
29 HDA_CODEC_RST#
29 HDA_CODEC_BITCLK
HDA_RST#
HDA_BITCLK
RN2102 SRN33J-5-GP-U

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+3VS_+1.5VS_HDA_IO
DY R2102 Do Not Stuff
HDA_SDOUT

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

+3VS_+1.5VS_HDA_IO
R2103 1KR2J-1-GP
HDA_SYNC

**This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310**

5V_S0 -1M Q2101 Do Not Stuff
HDA_SYNC_R
-1M R2124 Do Not Stuff
HDA_SYNC
HDA_CODEC_SYNC
Do Not Stuff
2ND = 84.2N702.031

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

PCH1A — 1 OF 10 — Cougar Point — COUGAR-GP-U2-NF

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3

RTC_X1 RTC_X2 RTC_RST# SRTC_RST# SM_INTRUDER# PCH_INTVRMEN
HDA_BITCLK HDA_SYNC SPKR HDA_RST# HDA_SDIN0
27 ME_UNLOCK — R2107 1KR2J-1-GP — HDA_SDOUT
?????
R2121 4K7R2J-2-GP PCH_JTAG_TCK_BUF
JE40 modify
R2108 33R2J-2-GP PCH_SPI_CLK
R2109 33R2J-2-GP PCH_SPI_CS0#
R2110 33R2J-2-GP PCH_SPI_SI
27,60 SPI_CLK_R
27,60 SPI_CS0#_R
27,60 SPI_SI_R
27,60 SPI_SO_R

LPC: FWH0/LAD0 C38 LPC_AD0, FWH1/LAD1 A38 LPC_AD1, FWH2/LAD2 B37 LPC_AD2, FWH3/LAD3 C37 LPC_AD3, FWH4/LFRAME# D36 LPC_FRAME# 27,71, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5 INT_SERIRQ 27
LPC_AD[0..3] 27,71

SATA 6G: SATA0RXN AM3 SATA_RXN0 56, SATA0RXP AM1 SATA_RXP0 56, SATA0TXN AP7 SATA_TXN0 56, SATA0TXP AP5 SATA_TXP0 56 — HDD1
SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10 — HDD2
SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4
SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1
SATA4RXN Y7 SATA_RXN4 56, SATA4RXP Y5 SATA_RXP4 56, SATA4TXN AD3 SATA_TXN4 56, SATA4TXP AD1 SATA_TXP4 56 — ODD
SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1 — ESATA
SATAICOMPO Y11, SATAICOMPI Y10 SATA_COMP R2112 1 37D4R2F-GP 1D05V_VTT
SATA3RCOMPO AB12, SATA3COMPI AB13 SATA3_COMP R2113 1 49D9R2F-GP 1D05V_VTT
SATA3RBIAS AH1 RBIAS_SATA3 R2114 1 750R2F-GP
SATALED# P3 SATA_LED# 68
SATA0GP/GPIO21 V14 SATA_DET#0
SATA1GP/GPIO19 P1

22 PSW_CLR#
RN2103 SRN10KJ-6-GP 3D3V_S0
SATA_LED#
INT_SERIRQ
SATA_DET#0

HDA_CODEC_BITCLK — EC2102 DY Do Not Stuff
HDA_CODEC_SDOUT — EC2103 DY Do Not Stuff
SPI_CS0#_R — EC2101 DY Do Not Stuff

HR UMA

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Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Pass Word Clear

JE40 delete G Sensor

SB add Zero ODD function

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

SB VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

VRAM Size

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

HR UMA	
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Title	PCH (GPIO/CPU)
Size A3	Document Number JE40-HR Rev -1
Date: Thursday, December 02, 2010	Sheet 22 of 102

SSID = PCH 6A

POWER

PCH1G — Cougar Point — 7 OF 10

VCC CORE

1D05V_VTT — 1.3A

(1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP; C2302 SC1U6D3V2KX-GP; C2303 SC1U6D3V2KX-GP; C2304 SC1U6D3V2KX-GP

AA23 AC23 AD21 AD23 AE21 AE23 AG21 AG23 AG24 AG26 AG27 AG29 AJ23 AJ26 AJ27 AJ29 AJ31 — VCCCORE

CRT

VCCADAC — U48 +VCCA_DAC_1_2

VSSADAC — U47

(0.1uF/0.01uF x1) (10uF x1_0603)

C2313 SCD01U16V2KX-3GP; C2314 SCD01U16V2KX-5GP; C2315 Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

R2301 Do Not Stuff — 3D3V_S0

R2315 Do Not Stuff — 3D3V_DAC_S0

R2304 0R3J-0-U-GP — 3D3V_S0

0.001A

UMA_PX_Muxless

LVDS

VCCALVDS — AK36 +3VS_VCCA_LVDS

VSSALVDS — AK37

R2303 Do Not Stuff

VCCTX_LVDS — AM37 AM38 AP36 AP37

0.06A

R2309 Do Not Stuff

C2316 SCD01U16V2KX-3GP; C2317 SCD01U16V2KX-3GP; C2318 Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

+1.8VS_VCCTX_LVDS

R2305 0R5J-5-GP — 1D8V_S0

UMA_PX_Muxless

(0.01uF x2) (22uF x1)

HVCMOS

VCC3_3 — V33 V34

3D3V_S0

C2319 SCD01U10V2KX-5GP

-2 modify power net name

DMI

VCCVRM — AT16 — VCCVRM_S0

VCCDMI — AT20 — JE40 modify — 1D05V_VTT — (1uF x1)

C2320 SC1U6D3V2KX-GP

VCCCLKDMI — AB36

0.02A

+1.05VS_VCC_DMI_CCI

L2303 IND-10UH-218-GP — 1D05V_VTT

68.10050.10Y

2nd = 68.10090.10B

(1uFx1) (10uFx1)

C2321 SC1U6D3V2KX-GP; C2325 Do Not Stuff

NAND / SPI

VccDFTERM — AG16 AG17 AJ16 AJ17

1D8V_S0

0.19A

JE40 modify

C2326 SCD1U10V2KX-5GP; C2322 SCD1U10V2KX-5GP

VCCSPI — V1

0.02A

3D3V_S5

(1uFx1)

C2323 SC1U6D3V2KX-GP

FDI

VCCIO — AN19 — 1D05V_VTT

JE40 modify 07/16

VCCAPLLEXP — BJ22 — JE40 modify — 1D05V_VTT

2.925A(Total current of VCCIO)

(1uF x4)

C2306 Do Not Stuff; C2307 SC1U6D3V2KX-GP; C2308 SC1U6D3V2KX-GP; C2309 SC1U6D3V2KX-GP

AN16 AN17 AN21 AN26 AN27 AP21 AP23 AP24 AP26 AT24 AN33 AN34 — VCCIO

0.266A (Totally VCC3_3 current)

(0.1uF x1)

3D3V_S0 — BH29 — VCC3_3

C2310 SCD1U10V2KX-5GP

0.159A(Totally current of VCCVRM)

-2 modify power net name

VCCVRM_S0 — AP16 — VCCVRM

0806 check VCCAFDIPLL — BG6 — VCCAFDIPLL

1D05V_VTT — AP17 — VCCIO

0.042A (Totally current of VCCDMI)

1D05V_VTT — AU20 — VCCDMI — JE40 modify

COUGAR-GP-U2-NF

U2301 for ANNIE flicker issue

R2312 for don't flicker solution

3.3V CRT LDO

U2301 G9091-330T11U-GP

74.09091.J3F

2nd = 74.09198.G7F

5V_S0 — VIN GND EN — VOUT NC#4 — 3D3V_DAC_S0

C2311 SC1U6D3V2KX-1GP — UMA_PX_Muxless

C2312 SC1U6D3V2KX-GP; C2327 SC1U6D3V3MX-GP — UMA_PX_Muxless

SB add C2327

-1M add LDO for VCCVRM_S0

3D3V_S0 — 1D5V_S0 — VCCVRM_S0

U2302 G913CF-GP

74.00913.A3F

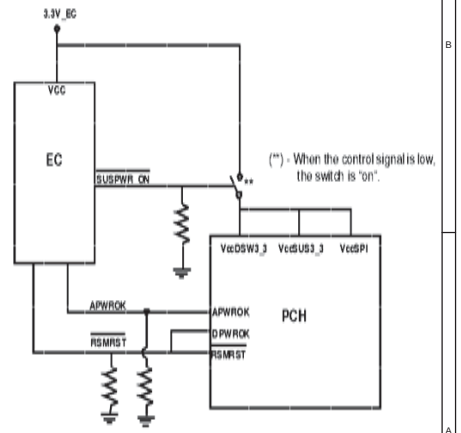
SHDN# GND IN — SET OUT

C2328 SC1U10V3KX-3GP DY; C2329 SC4D7U6D3V3KX-GP DY; C2330 SC22P50V2JN-4GP DY; C2331 SCD1U10V2KX-5GP DY

R2316 2K8R2F-GP DY; R2317 10KR2J-3-GP DY

Vout=1.25*(1+R1/R2)

Refer to NPCE795 shared SPI flash architecture



SB 公板suggest delete 3D3V_S0, R2313

SPI only support 3D3V_S5

The same BIOS SPI ROM power

HR UMA

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Title: PCH (POWER1)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 23 of 102

JE40 modify 07/16

SSID = PCH

POWER

PCH1J — 10 OF 10

Cougar Point

USB | Clock and Miscellaneous | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

COUGAR-GP-U2-NF

0.002A

0.097A (Totally current of VCCSUS3_3)

0.001A

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM

0.08A

0.08A

0.055A

0.095A

0.001A

6uA

0.01A

-1M

-1M modify power net name

JE40 modify 07/16

JE40 modify 07/16

JE40 modify 07/16

JE40 modify 07/16

JE40 modify 07/16

HR UMA

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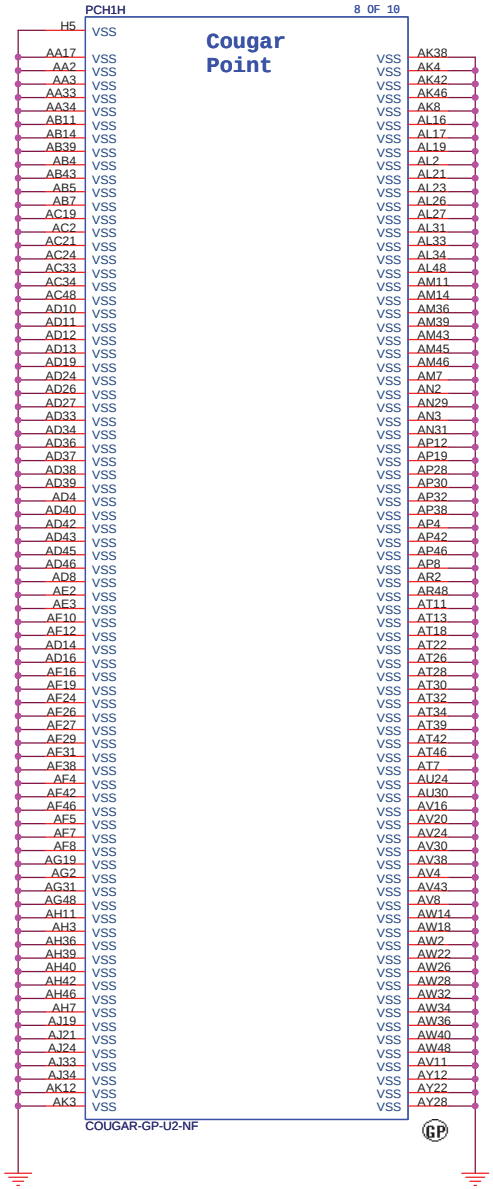
Taipei Hsien 221, Taiwan, R.O.C.

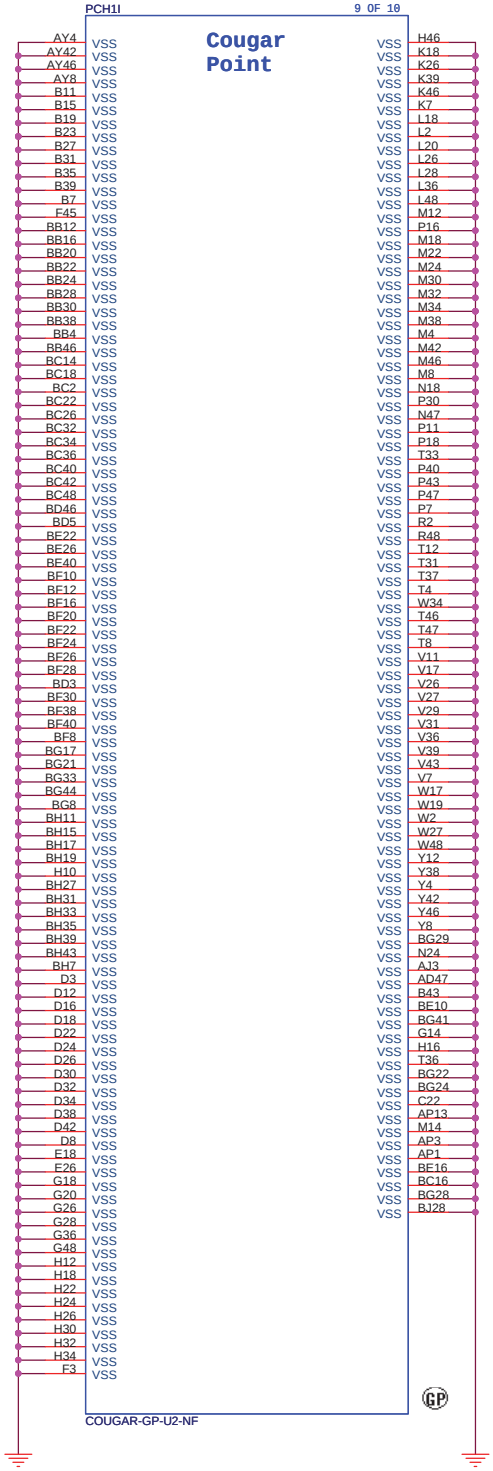
Title: PCH (POWER2)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 24 of 102

SSID = PCH





HR UMA

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Title: ***PCH (VSS)***

Size	Document Number	Rev
A3	**JE40-HR**	-1

Date: Thursday, December 02, 2010 Sheet 25 of 102

HR UMA

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Title: ***Clock(colay)***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 26 of 102

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
-1	100.0K	47.0K	2.24V
-1M	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

PSL SOLUTION
(Power Switch Control Logic)

NO PSL SOLUTION

SB modify R2756 stuff, R2760 change DY

SB to -1 default active Low

JE40 delete USB Charger function

JE40 VGA_THRM

0628 Modify:
Move R2771 to closed 3D3V_AUX_KBC power rail base on layout placement.

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

NOTE:
Locate resistors R2719 and R2722 close to the NPCE791L.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

<------ TP

<------ BATTERY / CHARGER

<------PCH / EDP

SB to -1

JE40 delete AMP function

C2716 need very close to EC

EC GPIO standard PH/PL

如果移除PLS function 要改成pull high 3D3V_AUX_S5

0604 Modify:
RN2704 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

SB LID_CLOSE# can not pull high, because push pull suggest RN2708 Pin5 change FAN_TACH1

0604 Modify:
Add Pull down 100k ohm at F_SDI for Power consumption concern.

Prevent BIOS data loss

SB to -1

EC_GPIO47 High Active

ADT_TYPE A/D(PIN99)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K	100.0K	0.55V
120W	33.0K	100.0K	0.82V
Reserved	47.0K	100.0K	1.06V
Reserved	64.9K	100.0K	1.3V

JE40 modify

65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete

SB EC_AGND , change GND

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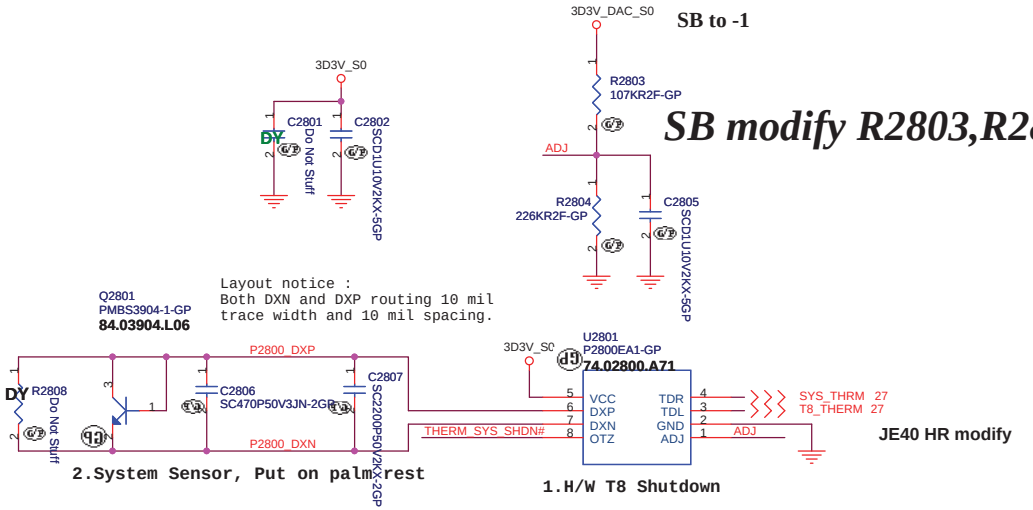
Title	KBC Nuvoton NPCE795
Size: Custom	Document Number: JE40-HR
Rev	-1
Date: Thursday, December 02, 2010	Sheet 27 of 102

SSID = Thermal

Thermal sensor P2800



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

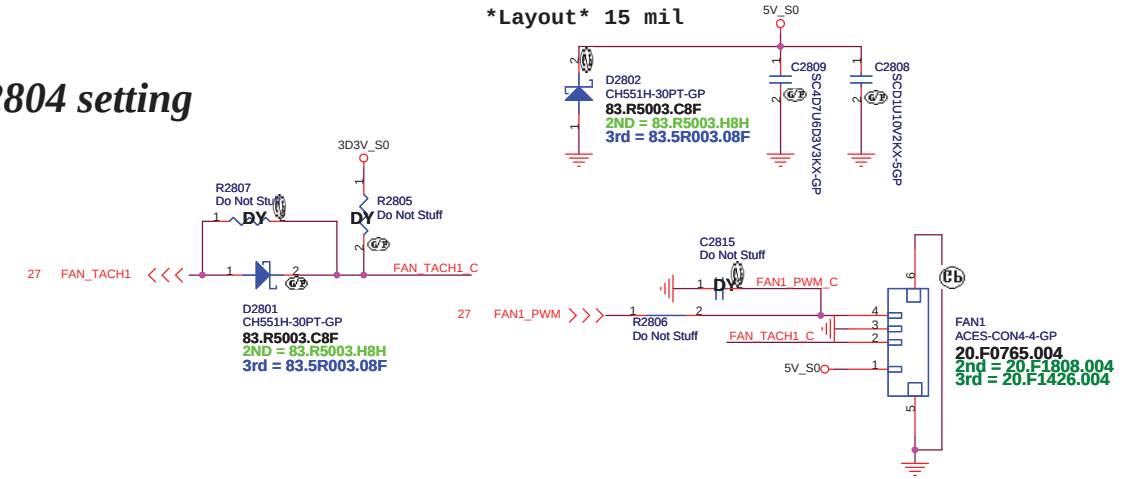
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

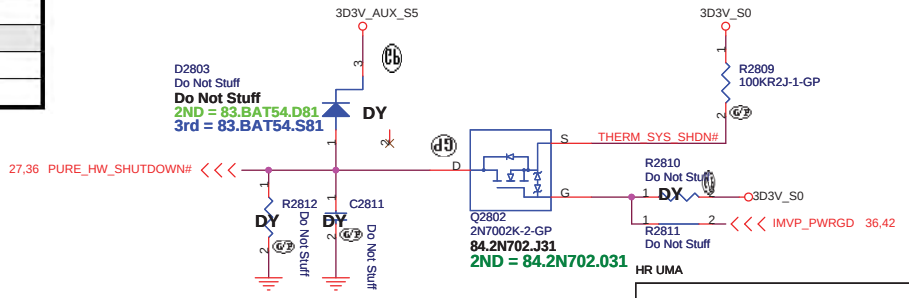
VGA Thermal sensor P2800

SMBUS modify to Page 84

Fan controller P2793

Layout 15 mil





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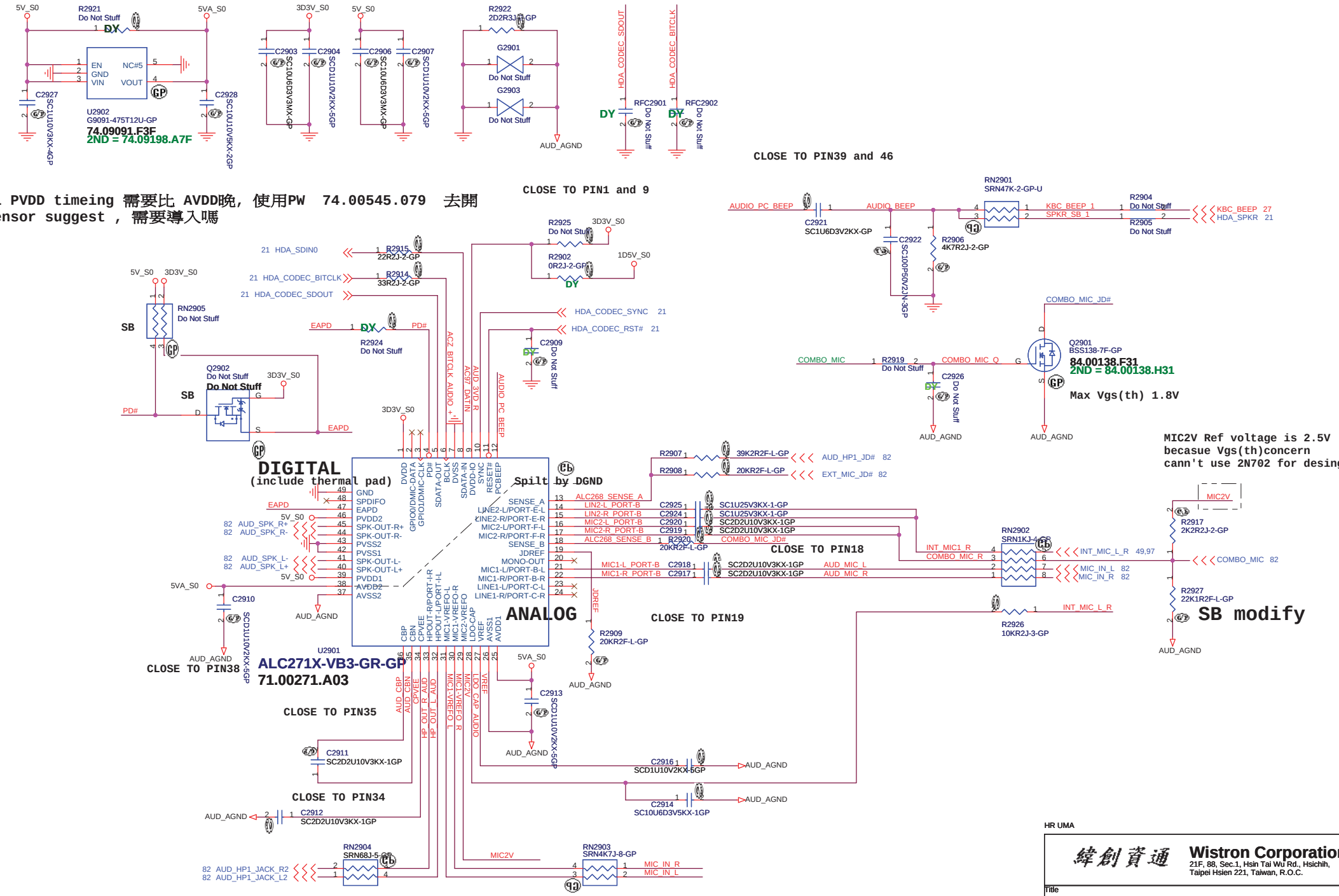
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 28 of 102


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
U2902
G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
CLOSE TO PIN18
CLOSE TO PIN19
CLOSE TO PIN35
CLOSE TO PIN34
CLOSE TO PIN38
SB modify
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
Max Vgs(th) 1.8V
84.00138.F31
2ND = 84.00138.H31
HR UMA
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
JE40-HR
-1
Thursday, December 02, 2010
Sheet 29 of 102

AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

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Title: *Audio AMP*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 30 of 102	

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

SB mmodify vendor suggest

SB delete EEPROM

128K byte

SB delete R3112

SB delete R3117

SB delete R3129 for LDO power

Card-reader Off-Page

Check VDDO_CR power plan

SB for B version

SB for B version can no use LDO delete LDO

SB to -1 modify to short pad

SB C3134, C3135 change 15P

68.00248.011

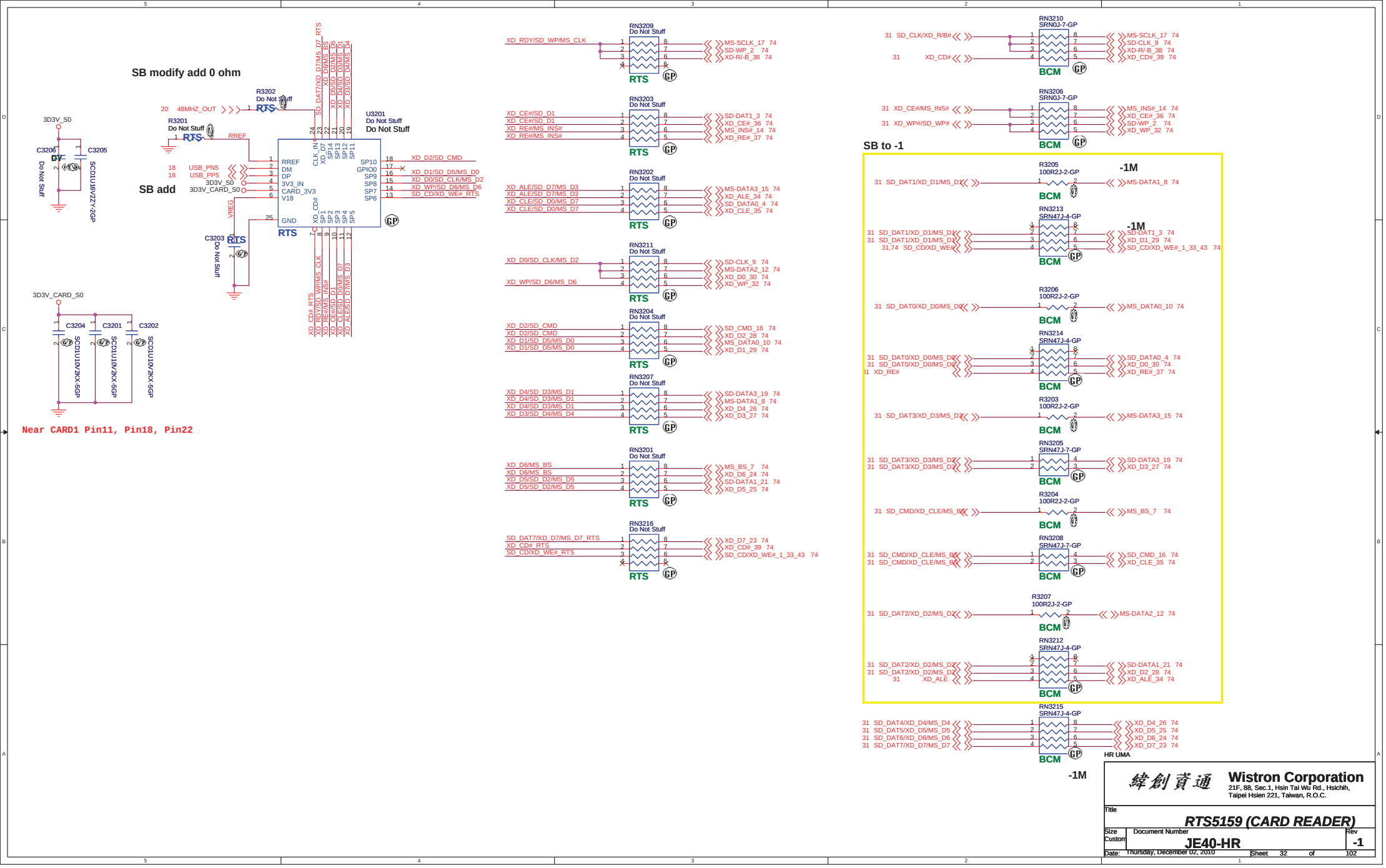
2nd = 68.00217.241

71.57785.M02

Change:71.57785.M03

10月底改打71.57785.M03

HR UMA	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BCM57780
Size: Custom	Document Number: JE40-HR
Rev	-1
Date: Thursday, December 02, 2010	Sheet 31 of 102



(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 33 of 102

(Blanking)

HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 34 of 102	

HR UMA

緯創資通 **Wistron Corporation**
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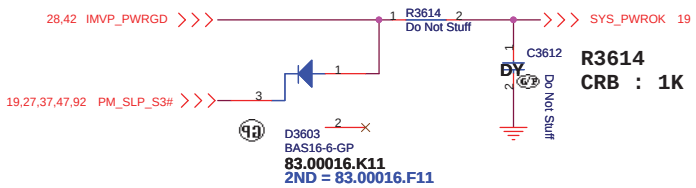
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

Size	Document Number	Rev
A3	**JE40-HR**	**-1**

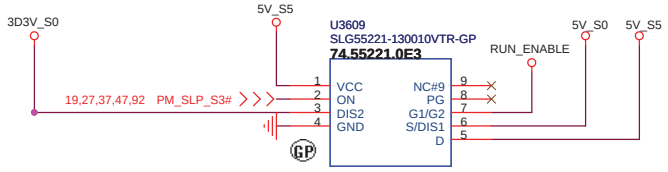
Date: Thursday, December 02, 2010 Sheet 35 of 102

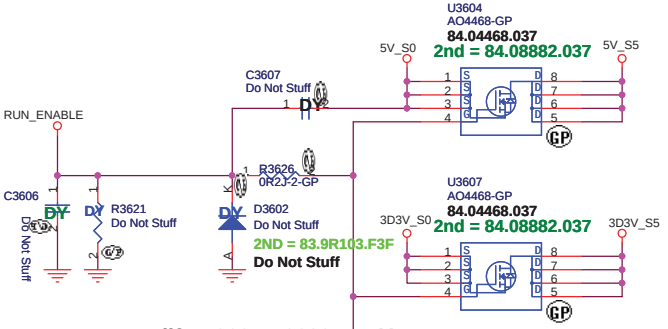
Power Sequence



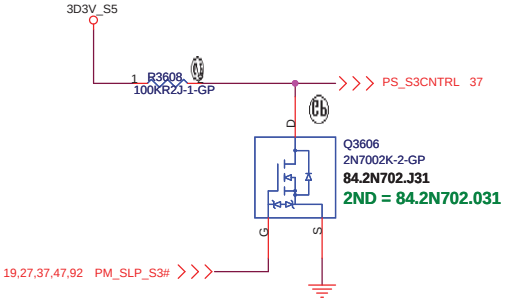
R3614
CRB : 1K

ANNIE Run Power



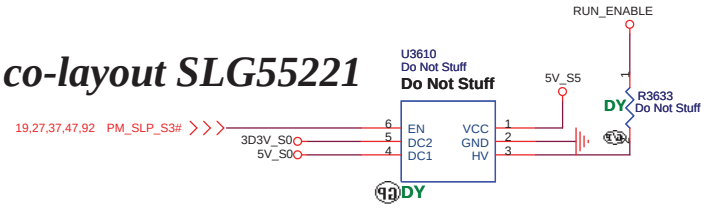


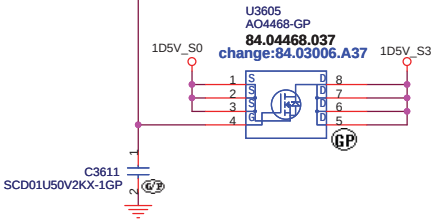
-1 modify R3621,D3602 to DY



SB modify part number

-1 co-layout SLG55221

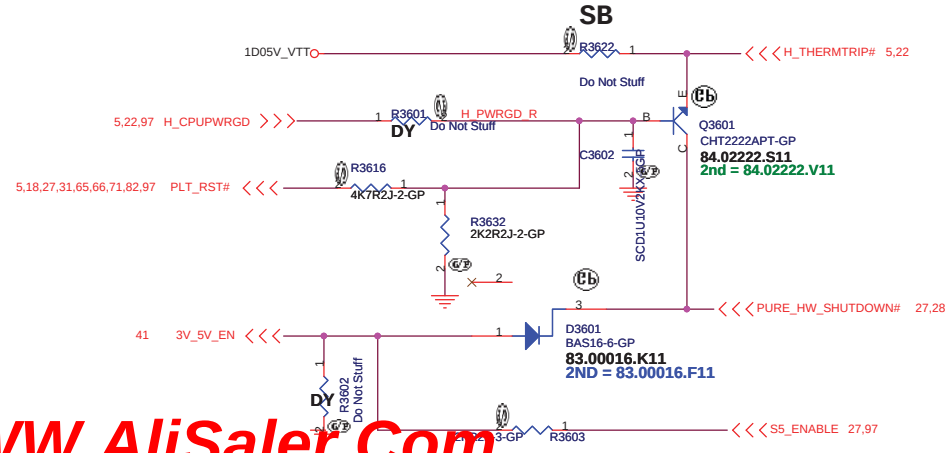




1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

SB



HR UMA

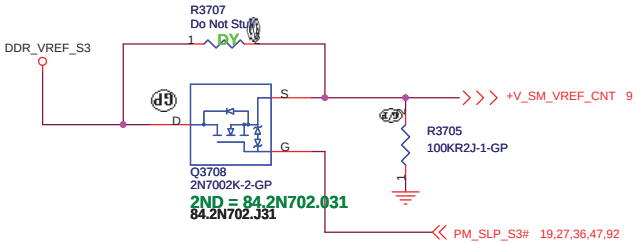
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

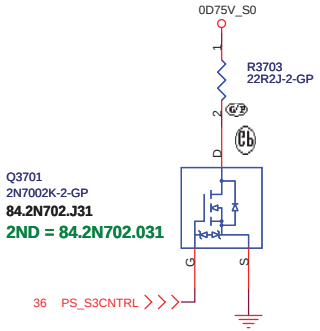
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 36 of 102

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

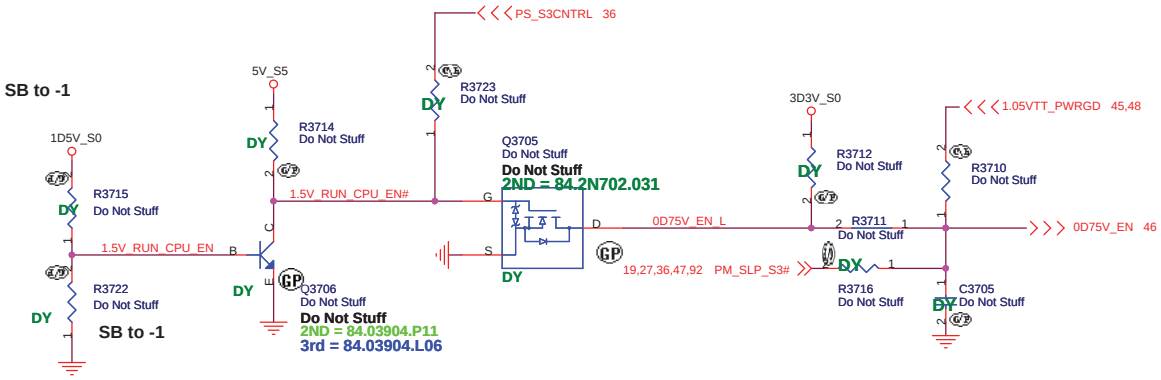


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

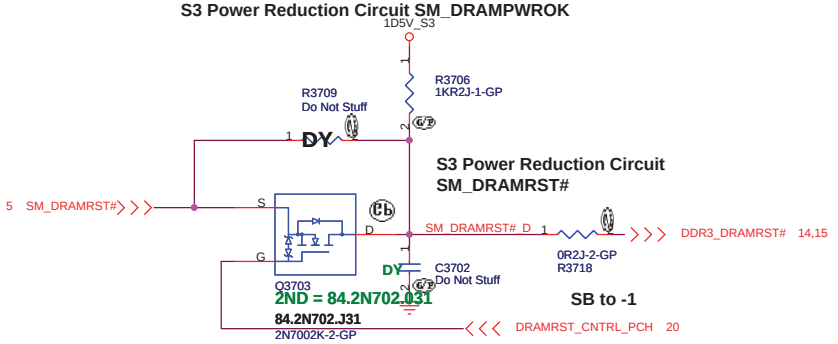


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

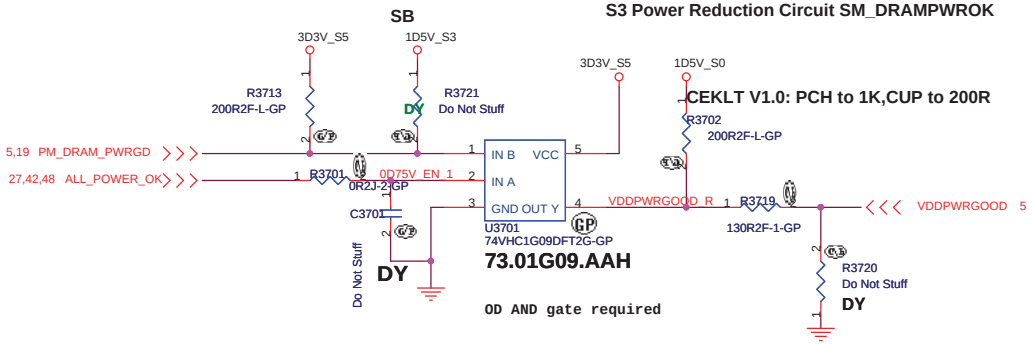
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

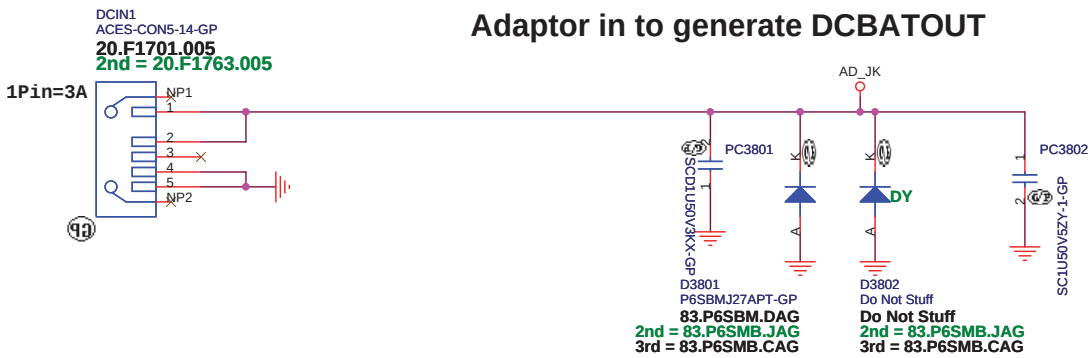
Title: ADAPTER

Size	Document Number	Rev
A3	JE40-HR	-1

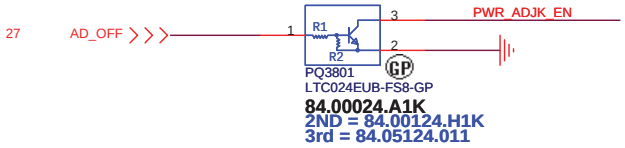
Date: Thursday, December 02, 2010 Sheet 37 of 102

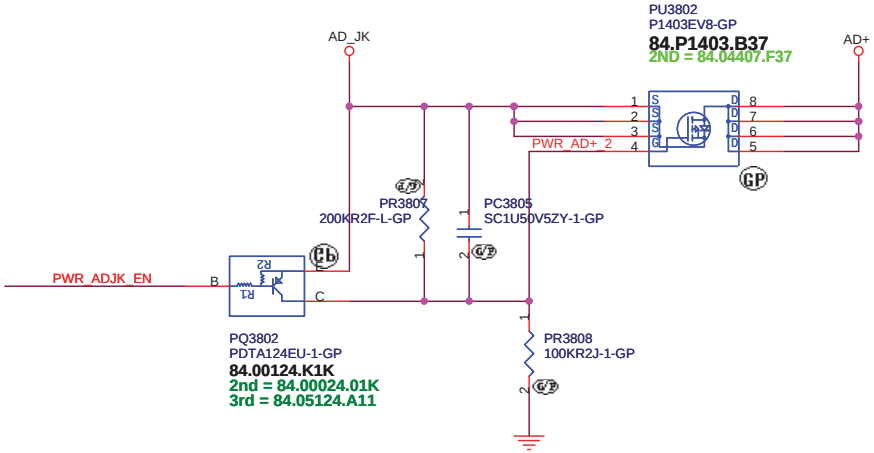
ANNIE solution

Adaptor in to generate DCBATOUT



JE40 change DCIN1 part number

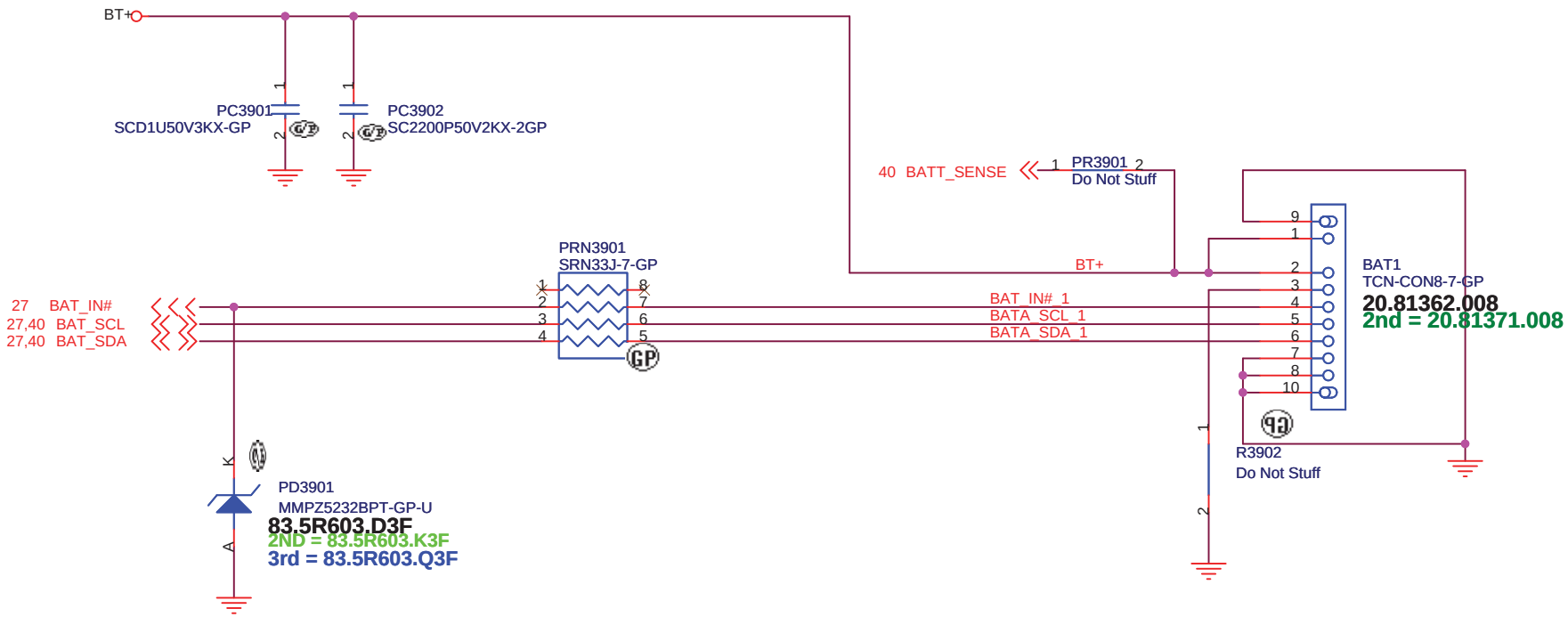




HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 38 of 102	

BATTERY CONNECTOR



EC Protect

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BATT CONN		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 39 of 102	

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

ADD A 24V ZENAR

20100706 Wayne

20100721

20101018

JE40 HR RF

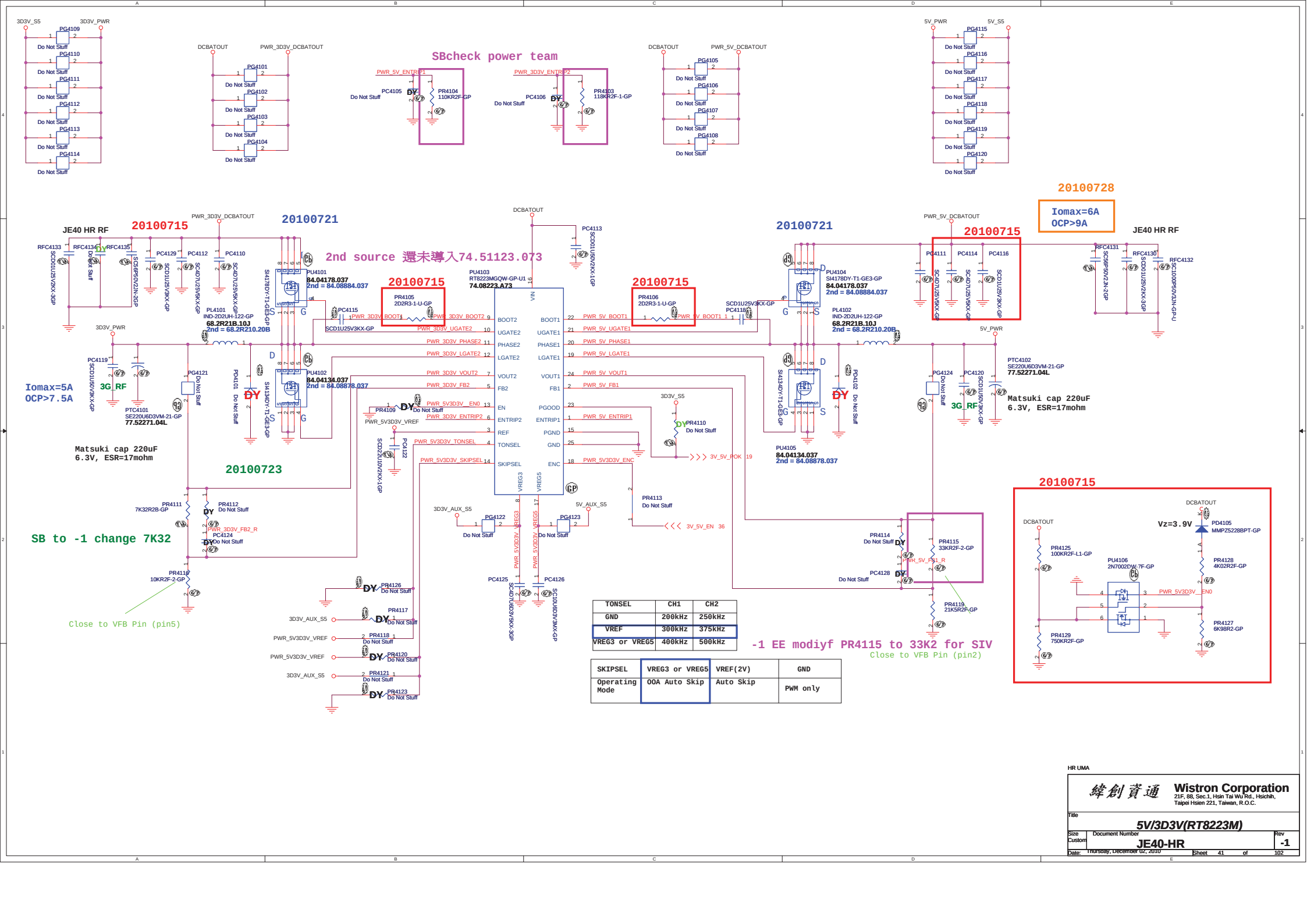
-1M

-1M

AC_OK to KBC

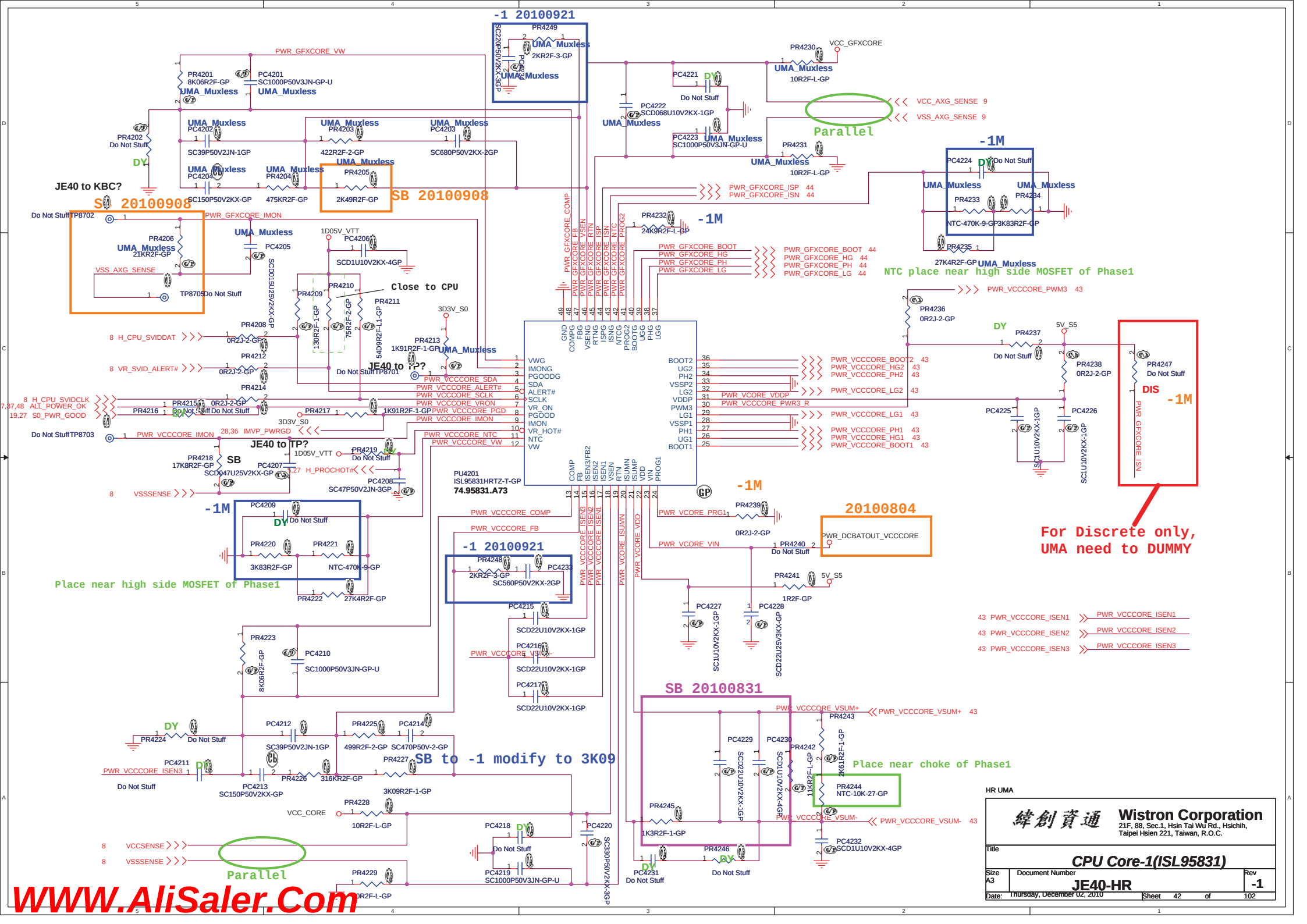
HR UMA

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CHARGER BQ24745	
Size: A3	Document Number: JE40-HR
Rev: -1	
Date: Thursday, December 02, 2010	Sheet 40 of 102



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only


-1 20100921
SB 20100908
JE40 to KBC?
SB 20100908
Close to CPU
JE40 to TP?
JE40 to TP?
SB
-1M
Place near high side MOSFET of Phase1
-1 20100921
SB to -1 modify to 3K09
SB 20100831
Place near choke of Phase1
Parallel
Parallel
-1M
NTC place near high side MOSFET of Phase1
-1M
20100804
PWR_DCBATOUT_VCCCORE
For Discrete only,
UMA need to DUMMY
DIS
-1M
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Core-1(ISL95831)
Size A3
Document Number
JE40-HR
Rev -1
Date: Thursday, December 02, 2010
Sheet 42 of 102
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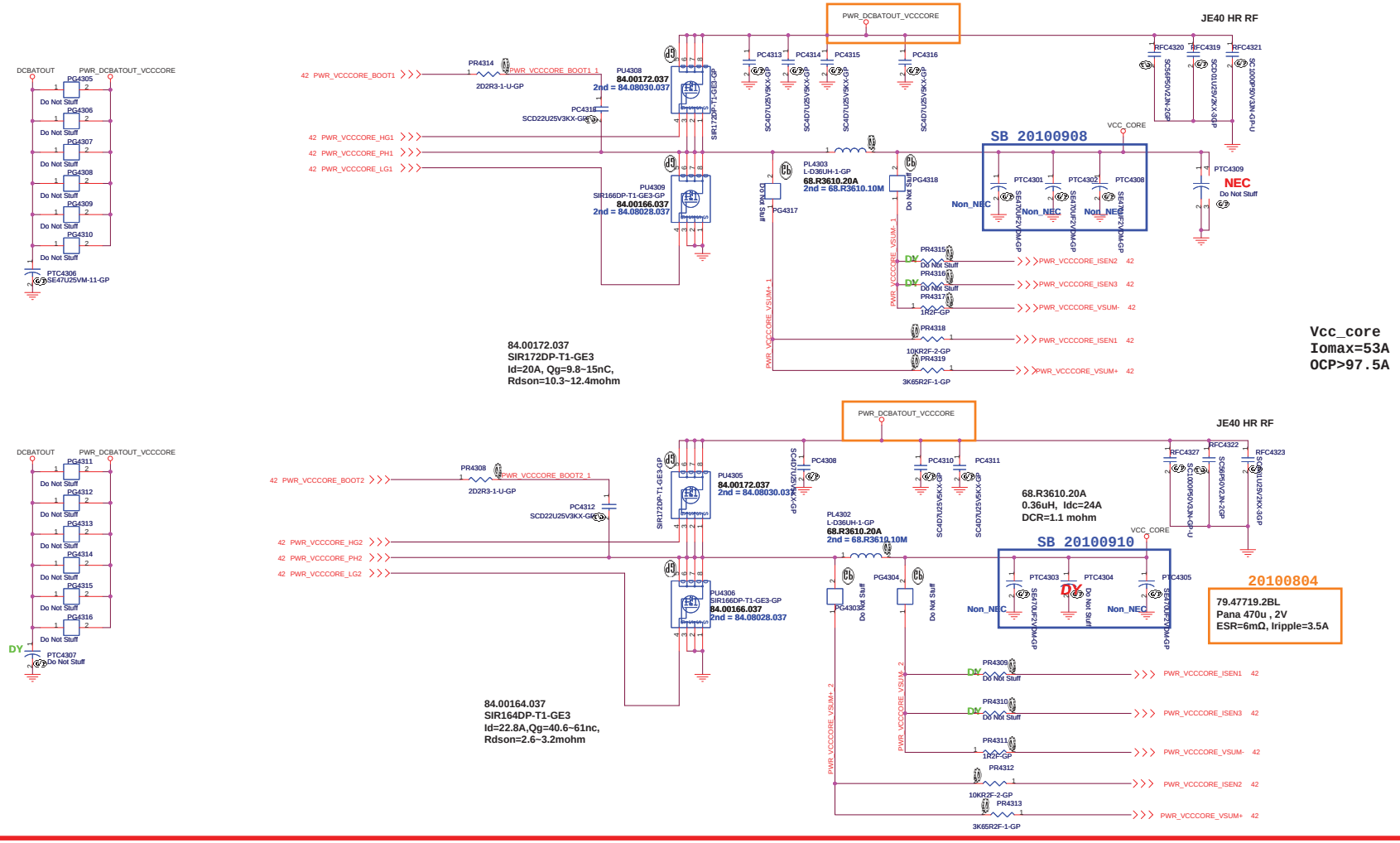


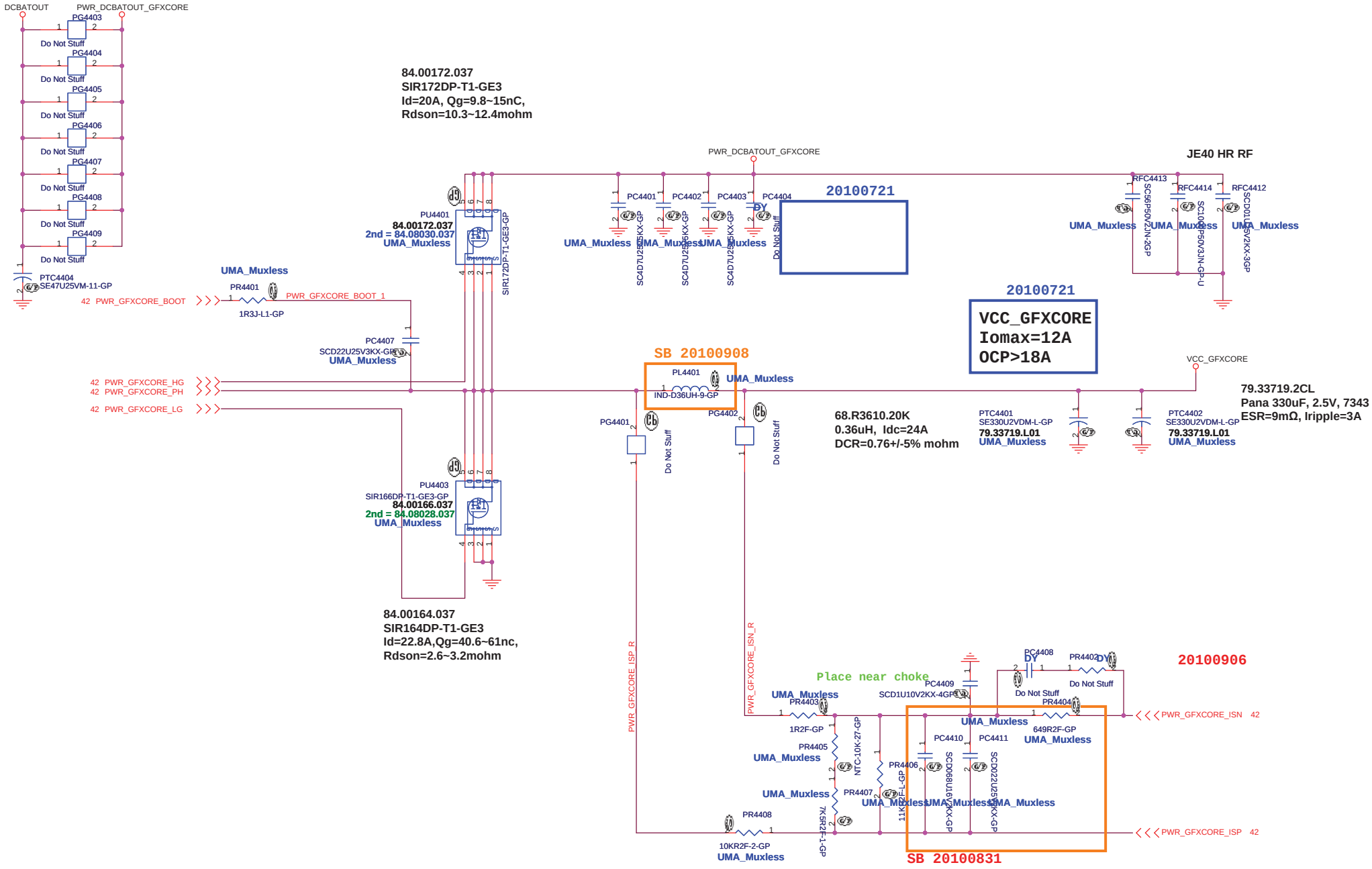
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU Core-2(ISL95831)*

Size: A2 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 43 of 102



HR UMA

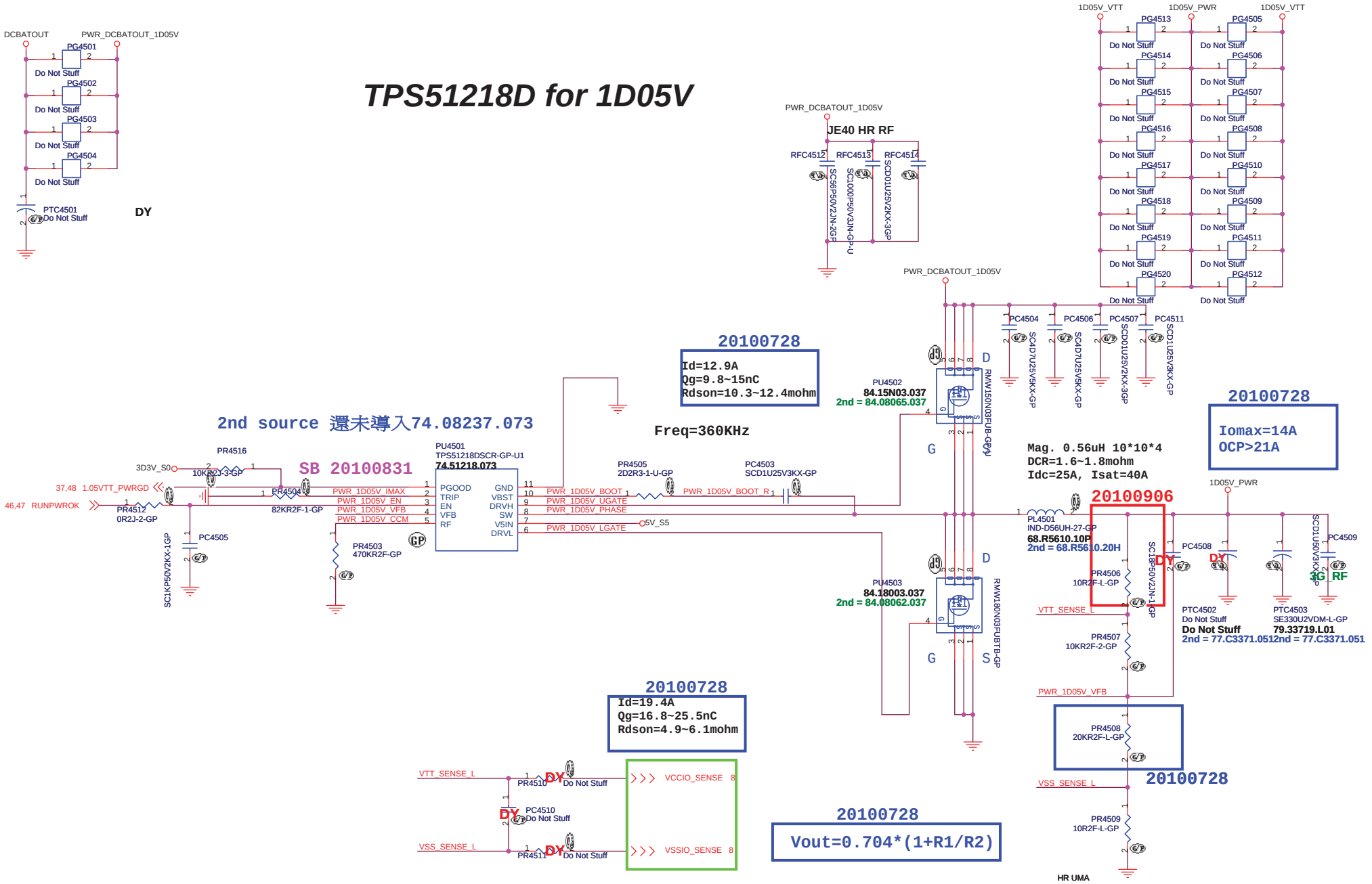
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Core-3(ISL95831)

Size: A3 | Document Number: JE40-HR | Rev: -1

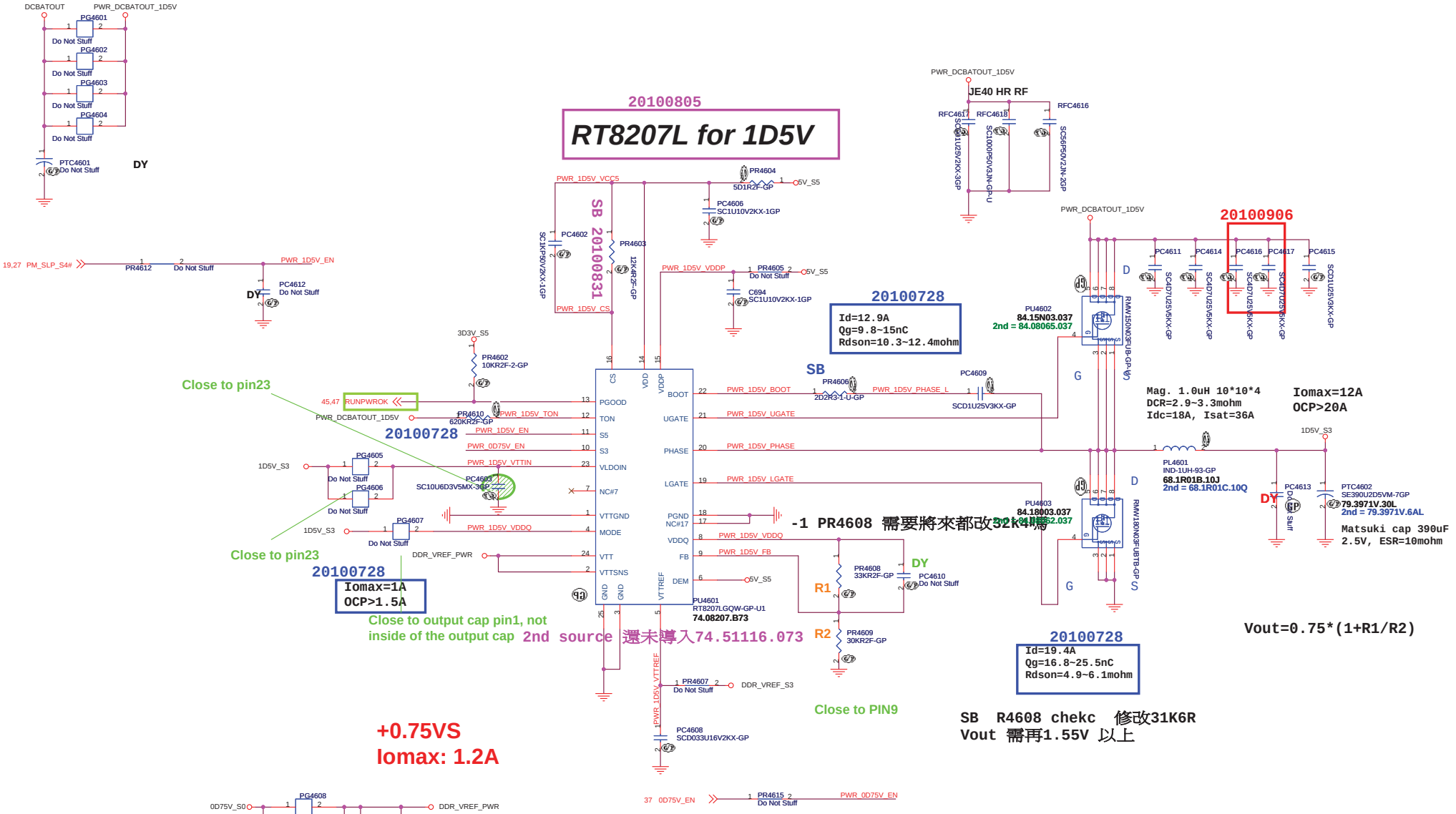
Date: Thursday, December 02, 2010 | Sheet 44 of 102

TPS51218D for 1D05V



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DC to DC 1D05V(TPS51218D)		
Size A3	Document Number JE40-HR	Rev	-1
Date: Thursday, December 02, 2010	Sheet 45 of 102		

SSID = PWR.Plane.Regulator_1p5v0p75v



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

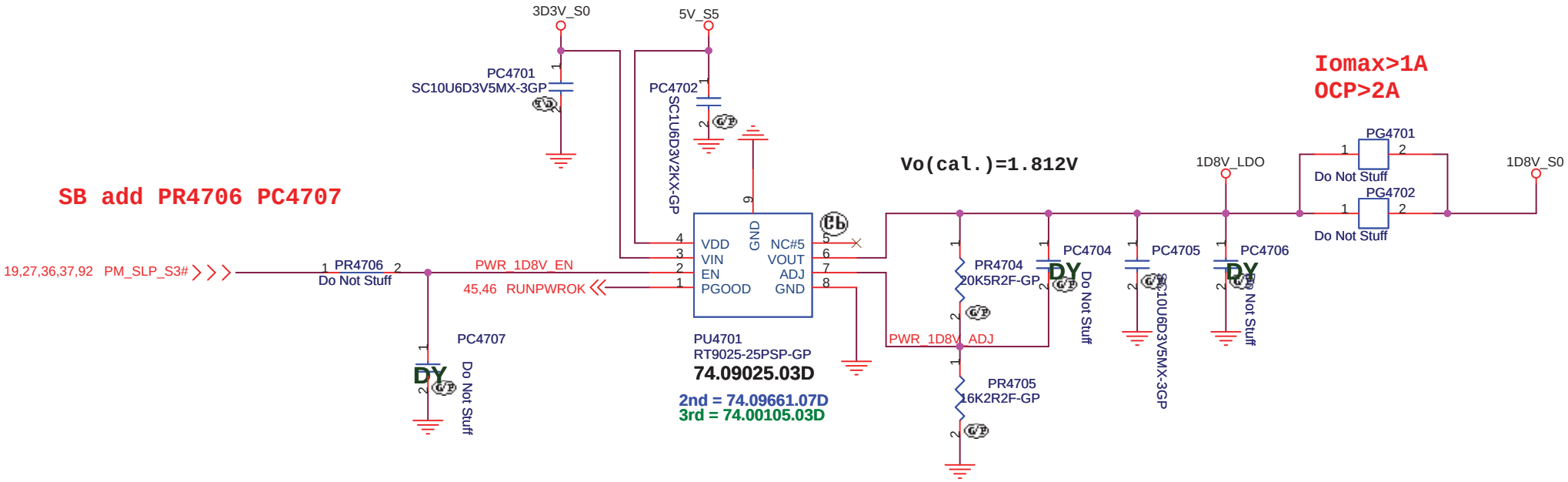
Title: TPS5111

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 46 of 102

SSID = PWR.Plane.Regulator_1p8v

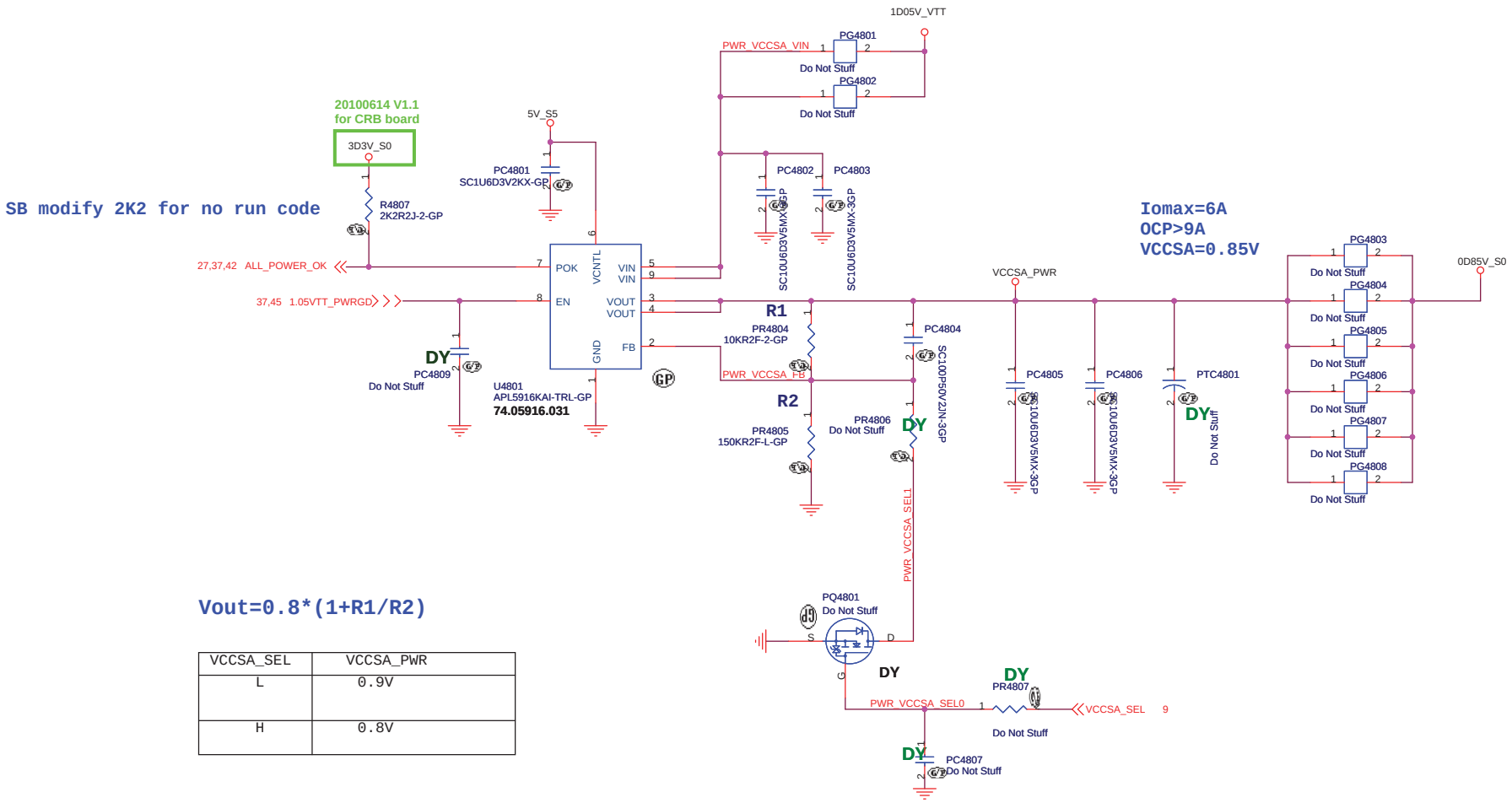
RT9025 for 1D8V_S0



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 47 of 102	

APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

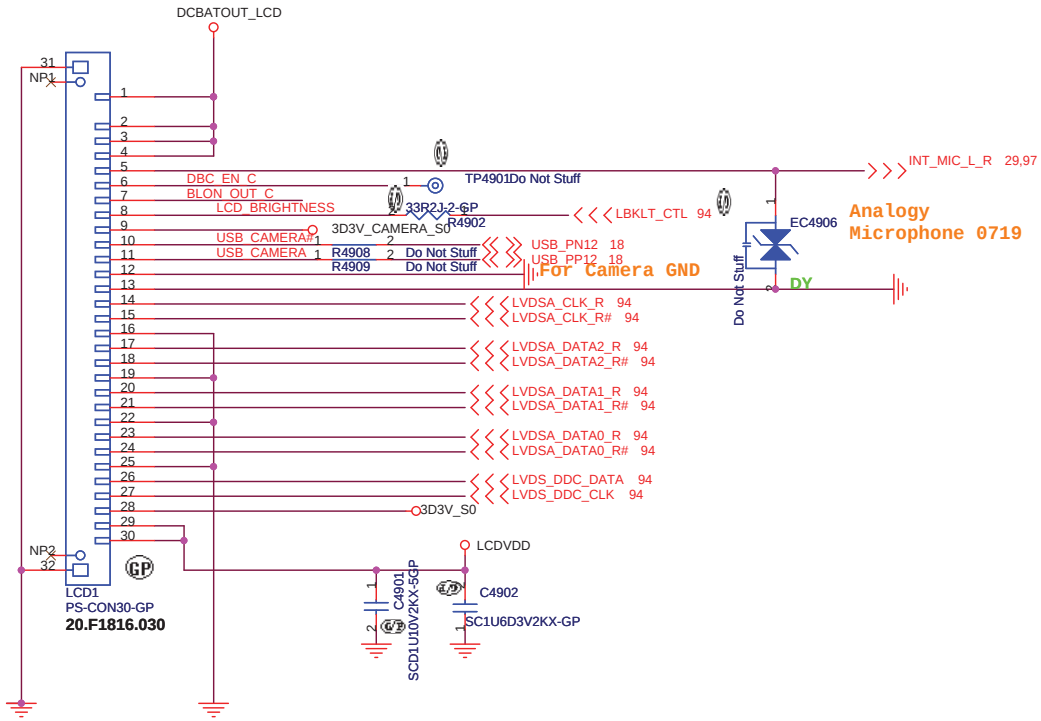
Title: *LDO VCCSA(APL5916)*

Size	Document Number	Rev
A3	JE40-HR	-1

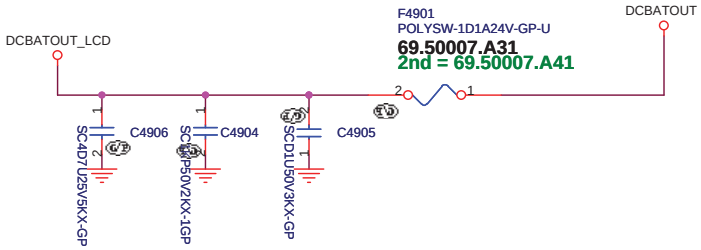
Date: Thursday, December 02, 2010 Sheet 48 of 102

SSID = VIDEO

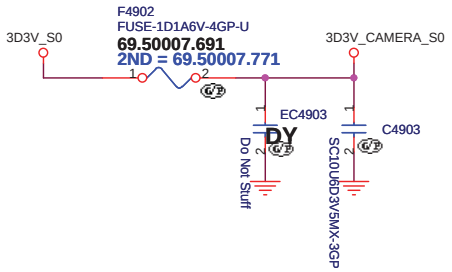
LVDS CONNECTOR



INVERTER POWER

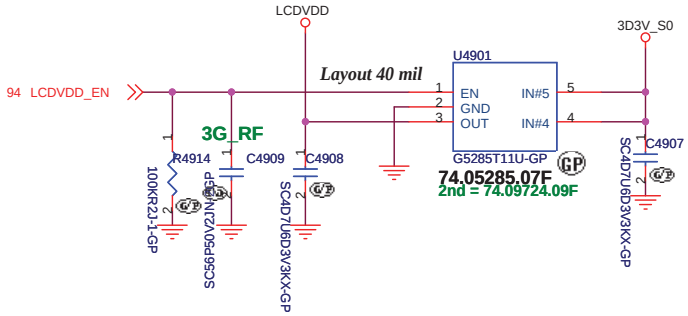


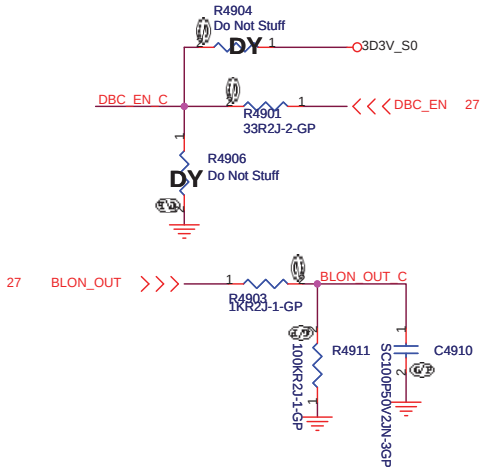
Camera Power



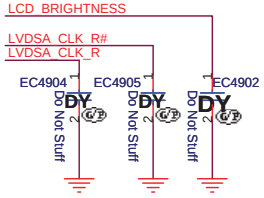
SSID = VIDEO

LCD POWER for ANNIE



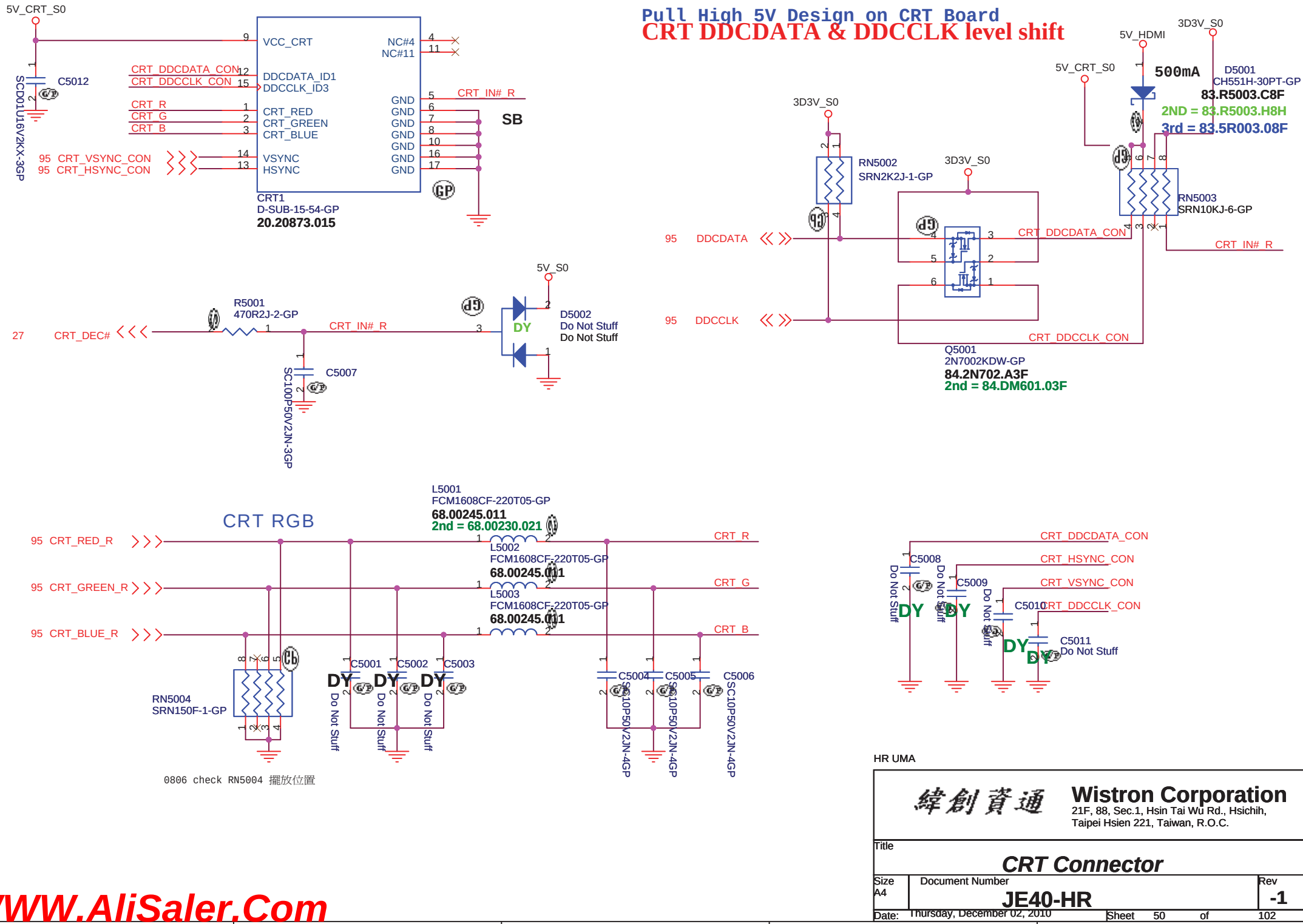


For EMI request
Close to LVDS connector



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LCD Connector*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 49 of 102	


Pull High 5V Design on CRT Board
CRT DDCDATA & DDCCLK level shift
5V_CRT_S0
C5012
SCD01U16V2KX-3GP
CRT_DDCDATA_CON
CRT_DDCCLK_CON
CRT_R
CRT_G
CRT_B
95 CRT_VSYNC_CON
95 CRT_HSYNC_CON
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
CRT_IN#_R
SB
CRT1
D-SUB-15-54-GP
20.20873.015
3D3V_S0
5V_HDMI
5V_CRT_S0
500mA
D5001
CH551H-30PT-GP
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F
RN5002
SRN2K2J-1-GP
RN5003
SRN10KJ-6-GP
95 DDCDATA
95 DDCCLK
Q5001
2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
5V_S0
R5001
470R2J-2-GP
27 CRT_DEC#
C5007
SC100P50V2JN-3GP
D5002
Do Not Stuff
Do Not Stuff
CRT RGB
L5001
FCM1608CF-220T05-GP
68.00245.011
2nd = 68.00230.021
L5002
FCM1608CF-220T05-GP
68.00245.011
L5003
FCM1608CF-220T05-GP
68.00245.011
95 CRT_RED_R
95 CRT_GREEN_R
95 CRT_BLUE_R
CRT_R
CRT_G
CRT_B
RN5004
SRN150F-1-GP
C5001
C5002
C5003
C5004
C5005
C5006
SC10P50V2JN-4GP
Do Not Stuff
DY
C5008
C5009
C5010
C5011
CRT_DDCDATA_CON
CRT_HSYNC_CON
CRT_VSYNC_CON
CRT_DDCCLK_CON
0806 check RN5004 擺放位置
HR UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT Connector
Size
A4
Document Number
JE40-HR
Rev
-1
Date: Thursday, December 02, 2010
Sheet 50 of 102
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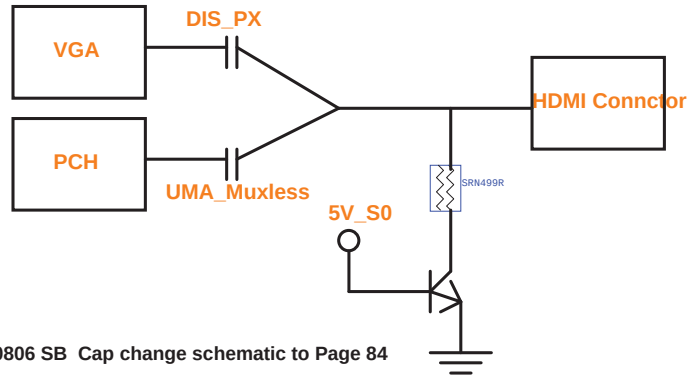
SSID = VIDEO

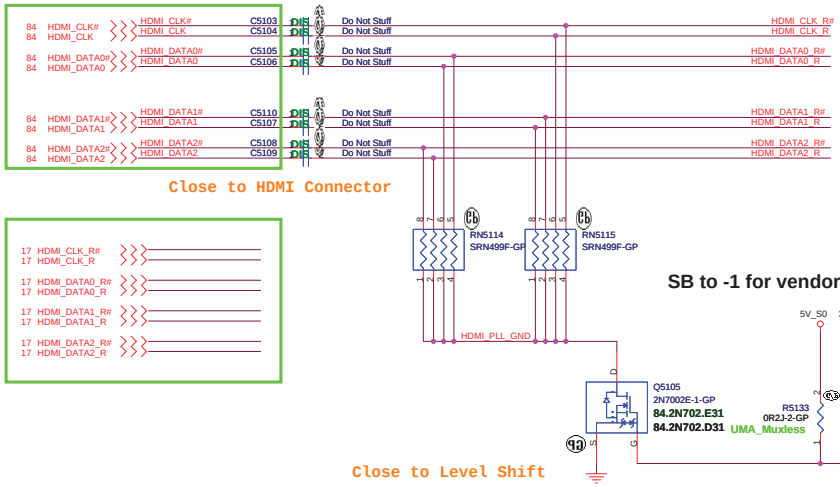
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

HDMI DISCRETE/ UMA Co-lay

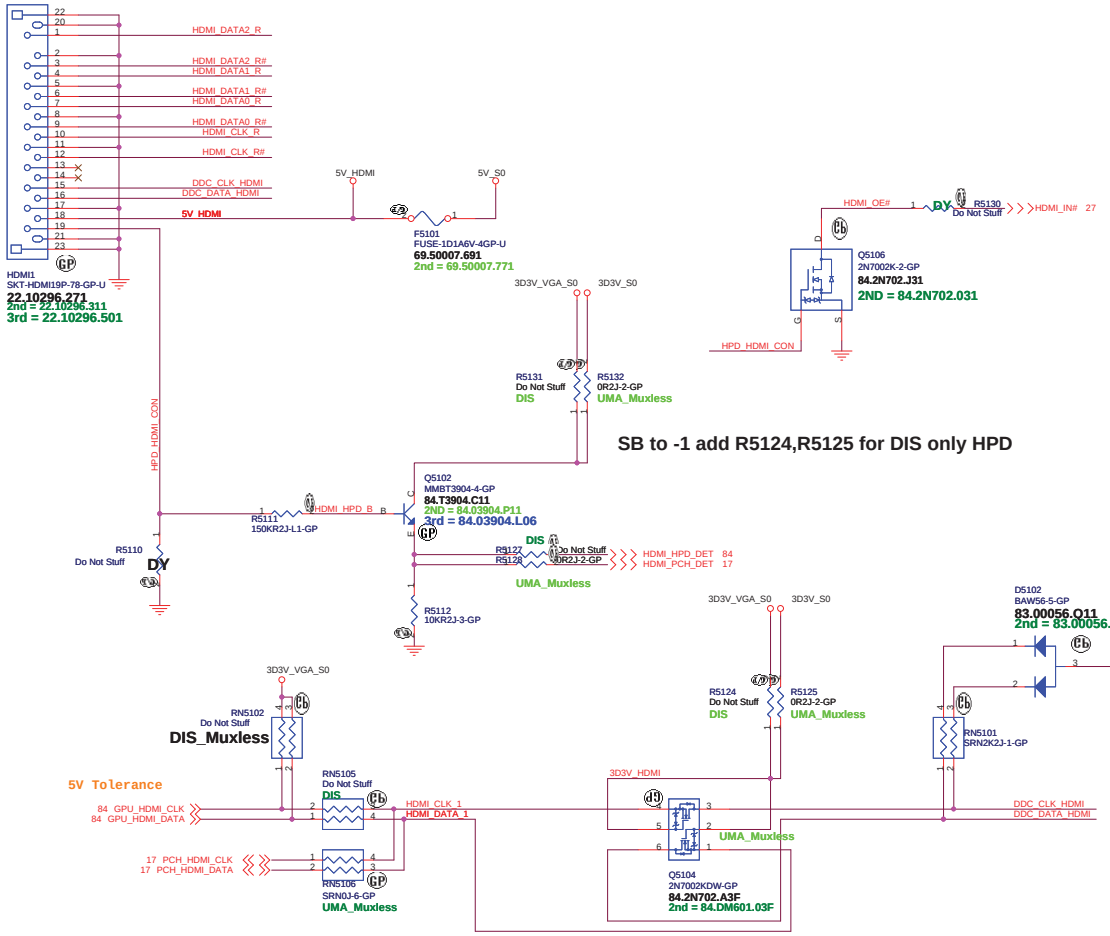


0806 SB Cap change schematic to Page 84



SB to -1 for vendor suggest

HDMI CONN



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
Custom	JE40-HR	-1

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LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***eDP***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 52 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 53 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

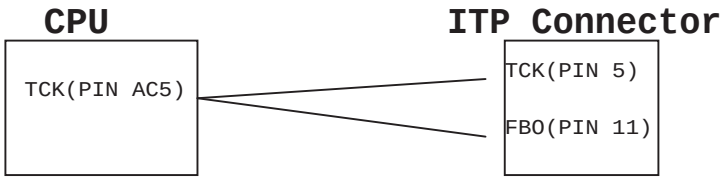
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

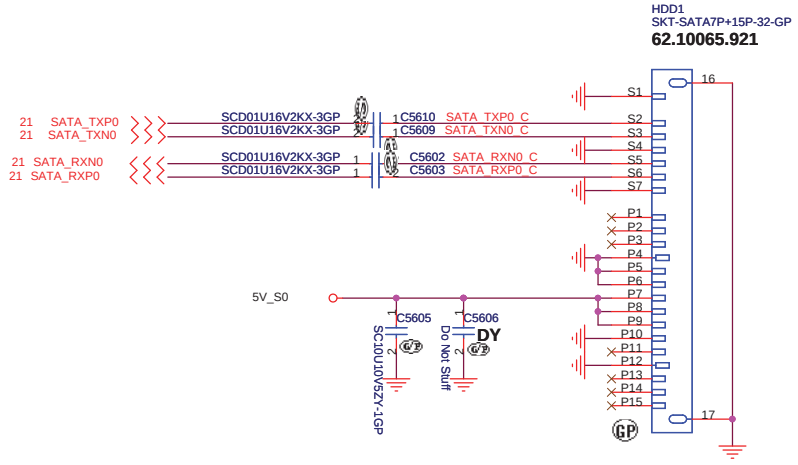


HR UMA

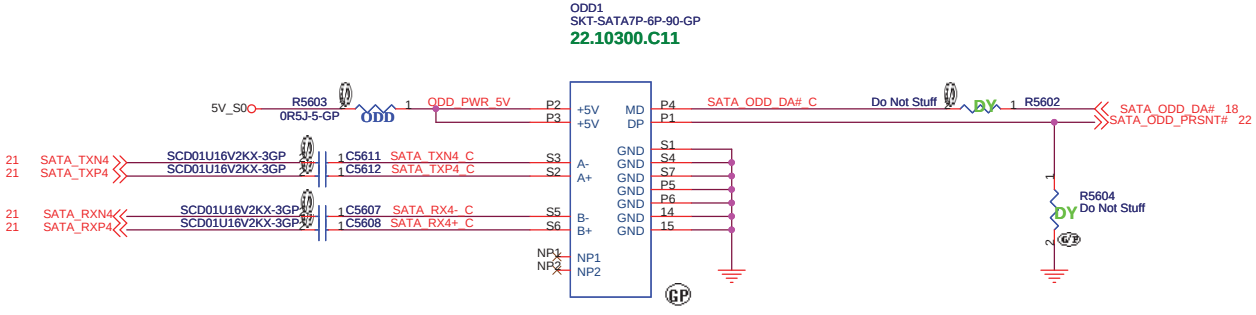
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ITP		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 55 of 102	

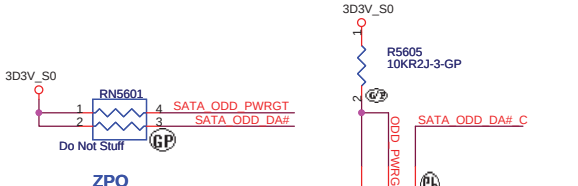
SSID = SATA

SATA HDD Connector



ODD Connector



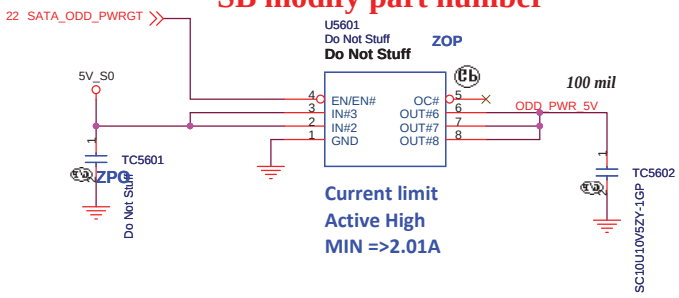


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 56 of 102

ESATA Power

USB CHARGER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***E-SATA/USB CHARGER***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

JE40 delete Line in function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

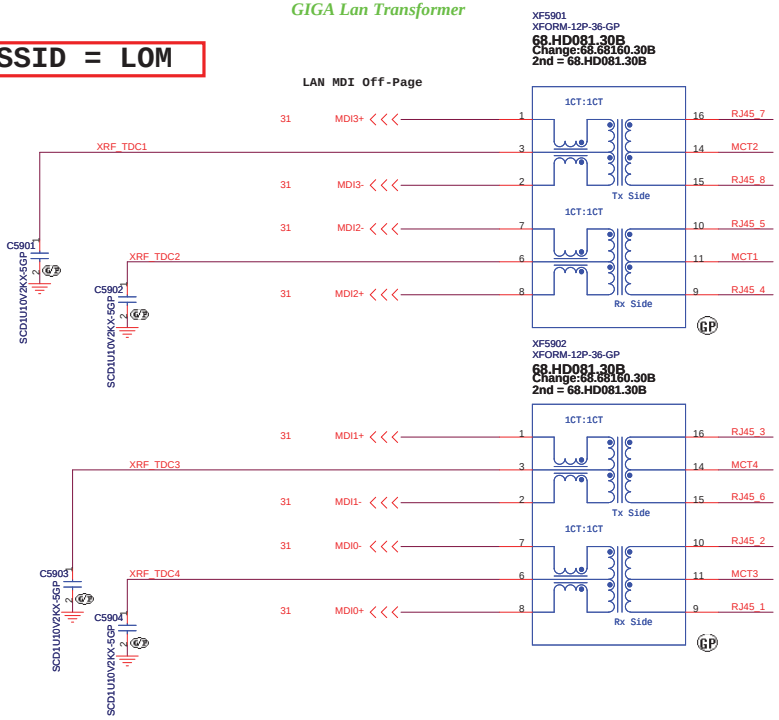
Size	Document Number	Rev
A3	JE40-HR	-1

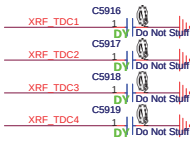
Date: Thursday, December 02, 2010 Sheet 58 of 102

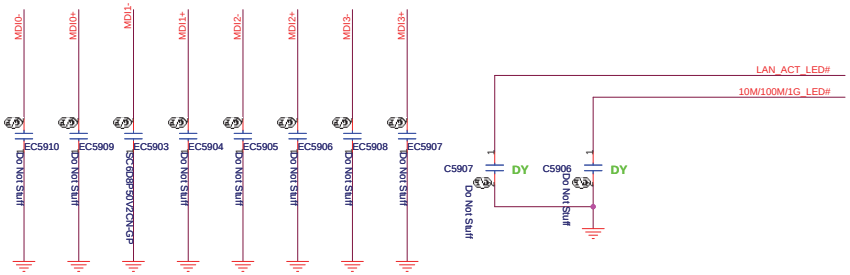
GIGA Lan Transformer

SSID = LOM

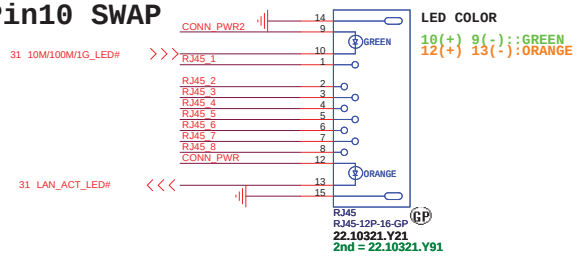
LAN MDI Off-Page

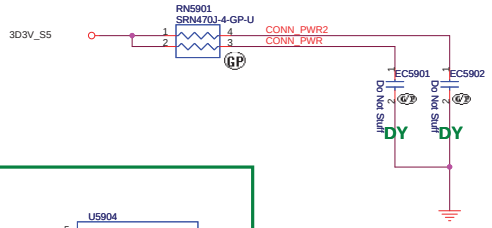




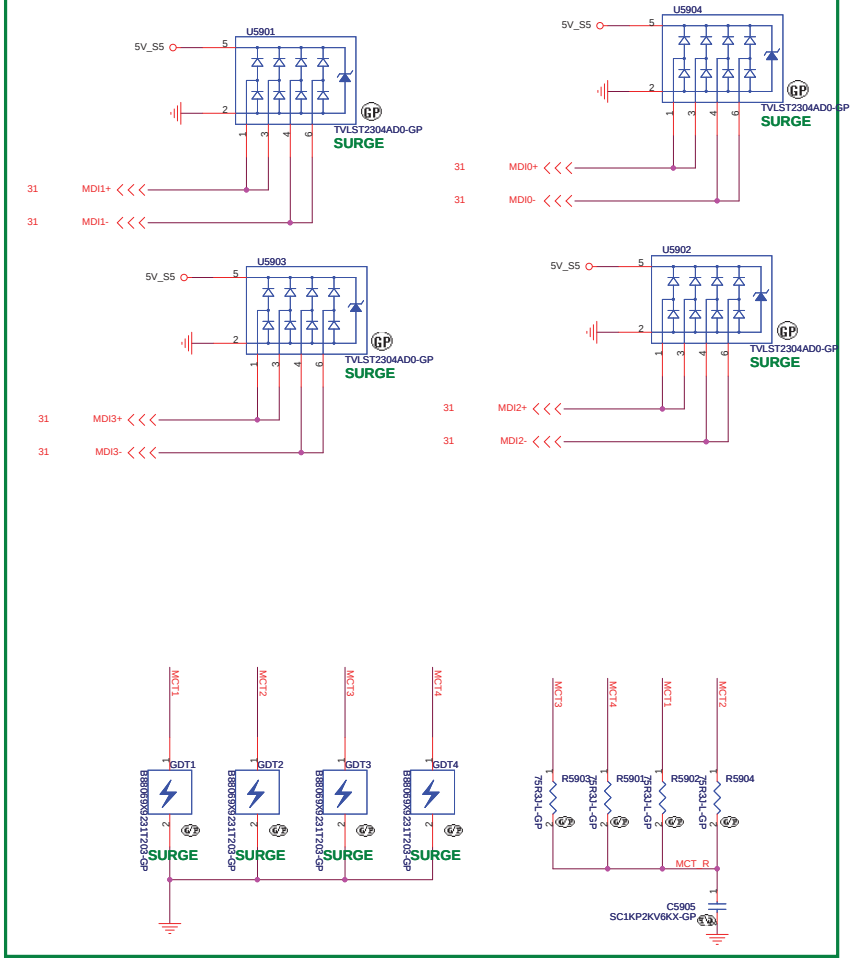


SB modiyf Pin9 Pin10 SWAP





SB modify For EMI

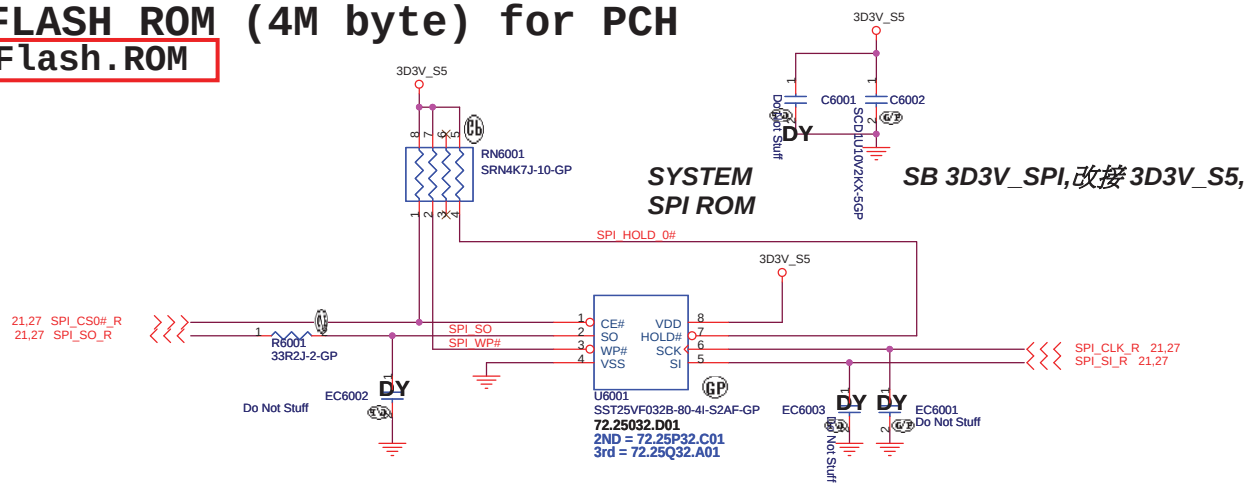


HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **LAN CONNECTOR**		
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 59 of 102	

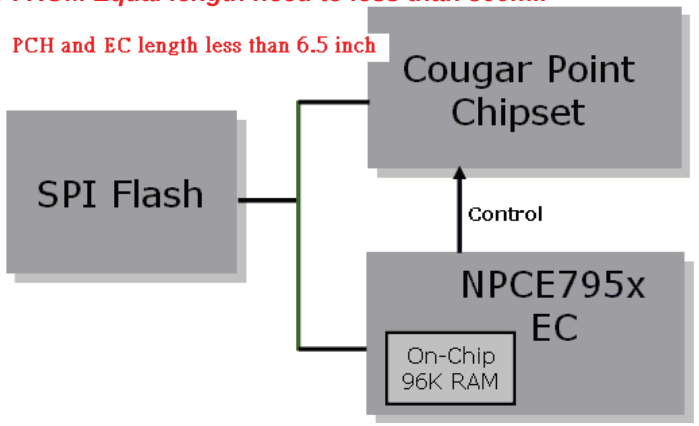
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

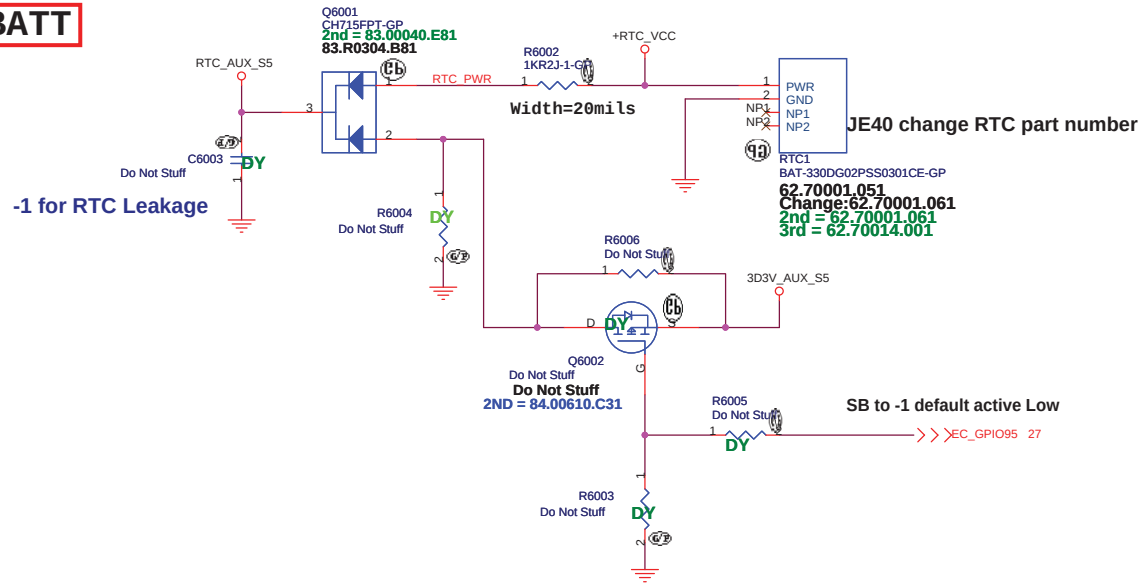


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT

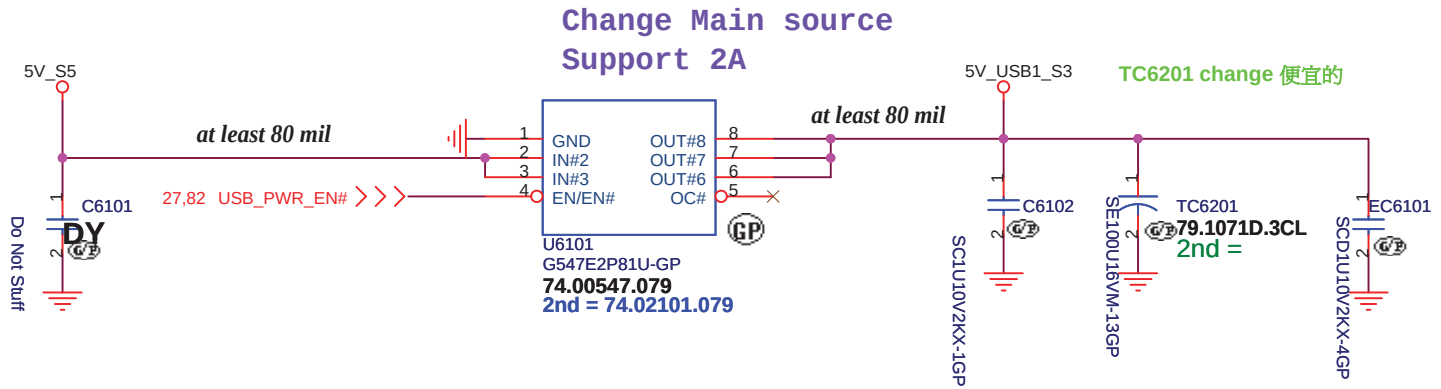


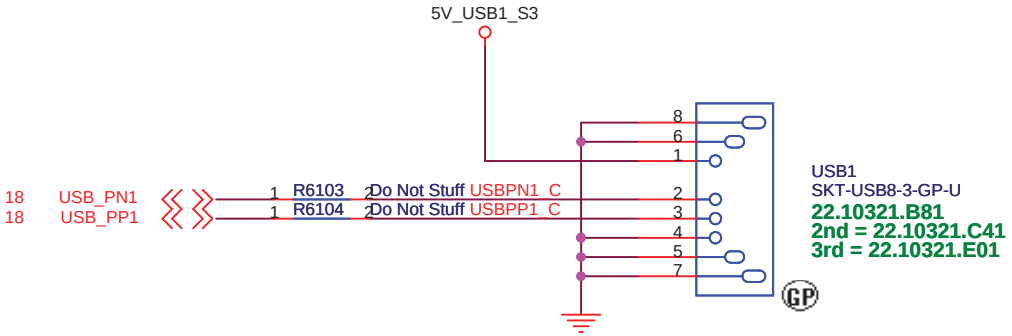
HR UMA

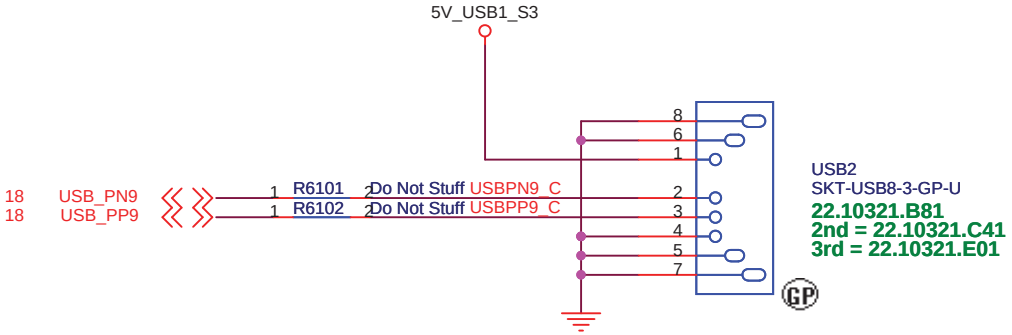
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 60 of 102	

SSID = USB

IO Board USB Power







HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB Power SW**

Size	Document Number	Rev
A4	JE40-HR	-1

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Port***

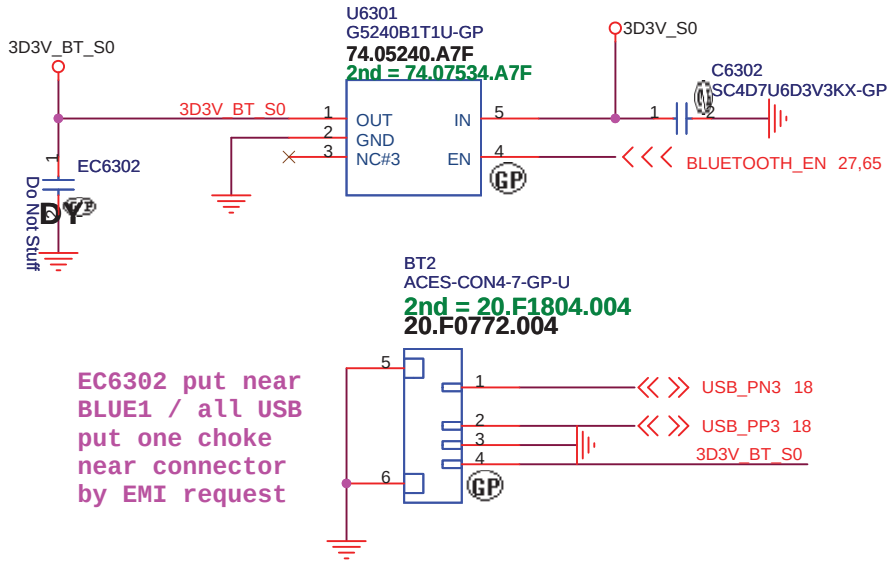
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Bluetooth*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 63 of 102	

Finger printer

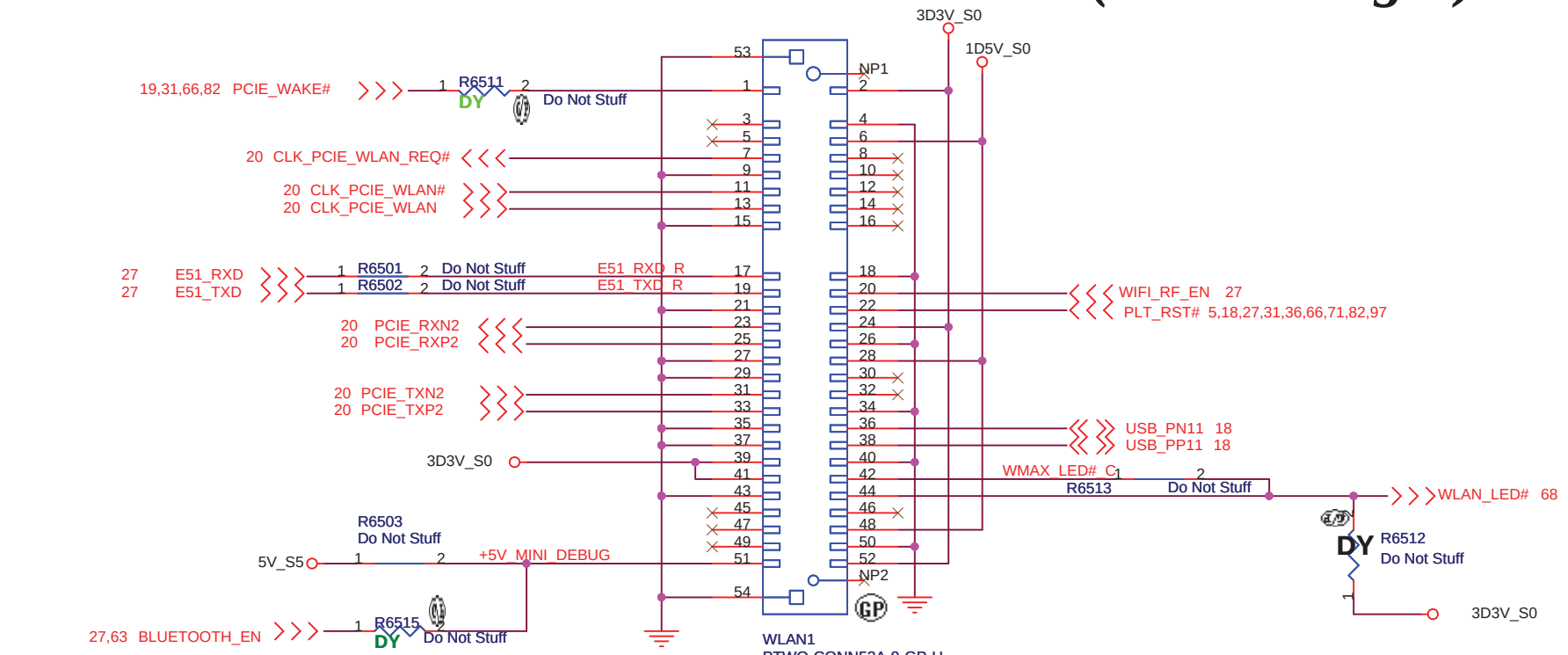
JE40 delete FP function

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 64 of 102	

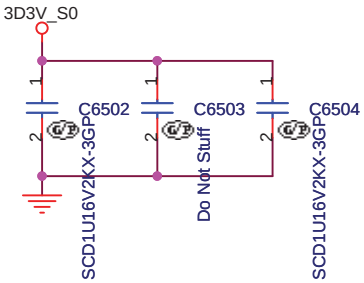
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



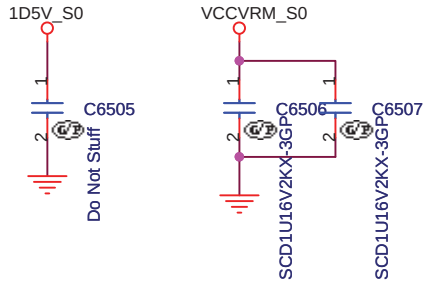
20.F1519.052

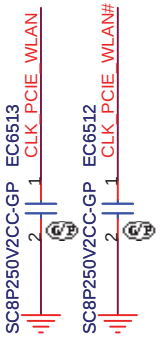
2nd = 62.10043.A51
3rd = 20.F1693.052
4th = 20.F1743.052



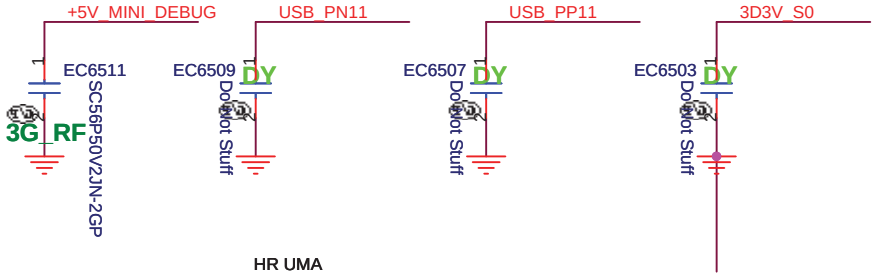
SB modify for SIV

-2





RF suggestion



HR UMA

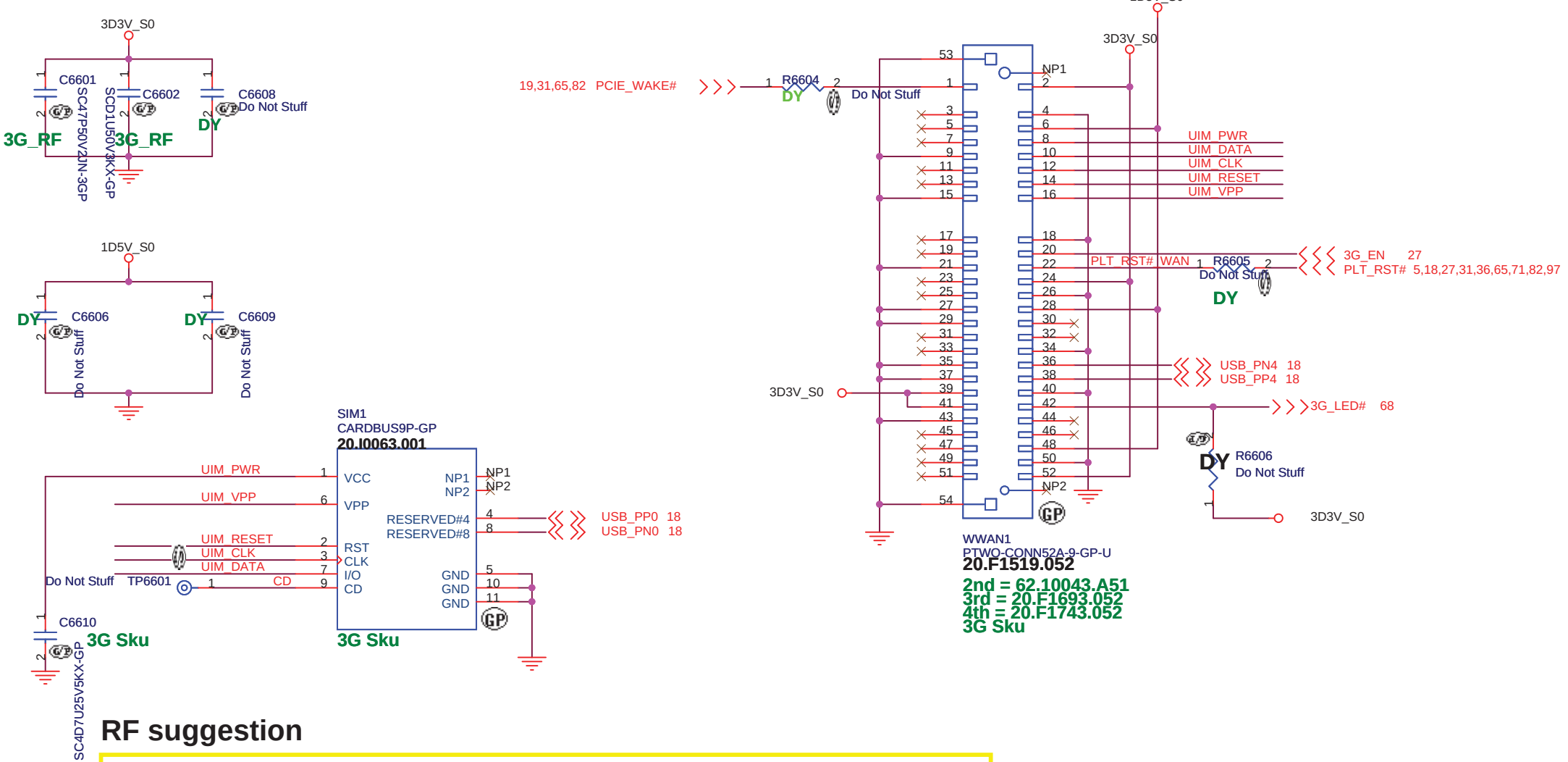
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINICARD(WLAN)/ITP CONN		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 65 of 102	

SSID = Wireless

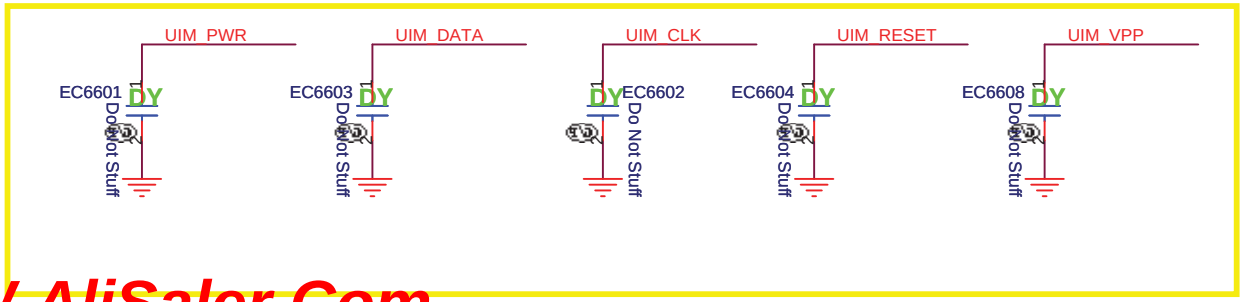
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **WWAN Connector**

Size	Document Number	Rev
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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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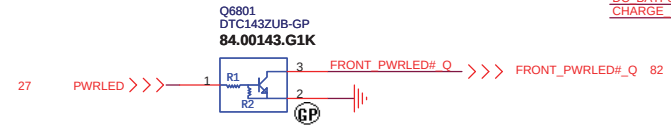
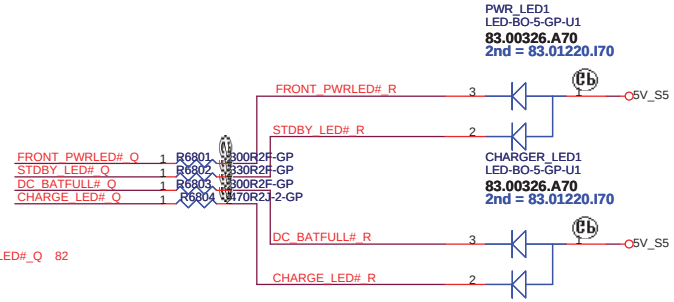
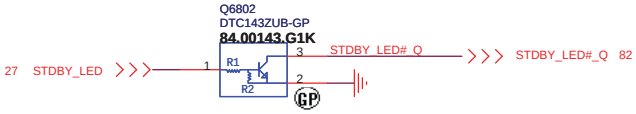
SSID = User.Interface

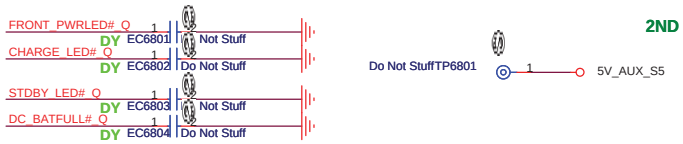
Power button LED



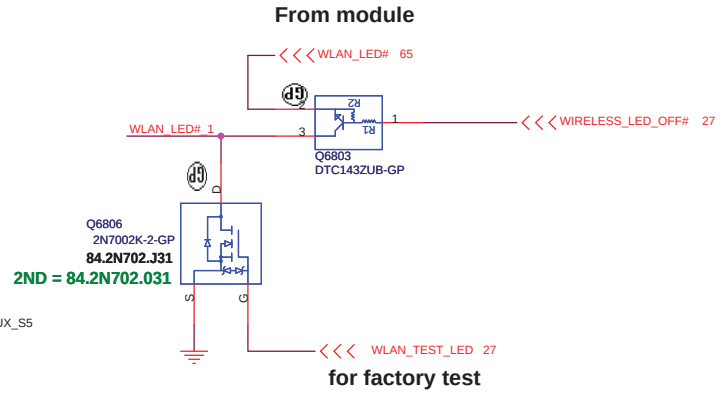


Power STDBY_LED

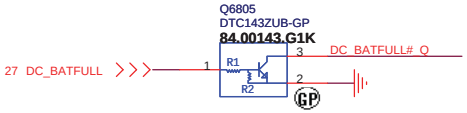




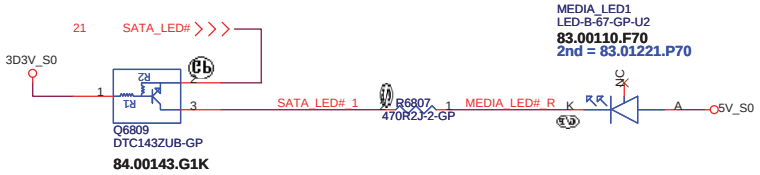
WLAN_LED



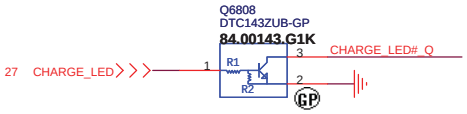
Battery LED2(DC_BATFULL)

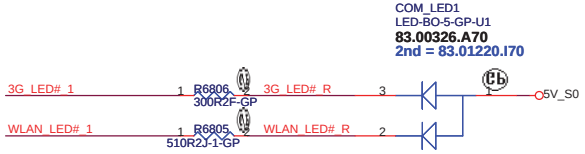


SATA HDD LED

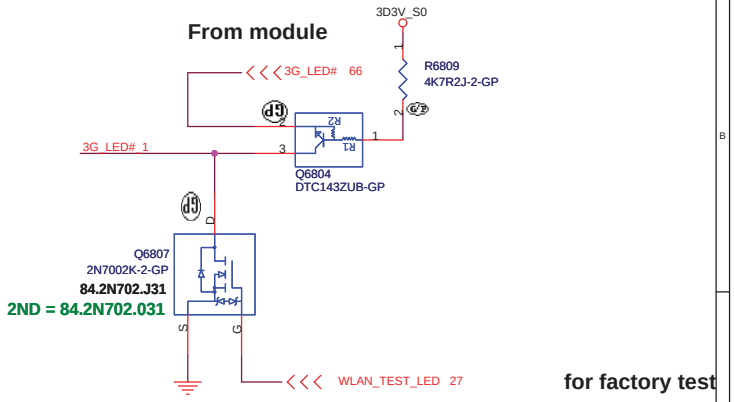


Battery LED1(CHARGE)





3G LED

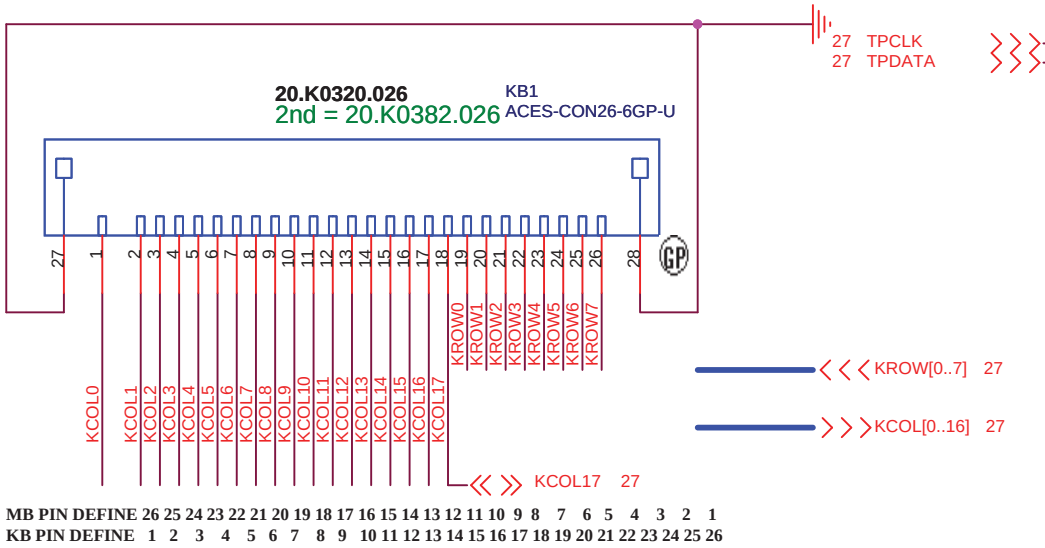


HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LED Bard/Power Button	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 68 of 102	

SSID = KBC

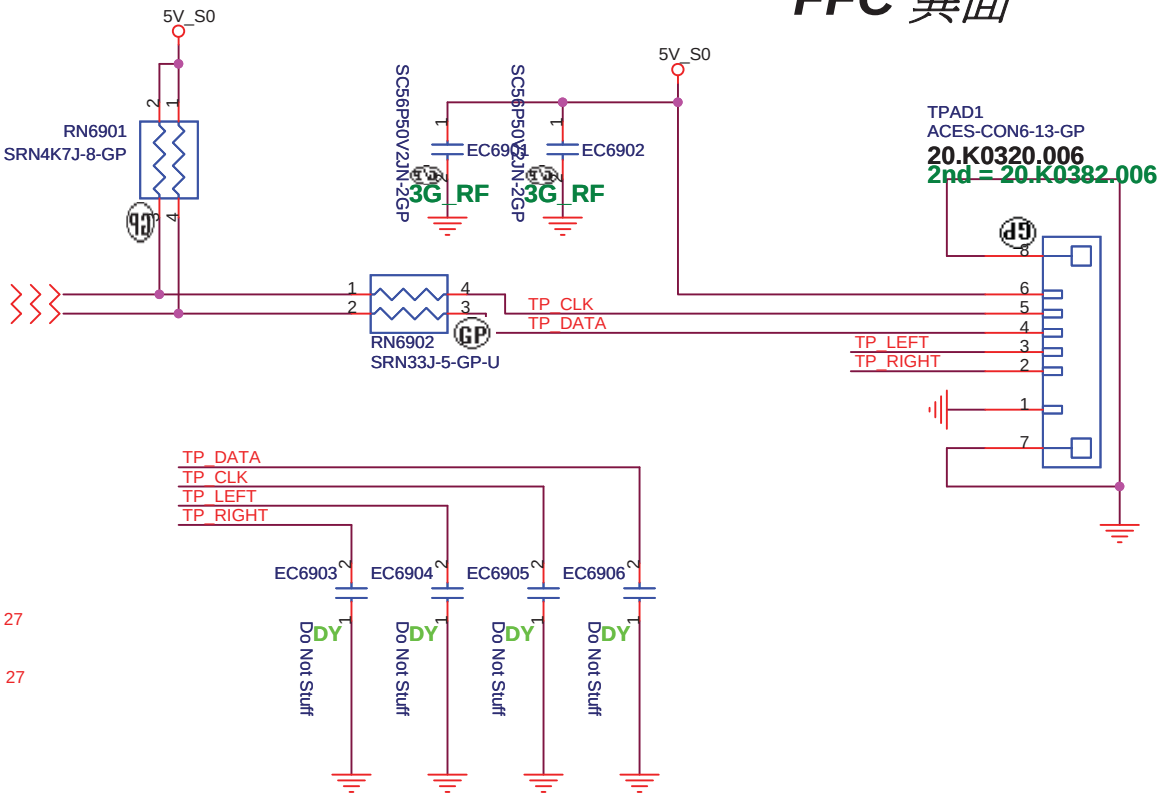
Internal KeyBoard Connector



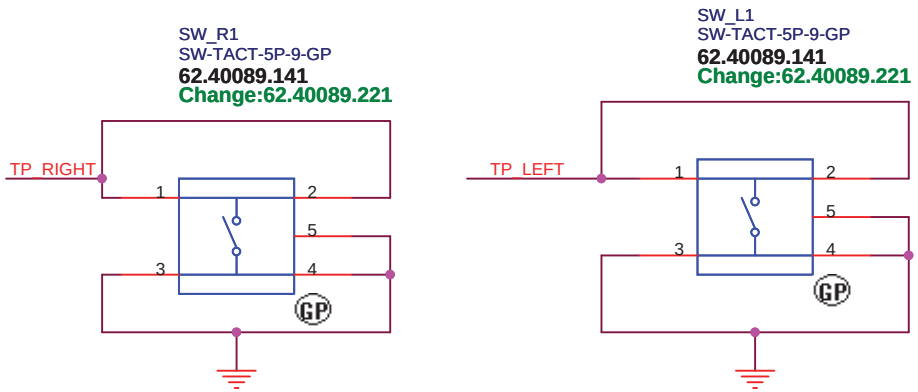
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 K/B 1 **SB to -1 modify Part number**

TOUCH PAD

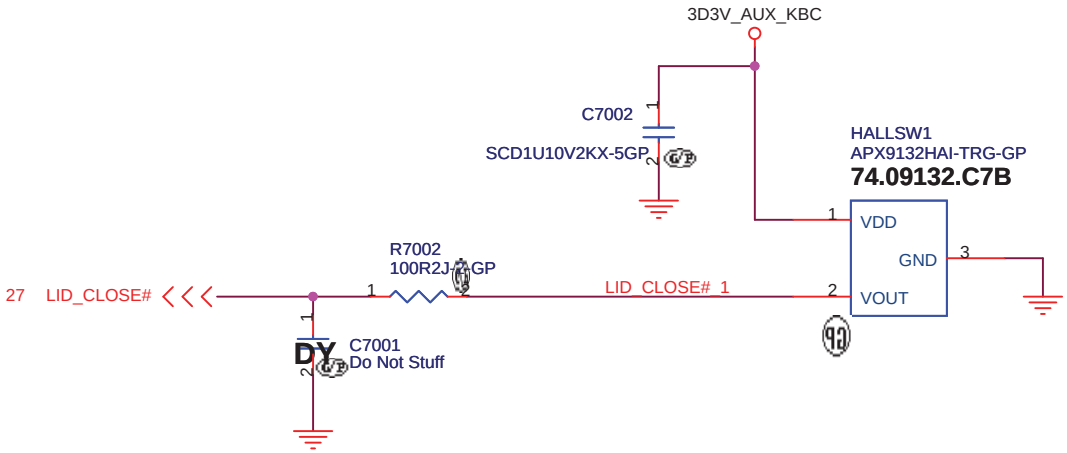


FFC 異面



HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Key Board/Touch Pad***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 69 of 102	



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	JE40-HR	-1

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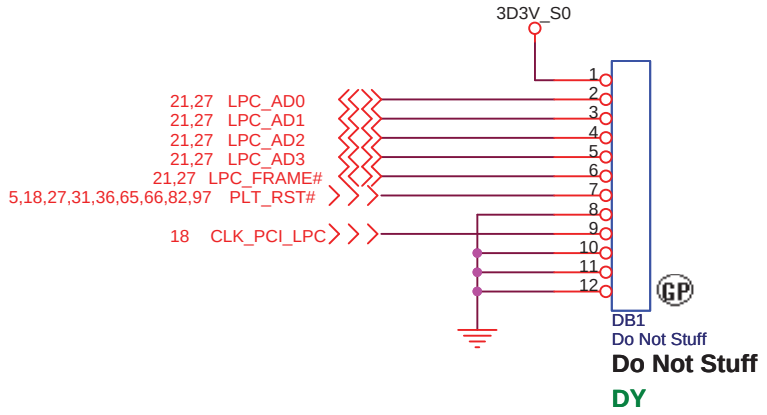

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

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HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 72 of 102

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HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: JE40-HR | Rev: -1

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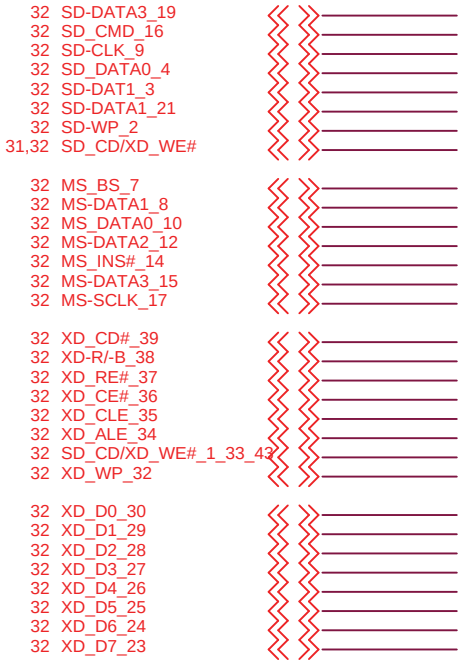
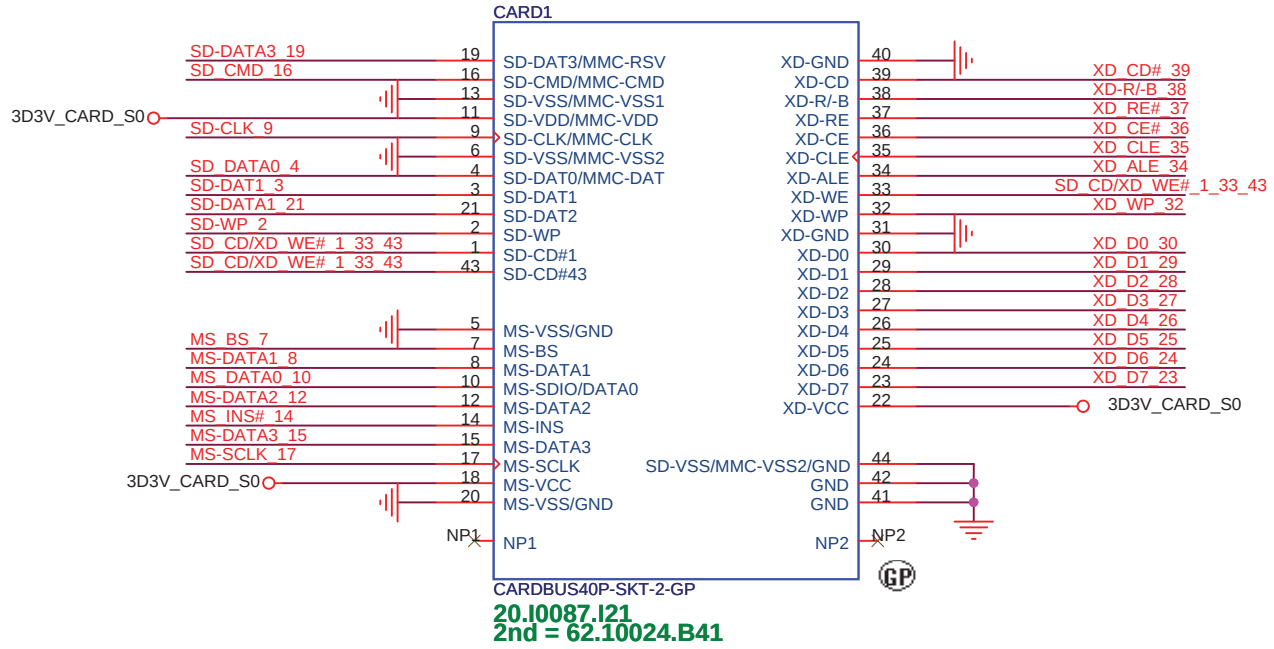
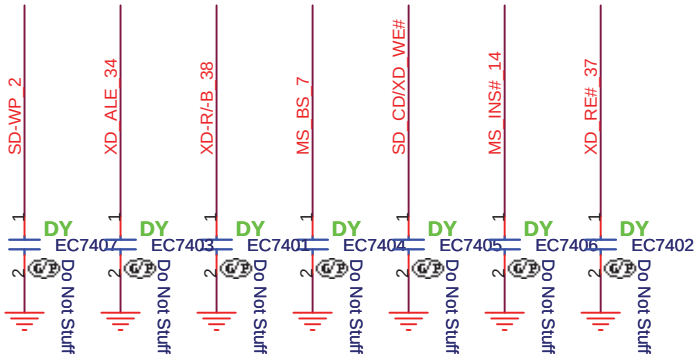
SD/XD/MS Card Reader

SSID = SDIO







HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
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Date: Thursday, December 02, 2010 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 75 of 102

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HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***Reserved***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 76 of 102	

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 77 of 102

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HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
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SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 79 of 102	

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Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 80 of 102

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

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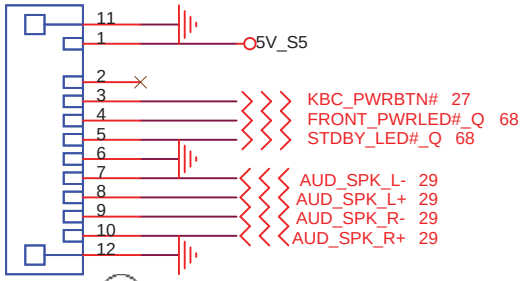
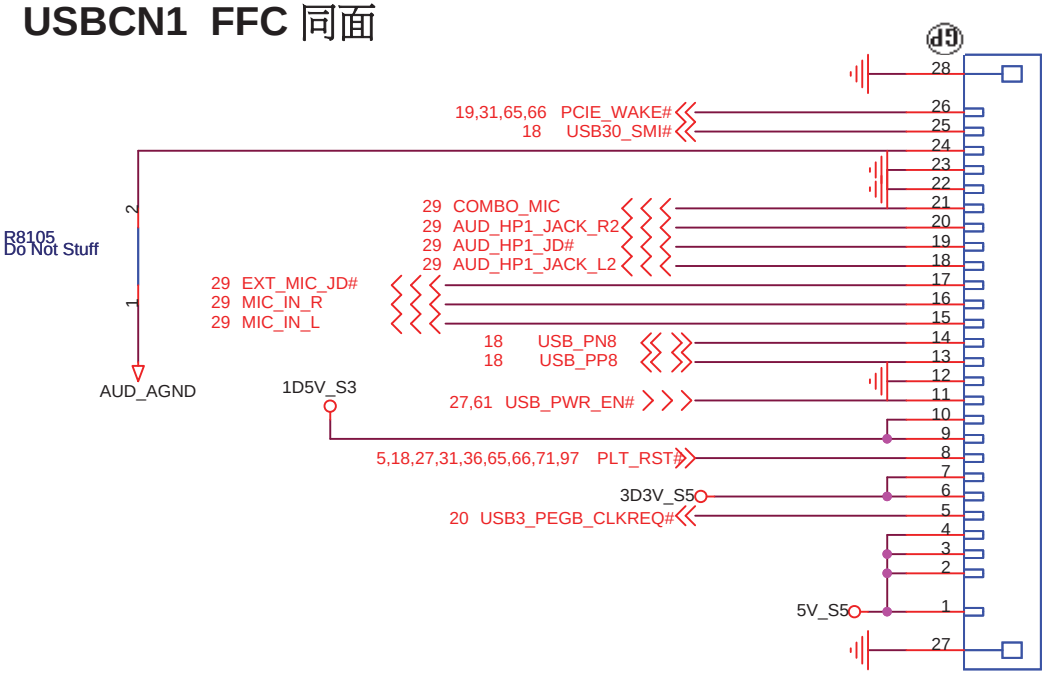
PWRCN1 FFC 異面



PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

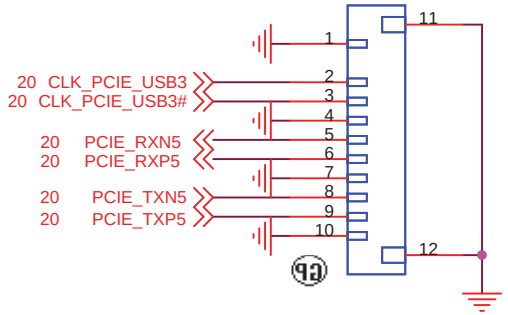
USBCN1 FFC 同面



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

0806 change 10Pin

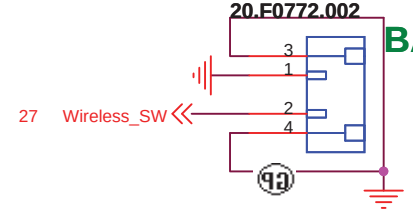
USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

RF_CN1
ACES-CON2-11-GP
20.F0772.002
BAE40



Cabele Wire to BD

HR UMA

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Title: ***IO Board Connector***

Size	Document Number	Rev
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SB 因爲 sequence 會有兩段
R8303 change to pull low 預留 ??

SB Missed 1x 22uF. C8355 Vendor suggest

1.05V +/- 3%
2,200mA
(See NV DG)

X7R, Under GPU.

SB Missed 1x 22uF. C8356 Vendor suggest

X7R, Under GPU.

3.3V +/- 5%
240mA
(See NV DG)

-1 Vendor suggest modify 3D3V_VGA_S0

3.3V +/- 5%
120mA
(See NV DG)

X7R, Under GPU.

-1 delete R8311 for suggest

SB modify to 3D3V_VGA_S0

1.05V +/- 3%
120mA
(See NV DG)

X7R, Under GPU.

X7R, Under GPU.

N12P GV : 71.0N12P.A0U
N12P GS: 71.0N12P.E0U
N11P GS: 71.0N11P.E0U

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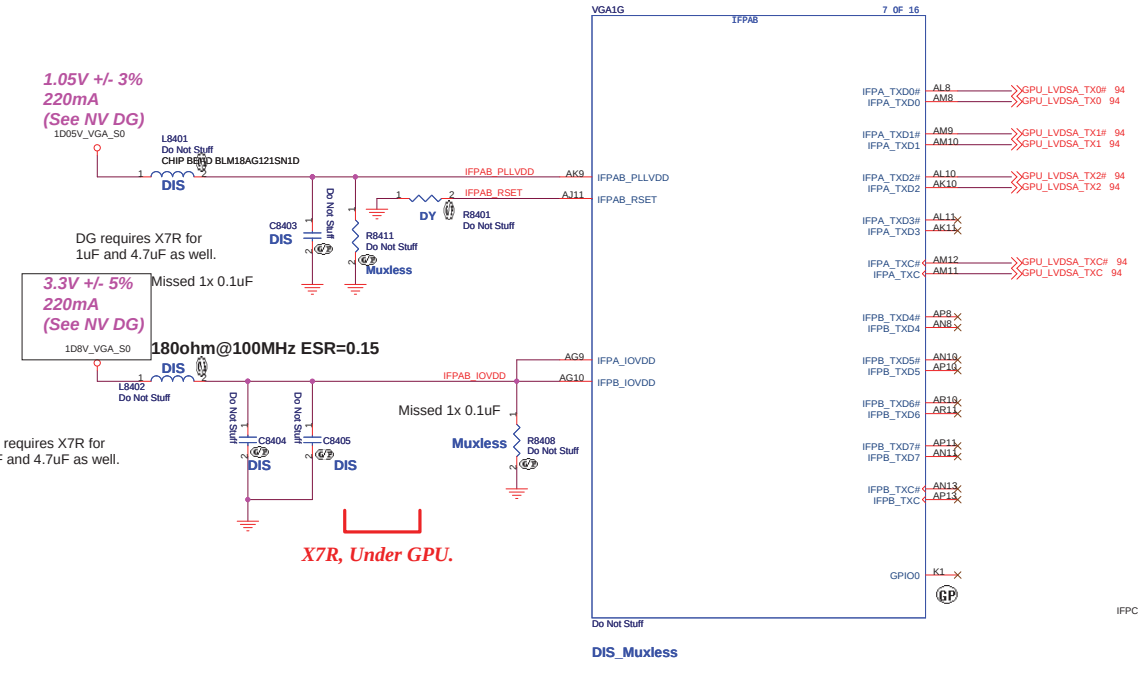
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

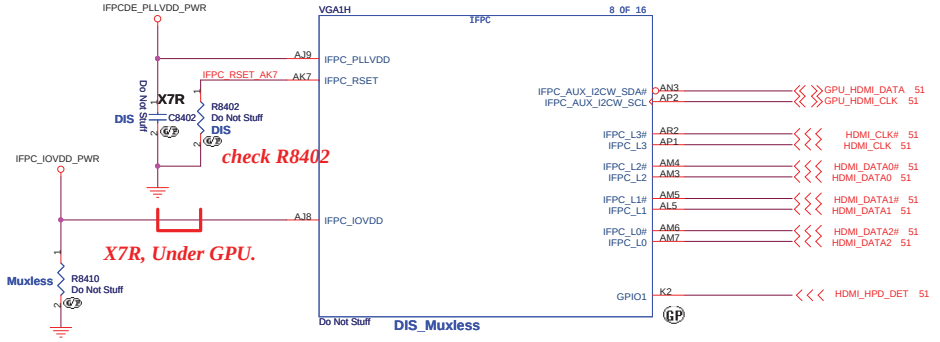
Title: GPU_PCIE/STRAPPING(1/5)

Size: A2 | Document Number: JE40-HR | Rev: -1

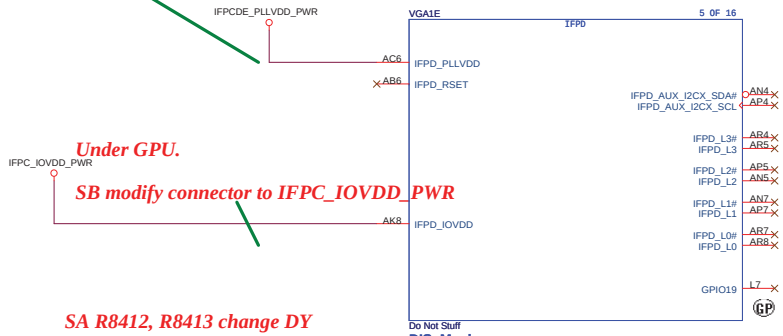
Date: Thursday, December 02, 2010 | Sheet 83 of 102

LVDS Interface





SB modify connector to IFPCDE_PLLVDD_PWR

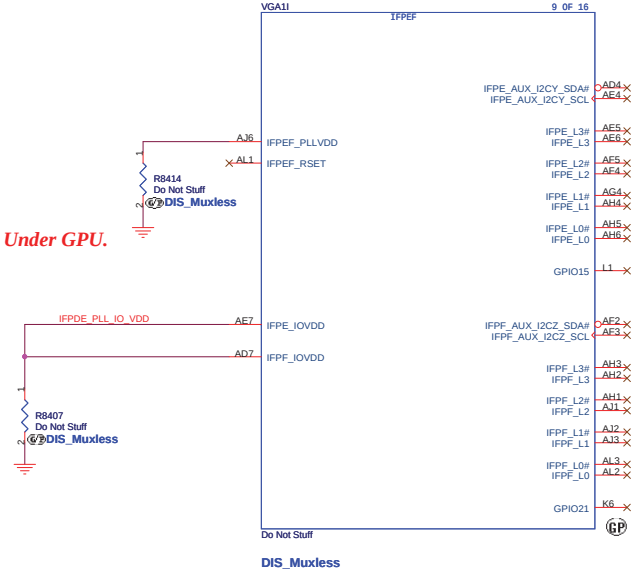


Under GPU.

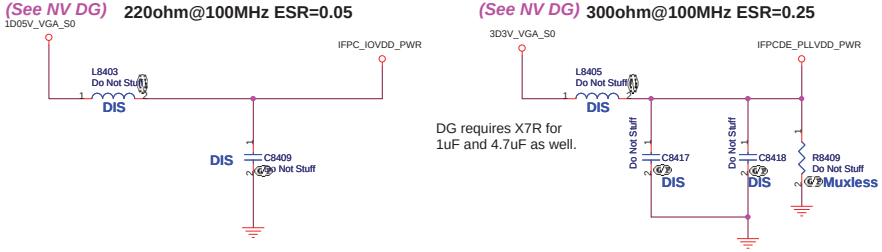
IFPC_IOVDD_PWR

SB modify connector to IFPC_IOVDD_PWR

SA R8412, R8413 change DY
SB R8412, R8413 change delete



HDMI Interface



HR UMA

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Title: GPU Memory(2/5)		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 84 of 102	

EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

Group A

Group B

HR UMA	
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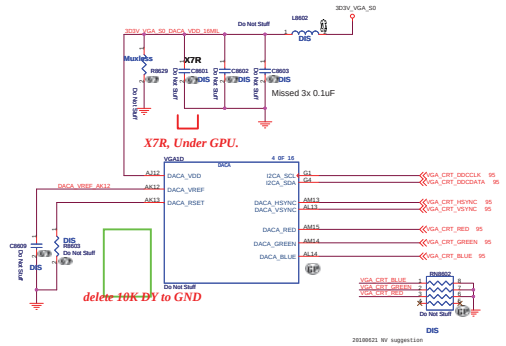
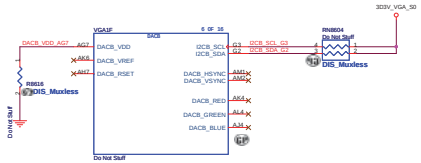
Title	GPU_DP/LVDS/CRT/GPIO(3/5)
Size: Custom	Document Number: JE40-HR
Rev	-1
Date: Thursday, December 02, 2010	Sheet 85 of 102

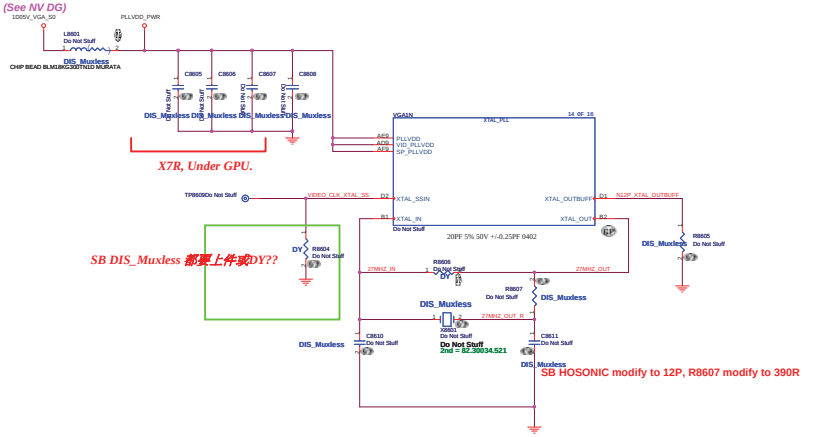
300ohm@100MHz ESR=0.25ohm

3.3V +/- 5%
120mA
(See NV DG)

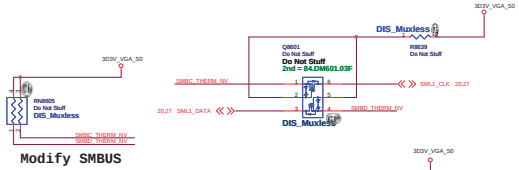


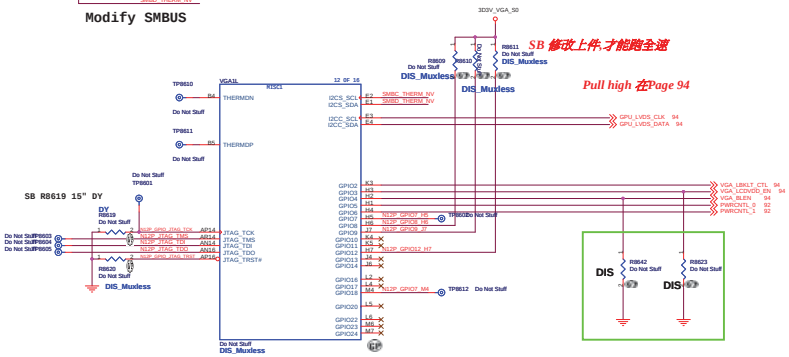


1.05V +/- 3%
150mA
(See NV DG)



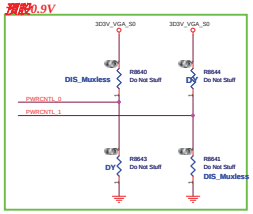
VGA Thermal sensor P2800





SJM50-CP SUPPORT							
P-STATE	NVVDD_ALTV1	NVVDD_ALTV0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1	N11P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.02V	1.02V	1.02V	0.95V	0.95V

預設0.9V



NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU_ROM_SI

```
for 1Gbit    for 2Gbit    for 1Gbit    for 2Gbit
Hynix VRAM   Hynix VRAM   Samsung VRAM Samsung VRAM
RAM_CFG[0]=0 RAM_CFG[0]=0 RAM_CFG[0]=1 RAM_CFG[0]=1
RAM_CFG[1]=1 RAM_CFG[1]=1 RAM_CFG[1]=1 RAM_CFG[1]=1
RAM_CFG[2]=0 RAM_CFG[2]=1 RAM_CFG[2]=0 RAM_CFG[2]=1
RAM_CFG[3]=0 RAM_CFG[3]=0 RAM_CFG[3]=0 RAM_CFG[3]=0
```

GPU_ROM_SO

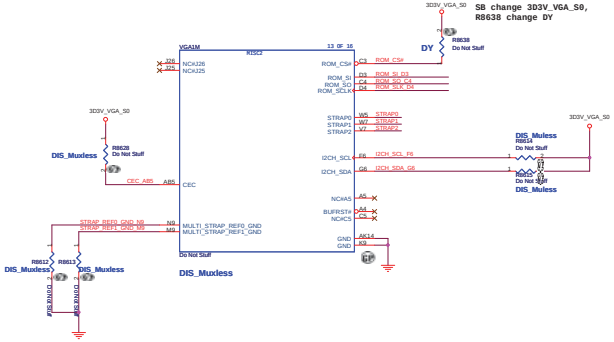
```
VGA_DEVICE   =1 (low bit)
SMB_ALT_ADDR =0
FB_0_BAR_SIZE =0
XCLK_417     =0 (High bit)
```

GPU_ROM_SCLK

```
PEX_PLL_EN_TERM =0
SLOT_CLK_CFG    =1
SUB_VENDOR      =0
PCI_DEVID[4]    =1
```

N11P Fermi QS 1

```
Logical Strap Bit Mapping
Resistor  Pull-up Pull-down
5Kohms    1000    0000
10Kohms   1001    0001
15Kohms   1010    0010
20Kohms   1011    0011
25Kohms   1100    0100
30Kohms   1101    0101
35Kohms   1110    0110
45Kohms   1111    0111
```



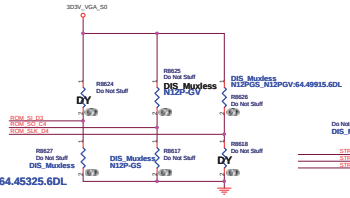


TABLE NVIDIA

71.0N12P.E0U

-1 modify N12P GV setting
71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL

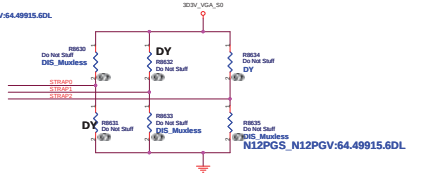
STRAP0 USER[0]=1 USER[1]=1 USER[2]=1 USER[3]=1 — N12P-GS — N12P-GV — N11P-GE Pull Low — N11P-GS Pull Low — N12P-GE

USE 1111 (45K)

STRAP1 3GIO_PADCFG[0]=0 3GIO_PADCFG[1]=1 3GIO_PADCFG[2]=1 3GIO_PADCFG[3]=1

USE 0110 (35K)

STRAP2
PCI_DEVID[0]=1 N12P-GS GF108-730-A1 0x0DF4 (0X4) (0100)
PCI_DEVID[1]=0 N12P-GV1 GF108-705-A1 0x0DF7 (0X7) (0111)
PCI_DEVID[2]=0 N11P-GS Fermi 0x0DF0 (0000)
PCI_DEVID[3]=0 N11P-GE Fermi 0x0DF1 (0001)



鮮創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU_POWER(4/5)
Size: A1 | Document Number: JE40-HR | Rev: -1
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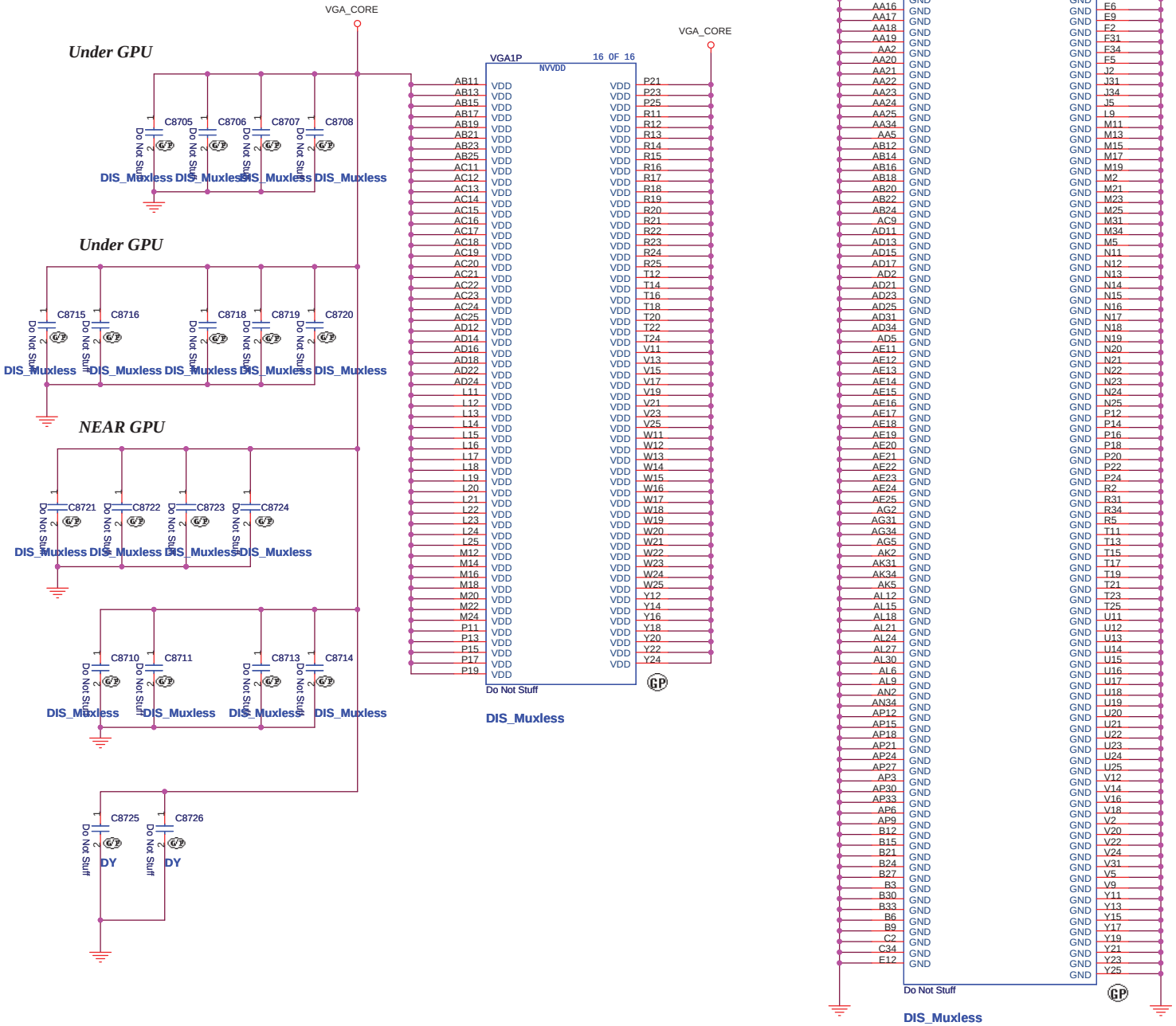
EDP 50A
(TDP 37W)



HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU_DPPWR/GND(5/5)***

Size	Document Number	Rev
A3	**JE40-HR**	-1

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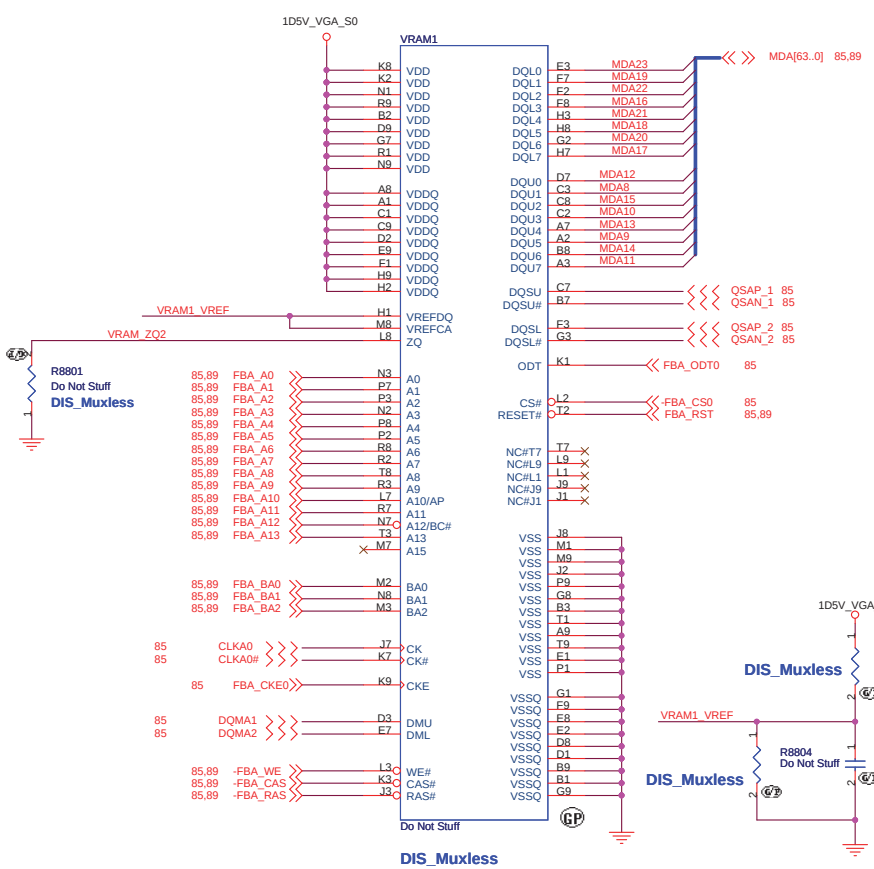
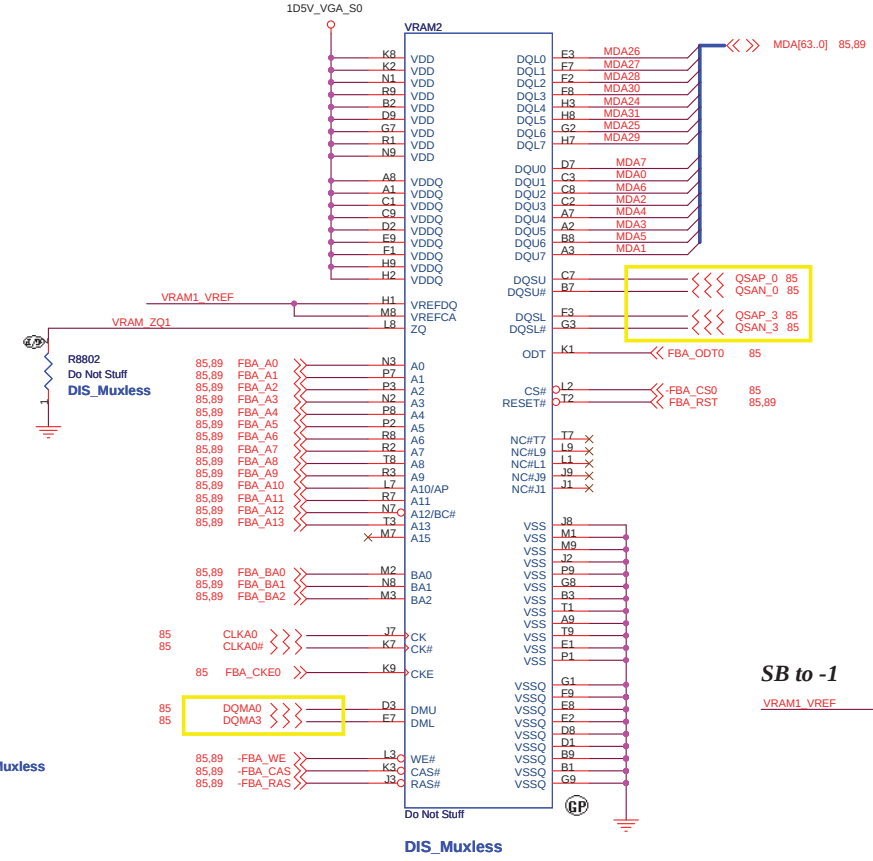


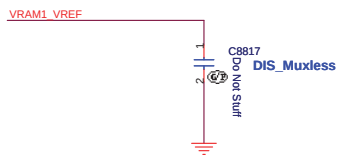
VRAM = N12PGS_N12PGV



VRAM = N12PGS_N12PGV

FB CMD mapping Mode D-N12x

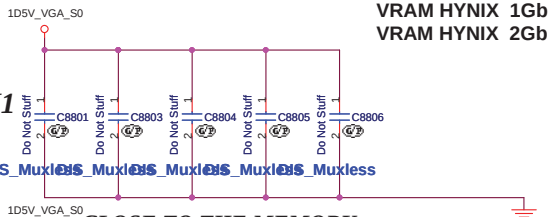
SB to -1



VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001

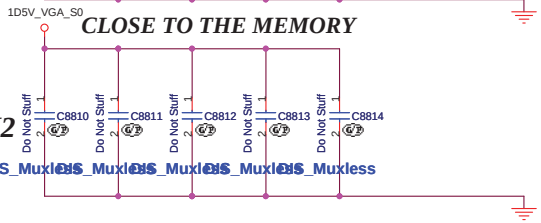
DG requires 4x0.1uF and 8x1.0uF per VRAM chip

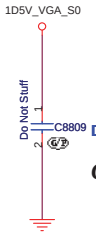
FOR VRAM1



CLOSE TO THE MEMORY

FOR VRAM2





CLOSE TO THE MEMORY

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GPU-VRAM1,2 (1/4)***

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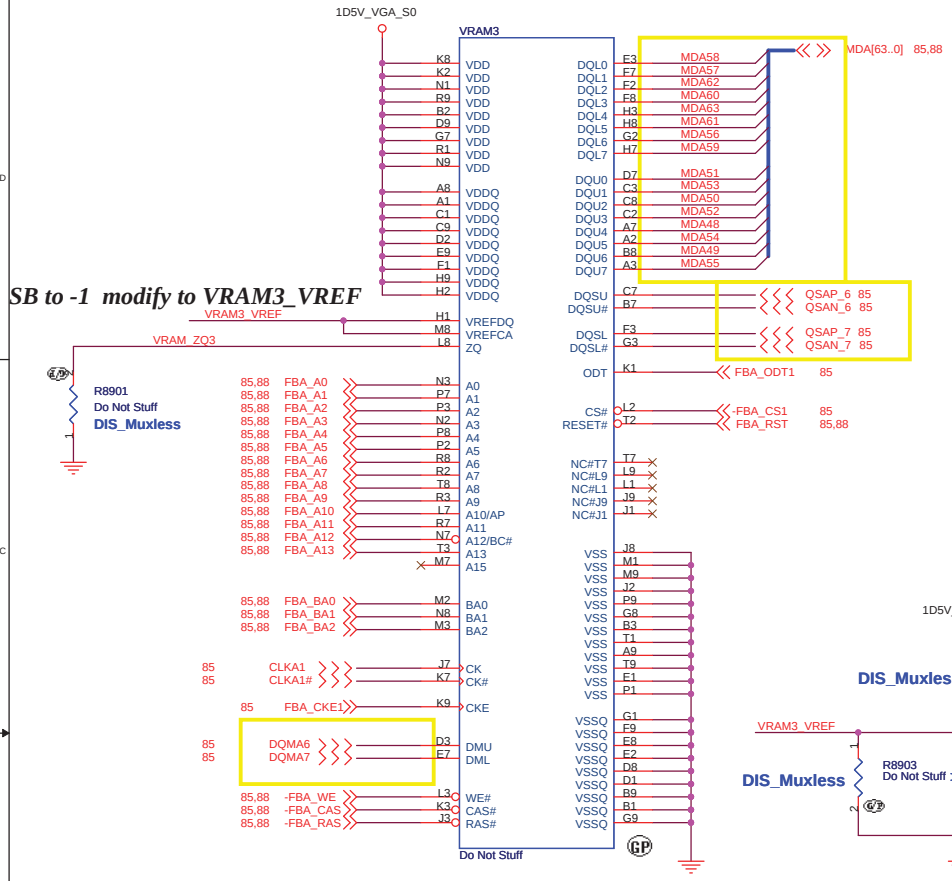
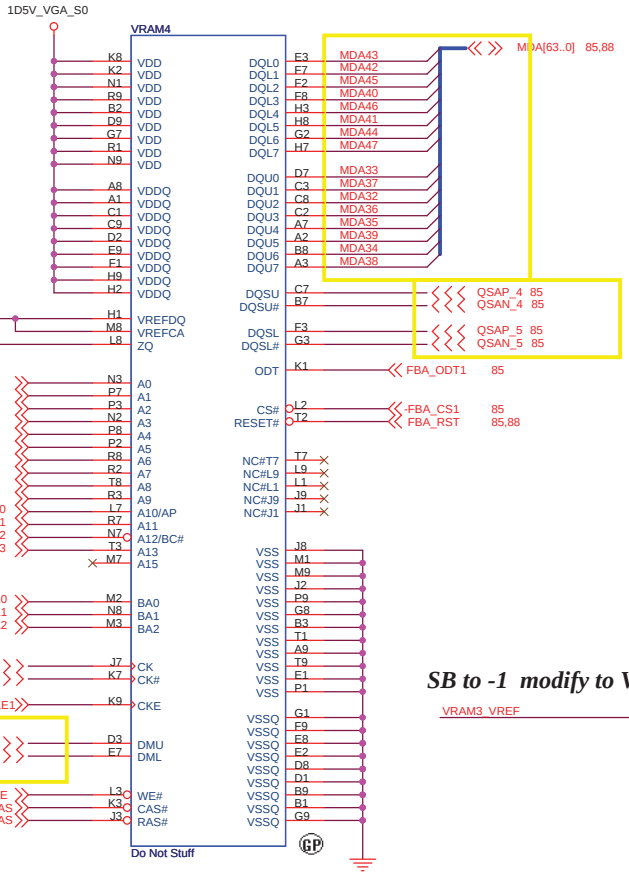
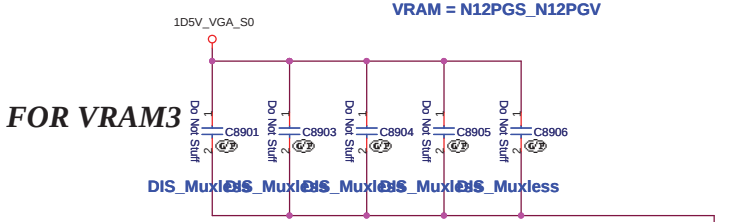
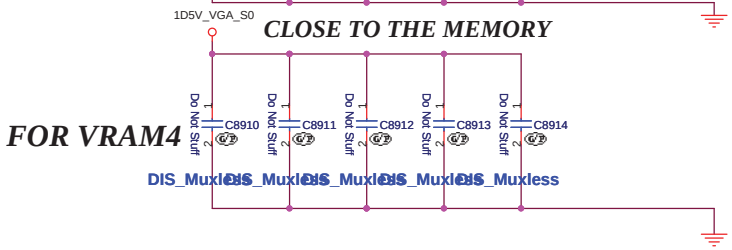


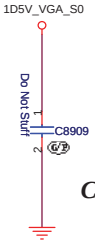


FB CMD mapping Mode D-N12x

VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001







HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: JE40-HR | Rev: -1

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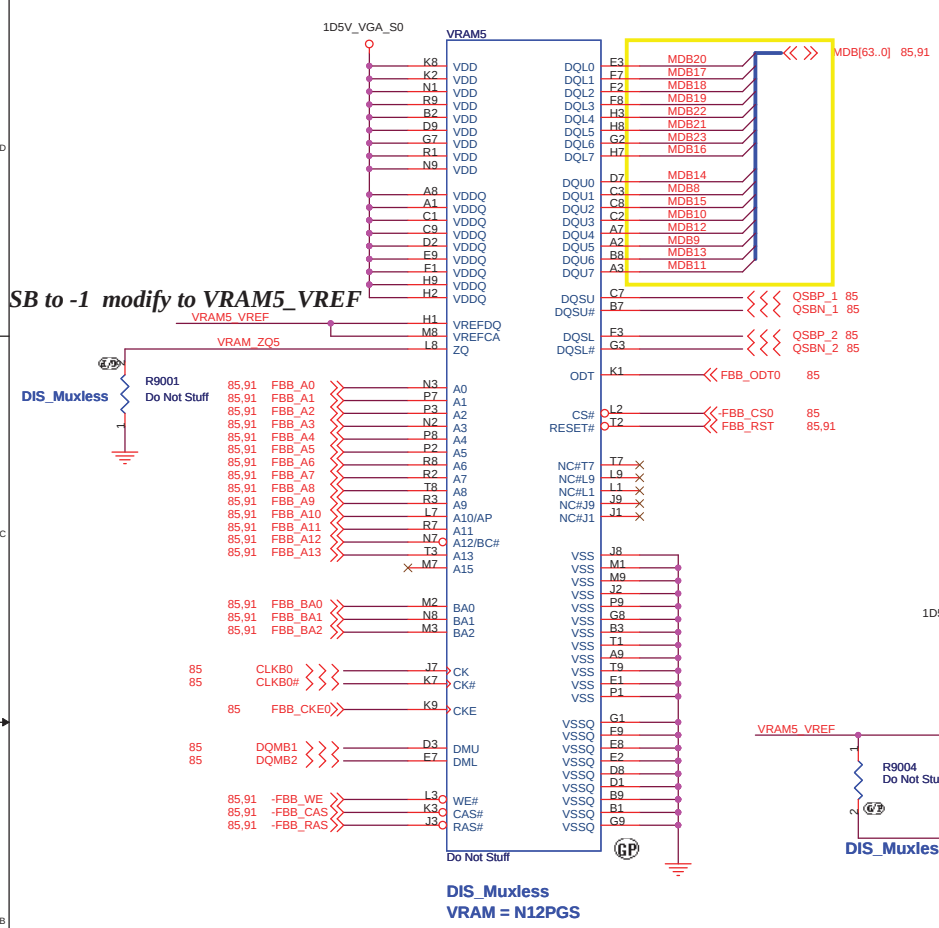
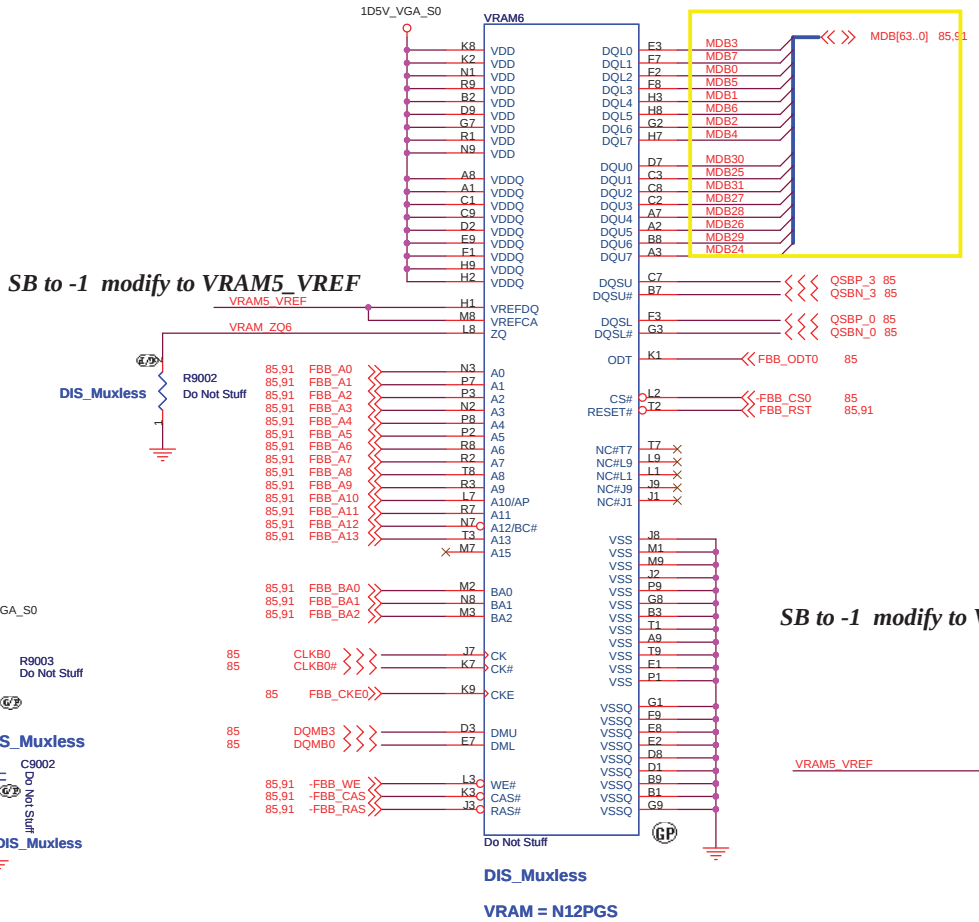
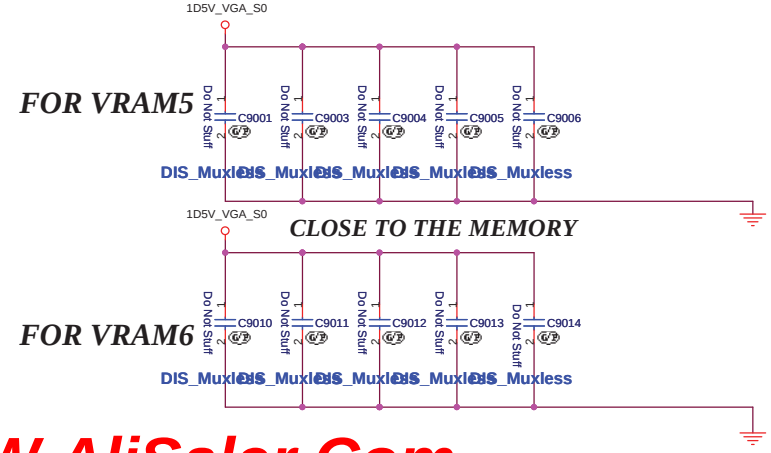
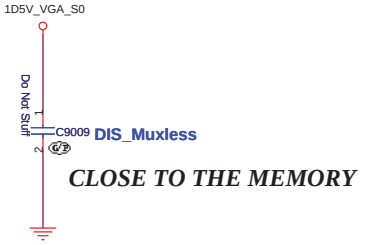




VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



DG requires 4x0.1uF and 8x1.0uF per VRAM chip



HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size	Document Number	Rev
Custom	JE40-HR	-1

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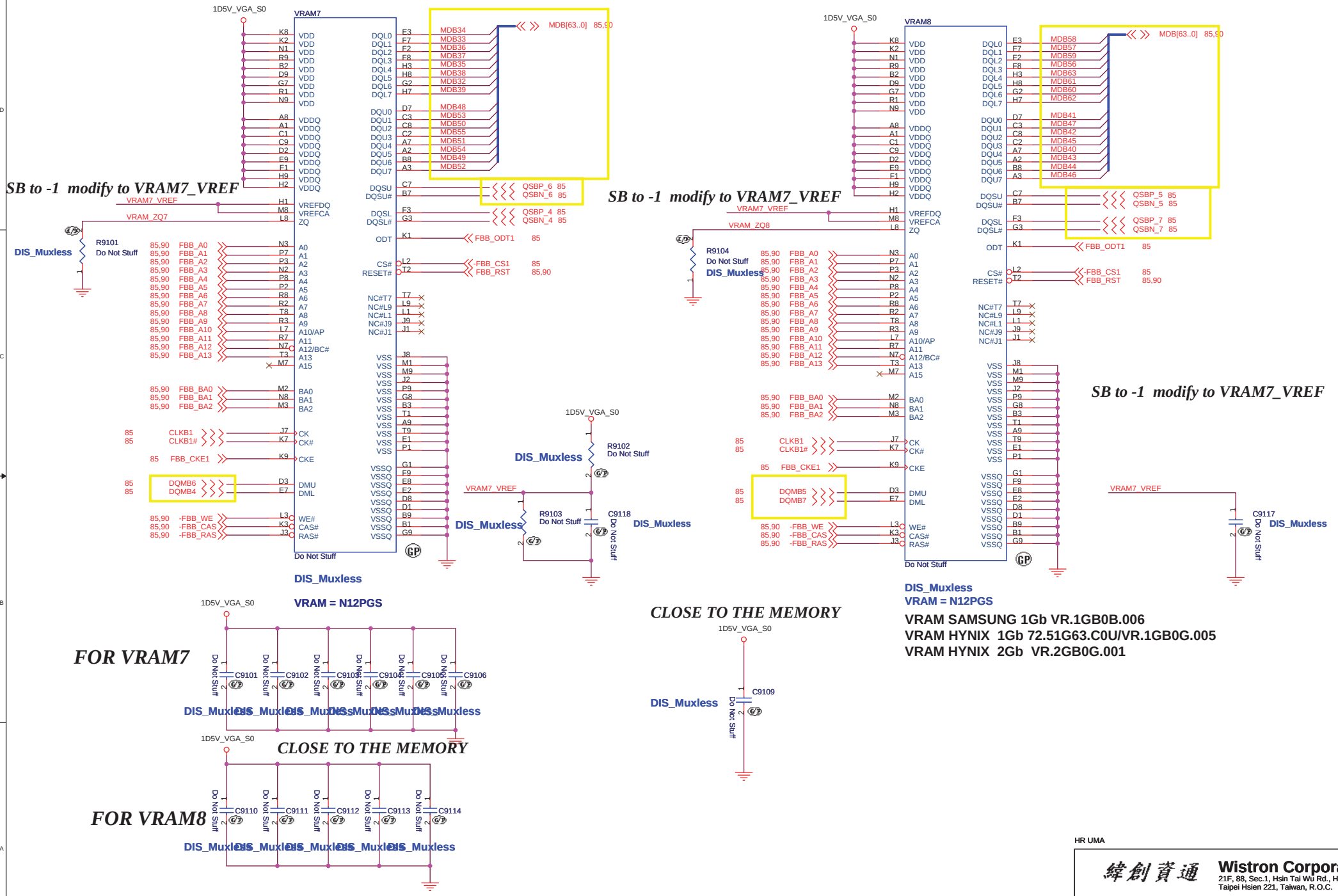

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU-VRAM7,8 (4/4)		
Size: Custom	Document Number: JE40-HR	Rev: -1
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20100715

SSID = PWR.Plane.Regulator_GFX

20100719

SB 20100831

SB 20100831

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

SB to -1 modify PR9213 VGA_Core to 1.05V

Vout=0.75V*(R1+R2)/R2

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

HR UMA

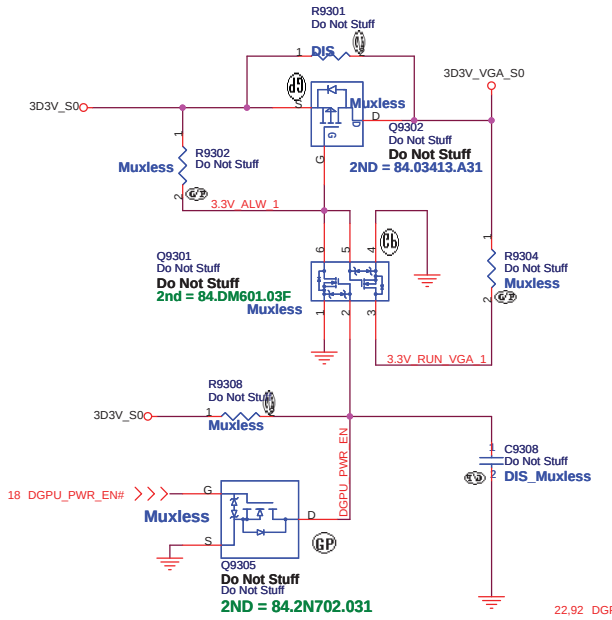
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B_+VGA_CORE

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 92 of 102

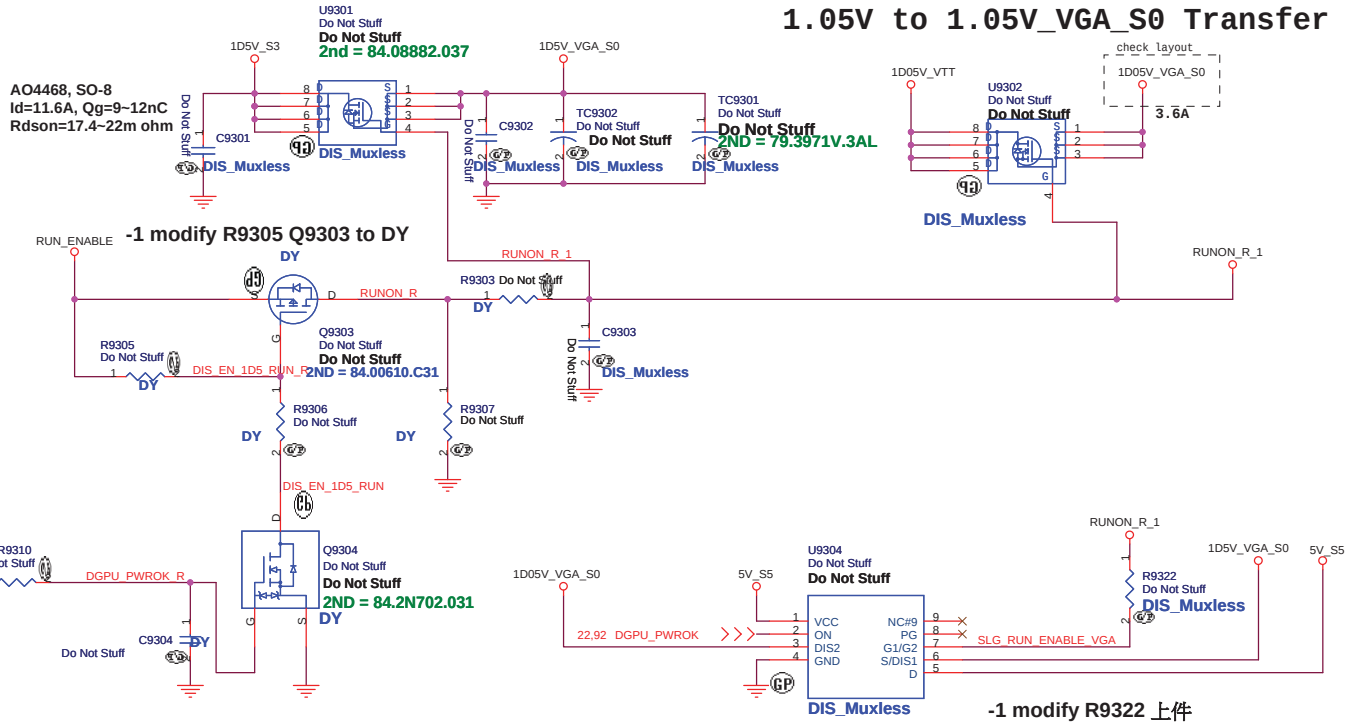
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

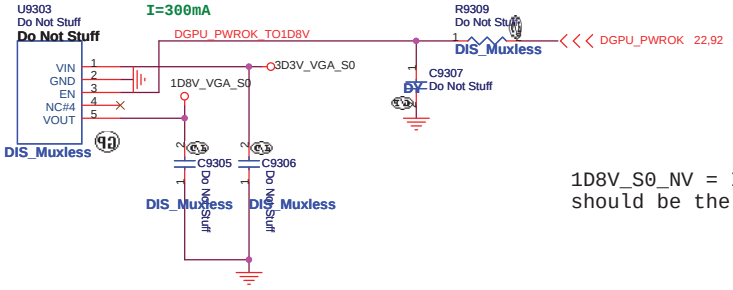
SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer



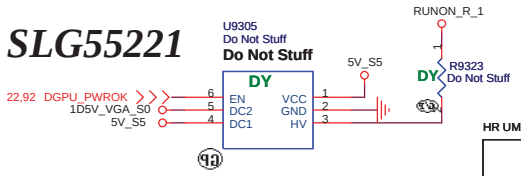
RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

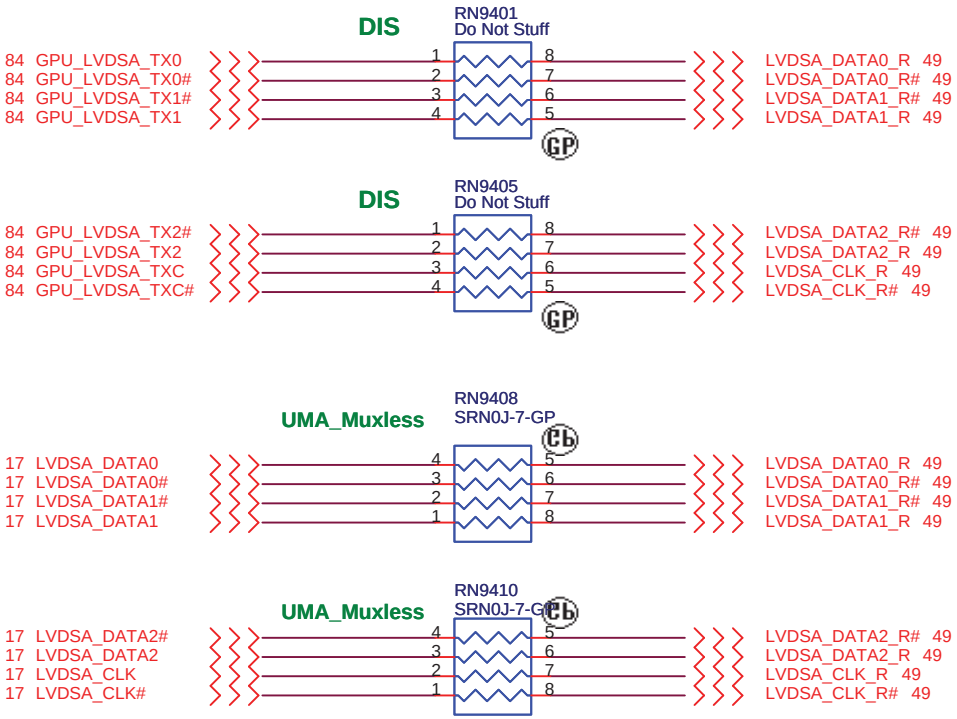
-1 co-layout SLG55221



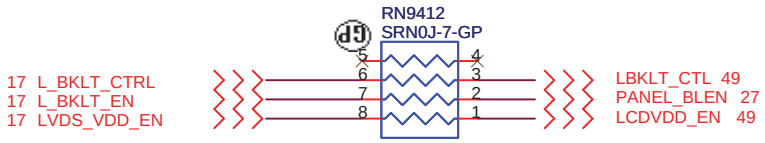
HR UMA

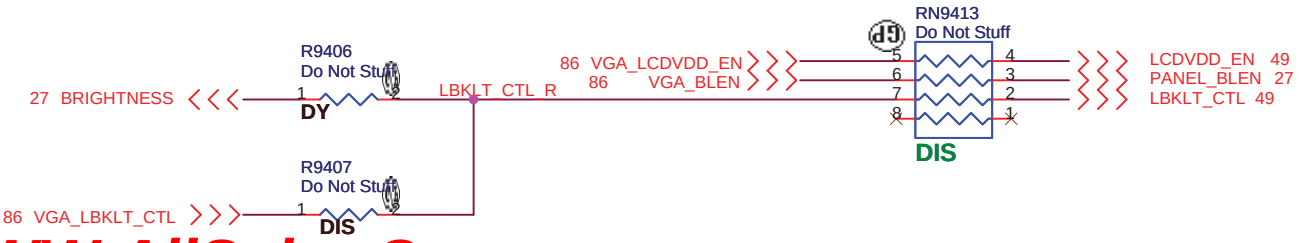
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DISCRETE VGA POWER		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 93 of 102	

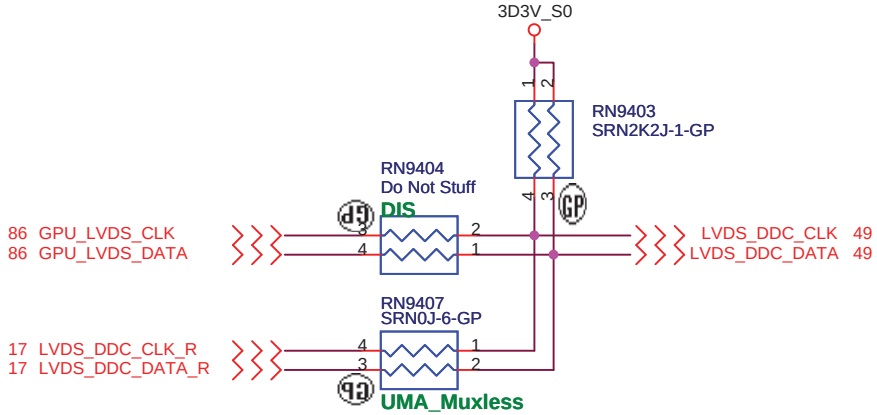
LVDS Channel A



Panel BL brightness/Power En/BL En



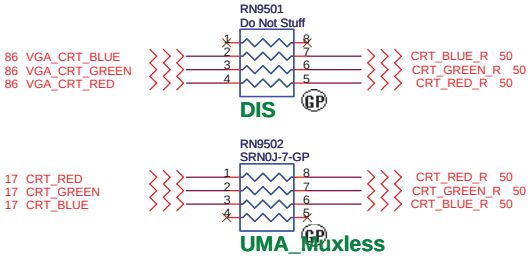




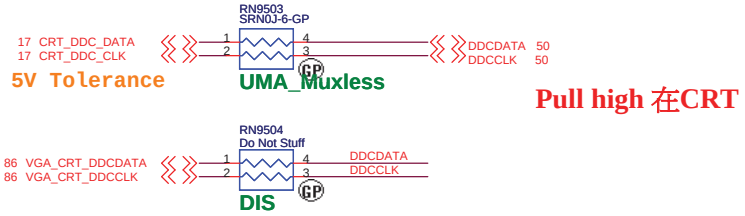
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LVDS_Switch*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 94 of 102	

Close to CRT Board CONN

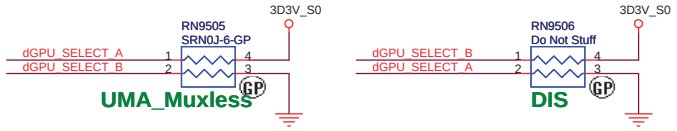


CRT DDCDATA & DDCCLK



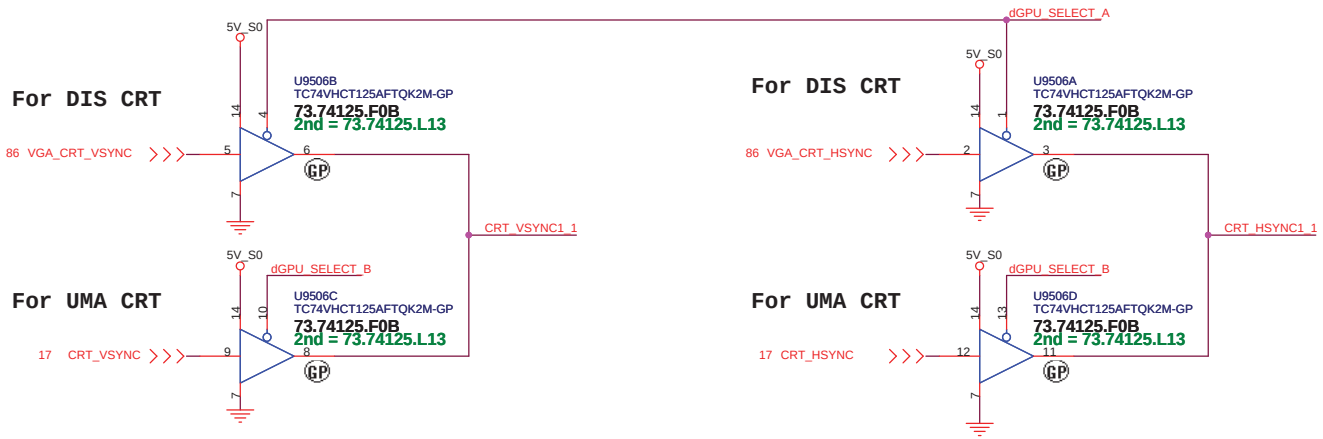
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA



SB to -1 modify R9503,R9504 to 10 ohm

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Switch

Size: A3 | Document Number: JE40-HR | Rev: -1

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SSID = SDIO

HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TOUCH PANEL

Size	Document Number	Rev
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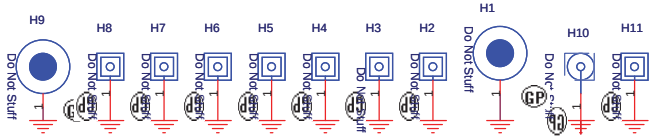
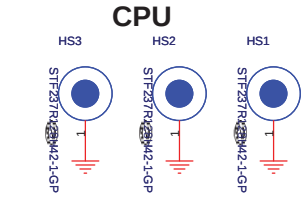
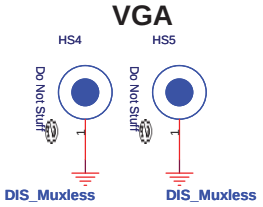
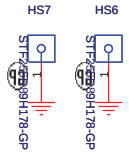
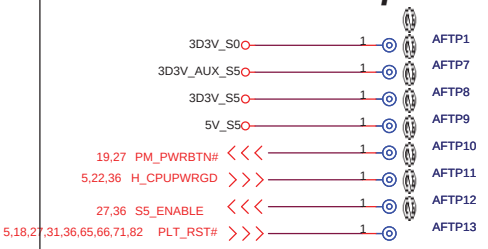








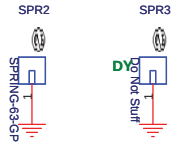
3G Sku



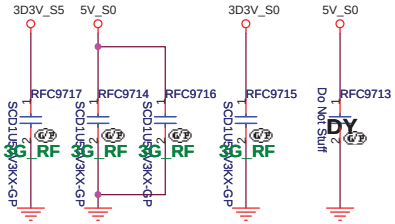
Test Point放在Dimm Door打開可量測處

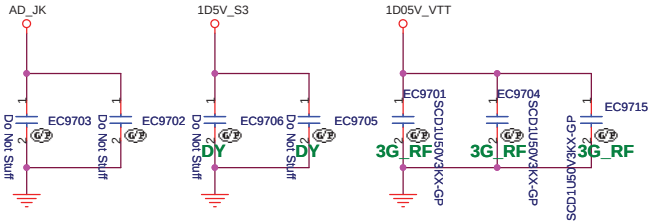
SB to -1 BOM add SPR2

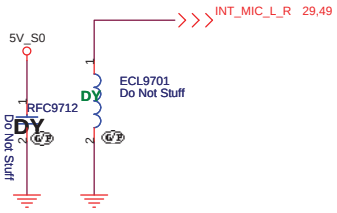
-2 delete SPR5

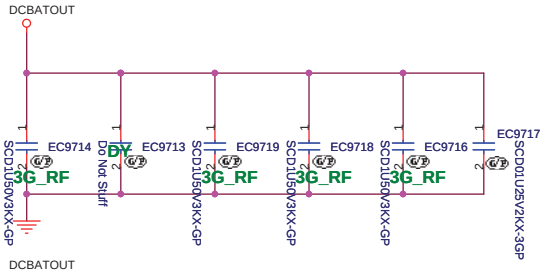


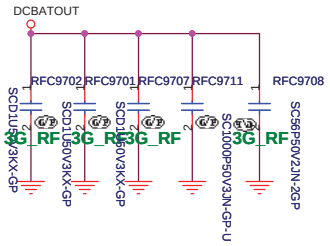
Change:34.40V16.001

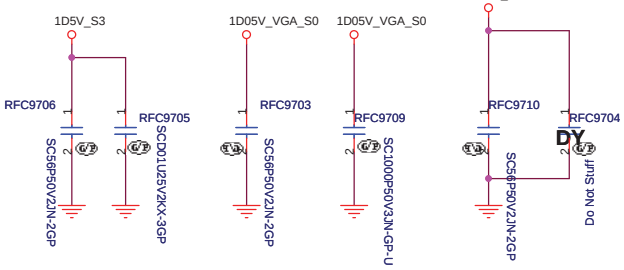


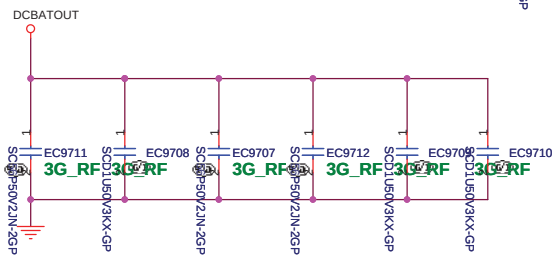












HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
A3	JE40-HR	-1

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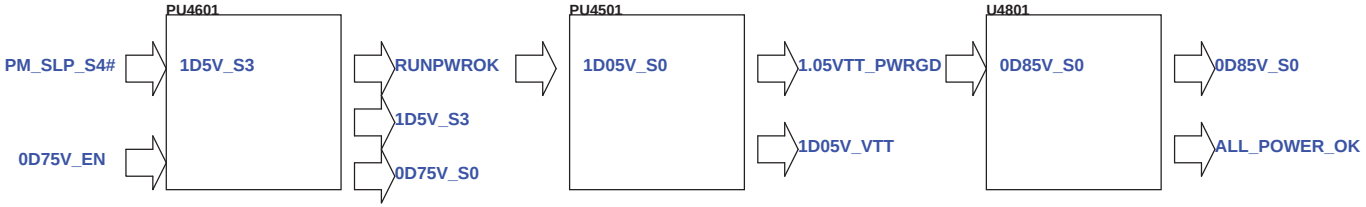
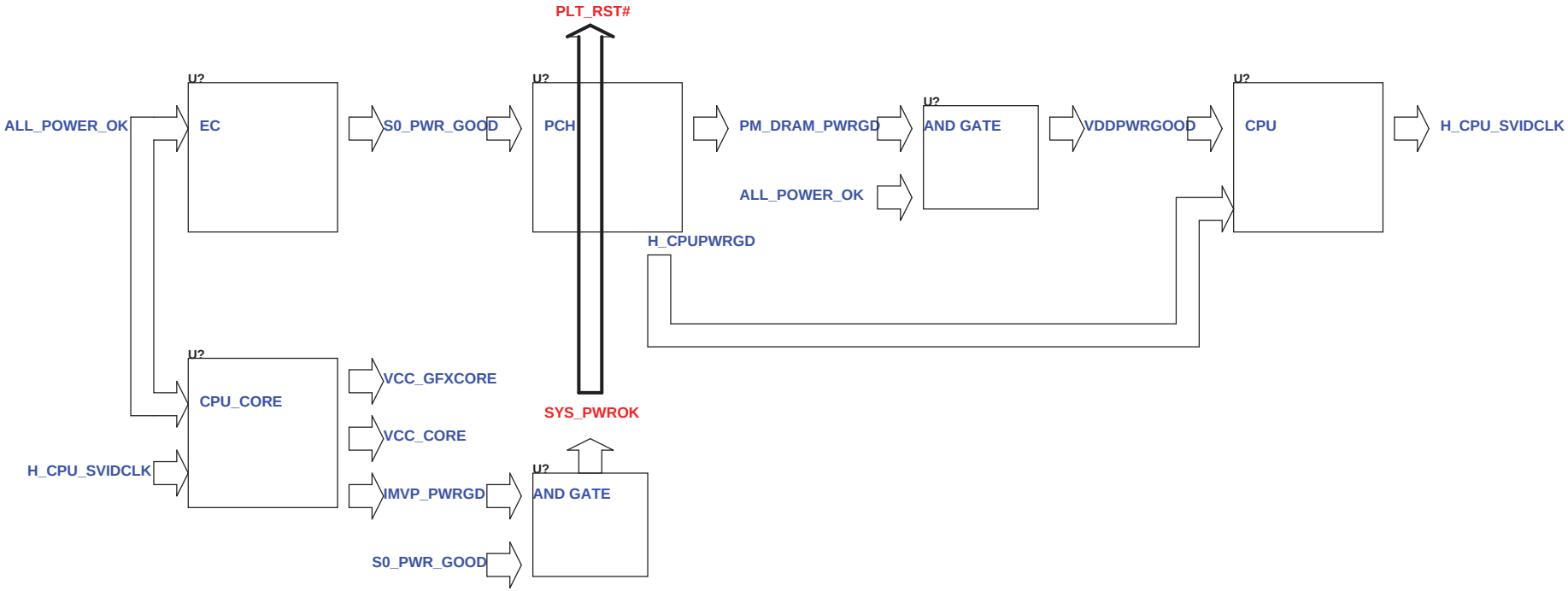
Power Sequence





HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

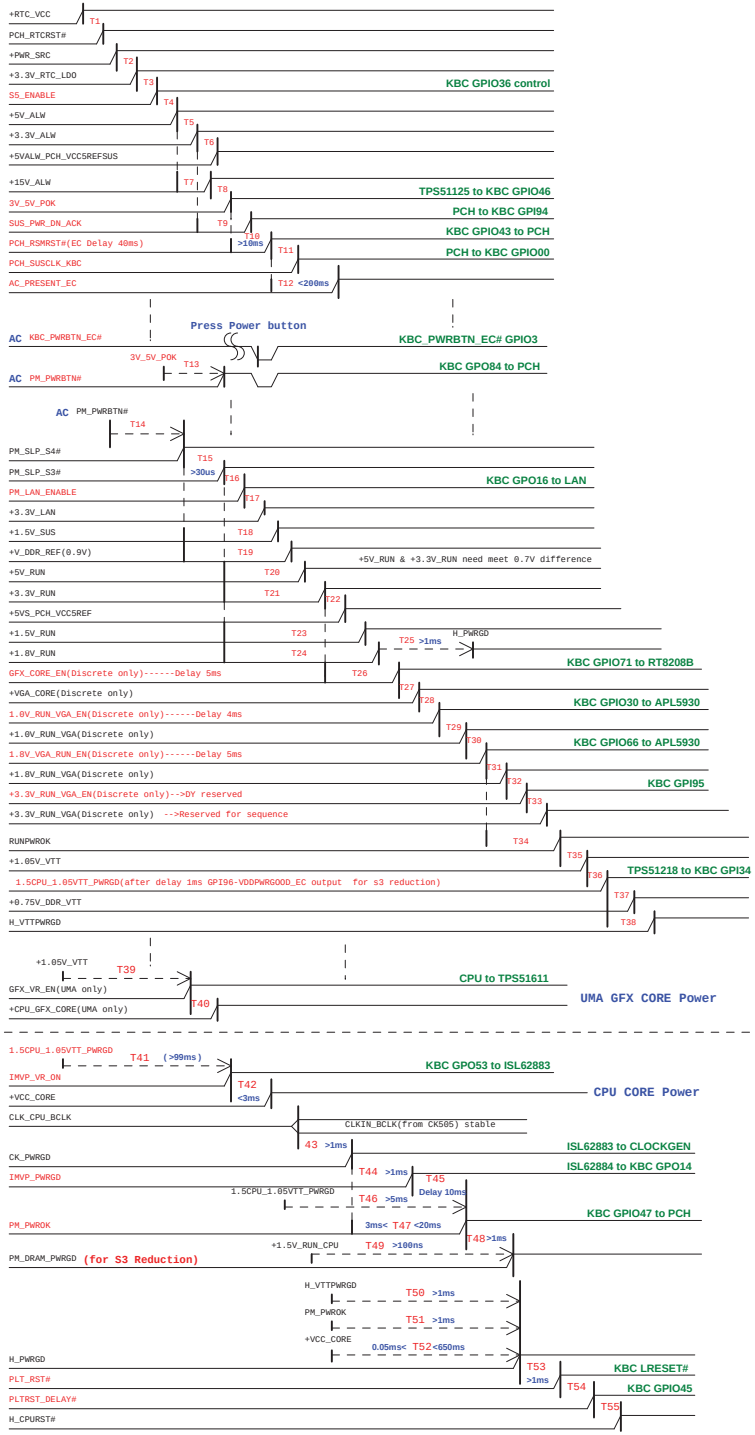
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 98 of 102

Intel-Power Up Sequence

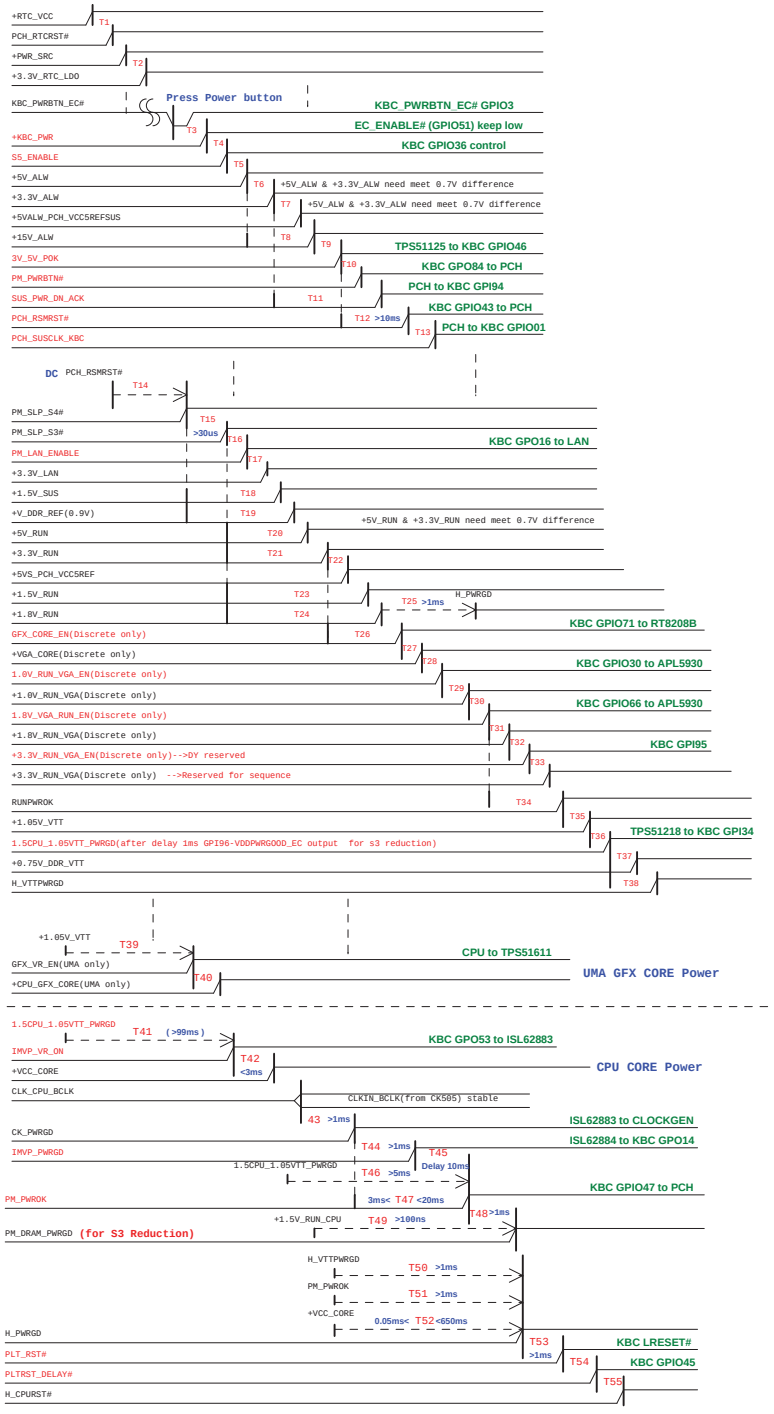
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



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2SF, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

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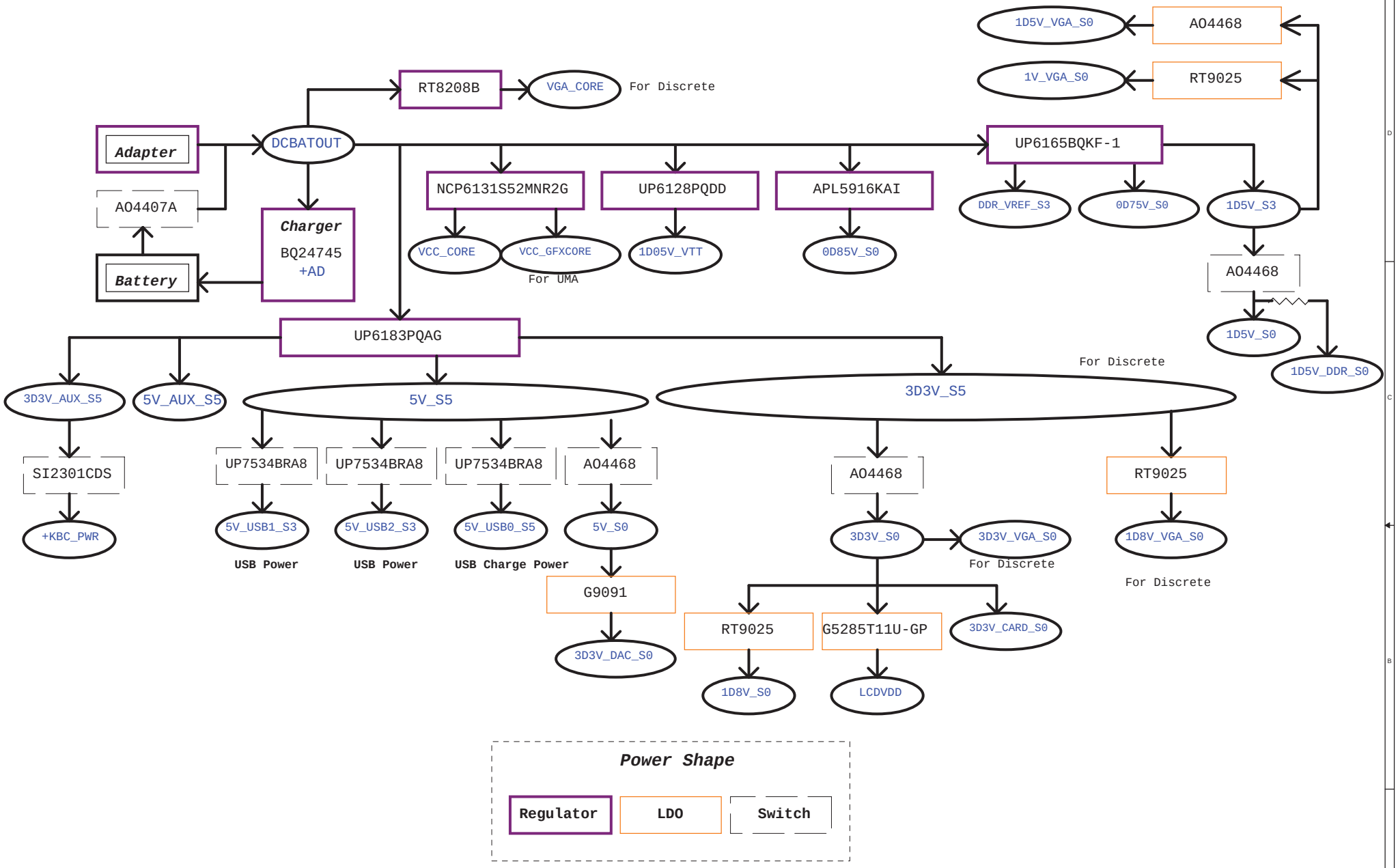
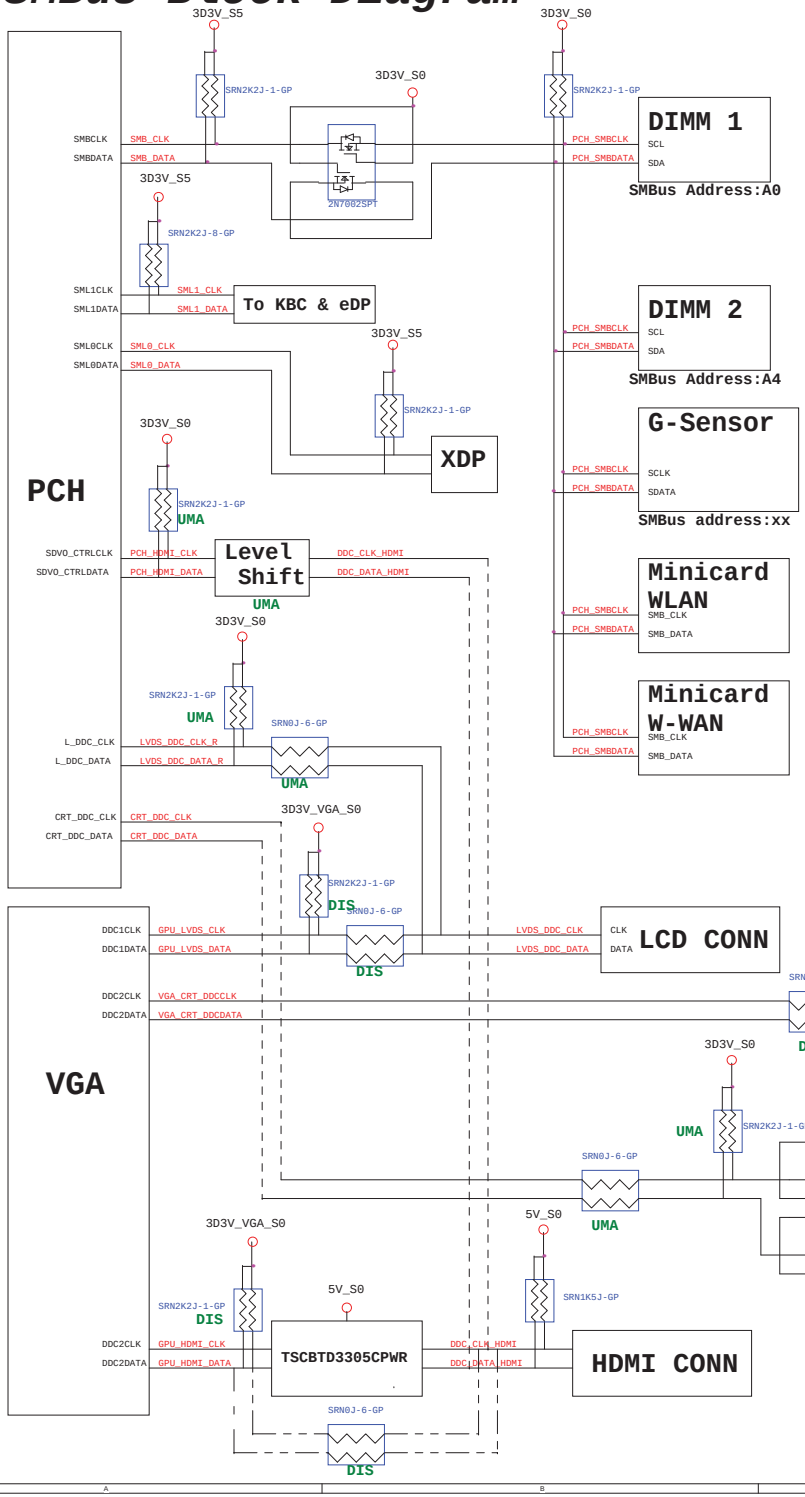


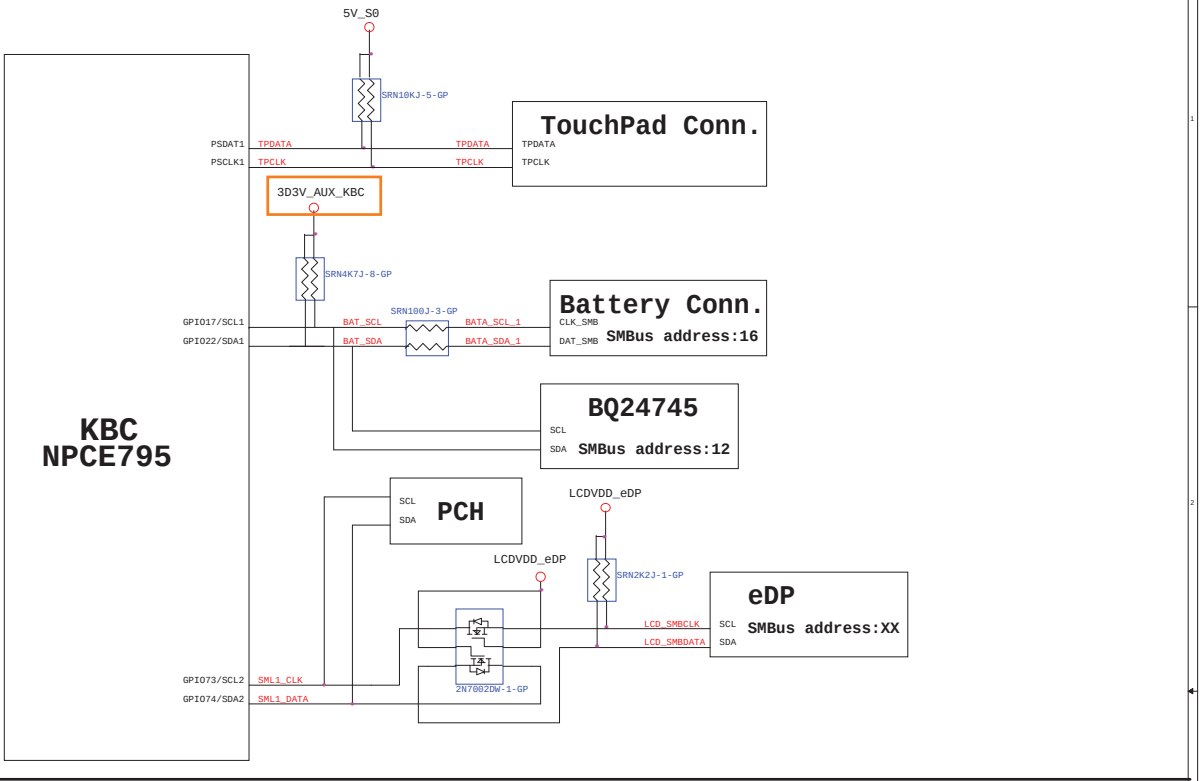
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Power Block Diagram		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 100 of 102	

PCH SMBus Block Diagram



KBC SMBus Block Diagram



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

Size	Document Number	Rev
A2	JE40-HR	-1

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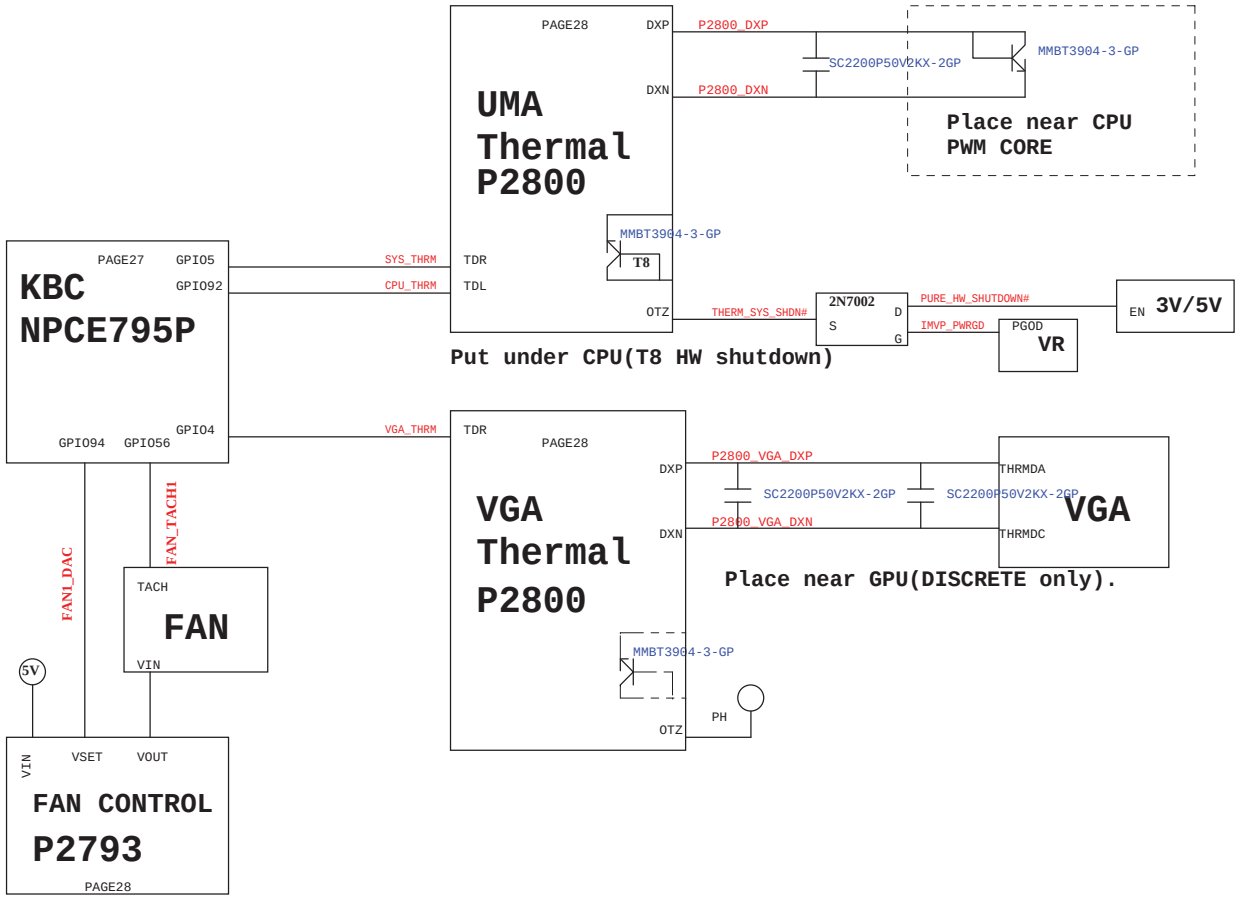
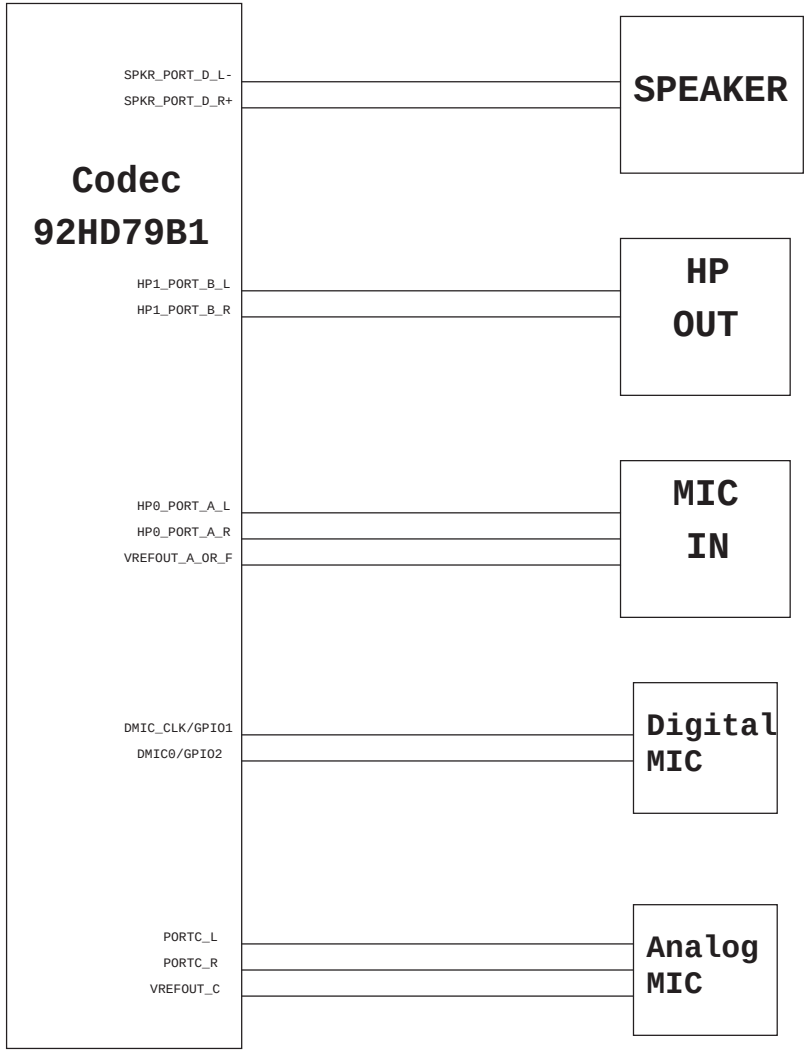
Thermal Block Diagram



Audio Block Diagram



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
Custom	JE40-HR	-1

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