

Enrico/Caruso 15" UMA Schematics Document

Sandy Bridge

Intel PCH

2011-06-02

REV : A00



DV15 HR Vos GIGA HDMI NoSurge



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

Enrico/Caruso 15 HR

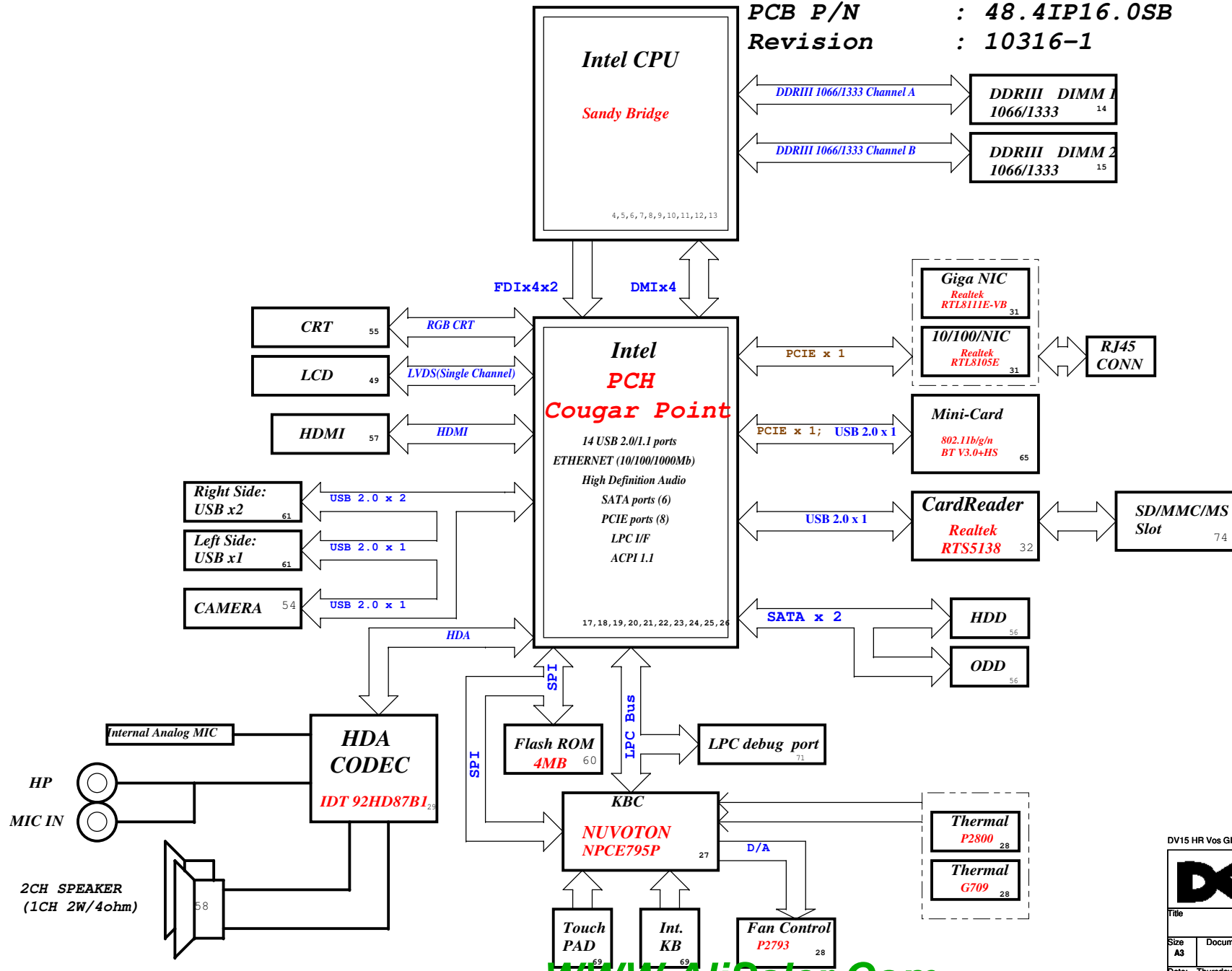
Rev
X01

Date: Thursday, June 02, 2011

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DV15 Huron River UMA Block Diagram

Project code : 91.4IP01.001
PCB P/N : 48.4IP16.0SB
Revision : 10316-1



SYSTEM DC/DC	
TPS51461	48
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0
CPU DC/DC	
ISL95831HRTZ	42~44
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
GFX DC/DC	
ISL95831HRTZ	44
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE
SYSTEM DC/DC	
TPS51218	45
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
TPS51123RGER	41
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5
SYSTEM DC/DC	
TPS51216RUKR	46
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3
MAXIM CHARGER	
BQ24707	40
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT
SYSTEM DC/DC	
TPS51311RGTR	47
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0
PCB LAYER	
L1: Top	L4: Signal
L2: GND	L5: VCC
L3: Signal	L6: Bottom

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Block Diagram		
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Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

Pair	Device
0	X
1	USB Ext. port 1
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	x
11	Mini Card1 (WLAN)
12	CAMERA
13	X

PCIE Routing

LANE1	X
LANE2	Onboard LAN
LANE3	x
LANE4	Mini Card1 (WLAN)
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	X
2	X
3	X
4	ODD1
5	X

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-12.6V 9V-19V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_RBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) MINI				PCH_SMBDATA/PCH_SMBCL PCH_SMBDATA/PCH_SMBCL PCH_SMBDATA/PCH_SMBCL PCH_SMBDATA/PCH_SMBCL

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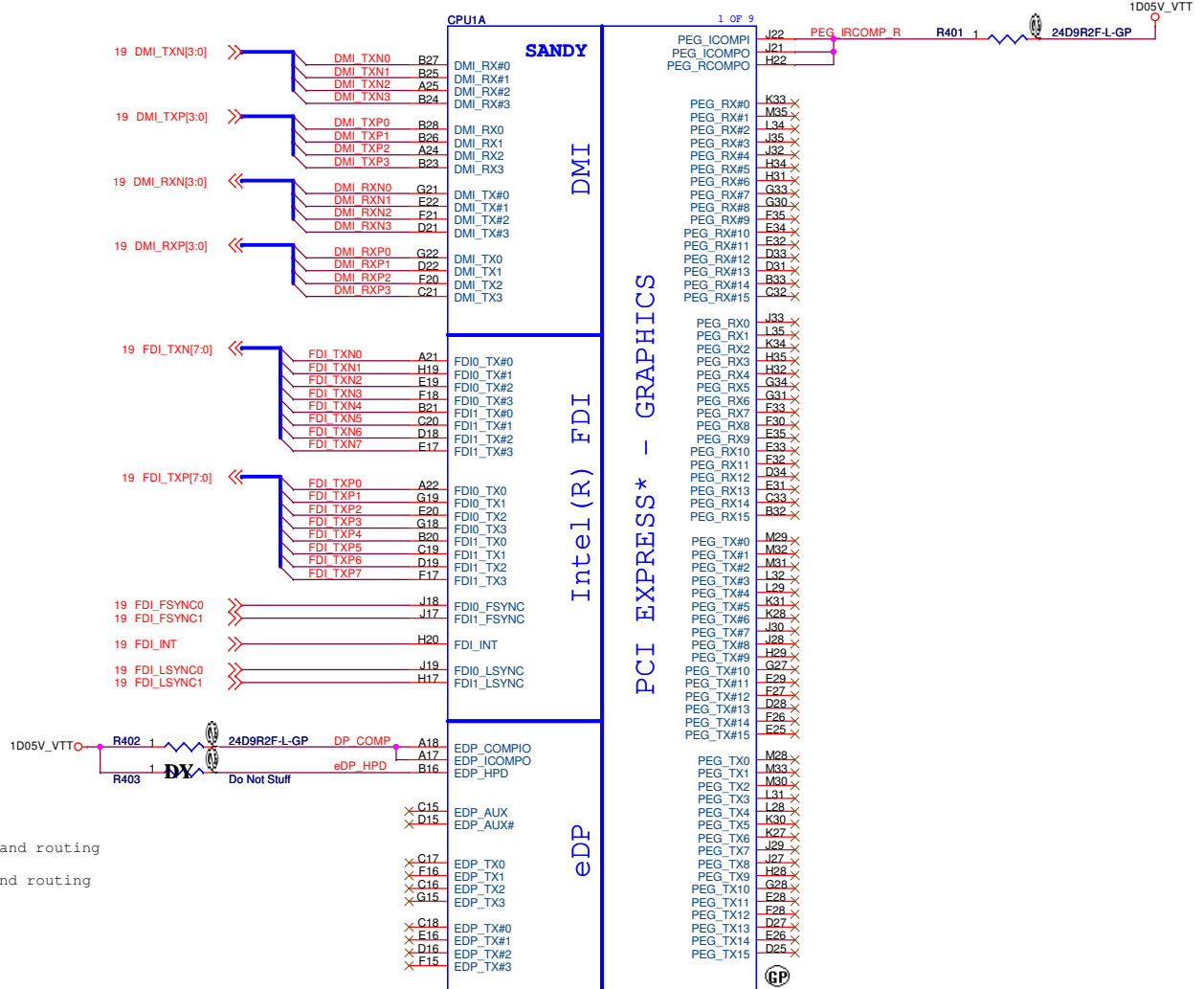
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SSID = CPU

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Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils..
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils..
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

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2nd = 62.10040.771

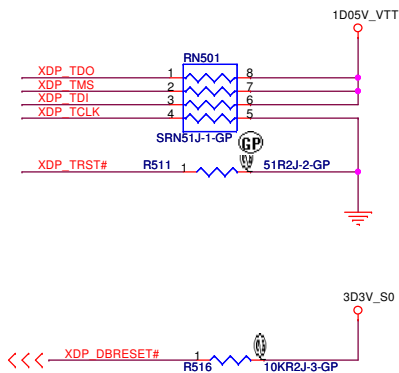
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DELL

File: CPU (PCIE/DMI/FDI)
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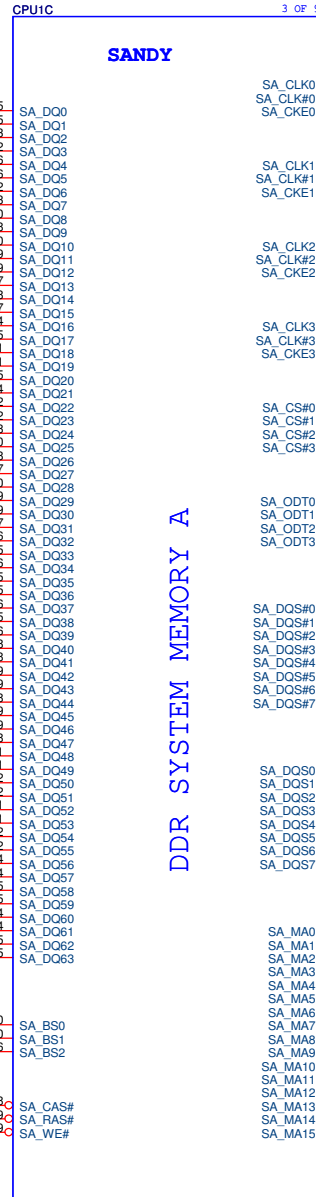
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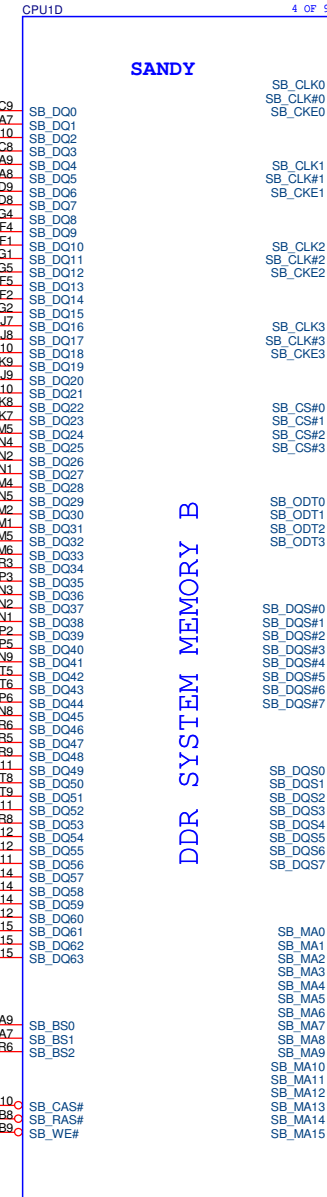
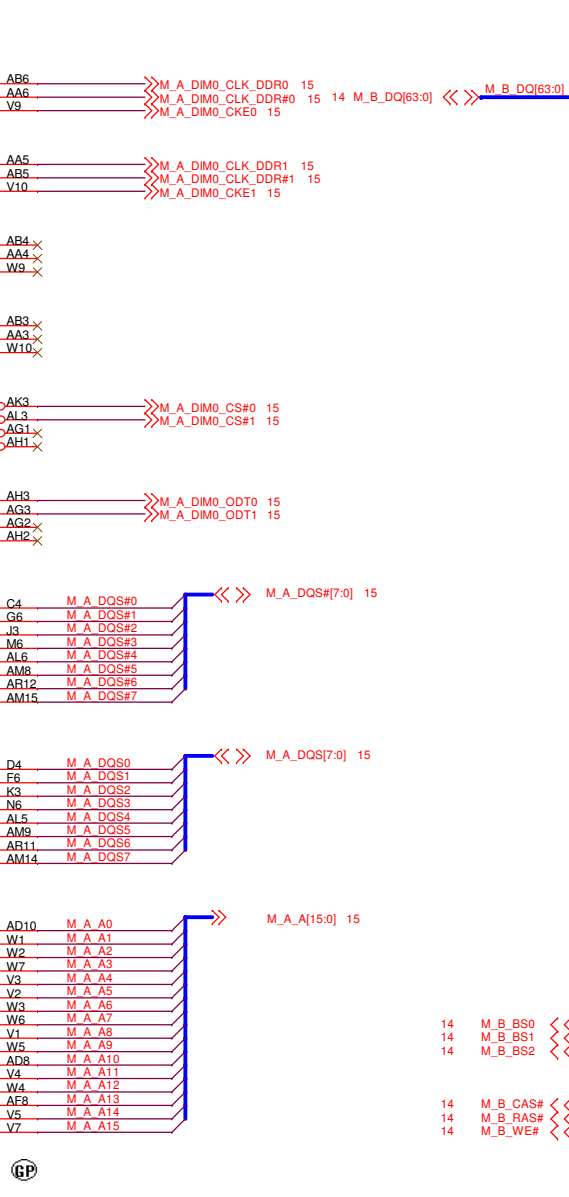


SSID = CPU

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62.10040.821
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62.10040.821
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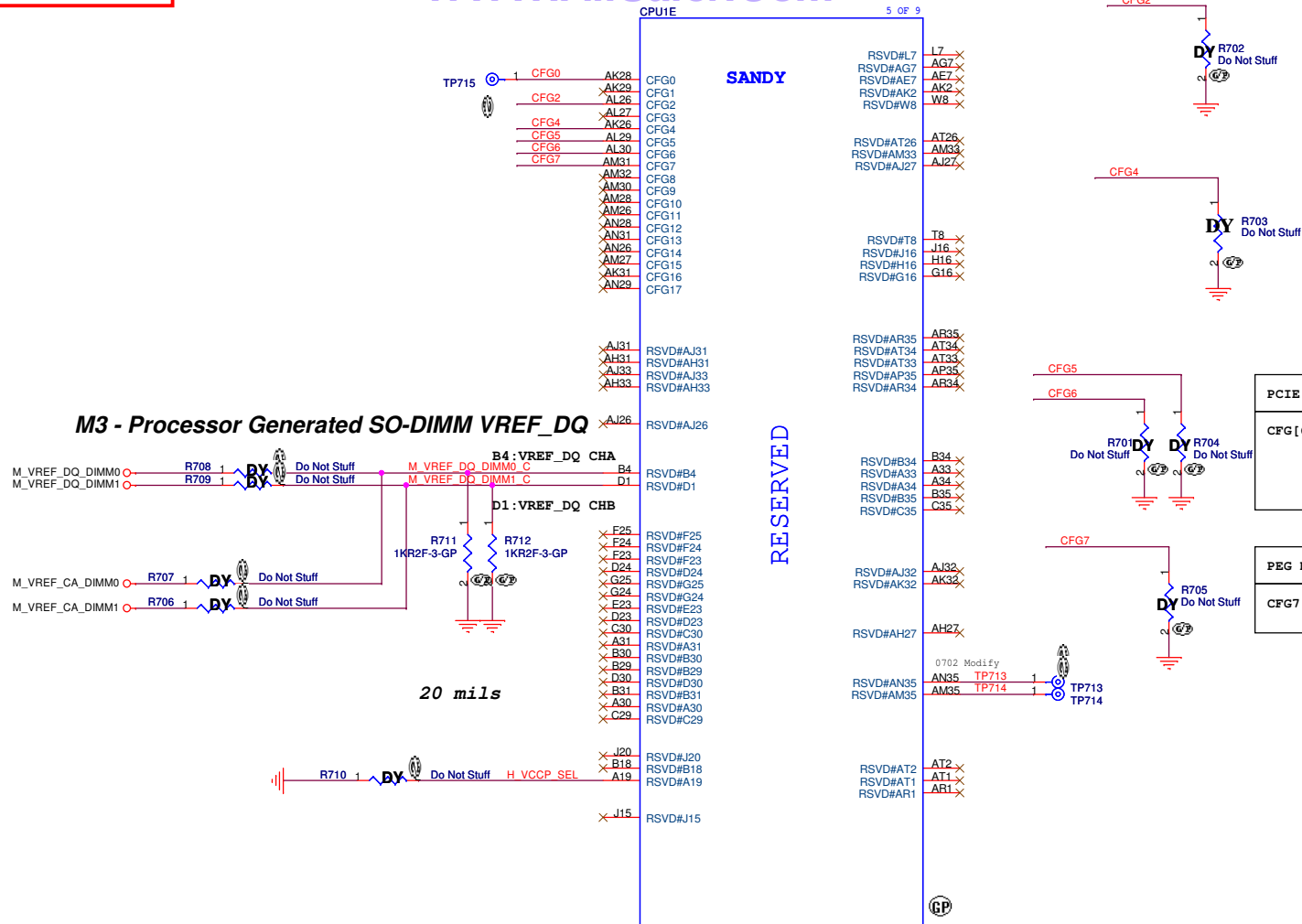
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SSID = CPU

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PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

SKT-BGA989C468393H184-NF
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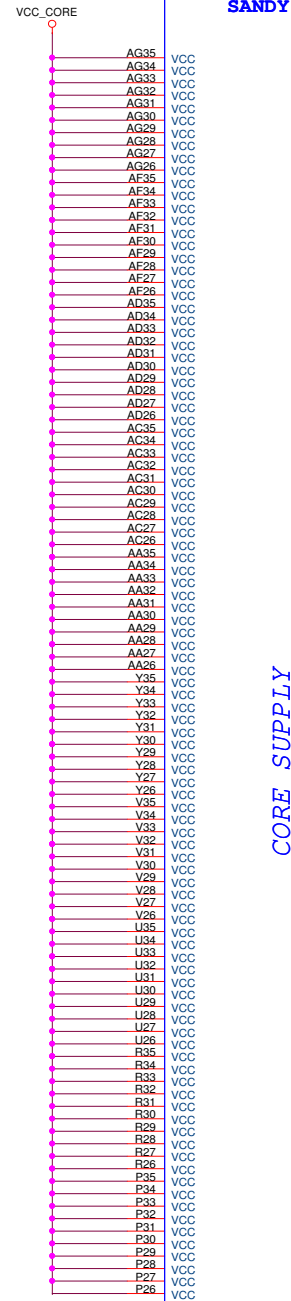
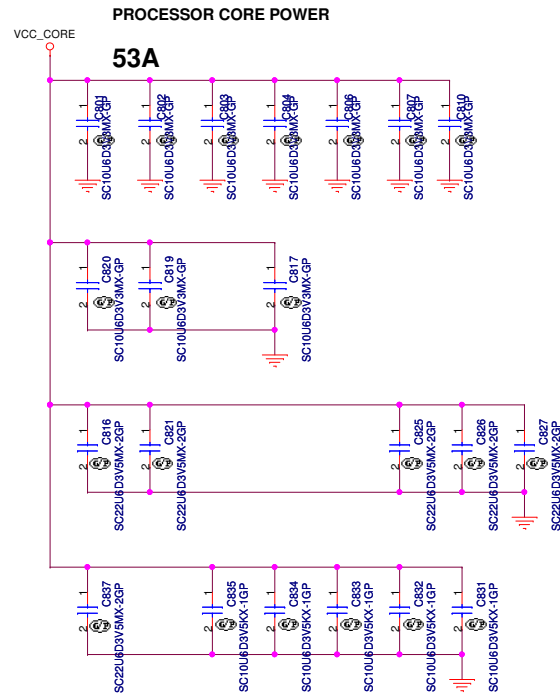
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SSID = CPU

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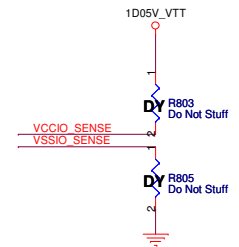
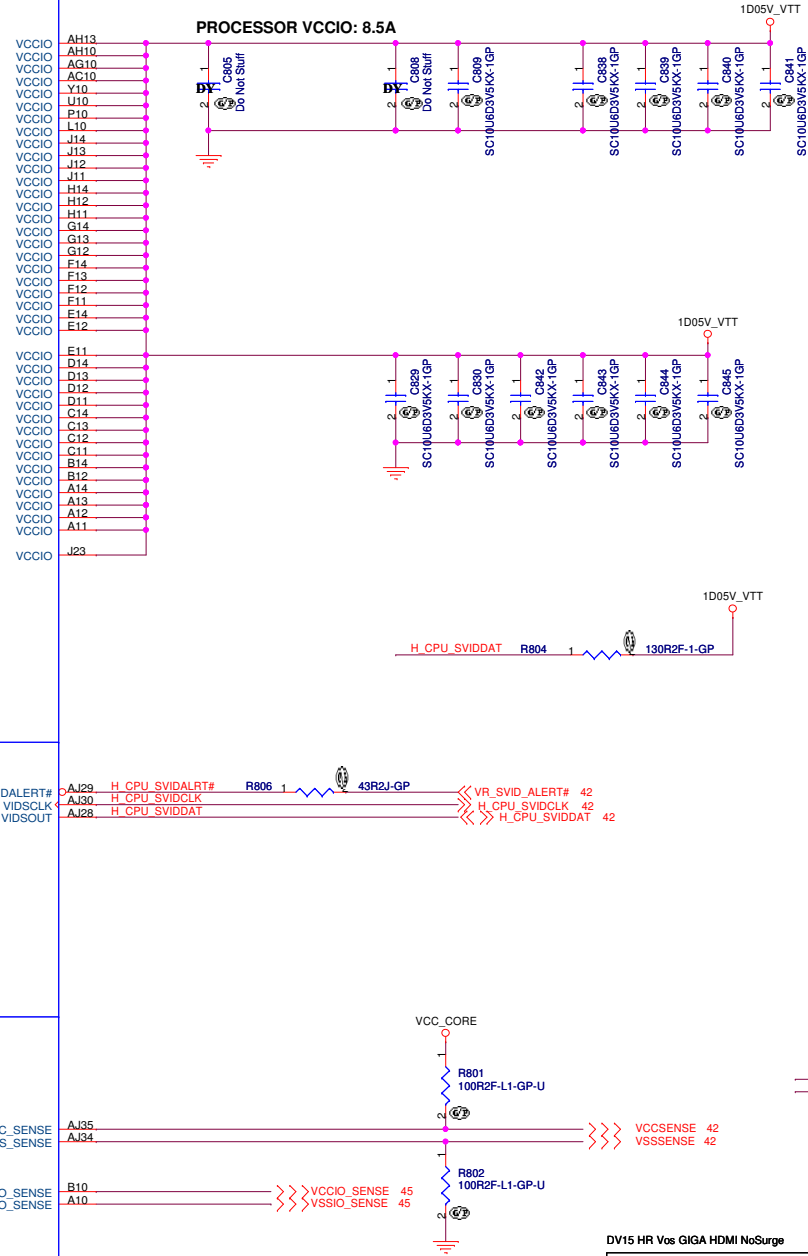


PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES



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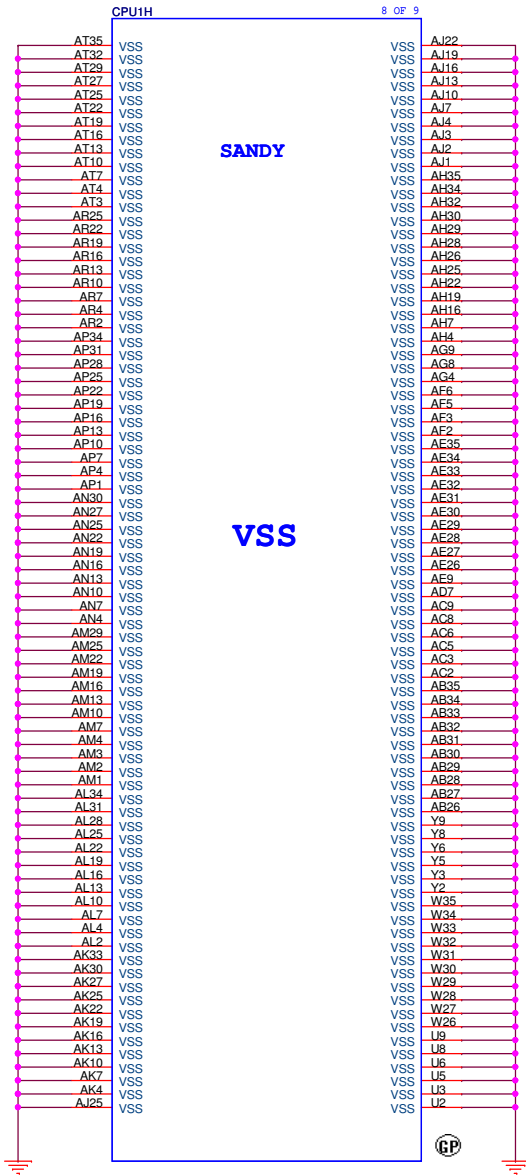
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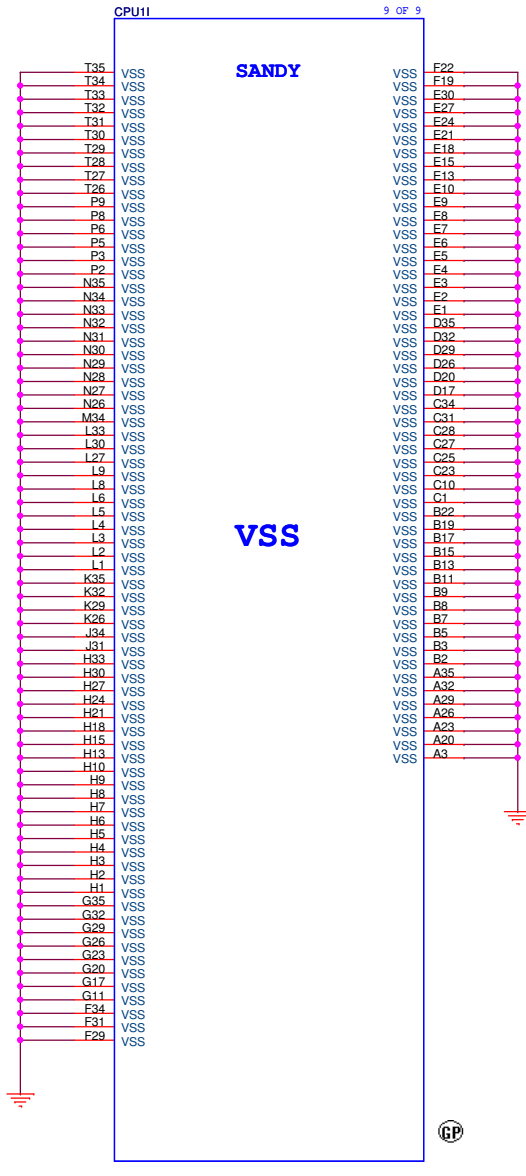
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62.10040.821
2nd = 62.10040.771

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Title **CPU (VSS)**

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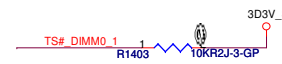
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DM2

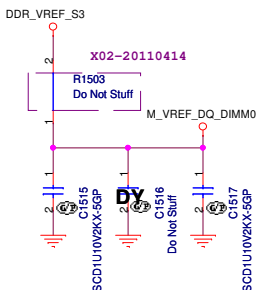
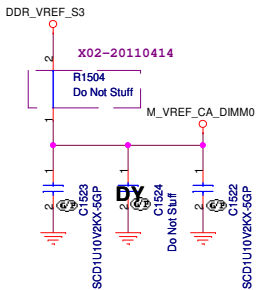


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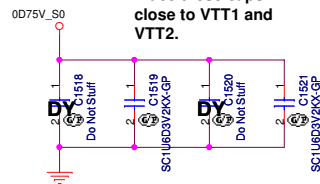
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M_A_A[15:0] 6

M_A_BS2
M_A_BS0
M_A_BS1
M_A_DQ[63:0]



Place these caps close to VTT1 and VTT2.



M_A_DQS# [7:0] 6
M_A_DQS [7:0] 6

M_A_DIM0_ODT0
M_A_DIM0_ODT1
M_VREF_CA_DIMM0
M_VREF_DQ_DIMM0

14.37 DDR3_DRAMRST#

0D75V_S0

DDR3-204P-106-GR

M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
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NP1
NP2
RASP
WEF
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CS0#
CS1#
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CK0
CK0#
CK1
CK1#

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DM2
DM3
DM4
DM5
DM6
DM7

SDA
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NC#2
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M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65
PCH_SMBCLK 14,20,65
TS#_DIMM0_1 14

SA0_DIM0
SA1_DIM0

SCD1U10V2KX-5GP
C1501
C1502
Do Not Stuff

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65
PCH_SMBCLK 14,20,65
TS#_DIMM0_1 14

SA0_DIM0
SA1_DIM0

SCD1U10V2KX-5GP
C1501
C1502
Do Not Stuff

105V_S3

105V_S3

105V_S3

105V_S3

105V_S3

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105V_S3

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105V_S3

105V_S3

105V_S3

105V_S3

M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65
PCH_SMBCLK 14,20,65
TS#_DIMM0_1 14

SA0_DIM0
SA1_DIM0

SCD1U10V2KX-5GP
C1501
C1502
Do Not Stuff

105V_S3

105V_S3

105V_S3

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105V_S3

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105V_S3

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105V_S3

105V_S3

105V_S3

M_A_RAS# 6
M_A_WE# 6
M_A_CAS# 6
M_A_DIM0_CS#0 6
M_A_DIM0_CS#1 6
M_A_DIM0_CKE0 6
M_A_DIM0_CKE1 6
M_A_DIM0_CLK_DDR0 6
M_A_DIM0_CLK_DDR#0 6
M_A_DIM0_CLK_DDR1 6
M_A_DIM0_CLK_DDR#1 6

PCH_SMBDATA 14,20,65
PCH_SMBCLK 14,20,65
TS#_DIMM0_1 14

SA0_DIM0
SA1_DIM0

SCD1U10V2KX-5GP
C1501
C1502
Do Not Stuff

105V_S3

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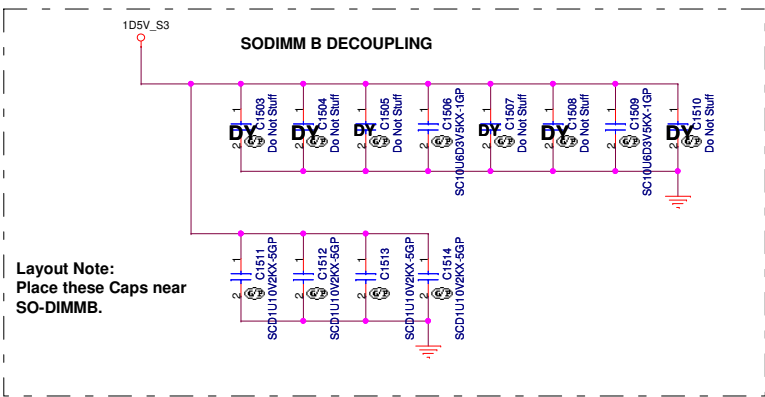
105V_S3

105V_S3

105V_S3

Note:
SO-DIMMB SPD Address is 0x44
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



Layout Note:
Place these Caps near SO-DIMMB.

DV15 HR Vos GIGA HDMI NoSurge

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Title: **DDR3-SODIMM1**

Size: Custom Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet: 15 of 104

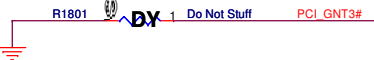
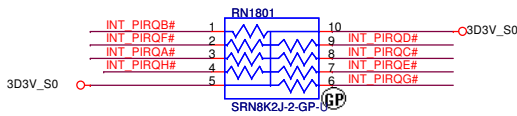
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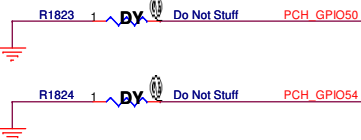
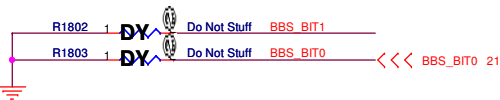
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Reserved			
Size	Document Number		Rev
A3	Enrico/Caruso 15 HR		X01
Date:	Thursday, June 02, 2011	Sheet	16 of 104



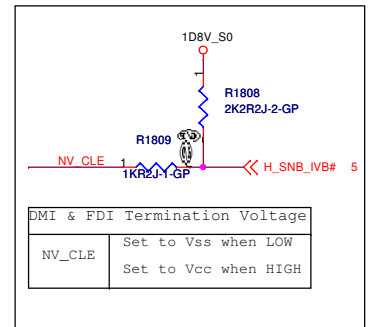
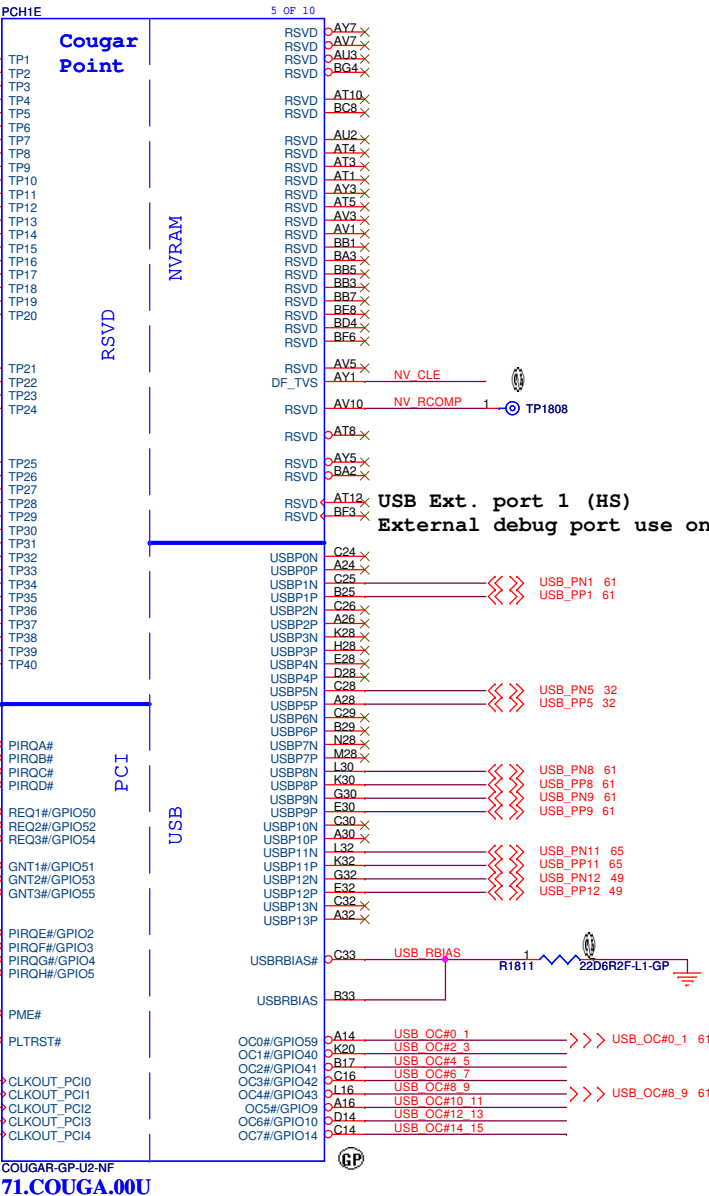
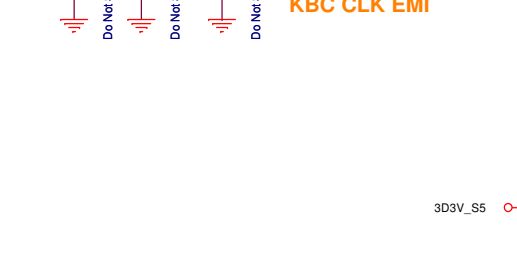
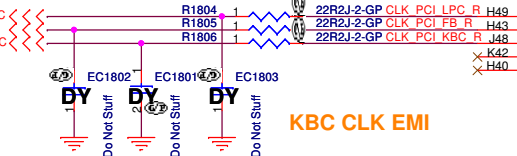
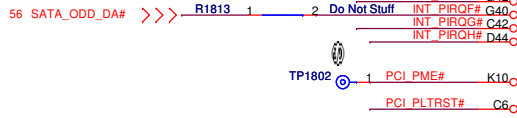
SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

USB Ext. port 1 (HS)
External debug port use on Huron river platform
USB Table

Pair	Device
0	X
1	USB Ext. port 1 (HS)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 2
9	USB Ext. port 3
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

Wistron Corporation
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Title: **PCH (PCI/USB/NVRAM)**
 Size A3: Document Number: **Enrico/Caruso 15 HR** Rev: **X01**
 Date: Thursday, June 02, 2011 Sheet 18 of 104

SSID = PCH

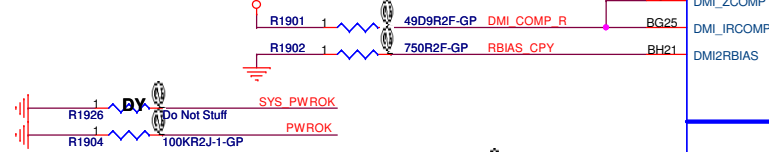
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Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

4 DMI_RXN[3:0] <<<<
4 DMI_RXP[3:0] <<<<
4 DMI_TXN[3:0] <<<<
4 DMI_TXP[3:0] <<<<

FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

1D05V_VTT



5.37 PM_DRAM_PWRGD <<<<
S0_PWR_GOOD after PM_SLP_S3# delay 150 ms

PCH1C

3 OF 10

Cougar Point

DMI

FDI

System Power Management

COUGAR-GP-U2-NF
71.COUGA.00U

FDI_RXN0 BJ14 <<<< FDI_TXN0 4
FDI_RXN1 AY14 <<<< FDI_TXN1 4
FDI_RXN2 BE14 <<<< FDI_TXN2 4
FDI_RXN3 BH13 <<<< FDI_TXN3 4
FDI_RXN4 BC12 <<<< FDI_TXN4 4
FDI_RXN5 BJ12 <<<< FDI_TXN5 4
FDI_RXN6 BG10 <<<< FDI_TXN6 4
FDI_RXN7 BG9 <<<< FDI_TXN7 4
FDI_RXP0 BG14 <<<< FDI_TXP0 4
FDI_RXP1 BB14 <<<< FDI_TXP1 4
FDI_RXP2 BE14 <<<< FDI_TXP2 4
FDI_RXP3 BE12 <<<< FDI_TXP3 4
FDI_RXP4 BG12 <<<< FDI_TXP4 4
FDI_RXP5 BJ10 <<<< FDI_TXP5 4
FDI_RXP6 BJ10 <<<< FDI_TXP6 4
FDI_RXP7 BH9 <<<< FDI_TXP7 4

FDI_INT AW16 >>>> FDI_INT 4
FDI_FSYNC0 AV12 >>>> FDI_FSYNC0 4
FDI_FSYNC1 BC10 >>>> FDI_FSYNC1 4
FDI_LSYNC0 AV14 >>>> FDI_LSYNC0 4
FDI_LSYNC1 BB10 >>>> FDI_LSYNC1 4

DSWVRMEN A18 DSWODVREN

DPWROK E22 PCH_DPWROK

WAKE# B9 PCH_WAKE# R

CLKRUN#/GPIO32 N3

SUS_STAT#/GPIO61 G8

SUSCLK/GPIO62 N14

SLP_S5#/GPIO63 D10

SLP_S4# H4

SLP_S3# F4

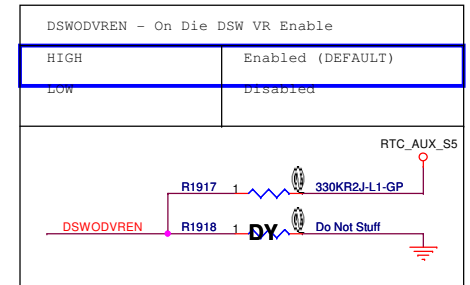
SLP_A# G10

SLP_SUS# G16

PMSYNCH AP14

SLP_LAN#/GPIO29 K14

PM_RSMRST# 1 2 Do Not Stuff <<<< RSMRST#_KBC 27
PCH_SUSCLK_KBC



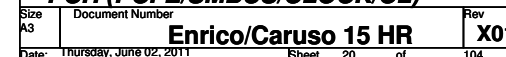
DV15 HR Vos GIGA HDMI NoSurge

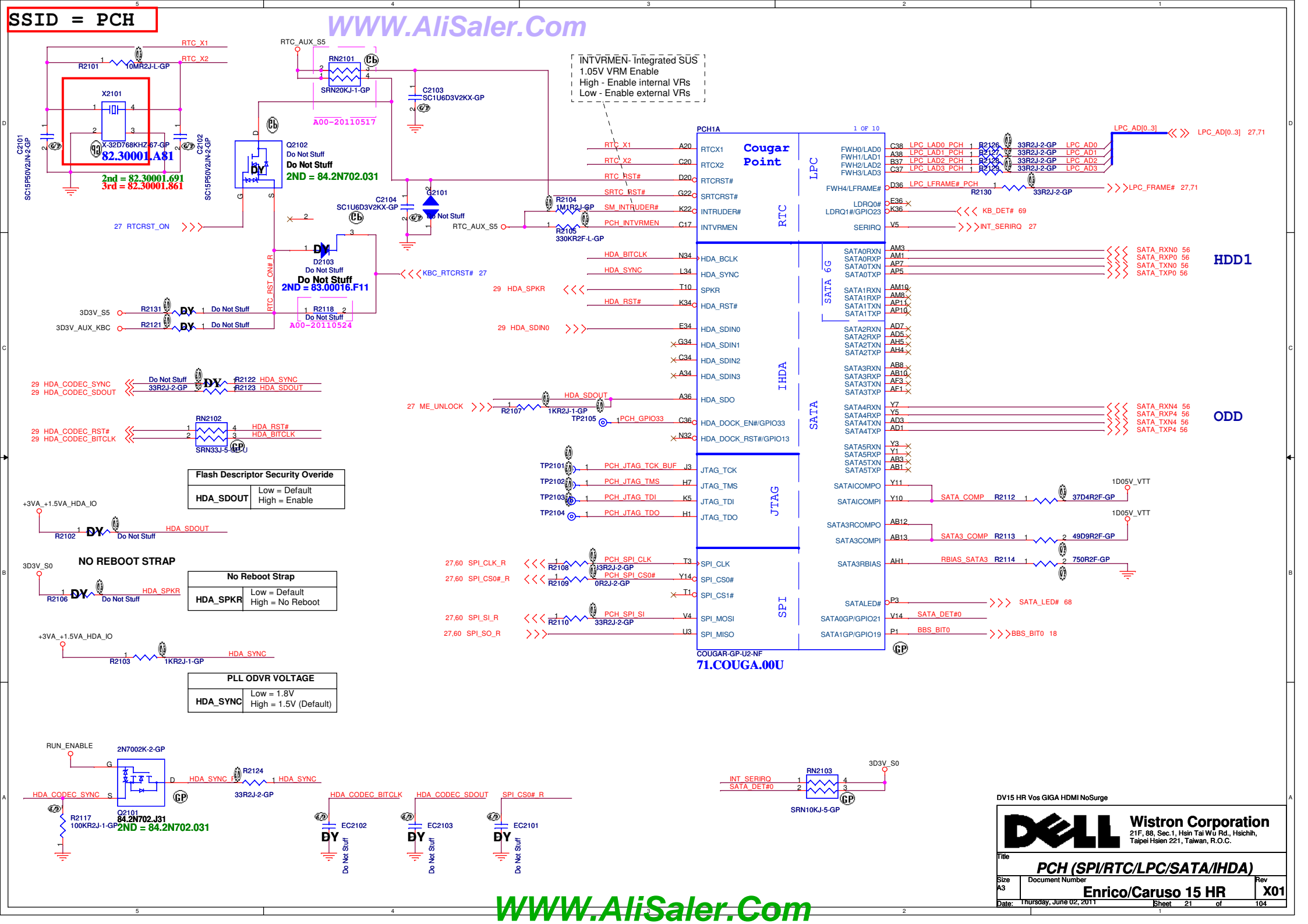
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

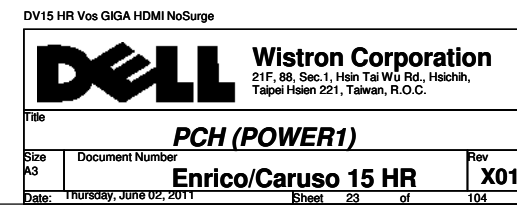
Title PCH (DM I/FDI/PM)
Size A3 Document Number Enrico/Caruso 15 HR Rev X01
Date Thursday, June 02, 2011 Sheet 19 of 104

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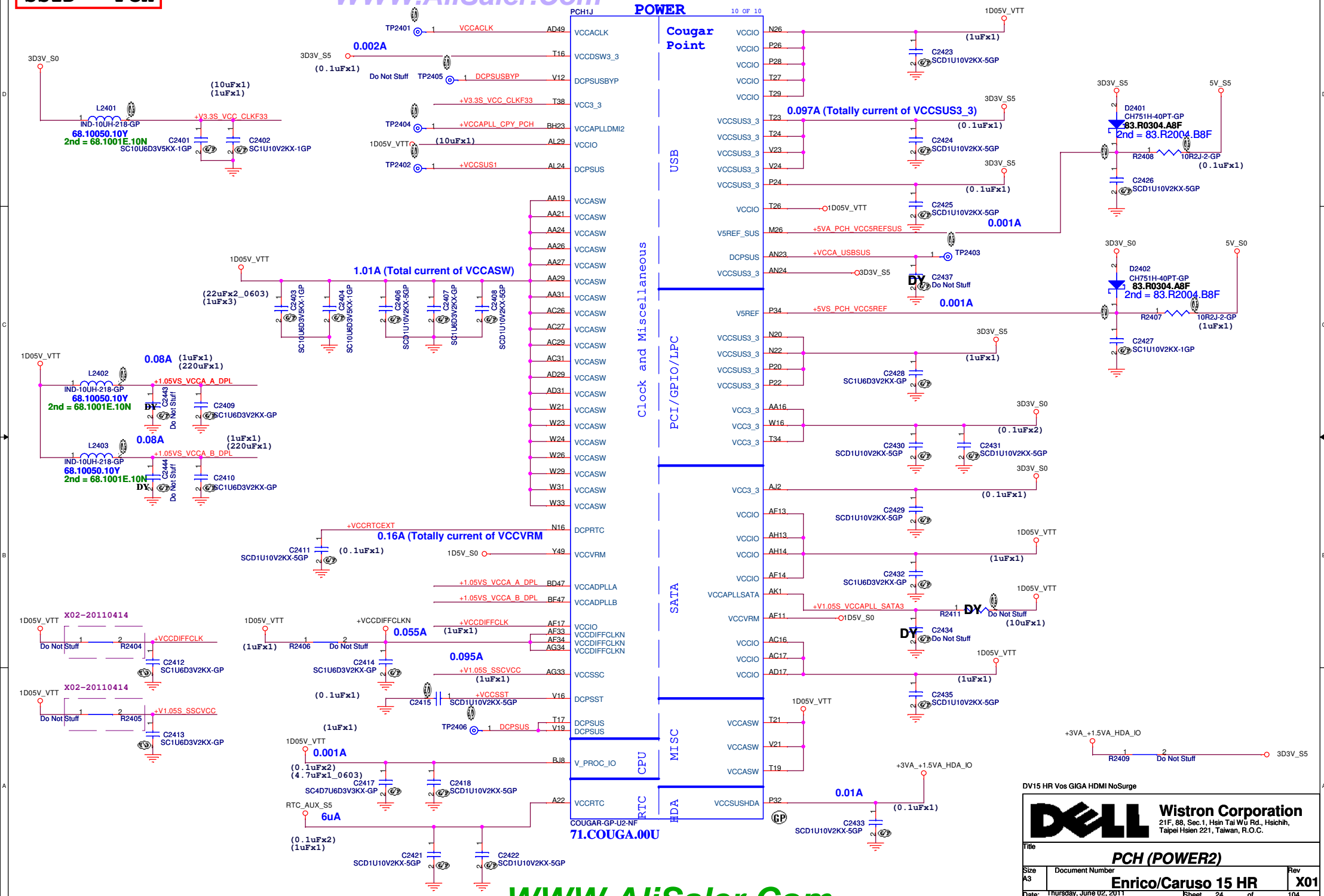







SSID = PCH

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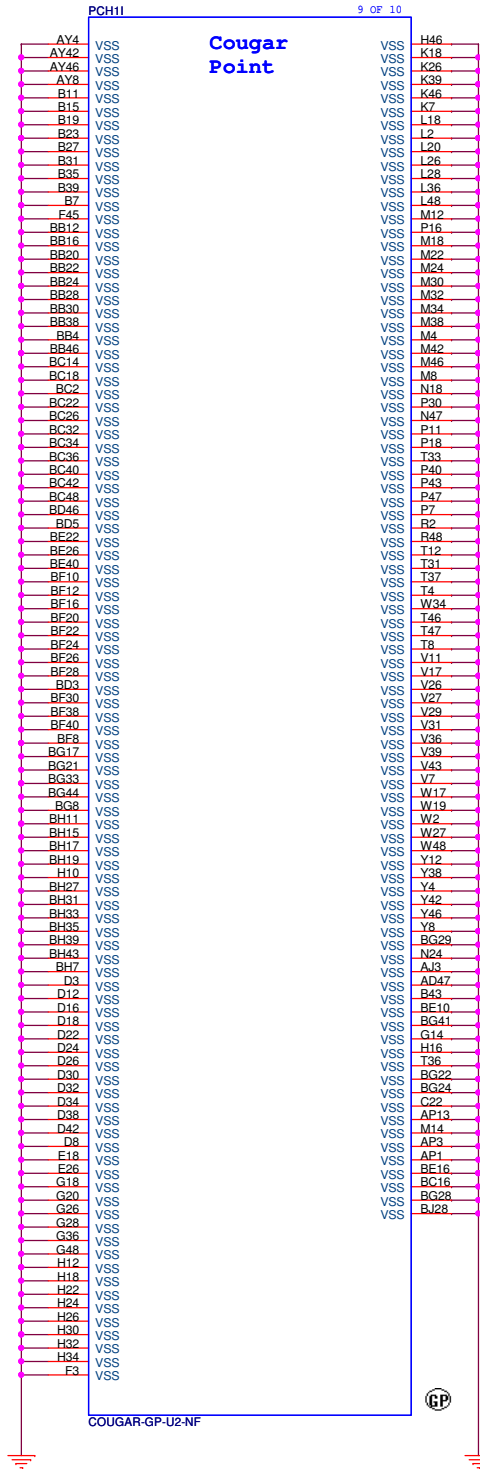
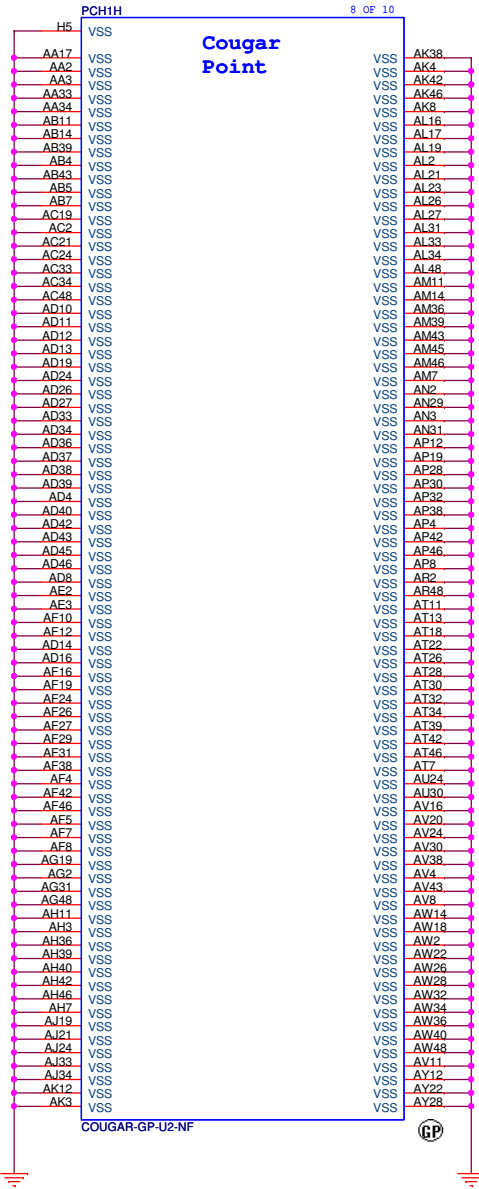


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DV15 HR Vos GIGA HDMI NoSurge			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PCH (POWER2)			
Size A3	Document Number	Enrico/Caruso 15 HR	Rev X01
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SSID = PCH

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Taipei Hsien 221, Taiwan, R.O.C.

Title			PCH (VSS)	
Size	Document Number	Rev		
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Taipei Hsien 221, Taiwan, R.O.C.

Title

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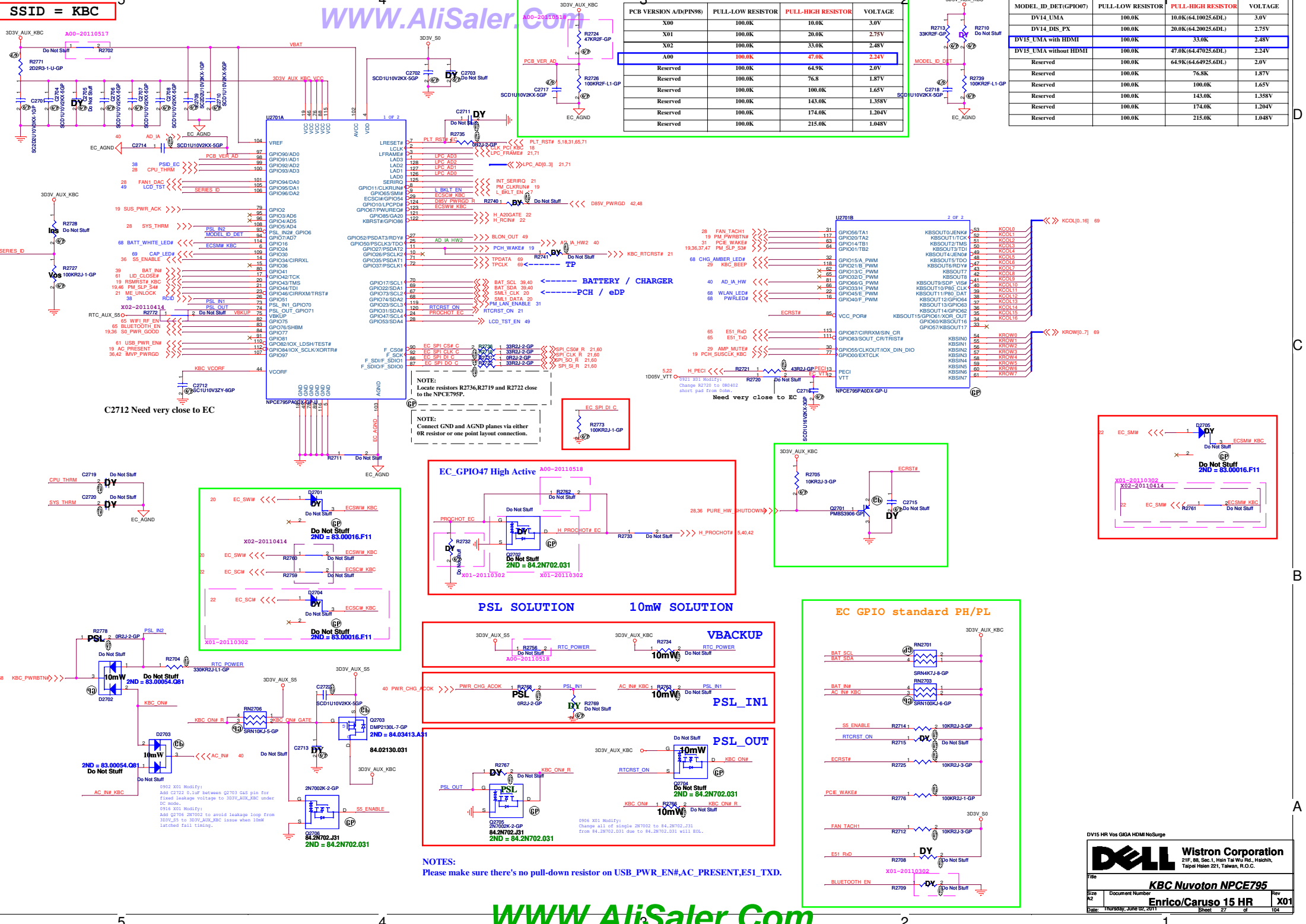
Size
A3

Document Number
Enrico/Caruso 15 HR

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X01

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MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

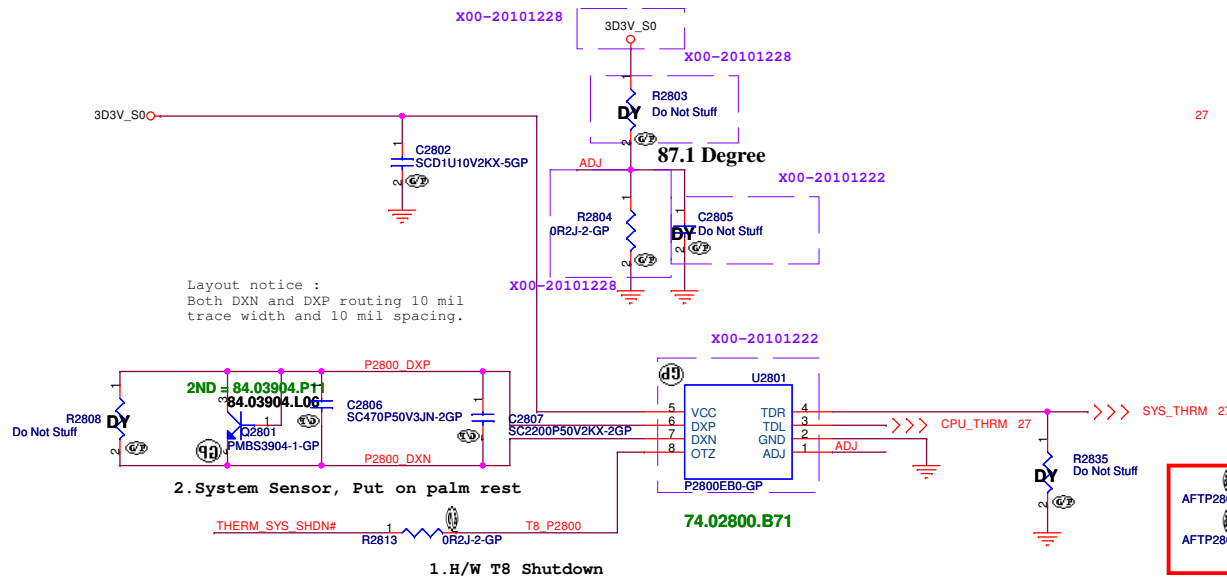
PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DV14_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DV14_DIS_PX	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
Reserved	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

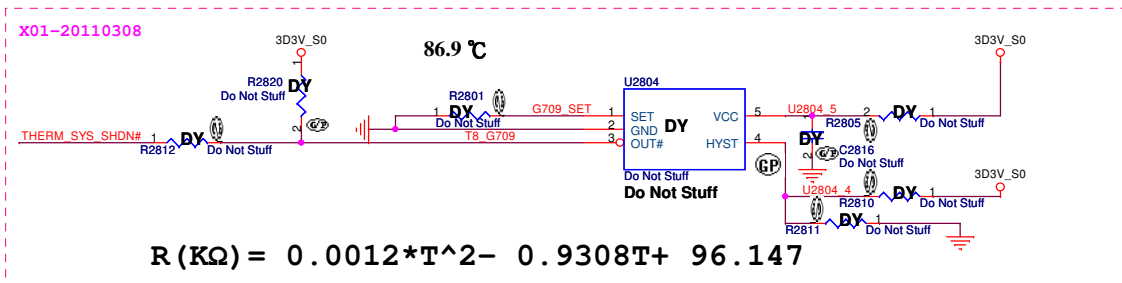
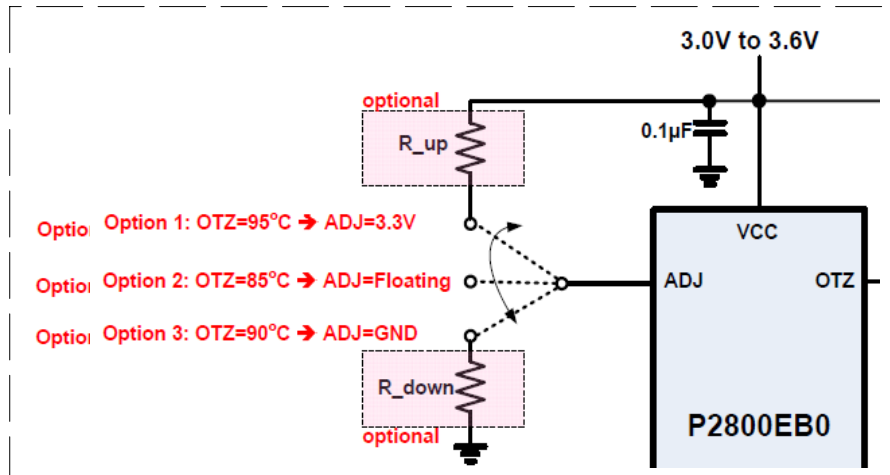
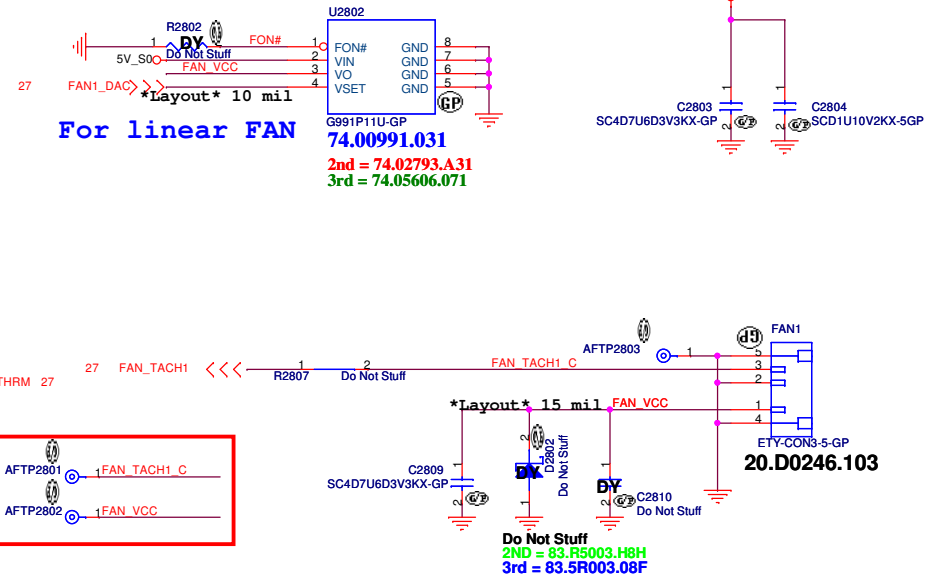
NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,ES1_TSD.

SSID = Thermal

Thermal sensor P2800



Fan controller G991






Title			
Audio Codec 92HD87B1			
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 HR	X01	
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DV15 HR Vos GIGA HDMI NoSurge



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Title

Size
A3

Document Number
Enrico/Caruso 15 HR

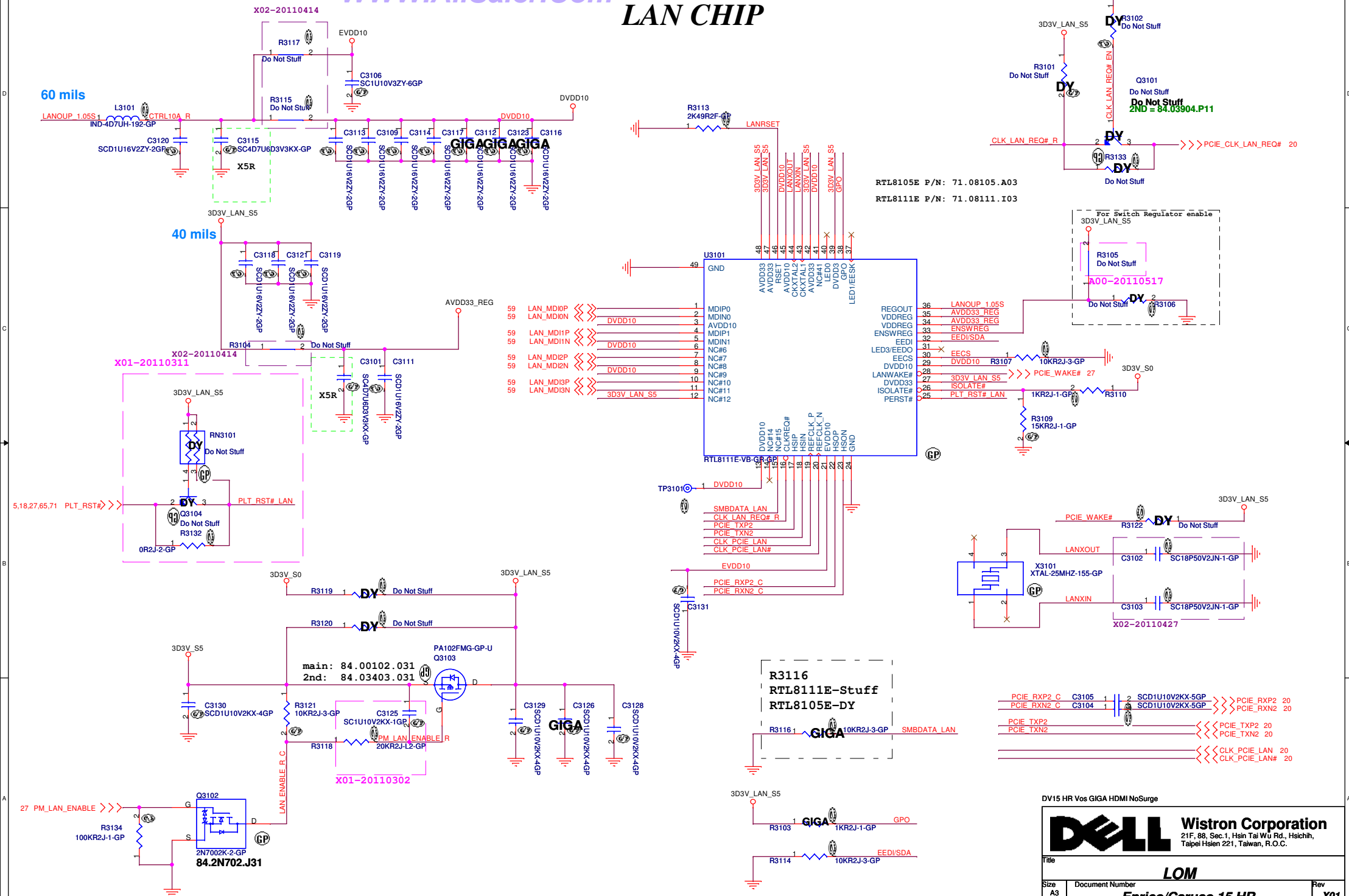
Rev
X01

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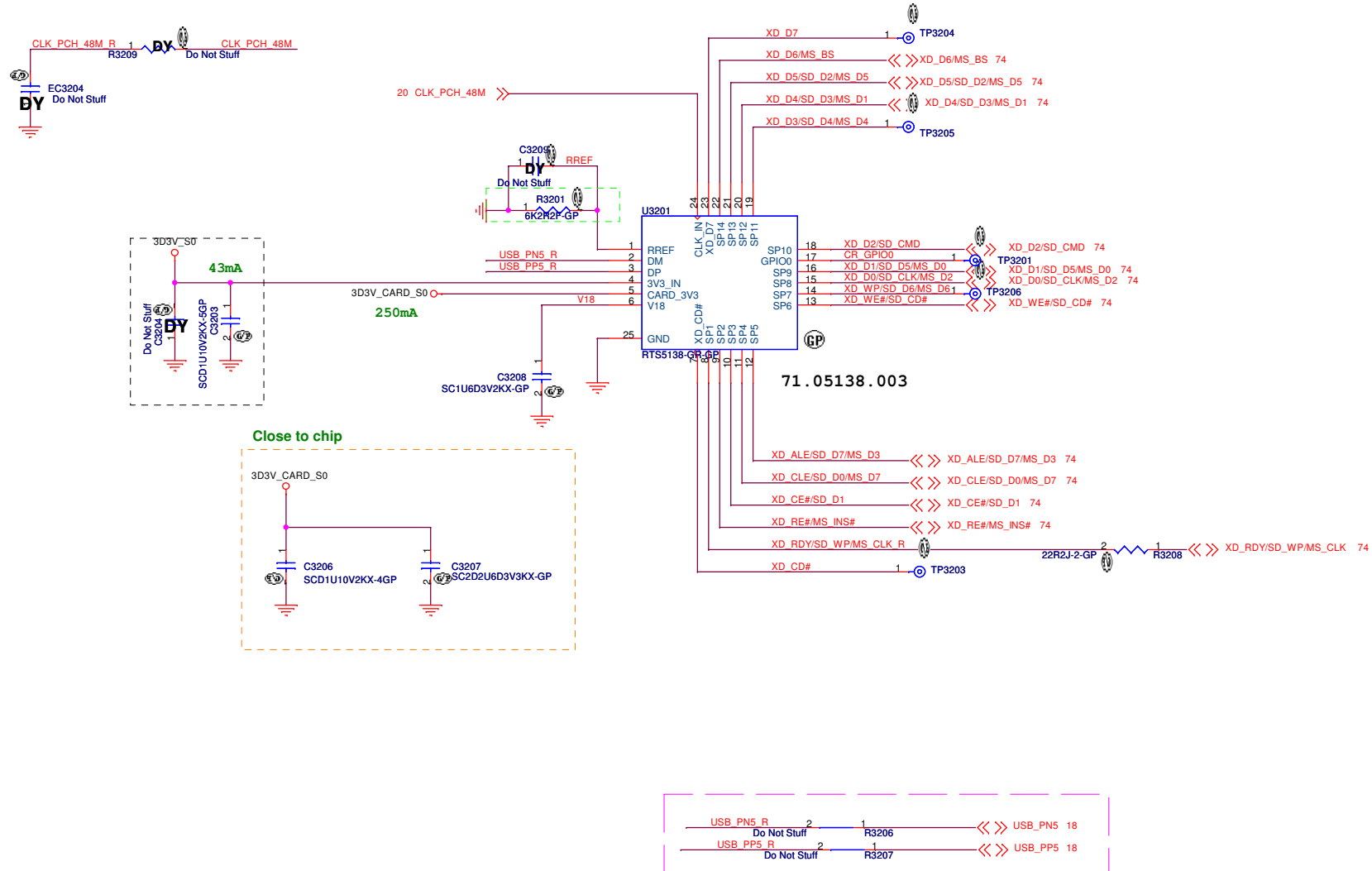
Date: Thursday, June 02, 2011

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LAN CHIP



SSID = SDIO




DV15 HR Vos GIGA HDMI NoSurge




Title				
Card Reader-RTS5138				
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DV15 HR Vos GIGA HDMI NoSurge

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Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
Date: Thursday, June 02, 2011	Sheet E	33 of	104

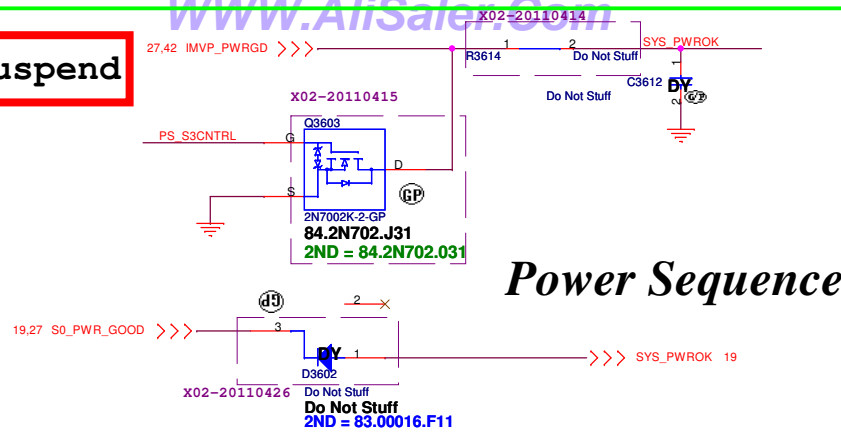
DV15 HR Vos GIGA HDMI NoSurge

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Size	Document Number		Rev
A3	Enrico/Caruso 15 HR		X01
Date:	Thursday, June 02, 2011	Sheet	34 of 104

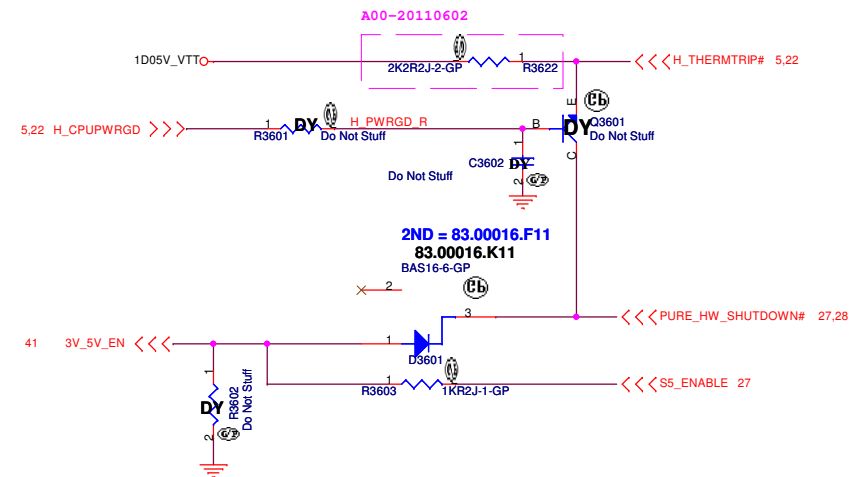
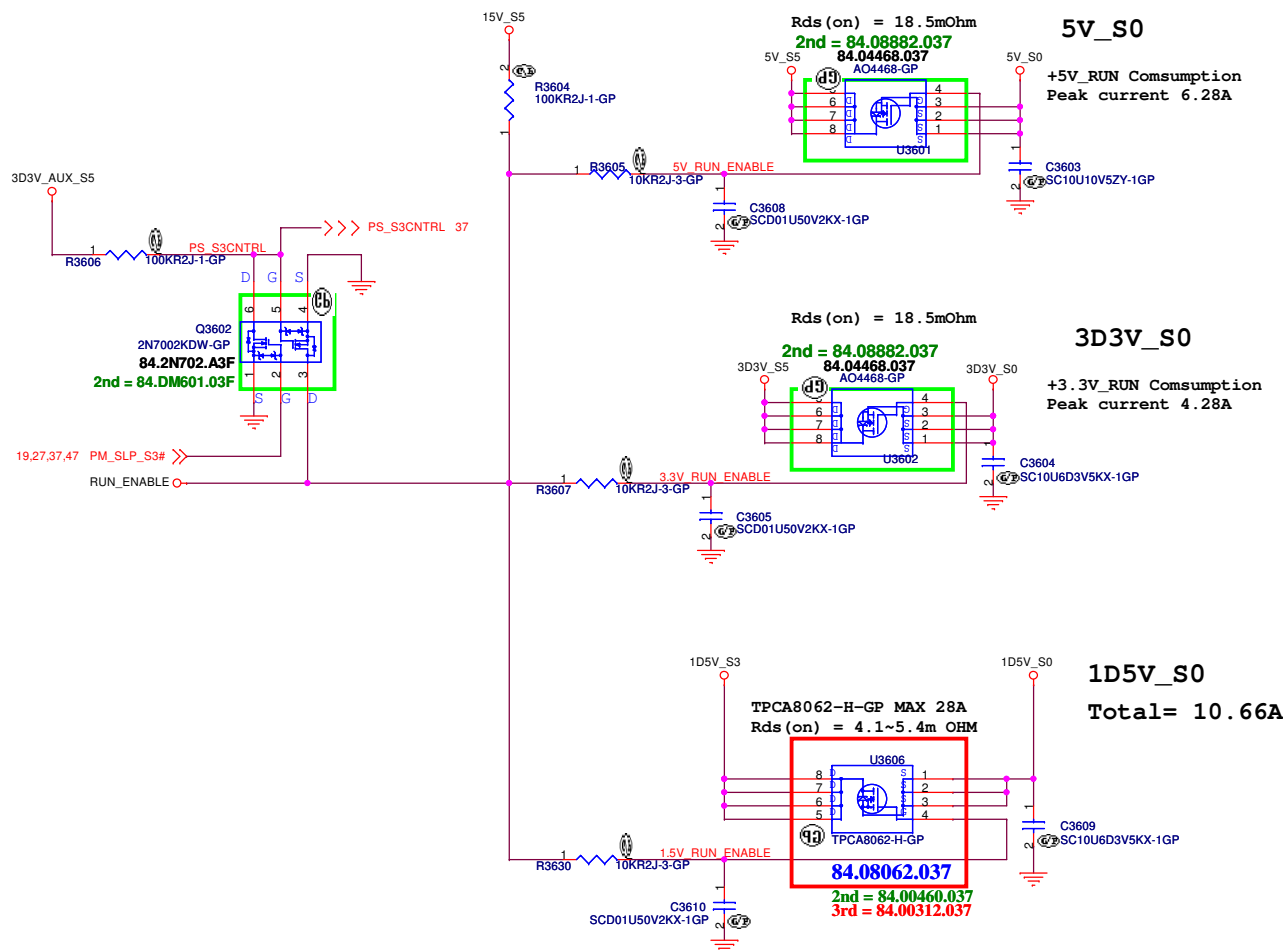
DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
Date: Thursday, June 02, 2011	Sheet	35	of 104

SSID = Reset.Suspend



ROSA Run Power



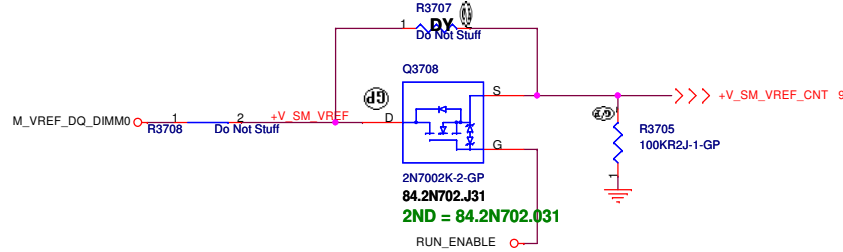
DV15 HR Vos GIGA HDMI NoSurge



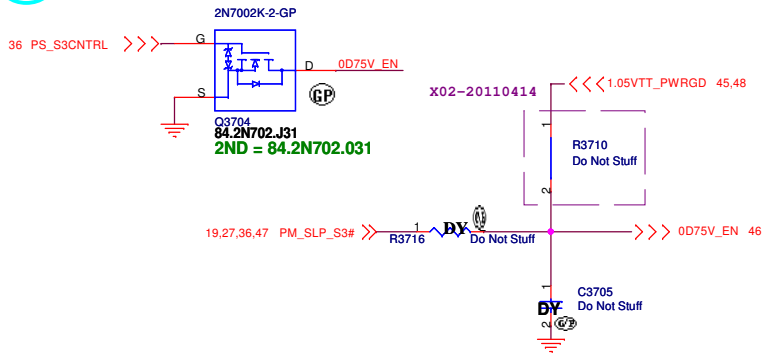
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

File			Power Plane Enable	
Size	Document Number		Rev	
A3			Enrico/Caruso 15 HR	
Date:	Thursday, June 02, 2011	Sheet	36	of 104

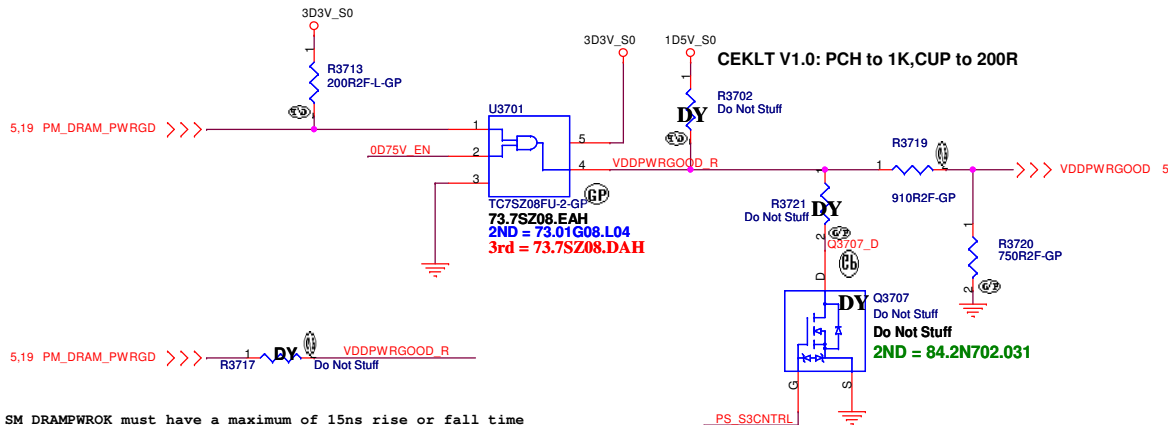
**Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation**



5 S3 Power Reduction

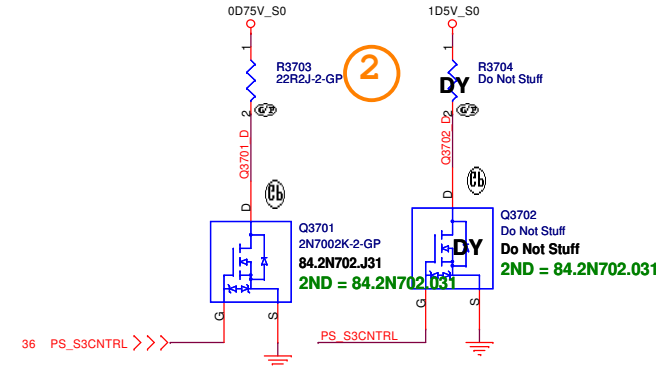


**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**

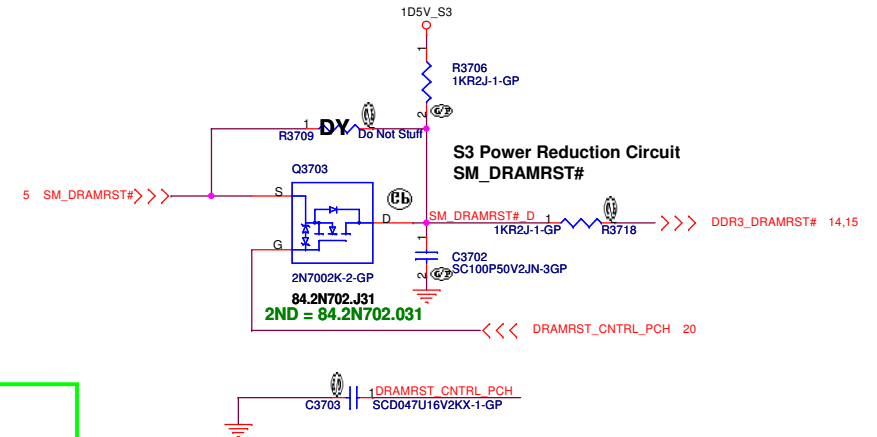


SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

**Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK**



**Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK**



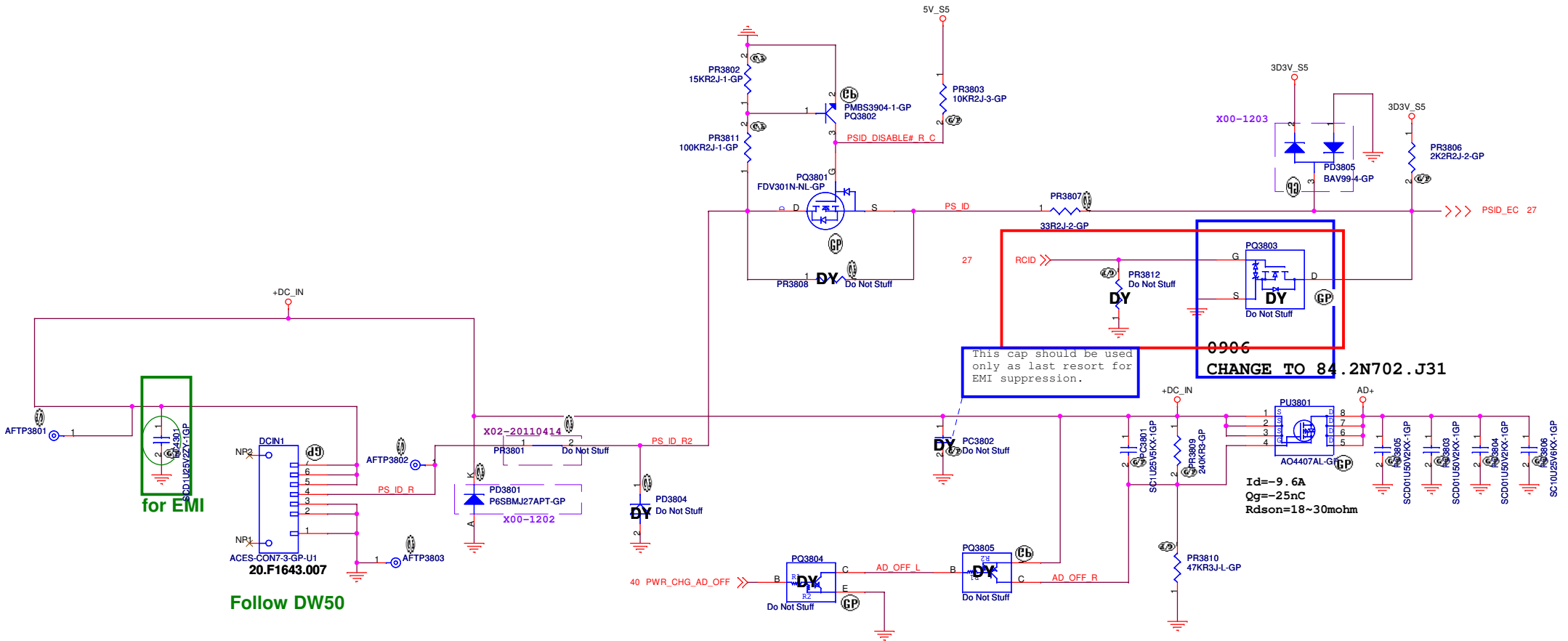
DV15 HR Vos GIGA HDMI NoSurge

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

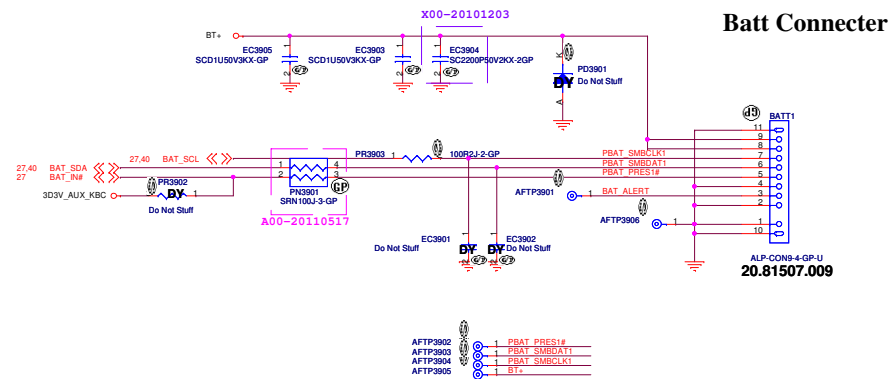
Title ADAPTER		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
Date: Thursday, June 02, 2011	Sheet 37	of 104

SSID = PWR.Support

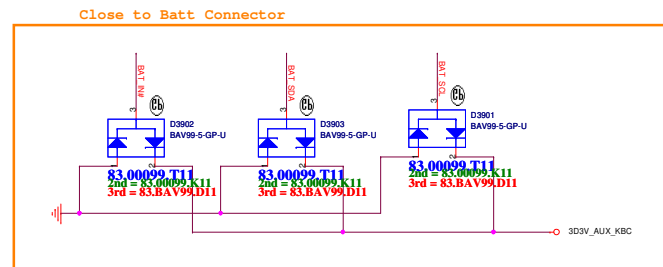
DCin CONN



DV15 HR Vos GIGA HDMI NoSurge
DELL Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.
 Title: **DCIN**
 Size: **A3** Document Number: **Enrico/Caruso 15 HR** Rev: **X01**
 Date: Thursday, June 02, 2011 Sheet 38 of 104



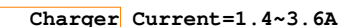
For actual location, need to be swap all pin



DV15 HR Vos GIGA HDMI NoSurge

0802 Rename H_PROCHOT#

5,27,42 H_PROCHOT# <<—



EE need check pull high

Adapter type	PR4023
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

DV15 HR Vos GIGA HDMI NoSurge

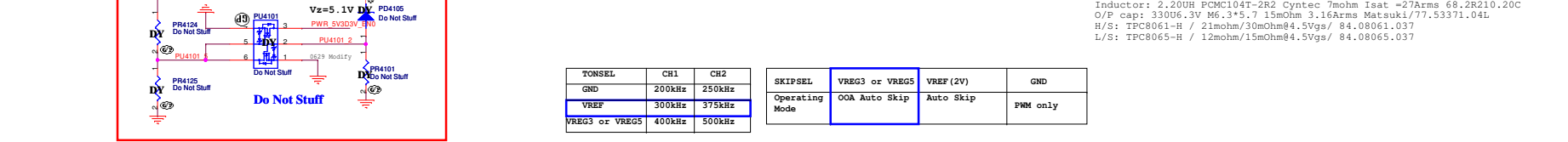
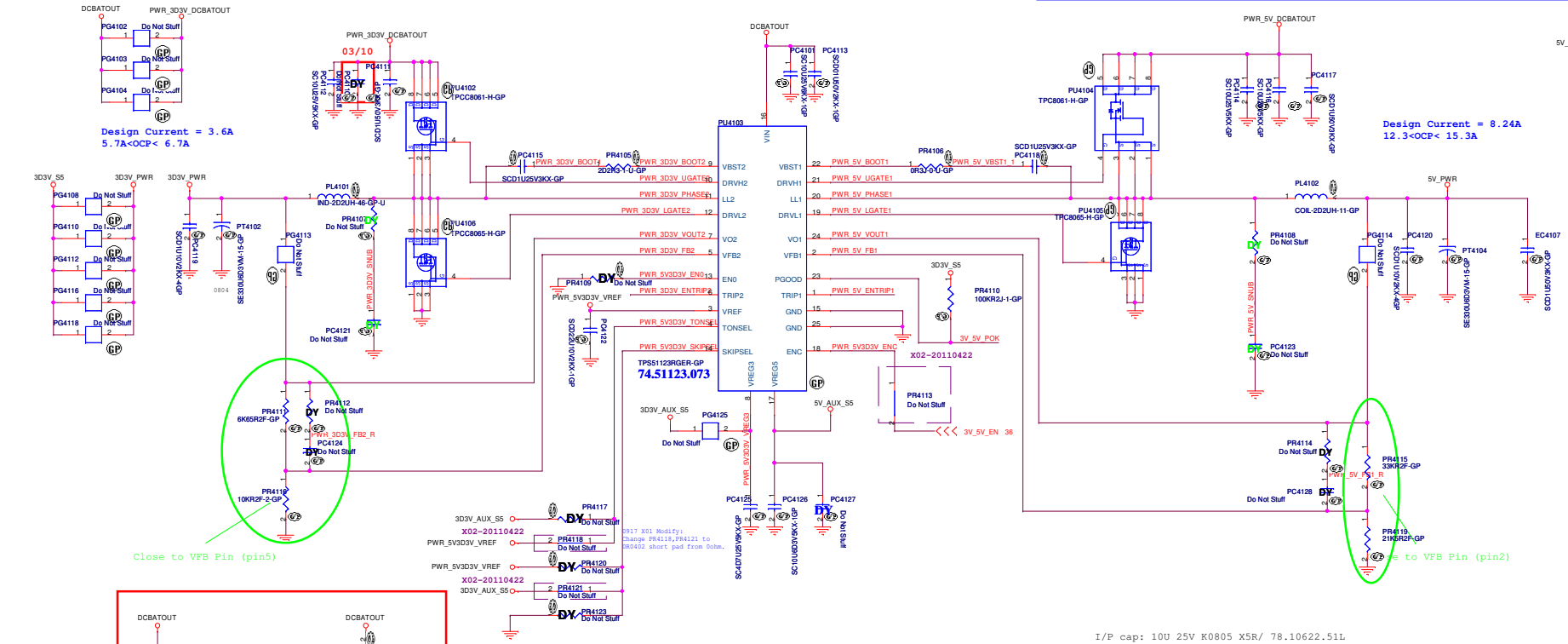
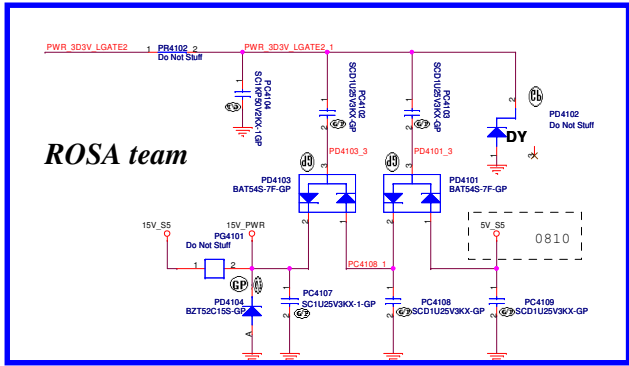


Title **CHARGER BQ24707**

Size	Document Number	Rev
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SSID = PWR.Plane.Regulator_5v3p3v

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TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	250kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	300kHz	375kHz				
VREG3 or VREG5	400kHz	500kHz				

I/P cap: 10u 25V K0805 X5R/ 78.10622.51L
Inductor: 2.20uH PCMC063T-2R2M Cyntec 20mohm Isat =14Arms 68.2R210.20B
O/P cap: 330uF 3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: TPC8061-H NC 8P / 21mohm/29mOhm@4.5Vgs/ 84.08061.A37
L/S: TPC8065-H NC 8P / 12.1mohm/17.4mOhm@4.5Vgs/ 84.08065.A37

DV15 HR Vos GIGA HDMI NoSurge

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File: **5V/3D3V(TP551123RGER)**
Size: A2 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**
Date: Thursday, June 02, 2011 Sheet: 41 of 104

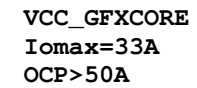
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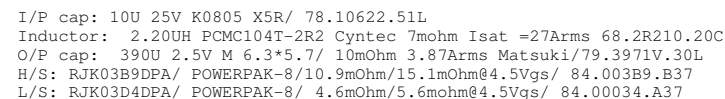


Title			
ISL95831_CPU_CORE (2 of 3)			
Size	Document Number	Rev	
Custom	Enrico/Caruso 15 HR	X01	
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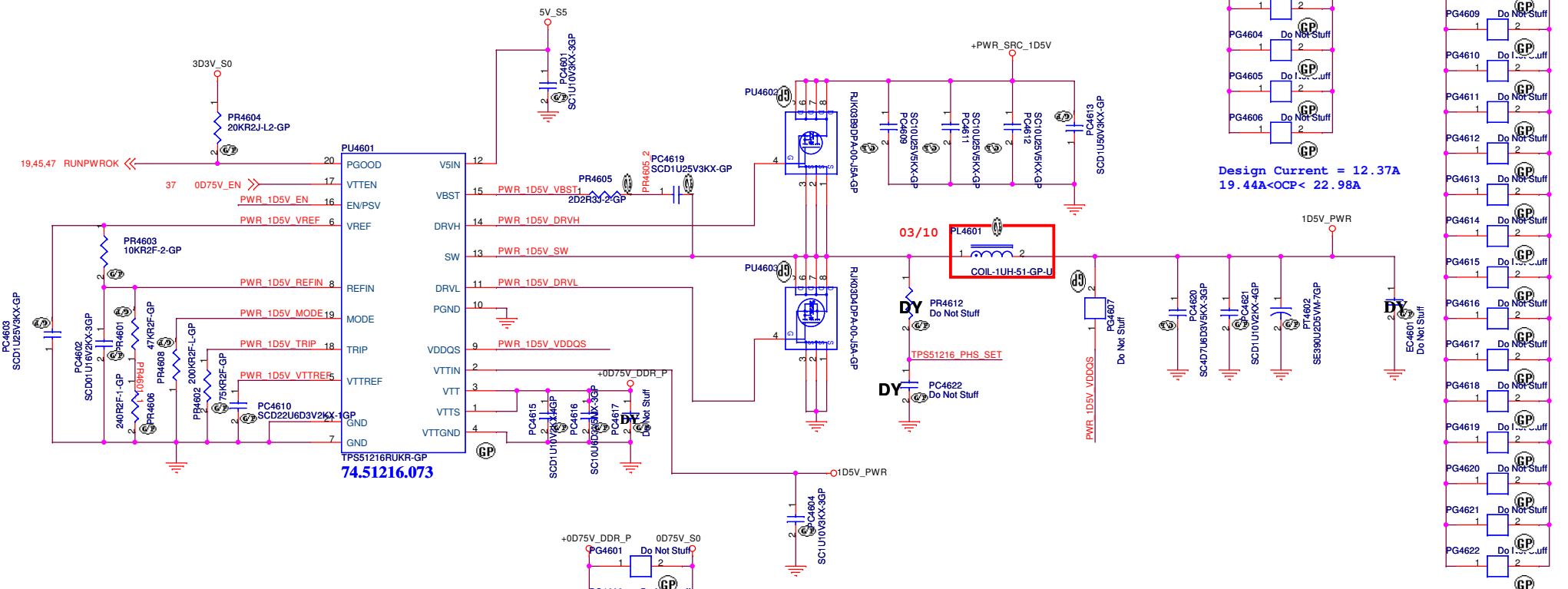
**EMI/ESD****ISL95831_CPU_CORE(3/3)**

Enrico/Caruso 15 HR

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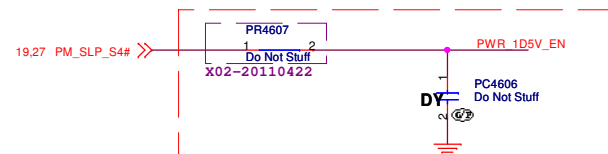
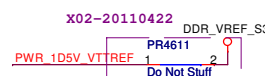


SSID = PWR.Plane.Regulator1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR4608	400kHz	Tracking Discharge
200k ohm	300kHz	
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.0UH PCMB104T-1R0M Cyntec 3mohm Isat =28Arms 68.1R01C.10Q
O/P cap: 390U 2.5V M 6.3*5.7/ 10mOhm 3.87Arms Matsuki/79.3971V.30L
H/S: RJK03B9DPA/ POWERPAK-8/10.9mOhm/15.1mOhm@4.5Vgs/ 84.003B9.B37
L/S: RJK03D4DPA/ POWERPAK-8/ 4.6mOhm/5.6mohm@4.5Vgs/ 84.00034.A37

DV15 HR Vos GIGA HDMI NoSurge

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File

TPS51116 +1.5V SUS

Size A3 Document Number

Enrico/Caruso 15 HR

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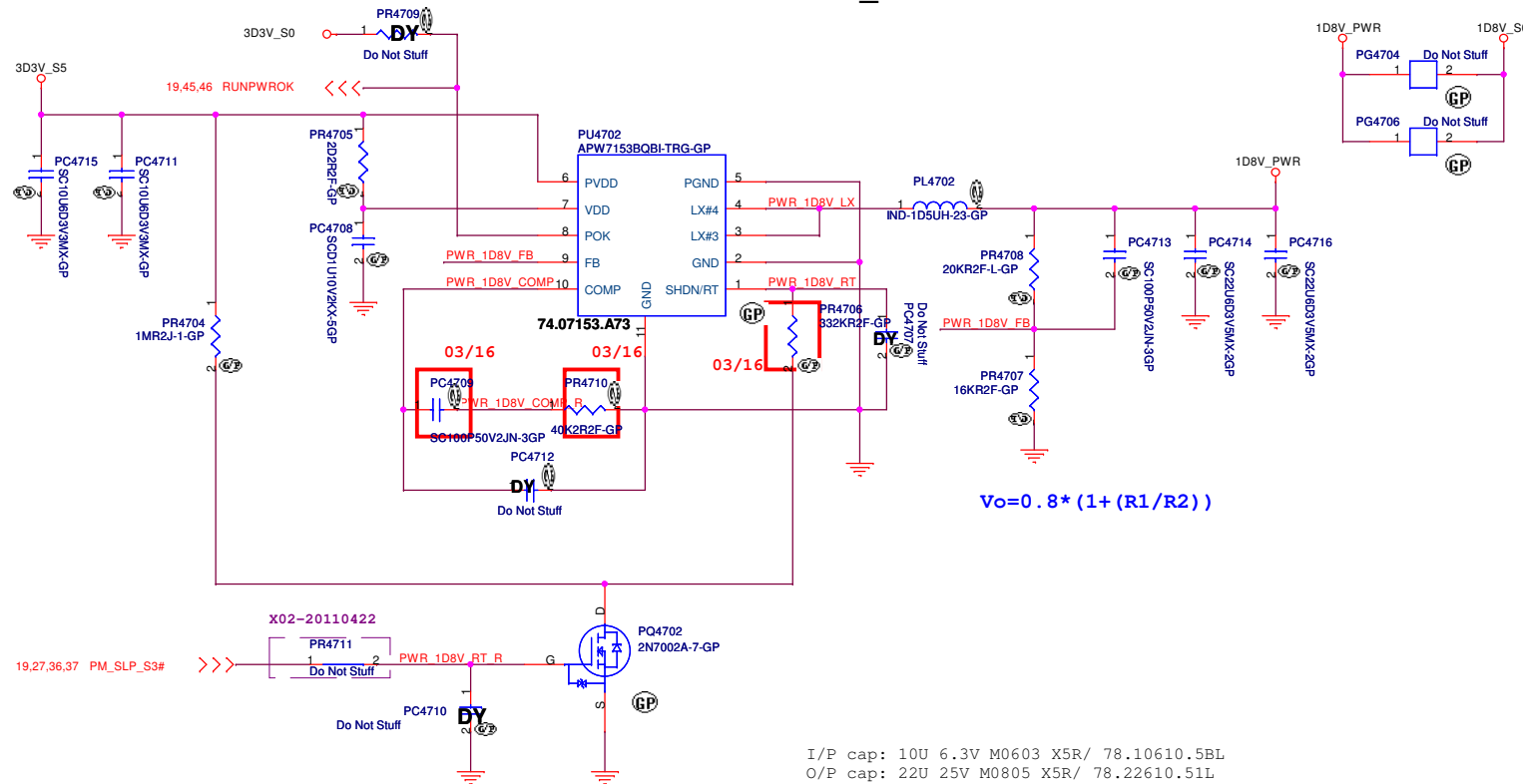
Rev **X01**

SSID = PWR.Plane.Regulator_1D8V_S0

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APW7153B for 1D8V_S0

+1.8V_RUN
Design current = 0.87A



I/P cap: 10U 6.3V M0603 X5R/ 78.10610.5BL
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

DV15 HR Vos GIGA HDMI NoSurge

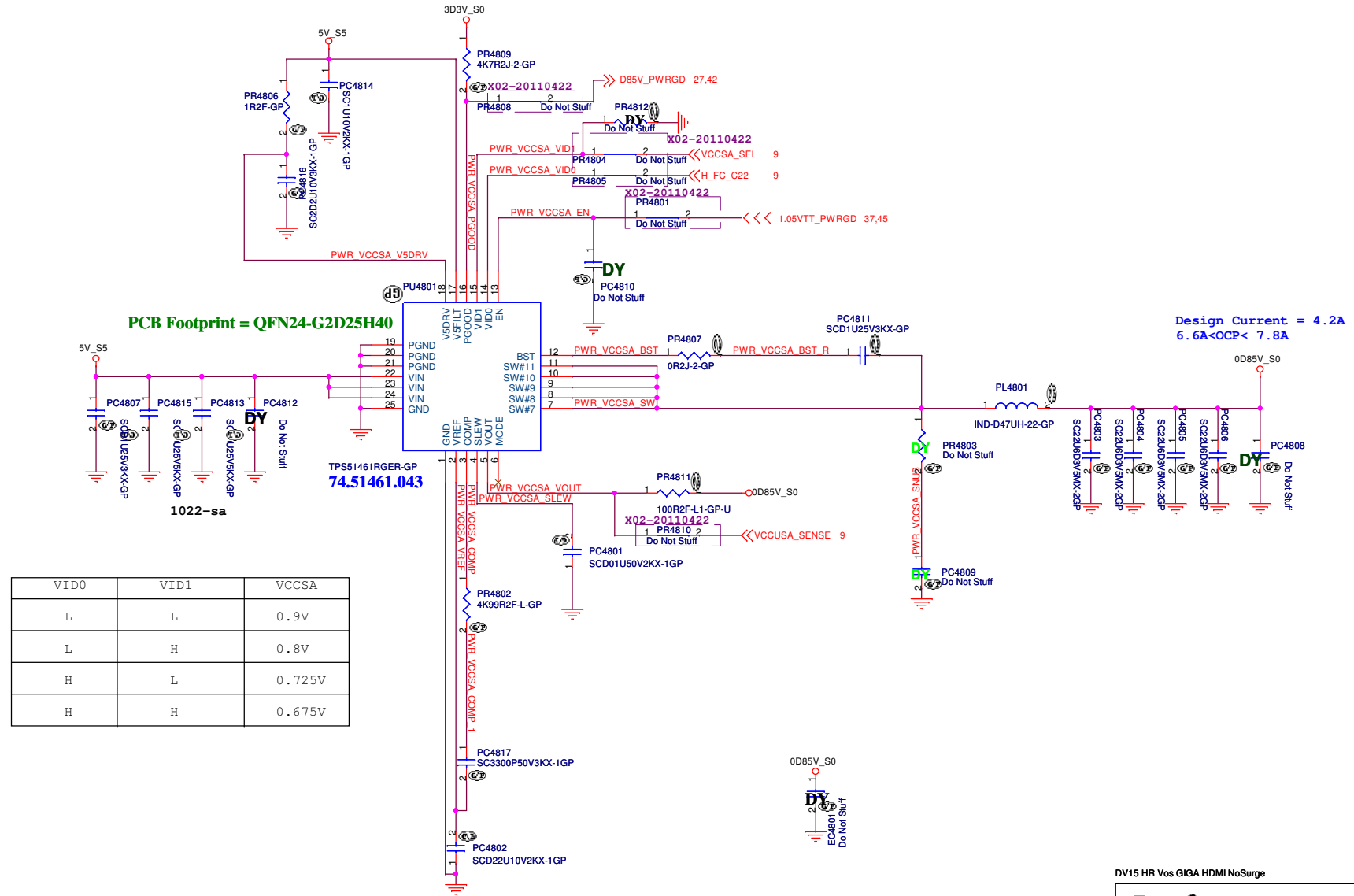


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Title			TPS51311 for 1D8V_S0	
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TPS51461 for VCCSA



DV15 HR Vos GIGA HDMI NoSurge

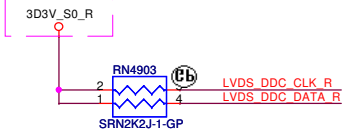


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Taipei Hsien 221, Taiwan, R.O.C.

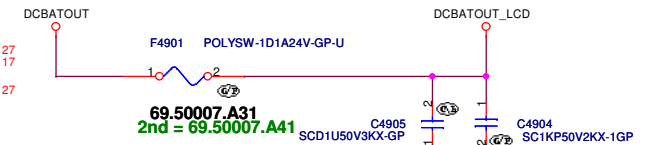
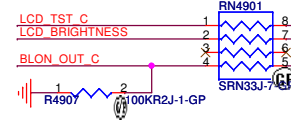
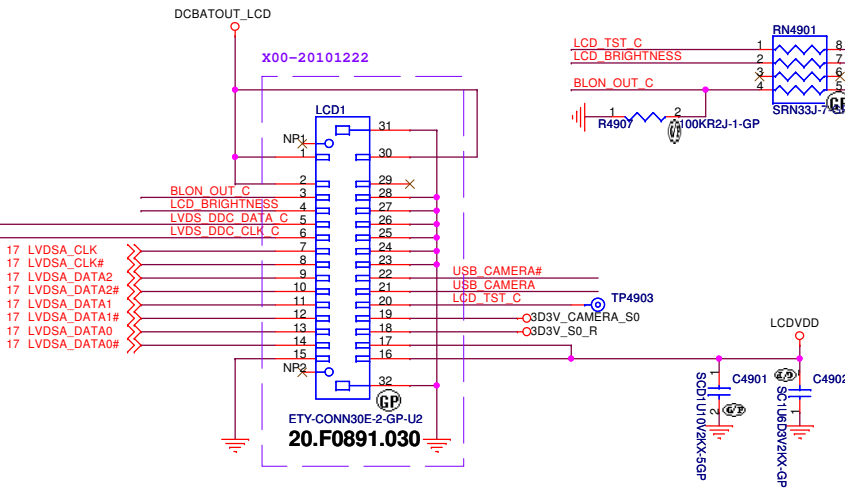
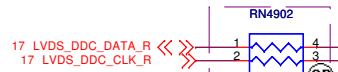
Title TPS51461 VCCSA		
Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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LVDS CONNECTOR

X01-20110307

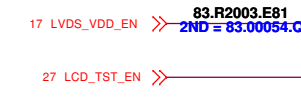
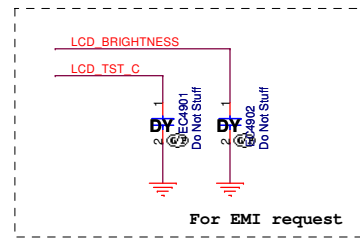
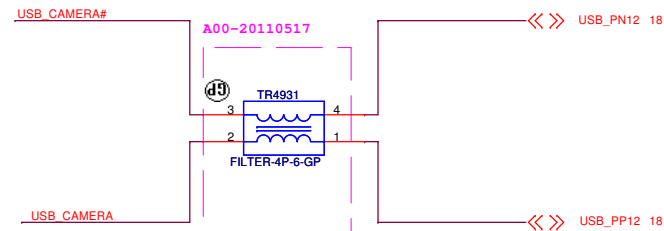
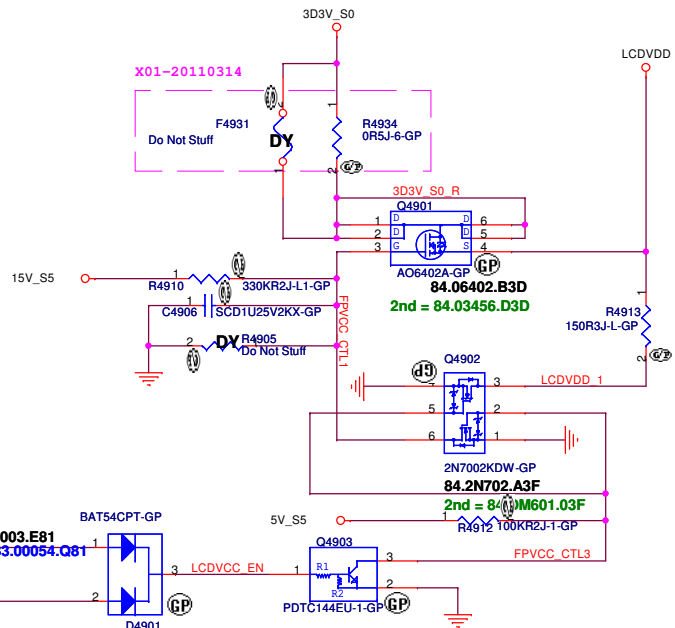
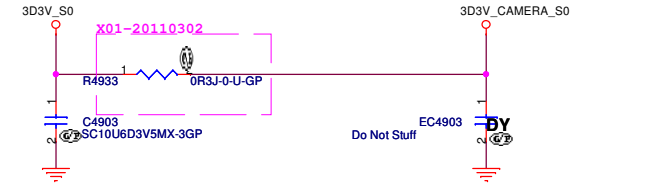


X02-20110415



INVERTER POWER

Camera Power



DV15 HR Vos GIGA HDMI NoSurge

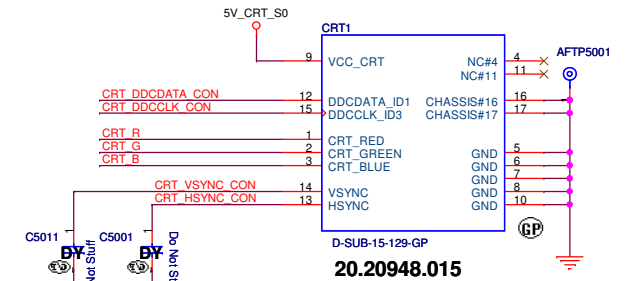
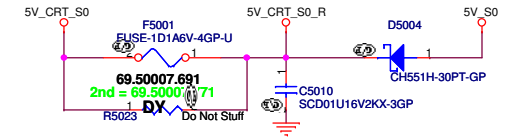
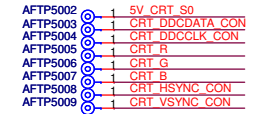
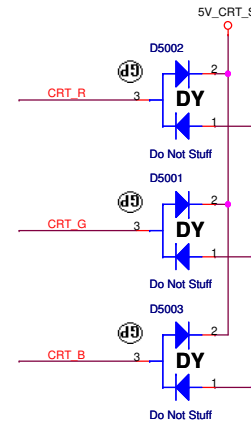
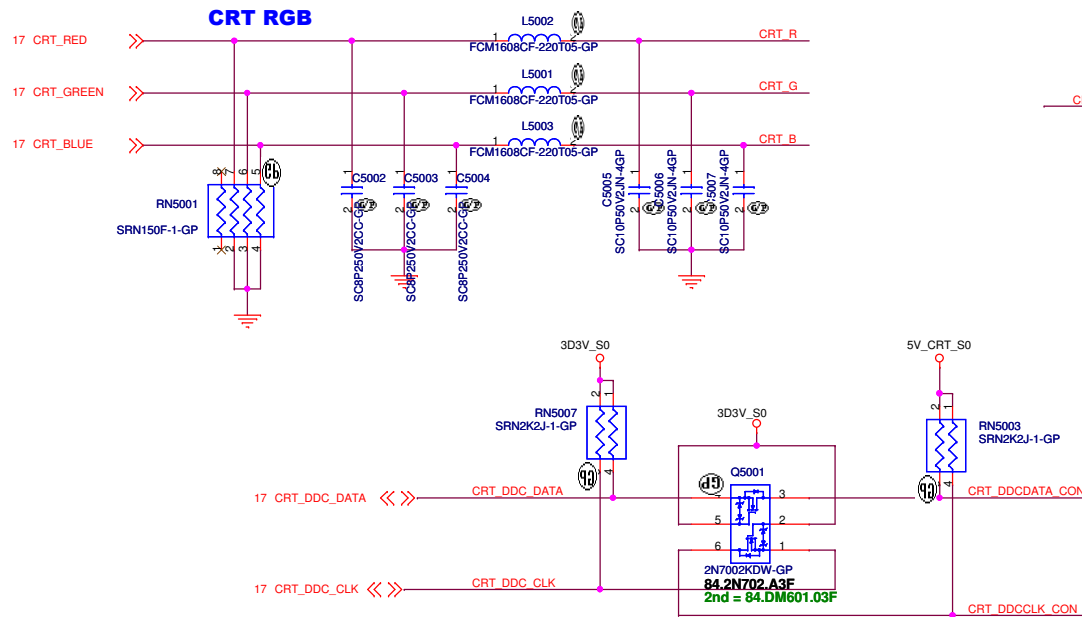
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
LCD Connector		
Title Size A3 Date: Thursday, June 02, 2011	Document Number Enrico/Caruso 15 HR	Rev X01
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SSID = VIDEO

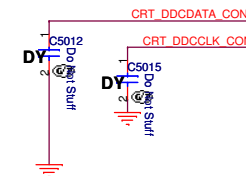
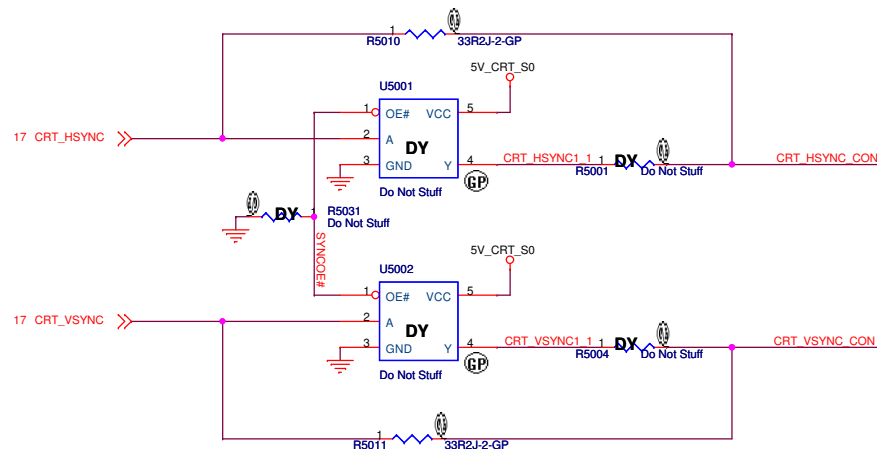
Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync



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Title

CRT Connector

Size	
Custom	

Document Number	
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Title			
Reserved			
Size	Document Number		Rev
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LVDS Switch			
Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
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DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size	Document Number		Rev
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SSID = User.Interface

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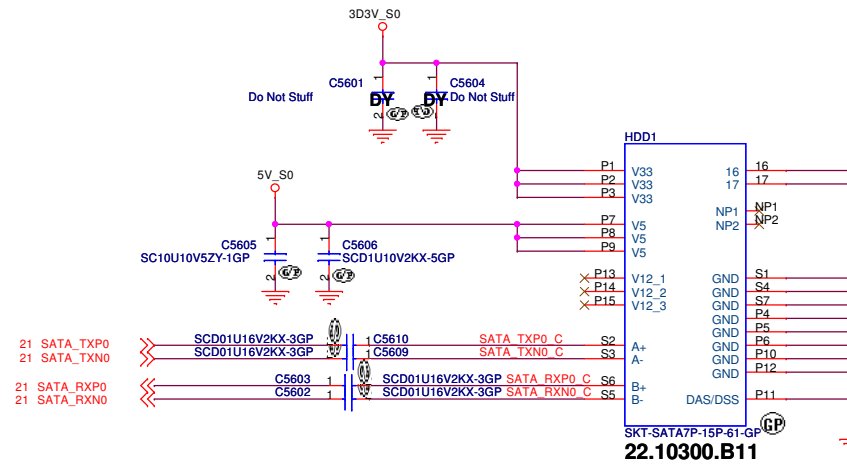
DV15 HR Vos GIGA HDMI NoSurge

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ITP/Fan Connector			
Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
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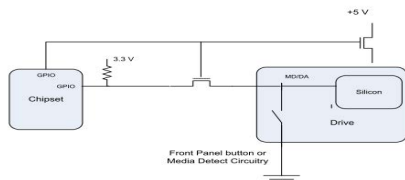
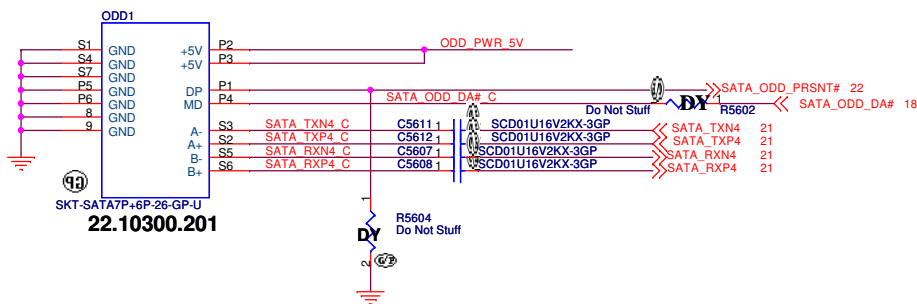
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SSID = SATA

SATA HDD Connector

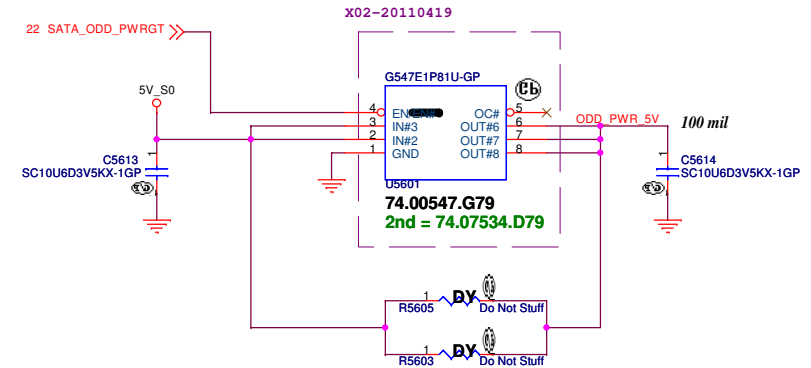
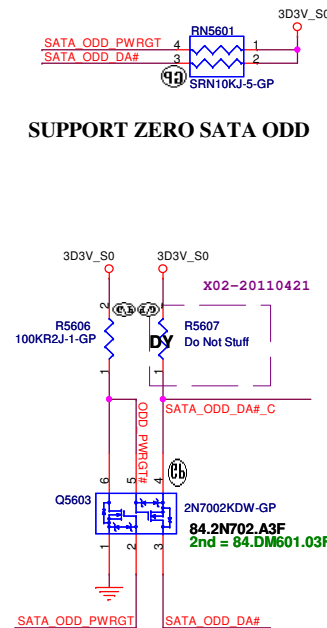


ODD Connector



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SUPPORT ZERO SATA ODD



DV15 HR Vos GIGA HDMI NoSurge



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Title			
HDD/ODD			
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SSID = ESATA

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Taipei Hsien 221, Taiwan, R.O.C.

Title **ESATA**

Size A3	Document Number Enrico/Caruso 15 HR	Rev X01
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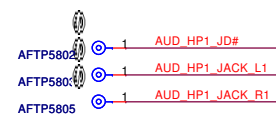
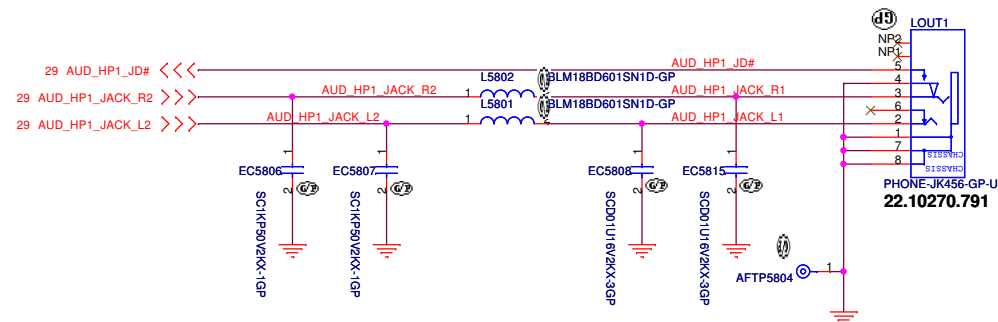
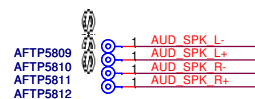
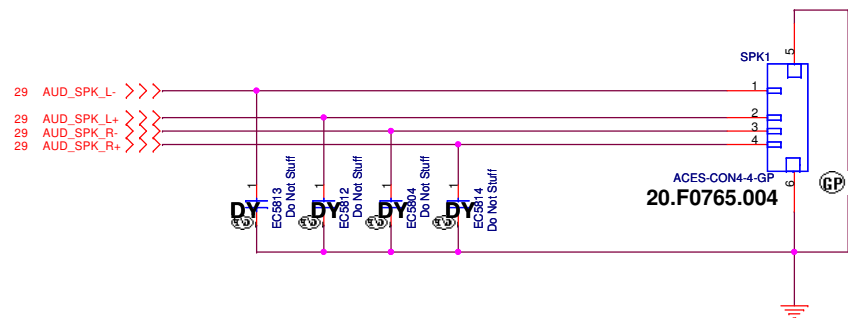
Date: Thursday, June 02, 2011	Sheet 57 of 104
-------------------------------	-----------------

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SSID = AUDIO

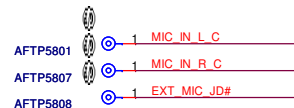
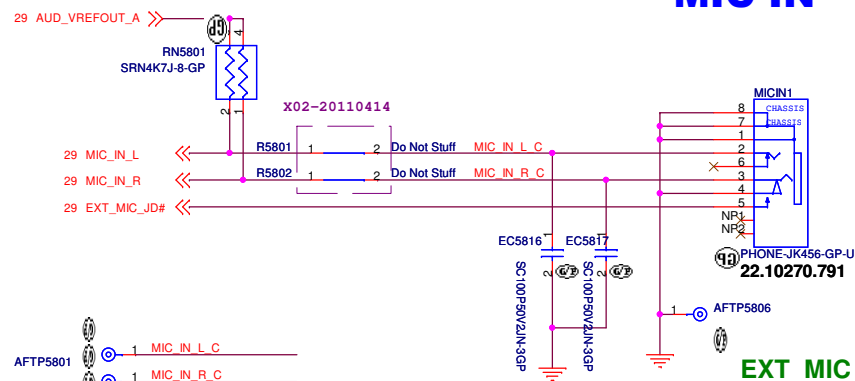
WWW.AliSaler.Com

Speaker Connector



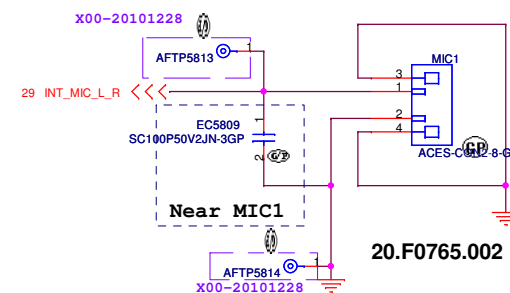
AUD_HP1_JD#
Normal Open

MIC IN



EXT_MIC_JD#
Normal Open

Internal Microphone



20.F0765.002

DV15 HR Vos GIGA HDMI NoSurge



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Taipei Hsien 221, Taiwan, R.O.C.

Title

SPEAKER CONN

Size
A3

Document Number

Enrico/Caruso 15 HR

Rev

X01

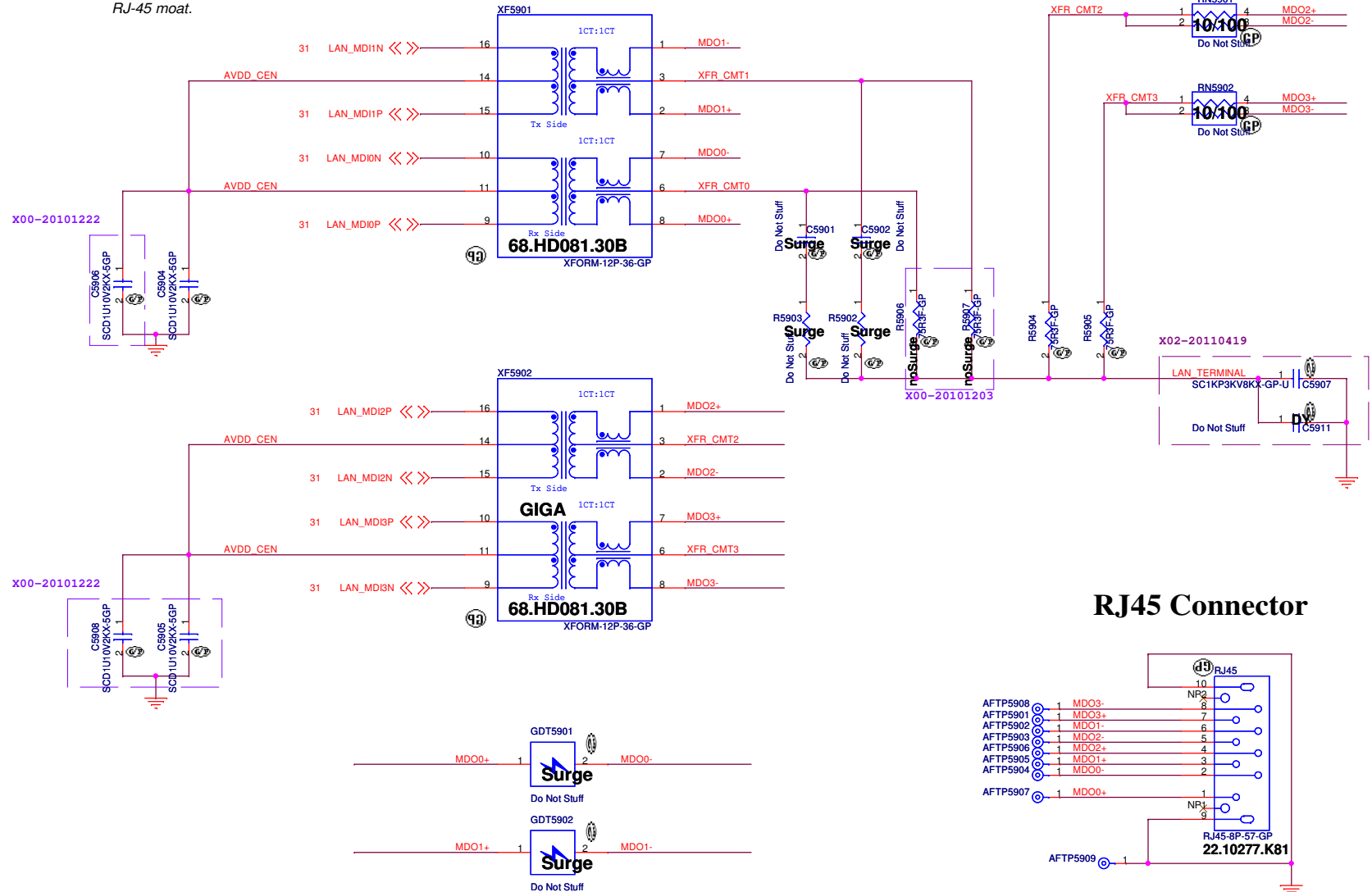
Date: Thursday, June 02, 2011

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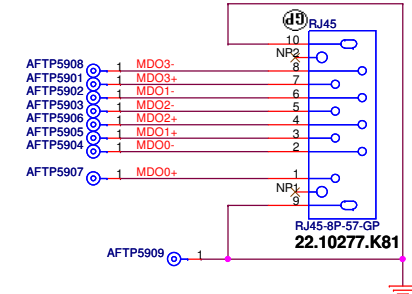
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

10/100M Lan Transformer

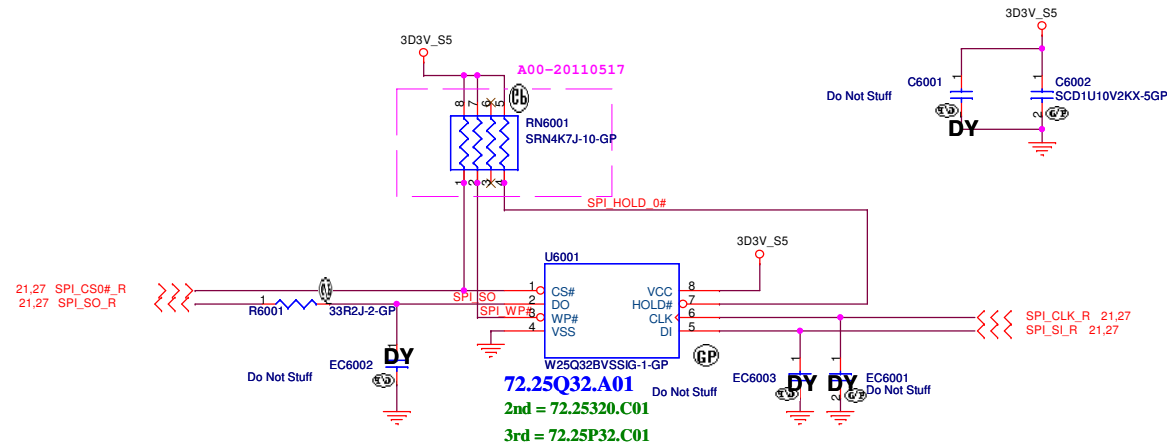


RJ45 Connector

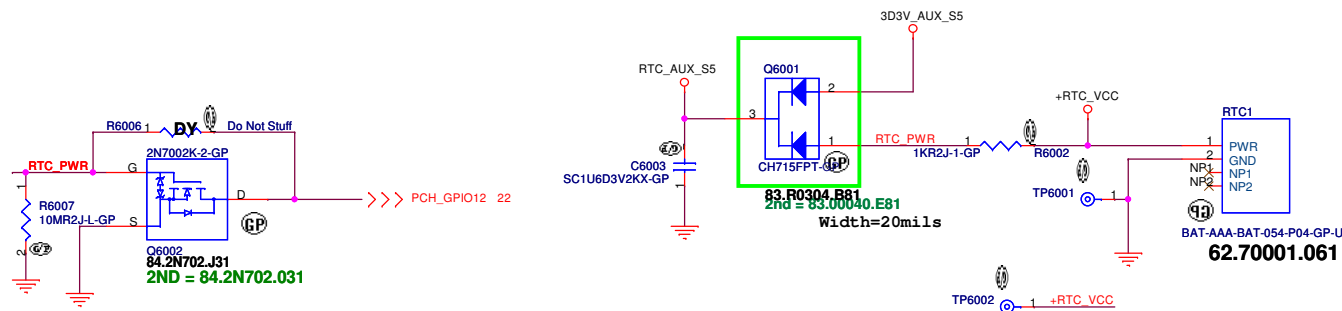


DV15 HR Vos GIGA HDMI NoSurge

SPI FLASH ROM (4M byte) for PCH



SSID = RBATT



DV15 HR Vos GIGA HDMI NoSurge



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Title

Flash/RTC

Size
A3

Document Number

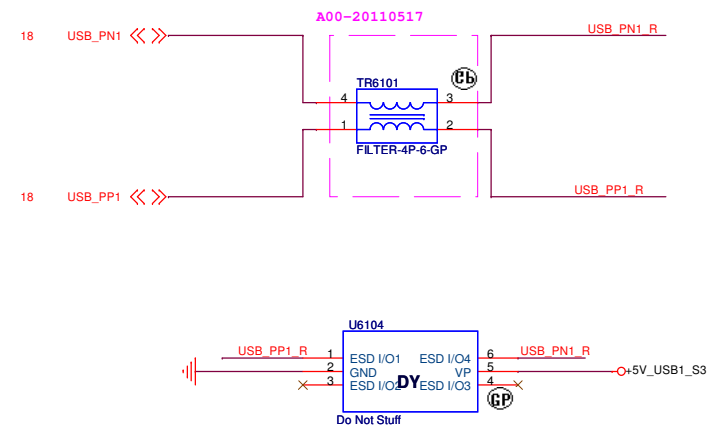
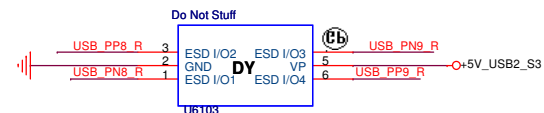
Enrico/Caruso 15 HR

Rev	
X01	

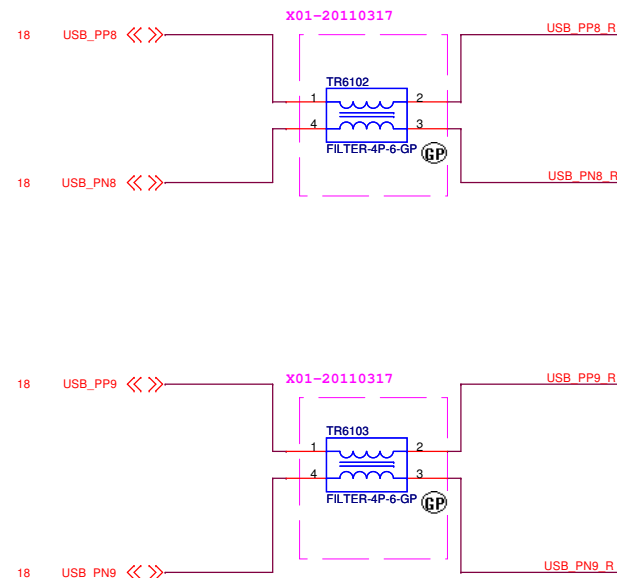
Date: Thursday, June 02, 2011

Sheet	60	of	104
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Left USB Power x1

[illegible]

X01-20110314



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USB Power SW


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Title			
Reserved			
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SSID = User.Interface

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Bluetooth

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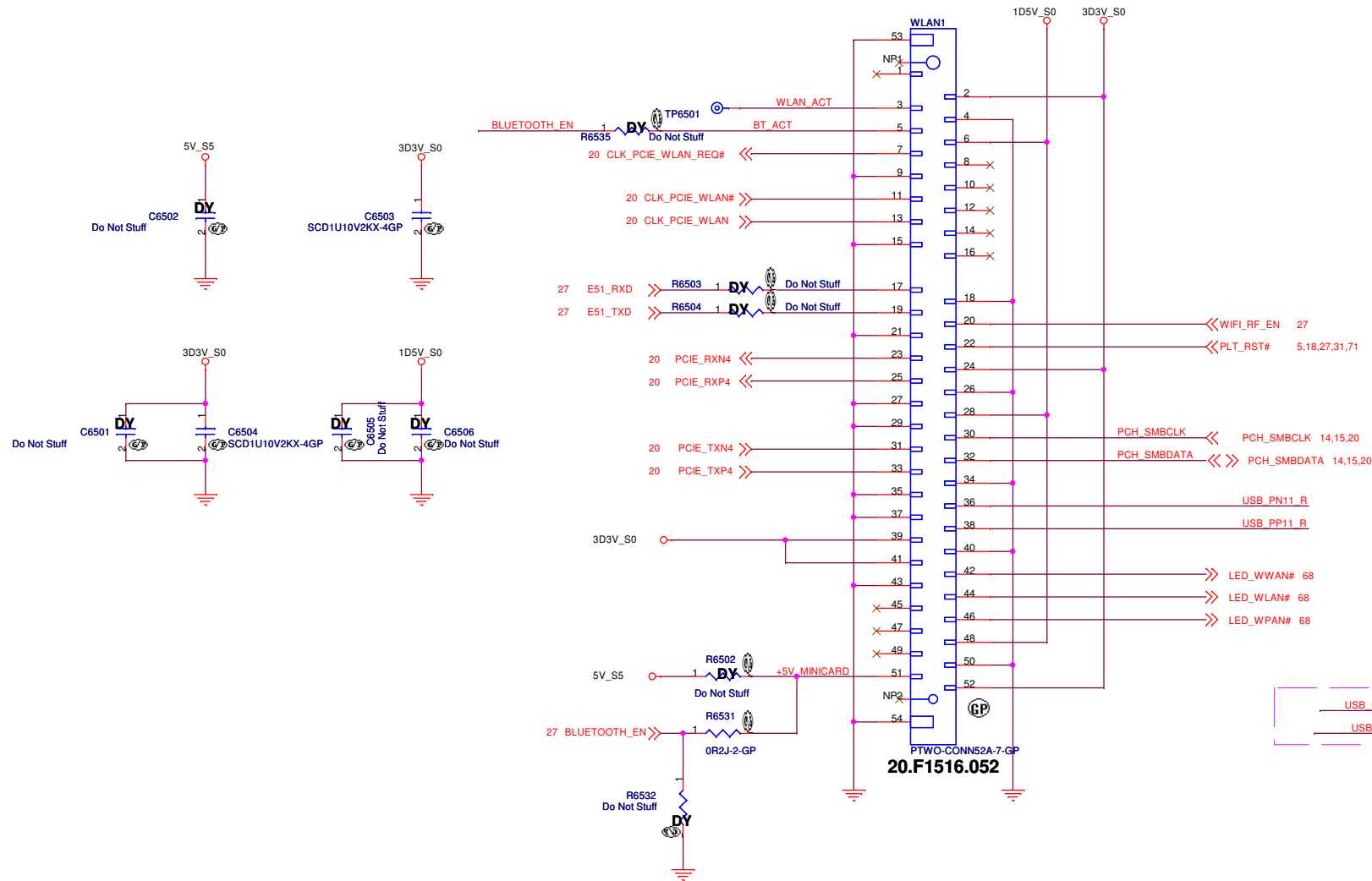


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Title			RESERVED	
Size	Document Number			Rev
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SSID = Wireless

Mini Card Connector(802.11b/g/n)




USB_PN11_R 2 1 Do Not Stuff USB_PN11 18
 USB_PP11_R 2 1 Do Not Stuff USB_PP11 18
 R6534 Do Not Stuff
 R6533 Do Not Stuff
 A00-20110525

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Title			RESERVED		
Size	Document Number	Rev			
A3	Enrico/Caruso 15 HR	X01			
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Title			
Reserved			
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Title

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Document Number
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Date: Thursday, June 02, 2011

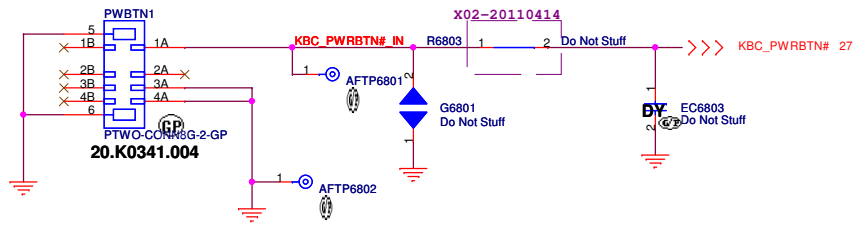
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Reserved

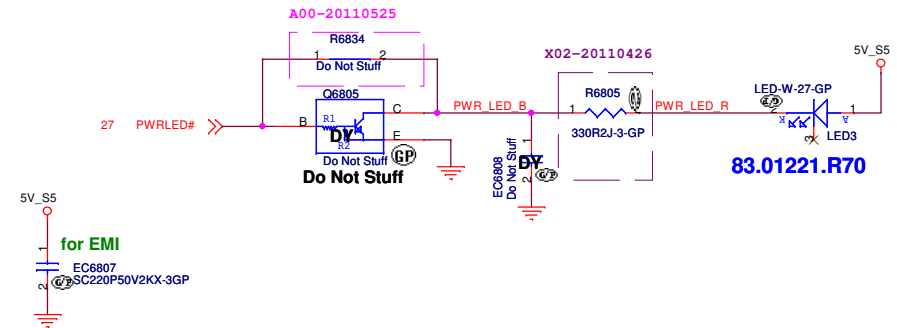
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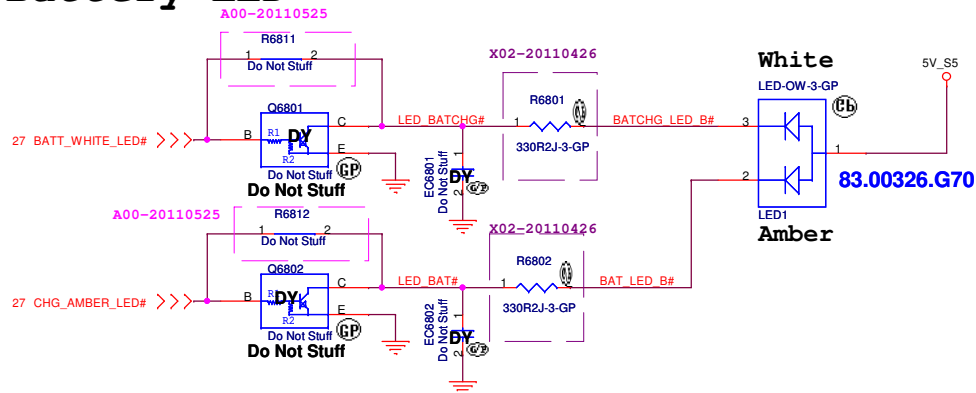
Power BTN Connector



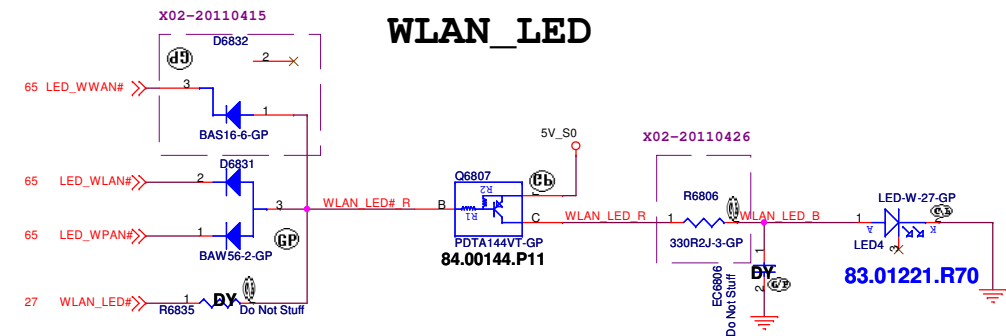
Power LED



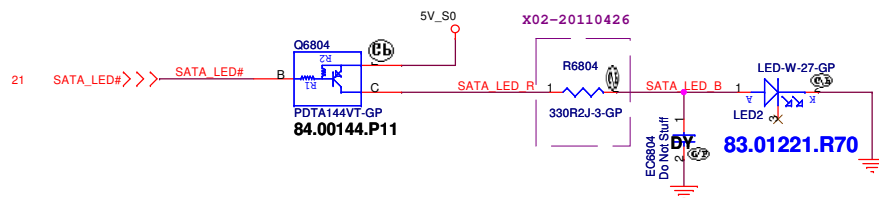
Battery LED



WLAN_LED



HDD LED



LED Location from left to right
(MB, Top View)

LED3 PWR LED2 HDD LED1 Battery LED4 WiFi

DV15 HR Vos GIGA HDMI NoSurge

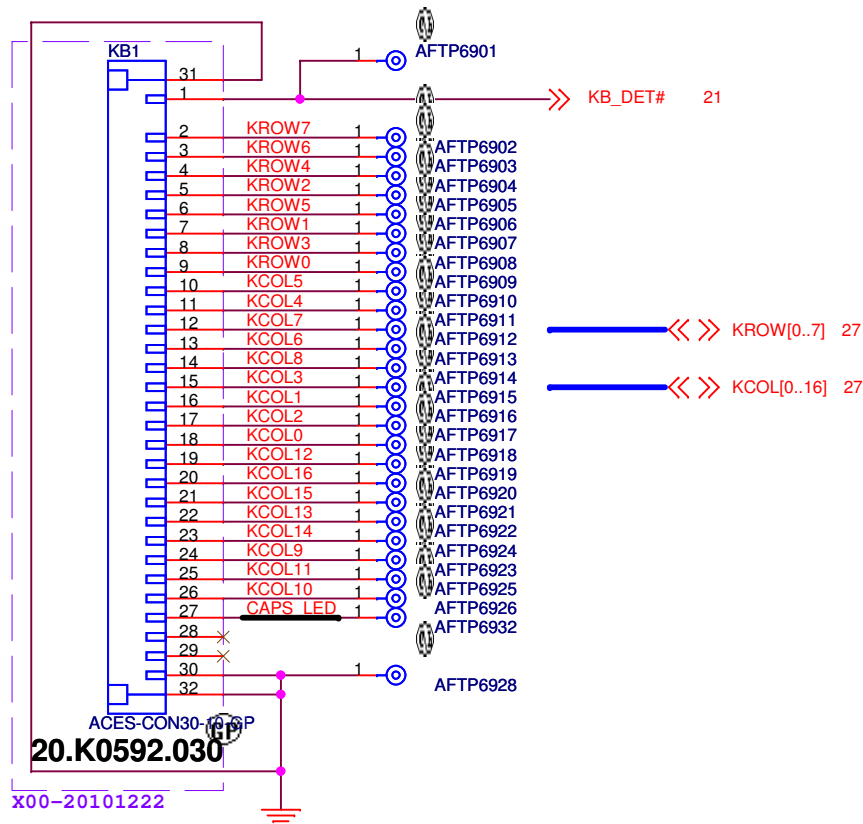


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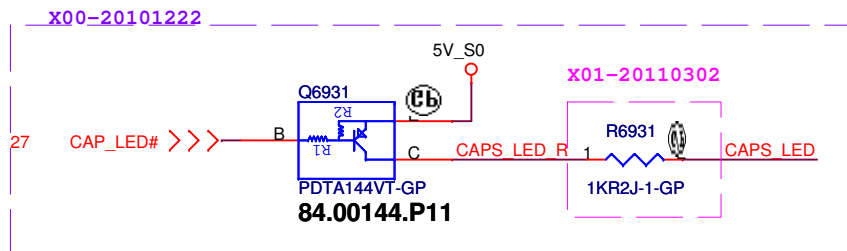
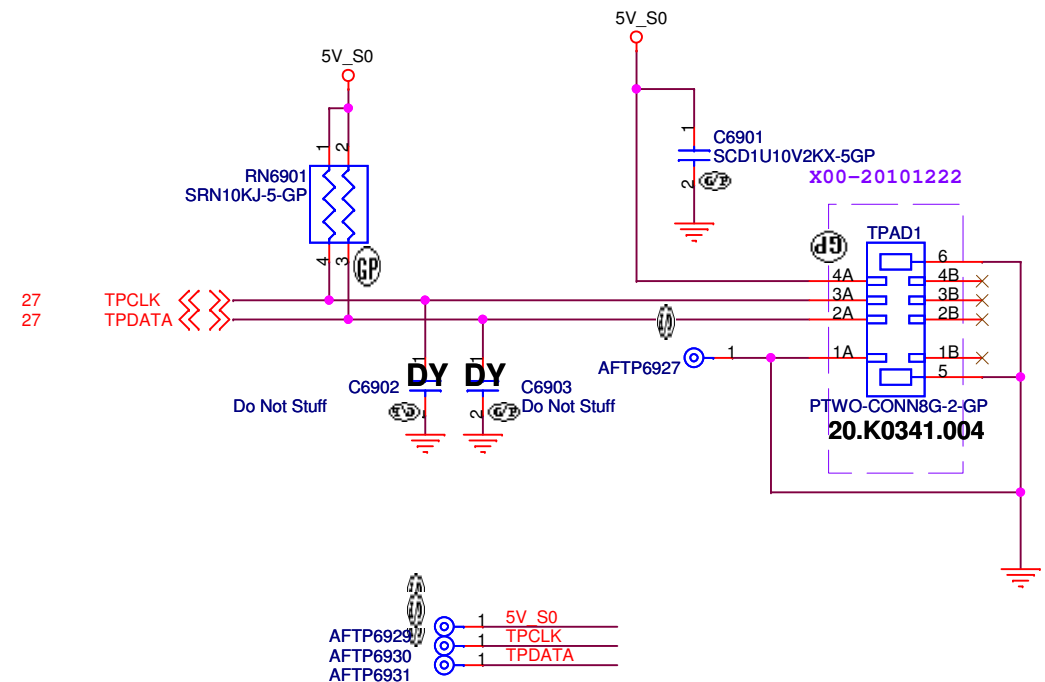
Title			LED Bard/Power Button
Size	Document Number	Rev	
A3		X01	
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Internal KeyBoard Connector



TouchPad Connector



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Title

Key Board/Touch Pad

Size

Document Number

Rev

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X01

Date: Thursday, June 02, 2011

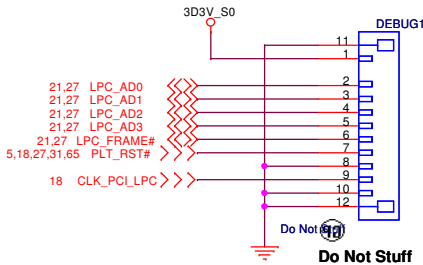
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Title		
Hall Sensor		
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Title			Dubug connector	
Size	Document Number			Rev
A3		Enrico/Caruso 15 HR		X01
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DV15 HR Vos GIGA HDMI NoSurge

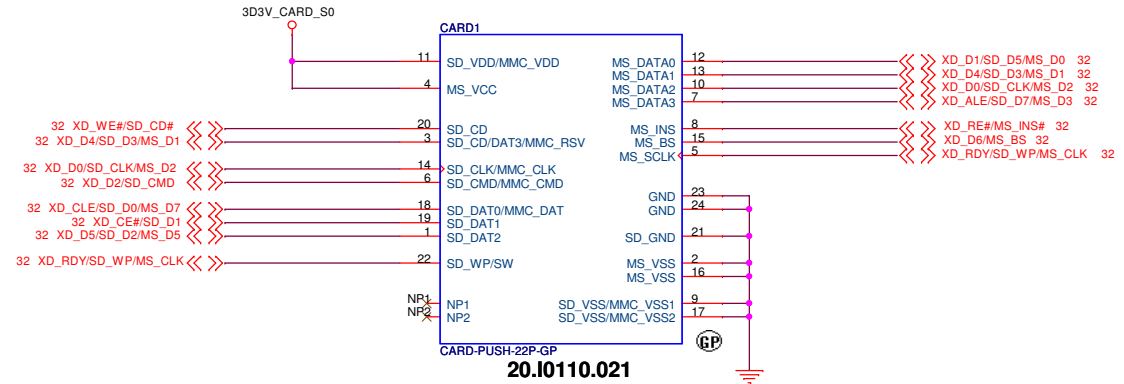
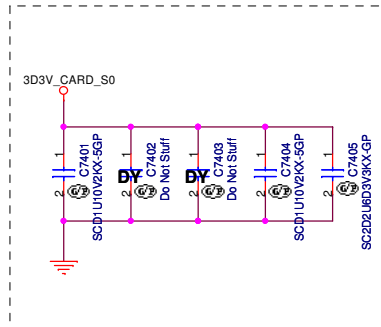
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Size	Document Number		Rev
A3	Enrico/Caruso 15 HR		X01
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DV15 HR Vos GIGA HDMI NoSurge

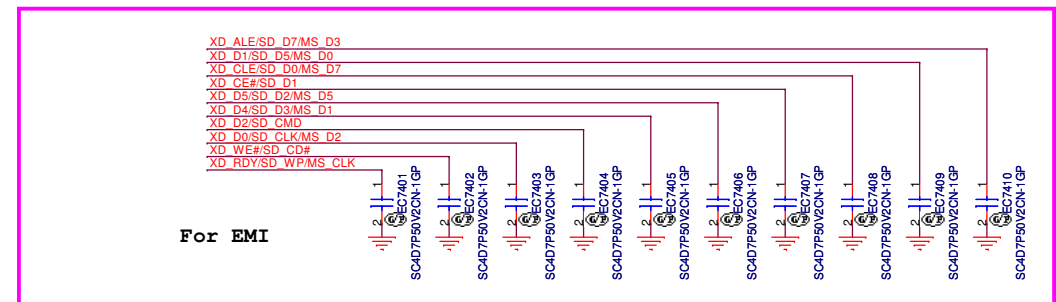
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Title			
Reserved			
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SSID = SDIO

SD/MMC/MS Card Reader



X01-20110315



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Title		
SD/MS/MMC Card CONN		
Size	Document Number	Rev
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SSID = ExpressCard

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Title			Express Card	
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A3	Enrico/Caruso 15 HR		X01	
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Reserved			
Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
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Title			
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Size A3	Document Number Enrico/Caruso 15 HR		Rev X01
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Title			
Reserved			
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SSID = User.Interface

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title			Free Fall Sensor	
Size	Document Number	Rev		
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Title			
Reserved			
Size	Document Number		Rev
A3	Enrico/Caruso 15 HR		X01
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Reserved			
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Title

IO Board Connector

Size
A3

Document Number
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Date: Thursday, June 02, 2011

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Title		
GPU PCIE/STRAPPING(1/5)		
Size	Document Number	Rev
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DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinshih, Taipei Hsien 221, Taiwan, R.O.C.			
File GPU_DP/LVDS/CRT/GPIO(3/5)			
Size PC	Document Number Enrico/Caruso 15 HR		Rev X01
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Title

GPU-VRAM1,2 (1/4)

Size
Custom

Document Number
Enrico/Caruso 15 HR

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Thursday, June 02, 2011

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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
GPU-VRAM3,4 (2/4)					
Size	Document Number				Rev
Custom	Enrico/Caruso 15 HR				X01
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		Wistron Corporation <small>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</small>	
Title			
GPU-VRAM5,6 (3/4)			
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Title

GPU-VRAM7,8 (4/4)

Size
A3

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Title		
RT8208B +VGA CORE		
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Wistron Corporation
 21F, 6th, Sec.1, Hsin Tsu Yiu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

Title

DISCRETE VGA POWER

Size

Document Number

Rev

A2

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X01

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title		
LVDS Switch		
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Title		
CRT Switch		
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SSID = SDIO

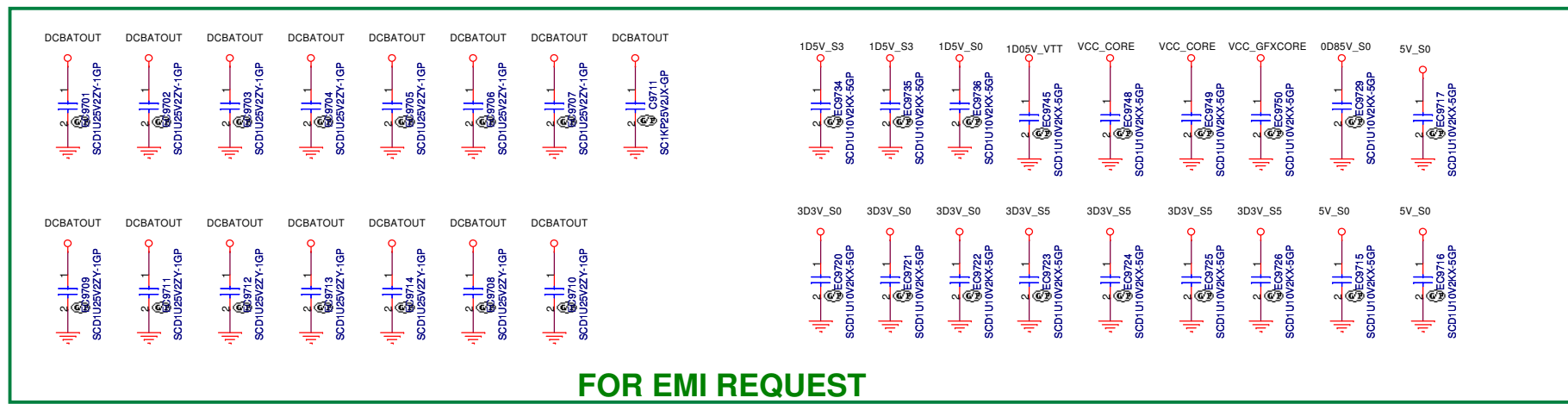
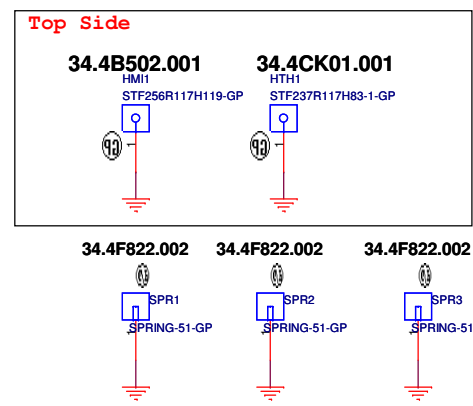
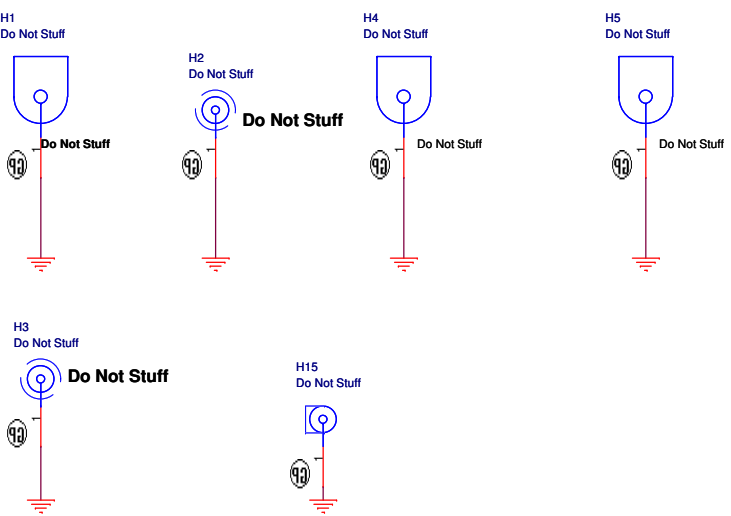
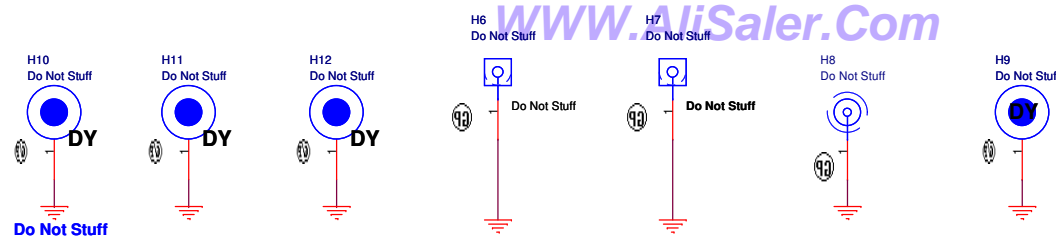
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TOUCH PANEL			
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SSID = Mechanical



FOR EMI REQUEST

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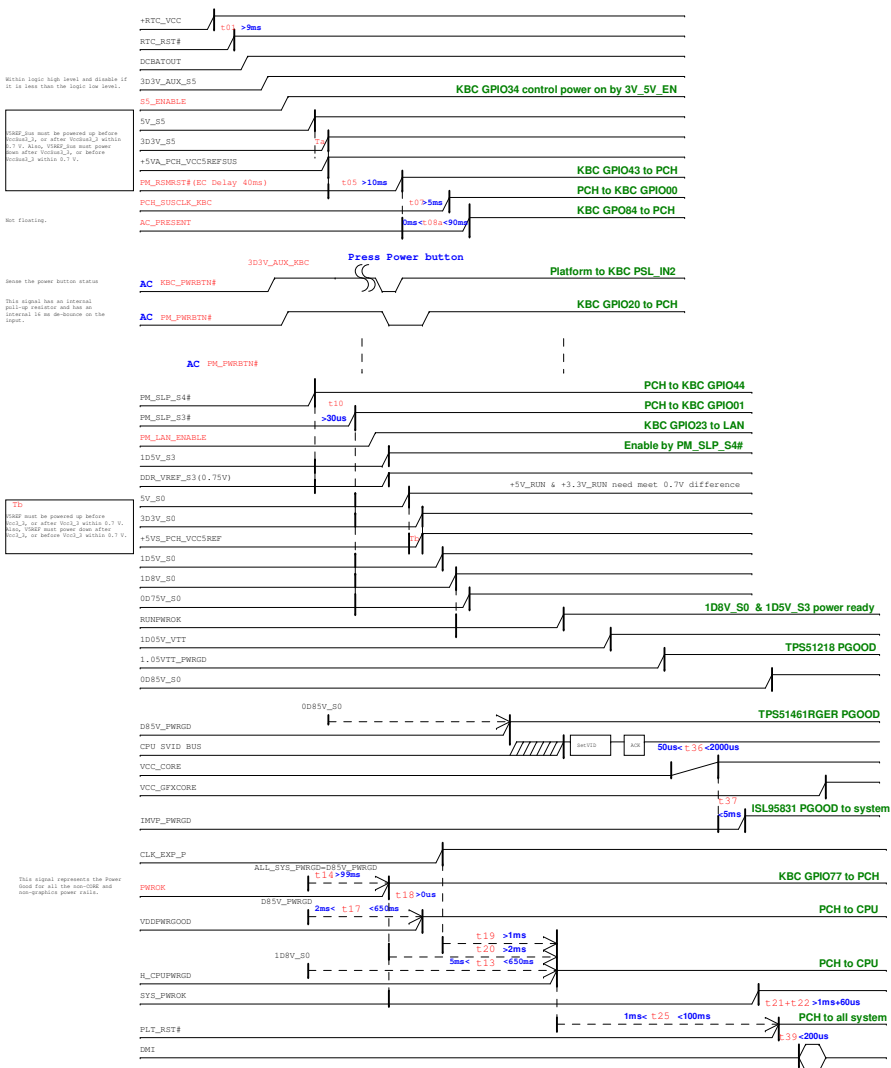
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Size: A3 Document Number: **Enrico/Caruso 15 HR** Rev: **X01**

Date: Thursday, June 02, 2011 Sheet: 97 of 104

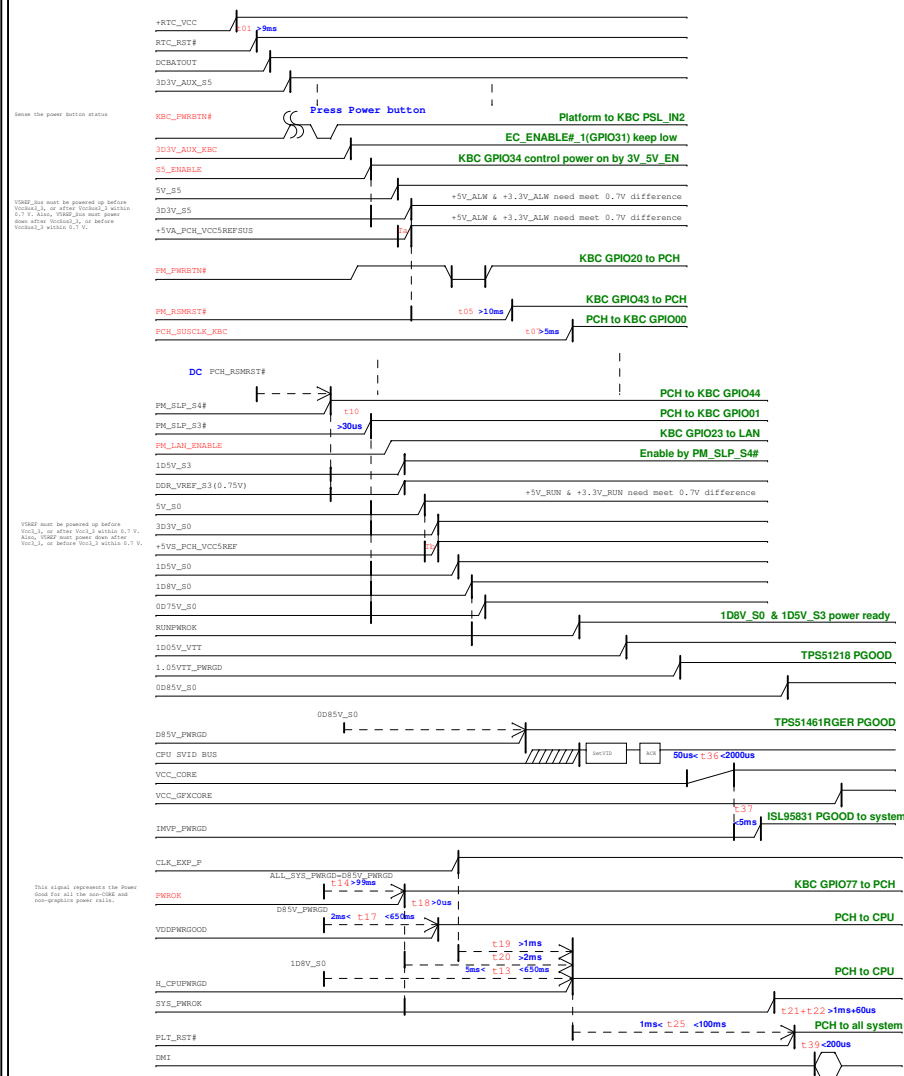
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red word: KBC GPIO

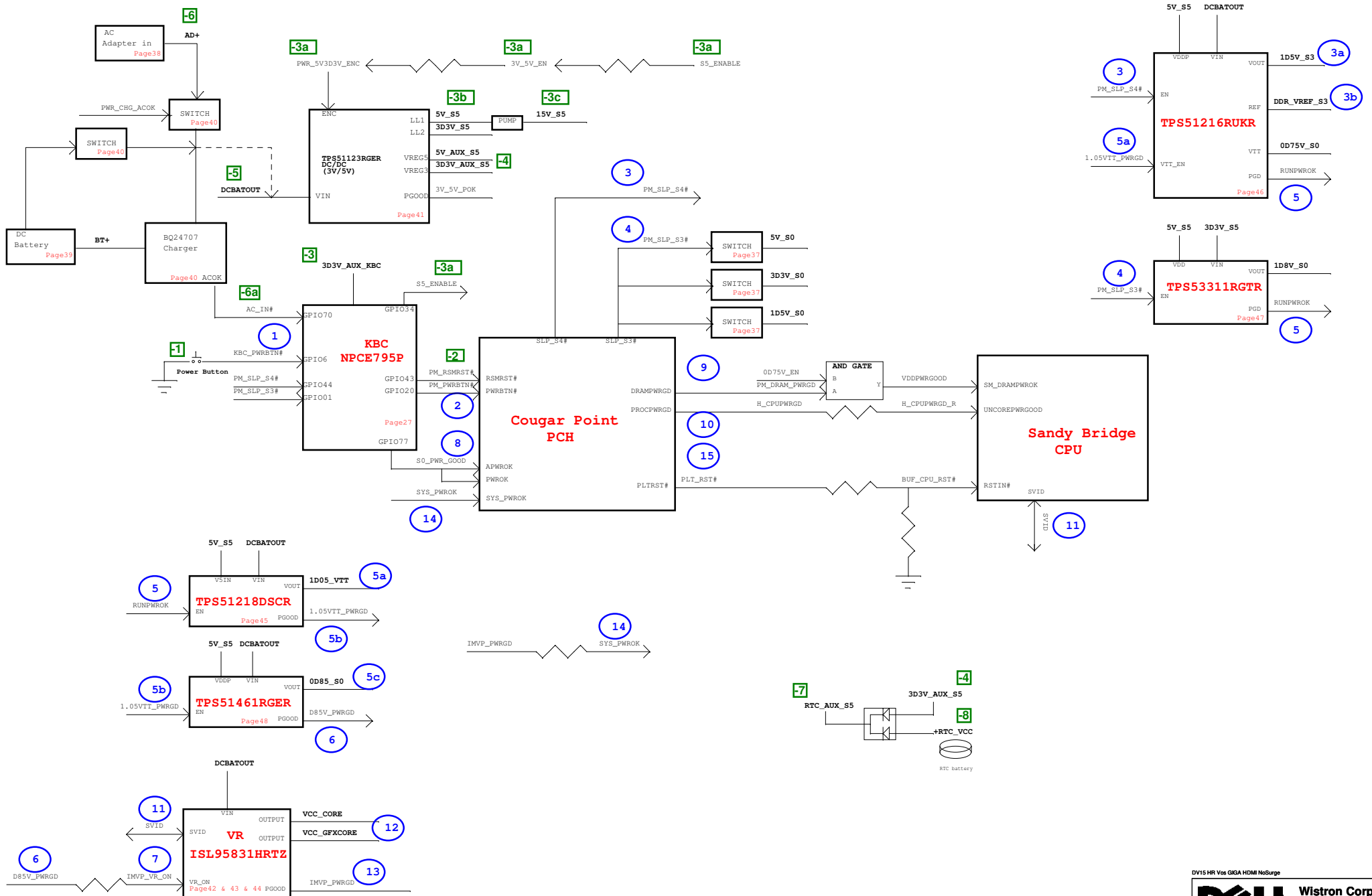


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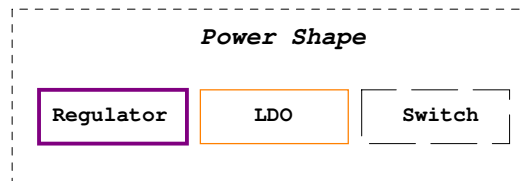
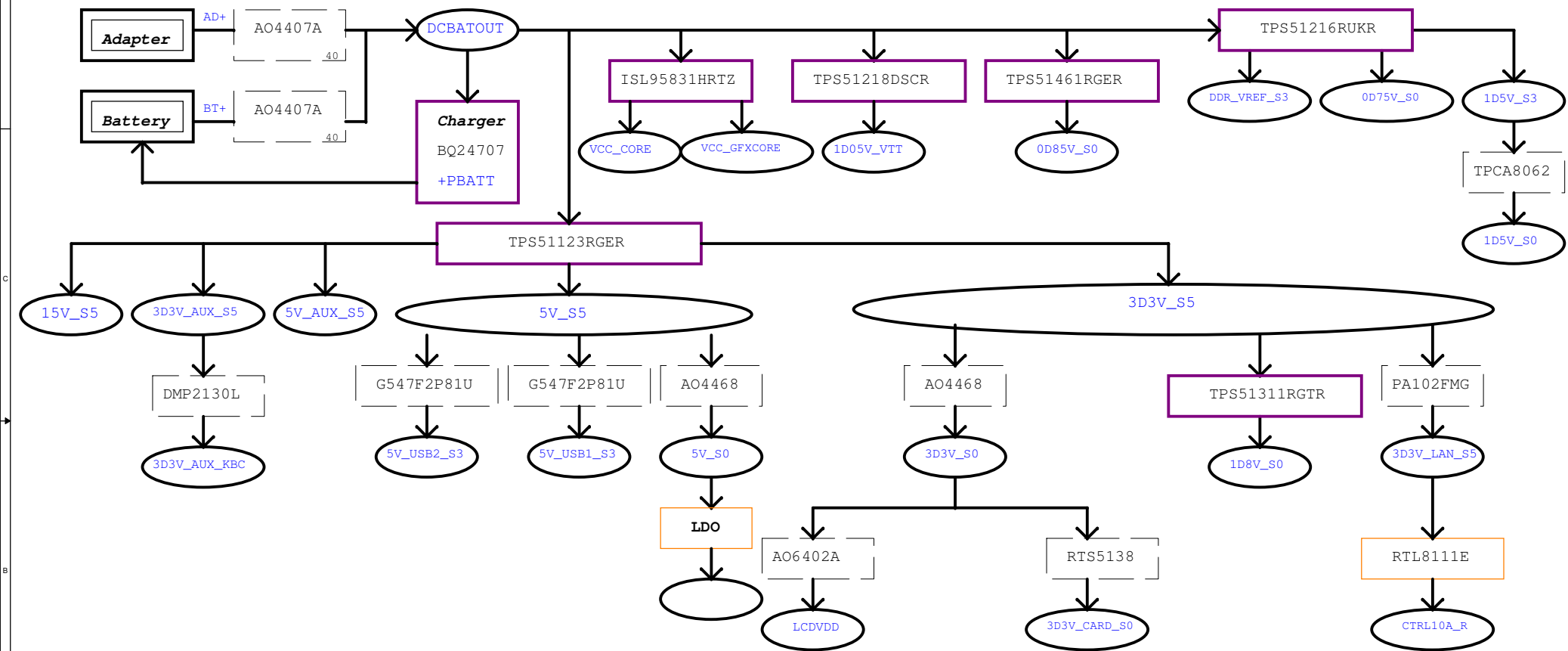
red word: KBC GPIO



Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 15



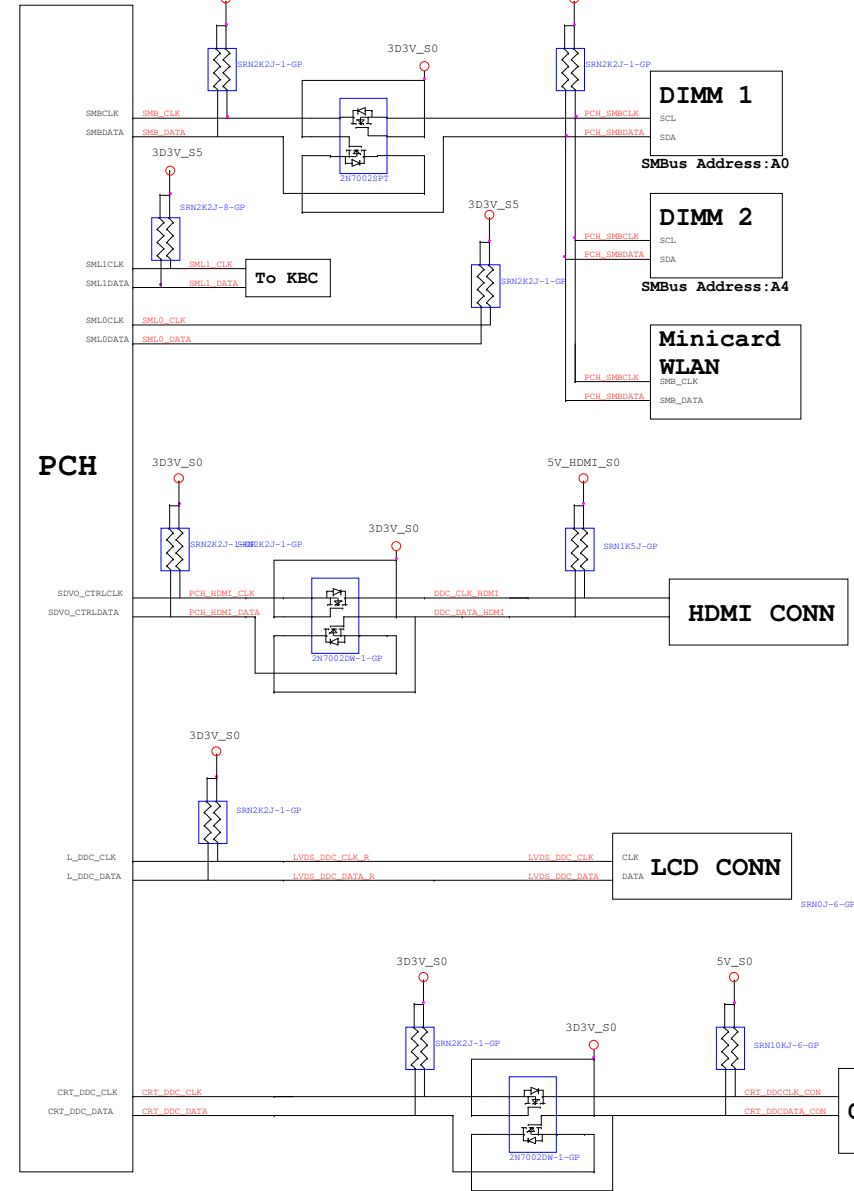
DV15 HR Vos GIGA HDMI NoSurge



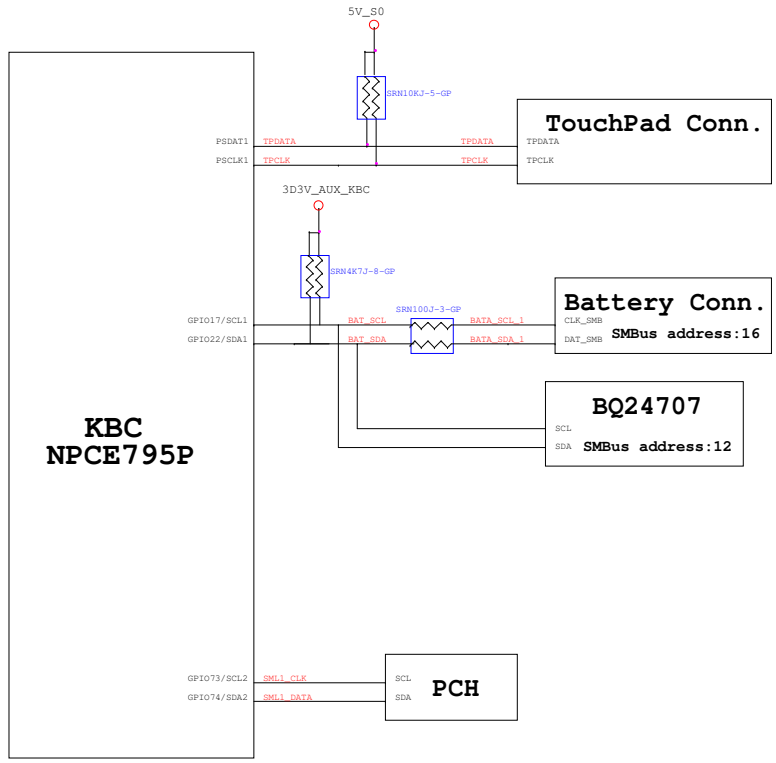
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title				
<i>Power Block Diagram</i>				
Size	Document Number			Rev
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PCH SMBus Block Diagram

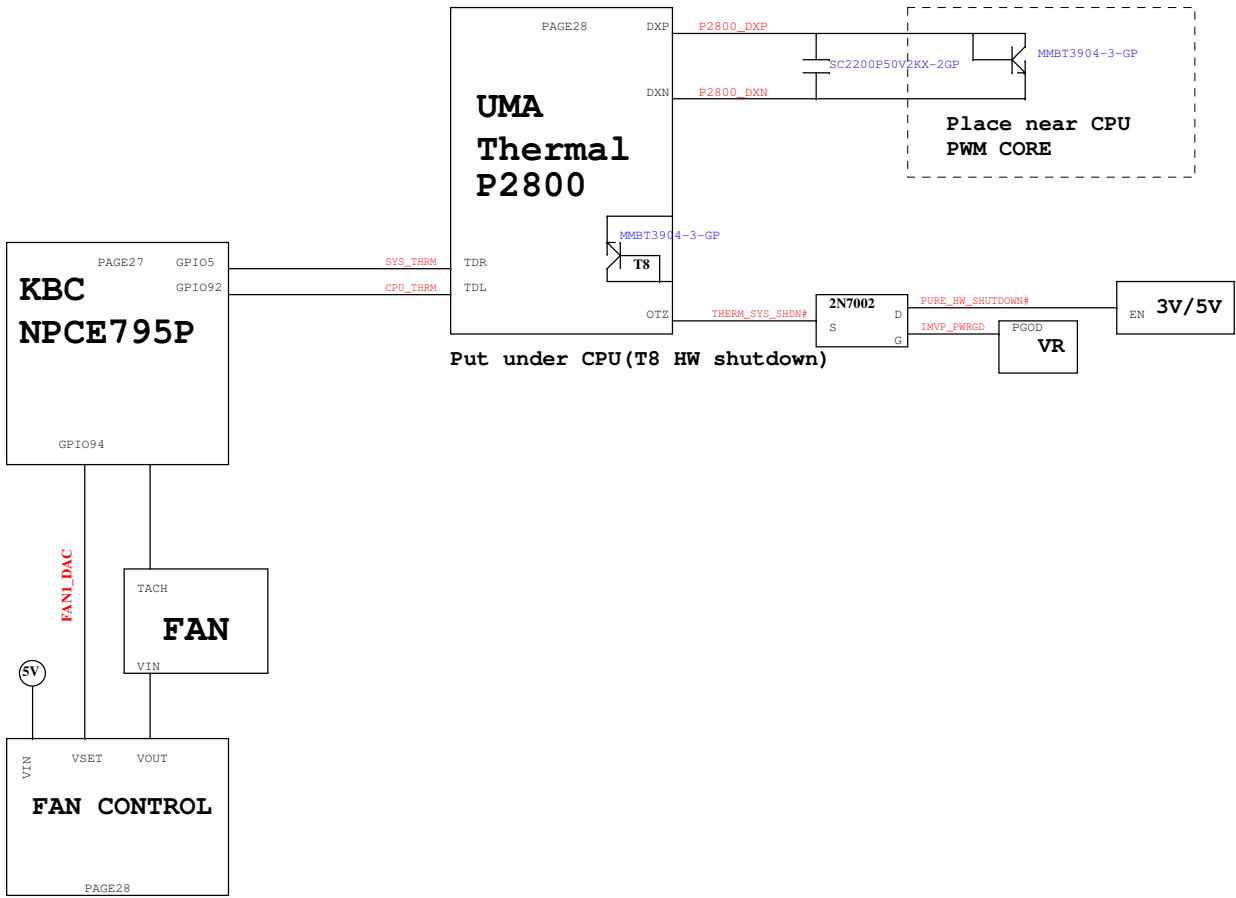


KBC SMBus Block Diagram

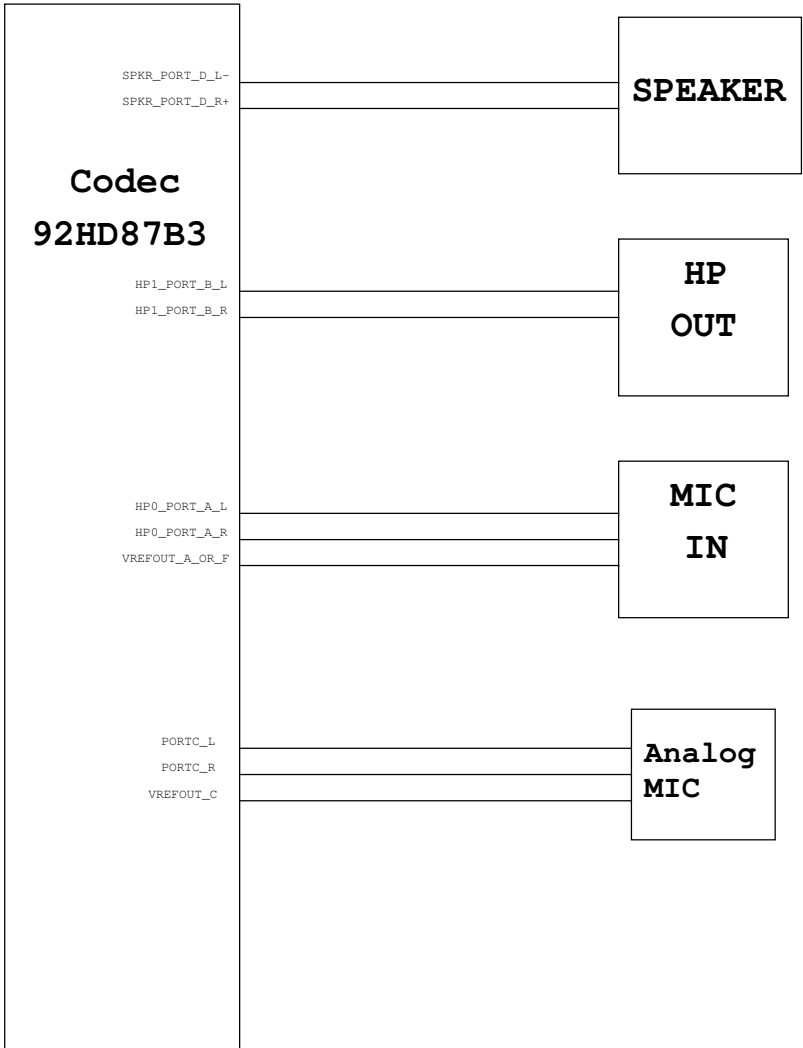


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Thermal Block Diagram



Audio Block Diagram



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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Change History</i>			
Size A3	Document Number	<i>Enrico/Caruso 15 HR</i>	
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