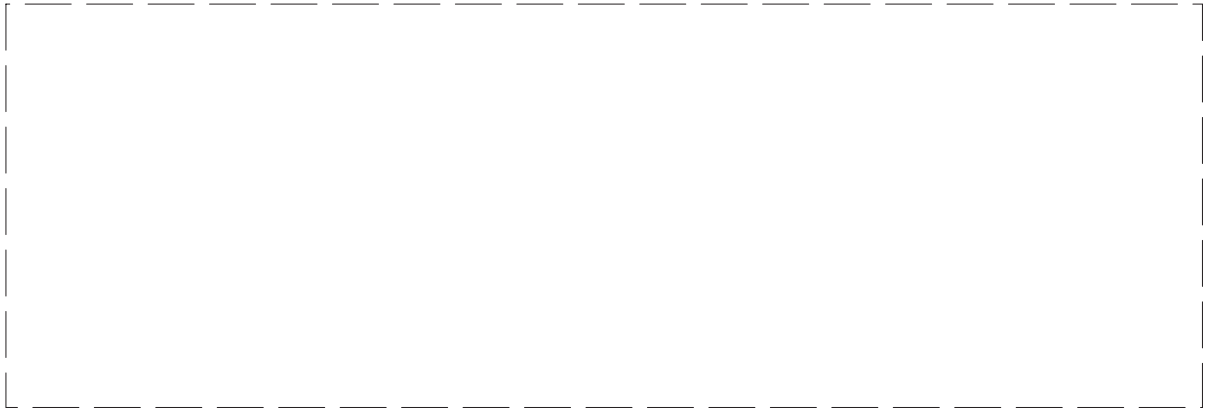
Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-03

REV : A00



<Core Design>

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Title		
Cover Page		
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##OnMainBoard

Berry Block Diagram (Discrete/UMA co-lay)

Project code : 91.4HH01.001
PCB P/N : 48.4HH01.0SA
Revision : 09909-1

1.Park-XT;512MB
(64Mx16b*4)
Dell P/N:9TGTN$AA HYNIX
Dell P/N:C995R$AA SAMSUNG
2.Park-XT;1GB (128Mx16b*4)
Dell P/N:PXFYJ$AA HYNIX
Dell P/N:C09DT$AA SAMSUNG
(1 and 2 co-lay)

VRAM 1GB/512MB 85,86,87,88
DDR3 800MHz
Clock Generator SLG8SP585 7
Park-XT (Discrete only) 80,81,82,83,84
PCIe x 16 (Discrete only)
Intel CPU Arrandale 8,9,10,11,12,13,14
DDRIII 800/1066 Channel A
DDRIII 800/1066 Channel B
DDRIII 800/1066 Slot 0 18
DDRIII 800/1066 Slot 1 19
FDIx4x2 (UMA only)
DMIx4
Discreet/UMA Co-lay
HDMI 57
LCD 54
HDMI
Level shifter 57
LVDS(Dual Channel)
RGB CRT
CRT
Left Side: USB x 2
CRT Board 77
Bluetooth 73
CAMERA 54
USB2.0 x 4
AZALIA
Intel PCH
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28
PCIE x 3
SATA x 1
USB 2.0 x 4
USB 2.0 x 1
I/O Board Connector 76
PCIE x 1 USB x 1
PCIE x 1
Mini-Card 802.11a/b/g
10/100 NIC Realtek RTL8103T-VB
RJ45 CONN
SATAx1 / USB2.0x1
ESATA/USB Combo
PCIE x 1,USB x 1
Mini-Card WWAN
SIM
USB 2.0 x 1
Right Side: USB x 1
CardReader Realtek RTS5159 78
SD/MMC+/MS/ MS Pro/xD
Internal Analog MIC
HP1
MIC IN
2CH SPEAKER
Azalia CODEC IDT 92HD79B1 30
SPI
Flash ROM 4MB 62
LPC Bus
LPC debug port 70
SATA x 2
HDD 59
ODD 59
KBC NUVOTON NPCE781BA0DX 37
SPI
SMBus
Flash ROM 256kB 62
Touch PAD
Int. KB
Thermal Main:G7922 Sec.EMC2102
Fan 58

CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA

SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.0V_RUN_VGA

Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

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Title: Block Diagram
Size: A3
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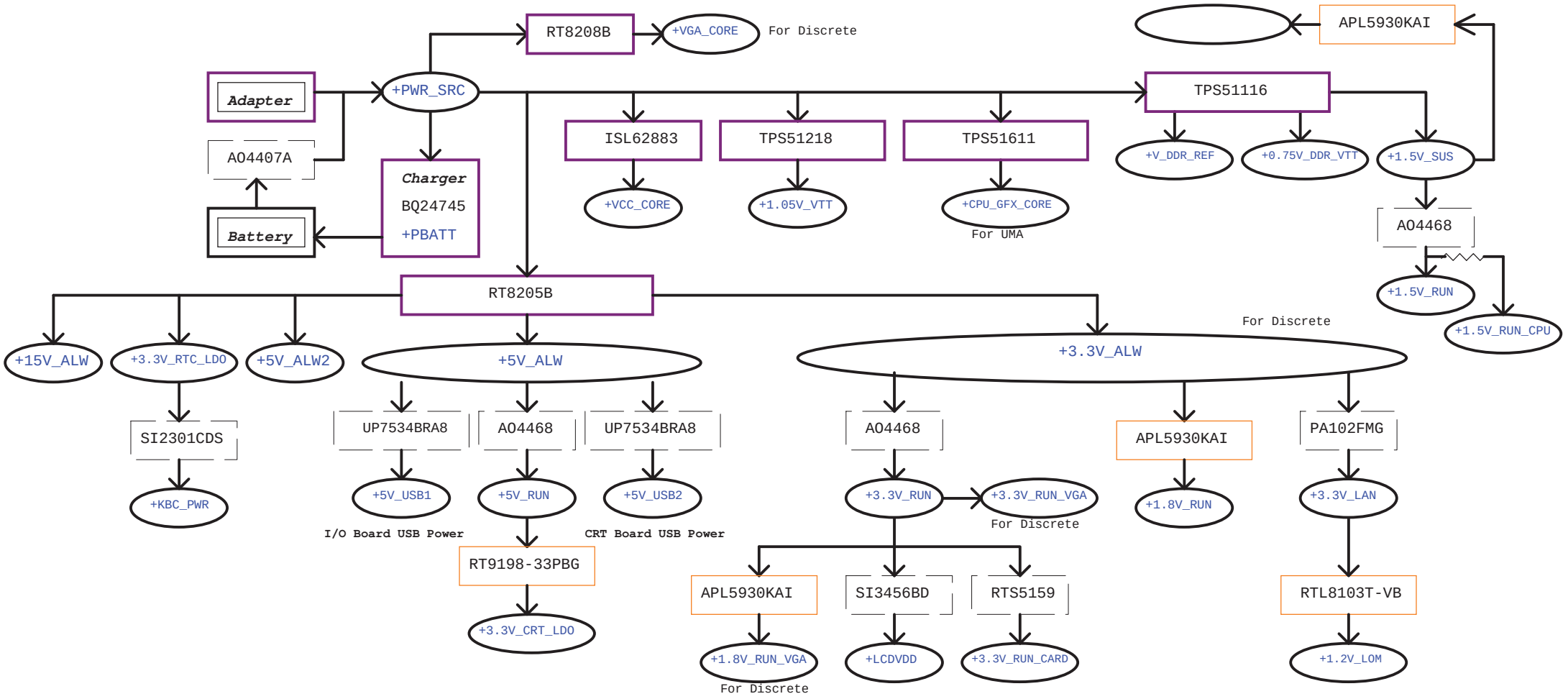

Power Shape

Regulator	LDO	Switch

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Title: *Power Block Diagram*

Size	Document Number	Rev
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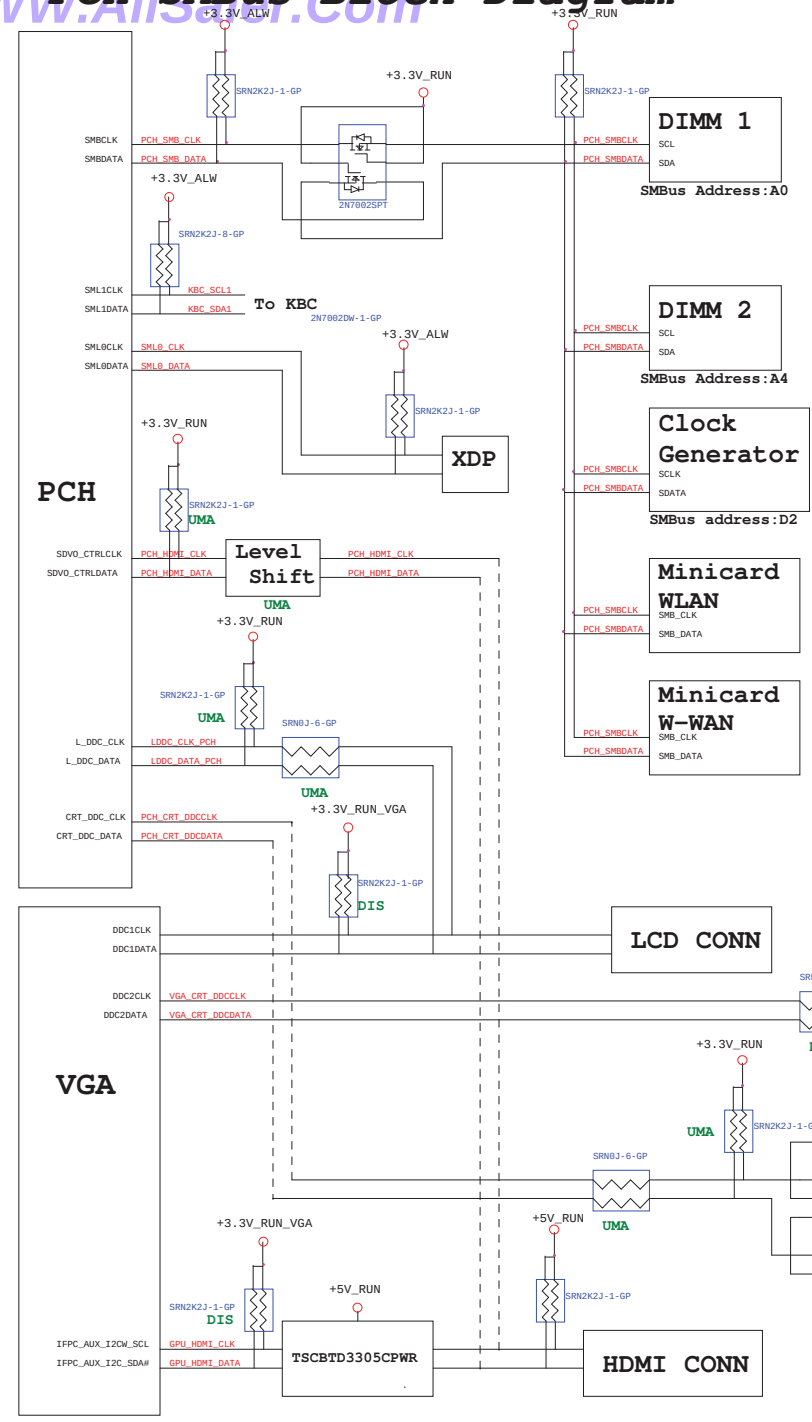
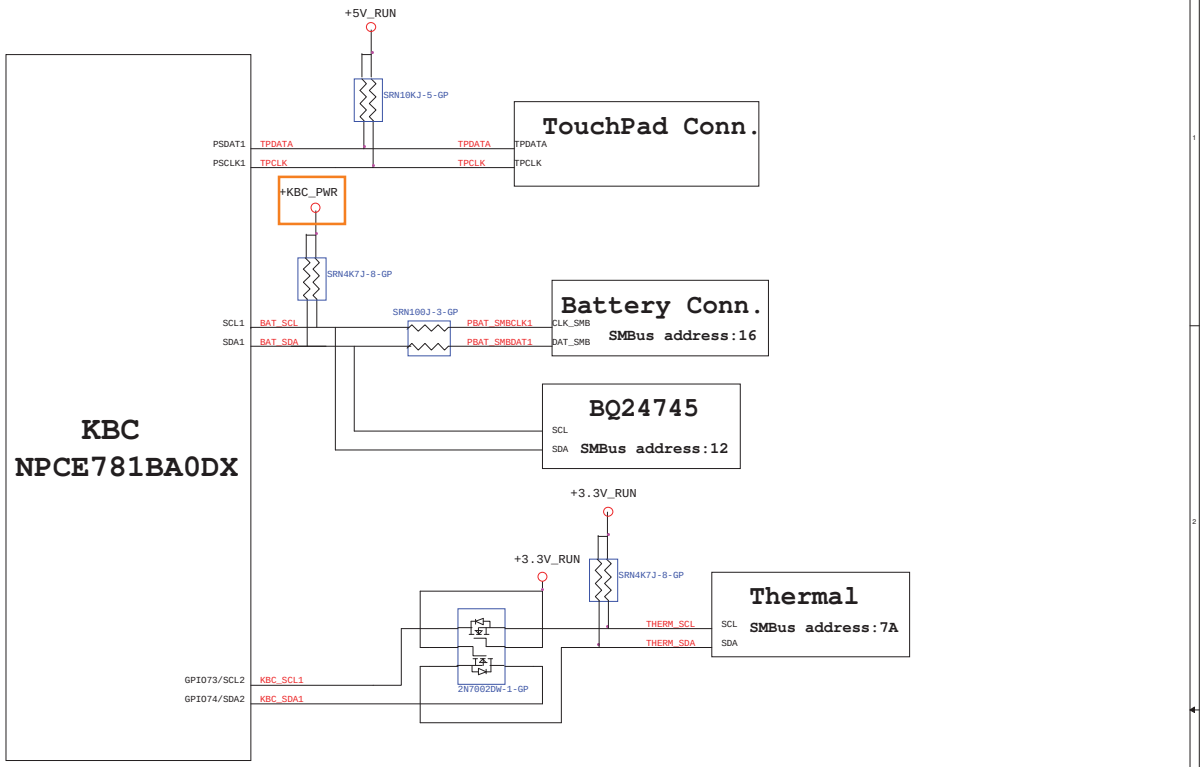
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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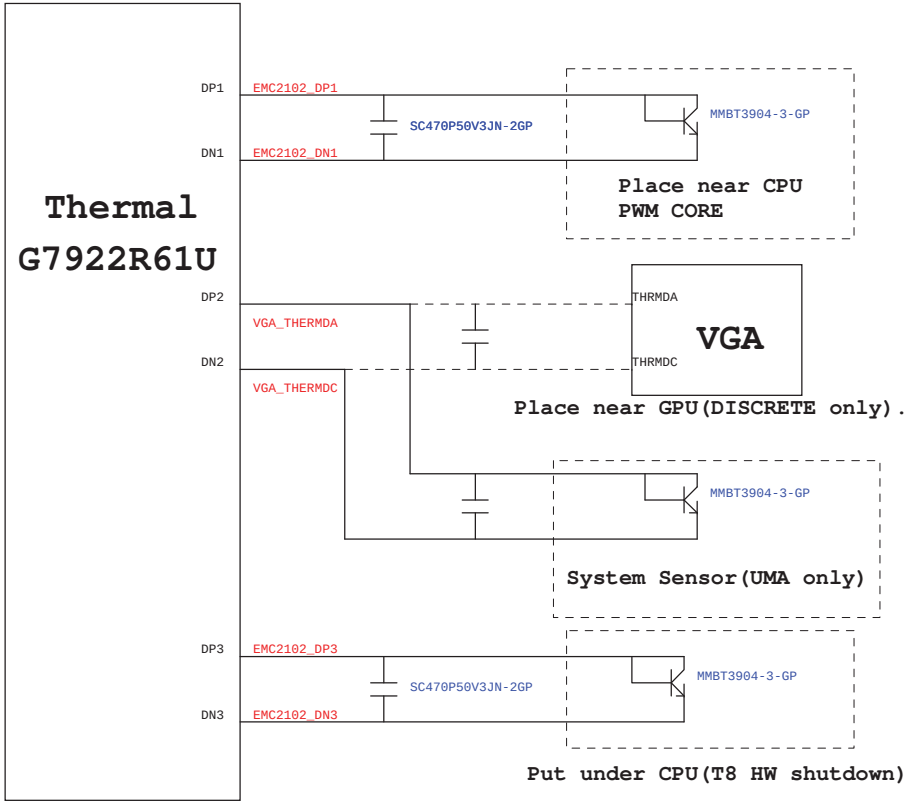
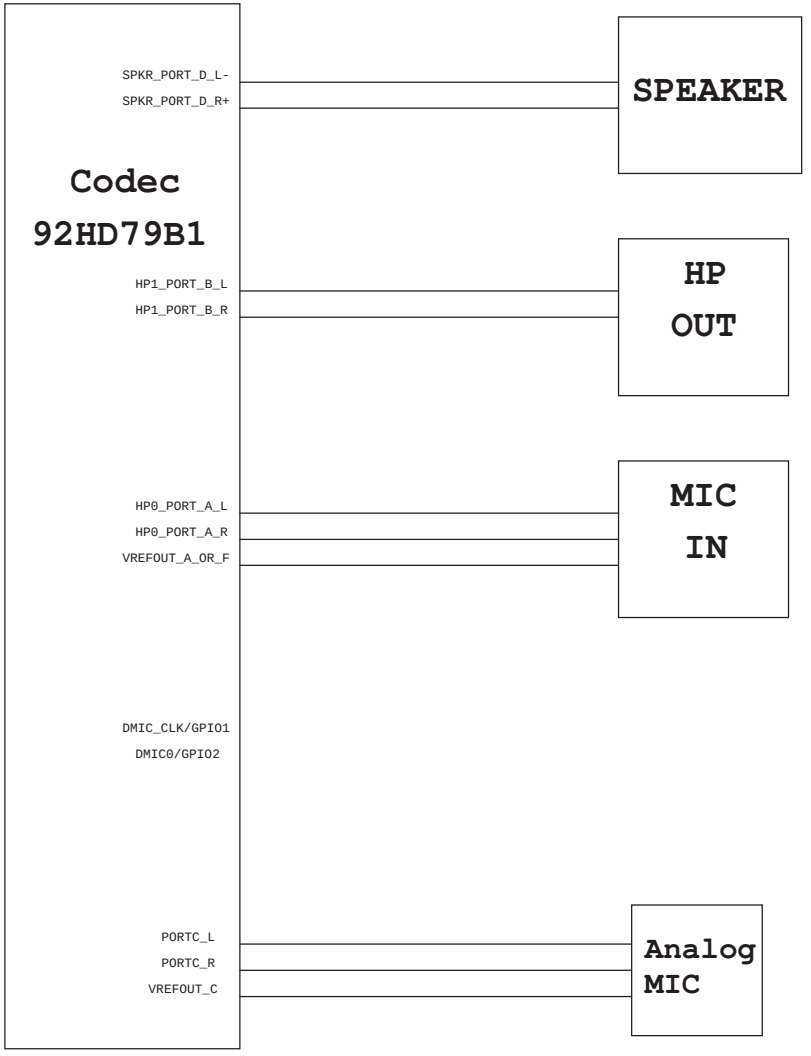
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

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Title: Table of Content

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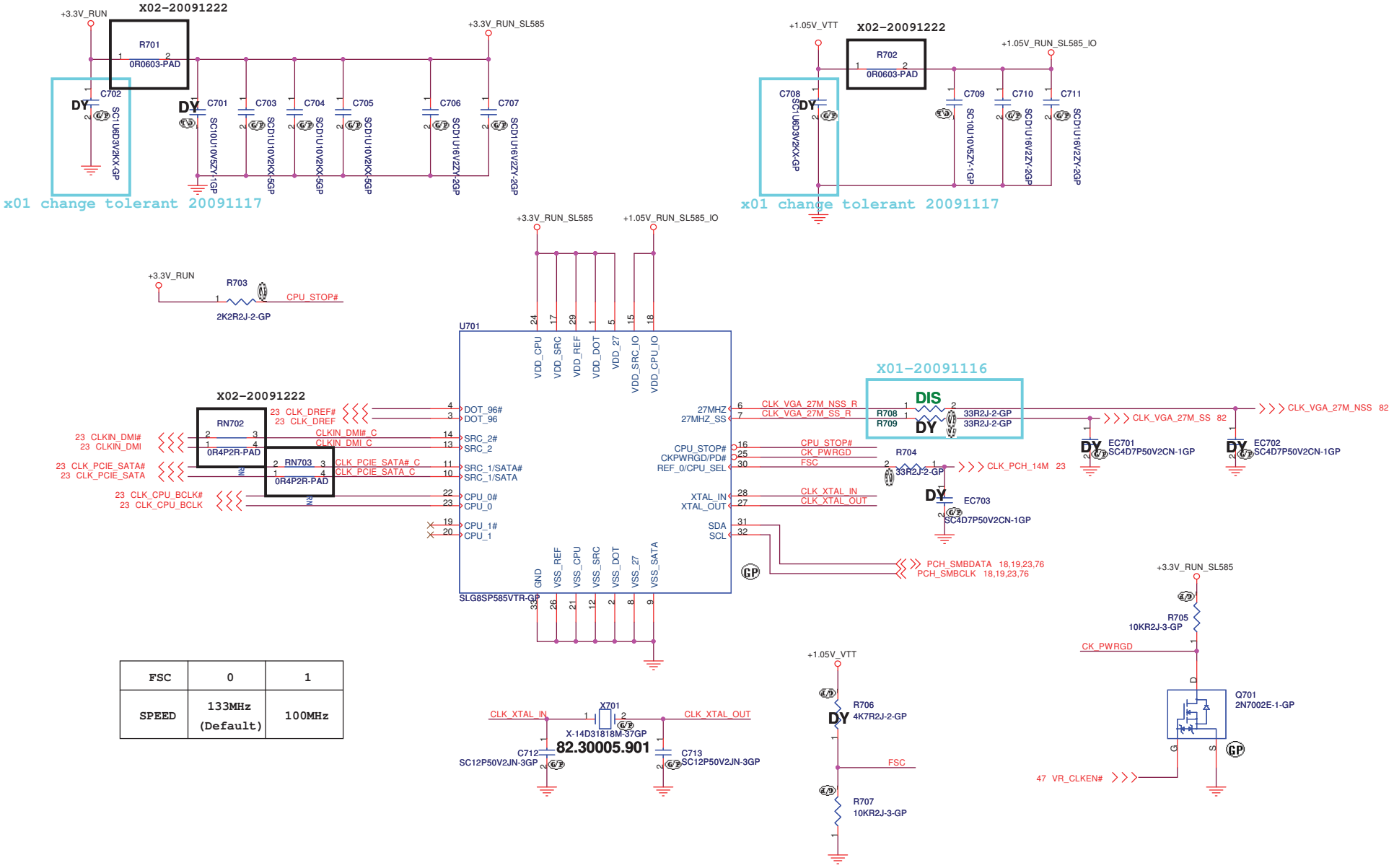
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

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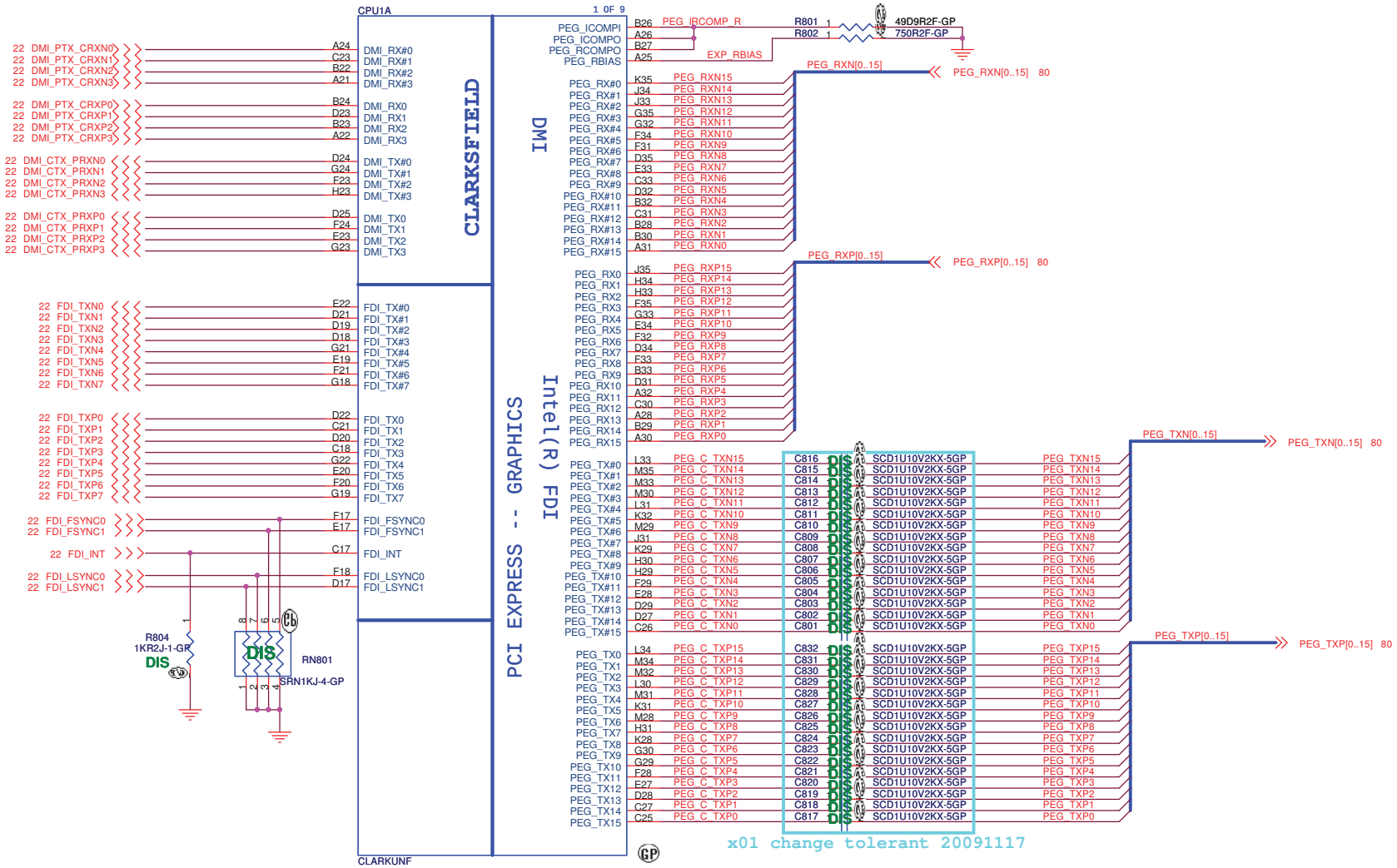
SSID = CPU



62.10055.341

SEC. 62.10053.561

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Title: CPU (PCIE/DMI/FDI)

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SSID = CPU

Processor Pullups

Processor Compensation Signals

CLARKSFIELD

CLOCKS

THERMAL

DDR3 MISC

PWR MANAGEMENT

DDR3 Compensation Signals

X01 20091121
VTTPWRGOOD signal must be clean and close to CPU

For EMI

x01 change tolerant 20091117

X01 20091112

A00-20100226

A00-20100208

JTAG MAPPING	
Scan Chain (Default)	Stuff --> R928, R931, R934 No Stuff --> R929, R933
CPU Only	Stuff --> R928, R929 No Stuff --> R931, R934, R933
GMCH Only	Stuff --> R933, R934 No Stuff --> R928, R929, R931

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Title: CPU (THERMAL/CLOCK/PM)

Size: | Document Number: Berry | Rev: A00

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SSID = CPU

CPU1C — 3 OF 9 — CLARKSFIELD — DDR SYSTEM MEMORY A — CLARKUNF

CPU1D — 4 OF 9 — CLARKSFIELD — DDR SYSTEM MEMORY - B — CLARKUNF

<Core Design>

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Title	CPU (DDR)	
Size	Document Number: Berry	Rev: A00
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SSID = CPU

CFG0

R1101 3KR2F-GP

DY

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3

R1104 3KR2J-2-GP

DIS

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4

R1105 3KR2F-GP

DY

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7

R1106 3KR2F-GP

DY

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

CPU1E 5 OF 9

CLARKSFIELD

RESERVED

CLARKUNF

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

R1107 0R0402-PAD

X02-20091224

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Title: CPU (RESERVED)

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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

x01 change tolerant 20091117

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

CLARKUNF

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

PSI# AN33 → PSI# 47

VID AK35 H_VID0, AK33 H_VID1, AK34 H_VID2, AL35 H_VID3, AL33 H_VID4, AM33 H_VID5, AM35 H_VID6 → H_VID[6..0] 47

PROC_DPRSLPVR AM34 → PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 → TP1201 TPAD14-GP

H_VTTVID1 = Low, 1.1V

H_VTTVID1 = High, 1.05V

ISENSE AN35 → IMVP_IMON 47

VCC_SENSE AJ34, VSS_SENSE AJ35 → VCC_SENSE 47, VSS_SENSE 47

VTT_SENSE B15, VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT → VTT_SENSE 49, TP1202 TPAD14-GP

R1201 100R2F-L1-GP-U

R1202 100R2F-L1-GP-U

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Title: CPU (VCC_CORE)

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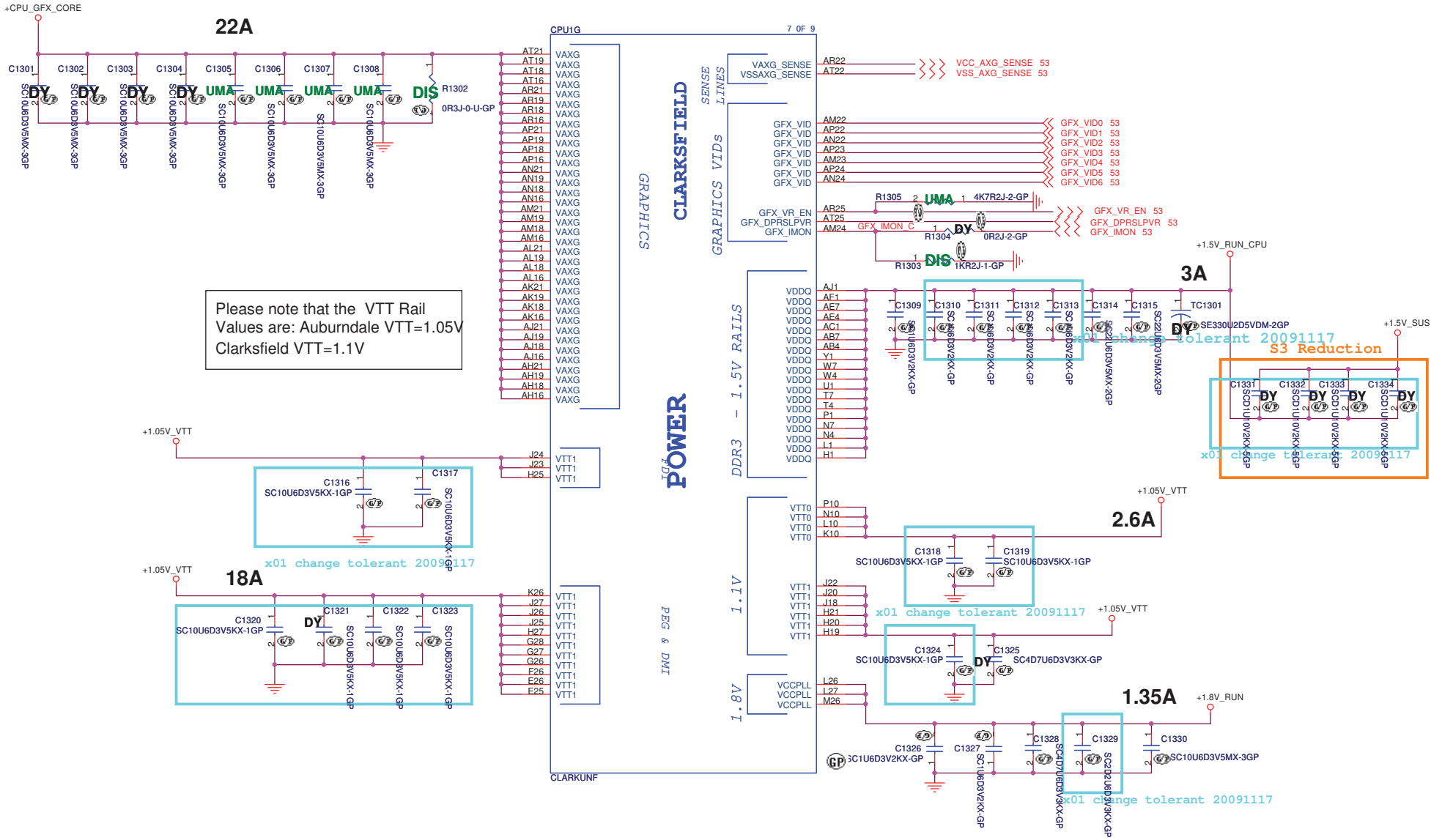
SSID = CPU



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Title: CPU (VCC_GFXCORE)

Size | Document Number: Berry | Rev: A00

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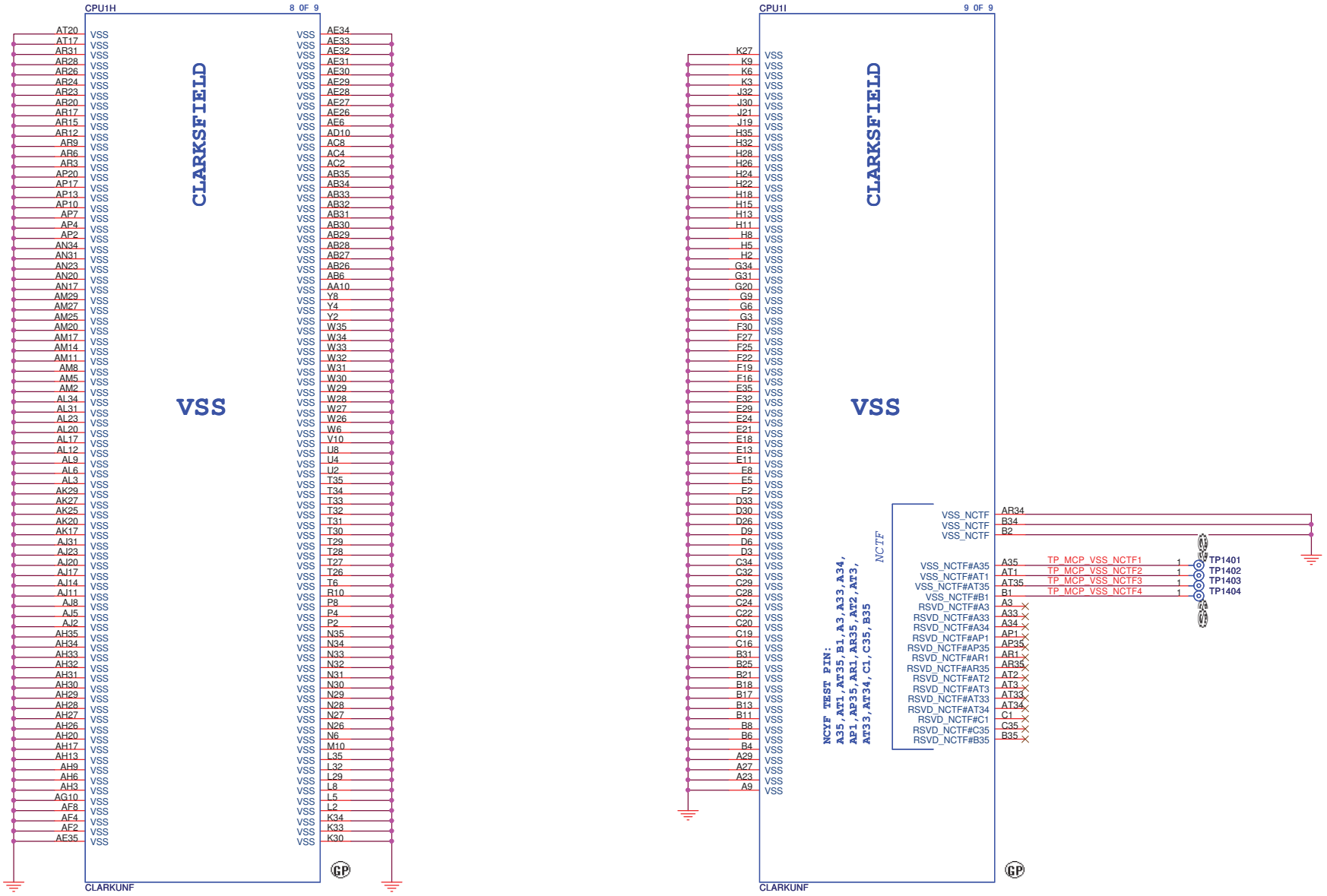
SSID = CPU



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Title	CPU (VSS)	
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Title: *Reserved*

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Title: *Reserved*

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Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

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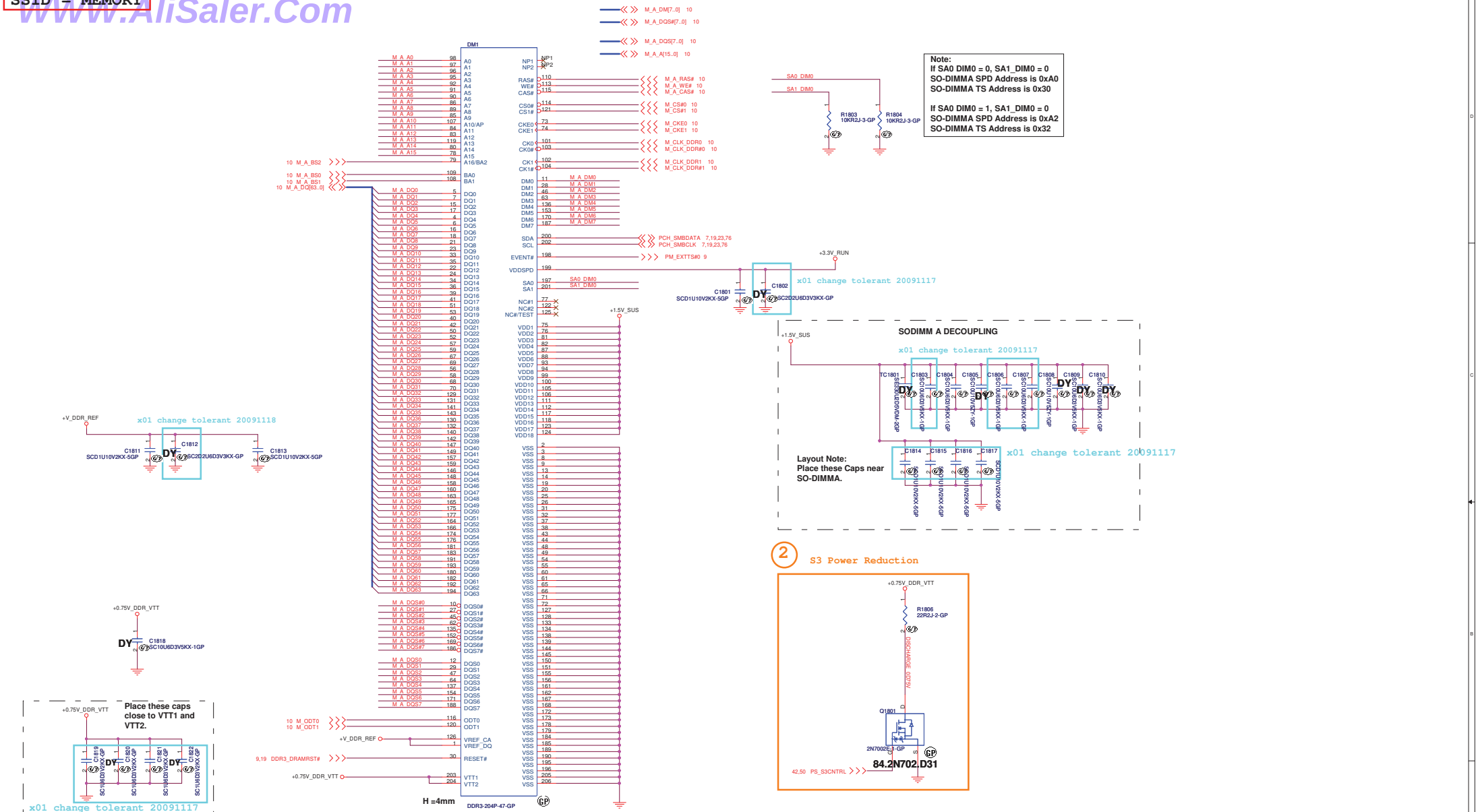
SSID = MEMORY



62.10017.P31

SEC. 62.10017.P11

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Title: DDR3-SODIMM1

Size | Document Number: Berry | Rev: A00

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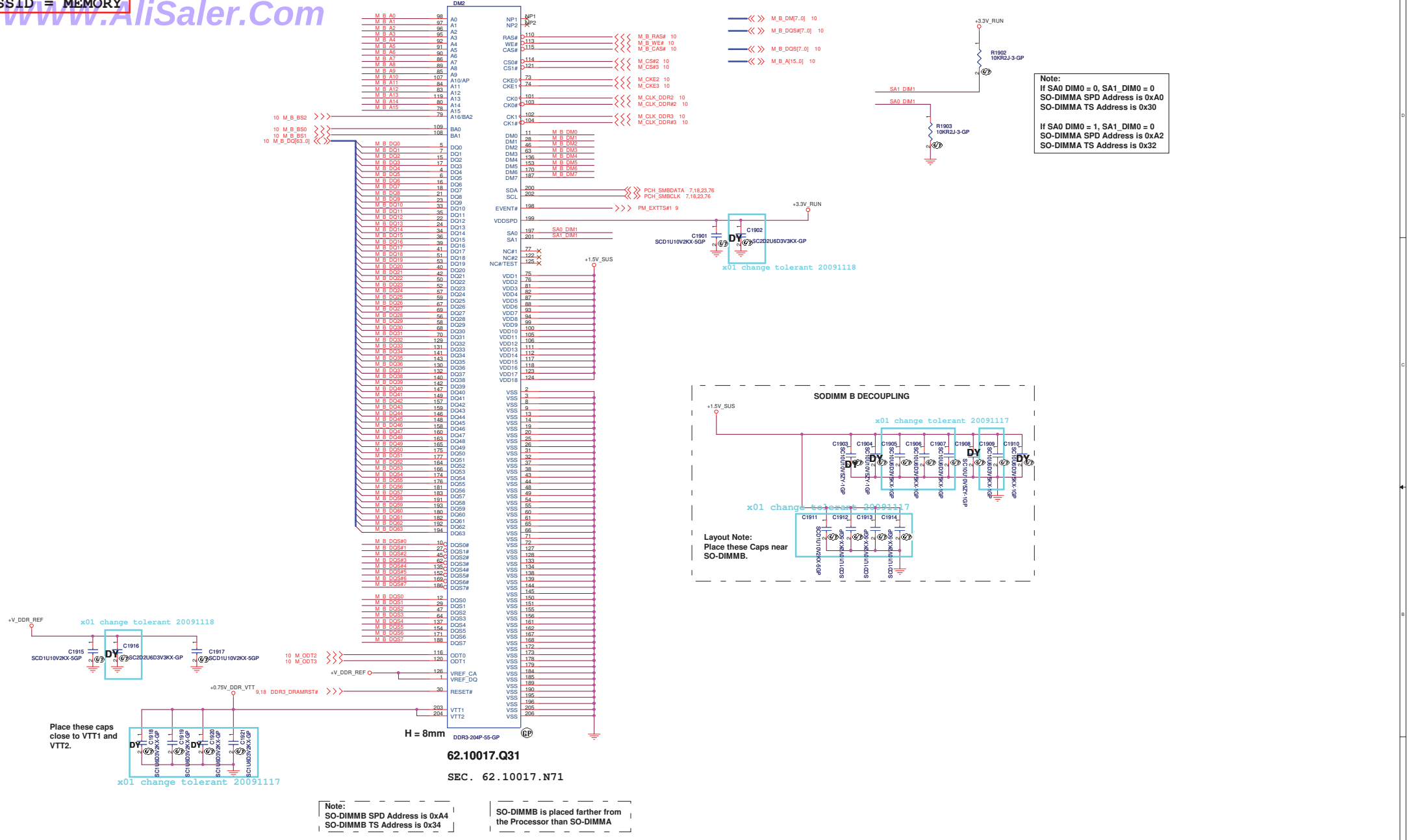
SSID = MEMORY



62.10017.Q31

SEC. 62.10017.N71

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Title: DDR3-SODIMM2

Size | Document Number: Berry | Rev: A00

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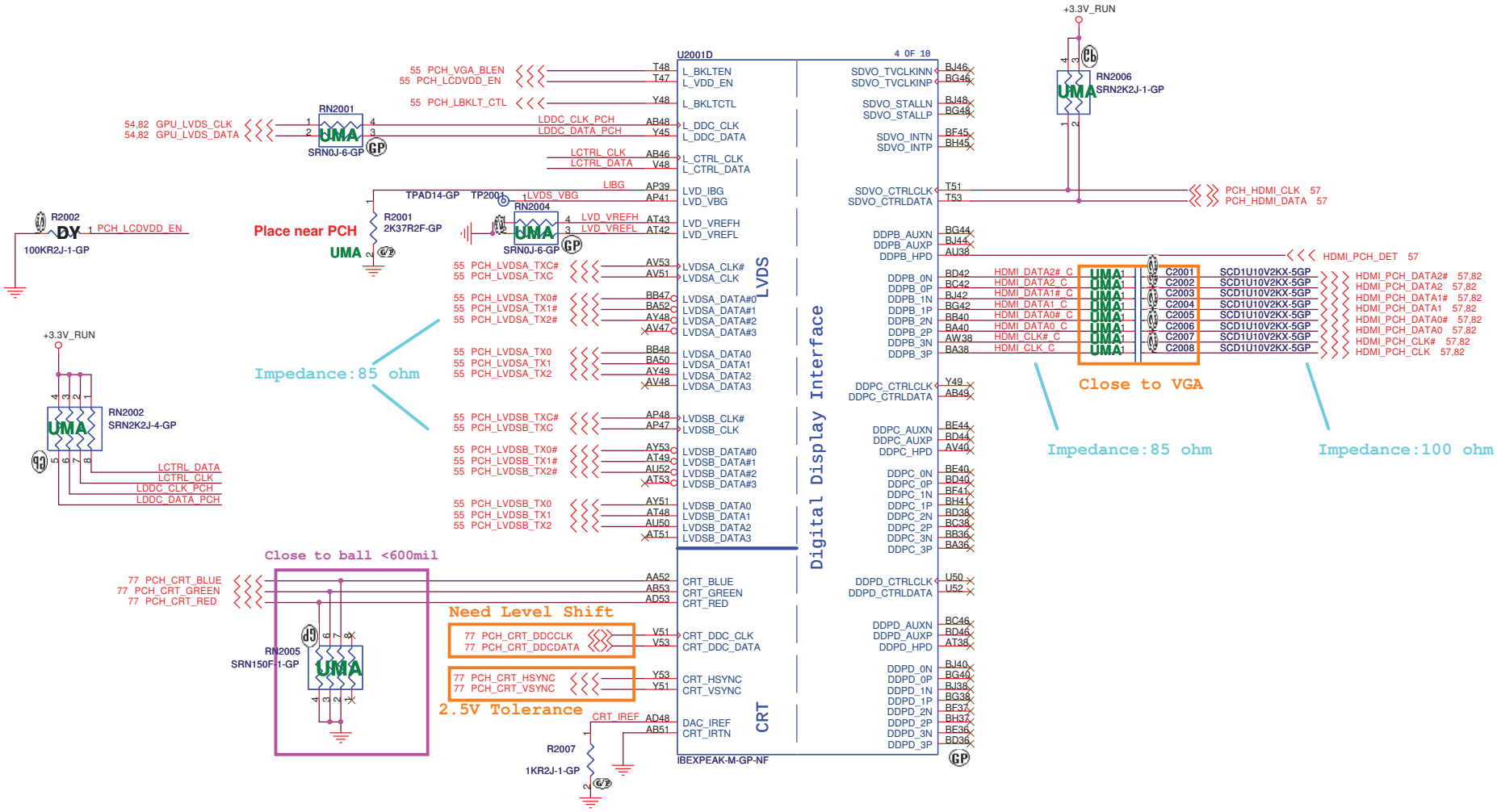

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Title: PCH (LVDS/CRT/DDI)

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SSID = PCH

RN2101 SRN8K2J-2-GP-U
PCI_TRDY# PCI_DEVSEL# INT_PIRQA# PCI_IRDY# PCI_FRAME# PCI_REQ2# INT_PIRQD# PCI_SERR#
+3.3V_RUN

RN2103 SRN8K2J-2-GP-U
INT_PIRQH# INT_PIRQB# INT_PIRQF# PCI_REQ3# PCI_REQ1# PCI_PLOCK# PCI_PERR# PCI_REQ0#
+3.3V_RUN

RN2102 SRN8K2J-4-GP
+3.3V_RUN
PCI_STOP# INT_PIRQE# INT_PIRQC# INT_PIRQG#

U2101 NL17SZ08DFT2G-GP
+3.3V_RUN
9,37,70,76,78,80 PLT_RST#
PCI_PLTRST#
R2101 0R0402-PAD
C2101 SC220P50V2KX-3GP

BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

RN2104 SRN8K2J-2-GP-U
USB_OC#2_3 SMC_WAKE_SCI#_R USB_OC#6_7 USB_OC#0_1 USB_OC#12_13 USB_OC#8_9 USB_OC#10_11 USB_OC#4_5
+3.3V_ALW
R2105 4K7R2J-2-GP
PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

U2001E IBEXPEAK-M-GP-NF
5 OF 10

PCI:
H40 AD0, N34 AD1, C44 AD2, A38 AD3, C36 AD4, J34 AD5, A40 AD6, D45 AD7, E36 AD8, H48 AD9, E40 AD10, C40 AD11, M48 AD12, M45 AD13, F53 AD14, M40 AD15, M43 AD16, J36 AD17, K48 AD18, F40 AD19, C42 AD20, K46 AD21, M51 AD22, J52 AD23, K51 AD24, L34 AD25, F42 AD26, J40 AD27, G46 AD28, F44 AD29, M47 AD30, H36 AD31
J50 C/BE0#, G42 C/BE1#, H47 C/BE2#, G34 C/BE3#
INT_PIRQA# G38 PIRQA#, INT_PIRQB# H51 PIRQB#, INT_PIRQC# B37 PIRQC#, INT_PIRQD# A44 PIRQD#
PCI_REQ0# F51 REQ0#, PCI_REQ1# A46 REQ1#/GPIO50, PCI_REQ2# B45 REQ2#/GPIO52, PCI_REQ3# M53 REQ3#/GPIO54
TPAD14-GP TP2102 PCI_GNT0# F48 GNT0#
TPAD14-GP TP2103 PCI_GNT1# K45 GNT1#/GPIO51
TPAD14-GP TP2104 PCI_GNT2# F36 GNT2#/GPIO53
PCI_GNT3# H53 GNT3#/GPIO55
INT_PIRQE# B41 PIRQE#/GPIO2, INT_PIRQF# K53 PIRQF#/GPIO3, INT_PIRQG# A36 PIRQG#/GPIO4, INT_PIRQH# A48 PIRQH#/GPIO5
TPAD14-GP TP2110 PCIRST# K6 PCIRST#
PCI_SERR# E44 SERR#, PCI_PERR# E50 PERR#
PCI_IRDY# A42 IRDY#, H44 PAR, PCI_DEVSEL# F46 DEVSEL#, PCI_FRAME# C46 FRAME#
PCI_PLOCK# D49 PLOCK#
PCI_STOP# D41 STOP#, PCI_TRDY# C48 TRDY#
TPAD14-GP TP2115 PCH_PME# M7 PME#
PCI_PLTRST# D5 PLTRST#

70 PCLK_FWH R2107 22R2J-2-GP PCLK_FWH_R N52
23 CLK_PCI_FB R2108 22R2J-2-GP CLK_PCI_FB_R P53
37 PCLK_KBC R2109 22R2J-2-GP PCLK_KBC_R P46
P51 CLKOUT_PCI3, P48 CLKOUT_PCI4
EC2101 SC4D7P50V2CN-1GP
KBC CLK EMI

NVRAM:
AY9 NV_CE#0, BD1 NV_CE#1, AP15 NV_CE#2, BD8 NV_CE#3
NV_DQS0 AY9, NV_DQS1 BG8
NV_DQ0/NV_IO0 AP7, NV_DQ1/NV_IO1 AP6, NV_DQ2/NV_IO2 AT6, NV_DQ3/NV_IO3 AT9, NV_DQ4/NV_IO4 BB1, NV_DQ5/NV_IO5 AV6, NV_DQ6/NV_IO6 BB3, NV_DQ7/NV_IO7 BA4, NV_DQ8/NV_IO8 BE4, NV_DQ9/NV_IO9 BB6, NV_DQ10/NV_IO10 BD6, NV_DQ11/NV_IO11 BB7, NV_DQ12/NV_IO12 BC8, NV_DQ13/NV_IO13 BJ8, NV_DQ14/NV_IO14 BJ6, NV_DQ15/NV_IO15 BG6
NV_ALE BD3, NV_CLE AY6
NV_RCOMP AU2 — NV_RCOMP 1 TP2105 TPAD14-GP
NV_RB# AV7
NV_WR#0_RE# AY8, NV_WR#1_RE# AY5
NV_WE#_CK0 AV11, NV_WE#_CK1 BF5

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

+V_NVRAM_VCCQ — R2102 KR2J-1-GP DY — NV_CLE
+V_NVRAM_VCCQ — R2103 KR2J-1-GP DY — NV_ALE

Danbury Technology:
Disabled when Low.
Enable when High.

USB:
USBP0N H18, USBP0P J18, USBP1N A18, USBP1P C18, USBP2N N20, USBP2P P20, USBP3N J20, USBP3P L20, USBP4N F20, USBP4P G20, USBP5N A20, USBP5P C20, USBP6N M22, USBP6P N22, USBP7N B21, USBP7P D21, USBP8N H22, USBP8P J22, USBP9N E22, USBP9P F22, USBP10N A22, USBP10P C22, USBP11N G24, USBP11P H24, USBP12N L24, USBP12P M24, USBP13N A24, USBP13P C24
USB_PN0 77, USB_PP0 77, USB_PN1 77, USB_PP1 77, USB_PN2 76, USB_PP2 76, USB_PN4 78, USB_PP4 78, USB_PN5 73, USB_PP5 73, USB_PN8 76, USB_PP8 76, USB_PN9 76, USB_PP9 76, USB_PN11 76, USB_PP11 76, USB_PN13 54, USB_PP13 54
USBRBIAS# B25 — USB_RBIAS_PN — R2106 22D6R2F-L1-GP
USBRBIAS D25
OC0#/GPIO59 N16 USB_OC#0_1, OC1#/GPIO40 J16 USB_OC#2_3, OC2#/GPIO41 F16 USB_OC#4_5, OC3#/GPIO42 L16 USB_OC#6_7, OC4#/GPIO43 E14 USB_OC#8_9, OC5#/GPIO9 G16 USB_OC#10_11, OC6#/GPIO10 F12 USB_OC#12_13, OC7#/GPIO14 T15 SMC_WAKE_SCI#_R
USB_OC#0_1 63, USB_OC#8_9 63

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

<Core Design>

Wistron Corporation
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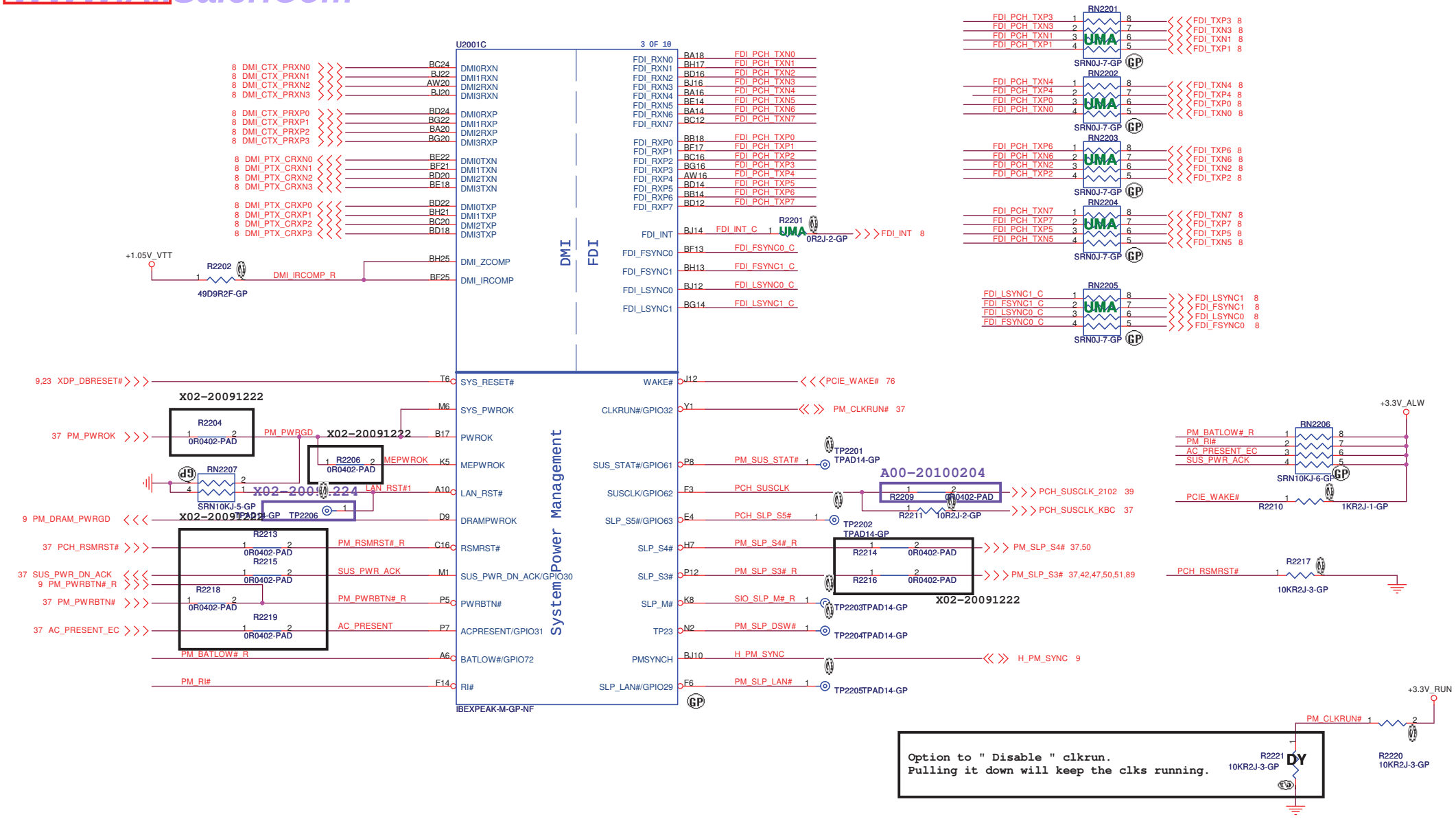
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: | Document Number: Berry | Rev: A00
Date: Monday, March 29, 2010 | Sheet 21 of 92

SSID = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 22 of 92

SSID = PCH

U2001B

2 OF 10

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

x01 change tolerant 20091117

x01 20091118

DIS uses 0ohm 63.R0034.1DL
UMA uses 12pF 78.12034.1FL

X01 2009/11/06

X01 2009/11/05

IBEXPEAK-M-GP-NF

<Core Design>

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Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 23 of 92

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH_RTCX1 — R2402 10MR2J-L-GP — PCH_RTCX2
X2401 X-32D768KHZ-GP
C2403 SC15P50V2JN-2-GP
C2401 SC15P50V2JN-2-GP
82.30001.A41
X01 X01

+RTC_CELL — R2401 20KR2J-L-GP — C2402 SC1U6D3V2KX-GP
+RTC_CELL — R2403 20KR2J-L-GP — C2404 SC1U6D3V2KX-GP — G2401 GAP-OPEN
R2407 1M1R2J-GP — R2404 330KR2F-L-GP — +RTC_CELL

U2001A 1 OF 10

PCH_RTCX1	B13	RTCX1	RTC
PCH_RTCX2	D13	RTCX2	
PCH_RTCRST#	C14	RTCRST#	
SRTCRST#	D17	SRTCRST#	
SM_INTRUDER#	A16	INTRUDER#	
PCH_INTVRMEN	A14	INTVRMEN	
ACZ_BIT_CLK	A30	HDA_BCLK	IHDA
ACZ_SYNC_R	D29	HDA_SYNC	
30 ACZ_SPKR	P1	SPKR	
ACZ_RST#_R	C30	HDA_RST#	
30 PCH_SDIN_CODEC	G30	HDA_SDIN0	
	F30	HDA_SDIN1	
	E32	HDA_SDIN2	
	F32	HDA_SDIN3	
ACZ_SDATAOUT_R	B29	HDA_SDO	
37 ME_UNLOCK#	H32	HDA_DOCK_EN#/GPIO33	SATA
	J30	HDA_DOCK_RST#/GPIO13	
TPAD14-GP TP2404	M3	JTAG_TCK	JTAG
TPAD14-GP TP2405	K3	JTAG_TMS	
TPAD14-GP TP2406	K1	JTAG_TDI	
TPAD14-GP TP2407	J2	JTAG_TDO	
TPAD14-GP TP2408	J4	TRST#	
62 PCH_SPI_CLK	BA2	SPI_CLK	SPI
62 PCH_SPI_CS0#	AV3	SPI_CS0#	
	AY3	SPI_CS1#	
62 PCH_SPI_DO	AY1	SPI_MOSI	
62 PCH_SPI_DI	AV1	SPI_MISO	

IBEXPEAK-M-GP-NF

	D33	FWH0/LAD0	LPC
	B33	FWH1/LAD1	
	C32	FWH2/LAD2	
	A32	FWH3/LAD3	
LPC_LAD[0..3]			
FWH4/LFRAME#	C34		LPC_LFRAME# 37,70
	A34	LDRQ0#	
	F34	LDRQ1#/GPIO23	
	AB9	SERIRQ	INT_SERIRQ 23,37

X01 20091118 layout swap

30 PCH_AZ_CODEC_SYNC
30 PCH_SDOUT_CODEC
RN2403 SRN33J-5-GP
ACZ_SYNC_R
ACZ_SDATAOUT_R

30 PCH_AZ_CODEC_RST#
30 PCH_AZ_CODEC_BITCLK
RN2402 SRN33J-5-GP-U
ACZ_RST#_R
ACZ_BIT_CLK

NO REBOOT STRAP

+3.3V_RUN — R2410 1KR2J-1-GP (DY) — ACZ_SPKR

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

For EMI

PCH_AZ_CODEC_BITCLK
PCH_AZ_CODEC_RST#
EC2402 SCD1U10V2KX-5GP (DY)
EC2401 SC22P50V2JN-4GP (DY)

x01 Change tolerant 20091117

x01 Change tolerant 20091117

SATA0RXN	AK7		SATA_RXN0_C 59
SATA0RXP	AK6		SATA_RXP0_C 59
SATA0TXN	AK11	SATA_TXN0_C C2409 SCD01U16V2KX-3GP	SATA_TXN0 59
SATA0TXP	AK9	SATA_TXP0_C C2410 SCD01U16V2KX-3GP	SATA_TXP0 59
SATA1RXN	AH6		SATA_RXN1_C 59
SATA1RXP	AH5		SATA_RXP1_C 59
SATA1TXN	AH9	SATA_TXN1_C C2405 SCD01U16V2KX-3GP	SATA_TXN1 59
SATA1TXP	AH8	SATA_TXP1_C C2406 SCD01U16V2KX-3GP	SATA_TXP1 59
SATA2RXN	AE11		
SATA2RXP	AE9		
SATA2TXN	AE7		
SATA2TXP	AE6		
SATA3RXN	AH3		
SATA3RXP	AH1		
SATA3TXN	AF3		
SATA3TXP	AF1		
SATA4RXN	AD9		SATA_RXN4_C 76
SATA4RXP	AD8		SATA_RXP4_C 76
SATA4TXN	AD6	SATA_TXN4_C C2407 SCD01U16V2KX-3GP	SATA_TXN4 76
SATA4TXP	AD5	SATA_TXP4_C C2408 SCD01U16V2KX-3GP	SATA_TXP4 76
SATA5RXN	AD3		
SATA5RXP	AD1		
SATA5TXN	AB3		
SATA5TXP	AB1		
SATAICOMPO	AF16		
SATAICOMPI	AF15	SATAICOMP 1 — R2412 37D4R2F-GP — +1.05V_VTT	
SATALED#	T3		SATA_LED# 66
SATA0GP/GPIO21	Y9		SATA_DET#0_R
SATA1GP/GPIO19	V1		SATA_DET#1_R

HDD
ODD
ESATA

+3.3V_RUN — RN2401 SRN10KJ-5-GP

<Core Design>

Wistron Corporation
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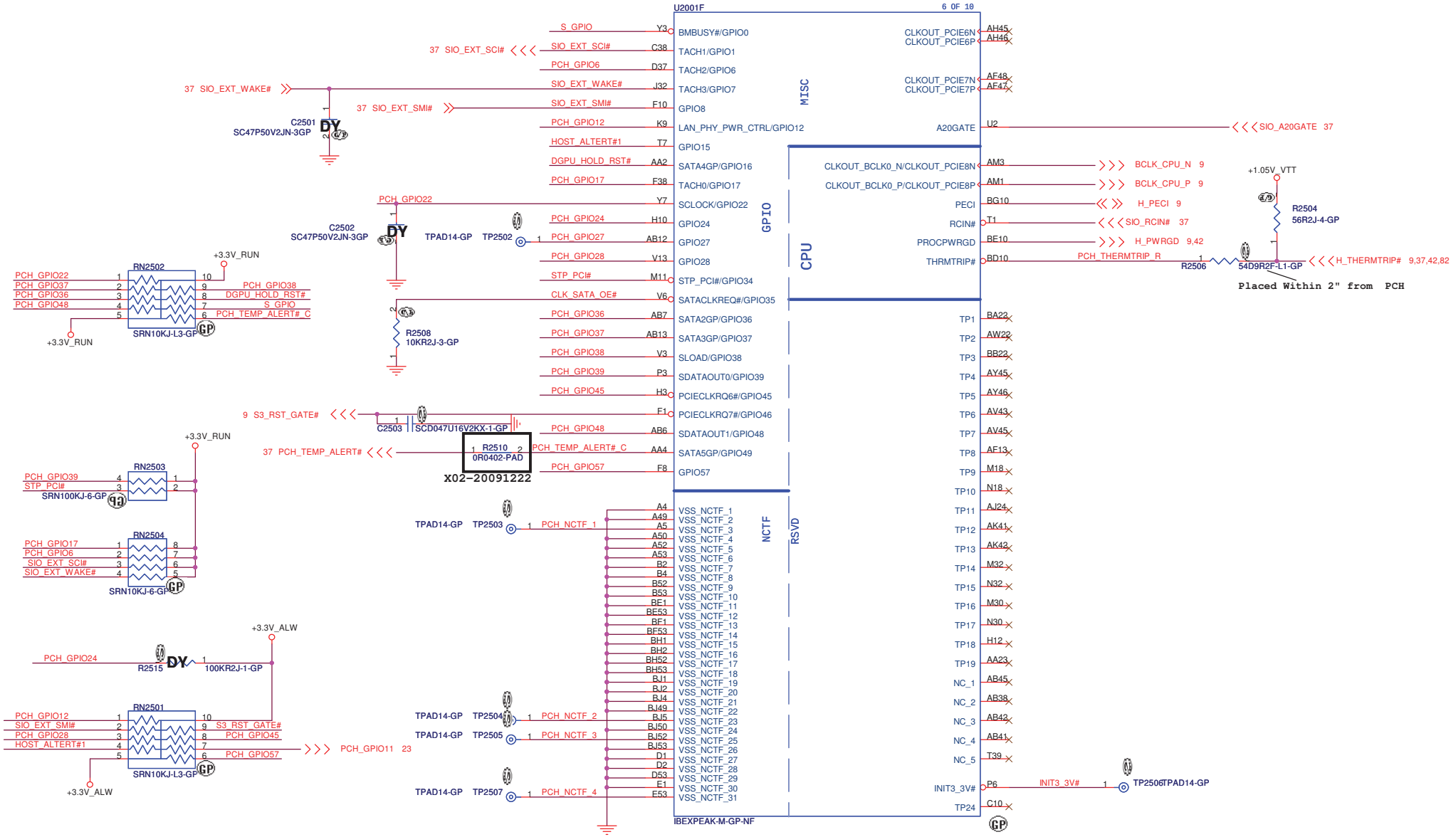
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size | Document Number: Berry | Rev: A00
Date: Monday, March 29, 2010 | Sheet 24 of 92

SSID = PCH



<Core Design>

Wistron Corporation
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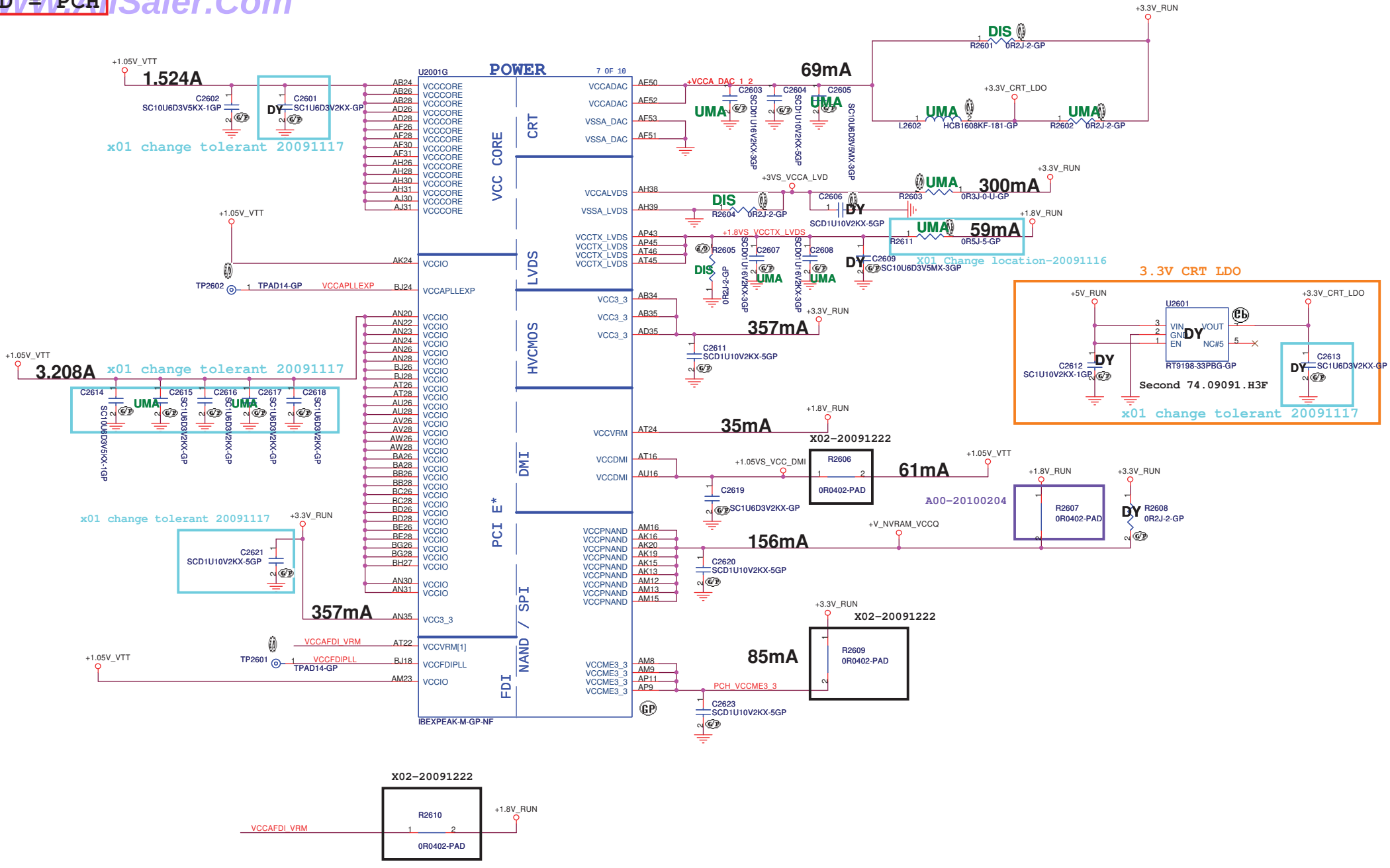
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (GPIO/CPU)	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 25 of 92	

SSID = PCH



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Title: PCH (POWER1)

Size | Document Number: Berry | Rev: A00

Date: Wednesday, February 10, 2010 | Sheet 26 of 92

SSID = PCH

U2001J POWER 10 OF 10

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | CPU | RTC | HDA

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK
AF23 VCCLAN
AF24 VCCLAN
Y20 DCPSUSBYP
AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
V9 DCPRTC
AU24 VCCVRM
BB51 VCCADPLLA
BB53 VCCADPLLA
BD51 VCCADPLLB
BD53 VCCADPLLB
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO
V12 DCPSST
Y22 DCPSUS
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
AT18 V_CPU_IO
AU18 V_CPU_IO
A12 VCCRTC
IBEXPEAK-M-GP-NF

V24 VCCIO
V26 VCCIO
Y24 VCCIO
Y26 VCCIO
V28 VCCSUS3_3
U28 VCCSUS3_3
U26 VCCSUS3_3
U24 VCCSUS3_3
P28 VCCSUS3_3
P26 VCCSUS3_3
N28 VCCSUS3_3
N26 VCCSUS3_3
M28 VCCSUS3_3
M26 VCCSUS3_3
L28 VCCSUS3_3
L26 VCCSUS3_3
J28 VCCSUS3_3
J26 VCCSUS3_3
H28 VCCSUS3_3
H26 VCCSUS3_3
G28 VCCSUS3_3
G26 VCCSUS3_3
F28 VCCSUS3_3
F26 VCCSUS3_3
E28 VCCSUS3_3
E26 VCCSUS3_3
C28 VCCSUS3_3
C26 VCCSUS3_3
B27 VCCSUS3_3
A28 VCCSUS3_3
A26 VCCSUS3_3
U23 VCCSUS3_3
V23 VCCIO
F24 V5REF_SUS
K49 V5REF
J38 VCC3_3
L38 VCC3_3
M36 VCC3_3
N36 VCC3_3
P36 VCC3_3
U35 VCC3_3
AD13 VCC3_3
AK3 VCCSATAPLL
AK1 VCCSATAPLL
AH22 VCCIO
AT20 VCCVRM
AH19 VCCIO
AD20 VCCIO
AF22 VCCIO
AD19 VCCIO
AF20 VCCIO
AF19 VCCIO
AH20 VCCIO
AB19 VCCIO
AB20 VCCIO
AB22 VCCIO
AD22 VCCIO
AA34 VCCME
Y34 VCCME
Y35 VCCME
AA35 VCCME
L30 VCCSUSHDA

C2705 SC1U6D3V2KX-GP DY
C2706 SCD1U10V2KX-5GP
C2709 SCD1U10V2KX-5GP
C2718 SCD1U10V2KX-5GP
C2719 SCD1U10V2KX-5GP
C2727 SC1U6D3V2KX-GP
C2733 SC1U6D3V2KX-GP
C2713 SC1U10V2KX-1GP
C2715 SC1U10V2KX-1GP
D2701 CH751H-40PT-GP
D2702 CH751H-40PT-GP
R2702 10R2J-2-GP
R2701 10R2J-2-GP
R2703 0R0402-PAD
TP2702 VCCSATAPLL TPAD14-GP

C2703 SCD1U10V2KX-5GP
C2707 SC10U6D3V5KX-1GP
C2704 SC10U6D3V5MX-3GP DY
C2708 SC1U6D3V2KX-GP
C2710 SC1U6D3V2KX-GP DY
C2711 SC10U6D3V5MX-3GP DY
C2712 SC1U6D3V2KX-GP
C2714 SCD1U10V2KX-5GP
C2716 SC10U6D3V5MX-3GP DY
C2717 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
C2721 SC1U6D3V2KX-GP
C2722 SC1U6D3V2KX-GP
C2725 SCD1U10V2KX-5GP
C2726 SCD1U10V2KX-5GP
C2728 SCD1U10V2KX-5GP
C2729 SCD1U10V2KX-5GP
C2730 SC10U6D3V5KX-1GP
C2731 SCD1U10V2KX-5GP
C2732 SCD1U10V2KX-5GP
C2734 SCD1U10V2KX-5GP
C2735 SCD1U10V2KX-5GP

L2702 IND-10UH-218-GP
L2703 IND-10UH-218-GP

+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+1.8V_RUN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
+1.05VALW_INT_VCCSUS
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
VCCSATAPLL
+VCCSUSHDA
+RTC_CELL

x01 change tolerant 20091117
x01 20091121
x01 change tolerant 20091118
1.998A
72mA
73mA
163mA
1mA
2mA
6mA
x02-20091222

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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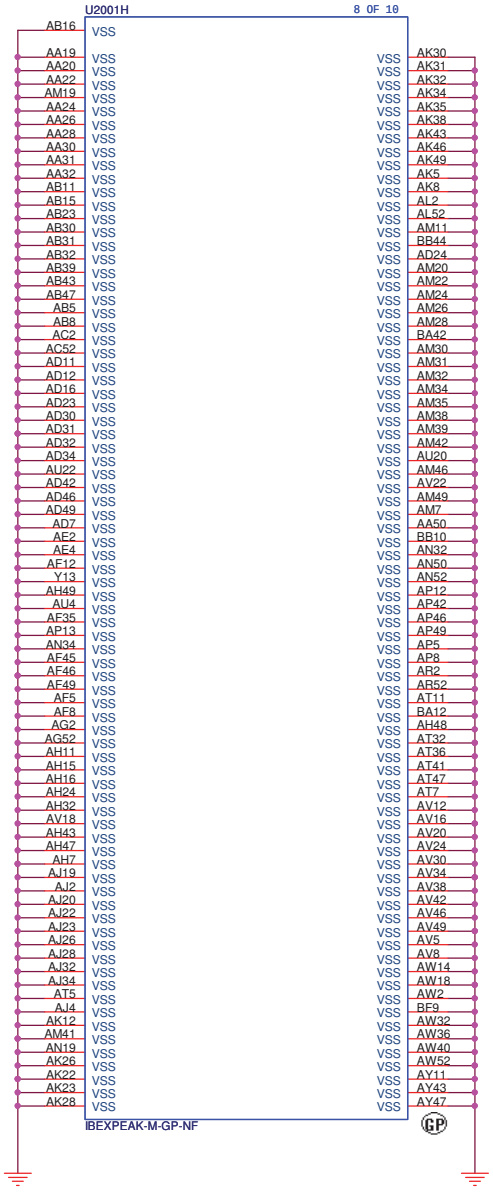
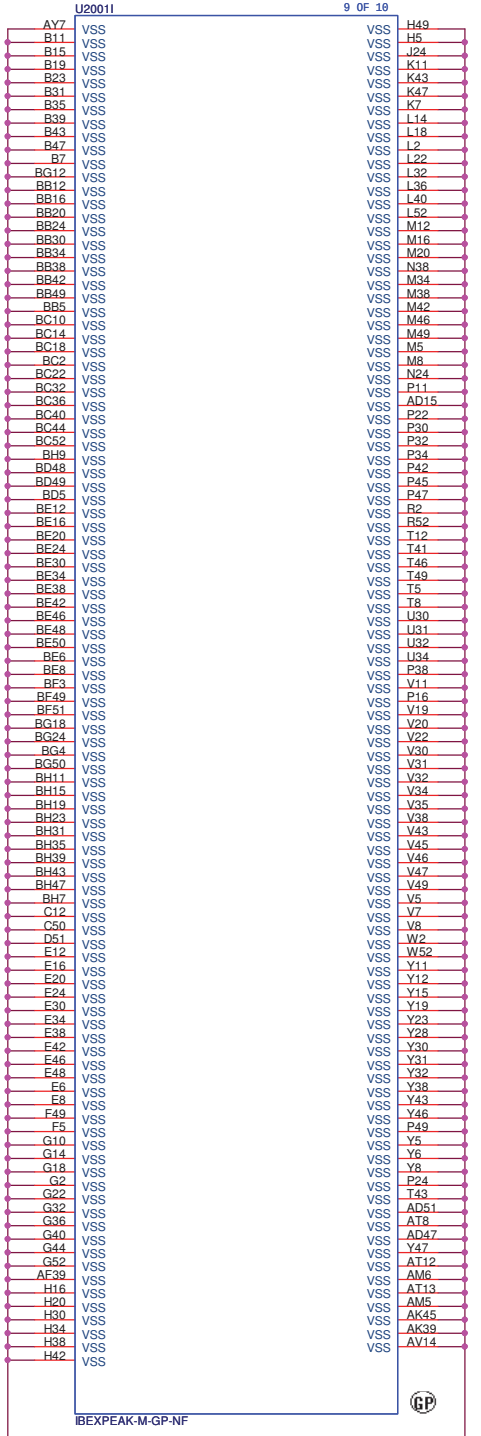
Title: PCH (POWER2)
Size:
Document Number: Berry
Rev: A00
Date: Wednesday, February 10, 2010
Sheet 27 of 92

SSID = PCH





<Core Design>

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Title: PCH (VSS)

Size	Document Number	Rev
	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 28 of 92

<Core Design>

Wistron Corporation
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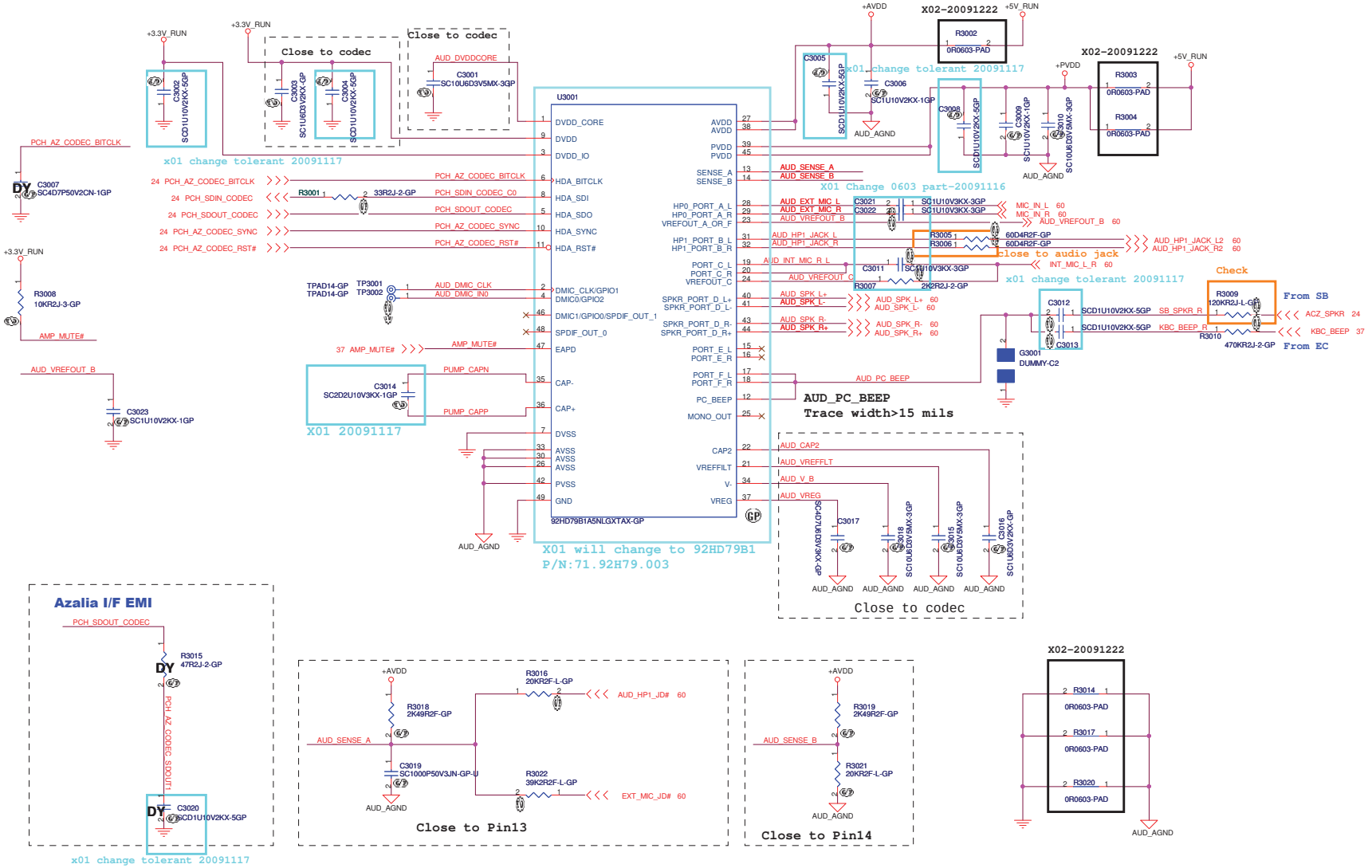
Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 29 of 92

SSID = AUDIO



<Core Design>

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Title: Audio Codec 92HD81B1

Size: Custom | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 30 of 92

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 31 of 92

<Core Design>

Wistron Corporation
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Title: Reserved

Size: Custom | Document Number: Berry | Rev: A00

Date: Wednesday, February 10, 2010 | Sheet 32 of 92

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 33 of 92

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 34 of 92

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 35 of 92

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 36 of 92

CAP close to VCC-GND pin pair

10mW circuit

SSID = KBC

Vendor recommend FW can do it

Vendor recommend can remove

For EMI

MB VERSION			
ID	VER2	VER1	VER0
A01	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

VGA STRAP		
option	GPIO24	GPIO5
UMA	0	0
Madisan	1	1
Park	1	0
M96	1	0

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 37 of 92

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
A4	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 38 of 92

SSID = Thermal

1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.

C3905 must be near Q3901

near EMC2102

2. System Sensor(UMA Only)

Layout notice :
Both DN2 and DP2 routing 10 mil
trace width and 10 mil spacing.

Reserved DISCRETE

3.VGA Sensor(DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.

C3907 must be near Q3902

4.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

x01 change tolerant 20091117

EMC2102

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

A00-20100204

84.2N702.D31

32K suspend clock output

84.2N702.D31

X02-20091222

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)

T8 shutdown is set 88 deg-C.

x01 change tolerant 20091117

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Berry | Rev: A00

Date: Tuesday, April 06, 2010 | Sheet 39 of 92

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 40 of 92

<Core Design>

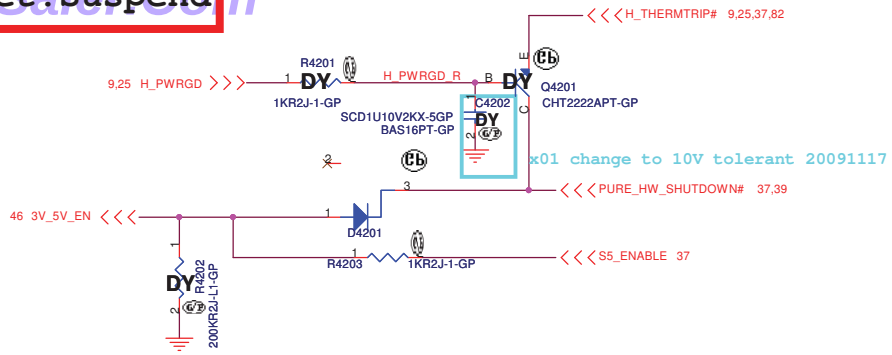
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

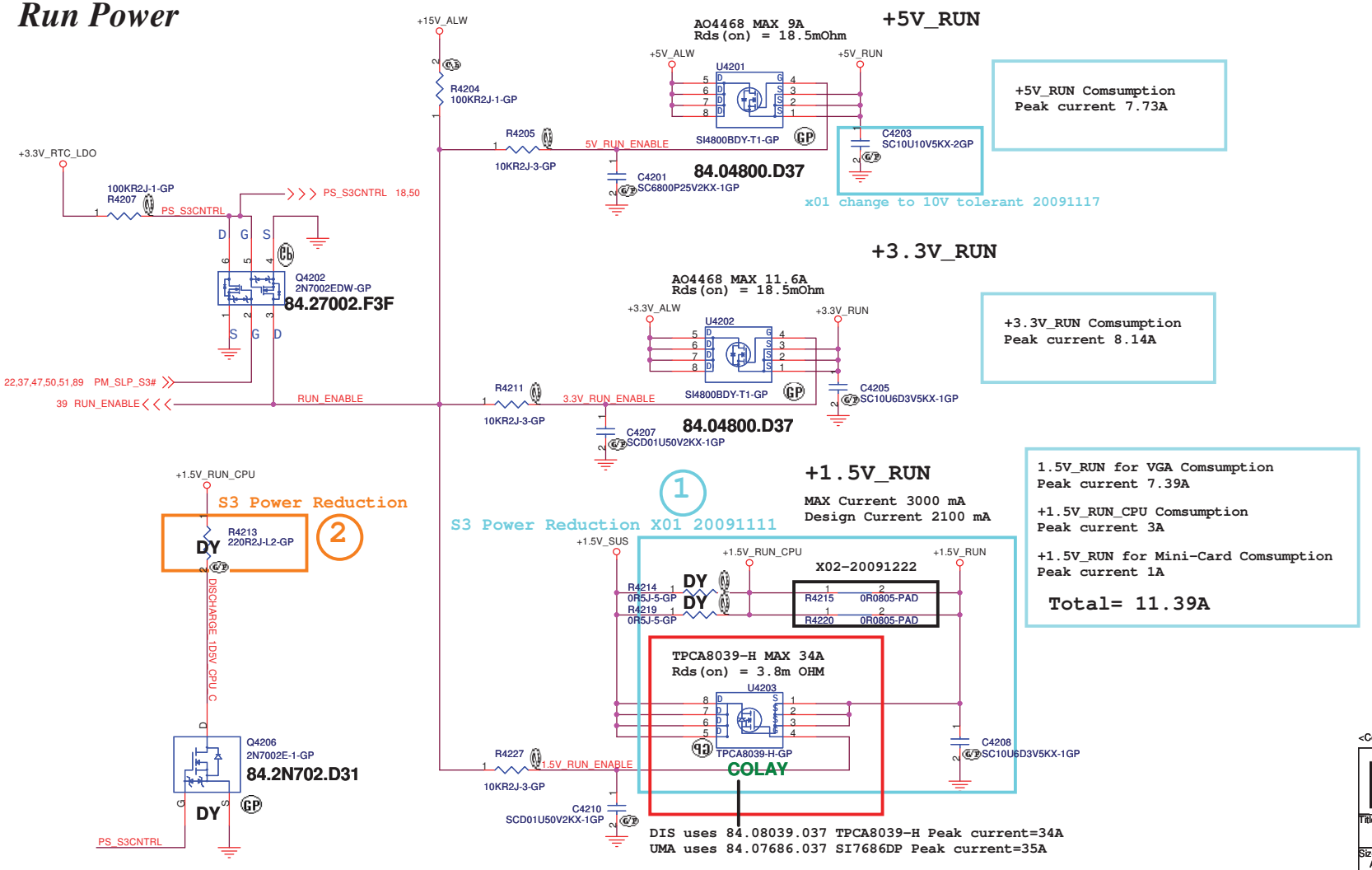
Size	Document Number	Rev
A3	Berry	A00

Date: Wednesday, February 10, 2010 Sheet 41 of 92

SSID = Reset_Suspend



Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Berry	A00

Date: Monday, March 29, 2010 Sheet 42 of 92

<Core Design>

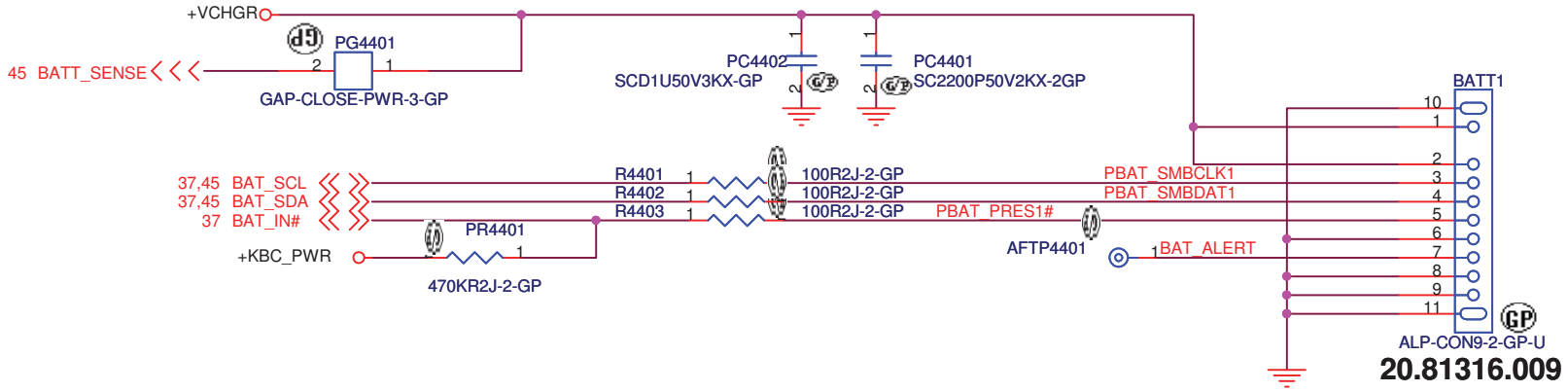
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

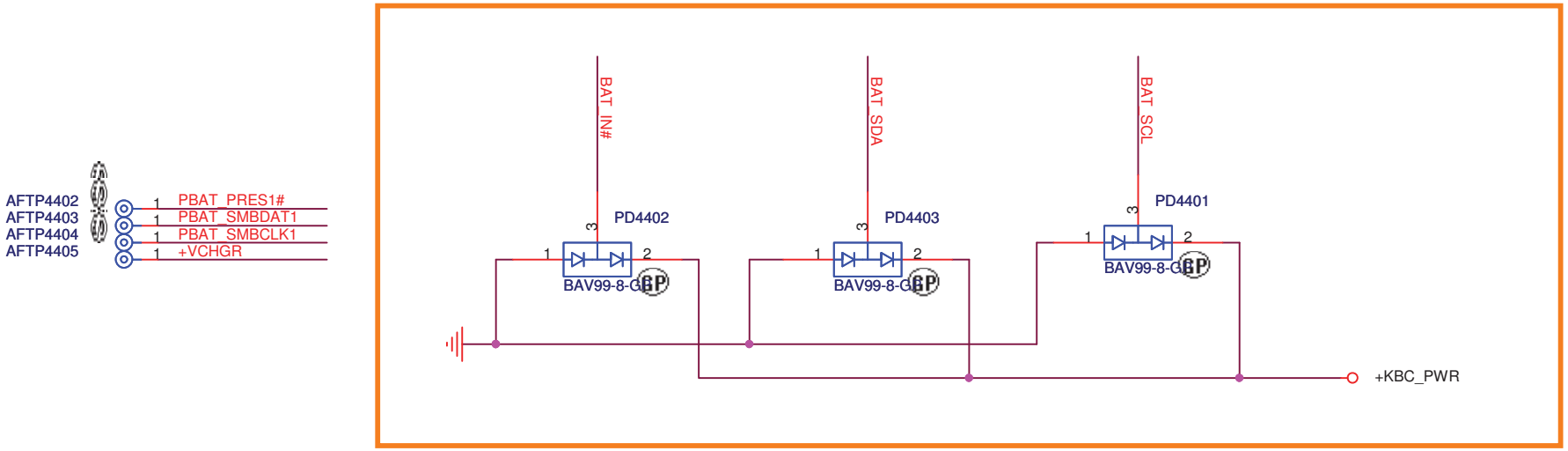
Date: Wednesday, February 10, 2010 Sheet 43 of 92

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN		
Size: A4	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 44 of 92	

SSID = Charger

modify +VCHGR

+DC_IN_SS

PU4502 AO4407A-GP

Id=-12A
Qg=-25nC
Rdson=10~38mohm

PR4513_03 PR4503 100KR2J-1-GP PR4504 10KR2J-3-GP PR4505 10KR2F-2-GP

PC4502_03 PC4502_05

PC4501 2N7002EDW-GP

BQ24745_ACOK

84.27002.F3F

X02-20091223

PR4511 0R0402-PAD

+SDC_IN +PWR_SRC

PR4502 D01R2512F-4-GP

PG4502 PG4503 GAP-CLOSE-PWR-3-GP

PR4507 0R2J-2-GP

PR4508 0R0402-PAD PR4510 0R0402-PAD

PC4502 SCD1U50V3KX-GP

PC4505 SCD1U50V3KX-GP

RC4504 SCD1U50V3KX-GP

CHG_AGND

PU4503 AO4407A-GP

+VCHGR

+DC_IN_SS PR4509 470KR2J-2-GP

Id=-12A
Qg=-25nC
Rdson=10~38mohm

PG4501 PG4506 PG4504 PG4505 GAP-CLOSE-PWR-3-GP

CHAGER_SRC

PC4507 SC10U25V6KX-1GP PC4508 SC10U25V6KX-1GP PC4509 SCD1U50V3KX-GP

PC4501 SC2200P50V2KX-2GP PC4502 SCD1U25V2ZY-1GP

Charger Current=1.4~3.6A

modify +VCHGR

2009/11/24

+VCHGR1 PR4519 D01R2512F-4-GP

PG4510 PG4509 GAP-CLOSE-PWR-3-GP

PC4515 PC4516 PC4517 PC4518 SC10U25V6KX-1GP PC4519 SCD1U50V3KX-GP

PD4502 15MA18AT3G-GP

BQ24745_PR4505

PR4524 0R0402-PAD X02-20091223

BQ24745_CSON

PC4531 SCD1U50V3KX-GP

CHG_AGND

X02-20100116

PL4501 L-5D6UH-GP-U

PU4504 PU4505 SI4800BDY-T1-GP

PC4506 SC1U63V2KX-GP

PR4513 33R3J-2-GP

PD4501 SD103AWS-1-GP

PC4511 SCD1U50V3KX-GP

PR4517 0R0603-PAD

PC4512 SCD1U50V3KX-GP

PC4513 SC3300P50V3KX-1GP

PR4518 0R0603-PAD

PC4514 SC220P50V2JN-3GP

PR4523 0R0402-PAD X02-20091223

PC4520 SCD1U50V3KX-GP

PC4523 SCD1U50V3KX-GP

PR4528 0R0402-PAD X02-20091223

PR4529 0R0402-PAD X02-20091223

PC4532 SCD1U25V2ZY-1GP

PR4530 1K8R0J-GP

BAT_SENSE BATT_SENSE 44

PU4501 BQ24745RHDR-GP

DCIN ACIN VDDSMB ACOK SCL SDA NC#14 VICM FBO EAI EAO VREF CE GND ICREF CSSP CSSN ICOUT BOOT VDDP UGATE PHASE LGATE PGND CSOP CSON NC#16 VFB

BQ24745_DCIN BQ24745_ACIN BQ24745_ACOK BAT_SCL_1 BAT_SDA_1 BQ24745_VICM BQ24745_FBO BQ24745_EAI BQ24745_EAO BQ24745_REF BQ24745_CE BQ24745_CSSP BQ24745_CSSN BQ24745_ICOUT BQ24745_BOOT BQ24745_LDO BQ24745_CHARGER_UGATE BQ24745_PHASE_GND BQ24745_LGATE_1 BQ24745_CSOP_1 BQ24745_LX1

BQ24745_LDO BQ24745_REF +KBC_PWR

x01 change tolerant 20091117

PC4501 SCD1U10V2KX-5GP PR4512 0R0402-PAD

PR4514 48K7R3F-1-GP PR4515 10KR2F-2-GP PR4516 10KR2F-2-GP PR4510 SCD1U50V2KX-1GP

ACAV CHG_AGND

PR4520 15K8R3F-GP

37,44 BAT_SCL 37,44 BAT_SDA

PG4507 PG4508 GAP-CLOSE-PWR-3-GP

2009/08/04

PR4501 0R2J-2-GP

37 AD_IA

X03-20100119

This Resistor must be 1% tolerance.

PR4525 8K45R2F-2-GP PR4521 4K7R2J-2-GP PR4522 200KR2F-L-GP PR4526 7K5R2F-1-GP PR4527 0R0402-PAD

PC4521 SC150P50V2JN-1GP PC4522 SC2200P50V2KX-2GP PC4524 SC220P50V2JN-3GP PC4526 PC4527 SC56P50V2JN-2GP PC4528 PC4529 SCD01U50V2KX-1GP PC4530 SCD1U10V2KX-5GP

BQ24745_FBO1

SCD1U50V3KX-GP SCD01U50V2KX-1GP SCD1U10V2KX-5GP

37 AC_IN#

PC4533 SCD1U10V2KX-5GP

Q4502 2N7002E-1-GP

ACAV_IN

x01 change tolerant 20091117

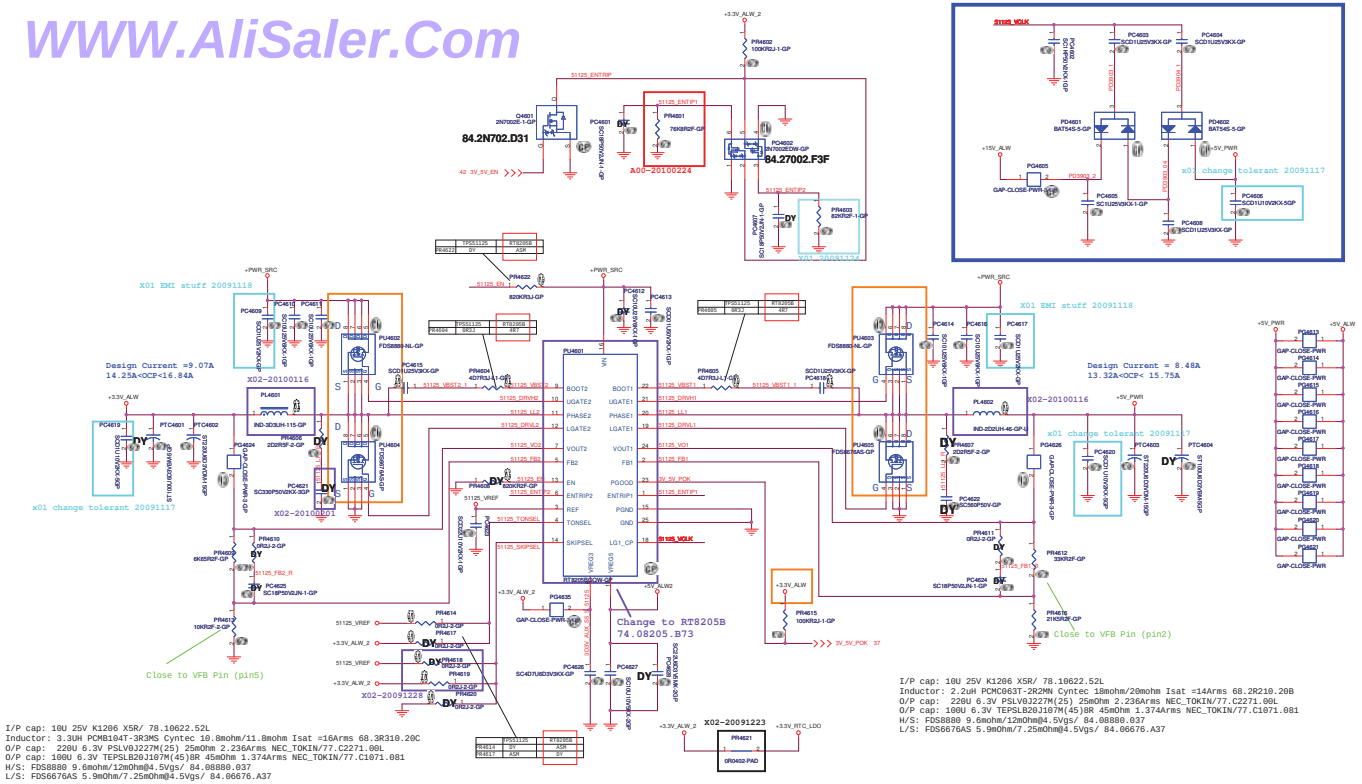
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size: Custom | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 45 of 92



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B:

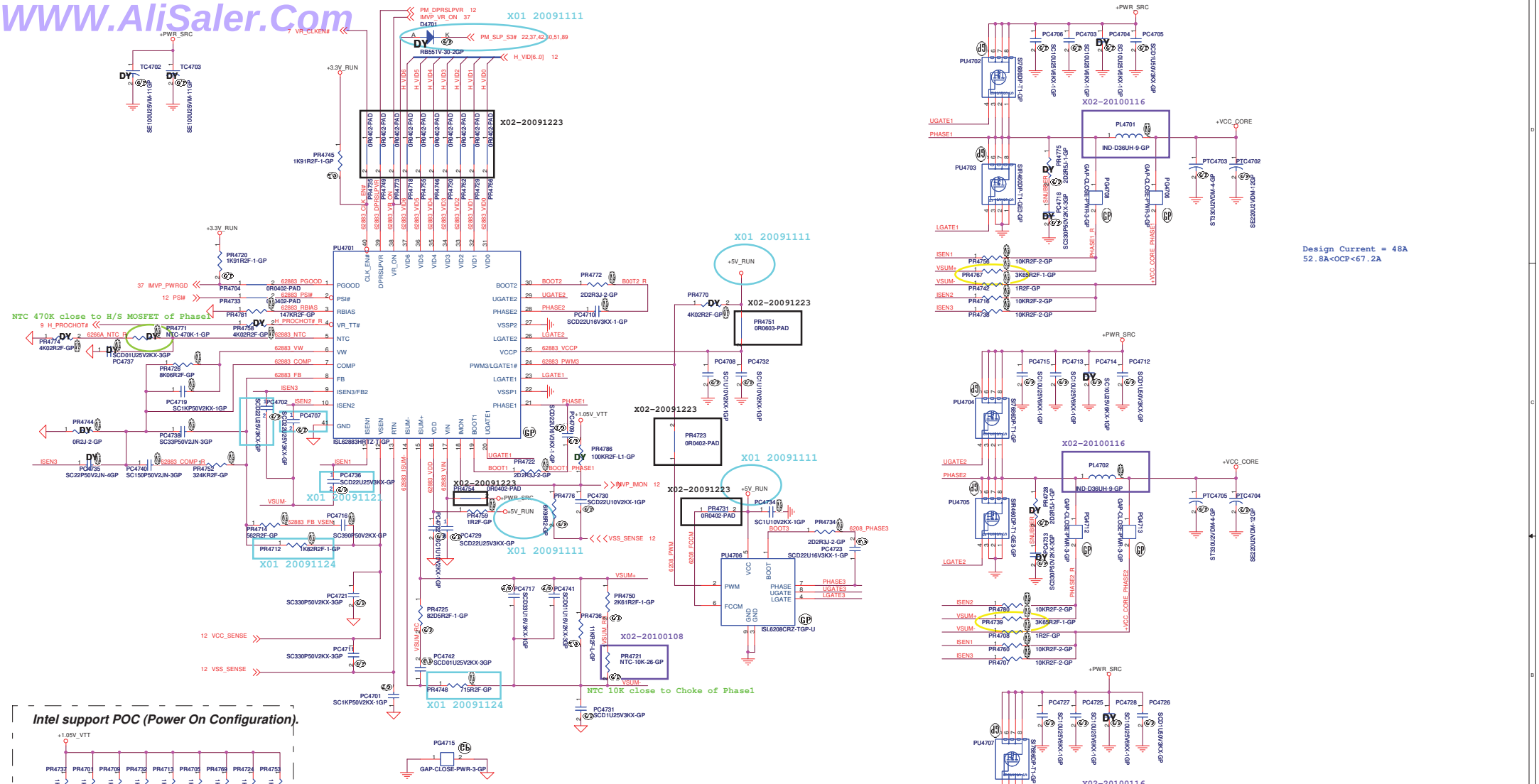
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

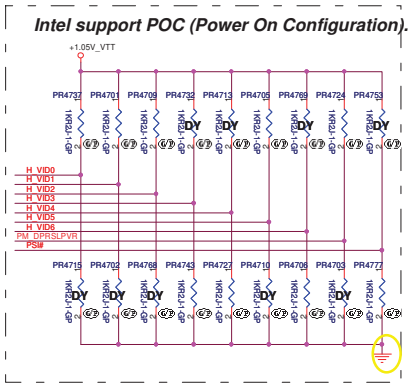
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8205B_5V/3D3V

Size	Document Number	Rev
A1	Berry	A00

Date: Monday, March 08, 2010 Sheet 46 of 50





I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size	Document Number	Rev
A2	Berry	A00

Date: Monday, March 29, 2010 Sheet 47 of 92

<Core Design>

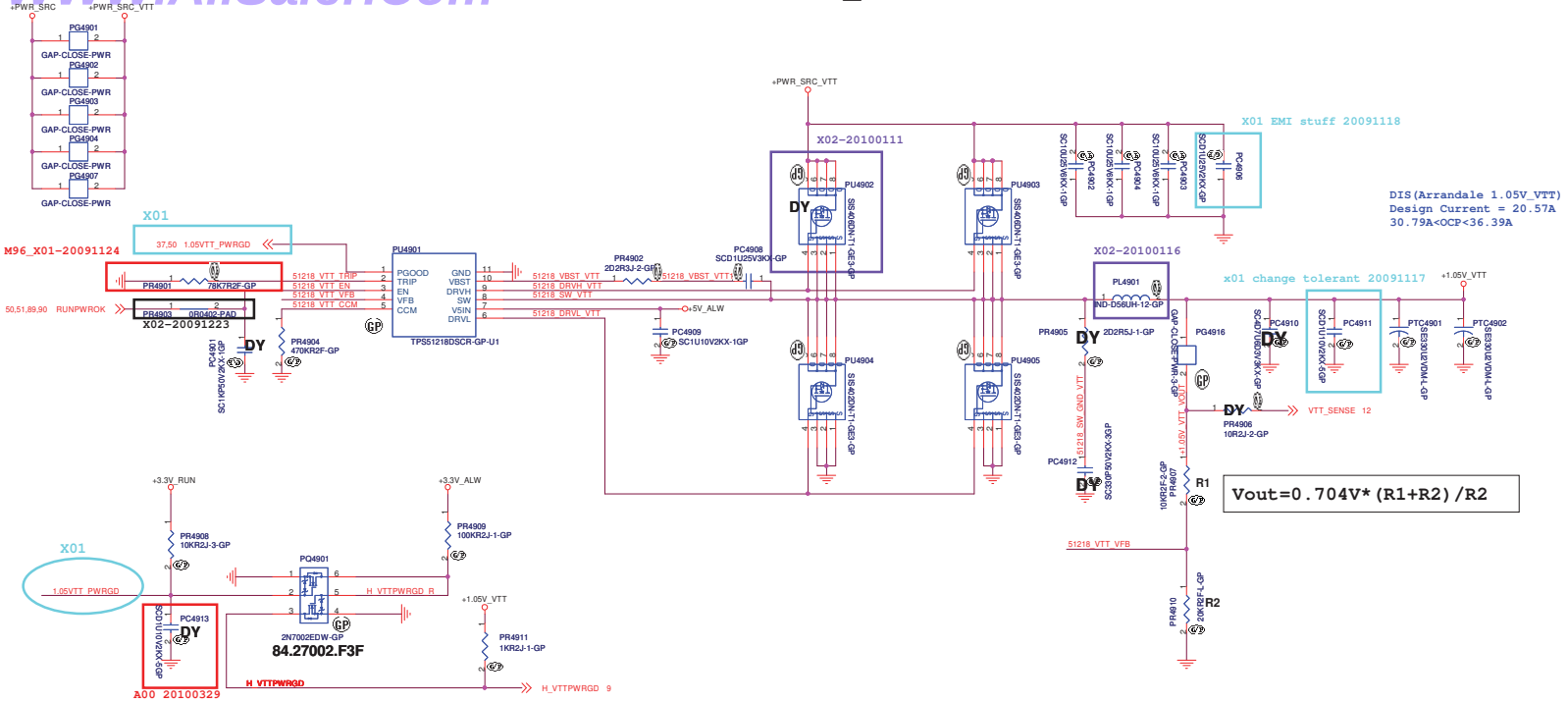
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 48 of 92

TPS51218 for +1.05V_VTT



Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V VTT

Size	Document Number	Rev
A2	Berry	A00

Date: Tuesday, April 06, 2010 Sheet 49 of 92

SSID = PWR.Plane.Regulator_1p5v0p75v

Modified net name

+PWR_SRC_1D5V

x01-20091124

PR5002 14K7R2F-L-GP

PC5002 SC1KP50V2KX-1GP

PC5003 SC1U10V2KX-1GP

PC5001 SC1U10V2KX-1GP

PR5001 5D1R3J-GP

PR5004 20KR2F-L-GP

PR5006 620KR2F-GP

PR5005 0R3J-0-U-GP

PD5001 RB551V-30-2GP

PU5001 TPS51116RGER-GP-U

PC5005 SC1U6D3V2KX-GP

PR5008 1M1R2J-GP

PR5009 0R0402-PAD

PC5007 SC1KP50V2KX-1GP

PR5010 0R2J-2-GP

PC5008 SC1U10V2KX-1GP

PR5011 0R0603-PAD

PC5010 SCD033U16V3KX-GP

x01 change tolerant 20091117

X02-20091223

RT: ASM
TI: Non_ASM

Design Current = 0.7A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

5 S3 Power Reduction X01 20091111

PQ5003 2N7002E-1-GP 84.2N702.D31

PQ5002 2N7002E-1-GP 84.2N702.D31

PQ5001 PMBS3904-1-GP

PR5016 100KR2J-1-GP

PR5017 4K7R2J-2-GP

PR5018 10KR2J-3-GP

PR5015 0R2J-2-GP

PR5019 0R0402-PAD

PR5003 0R2J-2-GP

PC5024 SCD1U10V2KX-5GP

PC5004 SCD1U10V2KX-5GP

x01 change tolerant 20091118

X02-20091224

X02-20091223

PR5007 0R0402-PAD

PC5006 SCD1U10V2KX-5GP

x01 change tolerant 20091117

PG5002 PG5003 PG5004 PG5006 GAP-CLOSE-PWR

PU5002 PU5003 PU5004 SI7686DP-T1-GP SIR460DP-T1-GE3-GP

PC5009 PC5011 PC5012 PC5013 PC5014 SC10U25V6KX-1GP SCD1U25V2KX-GP SC4D7U25V6KX-GP

Design Current = 14.45A
22.71A<OCP< 26.84A

PC5019 SCD1U25V3KX-GP

X02-20100116

PL5001 IND-1D5UH-34-GP

PR5012 2D2R5F-2-GP

PC5022 SC330P50V2KX-3GP

X02-20100201

PC5020 SC4D7U6D3V3KX-GP

PC5021 SCD1U10V2KX-5GP

PTC5002 PTC5001 SE330U2VDM-1-GP

x01 change to 330uF 20091124

x01 change tolerant 20091117

PR5013 30KR2F-GP

PR5014 30KR2F-GP

PC5023 SC18P50V2JN-1-GP

Close to VFB Pin (pin5)

PG5001 PG5016 GAP-CLOSE-PWR

PC5015 PC5016 PC5017 PC5018 SCD1U10V2KX-5GP SC10U6D3V5MX-3GP

x01 change tolerant 20091117

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

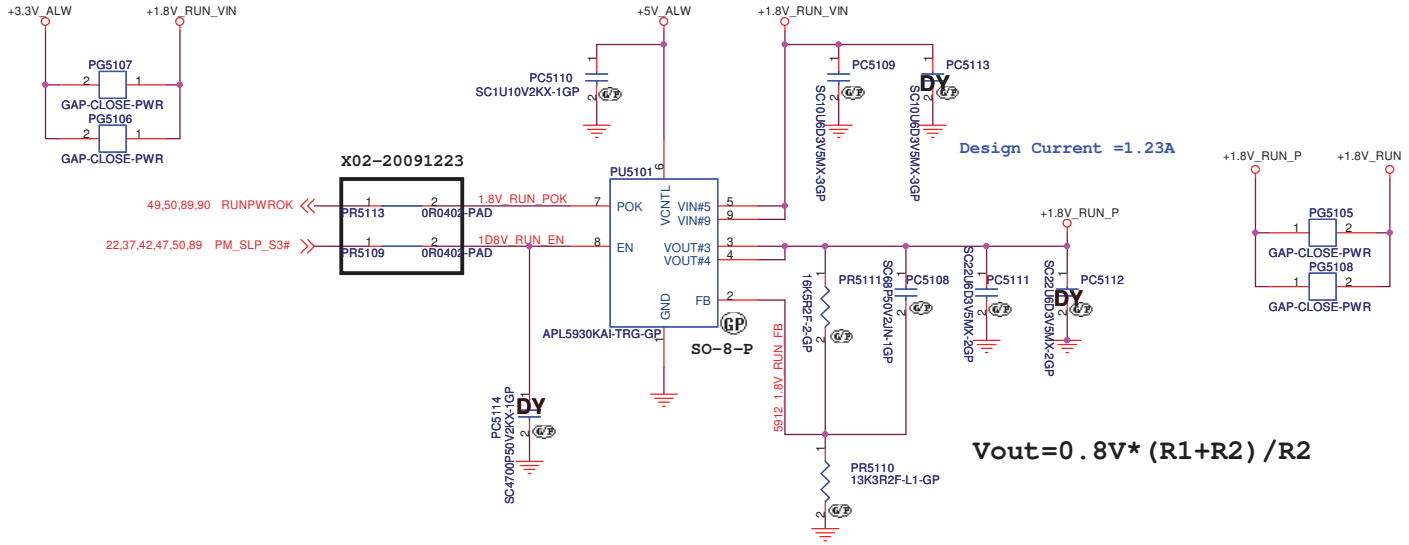
Title: TPS51116_+1.5V_SUS

Size: Custom | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 50 of 92

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930_+1.8V_RUN	
Size A3	Document Number Berry	Rev A00
Date: Monday, March 29, 2010	Sheet 51 of 92	

<Core Design>

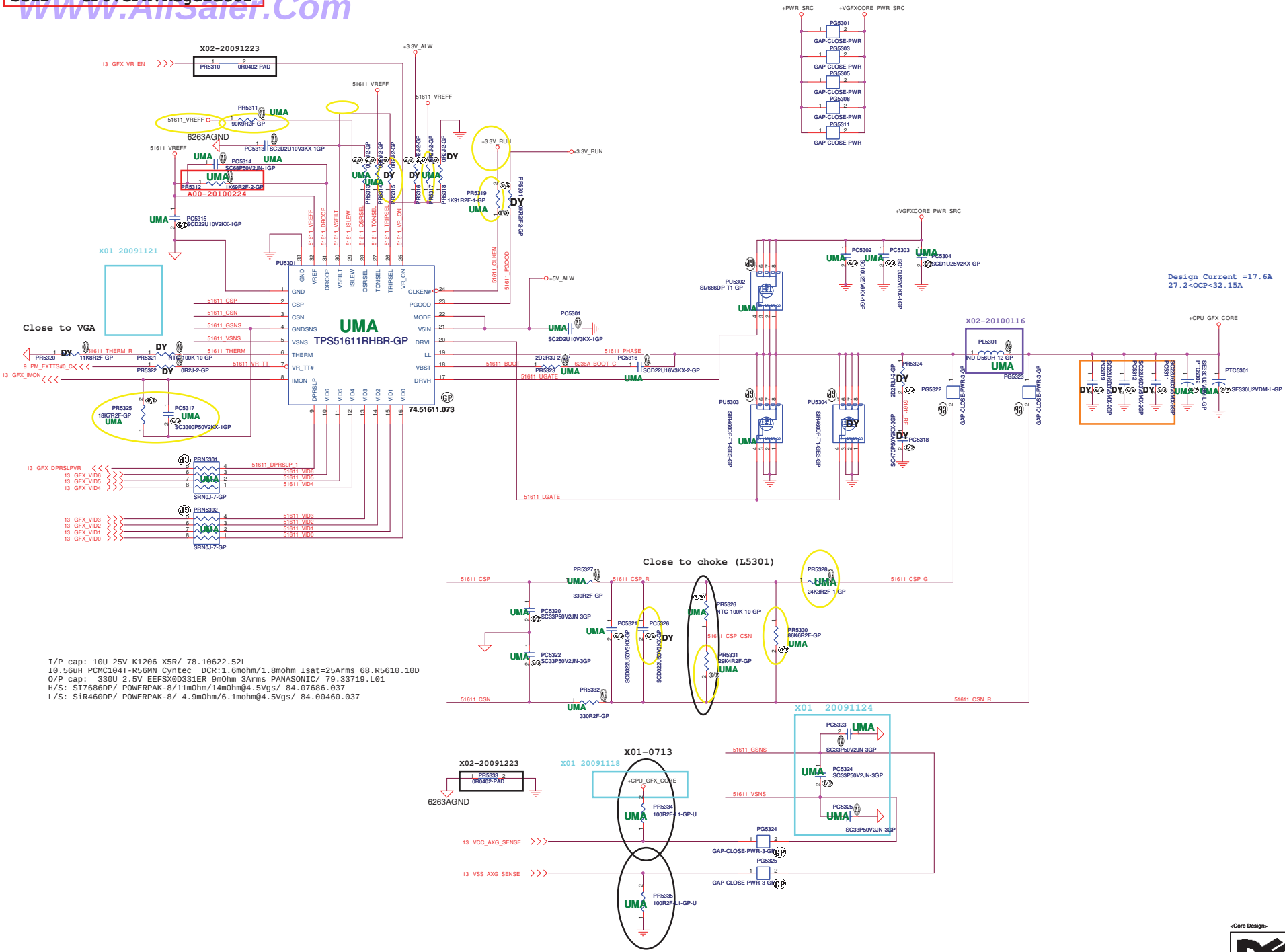
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

Date: Wednesday, February 10, 2010 Sheet 52 of 92

SSID = CPU.GFX.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

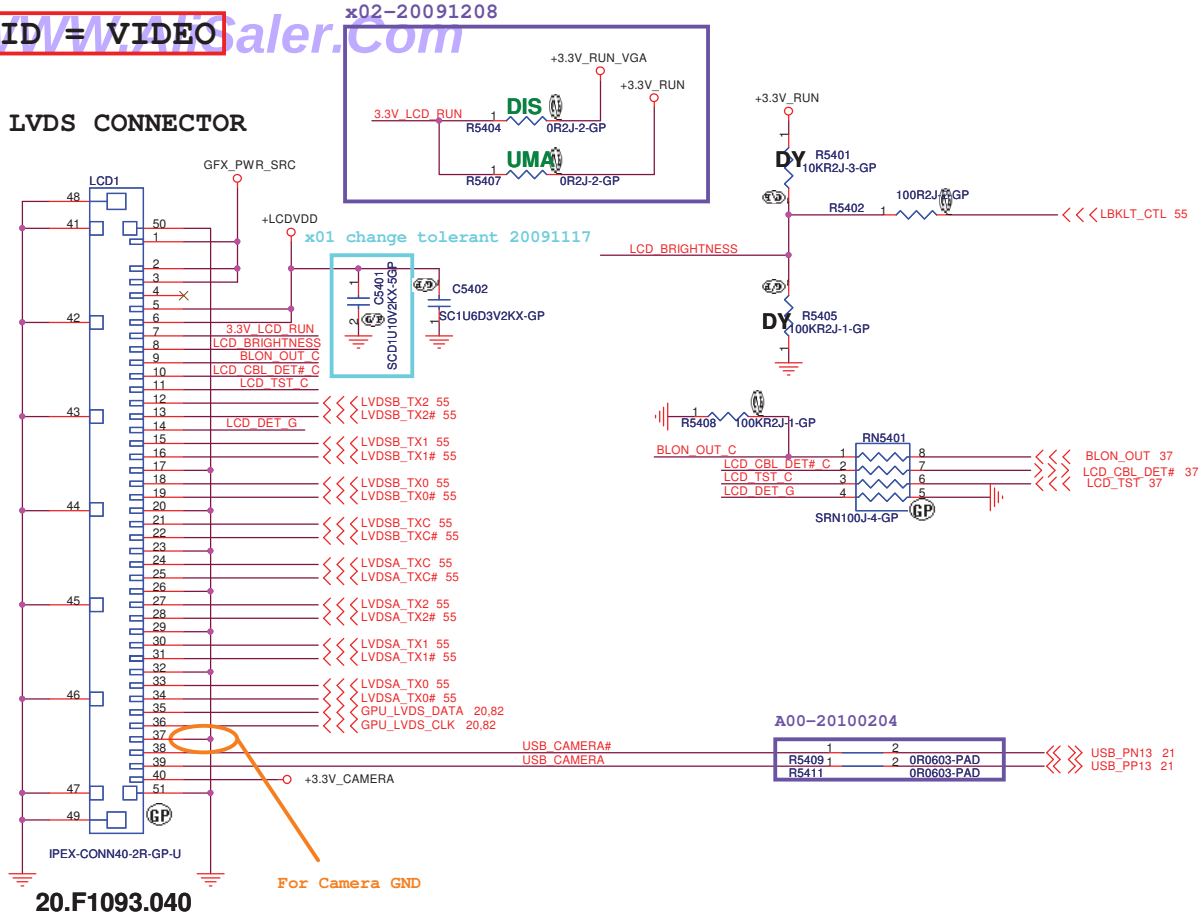
Title: TPS51611_+GFX_CORE(UMA)

Size	Document Number	Rev
A2	Berry	A00

Date: Monday, March 29, 2010 Sheet 53 of 92

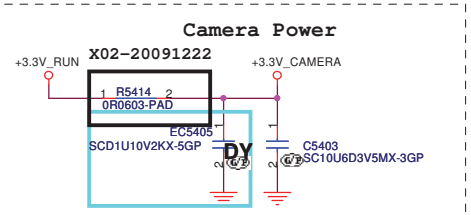
SSID = VIDEO

LVDS CONNECTOR



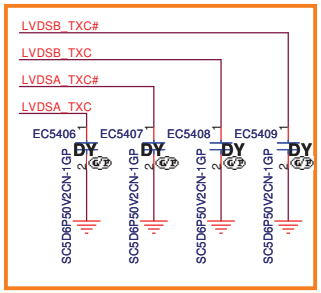
20.F1093.040

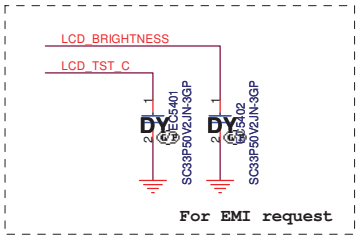
Camera Power



x01 change tolerant 20091117

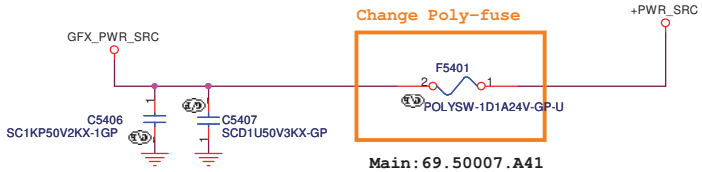
Close to LVDS connector





SSID = Inverter

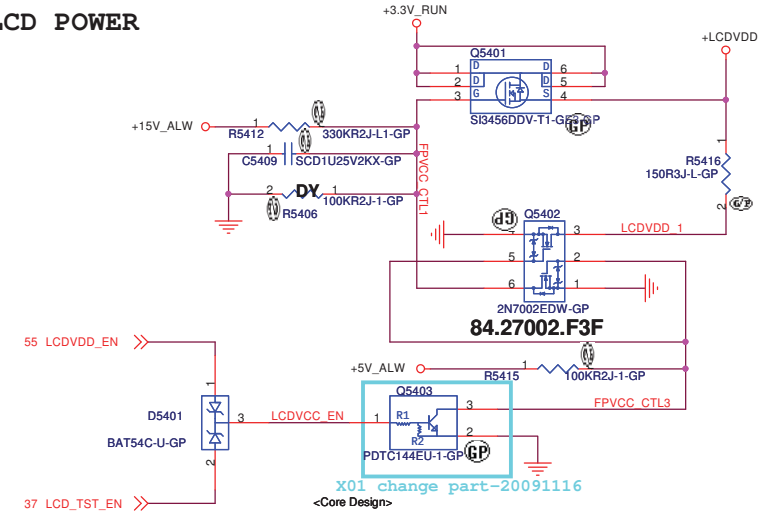
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER



X01 change part-20091116

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD/Inverter Connector		
Size: A3	Document Number: Berry	Rev: A00
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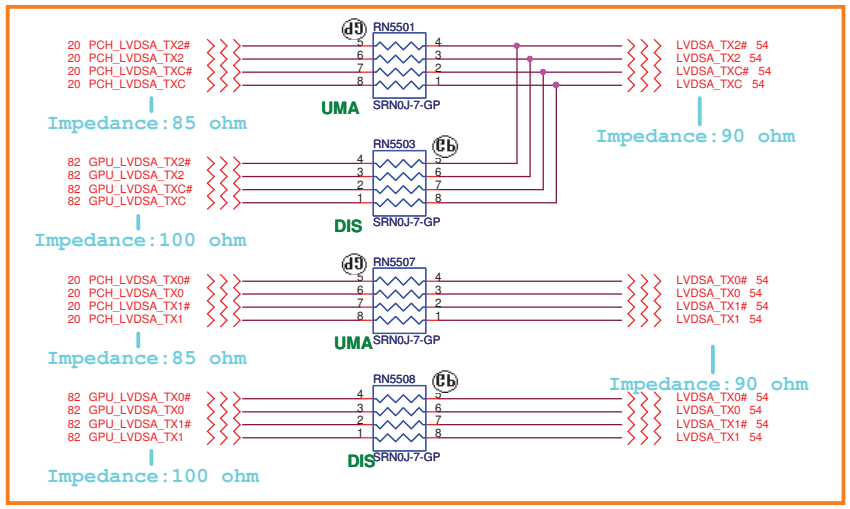
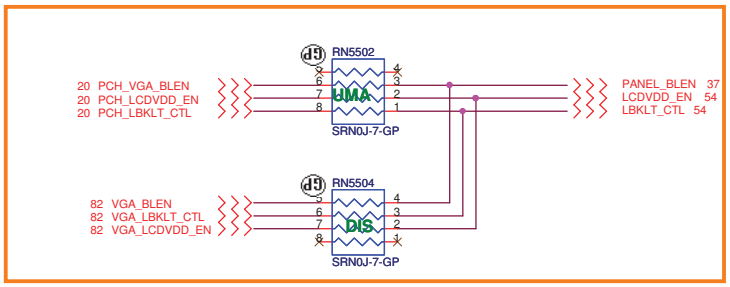
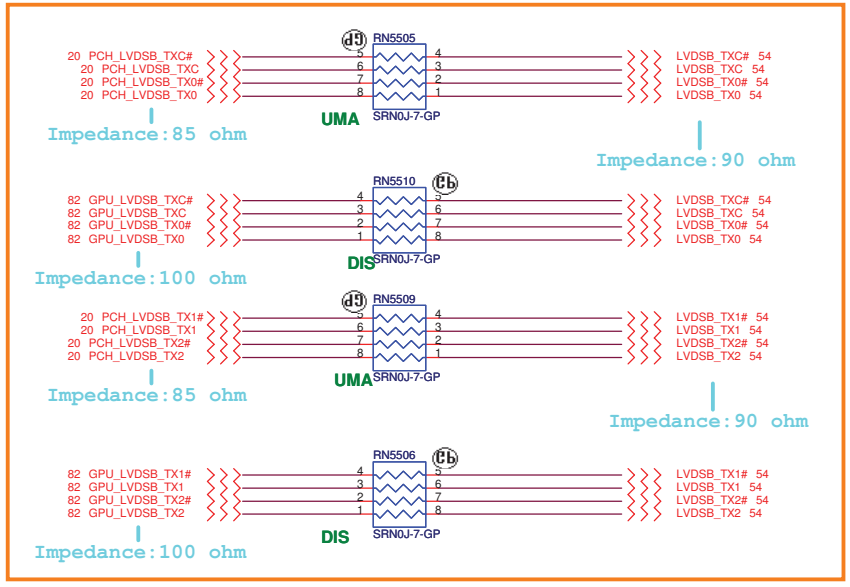
LVDS Channel A



Panel BL brightness/Power En/BL En



LVDS Channel B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LVDS_Switch	
Size	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 55 of 92	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS Switch

Size	Document Number	Rev
A3	Berry	A00

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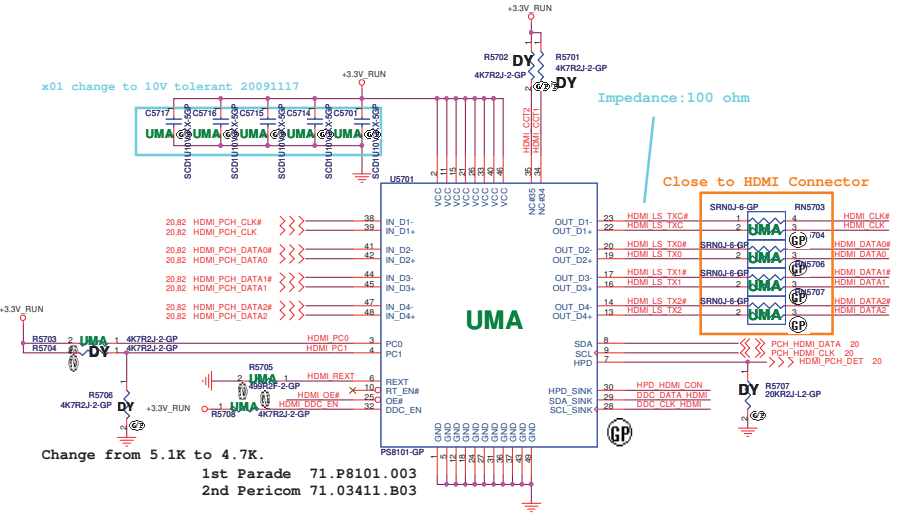
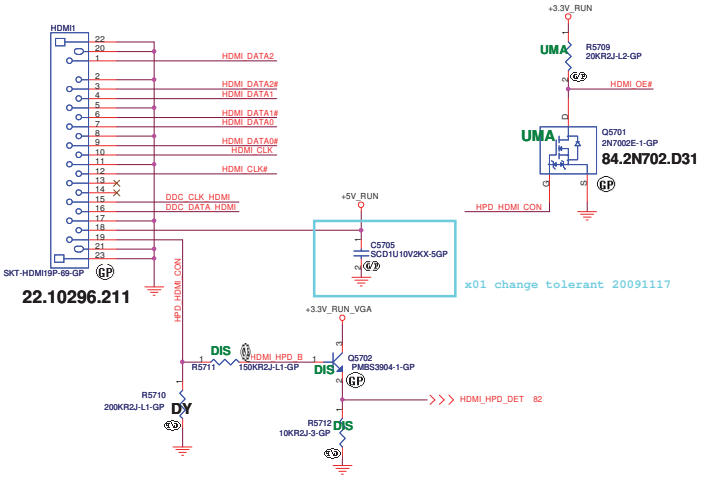
SSID = VIDEO

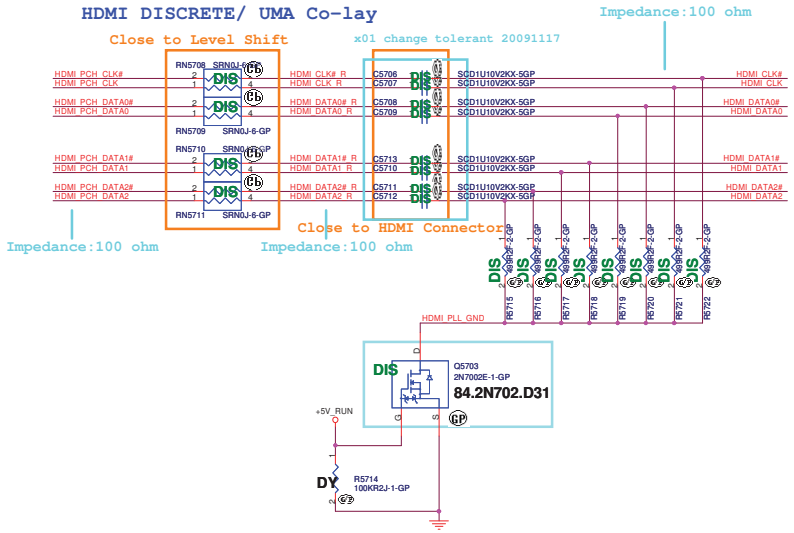
HDMI Level Shifter & CONNECTOR

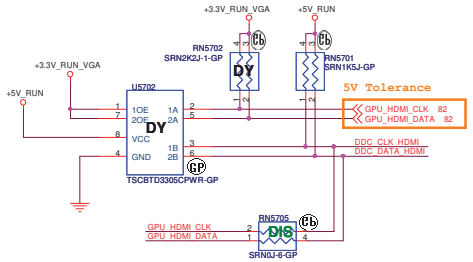


HDMI CONN



HDMI DISCRETE/ UMA Co-lay





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

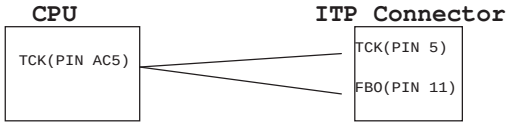
Size	Document Number	Rev
A2	Berry	A00

Date: Monday, March 29, 2010 Sheet 57 of 92

SSID = User.Interface

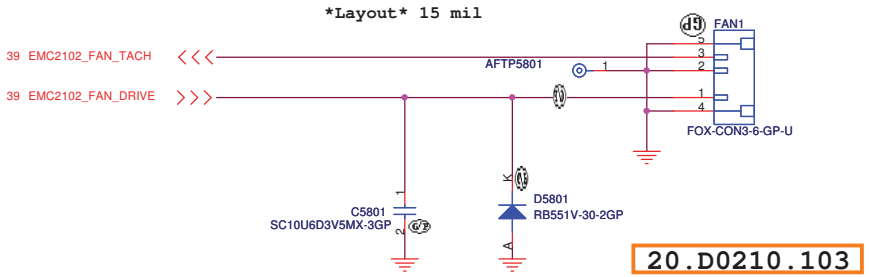
ITP Connector

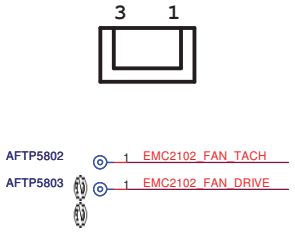
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector





20.D0210.103

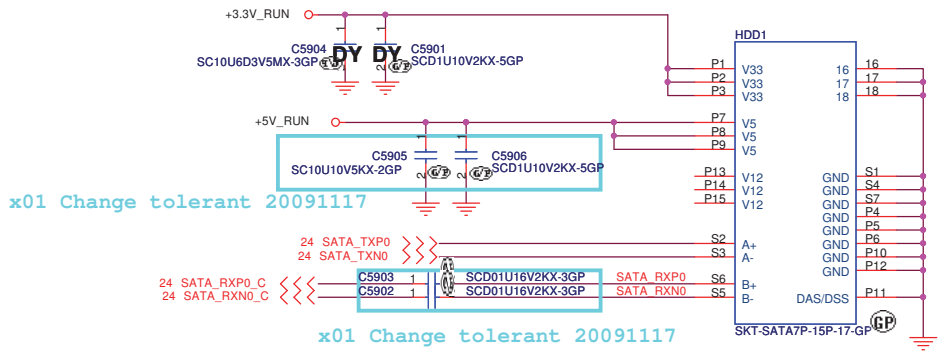
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector		
Size: A3	Document Number: Berry	Rev: A00
Date: Monday, March 29, 2010	Sheet 58 of 92	

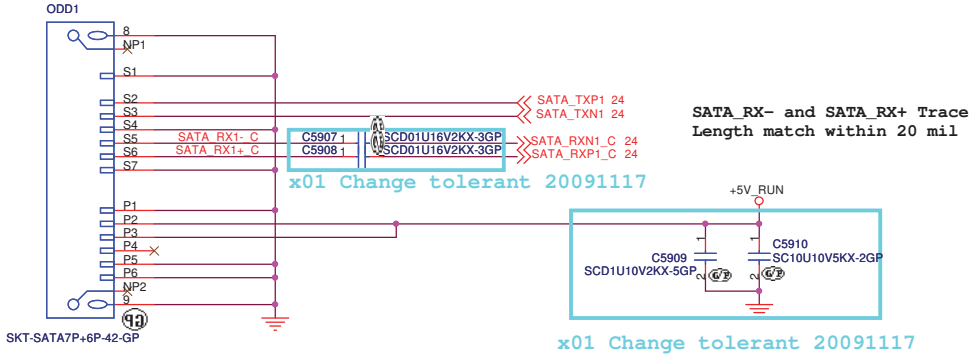
SSID = SATA

SATA HDD Connector



62.10065.C71

ODD Connector



SATA_RX- and SATA_RX+ Trace Length match within 20 mil

62.10065.581

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

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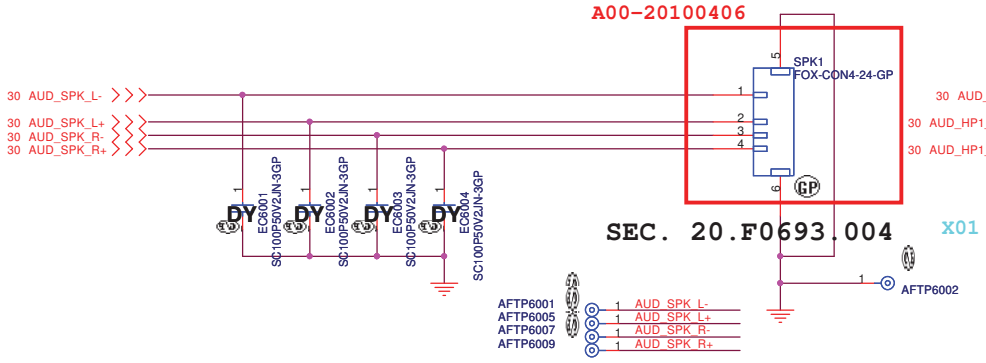
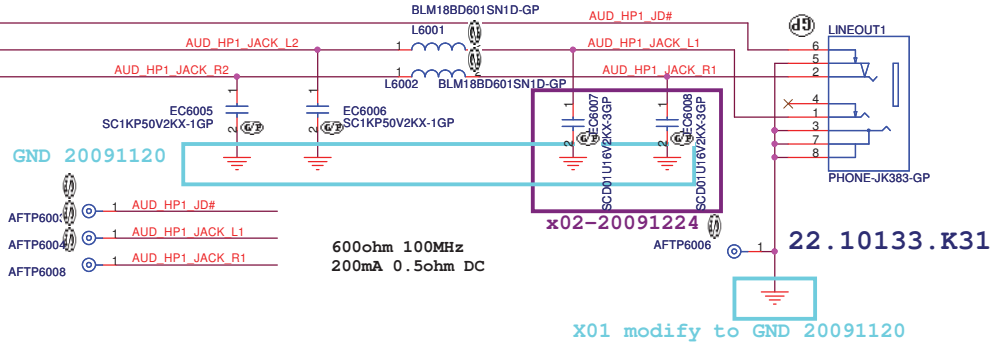
SSID = AUDIO

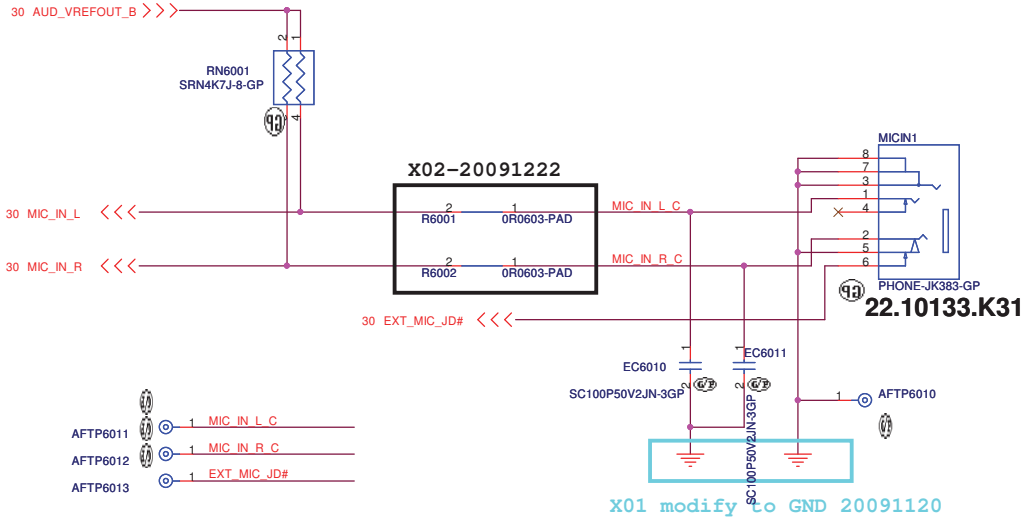
Speaker Connector



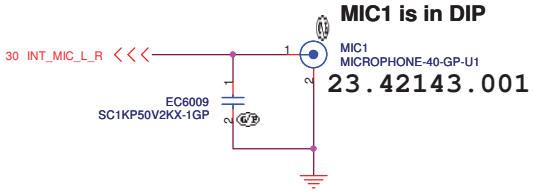
LINE1 OUT

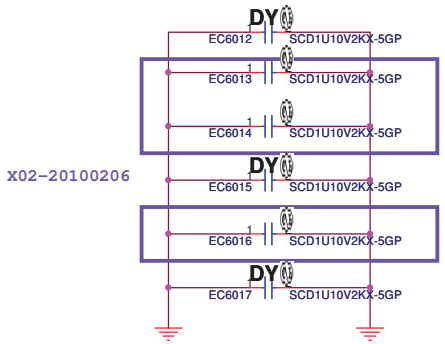


MIC IN



Internal Microphone





<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: Audio Jack
Size: A3
Document Number: Berry
Rev: A00
Date: Monday, April 26, 2010
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

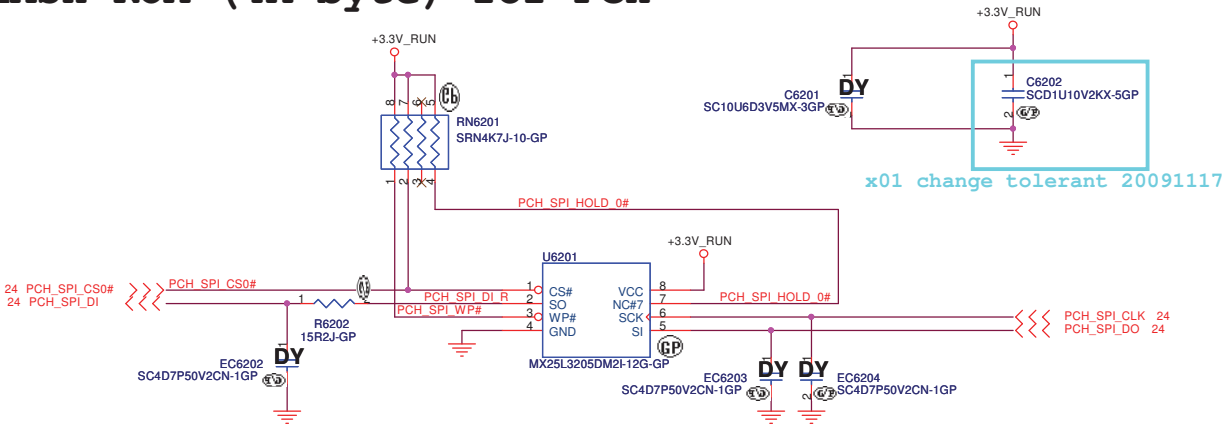
Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

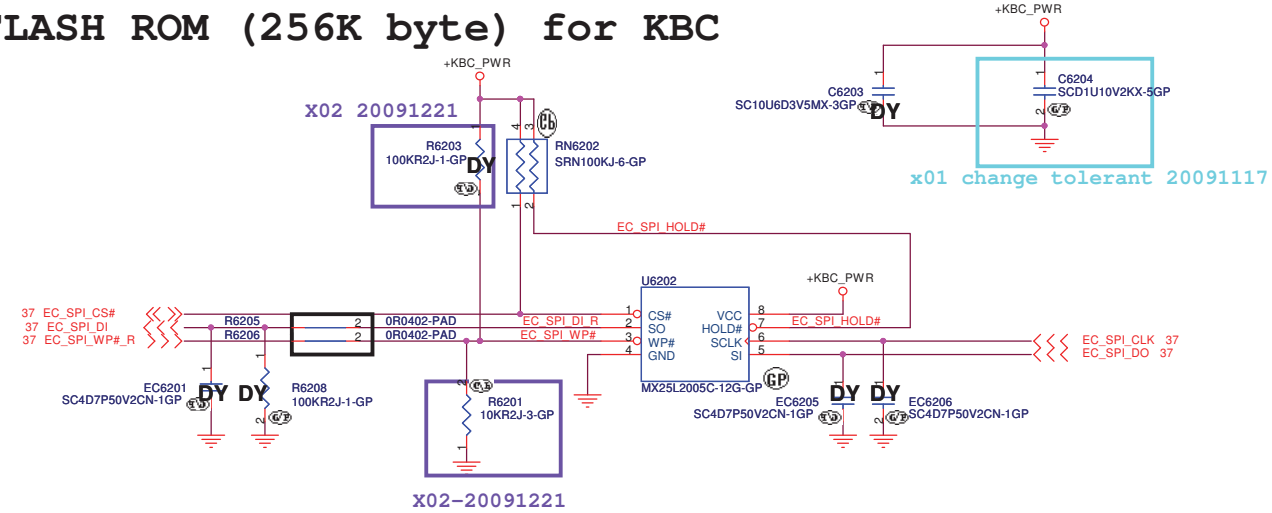
Date: Wednesday, February 10, 2010 Sheet 61 of 92

SSID = Flash.ROM

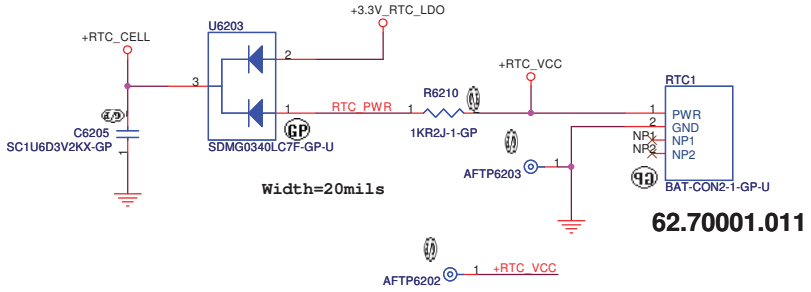
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

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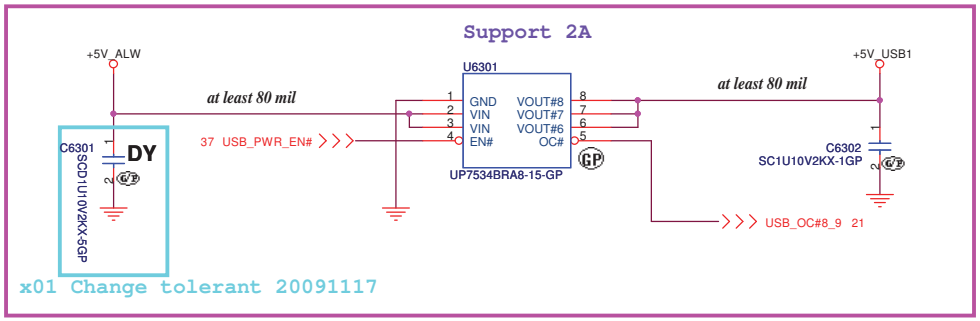
SSID = USB

IO Board USB Power

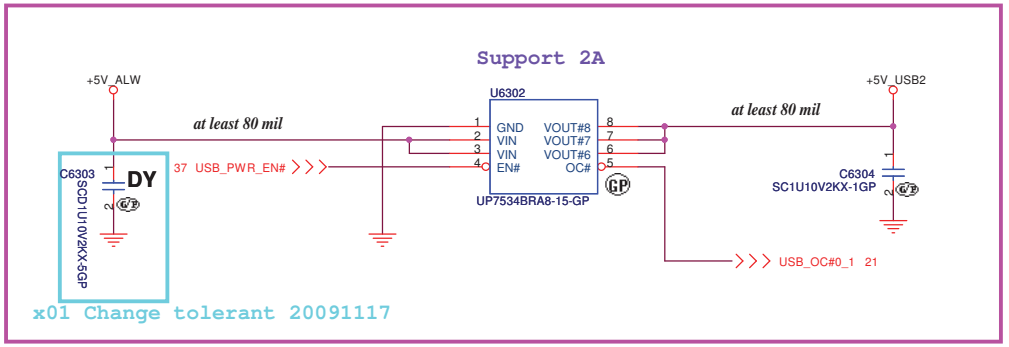
USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079

Close to I/O connector



CRT Board USB Power

Close to CRT Board connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
A3	*Berry*	*A00*

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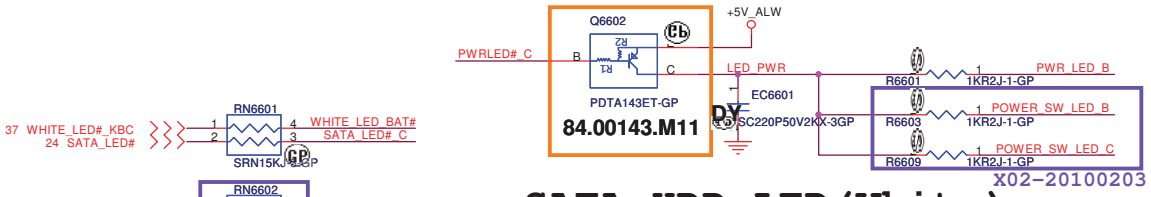
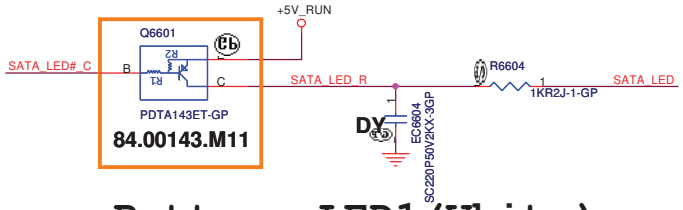
SSID = User Interface

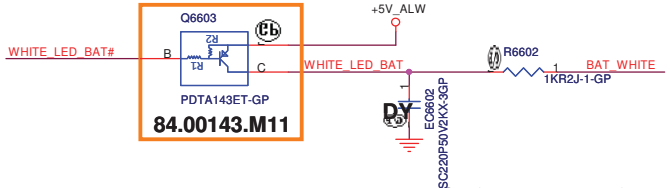
Power LED(White)

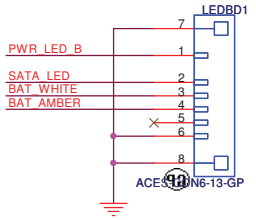


SATA HDD LED(White)

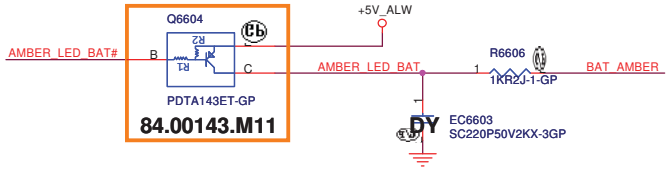


Battery LED1(White)

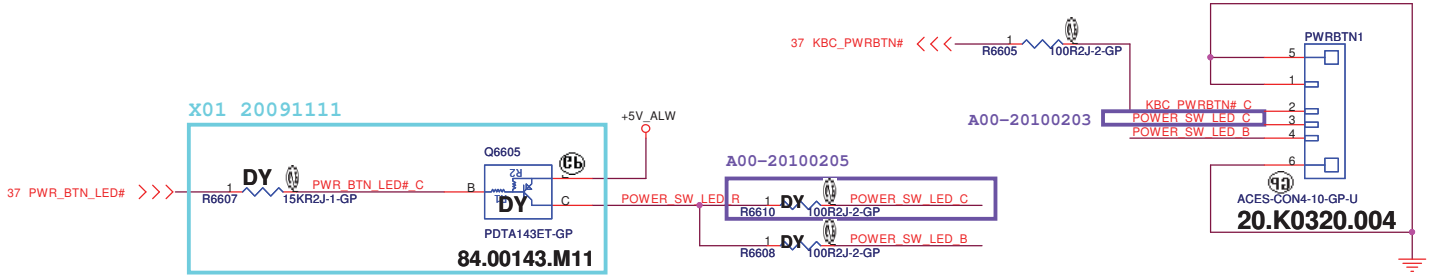




Battery LED2(Amber)



Power button LED(White)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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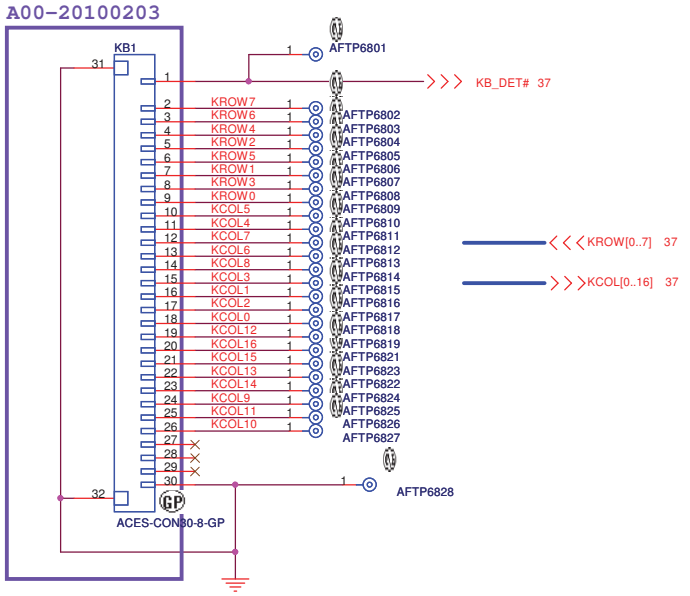
SSID = KBC

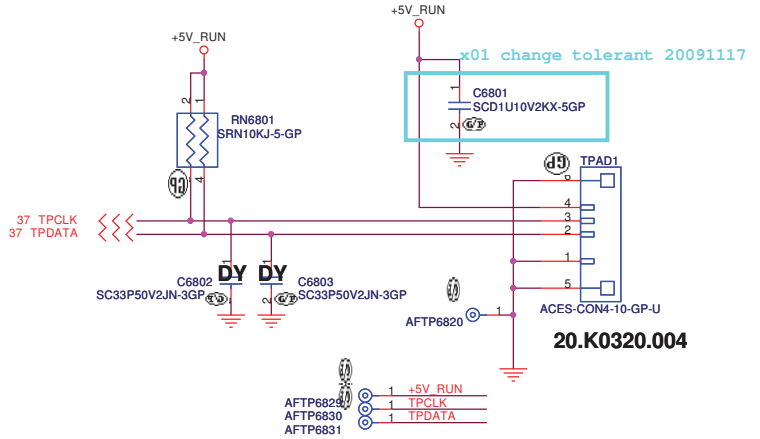
Internal KeyBoard Connector

A00-20100203



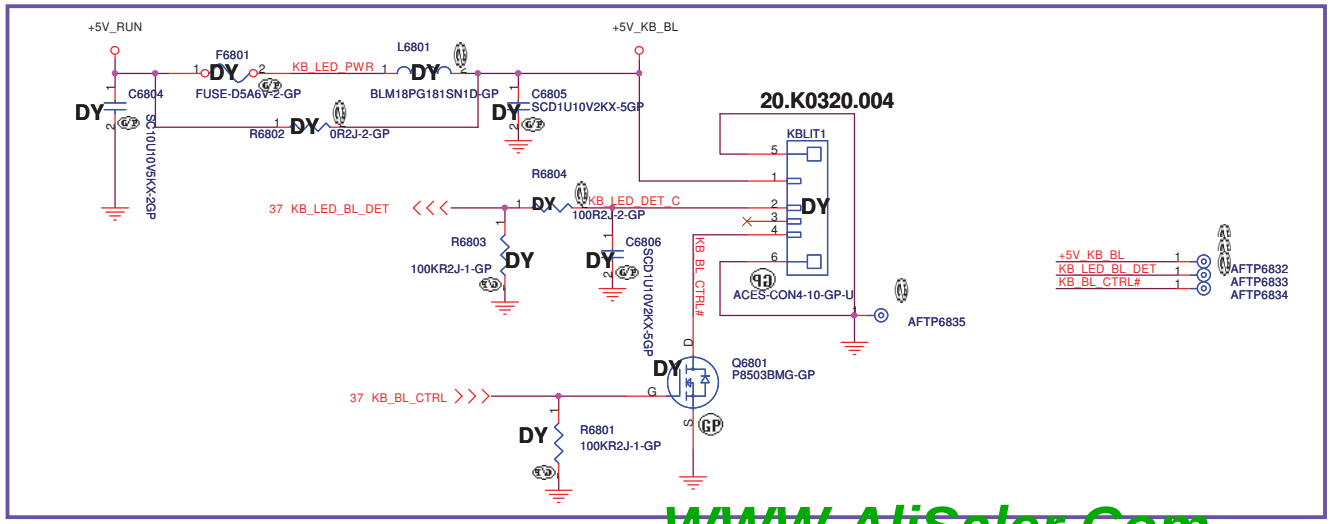
SSID = Touch.Pad

TouchPad Connector



KB Backlight Connector

A00-20100205



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

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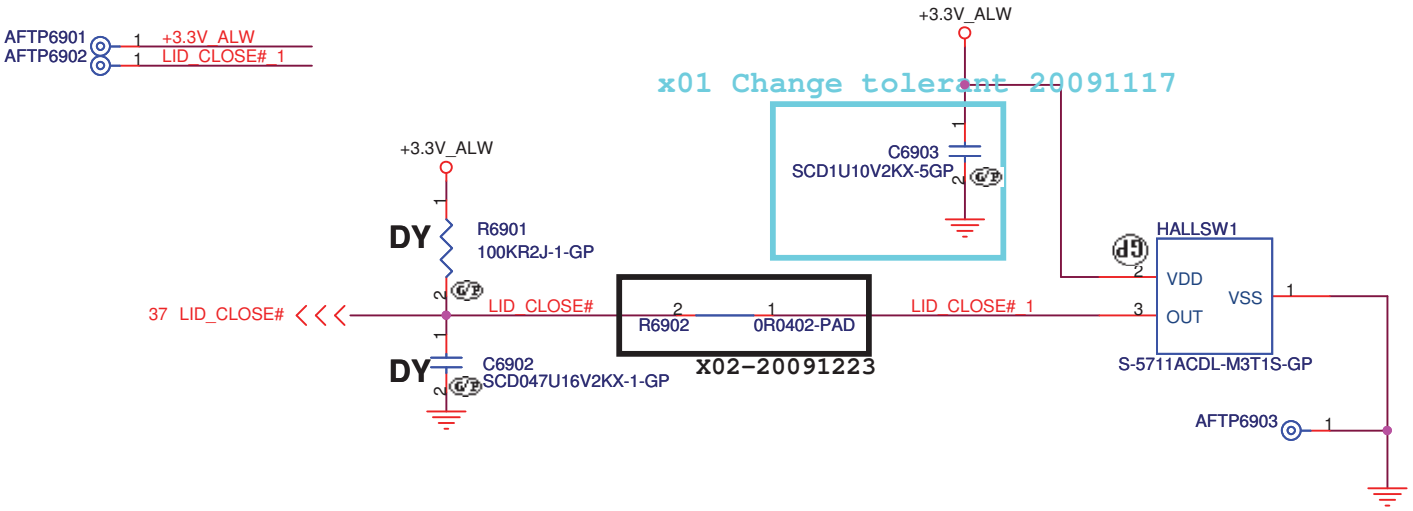

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

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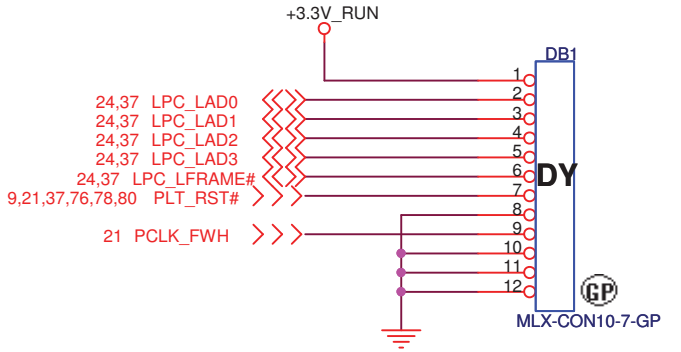

20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

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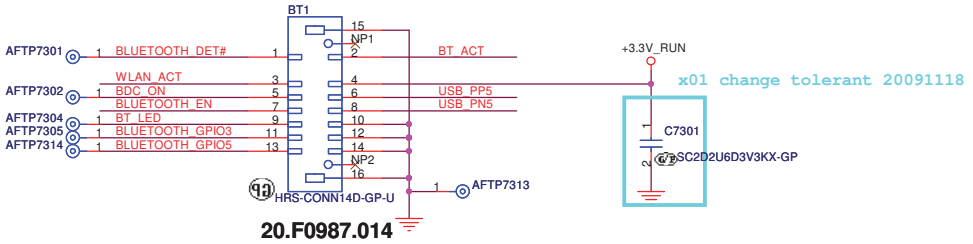
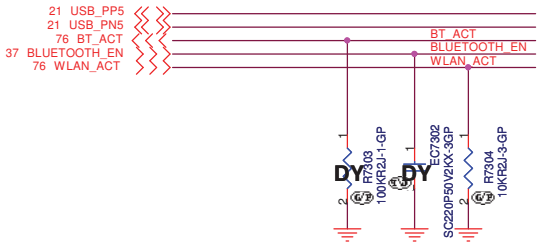
SSID = User.Interface

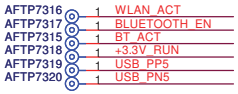
Bluetooth Module conn.



x01 change tolerant 20091118

20.F0987.014





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

Size: A3 | Document Number: Berry | Rev: A00

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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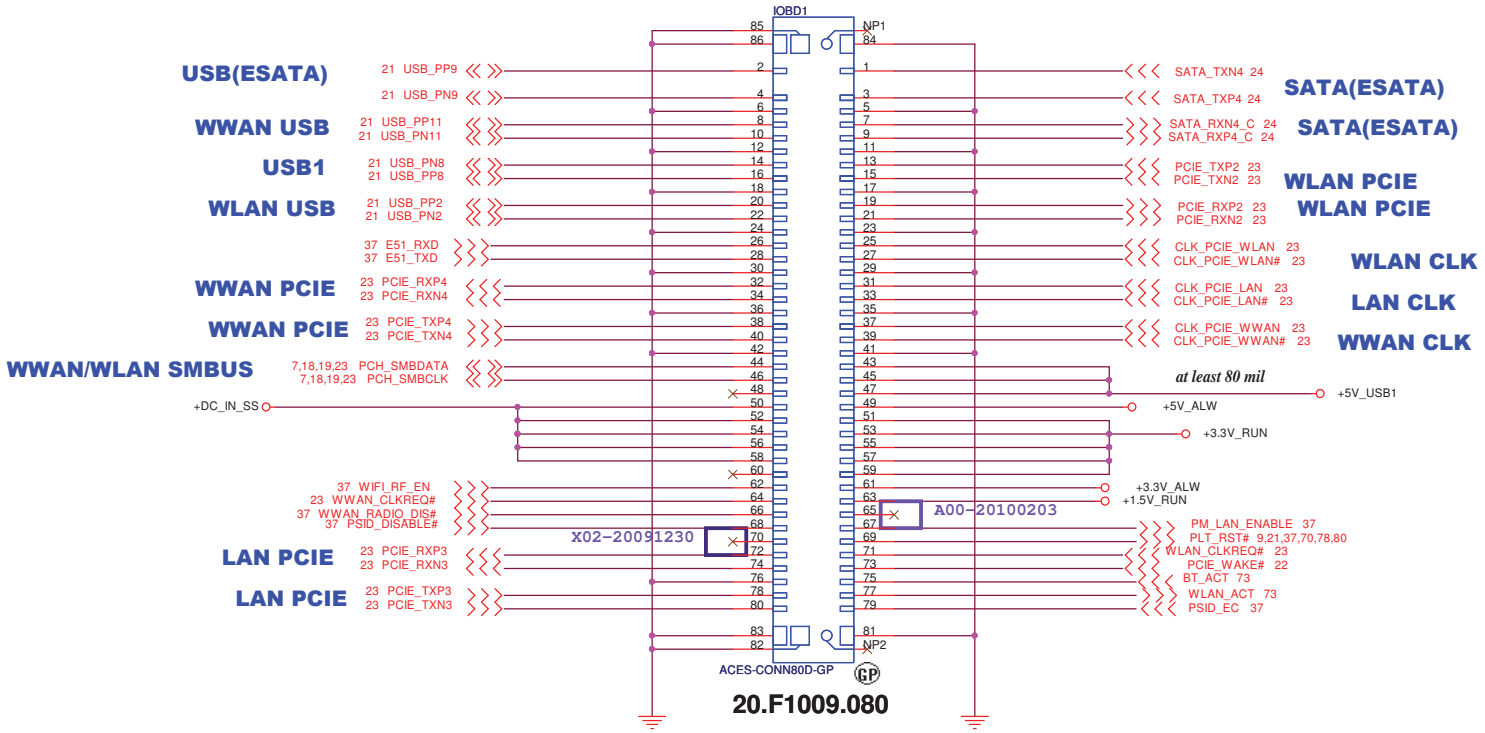
IO Board CONN 80 pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	IO Board Connector	
Size A3	Document Number Berry	Rev A00
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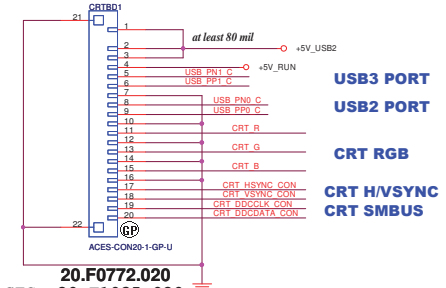
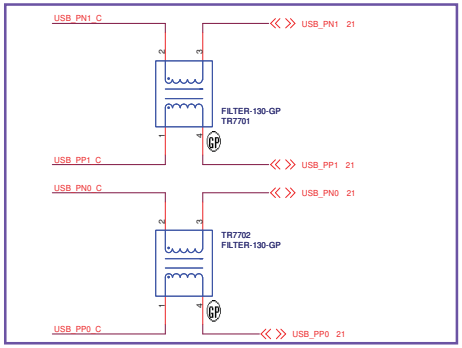
CRT Board Connector



20.F0772.020

SEC. 20.F1035.020

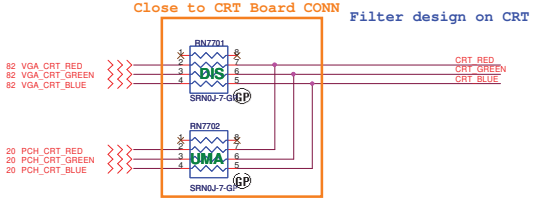
A00-20100120



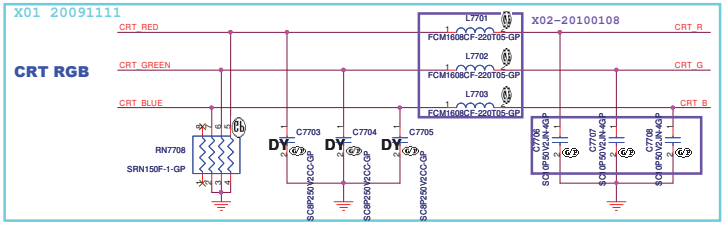
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board

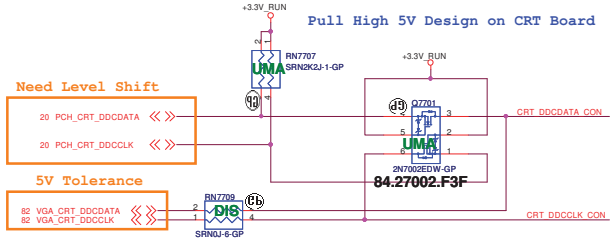


X01 20091111



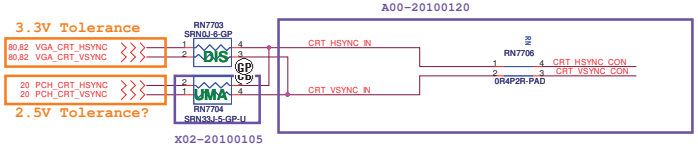
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

Close to CRT Board CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

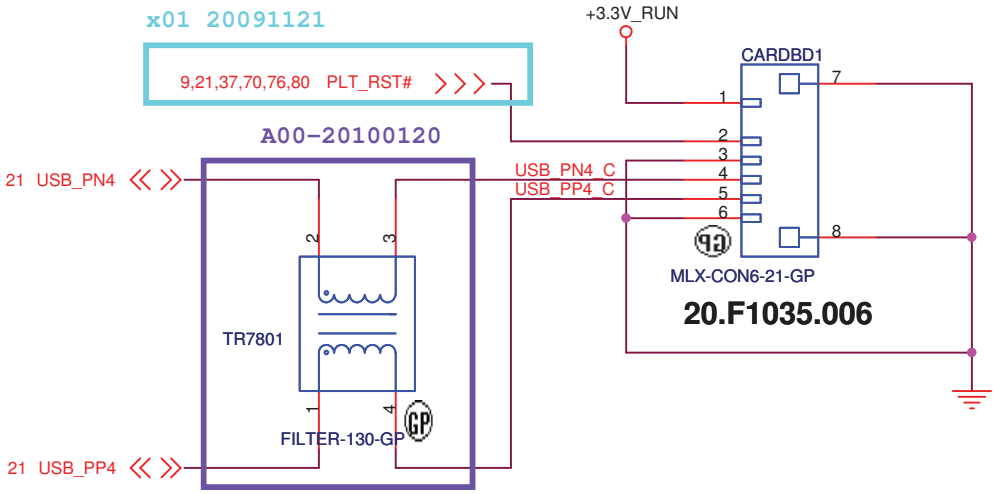
Title: CRT Board Connector

Size: A2 | Document Number: Berry | Rev: A00

Date: Monday, March 29, 2010 | Sheet 77 of 92

SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
A4	Berry	A00

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H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H5 HOLE256R111-GP
H6 HTE95BE95R29-R-5-GP
H7 HTE95BE95R29-R-5-GP
H8 HTE95BE95R29-R-5-GP
H9 HTE95BE95R29-R-5-GP

H10 HOLE335R115-GP
H11 HOLE256R111-GP

CPU Thermal module hole

HTML1 HOLE197R166-GP
HTML2 HOLE197R166-GP
HTML3 HOLE197R166-GP
DY DY DY

GPU Thermal module hole

HGPU1 STF237R117H83-1-GP

stand off

HBT1 STF237R117H123-GP

EMI Reserve

+PWR_SRC
X01 stuff 20091119
EC7901 EC7902 EC7904 EC7903 EC7905 EC7907 EC7909 SCD1U25V2KX-GP
DY EC7942 DY EC7940 DY EC7941 DY EC7939 DY EC7943 DY EC7938 SCD1U25V2KX-GP

+VGFXCORE_PWR_SRC
DY EC7906 SCD1U25V2KX-GP

+PWR_SRC_VTT
EC7911 SCD1U25V2KX-GP
X01 stuff 20091118

+PWR_SRC_1D5V
DY EC7916 SCD1U25V2KX-GP

EMI Reserve

SPR1 SPRING-58-GP
DY

X01 RF Reserved-20091118

+PWR_SRC_1D5V 56pF*1
DY EC7908 SC56P50V2JN-2GP

+PWR_SRC 56pF*7
DY EC7912 DY EC7913 DY EC7917 DY EC7919 DY EC7920 DY EC7922 DY EC7925 SC56P50V2JN-2GP

+PWR_SRC +1.5V_SUS 0.1uF*2
EC7921 EC7933 SCD1U25V2KX-GP

X02-20100208

+1.05V_VTT
DY EC7923 UMA EC7924 UMA EC7926 UMA EC7927 SCD1U25V2KX-GP

+1.5V_SUS
DY EC7945 DY EC7929 DY EC7936 DY EC7944 SCD1U25V2KX-GP

A00-20100204

+CPU_GFX_CORE 0.1uF*2
DY EC7946 DY EC7947 SCD1U25V2KX-GP

+VGA_CORE 56pF*1
DY EC7928 SC56P50V2JN-2GP

+1.5V_SUS 56pF*3
DY EC7930 DY EC7931 DY EC7932 SC56P50V2JN-2GP

+VCC_CORE 56pF*2
UMA EC7934 DY EC7935 SC56P50V2JN-2GP

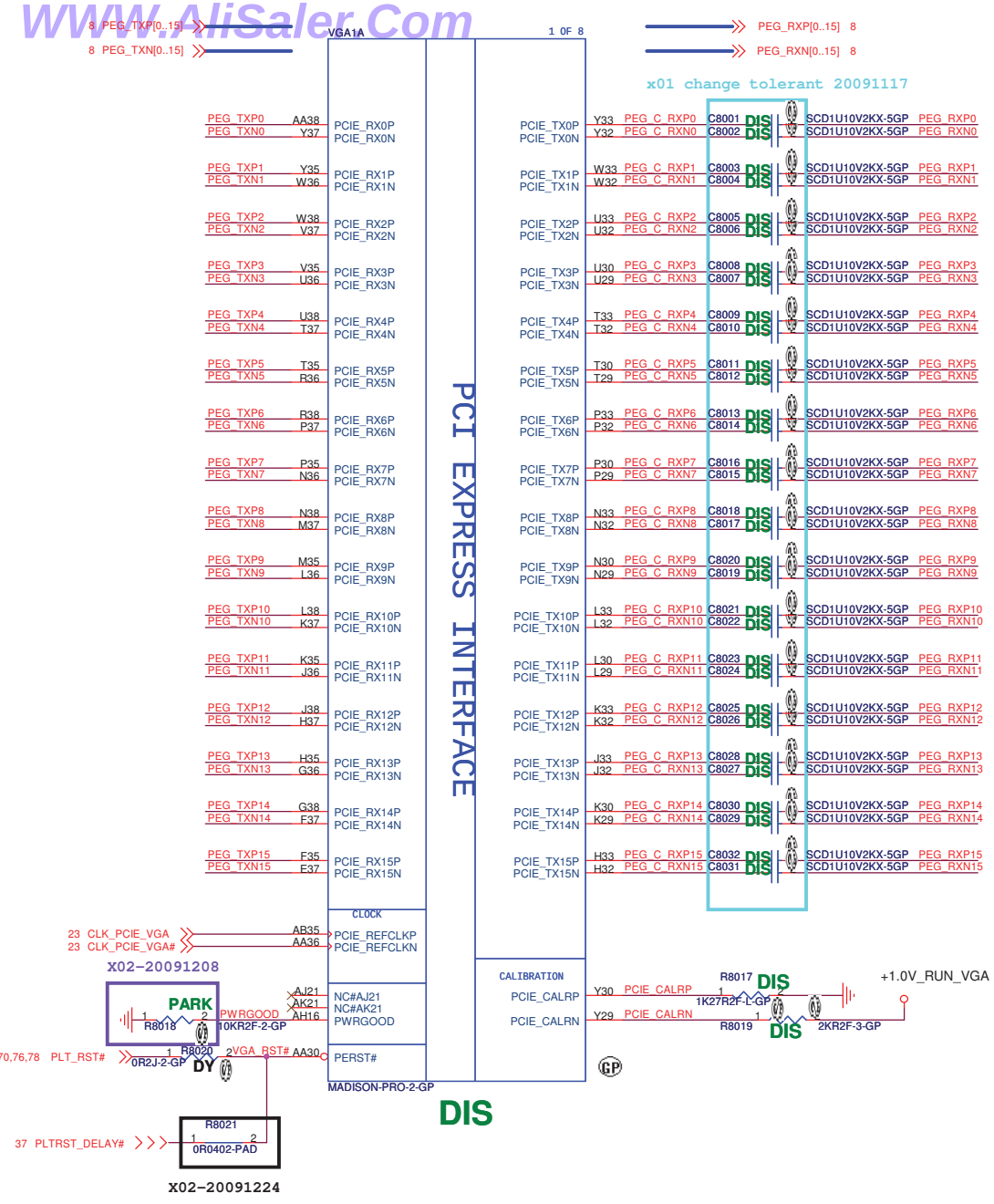
X02-20100209

+5V_RUN 56pF
DY EC7937 SC56P50V2JN-2GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: Berry | Rev: A00
Date: Wednesday, February 10, 2010 | Sheet 79 of 92



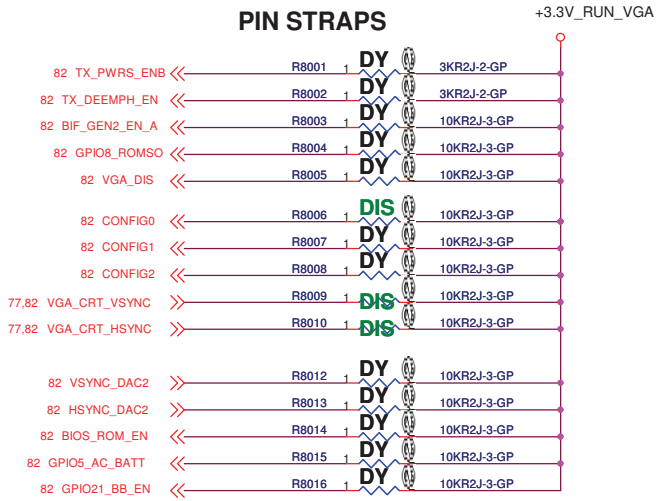
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A3	Berry	A00

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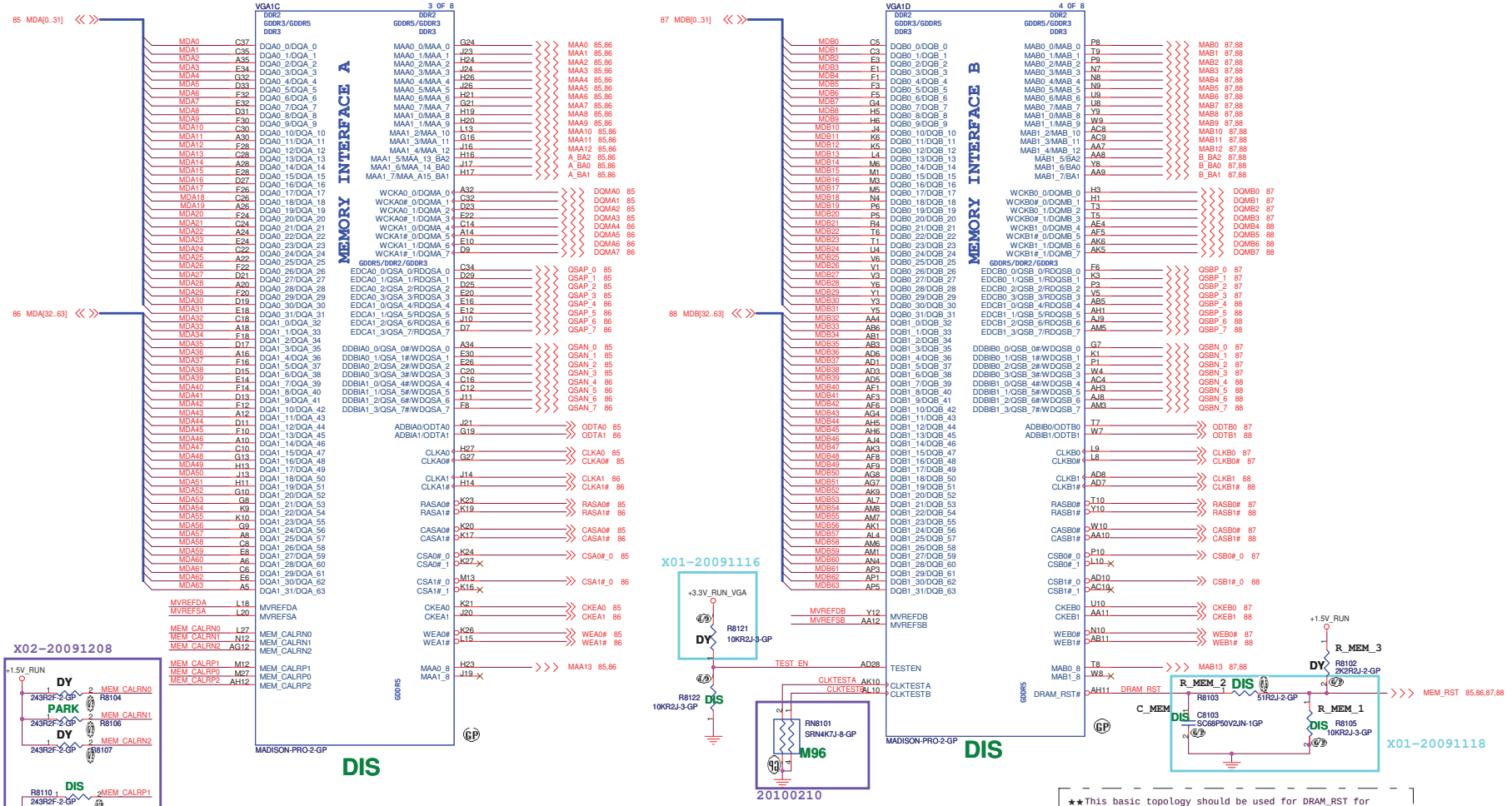

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

x01 Change tolerant 20091117

DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

DDR3/GDDR3 Memory Stuff Option(M92/M96)

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

**This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For Mannhatton	For M96-M2/M92-M2
R_MEM_1	10K	2.2nF
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	68pF	10K

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size	Document Number	Rev
C	Berry	A00

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MEMORY ID Table

DVPDATA[0:3]	Description
0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646B-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16

DVPDATA[0:3] Default:Pull down

MEM_ID Control
X02-20091222

LVDS Interface

I2C Bus for LVDS

Straps

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

X02-20091210
Voltage Swing:1.8V

X02-20091222

DDC1 channel for CRT

DDC2 channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

x01 Change tolerant 20091117

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: A00

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For DDR3/GDDR5, MVDDQ = 1.5V

x01 change tolerant 20091117

x02-20091208

x02-20091224

For UMA +VGA_CORE connect to GND

A00 change 22uF 20100329

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

M97, Broadway, Madison and Park only
M96 do not support core vsense feature

VCORE_SEN/RTN and VDDCI_SEN/RTN route as differetial pair

M97, Broadway, Madison and Park only

(M97, Broadway and Madison: 1.8V@150mA MPV18)
(Park: 1.8V@75mA MPV18)

MADISON-PRO-2-GP

DIS

NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

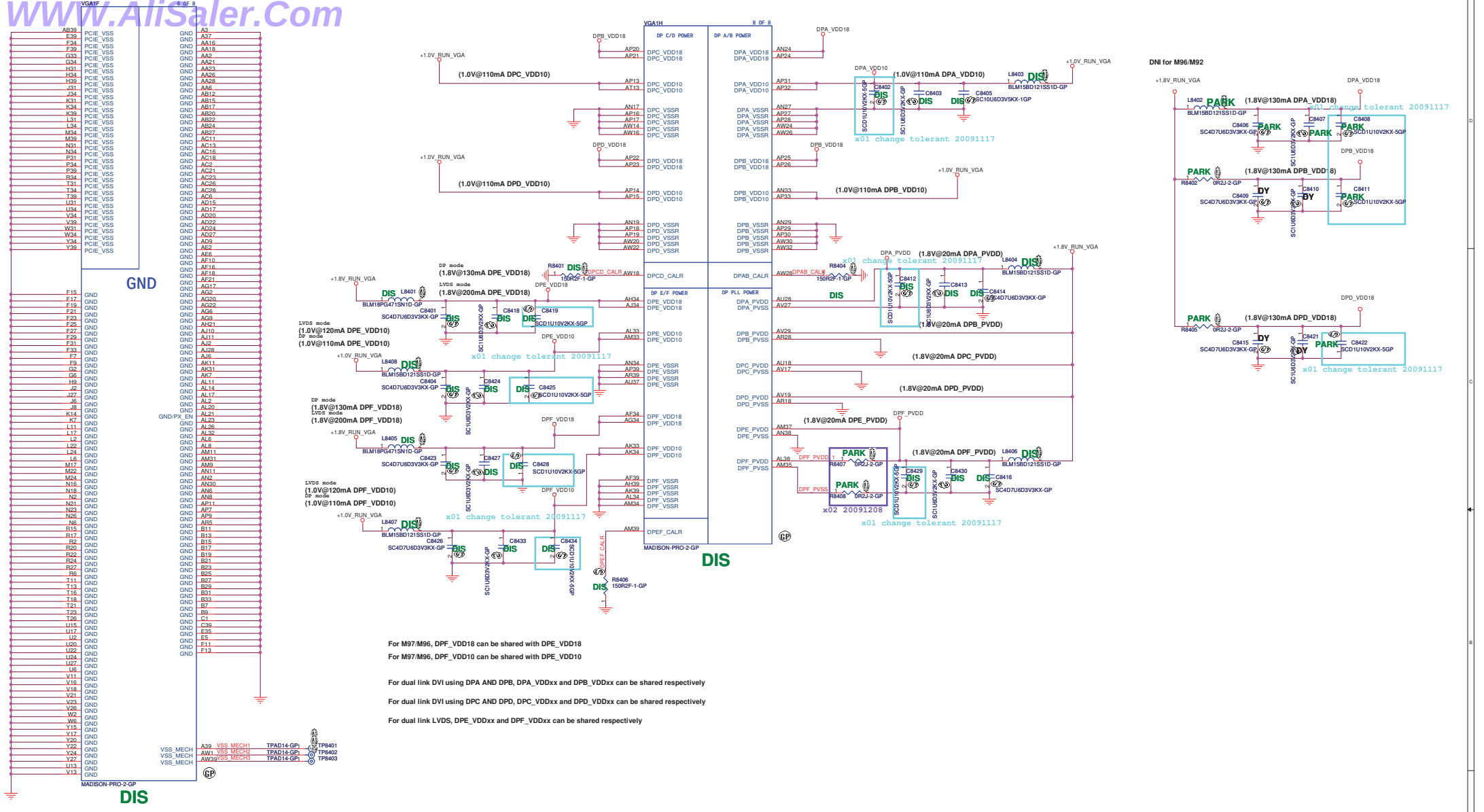
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 | Document Number: Berry | Rev: A00

Date: Wednesday, March 31, 2010 | Sheet 83 of 92



For M97/M96, DPF_VDD18 can be shared with DPE_VDD18

For M97/M96, DPF_VDD10 can be shared with DPE_VDD10

For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively

For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively

For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively

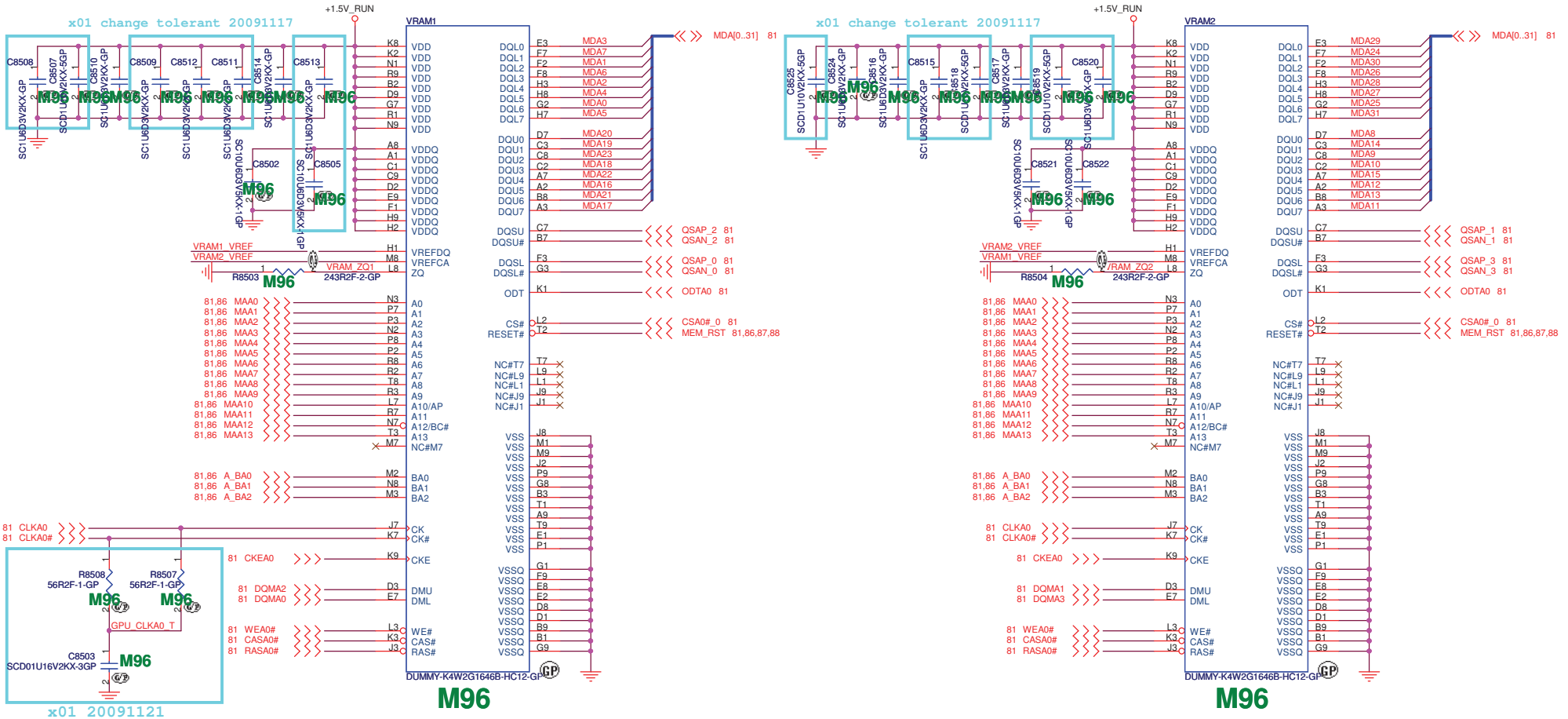
<Core Design>

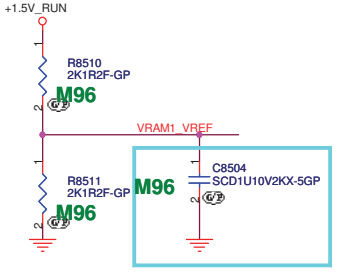
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

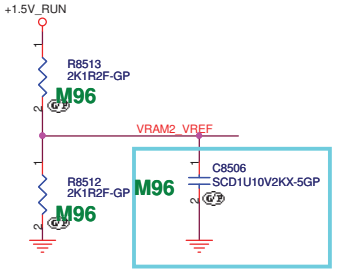
Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A2	Berry	A00

Date: Monday, February 22, 2010 Sheet 84 of 92







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size	Document Number	Rev
Custom	Berry	A00

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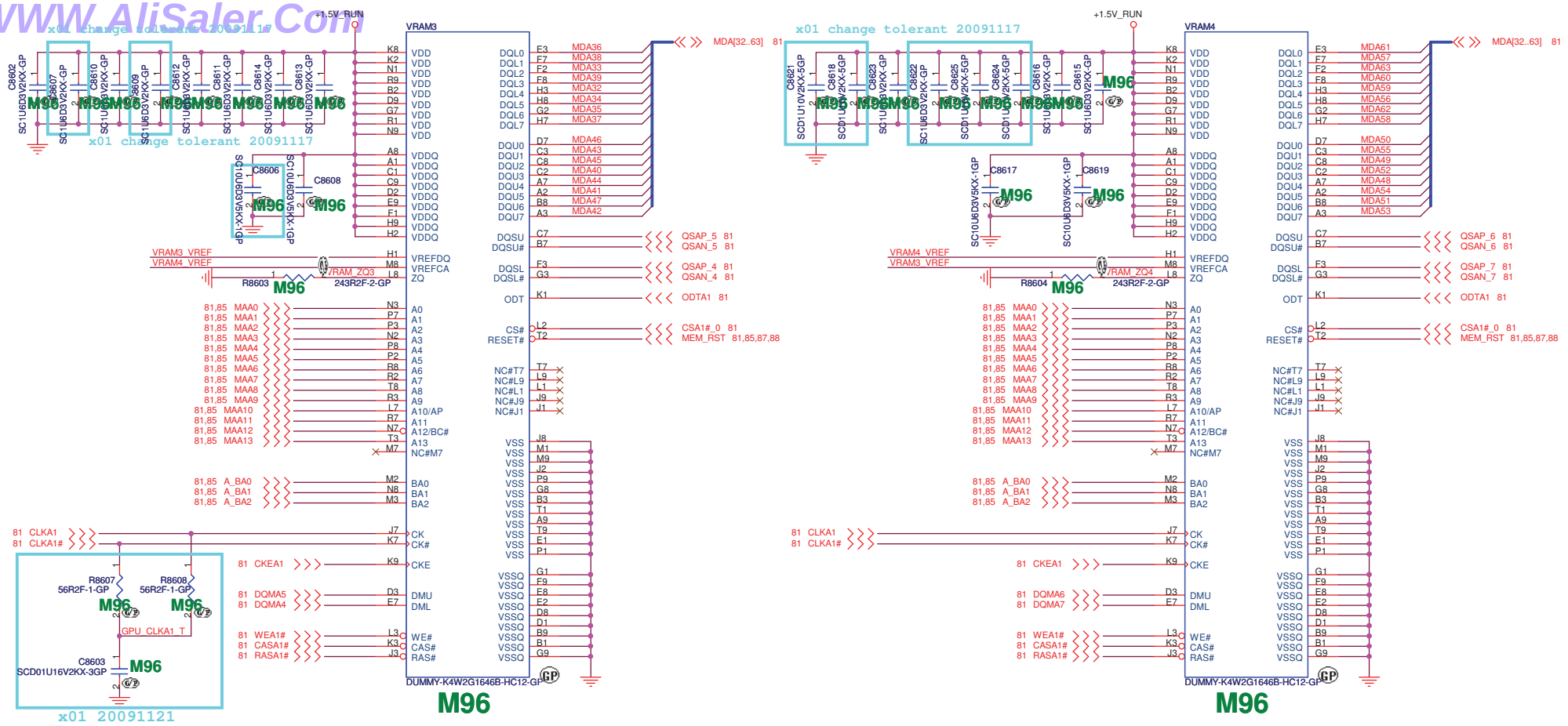

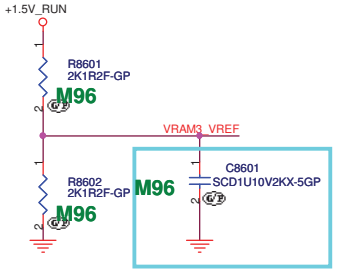

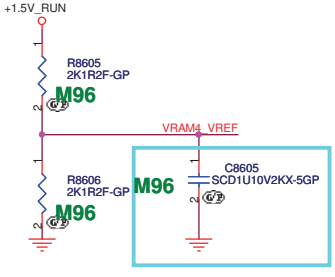

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Berry | Rev: A00

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x01 change tolerant 20091117

+1.5V_RUN

VRAM5

C8702 SC1U6D3V2KX-GP
C8707 SCD1U10V2KX-5GP
C8710 SC1U6D3V2KX-GP
C8709 SCD1U10V2KX-5GP
C87011 SC1U6D3V2KX-GP
C87012 SC1U6D3V2KX-GP
C87013 SC1U6D3V2KX-GP
C8714 SC1U6D3V2KX-GP
C8706 SC10U6D3V5KX-1GP
C8708 SC10U6D3V5KX-1GP

VDD: K8 K2 N1 R9 B2 D9 G7 R1 N9
VDDQ: A8 A1 C1 C9 D2 E9 F1 H9 H2

DQL0 E3 MDB14
DQL1 F7 MDB13
DQL2 F2 MDB12
DQL3 F8 MDB15
DQL4 H3 MDB11
DQL5 H8 MDB8
DQL6 G2 MDB9
DQL7 H7 MDB10
DQU0 D7 MDB26
DQU1 C3 MDB27
DQU2 C8 MDB30
DQU3 C2 MDB24
DQU4 A7 MDB31
DQU5 A2 MDB25
DQU6 B8 MDB29
DQU7 A3 MDB28

MDB[0..31] 81

DQSU C7 QSBP_3 81
DQSU# B7 QSBN_3 81
DQSL F3 QSBP_1 81
DQSL# G3 QSBN_1 81
ODT K1 ODTB0 81
CS# L2 CSB0#_0 81
RESET# T2 MEM_RST 81,85,86,88

VRAM5_VREF
VRAM6_VREF
R8704 DIS
VRAM_ZQ5 243R2F-2-GP

VREFDQ H1
VREFCA M8
ZQ L8

81,88 MAB0 N3 A0
81,88 MAB1 P7 A1
81,88 MAB2 P3 A2
81,88 MAB3 N2 A3
81,88 MAB4 P8 A4
81,88 MAB5 P2 A5
81,88 MAB6 R8 A6
81,88 MAB7 R2 A7
81,88 MAB8 T8 A8
81,88 MAB9 R3 A9
81,88 MAB10 L7 A10/AP
81,88 MAB11 R7 A11
81,88 MAB12 N7 A12/BC#
81,88 MAB13 T3 A13
NC#M7 M7

81,88 B_BA0 M2 BA0
81,88 B_BA1 N8 BA1
81,88 B_BA2 M3 BA2

NC#T7 T7
NC#L9 L9
NC#L1 L1
NC#J9 J9
NC#J1 J1

VSS: J8 M1 M9 J2 P9 G8 B3 T1 A9 T9 E1 P1
VSSQ: G1 F9 E8 E2 D8 D1 B9 B1 G9

20090902

81 CLKB0 J7 CK
81 CLKB0# K7 CK#
81 CKEB0 K9 CKE

R8707 56R2F-1-GP DIS
R8708 56R2F-1-GP DIS
GPU_CLKB0_T
C8703 SCD01U16V2KX-3GP DIS

81 DQMB3 D3 DMU
81 DQMB1 E7 DML
81 WEB0# L3 WE#
81 CASB0# K3 CAS#
81 RASB0# J3 RAS#

DUMMY-K4W2G1646B-HC12-GP

x01 20091121

DIS

x01 change tolerant 20091117

+1.5V_RUN

VRAM6

C8717 SC1U6D3V2KX-GP
C8715 SC1U6D3V2KX-GP
C8720 SC1U6D3V2KX-GP
C8723 SC1U6D3V2KX-GP
C8721 SCD1U10V2KX-5GP
C8722 SC1U6D3V2KX-GP
C8724 SC1U6D3V2KX-GP
C8725 SCD1U10V2KX-5GP
C8718 SC10U6D3V5KX-1GP
C8719 SC10U6D3V5KX-1GP

DY

VDD: K8 K2 N1 R9 B2 D9 G7 R1 N9
VDDQ: A8 A1 C1 C9 D2 E9 F1 H9 H2

DQL0 E3 MDB16
DQL1 F7 MDB18
DQL2 F2 MDB20
DQL3 F8 MDB19
DQL4 H3 MDB22
DQL5 H8 MDB17
DQL6 G2 MDB23
DQL7 H7 MDB21
DQU0 D7 MDB1
DQU1 C3 MDB5
DQU2 C8 MDB2
DQU3 C2 MDB4
DQU4 A7 MDB3
DQU5 A2 MDB7
DQU6 B8 MDB0
DQU7 A3 MDB6

MDB[0..31] 81

DQSU C7 QSBP_0 81
DQSU# B7 QSBN_0 81
DQSL F3 QSBP_2 81
DQSL# G3 QSBN_2 81
ODT K1 ODTB0 81
CS# L2 CSB0#_0 81
RESET# T2 MEM_RST 81,85,86,88

VRAM6_VREF
VRAM5_VREF
R8706 DIS
VRAM_ZQ6 243R2F-2-GP

VREFDQ H1
VREFCA M8
ZQ L8

81,88 MAB0 N3 A0
81,88 MAB1 P7 A1
81,88 MAB2 P3 A2
81,88 MAB3 N2 A3
81,88 MAB4 P8 A4
81,88 MAB5 P2 A5
81,88 MAB6 R8 A6
81,88 MAB7 R2 A7
81,88 MAB8 T8 A8
81,88 MAB9 R3 A9
81,88 MAB10 L7 A10/AP
81,88 MAB11 R7 A11
81,88 MAB12 N7 A12/BC#
81,88 MAB13 T3 A13
NC#M7 M7

81,88 B_BA0 M2 BA0
81,88 B_BA1 N8 BA1
81,88 B_BA2 M3 BA2

NC#T7 T7
NC#L9 L9
NC#L1 L1
NC#J9 J9
NC#J1 J1

VSS: J8 M1 M9 J2 P9 G8 B3 T1 A9 T9 E1 P1
VSSQ: G1 F9 E8 E2 D8 D1 B9 B1 G9

81 CLKB0 J7 CK
81 CLKB0# K7 CK#
81 CKEB0 K9 CKE

81 DQMB0 D3 DMU
81 DQMB2 E7 DML
81 WEB0# L3 WE#
81 CASB0# K3 CAS#
81 RASB0# J3 RAS#

DUMMY-K4W2G1646B-HC12-GP

DIS

+1.5V_RUN

R8701 2K1R2F-GP DIS
VRAM5_VREF
R8702 2K1R2F-GP DIS
C8701 SCD1U10V2KX-5GP DIS

x01 change tolerant 20091117

+1.5V_RUN

R8703 2K1R2F-GP DIS
VRAM6_VREF
R8705 2K1R2F-GP DIS
C8705 SCD1U10V2KX-5GP DIS

x01 change tolerant 20091117

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)
Size: A3
Document Number: Berry
Rev: A00
Date: Monday, March 29, 2010
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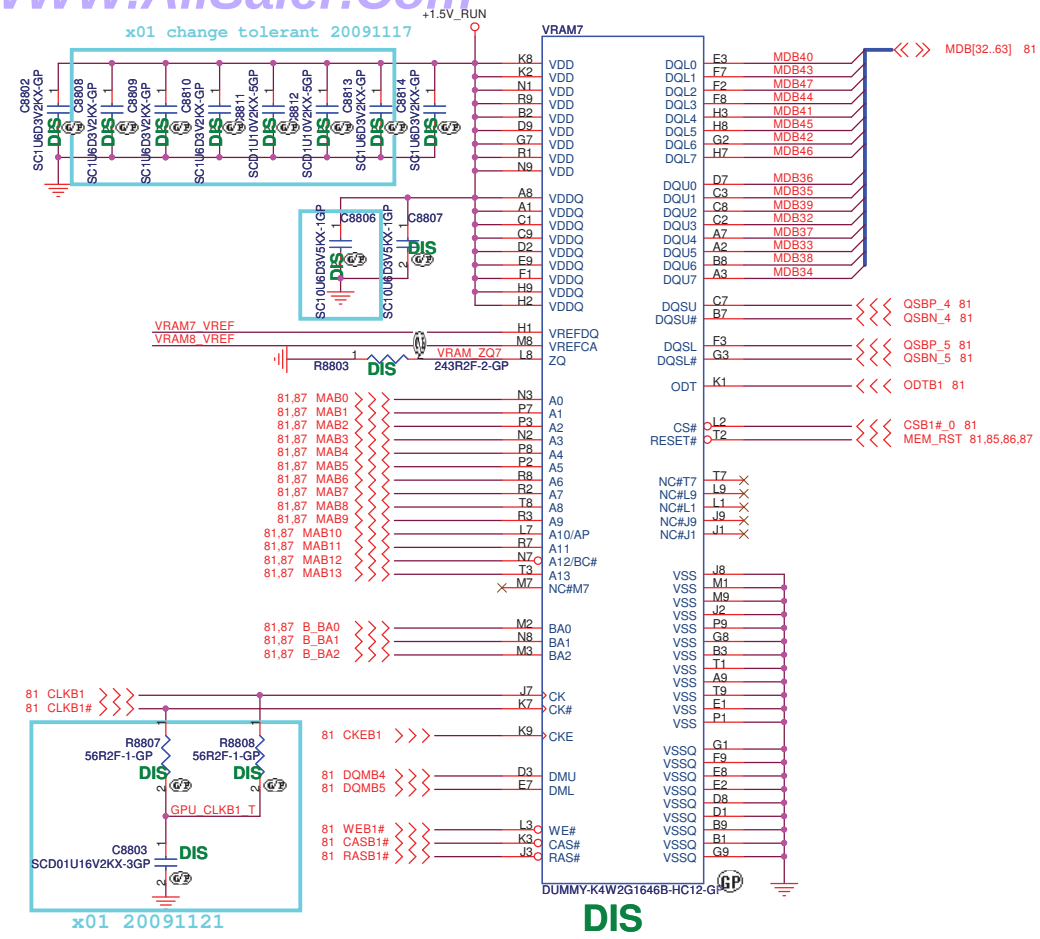

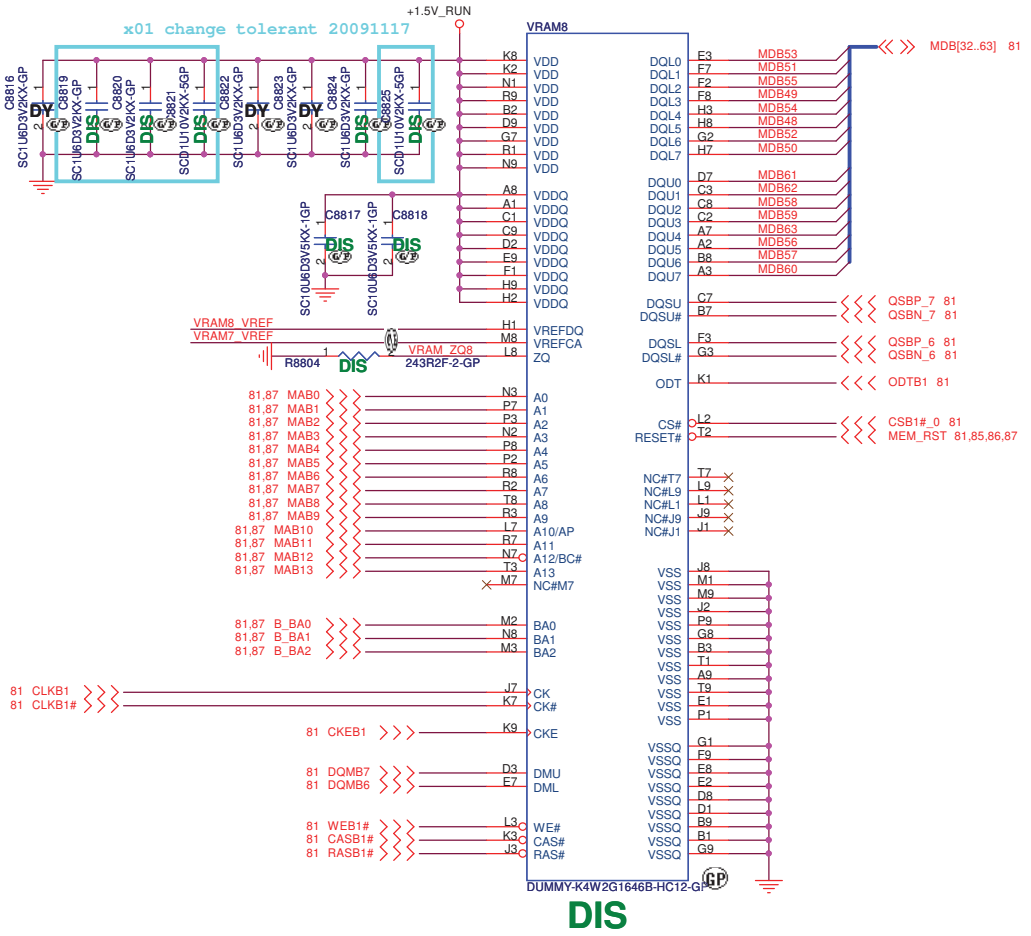

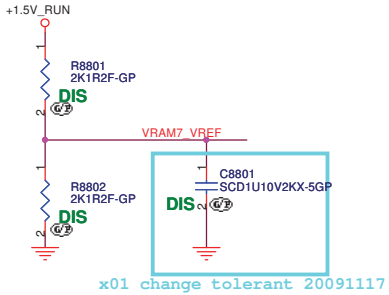

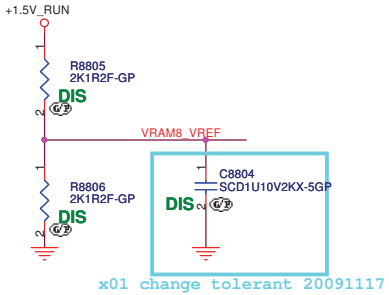

<Core Design>

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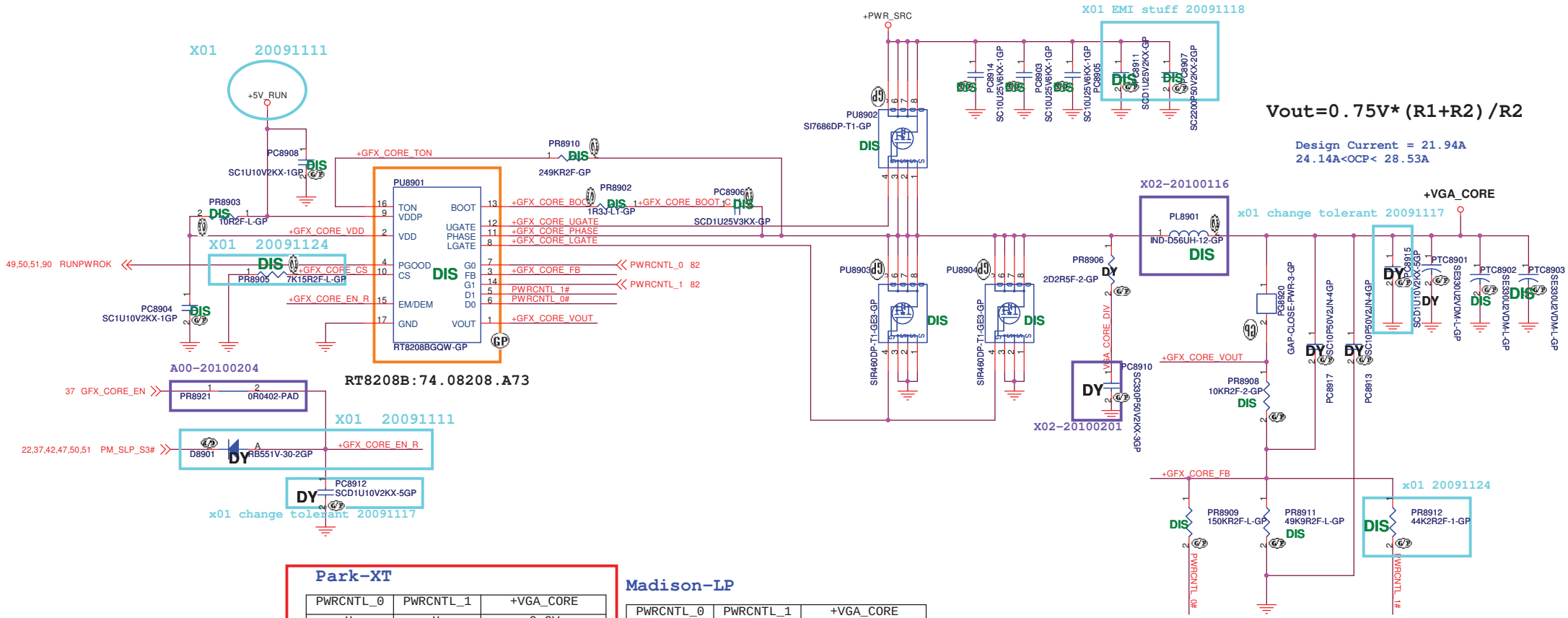
SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

Park-XT

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

Madison-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.12V

M96-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.0V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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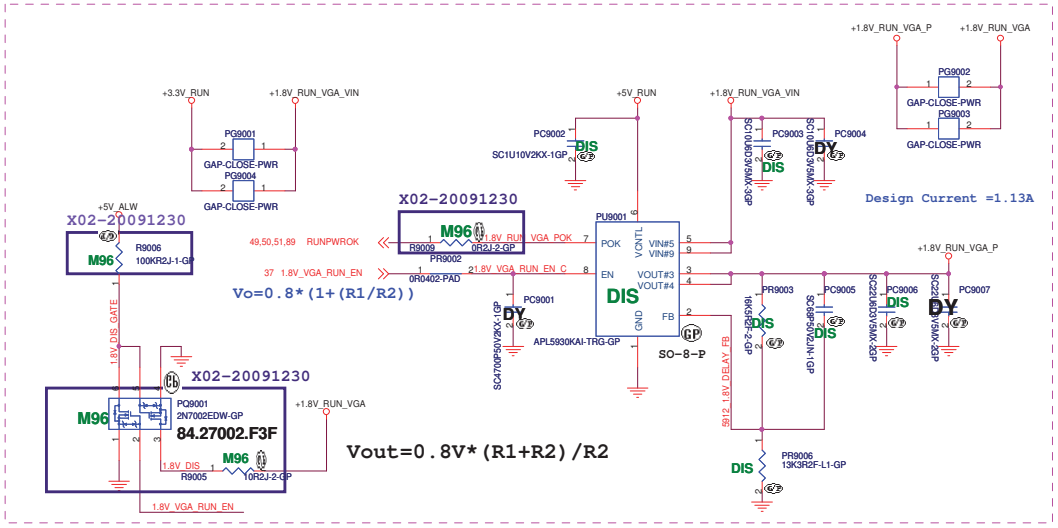
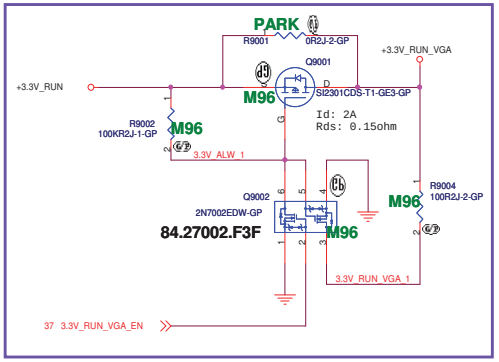
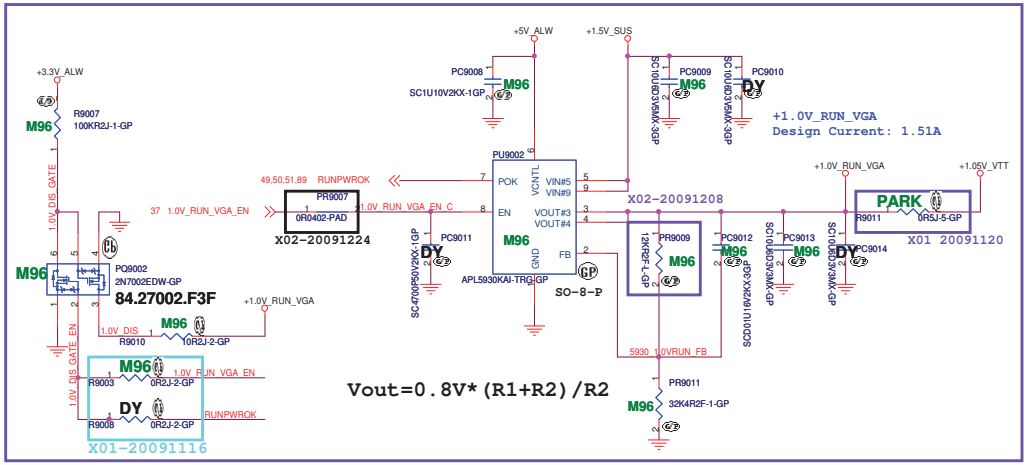
APL5930 for +1.8V_RUN_VGA



+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA



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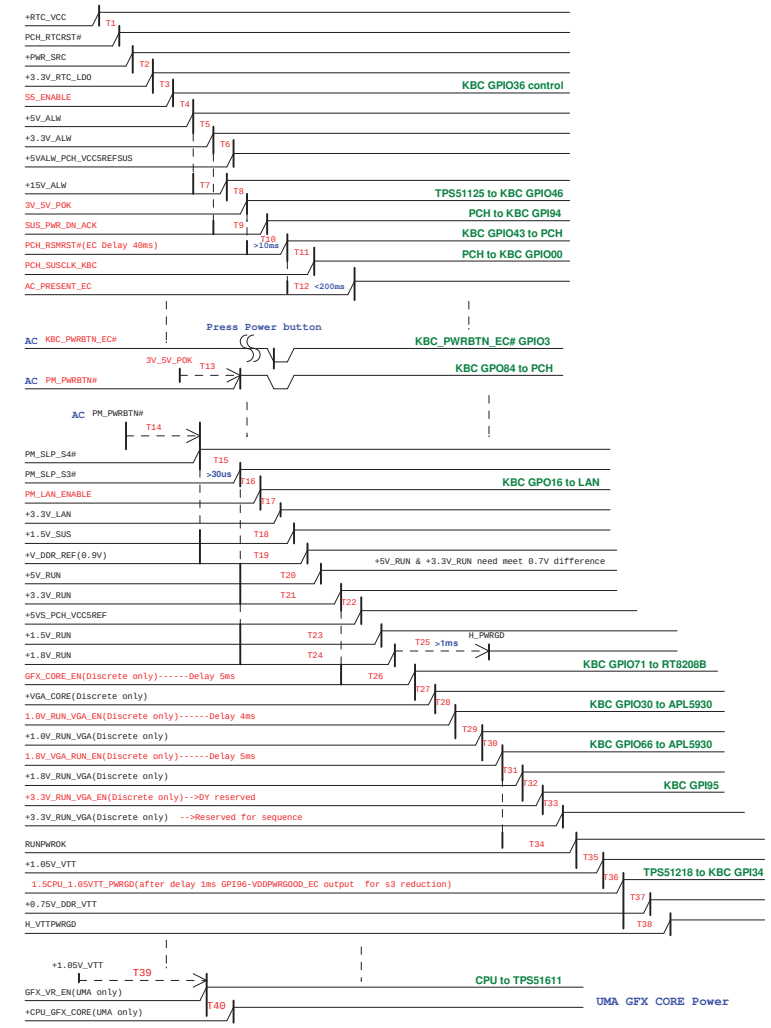
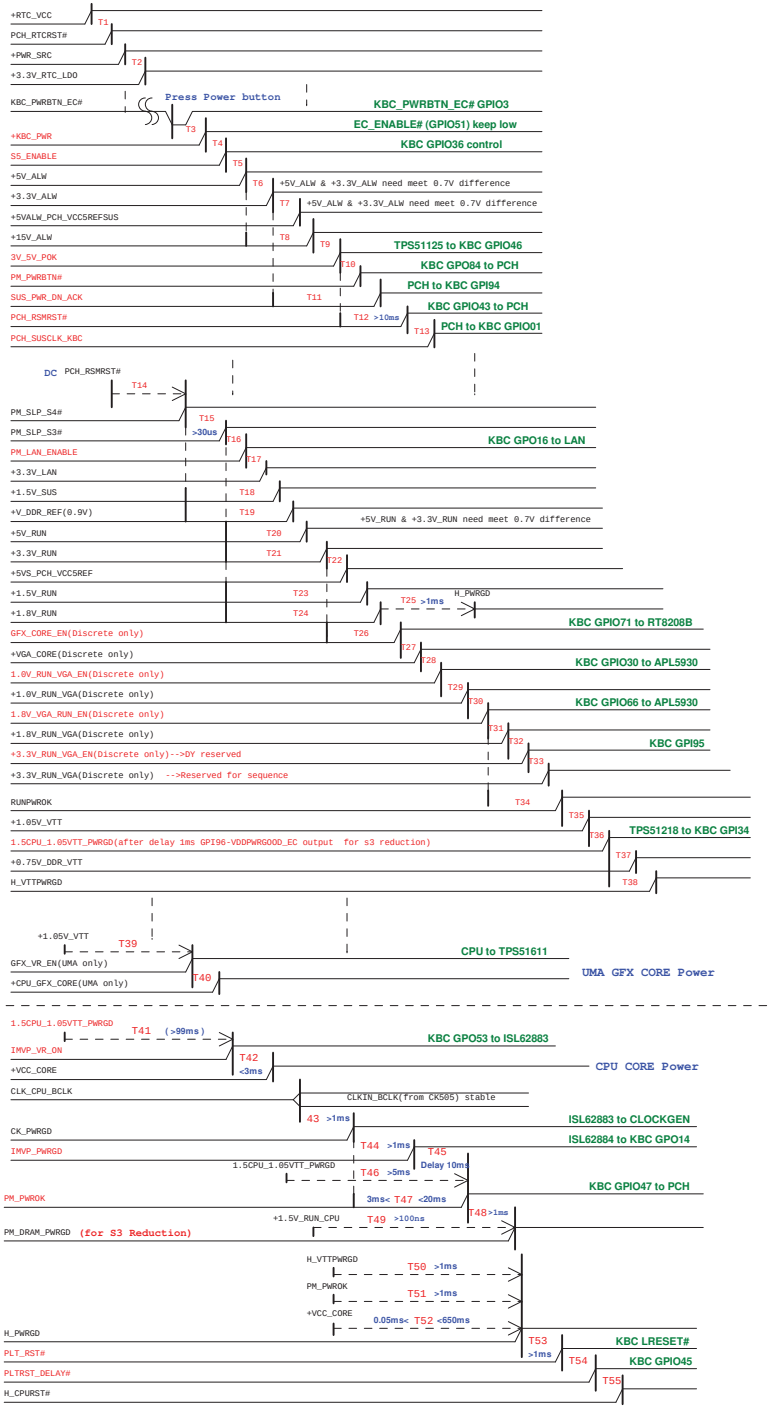
D15 Intel-Power Up Sequence

(AC mode)

red word: KBC GPIO



(DC mode)



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Title: Power Sequence

Size: A1 | Document Number: | Rev: A00

Date: Tuesday, March 02, 2010 | Sheet 91 of 96

<Core Design>

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Title

Change History

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