Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2010-02-24

REV : X01

```
DY :None Installed
UMA:UMA platform installed
PARK:DIS PARK platform installed
M96:DIS M96 platform installed
VRAM_1G:VRAM 128M*16 installed
Colay :Manual modify BOM
```

<Core Design>

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Title		
	Cover Page	
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Berry Block Diagram (Discrete/UMA co-lay)

##OnMainBoard

M96 LP; 1GB (64Mx16b*8)
VRAM Hynix 64M
Wistronl P/N:72.51G63.C0U
VRAM Samsung 64M
Dell P/N:9TGTN$AA
Wistronl P/N:72.41164.H0U

VRAM 1GB 85,86,87,88
DDR3 600MHz
AMD Graphic M96-LP (Discrete only) 80,81,82,83,84
PCIe x 16 (Discrete only)
Clock Generator SLG8SP585 7
Intel CPU Arrandale 8,9,10,11,12,13,14
DDRIII 800/1066 Channel A
DDRIII 800/1066 Channel B
DDRIII 800/1066 Slot 0 18
DDRIII 800/1066 Slot 1 19
FDIx4x2 (UMA only)
DMIx4
Discreet/UMA Co-lay
HDMI 57
LCD 54
HDMI Level shifter 57
LVDS(Dual Channel)
RGB CRT
Intel PCH HM57
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28
CRT
Left Side: USB x 2
CRT Board 77
Bluetooth 73
CAMERA 54
USB2.0 x 4
AZALIA
Internal Analog MIC
HP1
MIC IN
2CH SPEAKER
Azalia CODEC IDT 92HD79B1 30
SPI
Flash ROM 4MB 62
LPC Bus
LPC debug port 70
KBC NUVOTON NPCE781BA0DX 37
SPI
SMBus
Flash ROM 256kB 62
Touch PAD
Int. KB
Thermal Main:G7922 Sec.EMC2102
Fan 58
PCIE x 3
SATA x 1
USB 2.0 x 4
USB 2.0 x 1
SATA x 2
I/O Board Connector 76
PCIE x 1 USB x 1
PCIE x 1
Mini-Card 802.11a/b/g
10/100 NIC Realtek RTL8103T-VB
RJ45 CONN
SATAx1 / USB2.0x1
ESATA/USB Combo
PCIE x 1,USB x 1
Mini-Card WWAN
SIM
USB 2.0 x 1
Right Side: USB x 1
CardReader Realtek RTS5159 78
SD/MMC+/MS/ MS Pro/xD
HDD 59
ODD 59

Project code : 91.4HH01.001
PCB P/N :
Revision :

CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC TPS51611 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFX_CORE

VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE

TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA

SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS	+1.0V_RUN_VGA

Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

PCB LAYER

L1:Top
L2:VCC
L3:Signal
L4:Signal
L5:GND
L6:Bottom

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Title: Block Diagram
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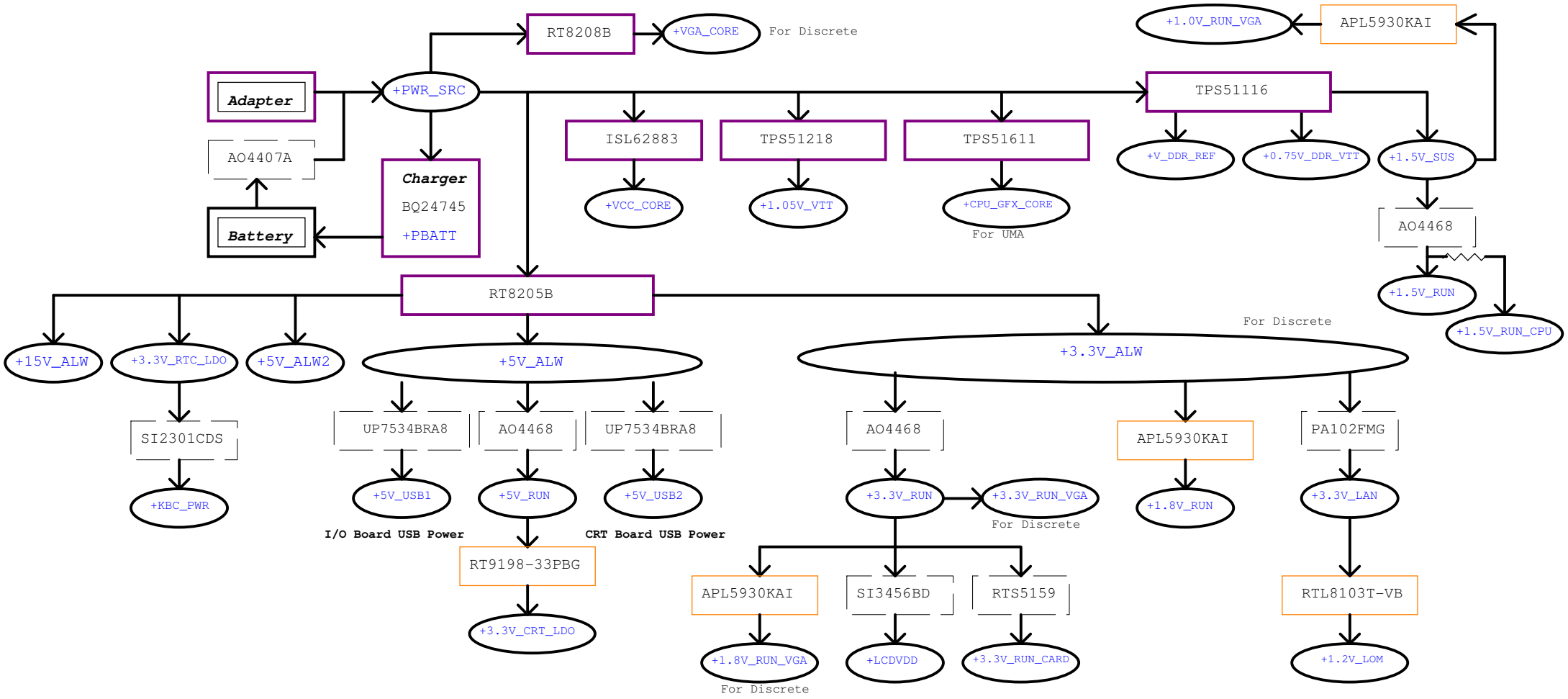

Power Shape

Regulator	LDO	Switch

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Title: **Power Block Diagram**

Size	Document Number	Rev
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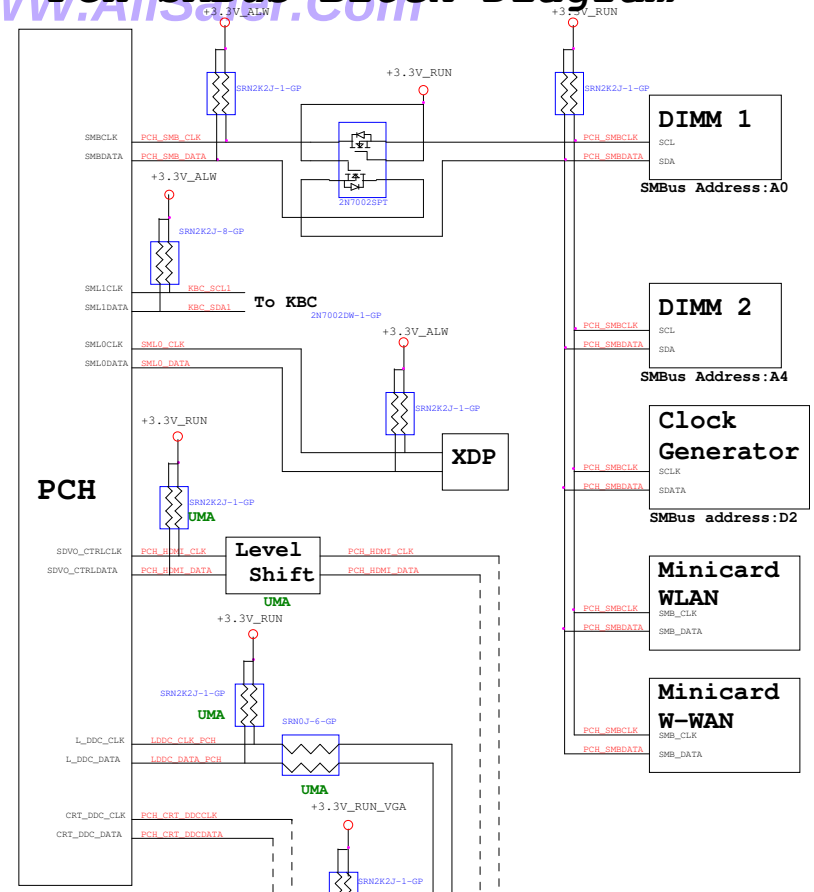
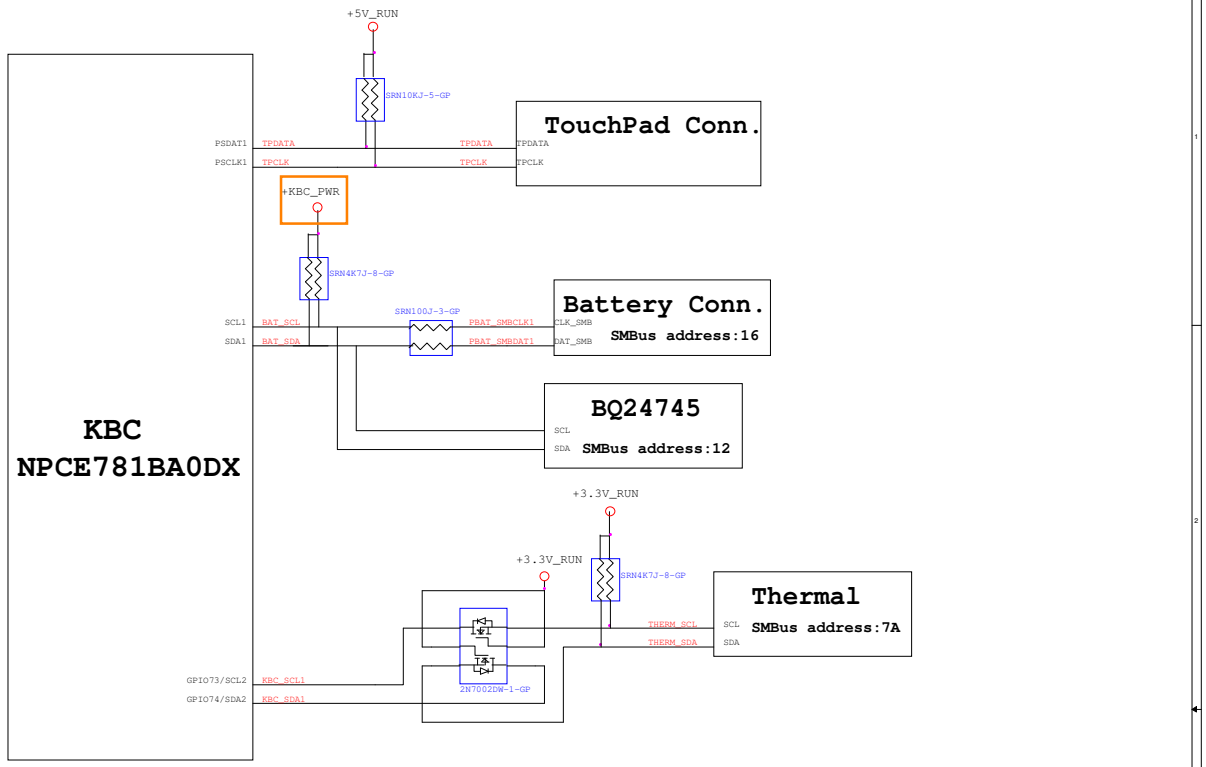
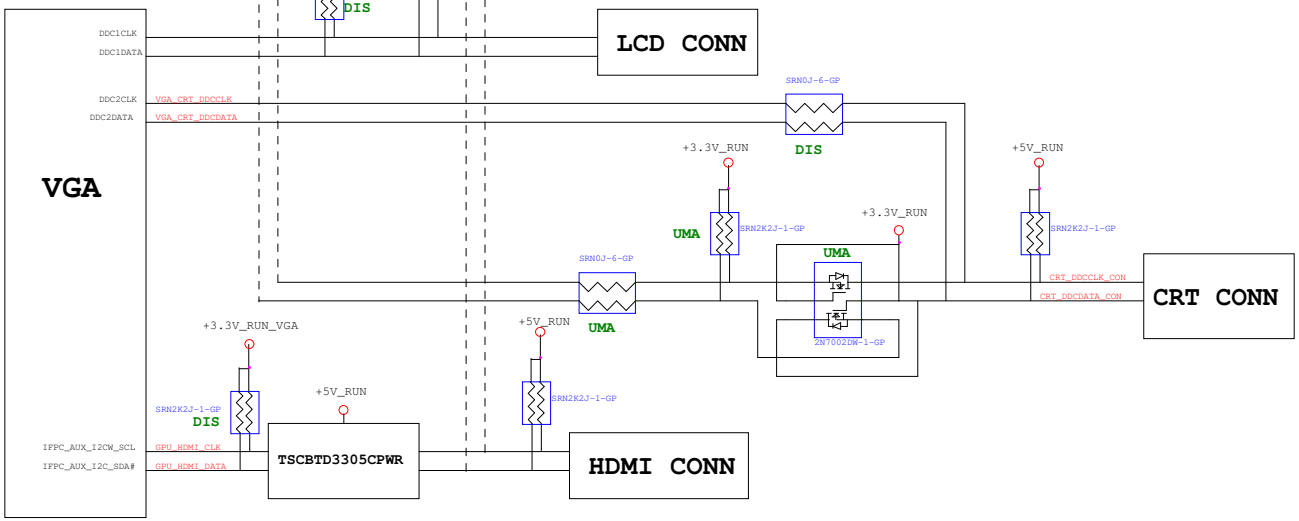
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram

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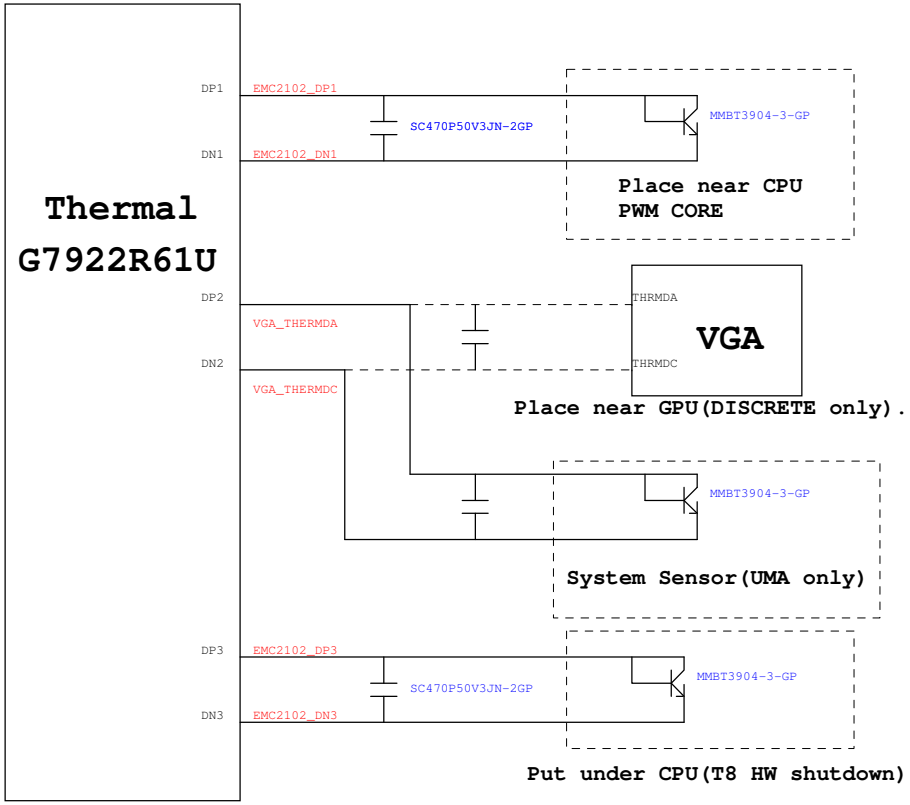
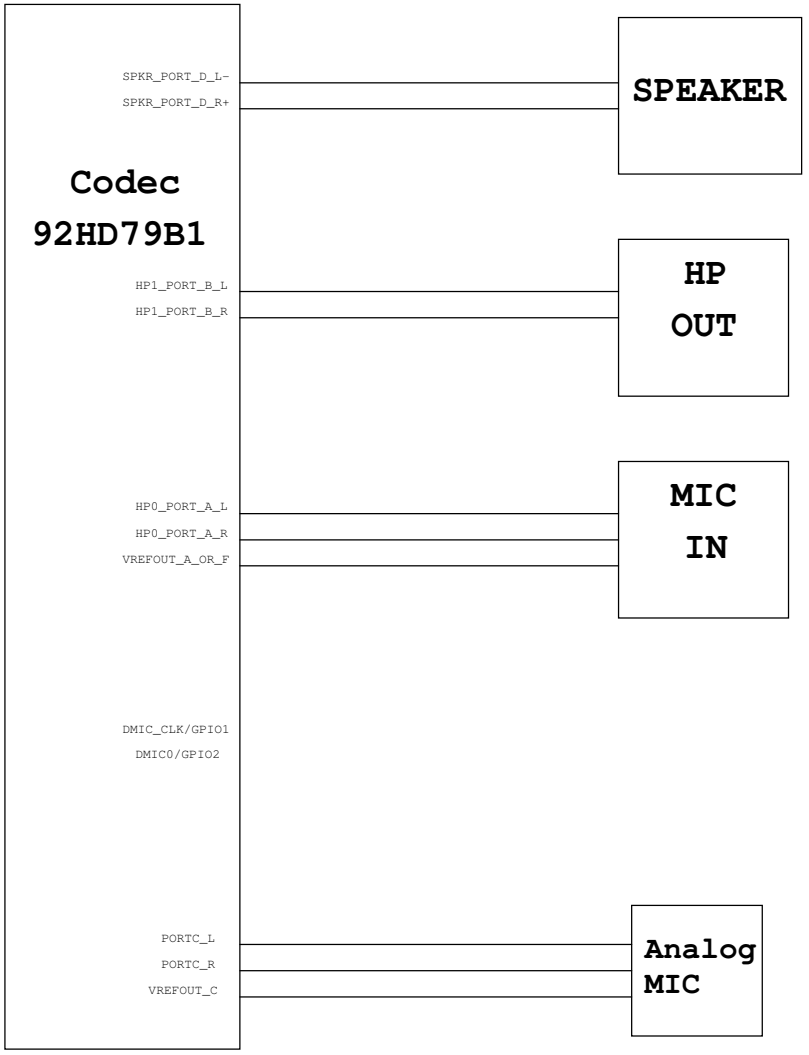
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Berry | Rev: X01

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PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

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Title: Table of Content

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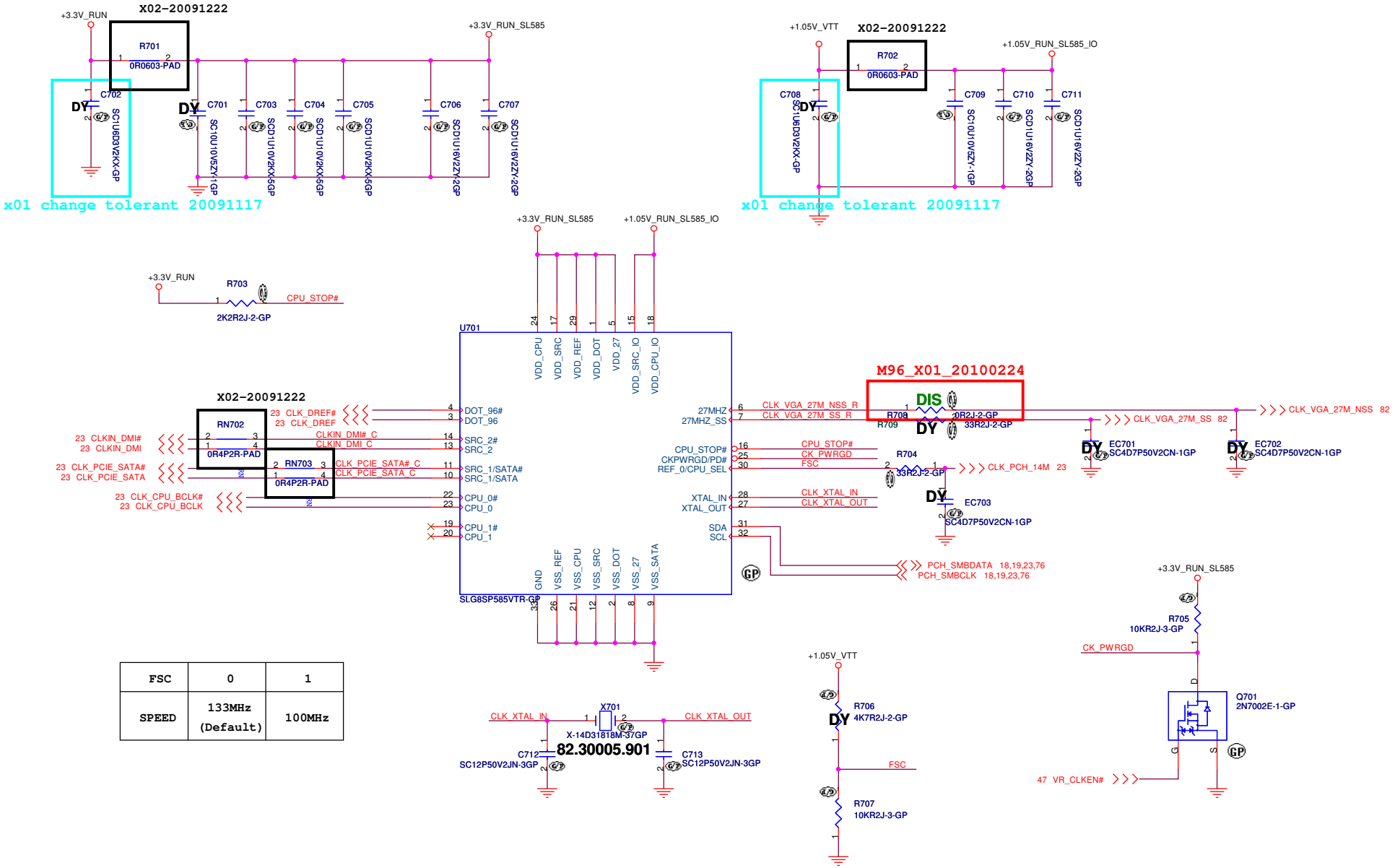
SSID = CLOCK



FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: Clock Generator SLG8SP585

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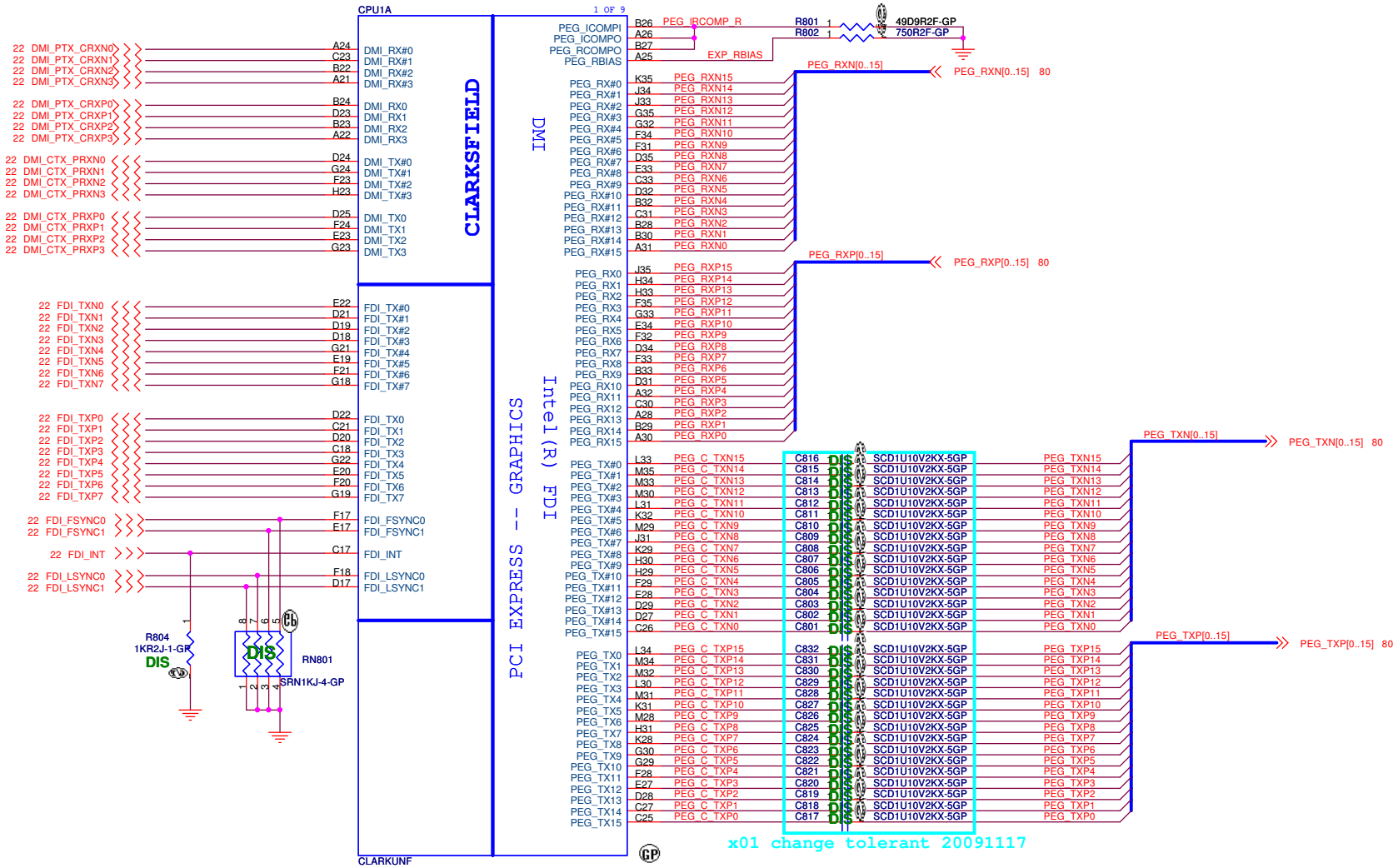
SSID = CPU



62.10055.341

SEC. 62.10053.561

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Title: CPU (PCIE/DMI/FDI)

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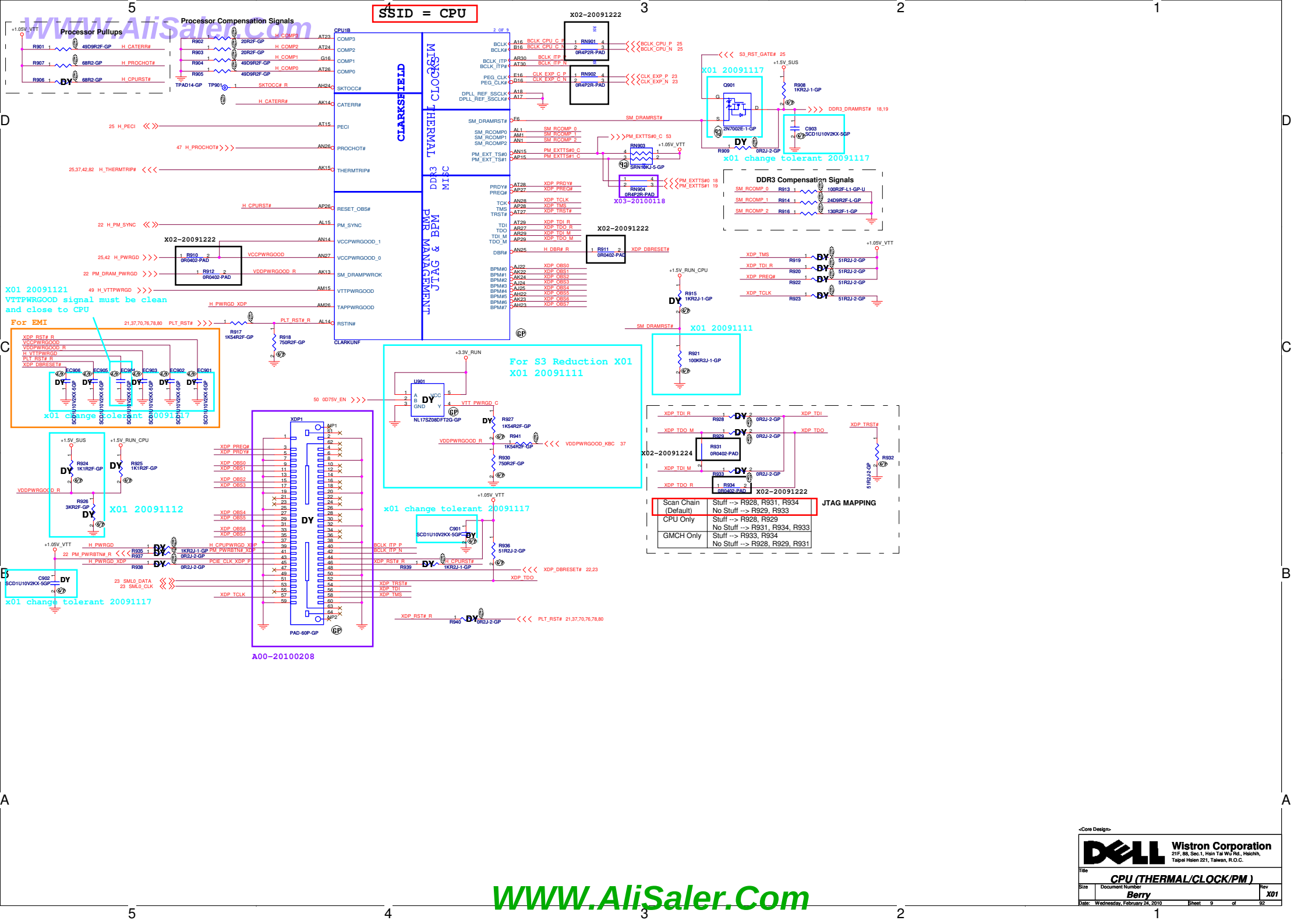
SSID = CPU
Processor Compensation Signals
Processor Pullups
CLARKSFIELD
CLARKUNF
MISC CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
X02-20091222
X02-20091224
X01 20091121
VTTPWRGOOD signal must be clean and close to CPU
For EMI
For S3 Reduction X01 X01 20091111
X01 20091112
X01 20091111
X01 20091117
x01 change tolerant 20091117
DDR3 Compensation Signals
JTAG MAPPING
Scan Chain (Default) Stuff --> R928, R931, R934 No Stuff --> R929, R933
CPU Only Stuff --> R928, R929 No Stuff --> R931, R934, R933
GMCH Only Stuff --> R933, R934 No Stuff --> R928, R929, R931
A00-20100208
WWW.AliSaler.Com
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CPU (THERMAL/CLOCK/PM)
Berry
X01
Wednesday, February 24, 2010
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SSID = CPU

CPU1C

3 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY A

CLARKUNF

CPU1D

4 OF 9

CLARKSFIELD

DDR SYSTEM MEMORY - B

CLARKUNF

<Core Design>

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Title	CPU (DDR)
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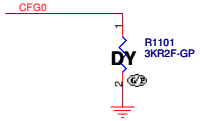
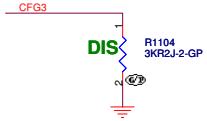
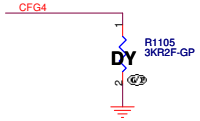
SSID = CPU



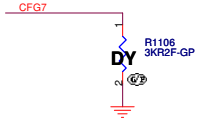
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



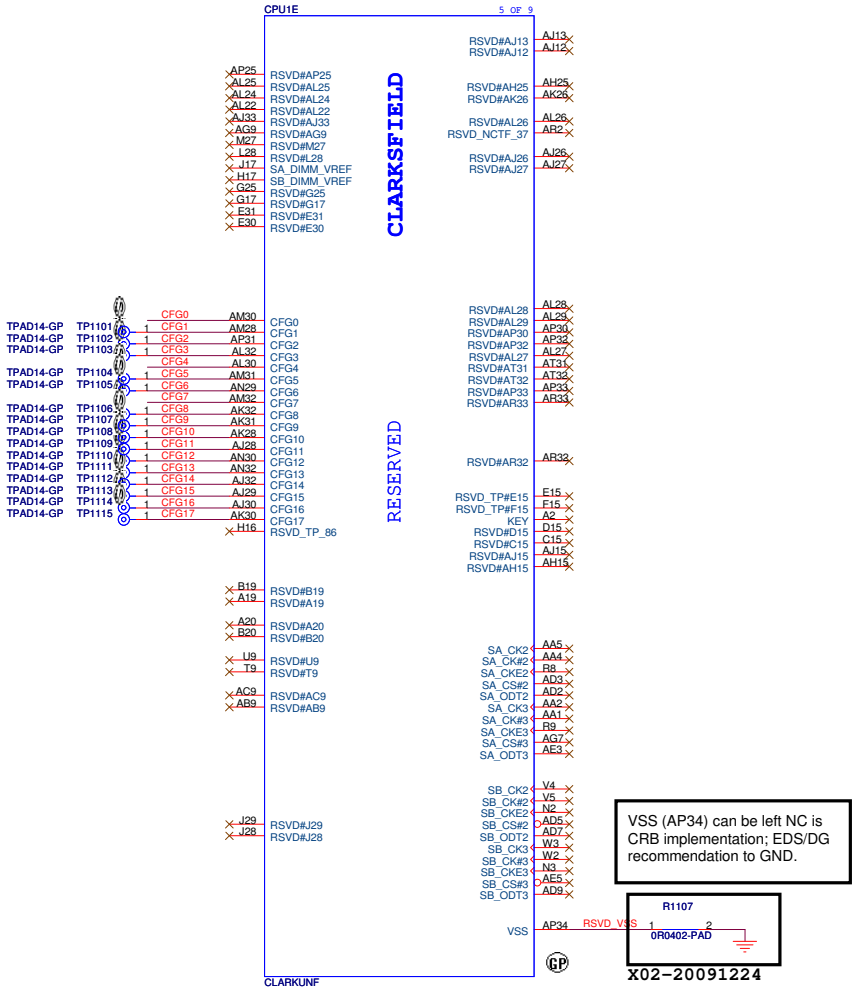
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

X02-20091224

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Title	CPU (RESERVED)	
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SSID = CPU

PROCESSOR CORE POWER

48A

CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

CLARKUNF

+VCC_CORE

x01 change tolerant 20091117

+1.05V_VTT

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

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Title: CPU (VCC_CORE)

Size | Document Number: Berry | Rev: X01

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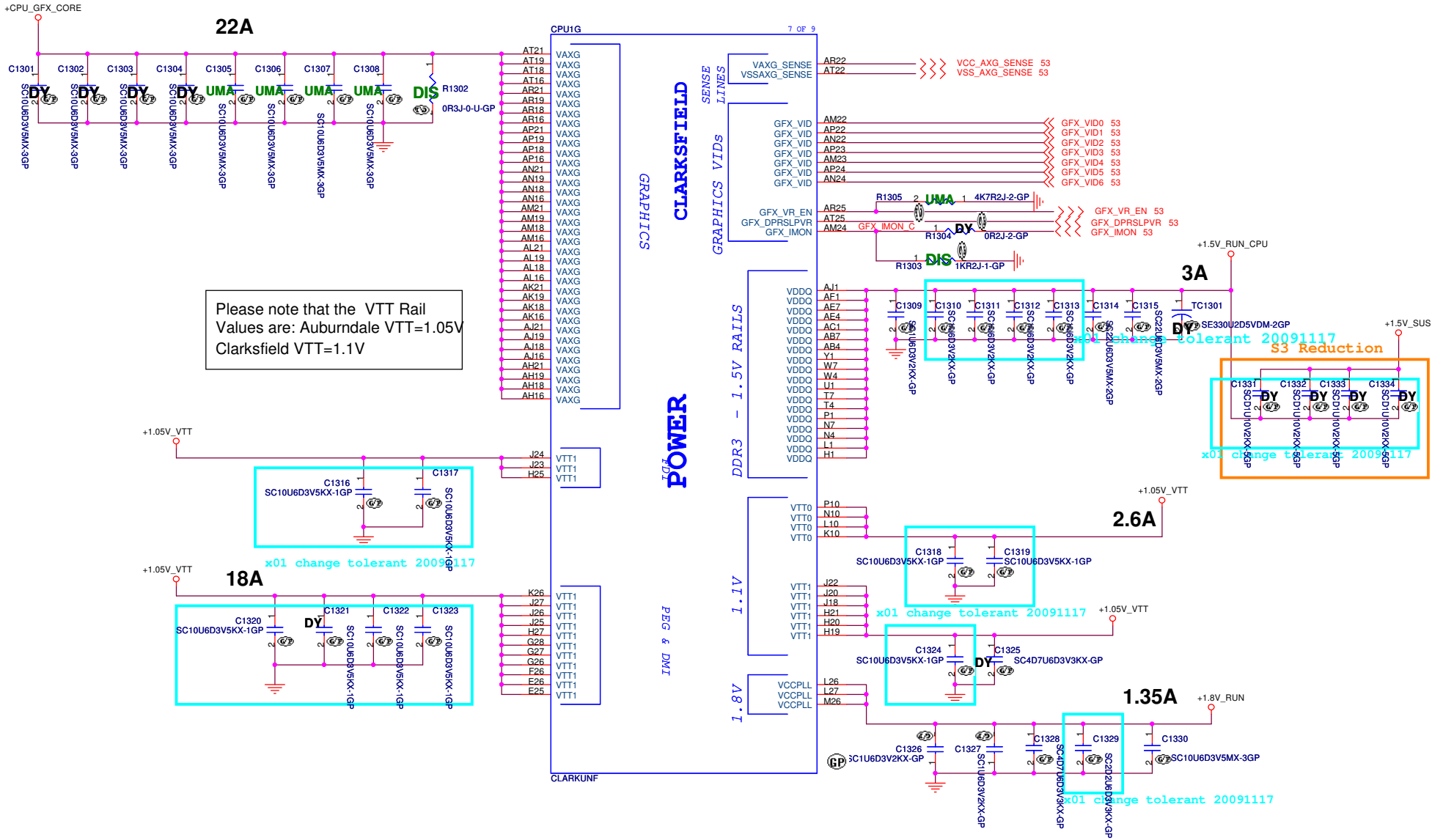
SSID = CPU



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Title: CPU (VCC_GFXCORE)

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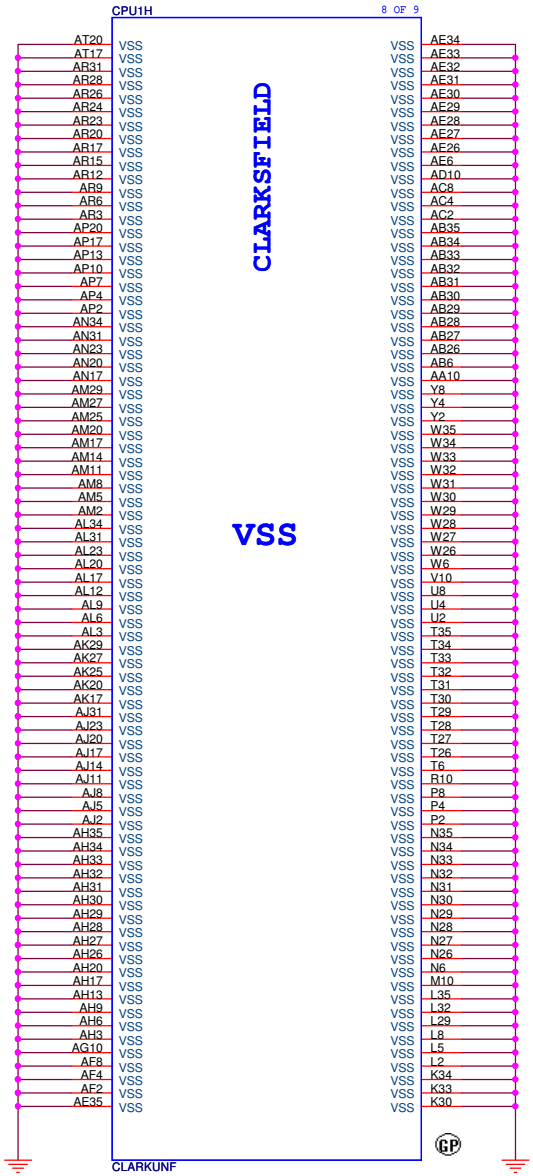
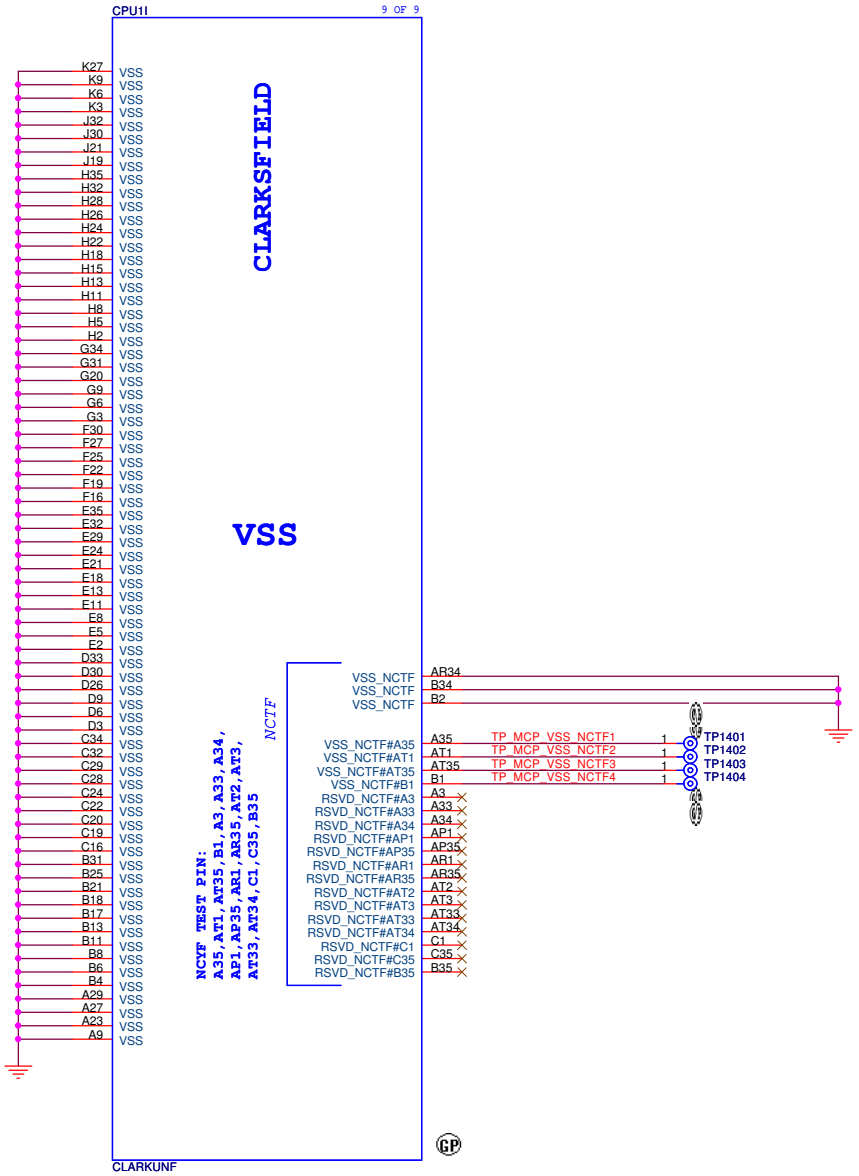
SSID = CPU





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Title: CPU (VSS)

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Title: Reserved

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Title: Reserved

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Title: Reserved

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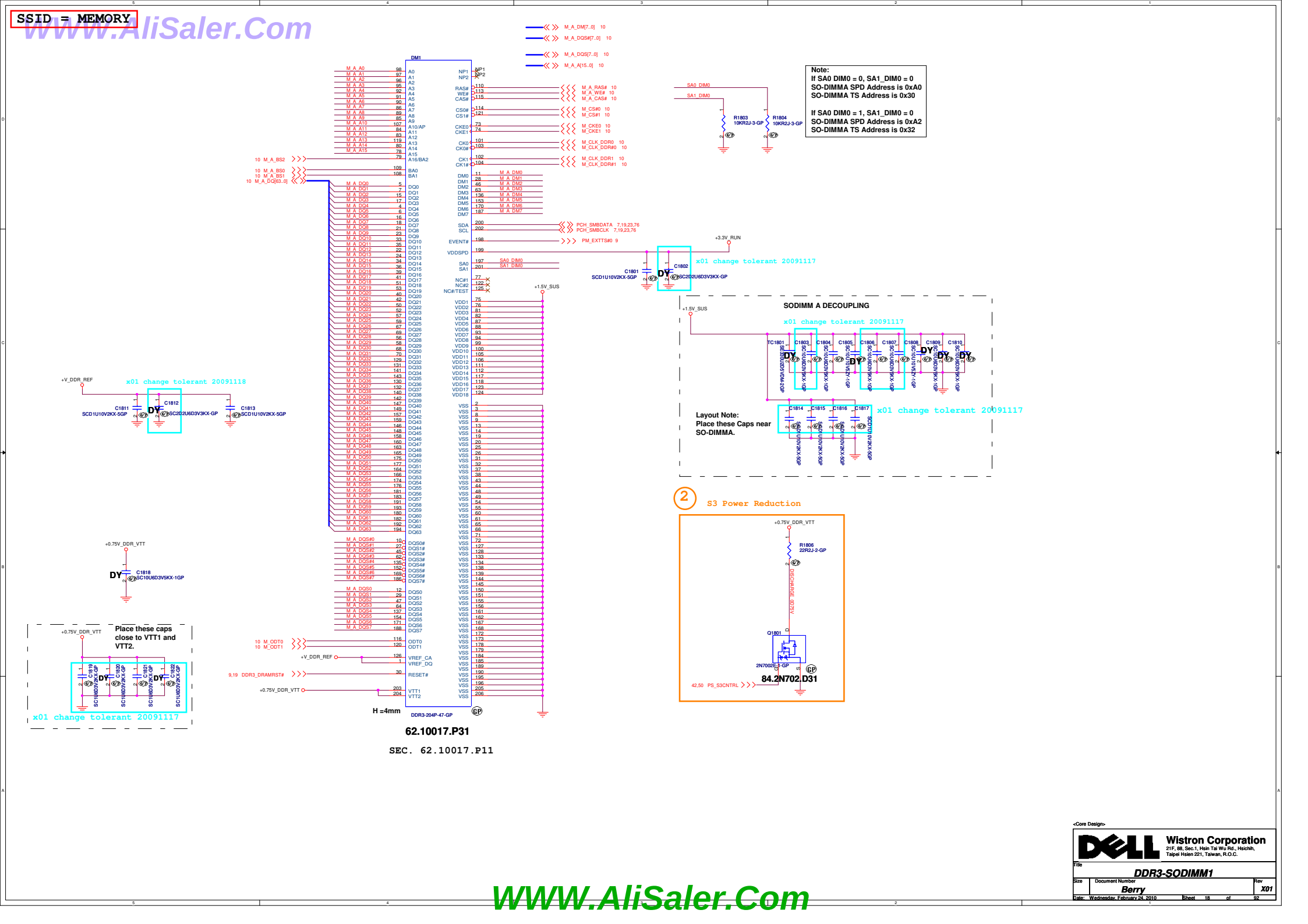
SSID = MEMORY



62.10017.P31

SEC. 62.10017.P11

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Title: DDR3-SODIMM1

Size | Document Number: Berry | Rev: X01

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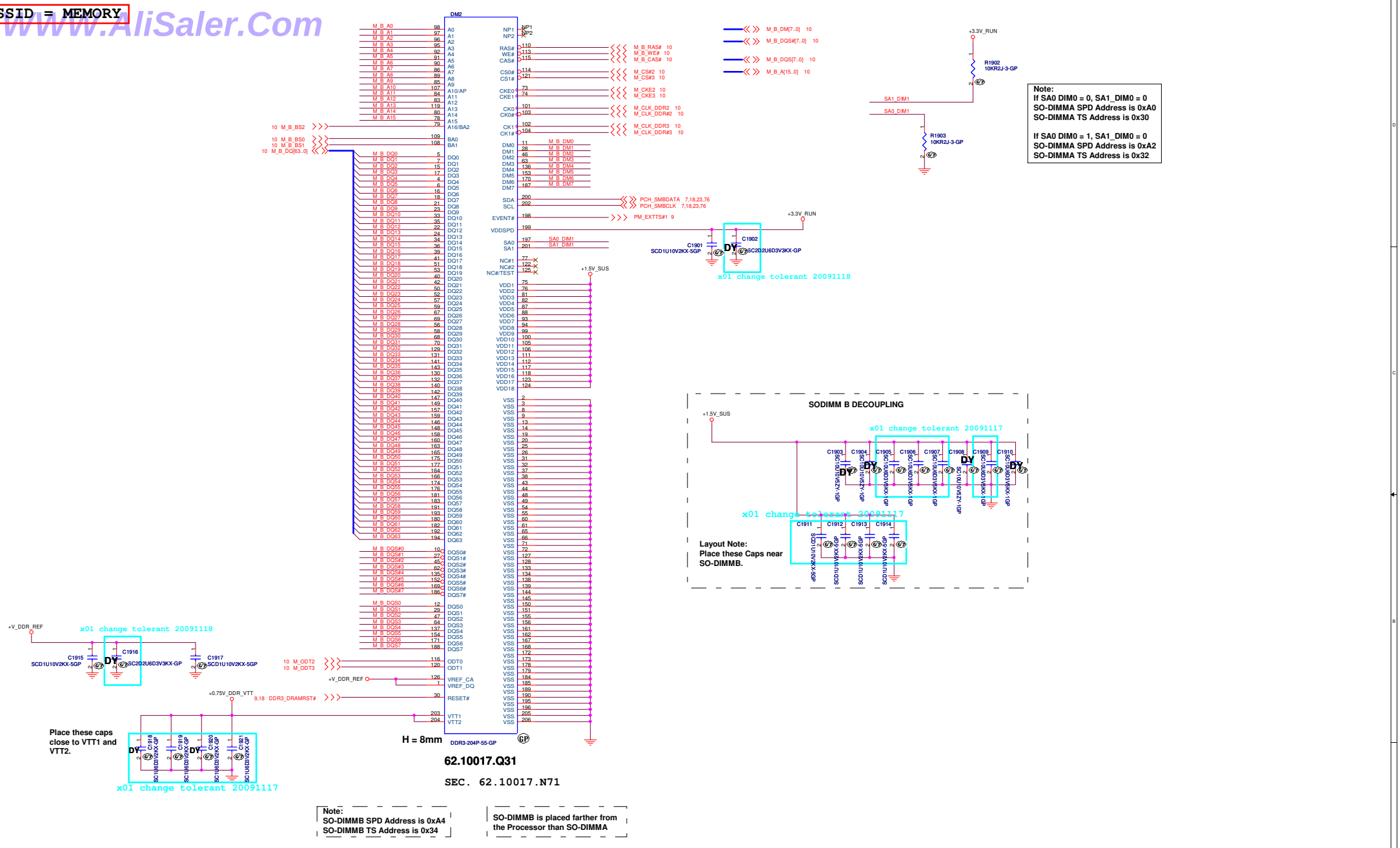
SSID = MEMORY



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Title: DDR3-SODIMM2

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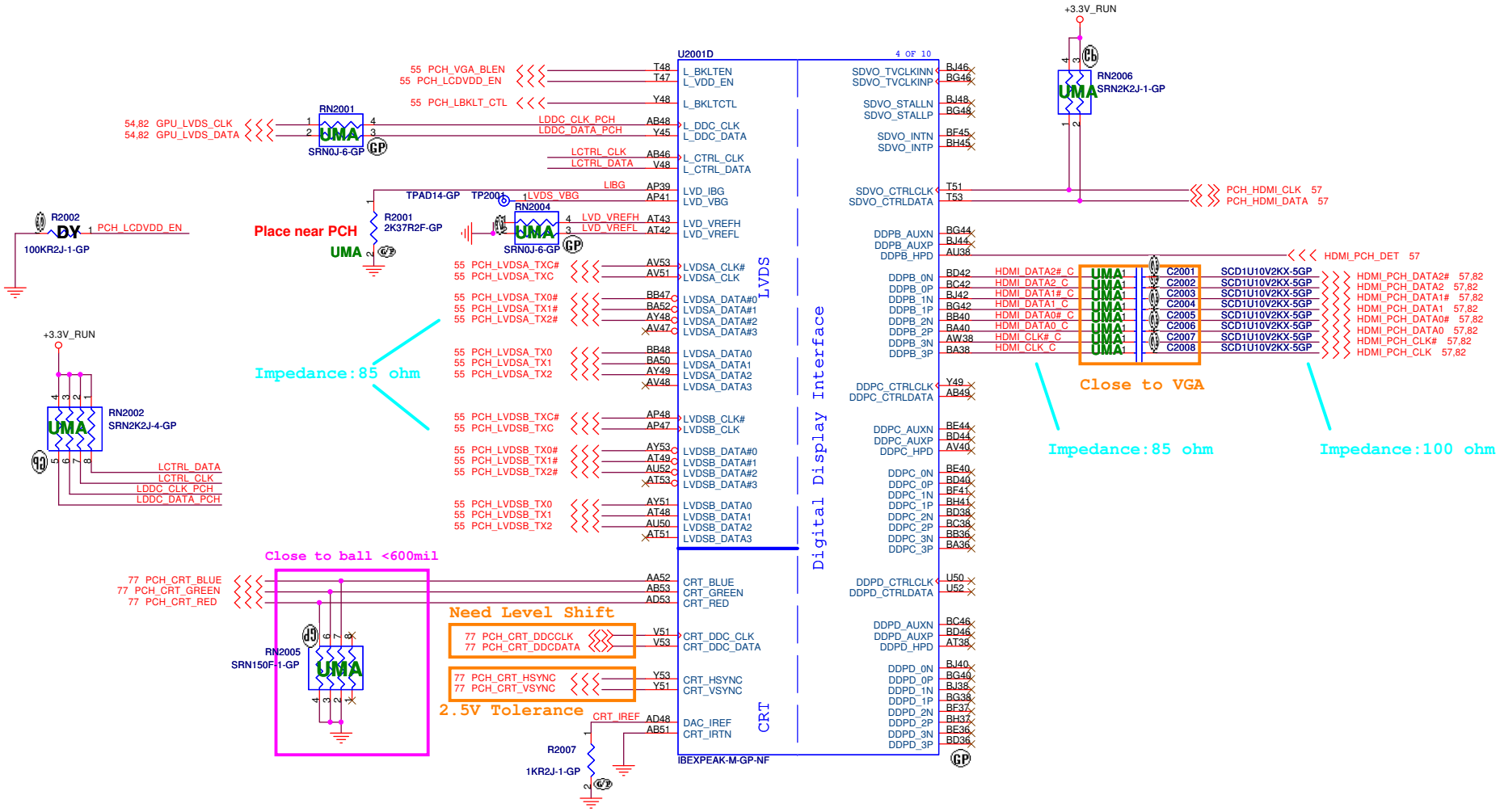

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Title: PCH (LVDS/CRT/DDI)

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SSID = PCH

RN2101 SRN8K2J-2-GP-U
PCI_TRDY# 1 10 +3.3V_RUN
PCI_DEVSEL# 2 9 PCI_FRAME#
INT_PIRQA# 3 8 PCI_REQ2#
PCI_IRDY# 4 7 INT_PIRQD#
+3.3V_RUN 5 6 PCI_SERR#

RN2103 SRN8K2J-2-GP-U
INT_PIRQH# 1 10 +3.3V_RUN
INT_PIRQB# 2 9 PCI_REQ1#
INT_PIRQF# 3 8 PCI_PLOCK#
PCI_REQ3# 4 7 PCI_PERR#
+3.3V_RUN 5 6 PCI_REQ0#

RN2102 SRN8K2J-4-GP
+3.3V_RUN
1 8 PCI_STOP#
2 7 INT_PIRQE#
3 6 INT_PIRQC#
4 5 INT_PIRQG#

U2101 NL17SZ08DFT2G-GP
+3.3V_RUN
VCC A
DY
Y GND B
9,37,70,76,78,80 PLT_RST# PCI_PLTRST#
R2101 0R0402-PAD
C2101 SC220P50V2KX-3GP

BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

RN2104 SRN8K2J-2-GP-U
USB_OC#2_3 1 10 +3.3V_ALW
SMC_WAKE_SCI#_R 2 9 USB_OC#12_13
USB_OC#6_7 3 8 USB_OC#8_9
USB_OC#0_1 4 7 USB_OC#10_11
+3.3V_ALW 5 6 USB_OC#4_5

R2105 4K7R2J-2-GP
PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

U2001E IBEXPEAK-M-GP-NF
5 OF 10

PCI:
AD0 H40, AD1 N34, AD2 C44, AD3 A38, AD4 C36, AD5 J34, AD6 A40, AD7 D45, AD8 E36, AD9 H48, AD10 E40, AD11 C40, AD12 M48, AD13 M45, AD14 F53, AD15 M40, AD16 M43, AD17 J36, AD18 K48, AD19 F40, AD20 C42, AD21 K46, AD22 M51, AD23 J52, AD24 K51, AD25 L34, AD26 F42, AD27 J40, AD28 G46, AD29 F44, AD30 M47, AD31 H36
C/BE0# J50, C/BE1# G42, C/BE2# H47, C/BE3# G34
PIRQA# G38, PIRQB# H51, PIRQC# B37, PIRQD# A44
REQ0# F51, REQ1#/GPIO50 A46, REQ2#/GPIO52 B45, REQ3#/GPIO54 M53
GNT0# F48, GNT1#/GPIO51 K45, GNT2#/GPIO53 F36, GNT3#/GPIO55 H53
PIRQE#/GPIO2 B41, PIRQF#/GPIO3 K53, PIRQG#/GPIO4 A36, PIRQH#/GPIO5 A48
PCIRST# K6
SERR# E44, PERR# E50
IRDY# A42, PAR H44, DEVSEL# F46, FRAME# C46
PLOCK# D49
STOP# D41, TRDY# C48
PME# M7
PLTRST# D5
CLKOUT_PCI0 N52, CLKOUT_PCI1 P53, CLKOUT_PCI2 P46, CLKOUT_PCI3 P51, CLKOUT_PCI4 P48

NVRAM:
NV_CE#0 AY9, NV_CE#1 BD1, NV_CE#2 AP15, NV_CE#3 BD8
NV_DQS0 AV9, NV_DQS1 BG8
NV_DQ0/NV_IO0 AP7, NV_DQ1/NV_IO1 AP6, NV_DQ2/NV_IO2 AT6, NV_DQ3/NV_IO3 AT9, NV_DQ4/NV_IO4 AV6, NV_DQ5/NV_IO5 BB1, NV_DQ6/NV_IO6 BB3, NV_DQ7/NV_IO7 BA4, NV_DQ8/NV_IO8 BE4, NV_DQ9/NV_IO9 BB6, NV_DQ10/NV_IO10 BD6, NV_DQ11/NV_IO11 BB7, NV_DQ12/NV_IO12 BC8, NV_DQ13/NV_IO13 BJ8, NV_DQ14/NV_IO14 BJ6, NV_DQ15/NV_IO15 BG6
NV_ALE BD3, NV_CLE AY6
NV_RCOMP AU2
NV_RB# AV7
NV_WR#0_RE# AY8, NV_WR#1_RE# AY5
NV_WE#_CK0 AV11, NV_WE#_CK1 BF5

USB:
USBP0N H18, USBP0P J18, USBP1N A18, USBP1P C18, USBP2N N20, USBP2P P20, USBP3N J20, USBP3P L20, USBP4N F20, USBP4P G20, USBP5N A20, USBP5P C20, USBP6N M22, USBP6P N22, USBP7N B21, USBP7P D21, USBP8N H22, USBP8P J22, USBP9N F22, USBP9P F22, USBP10N A22, USBP10P C22, USBP11N G24, USBP11P H24, USBP12N L24, USBP12P M24, USBP13N A24, USBP13P C24
USBRBIAS# B25, USBRBIAS D25
OC0#/GPIO59 N16, OC1#/GPIO40 J16, OC2#/GPIO41 F16, OC3#/GPIO42 L16, OC4#/GPIO43 E14, OC5#/GPIO9 G16, OC6#/GPIO10 F12, OC7#/GPIO14 T15

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

+V_NVRAM_VCCQ
R2102 KR2J-1-GP DY
NV_CLE
+V_NVRAM_VCCQ
R2103 KR2J-1-GP DY
NV_ALE

Danbury Technology:
Disabled when Low.
Enable when High.

NV_RCOMP 1 TP2105 TPAD14-GP

R2106 22D6R2F-L1-GP
USB_RBIAS_PN

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

TPAD14-GP TP2102, TP2103, TP2104
TPAD14-GP TP2110
TPAD14-GP TP2115

70 PCLK_FWH
23 CLK_PCI_FB
37 PCLK_KBC
R2107 22R2J-2-GP PCLK_FWH_R
R2108 22R2J-2-GP CLK_PCI_FB_R
R2109 22R2J-2-GP PCLK_KBC_R
EC2101 SC4D7P50V2CN-1GP DY

KBC CLK EMI

<Core Design>
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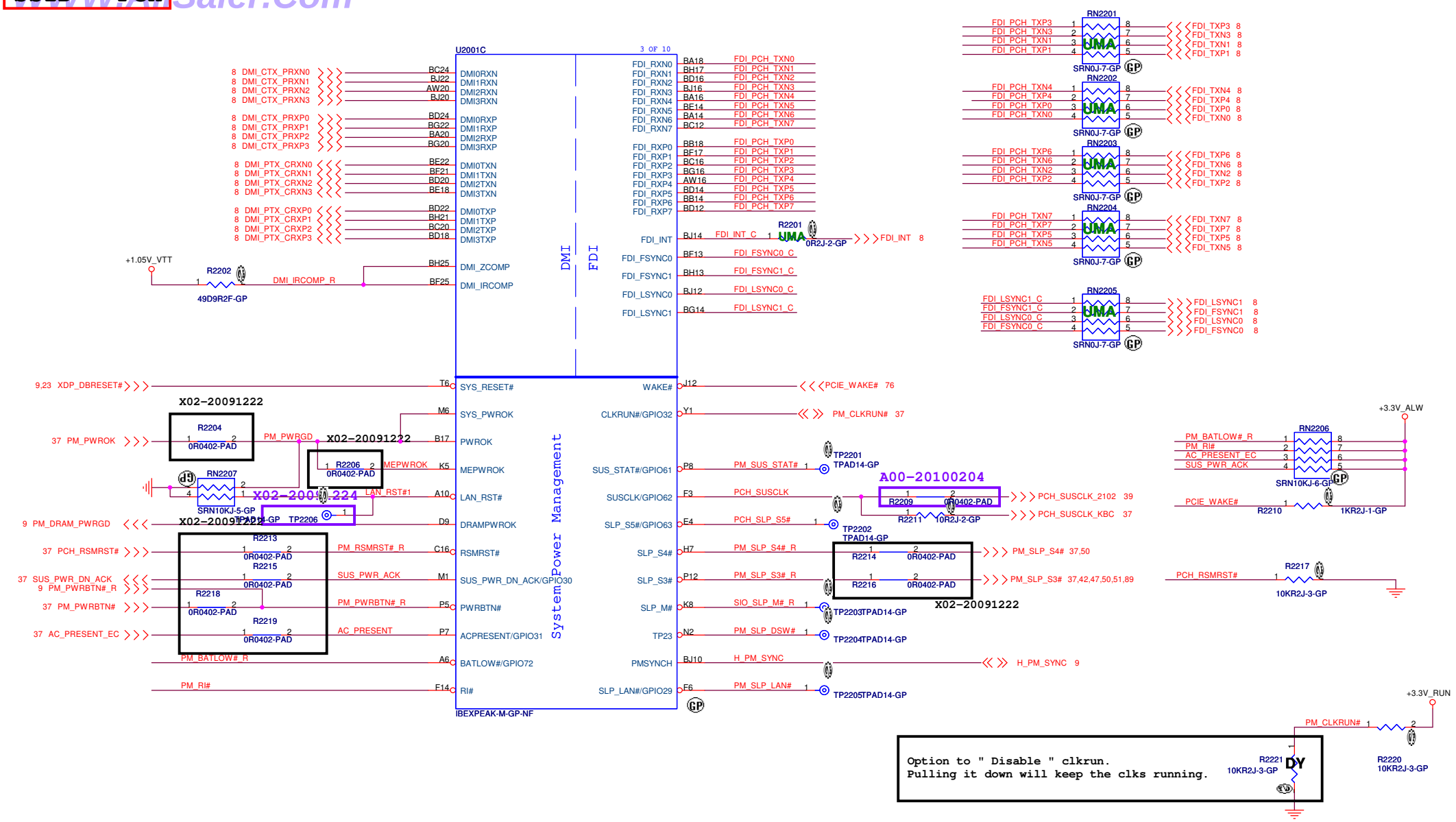
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: Document Number: Berry Rev: X01
Date: Wednesday, February 24, 2010 Sheet 21 of 92

SSID = PCH



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)

Size | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 22 of 92

SSID = PCH

U2001B

2 OF 10

PCIE_RXN2 PCIE_RXP2 PCIE_TXN2 PCIE_TXP2 — C2301 SCD1U10V2KX-5GP, C2302 SCD1U10V2KX-5GP — PCIE_C_TXN2 PCIE_C_TXP2 — WLAN

PCIE_RXN3 PCIE_RXP3 PCIE_TXN3 PCIE_TXP3 — C2303 SCD1U10V2KX-5GP, C2306 SCD1U10V2KX-5GP — PCIE_C_TXN3 PCIE_C_TXP3 — LAN

PCIE_RXN4 PCIE_RXP4 PCIE_TXN4 PCIE_TXP4 — C2304 SCD1U10V2KX-5GP, C2305 SCD1U10V2KX-5GP — PCIE_C_TXN4 PCIE_C_TXP4 — W-WAN

x01 change tolerant 20091117

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

PCI-E* Controller Link

SMBus

PEG

From CLK BUFFER

Clock Flex

SMBALERT#/GPIO11 — PCH_GPIO11 25
SMBCLK — PCH_SMB_CLK
SMBDATA — PCH_SMB_DATA
SML0ALERT#/GPIO60 — TPM_ID1
SML0CLK — SML0_CLK 9
SML0DATA — SML0_DATA 9
SML1ALERT#/GPIO74 — LPD_SPI_INTR#
SML1CLK/GPIO58 — KBC_SCL1 37
SML1DATA/GPIO75 — KBC_SDA1 37
CL_CLK1 — CL_CLK — TP2302 TPAD14-GP
CL_DATA1 — CL_DATA — TP2303 TPAD14-GP
CL_RST1# — CL_RST# — TP2304 TPAD14-GP
PEG_A_CLKRQ#/GPIO47 — PEG_CLKREQ#_C — R2310 0R2J-2-GP — PEG_CLKREQ# 82 — DY
CLKOUT_PEG_A_N/P — CLK_PCIE_VGA# / CLK_PCIE_VGA — CLK_PCIE_VGA# 80 / CLK_PCIE_VGA 80
CLKOUT_DMI_N/P — CLK_EXP_N / CLK_EXP_P — CLK_EXP_N 9 / CLK_EXP_P 9
CLKOUT_DP_N/CLKOUT_BCLK1_N — AT1
CLKOUT_DP_P/CLKOUT_BCLK1_P — AT3
CLKIN_DMI_N/P — CLKIN_DMI# / CLKIN_DMI — CLKIN_DMI# 7 / CLKIN_DMI 7
CLKIN_BCLK_N/P — CLK_CPU_BCLK# / CLK_CPU_BCLK — CLK_CPU_BCLK# 7 / CLK_CPU_BCLK 7
CLKIN_DOT_96N/P — CLK_DREF# / CLK_DREF — CLK_DREF# 7 / CLK_DREF 7
CLKIN_SATA_N/CKSSCD_N — CLK_PCIE_SATA# 7
CLKIN_SATA_P/CKSSCD_P — CLK_PCIE_SATA 7
REFCLK14IN — CLK_PCH_14M — CLK_PCH_14M 7
CLKIN_PCILOOPBACK — CLK_PCI_FB — CLK_PCI_FB 21
XTAL25_IN — XTAL25_IN
XTAL25_OUT — XTAL25_OUT
XCLK_RCOMP — XCLK_RCOMP — R2306 90D9R2F-1-GP — +1.05V_VTT
CLKOUTFLEX0/GPIO64 — CLK_PCH_GPIO64 — TP2301 TPAD14-GP
CLKOUTFLEX1/GPIO65 — P43
CLKOUTFLEX2/GPIO66 — T42
CLKOUTFLEX3/GPIO67 — CLK48_GPIO — TP2307 TPAD14-GP

X01 20091118

CLKOUT_PCIE0N/P — PCIECLKRQ0#/GPIO73 — PCIE_CLK_RQ0# P9
CLKOUT_PCIE1N/P — PCIECLKRQ1#/GPIO18 — PCIE_CLK_RQ1# U4
CLKOUT_PCIE2N/P — PCIECLKRQ2#/GPIO20 — 76 CLK_PCIE_WLAN# / 76 CLK_PCIE_WLAN — 76 WLAN_CLKREQ# N4
CLKOUT_PCIE3N/P — PCIECLKRQ3#/GPIO25 — 76 CLK_PCIE_LAN# / 76 CLK_PCIE_LAN — R2304 10KR2J-3-GP — PCIE_CLK_RQ3# A8
CLKOUT_PCIE4N/P — PCIECLKRQ4#/GPIO26 — 76 CLK_PCIE_WWAN# / 76 CLK_PCIE_WWAN — 76 WWAN_CLKREQ# M9
CLKOUT_PCIE5N/P — PCIECLKRQ5#/GPIO44 — PCIE_CLK_RQ5# H6
CLKOUT_PEG_B_N/P — PEG_B_CLKRQ#/GPIO56 — PEG_B_CLKRQ# P13

+3.3V_ALW
RN2307 — SRN10KJ-6-GP
WWAN_CLKREQ#
PCIE_CLK_RQ0#
PEG_B_CLKRQ#
PCIE_CLK_RQ5#

+3.3V_RUN
RN2308 — SRN10KJ-6-GP
XDP_DBRESET# — WLAN_CLKREQ# — INT_SERIRQ — PCIE_CLK_RQ1#
XDP_DBRESET# 9,22
INT_SERIRQ 24,37

+3.3V_ALW
TPM_ID1 — R2305 10KR2J-3-GP
LPD_SPI_INTR# — R2311 10KR2J-3-GP

+3.3V_ALW
RN2302 SRN2K2J-1-GP
PCH_SMB_CLK
PCH_SMB_DATA

+3.3V_ALW
RN2309 SRN2K2J-1-GP — SML0_DATA / SML0_CLK
RN2301 SRN2K2J-1-GP — KBC_SCL1 / KBC_SDA1

+3.3V_ALW
UMA R2308 10KR2J-3-GP
PEG_CLKREQ#_C
DIS R2309 10KR2J-3-GP

+3.3V_RUN
RN2303 SRN2K2J-1-GP
Q2301 2N7002EDW-GP
84.27002.F3F
PCH_SMB_DATA — PCH_SMBDATA 7,18,19,76
PCH_SMB_CLK — PCH_SMBCLK 7,18,19,76

DIS uses 0ohm 63.R0034.1DL
UMA uses 12pF 78.12034.1FL
X01 2009/11/06

XTAL25_IN — C2308 COLAY SC12P50V2JN-3GP — UMA R2303 1M1R2J-GP UMA — X2301 XTAL-25MHZ-96GP — C2307 UMA SC12P50V2JN-3GP — XTAL25_OUT
X01 2009/11/05

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)
Size: — Document Number: Berry — Rev: X01
Date: Wednesday, February 24, 2010 — Sheet 23 of 92

SSID = PCH

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

For EMI

x01 Change tolerant 20091117

X01 20091118 layout swap

x01 Change tolerant 20091117

<Core Design>

Wistron Corporation
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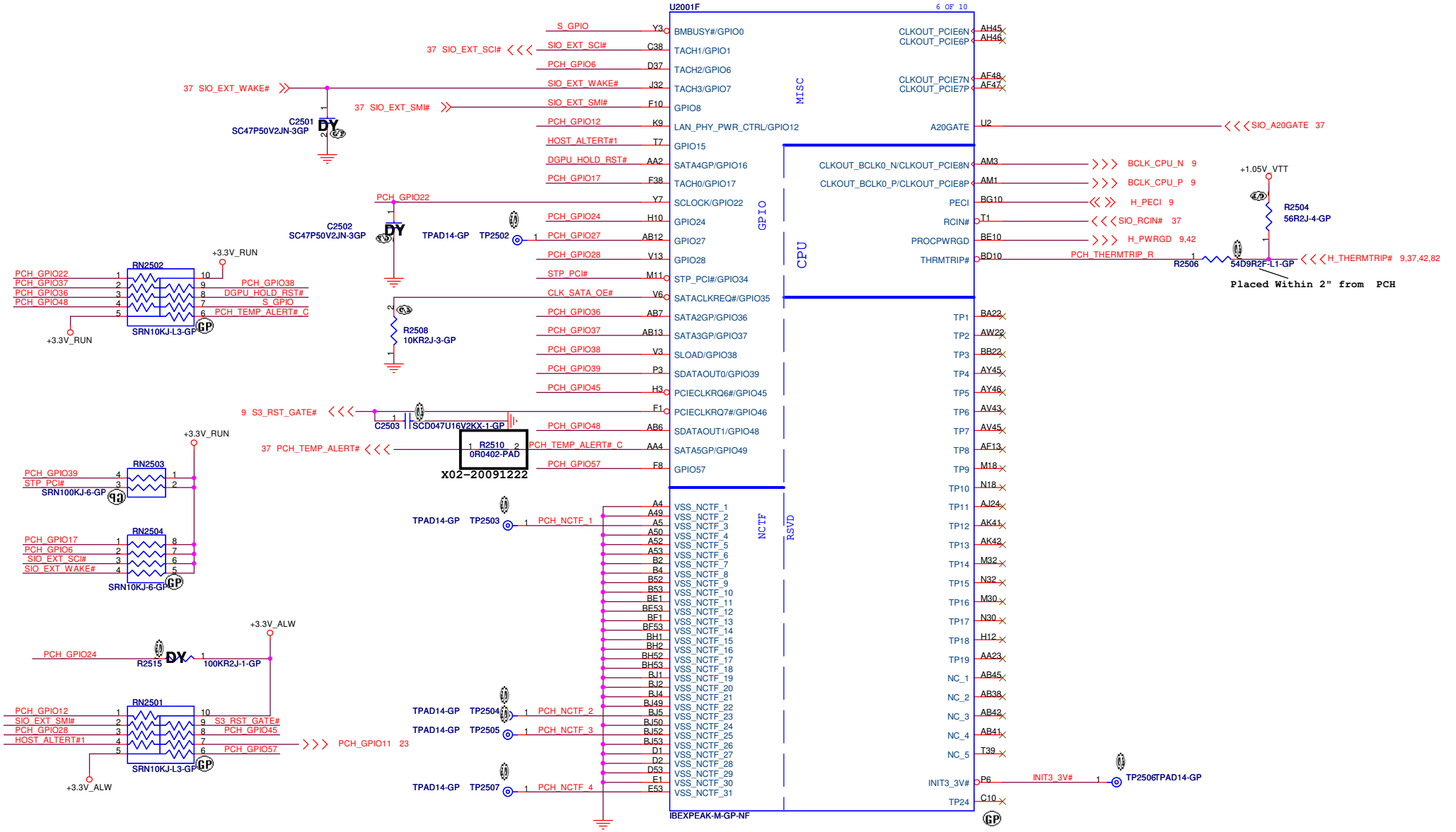
Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 24 of 92

SSID = PCH



<Core Design>

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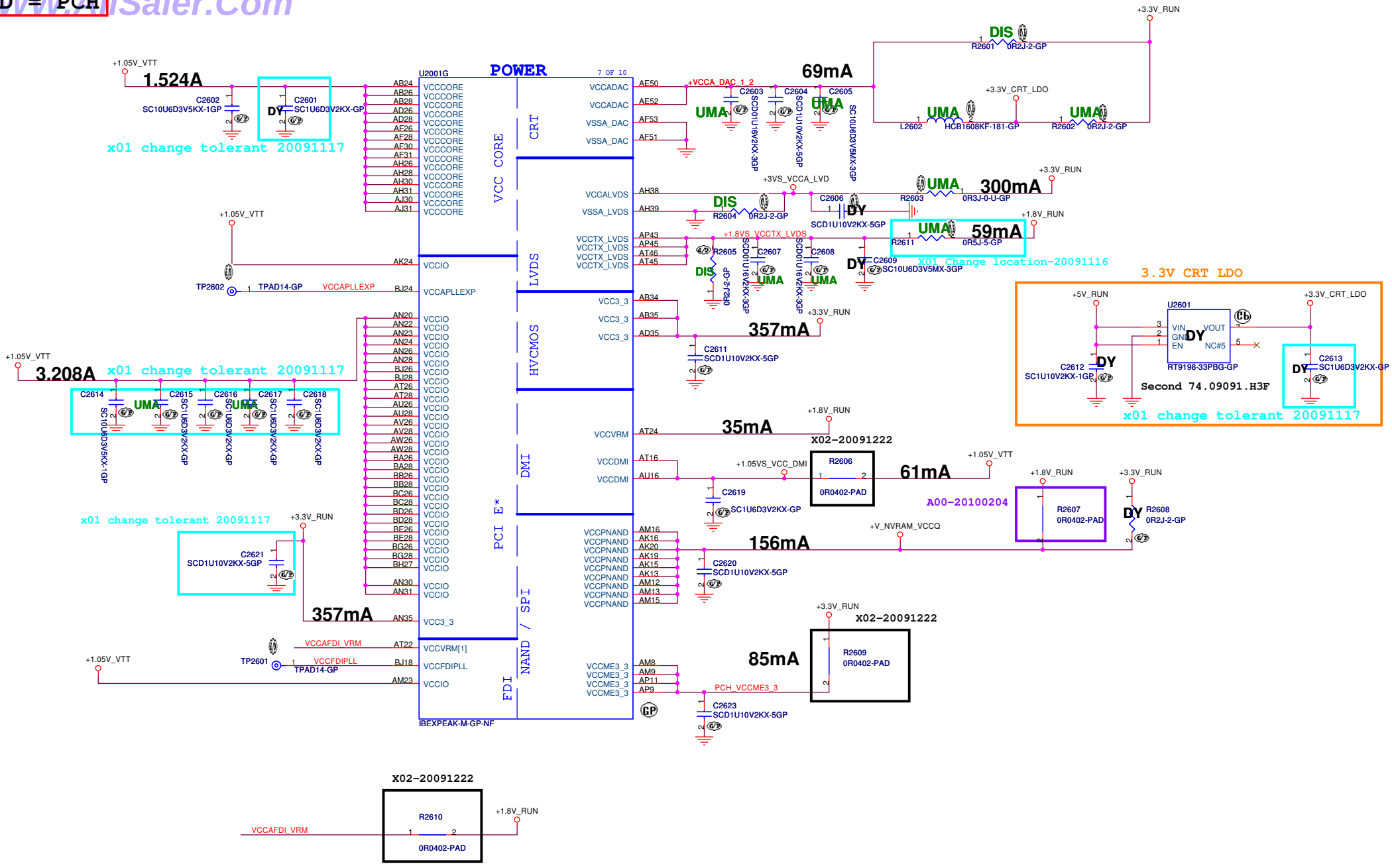
Title: PCH (GPIO/CPU)

Size | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 25 of 92

SSID = PCH



<Core Design>

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Title: PCH (POWER1)

Size | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 26 of 92

SSID = PCH

U2001J POWER 10 OF 10

TP2701 VCCACLK TPAD14-GP

AP51 VCCACLK
AP53 VCCACLK
AF23 VCCLAN
AF24 VCCLAN
DCPSUSBYP Y20 DCPSUSBYP
AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
V9 DCPRTC
AU24 VCCVRM
BB51 VCCADPLLA
BB53 VCCADPLLA
BD51 VCCADPLLB
BD53 VCCADPLLB
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO
V12 DCPSST
Y22 DCPUS
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
AT18 V_CPU_IO
AU18 V_CPU_IO
A12 VCCRTC

IBEXPEAK-M-GP-NF

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | PCI/GPIO/LPC | CPU | RTC | HDA

VCCIO V24, V26, Y24, Y26
VCCSUS3_3 V28, U28, U26, U24, P28, P26, N28, N26, M28, M26, L28, L26, J28, J26, H28, H26, G28, G26, F28, F26, E28, E26, C28, C26, B27, A28, A26
VCCSUS3_3 U23
VCCIO V23
V5REF_SUS F24
V5REF K49
VCC3_3 J38, L38, M36, N36, P36, U35
VCC3_3 AD13
VCCSATAPLL AK3, AK1
VCCIO AH22
VCCVRM AT20
VCCIO AH19, AD20, AF22, AD19, AF20, AE19, AH20, AB19, AB20, AB22, AD22
VCCME AA34, Y34, Y35, AA35
VCCSUSHDA L30

+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+1.8V_RUN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+1.05VALW_INT_VCCSUS
+VCCSST
+VCCRTCEXT
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+VCCSUSHDA
VCCSATAPLL TP2702 TPAD14-GP
+RTC_CELL

C2705 SC1U6D3V2KX-GP DY
C2706 SCD1U10V2KX-5GP
C2703 SCD1U10V2KX-5GP
C2707 SC10U6D3V5KX-1GP
C2704 SC10U6D3V5MX-GP DY
C2708 SC1U6D3V2KX-GP
C2710 SC1U6D3V2KX-GP DY
C2709 SCD1U10V2KX-5GP
D2701 CH751H-40PT-GP
D2702 CH751H-40PT-GP
R2702 10R2J-2-GP
R2701 10R2J-2-GP
C2713 SC1U10V2KX-1GP
C2715 SC1U10V2KX-1GP
C2718 SCD1U10V2KX-5GP
C2719 SCD1U10V2KX-5GP
C2727 SC1U6D3V2KX-GP
L2702 IND-10UH-218-GP
L2703 IND-10UH-218-GP
C2711 SC10U6D3V5MX-3GP DY
C2712 SC1U6D3V2KX-GP
C2716 SC10U6D3V5MX-3GP DY
C2717 SC1U6D3V2KX-GP
C2714 SCD1U10V2KX-5GP
C2720 SC1U6D3V2KX-GP
C2721 SC1U6D3V2KX-GP
C2722 SC1U6D3V2KX-GP
C2725 SCD1U10V2KX-5GP
C2726 SCD1U10V2KX-5GP
C2728 SCD1U10V2KX-5GP
C2729 SCD1U10V2KX-5GP
C2730 SC10U6D3V5KX-1GP
C2731 SCD1U10V2KX-5GP
C2732 SCD1U10V2KX-5GP
C2734 SCD1U10V2KX-5GP
C2735 SCD1U10V2KX-5GP
C2733 SC1U6D3V2KX-GP
R2703 0R0402-PAD

x01 change tolerant 20091117
x01 20091121
x01 change tolerant 20091118

1.998A
72mA
73mA
163mA
1mA
2mA
6mA

X02-20091222

<Core Design>

Wistron Corporation
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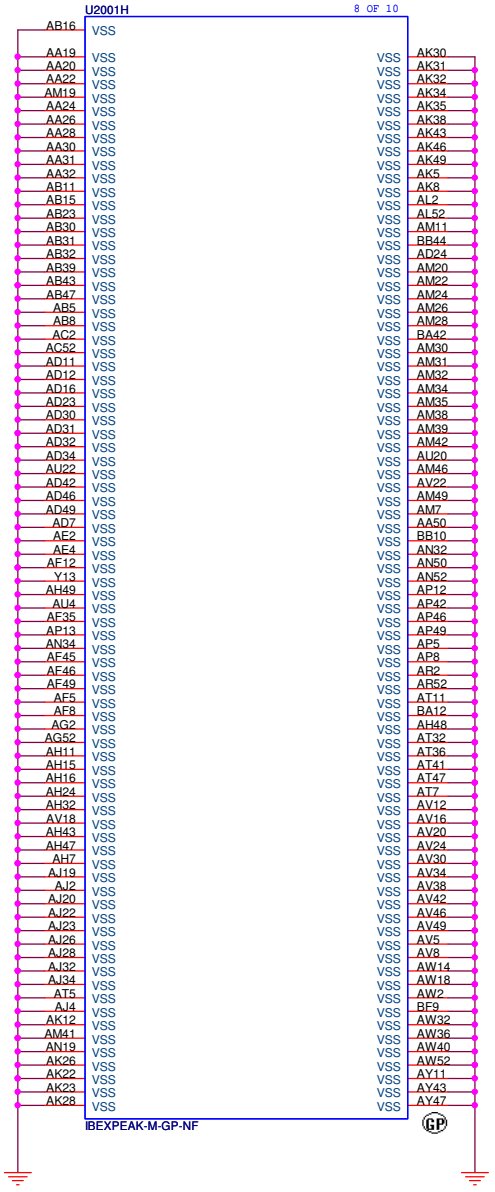
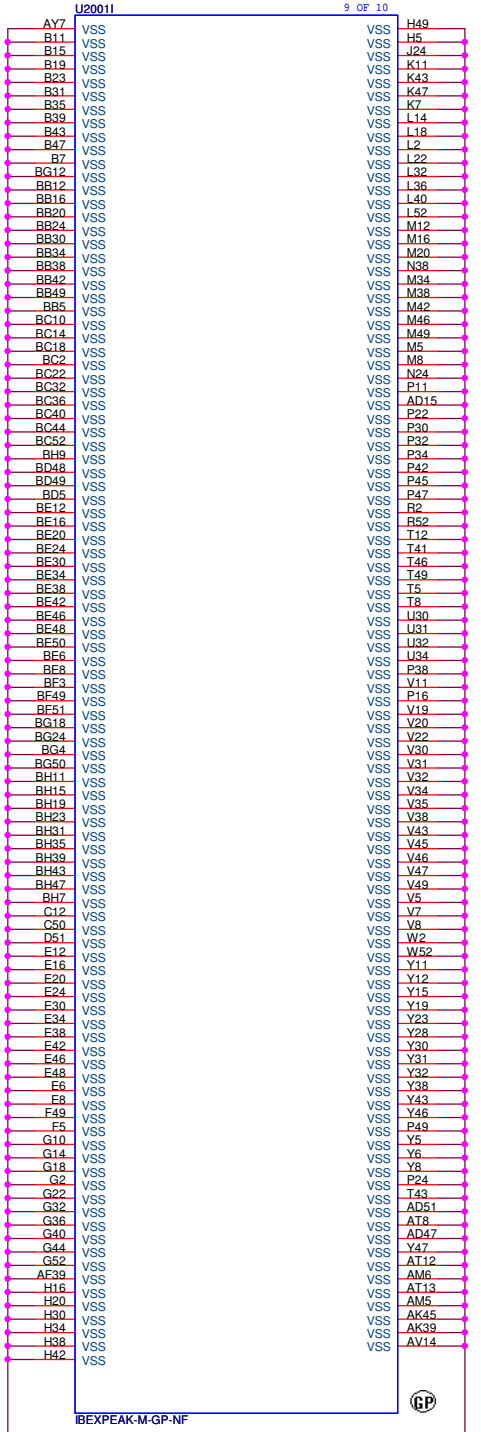
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER2)
Size:
Document Number: Berry
Rev: X01
Date: Wednesday, February 24, 2010 Sheet 27 of 92

SSID = PCH





<Core Design>

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Title: PCH (VSS)

Size	Document Number	Rev
	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 28 of 92

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<Core Design>

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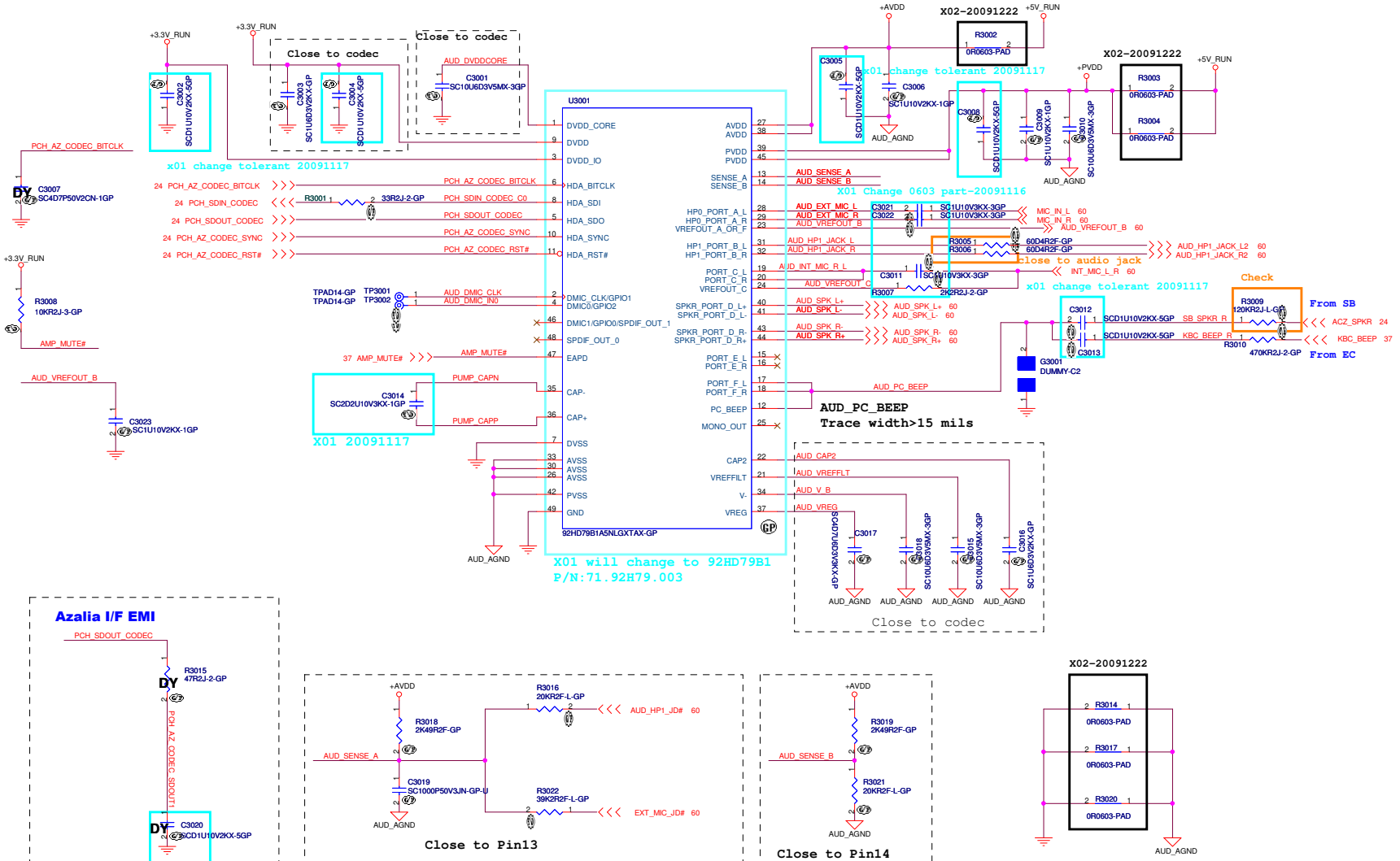
Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 29 of 92

SSID = AUDIO



<Core Design>

Wistron Corporation
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Title: Audio Codec 92HD81B1

Size: Custom | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 30 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 31 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size: Custom | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 32 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 33 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 34 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A3	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 35 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A3	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 36 of 92

CAP close to VCC-GND pin pair

10mW circuit

SSID = KBC

Vendor recommend FW can do it

Vendor recommend can remove

For EMI

MB VERSION			
ID	VER2	VER1	VER0
X00	0	0	0
X01	0	0	1
X02	0	1	0
A00	0	1	1

VGA STRAP		
option	GPIO24	GPIO5
UMA	0	0
Madisan	1	1
Park	1	0
M96	0	1

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Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE781BA0DX

Size: A2 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 37 of 92

(Blanking)

<Core Design>

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Title: Reserved

Size	Document Number	Rev
A4	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 38 of 92

SSID = Thermal

x01 change tolerant 20091117

1. Place near CPU PWM CORE and PCH.

Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.

C3905 must be near Q3901

near EMC2102

2. System Sensor(UMA Only)

Layout notice :
Both DN2 and DP2 routing 10 mil
trace width and 10 mil spacing.

Reserved DISCRETE

3.VGA Sensor(DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.

C3907 must be near Q3902

4.HW T8 sensor

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

EMC2102

GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

A00-20100204

X02-20091222

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

84.2N702.D31

32K suspend clock output

TRIP_SET Pin Voltage
V_DEGREE=(((Degree-75)/21)

T8 shutdown is set 88 deg-C.

x01 change tolerant 20091117

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor EMC2102

Size: Custom | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 39 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 40 of 92

(Blanking)

<Core Design>

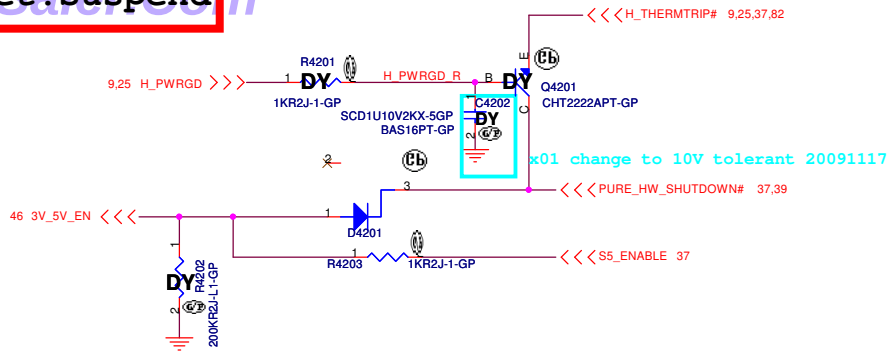
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

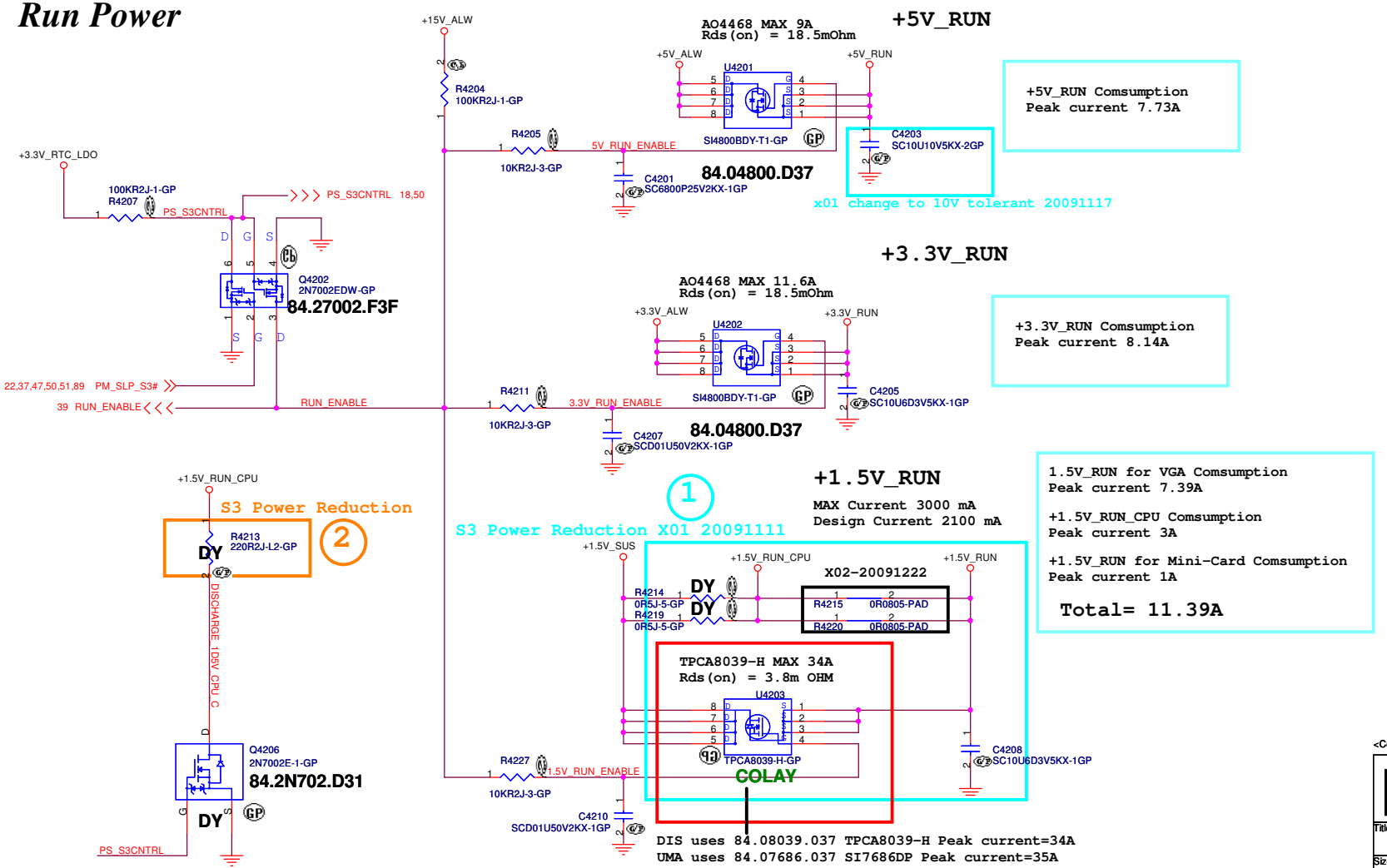
Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 41 of 92

SSID = Reset.Suspend



Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 42 of 92

(Blanking)

<Core Design>

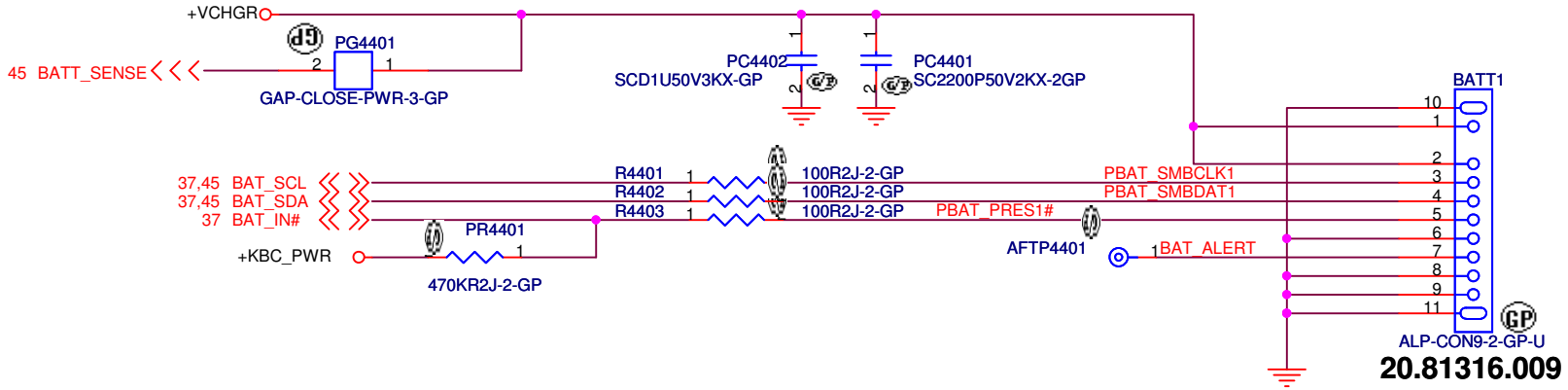
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

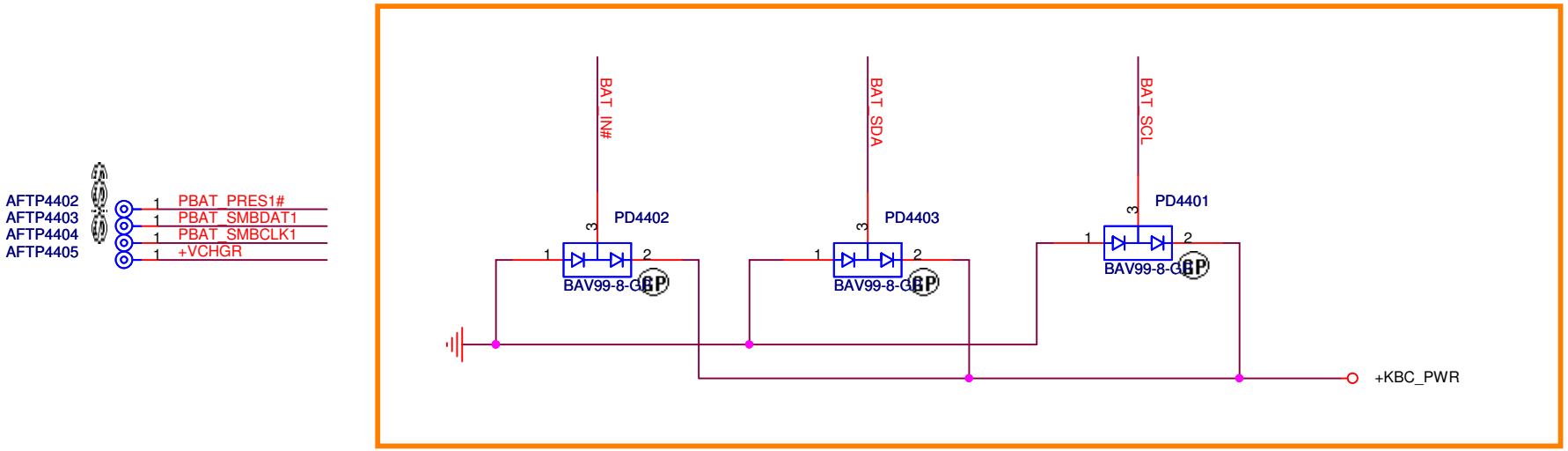
Date: Wednesday, February 24, 2010 | Sheet 43 of 92

Batt Connecter



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>

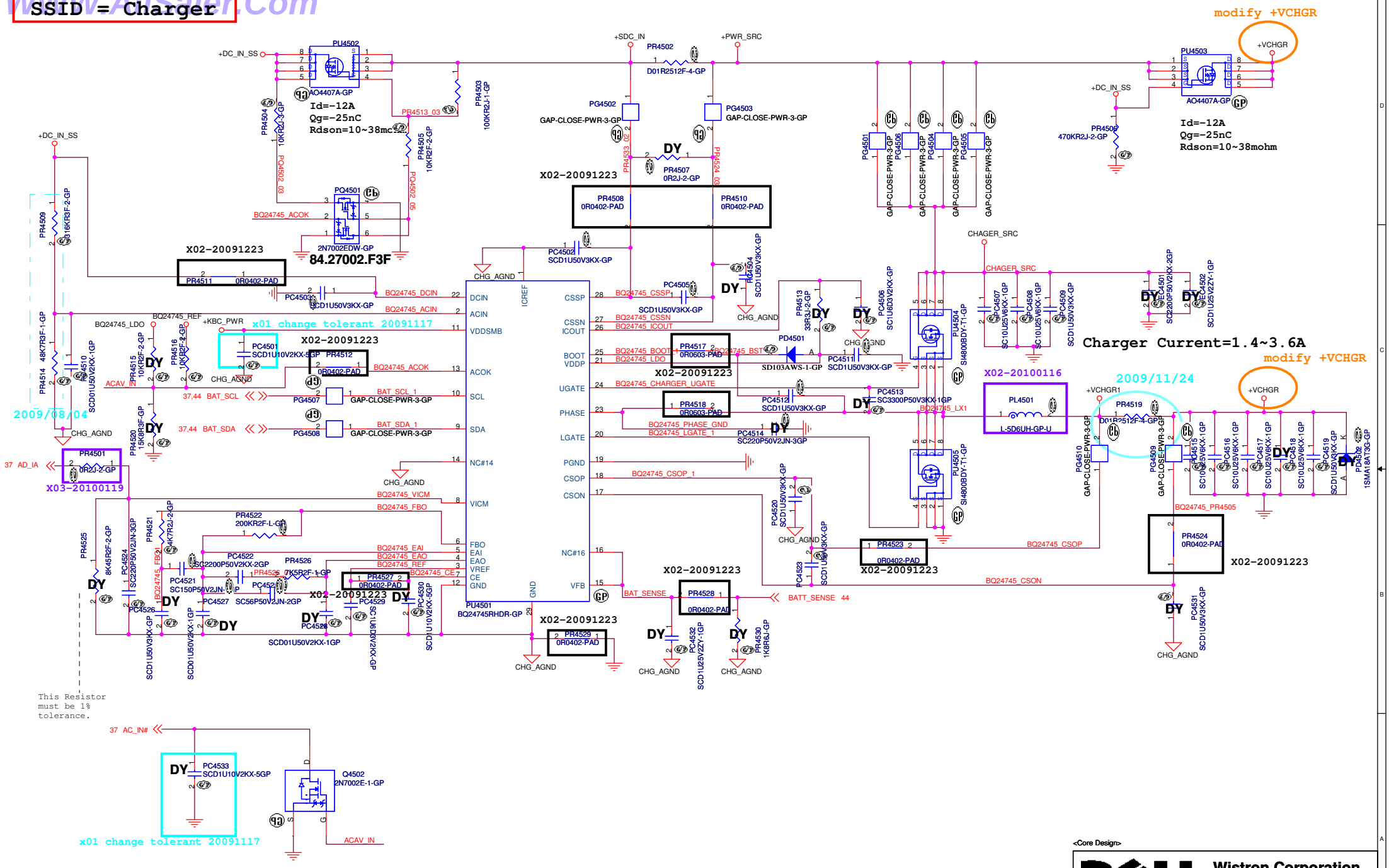
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 44 of 92

SSID = Charger



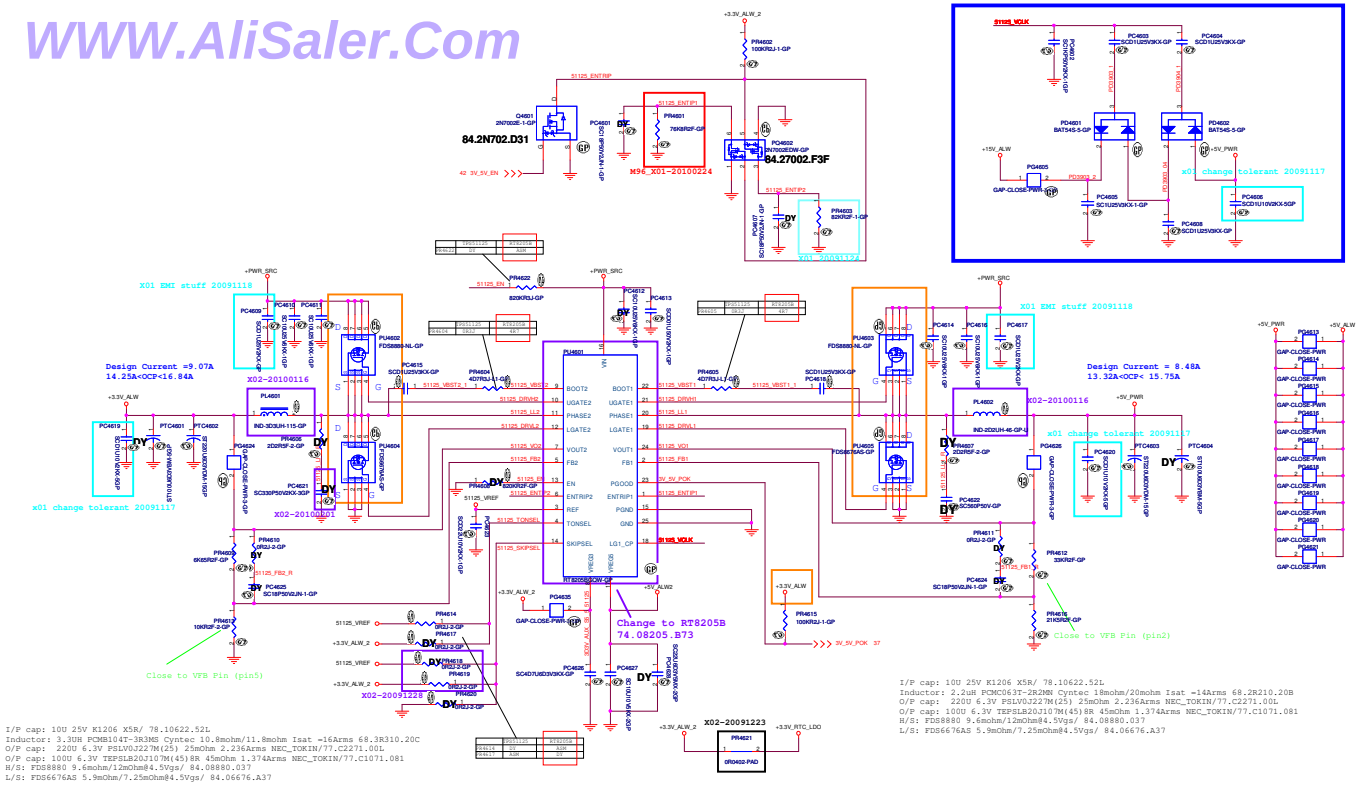
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER BQ24745

Size	Document Number	Rev
Custom	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 45 of 92



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mOhm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mOhm/7.25mOhm@4.5Vgs/ 84.06676.A37

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

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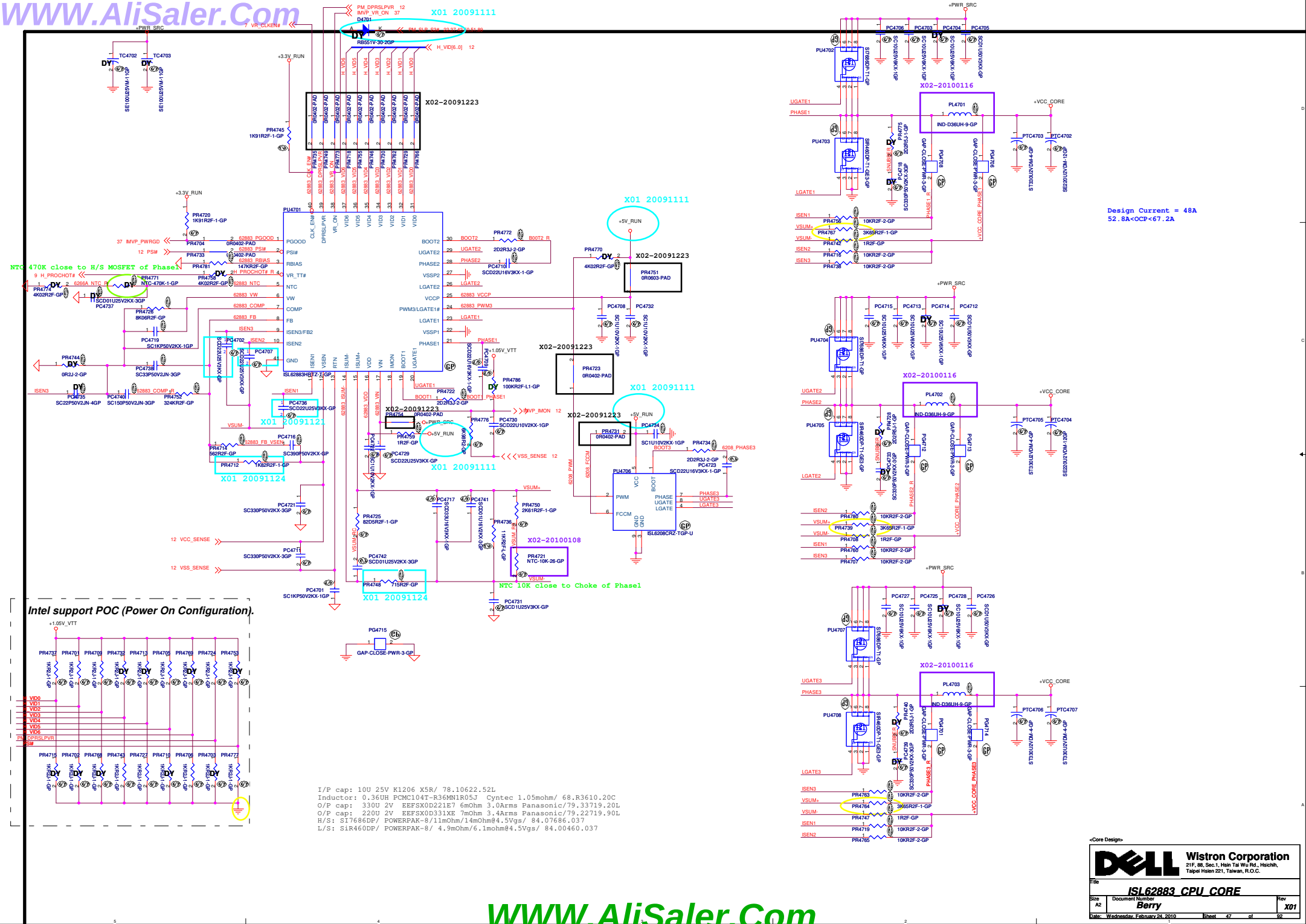
File: RT8205B_5V/3D3V

Size	Document Number	Rev
A1	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 46 of 50



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size: A2 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 47 of 92

(Blanking)

<Core Design>

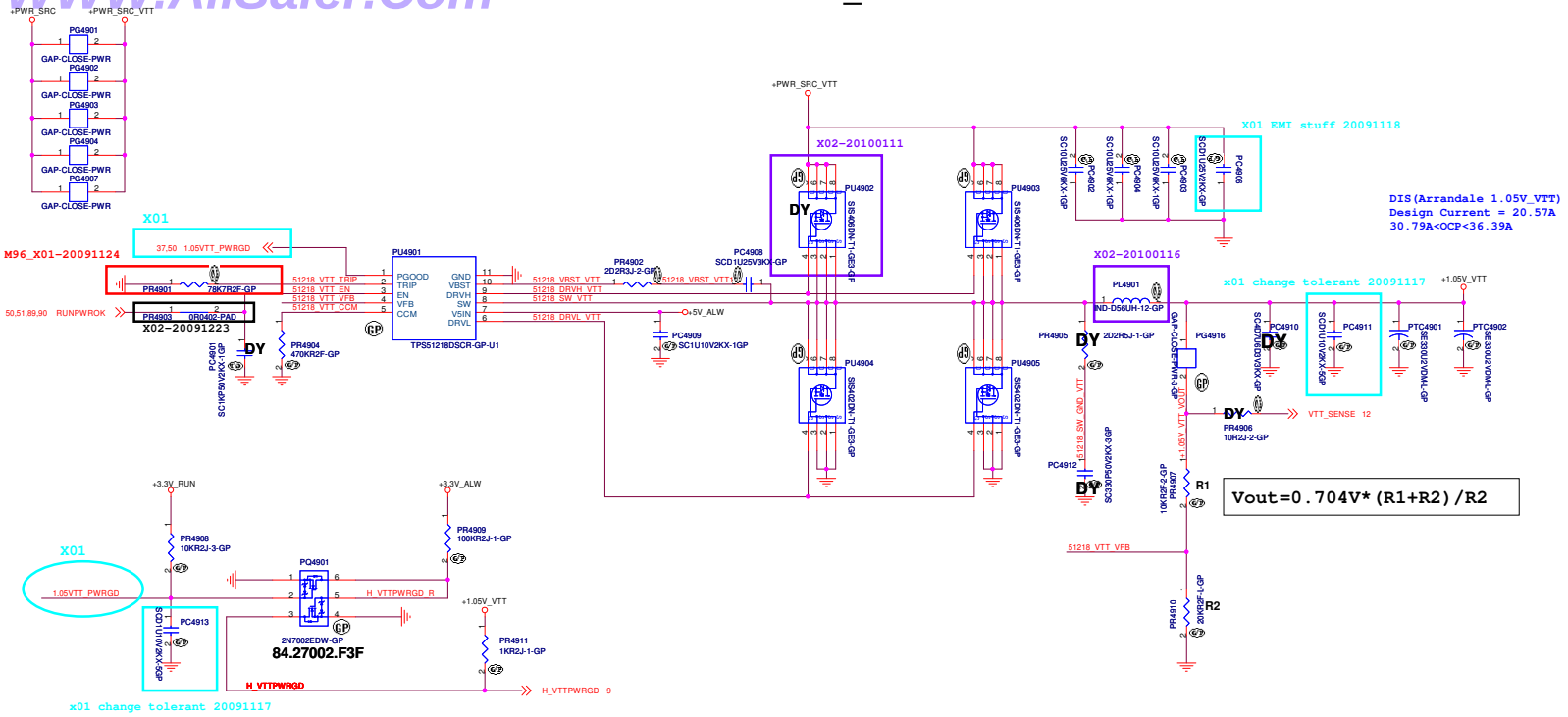
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 48 of 92

TPS51218 for +1.05V_VTT



Frequency setting
470K --->290KHz
200K --->340KHz
100K --->380KHz
39K --->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

DIS(Arrandale 1.05V_VTT)
Design Current = 20.57A
30.79A<OCP<36.39A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V_VTT

Size	Document Number	Rev
A2	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 49 of 92

SSID = PWR.Plane.Regulator_1p5v0p75v

Modified net name

+PWR_SRC_1D5V

x01-20091124

PR5002 4K7R2F-L-GP

PC5002 SC1KP50V2KX-1GP

PC5003 SC1U10V2KX-1GP

PC5001 SC1U10V2KX-1GP

PR5001 5D1R3J-GP

PR5004 20KR2F-L-GP

PR5006 620KR2F-GP

PR5005 0R3J-0-U-GP

PD5001 RB551V-30-2GP

PU5001 TPS51116RGER-GP-U

PC5005 SC1U6D3V2KX-GP

PR5008 1MR2J-GP

PR5009 0R0402-PAD

PC5007 SC1KP50V2KX-1GP

PR5010 0R2J-2-GP

PC5008 SC1U10V2KX-1GP

PR5011 0R0603-PAD

PC5010 SCD033U16V3KX-GP

x01 change tolerant 20091117

RT: ASM
TI: Non_ASM

5 S3 Power Reduction X01 20091111

PQ5003 2N7002E-1-GP 84.2N702.D31

PR5016 100KR2J-1-GP

PQ5002 2N7002E-1-GP 84.2N702.D31

PQ5001 PMBS3904-1-GP

PR5017 4K7R2J-2-GP

PC5024 SCD1U10V2KX-5GP

PR5018 10KR2J-3-GP

PR5015 0R2J-2-GP

PR5019 0R0402-PAD

PR5003 0R2J-2-GP

PC5004 SCD1U10V2KX-5GP

x01 change tolerant 20091117

x01 change tolerant 20091118

X02-20091223

PR5007 0R0402-PAD

PC5006 SCD1U10V2KX-5GP

x01 change tolerant 20091117

PG5002 PG5003 PG5004 PG5006 GAP-CLOSE-PWR

Design Current = 14.45A
22.71A<OCP< 26.84A

PU5002 PU5003 PU5004 SI7686DP-T1-GP SIR460DP-T1-GE3-GP

PC5009 PC5011 PC5012 PC5013 PC5014

PC5015 PC5016 PC5017 PC5018

Design Current = 0.7A

PG5001 PG5016 GAP-CLOSE-PWR

PC5019 SCD1U25V3KX-GP

PL5001 IND-1D5UH-34-GP

X02-20100116

PR5012 2D2R5F-2-GP

PC5022 SC330P50V2KX-3GP

X02-20100201

PG5017 GAP-CLOSE-PWR-3-GP

PC5020 PC5021 PTC5002 PTC5001

x01 change to 330uF 20091124

x01 change tolerant 20091117

PR5013 30KR2F-GP

PC5023 SC18P50V2JN-1-GP

PR5014 30KR2F-GP

Close to VFB Pin (pin5)

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

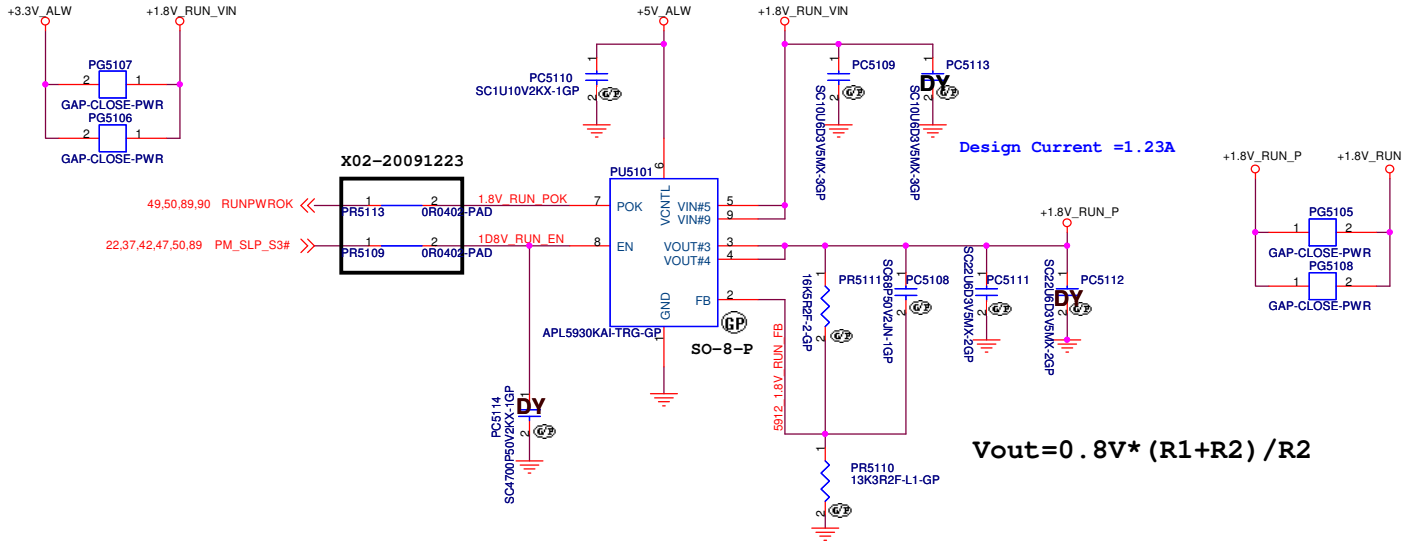
Title: TPS51116_+1.5V_SUS

Size: Custom | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 50 of 92

SSID = PWR.Plane.Regulator_1p8v

APL5930 for +1.8V_RUN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5930 +1.8V RUN	
Size A3	Document Number Berry	Rev X01
Date: Wednesday, February 24, 2010	Sheet 51 of 92	

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<Core Design>

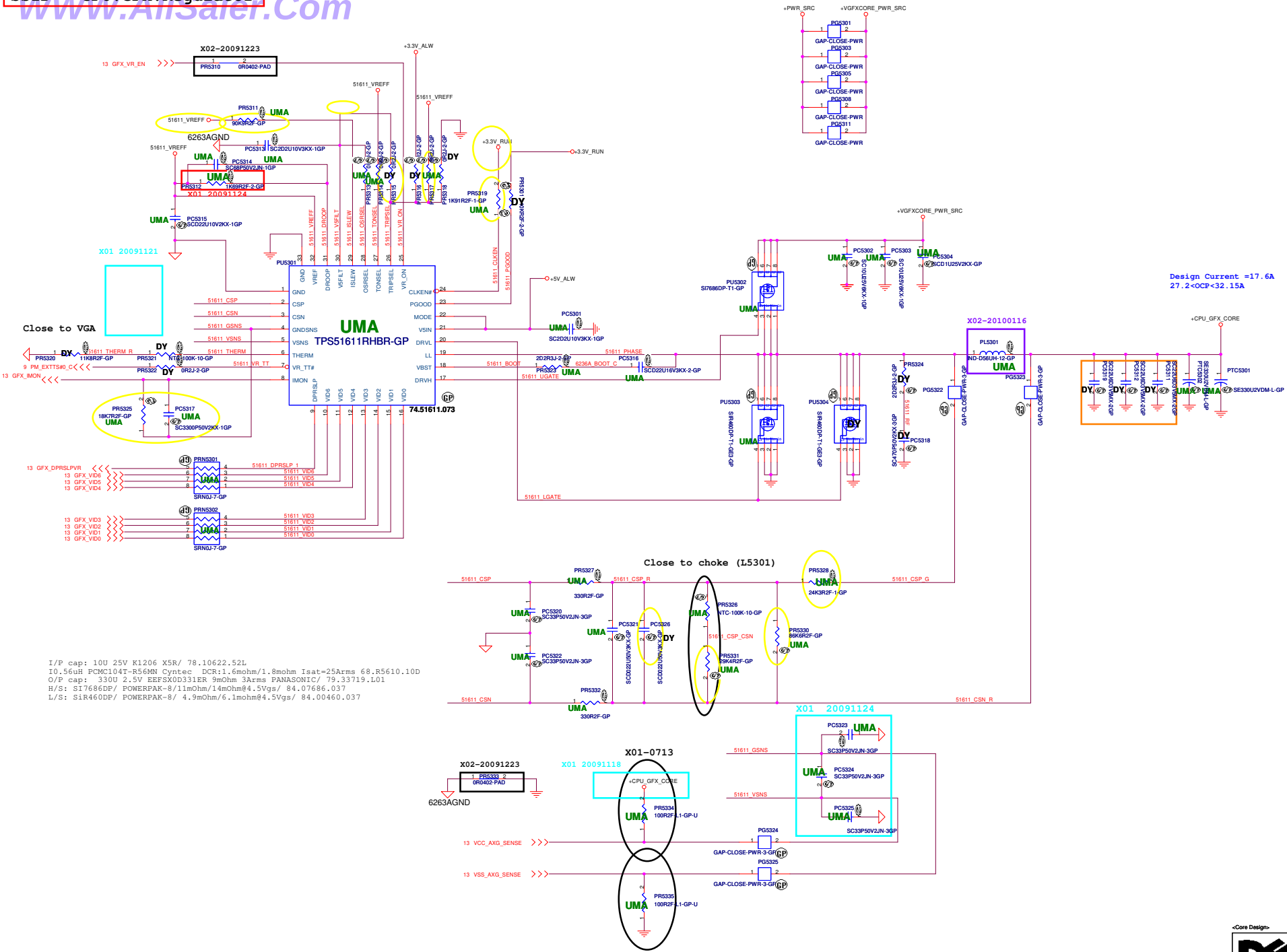
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 52 of 92

SSID = CPU.GFX.Regulator



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

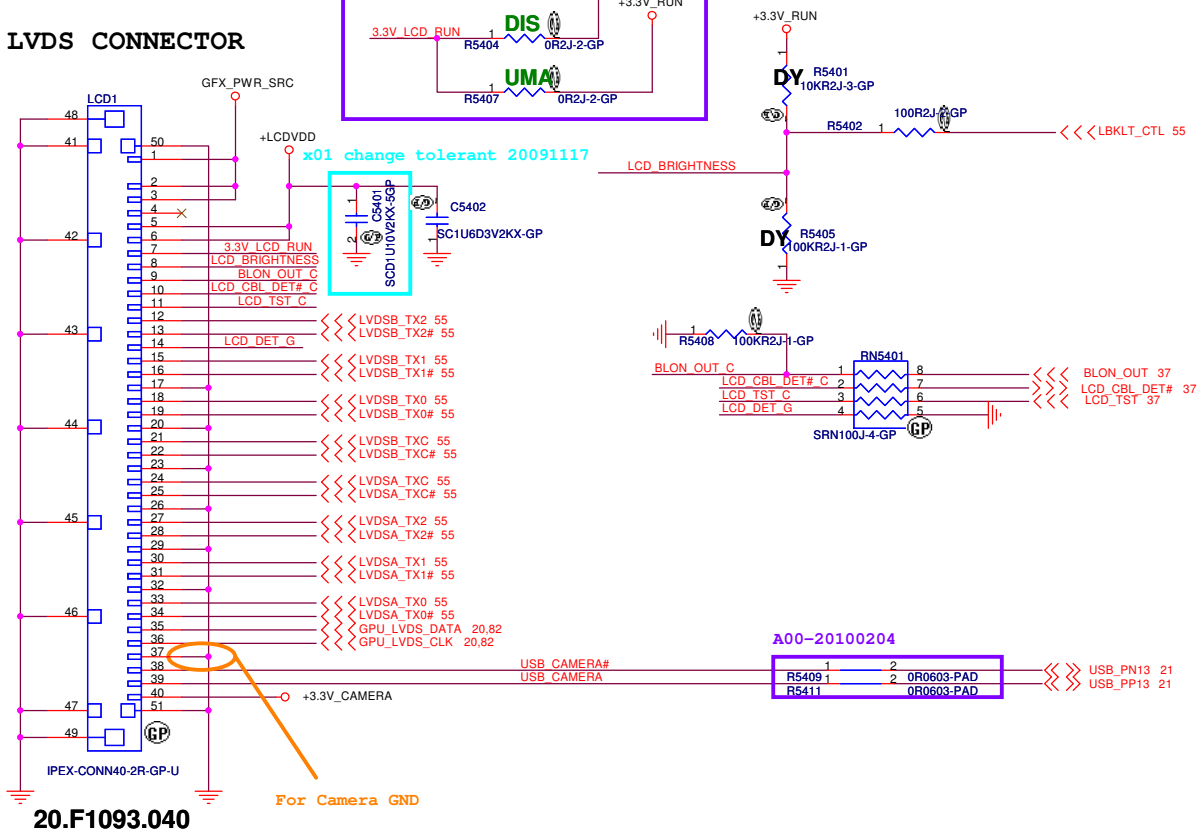
Title: TPS51611_+GFX_CORE(UMA)

Size: A2 | Document Number: Berry | Rev: X01

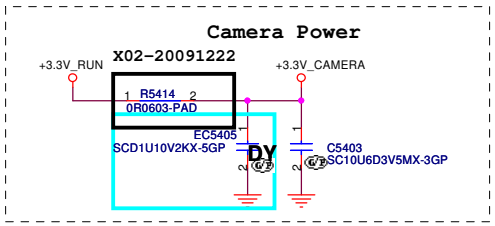
Date: Wednesday, February 24, 2010 | Sheet 53 of 92

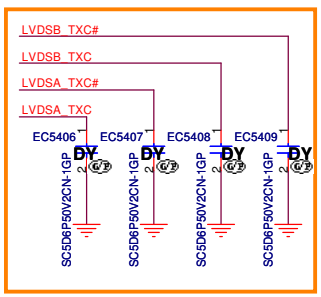
SSID = VIDEO

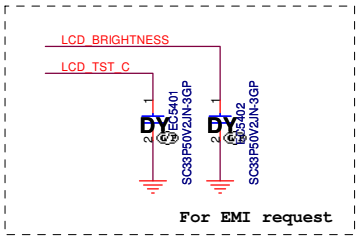
LVDS CONNECTOR



20.F1093.040

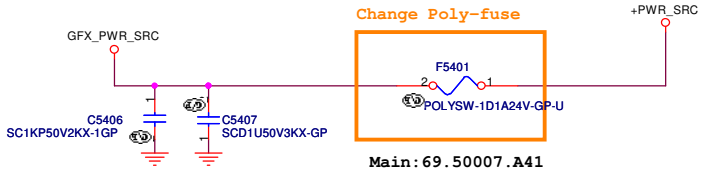






SSID = Inverter

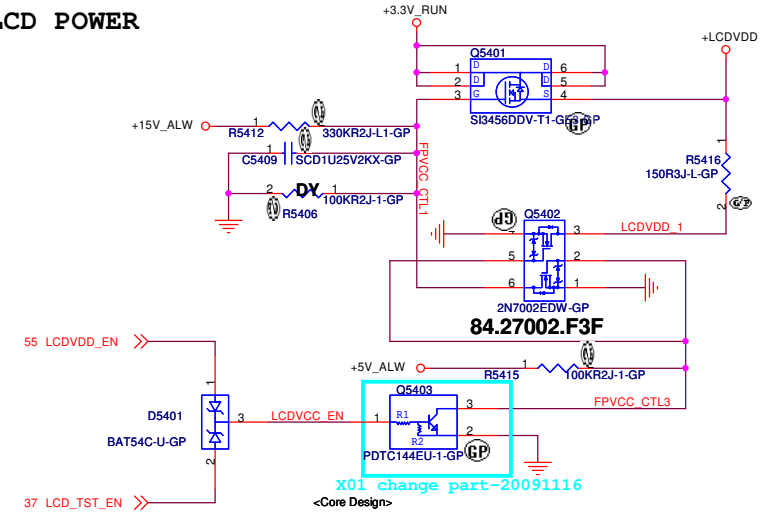
INVERTER POWER



Main:69.50007.A41
Second:69.50007.A31

SSID = VIDEO

LCD POWER

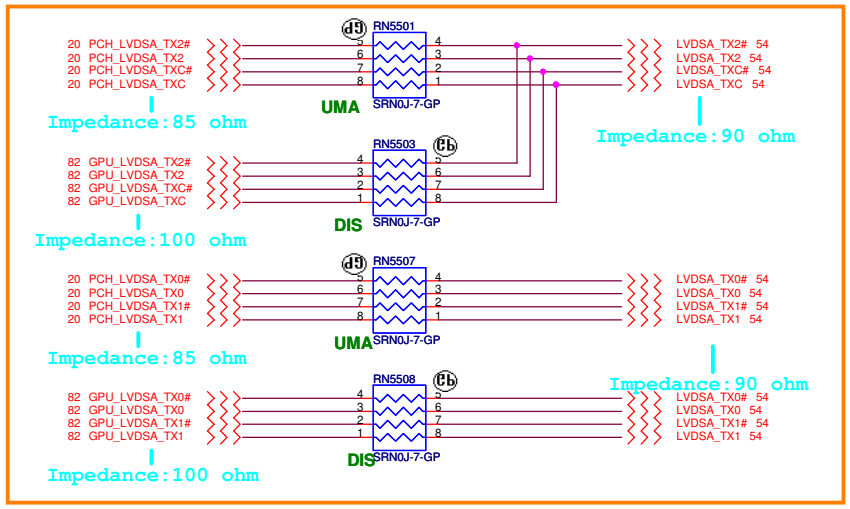


<Core Design>

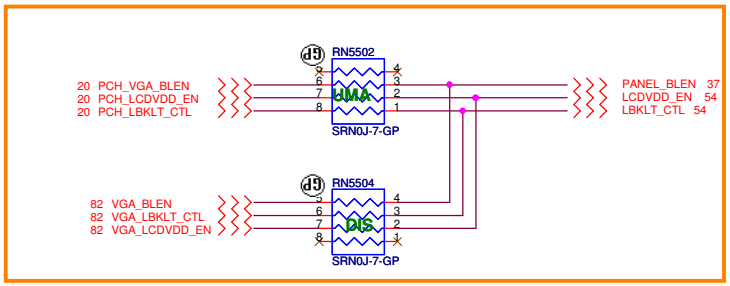
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD/Inverter Connector		
Size: A3	Document Number: Berry	Rev: X01
Date: Wednesday, February 24, 2010	Sheet 54 of 92	

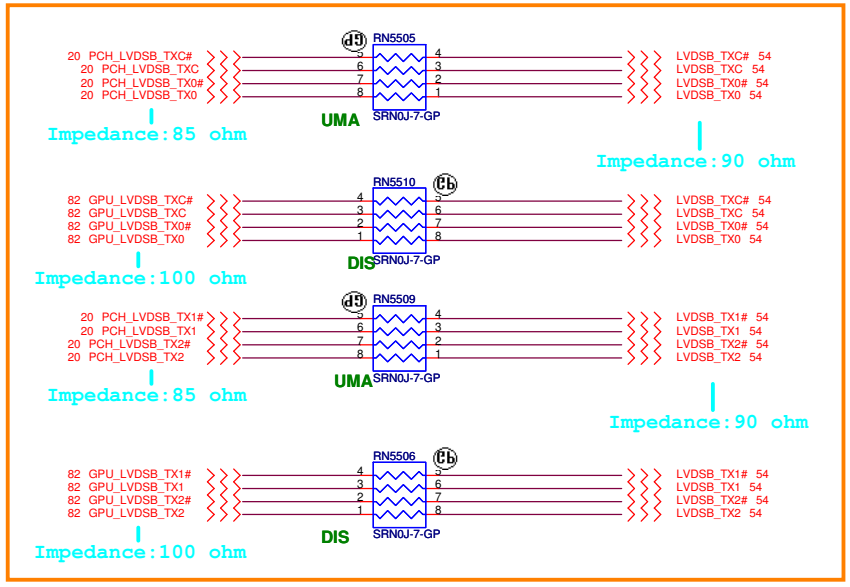
LVDS Channel A



Panel BL brightness/Power En/BL En



LVDS Channel B



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS Switch

Size | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 55 of 92

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

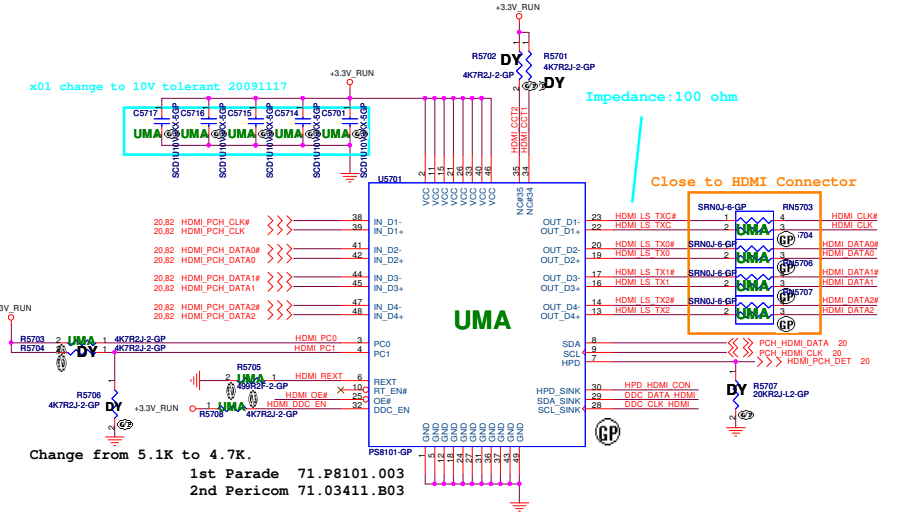
Title: LVDS_Switch

Size	Document Number	Rev
A3	Berry	X01

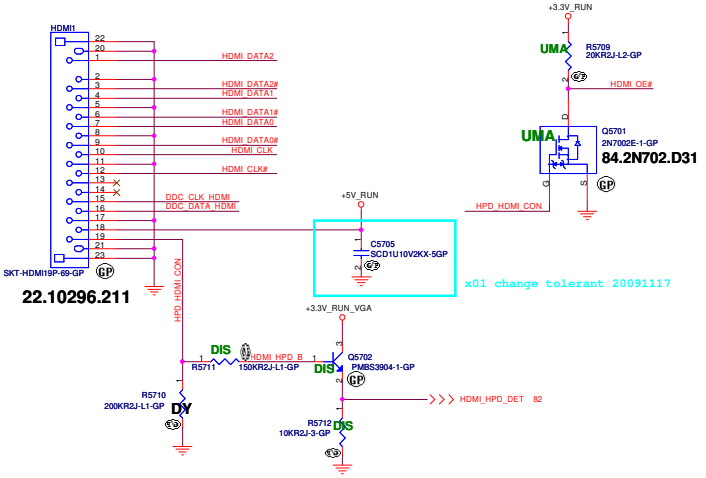
Date: Wednesday, February 24, 2010 Sheet 56 of 92

SSID = VIDEO

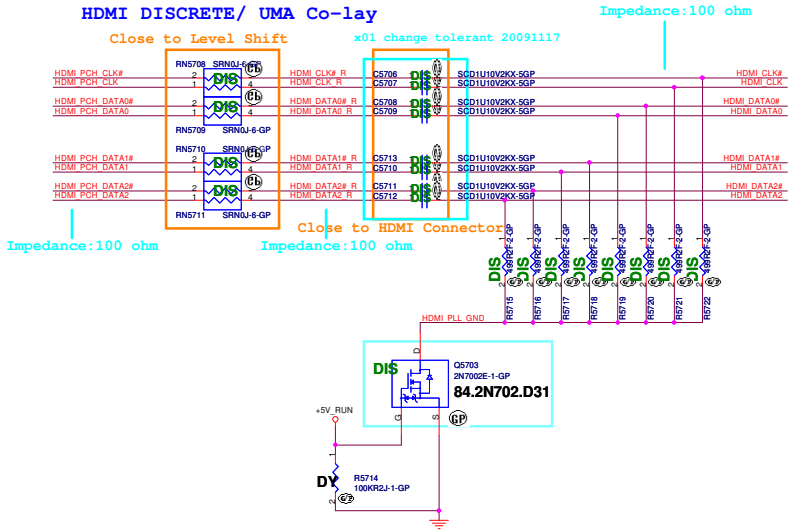
HDMI Level Shifter & CONNECTOR

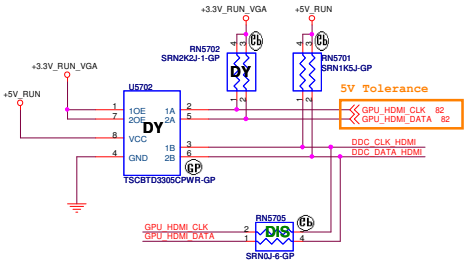


HDMI CONN



HDMI DISCRETE/ UMA Co-lay





<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

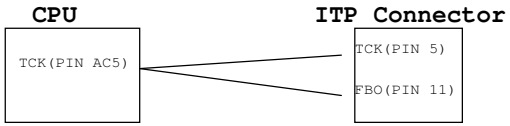
Size	Document Number	Rev
A2	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 57 of 92

SSID = User.Interface

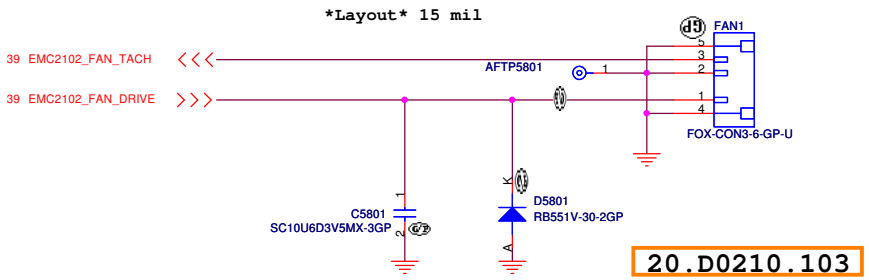
ITP Connector

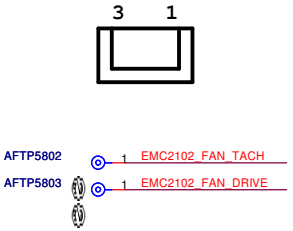
H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



SSID = Thermal

Fan Connector





20.D0210.103

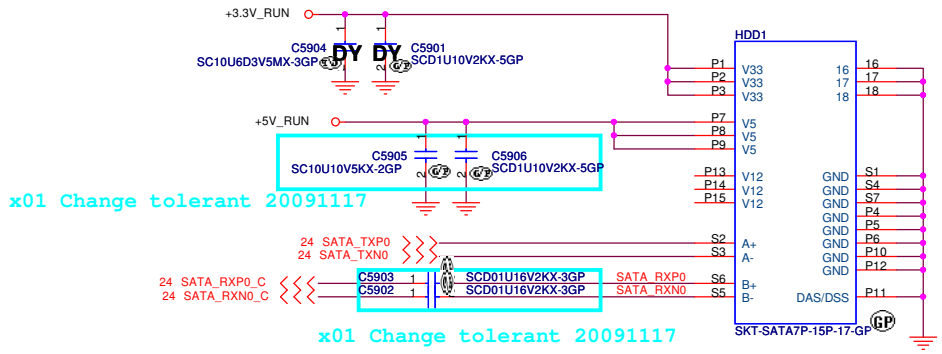
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ITP/Fan Connector		
Size: A3	Document Number: Berry	Rev: X01
Date: Wednesday, February 24, 2010	Sheet 58 of 92	

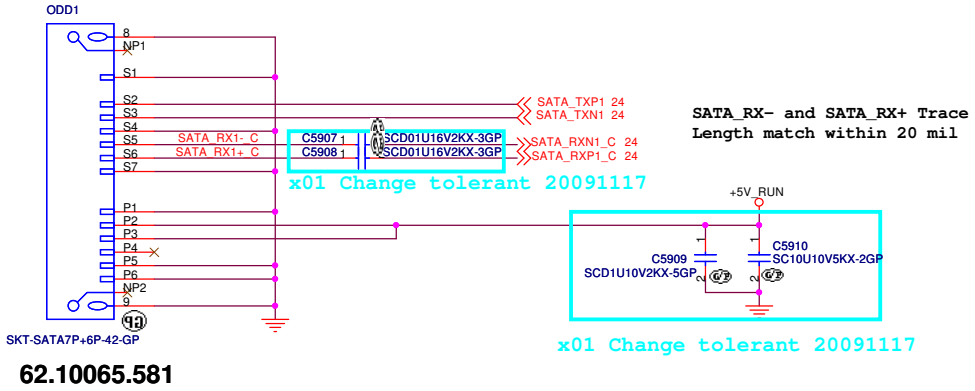
SSID = SATA

SATA HDD Connector



62.10065.C71

ODD Connector



62.10065.581

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size	Document Number	Rev
A3	Berry	X01

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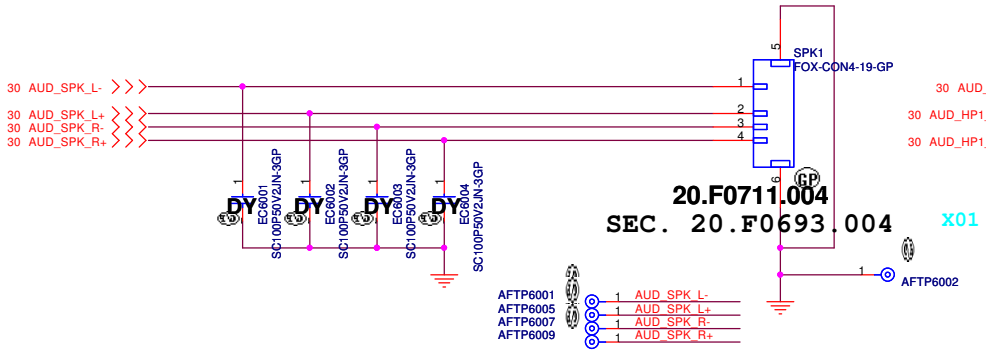
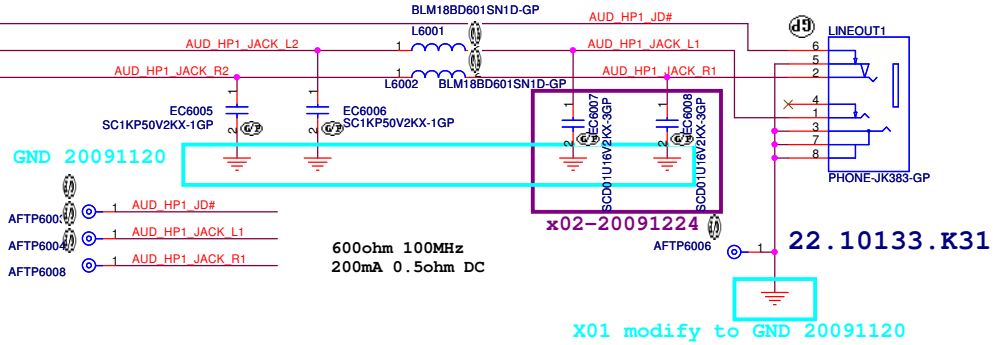
SSID = AUDIO

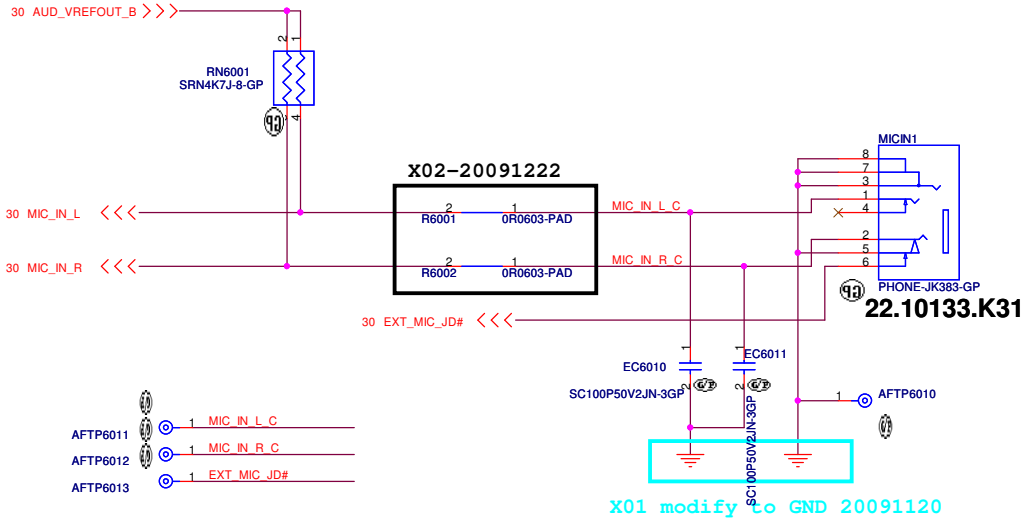
Speaker Connector



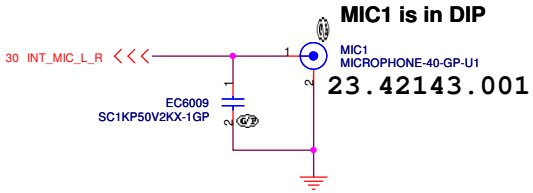
LINE1 OUT

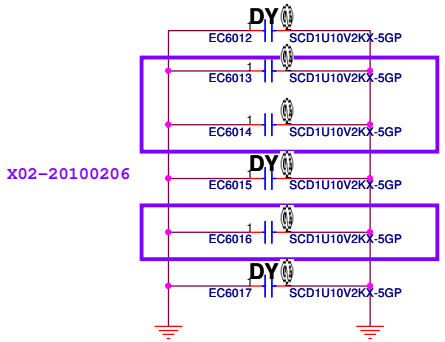


MIC IN



Internal Microphone





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack
Size: A3
Document Number: Berry
Rev: X01
Date: Wednesday, February 24, 2010
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

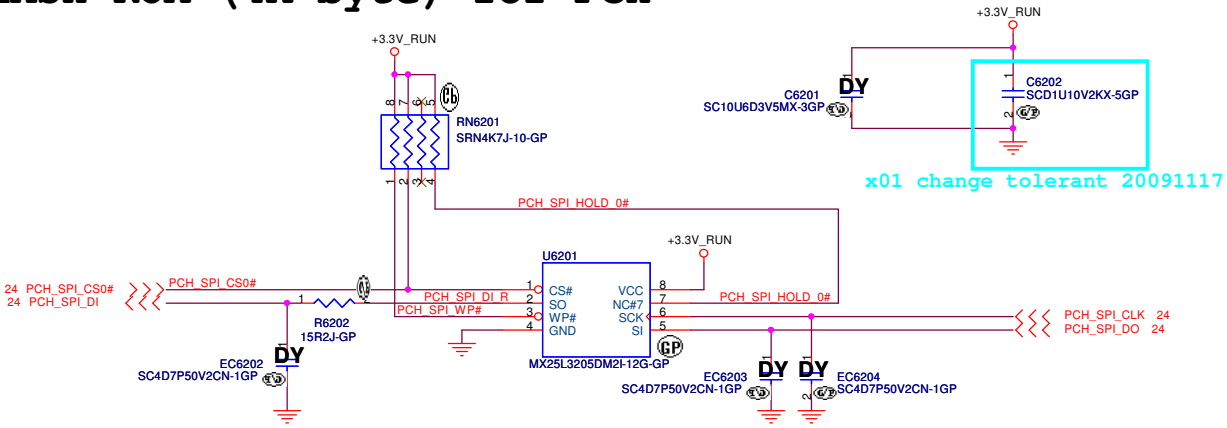
Title: Reserved

Size	Document Number	Rev
A3	Berry	X01

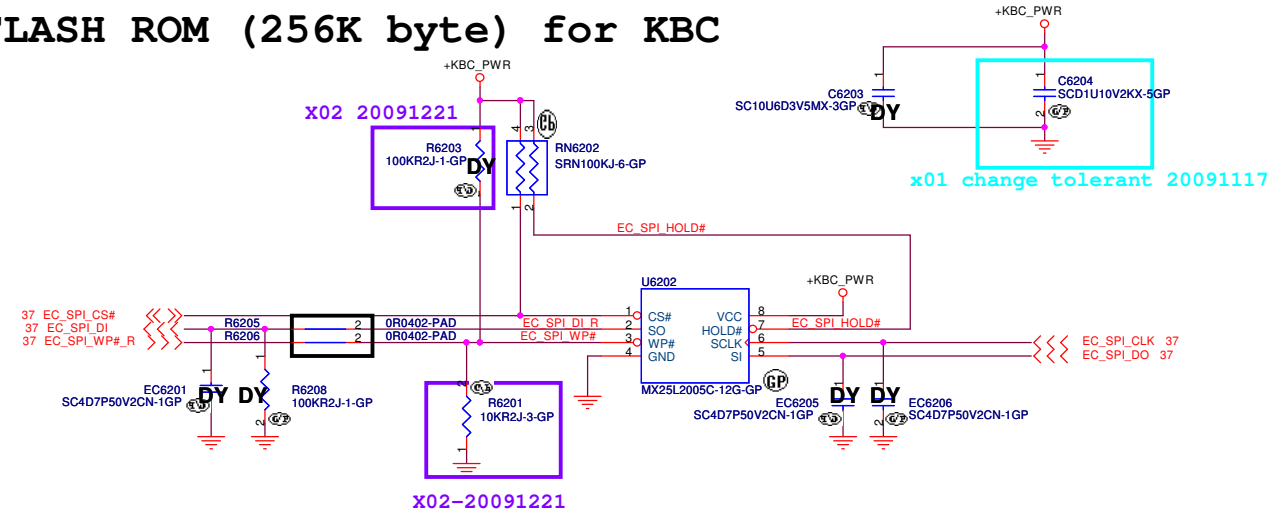
Date: Wednesday, February 24, 2010 Sheet 61 of 92

SSID = Flash.ROM

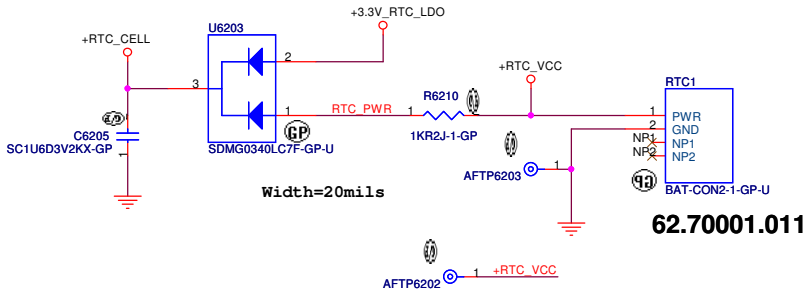
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

Size	Document Number	Rev
A3	Berry	X01

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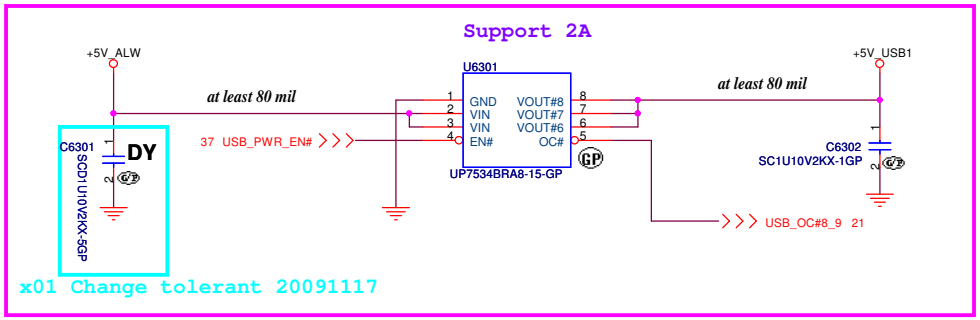
SSID = USB

IO Board USB Power

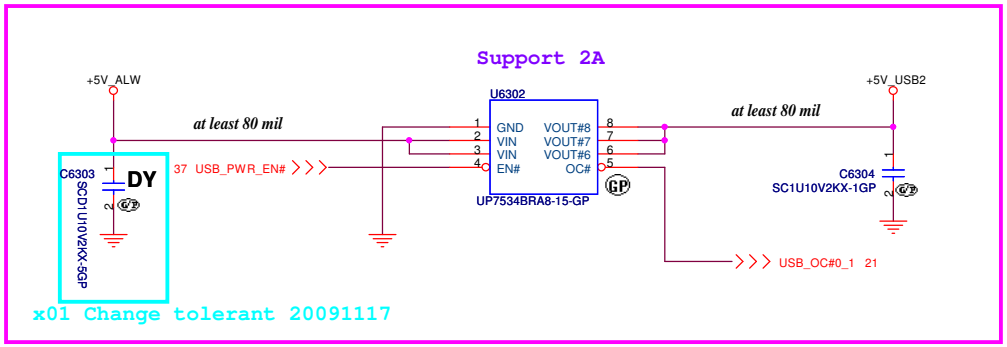
Close to I/O connector



USB POWER SW
Main UP7534BRA8-15 P/N:74.07534.079
SEC AP2101MPG-13 P/N: 74.02101.079

CRT Board USB Power

Close to CRT Board connector



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	USB Power SW	
Size	Document Number: Berry	Rev: X01
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A4	*Berry*	*X01*

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size	Document Number	Rev
A3	Berry	X01

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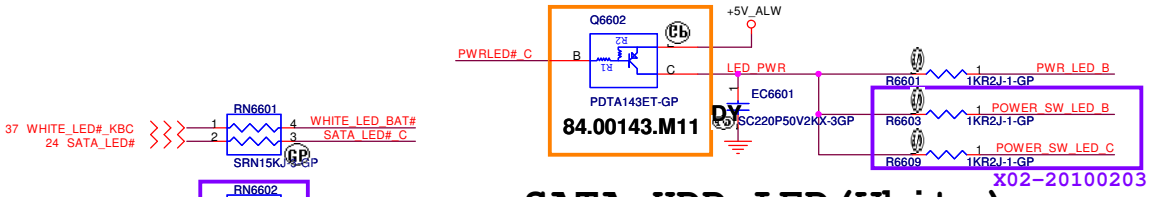
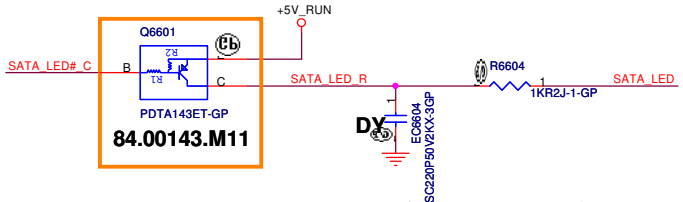
SSID = User Interface

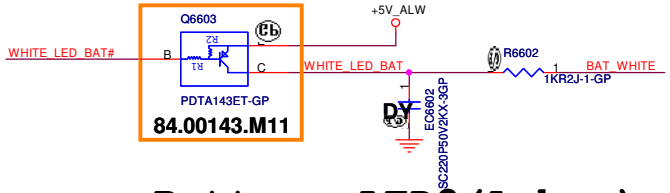
Power LED(White)

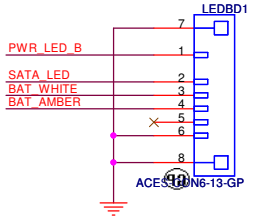


SATA HDD LED(White)

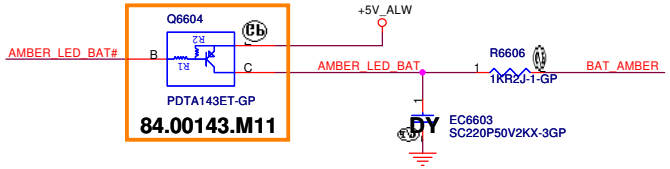


Battery LED1(White)

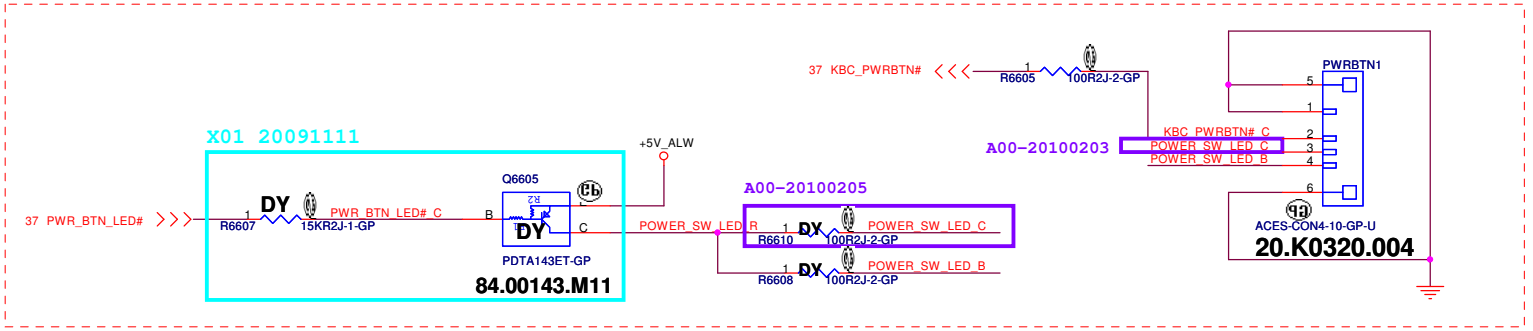




Battery LED2(Amber)



Power button LED(White)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size	Document Number	Rev
A3	Berry	X01

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

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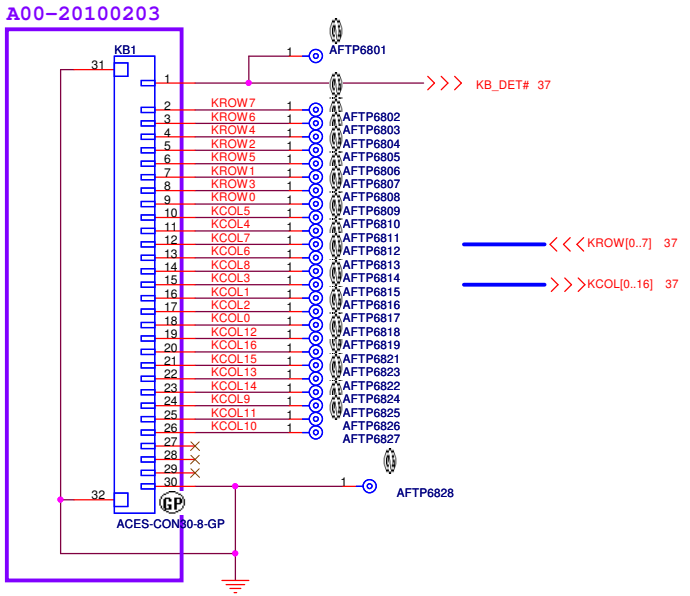
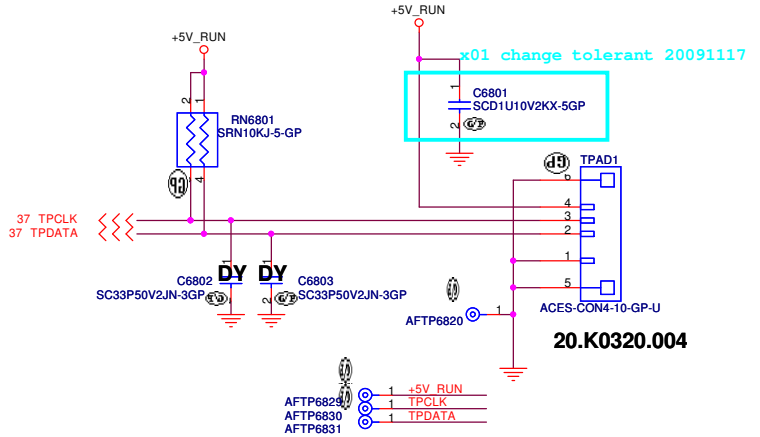
SSID = KBC

Internal KeyBoard Connector

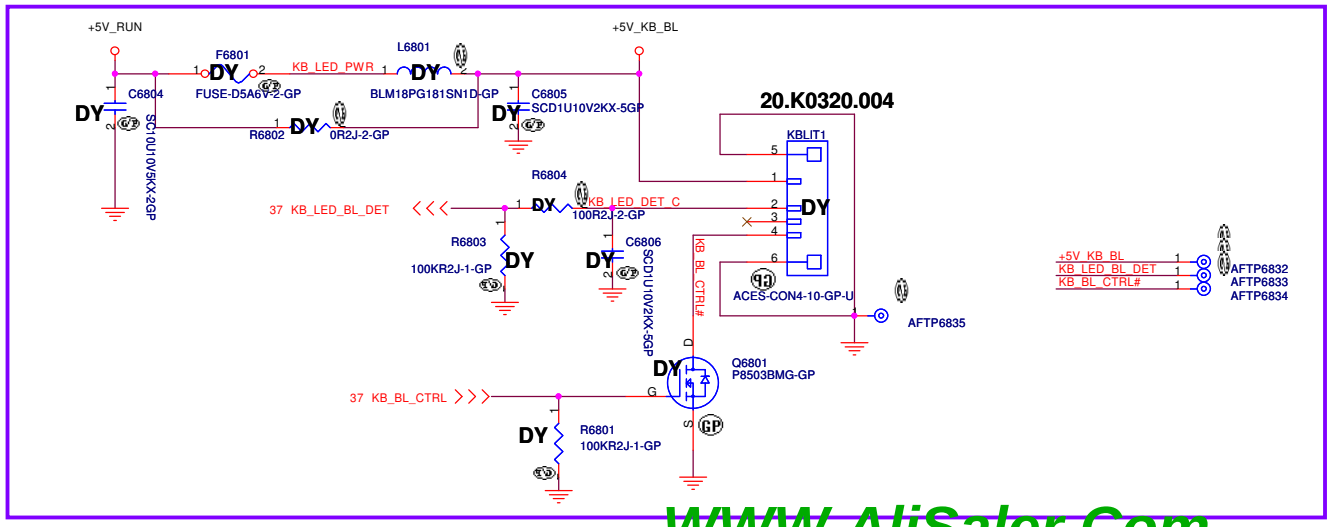


SSID = Touch.Pad

TouchPad Connector



KB Backlight Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

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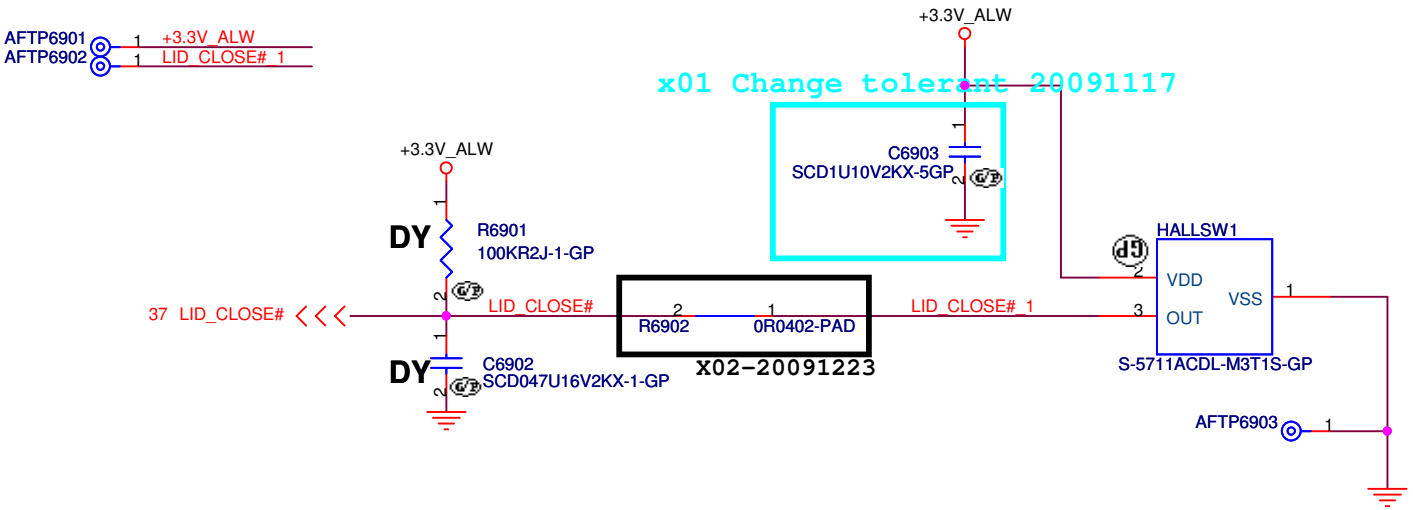

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

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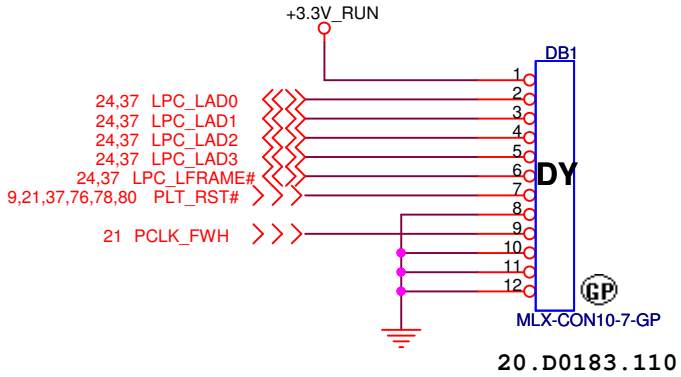

20.D0183.110

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	***Berry***	***X01***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size	Document Number	Rev
A4	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 71 of 92

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

Size	Document Number	Rev
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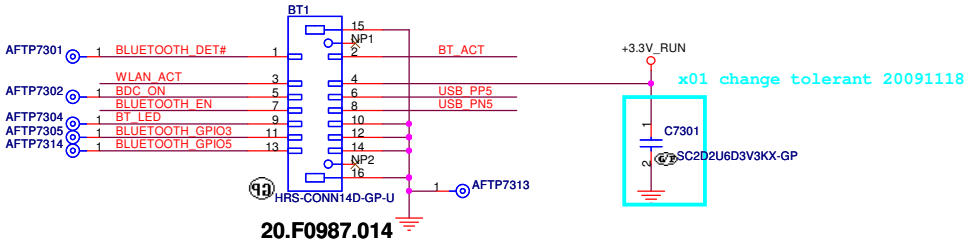
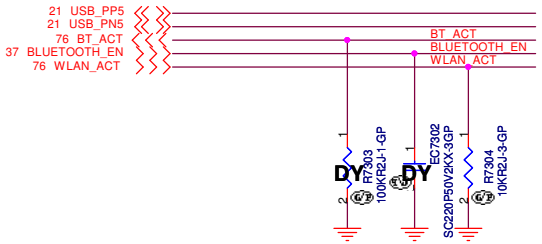
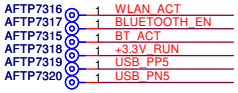
SSID = User.Interface

Bluetooth Module conn.



20.F0987.014





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth

Size	Document Number	Rev
A3	Berry	X01

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Berry | Rev: X01

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

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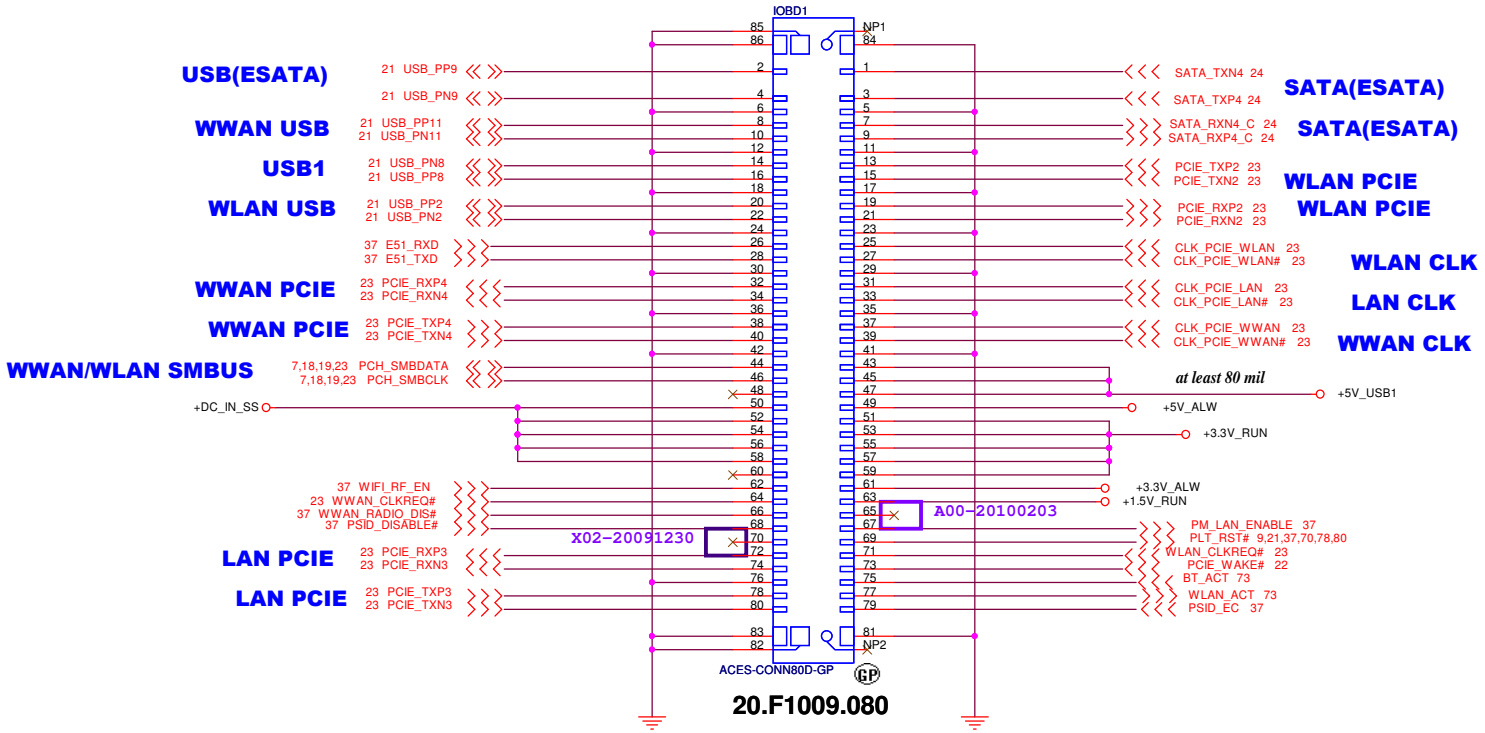
IO Board CONN 80 pin



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Berry | Rev: X01

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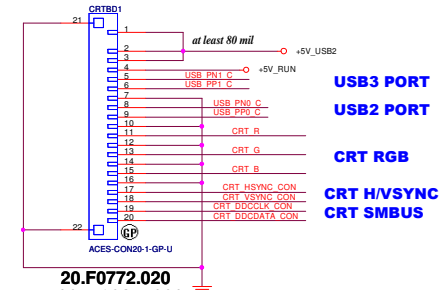
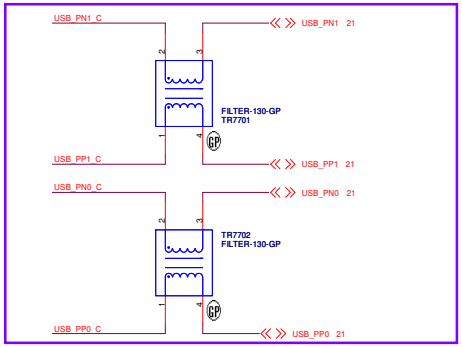
CRT Board Connector



20.F0772.020

SEC. 20.F1035.020

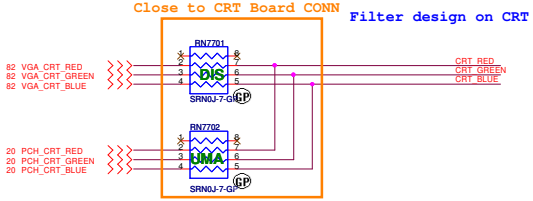
A00-20100120



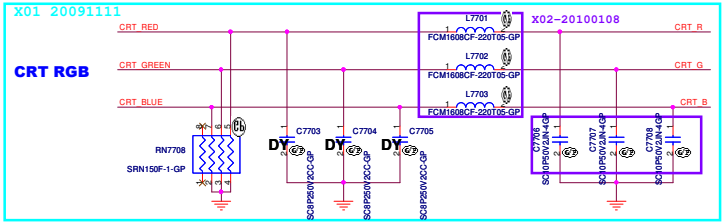
CRT RGB

Close to CRT Board CONN

Filter design on CRT Board

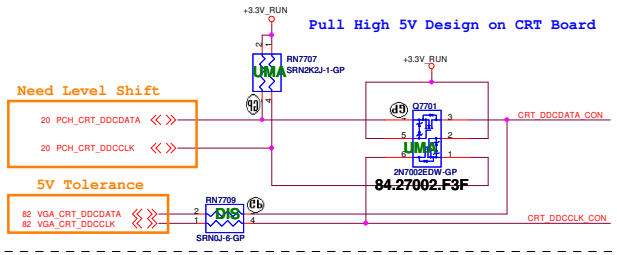


X01 20091111



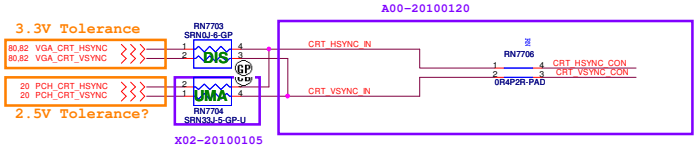
CRT DDCDATA & DDCCLK level shift

Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift

Close to CRT Board CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Board Connector

Size: A2 | Document Number: Berry | Rev: X01

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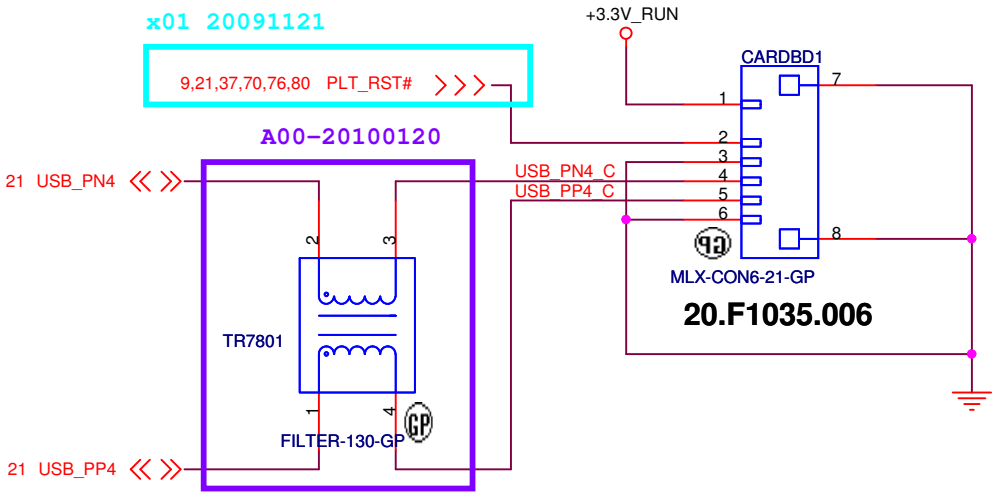
SSID = SDIO

Card Reader connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARD Reader CONN

Size	Document Number	Rev
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H1 HTE95BE95R29-R-5-GP
H2 HTE95BE95R29-R-5-GP
H3 HTE95BE95R29-R-5-GP
H4 HTE95BE95R29-R-5-GP
H5 HOLE256R111-GP
H6 HTE95BE95R29-R-5-GP
H7 HTE95BE95R29-R-5-GP
H8 HTE95BE95R29-R-5-GP
H9 HTE95BE95R29-R-5-GP

H10 HOLE335R115-GP
H11 HOLE256R111-GP

CPU Thermal module hole

HTML1 HOLE197R166-GP
HTML2 HOLE197R166-GP
HTML3 HOLE197R166-GP
DY DY DY

GPU Thermal module hole

HGPU1 STF237R117H83-1-GP

stand off

HBT1 STF237R117H123-GP

EMI Reserve

+PWR_SRC
X01 stuff 20091119
EC7901 EC7902 EC7904 EC7903 EC7905 EC7907 EC7909
EC7942 EC7940 EC7941 EC7939 EC7943 EC7938
SCD1U25V2KX-GP

+VGFXCORE_PWR_SRC
EC7906 DY SCD1U25V2KX-GP

+PWR_SRC_VTT
EC7911 SCD1U25V2KX-GP
X01 stuff 20091118

+PWR_SRC_1D5V
EC7916 DY SCD1U25V2KX-GP

EMI Reserve

SPR1 SPRING-58-GP DY

X01 RF Reserved-20091118

+PWR_SRC_1D5V 56pF*1
EC7908 DY SC56P50V2JN-2GP

+PWR_SRC 56pF*7
EC7912 EC7913 EC7917 EC7919 EC7920 EC7922 EC7925
SC56P50V2JN-2GP

+PWR_SRC +1.5V_SUS 0.1uF*2
EC7921 EC7933 SCD1U25V2KX-GP

X02-20100208

+1.05V_VTT
EC7923 DY
EC7924 EC7926 EC7927 UMA
SCD1U25V2KX-GP

+1.5V_SUS
EC7945 EC7929 EC7936 EC7944 DY
SCD1U25V2KX-GP

A00-20100204

+CPU_GFX_CORE 0.1uF*2
EC7946 EC7947 DY
SCD1U25V2KX-GP

+VGA_CORE 56pF*1
EC7928 DY SC56P50V2JN-2GP

+1.5V_SUS 56pF*3
EC7930 EC7931 EC7932 DY
SC56P50V2JN-2GP

+VCC_CORE 56pF*2
EC7934 UMA EC7935 DY
SC56P50V2JN-2GP

X02-20100209

+5V_RUN 56pF
EC7937 DY SC56P50V2JN-2GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Berry
Rev: X01
Date: Wednesday, February 24, 2010
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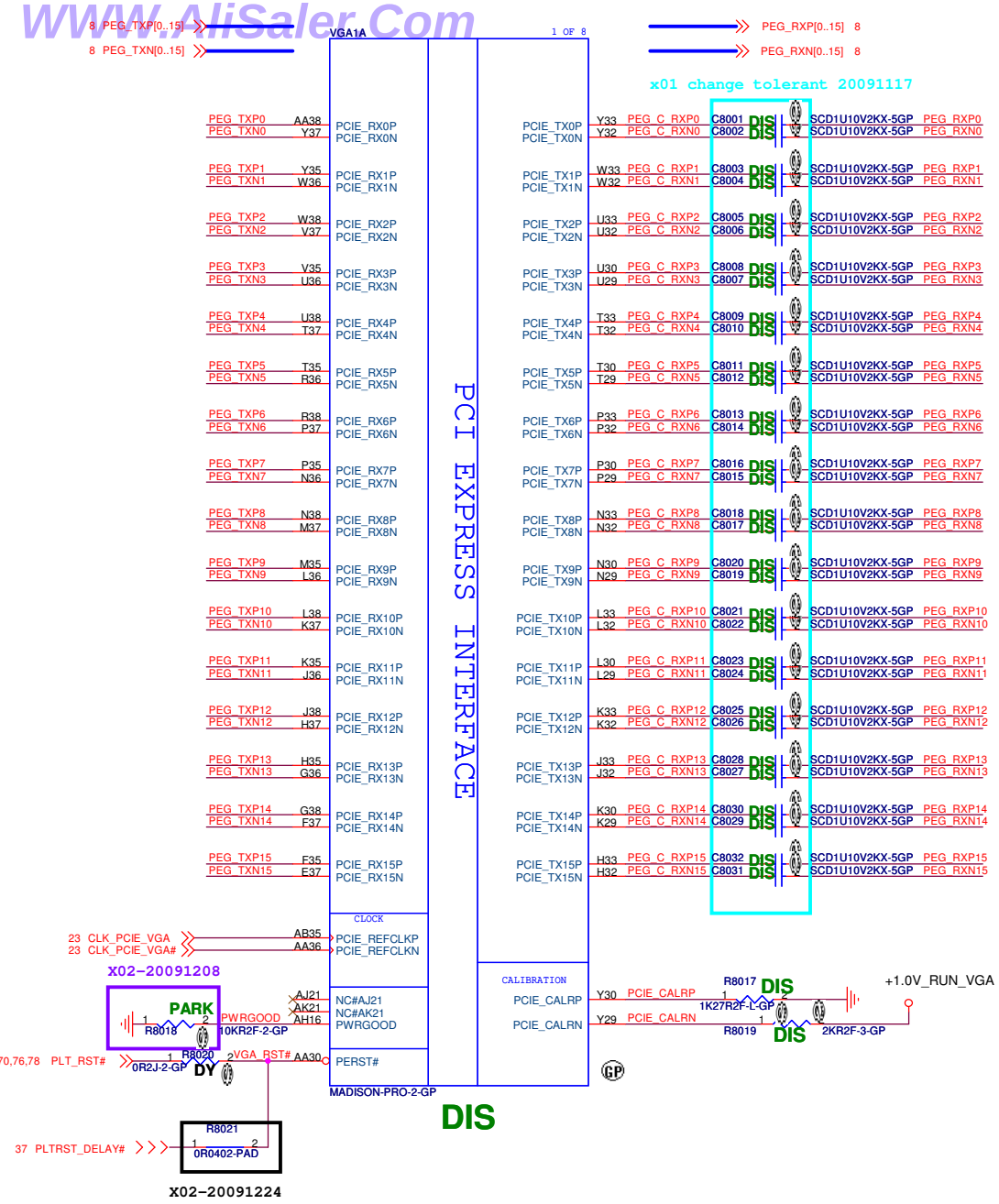


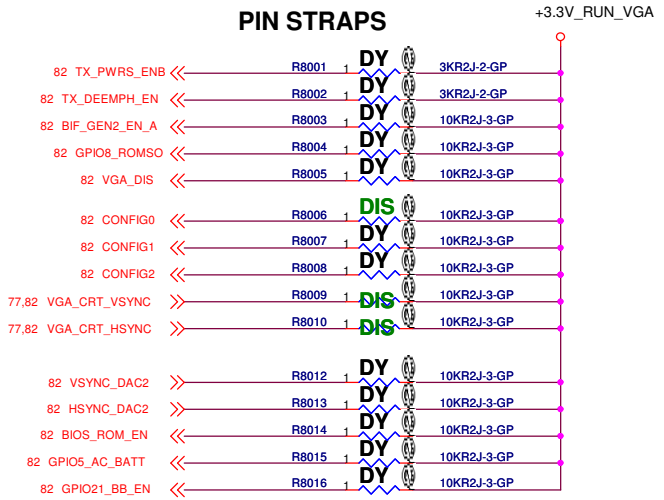
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
RESERVED	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
RESERVED	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

PIN STRAPS



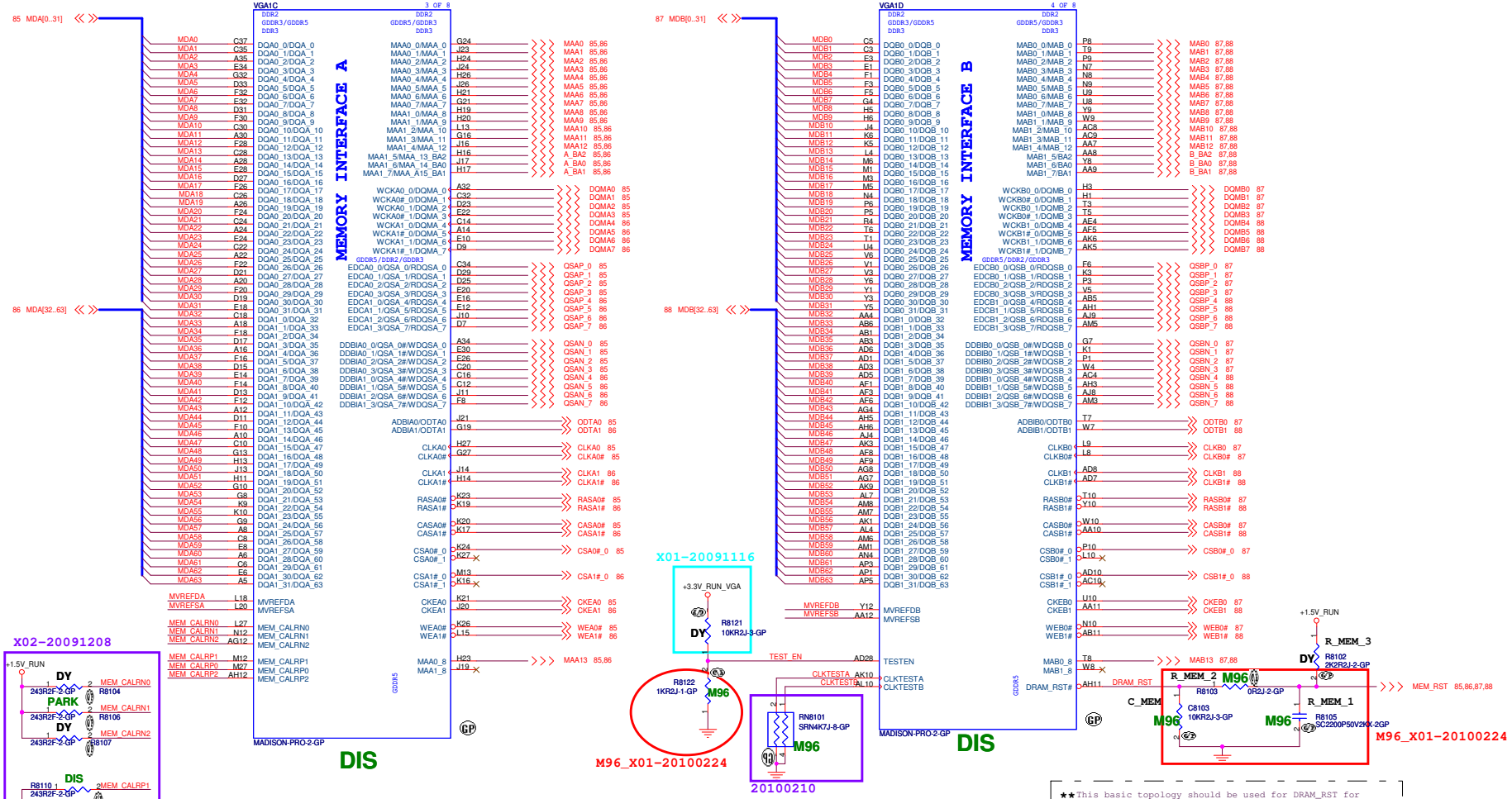
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size	Document Number	Rev
A3	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 80 of 92



Designator	For Mannhatton	For M96-M2/M92-M2
R_MEM_1	10K	2.2nF
R_MEM_2	51R	0R/Short
R_MEM_3	DNI	DNI
C_MEM	68pF	10K

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

	GDDR3	DDR3
MVDDQ	1.8V/1.5V	1.5V
Ra	40.2R	100R
Rb	100R	100R

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)
Size: C | Document Number: Berry | Rev: X01
Date: Wednesday, February 24, 2010 | Sheet 81 of 92

MEMORY ID Table

DVPDATA[0:3]	Description
0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646B-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16

DVPDATA[0:3] Default:Pull down

MEM_ID Control
X02-20091222

LVDS Interface

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

For new version no 27M

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

X02-20091210
Voltage Swing:1.8V

X02-20100104

X02-20100104

X01-20091116

X01-20091116

X02-20091222

X02 20091208

x01 Change tolerant 20091117

x01 Change tolerant 20091117

x01 Change tolerant 20091117

x01 Change tolerant 20091117

x01 Change tolerant 20091117

x01 Change tolerant 20091117

DDC1 channel for CRT

DDC2 channel for HDMI

DDC1/DDC2/DDC6 have 5V-tolerant

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

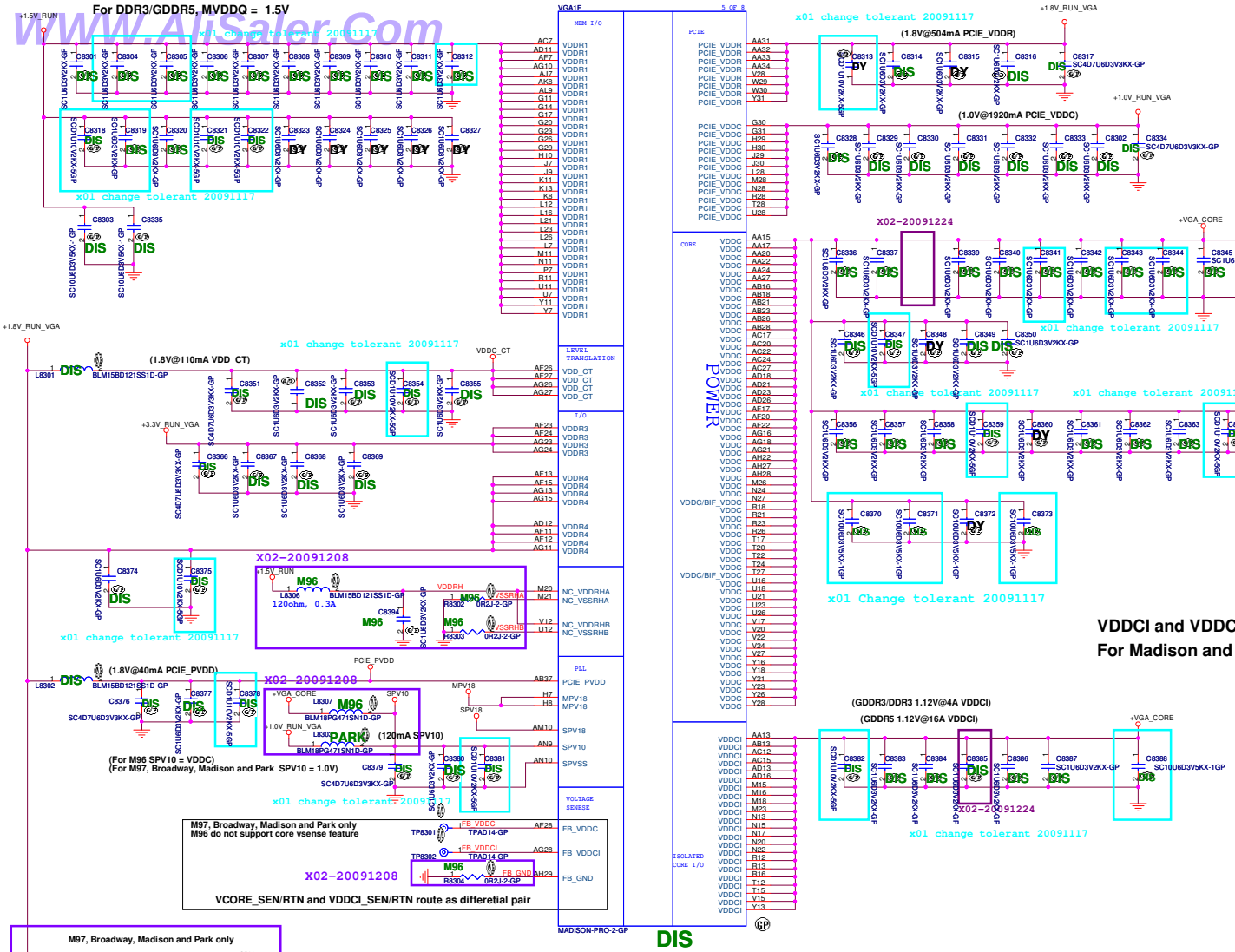
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 82 of 92



VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator

NOTE1:
Back Bias is not supported on M97, Broadway, Madison and Park
For the M96 Back Bias circuitry, refer to REF134

NOTE2:
FB_VDDC, FB_VDDCI and FB_GND are not support on M96

NOTE3:
M97 VDDC and VDDCI ball assignments are different from M96.
If M96 is populated on this design, VDDC and VDDCI will be shorted on the substrate.

NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

<Core Design>

Wistron Corporation
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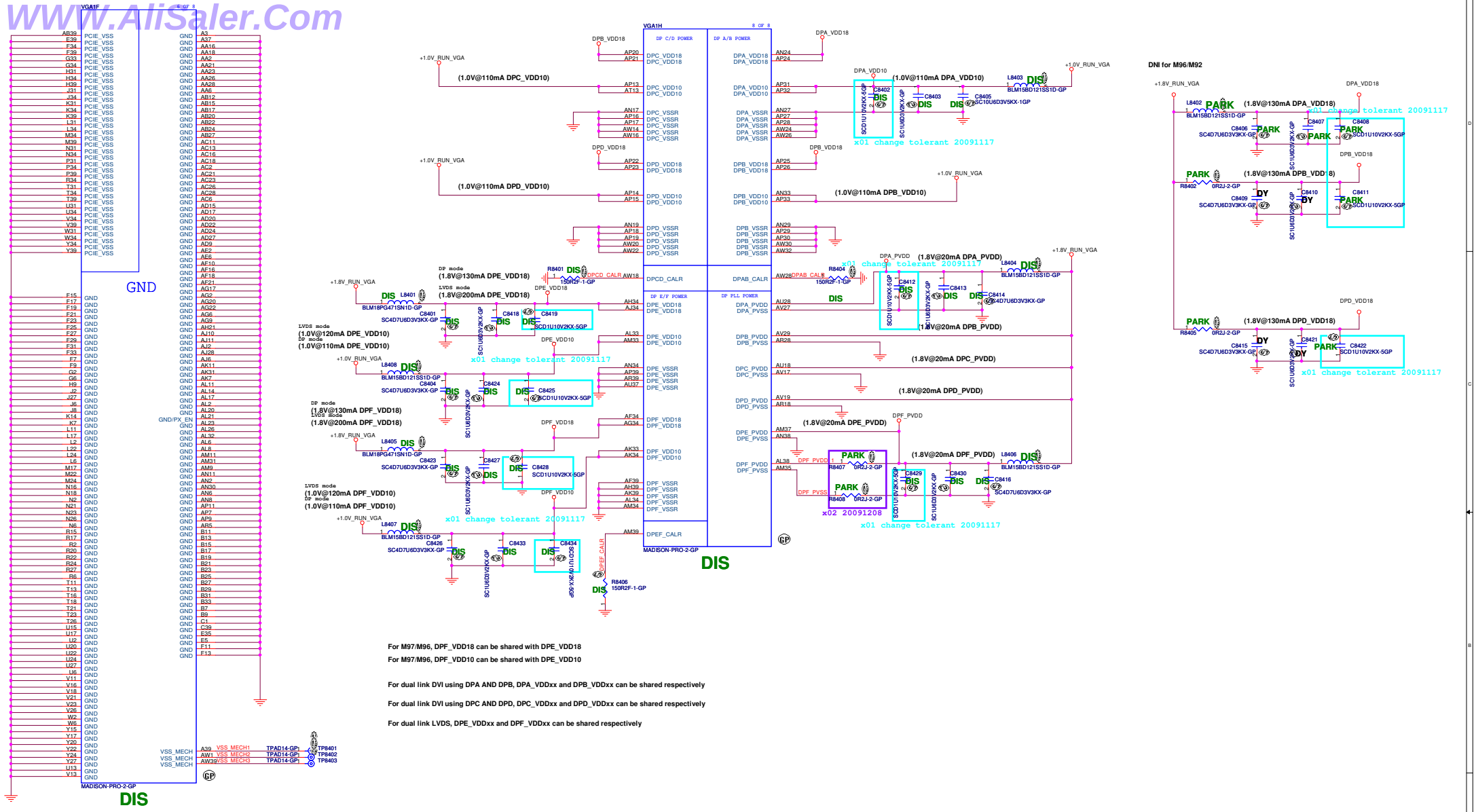
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_POWER(4/5)

Size: A2 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 83 of 92



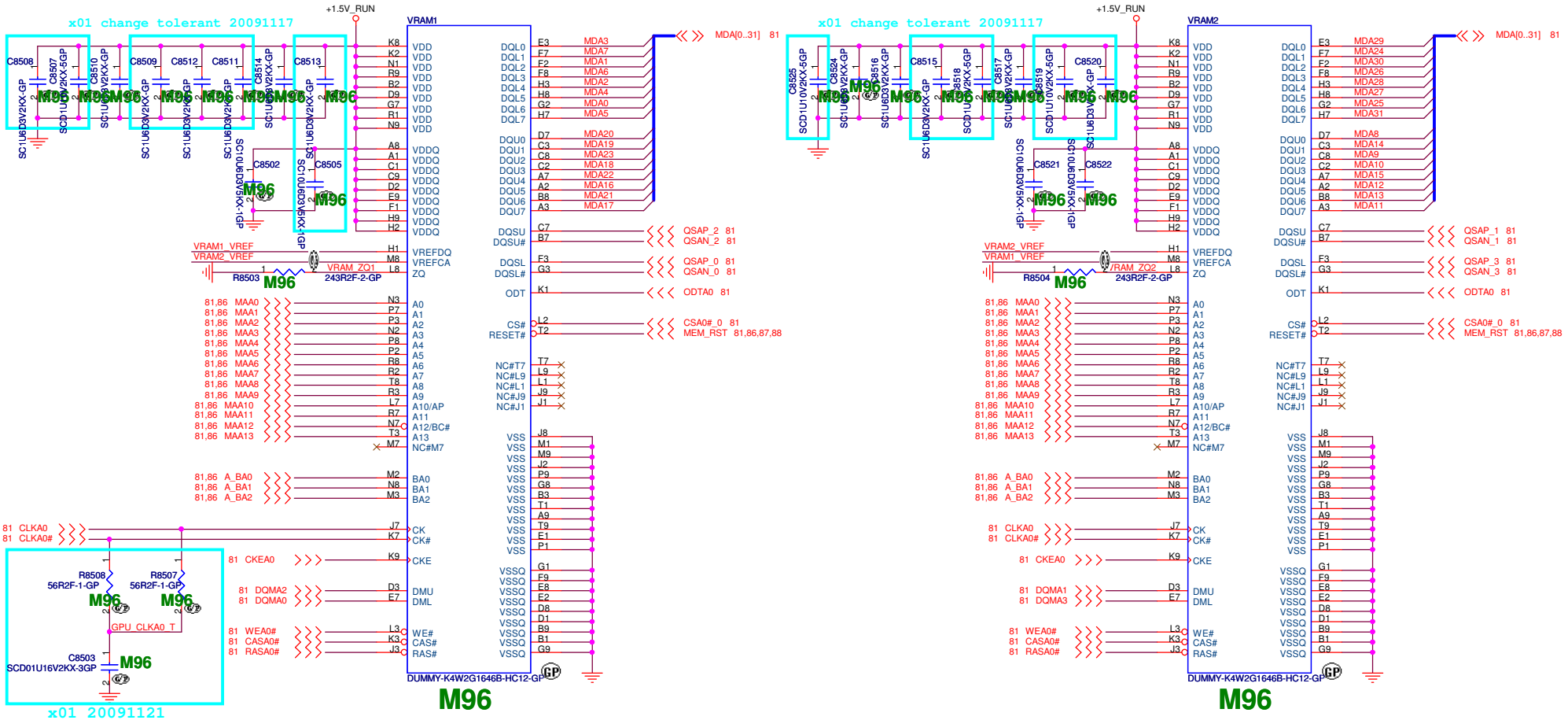
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size	Document Number	Rev
A2	Berry	X01

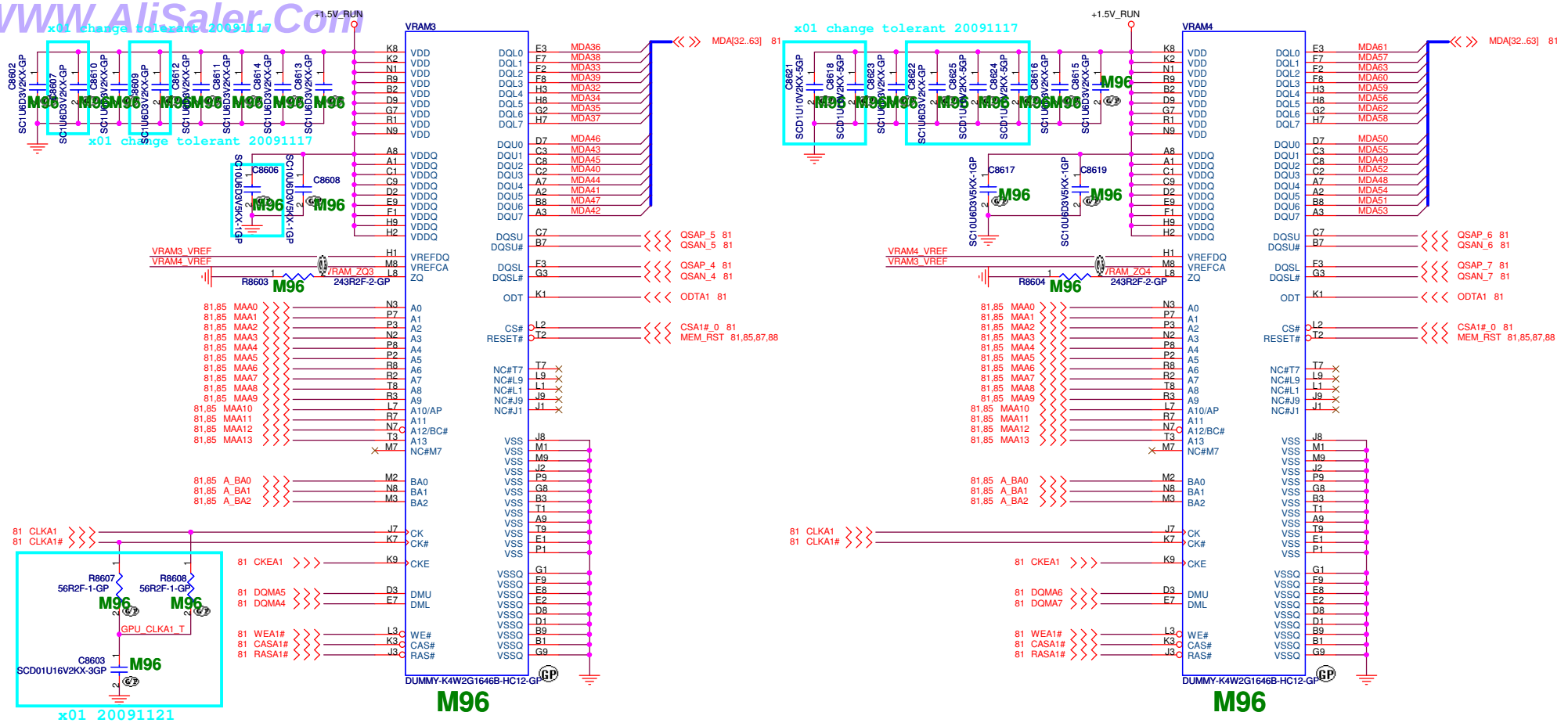
Date: Wednesday, February 24, 2010 Sheet 84 of 92

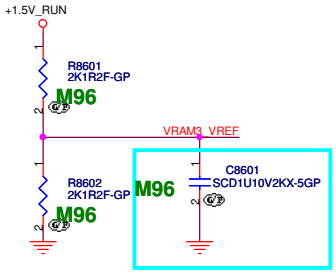


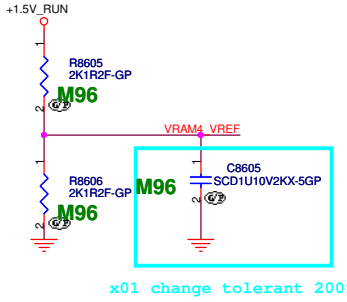
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)
Size: Custom | Document Number: Berry | Rev: X01
Date: Wednesday, February 24, 2010 | Sheet 85 of 92







<Core Design>

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Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 86 of 92

x01 change tolerant 20091117

+1.5V_RUN

VRAM5

C8702 SC1U6D3V2KX-GP
C8707 SCD1U10V2KX-5GP
C8710 SC1U6D3V2KX-GP
C8709 SCD1U10V2KX-5GP
C87011 SC1U6D3V2KX-GP
C87012 SC1U6D3V2KX-GP
C87013 SC1U6D3V2KX-GP
C8714 SC1U6D3V2KX-GP
C8706 SC10U6D3V5KX-1GP
C8708 SC10U6D3V5KX-1GP

K8 K2 N1 R9 B2 D9 G7 R1 N9 VDD
A8 A1 C1 C9 D2 E9 F1 H9 H2 VDDQ
H1 VREFDQ
M8 VREFCA
L8 ZQ

VRAM5_VREF
VRAM6_VREF
R8704 DIS
VRAM_ZQ5 243R2F-2-GP

DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
E3 F7 F2 F8 H3 H8 G2 H7
MDB14 MDB13 MDB12 MDB15 MDB11 MDB8 MDB9 MDB10

DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
D7 C3 C8 C2 A7 A2 B8 A3
MDB26 MDB27 MDB30 MDB24 MDB31 MDB25 MDB29 MDB28

DQSU DQSU#
C7 B7
QSBP_3 81
QSBN_3 81

DQSL DQSL#
F3 G3
QSBP_1 81
QSBN_1 81

ODT
K1
ODTB0 81

CS# RESET#
L2 T2
CSB0#_0 81
MEM_RST 81,85,86,88

NC#T7 NC#L9 NC#L1 NC#J9 NC#J1
T7 L9 L1 J9 J1

VSS
J8 M1 M9 J2 P9 G8 B3 T1 A9 T9 E1 P1

VSSQ
G1 F9 E8 F2 D8 D1 B9 B1 G9

81,88 MAB0
81,88 MAB1
81,88 MAB2
81,88 MAB3
81,88 MAB4
81,88 MAB5
81,88 MAB6
81,88 MAB7
81,88 MAB8
81,88 MAB9
81,88 MAB10
81,88 MAB11
81,88 MAB12
81,88 MAB13
N3 P7 P3 N2 P8 P2 R8 R2 T8 R3 L7 R7 N7 T3 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 NC#M7

81,88 B_BA0
81,88 B_BA1
81,88 B_BA2
M2 N8 M3
BA0 BA1 BA2

20090902

81 CLKB0
81 CLKB0#
J7 K7
CK CK#

R8707 56R2F-1-GP DIS
R8708 56R2F-1-GP DIS
GPU_CLKB0_T
C8703 SCD01U16V2KX-3GP DIS

81 CKEB0
K9
CKE

81 DQMB3
81 DQMB1
D3 E7
DMU DML

81 WEB0#
81 CASB0#
81 RASB0#
L3 K3 J3
WE# CAS# RAS#

DUMMY-K4W2G1646B-HC12-GP

x01 20091121

DIS

x01 change tolerant 20091117

+1.5V_RUN

VRAM6

C8717 SC1U6D3V2KX-GP
C8715 SC1U6D3V2KX-GP
C8720 SC1U6D3V2KX-GP
C8722 SC1U6D3V2KX-GP
C8723 SC1U6D3V2KX-GP
C8721 SCD1U10V2KX-5GP
C8724 SC1U6D3V2KX-GP
C8725 SCD1U10V2KX-5GP
C8718 SC10U6D3V5KX-1GP
C8719 SC10U6D3V5KX-1GP

DY

K8 K2 N1 R9 B2 D9 G7 R1 N9 VDD
A8 A1 C1 C9 D2 E9 F1 H9 H2 VDDQ
H1 VREFDQ
M8 VREFCA
L8 ZQ

VRAM6_VREF
VRAM5_VREF
R8706 DIS
VRAM_ZQ6 243R2F-2-GP

DQL0 DQL1 DQL2 DQL3 DQL4 DQL5 DQL6 DQL7
E3 F7 F2 F8 H3 H8 G2 H7
MDB16 MDB18 MDB20 MDB19 MDB22 MDB17 MDB23 MDB21

DQU0 DQU1 DQU2 DQU3 DQU4 DQU5 DQU6 DQU7
D7 C3 C8 C2 A7 A2 B8 A3
MDB1 MDB5 MDB2 MDB4 MDB3 MDB7 MDB0 MDB6

DQSU DQSU#
C7 B7
QSBP_0 81
QSBN_0 81

DQSL DQSL#
F3 G3
QSBP_2 81
QSBN_2 81

ODT
K1
ODTB0 81

CS# RESET#
L2 T2
CSB0#_0 81
MEM_RST 81,85,86,88

NC#T7 NC#L9 NC#L1 NC#J9 NC#J1
T7 L9 L1 J9 J1

VSS
J8 M1 M9 J2 P9 G8 B3 T1 A9 T9 E1 P1

VSSQ
G1 F9 E8 F2 D8 D1 B9 B1 G9

81,88 MAB0
81,88 MAB1
81,88 MAB2
81,88 MAB3
81,88 MAB4
81,88 MAB5
81,88 MAB6
81,88 MAB7
81,88 MAB8
81,88 MAB9
81,88 MAB10
81,88 MAB11
81,88 MAB12
81,88 MAB13
N3 P7 P3 N2 P8 P2 R8 R2 T8 R3 L7 R7 N7 T3 M7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 NC#M7

81,88 B_BA0
81,88 B_BA1
81,88 B_BA2
M2 N8 M3
BA0 BA1 BA2

81 CLKB0
81 CLKB0#
J7 K7
CK CK#

81 CKEB0
K9
CKE

81 DQMB0
81 DQMB2
D3 E7
DMU DML

81 WEB0#
81 CASB0#
81 RASB0#
L3 K3 J3
WE# CAS# RAS#

DUMMY-K4W2G1646B-HC12-GP

DIS

+1.5V_RUN

R8701 2K1R2F-GP DIS
VRAM5_VREF
R8702 2K1R2F-GP DIS
C8701 SCD1U10V2KX-5GP DIS

x01 change tolerant 20091117

+1.5V_RUN

R8703 2K1R2F-GP DIS
VRAM6_VREF
R8705 2K1R2F-GP DIS
C8705 SCD1U10V2KX-5GP DIS

x01 change tolerant 20091117

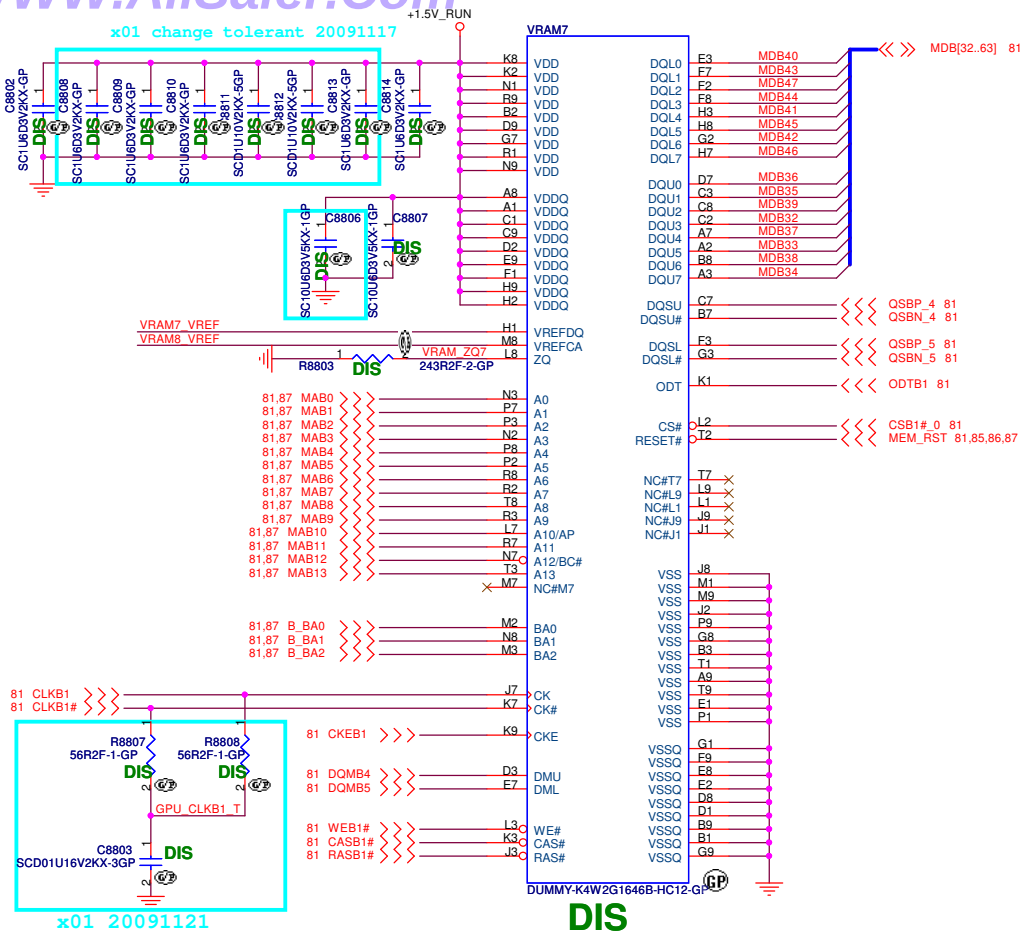
<Core Design>

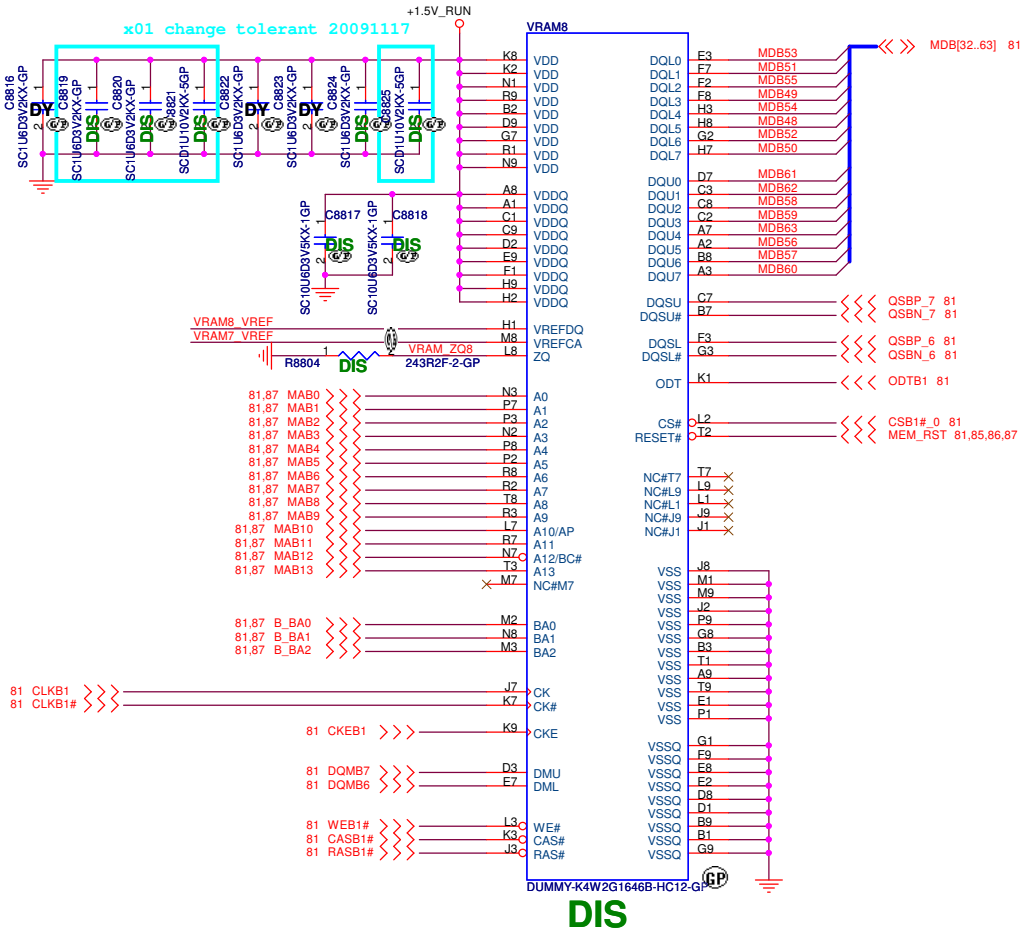
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

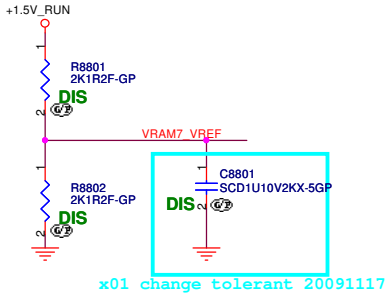
Title: GPU-VRAM5,6 (3/4)

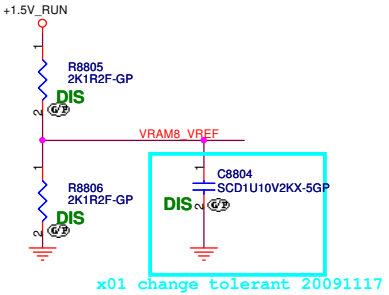
Size: A3 | Document Number: Berry | Rev: X01

Date: Wednesday, February 24, 2010 | Sheet 87 of 92









<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size	Document Number	Rev
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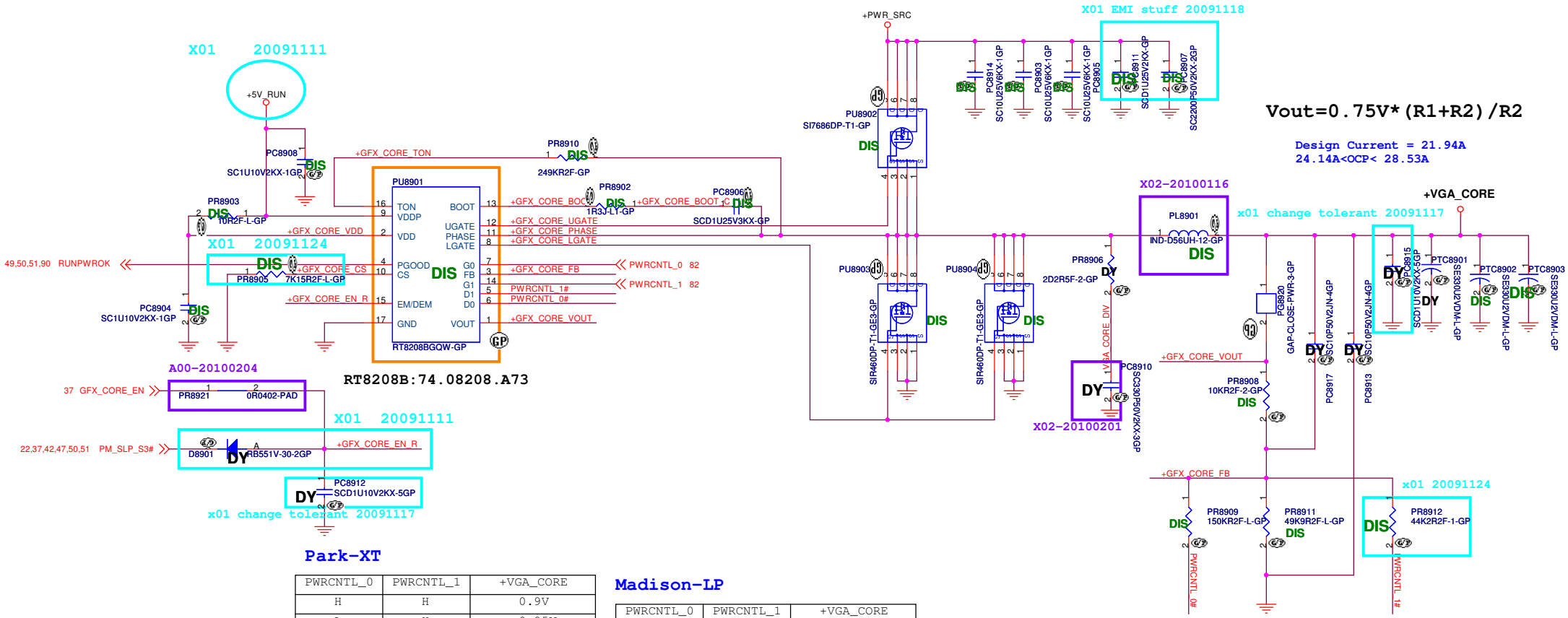
Date: Wednesday, February 24, 2010 Sheet 88 of 92

SSID = Video.PWR.Regulator

RT8208BGQW for +VGA_CORE



Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

Park-XT

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.12V

Madison-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V

A00-20100224

M96-LP

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.0V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: RT8208B_+VGA_CORE
Size: A3
Document Number: Arsenal DJ1 Discrete
Rev: X01
Date: Wednesday, February 24, 2010
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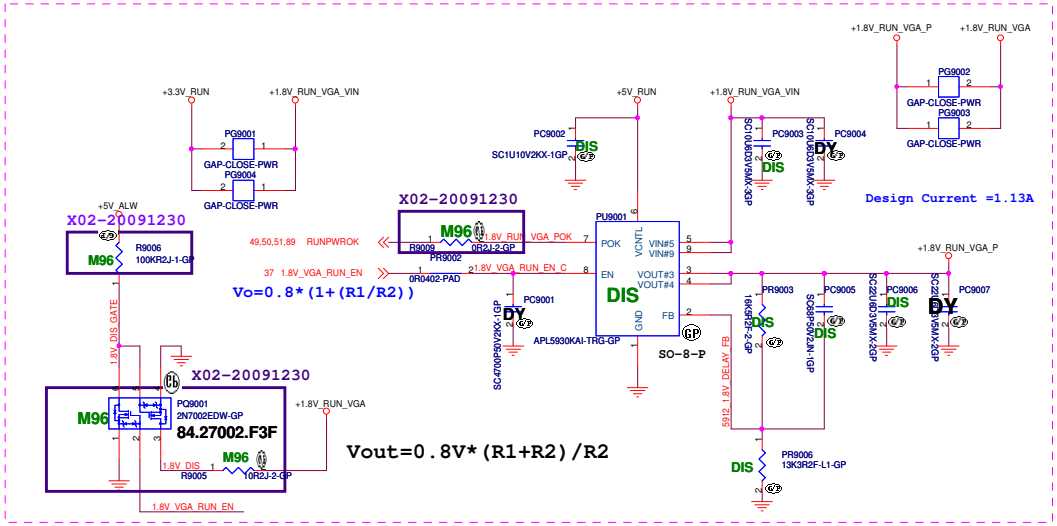
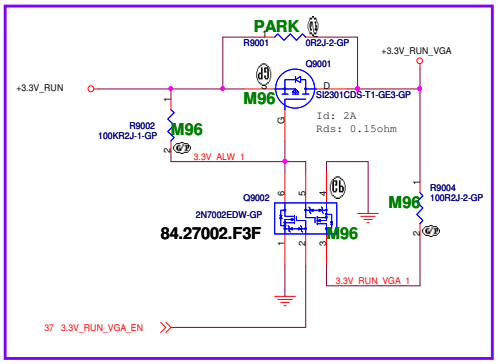
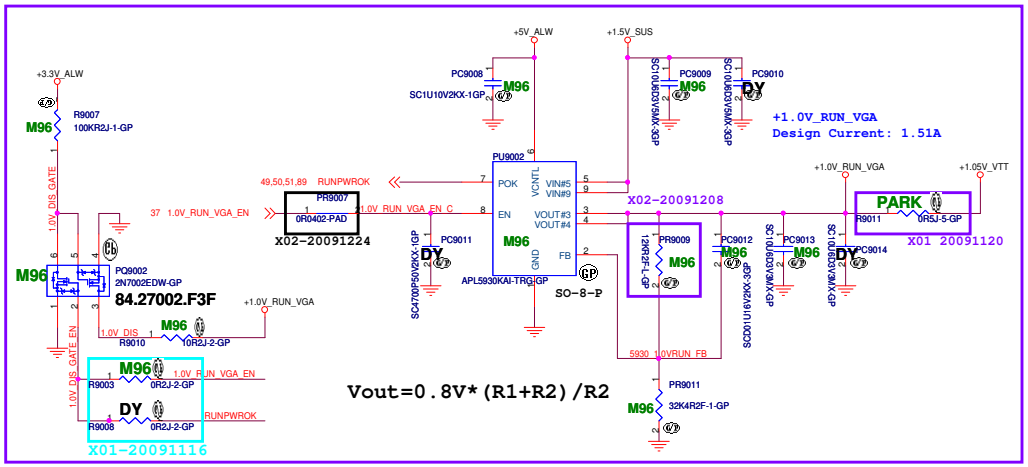
APL5930 for +1.8V_RUN_VGA



+3.3V_RUN_VGA



APL5930KAI for +1.0V_RUN_VGA



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DISCRETE VGA POWER

Size	Document Number	Rev
C	Berry	X01

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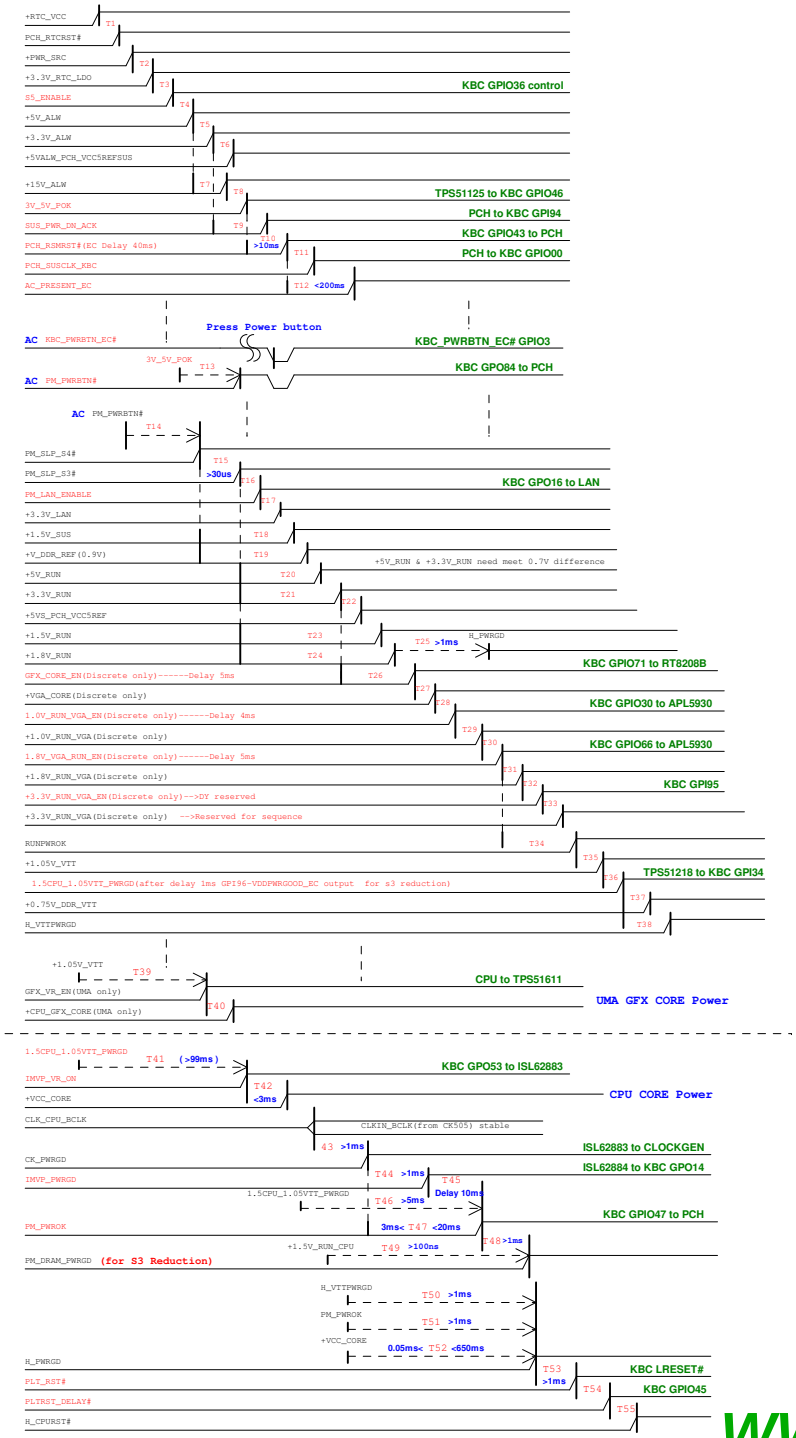
D15 Intel-Power Up Sequence

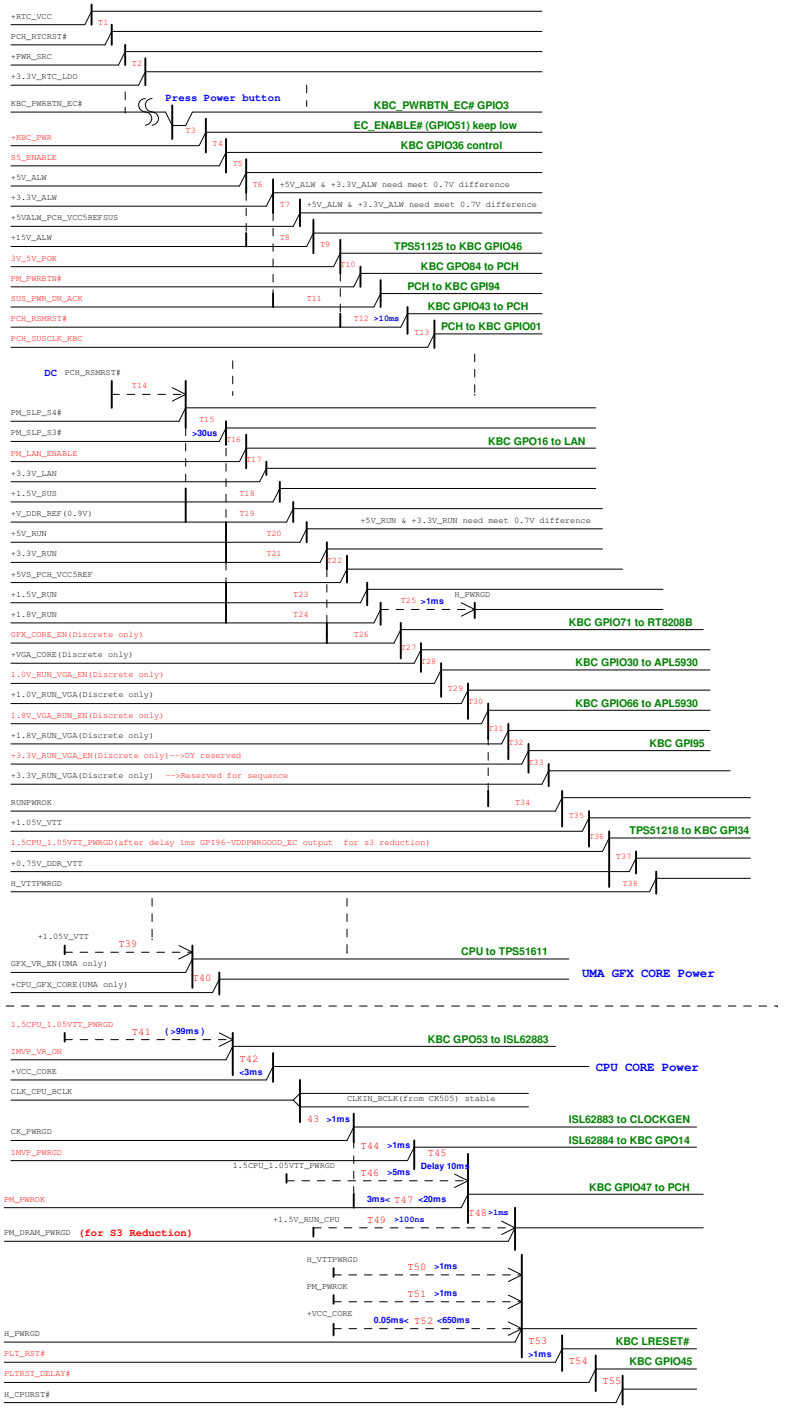
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: Power Sequence

Size	Document Number	Rev
A1	Berry	X01
Date: Wednesday, February 24, 2010	Sheet 91 of 96	

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

Size	Document Number	Rev
A3	Berry	X01

Date: Wednesday, February 24, 2010 Sheet 92 of 92