LB46E Block Diagram

Project code: 91.4HK01.A01
PCB P/N :
REVISION : 10307-sc

CLK GEN. 3

Mobile CPU
Penryn 479
4, 5

THERMAL EMC2102
27

HOST BUS 667/800/1067MHz@1.05V

DDR3 DIMM1
800/1066 MHz
16

DDR3 DIMM2
800/1066 MHz
17

800/1066MHz

800/1066MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

UMA

CRT 19

LCD 18

DIS

PCIE x 16

nVIDIA
N11M-OP1
46~51

CRT 19

LCD 18

4X128MB
GDDRIII 52,53

X4 DMI
400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
12,13,14,15

Line Out
(NO SPDIF)
25

MIC In
25

Internal MIC
25

Codec
CX20671
25

AZALIA

25
INT.SPKR

PCIex1

LAN
RTL8111E 23

TXFM 24

RJ45

PCIex1

Mini Card
Kedron a/b/g/n
26

LPC BUS

Camera
(USB) 18

USB

HDD SATA 20

SATA

USB
3 Port 22

USB

ODD SATA 21

SATA

KBC
KBC773L
28

BIOS
Winbond
W25X16
16M Bits
29

LPC
DEBUG
CONN 34

Touch
Pad 30

INT.
KB 30

Power Board
31

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC
TPS51125 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
TPS51218/RT9025 39

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S0

TPS51116 38

DCBATOUT	1D5V_S3

TPS51116 38

1D5V_S3	0D75V_S0

CPU DC/DC
ISL6266A 36

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER
BQ24745 41

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title: 1 BLOCK DIAGRAM
Size: A3 | Document Number: LB46E | Rev: SA
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

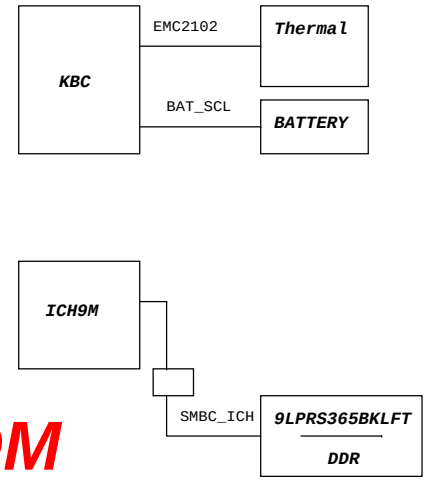
PCIE Routing

LANE1	RTL8111E
LANE2	MiniCard WLAN
LANE3	*NC*
LANE4	*NC*
LANE5	*NC*
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB3*
2	*NC*
3	*MINIC1*
4	*WEBCAM*
5	*NC*
6	*NC*
7	*NC*
8	*NC*
9	*USB2*
10	*NC*
11	*NC*

SMBus



<Core Design>

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Title: **Reference**

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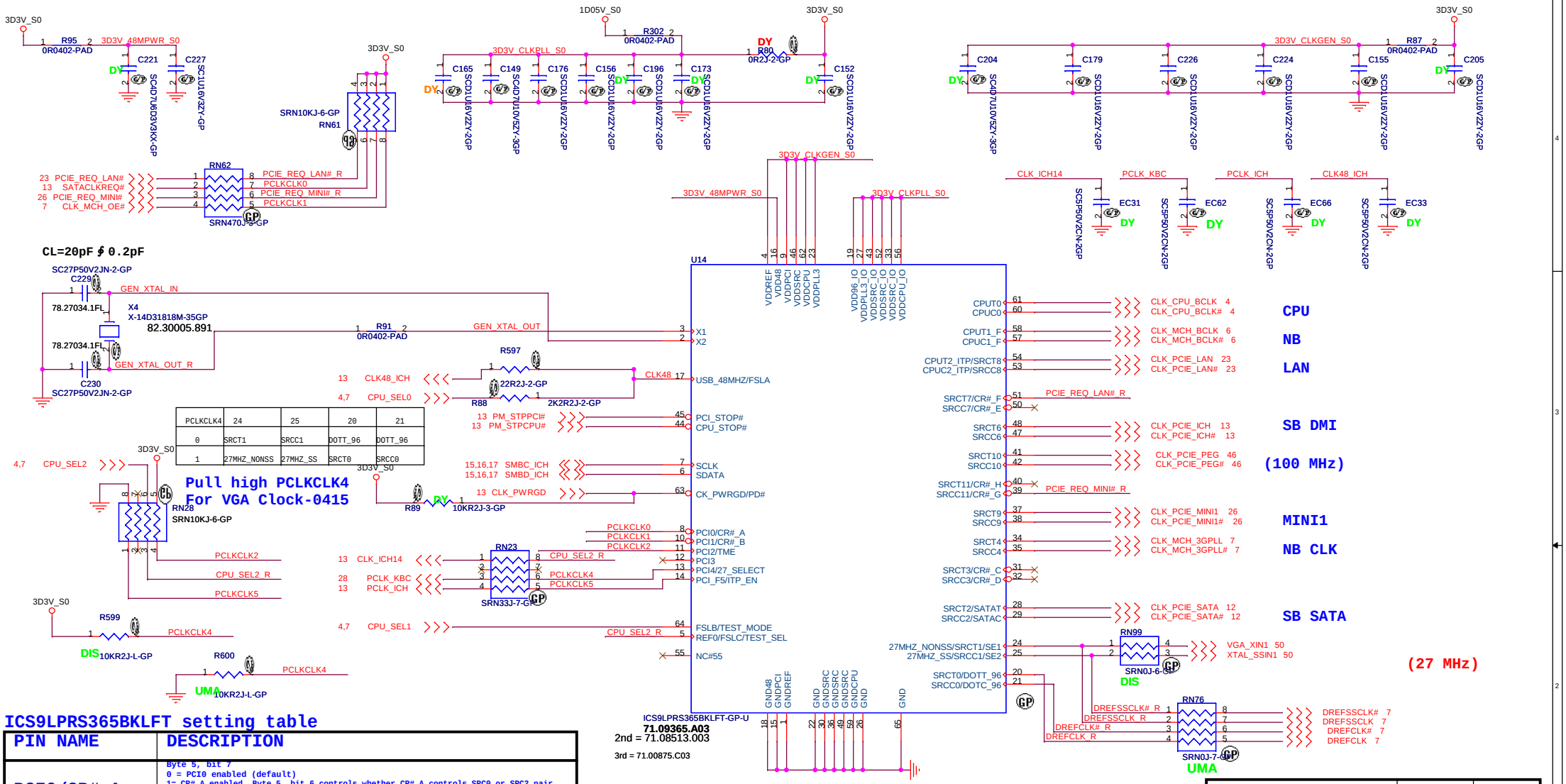

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

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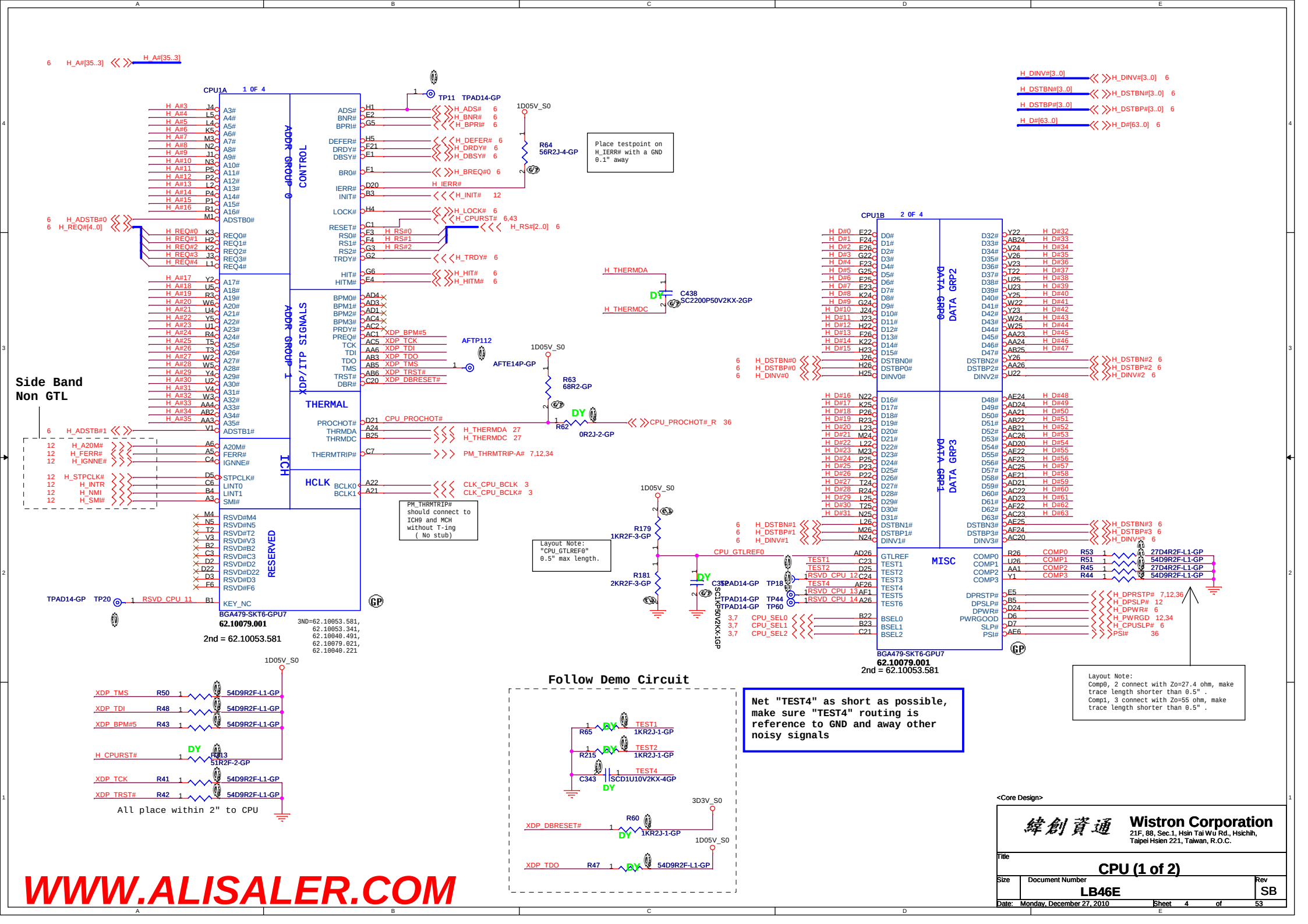
CPU1A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.581
CPU1B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
Side Band
Non GTL
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place testpoint on H_IERR# with a GND 0.1" away
Layout Note: "CPU_GTLREF0" 0.5" max length.
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
All place within 2" to CPU
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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CPU (1 of 2)
LB46E
Monday, December 27, 2010
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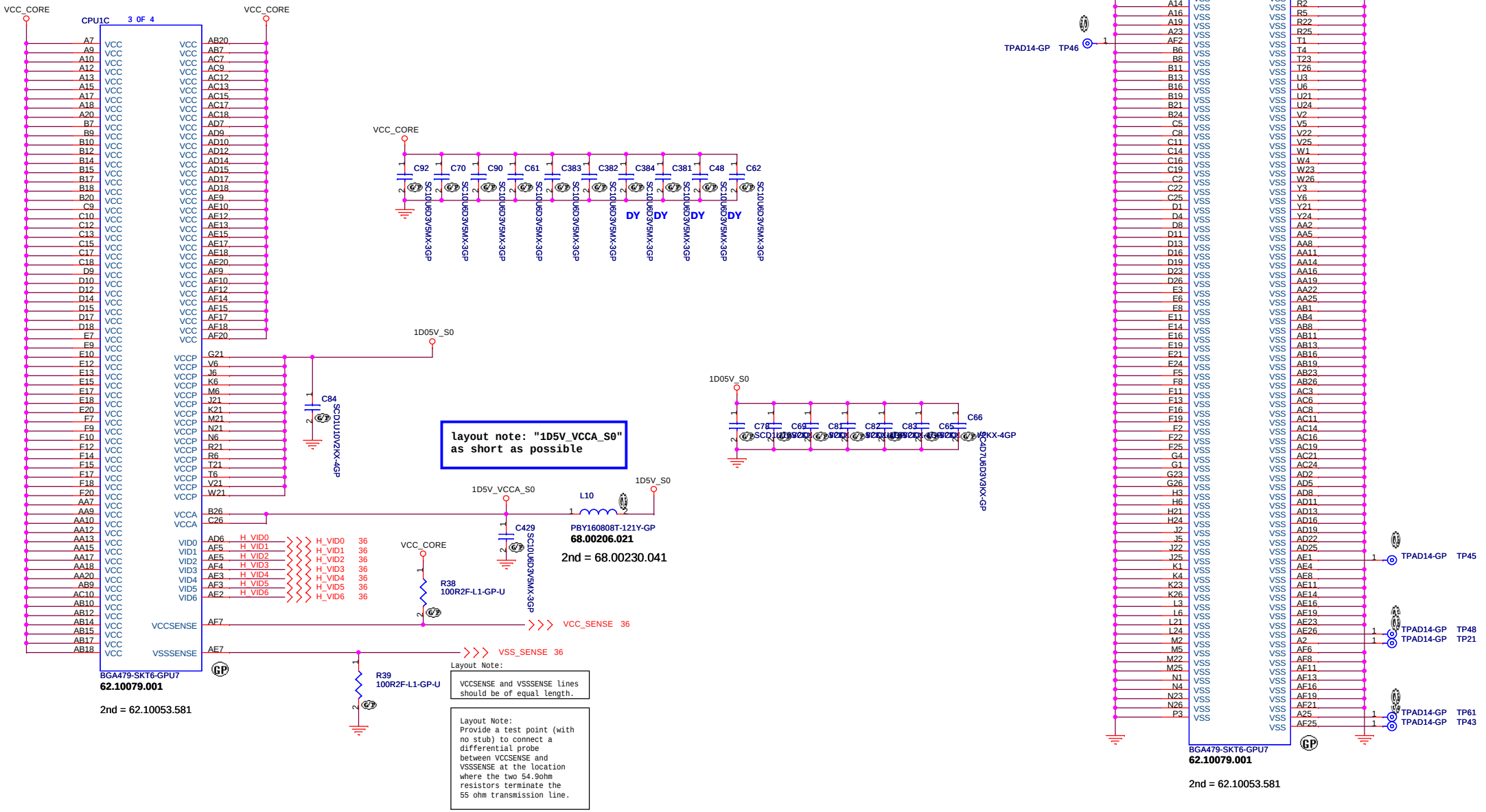

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Title	CPU (2 of 2)	
Size	Document Number: LB46E	Rev: SB
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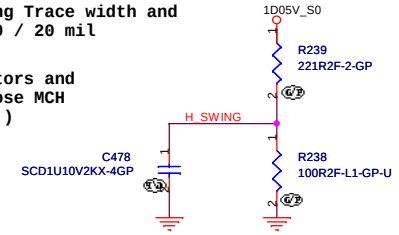
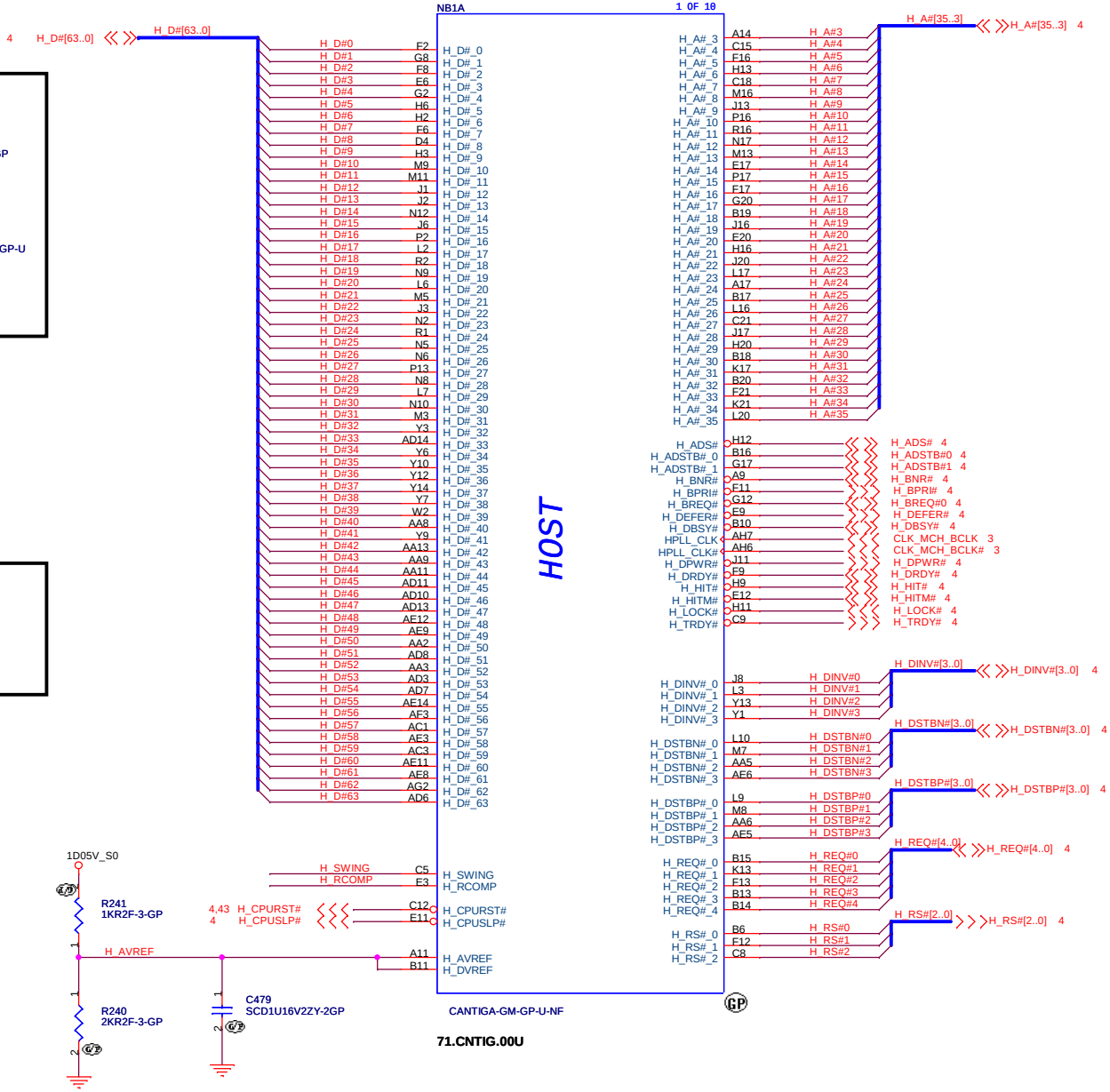
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6) HOST

Size | Document Number: LB46E | Rev: SB

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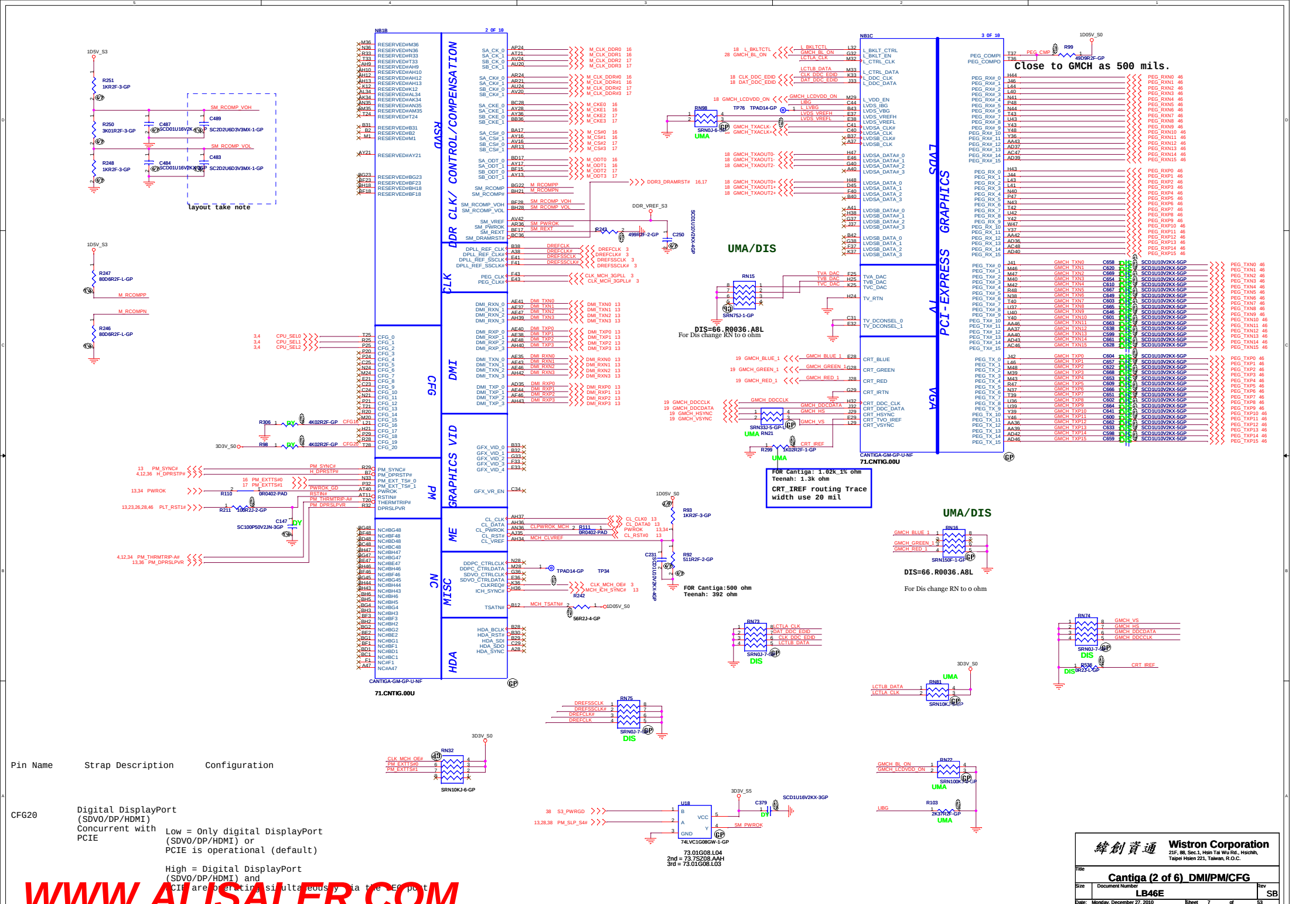

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port.

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Title	Cantiga (2 of 6)_DMI/PM/CFG	
Size	Document Number	Rev
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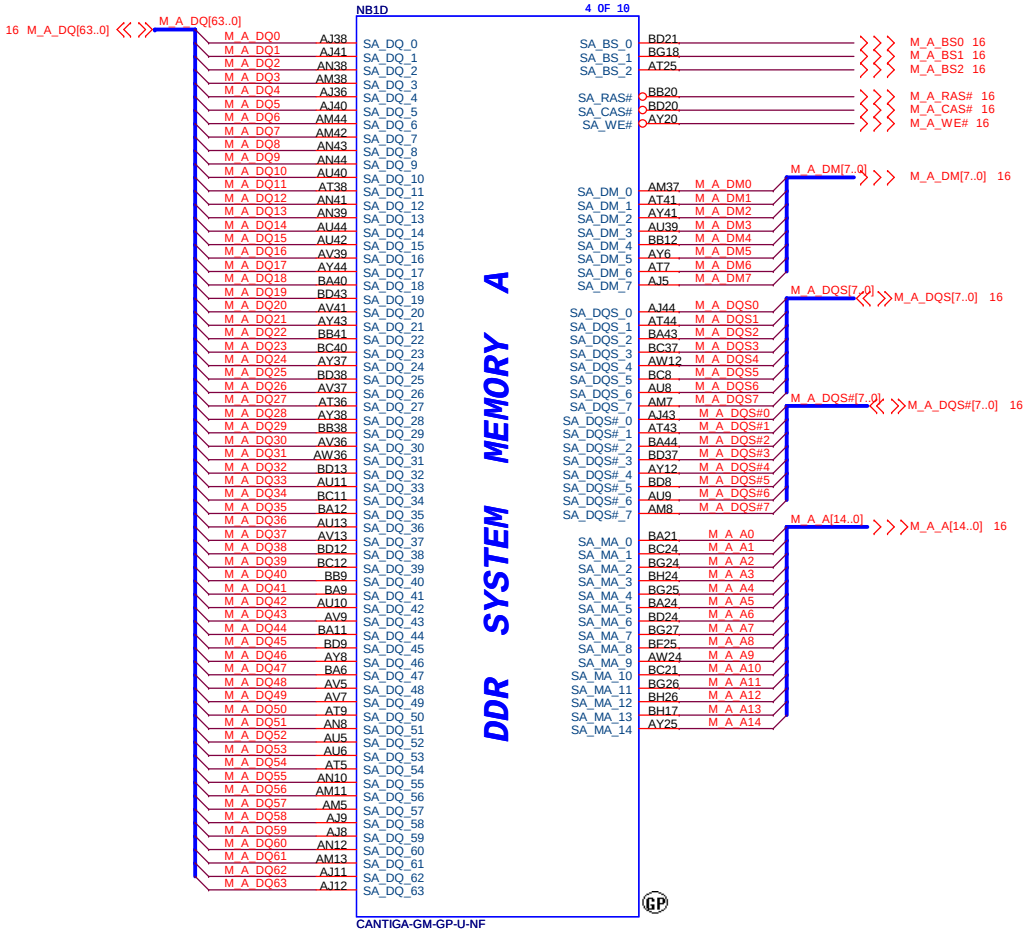
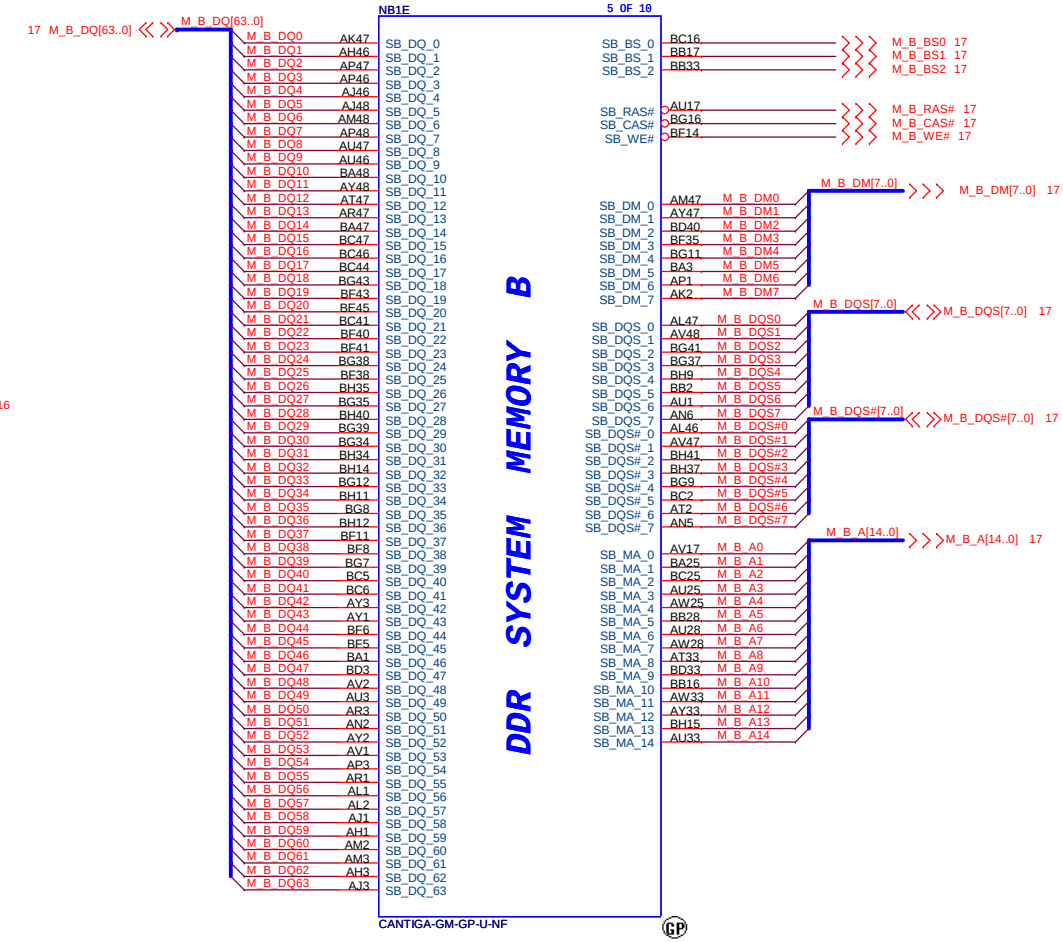
Date: Monday, December 27, 2010	Sheet 7 of 53	





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Title: 8_Cantiga (3 of 6)_DDR

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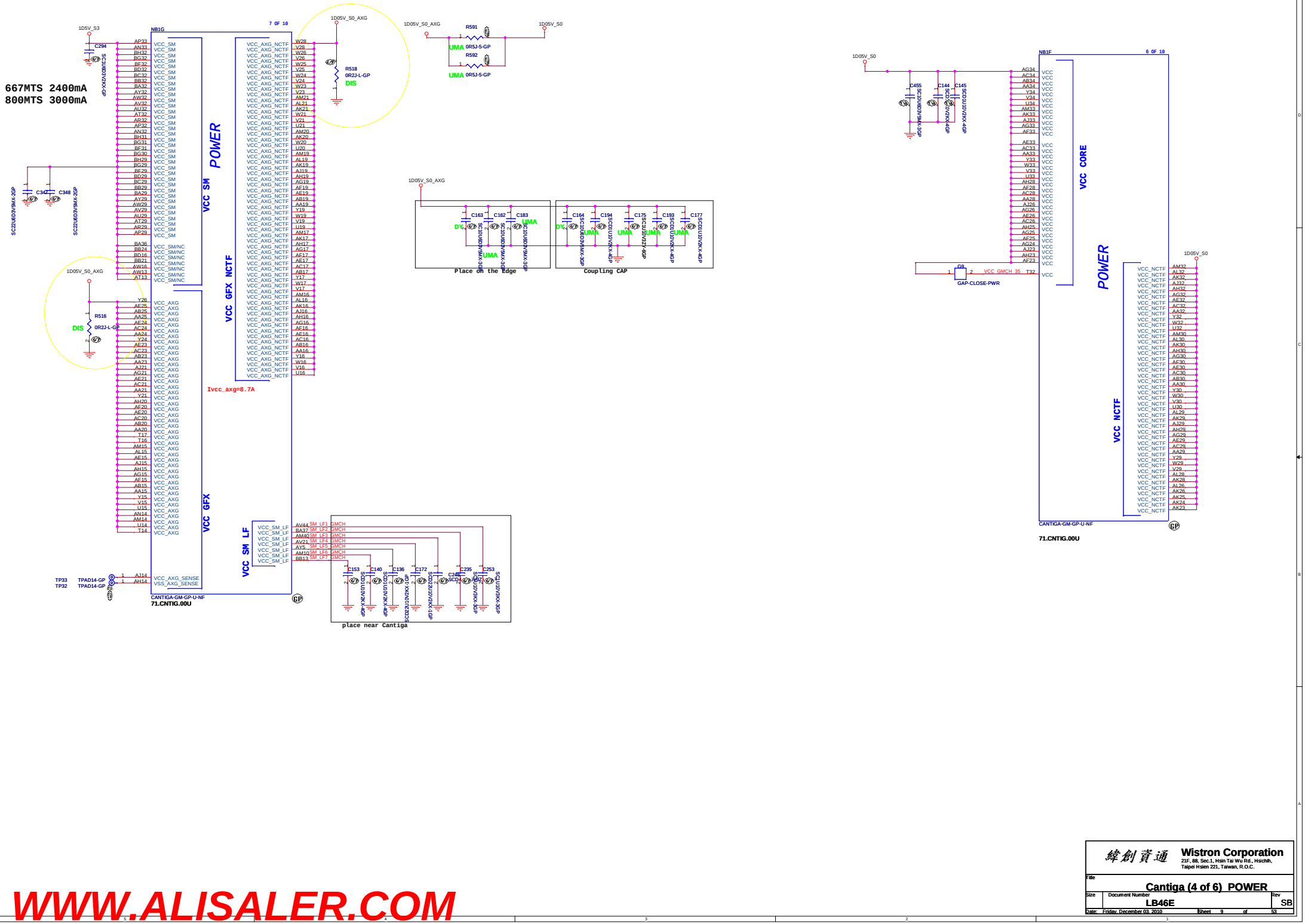

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Title	Cantiga (4 of 6) POWER
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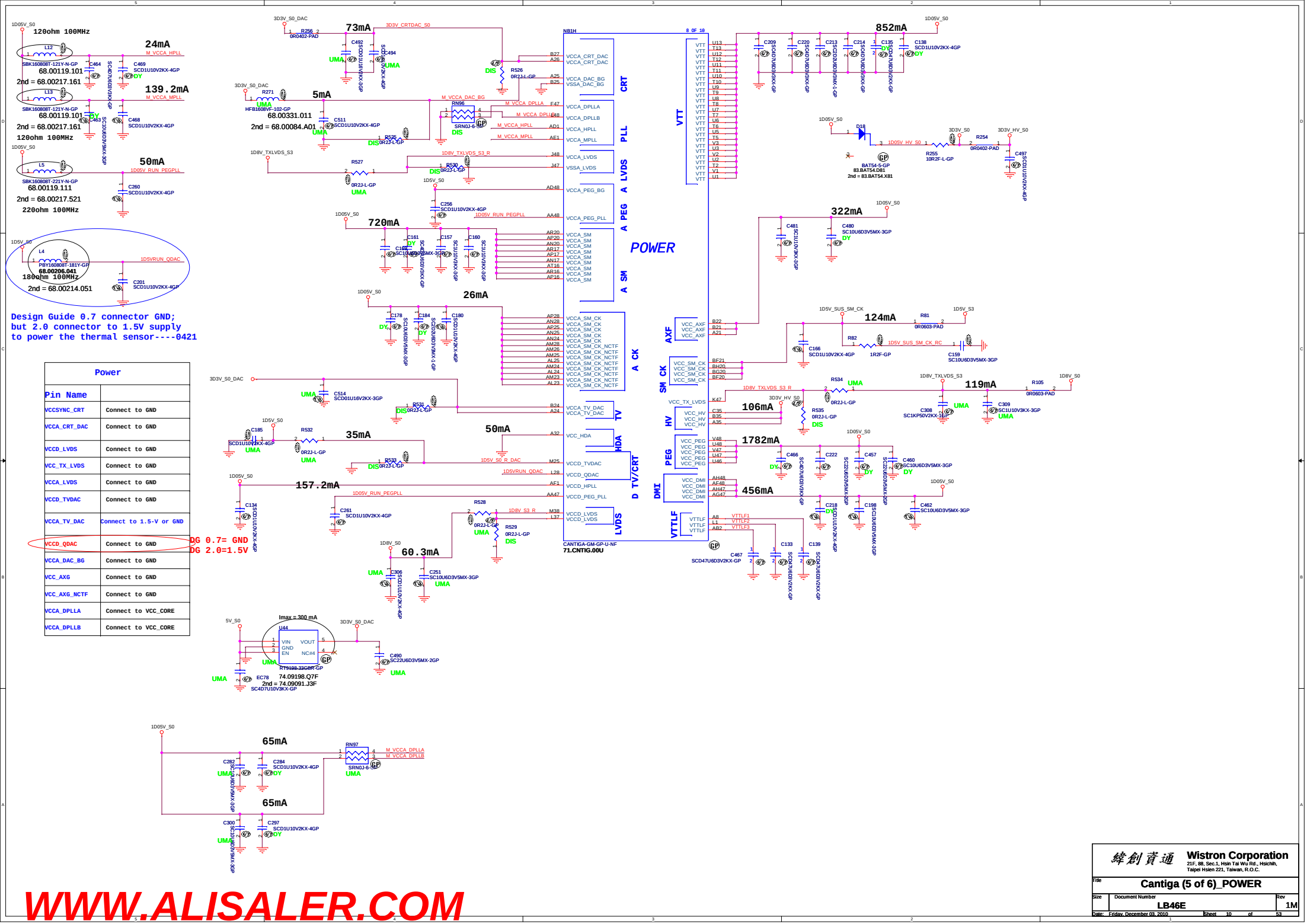
Date: Friday, December 03, 2010	Sheet 9 of 53


POWER
NB1H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
8 OF 10
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
73mA
852mA
5mA
139.2mA
24mA
50mA
720mA
322mA
26mA
124mA
119mA
106mA
35mA
50mA
1782mA
157.2mA
456mA
60.3mA
65mA
65mA
Design Guide 0.7 connector GND;
but 2.0 connector to 1.5V supply
to power the thermal sensor----0421
DG 0.7= GND
DG 2.0=1.5V
Power
Pin Name
VCCSYNC_CRT Connect to GND
VCCA_CRT_DAC Connect to GND
VCCD_LVDS Connect to GND
VCC_TX_LVDS Connect to GND
VCCA_LVDS Connect to GND
VCCD_TVDAC Connect to GND
VCCA_TV_DAC Connect to 1.5-V or GND
VCCD_QDAC Connect to GND
VCCA_DAC_BG Connect to GND
VCC_AXG Connect to GND
VCC_AXG_NCTF Connect to GND
VCCA_DPLLA Connect to VCC_CORE
VCCA_DPLLB Connect to VCC_CORE
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Cantiga (5 of 6)_POWER
LB46E
1M
Friday, December 03, 2010
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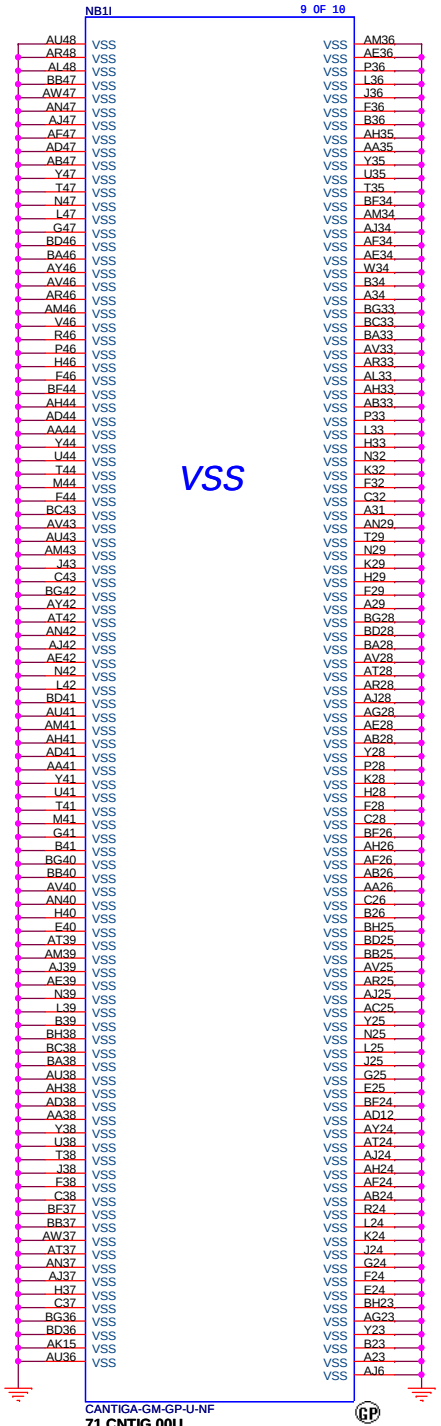

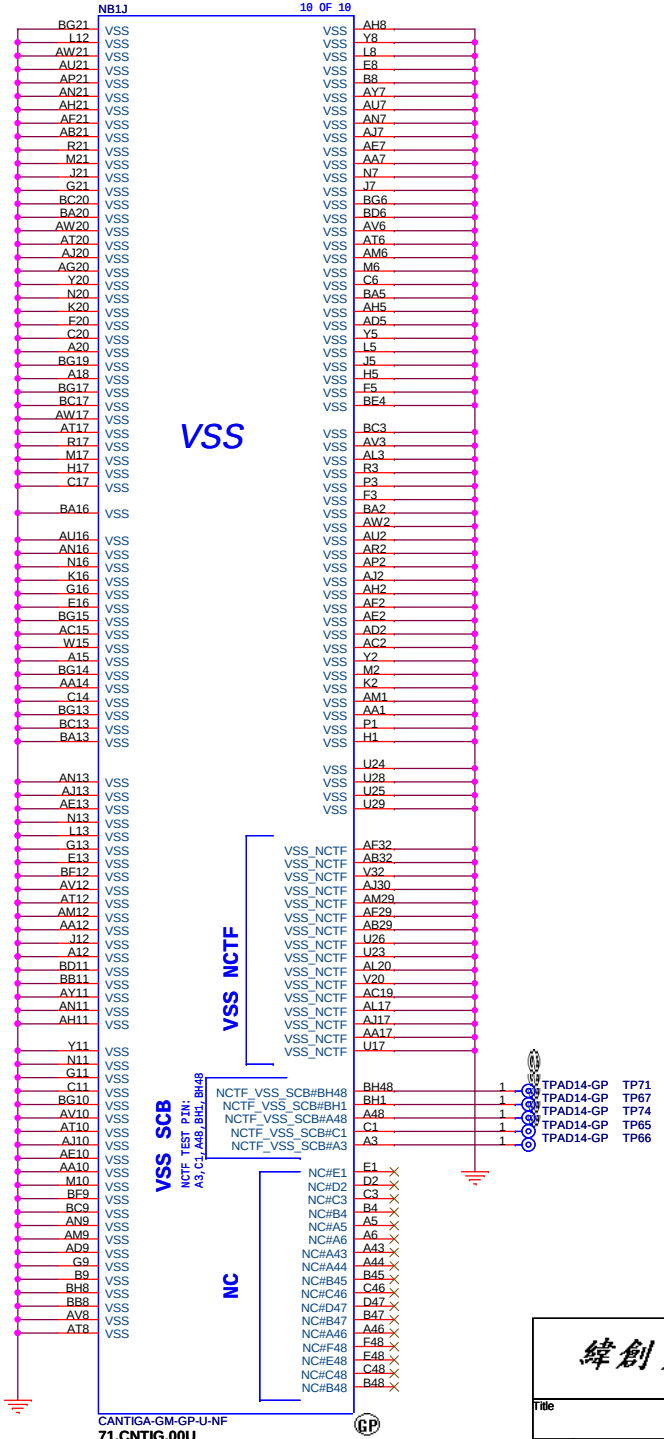

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Title: **Cantiga (6 of 6)**

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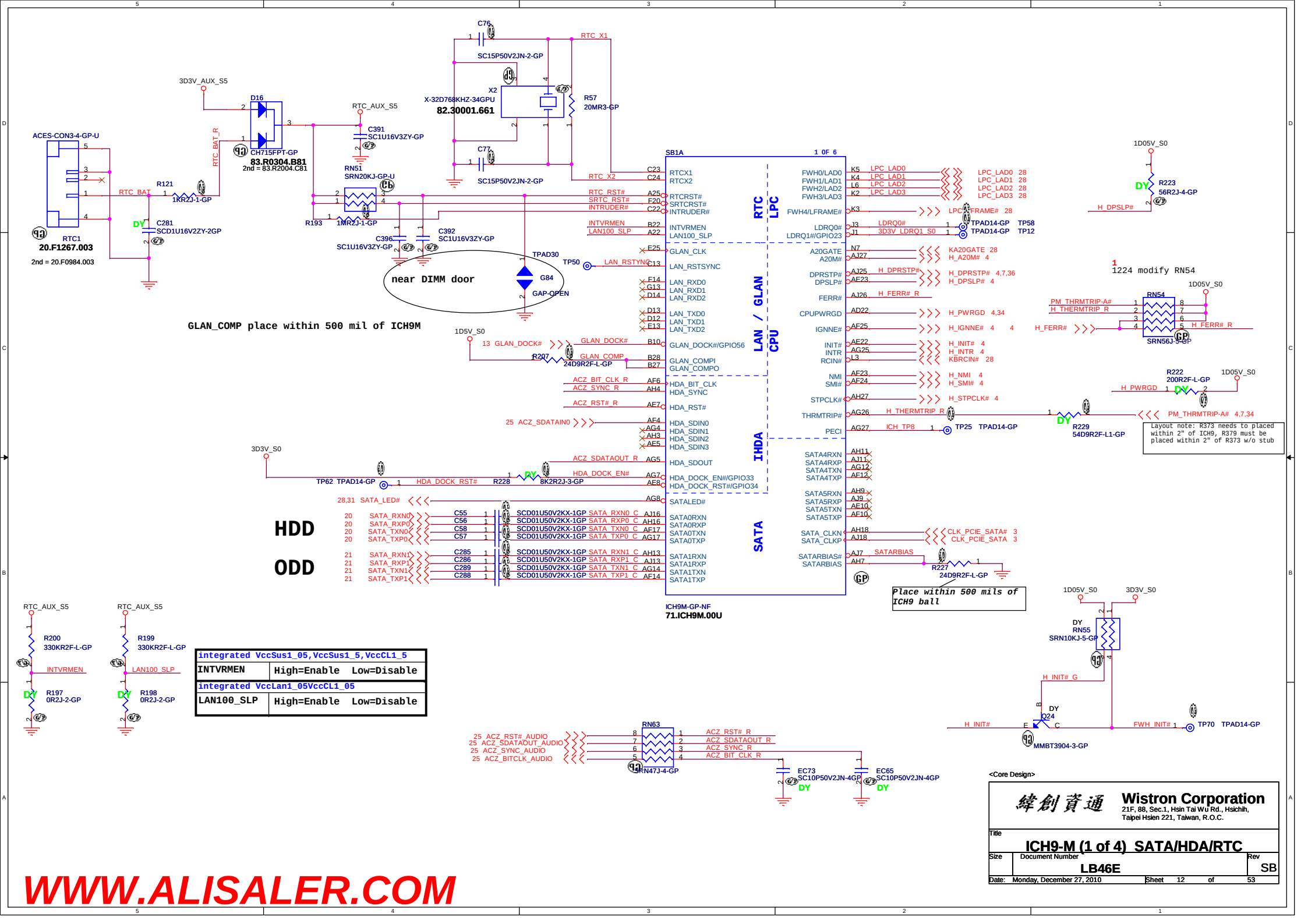

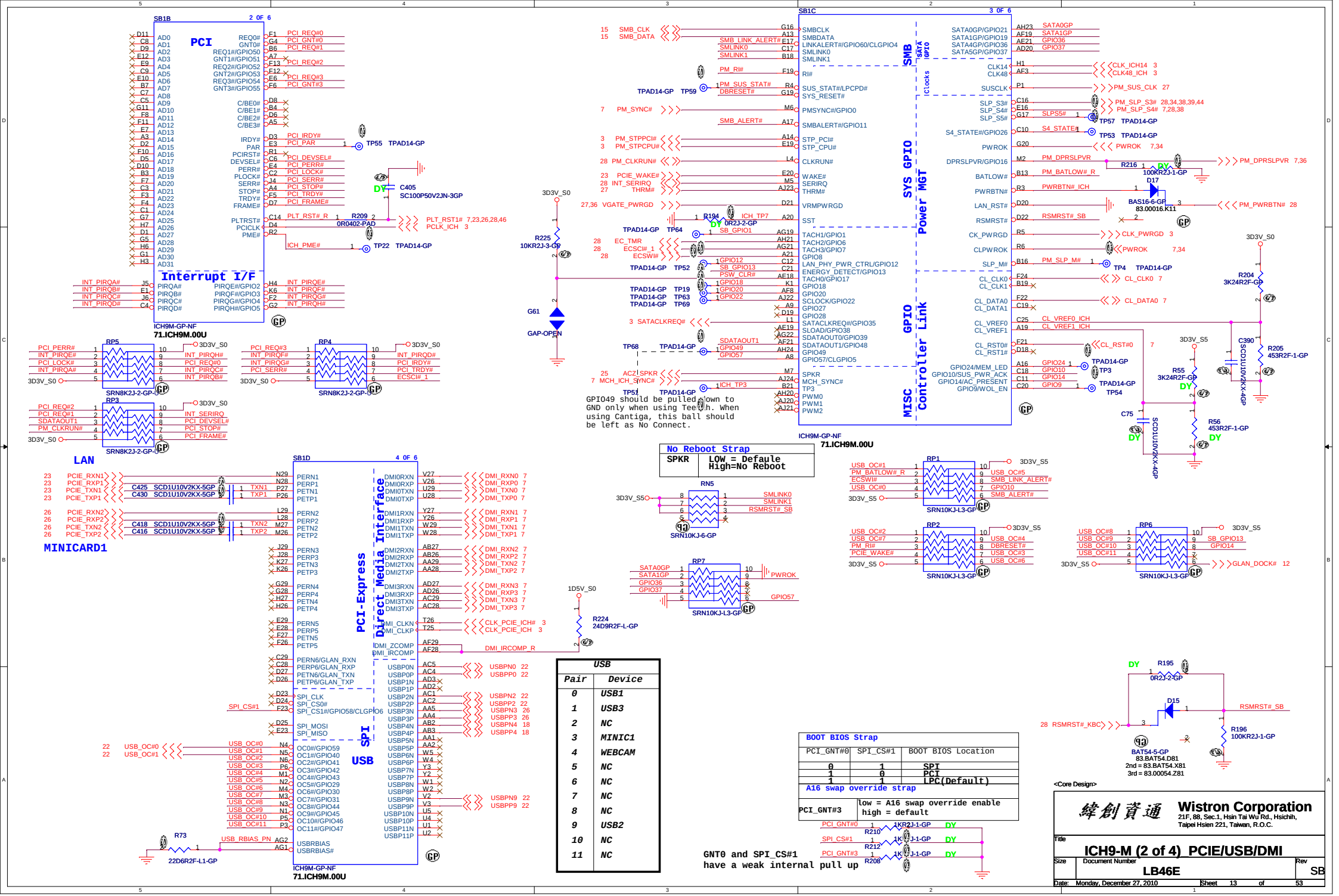

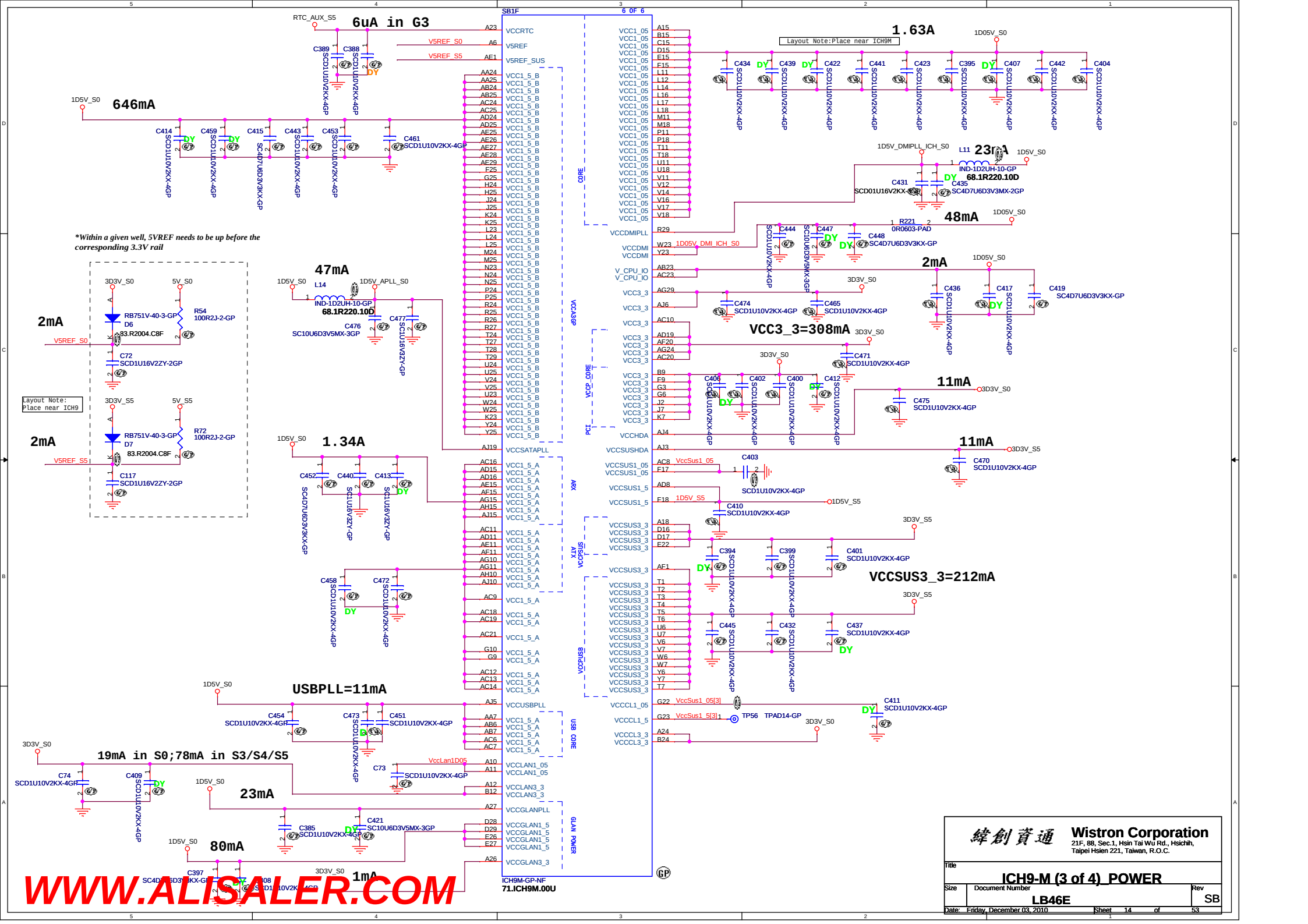

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Title: ICH9-M (3 of 4)_POWER

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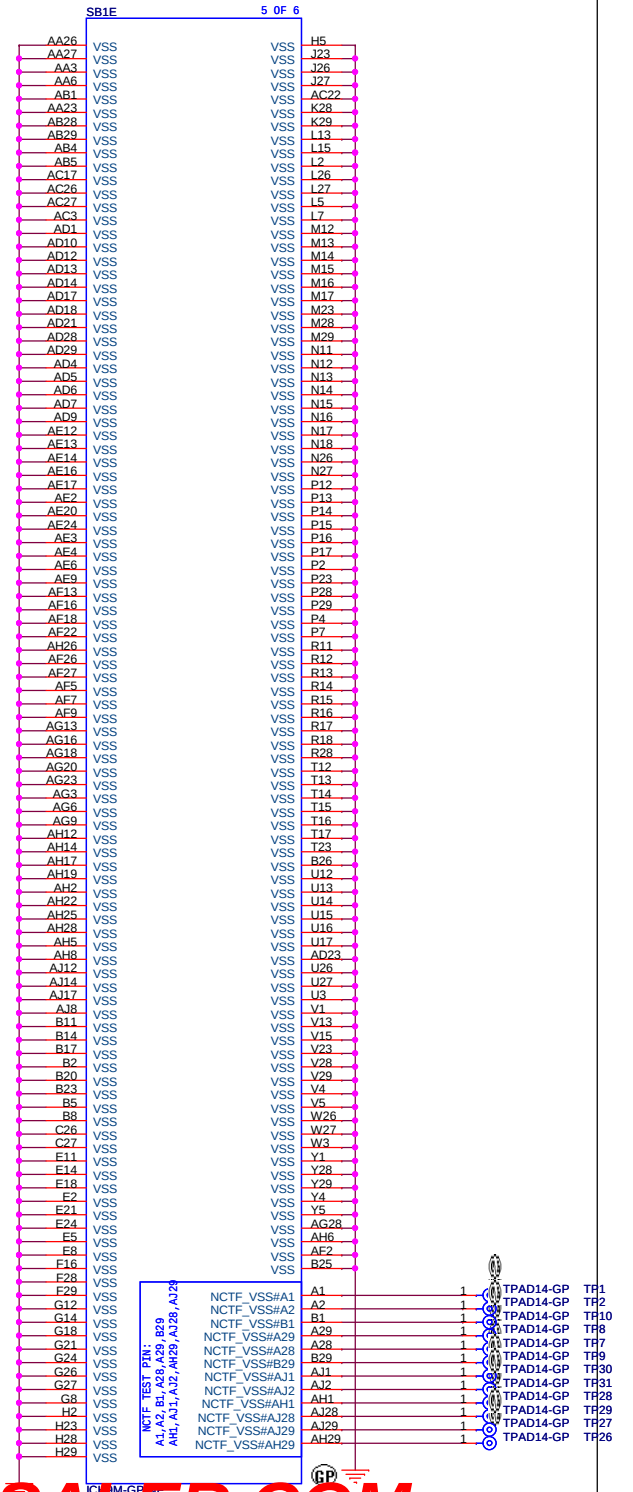

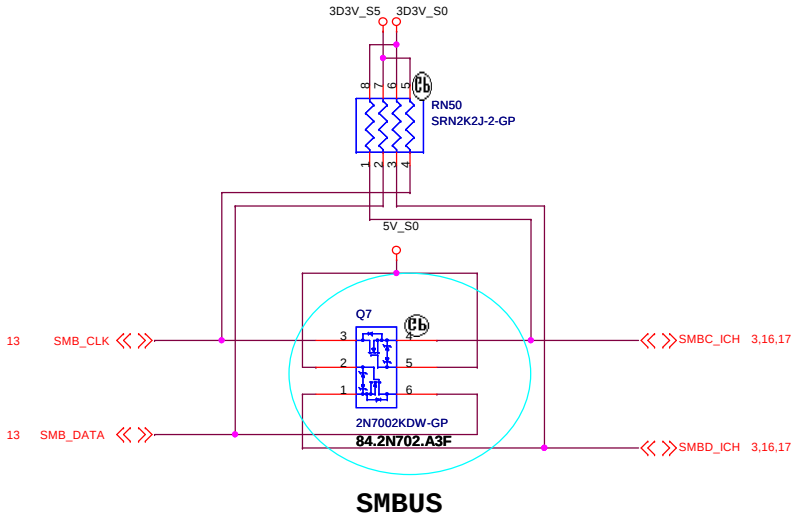

SMBUS

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Title: **ICH9-M (4 of 4)**

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	LB46E	SB

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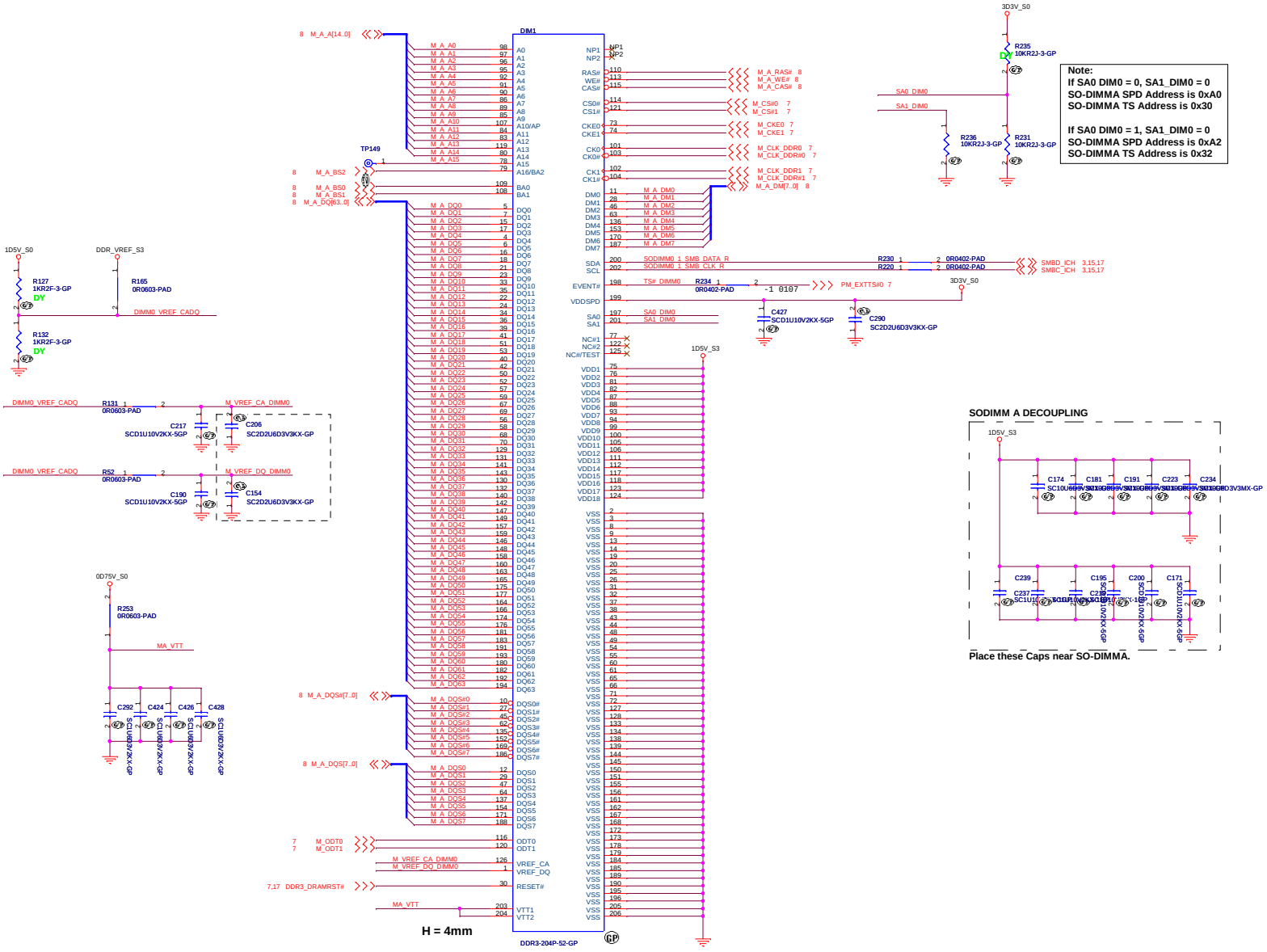

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C

Title: 16_DDR3-SODIMM1

Size: A2 | Document Number: LB46E | Rev: SA

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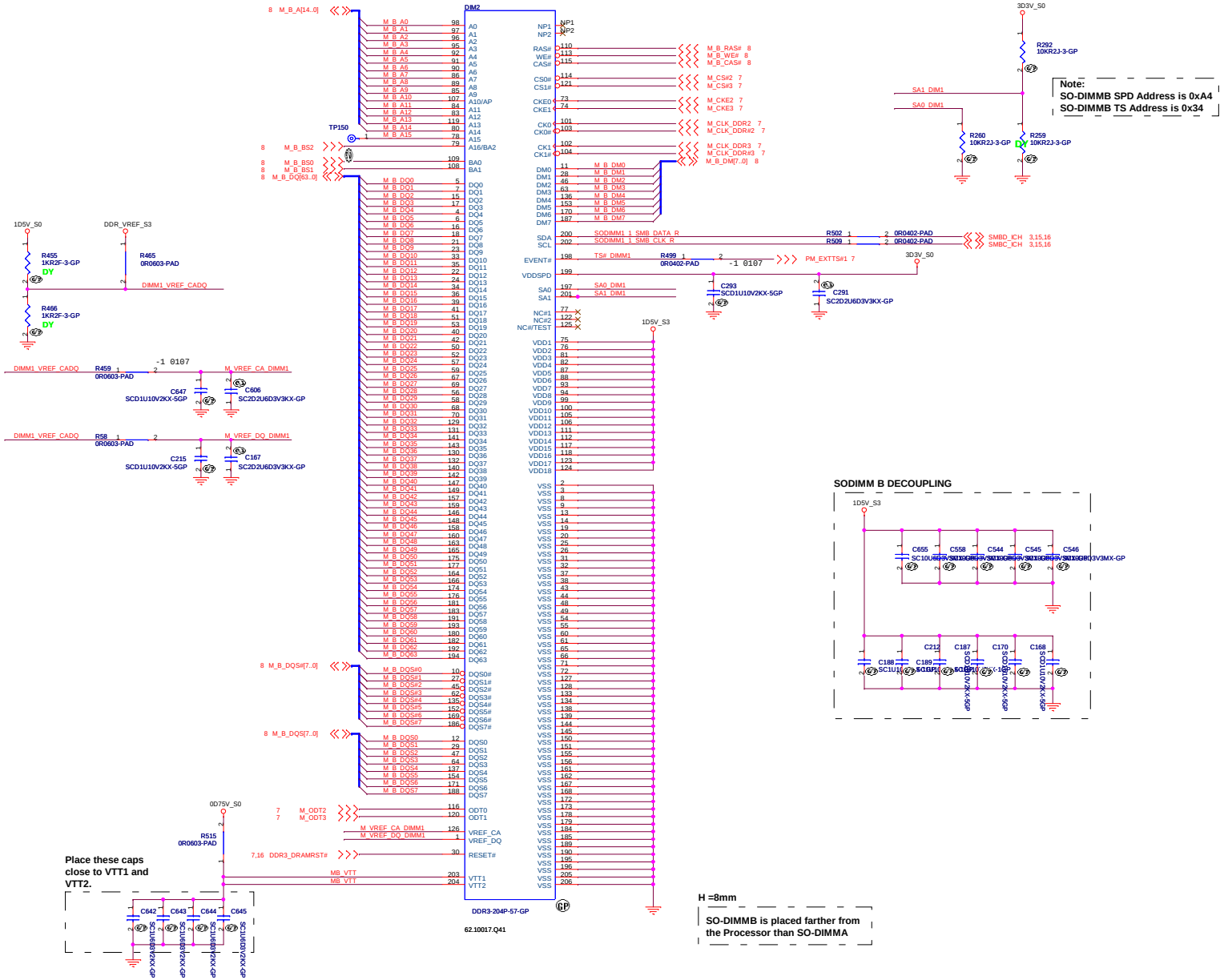
2010/9/27 Changed



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: 17_DDR3-SODIMM2

Size: A2 | Document Number: LB46E | Rev: SA

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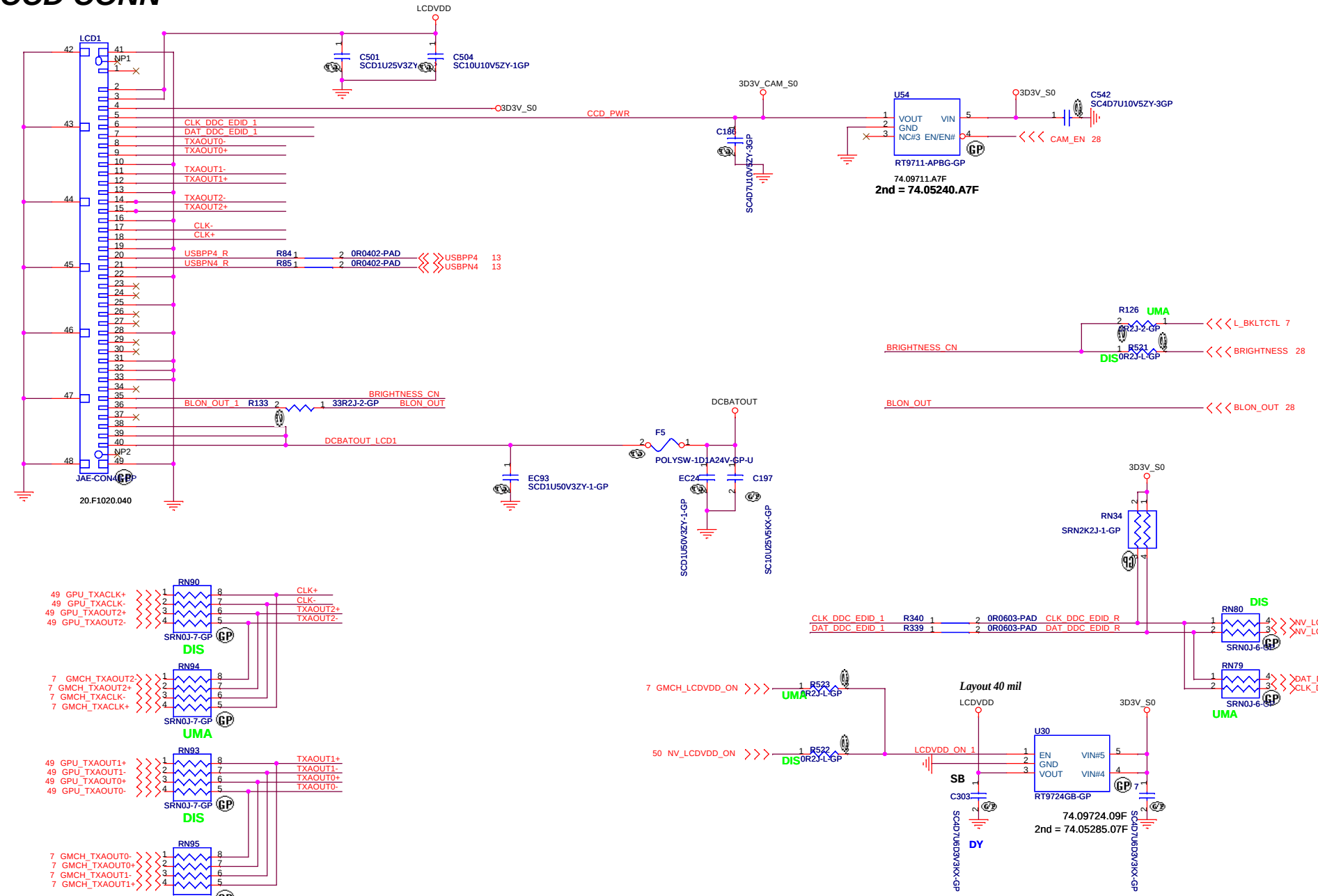
LCD/CCD CONN



<Core Design>

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Title		
LCD CONN		
Size	Document Number	Rev
	LB46E	SB
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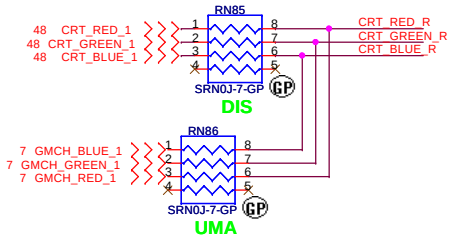
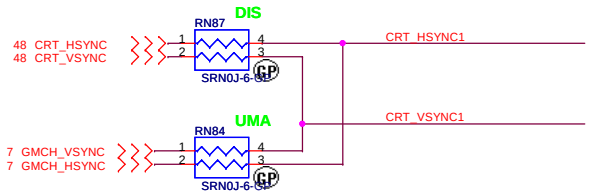
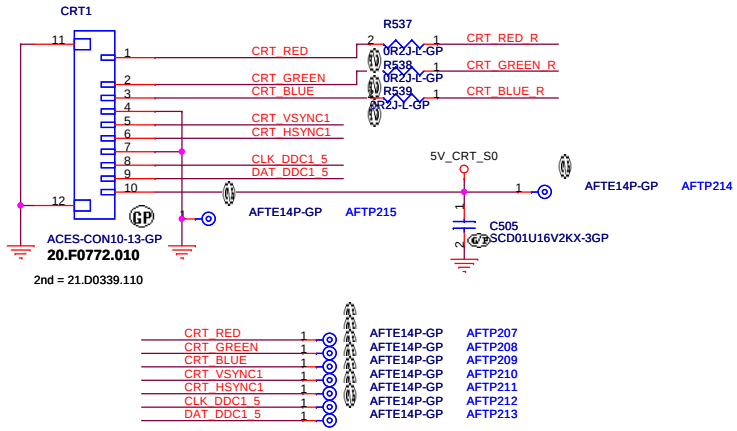


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

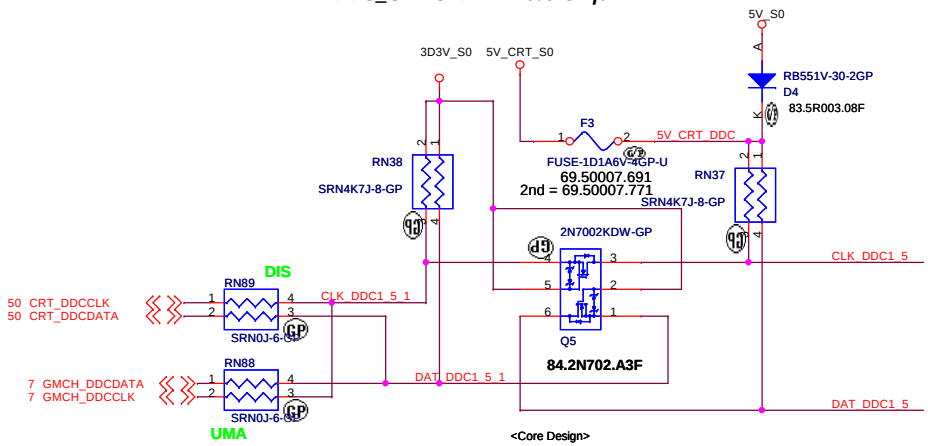
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
CRT Connector		
Size	Document Number	Rev
	LB46E	SB
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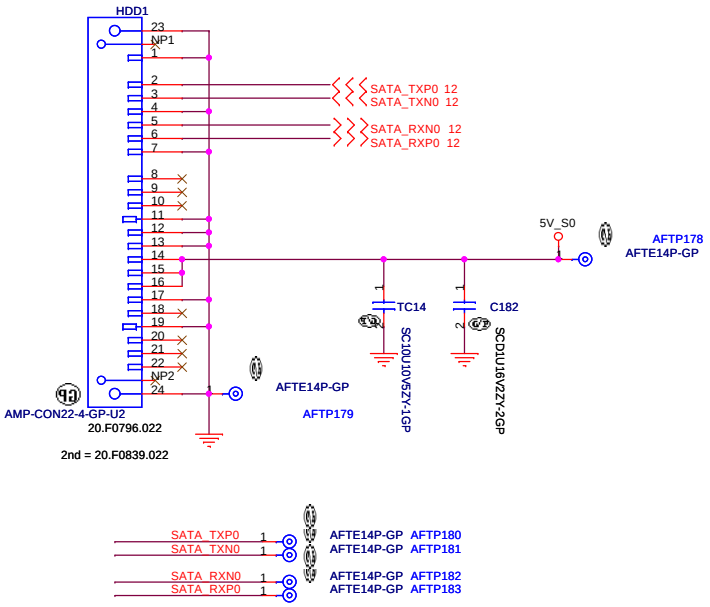
SATA Connector

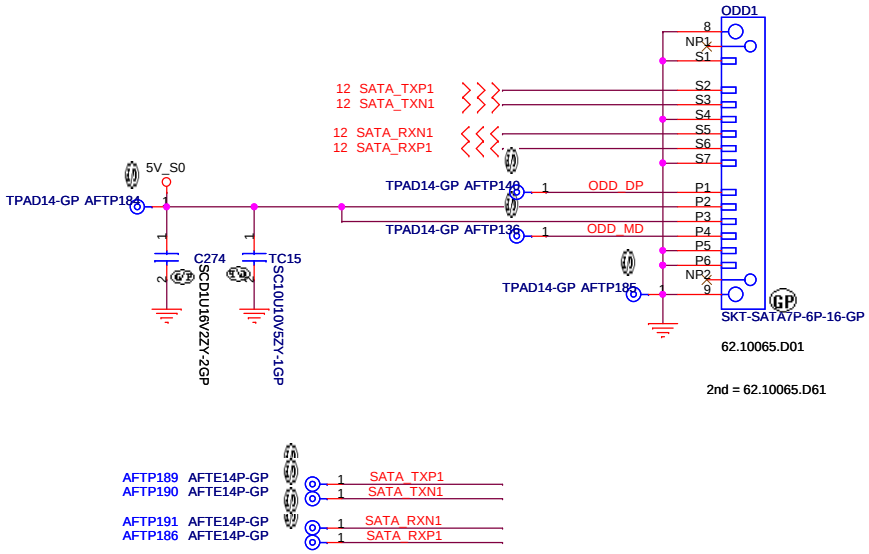


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD		
Size	Document Number	Rev
	LB46E	SB
Date: Monday, December 27, 2010	Sheet 20 of 53	

SATA ODD Connector



<Core Design>

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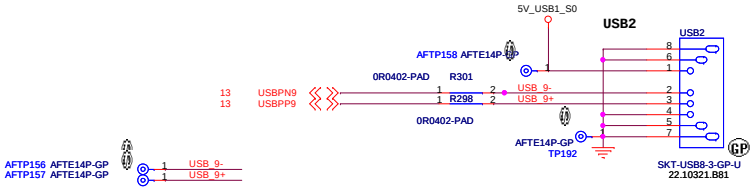
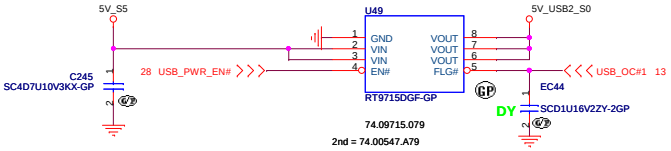
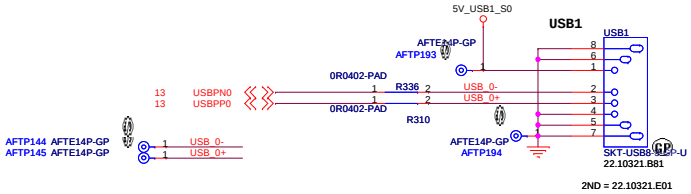
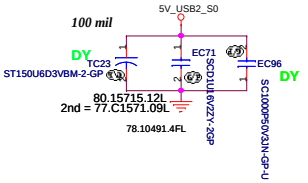
Title: ODD		
Size	Document Number: LB46E	Rev: SB
Date: Monday, December 27, 2010	Sheet 21 of 53	

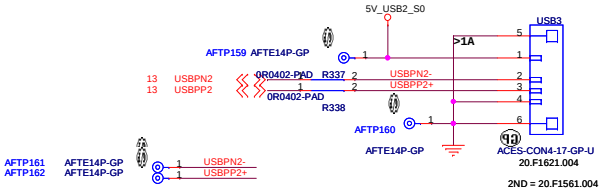


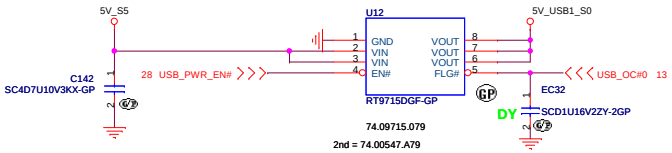


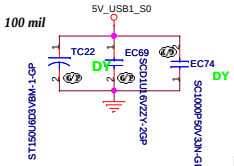




Connect to USB BD







<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB**

Size	Document Number	Rev
	LB46E	SB

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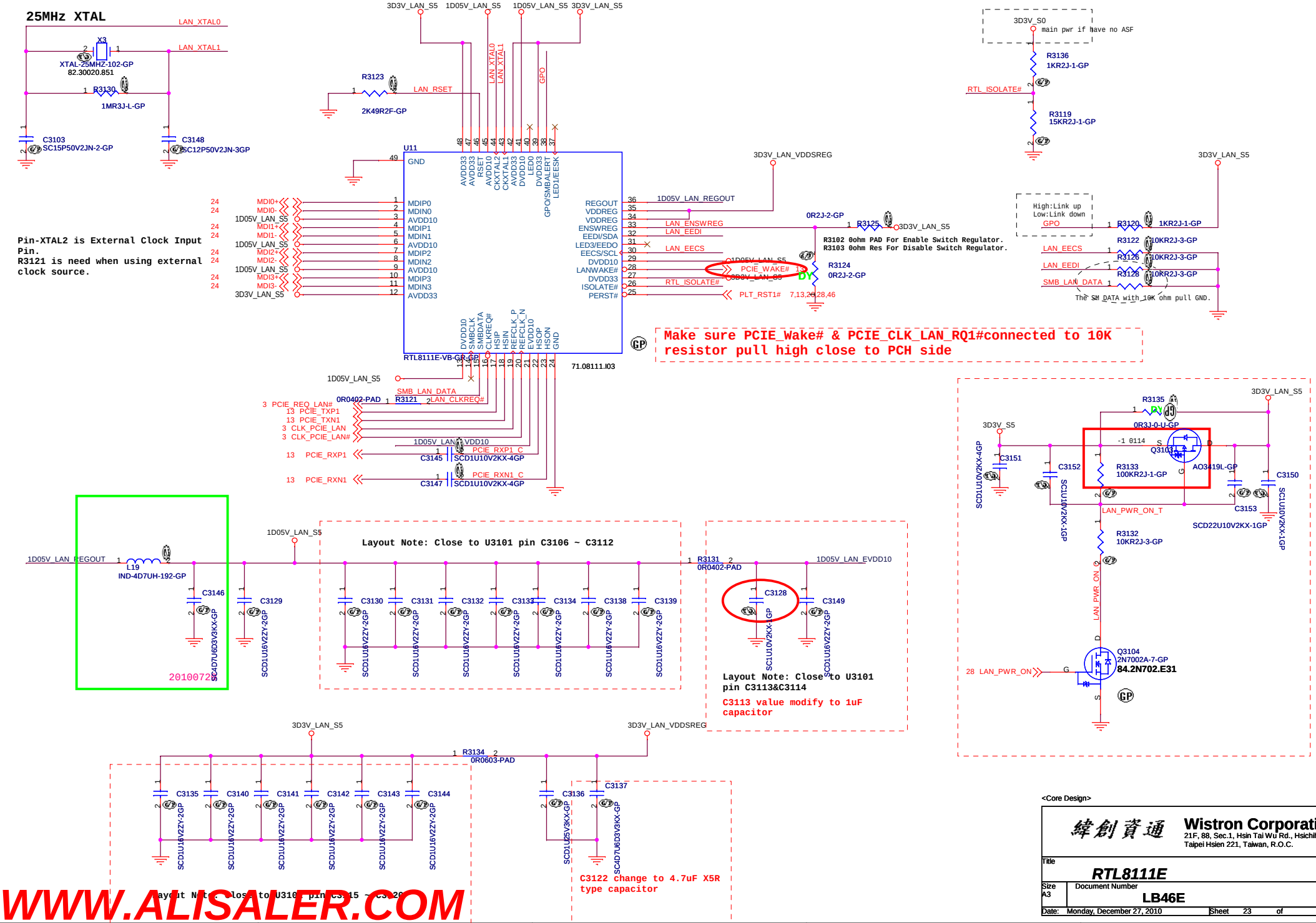
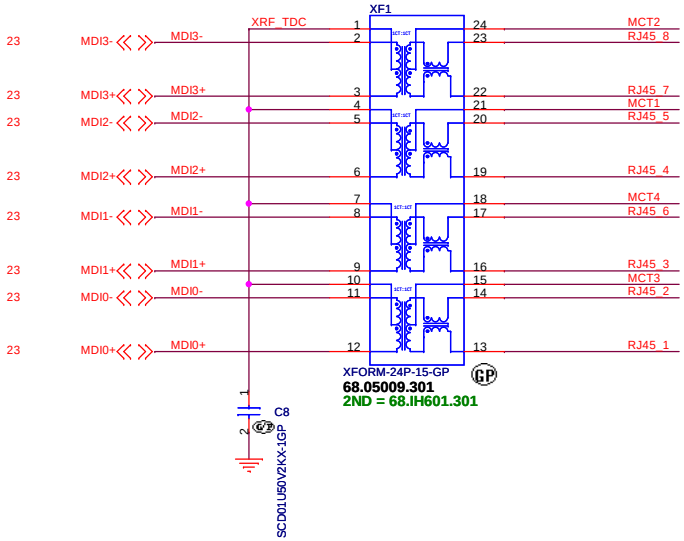
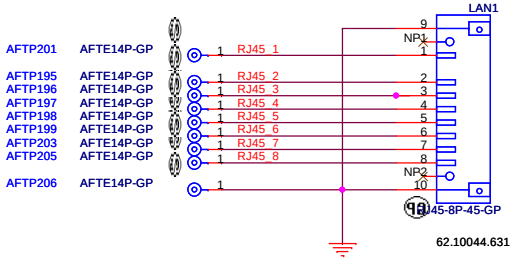
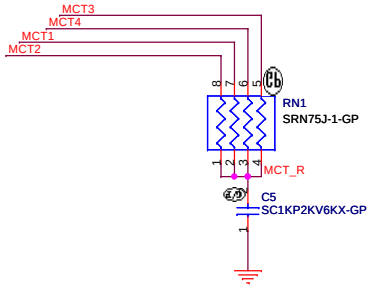


1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector

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A3	LB46E	SB

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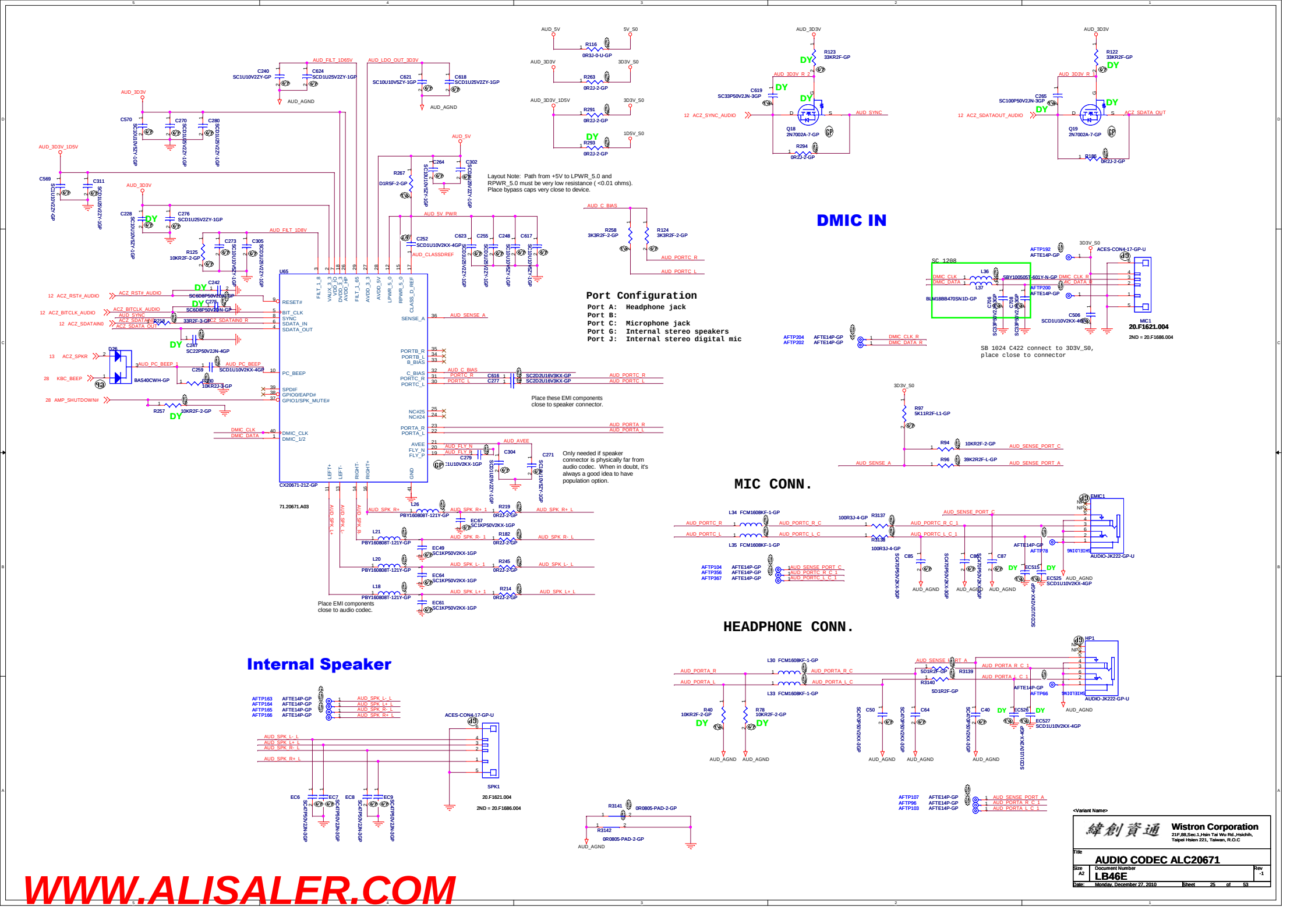
Port Configuration
Port A: Headphone jack
Port B:
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Internal stereo digital mic
DMIC IN
MIC CONN.
HEADPHONE CONN.
Internal Speaker
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.
Place these EMI components close to speaker connector.
Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.
Place EMI components close to audio codec.
SB 1024 C422 connect to 3D3V_S0, place close to connector
U65
CX20671-21Z-GP
71.20671.A03
ACES-CON4-17-GP-U
SPK1
20.F1621.004
2ND = 20.F1686.004
MIC1
20.F1621.004
2ND = 20.F1686.004
AUDIO-JK222-GP-U
HP1
AUDIO-JK222-GP-U
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AUDIO CODEC ALC20671
LB46E
Monday, December 27, 2010
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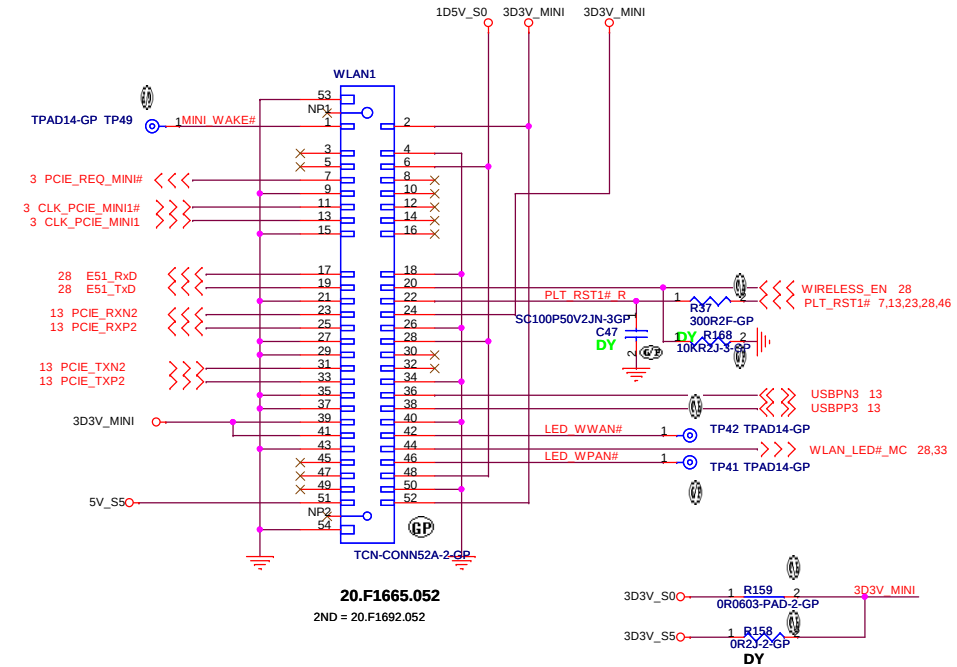
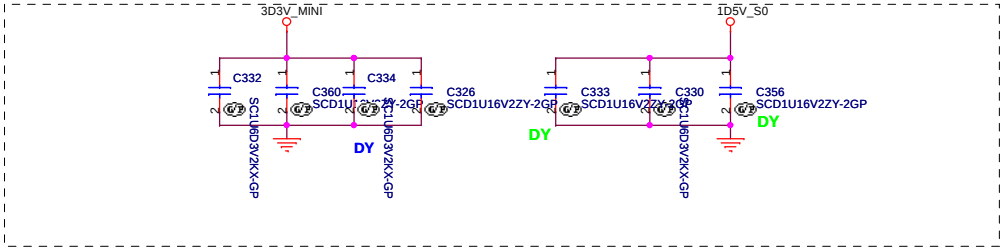
Mini Card Connector(WLAN)



Place near MINIC1



<Core Design>

緯創資通 Wistron Corporation
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Title		
MINI CARD		
Size	Document Number	Rev
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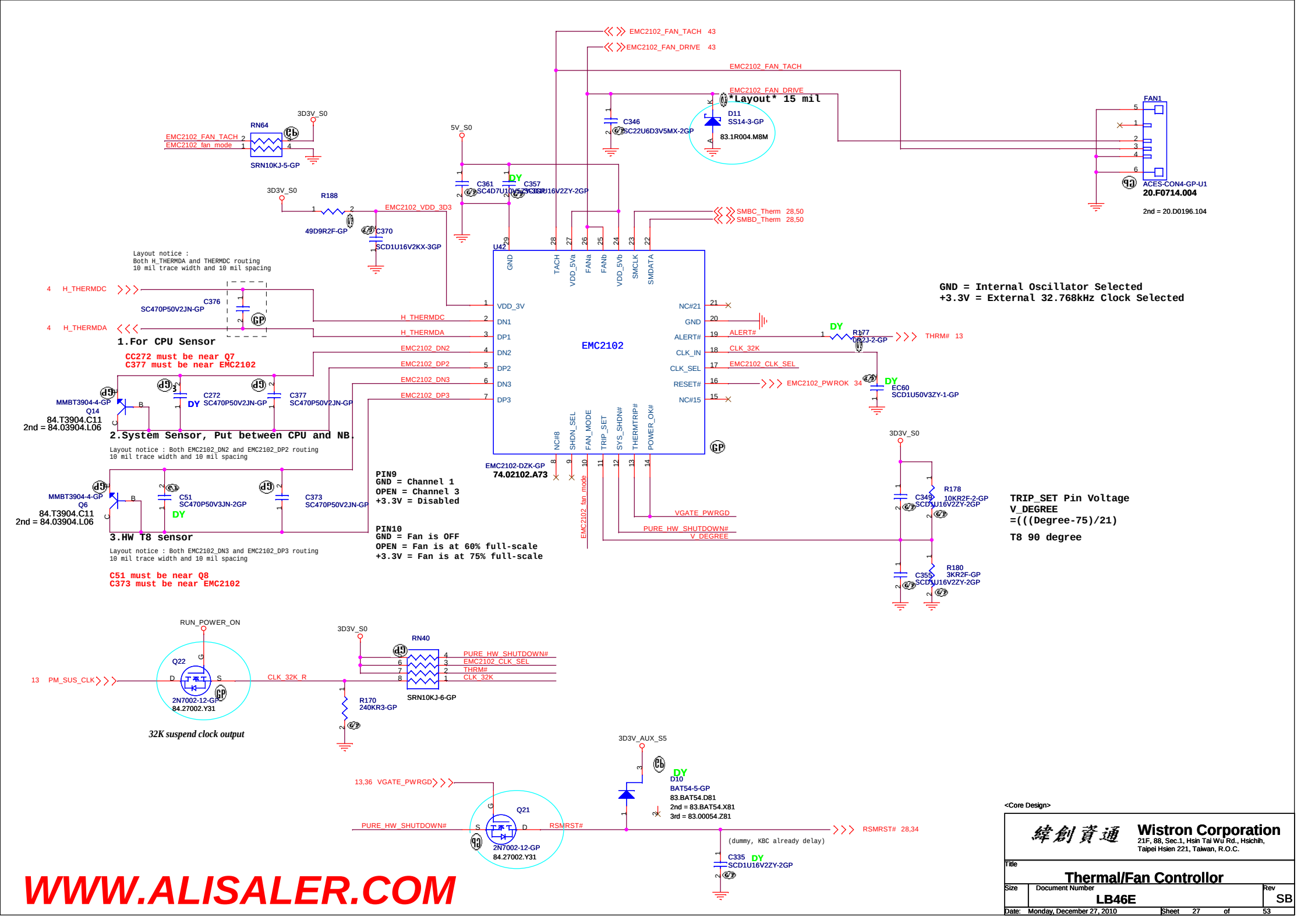

<Core Design>

緯創資通 Wistron Corporation
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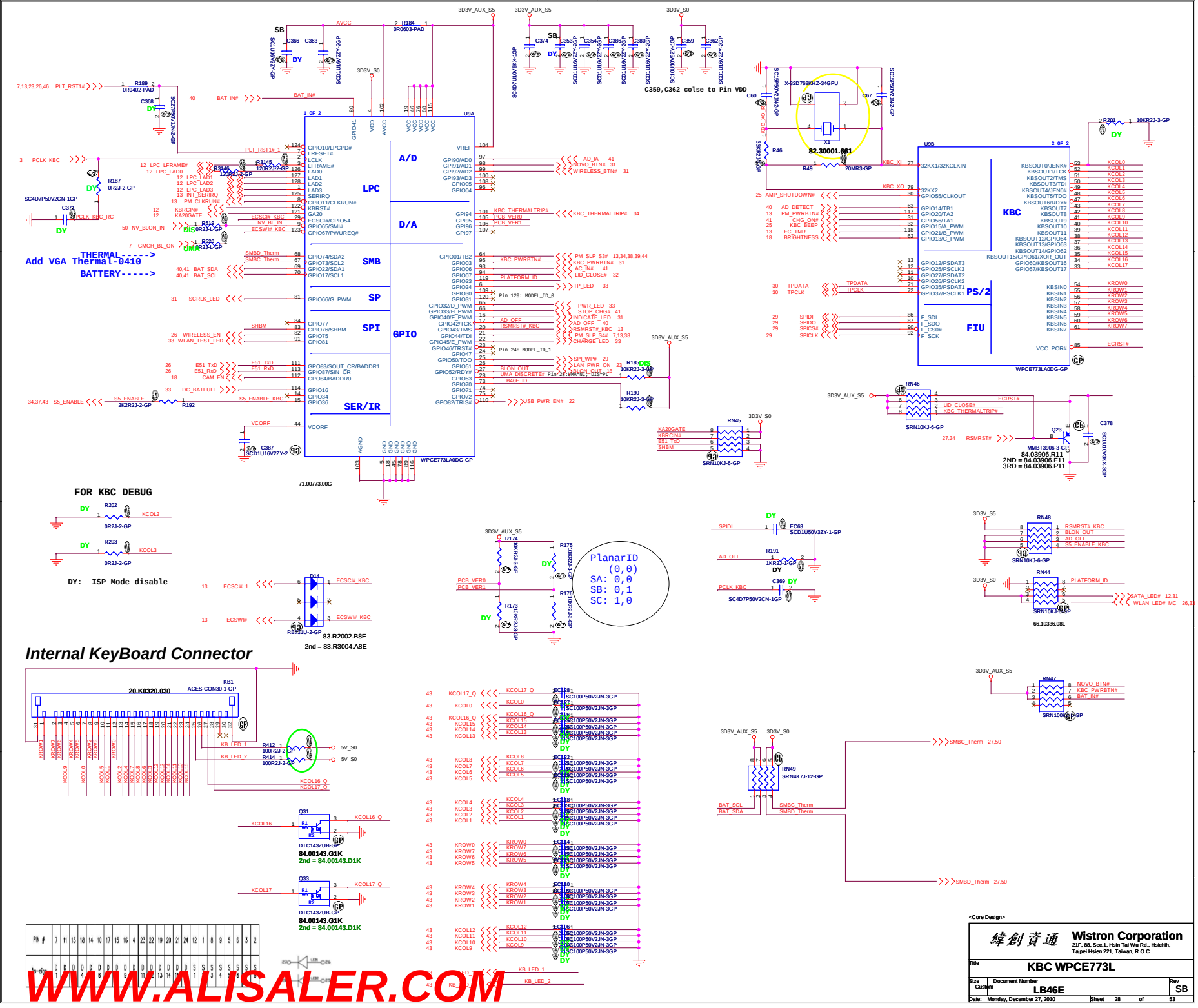
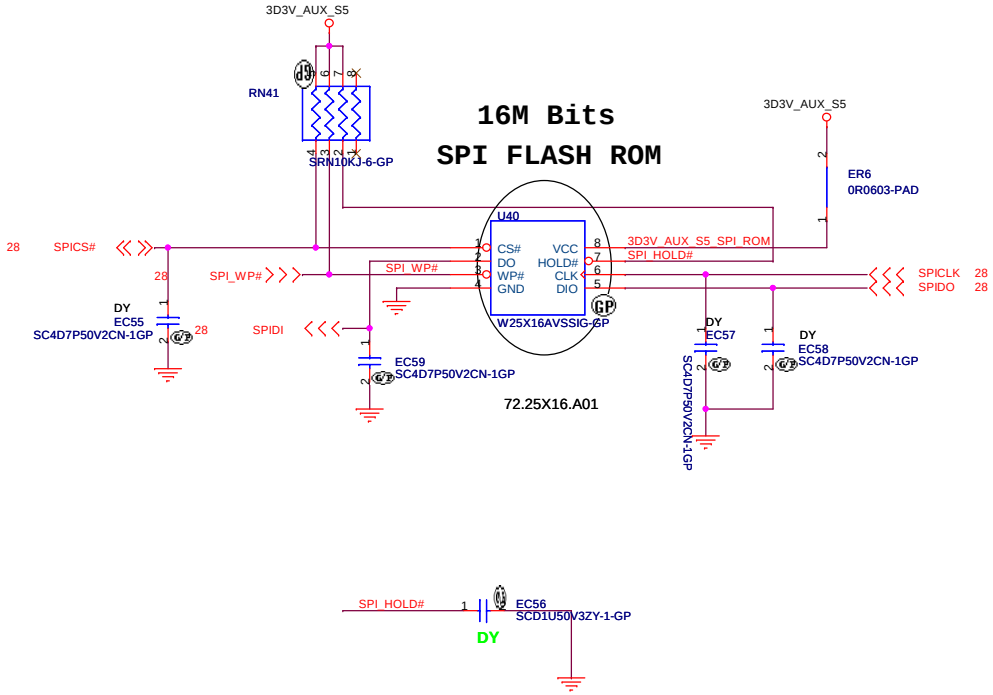
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor

Size	Document Number	Rev
	LB46E	SB

Date: Monday, December 27, 2010 Sheet 27 of 53





<Core Design>

緯創資通 **Wistron Corporation**
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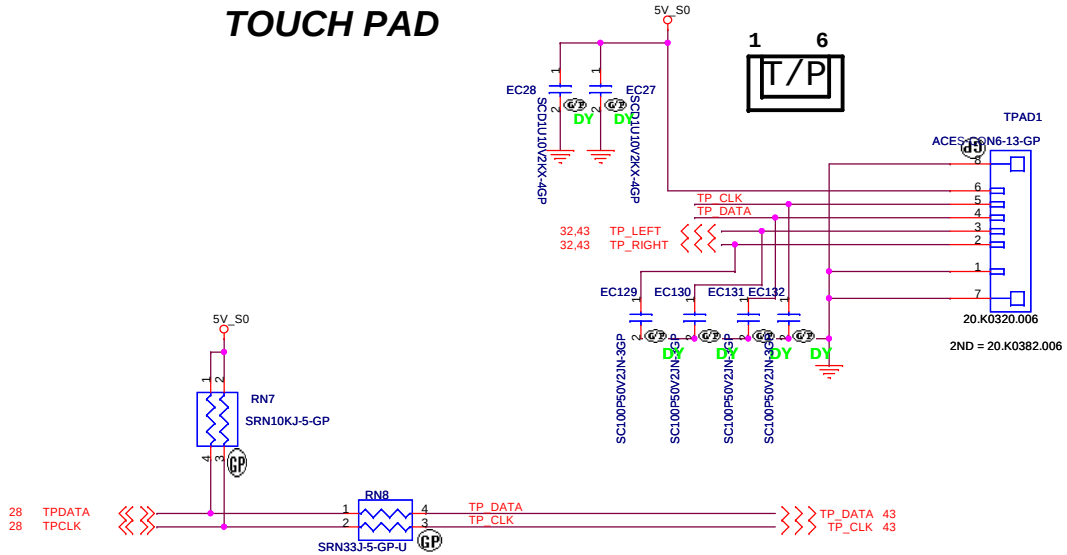
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size	Document Number: LB46E	Rev: SB
Date: Monday, December 27, 2010	Sheet 29 of 53	

TOUCH PAD



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Touch pad	
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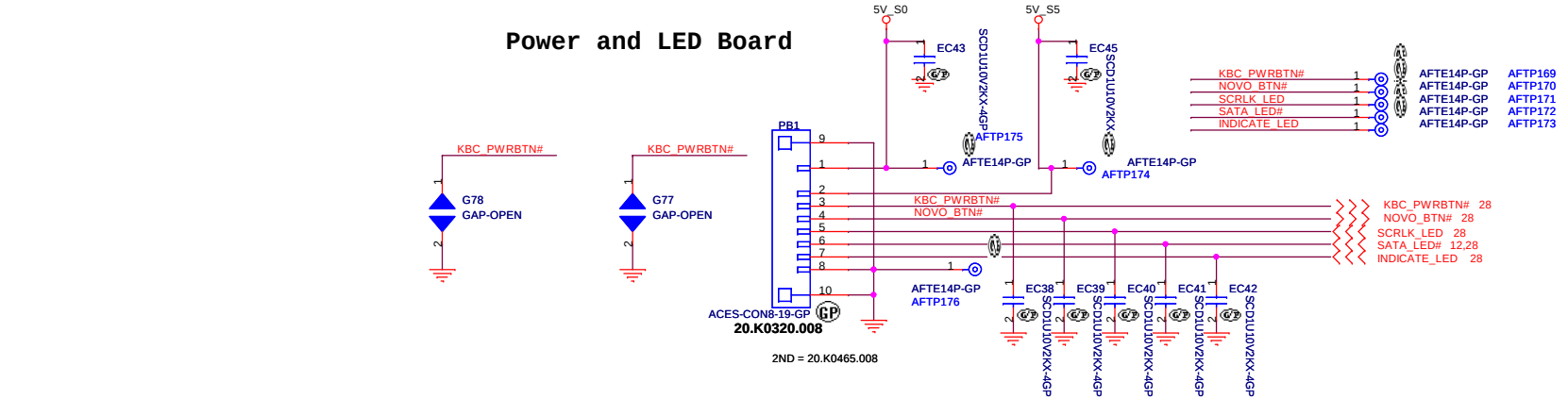
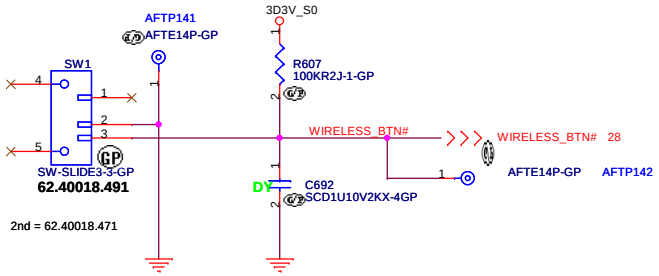
Power and LED Board





<Core Design>

緯創資通 **Wistron Corporation**
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Title	Power Board	
Size	Document Number: LB46E	Rev: SB
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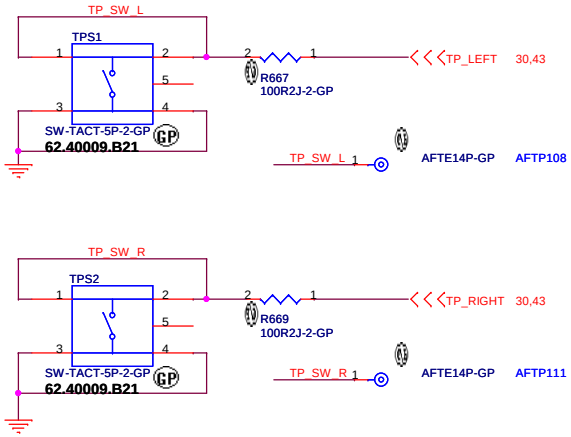
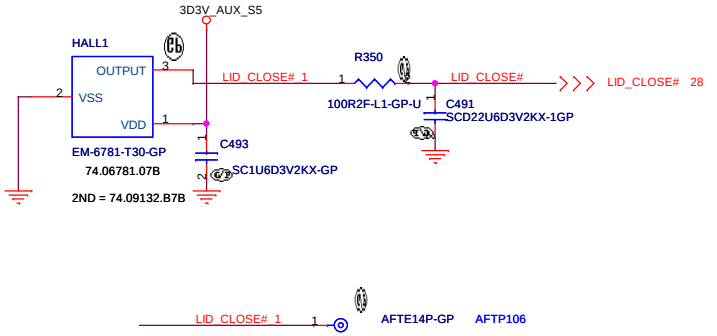
Cover Up Switch





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	SWITCHS	
Size	Document Number: LB46E	Rev: SB
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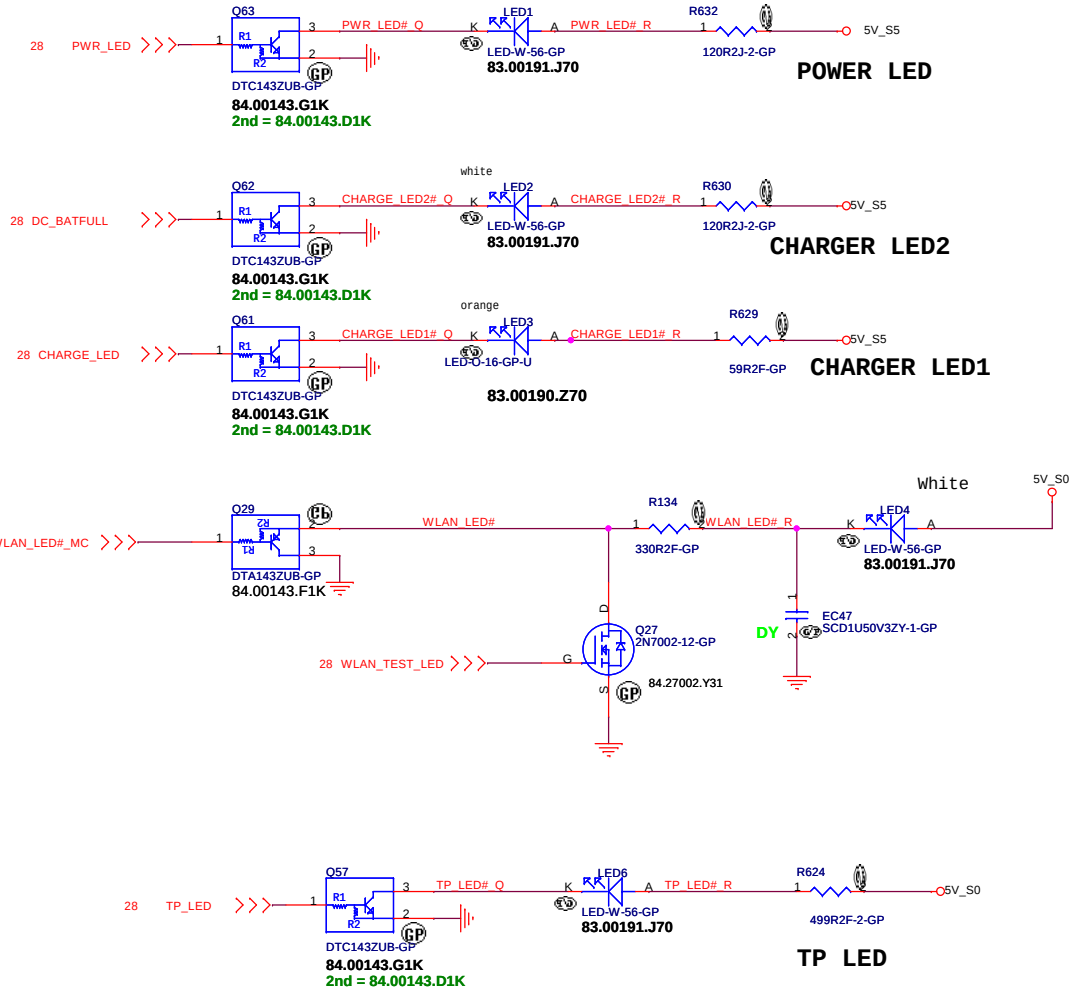

<Core Design>

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Title: LED

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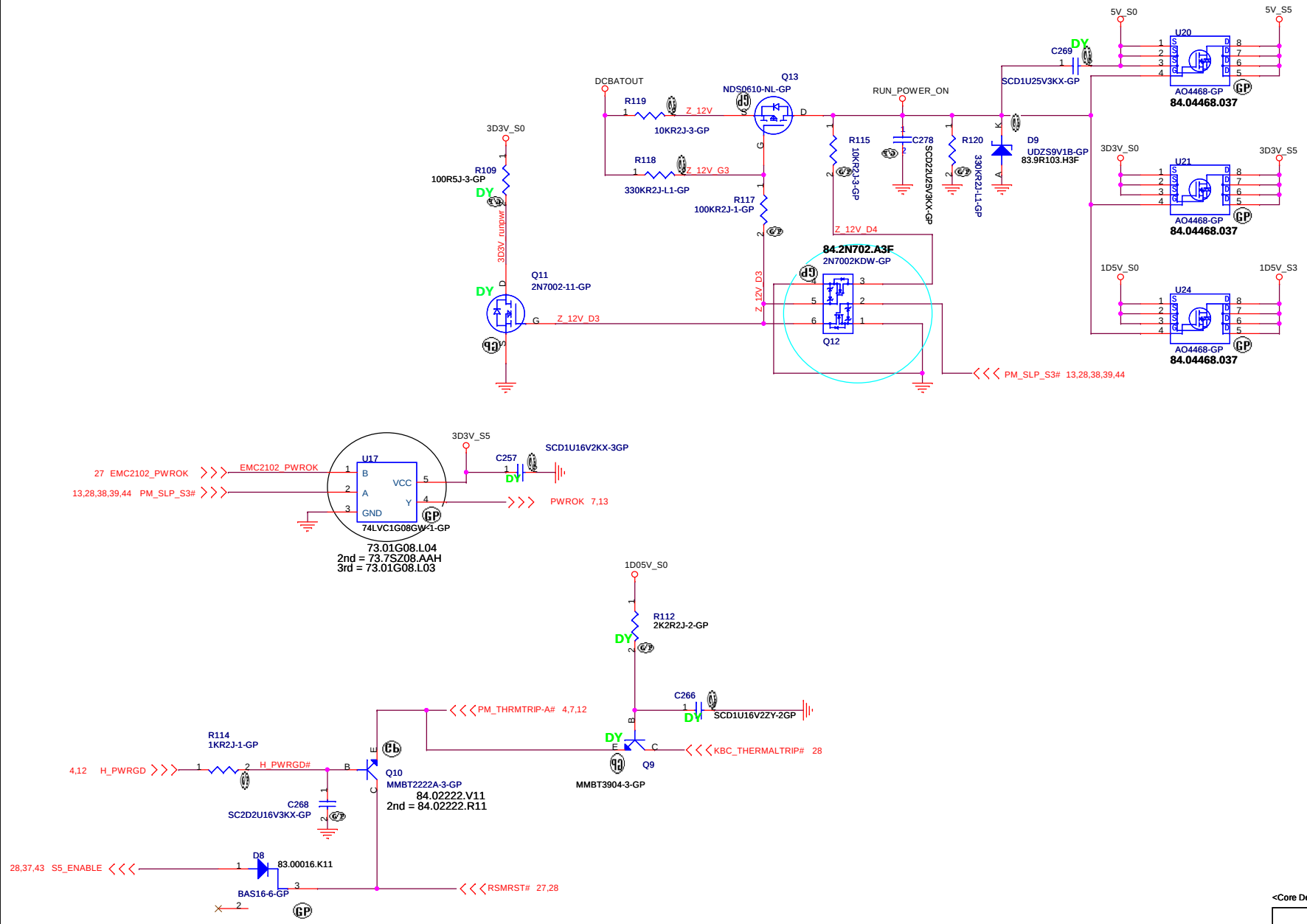
Run Power



<Core Design>

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Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: LB46E	Rev: SB
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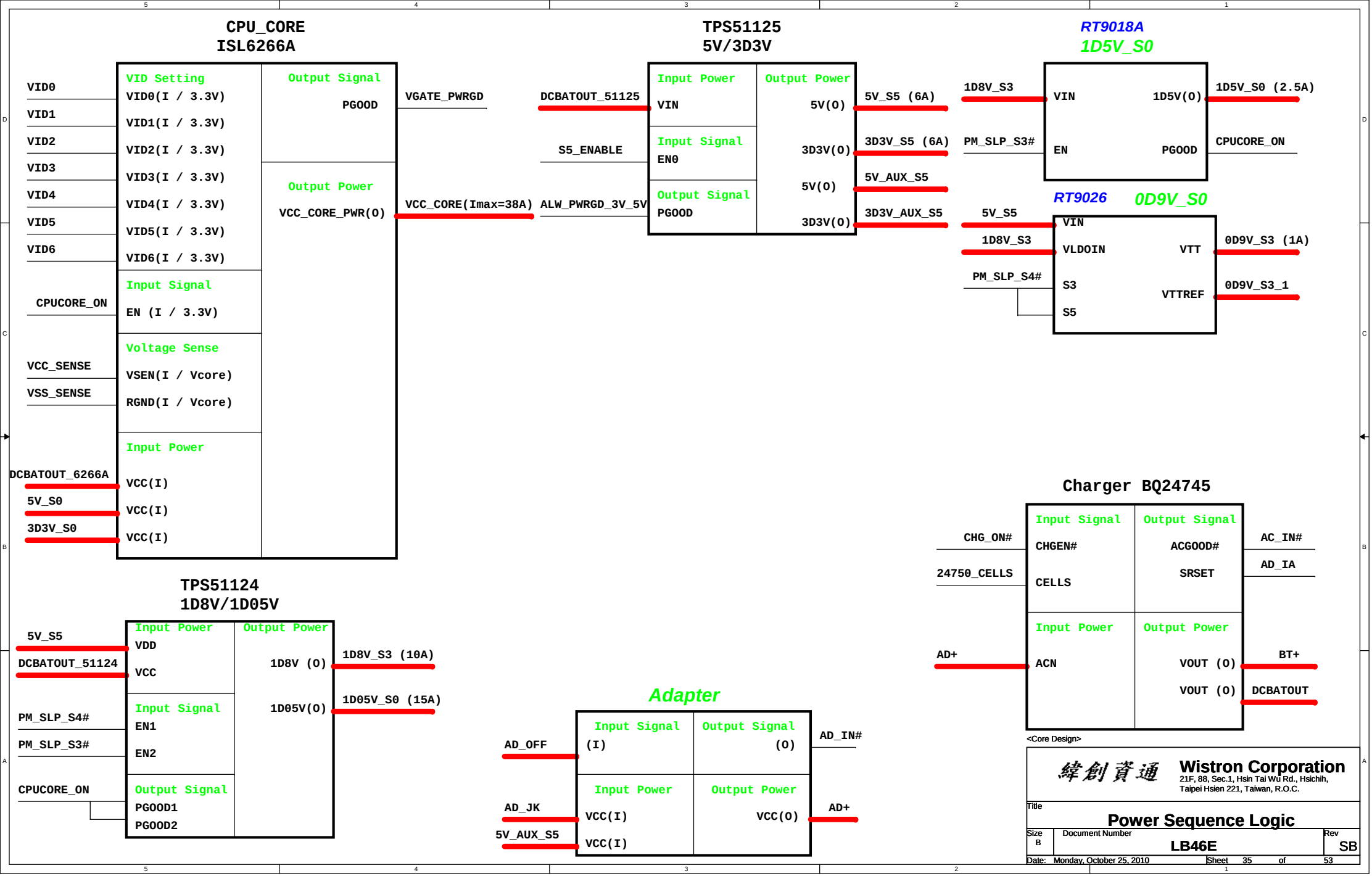

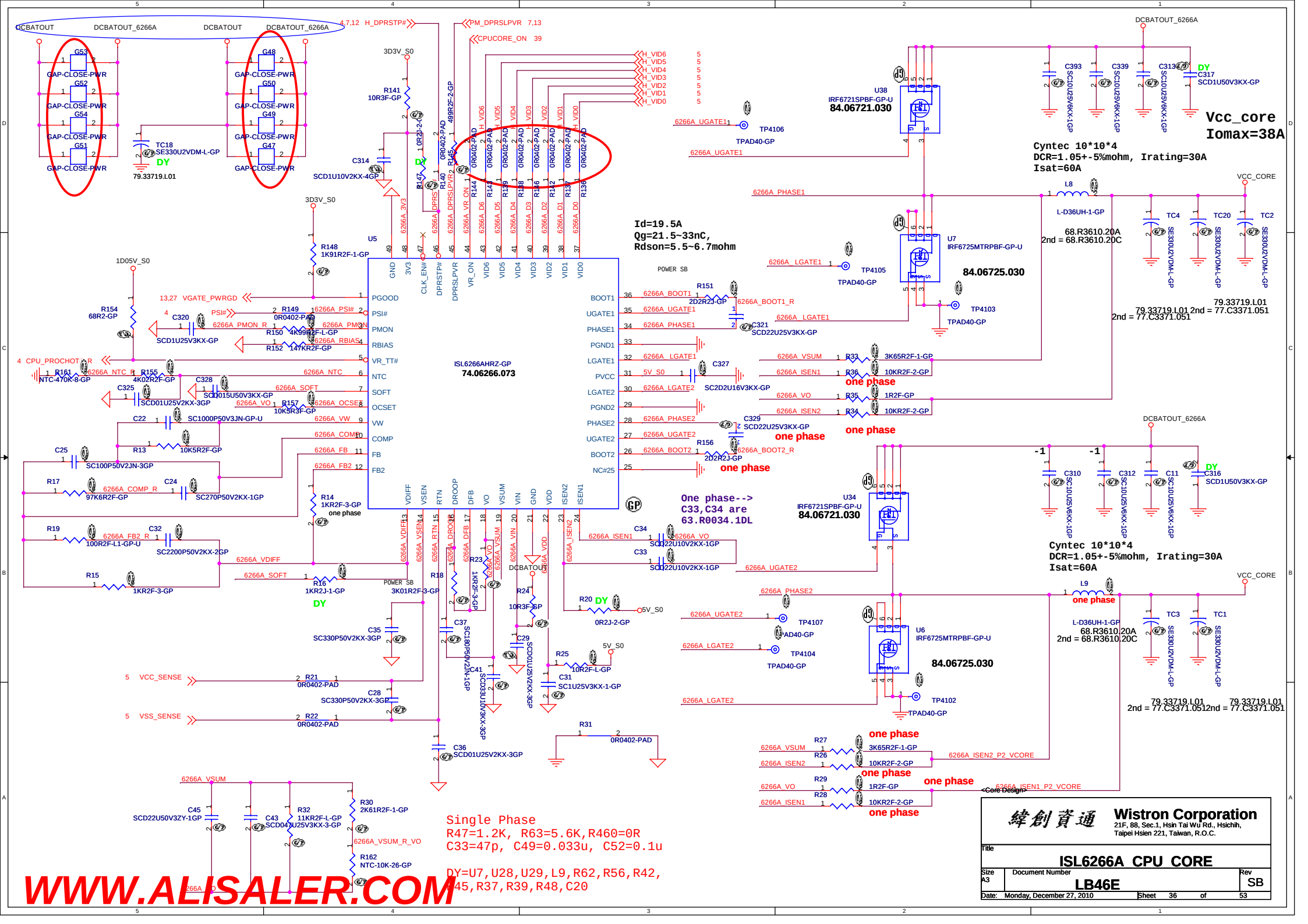
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74.06266.073
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Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
84.06721.030
84.06725.030
One phase-->
C33,C34 are
63.R0034.1DL
Single Phase
R47=1.2K, R63=5.6K,R460=0R
C33=47p, C49=0.033u, C52=0.1u
DY=U7,U28,U29,L9,R62,R56,R42,
R45,R37,R39,R48,C20
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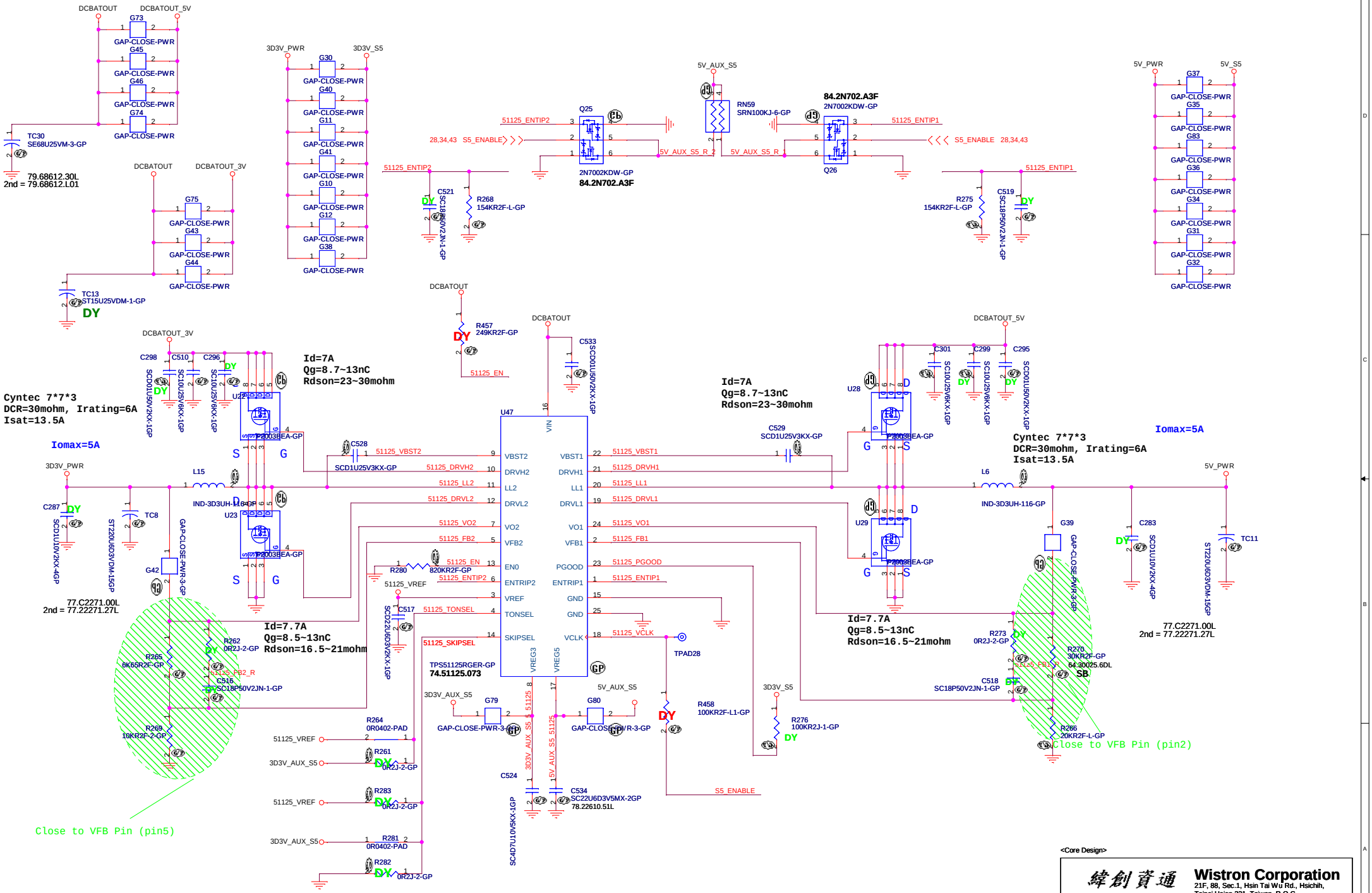
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
LB46E
Monday, December 27, 2010



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC 5V/3D3V (TPS51125)

Size	Document Number	Rev
Custom	LB46E	SB

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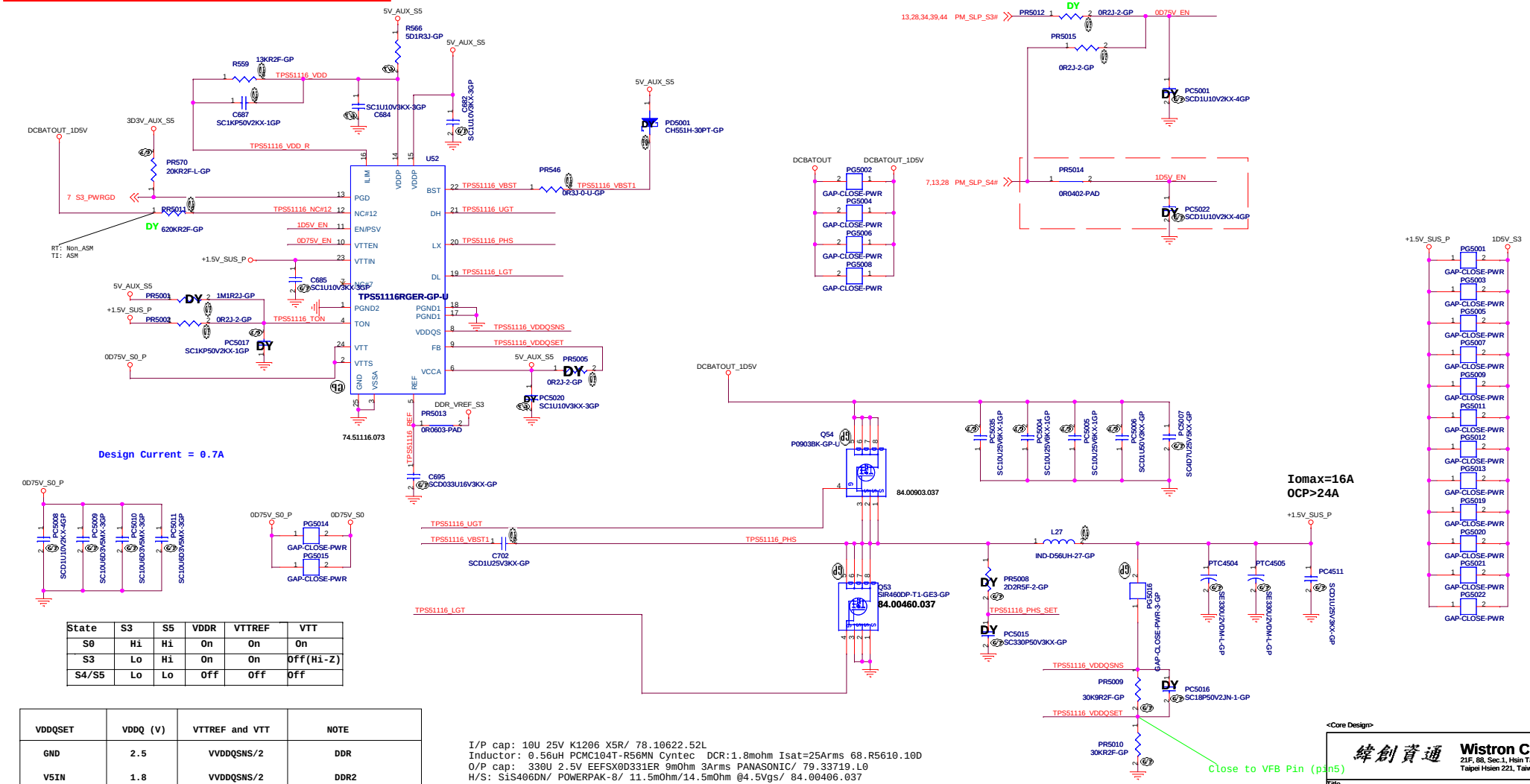
SSID = PWR.Plane.Regulator_1p5v0p75v



Design Current = 0.7A

Iomax=16A
OCP>24A

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
Switching freq-->400KHz

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51116_+1.5V_S3
Size: Custom | Document Number: LB46E | Rev: SB
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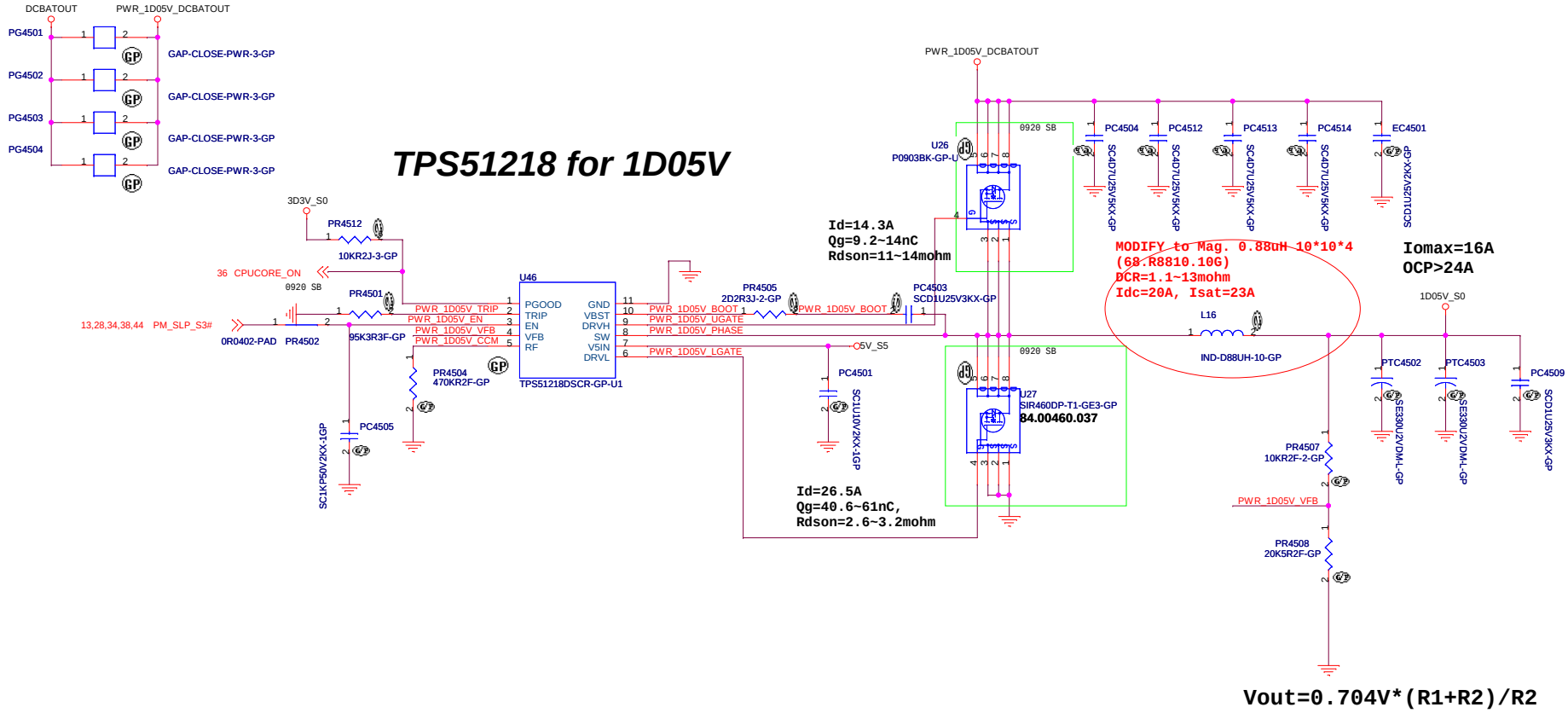
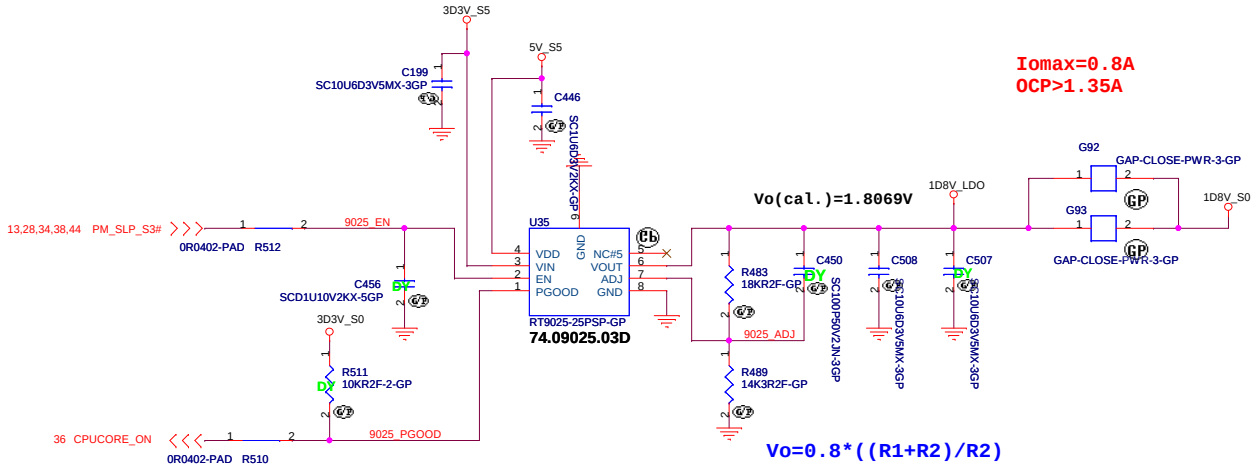


RT9025 for 1D8V_S0



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緯創資通 Wistron Corporation
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Title	DC/DC_1D05V_TPS51218	
Size	Document Number LB46E	Rev SA
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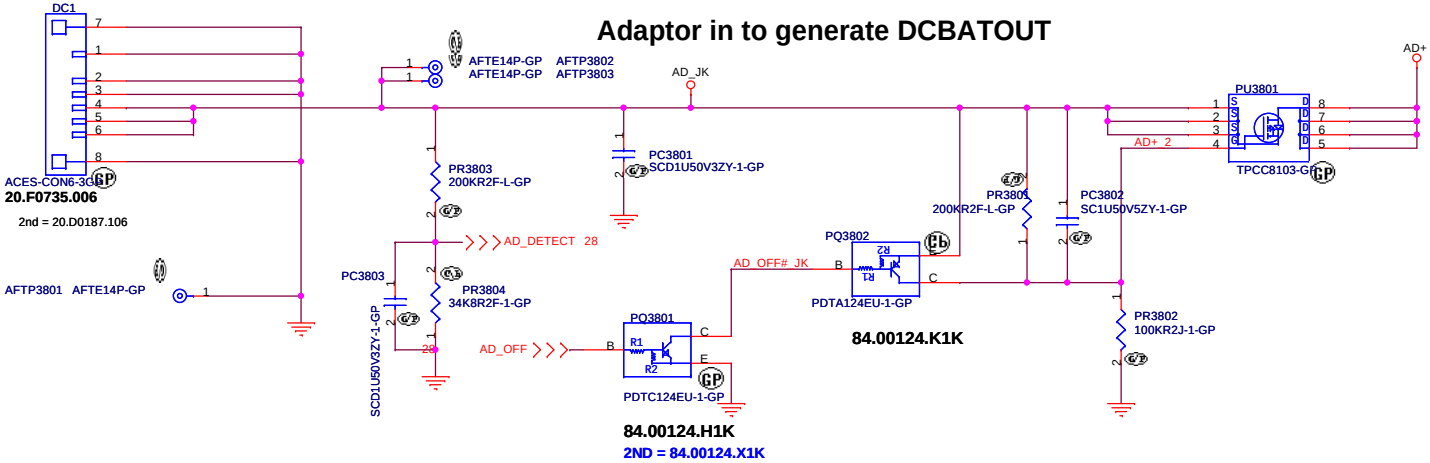
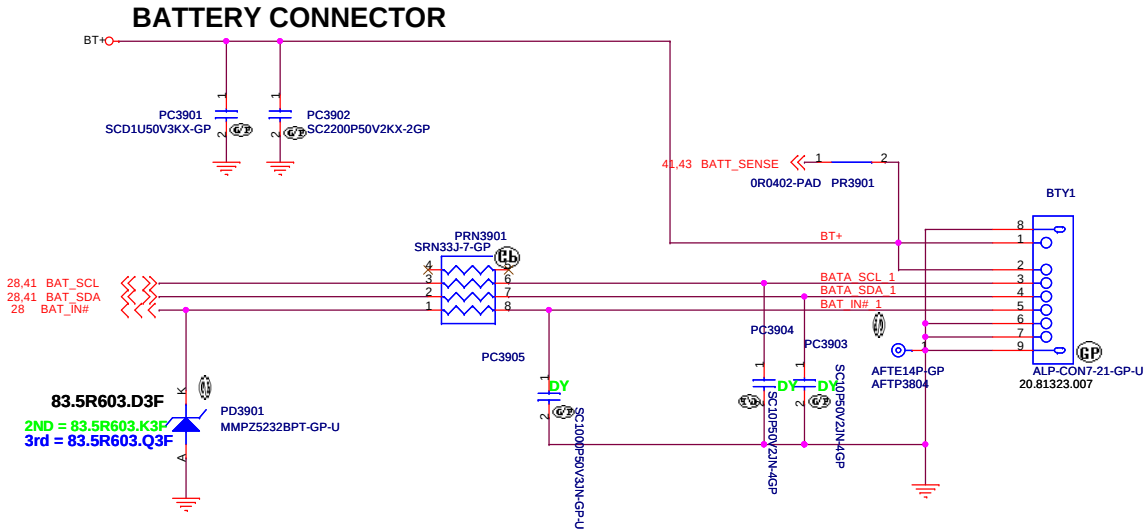
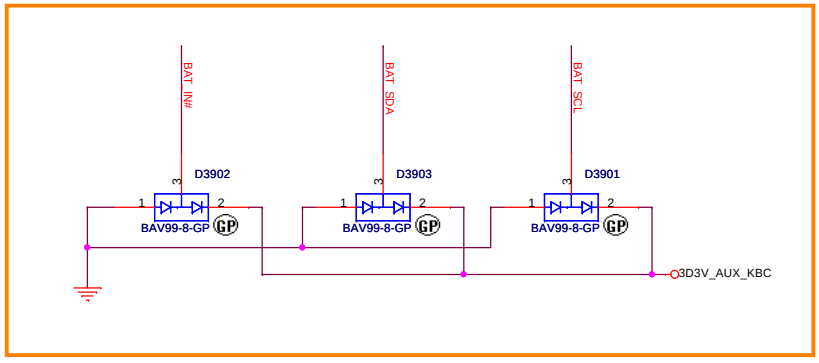


BATA_SDA_1 43
BATA_SCL_1 43
BAT_IN#_1 43
BATT_SENSE 41,43





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Title: AD/BATT CONN

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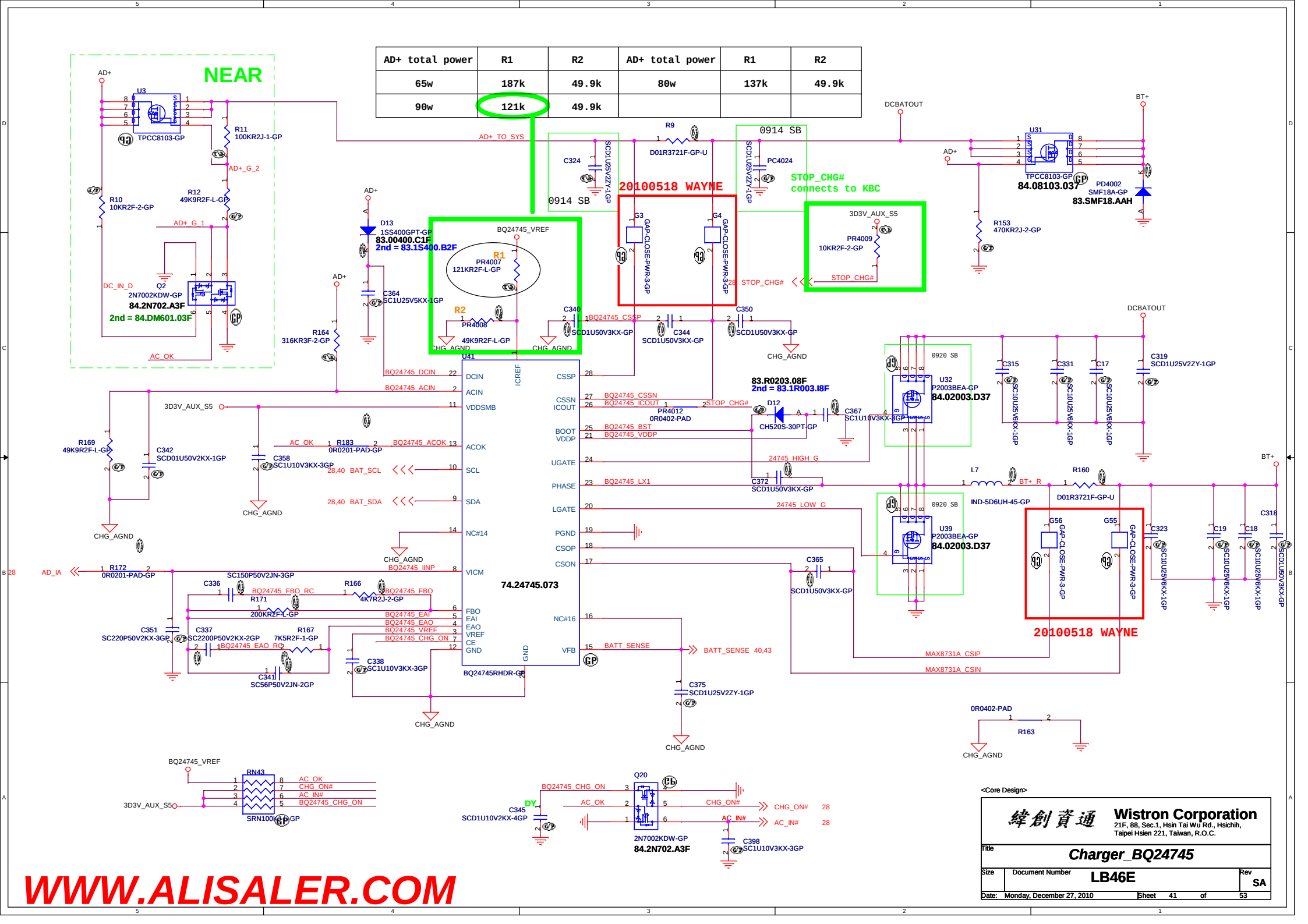
AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24745

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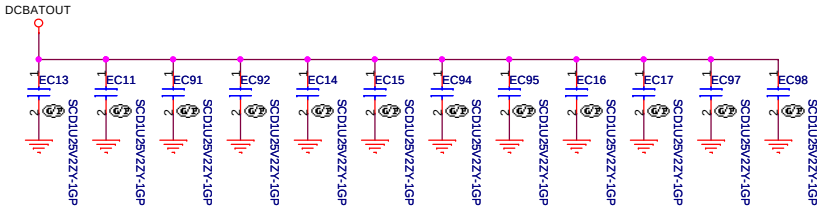

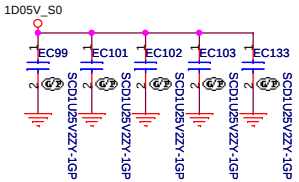

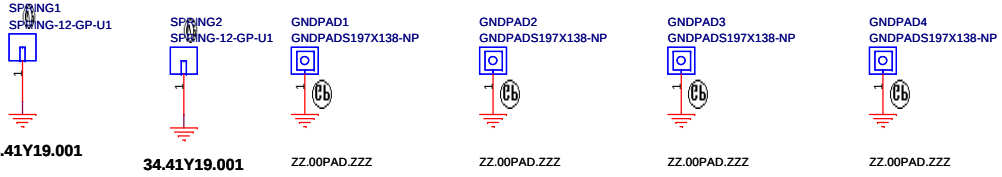

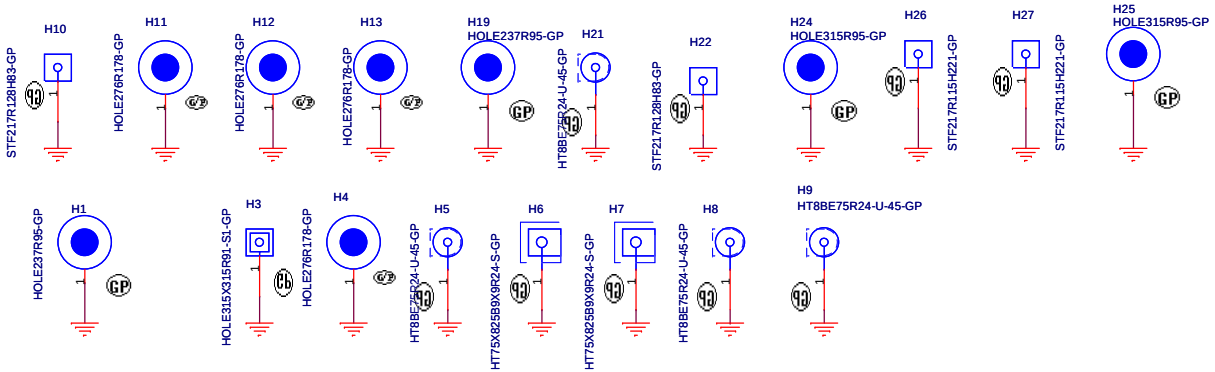

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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

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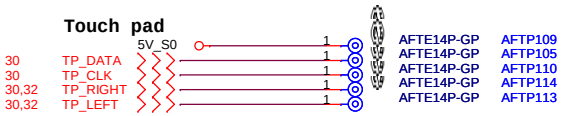

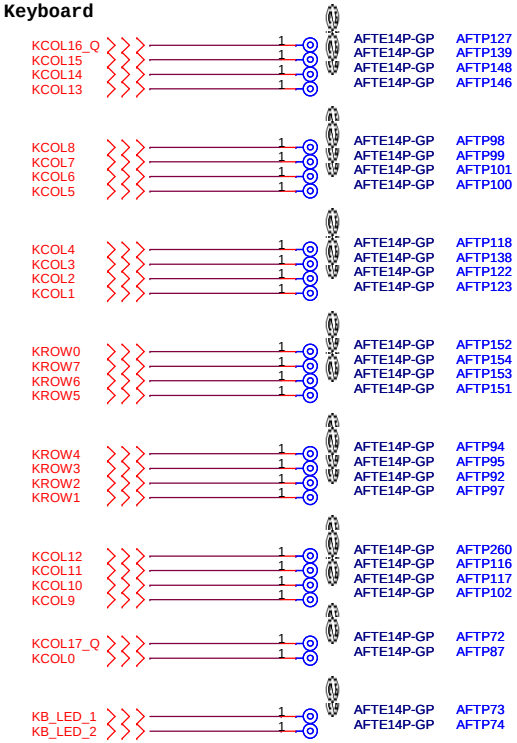

Check test point

Test Point locate near DIMM Door where can be tested

<Core Design>

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Title: **AFTE test point**

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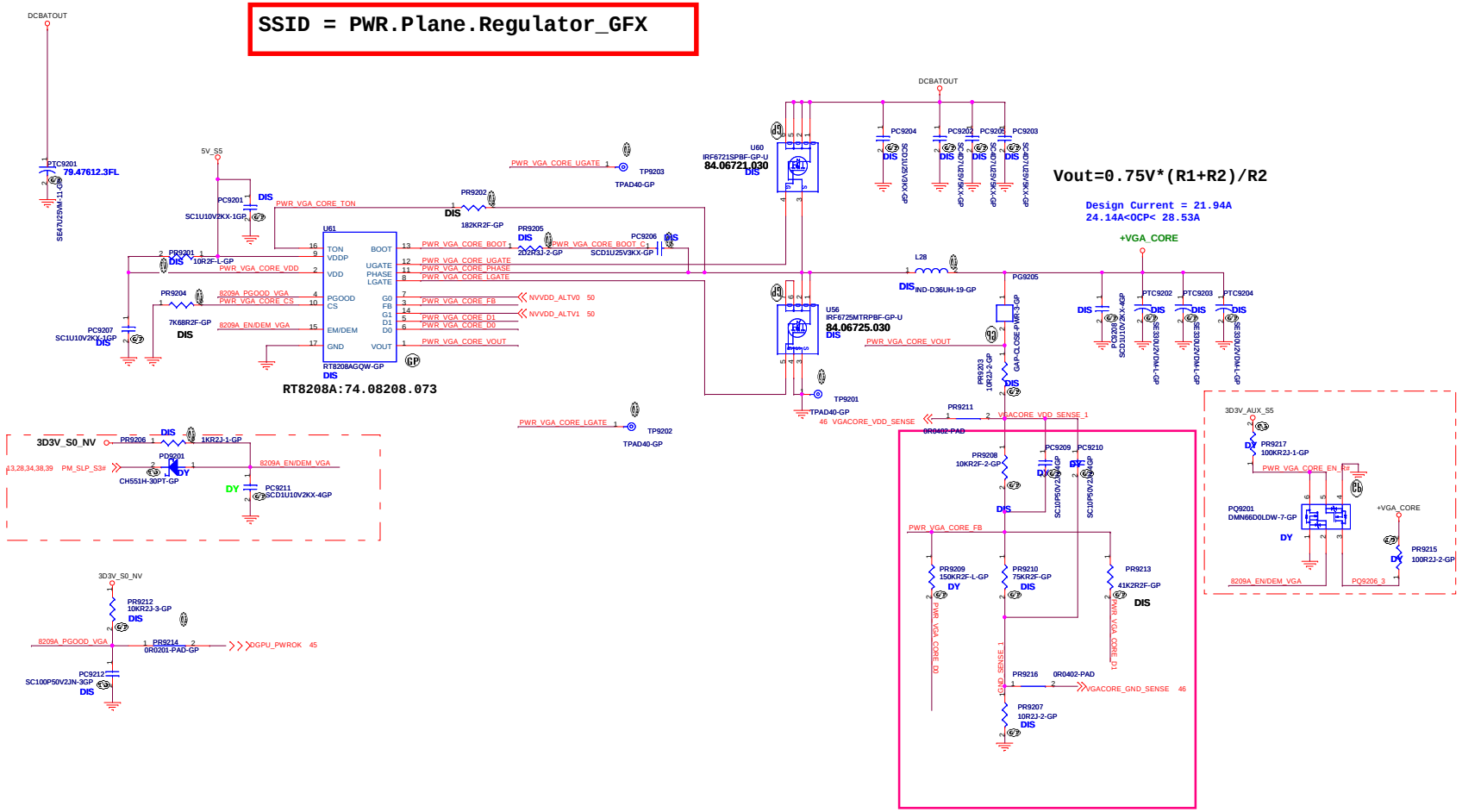
SSID = PWR.Plane.Regulator_GFX



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Title: DC/DC_VGA CORE_RT8208B

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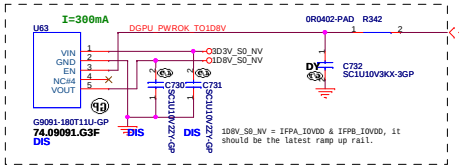
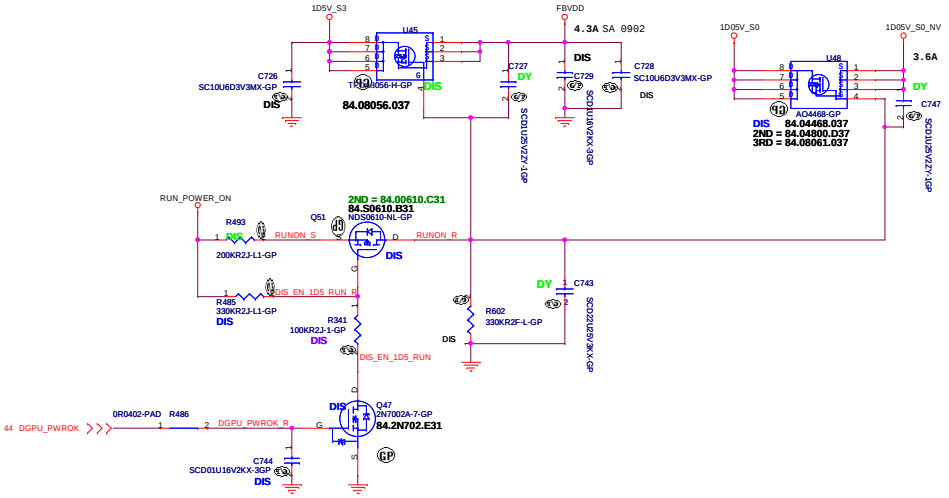
Del +3VS to 1.8V Transfer for OP 0119
+3VS to 1.8V Transfer



+1.5V to FBVDD Transfer

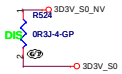
+1.05V to +1.05V_NV Transfer



+3VS to 3.3V_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C

Title: NV power

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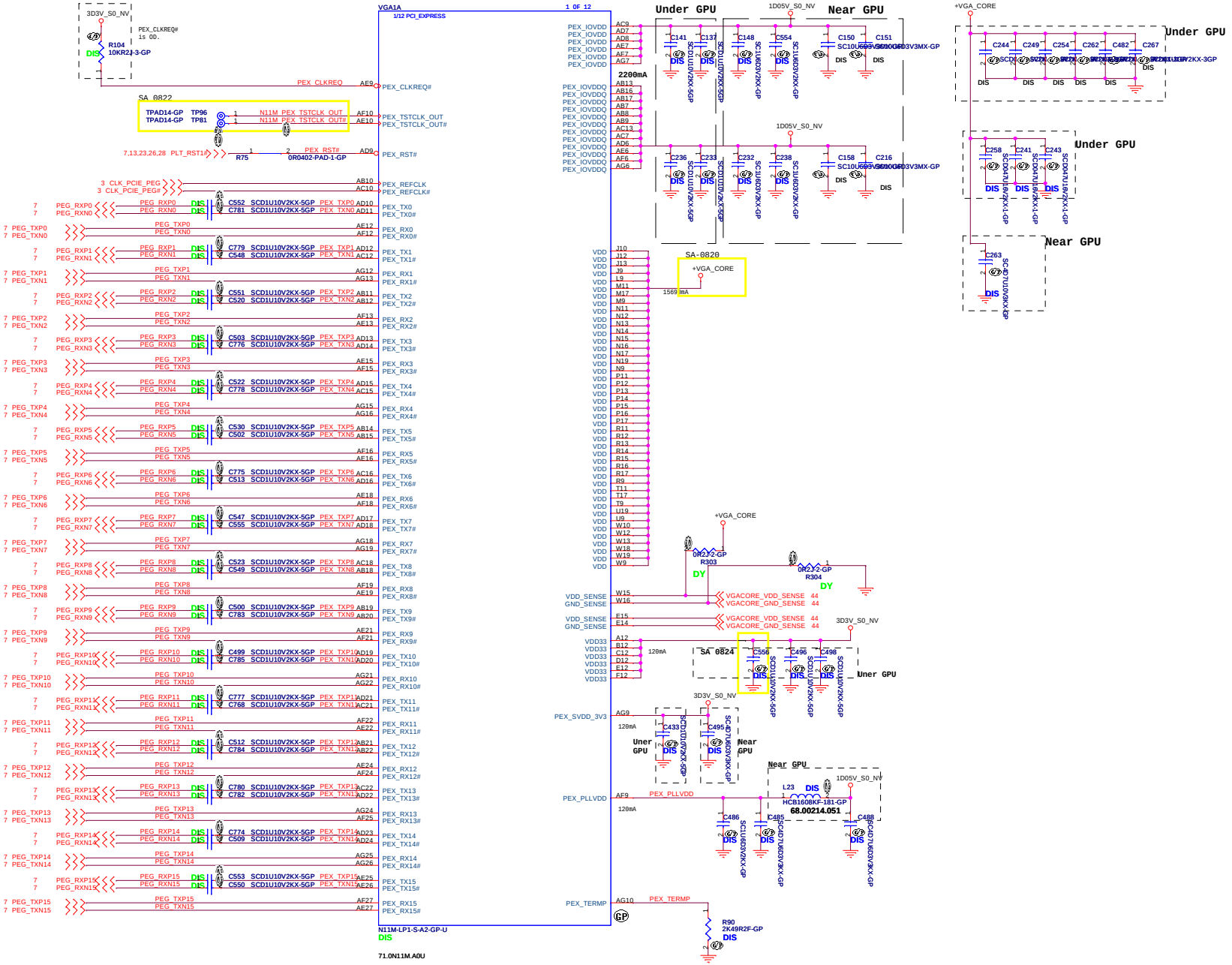
71.0N11M.C1U



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綽創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: N11M(1/6)_PEG

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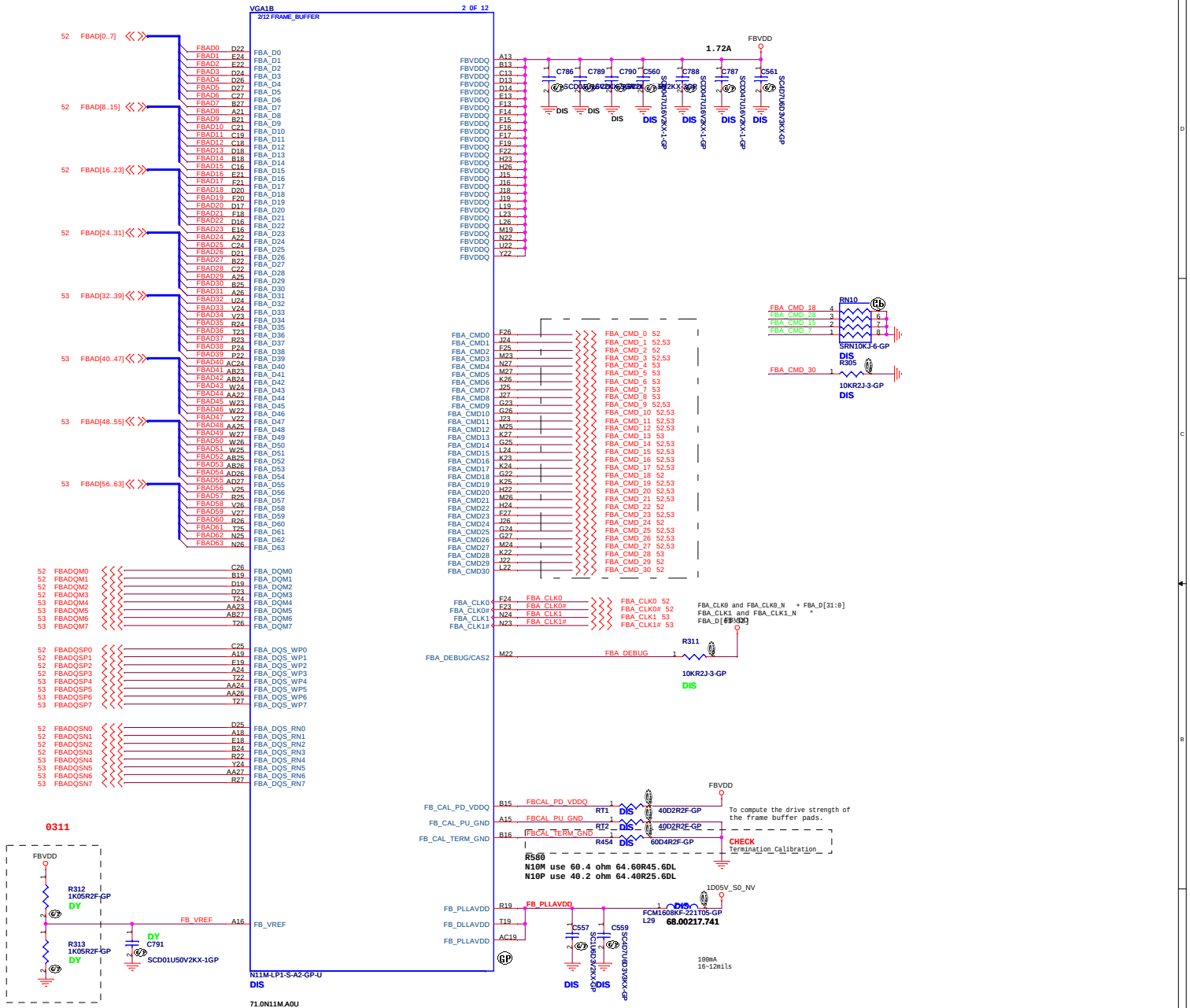

<Core Design>

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Title: 52_N11M(2/6)_MEMORY

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Custom	LB46E	SA

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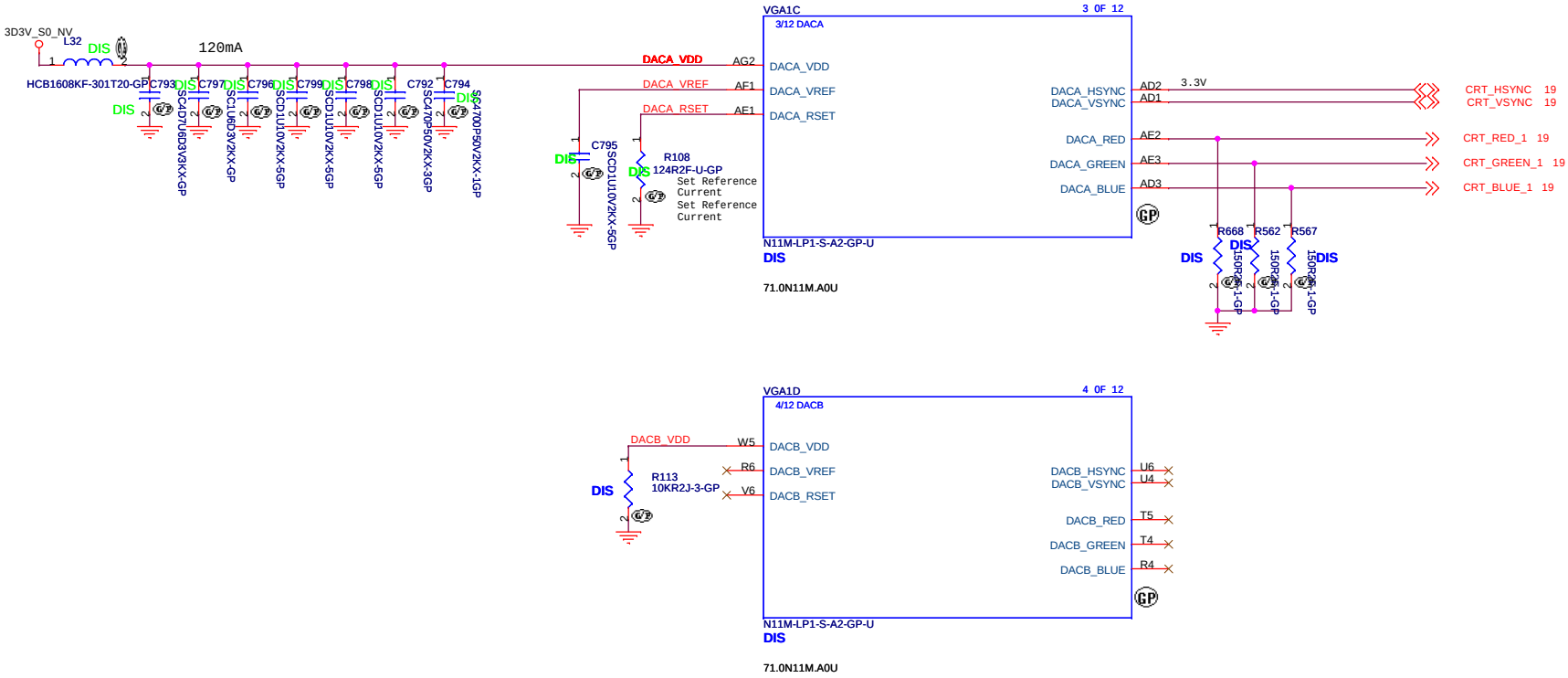

<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	N11M(3/6)_DAC
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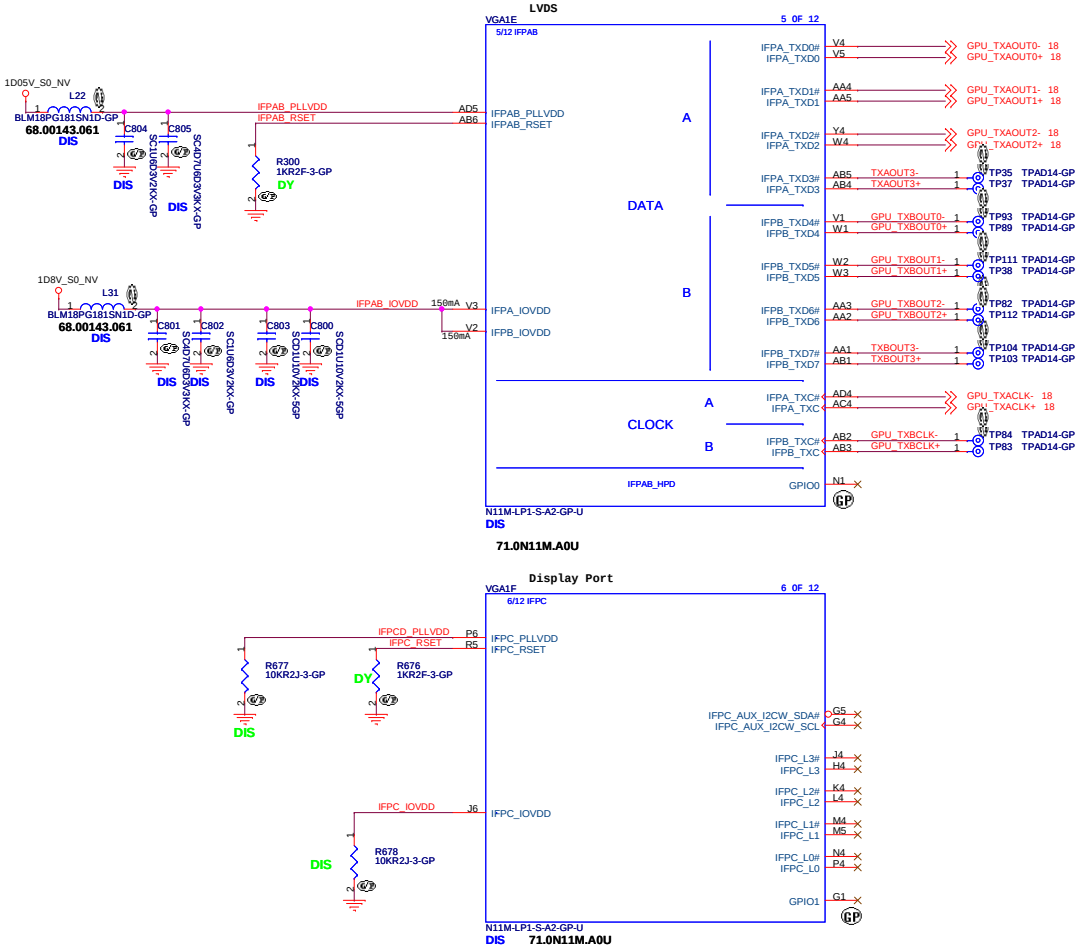

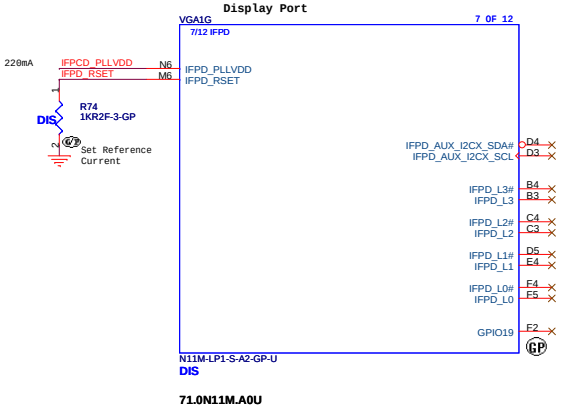

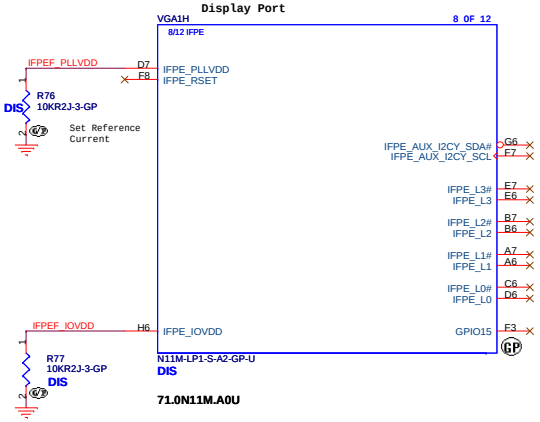

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Taipei Hsien 221, Taiwan, R.O.C.

Title: N11M(4/6)

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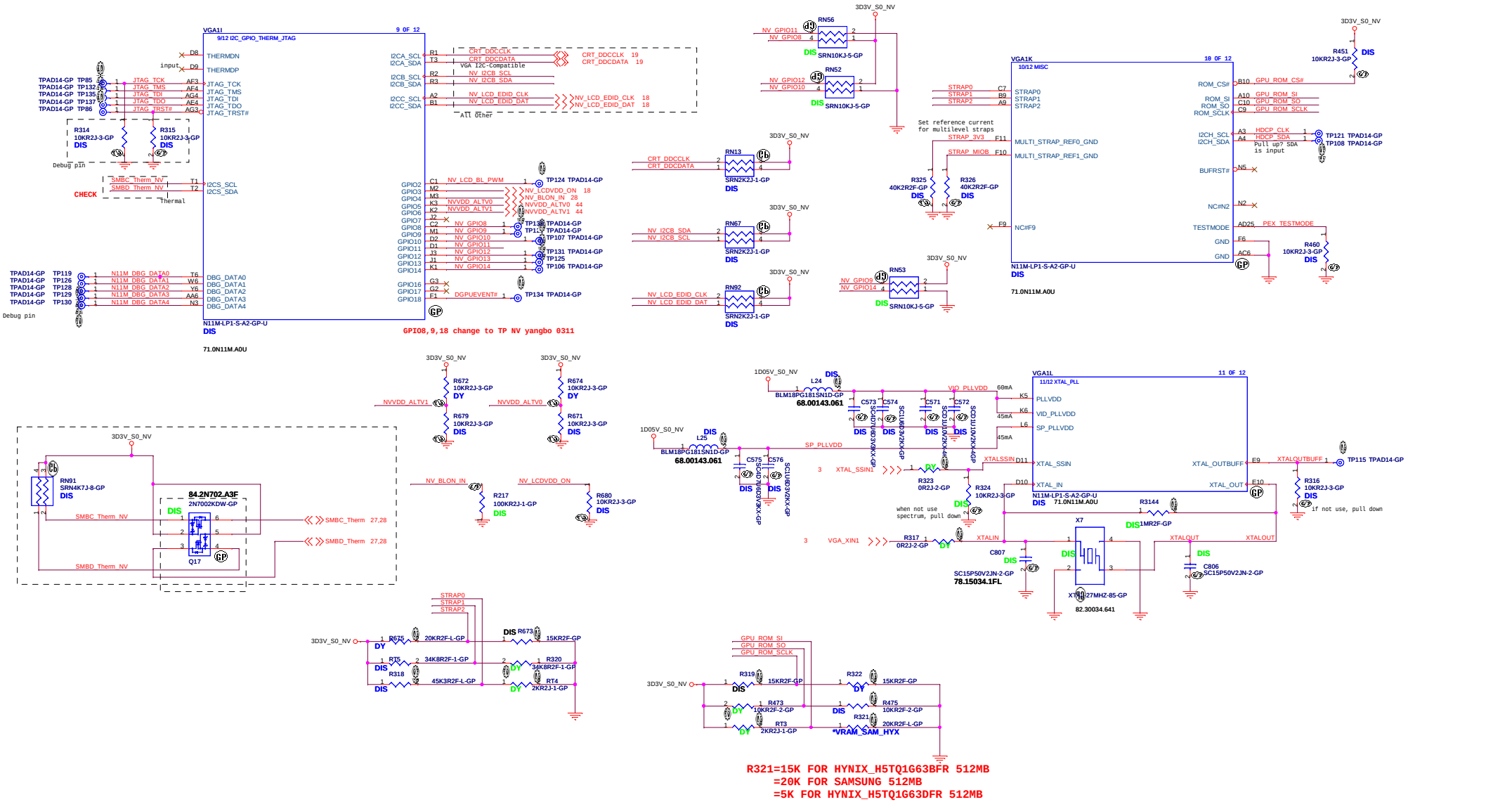

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: N11M(5/6)_MIO/ GPIO

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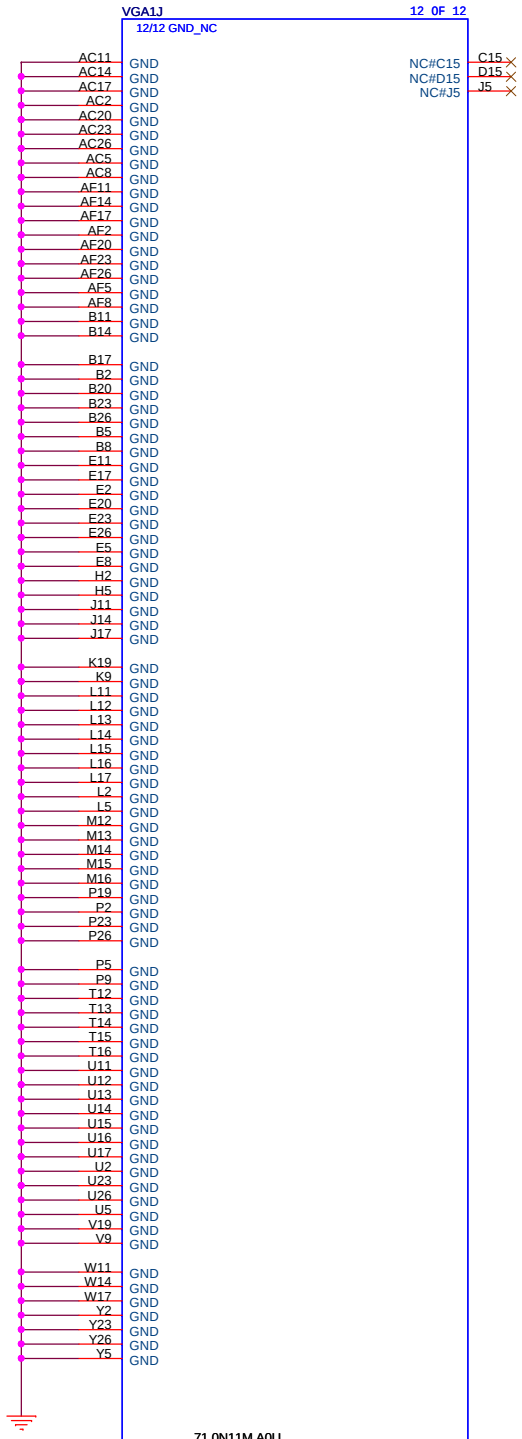

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Taipei Hsien 221, Taiwan, R.O.C.

Title: N11M(6/6)_POWER

Size	Document Number	Rev
Custom	LB46E	SA

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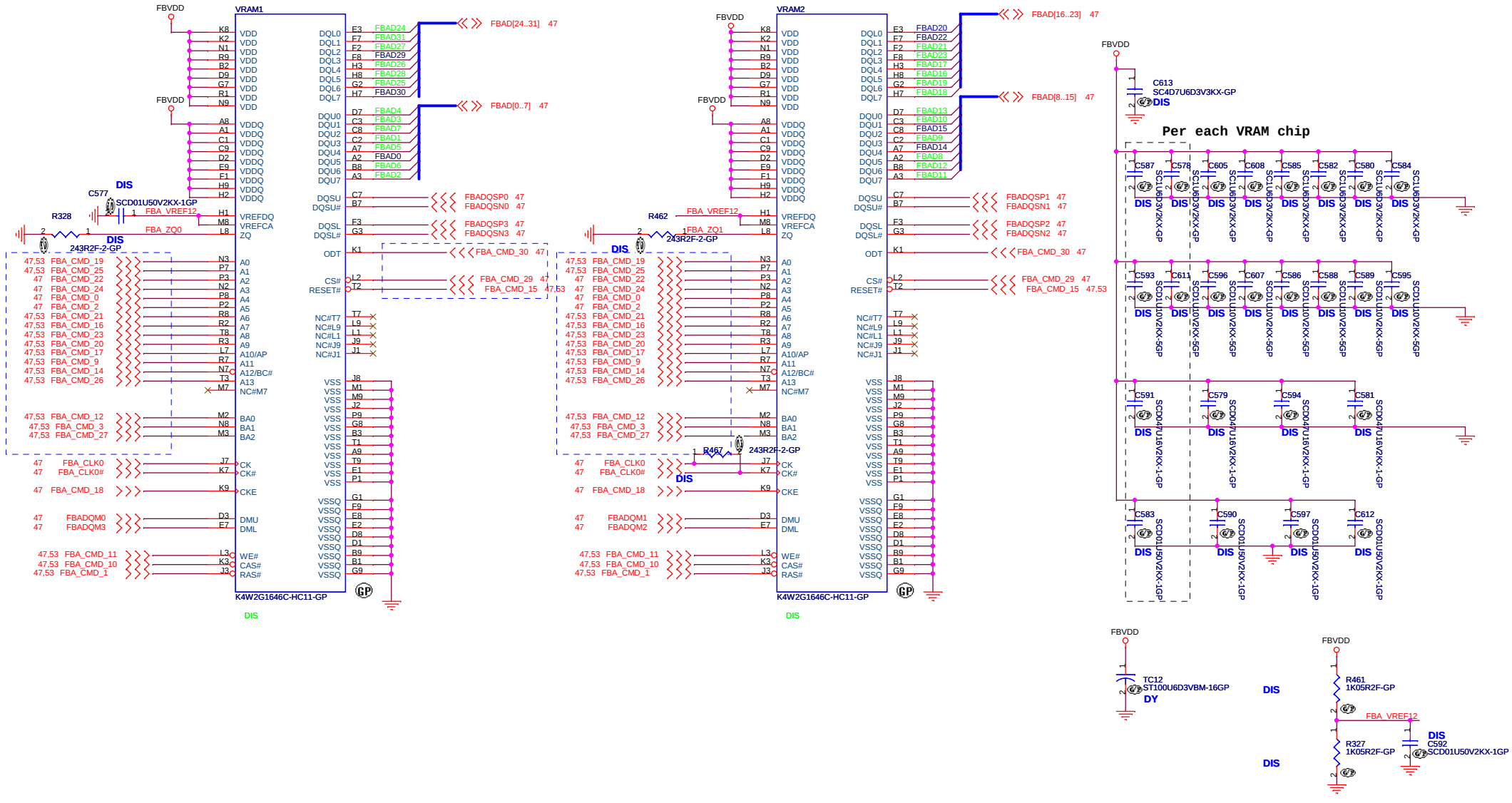

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(1/4)**

Size: Custom | Document Number: **LB46E** | Rev: **SA**

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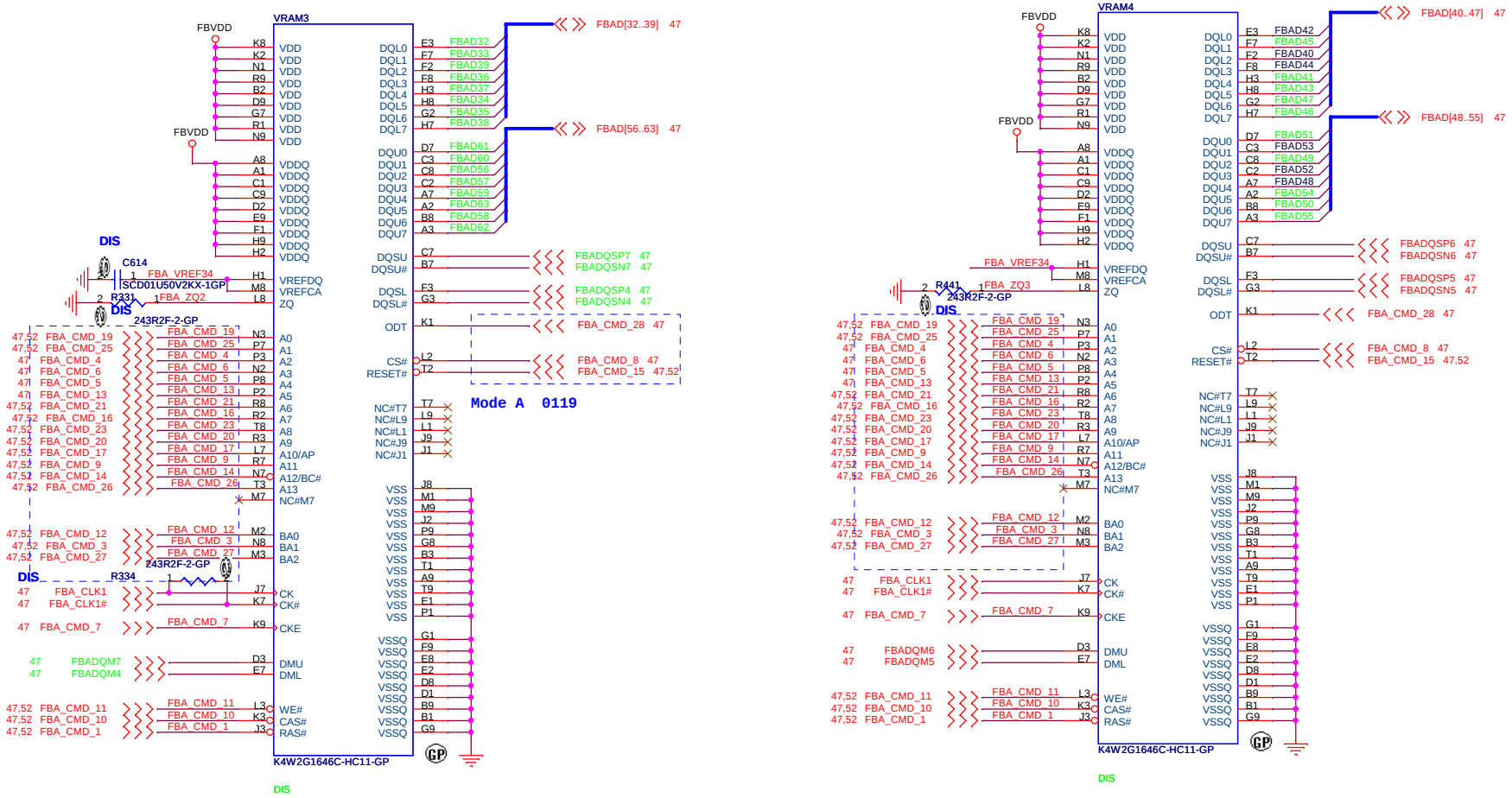

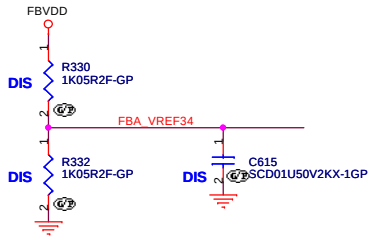

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(2/4)***	
Size A3	Document Number **LB46E**	Rev **SA**
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