LA14 Block Diagram

Project code: 91.4BW01.001
PCB P/N : 48.4BW01.01M
REVISION : SA

CLK GEN.
ICS 9LPRS365BKLFT (71.09365.A03)
SILEGO SLG8SP513VTR(71.08513.003)
3

Mobile CPU
Penryn 479
4, 5

THERMAL EMC2102
32

HOST BUS 667/800/1067MHz@1.05V

DDR2 DIMM1
667/800 MHz
16

DDR2 DIMM2
667/800 MHz
17

667/800MHz

667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

CRT 19

LCD 18

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
12,13,14,15

Codec
CX20561
26

AZALIA

MIC In
28

28
INT.SPKR

OP AMP
G1454
27

28
Line Out
(NO SPDIF)

PCIex1

LAN
Atheros
AR8114
AR8132
24

TXFM
25

RJ45
25

PCIex1

Mini Card
Kedron a/b/g/n
31

LPC BUS

KBC
KBC773L
33

BIOS
Winbond
W25X16
16M Bits
34

LPC
DEBUG
CONN
34

Touch Pad 35

INT. KB 33

Camera (USB) 18

USB

HDD SATA 20

SATA

ODD SATA 21

SATA

USB
4 Port 23

USB

CardReader
Realtek
RTS5159
30

MS/MS Pro/xD
/MMC/SD
5 in 1
30

Power Board
36

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
TPS51125 42

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC
TPS51124 44

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 43

1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 43

1D8V_S3	1D5V_S0

CPU DC/DC
ISL6266A 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER
BQ24745 46

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

<Core Design>

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: LA14 | Rev: SB
Date: Thursday, May 07, 2009 | Sheet 1 of 52

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

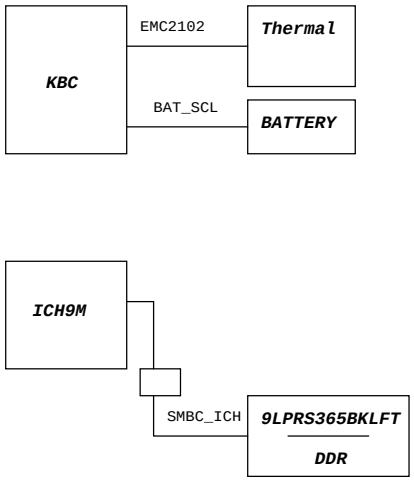
PCIE Routing

LANE1	LAN Atheros AR8114A
LANE2	MiniCard WLAN
LANE3	*NC*
LANE4	*NC*
LANE5	*NC*
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*NC*
2	*NC*
3	*MINIC1*
4	*WEBCAM*
5	*NC*
6	*NC*
7	*Bluetooth*
8	*NC*
9	*USB2(High speed)*
10	*NC*
11	*CardReader*

SMBus



<Core Design>
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Title: Reference
Size: A3 | Document Number: LA14 | Rev: SB
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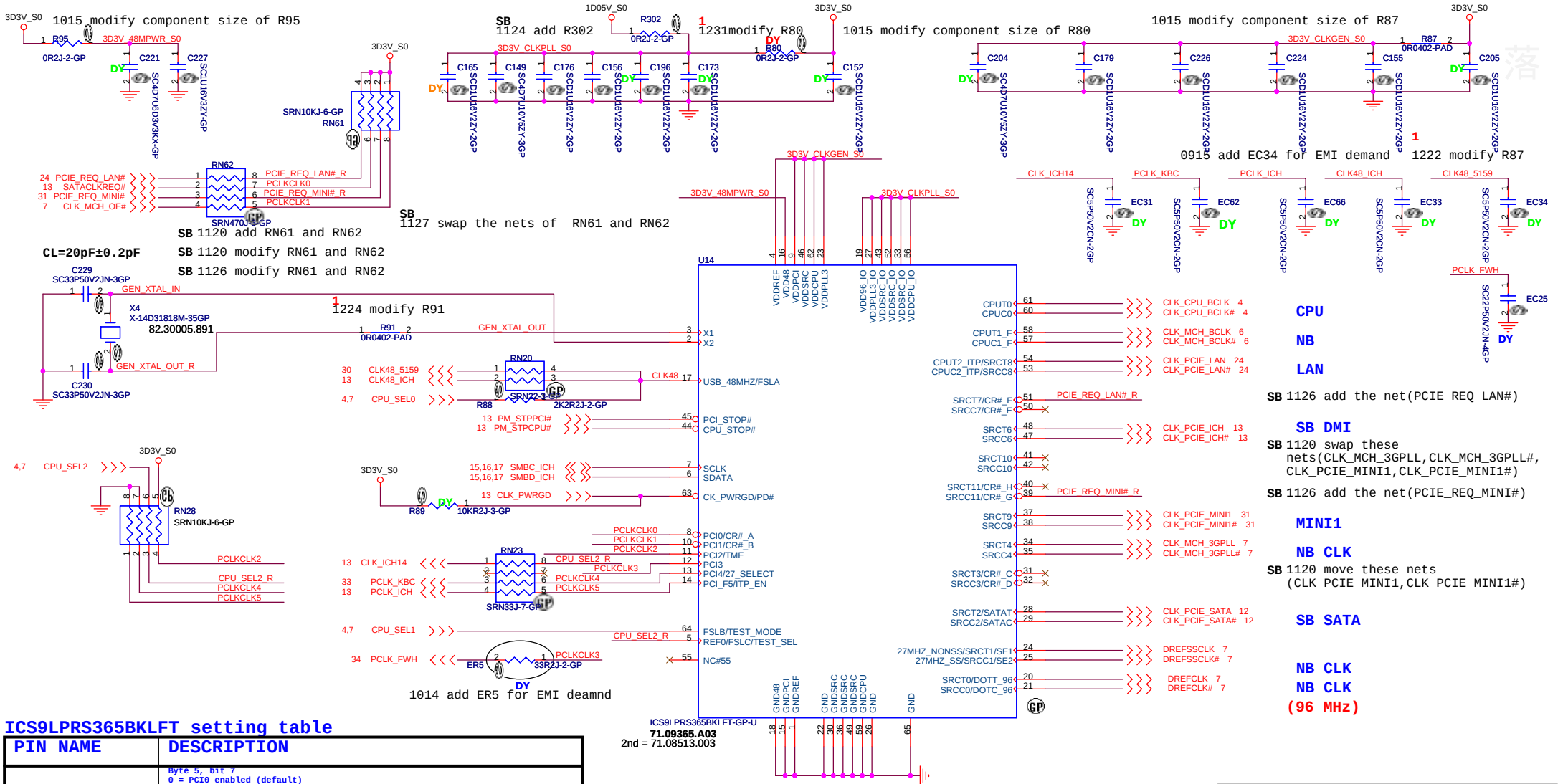

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

<Core Design>

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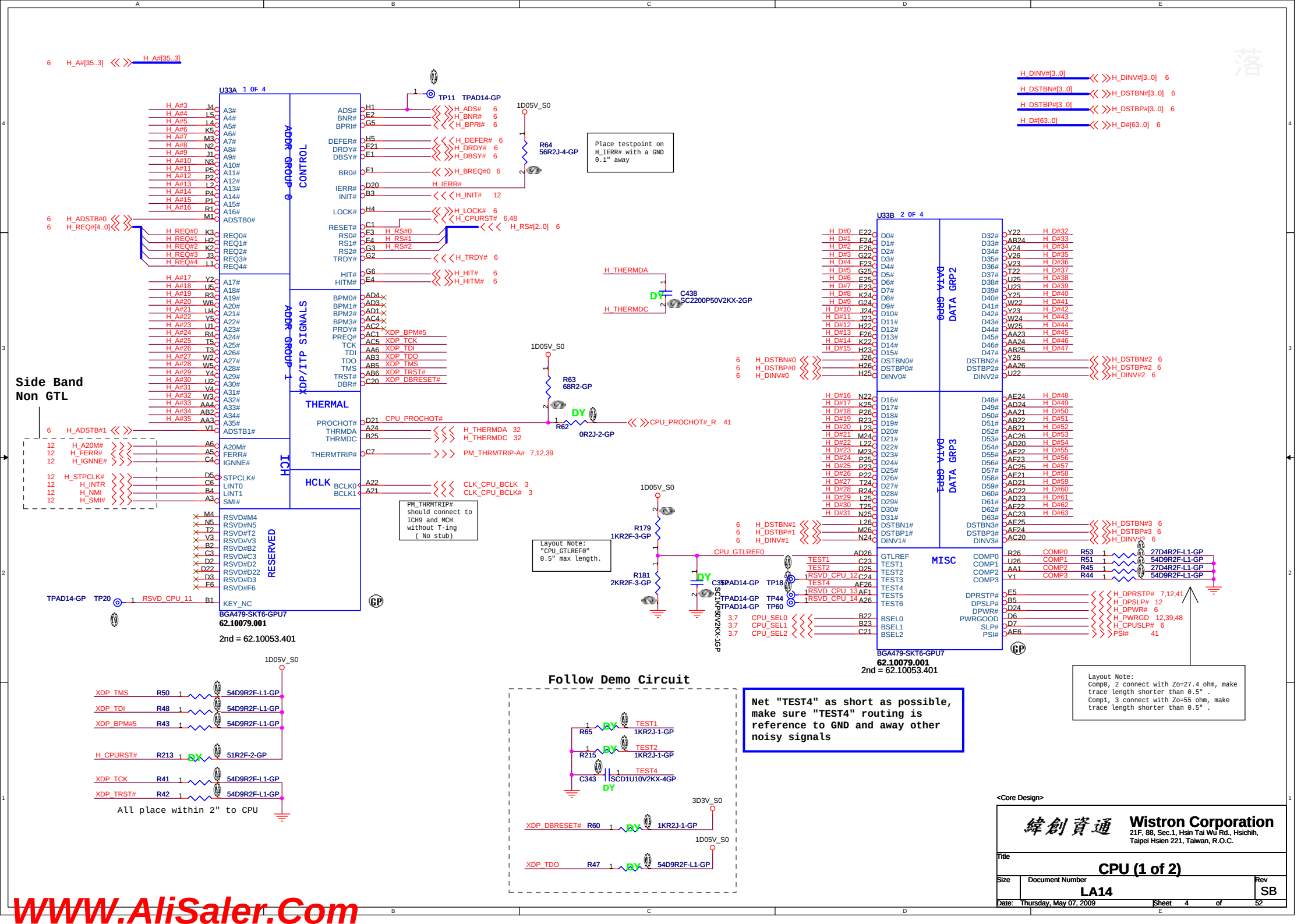
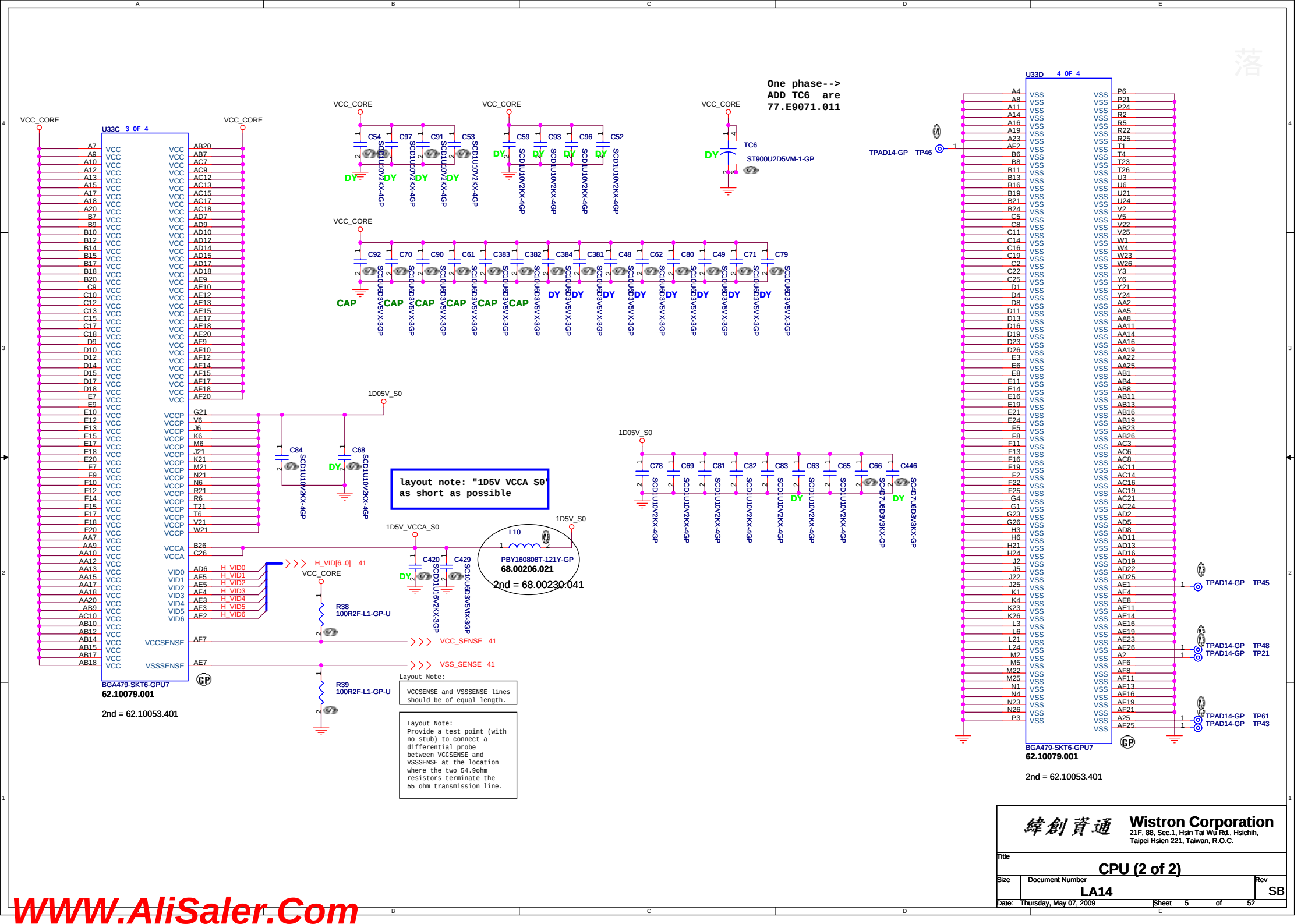
Title: Clock Generator

Size: | Document Number: LA14 | Rev: SB

Date: Thursday, May 07, 2009 | Sheet 3 of 52





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Title: CPU (2 of 2)

Size	Document Number	Rev
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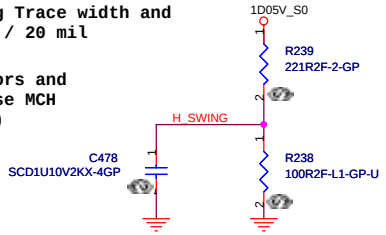
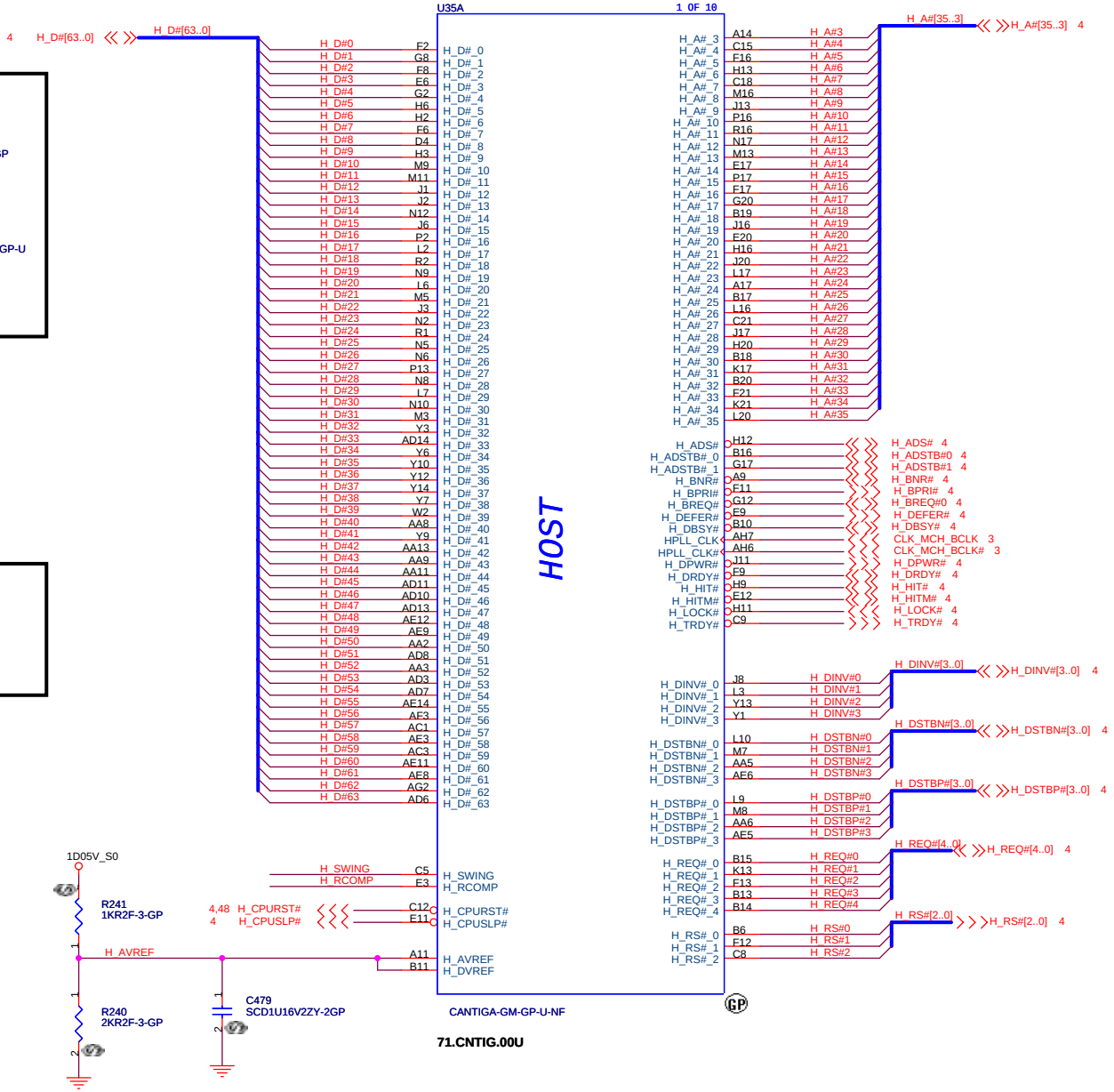
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



Place them near to the chip (< 0.5")

<Core Design>

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Title: Cantiga (1 of 6) HOST

Size	Document Number	Rev
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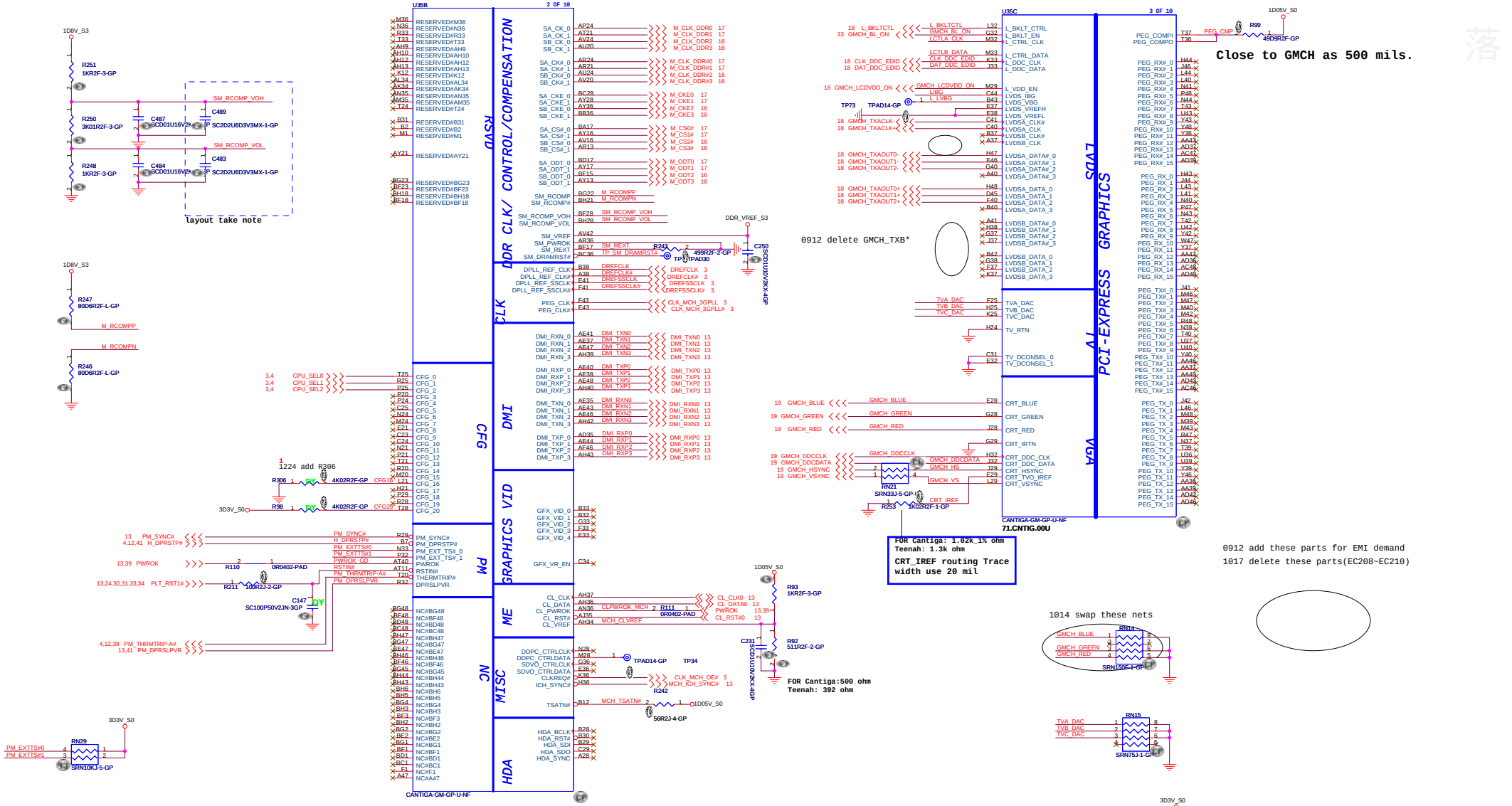

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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Title: Cantiga (2 of 6)_DMI/PM/CFG

Size: | Document Number: LA14 | Rev: SB

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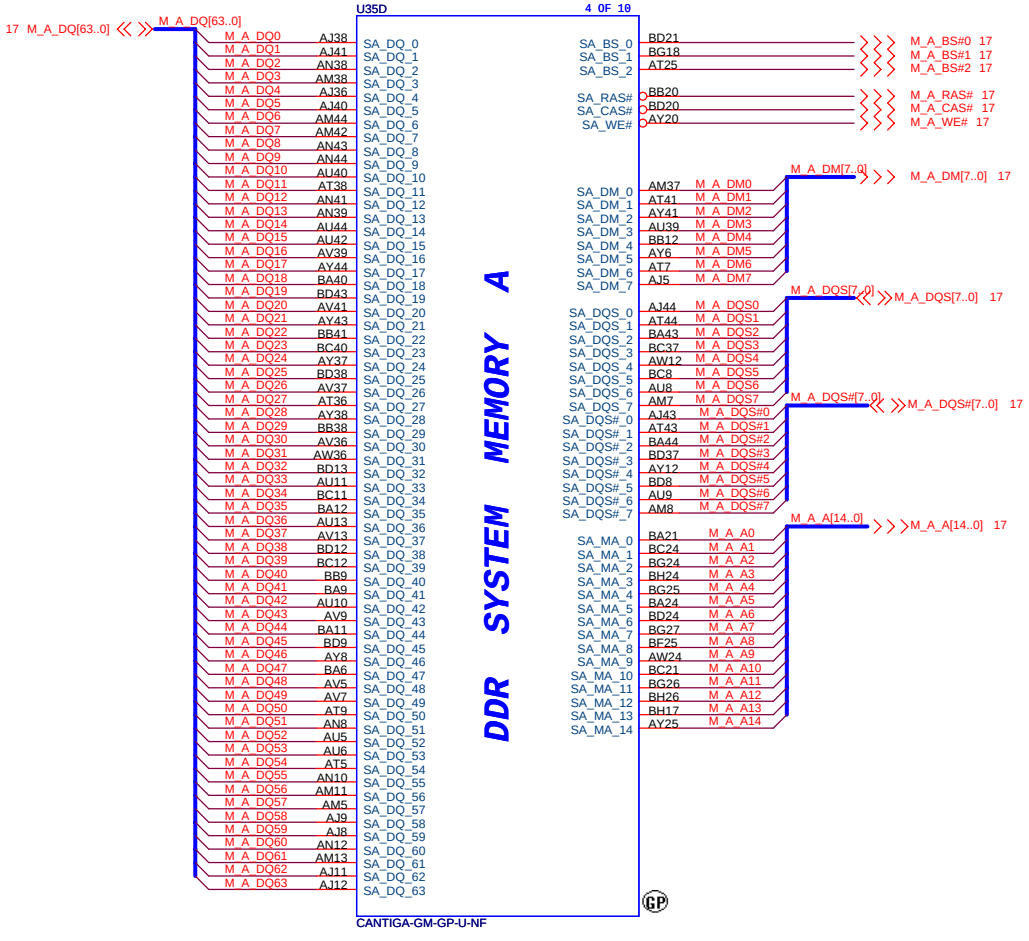

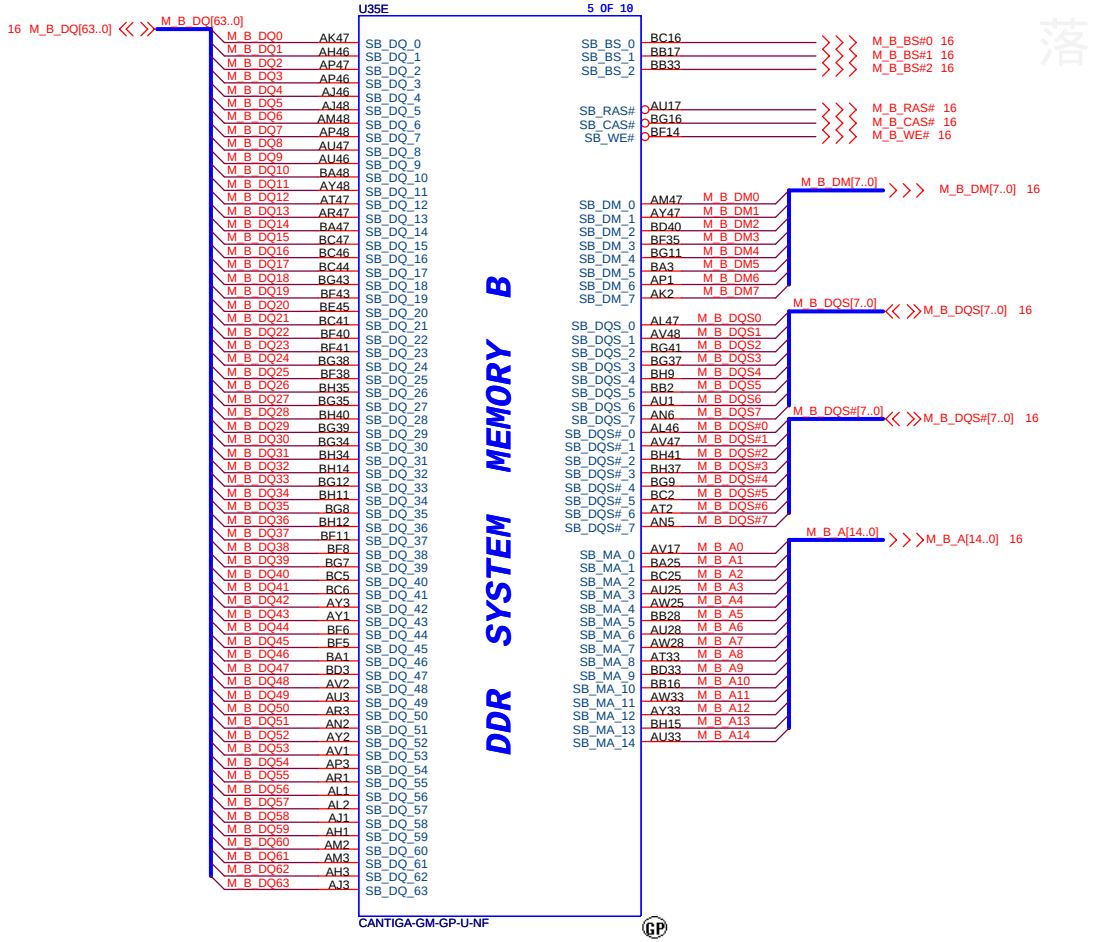

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Title: Cantiga (3 of 6) DDR

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667MTS 2400mA
800MTS 3000mA

U35G 7 OF 10

VCC SM POWER

VCC GFX NCTF

VCC GFX

VCC SM LF

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

Place CAP where LVDS and DDR2 taps

FOR VCC SM

Place on the Edge

place near Cantiga

SB 1118 delete TC27

Coupling CAP 370 mils from the Edge

Coupling CAP

GAP-CLOSE-PWR

U35F 6 OF 10

VCC CORE

POWER

VCC NCTF

CANTIGA-GM-GP-U-NF
71.CNTIG.00U

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Title	Cantiga (4 of 6) POWER
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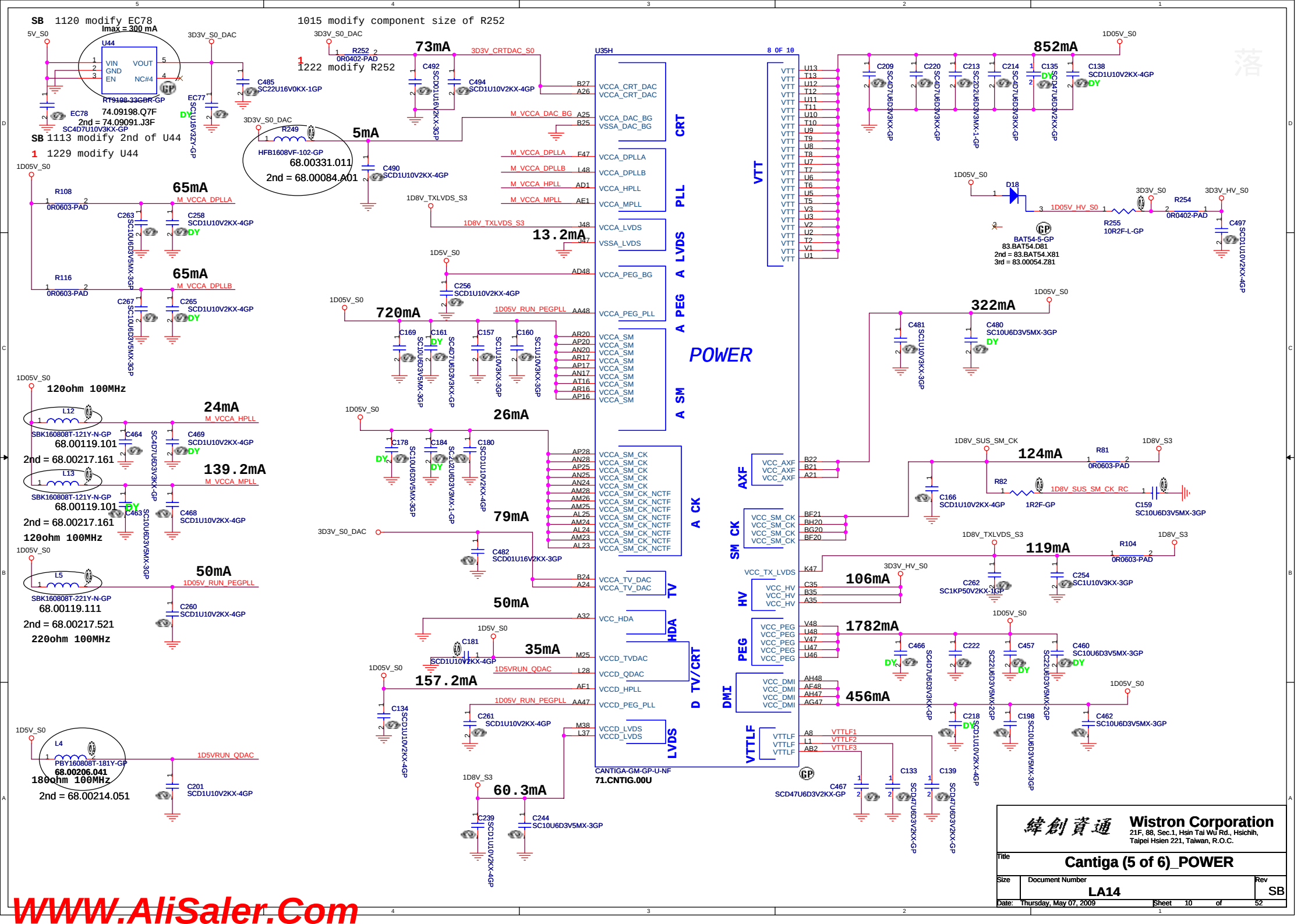
SB 1120 modify EC78

1015 modify component size of R252

SB 1113 modify 2nd of U44

1 1229 modify U44

1 1222 modify R252



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Title	Cantiga (5 of 6)_POWER
Size	Document Number: LA14 — Rev: SB
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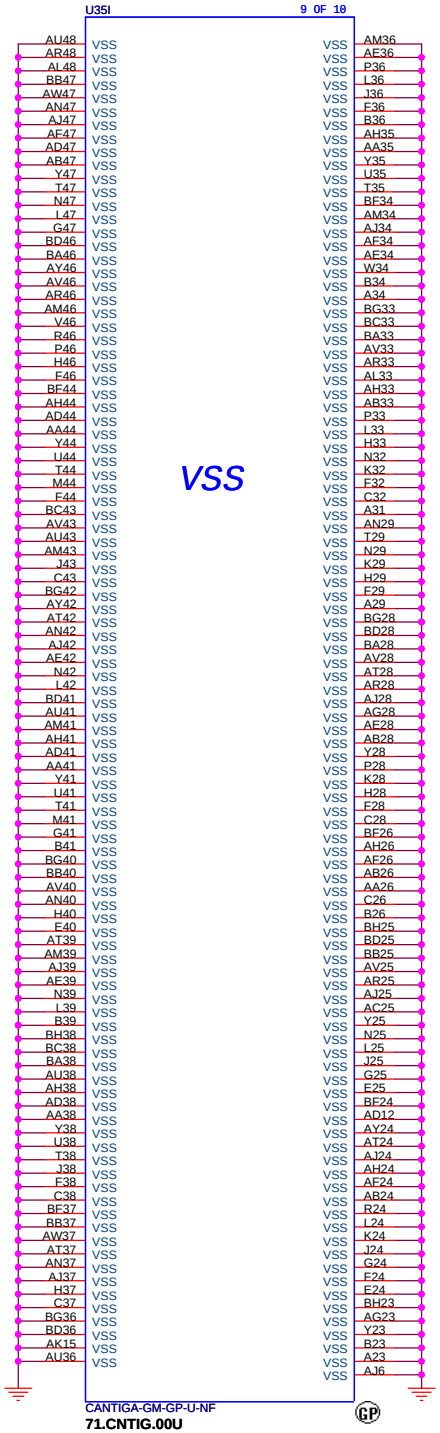

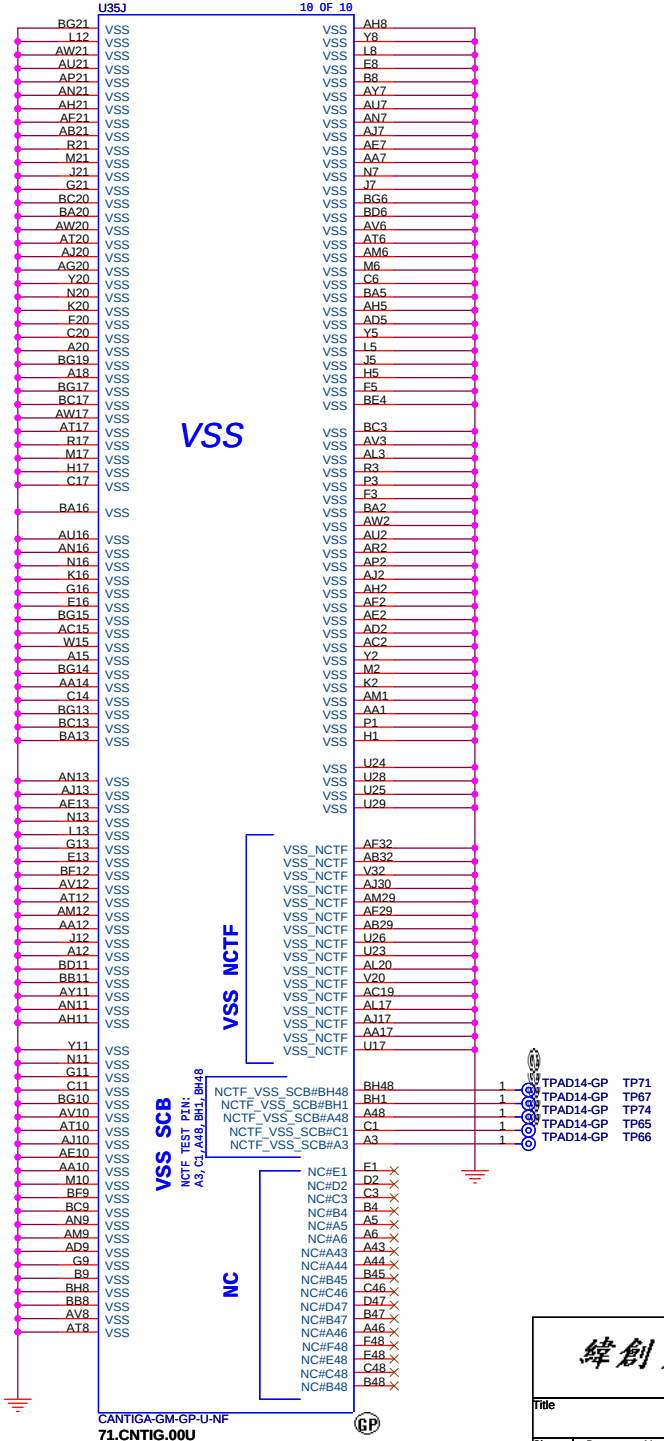

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Title: **Cantiga (6 of 6)**

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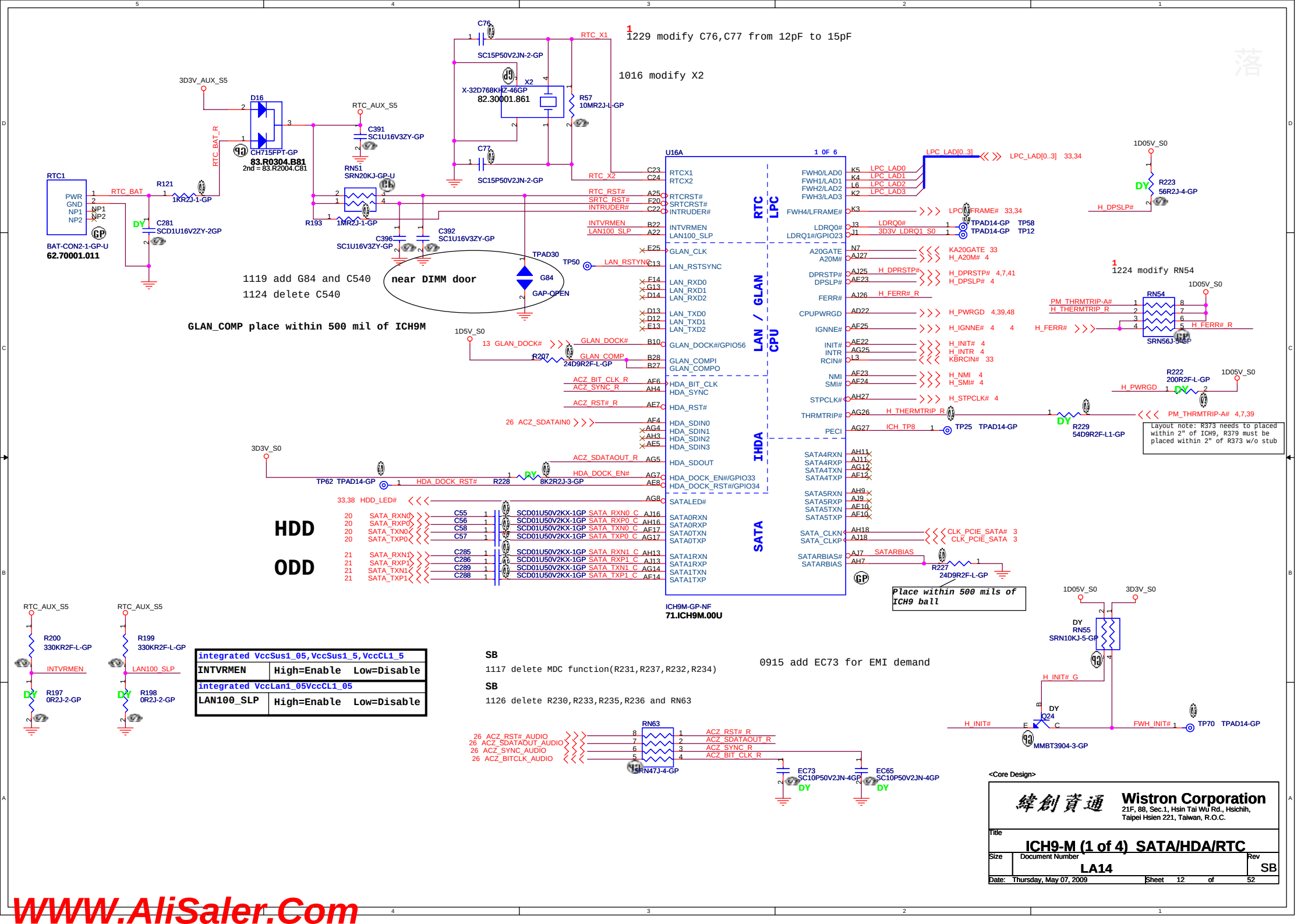

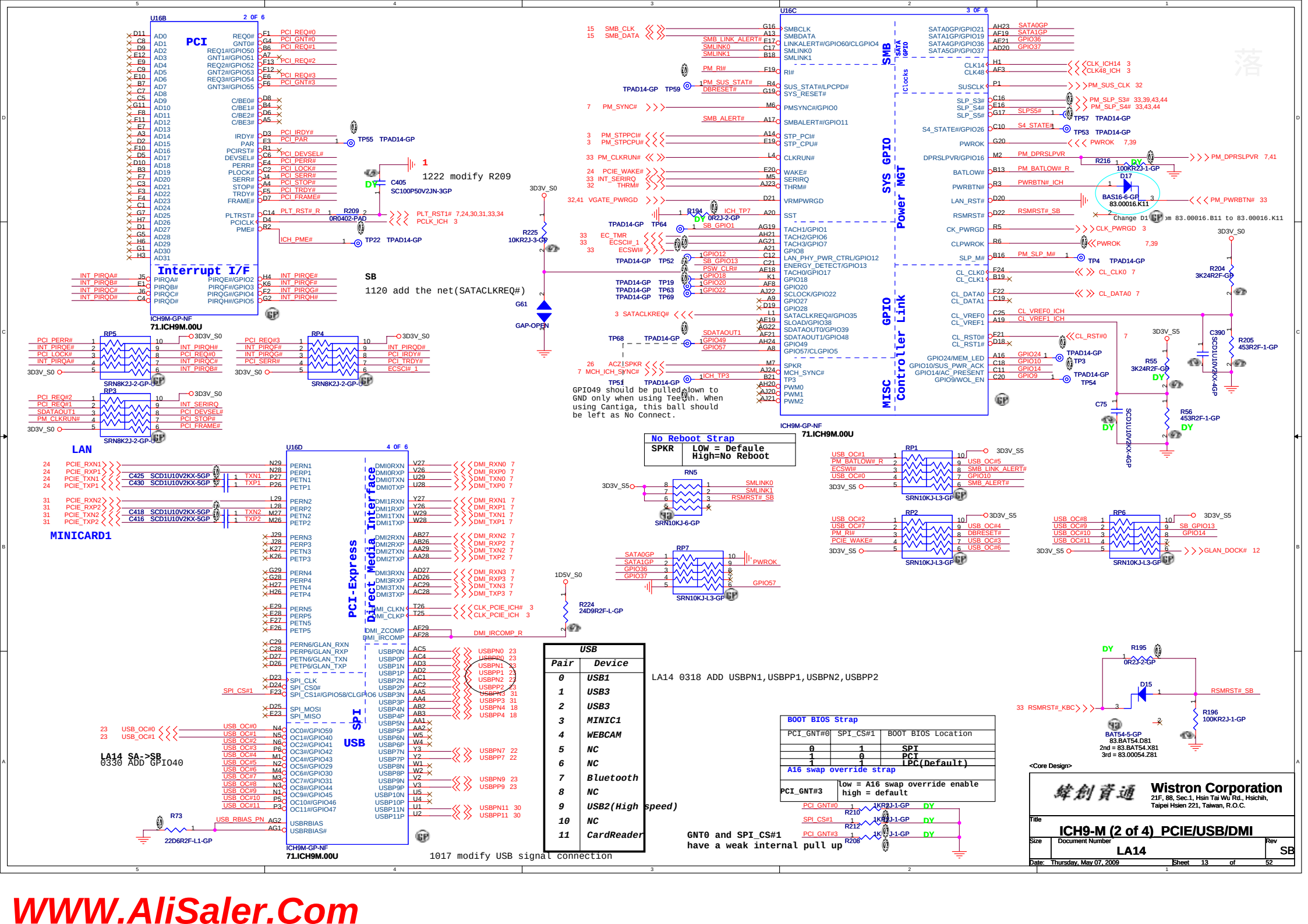

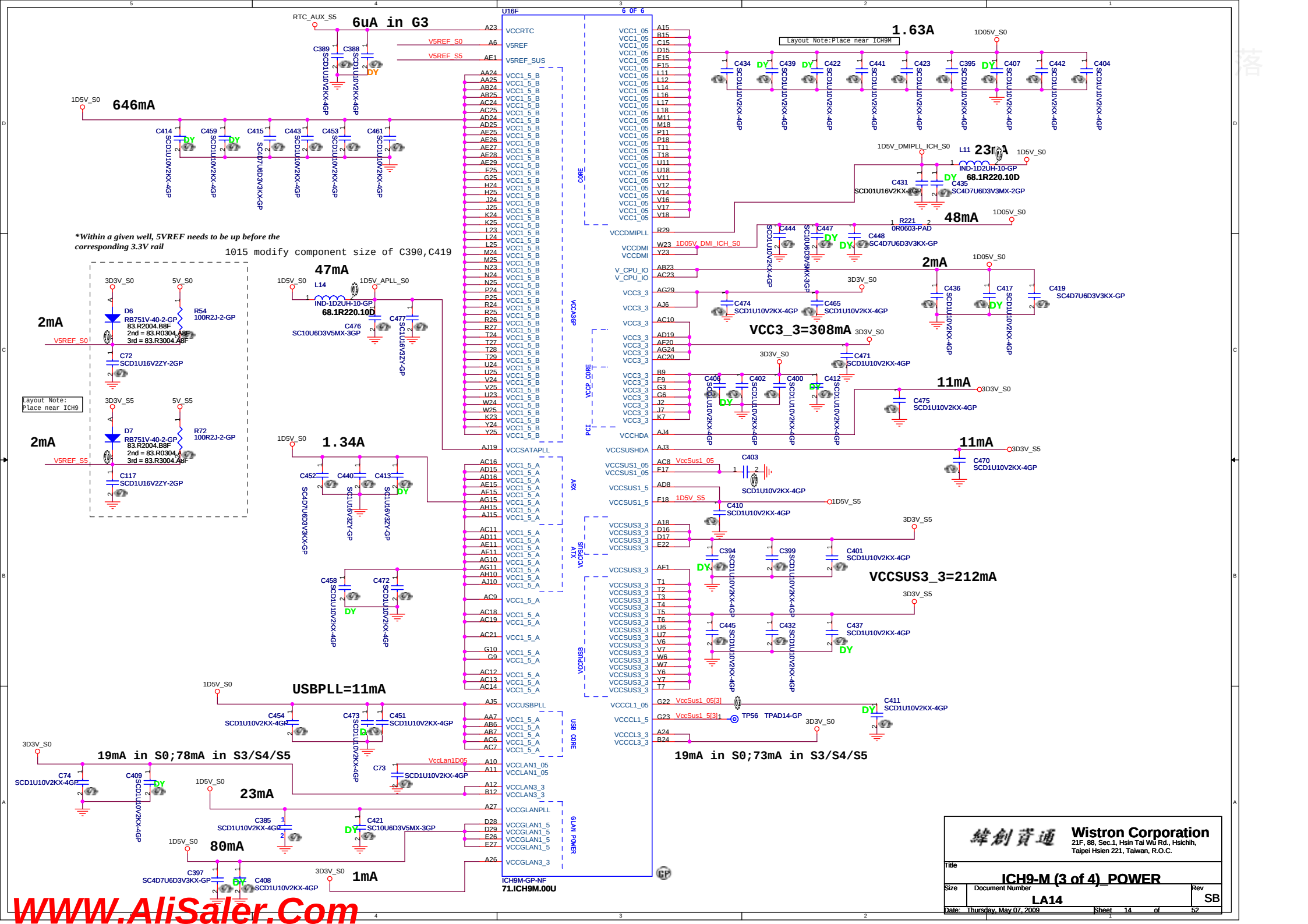
6uA in G3
646mA
1.63A
23mA
48mA
2mA
47mA
1.34A
VCC3_3=308mA
11mA
VCCSUS3_3=212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
19mA in S0;73mA in S3/S4/S5
23mA
80mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
1015 modify component size of C390,C419
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
ICH9M-GP-NF
71.ICH9M.00U
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ICH9-M (3 of 4)_POWER
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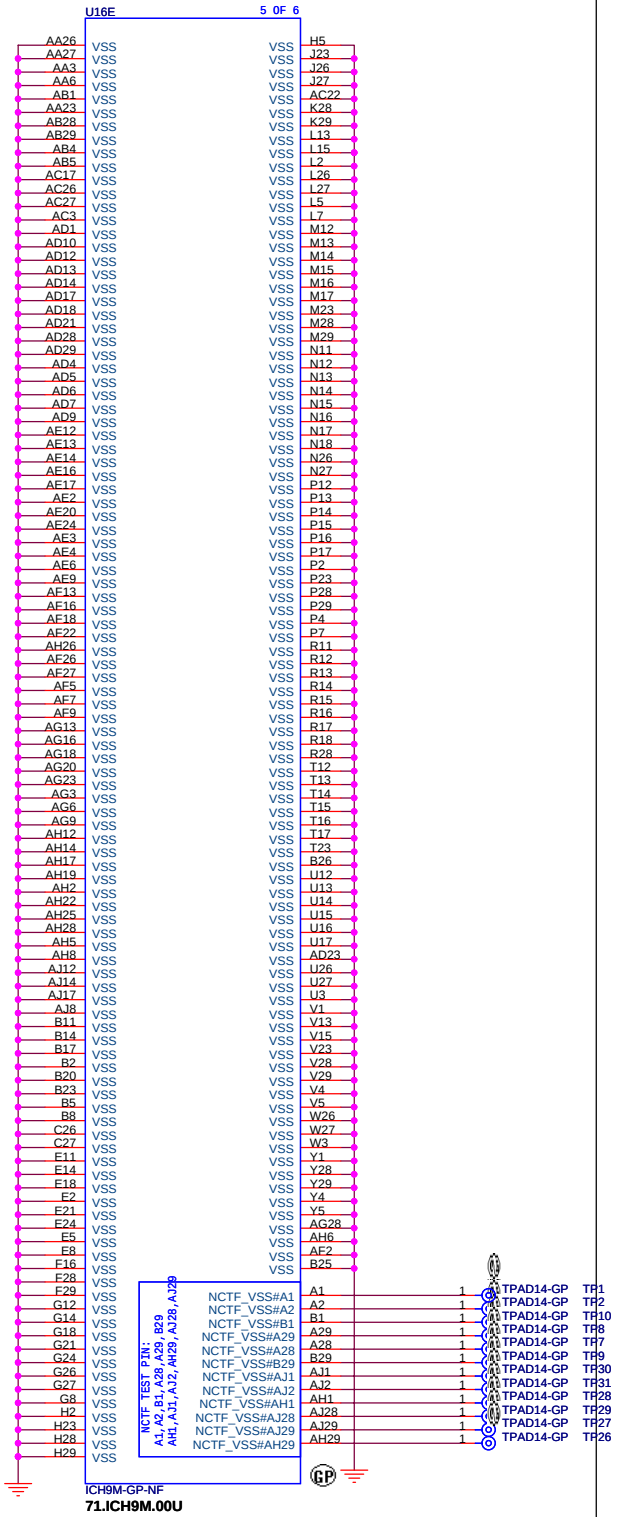

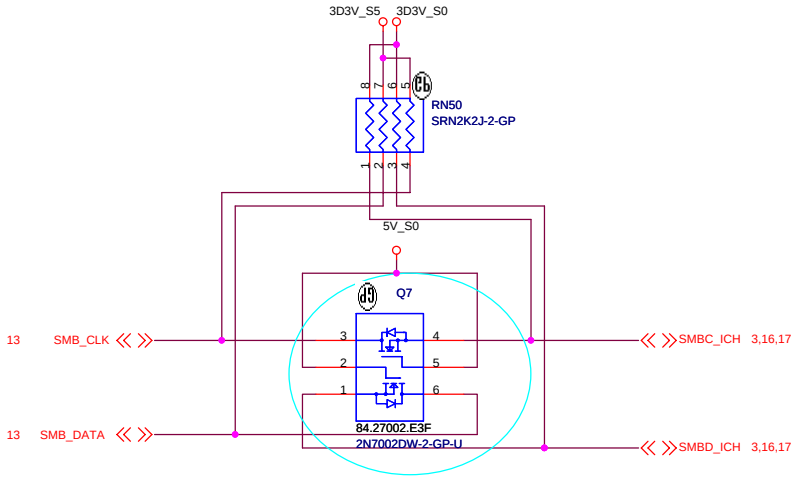

SMBUS

LA14 SA->SB
0403 Change Q7 from 84.27002.D3F to 84.27002.E3F

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Title	**ICH9-M (4 of 4)**	
Size	Document Number **LA14**	Rev SB
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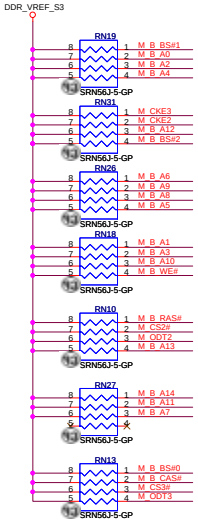
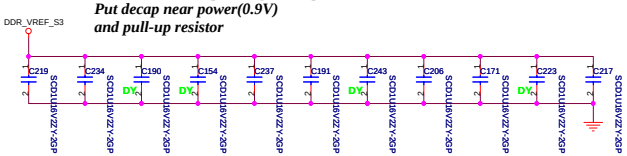
PARALLEL TERMINATION

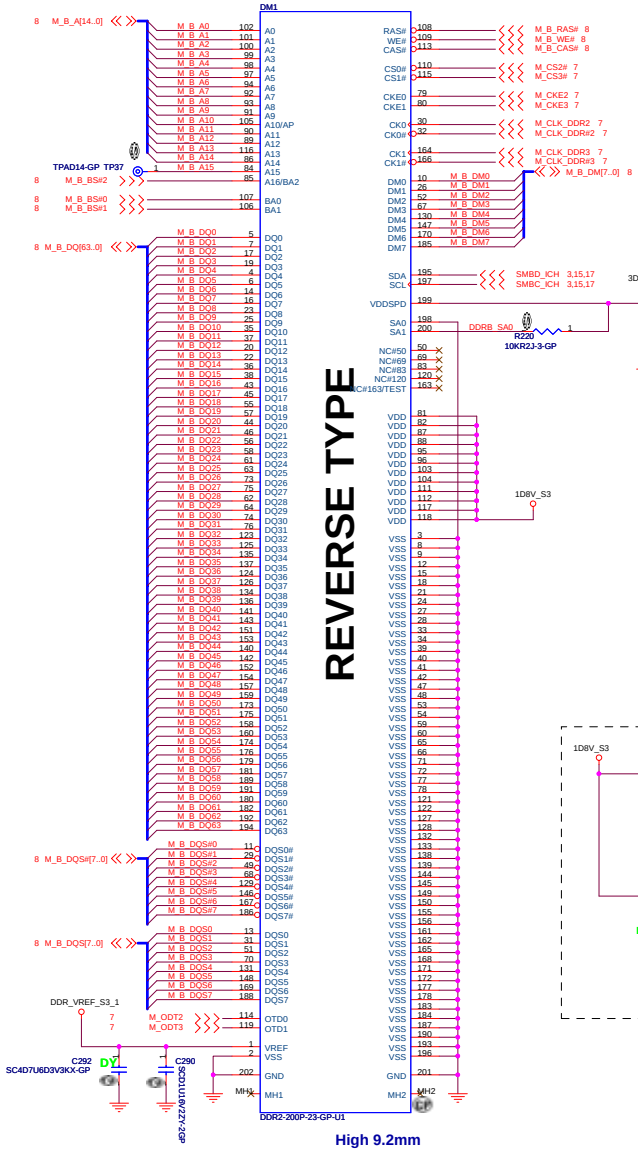
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

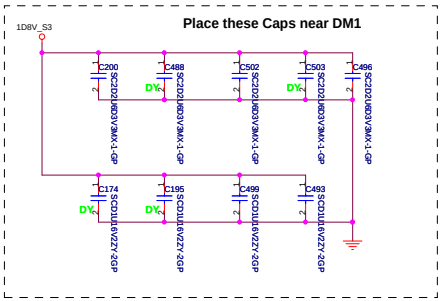
Put decap near power(0.9V) and pull-up resistor





High 9.2mm

62.10017.A71
2nd = 62.10017.B51
3rd = 62.10017.K51



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Title	DDR2 Socket 0 (DM1)
Size	Document Number: LA14
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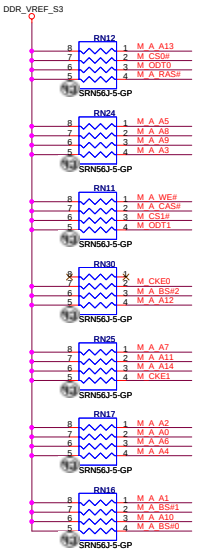
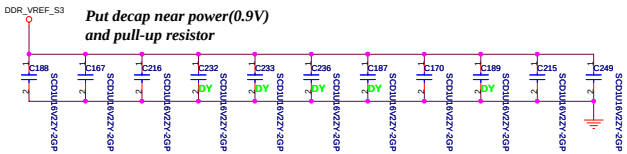
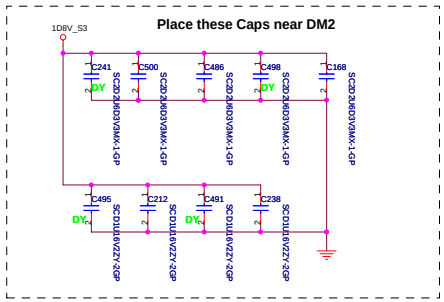
PARALLEL TERMINATION

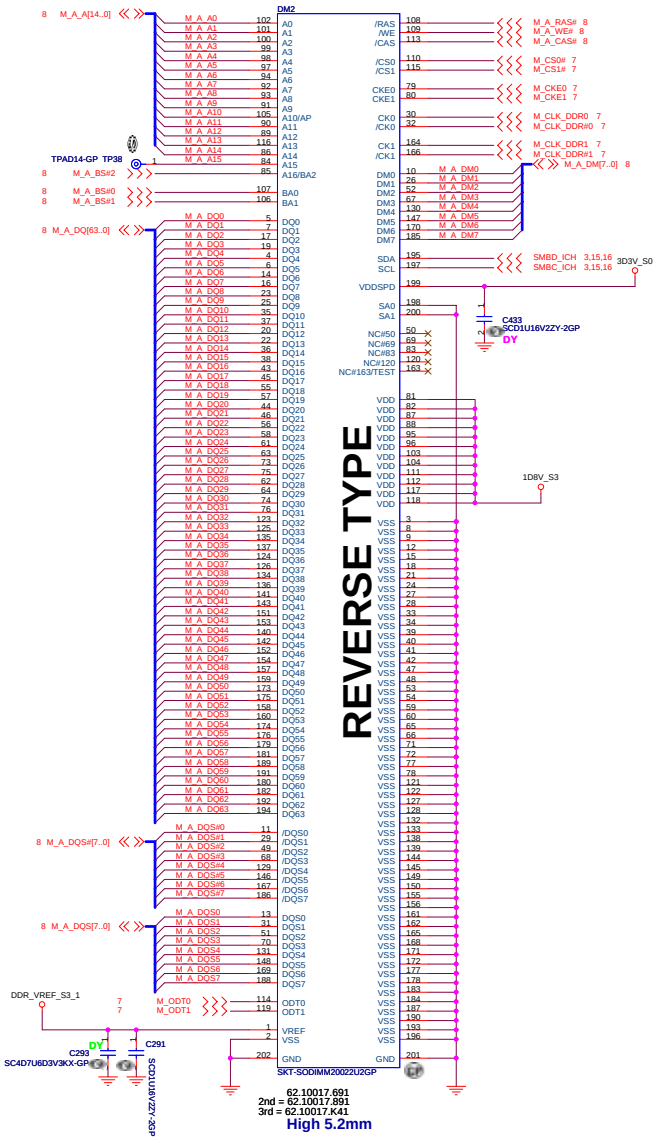
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor





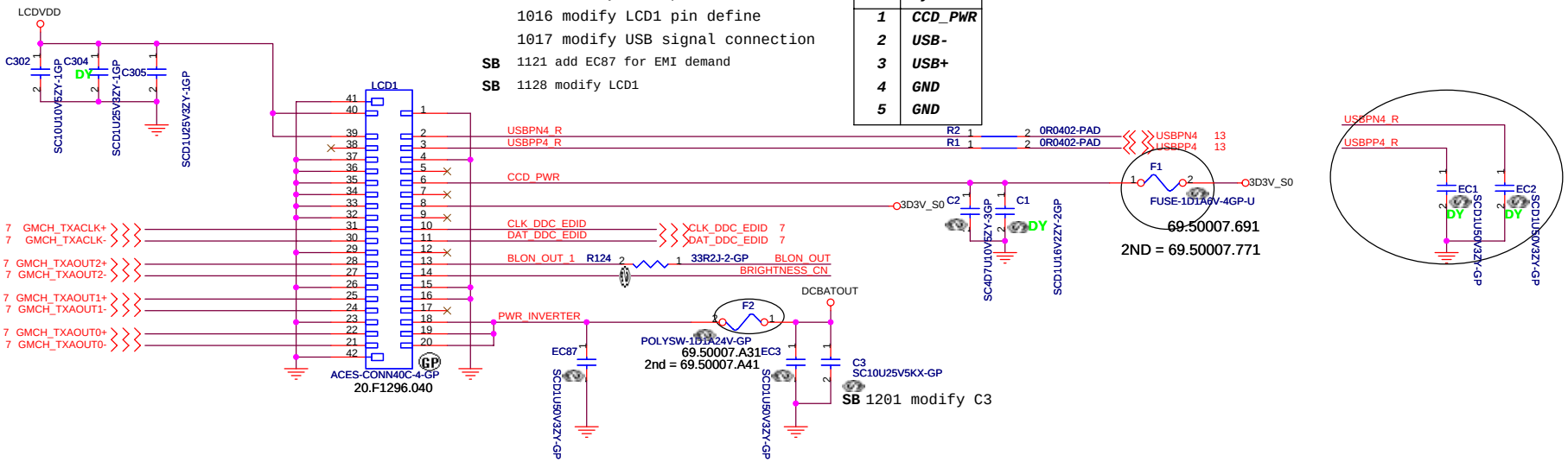


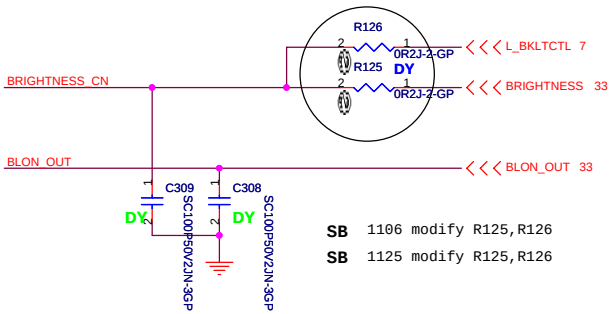
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR2 Socket 1 (DM2)	
Size	Document Number: LA14	Rev: SB
Date: Thursday, May 07, 2009	Sheet 17 of 52	

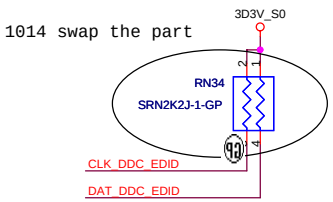
LCD/CCD CONN

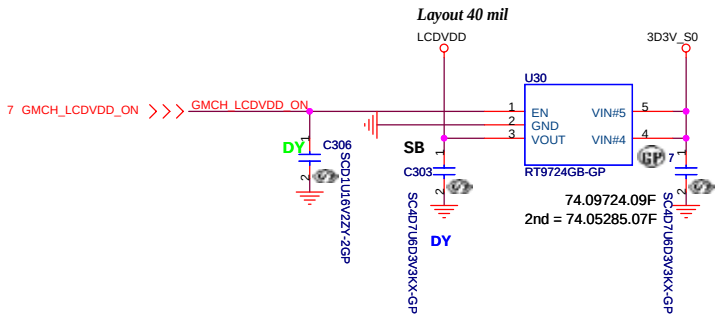
1015 modify F1
1015 modify LCD1 pin define
1016 modify LCD1 pin define
1017 modify USB signal connection
SB 1121 add EC87 for EMI demand
SB 1128 modify LCD1

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND









1015 modify component size of C303,C307
1
1229 modify U30

<Core Design>

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Title: LCD CONN
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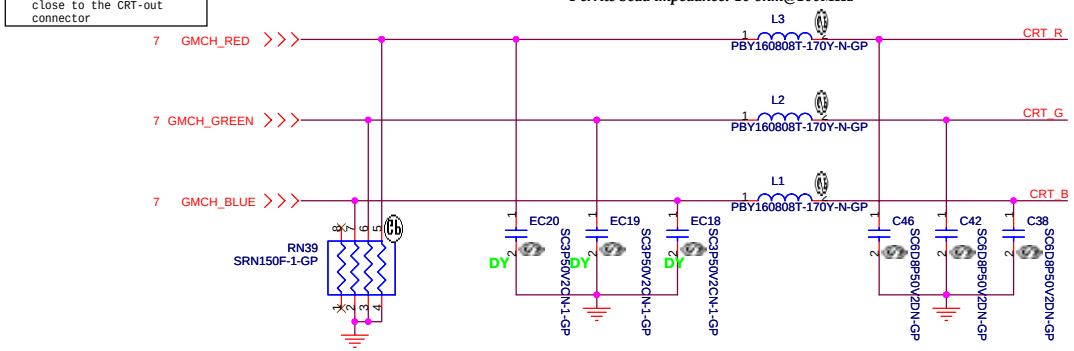
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

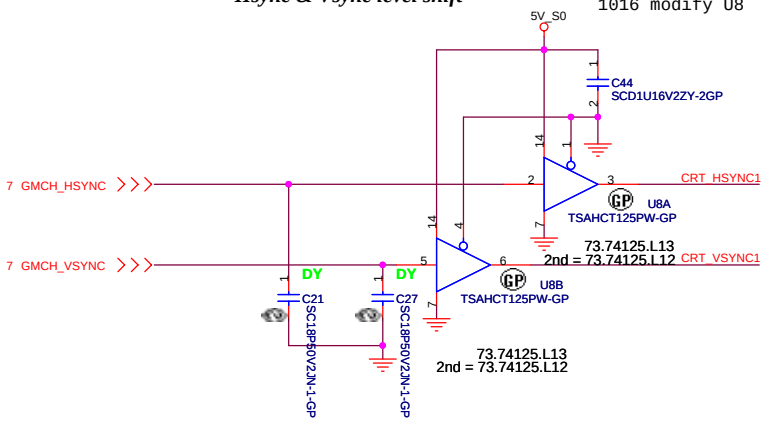


1016 modify L1,L2 and L3
10105 modify L1,L2 and L3

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

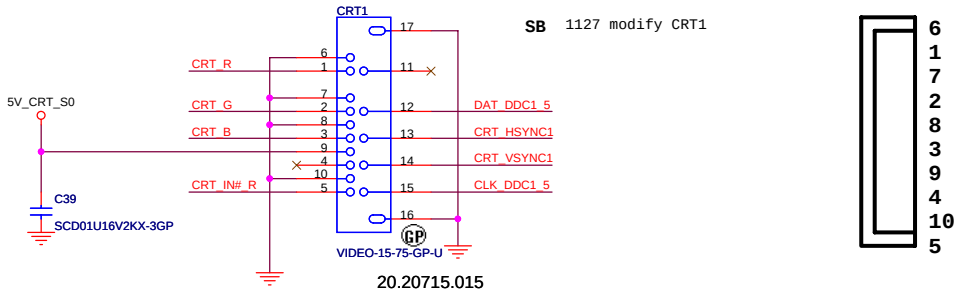
Hsync & Vsync level shift

1016 modify U8

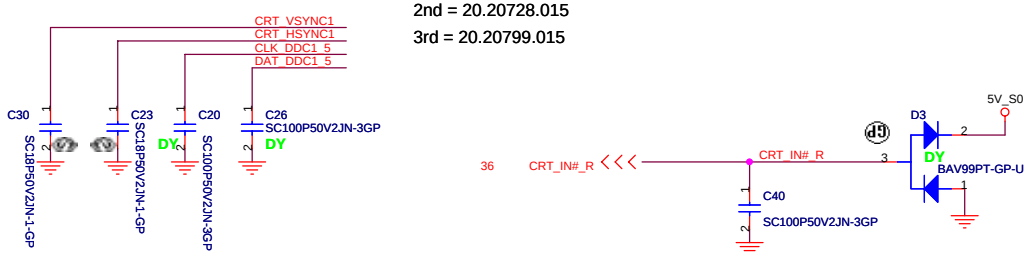


CRT I/F & CONNECTOR

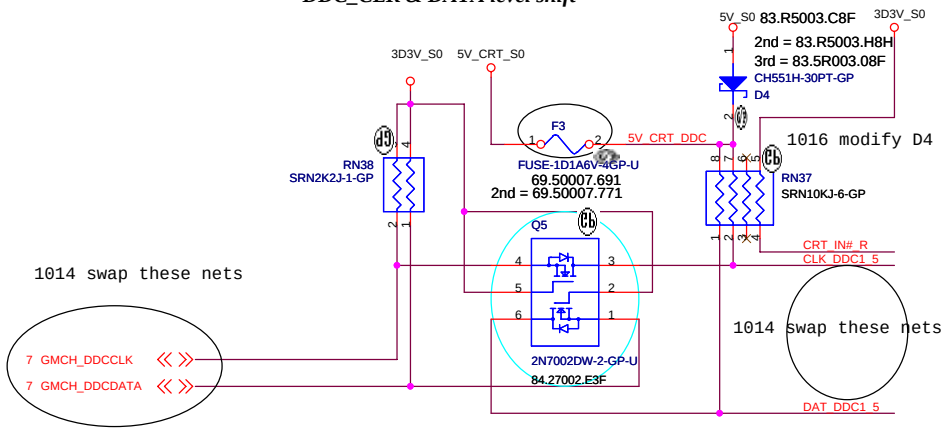
SB 1127 modify CRT1



20.20715.015
2nd = 20.20728.015
3rd = 20.20799.015



DDC_CLK & DATA level shift



LA14 SA->SB
0403 Change Q5 from 84.27002.D3F to 84.27002.E3F

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Title	CRT Connector	
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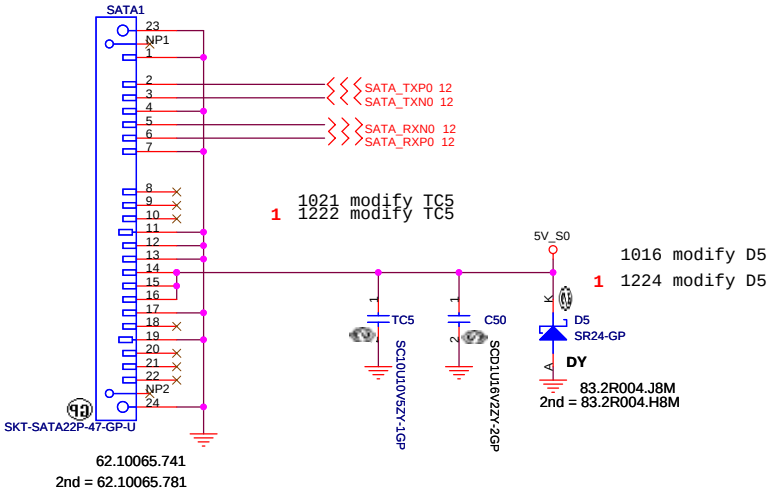
SATA Connector

0912 add these parts for EMI demand
1001 delete these parts for EMI demand
1021 modify SATA1



<Core Design>

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Title	HDD	
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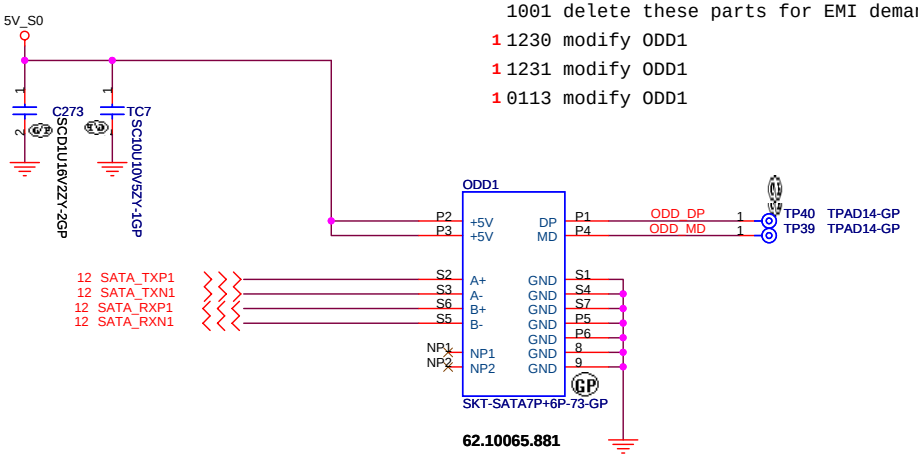
SATA ODD Connector

0912 add these parts for EMI demand
1001 delete these parts for EMI demand
1 1230 modify ODD1
1 1231 modify ODD1
1 0113 modify ODD1



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Title: ODD

Size | Document Number: LA14 | Rev: SB

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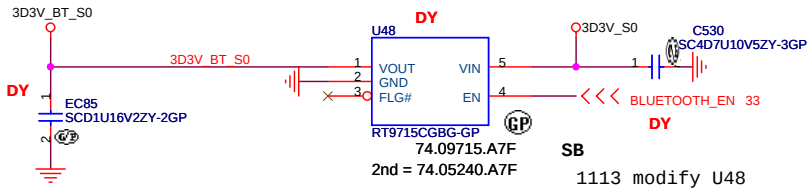
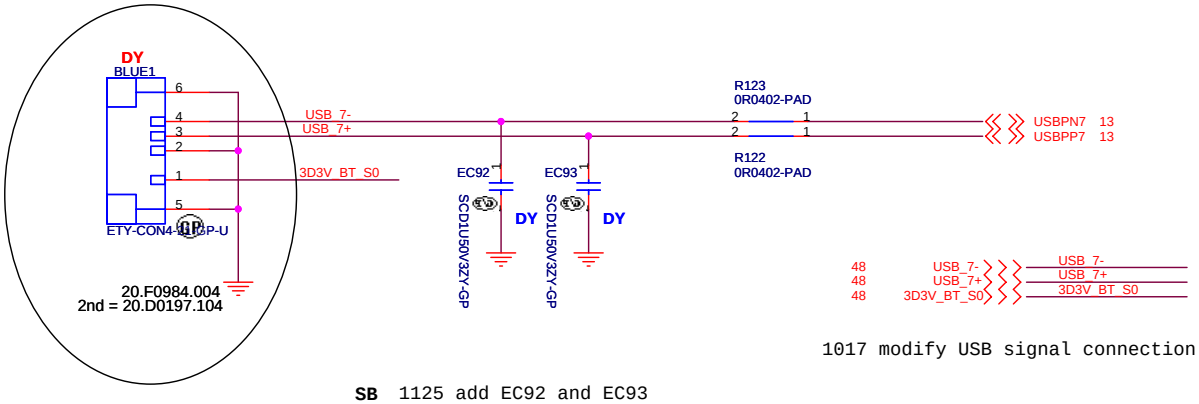
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



SB 1113 modify U48

EC21 put near BLUE1 / all USB put one choke near connector by EMI request



1017 modify USB signal connection

SB 1125 add EC92 and EC93

0930 modify BLUE1

1017 modify BLUE1

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Title: **Bluetooth**		
Size	Document Number: **LA14**	Rev: SB
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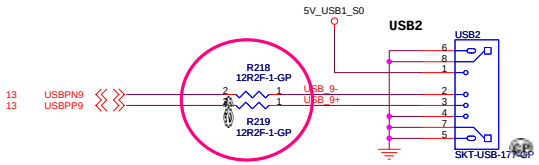
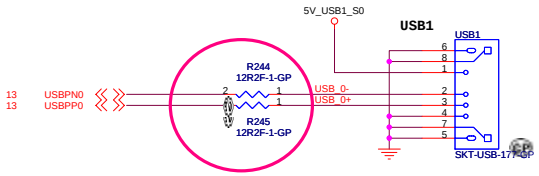
1017 modify USB signal connection
1021 modify and swap these parts(USB1 and USB2)

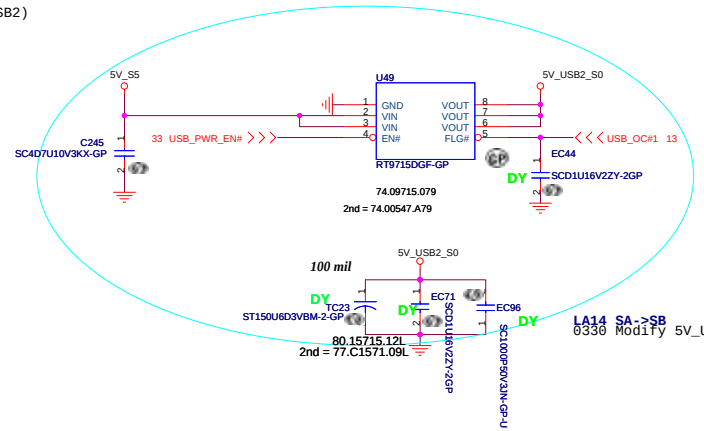


Modify 04/27 Change R218,R219,R244,R245
from 0ohm to 12ohm

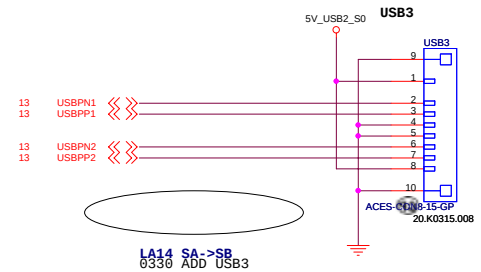
22.10218.U11
2nd = 22.10321.151



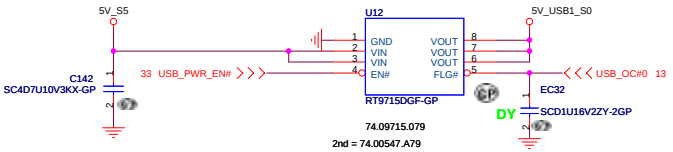
22.10218.U11
2nd = 22.10321.151



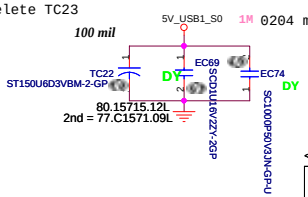
LA14 SA->SB
0330 Modify 5V_USB2_S0,ADD U49 C245,TC23



LA14 SA->SB
0330 ADD USB3

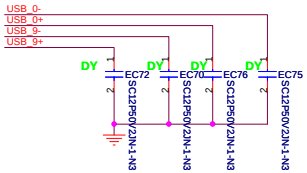


1021 delete TC23



1M 0204 modify the symbol of EC74 (page23)

0912 add these parts for EMI demand



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Title: USB

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1015 modify component size of R69

1 1222 modify R69

Close to AR8114 Pin2

AR8132 use 0 ohm resiter

AR8114A Atheros suggestion change to Bead
60 ohms/100Mhz 500mA (68.60090.0D1)

1 1224 modify R71

FOR AR8114A LAN_ACT_LED is high enable pin

Modify 0504 SB->SC
Change U11 P/N to 71.08132.M01

LA14 SA->SB
0401 DY C109

LA14 SA->SB
0401 DY R303

SB 1126 add R303,R304

1016 modify RN53 and U10

Close to U13 Pin8

72.24C08.I01

2nd = 72.24C08.J01

1001 modify RN9

1014 swap these nets

SB

1113 modify C103 and C106

82.30020.791
2nd = 82.30020.851

1 1222 modify R68

AR8114 use 0ohm resister
AR8132 Atheros suggest to change 4.7uH choke

1 1229 modify L19

SB
1128 Add L19

1015 modify component size of R79

-1 1222 modify R79

84.00069.B1B
2nd = 84.DCP69.01B
3rd = 84.00069.A1B

1016 modify Q8

Close to AR8114 Pin1

1 1224 add R307 and R308

1 1224 modify R67

Atheros suggestion change to Bead
60 ohms/100Mhz 500mA (68.60090.0D1)

Close to AR8114 Pin6

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Title: Atheros AR8114/8132

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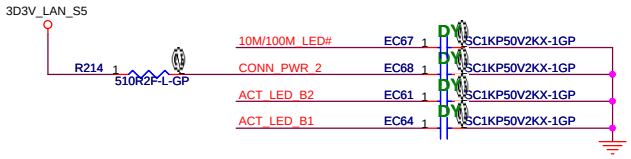
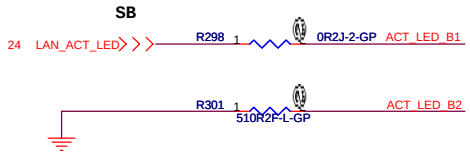
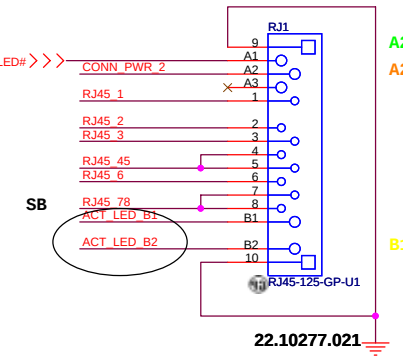
LAN Connector



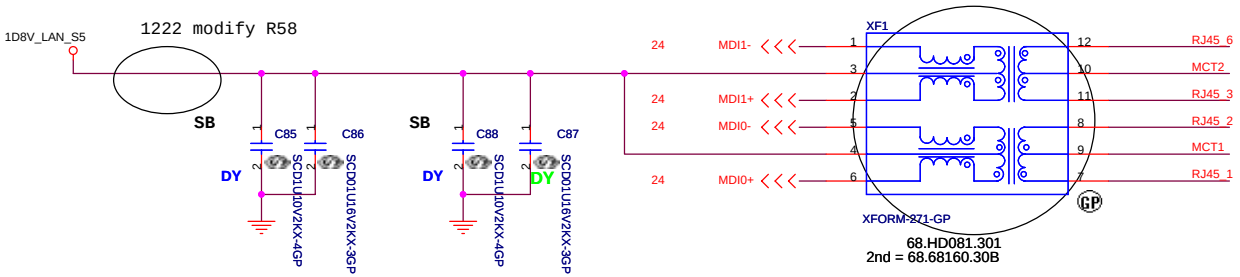


LA14 SA->SB
0313 Del R299,R300



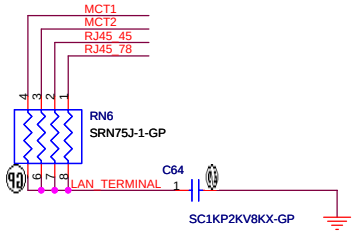
22.10277.021
2nd = 22.10277.231
SB 1204 modify second source of RJ1

10/100 Lan Transformer



68.HD081.301
2nd = 68.68160.30B

1016 modify XF1



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Core Design>

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Title: **LAN Connector**
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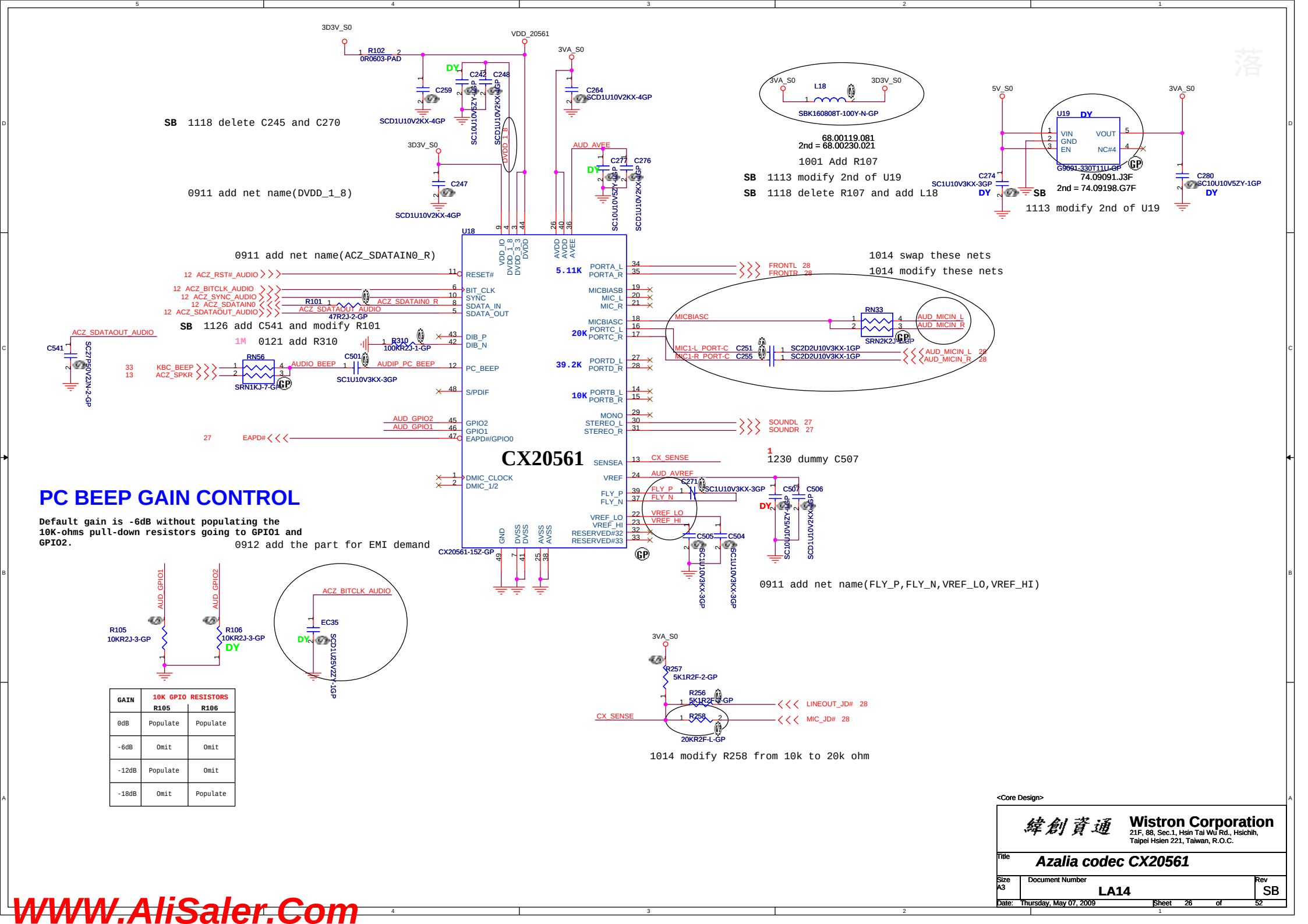
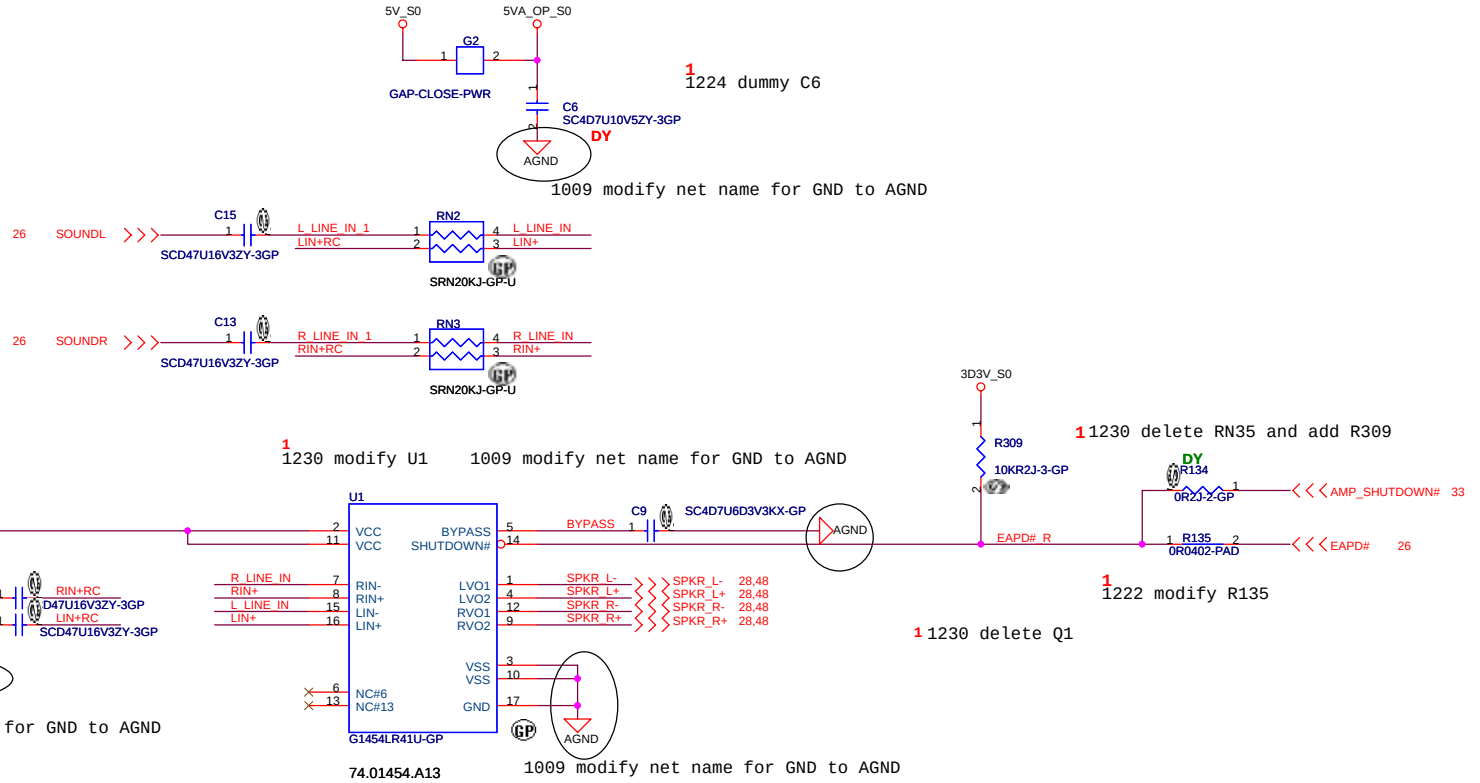
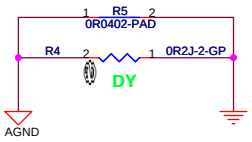


AUDIO OP AMPLIFIER

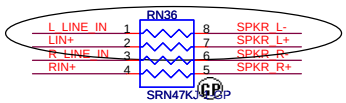


AC decopling

1222 modify R5



1014 swap these nets



SB 1204 modify RN36

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Title: AUDIO AMP

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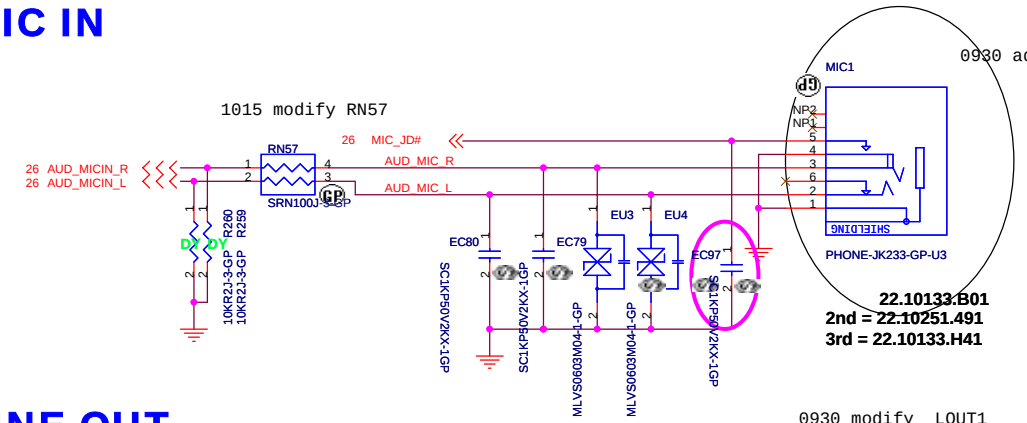
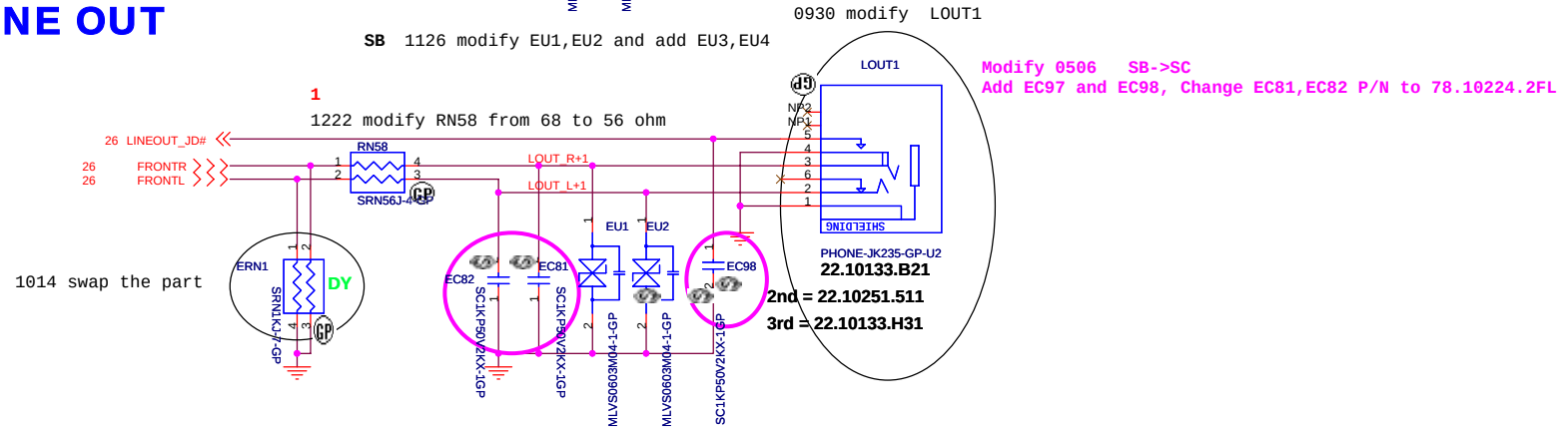
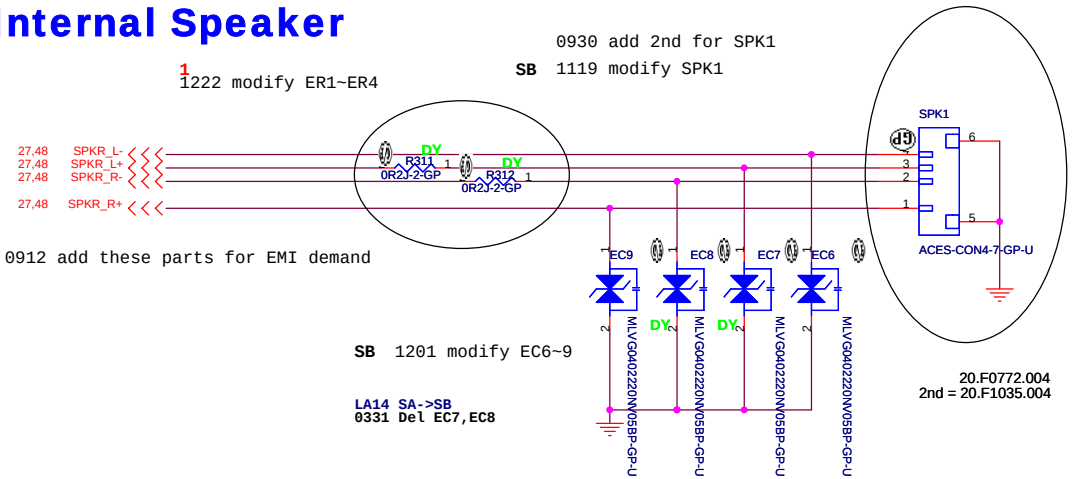
MIC IN



LINE OUT



Internal Speaker



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Title	AUDIO JACK	
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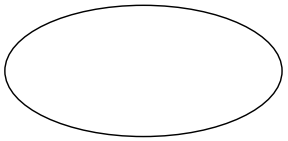
MDC 1.5 CONN

0912 add the part for EMI demand

1002 modify MDC1

SB

1112 delete MDC function



<Core Design>

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Title: **MDC**

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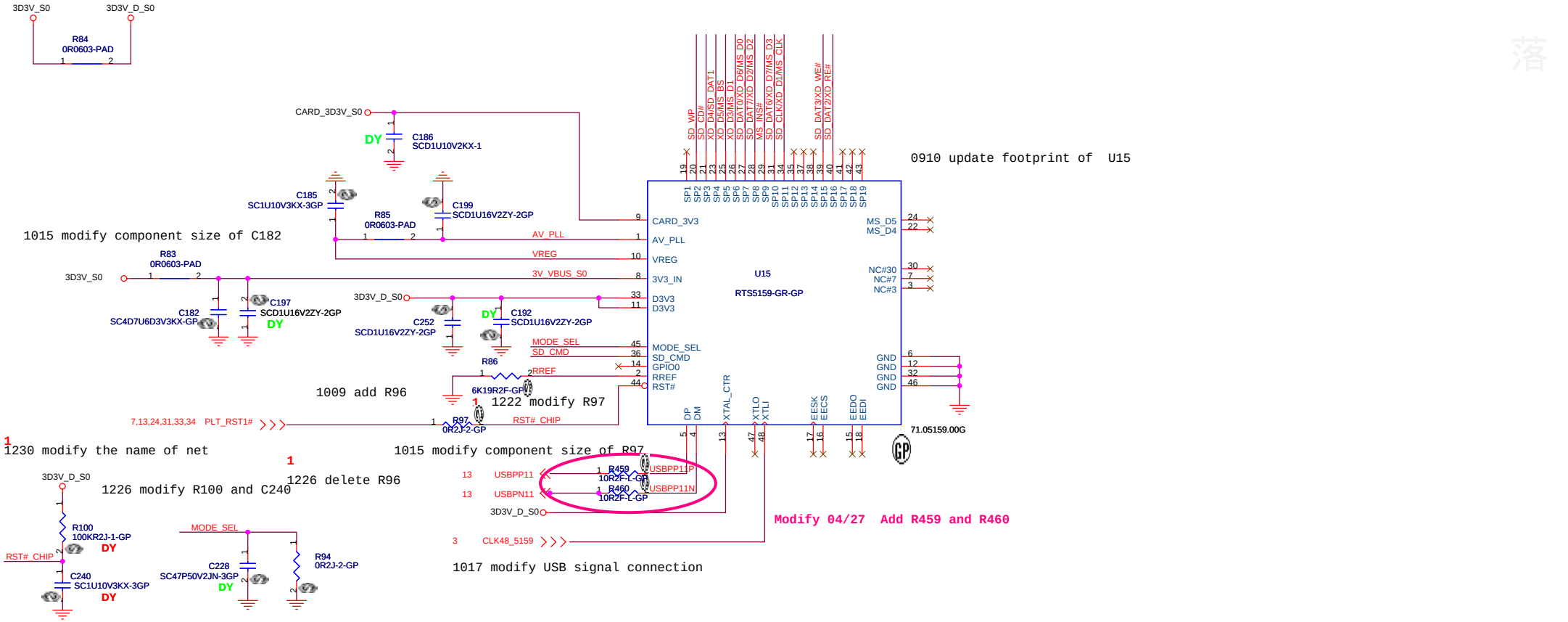
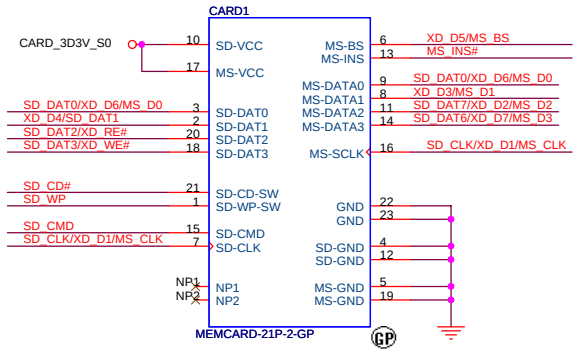
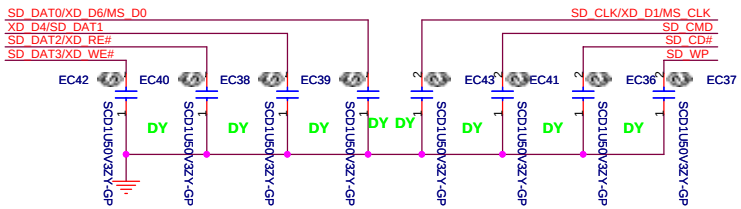
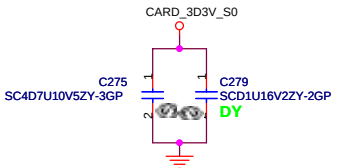


3 IN1 CARD-READER (SD/MMC/MS)



1009 modify this net
1013 modify card1
1 1222 modify card1 from 20.I0043.001 to 20.I0043.011
1 1229 modify card1
LA14 SA 0217 modify card1 from 20.I0043.011 to 20.I0033.021





<Core Design>

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Title: CARD READER- RTS5159

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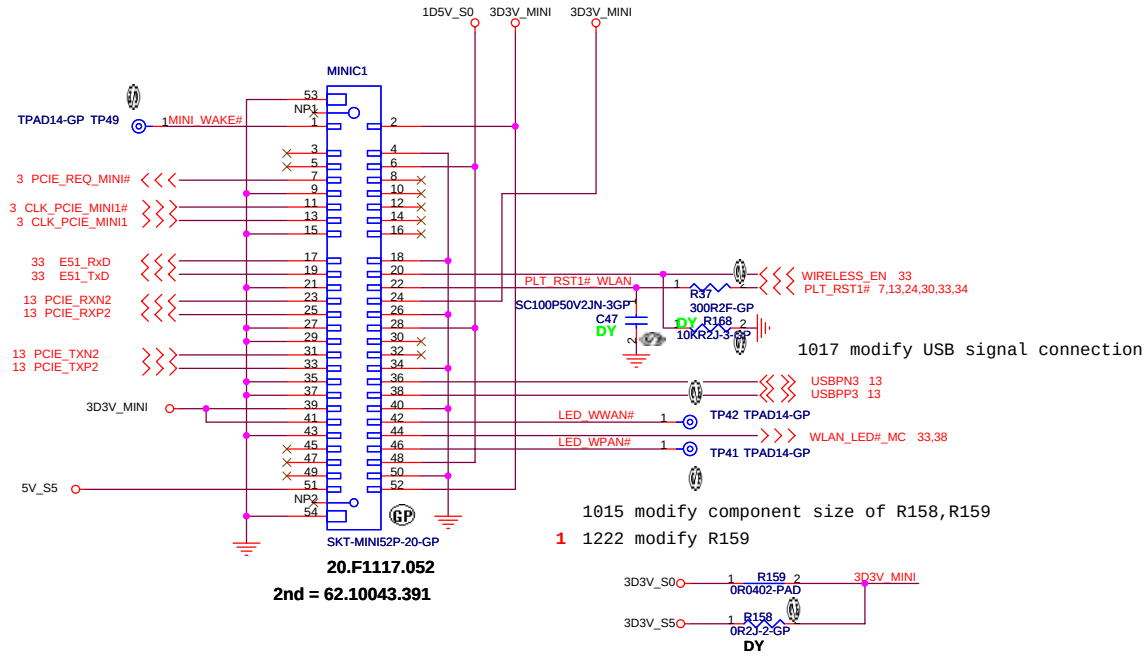
Mini Card Connector(WLAN)

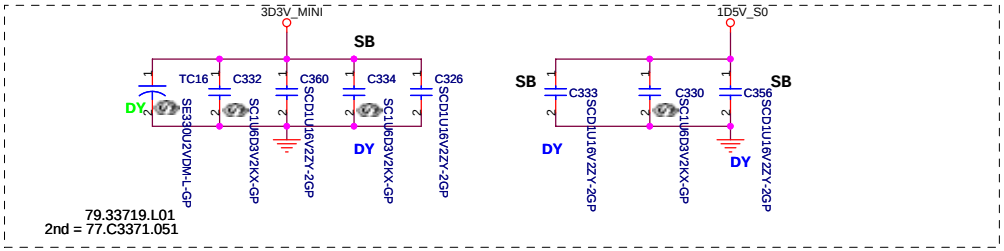


1017 modify USB signal connection

1015 modify component size of R158,R159

1 1222 modify R159

1021 modify TC16 Place near MINIC1



<Core Design>

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Title: MINI CARD

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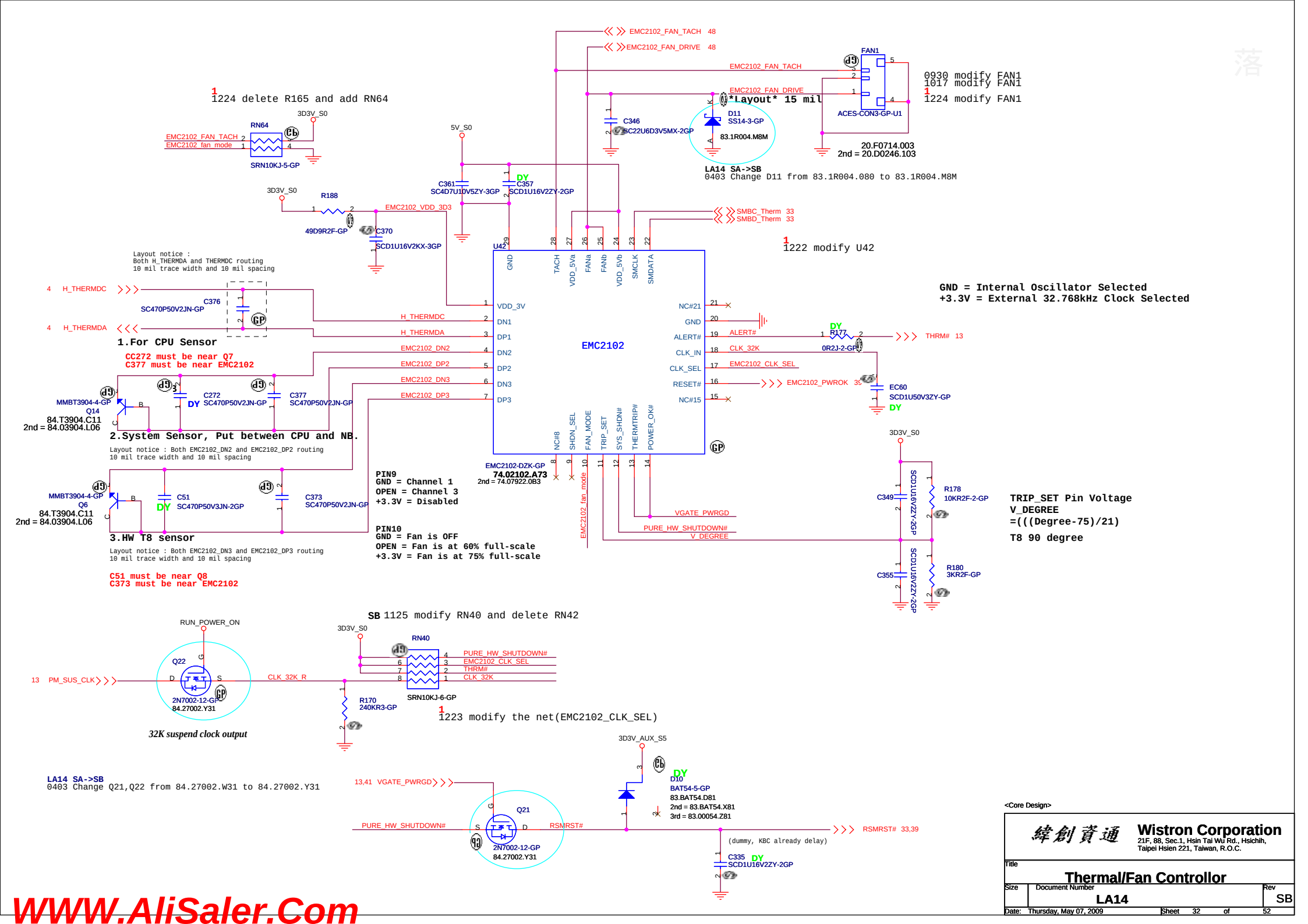
1
1224 delete R165 and add RN64
RN64
SRN10KJ-5-GP
EMC2102_FAN_TACH
EMC2102_fan_mode
3D3V_S0
5V_S0
R188
49D9R2F-GP
C370
SCD1U16V2KX-3GP
C361
SC4D7U10V5ZY-3GP
C357
SCD1U16V2ZY-2GP
DY
EMC2102_VDD_3D3
EMC2102_FAN_TACH 48
EMC2102_FAN_DRIVE 48
Layout 15 mil
D11
SS14-3-GP
83.1R004.M8M
C346
SC22U6D3V5MX-2GP
FAN1
ACES-CON3-GP-U1
20.F0714.003
2nd = 20.D0246.103
0930 modify FAN1
1017 modify FAN1
1
1224 modify FAN1
LA14 SA->SB
0403 Change D11 from 83.1R004.080 to 83.1R004.M8M
SMBC_Therm 33
SMBD_Therm 33
1
1222 modify U42
U42
EMC2102
EMC2102-DZK-GP
74.02102.A73
2nd = 74.07922.0B3
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
H_THERMDC
H_THERMDA
C376
SC470P50V2JN-GP
1.For CPU Sensor
CC272 must be near Q7
C377 must be near EMC2102
MMBT3904-4-GP
Q14
84.T3904.C11
2nd = 84.03904.L06
C272
SC470P50V2JN-GP
C377
SC470P50V2JN-GP
2.System Sensor, Put between CPU and NB.
Layout notice : Both EMC2102_DN2 and EMC2102_DP2 routing
10 mil trace width and 10 mil spacing
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
ALERT#
CLK_32K
EMC2102_CLK_SEL
EMC2102_PWROK 35
R177
0R2J-2-GP
THRM# 13
EC60
SCD1U50V3ZY-GP
PIN9
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
PIN10
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
MMBT3904-4-GP
Q6
84.T3904.C11
2nd = 84.03904.L06
C51
SC470P50V3JN-2GP
C373
SC470P50V2JN-GP
3.HW T8 sensor
Layout notice : Both EMC2102_DN3 and EMC2102_DP3 routing
10 mil trace width and 10 mil spacing
C51 must be near Q8
C373 must be near EMC2102
VGATE_PWRGD
PURE_HW_SHUTDOWN#
V_DEGREE
R178
10KR2F-2-GP
R180
3KR2F-GP
C349
C355
SCD1U16V2ZY-2GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
T8 90 degree
SB 1125 modify RN40 and delete RN42
RUN_POWER_ON
Q22
2N7002-12-GP
84.27002.Y31
13 PM_SUS_CLK
CLK_32K_R
32K suspend clock output
RN40
SRN10KJ-6-GP
R170
240KR3-GP
PURE_HW_SHUTDOWN#
EMC2102_CLK_SEL
THRM#
CLK_32K
1
1223 modify the net(EMC2102_CLK_SEL)
LA14 SA->SB
0403 Change Q21,Q22 from 84.27002.W31 to 84.27002.Y31
3D3V_AUX_S5
D10
BAT54-5-GP
83.BAT54.D81
2nd = 83.BAT54.X81
3rd = 83.00054.Z81
13,41 VGATE_PWRGD
PURE_HW_SHUTDOWN#
Q21
2N7002-12-GP
84.27002.Y31
RSMRST#
RSMRST# 33,39
(dummy, KBC already delay)
C335
SCD1U16V2ZY-2GP
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<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
LA14
Rev
SB
Date: Thursday, May 07, 2009
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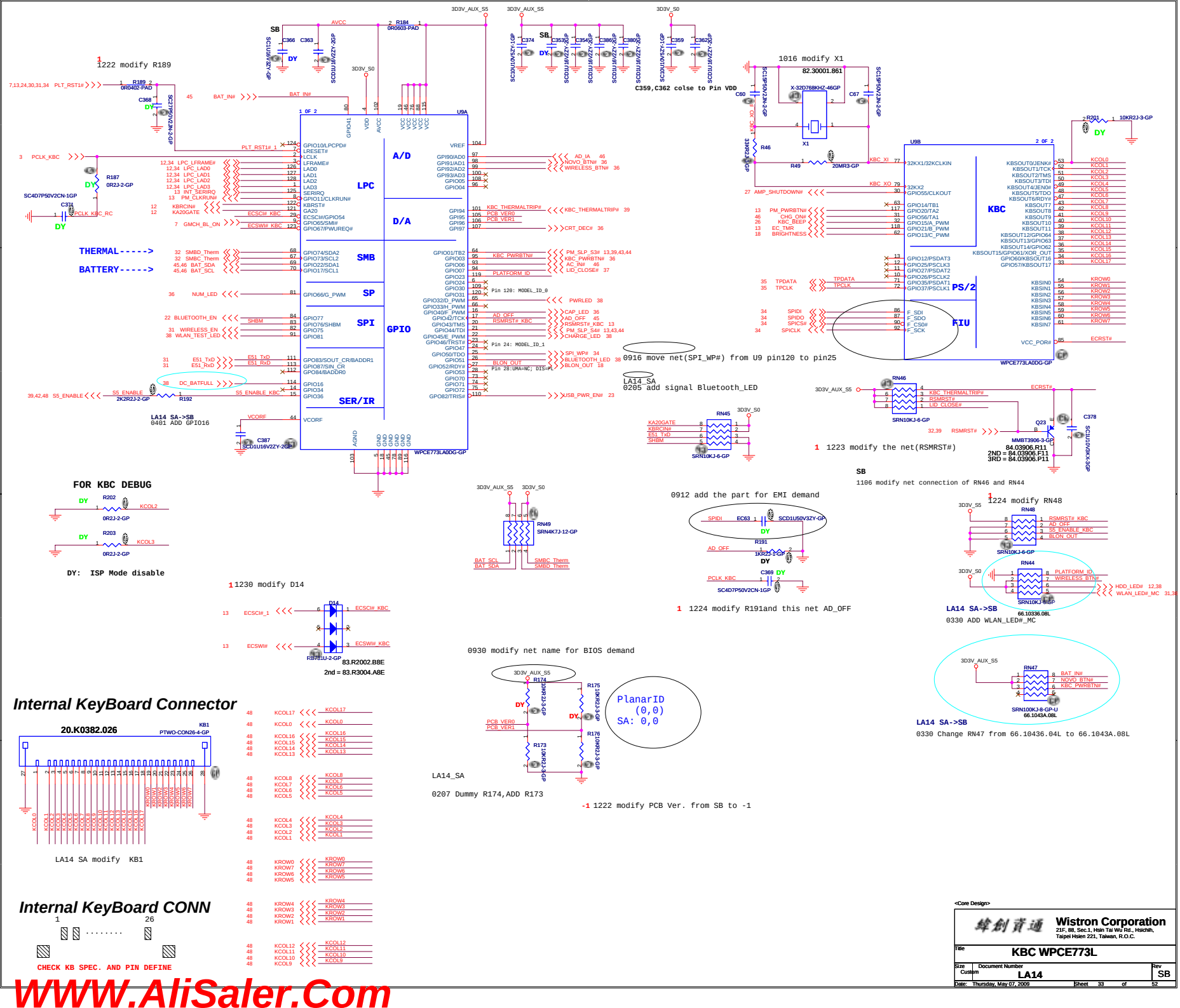
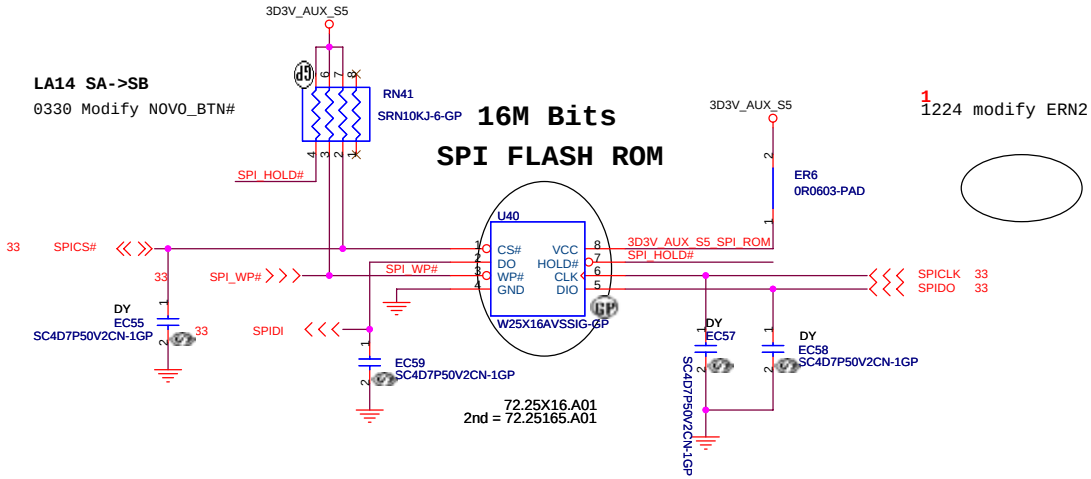


LA14 SA->SB

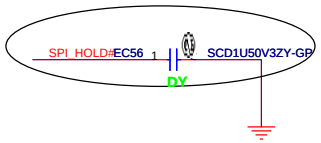
0330 Modify NOVO_BTN#

1224 modify ERN2

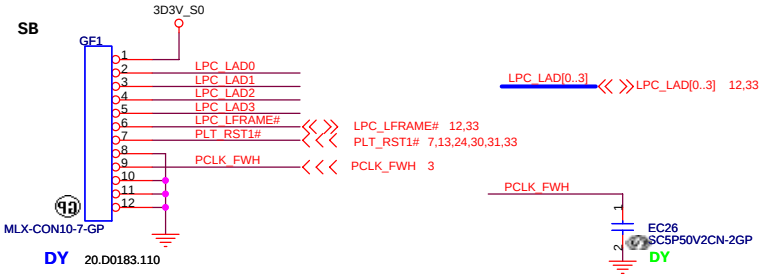


1013 modify U40 from 72.25X16.001 to 72.25X16.A01

0912 add the part for EMI demand



GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

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Title: BIOS/GOLDEN FINGER

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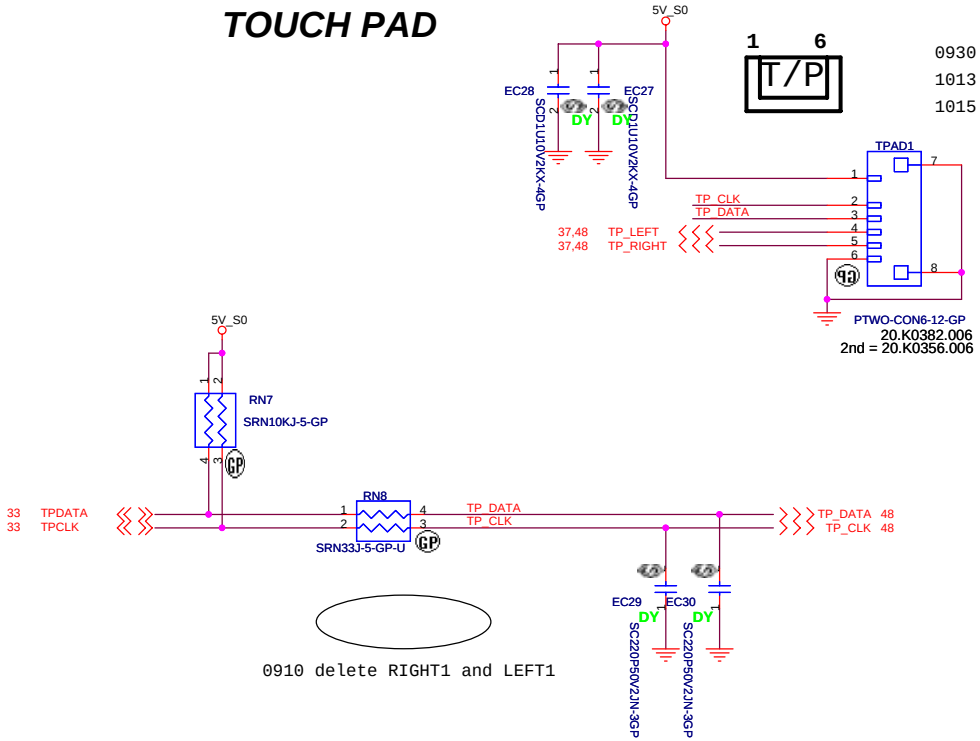
TOUCH PAD



0930 modify TPAD1 1124 modify TPAD1
1013 modify TPAD1
1015 modify TPAD1

<Core Design>

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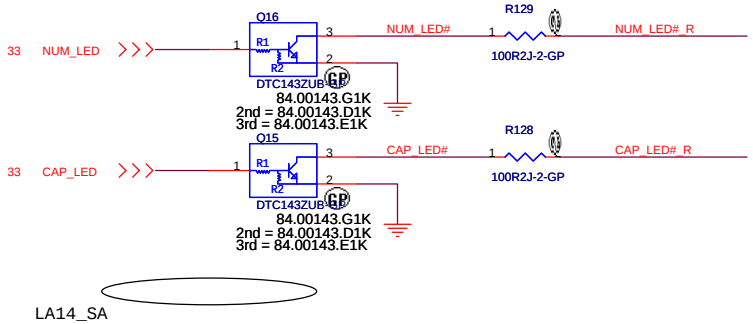
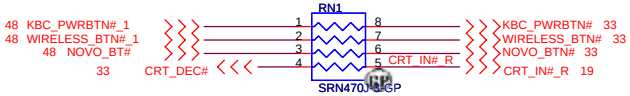
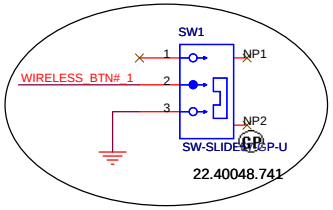
Title: Touch pad		
Size	Document Number: LA14	Rev: SB
Date: Thursday, May 07, 2009	Sheet 35 of 52	

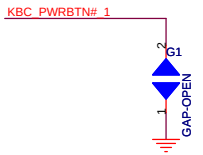


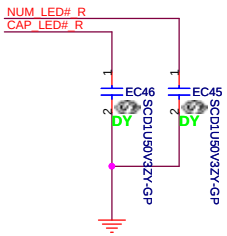
LA14_SA

0205 remove signals(TP_LOCK_LED,TP_LOCK_LED#,TP_LOCK_LED#_R)and R132,Q17



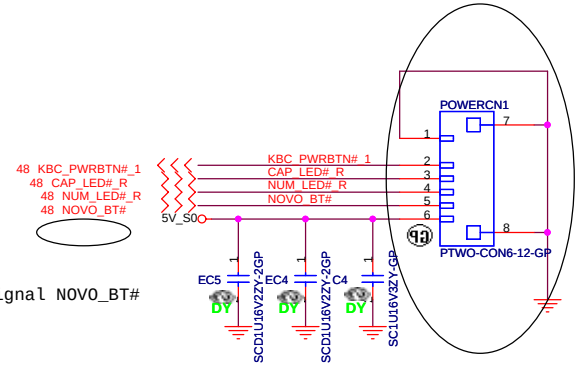






LA14_SA

0205 remove EC49



LA14_SA

0205 ADD signal NOVO_BT#

LA14_SA

0205 modify POWERCN1 from 20.K0384.016 to 20.K0204.006

0223 modify POWERCN1 from 20.K0204.006 to 20.K0382.006

<Core Design>

緯創資通 Wistron Corporation

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Title	Power Board		
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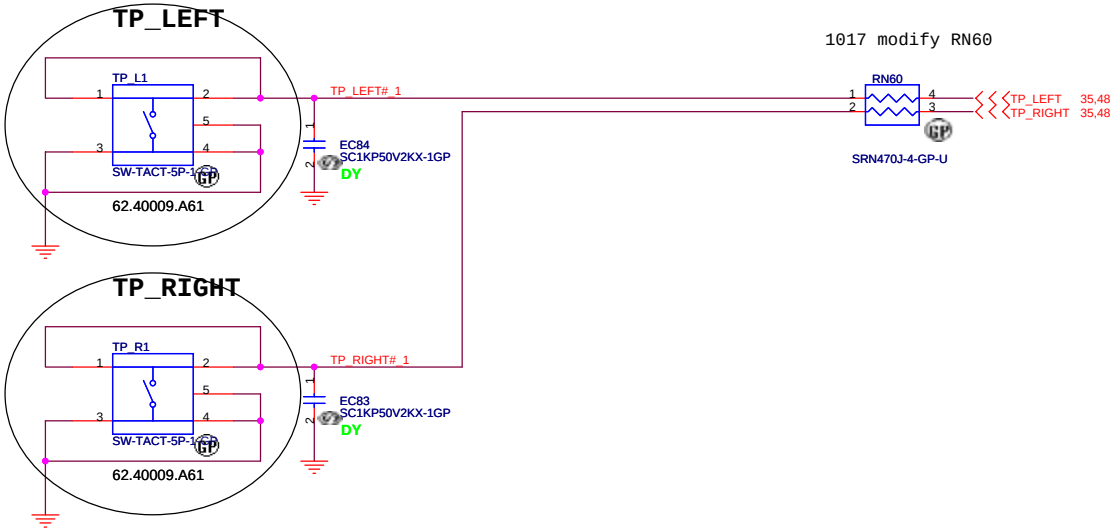
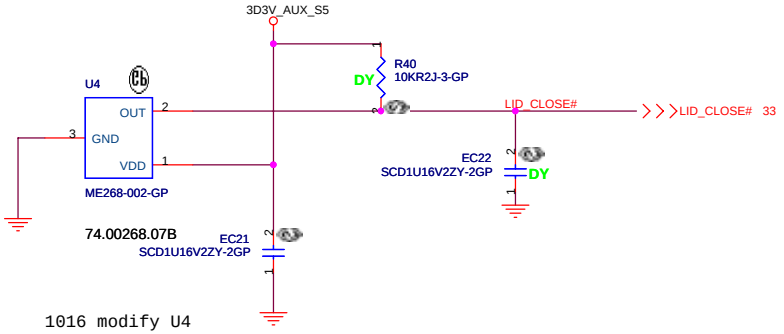


1017 modify RN60

1

1226 modify TP_L1 and TP_R1

Cover Up Switch



1016 modify U4

1017 modify U4

1017 add U61,R52,EC24 and EC23

1020 delete U61,R52,EC24 and EC23

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: SWITCHS

Size | Document Number: LA14 | Rev: SB

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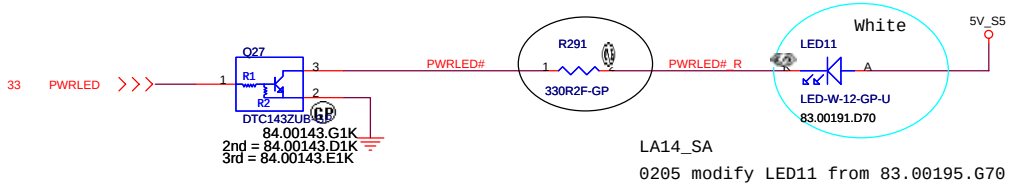
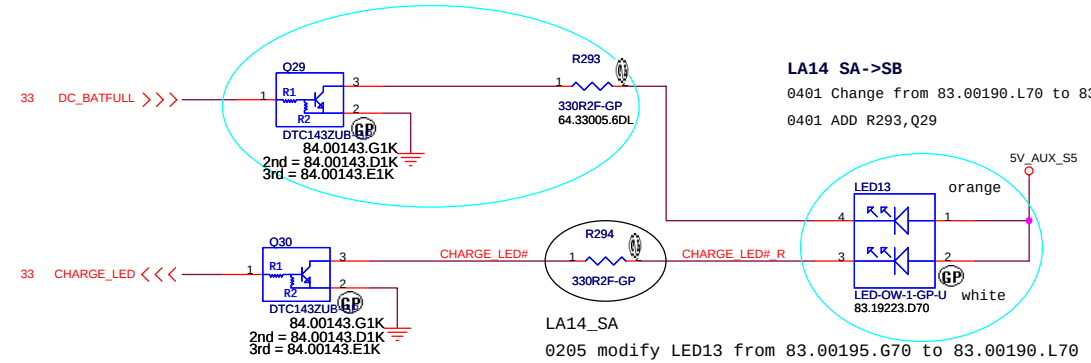


LA14_SA

0205 modify LED11 from 83.00195.G70 to 83.00190.L70



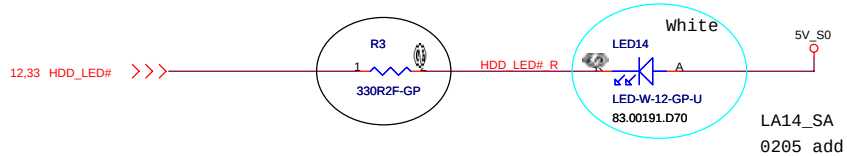
LA14 SA->SB

0401 Change from 83.00190.L70 to 83.19223.D70

0401 ADD R293,Q29

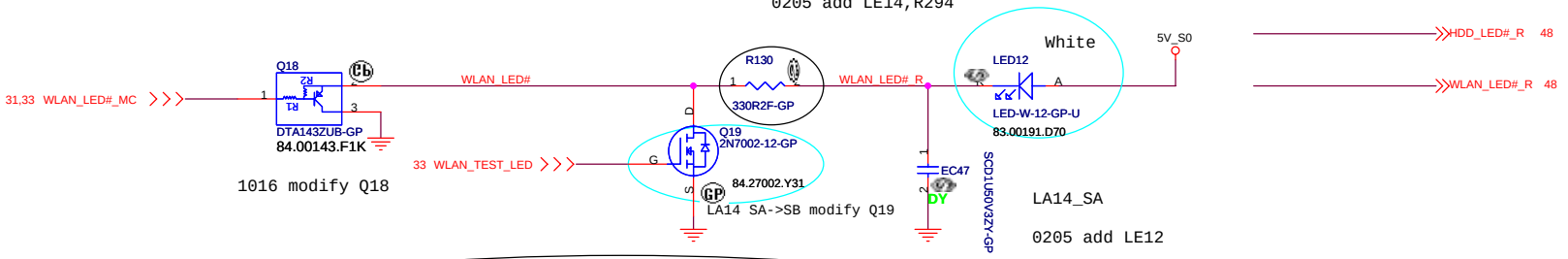
LA14_SA

0205 modify LED13 from 83.00195.G70 to 83.00190.L70



LA14_SA

0205 add LE14,R294

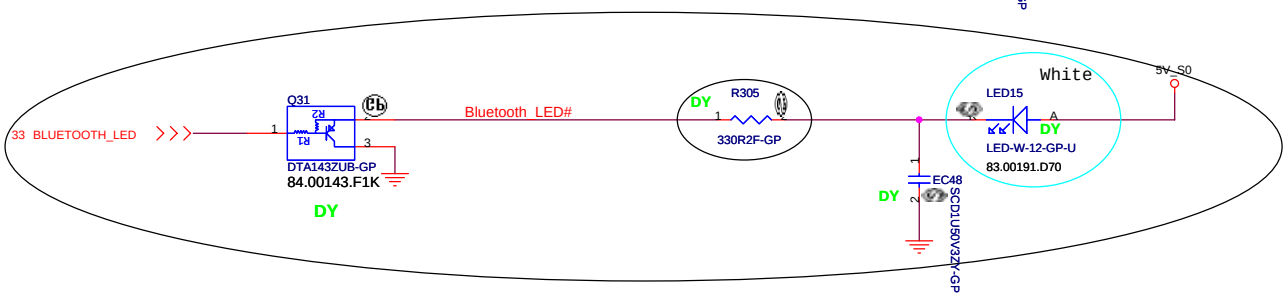


1016 modify Q18

LA14 SA->SB modify Q19

LA14_SA

0205 add LE12



LA14_SA

0209 Change R305,R291,R294,R130,R3 from 29L2589AA to 64.33005.6DL

LA14 SA->SB

0331 Change LED11,LED12,LED14,LED15 from 83.19213.H70 to 83.00191.D70

<Core Design>

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Title		
LED		
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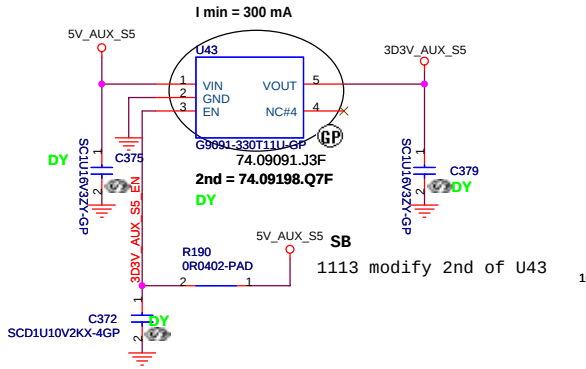
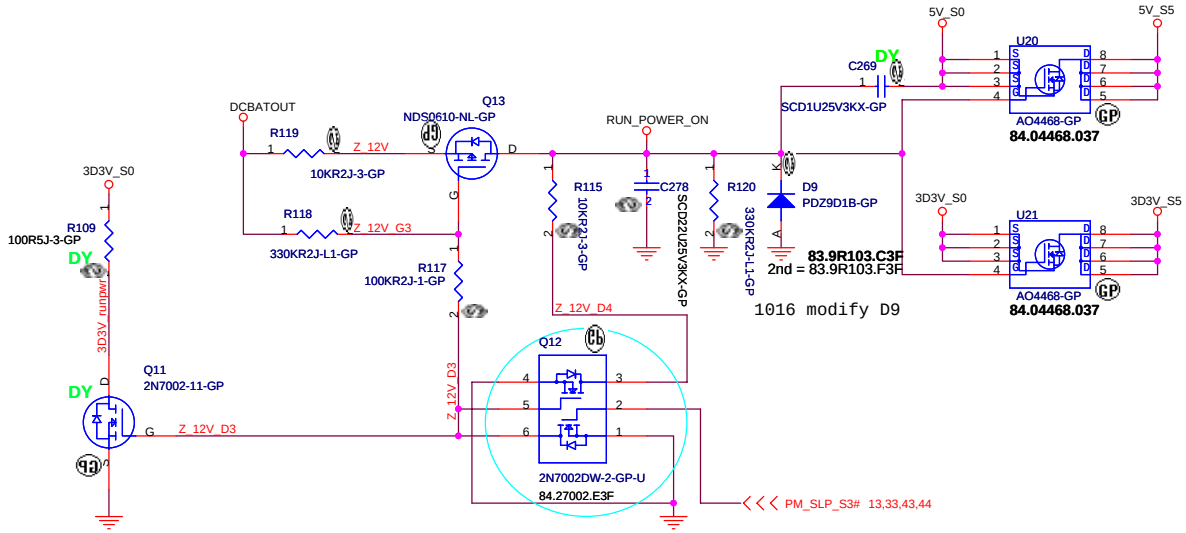
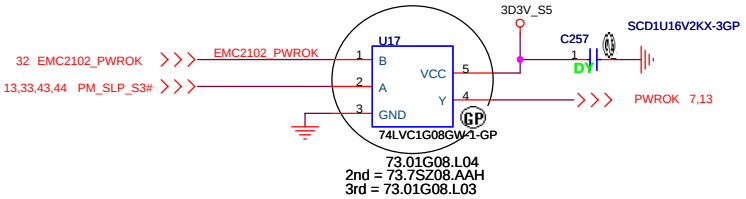
Aux Power 3D3V_AUX_S5



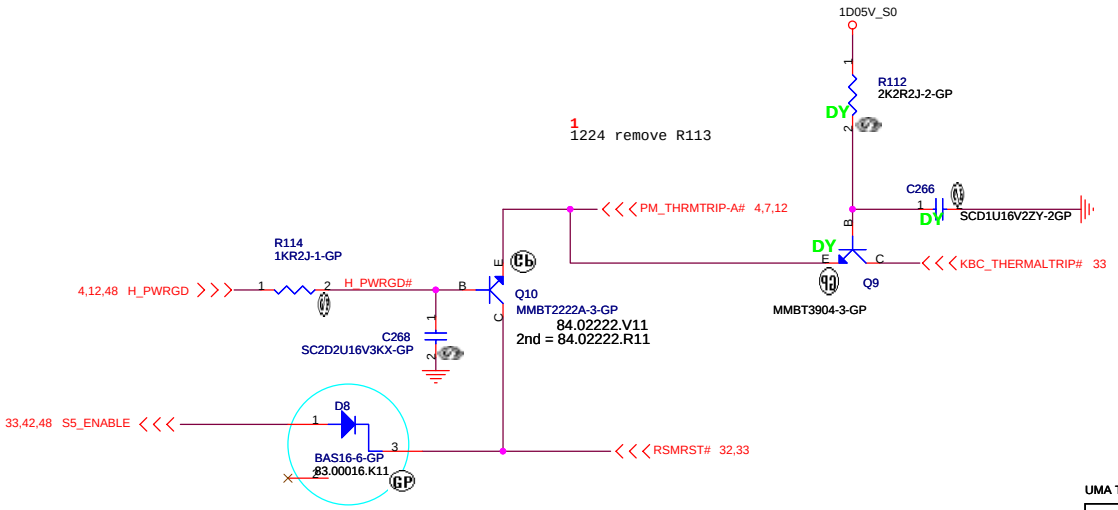
Run Power



LA14 SA->SB
0403 Change Q12 from 84.27002.D3F to 84.27002.E3F



1
1224 remove R113



LA14 SA->SB
0403 Change D8 from 83.00016.B11 to 83.00016.K11

UMA Two Phase

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**RUN POWER and 3D3V_AUX_S5**
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CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VGATE_PWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125

S5_ENABLE

ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Charger BQ24745

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

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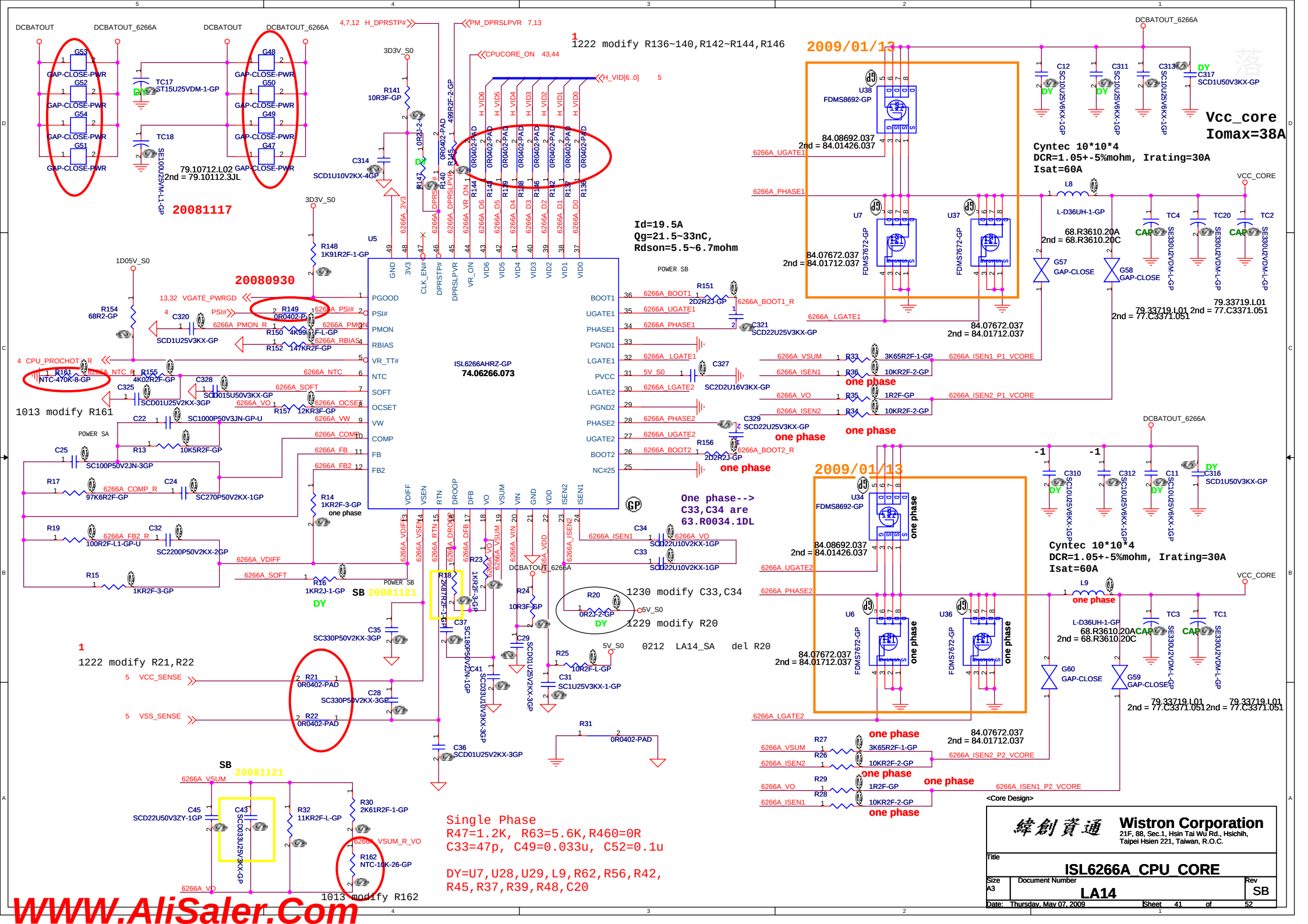
1222 modify R136~140,R142~R144,R146
2009/01/13
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
ISL6266AHRZ-GP
74.06266.073
20081117
20080930
1013 modify R161
1222 modify R21,R22
SB 20081121
One phase--> C33,C34 are 63.R0034.1DL
1230 modify C33,C34
1229 modify R20
0212 LA14_SA del R20
Single Phase
R47=1.2K, R63=5.6K,R460=0R
C33=47p, C49=0.033u, C52=0.1u
DY=U7,U28,U29,L9,R62,R56,R42,
R45,R37,R39,R48,C20
1013 modify R162
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
LA14
SB
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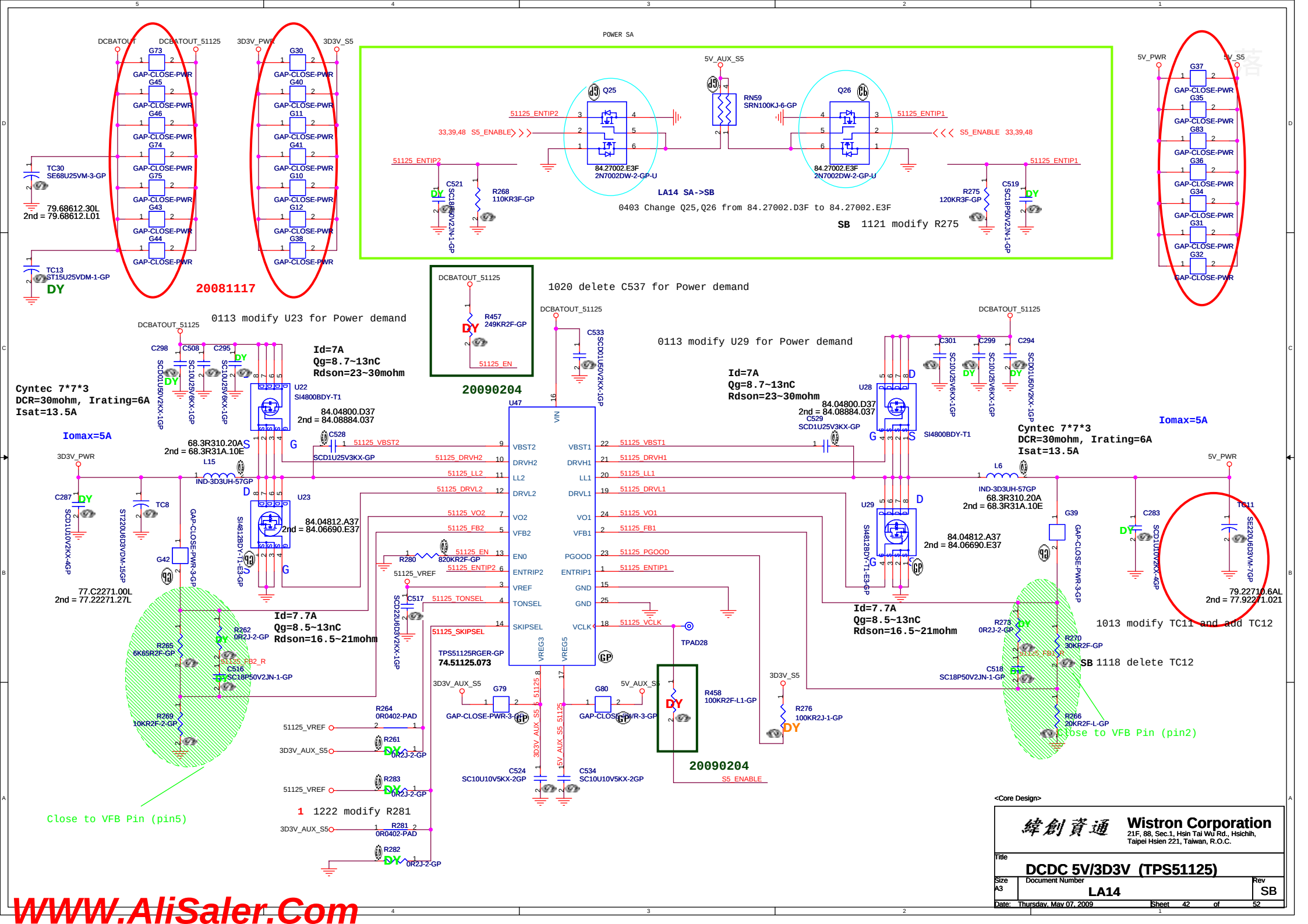
POWER SA
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
Q25
Q26
RN59
SRN100KJ-6-GP
51125_ENTIP2
51125_ENTIP1
33,39,48 S5_ENABLE
S5_ENABLE 33,39,48
84.27002.E3F
2N7002DW-2-GP-U
LA14 SA->SB
0403 Change Q25,Q26 from 84.27002.D3F to 84.27002.E3F
SB 1121 modify R275
20081117
0113 modify U23 for Power demand
1020 delete C537 for Power demand
0113 modify U29 for Power demand
20090204
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Iomax=5A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
Id=7.5A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
1 1222 modify R281
1013 modify TC11 and add TC12
SB 1118 delete TC12
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
LA14
SB
Thursday, May 07, 2009
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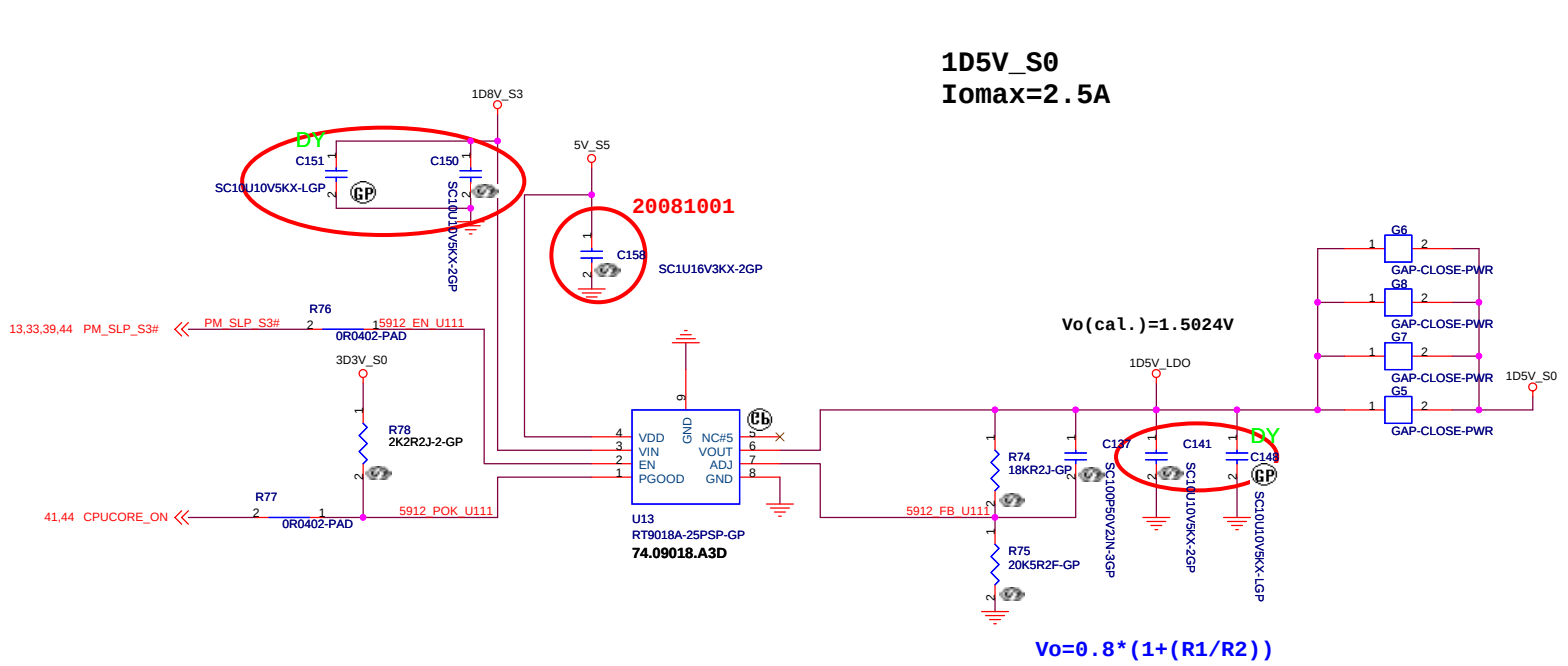

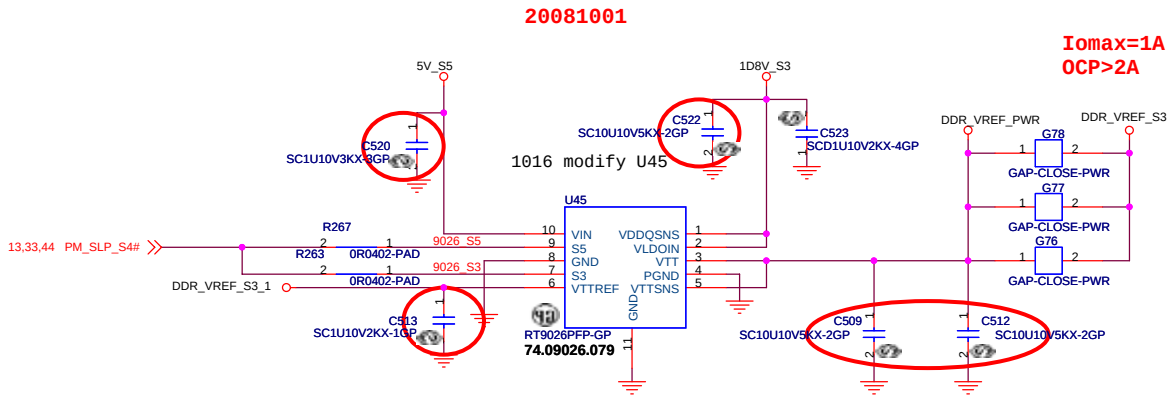

<Core Design>

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Title: 1D5V & 0D9V

Size: A3 | Document Number: LA14 | Rev: SB

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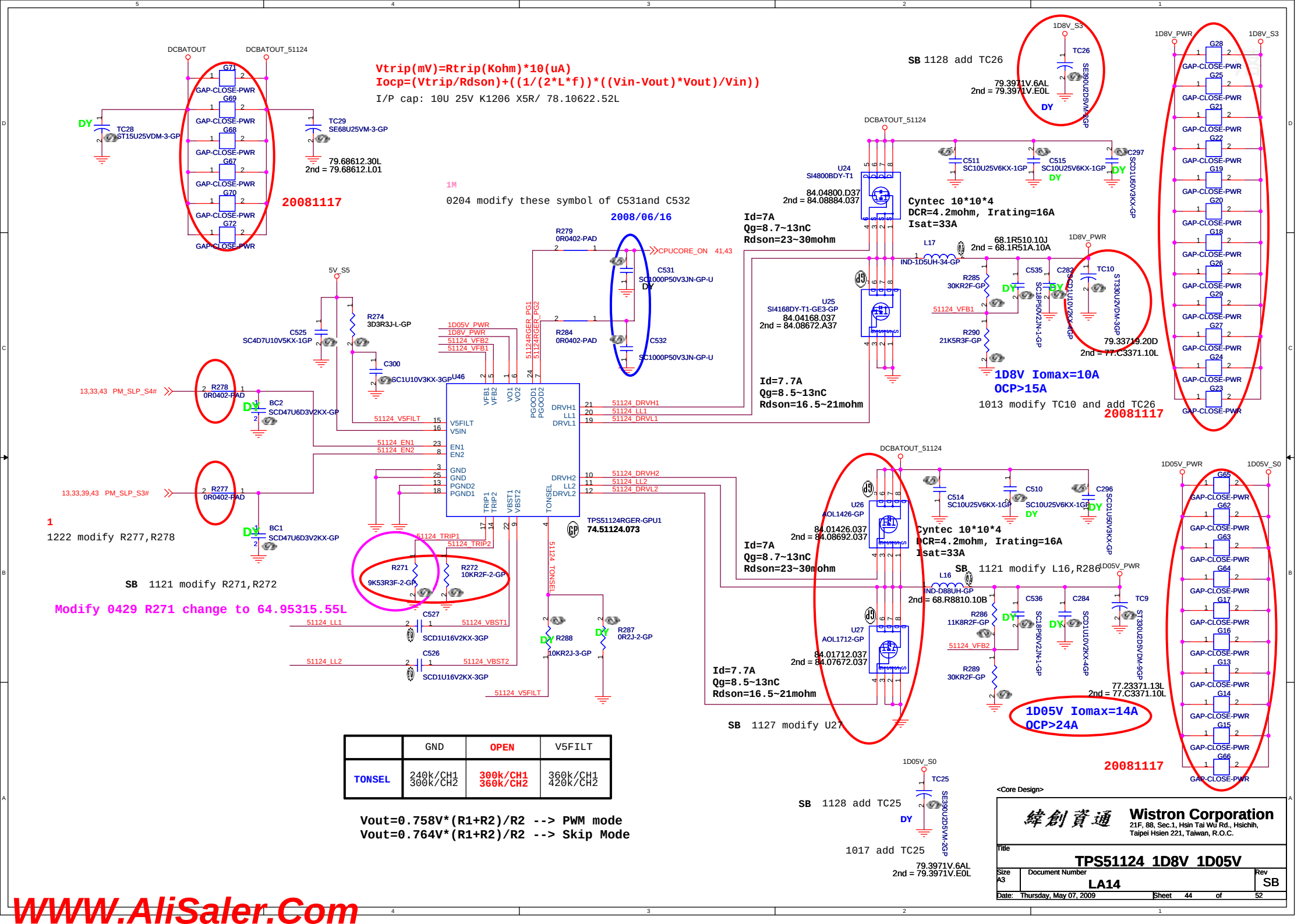
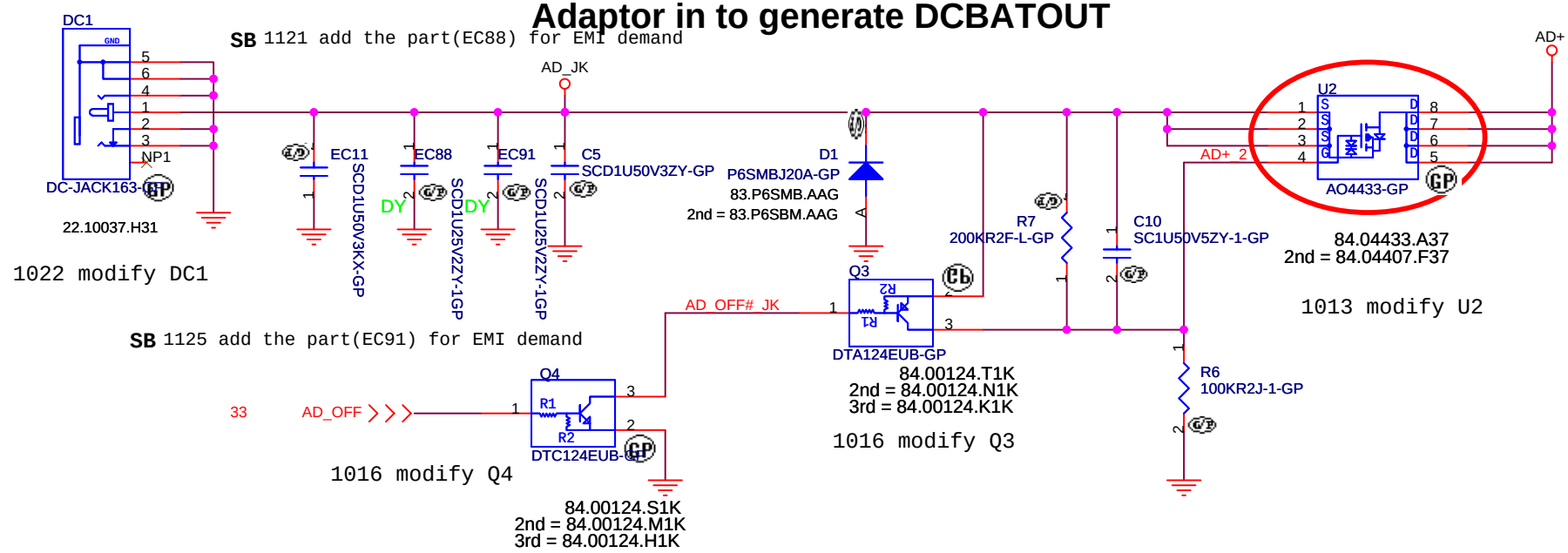


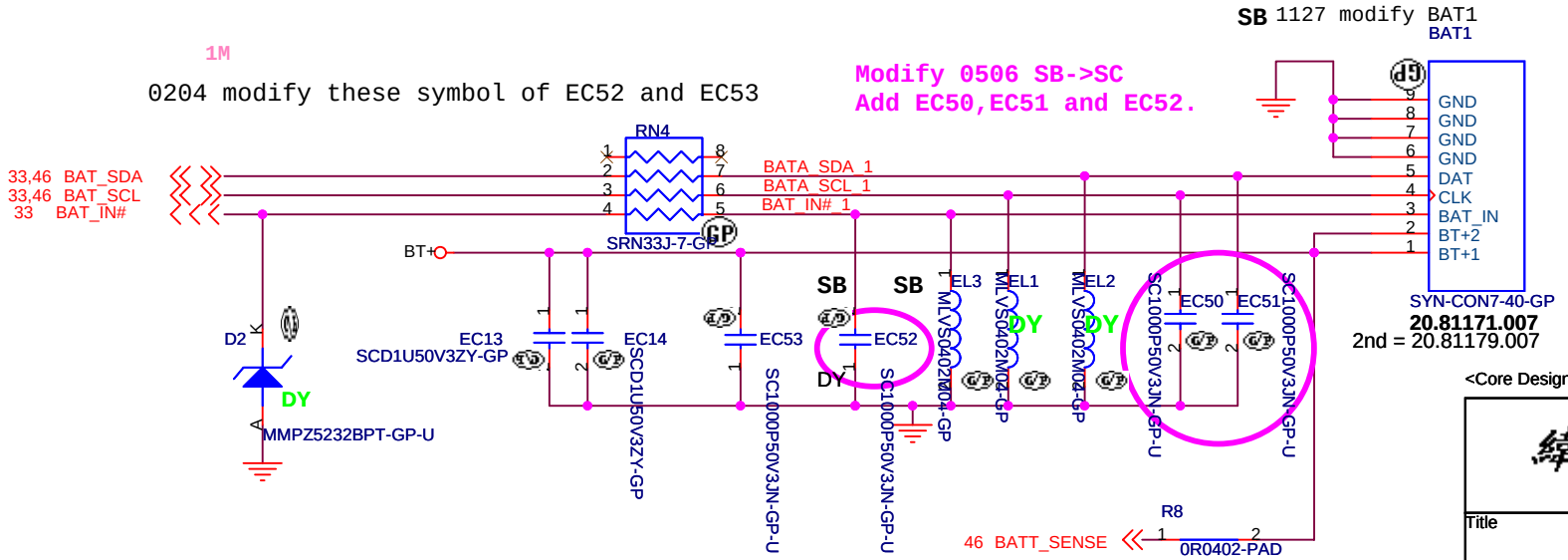
Adaptor in to generate DCBATOUT



LA_SA 0216 Change DC1 from 22.10037.F11 to 22.10037.H31

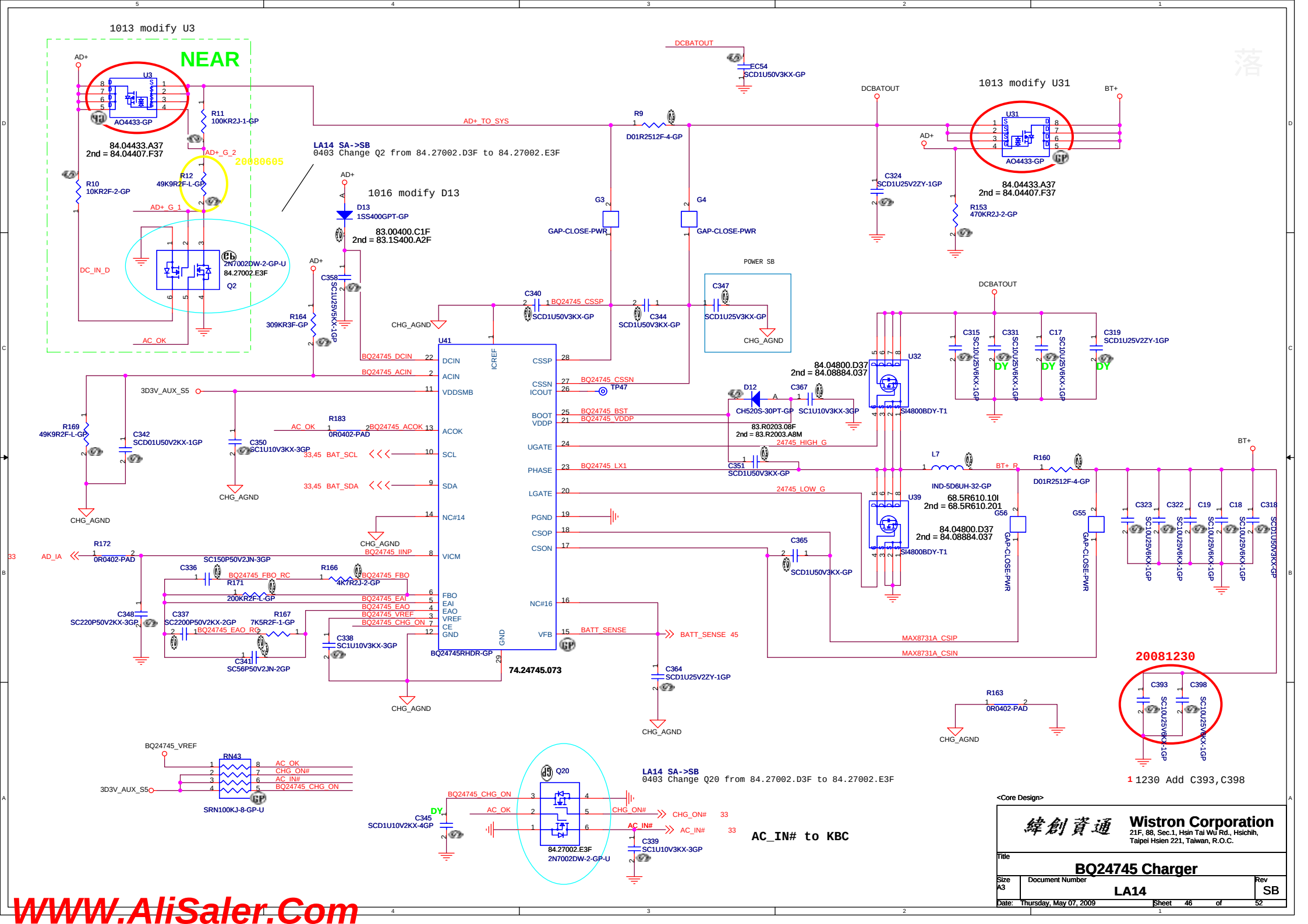
BATA_SDA_1 48
BATA_SCL_1 48
BAT_IN#_1 48

BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size	Document Number **LA14**	Rev SB
Date: Thursday, May 07, 2009	Sheet 45 of 52	


1013 modify U3
NEAR
AO4433-GP
84.04433.A37
2nd = 84.04407.F37
R11 100KR2J-1-GP
R10 10KR2F-2-GP
R12 49K9R2F-L-GP
20080605
AD+_G_2
AD+_G_1
2N7002DW-2-GP-U
84.27002.E3F
Q2
DC_IN_D
AC_OK
AD+_TO_SYS
LA14 SA->SB
0403 Change Q2 from 84.27002.D3F to 84.27002.E3F
1016 modify D13
D13 1SS400GPT-GP
83.00400.C1F
2nd = 83.1S400.A2F
C358 SC1U25V3KX-1GP
R164 309KR3F-GP
DCBATOUT
EC54 SCD1U50V3KX-GP
R9 D01R2512F-4-GP
G3 GAP-CLOSE-PWR
G4 GAP-CLOSE-PWR
POWER SB
C347 SCD1U25V3KX-GP
C340 SCD1U50V3KX-GP
C344 SCD1U50V3KX-GP
BQ24745_CSSP
CHG_AGND
1013 modify U31
U31 AO4433-GP
84.04433.A37
2nd = 84.04407.F37
C324 SCD1U25V2ZY-1GP
R153 470KR2J-2-GP
BT+
U41
BQ24745RHDR-GP
74.24745.073
ICREF
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745_DCIN
BQ24745_ACIN
BQ24745_ACOK
BQ24745_IINP
BQ24745_FBO_RC
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_EAO_RC
BQ24745_CSSN
BQ24745_BST
BQ24745_VDDP
BQ24745_LX1
24745_HIGH_G
24745_LOW_G
BATT_SENSE
BATT_SENSE 45
MAX8731A_CSIP
MAX8731A_CSIN
TP47
D12 CH520S-30PT-GP
C367 SC1U10V3KX-3GP
C351 SCD1U50V3KX-GP
83.R0203.08F
2nd = 83.R2003.A8M
U32 SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
U39 SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
L7 IND-5D6UH-32-GP
68.5R610.10I
2nd = 68.5R610.201
R160 D01R2512F-4-GP
C315 SC10U25V6KX-1GP
C331 SC10U25V6KX-1GP
C17 SC10U25V6KX-1GP
C319 SCD1U25V2ZY-1GP
C323 SC10U25V6KX-1GP
C322 SC10U25V6KX-1GP
C19 SC10U25V6KX-1GP
C18 SC10U25V6KX-1GP
C318 SCD1U50V3KX-GP
C365 SCD1U50V3KX-GP
C364 SCD1U25V2ZY-1GP
G56 GAP-CLOSE-PWR
G55 GAP-CLOSE-PWR
R163 0R0402-PAD
20081230
C393 SC10U25V6KX-1GP
C398 SC10U25V6KX-1GP
1 1230 Add C393,C398
R169 49K9R2F-L-GP
C342 SCD01U50V2KX-1GP
C350 SC1U10V3KX-3GP
R183 0R0402-PAD
R172 0R0402-PAD
SC150P50V2JN-3GP
C336
R171 200KR2F-1-GP
R166 4K7R2J-2-GP
C348 SC220P50V2KX-3GP
C337 SC2200P50V2KX-2GP
R167 7K5R2F-1-GP
C338 SC1U10V3KX-3GP
C341 SC56P50V2JN-2GP
AD_IA
33,45 BAT_SCL
33,45 BAT_SDA
3D3V_AUX_S5
CHG_AGND
BQ24745_VREF
RN43
SRN100KJ-8-GP-U
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q20
2N7002DW-2-GP-U
84.27002.E3F
C345 SCD1U10V2KX-4GP
C339 SC1U10V3KX-3GP
LA14 SA->SB
0403 Change Q20 from 84.27002.D3F to 84.27002.E3F
AC_IN# to KBC
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number LA14
Rev SB
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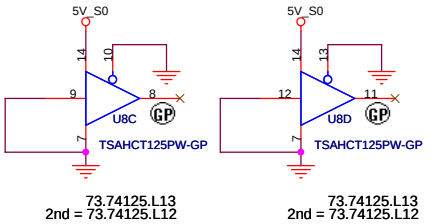
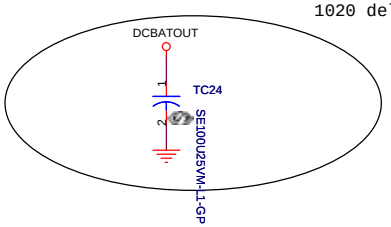


73.74125.L13
2nd = 73.74125.L12

73.74125.L13
2nd = 73.74125.L12

1020 delete TC14,TC15

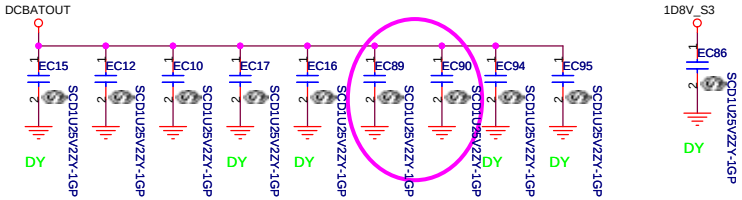


SB
1117 delete TC19

79.10712.L02
2nd = 79.10112.3JL

1016 modify U32

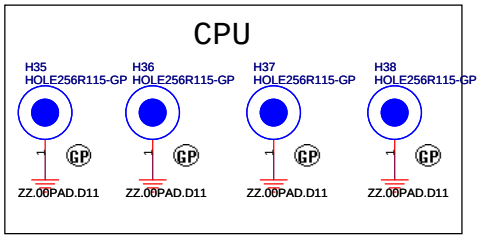
1017 add these parts(EC10,EC12,EC15~EC17,EC86) for EMI demand
1020 add the part(EC86) for EMI demand
1125 add the part(EC90) for EMI demand
SB 1121 add the part(EC89) for EMI demand
1128 add EC94,EC95 for EMI demand



Modify 0506 SB->SC
Add EC89 and EC90 for EMI demand

1016 add GND1 and GND2 for EMI demand
1017 add GND3 and modify GND2 for EMI demand

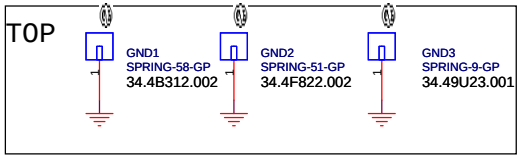
LA14 SA->SB
0401 DY GND9
0402 Del GND4,GND7,GND8,GND9



1016 modify H35~H38
1016 delete H9~H12

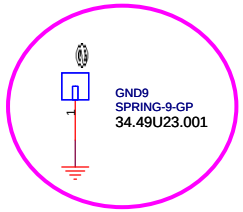
LA14 SB 0402 modify H35~H36

1016 modify H31 and H32
SB 1120 remove H31and H32



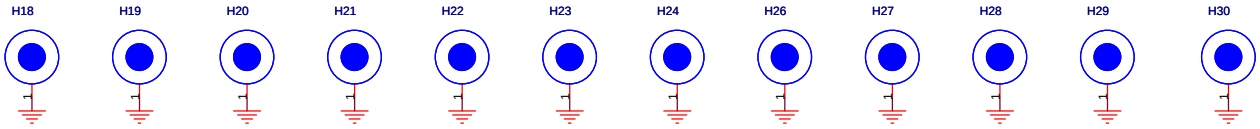
SB 1128 Add GND4,GND7,GND8

1 1230 Add GND9



Modify 0506 SB->SC
Add GND9 for EMI demand

LA_SA 0218 Change H35~H38 from ZZ.00PAD.571 to ZZ.00PAD.801



LA14 SA->SB
0401 DY H8
0402 Del H8

SB 1128 Add H43

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Title: EMI/Spring/Boss
Size: Document Number: LA14 Rev: SB
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Speaker

27,28	SPKR_R+	AFTE14P-GP	TP244
27,28	SPKR_R-	AFTE14P-GP	TP243
27,28	SPKR_L+	AFTE14P-GP	TP245
27,28	SPKR_L-	AFTE14P-GP	TP246

Touch pad

	5V_S0	AFTE14P-GP	TP109
35	TP_DATA	AFTE14P-GP	TP105
35	TP_CLK	AFTE14P-GP	TP110
35,37	TP_RIGHT	AFTE14P-GP	TP114
35,37	TP_LEFT	AFTE14P-GP	TP113

Keyboard

33	KCOL16	AFTE14P-GP	TP127
33	KCOL15	AFTE14P-GP	TP139
33	KCOL14	AFTE14P-GP	TP148
33	KCOL13	AFTE14P-GP	TP146
33	KCOL8	AFTE14P-GP	TP98
33	KCOL7	AFTE14P-GP	TP99
33	KCOL6	AFTE14P-GP	TP101
33	KCOL5	AFTE14P-GP	TP100
33	KCOL4	AFTE14P-GP	TP118
33	KCOL3	AFTE14P-GP	TP138
33	KCOL2	AFTE14P-GP	TP122
33	KCOL1	AFTE14P-GP	TP123
33	KROW0	AFTE14P-GP	TP152
33	KROW7	AFTE14P-GP	TP154
33	KROW6	AFTE14P-GP	TP153
33	KROW5	AFTE14P-GP	TP151
33	KROW4	AFTE14P-GP	TP94
33	KROW3	AFTE14P-GP	TP95
33	KROW2	AFTE14P-GP	TP92
33	KROW1	AFTE14P-GP	TP97
33	KCOL12	AFTE14P-GP	TP260
33	KCOL11	AFTE14P-GP	TP116
33	KCOL10	AFTE14P-GP	TP117
33	KCOL9	AFTE14P-GP	TP102
33	KCOL17	AFTE14P-GP	TP72
33	KCOL0	AFTE14P-GP	TP87

Bluetooth

22	USB_7-	AFTE14P-GP	TP134
22	USB_7+	AFTE14P-GP	TP136
22	3D3V_BT_S0	AFTE14P-GP	TP133

1017 modify USB signal connection

LED

	5V_S0	AFTE14P-GP	TP88
38	WLAN_LED#_R	AFTE14P-GP	TP229
36	NOVO_BT#	AFTE14P-GP	TP230
36	WIRELESS_BTN#_1	AFTE14P-GP	TP231
36	CAP_LED#_R	AFTE14P-GP	TP91
36	NUM_LED#_R	AFTE14P-GP	TP90
38	HDD_LED#_R	AFTE14P-GP	TP234
	3D3V_S0	AFTE14P-GP	TP253
36	KBC_PWRBTN#_1	AFTE14P-GP	TP254

SB

1112 remove the signal(STDBY_LED#_R)

Battery

45	BATA_SDA_1	AFTE14P-GP	TP16
45	BATA_SCL_1	AFTE14P-GP	TP17
45	BAT_IN#_1	AFTE14P-GP	TP15
	BT+	AFTE14P-GP	TP14
	BT+	AFTE14P-GP	TP13
	AD_JK	AFTE14P-GP	TP6
		AFTE14P-GP	TP5

Check test point

	3D3V_S0	AFTE14P-GP	TP237
	3D3V_AUX_S5	AFTE14P-GP	TP240
	3D3V_S5	AFTE14P-GP	TP236
	5V_S5	AFTE14P-GP	TP238
4,12,39	H_PWRGD	AFTE14P-GP	TP241
33,39,42	S5_ENABLE	AFTE14P-GP	TP242
4,6	H_CPURST#	AFTE14P-GP	TP239

Test Point放在Dimm Door打開可量測處

FAN

32	EMC2102_FAN_TACH	AFTE14P-GP	TP187
32	EMC2102_FAN_DRIVE	AFTE14P-GP	TP188

落

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AFTE test point**

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0910 delete F4(Page 18)
0910 update footprint of U15(Page 30)
0910 delete RIGHT1 and LEFT1(Page 33)
0910 modify net names of TP_LEFT and TP_RIGHT(Page 36)
0910 modify test points of AFTE and TPAD
0911 modify net name from LPC_RST to PLT_RST1#(Page 24)
0911 add net name(RBIAS,LED_DUPLEX#,SMDATA,SMCLK)(Page 24)
0911 add net name(DVDD_1_8,ACZ_SDATAIN0_R,FLY_P,FLY_N,VREF_LO,VREF_HI)(Page 26)
0911 add net name(EAPD#_R)(Page 27)
0912 modify the schematic of Page 33
0912 delete GMCH_TXB*(Page 7& 18)
0912 add these parts for EMI demand(page 7,18,20,21,23,26,28,29,30,32,33,34,35)
0915 modify net name from 10M/100M/1G_LED# to 10M/100M_LED#(page24,25)
0915 delete these parts for EMI demand(page 30)
0915 add EC34 for EMI demand(page3)
0915 add EC73 for EMI demand(page 12)
0915 modify LEDs port
0916 move net(SPI_WP#) from U9 pin120 to pin25(page33)
0930 modify BLUE1(page22)
0930 add 2nd for SPK1, MIC1 and modify LOUT1 (page28)
0930 modify FAN1(page32)
0930 modify TPAD1(page35)
0930 modify KB1(page33)
0930 modify net name for BIOS demand(page33)
1001 delete these parts for EMI demand(ED1~8)
1009 modify net name for GND to AGND(page27)
1009 add R4,R5 for AC decopling(page27)
1009 add R96(page30)
1013 modify TPAD1(page35)
1013 modify U40 from 72.25X16.001 to 72.25X16.A01(page 34)
1013 modify TC11 and add TC12(page42)
1013 modify TC10 and add TC26(page44)
1013 modify U2(page45)
1013 modify U3 and U31(page 46)
1013 modify R161 and R162(page41)
1013 modify card1(page 30)
1014 modify these LEDs(LED11,LED12)(page38)
1014 modify these nets(page 26)
1014 modify R258 from 10k to 20k ohm(page26)
1014 add ER5 for EMI deamnd(page3)
1015 modify LCD1 pin define(page 18)
1015 modify the power from 3D3V_S5 to 5V_S5(page38)
1015 modify TPAD1(page35)
1015 modify RN57(page28)
1015 modify F1(page18)

<Core Design>

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Title: Change List

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1016 modify L1,L2 and L3(page 19)
1016 modify XF1(page 25)
1016 modify RN53 and U10(page 24)
1016 modify U8(page19,47)
1016 modify U4(page 37)
1016 modify U23(page 43)
1016 modify X2(page12)
1016 modify X1(page 33)
1016 modify X3(page 3)
1016 modify D13(page 46)
1016 modify D23(page 20)
1016 modify D9(page 39)
1016 modify D4(page 19)
1016 modify Q3 and Q4(page45)
1016 modify Q18(page 36)
1016 modify Q15~Q17(page 36)
1016 modify Q27~Q30(page38)
1016 modify Q6 and Q14(page 32)
1016 modify Q8(PAGE 24)
1016 add GND1 nad GND2 for EMI demand(page 47)
1016 modify LCD1 pin define(page 18)
1016 delete H9~H12 and modify H35~H38,H31,H32(page 47)
1017 add these parts for EMI demand(page 47)
1017 delete these parts(EC208~EC210)(page 7)
1017 modify BLUE1(page 22)
1017 modify FAN1(page 32)
1017 modify R291 and R293(page 38)
1017 add U61,R52,EC23 and EC24(page 37)
1017 modify RN60(page37)
1017 add TC25(page 44)
1017 add GND3 and modify GND2 for EMI demand(page 47)
1017 modify USB signal connection(page13,18,22,23,30,31,48)
1020 delete C537 for Power demand(page42)
1020 add the part(EC86) for EMI demand(page 47)
1020 delete U61,R52,EC24 and EC23(page 37)
1020 delete TC14,TC15(page 47)
1021 modify TC16(page 31)
1021 delete TC23(page 23)
1021 modify TC5(page 20)
1021 modify and swap these parts(USB1 and USB2)(page 23)
1021 modify SATA1(page 20)
1022 modify DC1(page 45)

<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Change List

Size	Document Number	Rev
	LA14	SB

Date: Thursday, May 07, 2009 Sheet 50 of 52

SA to SB

1106 modify net connection of RN46 and RN44(page33) for layout demand
1106 modify LED11 and LED12(page38) for fixing issue
1106 modify LED power from 5V_S5 to 5V_AUX_S5(page38) for customer demand
1112 remove the signal(STDBY_LED#_FR)page38 for customer demand
1112 remove these signals(STDBY_LED#_FR and STDBY_LED#_R) and R131(page36) for customer demand
1112 remove the signal(STDBY_LED#_R)page36 for customer demand
1112 remove the signal(STDBY_LED#_R)and TP253(page48) for customer demand
1113 modify C103 and C106(page24) for crystal issue
1113 modify 2nd of U19(page26)
1113 modify 2nd of U43(page39)
1113 modify 2nd of U44(page10)
1113 modify U48(page22)
1117 delete MDC function(R231,R237,R232,R234)(page12)
1117 delete TC19(page 47) for ME deamnd
1118 modify PCB Ver. from SA to SB(page33)
1118 delete TC12(page42) for layout demand
1118 delete TC27(page9) for layout demand
1118 delete R107 and add L18 for cost down
1119 modify R130 and R133(page 36) for LED brightness
1119 modify EC52 and EL3(page45) for EMI demand
1119 modify SPK1(page 28) for ME deamnd
1119 add G84 for RTC reset demand
1120 modify EC78for EMI demand((page10)
1120 modify PowerCN1 pin3 and remove EC44(page36) fro LED function
1120 remove H31 and H32(page47)for ME demand
1120 add RN61 and RN62(page3) for layout demand
1120 swap these nets(CLK_MCH_3GPLL,CLK_MCH_3GPLL#, CLK_PCIE_MINI1,CLK_PCIE_MINI1#)(page3)for CLK REQ demand
1120 add the net(SATACLKREQ#)(page3,13)for CLK REQ demand
1120 move these nets (CLK_PCIE_MINI1,CLK_PCIE_MINI1#)(page3)for CLK REQ demand
1120 modify RN61 and RN62(page3)for CLK REQ demand
1121 add EC87 for EMI demand(page18)
1121 add the part(EC89) for EMI demand(page47)
1121 add the part(EC88) for EMI demand(page45)
1121 modify R18,C43(page41) for Power demand
1121 modify R275(page42)for Power demand
1121 modify R271,R272,R286 and L16(page44) for Power demand
1124 modify U42 and delete R182,R185 (page32) for thermal function
1124 modify these names of these nets(G7922_SGND2,G7922_SGND3...) (page32) for thermal function
1124 add R302(page3) for clock gen function
1125 add the part(EC90) for EMI demand(page47)
1125 add the part(EC91) for EMI demand(page45)
1125 modify R125,R126(page18) for LCD brightness control
1125 modify RN40 and delete RN42(page32) for layout demand
1125 add EC92 and EC93 for EMI demand(page 22)
1126 add these nets (PCIE_REQ_LAN#,PCIE_REQ_MINI#)(page3)for CLK REQ demand
1126 delete R230,R233,R235,R236 and RN63(page12) for removing MDC function
1126 add C541 and modify R101(page26) for codec function
1126 modify RN61 and RN62(page3) for layout demand
1126 modify EU1,EU2 and add EU3,EU4 for EMI demand(page28)
1127 modify CRT1(page19) for customer demand
1127 swap the nets of RN61 and RN62 for layout demand(page3)
1127 modify BAT1(page45) for ME demand
1127 modify U27(page44) for power demand
1127 modify C377(page32) for thermal function
1128 Add H43,GND4,GND7,GND8(page47) for EMI demand
1128 modify LCD1(page18) for cost down
1128 Add L19(page24) for vender demand
1128 add EC94,EC95 for EMI demand(page47)
1201 modify C3 (page18)
1201 modify EC6~9(page28)
1204 modify RN36
1204 modify second source of RJ1

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SB to 1

1222 modify U42 for customer demand(page32)
1222 modify these names of nets (BMC2102_DN2,DP2,DN3,DP3,PWROK,FAN_TACH,FAN_DRIVE)(page32)
1222 modify RN58 from 68 to 56 ohm for customer demand(page28)
1222 modify PCB Ver. from SB to -1(page33)
1222 modify TC5 for HDD side(page20)
1222 modify card1 from 20.I0043.001 to 20.I0043.011for CE demand(PAGE30)
1223 modify the net(EMC2102_CLK_SEL) for reducing component (page32)
1223 modify the net(RSMRST#) for reducing component(page33)
1224 dummy C6(page27)
1224 add R306 for FSB Dynamic ODT(dummy)(page7)
1224 add R307 and R308 for LAN co-layout demand(page24)
1224 modify FAN1for CE demand(page32)
1224 remove R113 for reducing component (page39)
1224 modify RN54 for reducing component (page12)
1224 modify R191,RN48 and this net AD_OFF for reducing component (page33)
1224 modify D5(dummy)(page20)
1224 delete R165 and add RN64 for reducing component (page32)
1226 modify TP_L1 and TP_R1 for ME demand(page37)
1226 modify R100 and C240(dummy)(page30)
1226 delete R96 for reducing component (page30)
1229 modify C76,C77 from 12pF to 15pF for vender demand(page12)
1229 modify L19 for vender demand(page24)
1229 modify U30 for cost down(page18)
1229 modify U44 for cost down(page10)
1229 modify R20 for power team demand(page41)
1230 modify the name of net(RST#_CHIP)(beacuse R97 was removed)(page30)
1230 modify ODD1 for CE demand(page21)
1230 modify C33,C34 for power team demand (page41)
1230 modify D14 for CE demand(page33)
1230 Add C393,C398 for power team demand(page46)
1230 Add GND9 for EMI demand(page47)
1230 dummy C507(page26)
1230 delete Q1 and modify U1 for new AMP IC(page27)
1230 delete RN35 and add R309(page27)
1231 modify R80 for clock gen voltage(3.3V to 1.05V) (page3)
1231 modify ODD1 for ME demand(page21)
0105 modify R3,R128,R129,R130,R132 and R133 for LED brightness conrtol(page36)
0105 modify R291,R292,R293 and R294 for LED brightness conrtol (page38)
0105 modify L1,L2 and L3 for EMI demand(page19)
0112 modify TC10(page44)
0113 modify ODD1 for ME demand(page21)
0113 modify U34,U38,U6,U7,U36 and U37 for power demand(page41)
0113 modify U23 and U29 for power demand(page42)
0113 modify U25,U27,TC10 and L16 for power demand(page44)

1 to 1M

0121 modify PCB Ver. from 1 to 1M(page33)
0121 add R310(page26)
0204 add R457,R458 for power demand(co-layout)(page42)
0204 modify R130,R132 and R133 for LED brightness conrtol(page36)
0204 modify KB1 for CE demand(add mylar)(page33)
0204 modify the symbol of C22 (page41)
0204 modify these symbol of C531and C532 (page44)
0204 modify these symbol of EC52 and EC53 (page45)
0204 modify the symbol of EC74 (page23)

0 ohm to short pad

1222 modify R277,R278(page44)
1222 modify R135,R5(page27)
1222 modify R58(page25)
1222 modify R136~140,R142~R144,R146,R149(page41)
1222 modify R21,R22(page41)
1222 modify R80,R87(page3)
1222 modify R252(page10)
1222 modify R209(page13)
1222 modify R68,R69,R79(page24)
1222 modify R97(page30)
1222 modify R159(page31)
1222 modify R189(page33)
1222 modify R281(page42)
1222 modify ER1~ER4(page28)
1224 modify R91(page3)
1224 modify R67,R71(page24)
1224 modify ERN2(page34)

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