

Model Name : ZIWB0/ZIWB1/ZIWE0

File Name :

Compal Confidential

ZIWB0/ZIWB1/ZIWE0 UMA M/B Schematics Document

Intel Bay Trail M

2014-02-10

REV:1.0

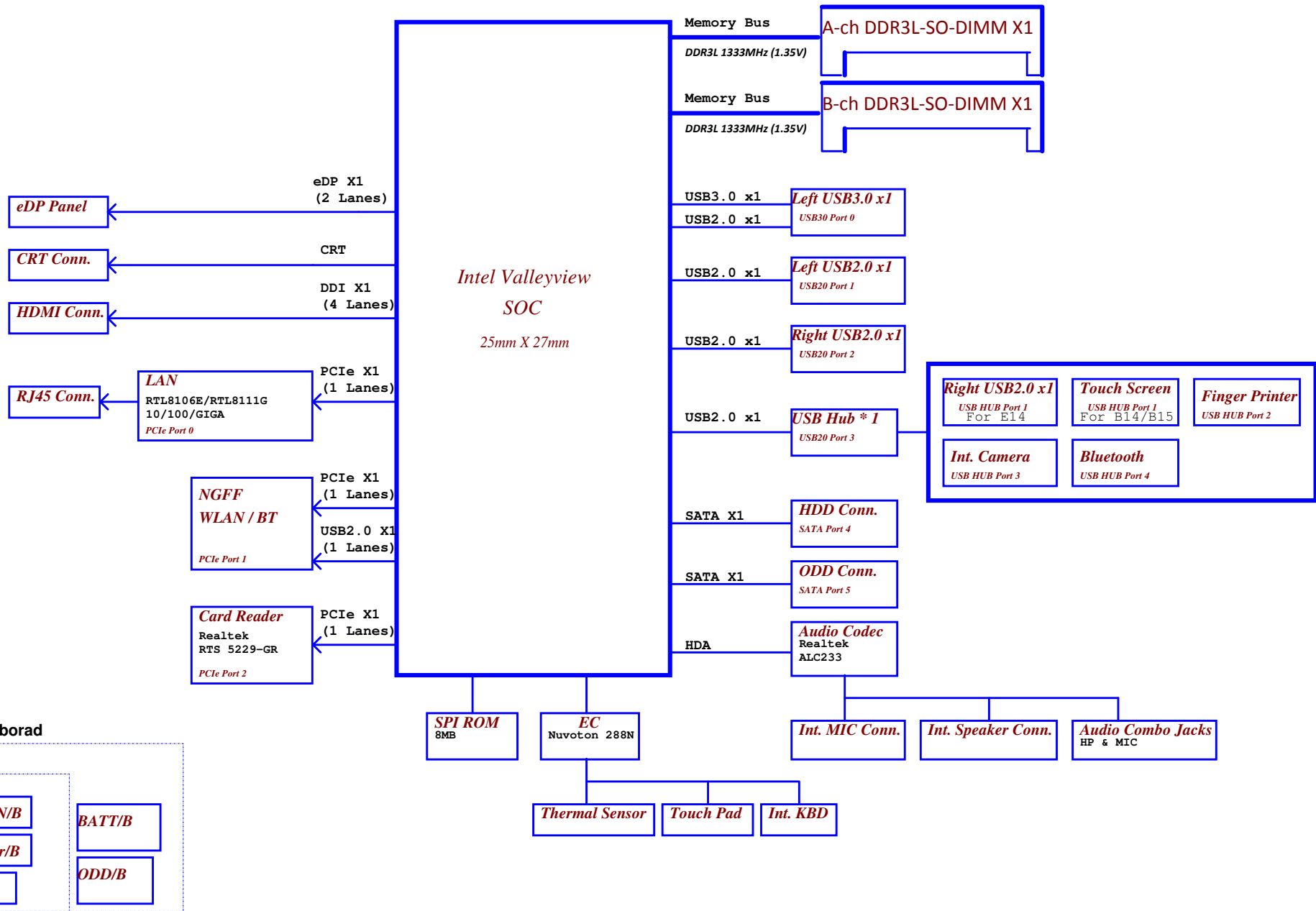
14PCB@
DA1 PCB

Part Number	Description
DA60013Z010	REV1.0 M/B

15PCB@
DA2 PCB

Part Number	Description
DA60013Z110	REV1.0 M/B

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Touch Screen	TS@
B/E series sku	B14@
B/E series sku	B15@
B/E series sku	E14@

EC SM Bus1 address

EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

Device	Address
GPU	0x9E
Thermal	1001_101xb

43 level BOM table

43 Level	Description	BOM Structure

USOC1
N2920@

S IC FH8065301616203 SR1SF B3 1.86G C38!
Part Number = SA00007E860

USOC1
N3520@

S IC FH8065301616103 SR1SE B3 2.17G C38!
Part Number = SA00007E990

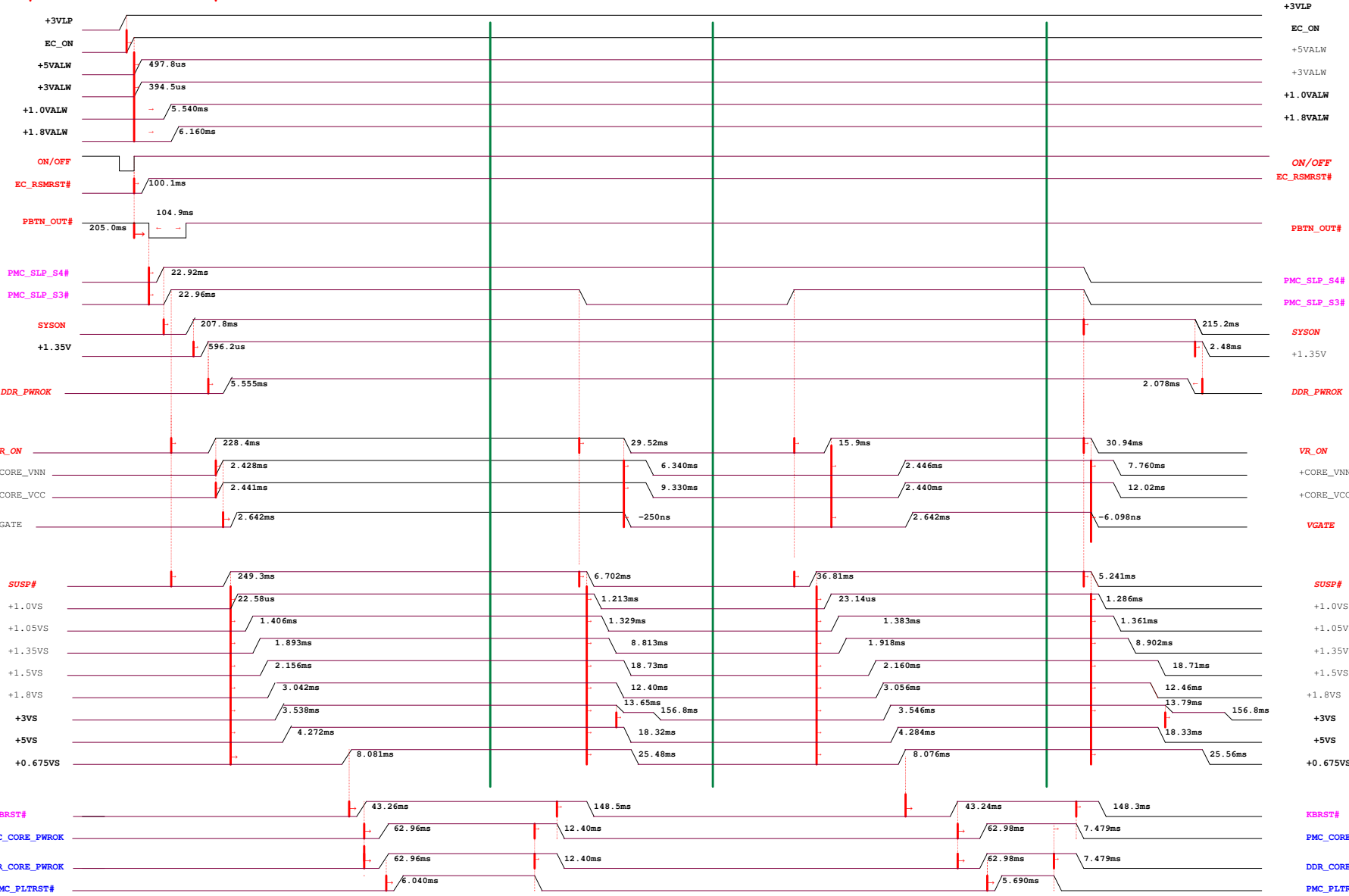
USOC1
N2815@

S IC FH8065301619509 SR1SJ B3 1.86G C38!
Part Number = SA00007EO50

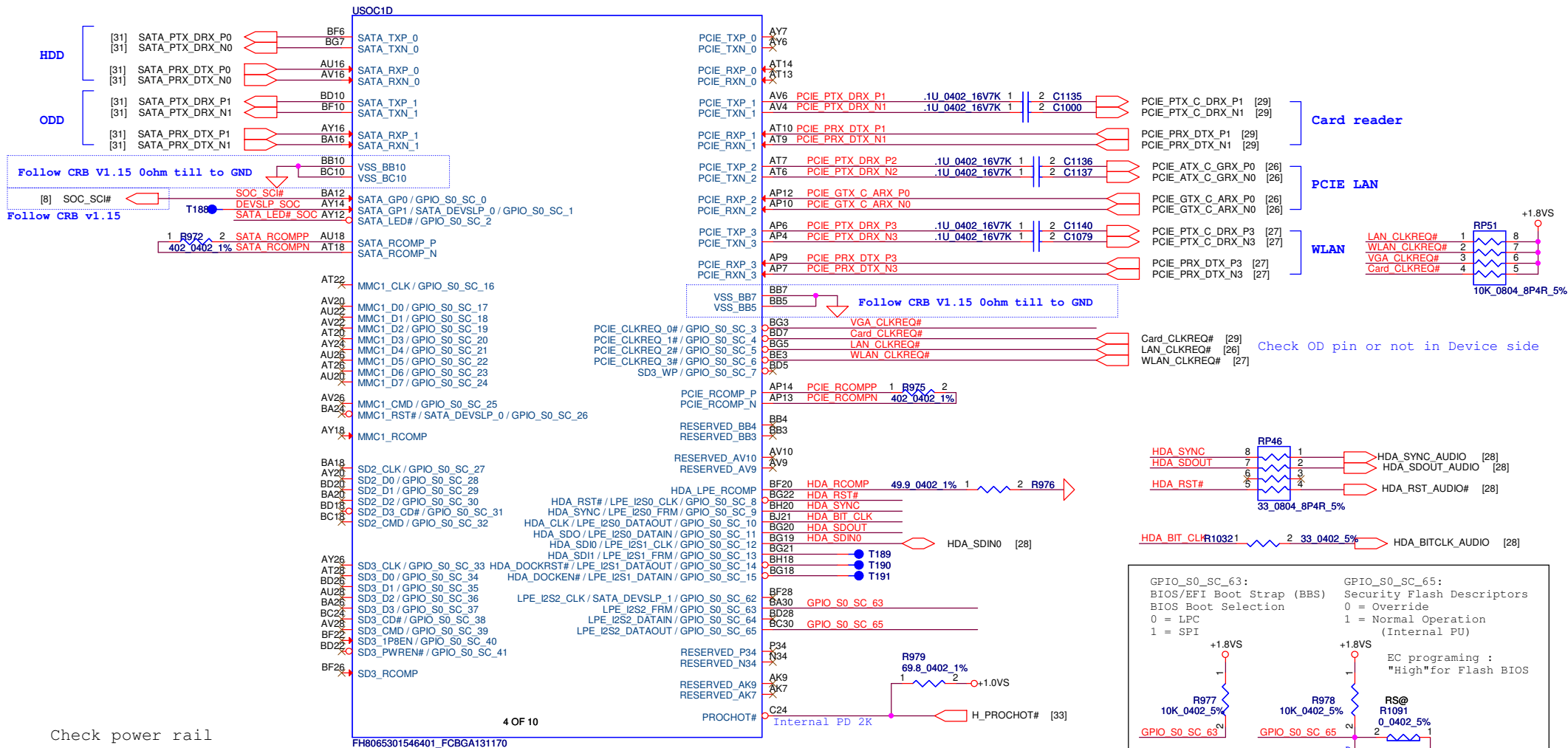
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Power On S3 S3 Resume Power Off

Plug in

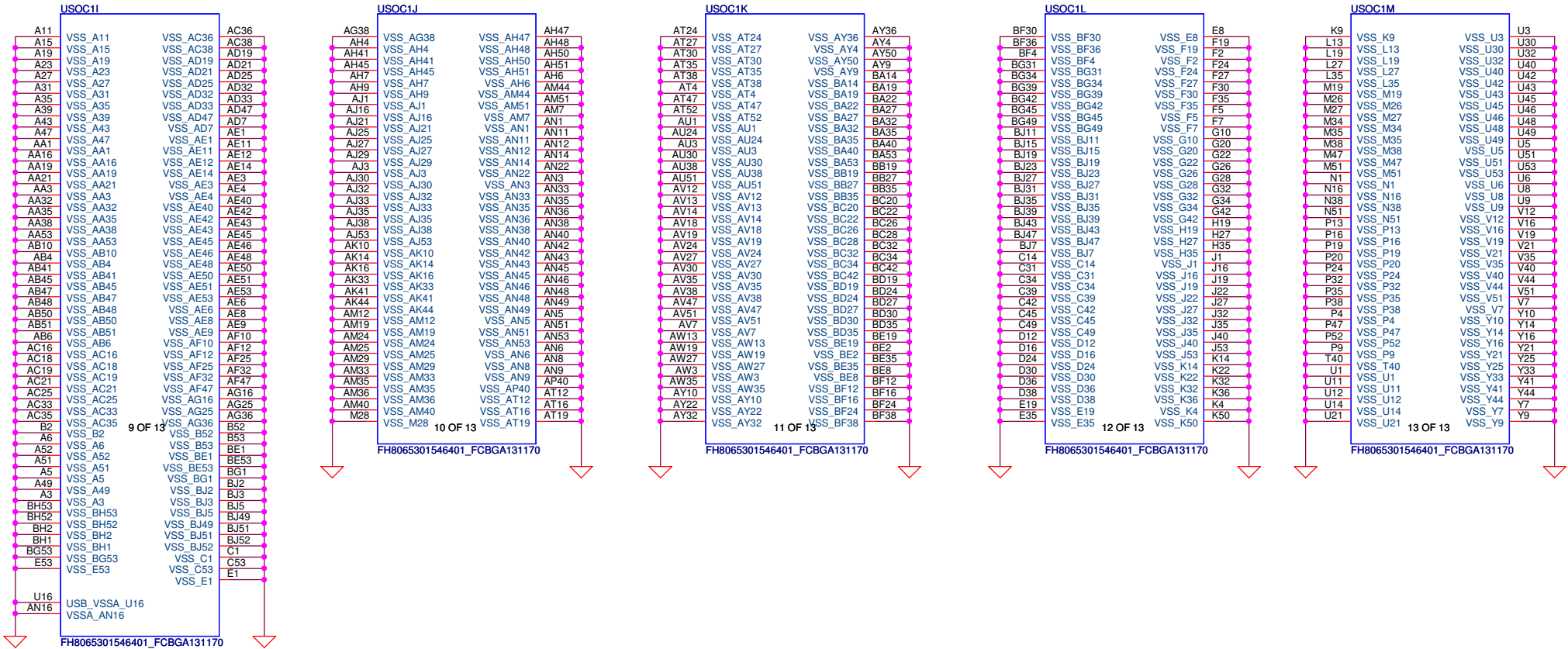


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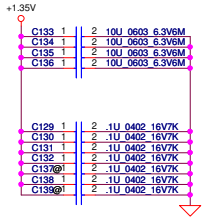
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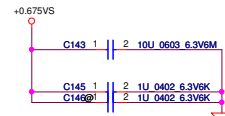


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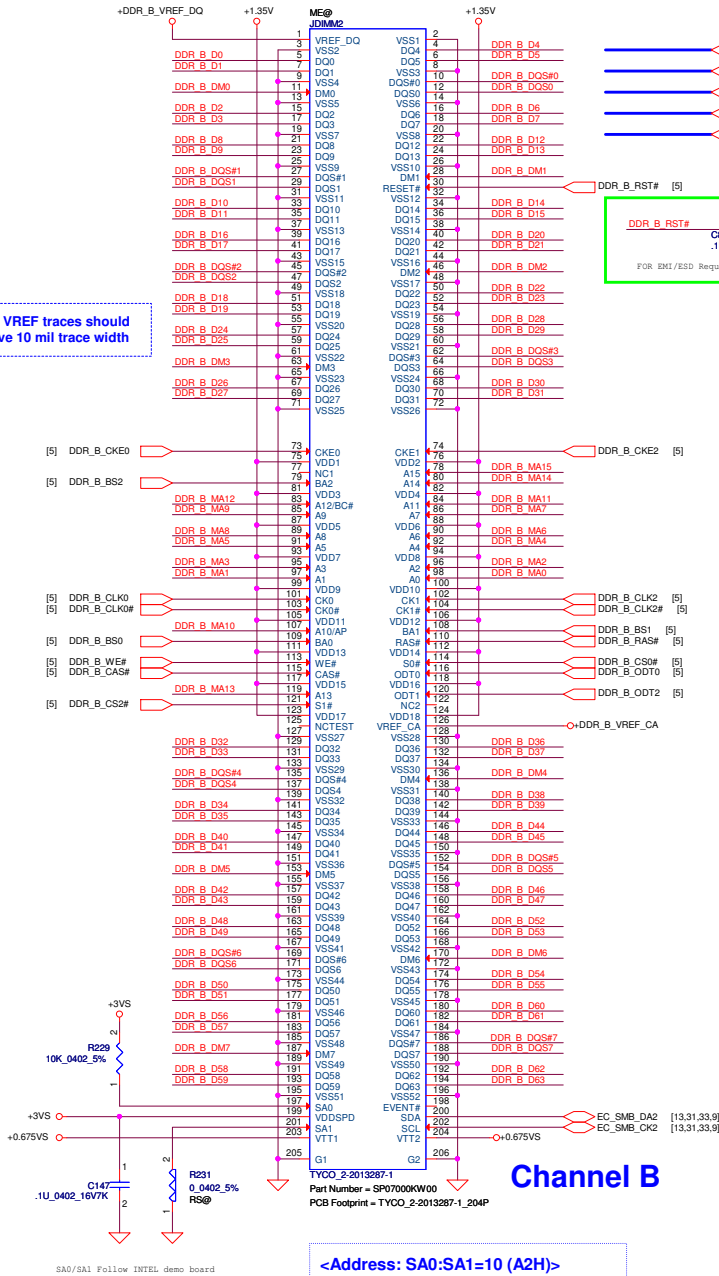
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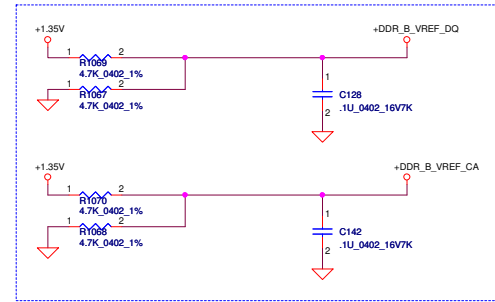
All VREF traces should
have 10 mil trace width



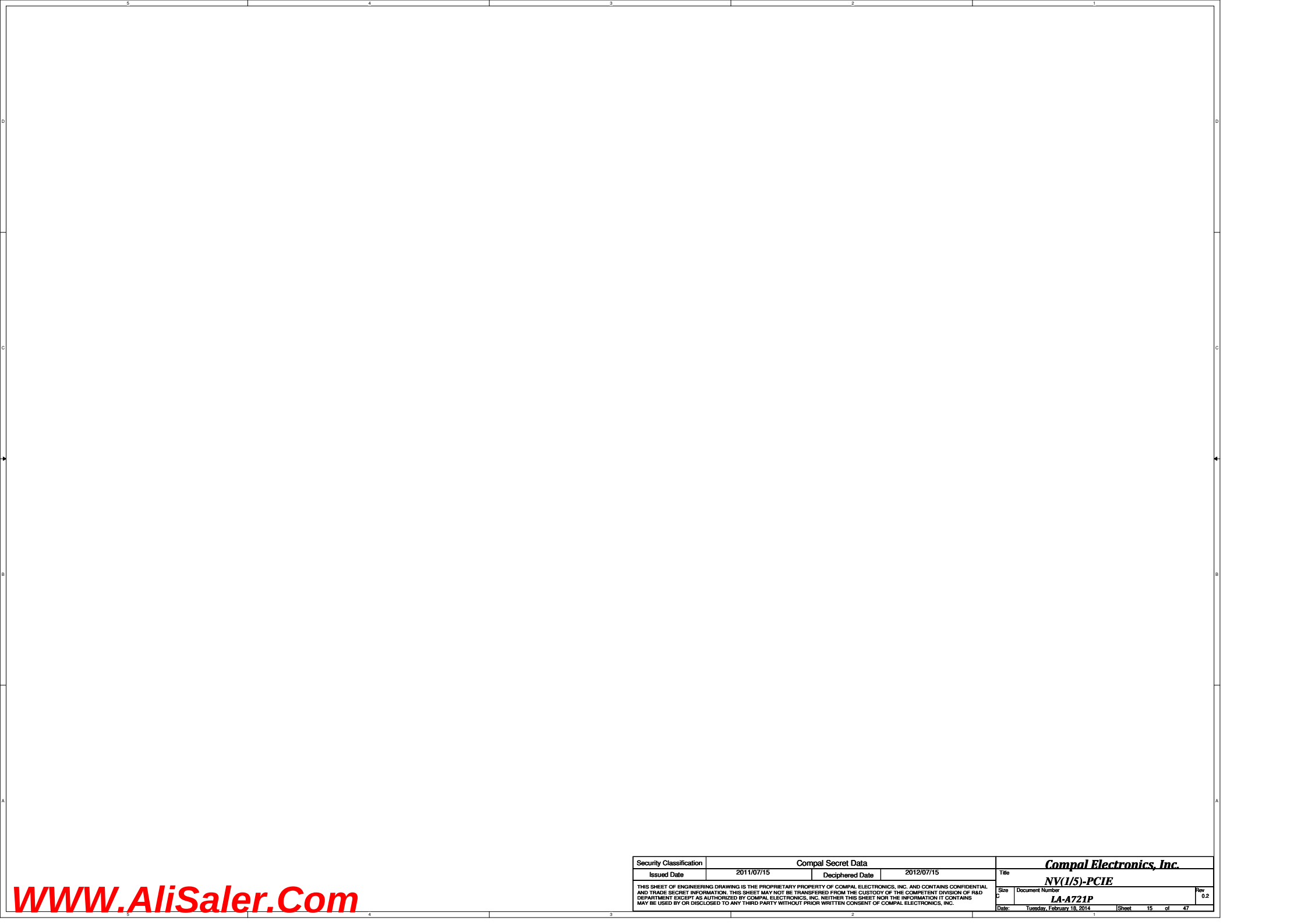
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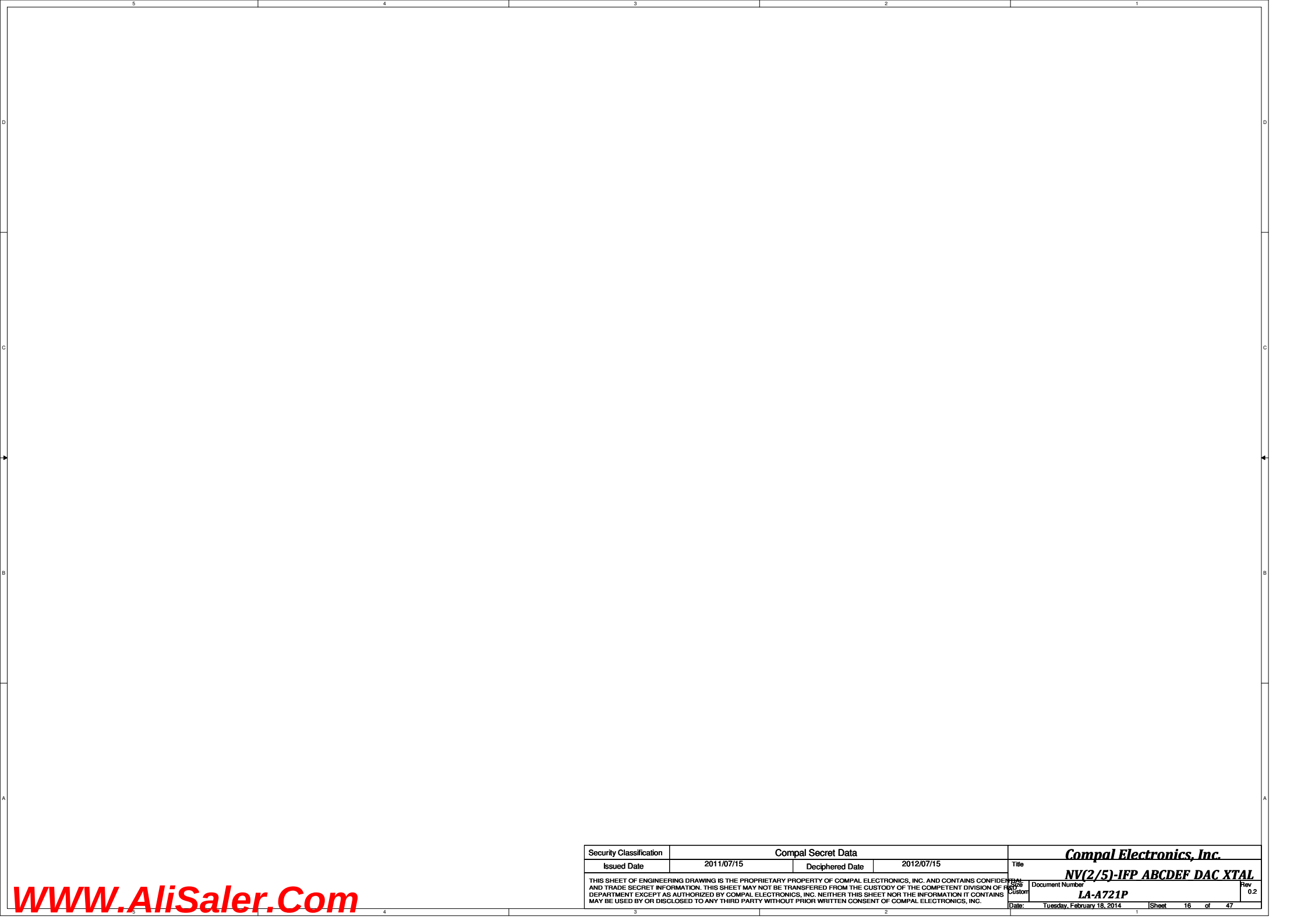
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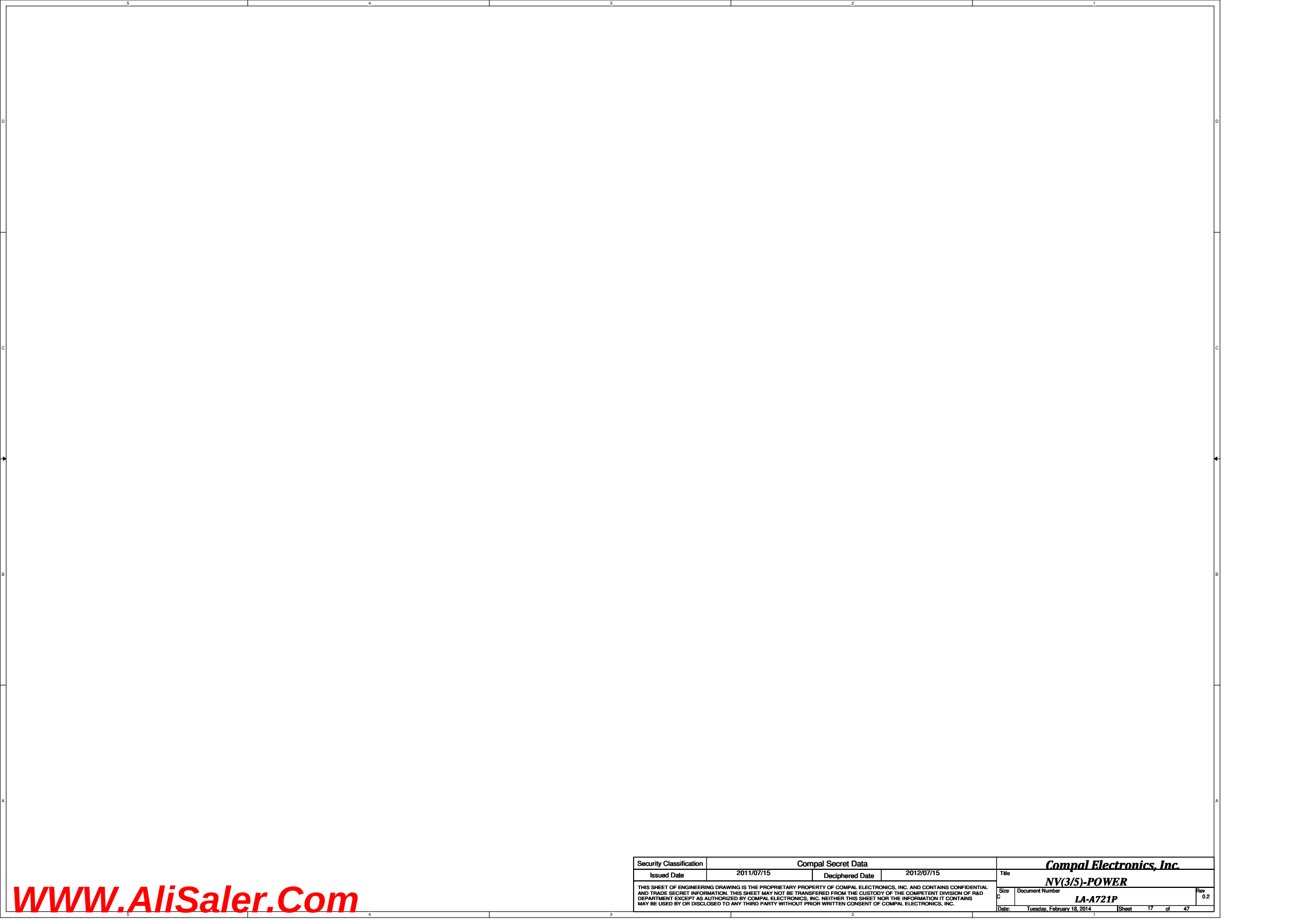
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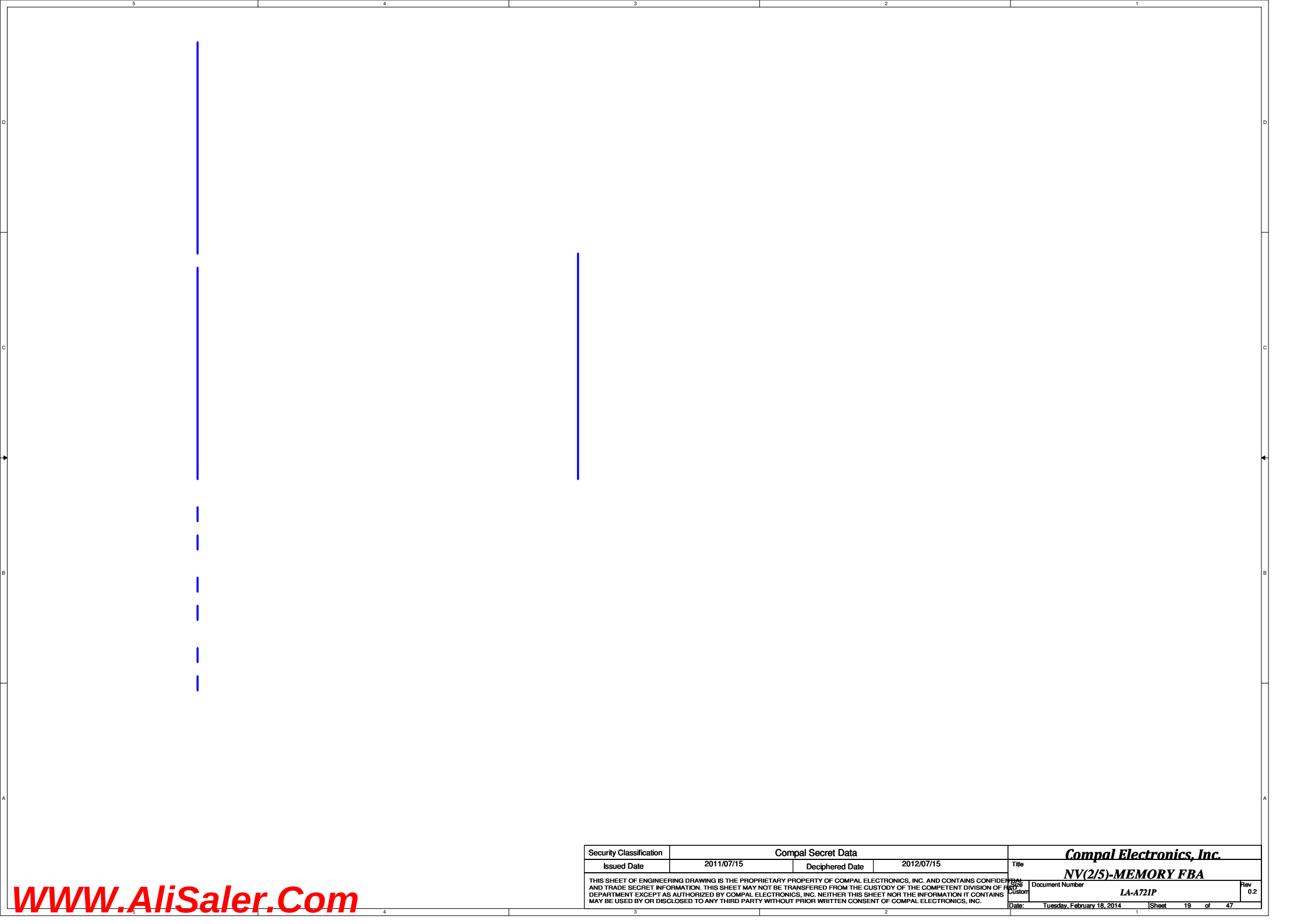


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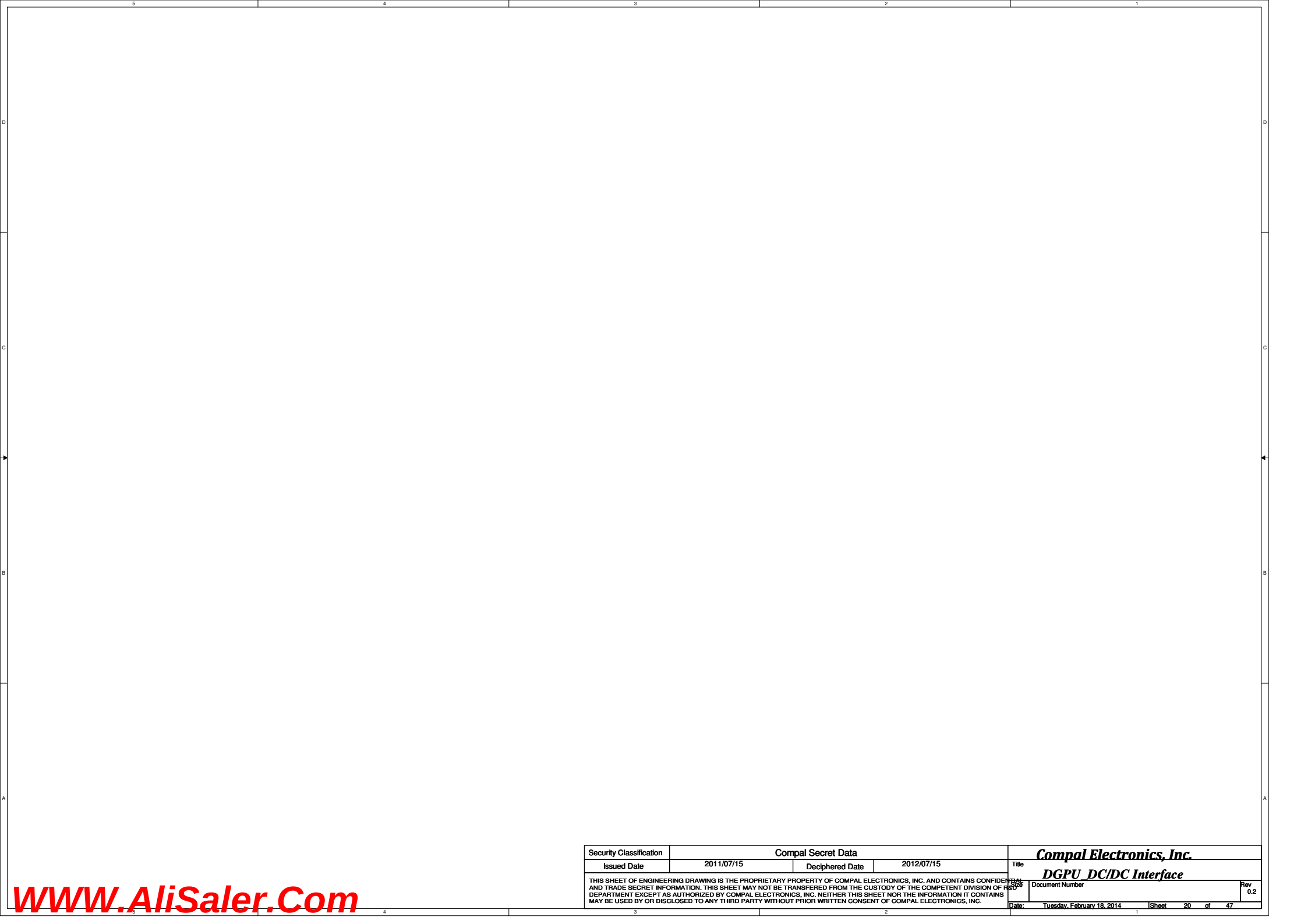


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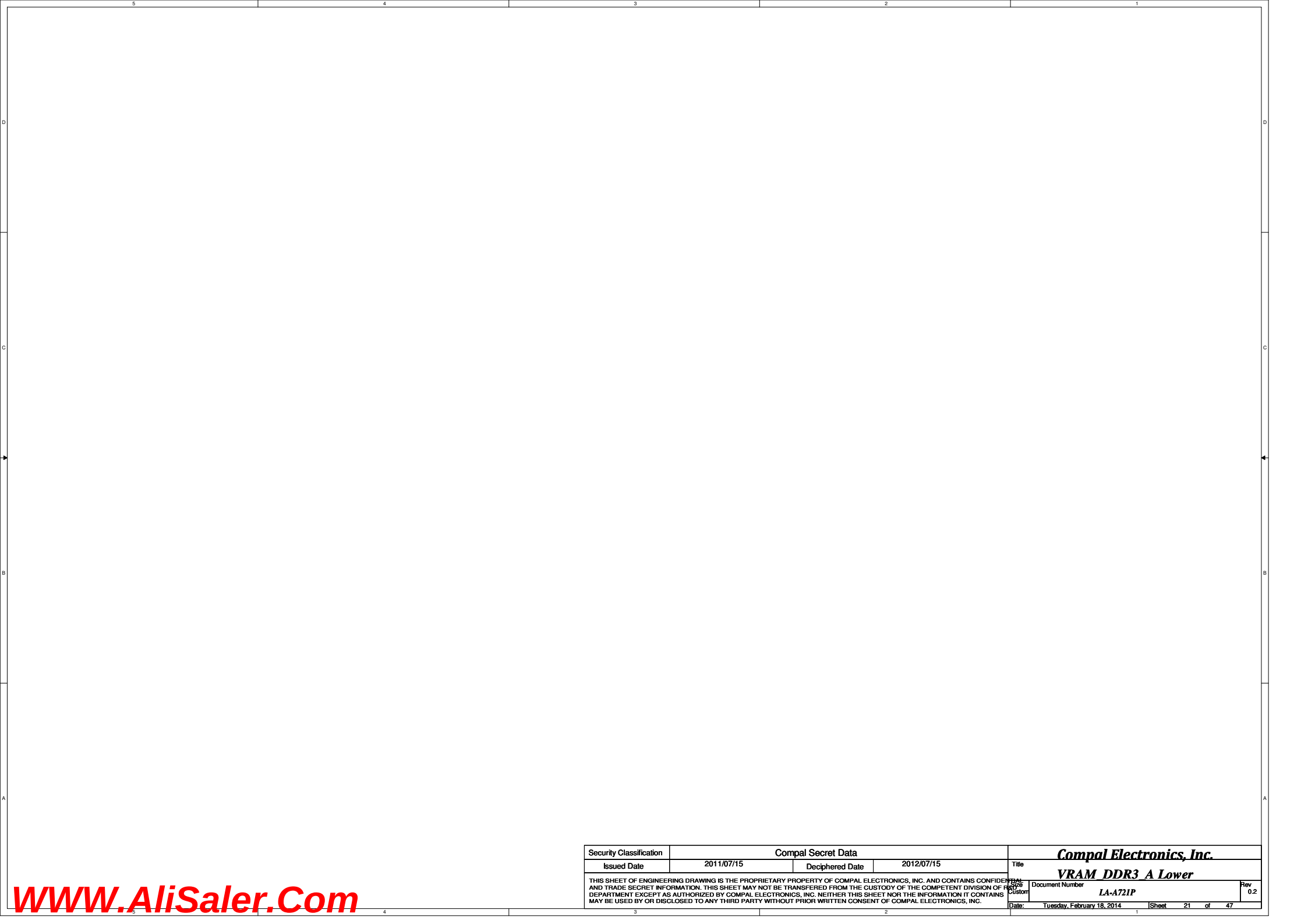
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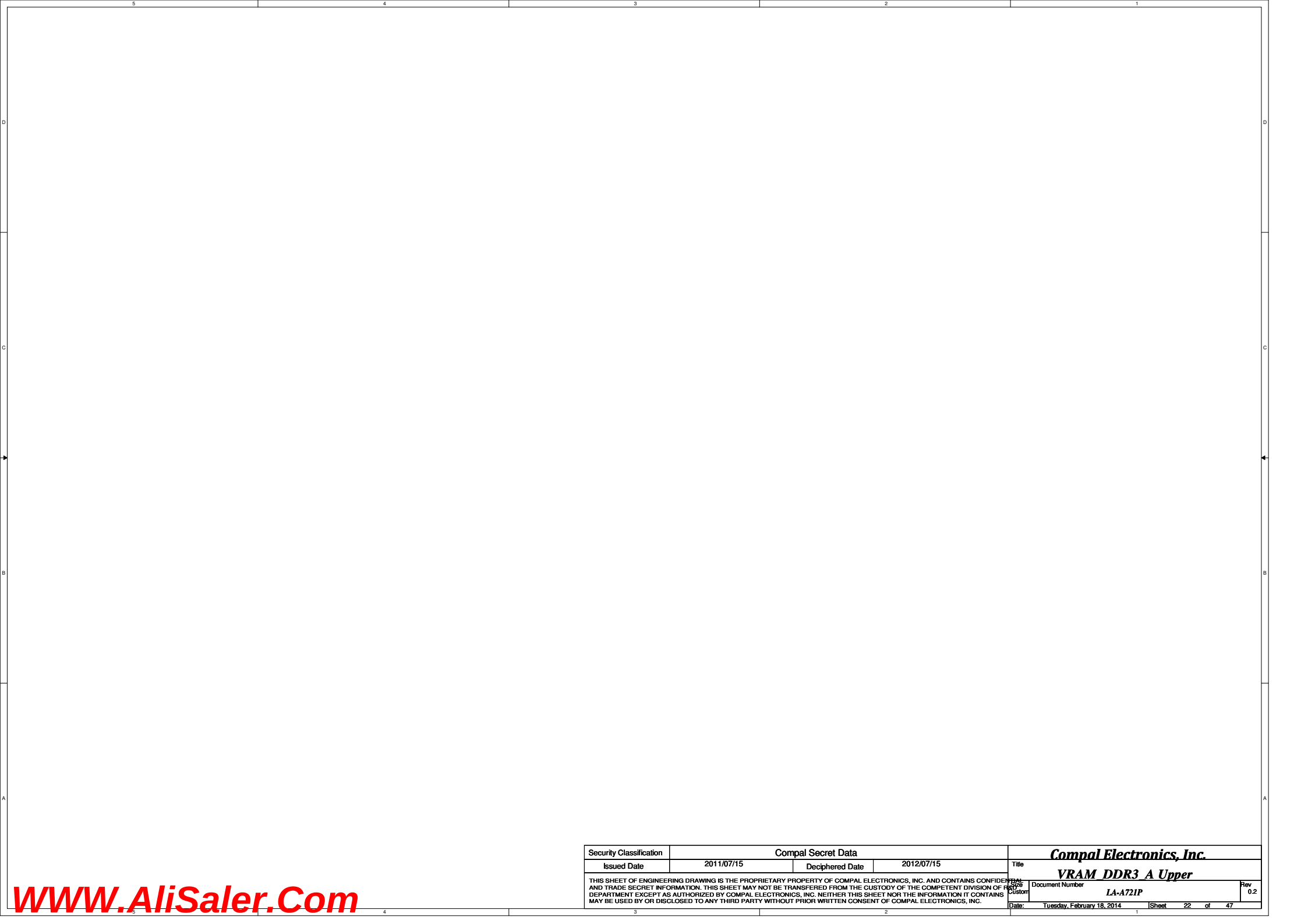
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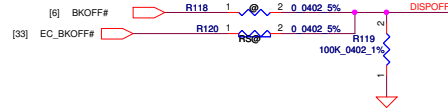
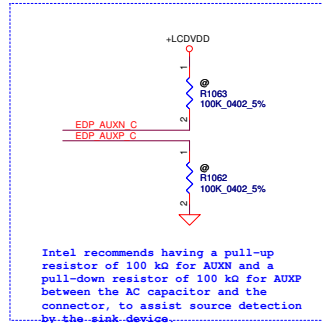
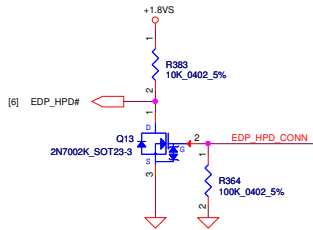
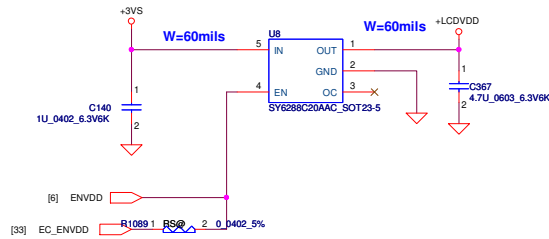


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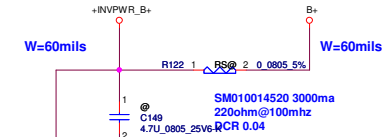


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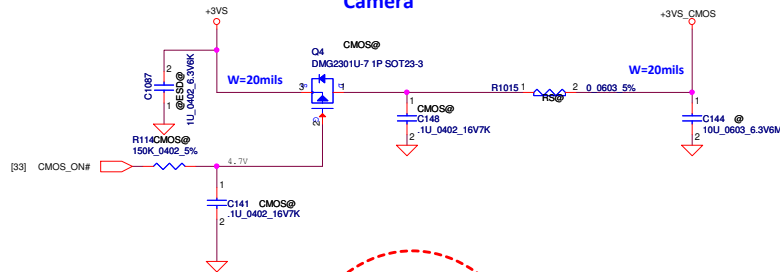
LCD POWER CIRCUIT



LCD/ LED PANEL Conn.

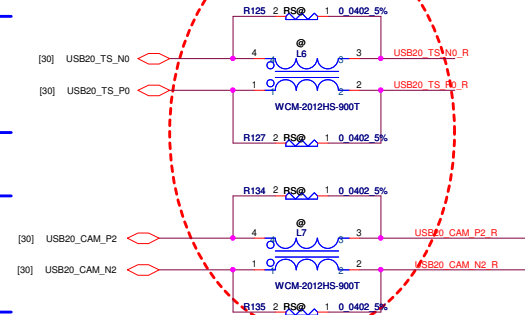


Camera



Camera

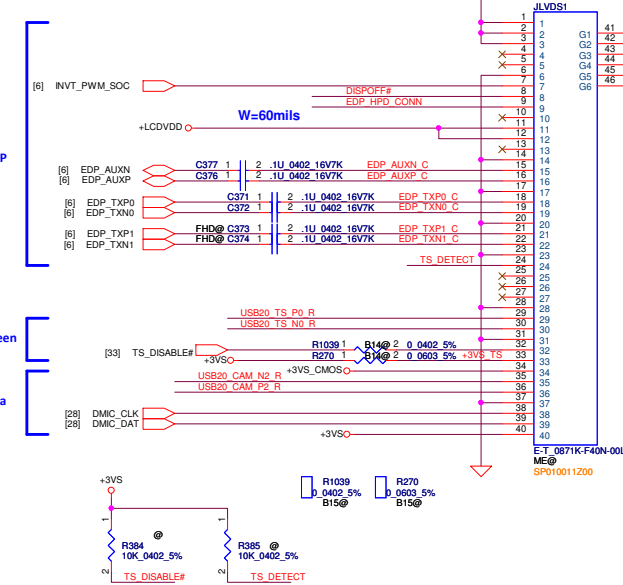
Touch Screen



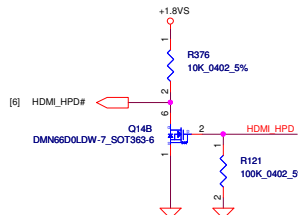
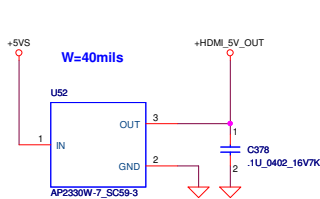
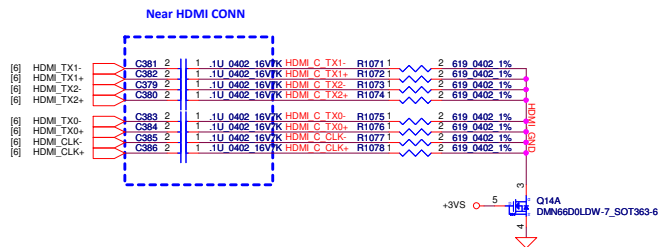
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Touch Screen

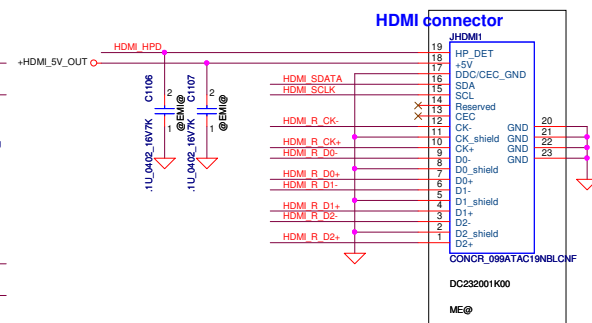
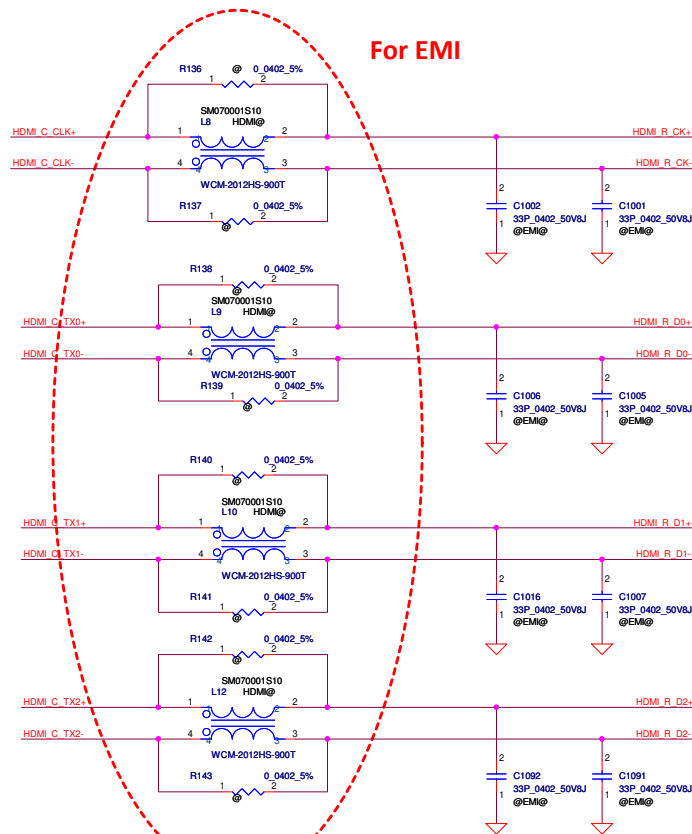
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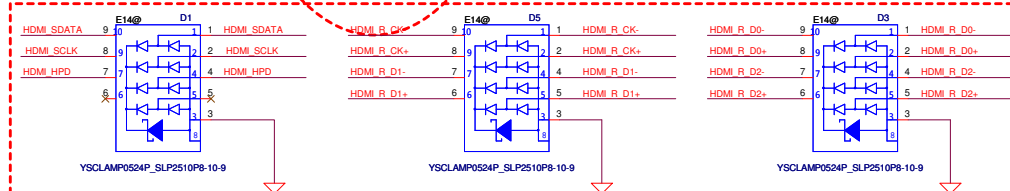
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For EMI

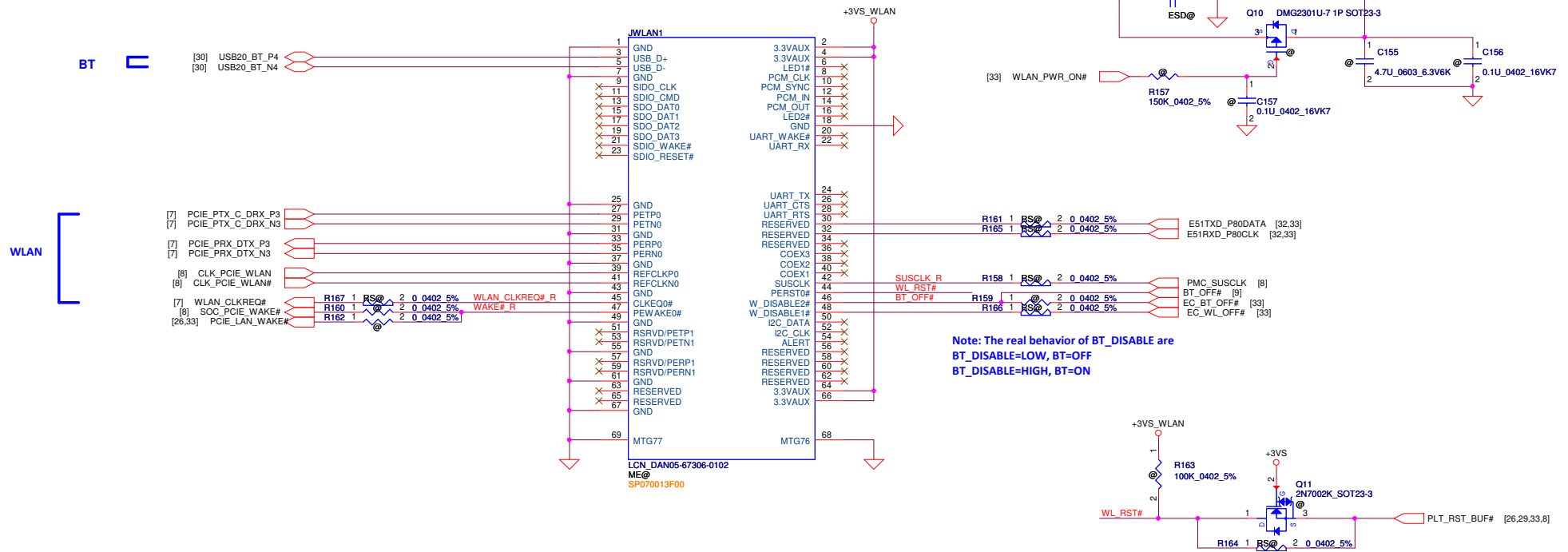


ESD

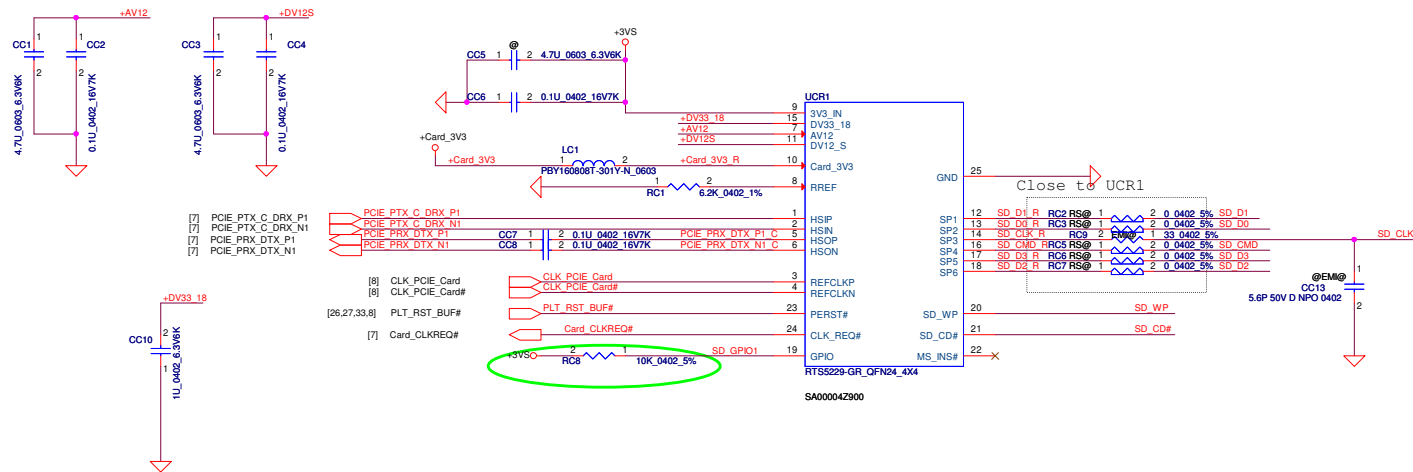


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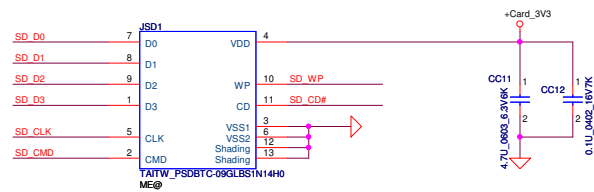
NGFF for WLAN / BT(Key E)



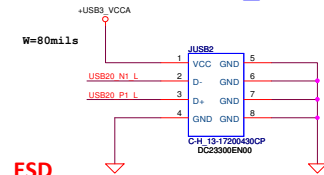
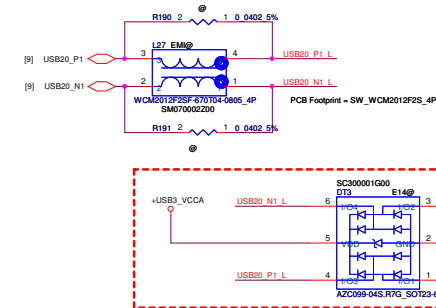
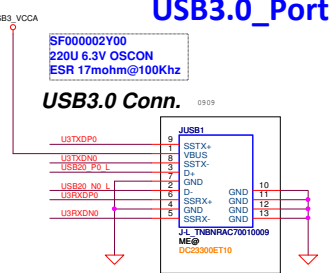
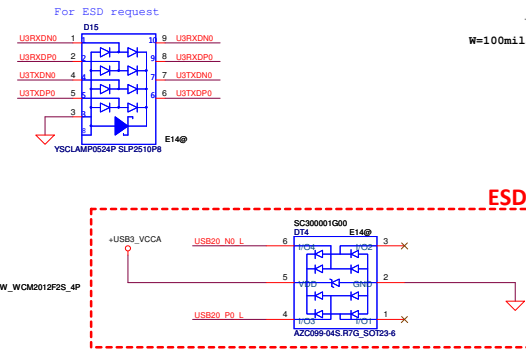
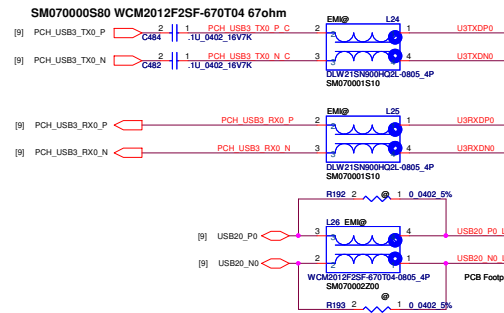
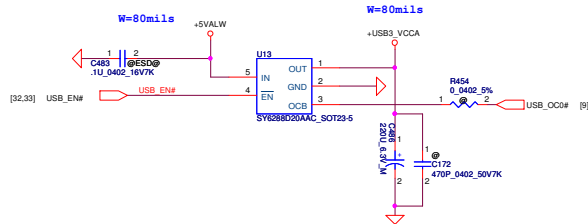
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Mini PCIE(WLAN)	
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				Intel BayTrail-M Platform	
				Date: Tuesday, February 18, 2014	Sheet 27 of 47



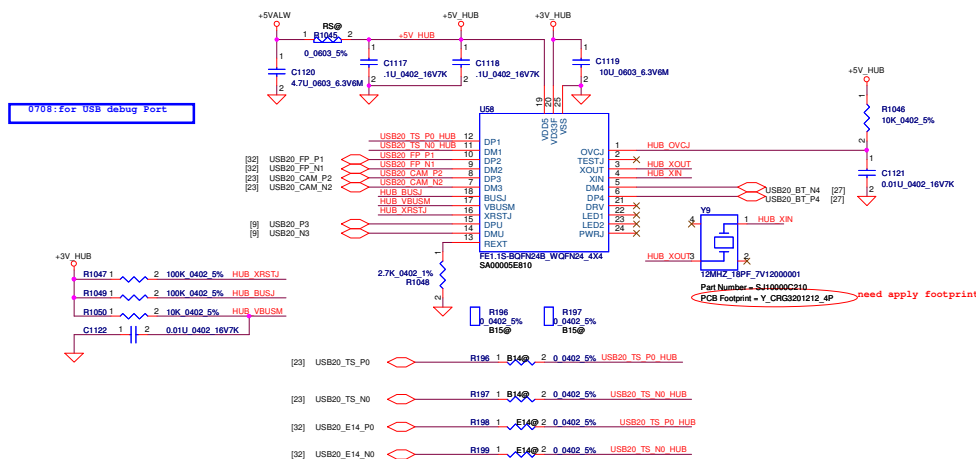
SD/SDXC



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Issued Date	2012/10/11	Deciphered Date	2014/10/11	Title
				P29-CardRead/RTS5229
				Document Number
				Rev 0.2
				Date: Tuesday, February 18, 2014
				Sheet 29 of 47

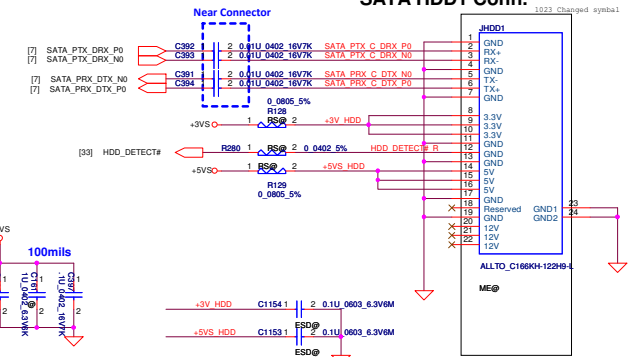


USB2.0 HUB

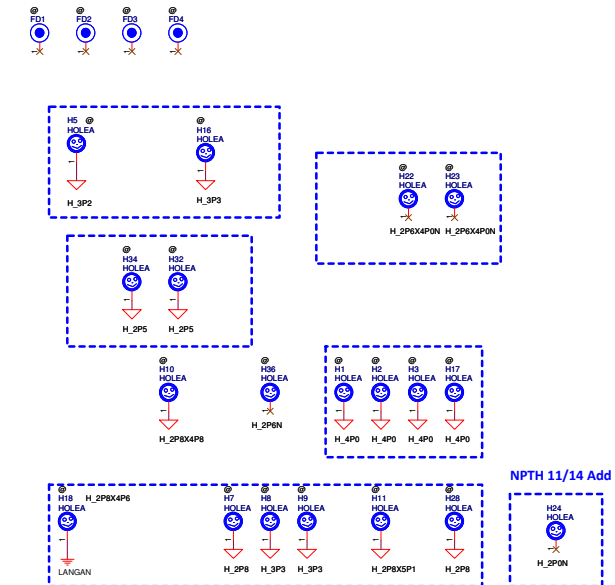
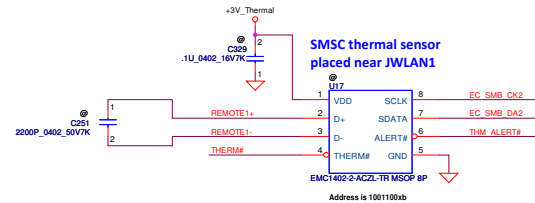
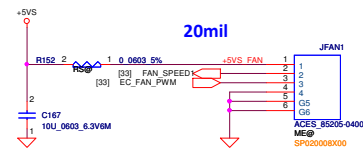
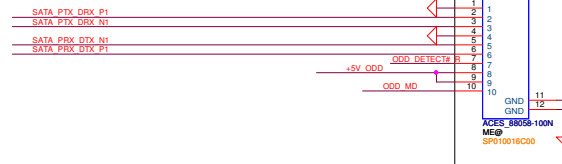


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				Document Number	0.2
				Intel BayTrail-M Platform	
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				Sheet	30 of 47

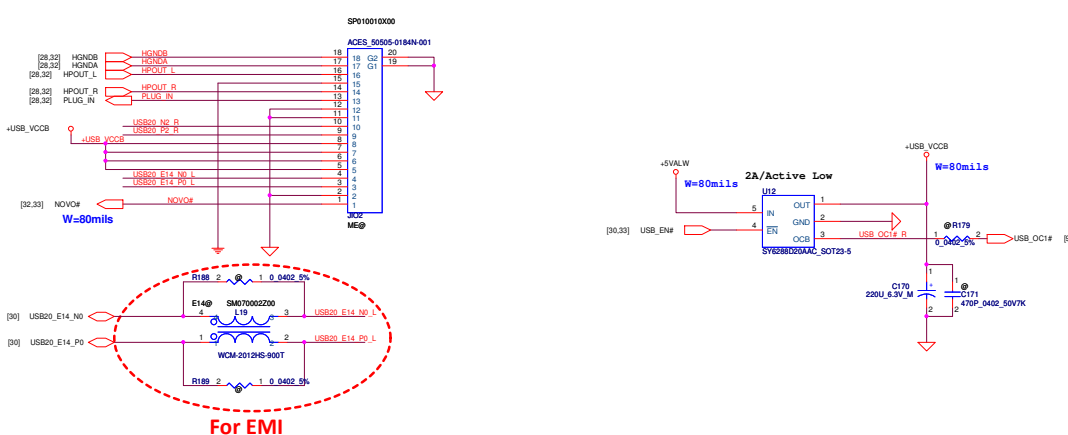
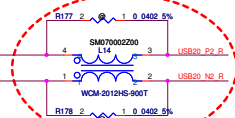
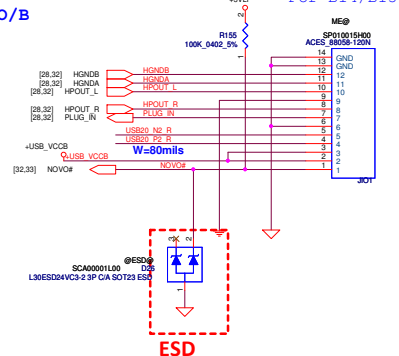
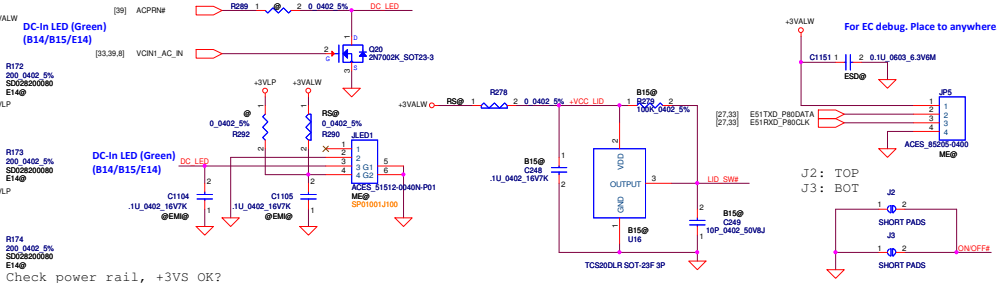
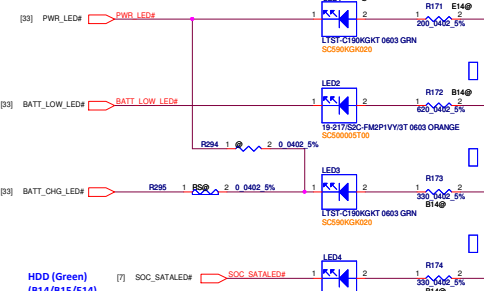
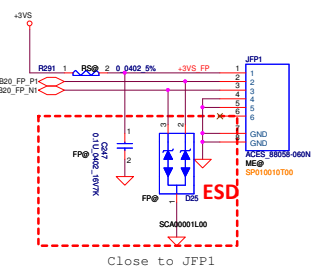
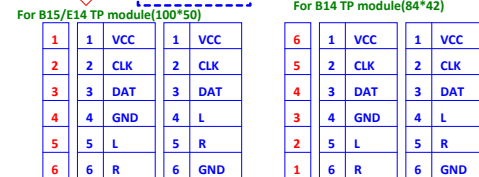
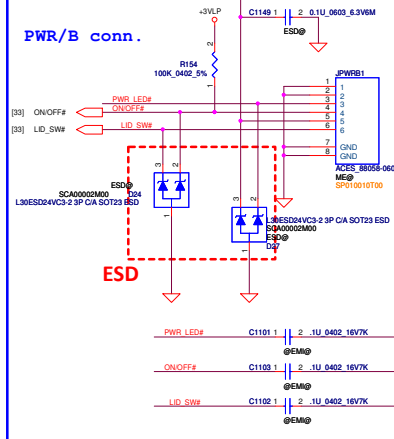
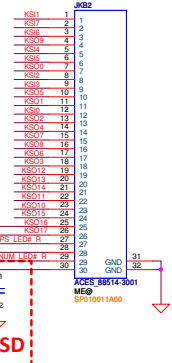
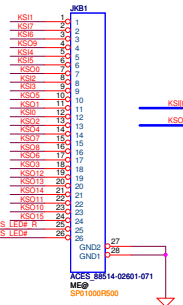
SATA HDD1 Conn.



SATA ODD Conn.

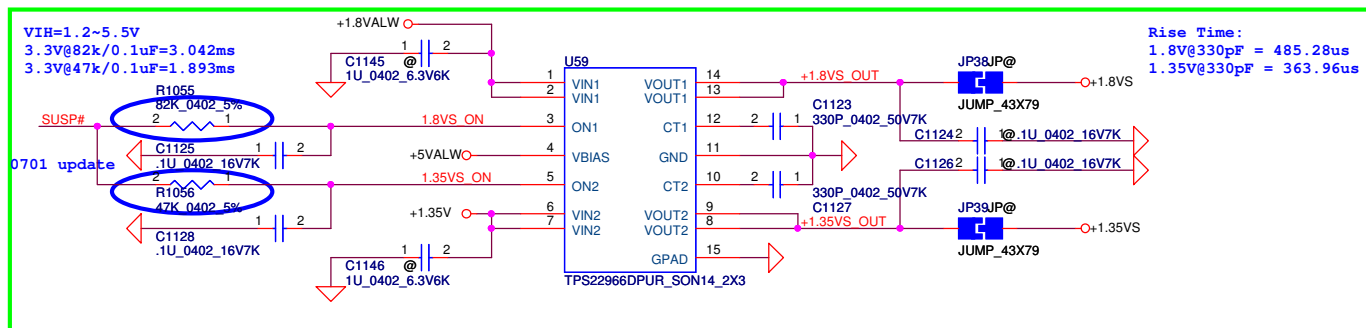
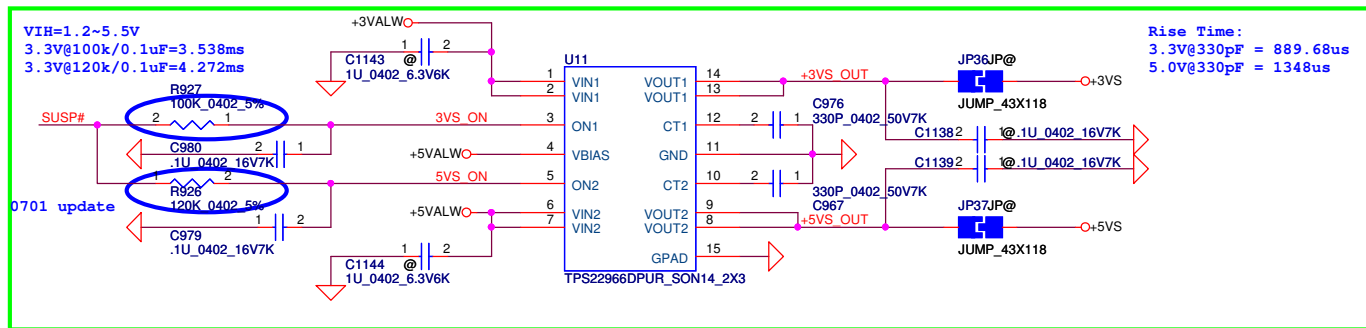


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				Customer	Intel Bay Trail M Platform		0.2
				Date	Tuesday, April 23, 2014	Time	8:47 AM

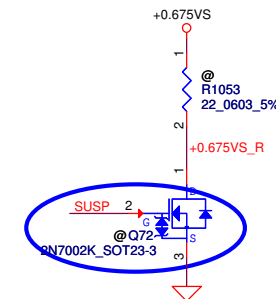
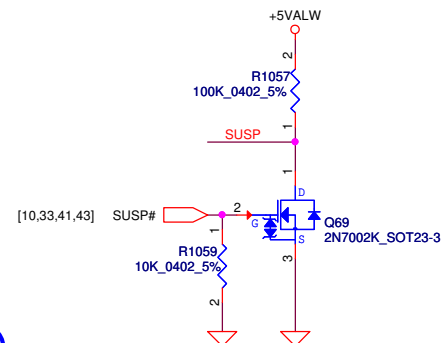
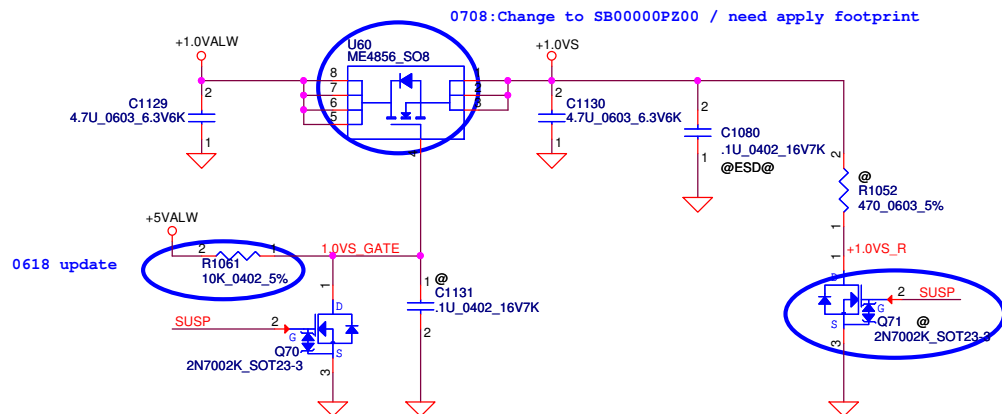


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			Int'l Bay/Trait M Platform		
			Date:	Thursday, February 20, 2014	Sheet 3 of 4





+1.0VALW TO +1.0VS



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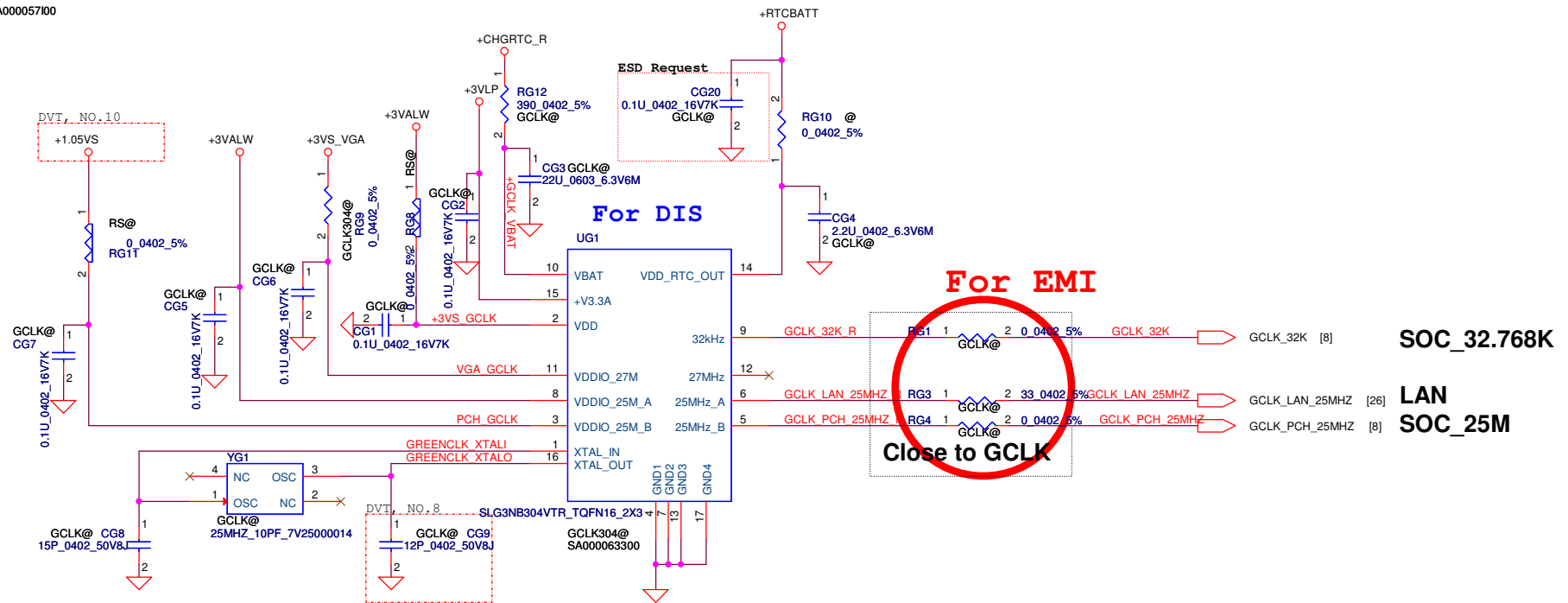
For UMA



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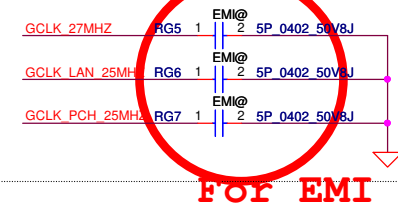
SA000057100

Every power trace need:
W=20mils



For EMI
Close to GCLK

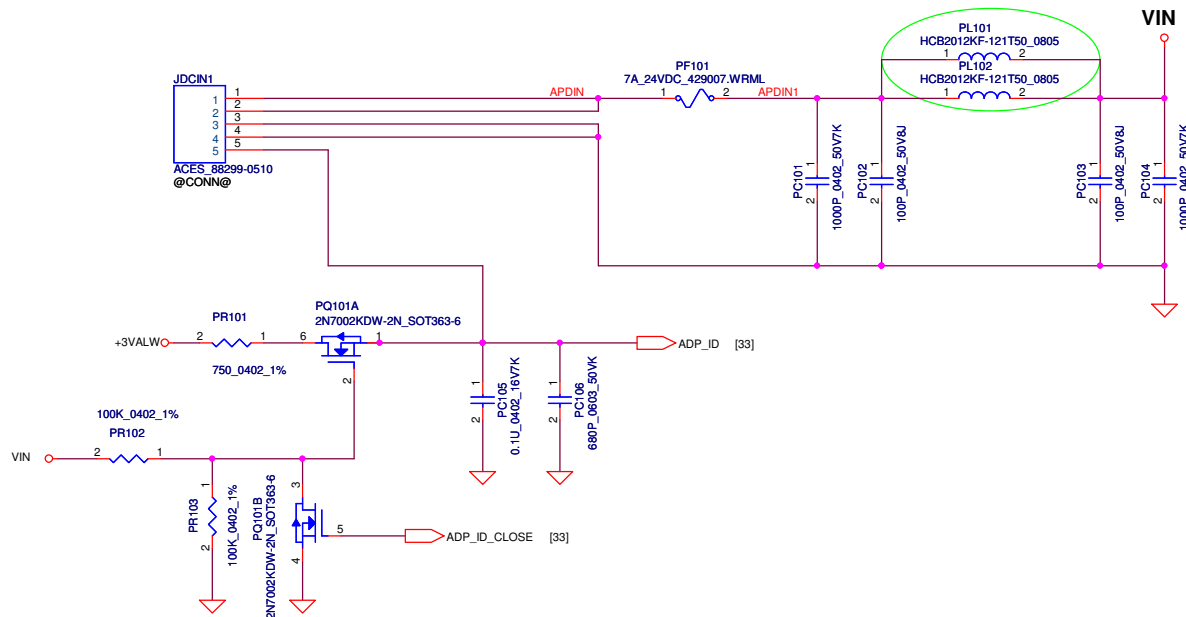
Reserved for Swing Level adjustment
(Close GCLK side)



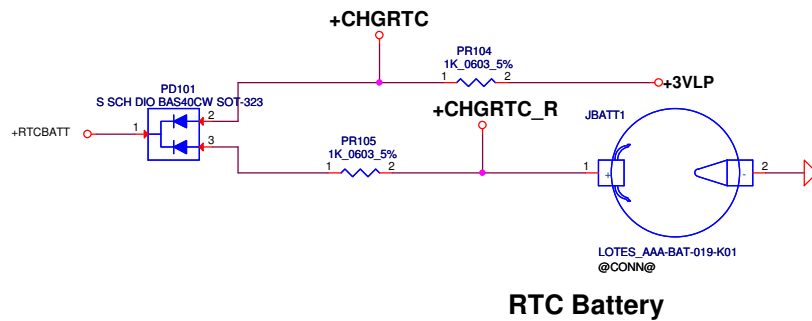
For EMI

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Issued Date	2012/10/11	Deciphered Date	2014/10/11	P35-GCLK	
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5	4	3	2	1
D				D
C				C
B				B
A				A
Security Classification Compal Secret Data Issued Date 2013/04/12 Deciphered Date 2014/04/12 THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. Size B Document Number Rev 0.2 Compal Electronics, Inc. HW RIR Intel BayTrail-M Platform Date: Tuesday, February 18, 2014 Sheet 36 of 47				

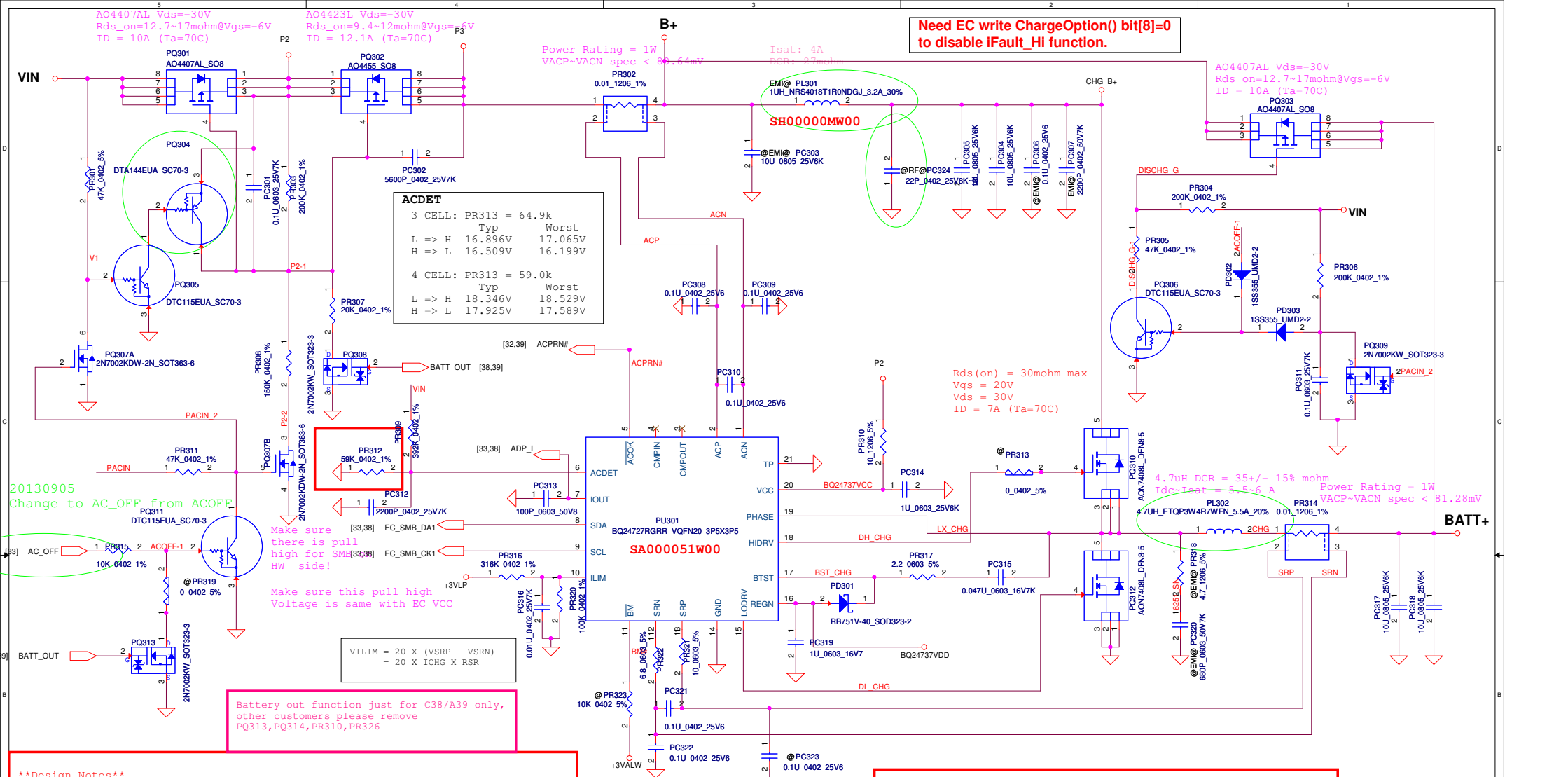


20131023
Change PL101 to SM01000C000*2 from SM010008E10



RTC Battery

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****Design Notes****
Maximum Charging current 2.0A
Battery discharge power 55W.
#Register Setting
1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
3. 0X12 bit[12:11] set 00 (default 11) to set BAT Depletion Comparator Threshold
Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell)
4. Disable turbo when AC only
#Circuit Design
1. Make sure there is pull high for SMB on HW side
2. Use 10X10 choke and 3X3 H/L side MOSFET
Charge current 2.0A
Power loss : 1.82W
Power density : 0.81 (15X15)
3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)
4. For hybrid design, need double check PQ301, PQ302, PQ303, PQ309 component rating
#Protect function
1. ACOVP : ACDET voltage > 3.15V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting(default)
4. CHGOCV : 3/4.5/6A based on current setting
5. BATOV : 104%
6. BATLOW : 2.5V

WWW.AliSaler.Com

Module model information
BQ24737_V1.mdd for dual layer

20131028

1. Change PQ314 to SB000009Q80 2N7002 from BJT SB301150200

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				Date	Rev
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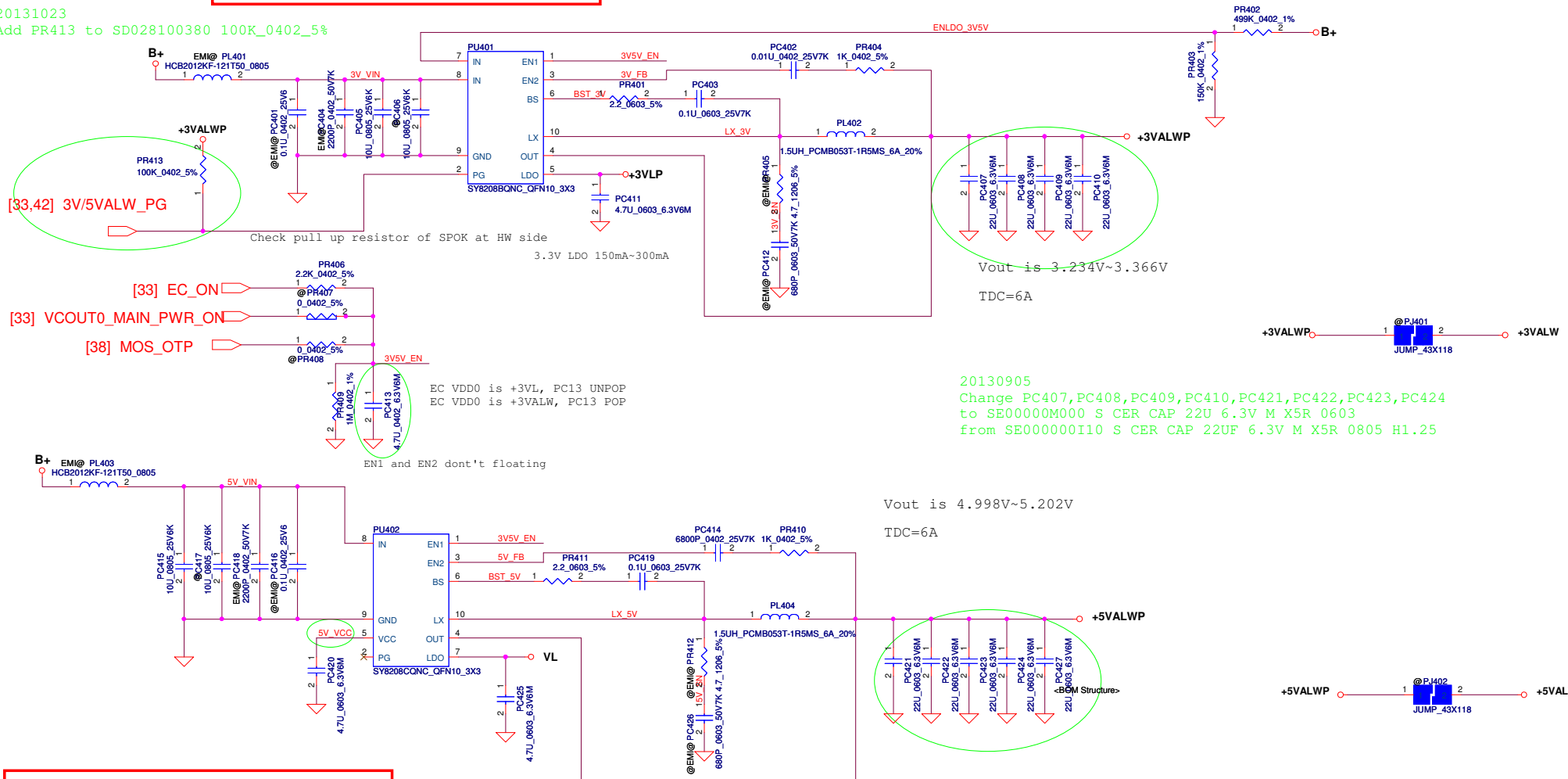
Module model information

SY8208B_V2.mdd

EN1 and EN2 don't floating

20130905
Change to 3V/5VALW_PG from SPOK

20131023
Add PR413 to SD028100380 100K_0402_5%



Module model information

SY8208C_V2.mdd

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				Tuesday, February 18, 2014	0.1
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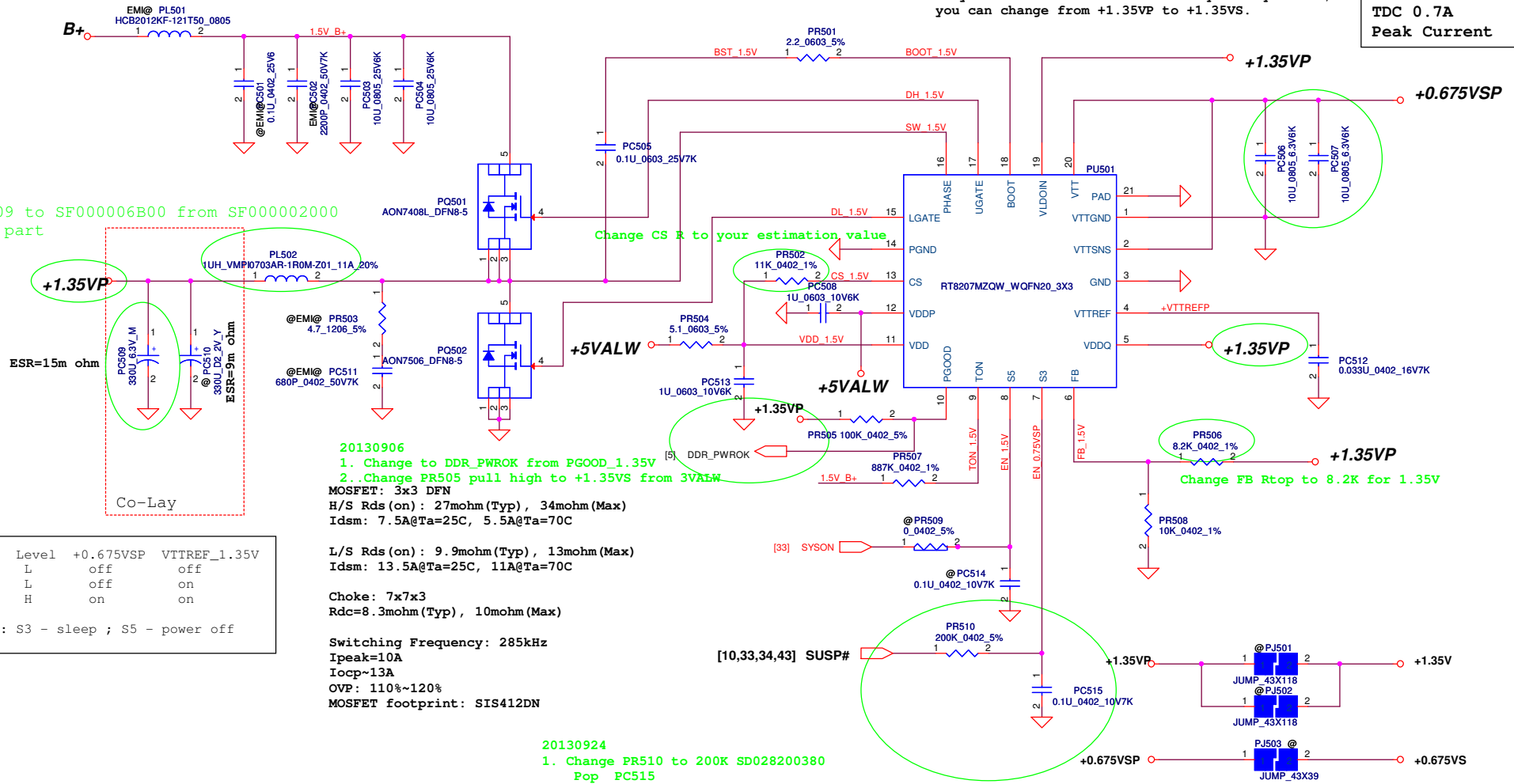
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

20131023
Change PC509 to SF000006B00 from SF000002000
for common part

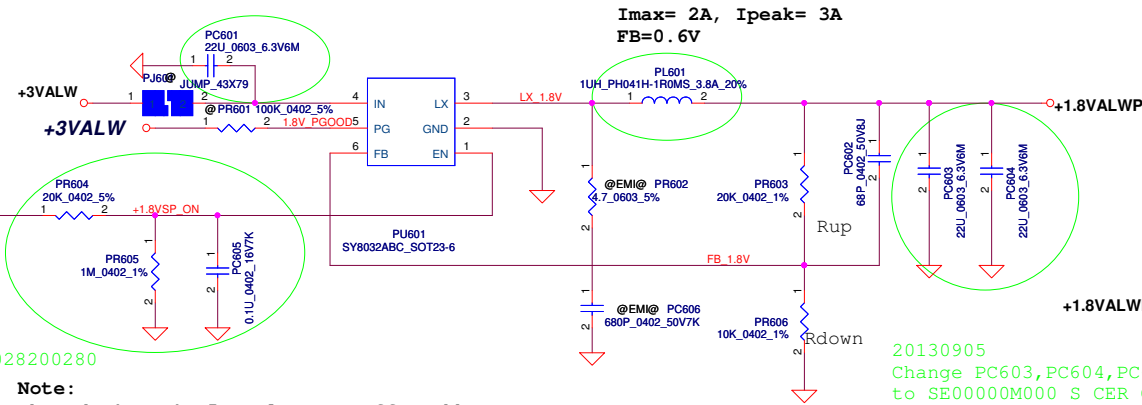


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					Size	Document Number	Rev
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Module model information

SY8032_V1.mdd

20130913
Need to change PC702 to 0603 from 0805



20130905
Change to 3V/5VALW_PG from SPOK

20130924
Change PR604 to 20K SD028200280
Pop PC605 to 0.1u

20130905
Change PC603, PC604, PC617, PC618 to SE00000M000 S CER CAP 22U 6.3V M X5R 0603 from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

$V_{out}=0.6V * (1+R_{up}/R_{down})$

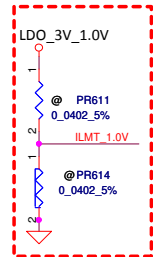
20130924
1. Change PR607 to 10K SD028100280
Pop PC607 to 0.1U_0402_16V7K SE076104K80

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

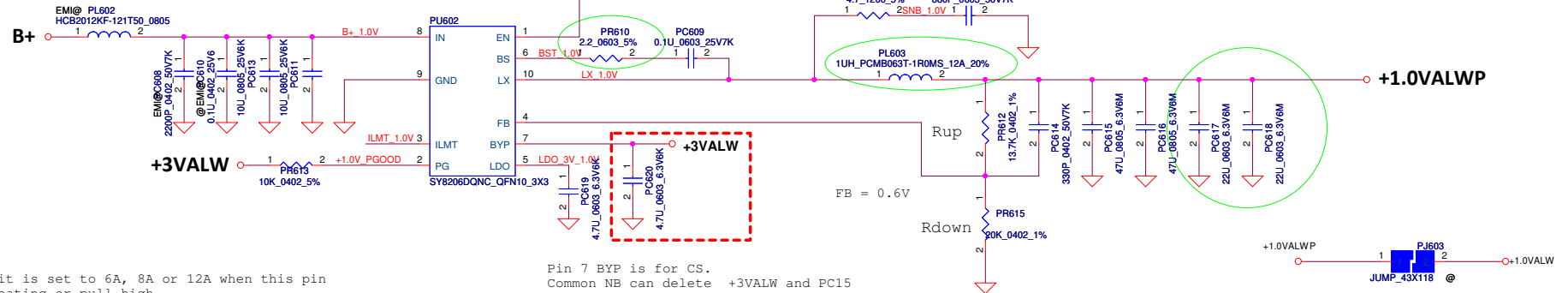
20130905
Change to 3V/5VALW_PG from SPOK

SY8206D_V1.mdd

Module model information



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high



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						PWR-1.8VALW/1.0VALW			
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Module model information

20130913
Need to change PC702 to 0603 from 0805

Imax= 2A, Ipeak= 3A
FB=0.6V

DIS:SY8003
UMA:SY8032

20130924
Change PR701 to 2.55k 1% SD034255180
Pop PC703 to 0.1u
unpop PR710

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out}=0.6V \cdot (1+R_{up}/R_{down})$$

20130905
Change PR702 to 75K SD034750280
PR705 to 100K SD034100380

20130905
Change PC701,PC703,PC704,PC711
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

change input cap from 0805 to 0603

2013/5/13
Change PR714 from 100kto 47k
Change PR720 from 47kto 100k

VFB=0.6V
Vout=0.6V * (1+Rup/Rdown)
Vout=1.011V

Ultra Low Dropout 0.23V(typical) at 3A Output Current

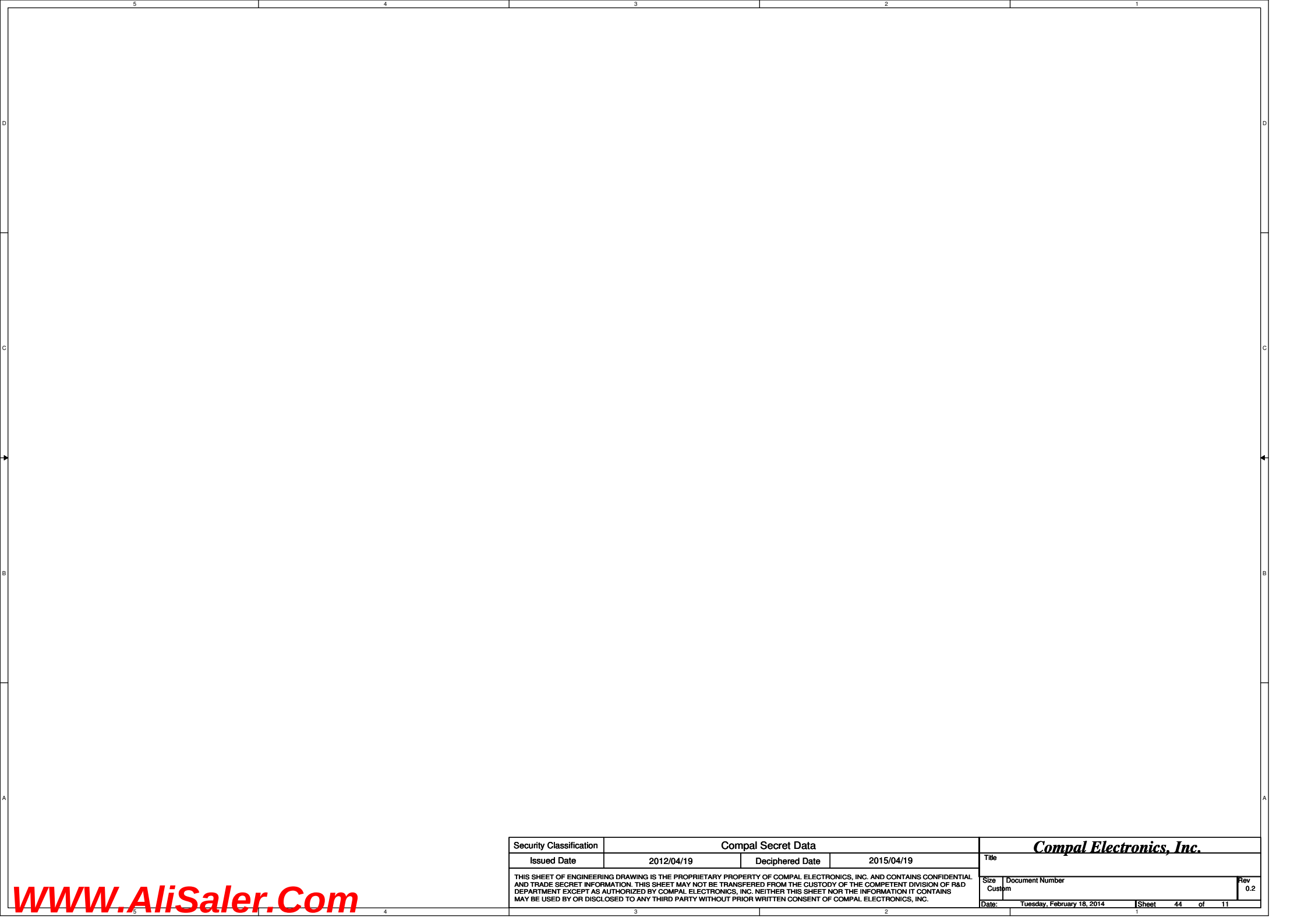
2013/5/13
Change PR716 from 47kto 100k

20130924
Change PR706 to 51K SD028510280
Pop PC710 0.15U_0402_10V6K SE00000H300
unpop PR708

$$V_{out}=0.8V \cdot (1+R_{up}/R_{down})$$

$$V_{out}=1.512V$$

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Power module of ISL95833 VR
for 4.5W processor

PR15 and PR27
27.4K ohm for 100 degree
61.9K ohm for 110 degree

Alert assert
threshold: 100C

Close GFX choke

Close GFX L/S MOS

+3VALW

+5VALW

VR_Hot# assert
threshold: 100C

Close CPU L/S MOS

Close CPU choke

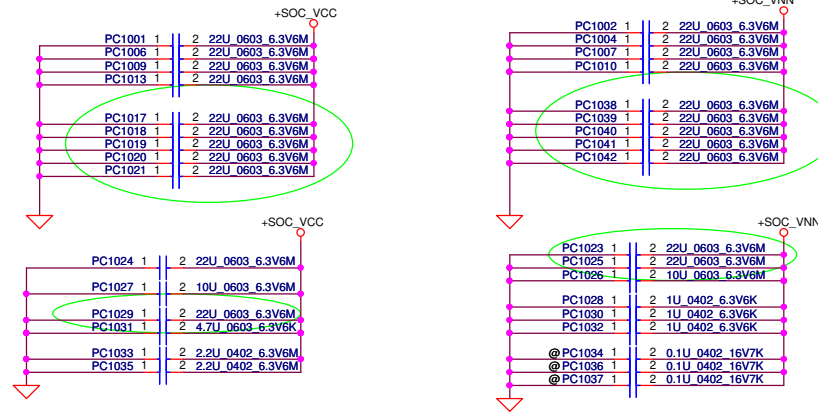
SOC_VNN OCP is around 21A
SOC_VCC OCP is around 19A

20130905
1. Del PC940 33U_25V_M
2. Change PC939 to 68U_25V_M R0.36 SF000000W00
From 33U_25V_M SF000005200

0.22uH DCR= 0.97+-5% m ohm, Idc-Isat= 25-34A

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22uF 0805 size change to 0603



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Date:				Sheet 46	of 49

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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