PROJECT S6F

Revision History

R1.0	SR	2005/07/01
R1.1	ER	2005/11/25
R2.0	PR	2005/01/18

SMB Signals

Host	Name	Devices	Address
Chipset	SMBCK,SMBDA	ICH7-M ADT7460(Thermal) ICS954213(Clock Genertor) DDR2 SO-DIMM	0001 000X b 0101 110X b D2h A0h

Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+*VALWAYS	+*V	+*VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

CPU
PM667 LV 1.5 GHz: 01G011010110
PM667 LV 1.66 GHz: 01G011010010

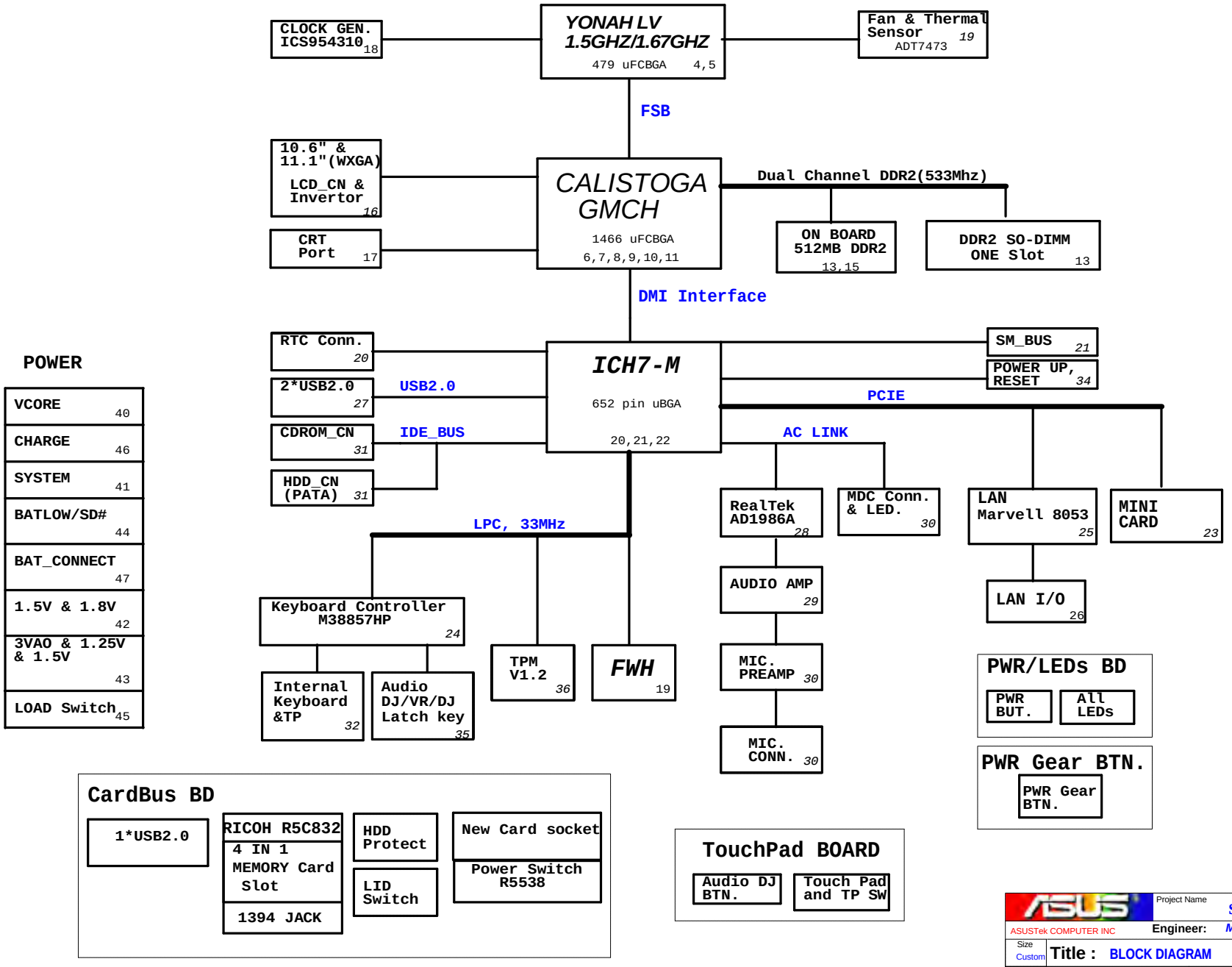
Chipset
02G010009210   C.S QG82945GM SL8Z2   INTEL CALISTOGA 876956
02G010007741   C.S NH82801GBM SL8YB   INTEL ICH7-M 876595

Memory
Infineon: 03G15073B010
Nanya: 03G15133E110

ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : Table of Contens	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 1 of 37	

YONAH/CALISTOGA(945GM) BLOCK DIAGRAM (NAPA PLATFORM)

2005.6.13 V1.0



ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : BLOCK DIAGRAM	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 2 of 37	

M38857MB_GPIO	Use As	Signal Name
P20	GPO	ANKEY_RSM
P21	GPIO	BAT_SEL#
P22	GPO	BAT_LEARN
P23	GPO	TBD
P27	GPO	SCROLLOCK#_3
P42	GPO	TP_LED
P43	GPO	TBD
P44	GPO	KBDCPURST_3Q
P45	GPO	A20GATE_3Q
P46	GPO	KBDSCI_3Q
P47	GPIO	CLKRUN#_3
P50	GPI	BAT_LLOW#_OC
P51	GPI	TBD
P52	GPI	TBD
P53	GPI	TBD
P54	GPI	LID_SW#
P55	GPI	BATIN_OC#
P56	GPO	TBD
P57	GPO	ADJ_BL
P67	GPI	TBD
P66	GPI	PWRLMT#
P65	GPI	BAT_SAVING#
P64	GPI	ACIN_OC
P63	GPO	CPPE_EN
P62	GPO	RST#NEWCARD
P61	GPI	CPPE#DET
P60	GPO	PP_TPM
P77	GPI	SMC_BAT
P76	GPI	SMD_BAT
P26	GPI	KBNUM#_3
P25	GPI	KBCAP#_3
P24	GPO	PCIRST#_GATE
P40		EXTSMI_3

ICH7_GPIO	Use As	Signal Name
GPI6	GPO	BACK_OFF#
GPIO7	GPI	WIRELESS_SW#
GPI8	GPI	EXTSMI#
GPI9	TBD	
GPI10	GPI	CHG_FULL_OC
GPI12	GPI	KB_SCI#
GPI13	GPI	MEM_ID0
GPI14	GPI	MEM_ID1
GPIO15	GPO	WL_LAN_LED#
GPIO19	GPI	PANEL_ID
GPIO24	GPI	MEM_400/533#
GPIO25	GPO	CB_SD#
GPIO26	GPO	OP_MUTE#
GPIO27	GPO	WIRELESS_LAN_ON/OFF#
GPIO28	GPO	PWR_1HZ
GPI33	GPO	BT_ON/OFF#
GPI34	GPO	FWH_WP#
GPI35	TBD	
GPI36	GPO	BT_LED#
GPI37	GPI	PCB_ID0
GPIO38	GPI	PCB_ID1
GPIO39	GPI	MEM_ID2

ASUSTek COMPUTER INC

Project Name: S6F

Engineer: MICHAEL WANG

Size: Custom

Title : System Information

Rev: 1.0

Date: Wednesday, January 18, 2006

Sheet 3 of 37

New NET on Yonah

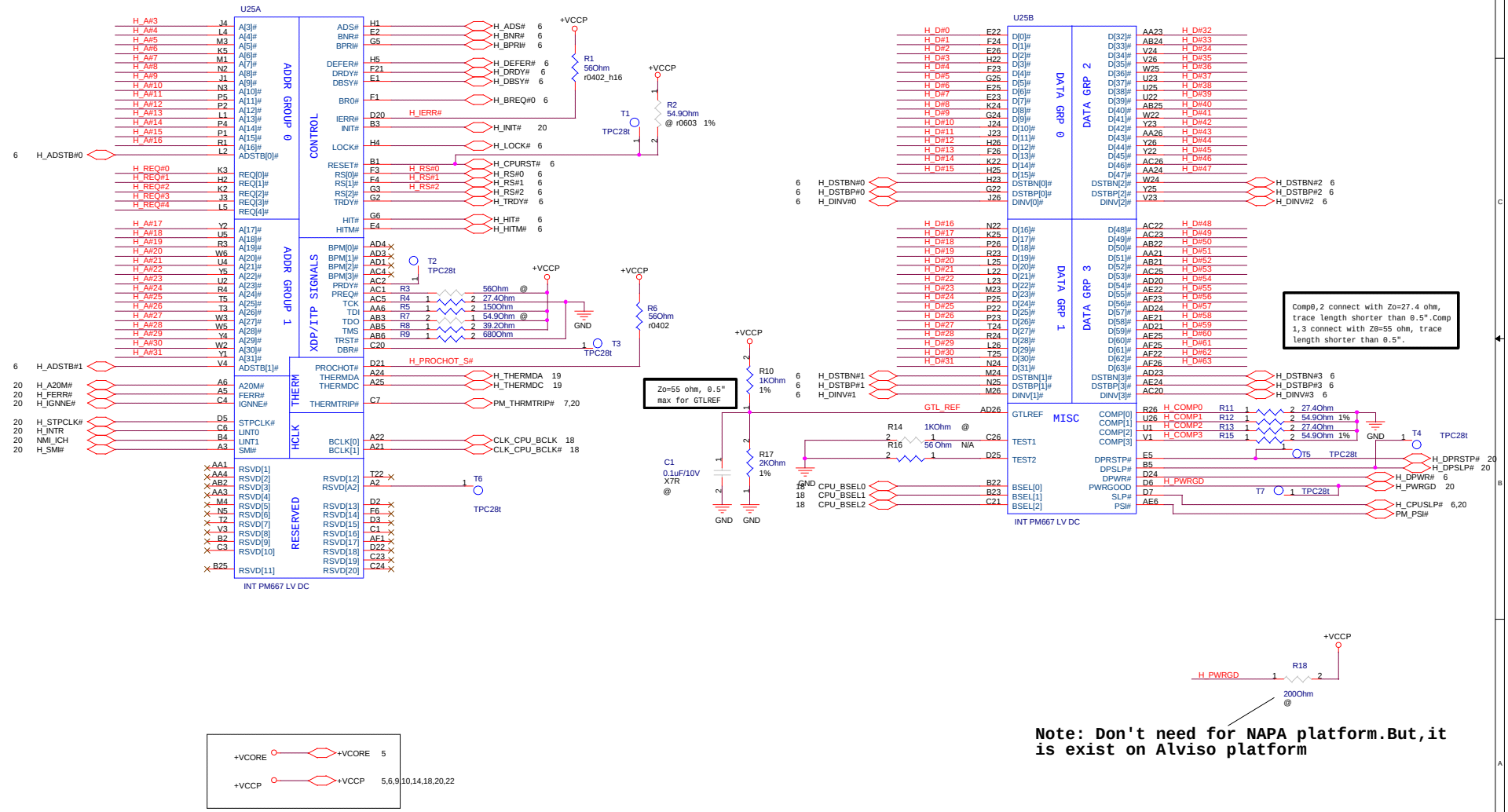
CPU_BSEL2
VR_VID6

Need Check

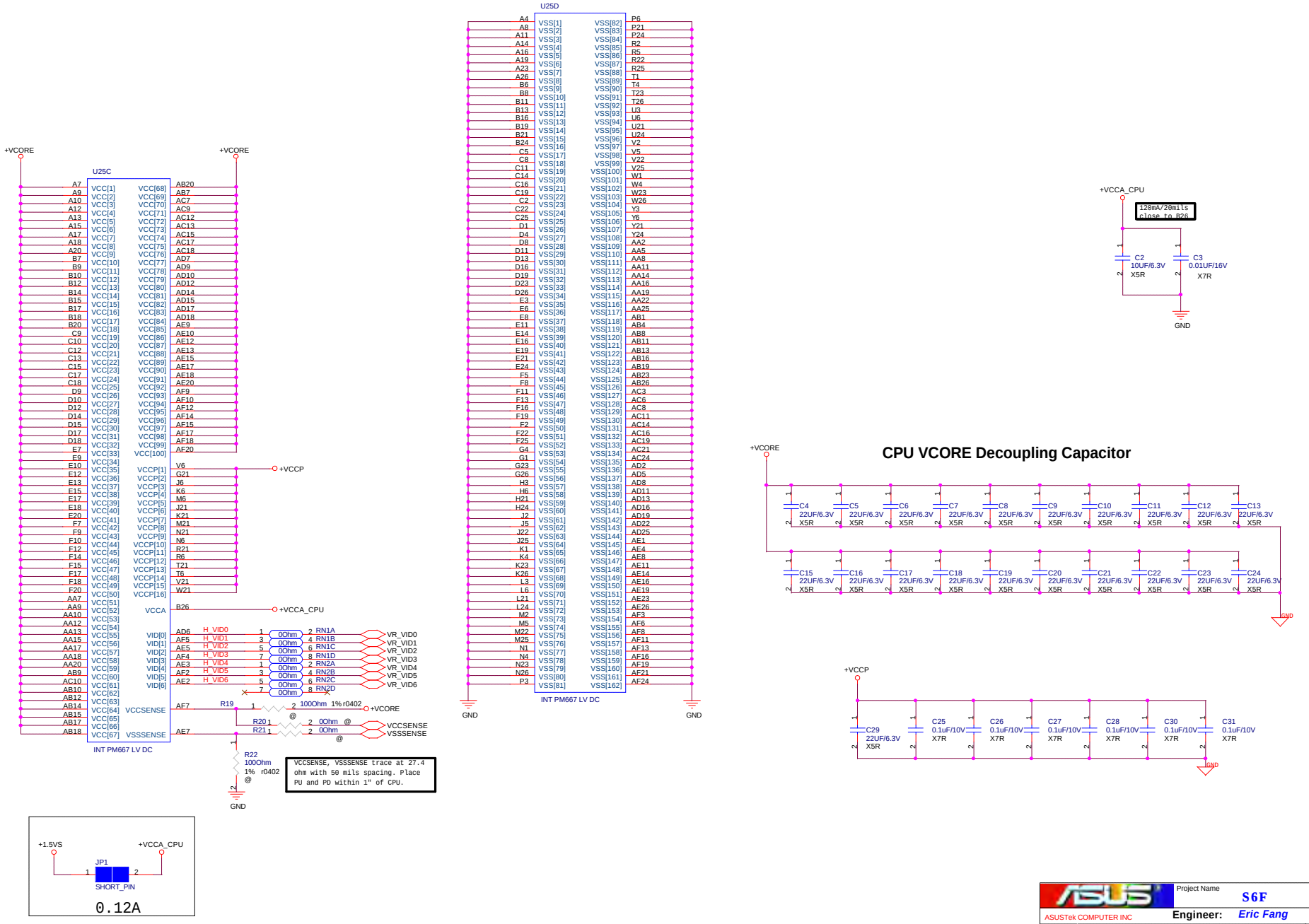
VCCSENSE
VSSENSE

CPU PART NUMBER

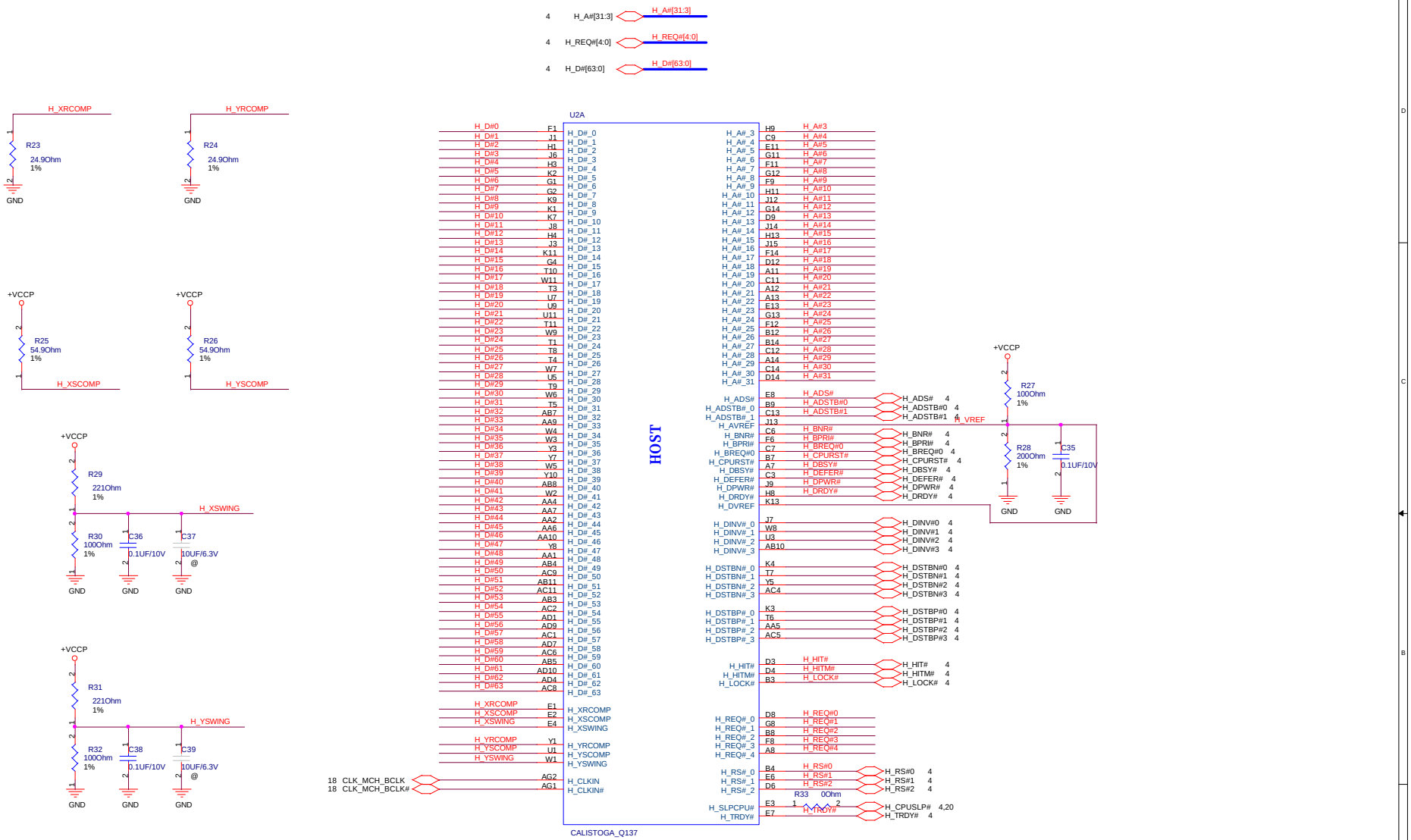
01-011010010	CPU	INT PM667 LV DC 1.66G X48
01-011010011	CPU	INT PM667 LV DC 1.5G X38



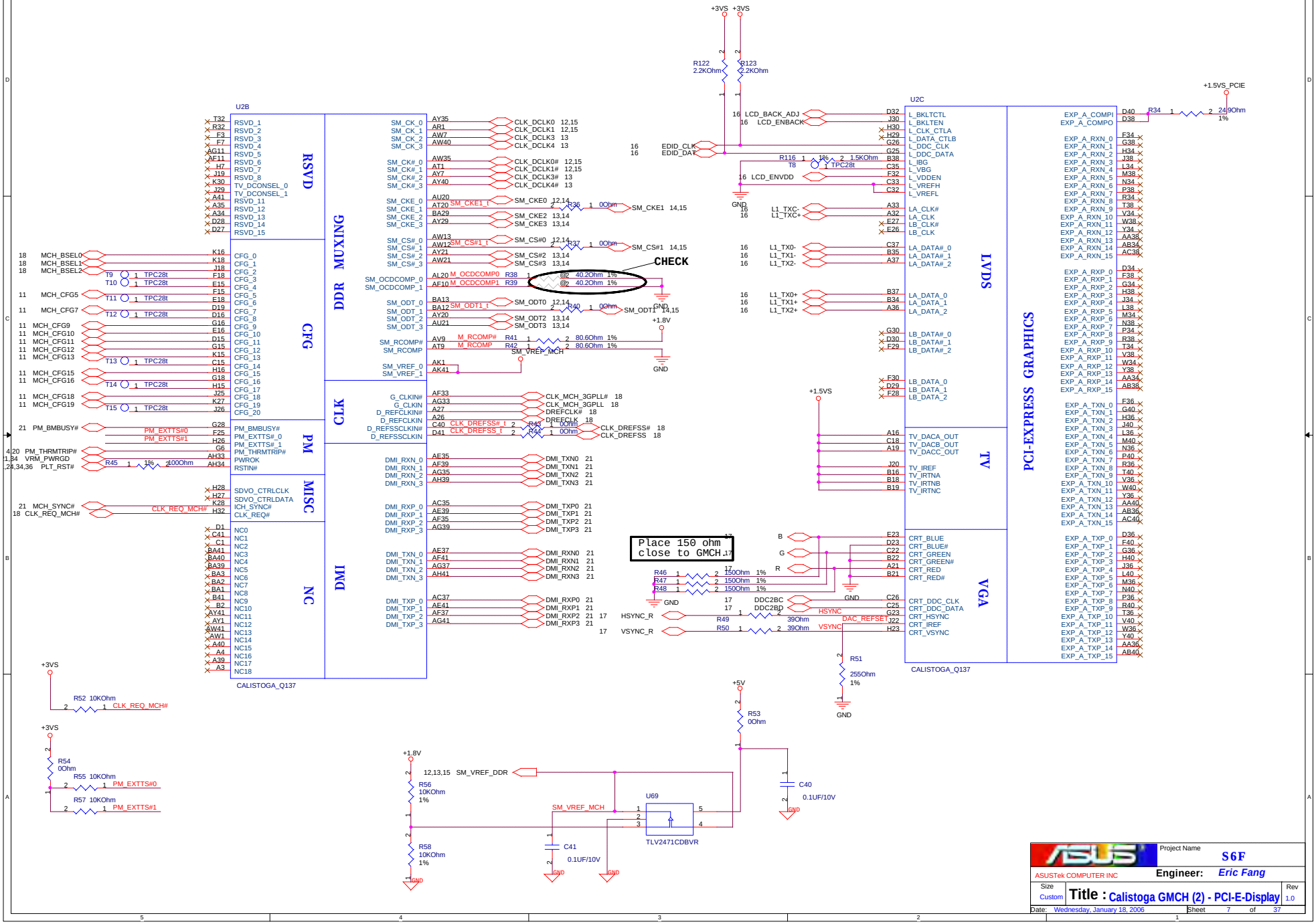
Project Name	S6F
ASUSTek COMPUTER INC	Engineer: Eric Fang
Size: Custom	Title : Yonah CPU (1)
Rev: 1.0	
Date: Wednesday, January 18, 2006	Sheet 4 of 37

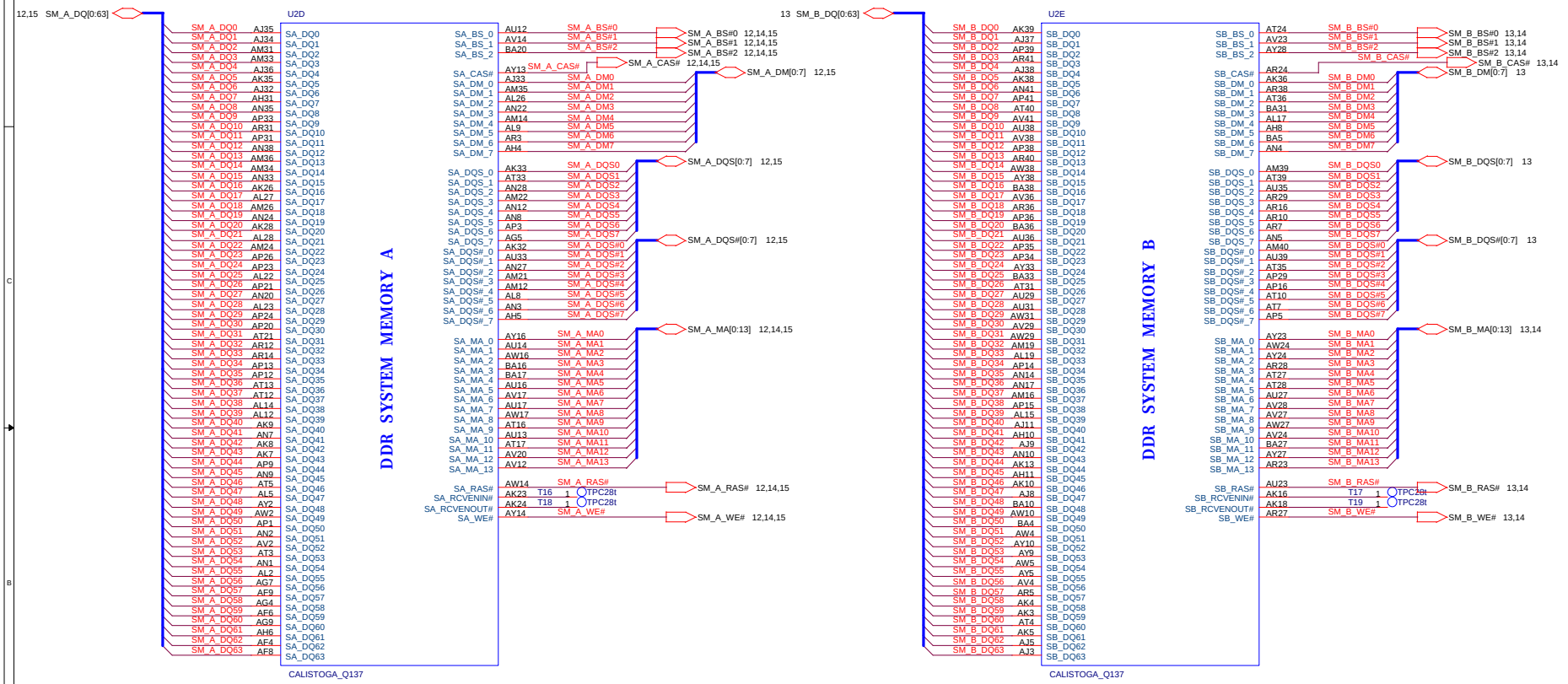


Project Name	S6F
ASUSTek COMPUTER INC	Engineer: Eric Fang
Size: Custom	Title : Yonah CPU (2)
Rev	1.0
Date: Wednesday, January 18, 2006	Sheet 5 of 37



Project Name	S6F
ASUSTek COMPUTER INC	Engineer: Eric Fang
Size: Custom	Title : Calistoga GMCH (1) - HOST
Rev: 1.0	
Date: Wednesday, January 18, 2006	Sheet 6 of 37


U2B
RSVD
DDR MUXING
CFG
CLK
PM
MISC
DMI
NC
CALISTOGA_Q137
U2C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA_Q137
CHECK
Place 150 ohm close to GMCH
U69
TLV2471CDBVR
+3VS
+1.5VS
+1.5VS_PCIE
+1.8V
+5V
GND
R122 2.2KOhm
R123 2.2KOhm
R53 0Ohm
R51 255Ohm 1%
R52 10KOhm
R54 0Ohm
R55 10KOhm
R57 10KOhm
R56 10KOhm 1%
R58 10KOhm 1%
C40 0.1UF/10V
C41 0.1UF/10V
R46 150Ohm 1%
R47 150Ohm 1%
R48 150Ohm 1%
R49 39Ohm
R50 39Ohm
HSYNC
VSYNC
DAC_REFSET
HSYNC_R
VSYNC_R
CLK_REQ_MCH#
PM_EXTTS#0
PM_EXTTS#1
SM_VREF_MCH
SM_VREF_DDR
SM_CKE1
SM_CS#1
SM_ODT1
M_OCDCOMP0
M_OCDCOMP1
M_RCOMP#
M_RCOMP
CLK_DREFSS#
CLK_DREFSS
SM_VREF_0
SM_VREF_1
LCD_BACK_ADJ
LCD_ENBACK
LCD_ENVDD
EDID_CLK
EDID_DAT
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
MCH_CFG5
MCH_CFG7
MCH_CFG9
MCH_CFG10
MCH_CFG11
MCH_CFG12
MCH_CFG13
MCH_CFG15
MCH_CFG16
MCH_CFG18
MCH_CFG19
PM_BMBUSY#
PM_THRMTRIP#
VRM_PWRGD
PLT_RST#
MCH_SYNC#
Project Name S6F
ASUSTek COMPUTER INC
Engineer: Eric Fang
Size Custom
Title : Calistoga GMCH (2) - PCI-E-Display
Rev 1.0
Date: Wednesday, January 18, 2006
Sheet 7 of 37



Project Name: S6F

ASUSTek COMPUTER INC

Engineer: Eric Fang

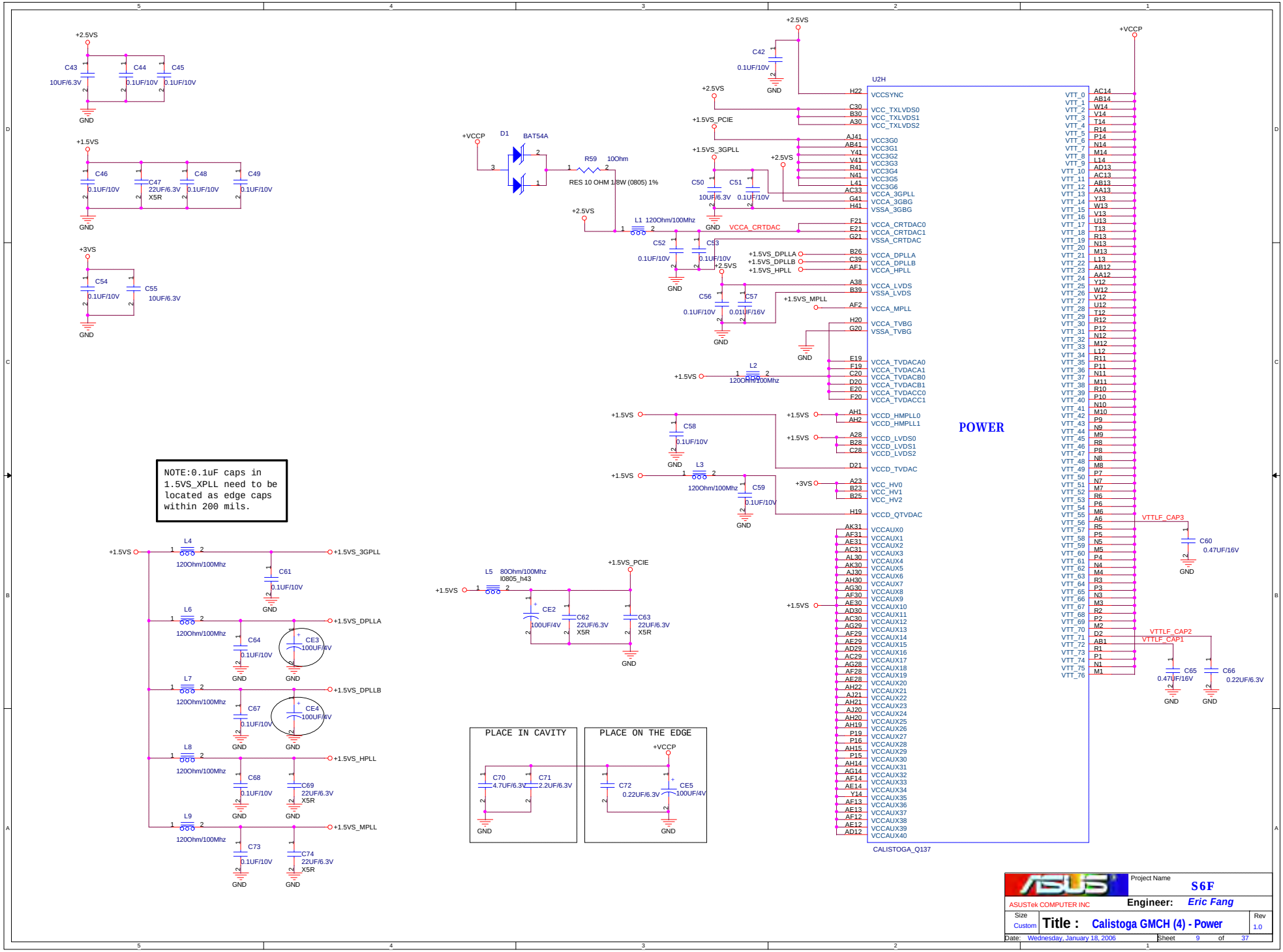
Size: Custom

Title : Calistoga GMCH (3) - DDR2

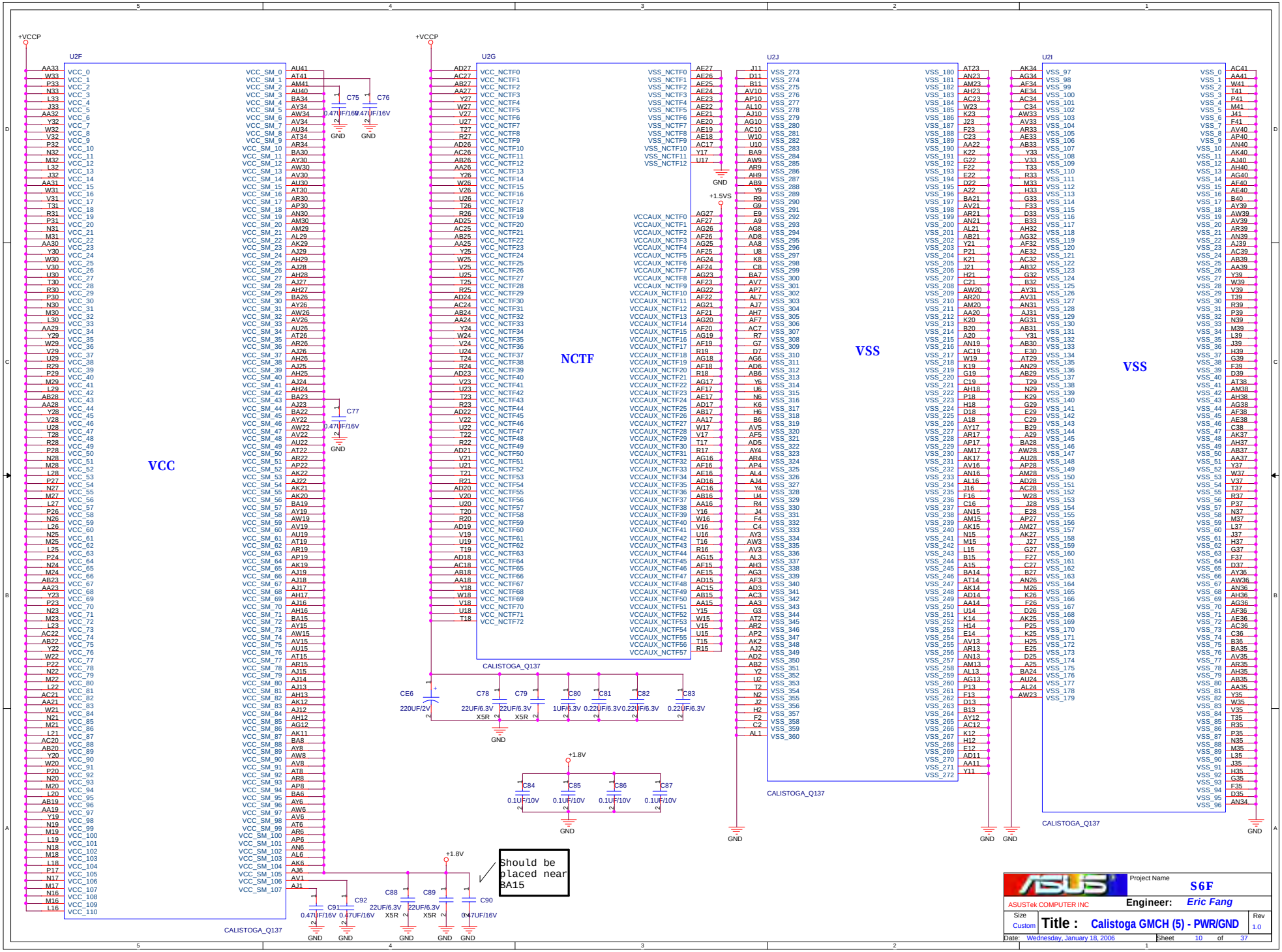
Rev: 1.0

Date: Wednesday, January 18, 2006

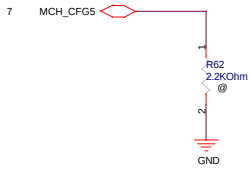
Sheet 8 of 37



ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : Calistoga GMCH (4) - Power	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 9 of 37	



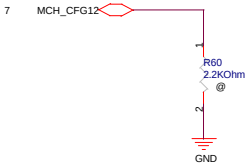
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : Calistoga GMCH (5) - PWR/GND	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 10 of 37	

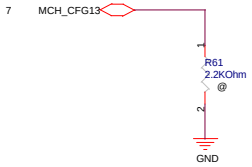


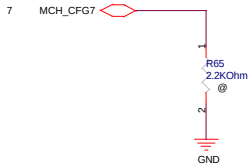
CFG5 : DMI STRAP

LOW = DMI X 2

HIGH = DMI X 4 (Default)



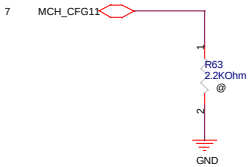




CFG7 : CPU STRAP

LOW = Mobile Prescott

HIGH = Dothan CPU (Default)



CFG11 : PSB 4X CLK ENABLE

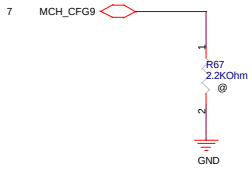
LOW = 4X ENABLED

HIGH 8X ENABLED (Default)

CFG19 : DMI LANE REVERSAL

LOW = NORMAL

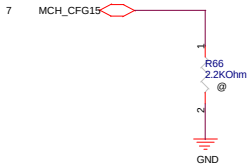
HIGH = LANES REVERSED



CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE

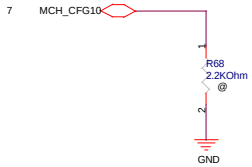
HIGH = NORMAL OPERATION (Default)



CFG15 :ICH RESET DISABLE

LOW = ICH RESET DISABLE

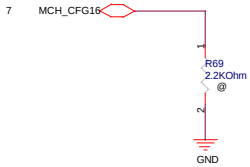
HIGH = NORMAL OPERATION



CFG10: HOST PLL VCO SELECT

LOW = RESERVED

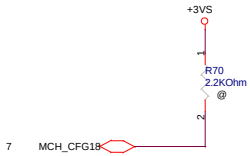
HIGH = MOBILITY



CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled

HIGH = Dynamic ODT Enabled (Default)

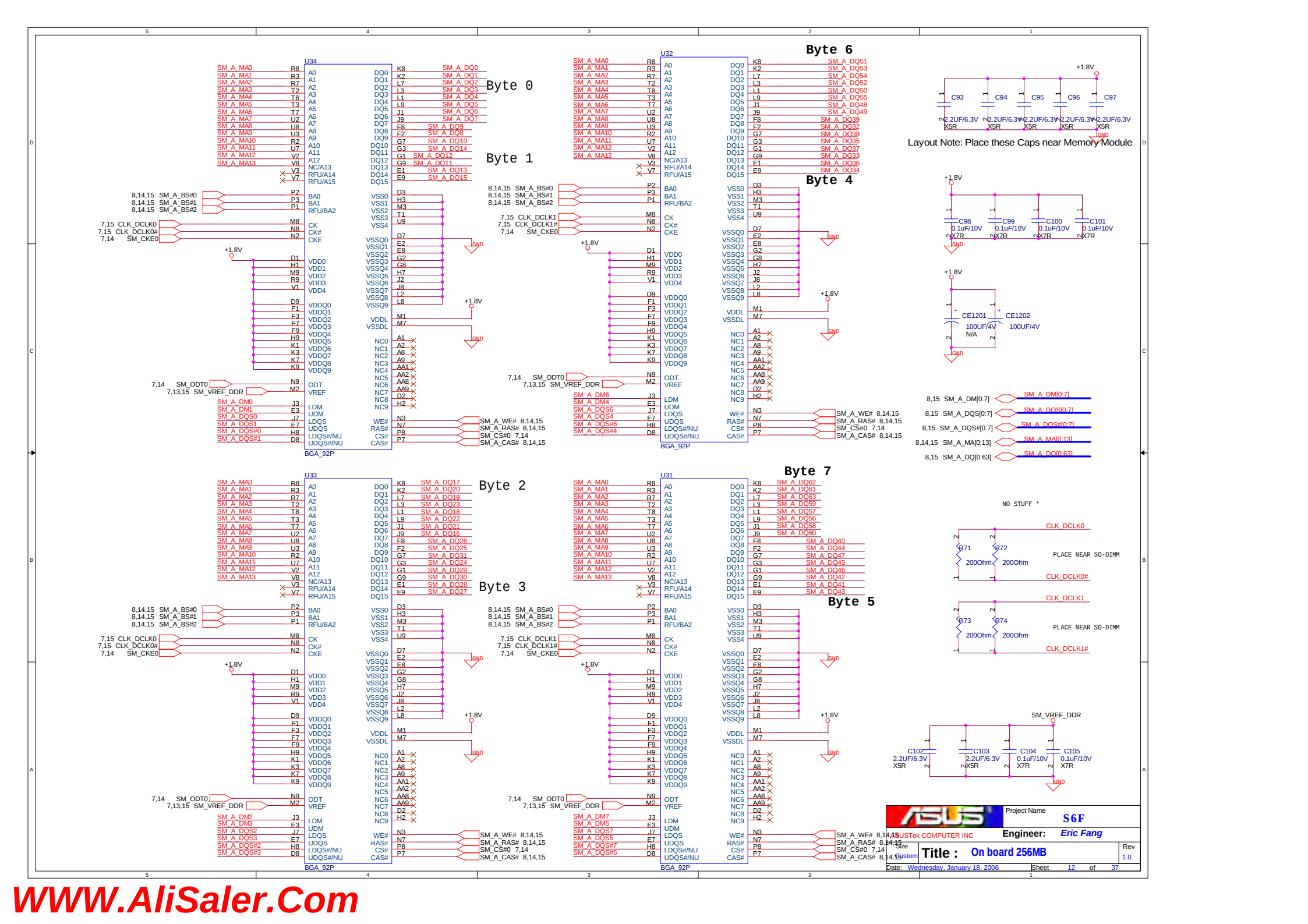


CFG18 : GMCH Core Voltage Level

LOW = 1.05V (Default)

HIGH = 1.5V

ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: *Eric Fang*	
Size: Custom	Title : Calistoga GMCH (6) - Strapping	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 11 of 37	



SM_B_MA[0:13] SM_B_MA[0:13] 8,14

SM_B_DQ[0:63] SM_B_DQ[0:63] 8

SM_B_DM[0:7] SM_B_DM[0:7] 8

SM_B_DQS[0:7] SM_B_DQS[0:7] 8

SM_B_DQS#[0:7] SM_B_DQS#[0:7] 8

U70A

DDR_DIMM_200P

Byte7

Byte 5

Byte4

Byte6

Byte3

Byte 2

Byte1

Byte 0

U70B

DDR_DIMM_200P

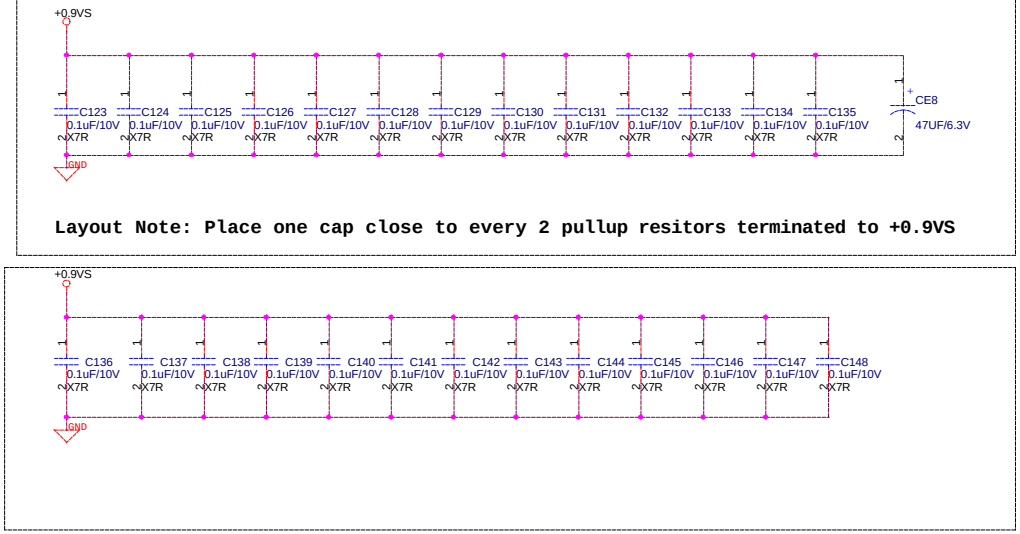
NO STUFF *

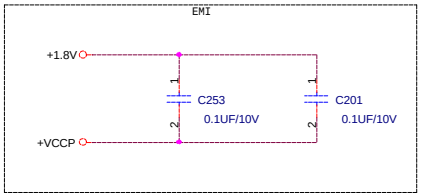
Layout Note: Place these Caps near uDIMM

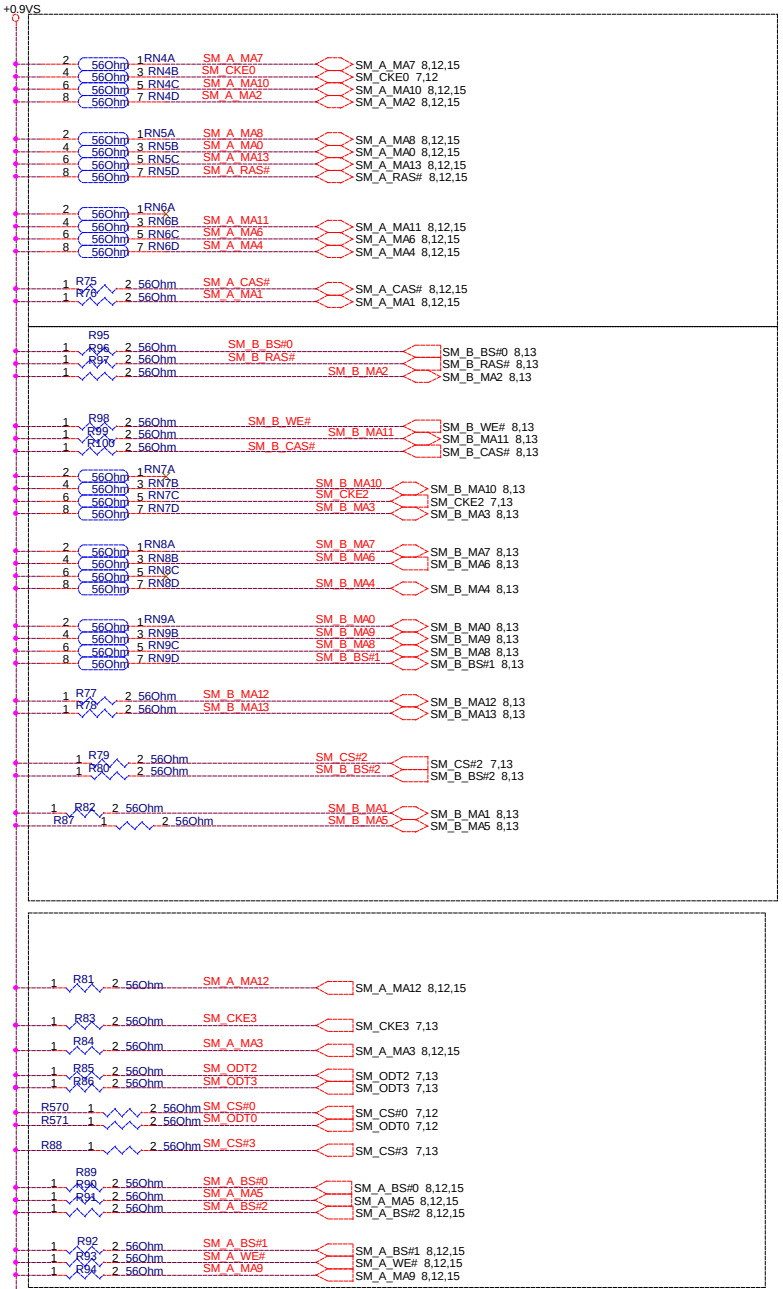
Layout Note: Place these Caps near uDIMM

Layout Note: Place these High-Freq decoupling Caps near the GMCH

ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : DDR2 Micro DIMM	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 13 of 37	







For 8 pcs memory implement

ASUSTek COMPUTER INC

Project Name: S6F

Engineer: Eric Fang

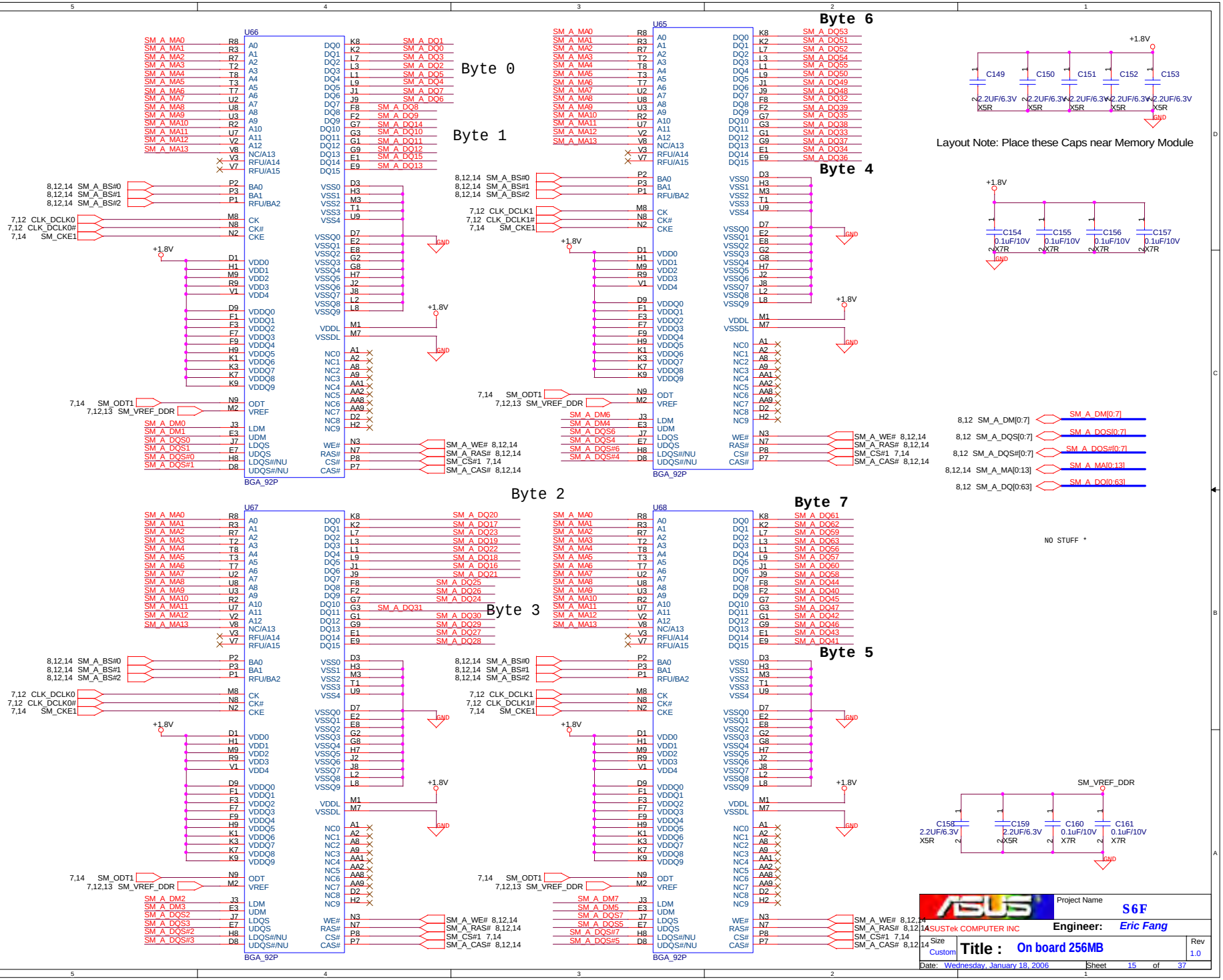
Size: Custom

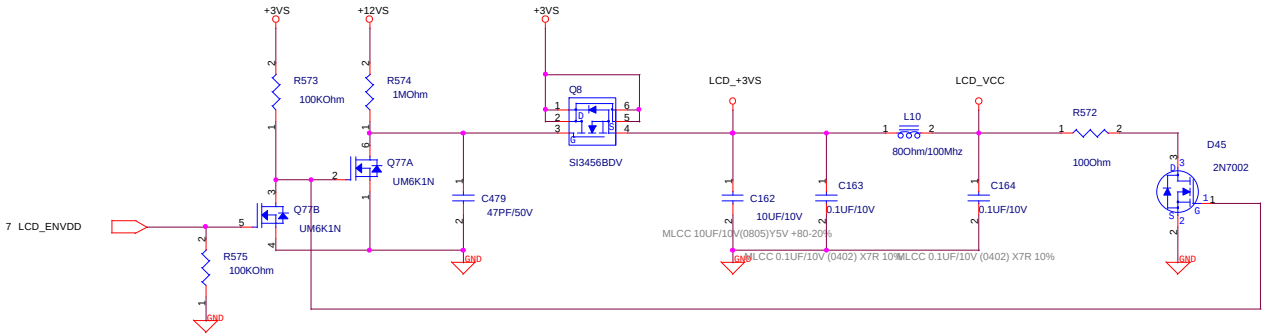
Title : DDR2 Termination

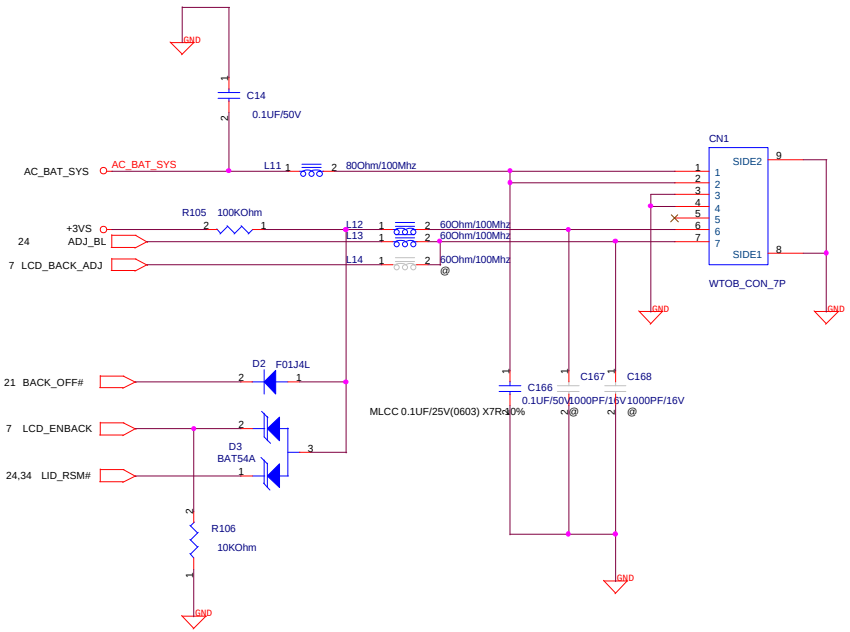
Rev: 1.0

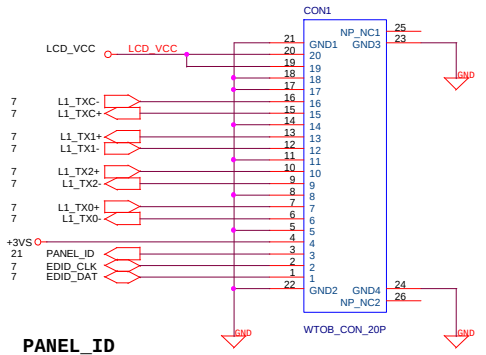
Date: Wednesday, January 18, 2006

Sheet 14 of 37


Byte 0
Byte 1
Byte 2
Byte 3
Byte 4
Byte 5
Byte 6
Byte 7
U66
U65
U67
U68
BGA_92P
Layout Note: Place these Caps near Memory Module
NO STUFF *
Project Name
S6F
SUSTek COMPUTER INC
Engineer:
Eric Fang
Title :
On board 256MB
Size
Custom
Rev
1.0
Date: Wednesday, January 18, 2006
Sheet 15 of 37



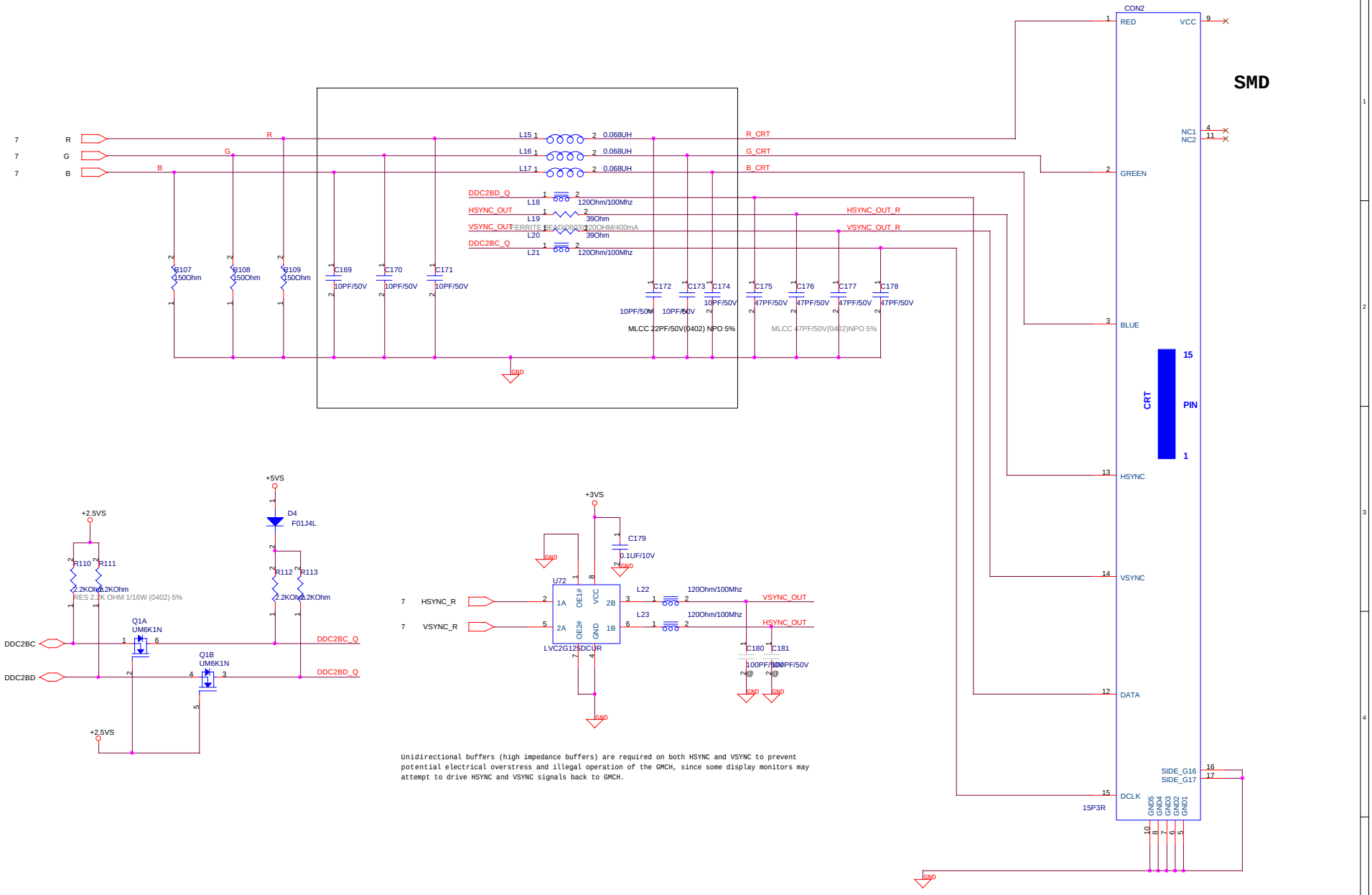




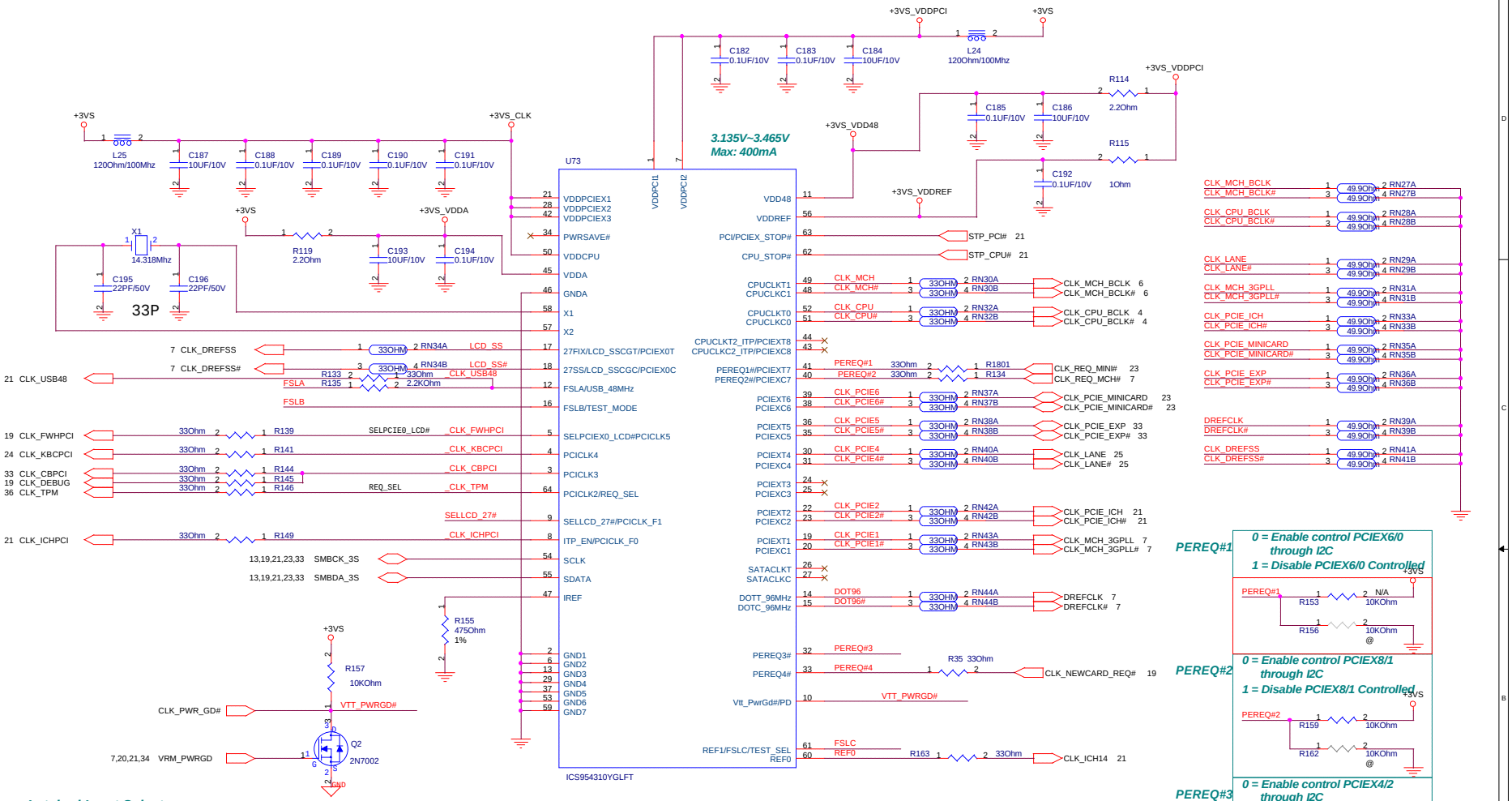
PANEL_ID
HI 10.6
LO 11.1

current rating = 0.3A

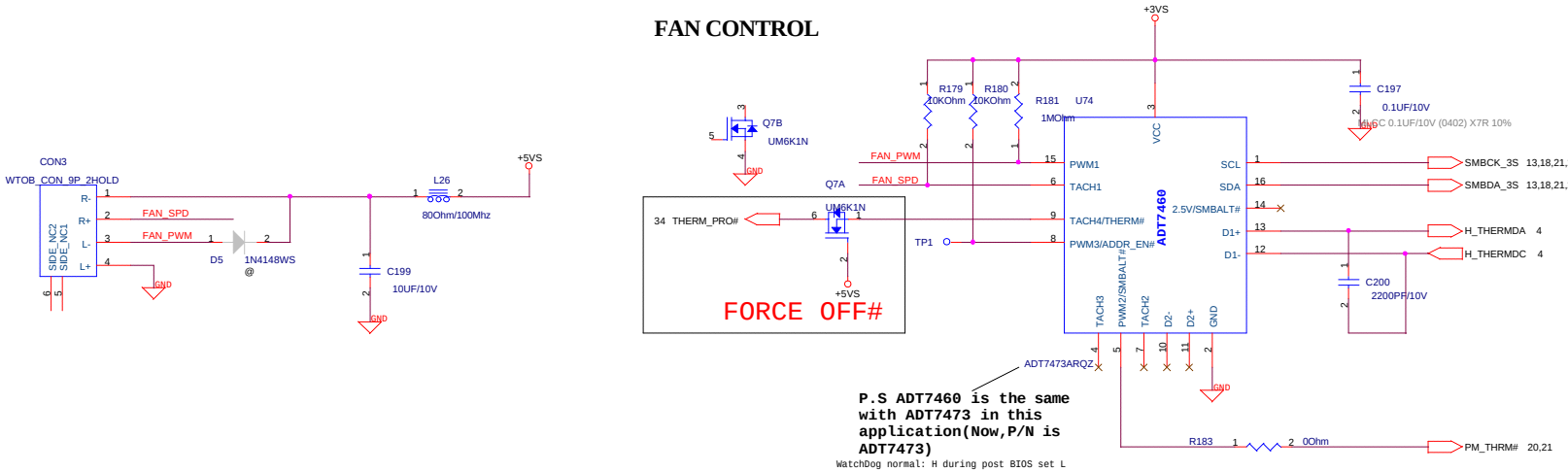
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title :	LCD CON	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 16 of 37		



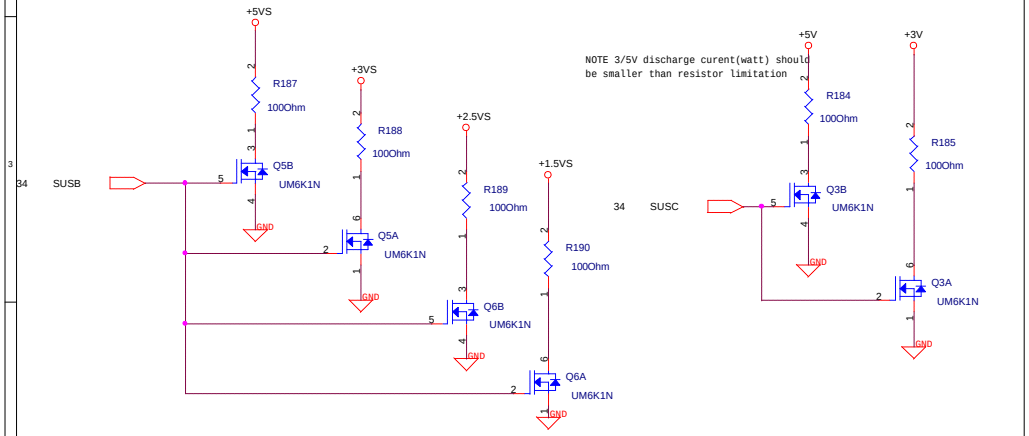
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	Eric Fang	
Size: Custom	Title : CRT PORT		Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 17 of 37		



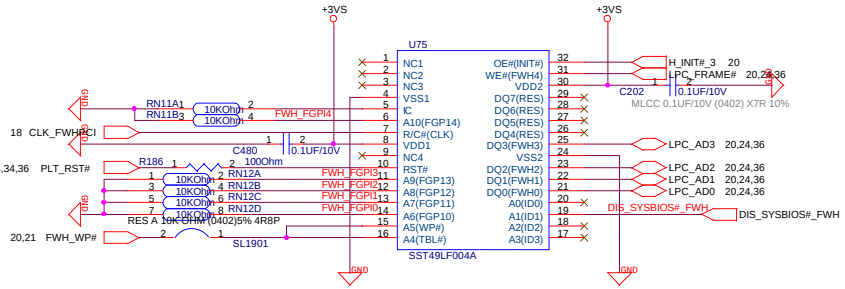
FAN CONTROL



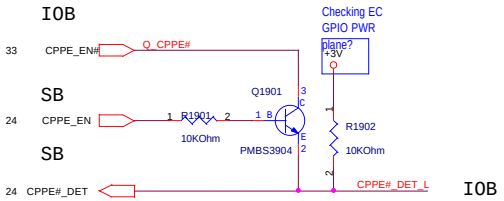
Discharge circuit for power fast down

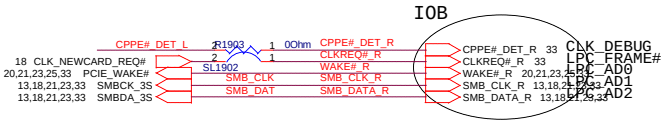


BIOS

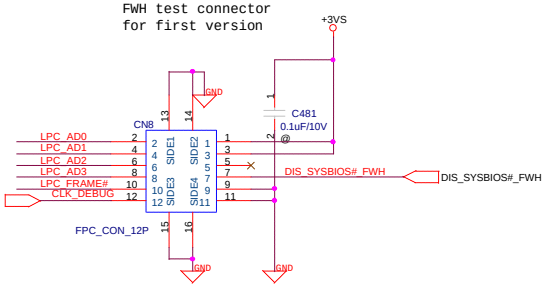


IOB

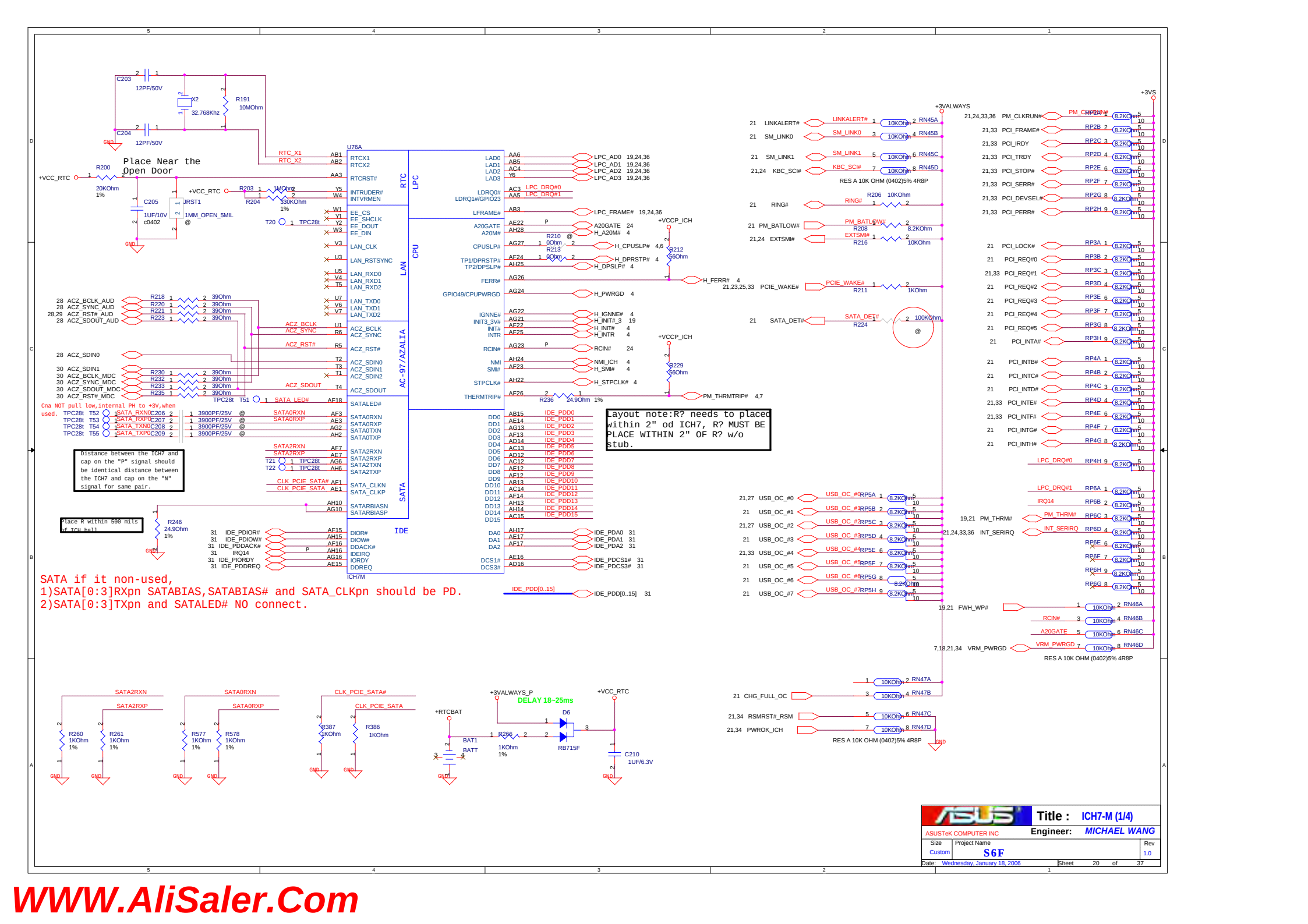


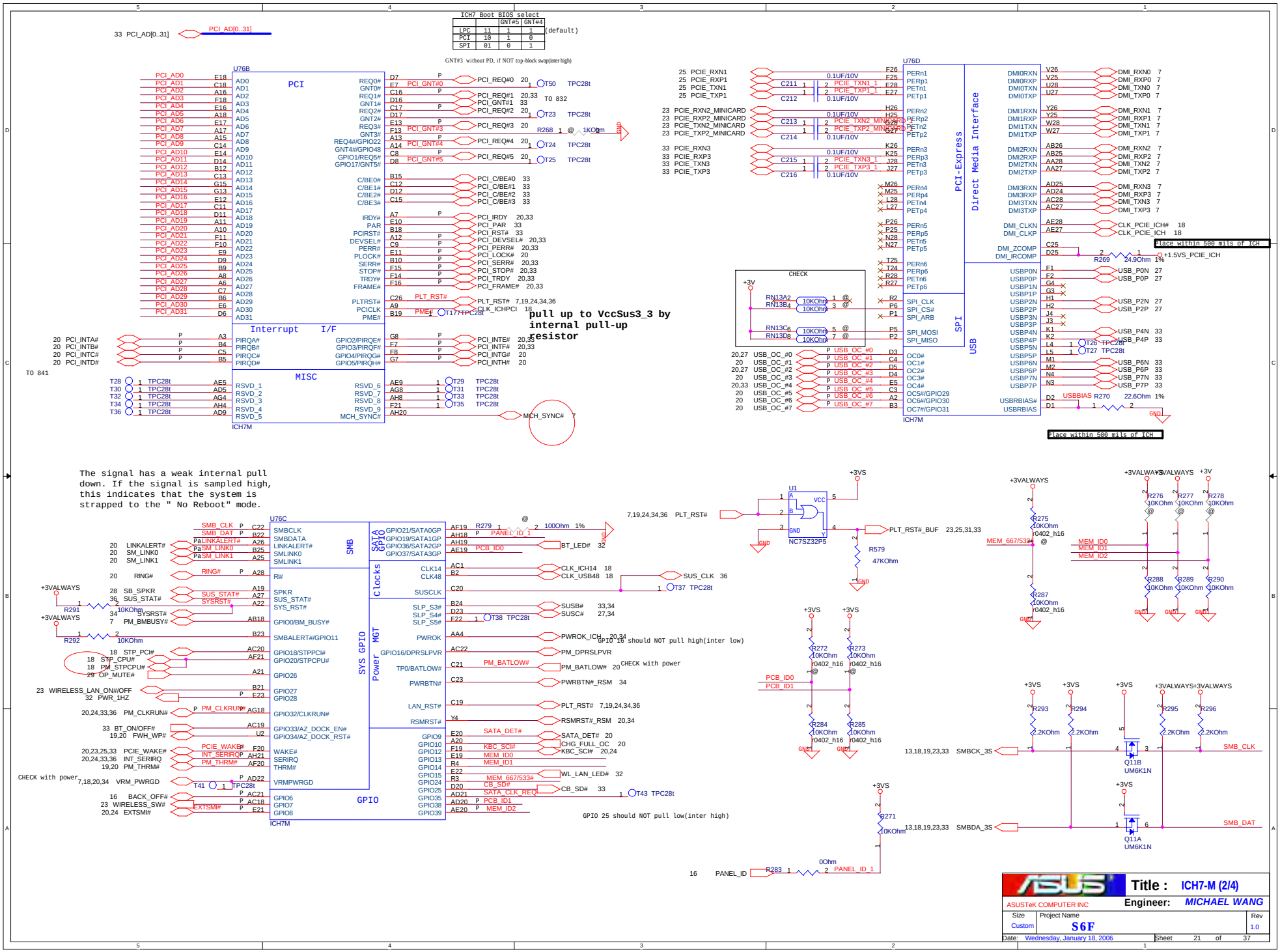


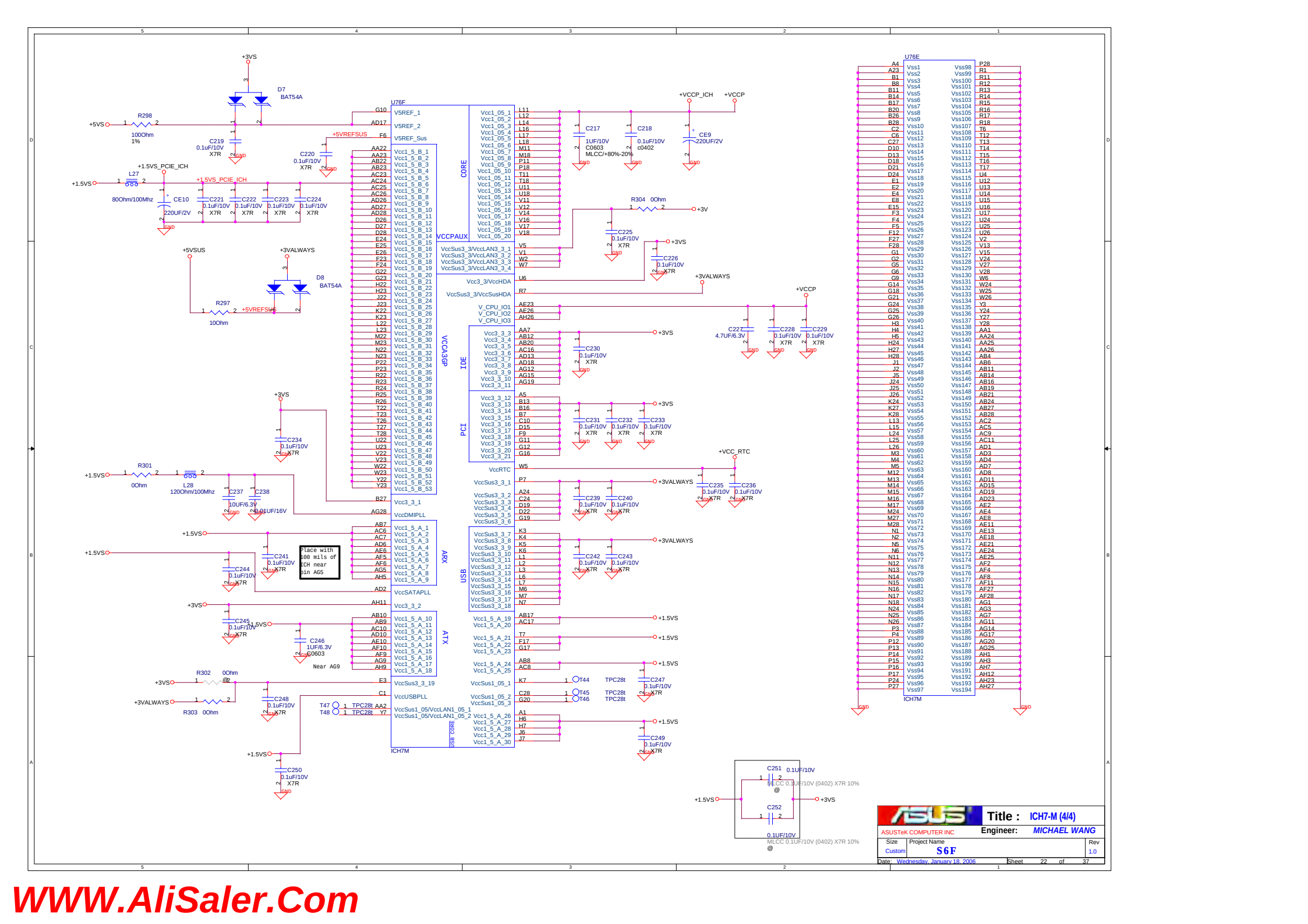
FWH test connector for first version



ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : FAN/THERMAL/FWH	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 19 of 37	

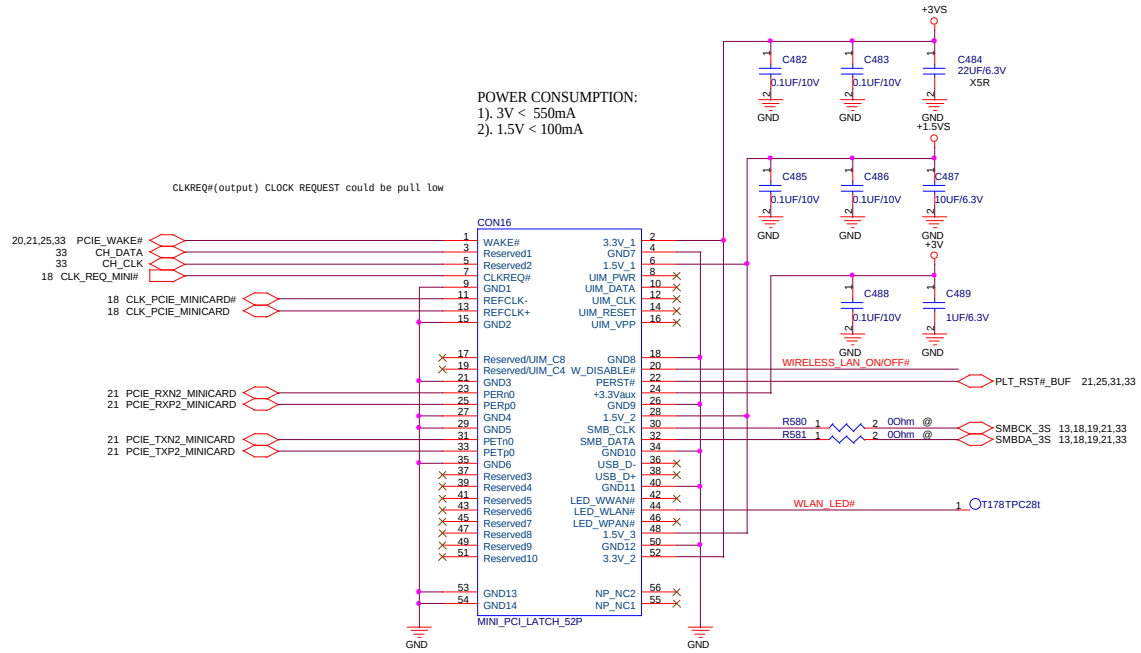


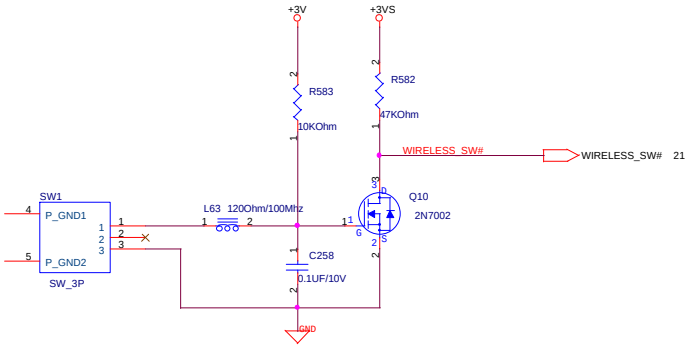

ICH7 Boot BIOS select
GNT#5 GNT#4
LPC 11 1 1 (default)
PCI 10 1 0
SPI 01 0 1
GNT#3 without PD, if NOT top-block swap(inter high)
33 PCI_AD[0..31]
PCI_AD[0..31]
U76B
PCI
Interrupt I/F
MISC
SYS GPIO
SMB
Clocks
Power MGT
GPIO
ICH7M
TO 841
pull up to VccSus3_3 by internal pull-up resistor
The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.
GPIO 16 should NOT pull high(inter low)
CHECK with power
GPIO 25 should NOT pull low(inter high)
U76D
PCI-Express
Direct Media Interface
SPI
USB
CHECK
Place within 500 mils of ICH
Title : ICH7-M (2/4)
ASUSTeK COMPUTER INC
Engineer: MICHAEL WANG
Size Custom
Project Name S6F
Rev 1.0
Date: Wednesday, January 18, 2006
Sheet 21 of 37

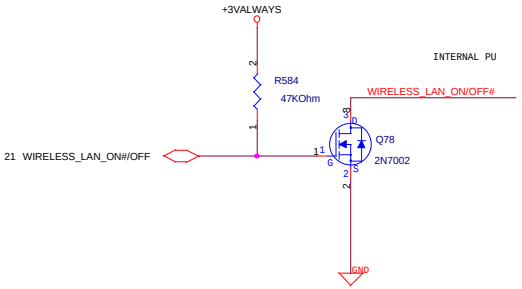


POWER CONSUMPTION:
1). 3V < 550mA
2). 1.5V < 100mA

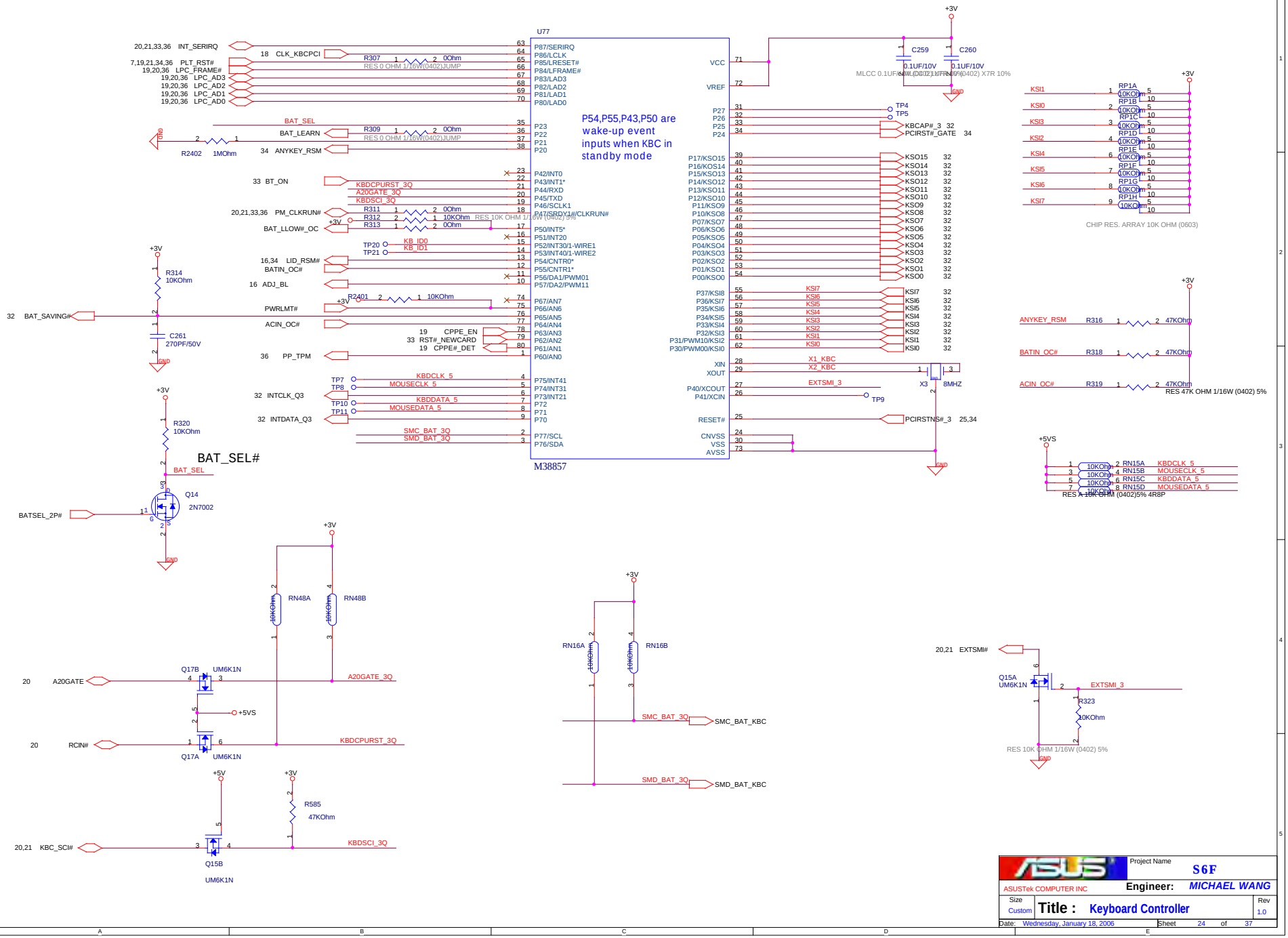
CLKREQ#(output) CLOCK REQUEST could be pull low



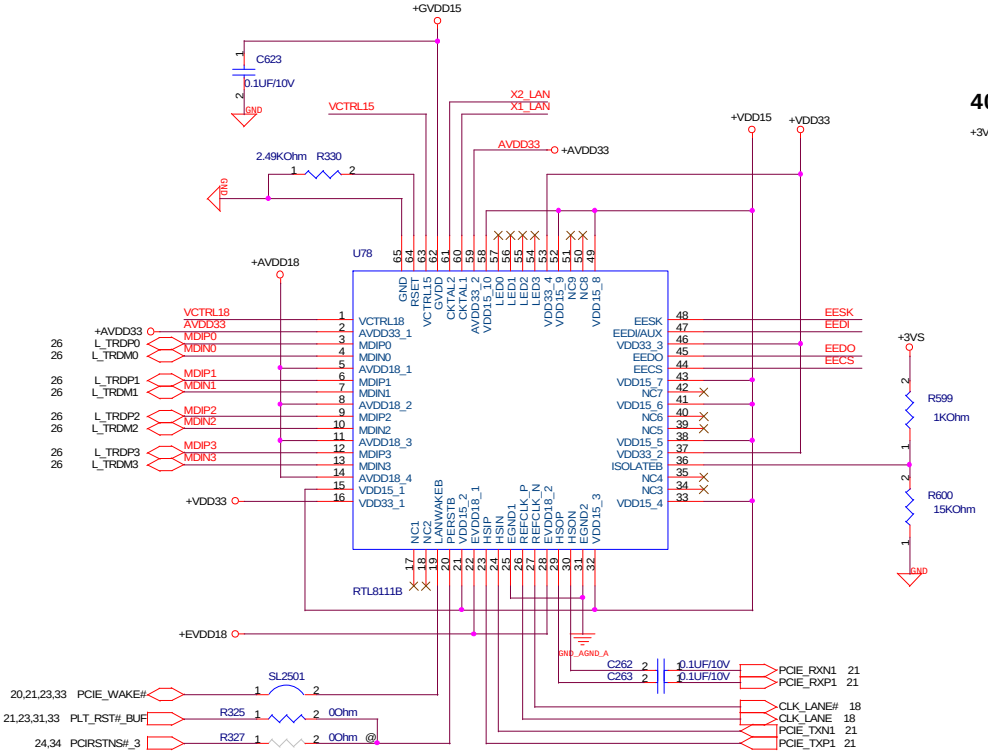


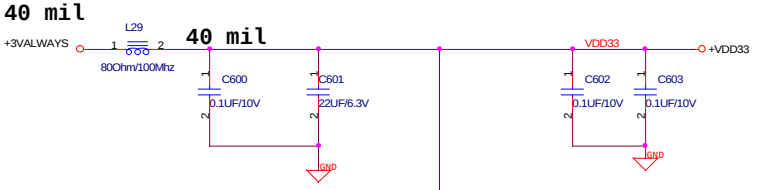


ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : MINI PCI	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 23 of 37	



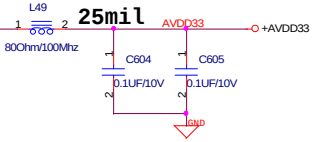
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA

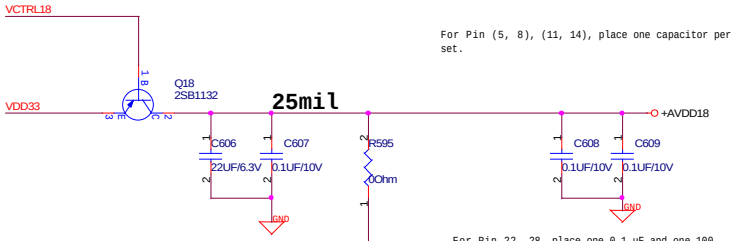




For Pin 16, 37, 46, 53, place one capacitor per pin.

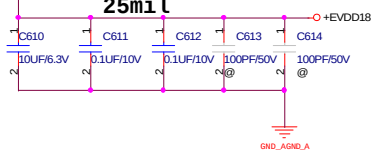
For Pin 2, 59, place one capacitor per pin.

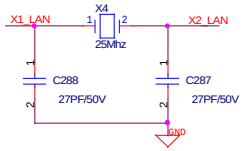


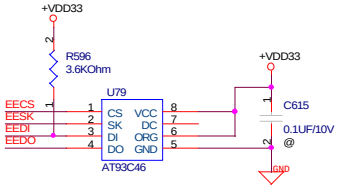


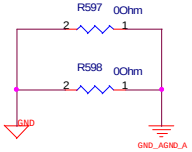
For Pin (5, 8), (11, 14), place one capacitor per set.

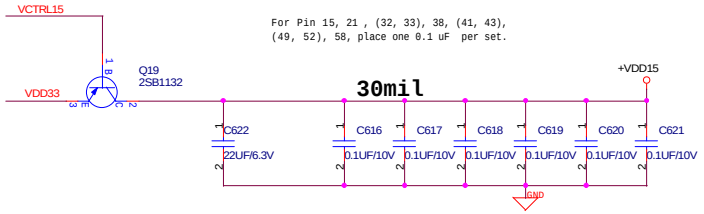
For Pin 22, 28, place one 0.1 uF and one 100 pF per pin.





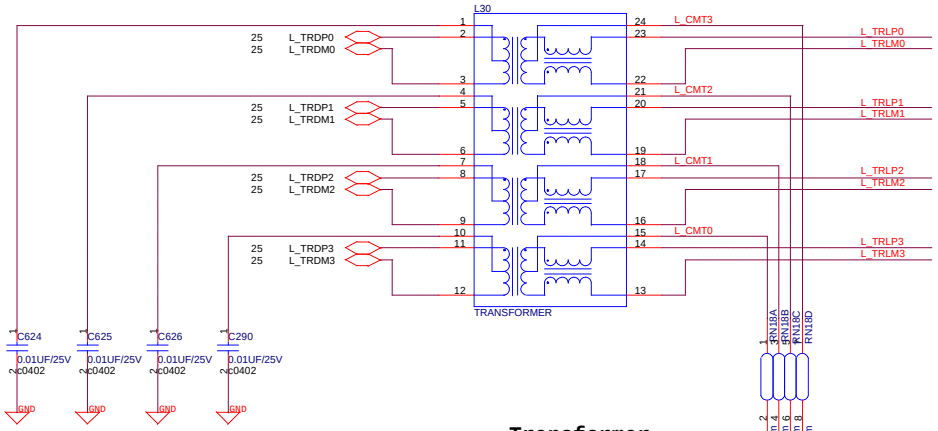






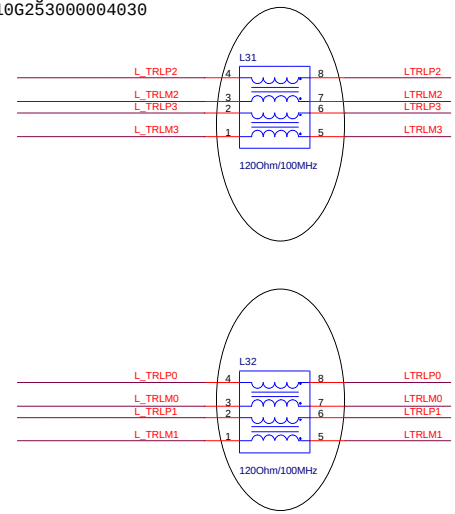
For Pin 15, 21 , (32, 33), 38, (41, 43), (49, 52), 58, place one 0.1 uF per set.

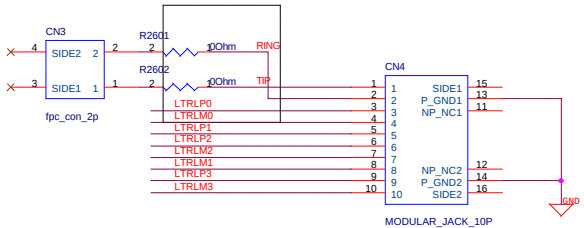
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Edmmund Hu	
Size: Custom	Title : Realtek RTL8111b	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 25 of 37	

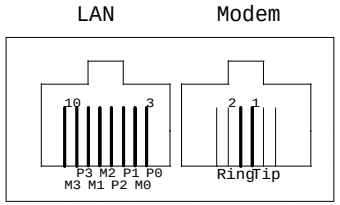


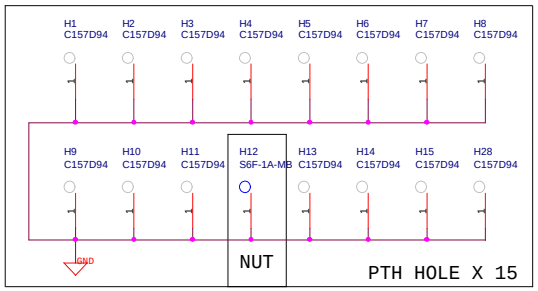
Transformer close CN4

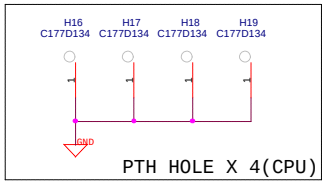
changed 09-091120000 to 10G253000004030

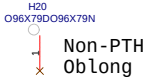


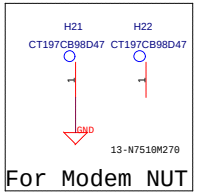


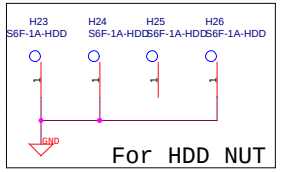




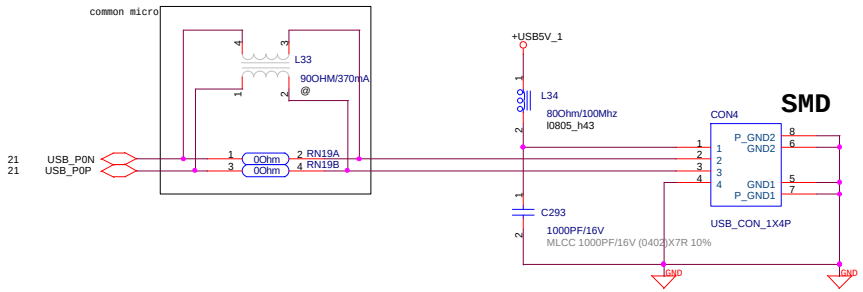


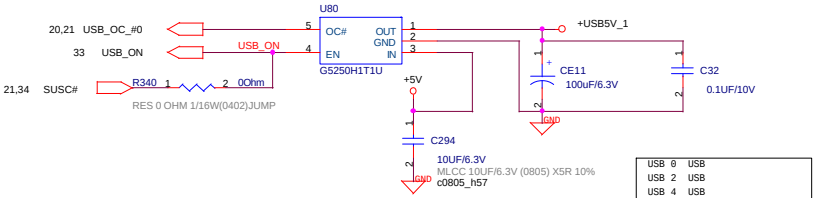




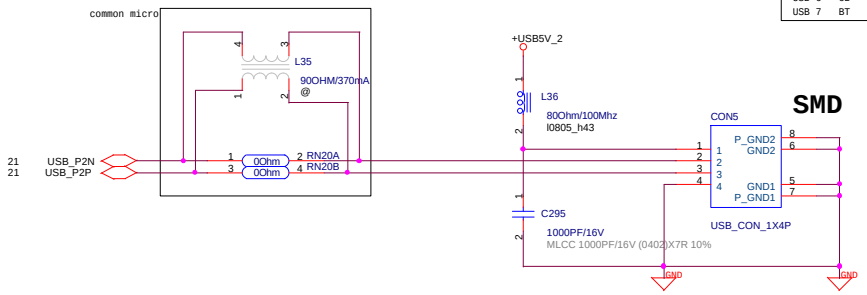


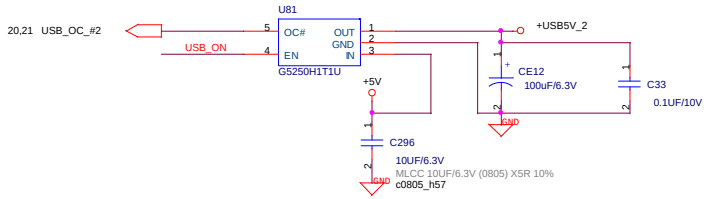
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : LAN I/O	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 26 of 37	

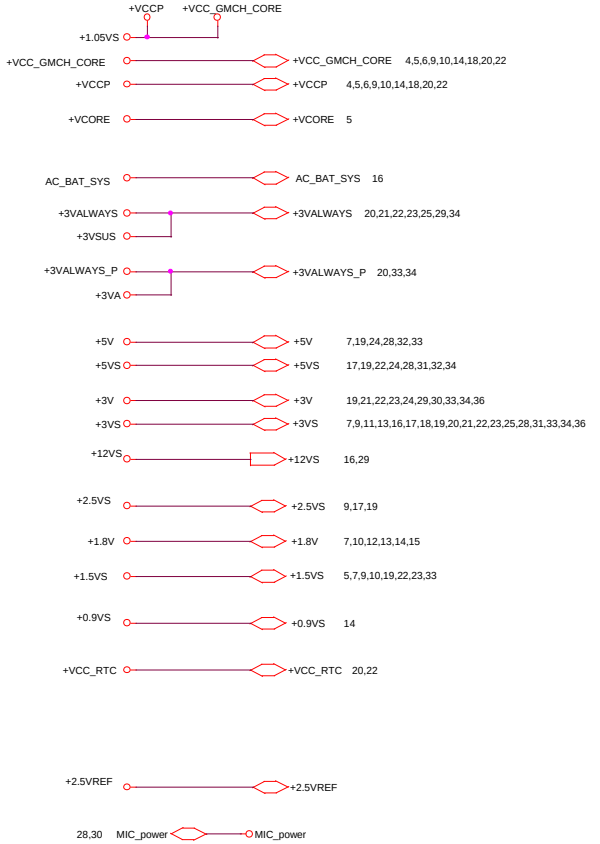




USB 0	USB		
USB 2	USB		
USB 4	USB		
USB 6	CB	/Do Not OC#	
USB 7	BT	/Do Not OC#	

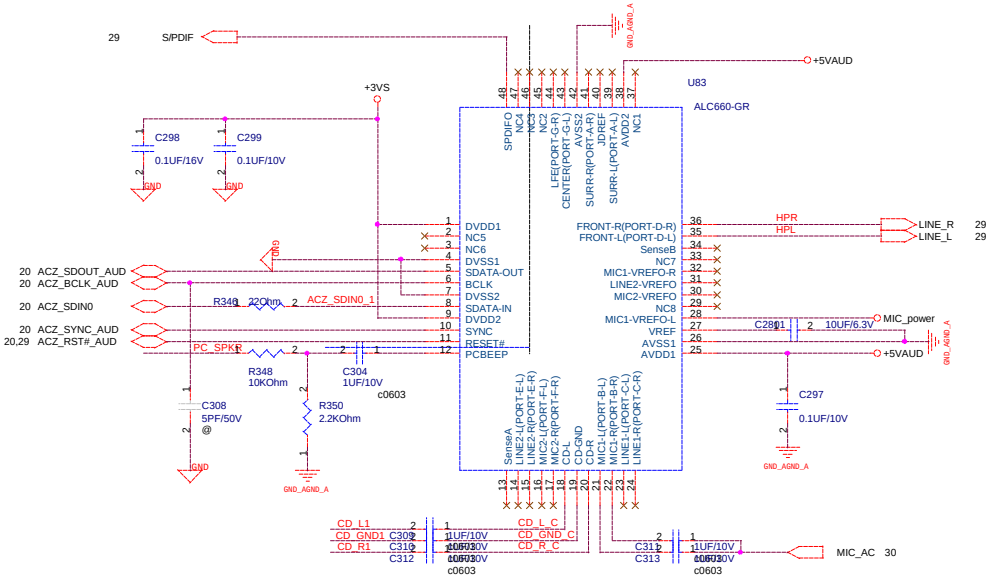


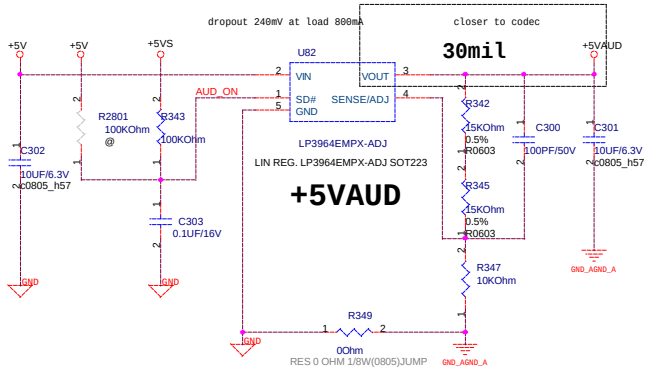


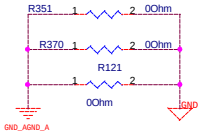


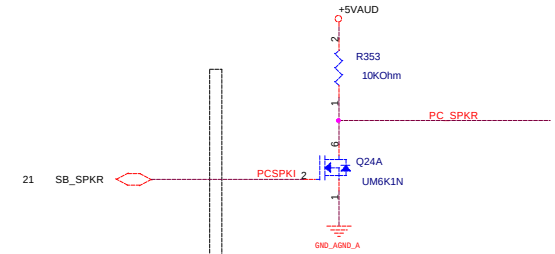
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 27 of 37	

D0 (DVDD/AVDD) 15.5mA/45.9mA

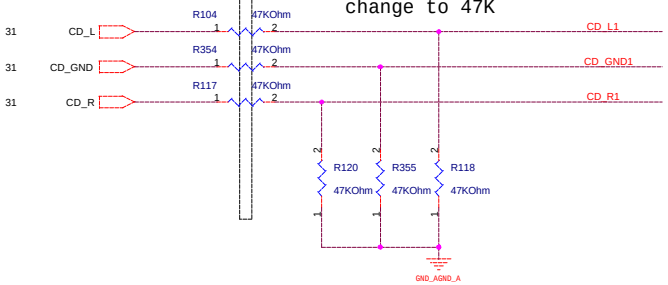




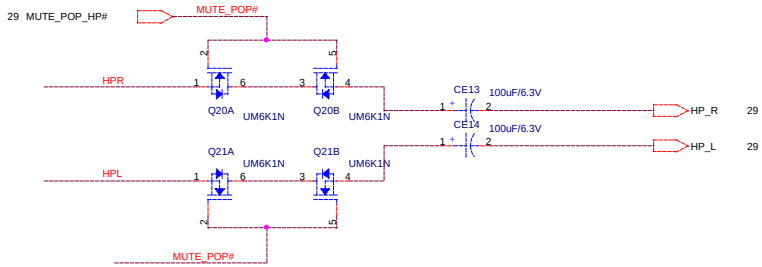




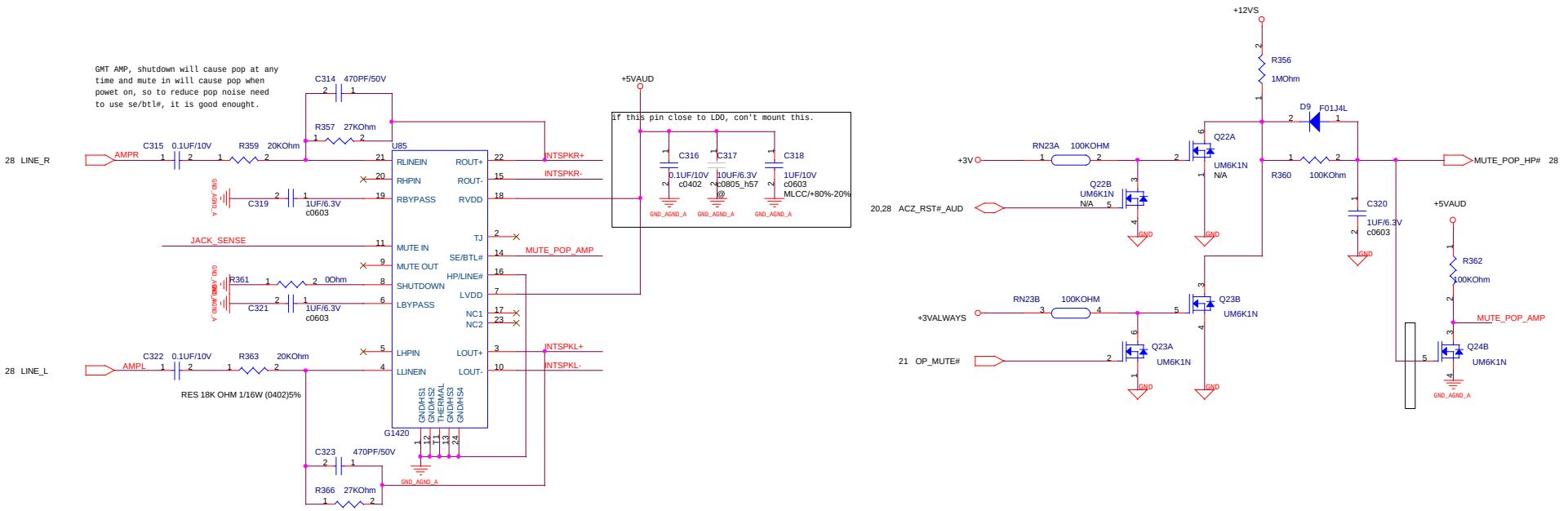
change to 47K



To HeadPhone



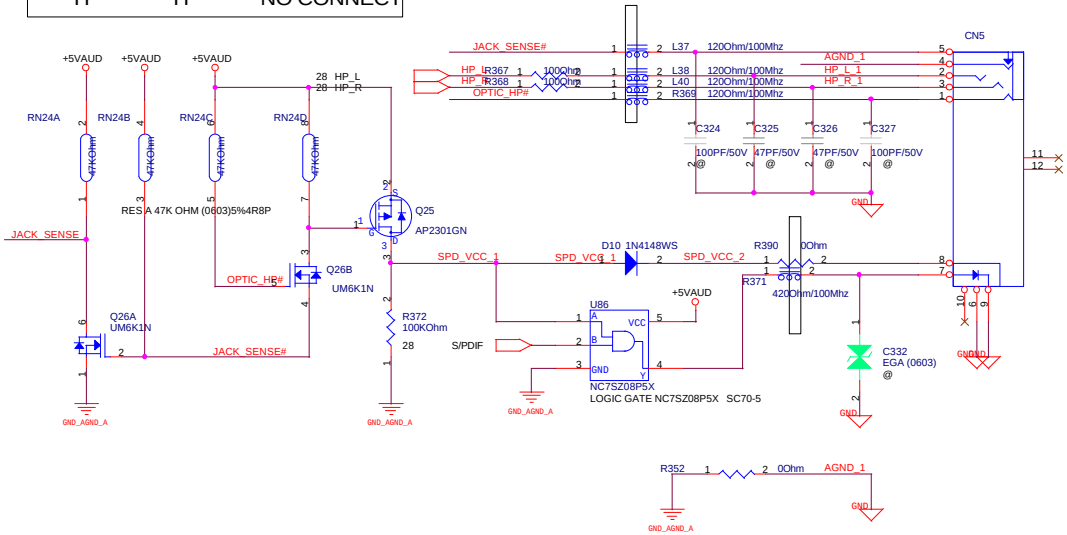
ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : REALTEK ALC861	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 28 of 37	

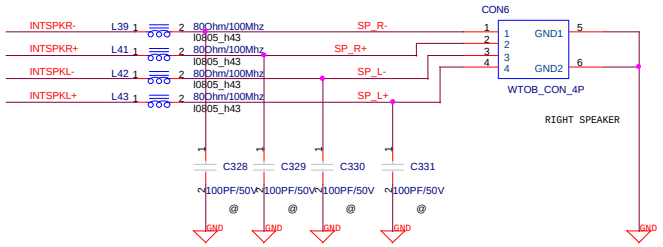


A

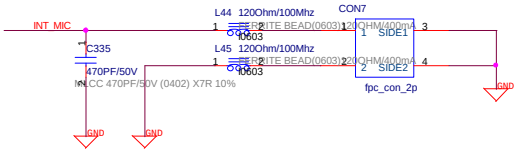
A

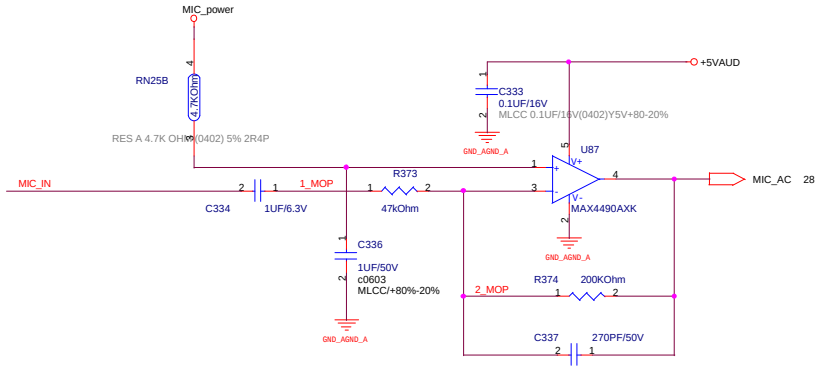
JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT



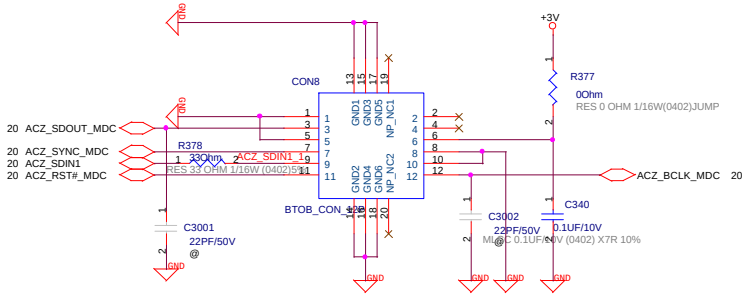


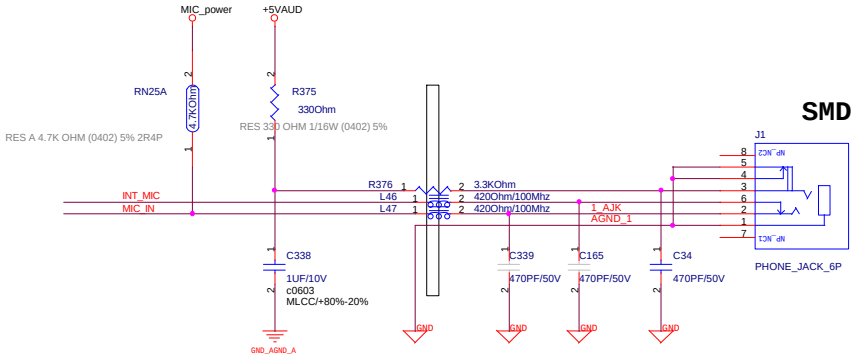
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	MICHAEL WANG	
Size: Custom	Title :	AUDIO AMP	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet	29 of 37	



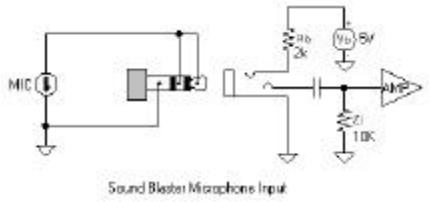


MDC CNT



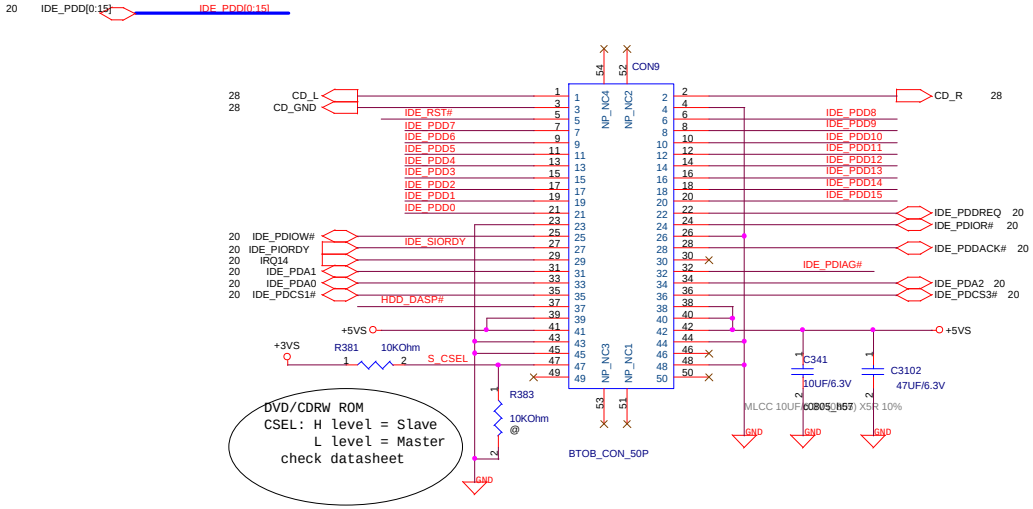


SMD

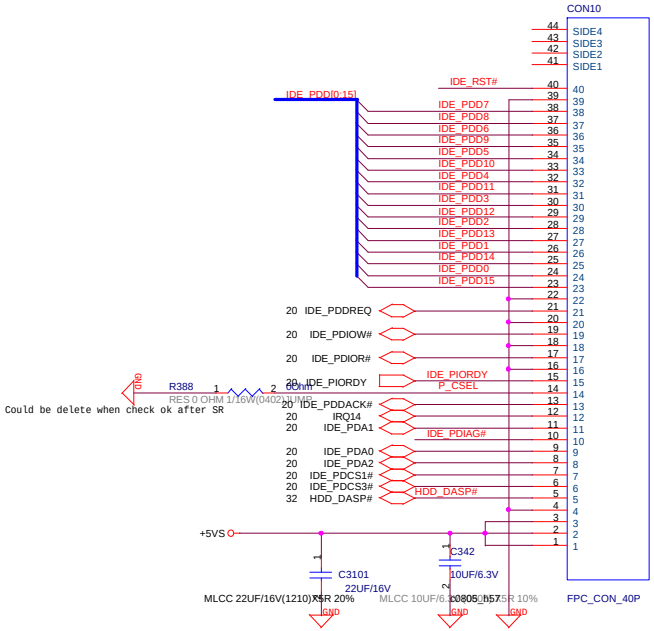


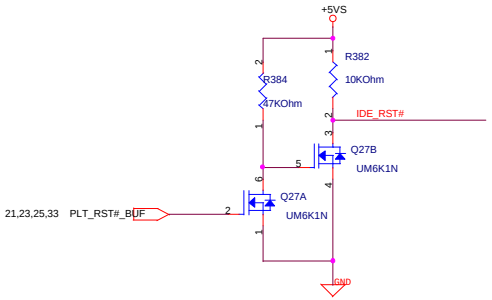
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : MDC CONN & LED	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 30 of 37	

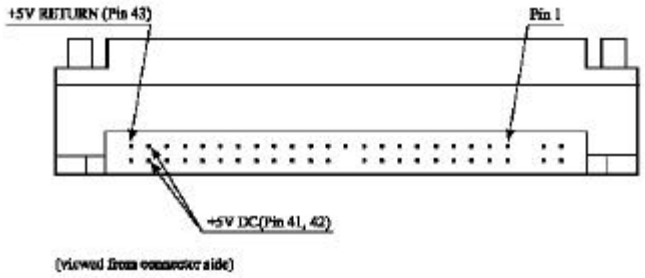
ODD CONNECTOR



HDD CONNECTOR

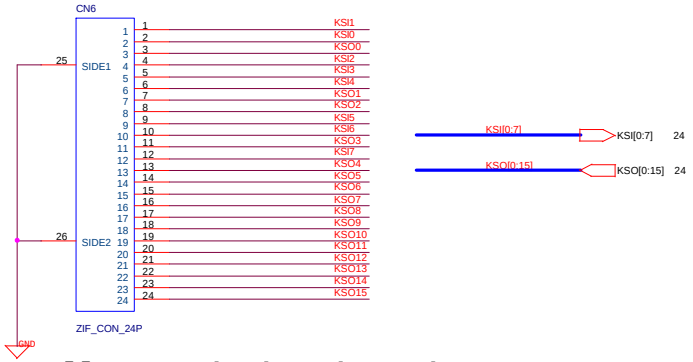






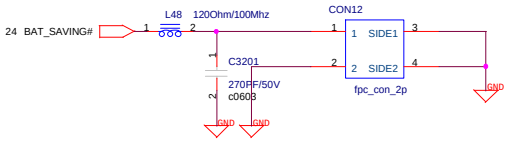
ASUSTek COMPUTER INC	Project Name	S6F	
	Engineer:	MICHAEL WANG	
Size: Custom	Title :	HDD/ODD CON.	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet	31 of 37	

KEYBOARD CONN.

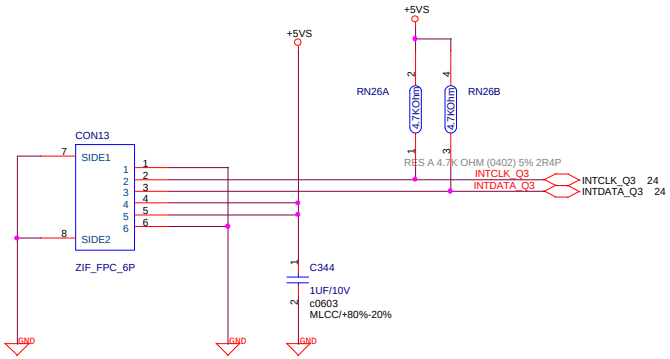


Follow J4A keyboard Matrix

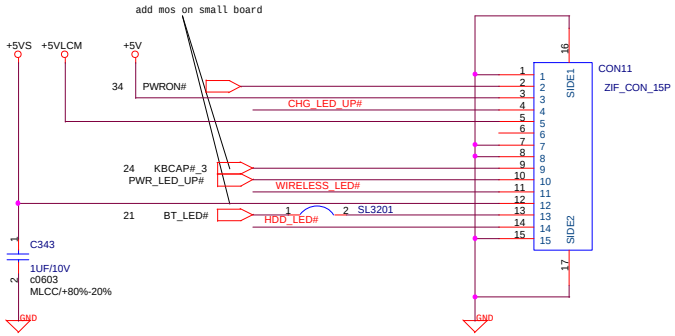
TO POWER4GEER SMALL BOARD

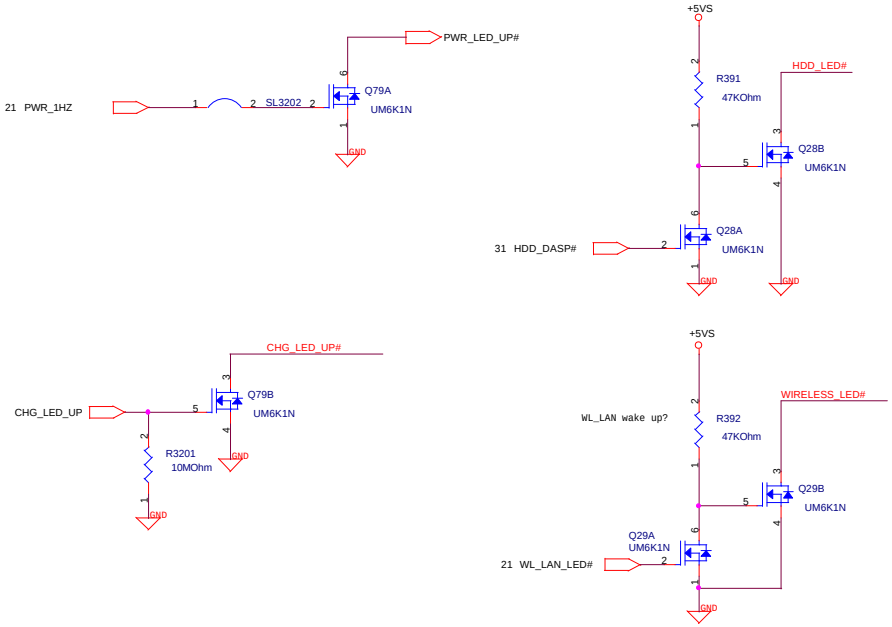


Touch PAD



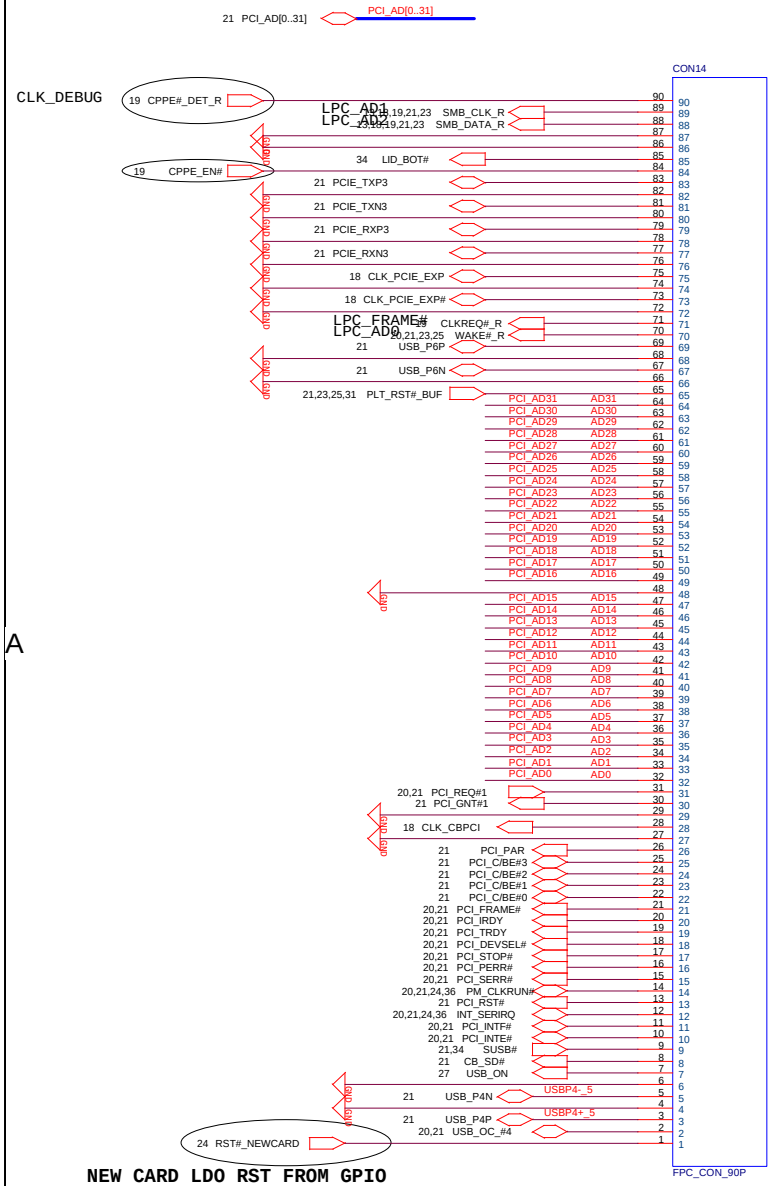
HotKey/PWRBT CON





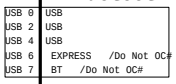
ASUSTek COMPUTER INC	Project Name: S6F	Engineer: MICHAEL WANG
Size: Custom	Title : DCIN Jack & PID & PCB_ID	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 32 of 37	

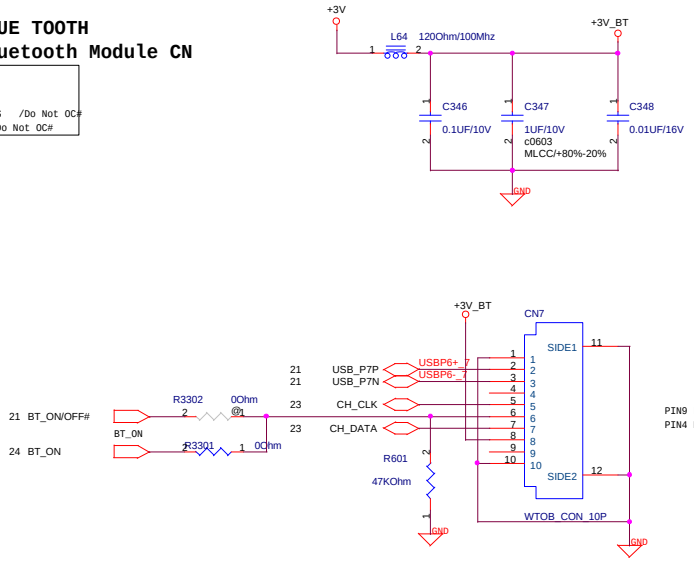
To I/O board connector (signal)



NEW CARD LDO RST FROM GPIO

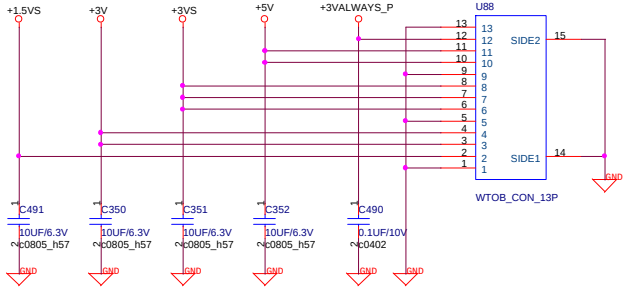
BLUE TOOTH
Bluetooth Module CN



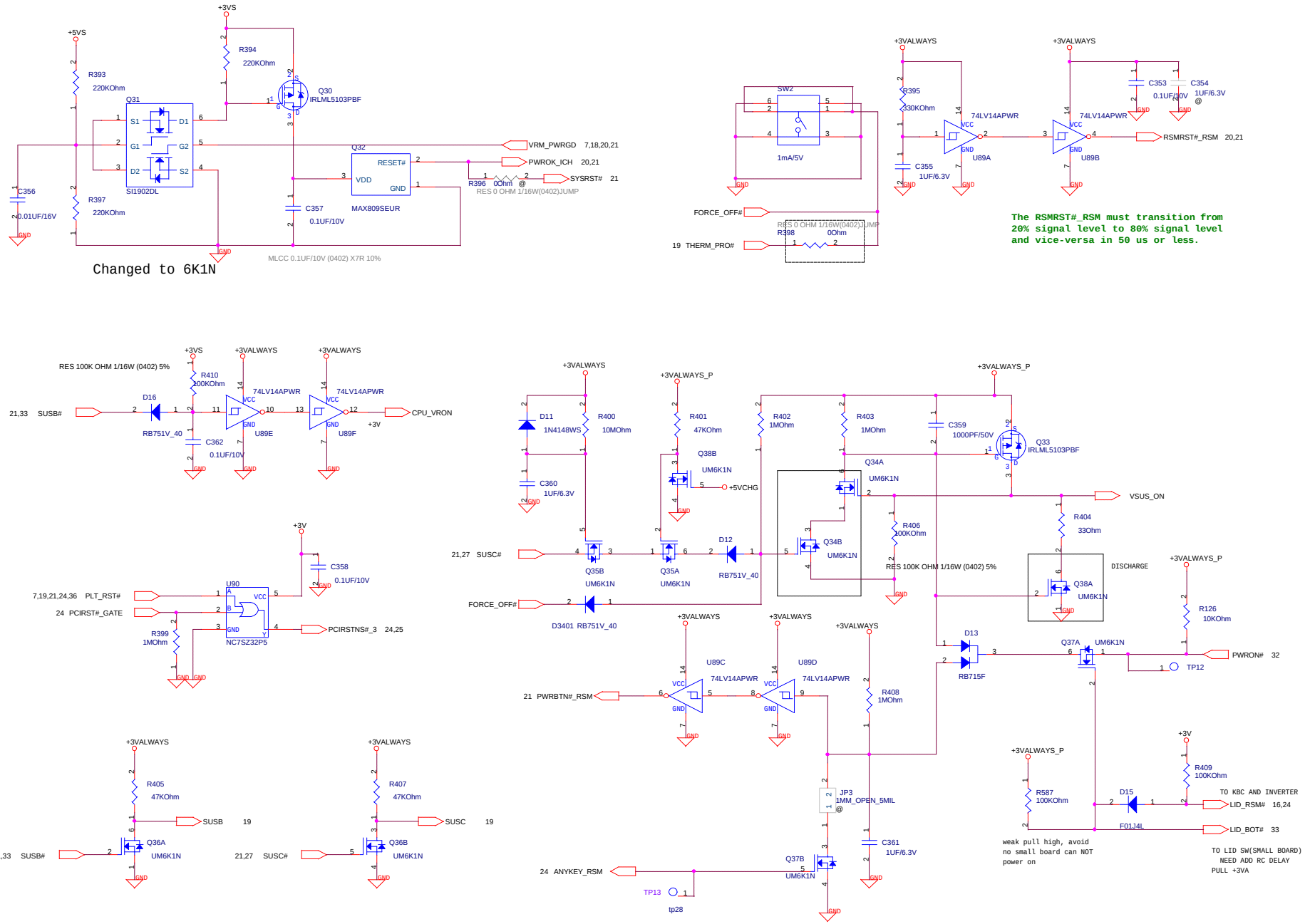


To I/O board connector (power)

Check with io baord



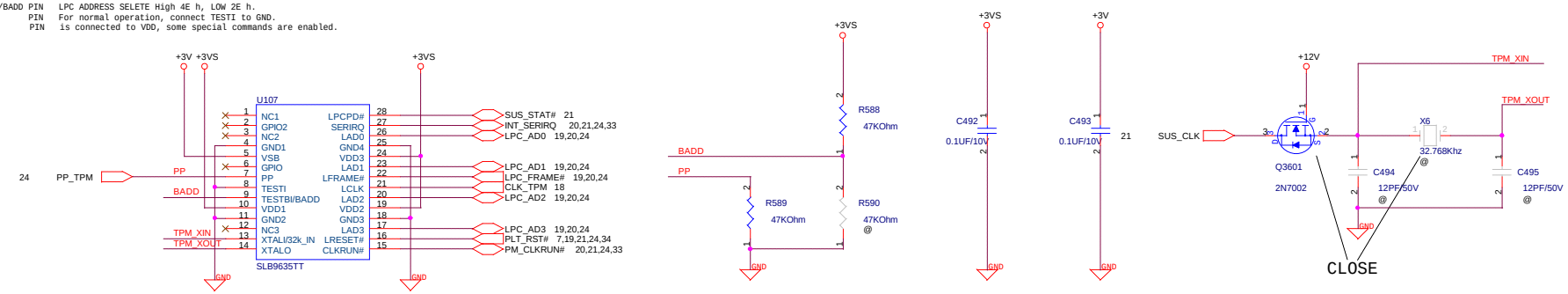
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : SMALL BOARD CON.	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 33 of 37	



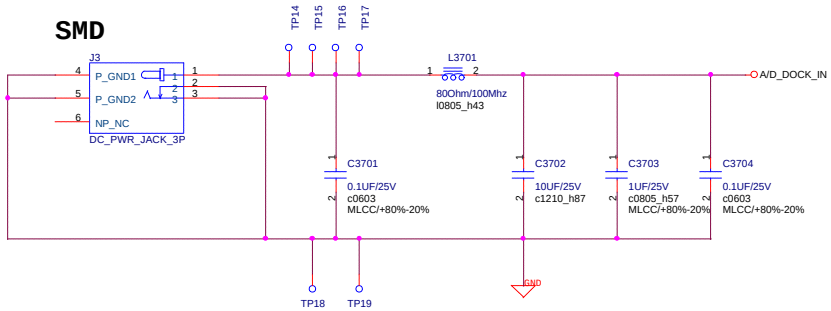
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : RESET SKT	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 34 of 37	

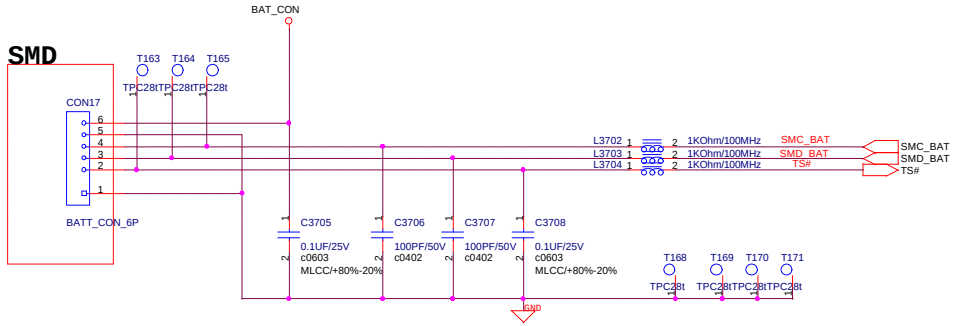
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: Eric Fang	
Size: Custom	Title : Audio DJ	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 35 of 37	

TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.



ASUSTek COMPUTER INC	Project Name	S6A	
	Engineer:	MICHAEL WANG	
Size: Custom	Title : TPM 1.2		Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 36 of 37		





ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: Custom	Title : DC IN	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 37 of 37	

Release S6F R1.0 on AUG, 2005
S6F R1.1

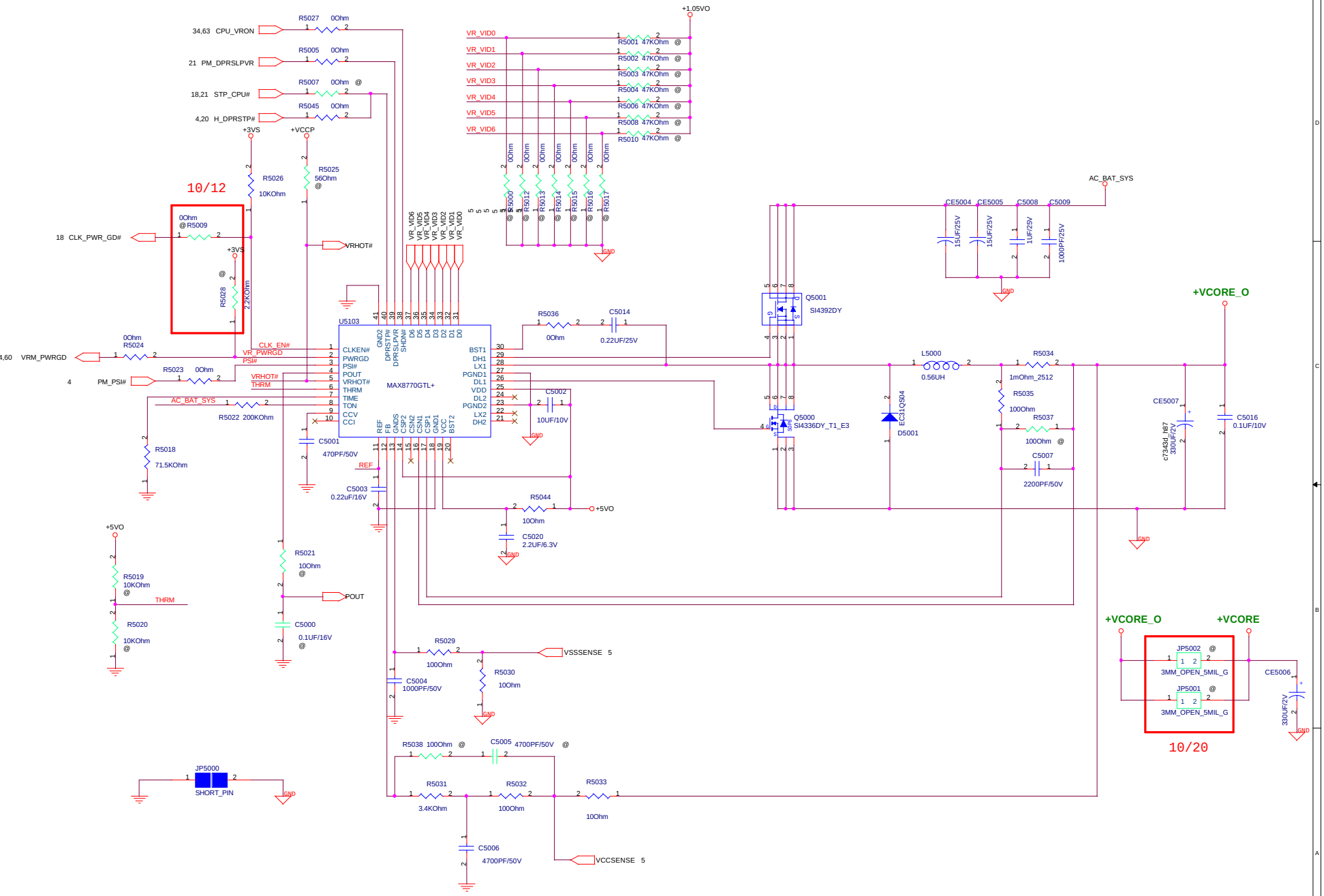
short pad footprint:
shortpin_sl

1. Delete assistance power led(for power on led delay), delete D49 D48 Q81 Q80 R591~R593 C496 and U92B in Page 36, and delete net PWRON_LED#.
2. Delete AUDIO DJ FUNCTION, delete D14 in page 34 and delete all coomponents in page 35.
   Delete net SWDJ_EN#, PWR_DJ_ON#, DJ_SCAN AND DJ_SW_BTN#.
3. In page 4, to mount R16 56 Ohm for "can not boo tissue".
4. In page 16. modify LCD discharge circuit, repleacemnet of diode by 2N7002, and we swap LCD con. pin defined for ME rotation CON 1.
5. In page 22, for +3VALWAYS leakage to +5V, we delete Q12, Q13, R299 and R300. And R297 pull high to +5VSUS.
6. In page 25, R599 pull high to +3Vs for lan con not wake-up from S3 ....
7. In page 27, we repleacemant of G5250 by G5251, u80 u81.
8. In page 31, we delete RN49 and RN50, add R124&R125.WIRE-OR IDE_PDIAG# AND IDE_SDIAG# ,WIRE-OR
   HDD_DASP# AND CDROM_DASP#, FOR HDD AND CD CAN NOT WORK AT THE SAME TIME.
9. In page 33, con13 connector changed 6pin for 15pin for remove audio DJ.
10. In page 34, add R126 and pull high +3VALWAYS_P for PWR_BTN# can not work stable.
11. In page 20&36, X2&X6 07G010313271 CM519 32.768000KDZFTR instead of ORIGINAL.(x6 OPTION)
12. Added Debug circuit for Express debug card.
13. In page 25, audio codce changed RTL660 for ADI 1986 .
14. In page 18, Added R1801 for MINICARD CLK_REQ .

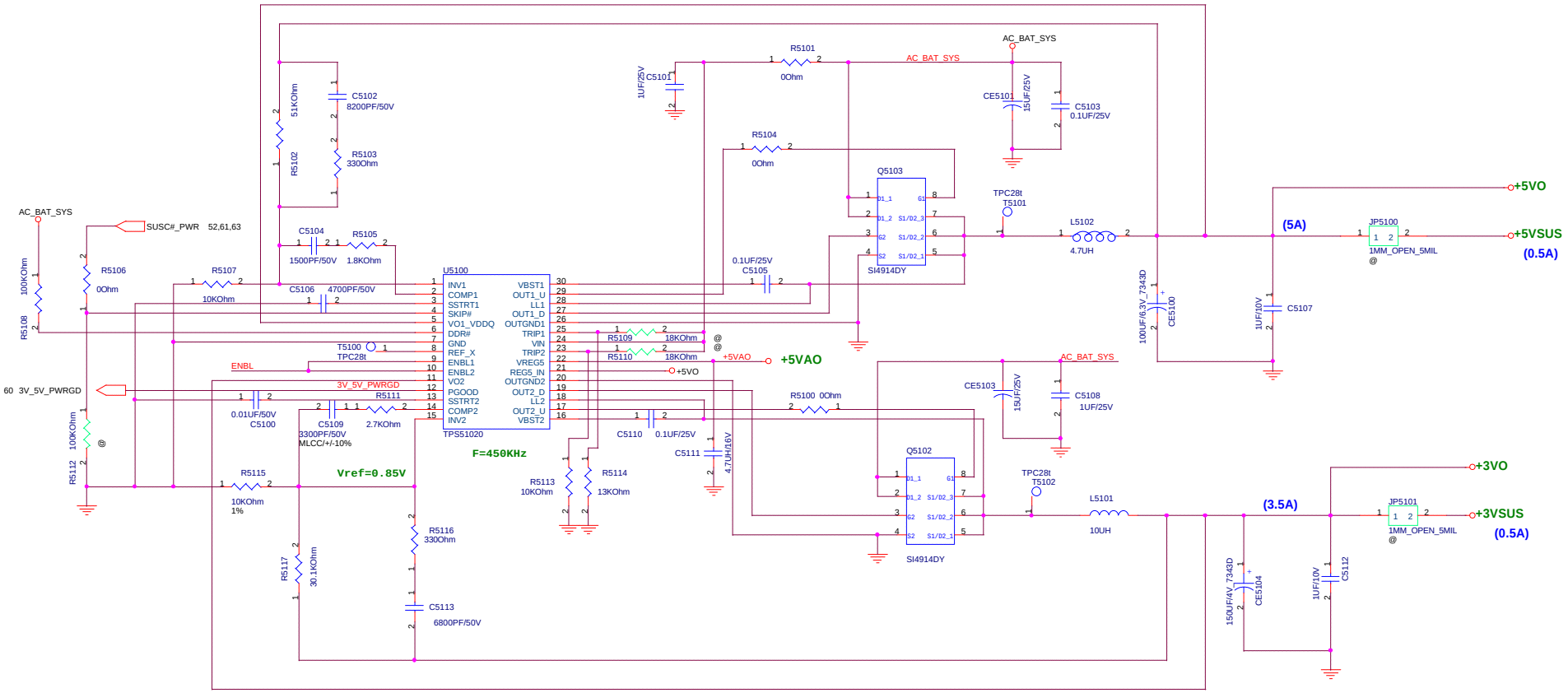
S6F R2.0

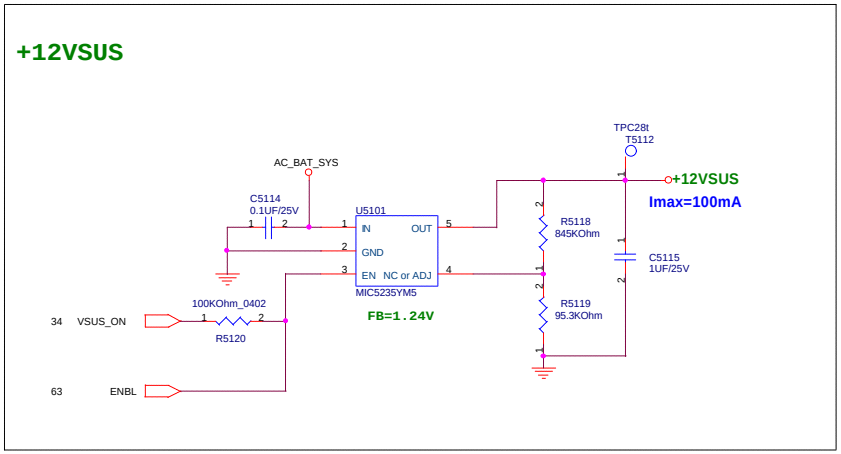
15. In Page 24, Q14 changed to 2N7002, and correct the route batsel_2p# throght Q14(nand get)to U77.35.(Not barsel_3s# to
    U77.37. U77.37 need pull down resistor R2402(1M Ohm)
16. In page 24, for S3 resume issue, reserve a BT ON route from EC(U77.22) and R3301 R3302.
    (added R3301 R3302 and net BT_on from EC)
17. In page 32&24, for deleted TP_led function, we deleted Q14B.refer item 15.
18. In page 12, added c1201 and c1202 on +1.8V.
19. In page34, reset circuit modify, R395 and C355 close to U89 and added D3401 to avoid restart itself after push reset botton.
20. In page36, added Q3601 to replease R608 to avoid +3Va(susclock) leakage to +3V.
21. In page 19&33, deleted debug citcuit of PCIE, delete ic1901, c1901 and sl3301
22. In page 26, LAN connector change ner part, and added R2601 R2602 for EMI
23. In page 37, DC_IN CON changed new part
24. In page 32, added R3201 pull low CHG_LED_UP to avoid indetermination state.
25. Update new foorprint of JP and short pad for GA process.
26. In page 32, internel speaker route replacemant of PIN 39&41 by Pin 35&36 to avoid non-pcbeep to speaker.
27, In page 16,added C1601 for EMI
28, C163 change Net into LCD_+3VS
29, N19145985 reserve 1pcs cap.

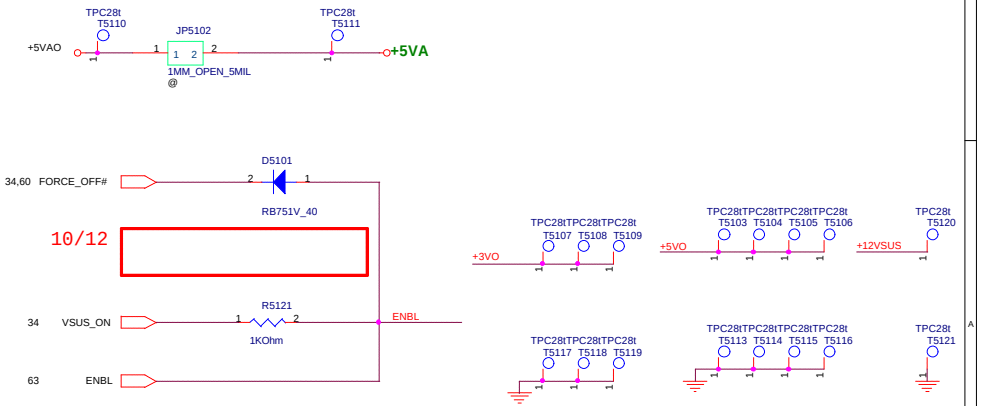
ASUSTek COMPUTER INC	Project Name: S6F	
	Engineer: MICHAEL WANG	
Size: C	Title : History	Rev: 1.0
Date: Wednesday, January 18, 2006	Sheet 38 of 37	



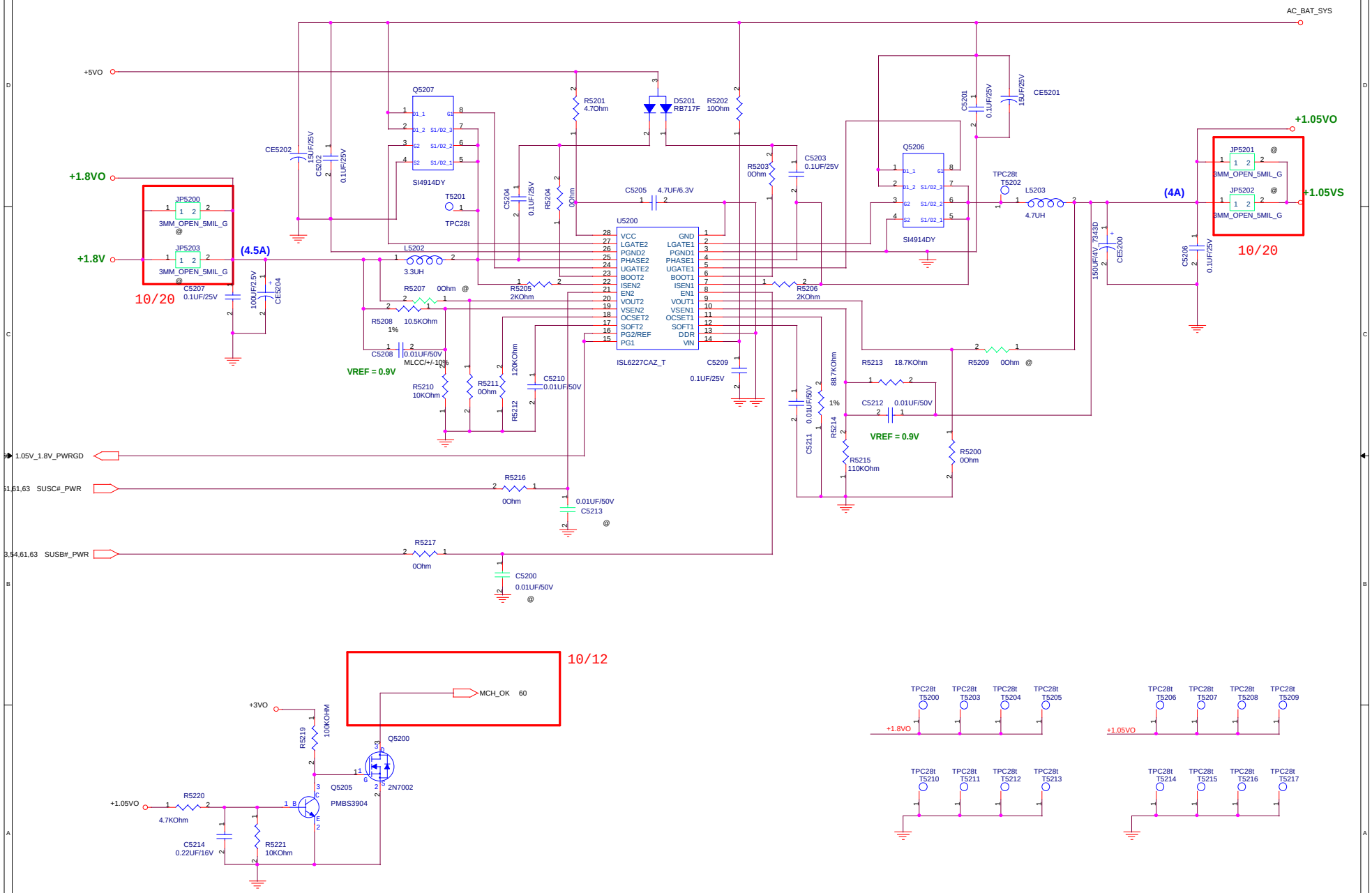
PROJECT: **S6F**	REVISION **2.0**	DATE: Wednesday, January 18, 2006	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : Vcore Power	DESIGN ENGINEER :
		SHEET **50** OF **63**		RELEASE DATE :	



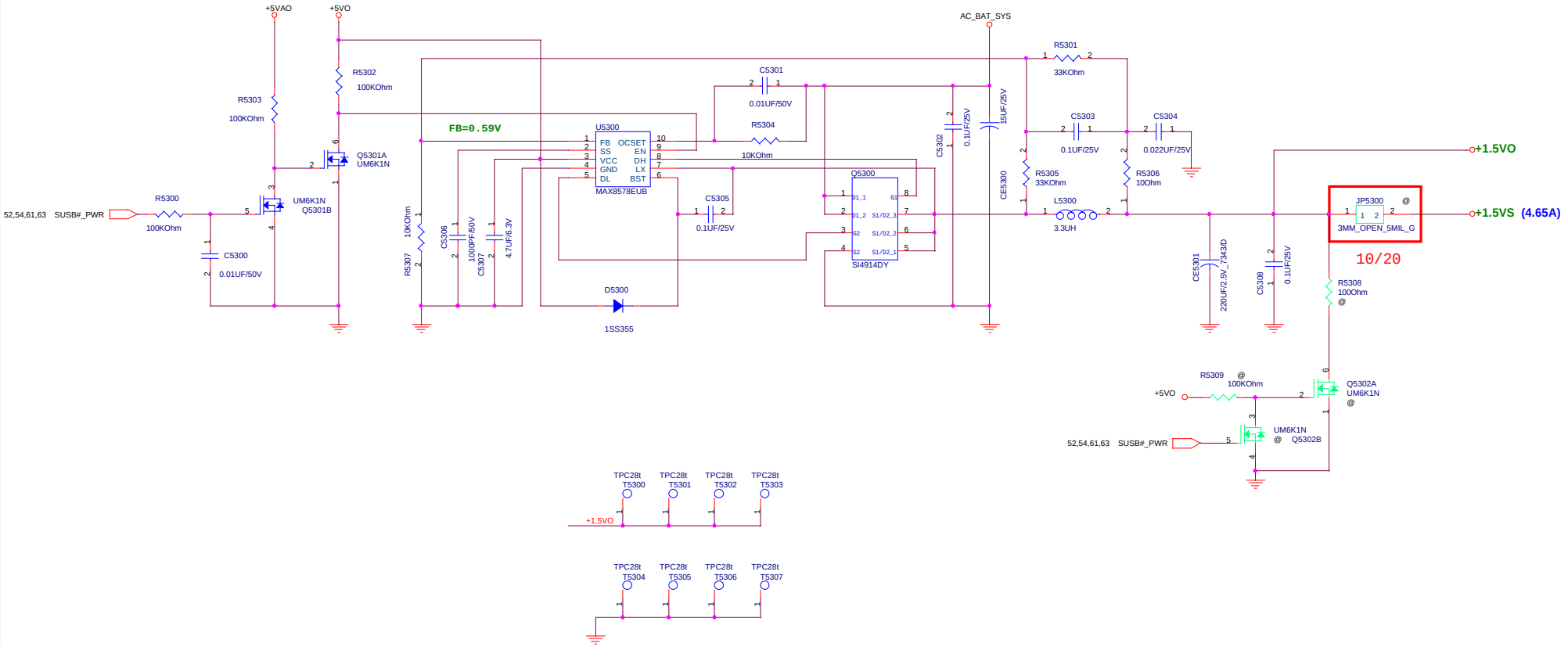




PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **System Power**	DESIGN ENGINEER :
		SHEET **51** OF **63**		RELEASE DATE :	

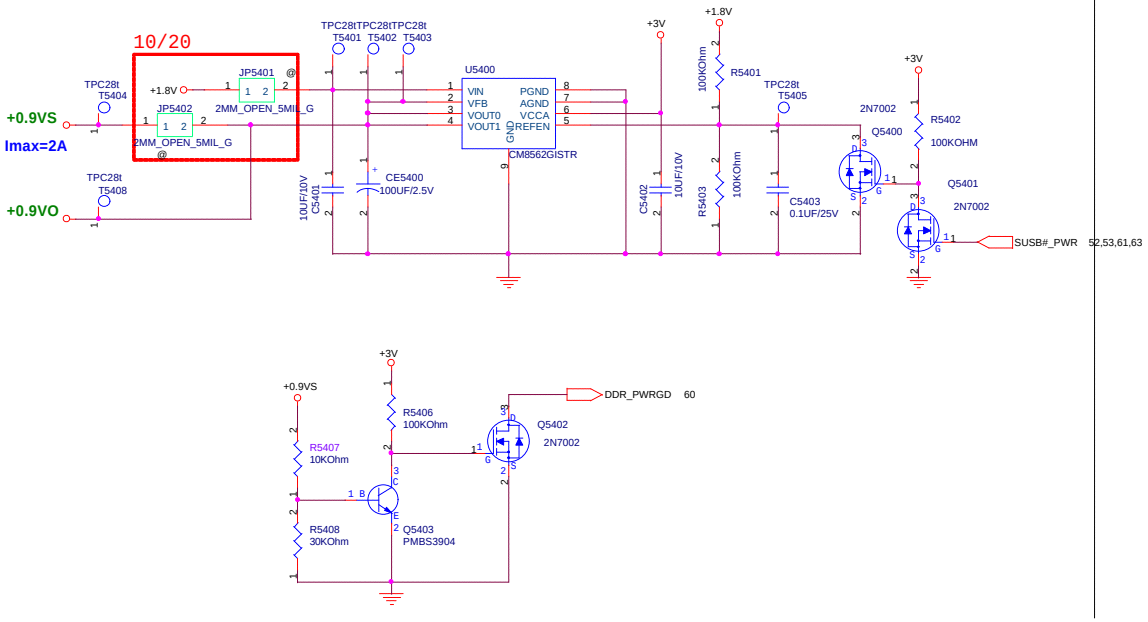


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **1.05VS & 1.5VS**	DESIGN ENGINEER :
		SHEET **52** OF **63**		RELEASE DATE :	

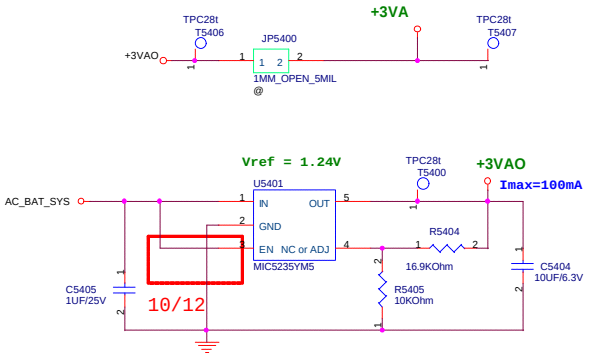


PROJECT: **S6F**	REVISION: **2.0**	DATE: Wednesday, January 18, 2006	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **1.8V & 0.9VS**	DESIGN ENGINEER :
		SHEET **53** OF **63**		RELEASE DATE :	

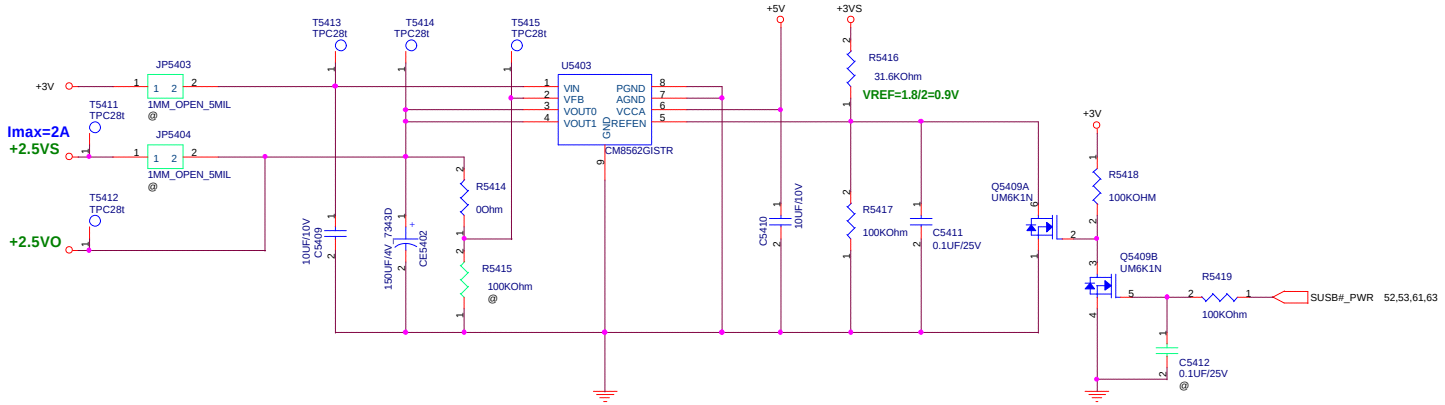
DDR-->VTT



+3VA0



+2.5VS

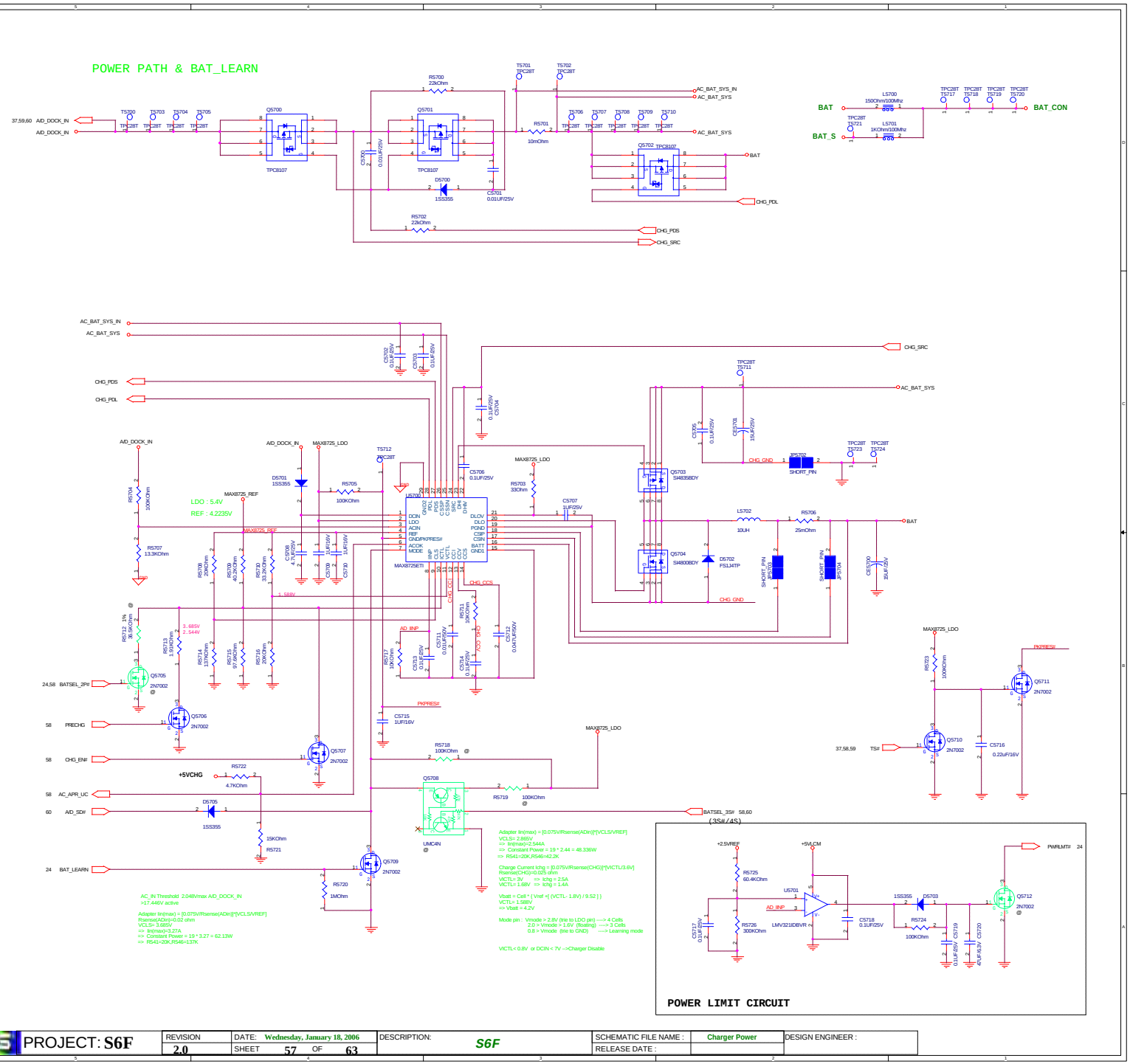


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **Oterh Power**	DESIGN ENGINEER :
		SHEET **54** OF **63**		RELEASE DATE :	

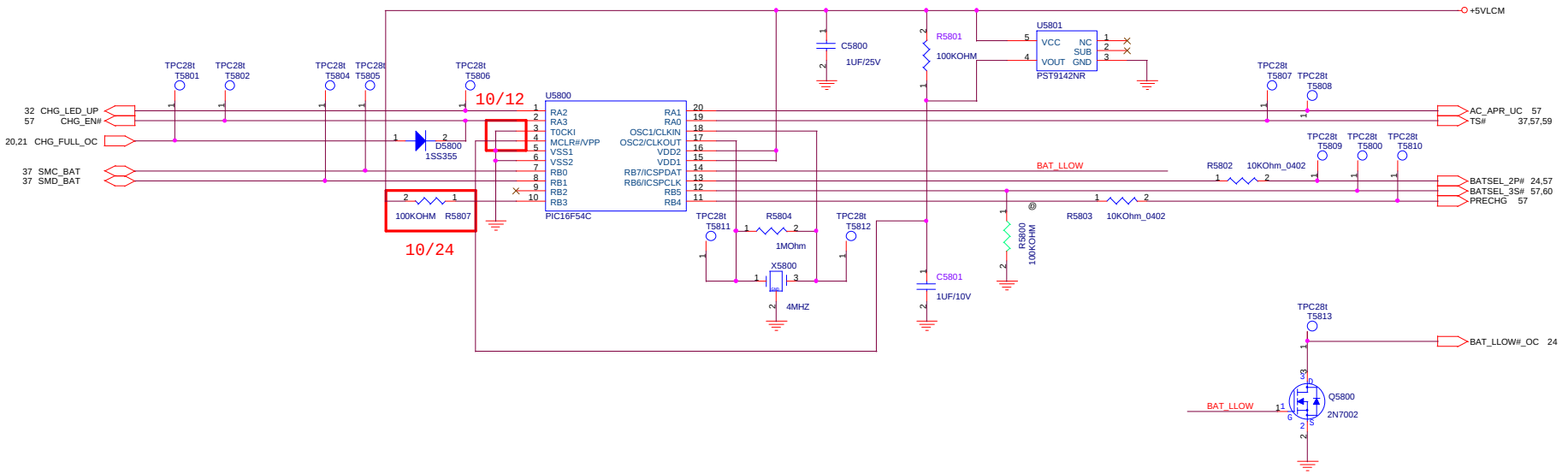
PROJECT: **S6F**

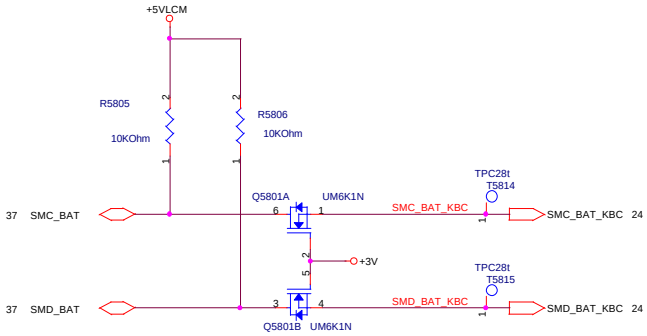
REVISION	DATE: Wednesday, January 18, 2006	DESCRIPTION:	SCHEMATIC FILE NAME :	VGA CORE	DESIGN ENGINEER :
2.0	SHEET 55 OF 63	S6F	RELEASE DATE :		

PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006** SHEET **56** OF **63**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **VGA RAM** RELEASE DATE :	DESIGN ENGINEER :



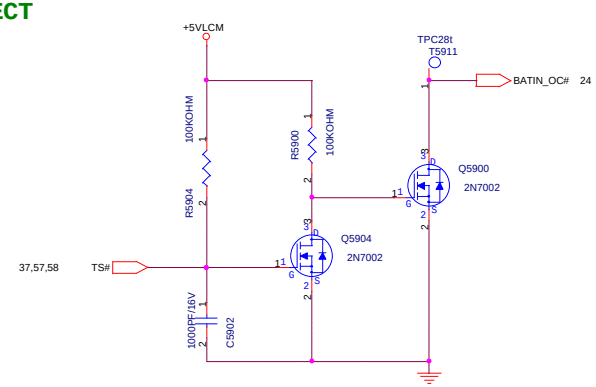
PIC16C54C



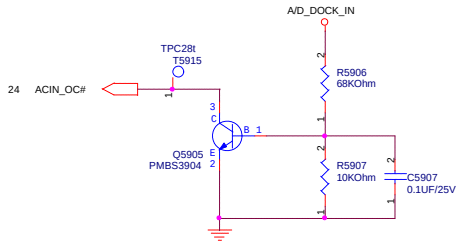


PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **PIC**	DESIGN ENGINEER :
		SHEET **58** OF **63**		RELEASE DATE :	

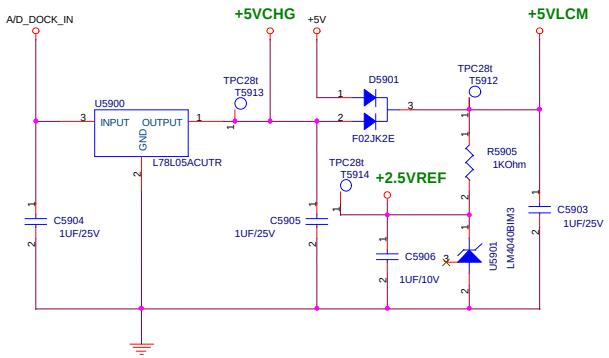
BATTERY IN DETECT



ADAPTER IN DETECT

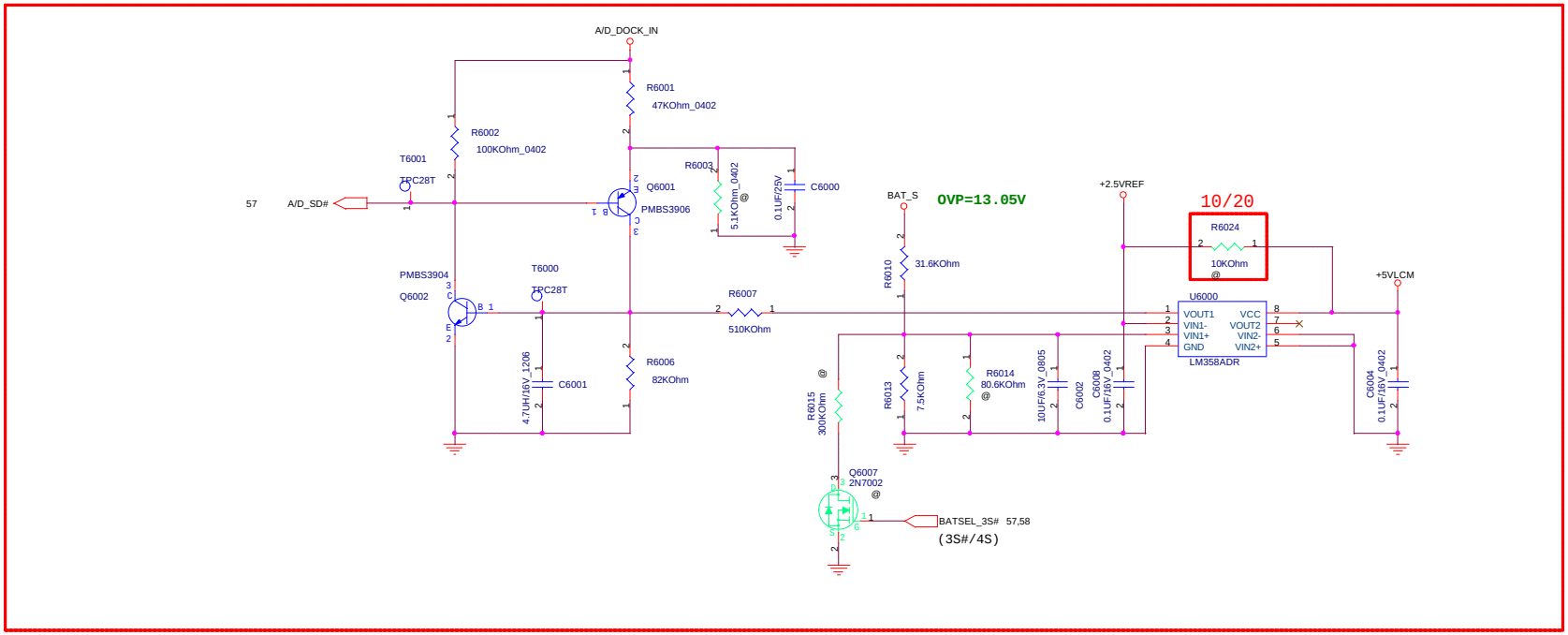


+5VLCM, +5VCHG & +2.5VREF

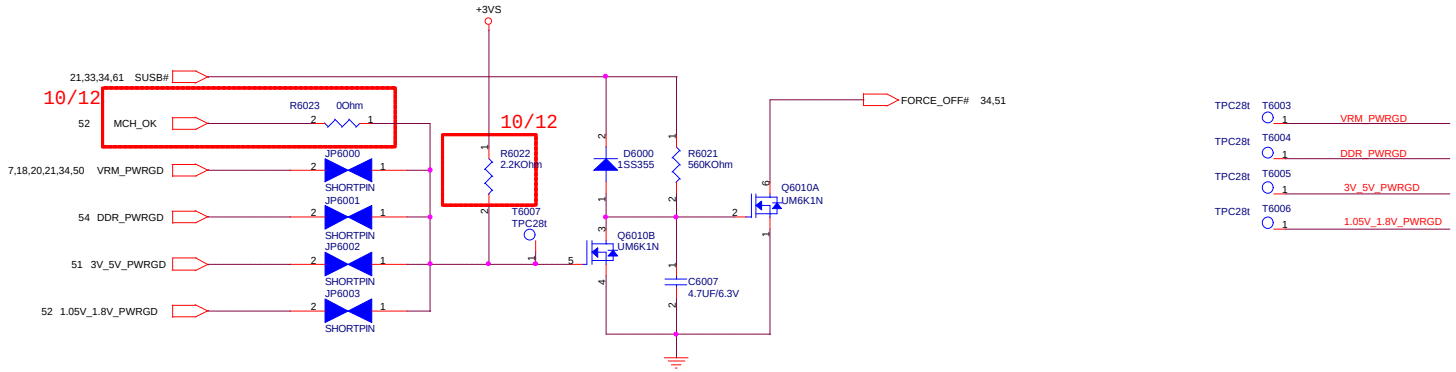


PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME : Selector	DESIGN ENGINEER :
		SHEET 59 OF 63		RELEASE DATE :	

BATTERY A/D_SD# (OVP)

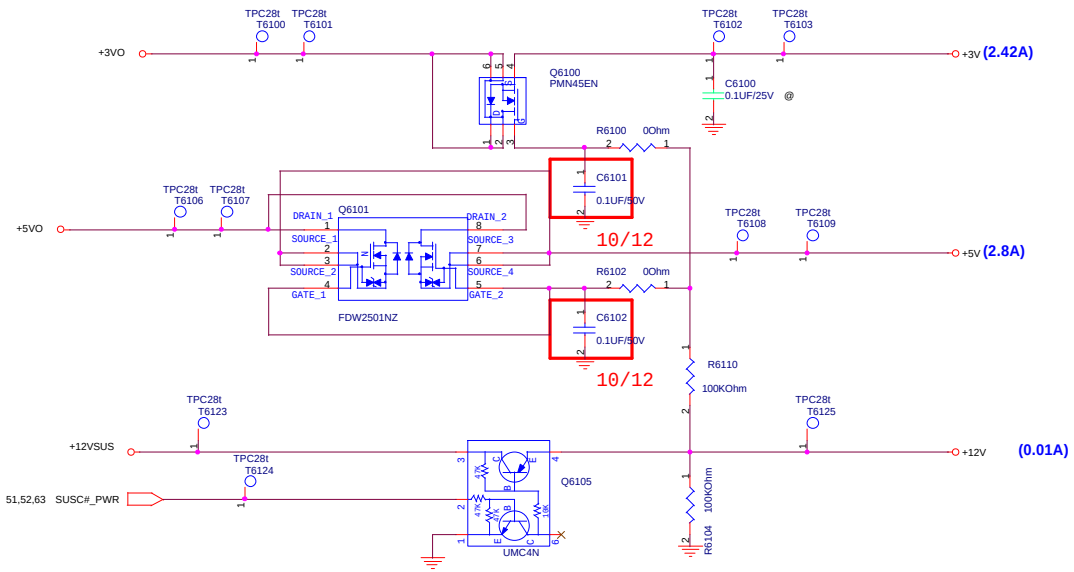


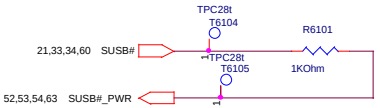
POWER GOOD DETECTER



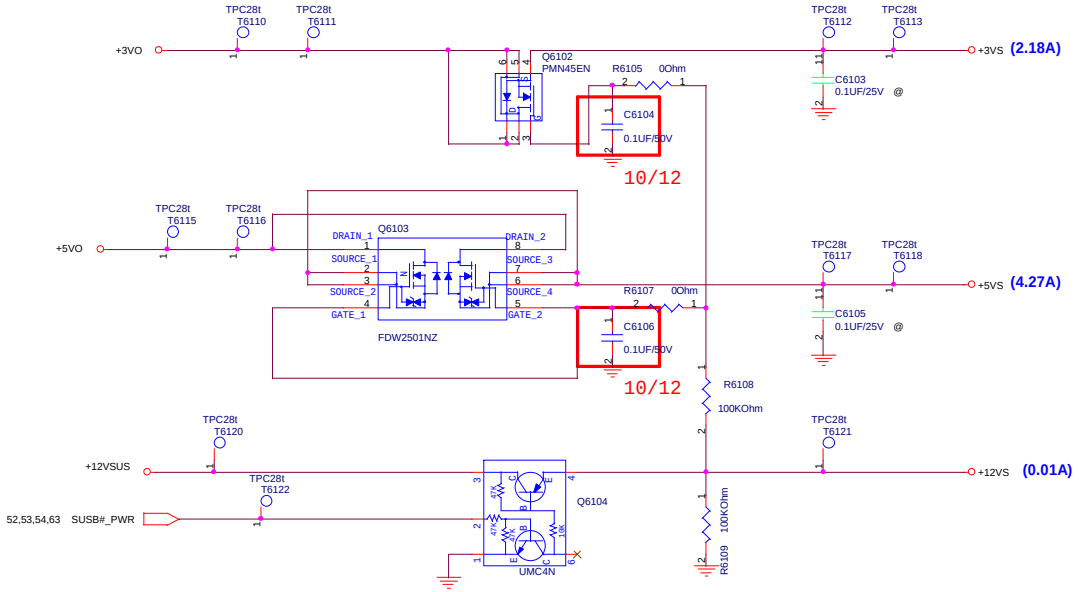
PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME :	BATLOW/SD#	DESIGN ENGINEER :
		SHEET 60 OF 63		RELEASE DATE :		

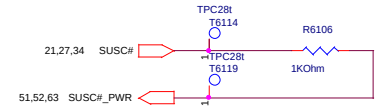
SUSC#_PWR POWER



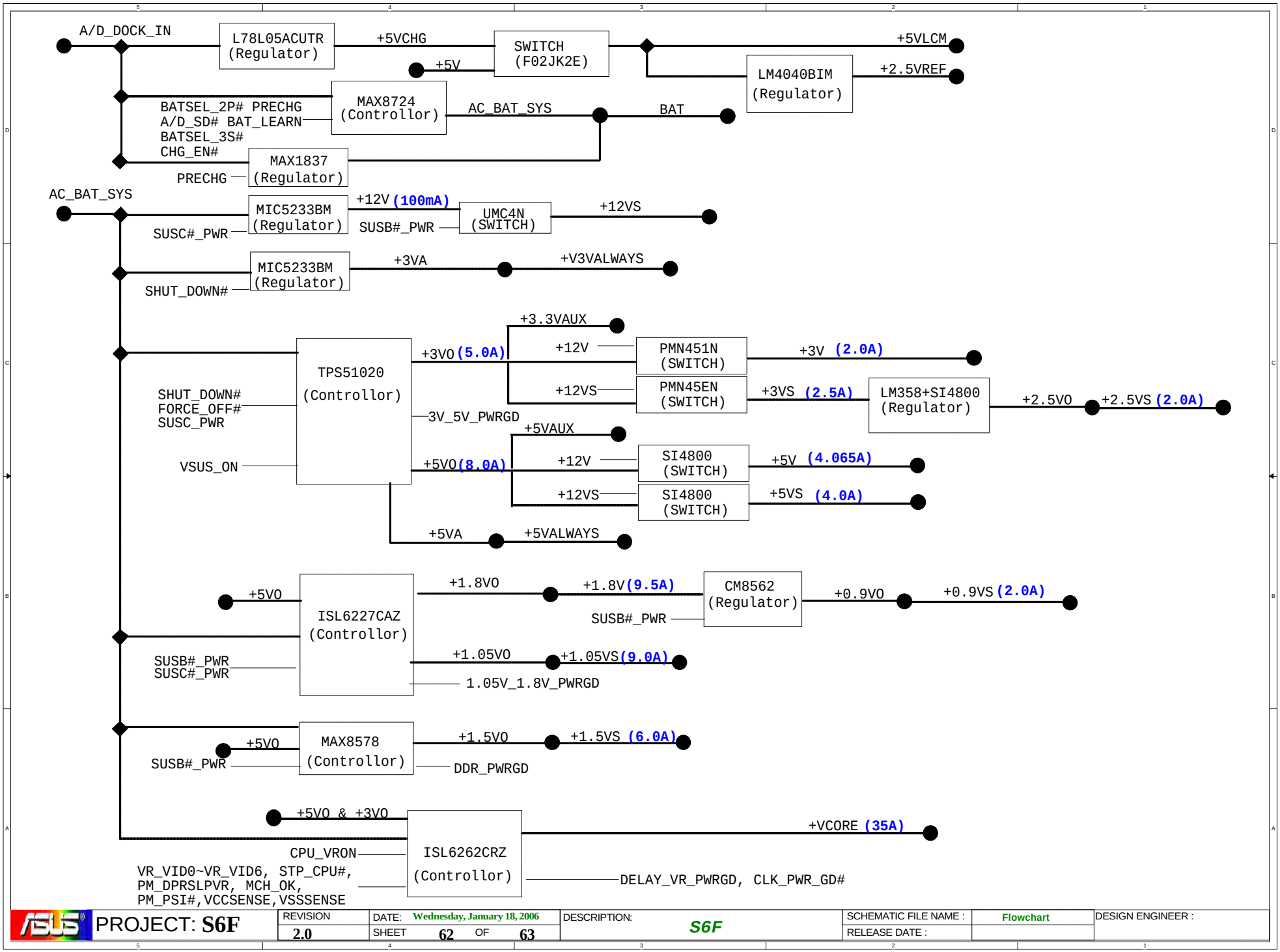


SUSB#_PWR POWER



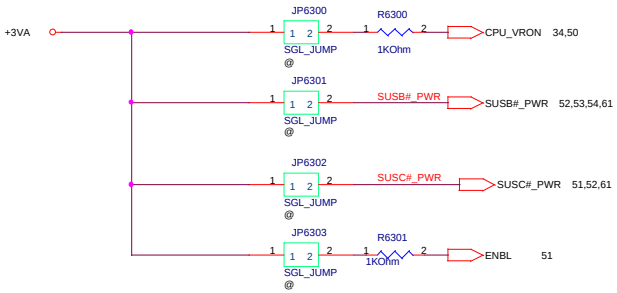


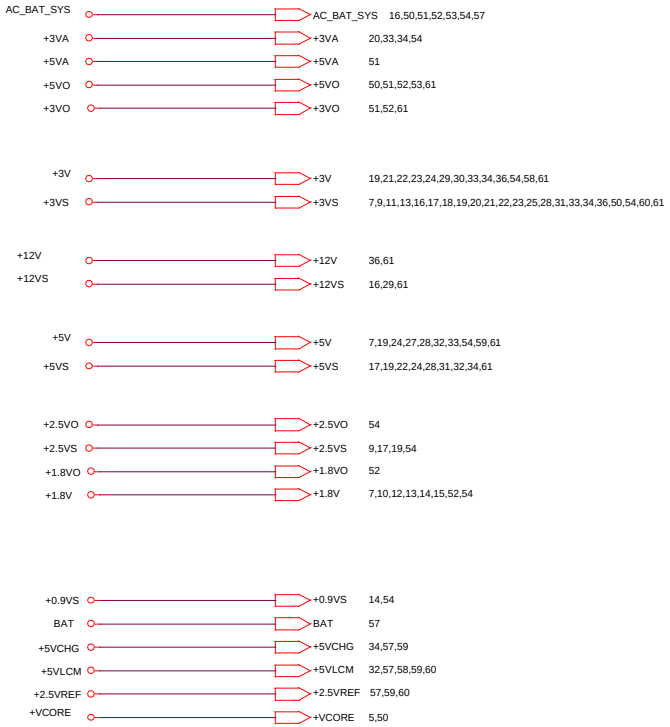
PROJECT: S6F	REVISION 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME :	LOAD SWITCH	DESIGN ENGINEER :
		SHEET 61 OF 63		RELEASE DATE :		



PROJECT: S6F	REVISION: 2.0	DATE: Wednesday, January 18, 2006	DESCRIPTION: S6F	SCHEMATIC FILE NAME : Flowchart	DESIGN ENGINEER :
		SHEET 62 OF 63		RELEASE DATE :	

FOR POWER TEST





PROJECT: **S6F**	REVISION **2.0**	DATE: **Wednesday, January 18, 2006**	DESCRIPTION: ***S6F***	SCHEMATIC FILE NAME : **SIGNAL**	DESIGN ENGINEER :
		SHEET **63** OF **63**		RELEASE DATE :	