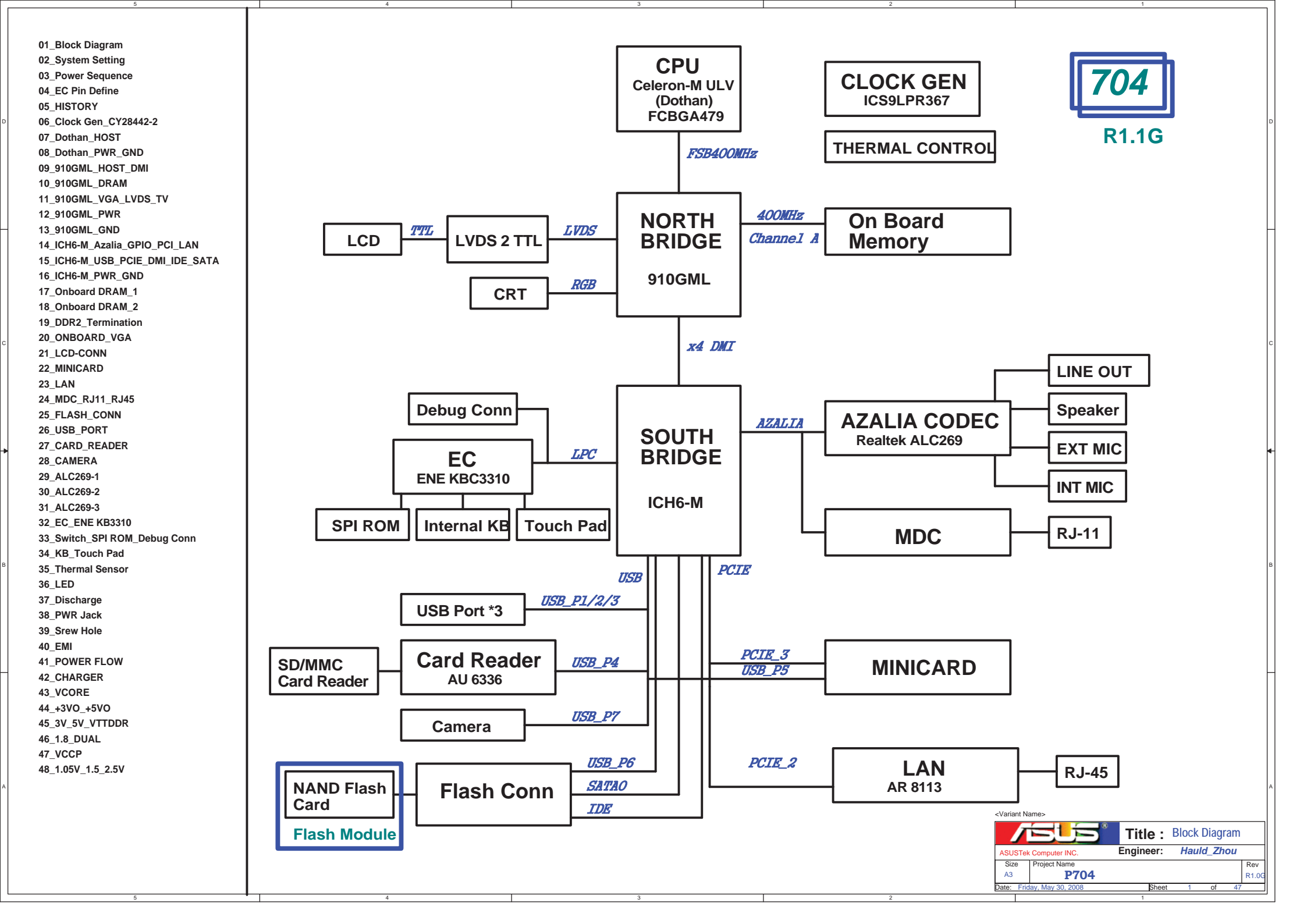


- 
- The diagram illustrates the system architecture of the ASUS P704. At the top, the CPU (Celeron-M ULV, Dothan, FCBGA479) is connected to the North Bridge (910GML) via FSB400MHz. The North Bridge is also connected to On Board Memory (400MHz, Channel A) and the South Bridge (ICH6-M) via x4 DMI. The South Bridge manages various peripherals: it connects to the EC (ENE KBC3310) via LPC, which in turn controls the SPI ROM, Internal KB, and Touch Pad. It also manages the Debug Conn, USB Port \*3 (via USB\_P1/2/3), Card Reader (AU 6336, via USB\_P4), Camera (via USB\_P7), and Flash Conn (via USB\_P6, SATA0, and IDE). The South Bridge is connected to the AZALIA CODEC (Realtek ALC269) via AZALIA, which handles LINE OUT, Speaker, EXT MIC, and INT MIC. It also connects to the MDC (via RJ-11) and the MINICARD (via PCIE\_3 and USB\_P5). The LAN (AR 8113) is connected to the South Bridge via PCIE\_2 and to an RJ-45 port. The system is powered by a CLOCK GEN (ICS9LPR367) and includes THERMAL CONTROL. A NAND Flash Card is highlighted as the Flash Module. The diagram is titled '704 R1.1G'.
- 01\_Block Diagram  
02\_System Setting  
03\_Power Sequence  
04\_EC Pin Define  
05\_HISTORY  
06\_Clock Gen\_CY28442-2  
07\_Dothan\_HOST  
08\_Dothan\_PWR\_GND  
09\_910GML\_HOST\_DMI  
10\_910GML\_DRAM  
11\_910GML\_VGA\_LVDS\_TV  
12\_910GML\_PWR  
13\_910GML\_GND  
14\_ICH6-M\_Azalia\_GPIO\_PCI\_LAN  
15\_ICH6-M\_USB\_PCIE\_DMI\_IDE\_SATA  
16\_ICH6-M\_PWR\_GND  
17\_Onboard DRAM\_1  
18\_Onboard DRAM\_2  
19\_DDR2\_Termination  
20\_ONBOARD\_VGA  
21\_LCD-CONN  
22\_MINICARD  
23\_LAN  
24\_MDC\_RJ11\_RJ45  
25\_FLASH\_CONN  
26\_USB\_PORT  
27\_CARD\_READER  
28\_CAMERA  
29\_ALC269-1  
30\_ALC269-2  
31\_ALC269-3  
32\_EC\_ENE KB3310  
33\_Switch\_SPI ROM\_Debug Conn  
34\_KB\_Touch Pad  
35\_Thermal Sensor  
36\_LED  
37\_Discharge  
38\_PWR Jack  
39\_Srew Hole  
40\_EMI  
41\_POWER FLOW  
42\_CHARGER  
43\_VCORE  
44\_+3VO\_+5VO  
45\_3V\_5V\_VTTDDR  
46\_1.8\_DUAL  
47\_VCCP  
48\_1.05V\_1.5\_2.5V
- ASUS® Title : Block Diagram  
ASUSTek Computer INC. Engineer: Hauld\_Zhou  
Size Project Name Rev  
A3 P704 R1.0G  
Date: Friday, May 30, 2008 Sheet 1 of 47




## ICH6 GPIO SETTING

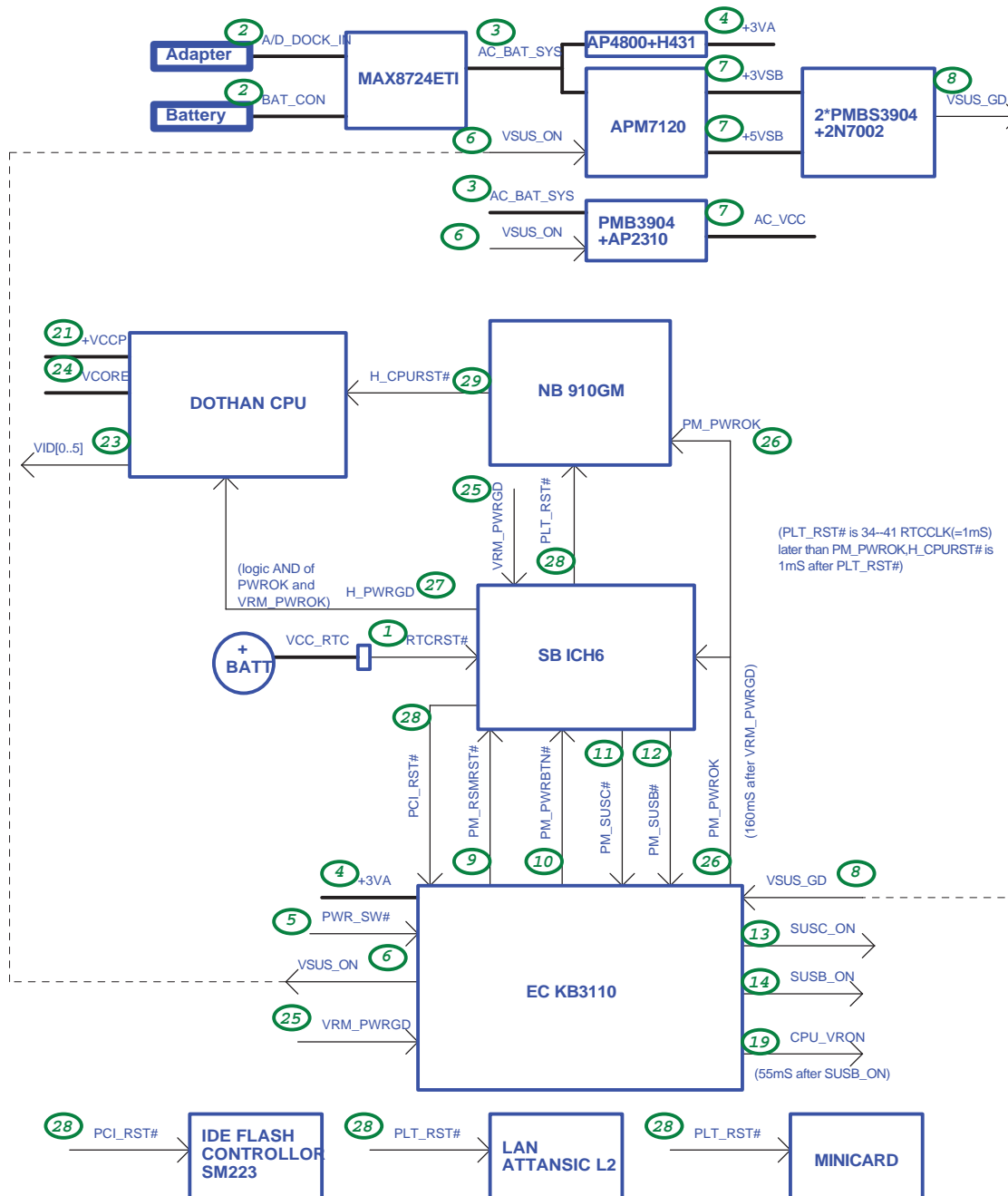
Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPIO/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GP11 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GP12 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GP13 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GP14 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GP15 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GP16 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GP17	NC	GPI	fixed as Input only
R1	GP18	EC KBC_SCI#	GPI	fixed as Input only
C23	GP19/OC4#	10K Pull +3V	I	Input
D23	GP110/OC5#	10K Pull +3V	I	Input
W6	GP111 / SMBALERT#	10K Pull +3V	I	Input
M2	GP112	NC	GPI	fixed as Input only
R6	GP113	EC EXTSMI#	GPI	fixed as Input only
C25	GP114/OC6#	10K Pull +3V	I	Input
C24	GP115/OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PC#	Clock GEN STP_PC#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	NC	GPO	fixed as Output only
NA	GPIO22	NA	NA	NA
AD21	GPO23	NC	GPO	fixed as Output only
V3	GPIO24	WLAN	I/O	Output
P5	GPIO25	NC	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GP126/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	NC	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GP129 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GP130 / SATA2GP	NC	GPI	(GPI)Input
AG18	GP131 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	NC	I/O	Output
AC18	GPIO34	NC	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GP140 / REQ4#	10K Pull +3V	I	Input
P4	GP141 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 / GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

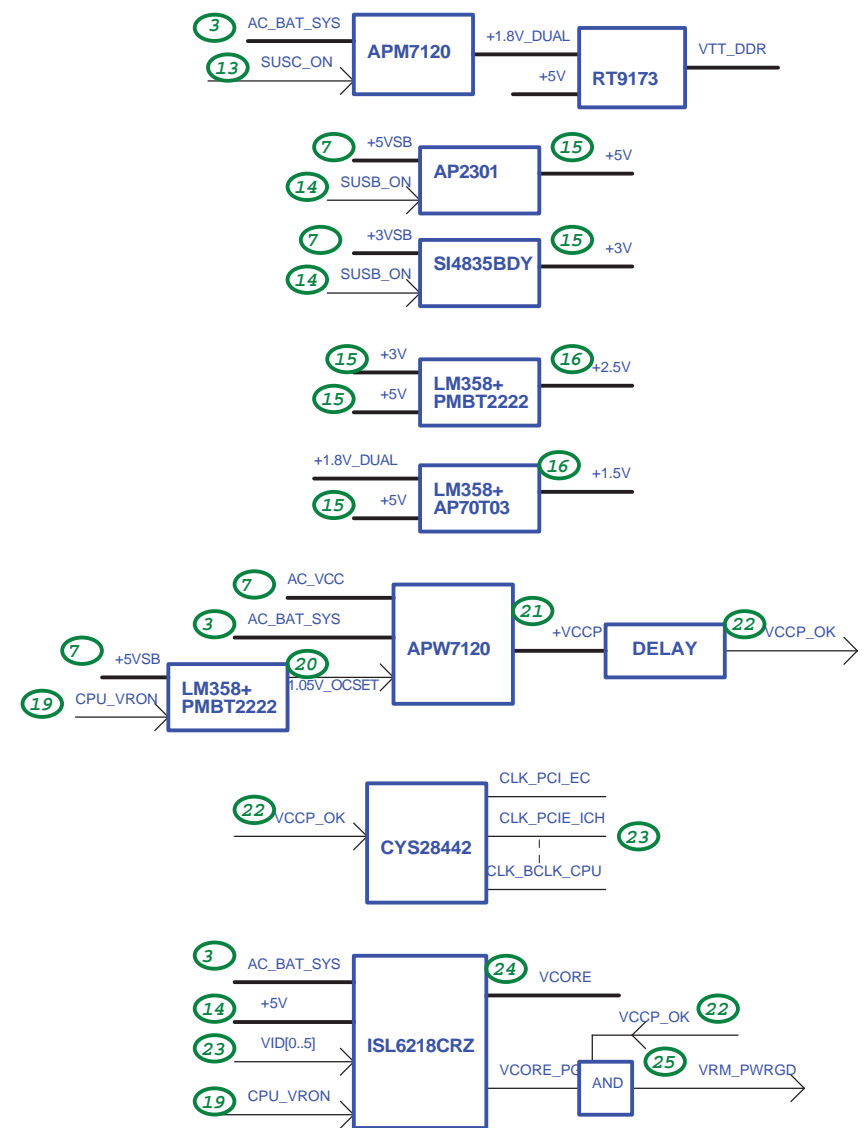
<Variant Name>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	P704		R1.0G
Date: Friday, May 30, 2008		Sheet	2 of 47

\*This sequence is for Battery Plug-in and no Adapter,  
if Adapter Plug-in,the sequence change to:  
A/D\_DOCK\_IN-->AC\_BAT\_SYS-->+3VA-->VSUS\_ON-->+3VSB & +5VSB  
-->VSUS\_GD-->PM\_REMRST#-->PWR\_SW#-->PM\_PWRBTN-->PM\_SUSC#-->PM\_SUSB#



	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL



## EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	CTRL_CAMER_PWR	I	Default : High
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	N.C	O	Reserved
15	GPIO08	EXTSMH#	O	EXTSMH#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	LCD_CSB	O	LCD chip select
18	GPIO0C	LCD_SDA	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SC#	KBC_SC#	O	KBC_SC#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	LCD_SCL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB,*
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	N.C	O	Reserved
32	GPIO18	PWR_SW#	I	power button,*
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	CTRL_Mincard_PWR	O	Default : High
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	P_PMON_10	I	Sense Power Loading
64	AD1	BAT_IN	I	sense Battery
65	AD2	N.C	I	Reserved
66	AD3	N.C	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen

Pin No.	Pin Name	Signal Name	Type	NOTE
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSERVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB0_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB0_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB1_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB1_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	N.C	O	Reserved
84	PSDAT1	N.C	O	Reserved
85	PSCLK2	N.C	O	Reserved
86	PSDAT2	N.C	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series, Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CTRL_L2_PWR	O	Default : High
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	*HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH8_PWROK	O	
103	GPXOA06	N.C	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel, Hi:1P, Lo:2P-3P
110	GPXID1	N.C	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is Pull Down 100K ohm to GND
114	GPXID3	SUSB#	I	
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	N.C	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

## EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	


<Variant Name>

		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name P704	Rev R1.0G	
Date: Friday, May 30, 2008		Sheet	4 of 47

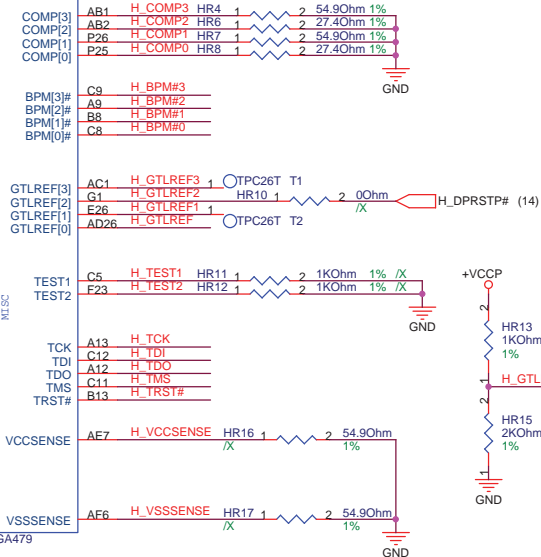
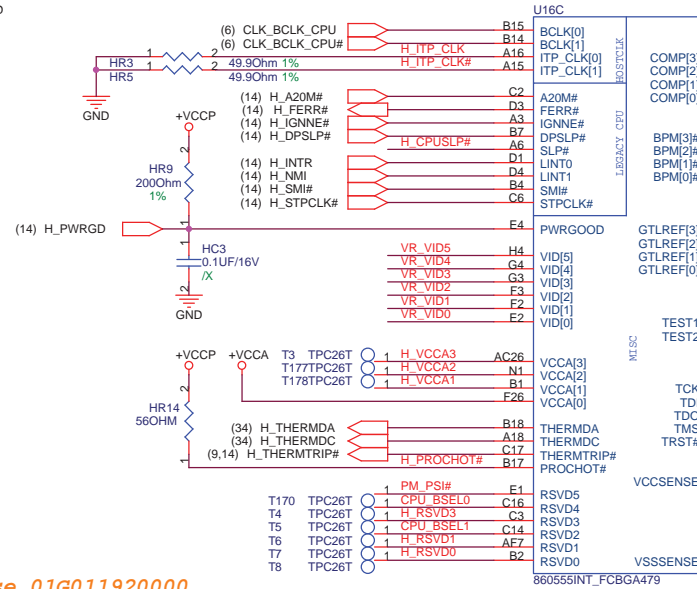
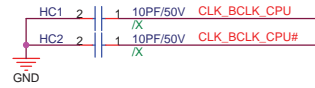
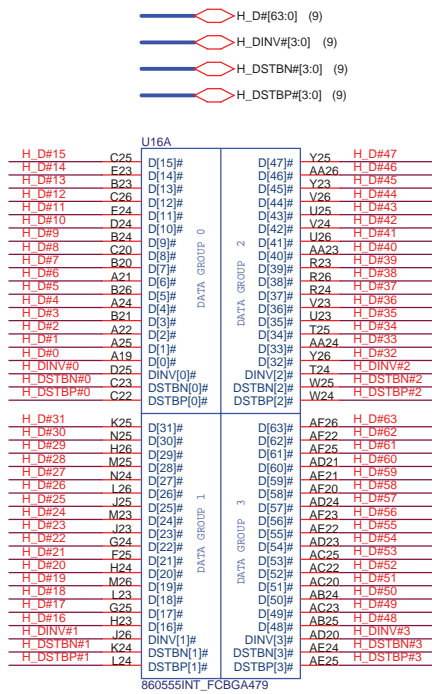
### CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.0G		P704 Schematic 1.0G Beginning

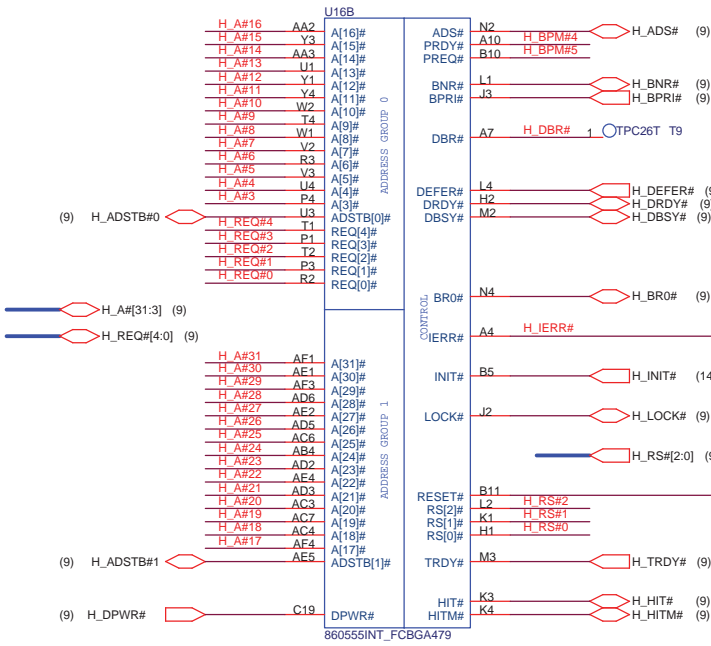
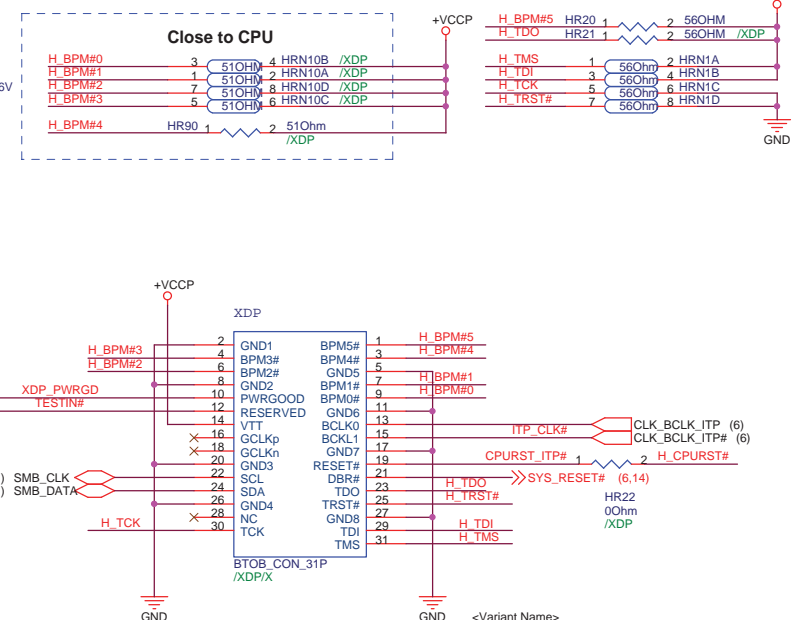
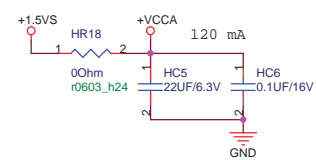
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		Title : History	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name <b>P704</b>	Rev R1.0G	
Date: Friday, May 30, 2008		Sheet	5 of 47

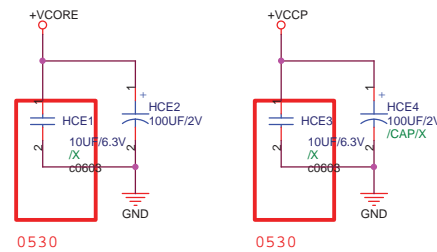
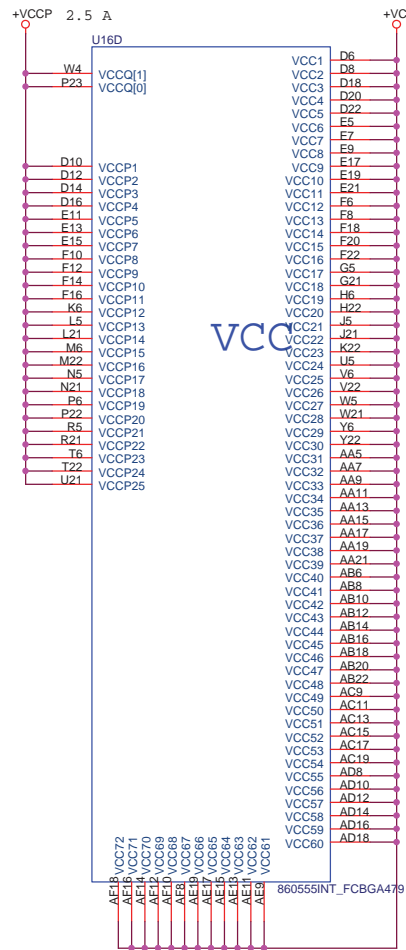




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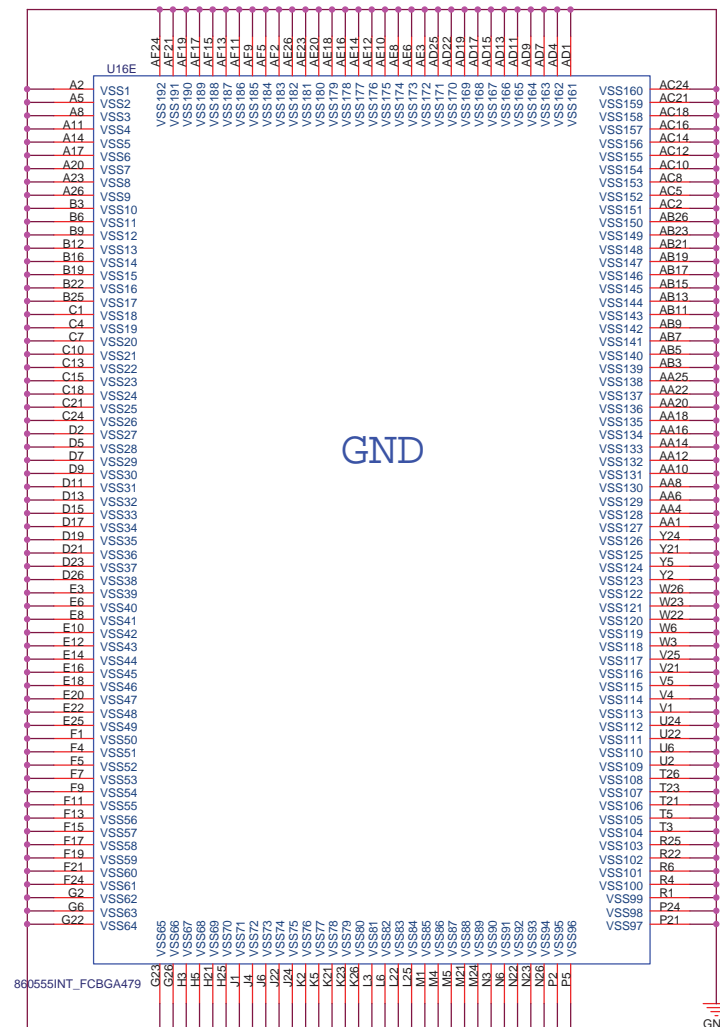
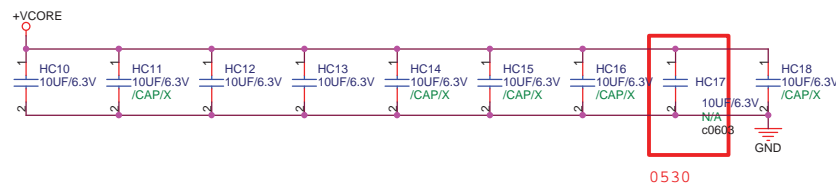
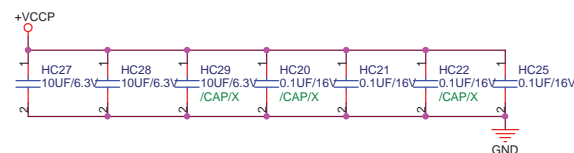
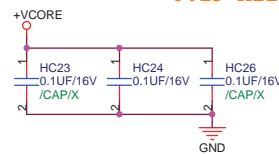




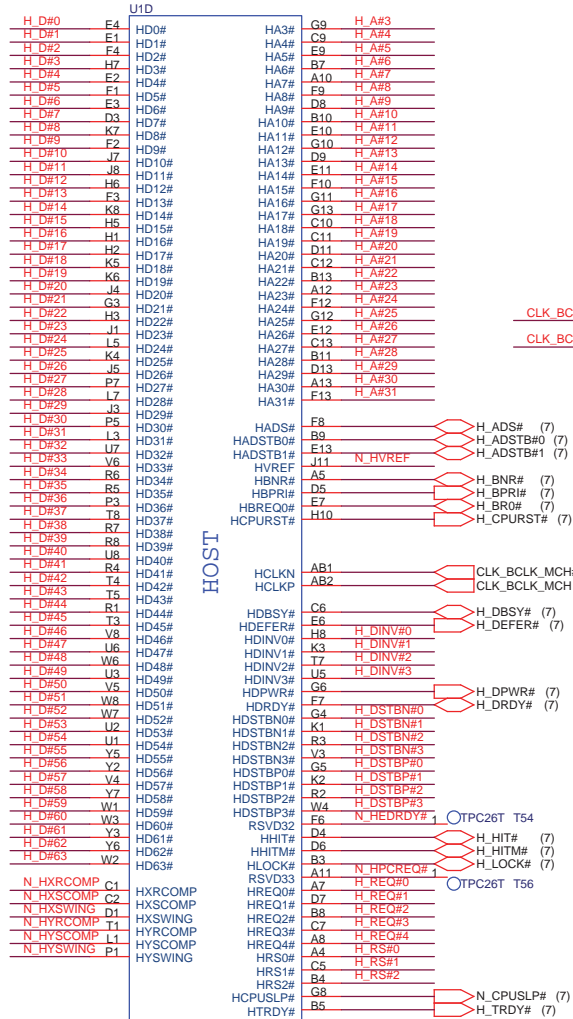
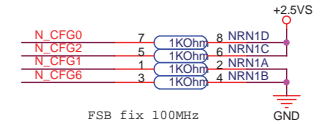


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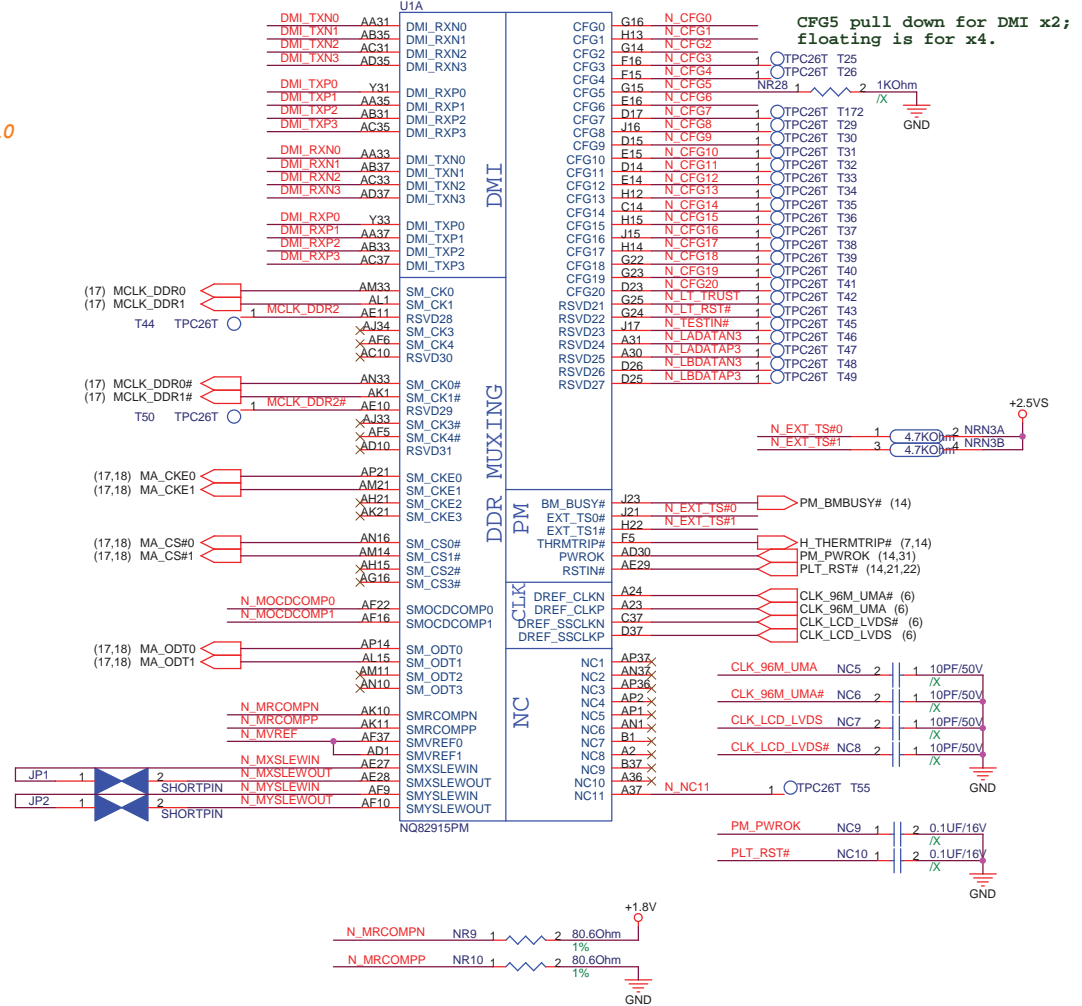
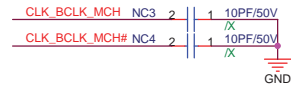
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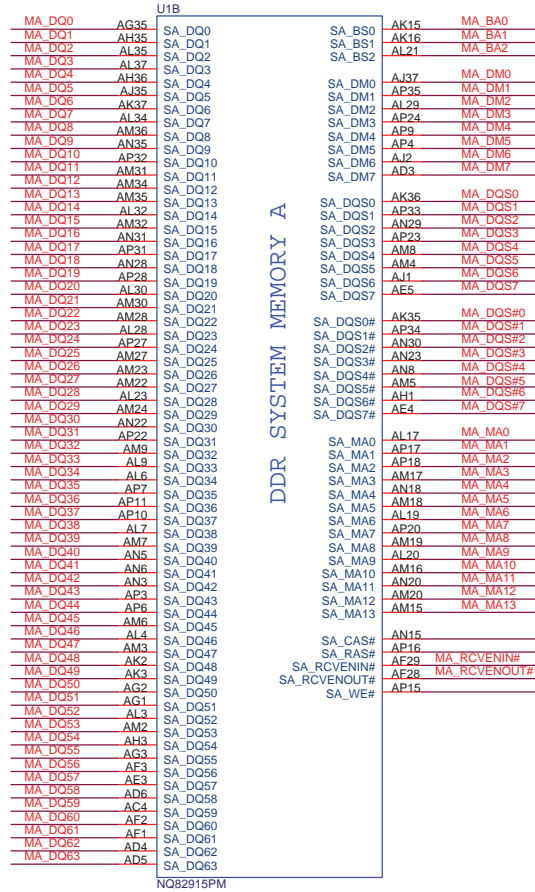


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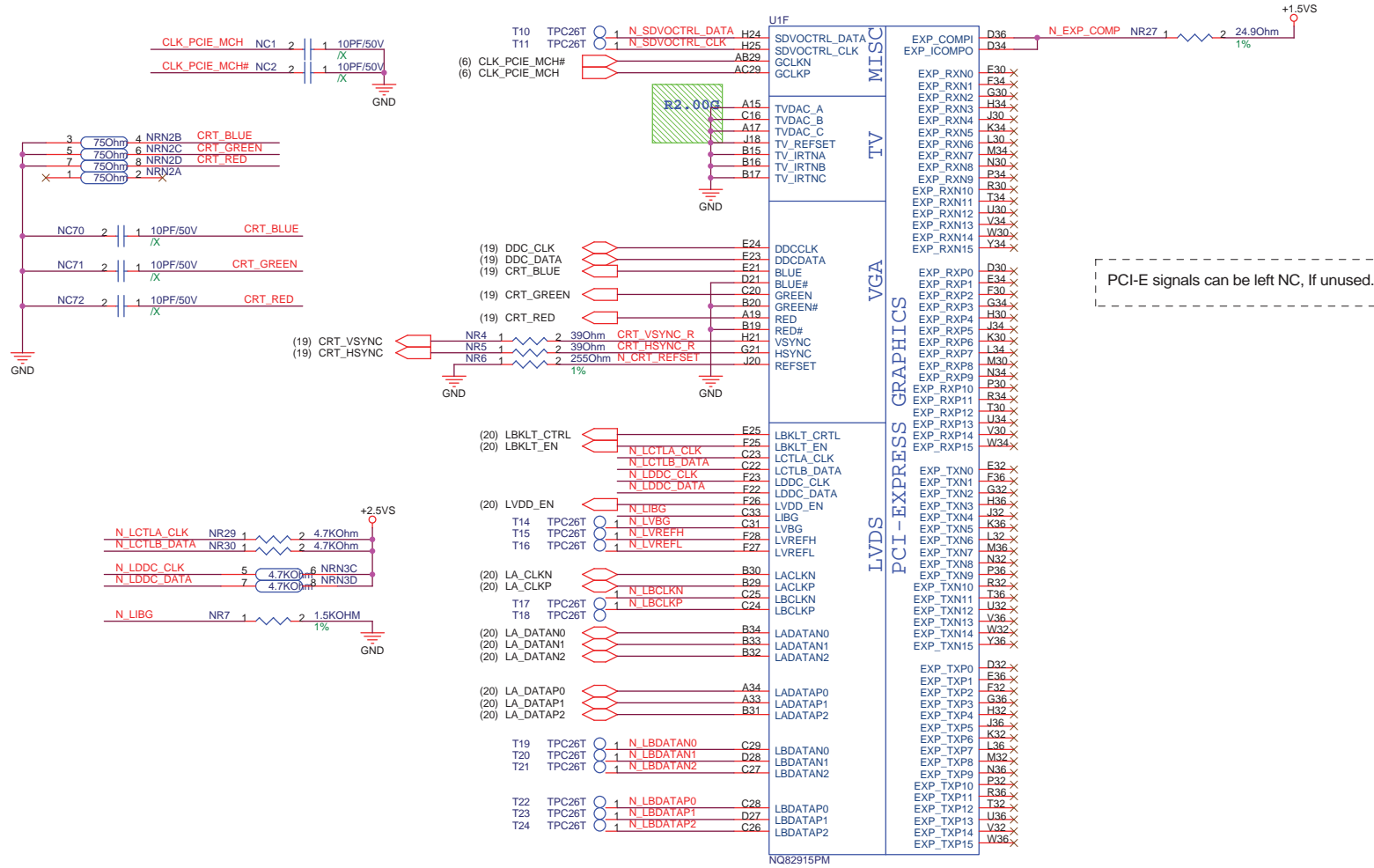
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ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name		Rev
A3	P704		R1.0G
Date: Friday, May 30, 2008		Sheet	10 of 47

SDVO Smbus have  
internal pull down

SDVOCTRL\_DATA Int PD  
0 : No SDVO device  
1 : SDVO device present

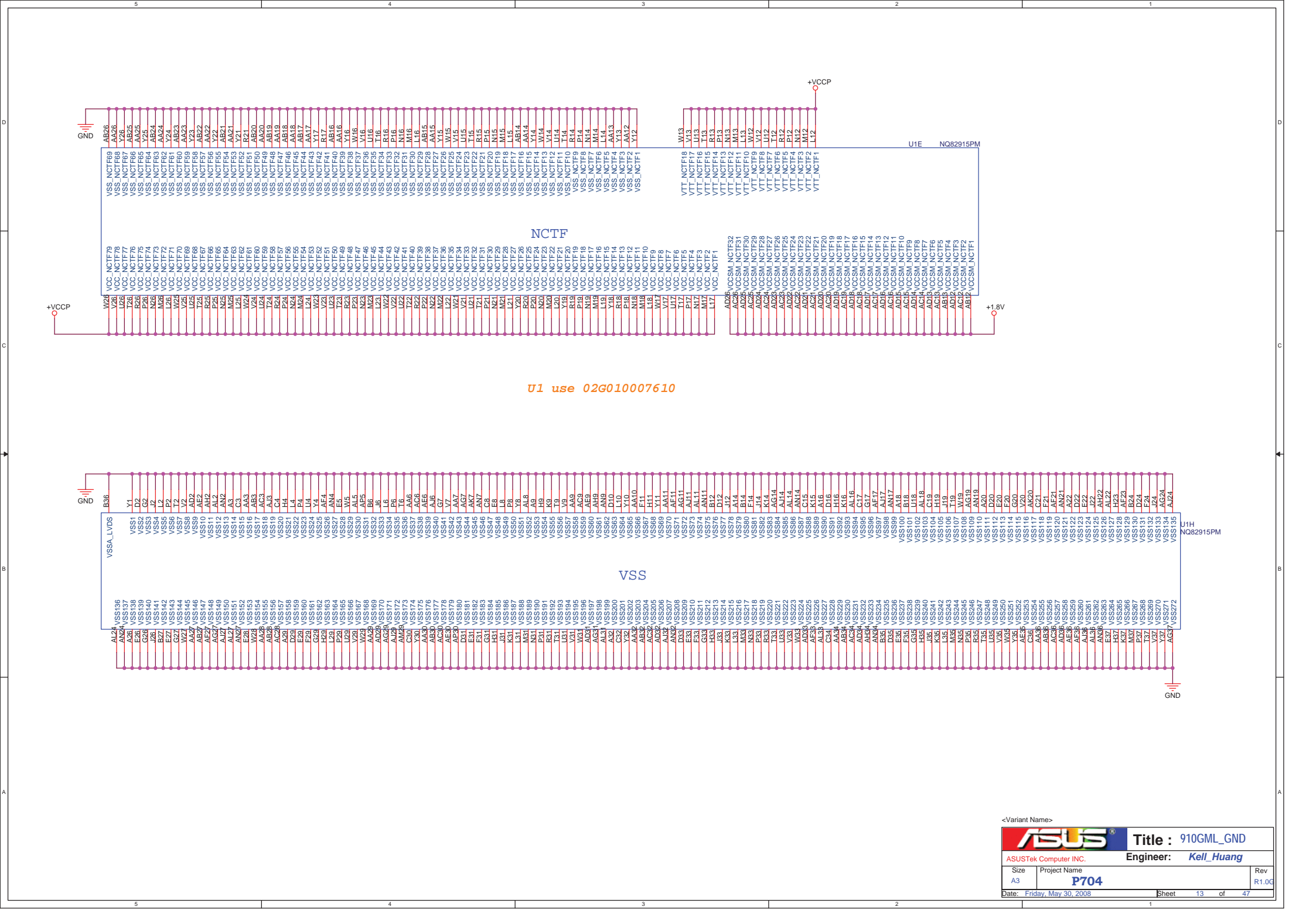
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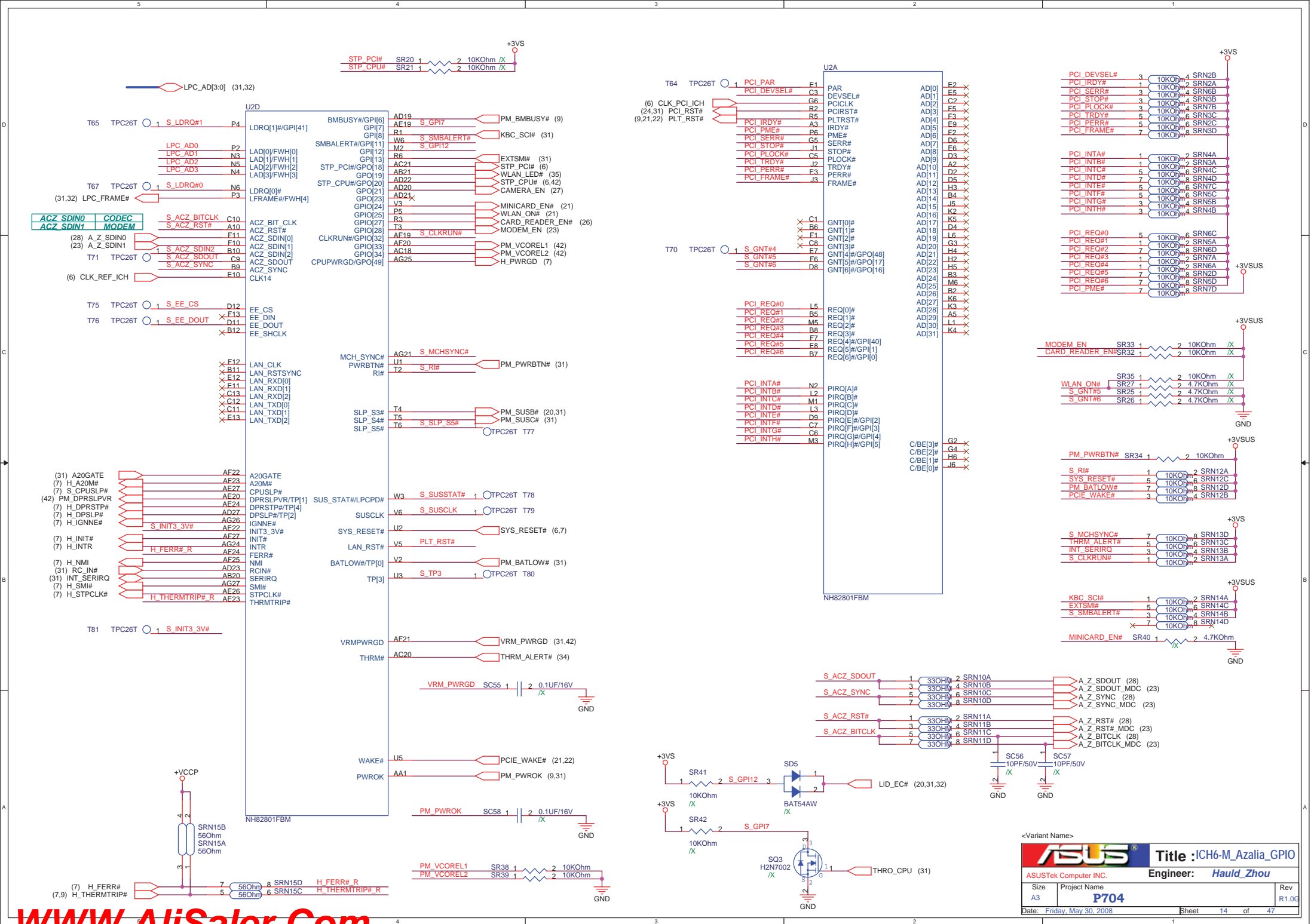


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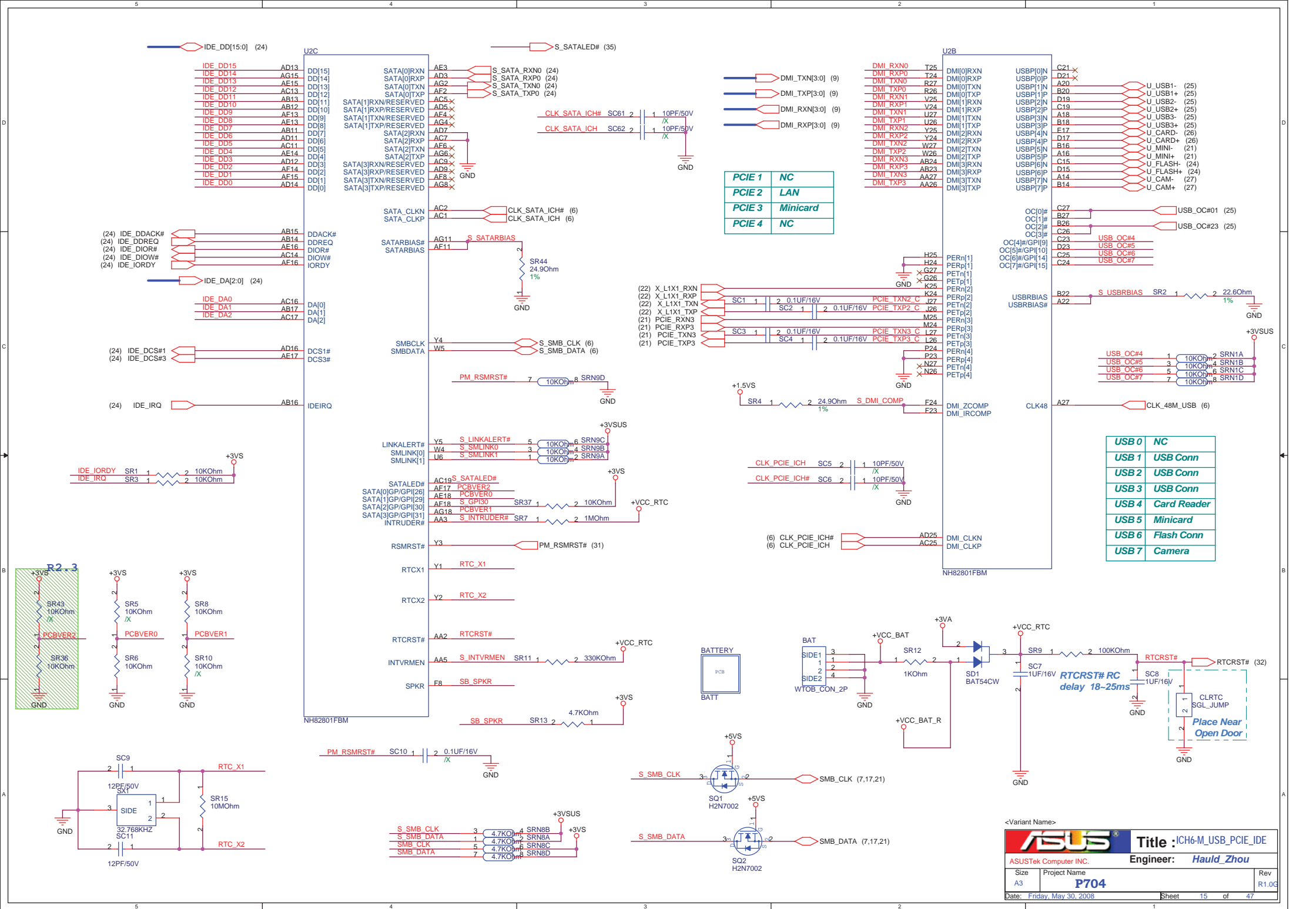
<b>ASUS</b>		<b>Title :910GML_VGA_LVDS</b>	
ASUSTek Computer INC.		Engineer: <b>Kell_Huang</b>	
Size A3	Project Name <b>P704</b>	Rev R1.0G	
Date: Friday, May 30, 2008		Sheet	11 of 47



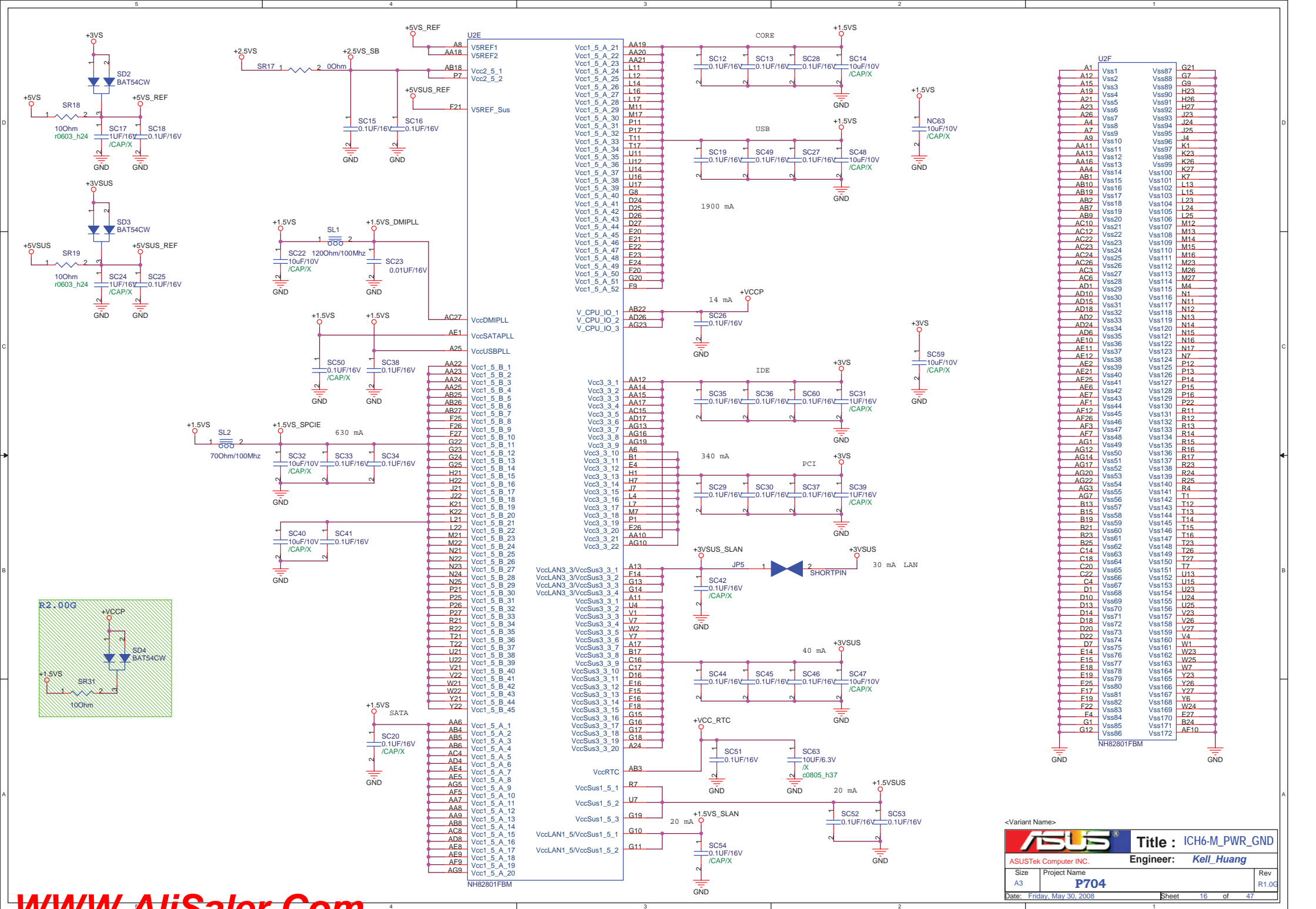


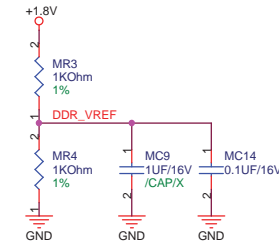
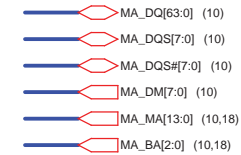




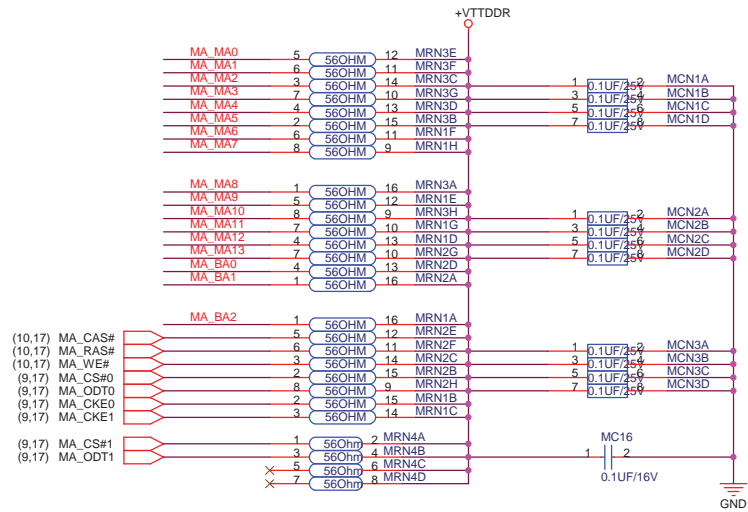


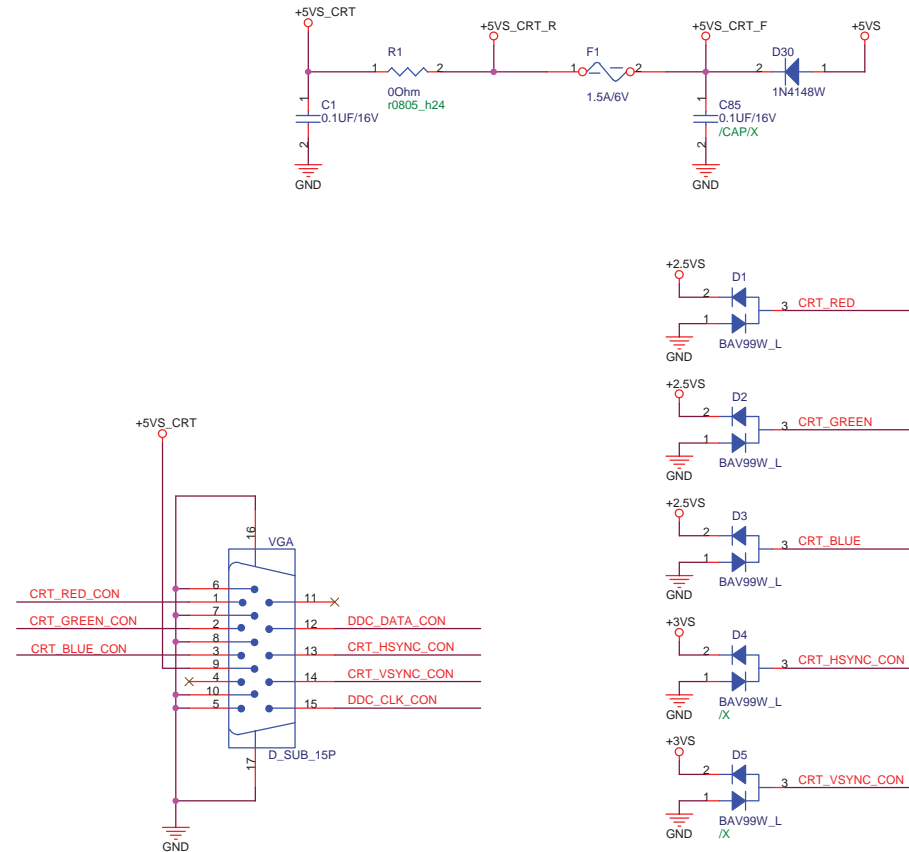
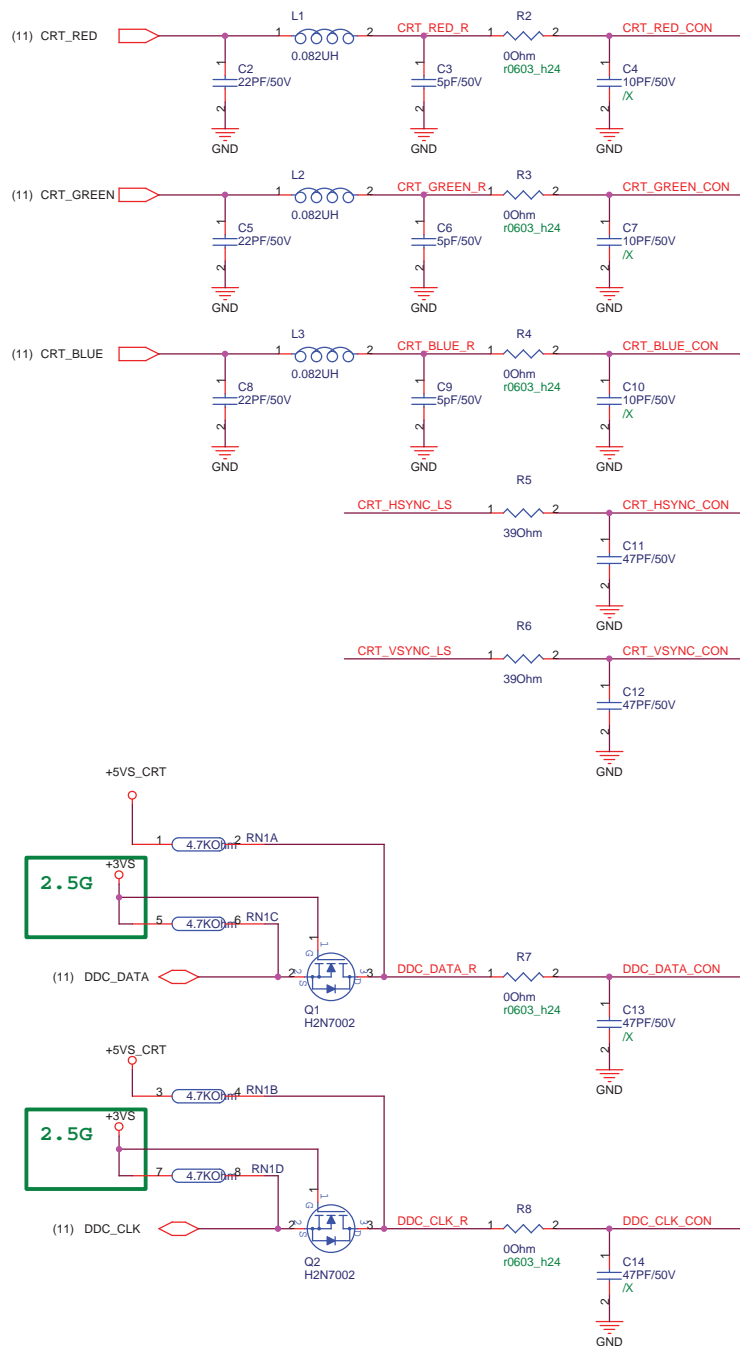




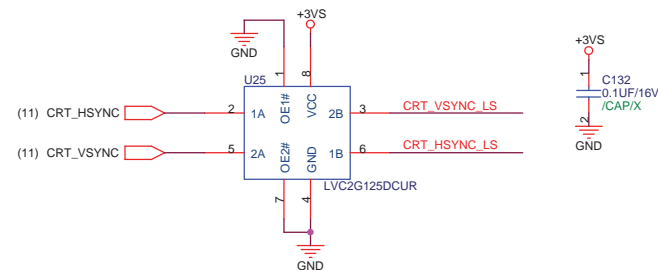


MA\_MA[13:0] (10,17)  
MA\_BA[2:0] (10,17)

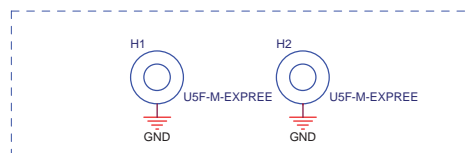




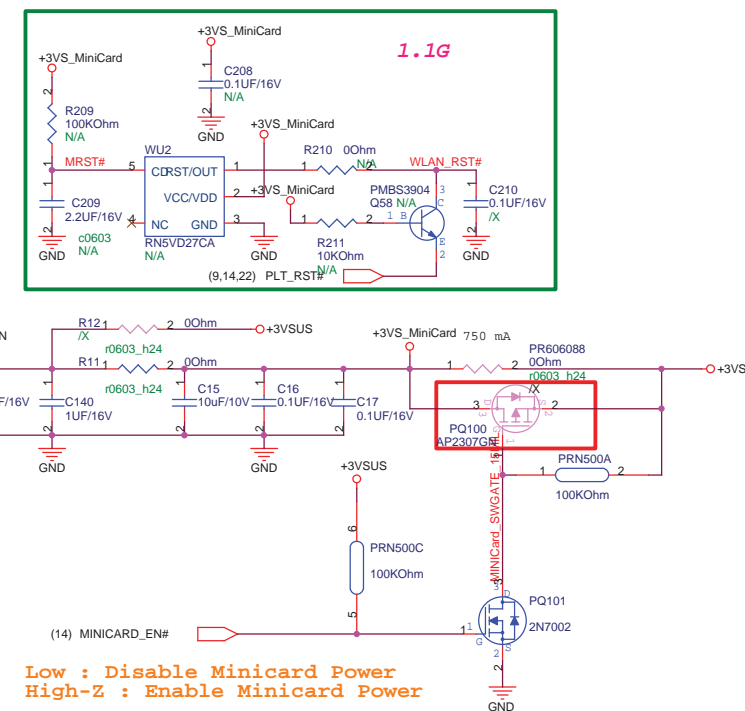
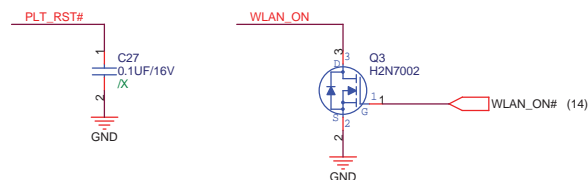
VGA use 12G10110015W or 12G10110015N



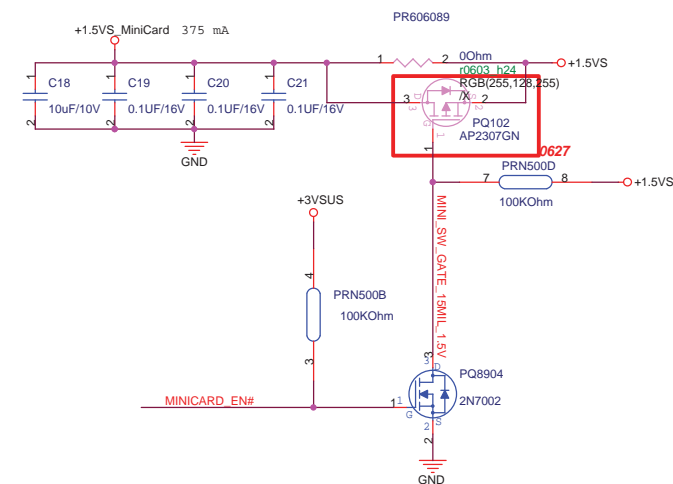


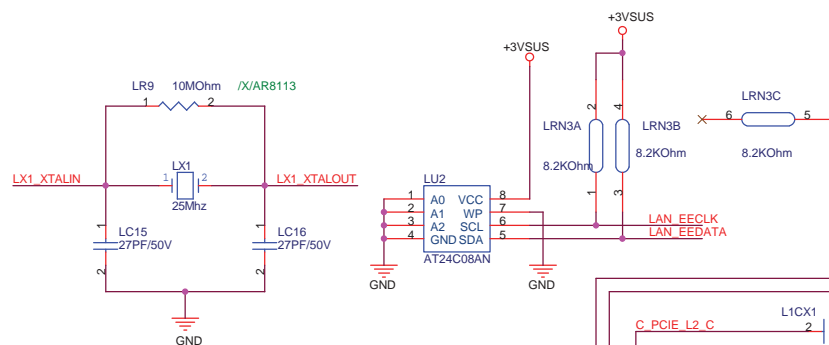
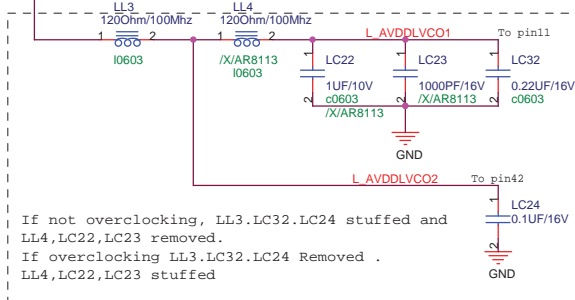
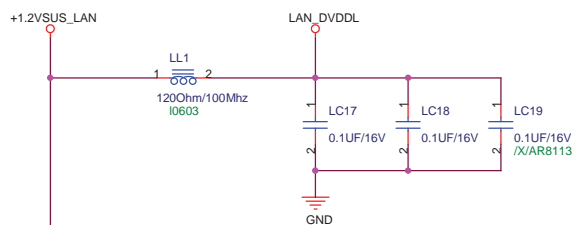
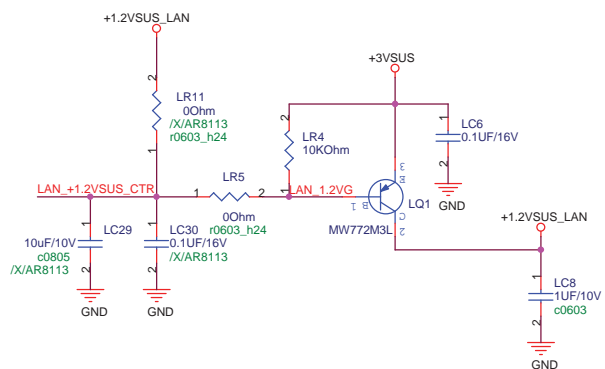
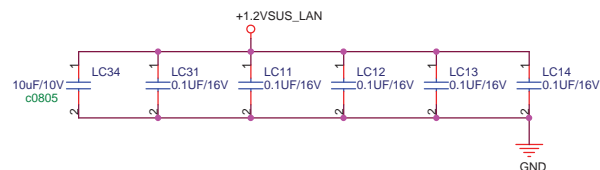
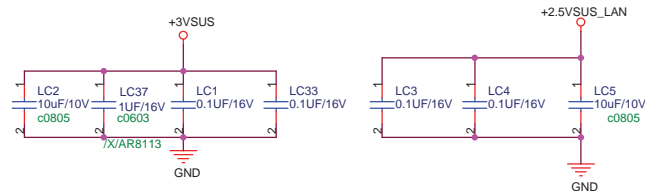


MINI CARD NUT(1.6mm) \*2

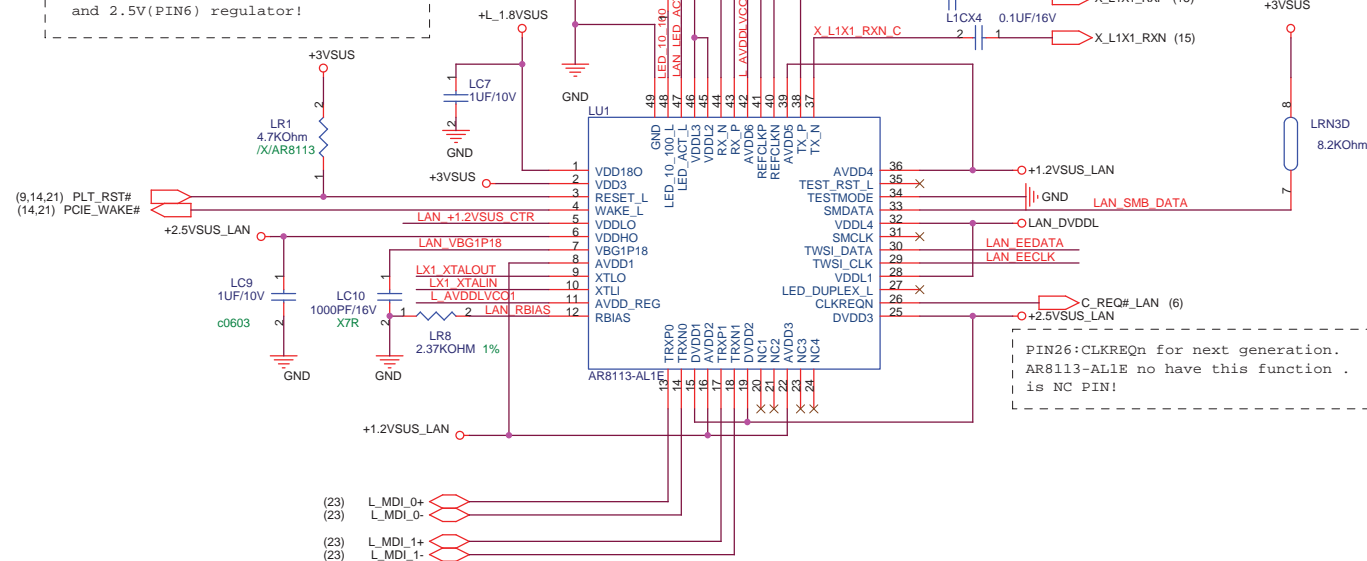


Low : Disable Minicard Power  
High-Z : Enable Minicard Power

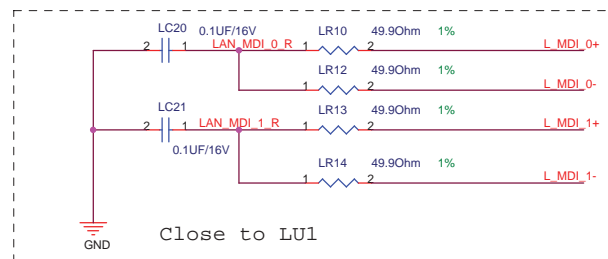




AR8113 internal integrated 1.8V(PIN1) and 2.5V(PIN6) regulator!

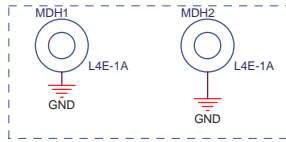


PIN26:CLKREQn for next generation.  
AR8113-AL1E no have this function .  
is NC PIN!

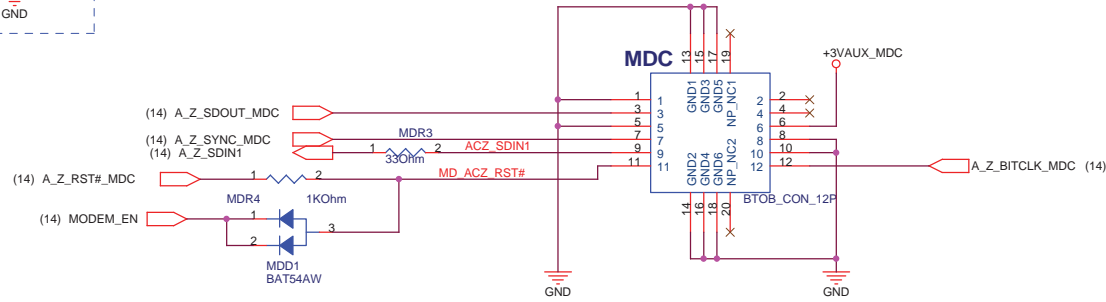


ASUS		Title : LAN_8113	
ASUSTek Computer INC.		Engineer: Hauld_Zhou	
Size	A3	Project Name	P704
Date:	Friday, May 30, 2008	Sheet	22 of 47

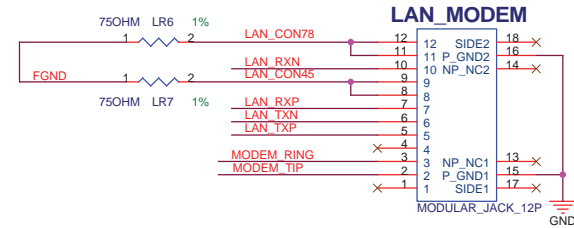
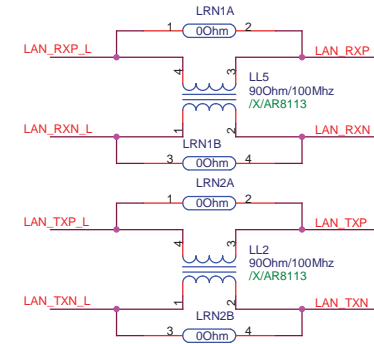
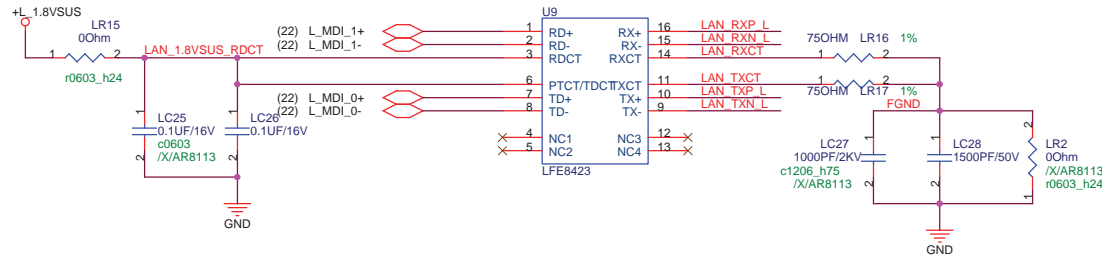
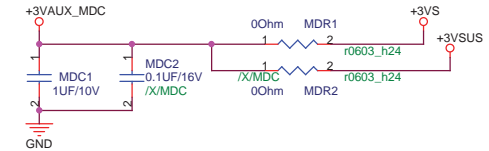
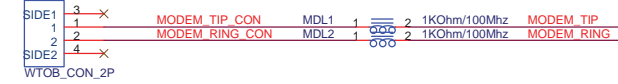




MODEM NUT(3.0mm) \*2

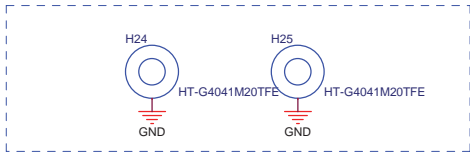


### MODEM

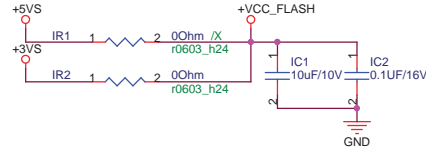


<Variant Name>

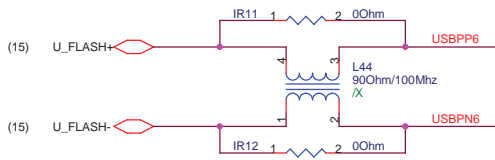
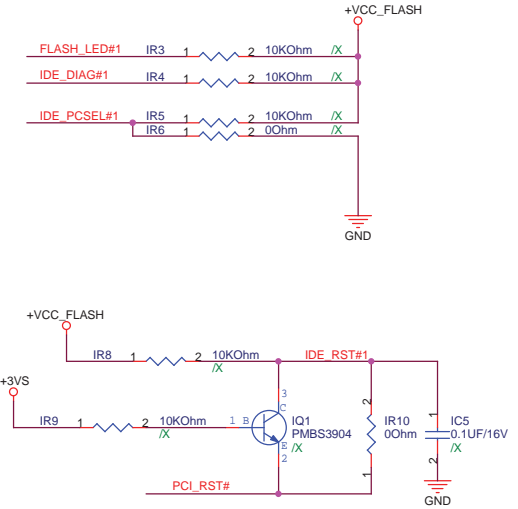
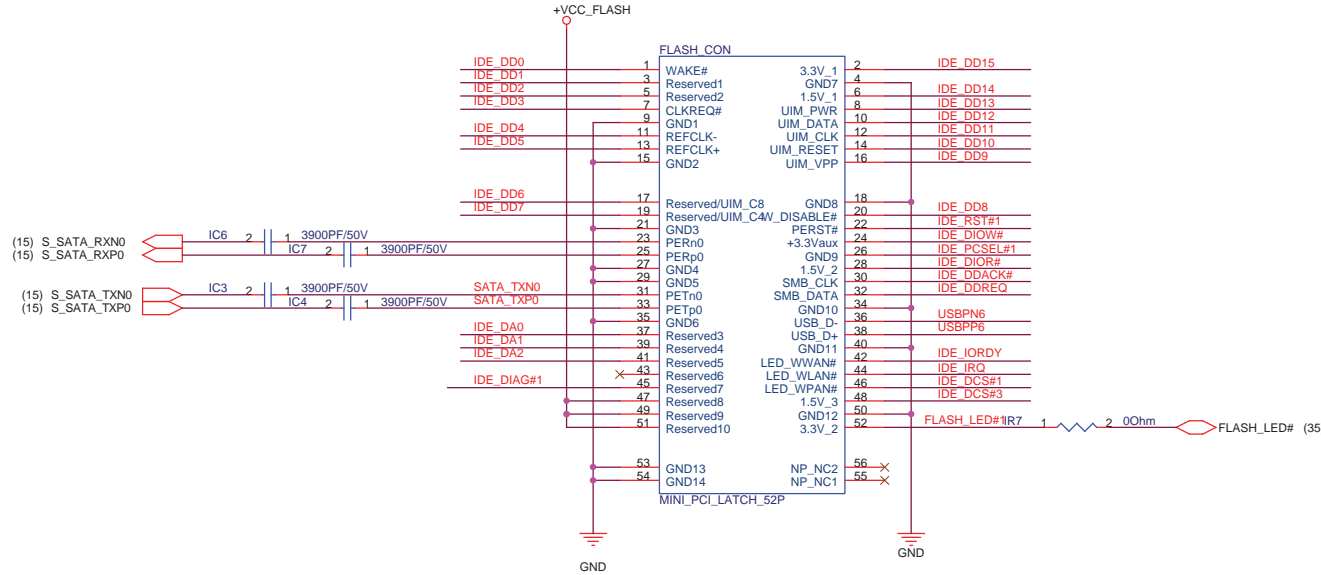
<b>ASUS</b>		Title : MDC_RJ11_RJ45	
ASUSTek Computer INC.		Engineer: Hauld_Zhou	
Size	Project Name		Rev
A3	P704		R1.0G
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FLASH CARD NUT(3.3mm) \*2



- IDE\_DD[15:0] (15)
- IDE\_DA[2:0] (15)
- IDE\_DDACK# (15)
- IDE\_DDREQ (15)
- IDE\_DIOR# (15)
- IDE\_DIOW# (15)
- IDE\_IORDY (15)
- IDE\_DCS#1 (15)
- IDE\_DCS#3 (15)
- IDE\_IRQ (15)
- PCI\_RST# (14,31)

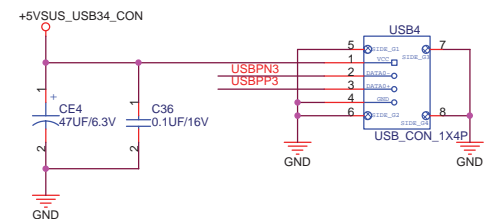
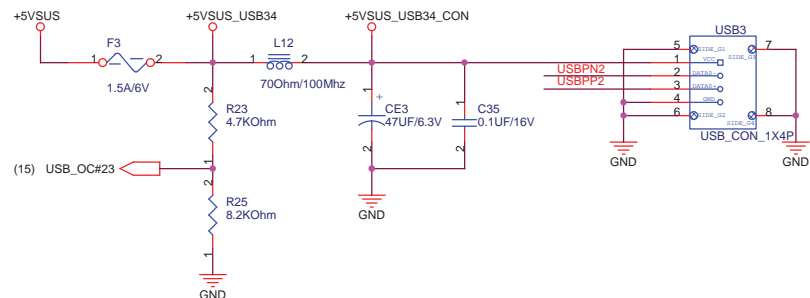
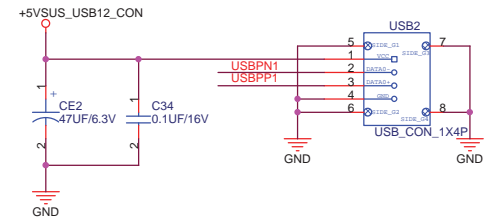
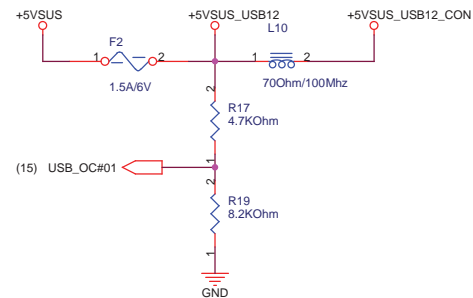
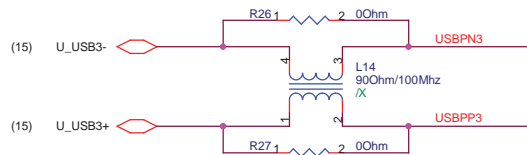
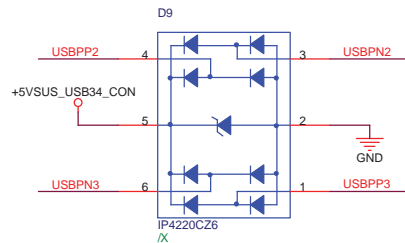
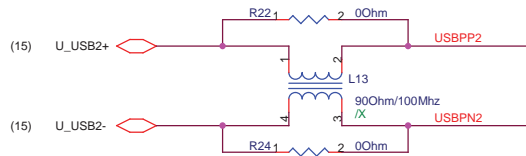
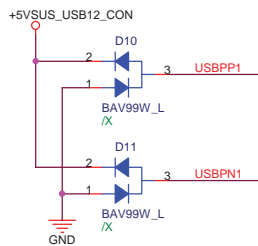
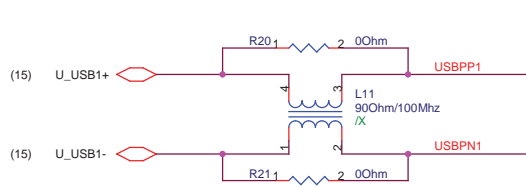


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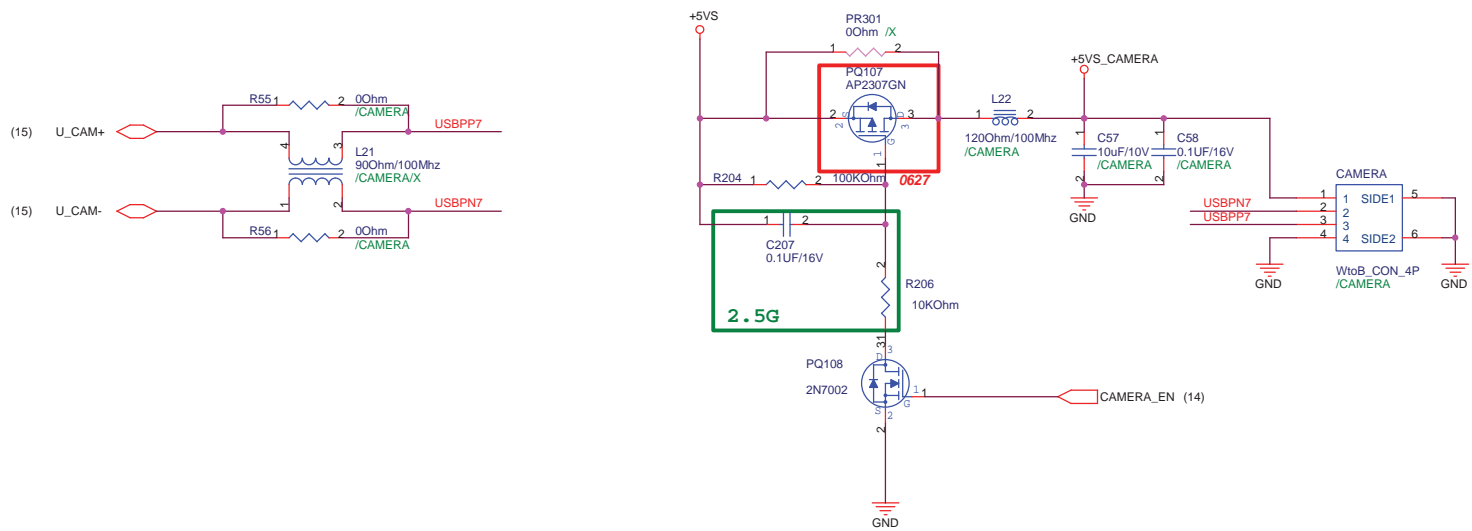
**ASUS** Title : MDC\_RJ11\_RJ45

ASUSTek Computer INC. Engineer: Hauld\_Zhou

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A3	P704	R1.0G
Date: Friday, May 30, 2008	Sheet 24 of 47	





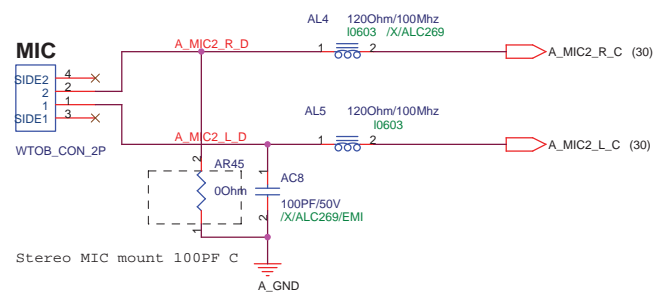


<Variant Name>

<b>ASUS</b>		<b>Title : Camera Conn</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		Rev
A3	<b>P704</b>		R1.0G
Date: Friday, May 30, 2008		Sheet	27 of 47

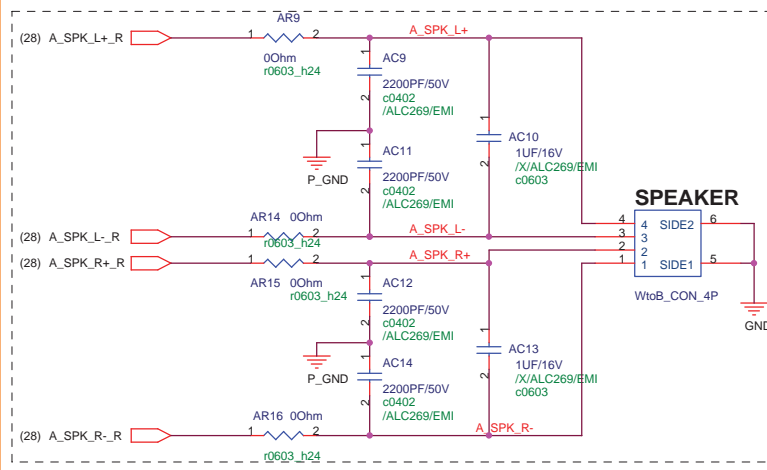


## Internal MIC



## SPEAKER

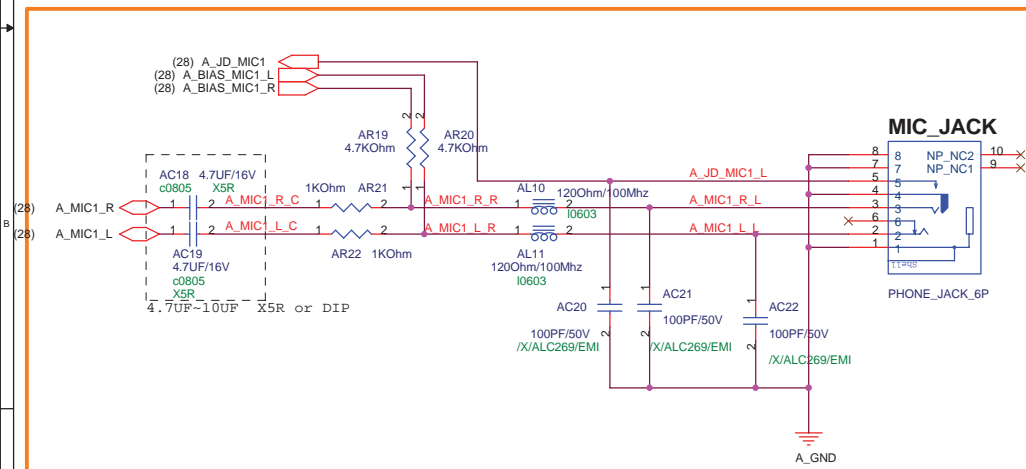
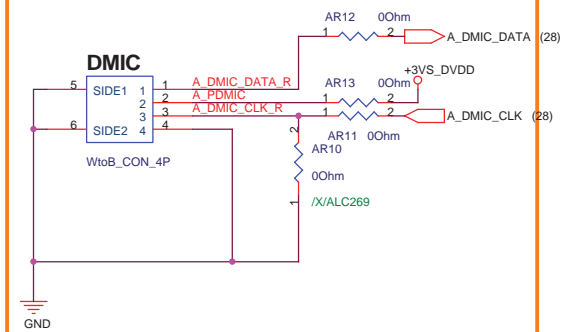
Demodulation Filter  
Placement near  
Audio Codec



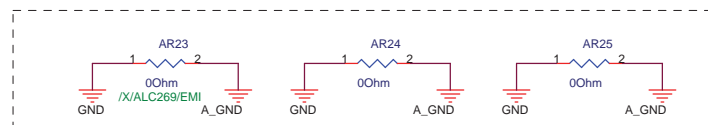
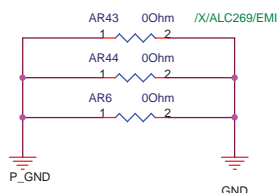
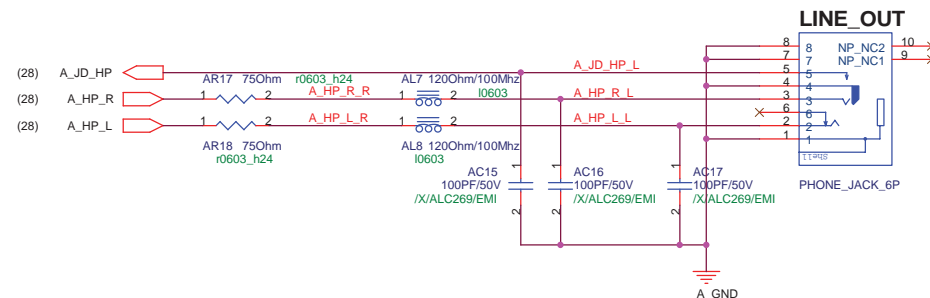
<<Attention>>

you can use LC filter (AR9, AR14, AR15, AR16 mount 8.2uH L ; and mount AC10, AC13) to eliminate the EMI (please don't use general beads, because they may influence the THD+N quality) , AC9/AC11/AC12/AC14 are used for EMI fine-tune ; For EMI issue, All L and C should near to codec

## Digital Mic Interface



## HP

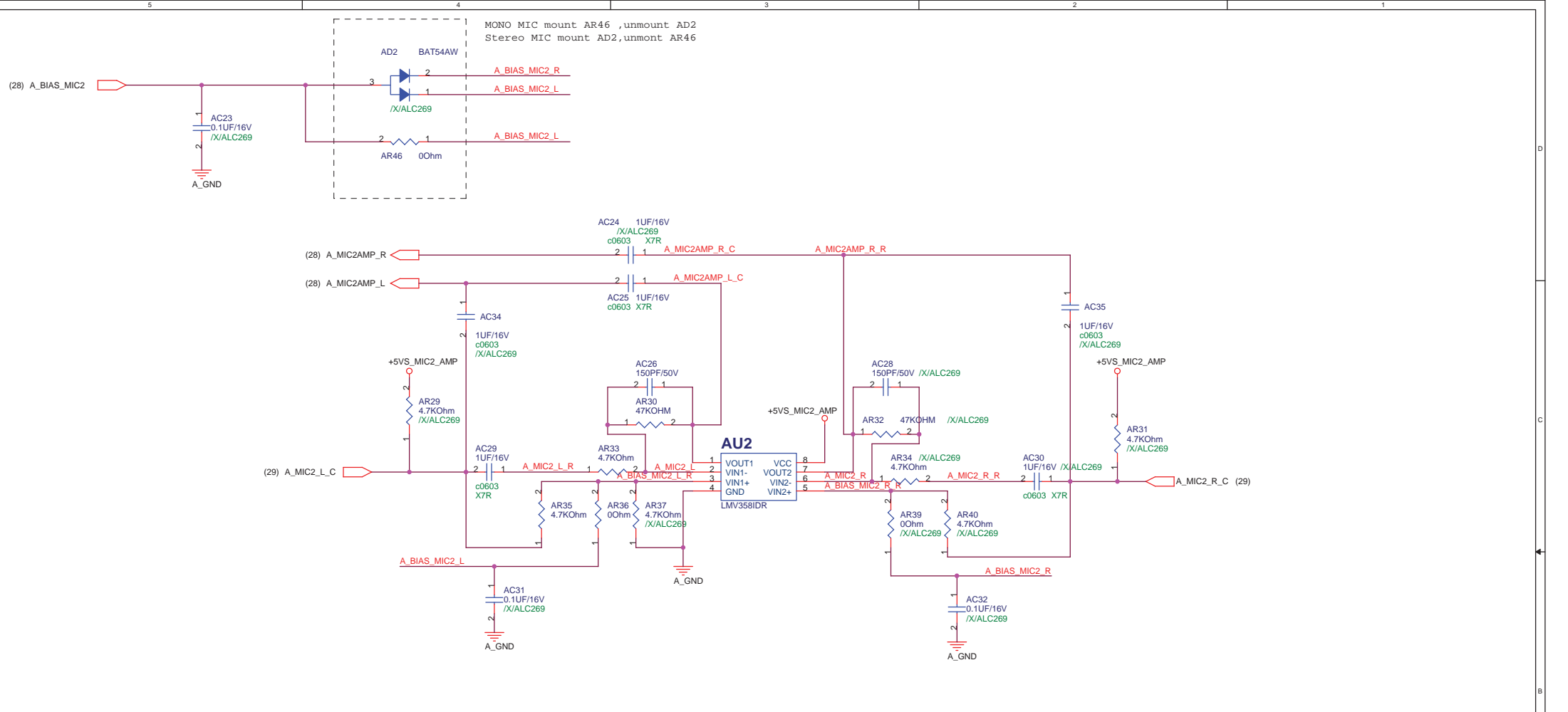


AR24, AR25 can use  
0.1uF 11G233310432320  
for EMI

<Variant Name>

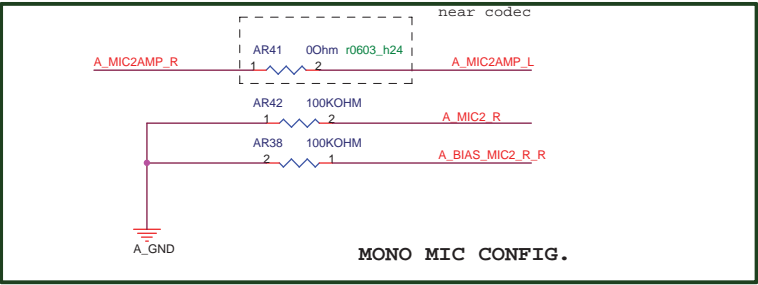
<b>ASUS</b>		Title : ALC269-2(I/O)	
ASUSTek Computer INC.		Engineer: Jeff_Li	
Size A3	Project Name <b>P704</b>		Rev R1.0G
Date: Friday, May 30, 2008		Sheet 29 of 47	



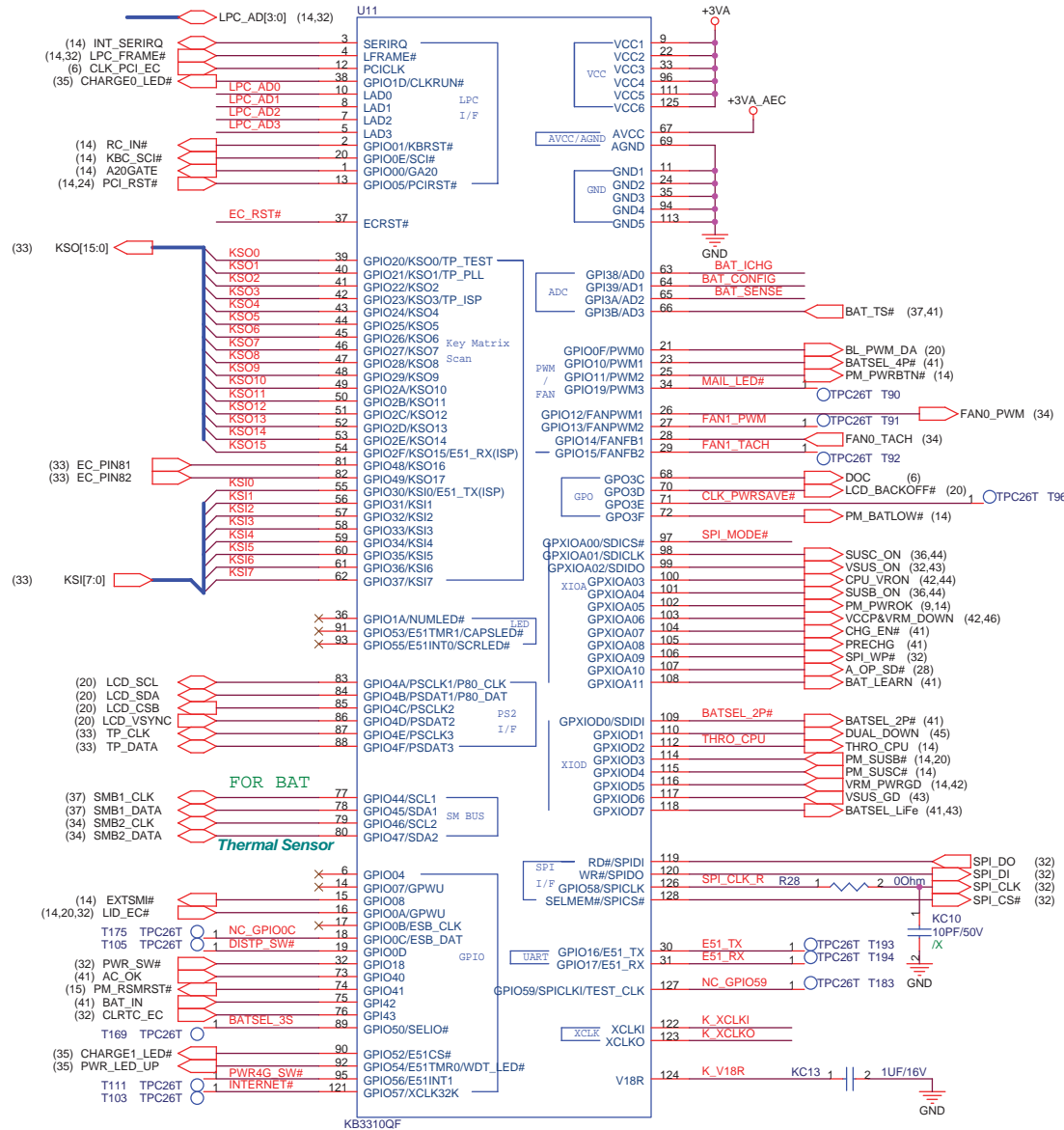
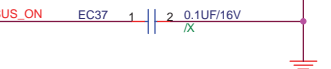
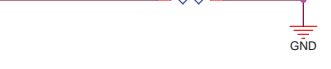
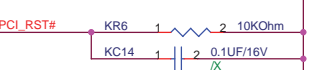
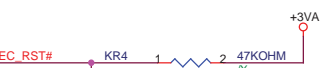
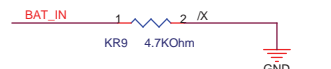
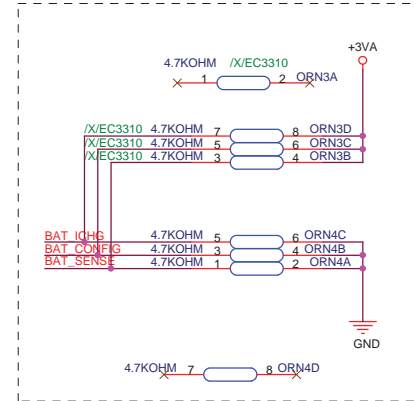
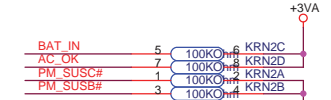
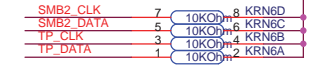
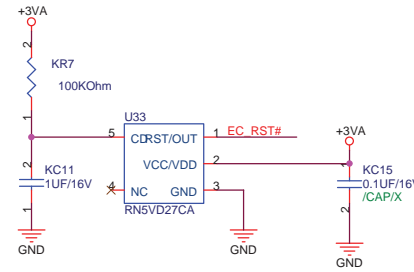
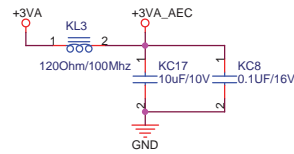
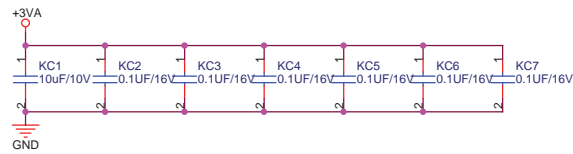


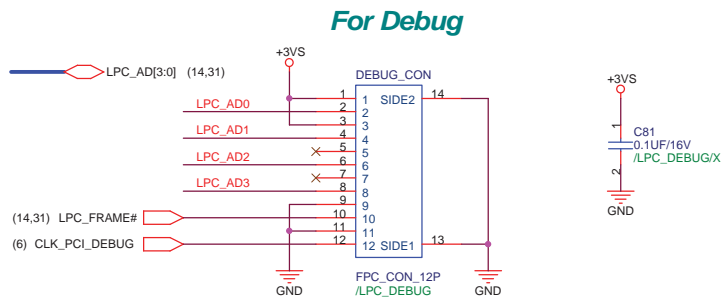
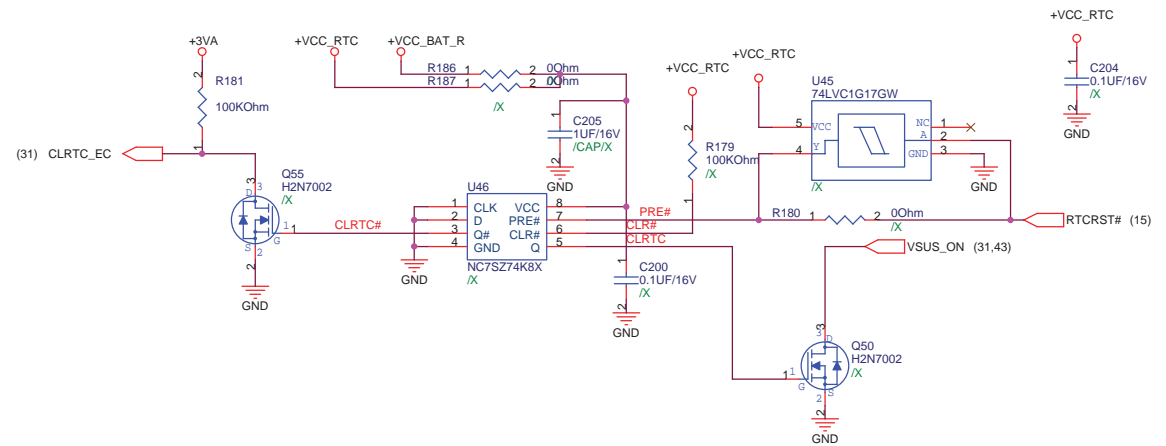
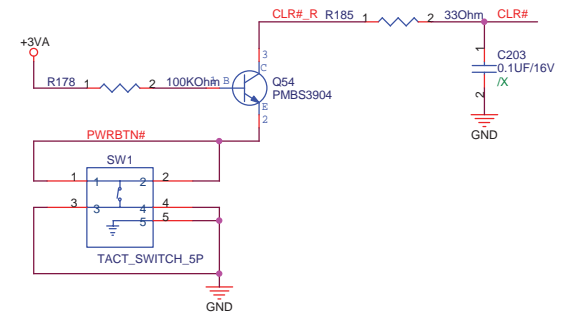
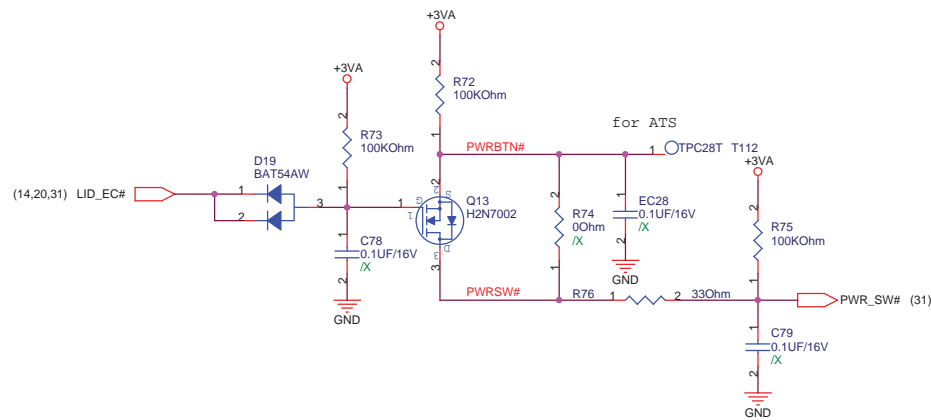
# Internal MIC Amp.

FL = 33.86kHz, FH = 22.5kHz

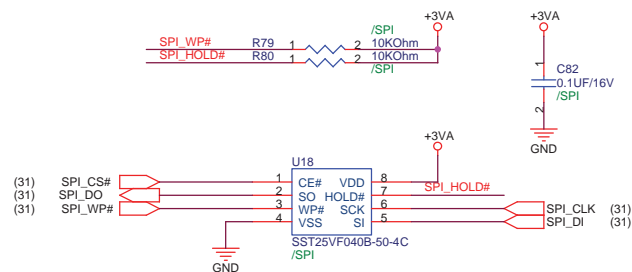


<Variant Name>		ASUS®		Title : ALC269-3(MIC AMP)	
ASUSTek Computer INC.		Engineer: Jeff_Li			
Size	Project Name			Rev	
A3	P704			R1.0G	
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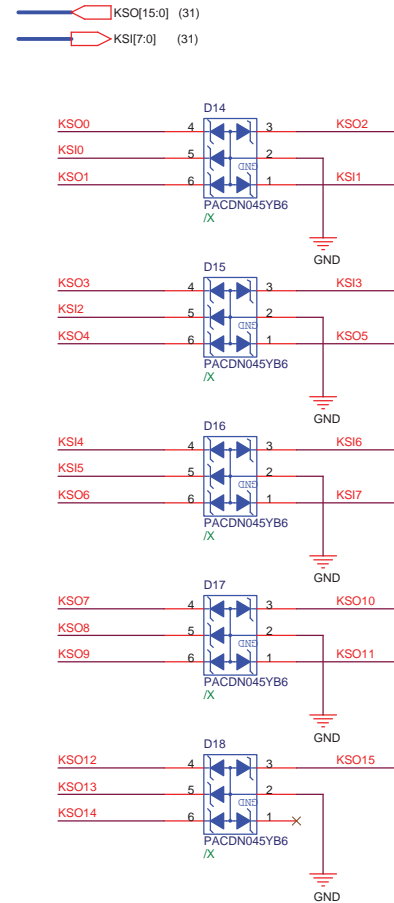
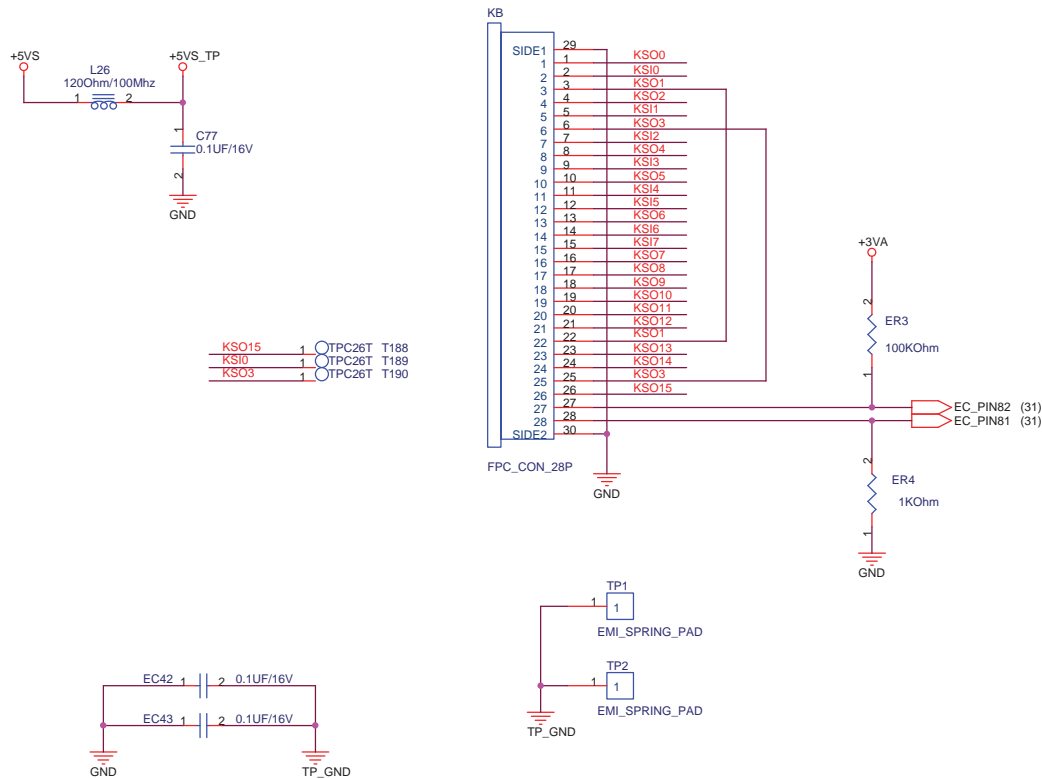
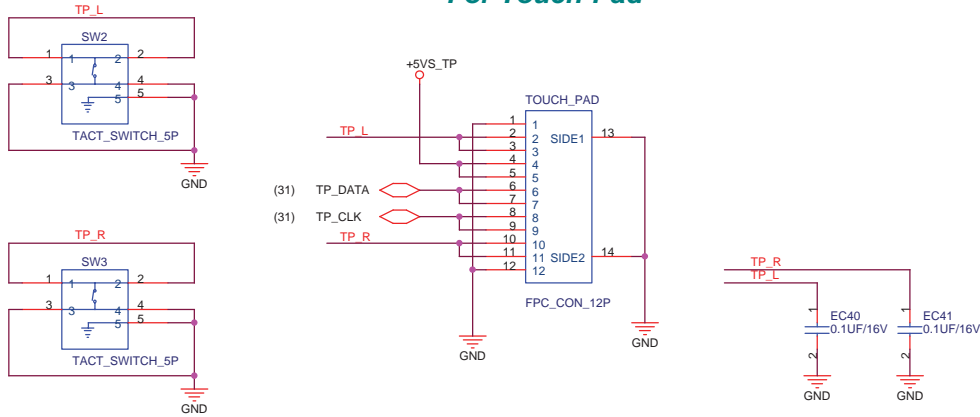


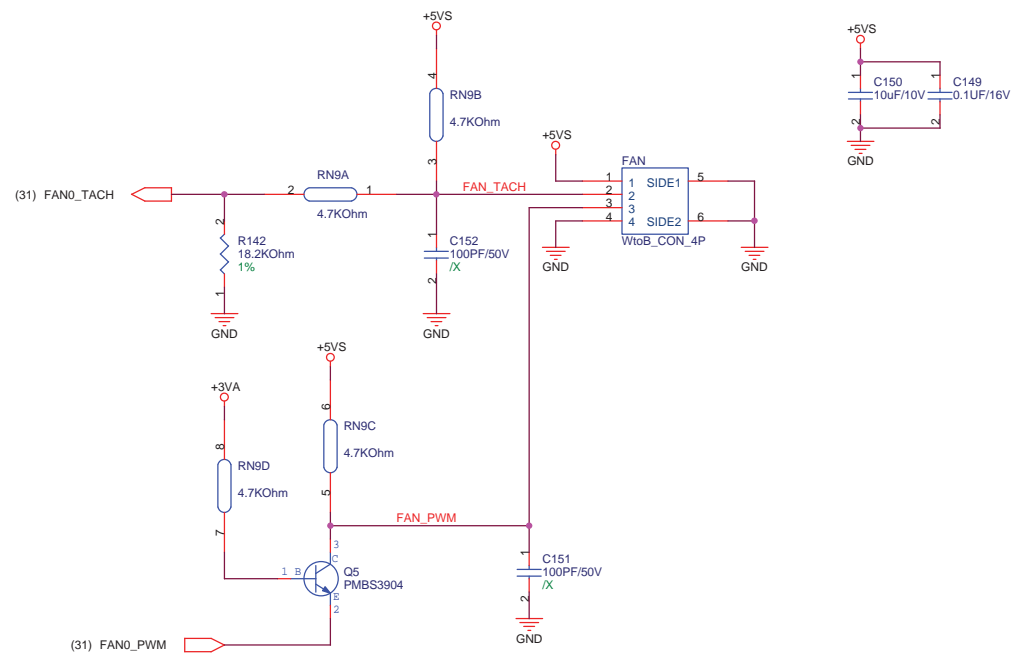
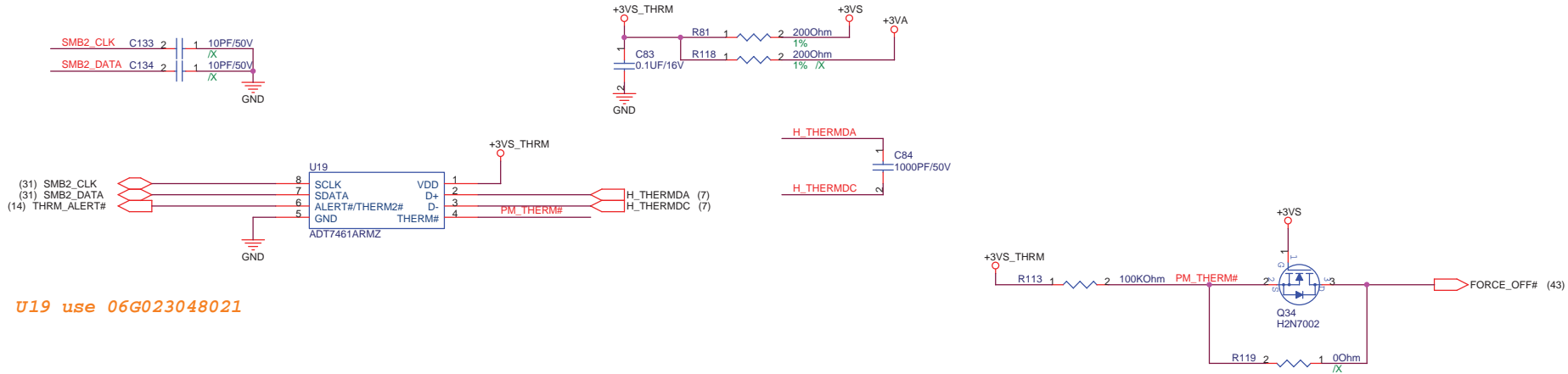


Debug Card cable use Z96 Touch Pad cable, P/N:  
14G124110126, 14G124110120, 14G124110121  
14G124110124, 14G124110125



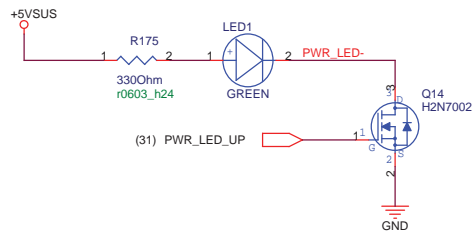
ASUS		Title : Switch_SPI ROM	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	A3	Project Name	P704
Date:	Friday, May 30, 2008	Sheet	32 of 47
		Rev	R1.0G



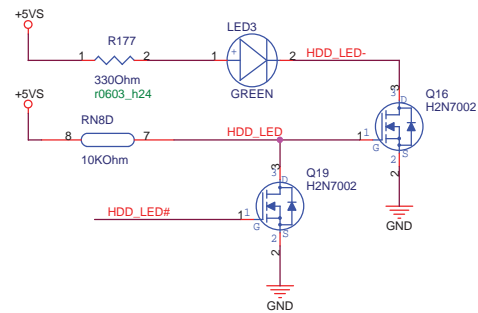


<Variant Name>		Title : Thermal Sensor_FAN	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	P704	R1.0G	
Date: Friday, May 30, 2008	Sheet	34	of 47

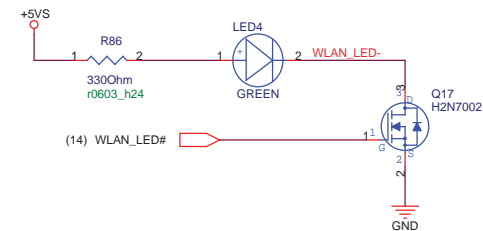
### for POWER LED



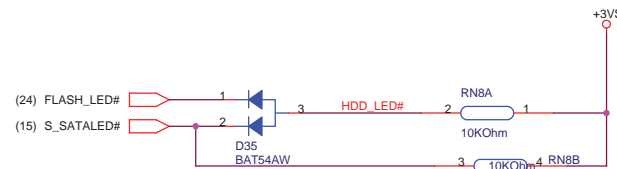
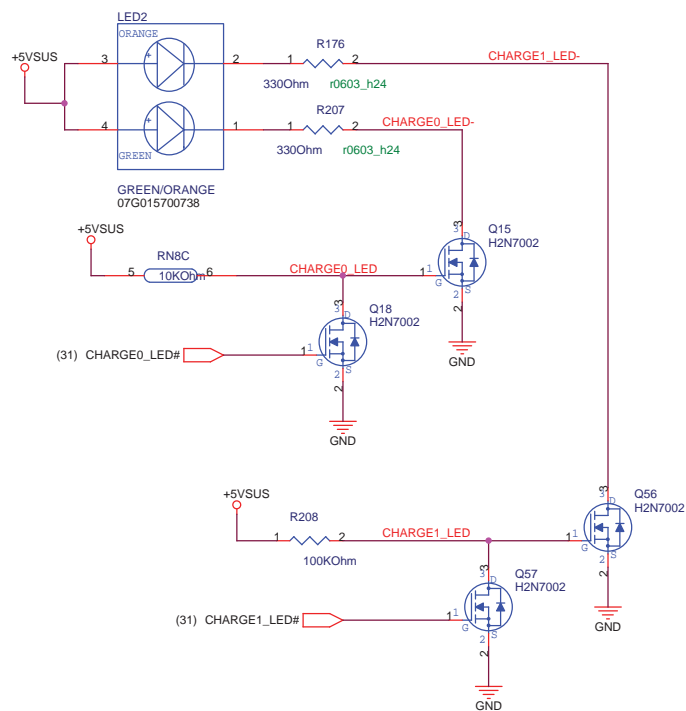
### for FLASH LED

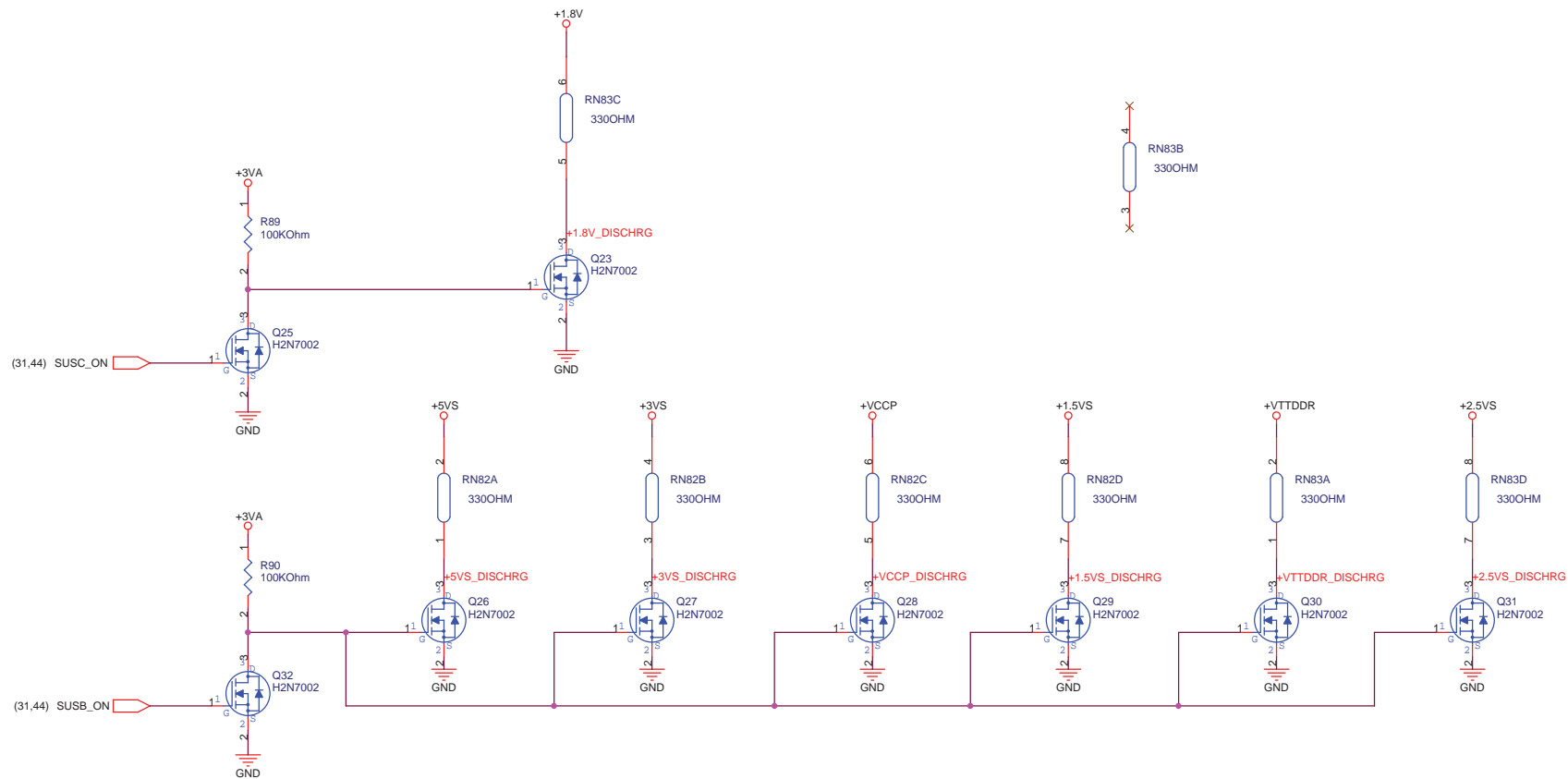


### for WLAN LED



### for CHARGE LED

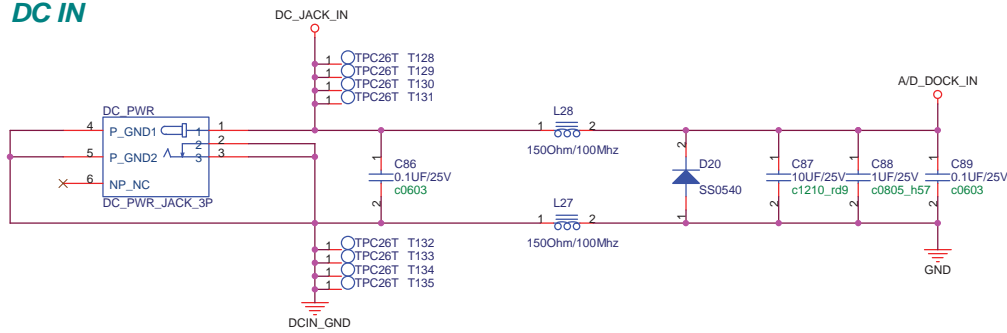




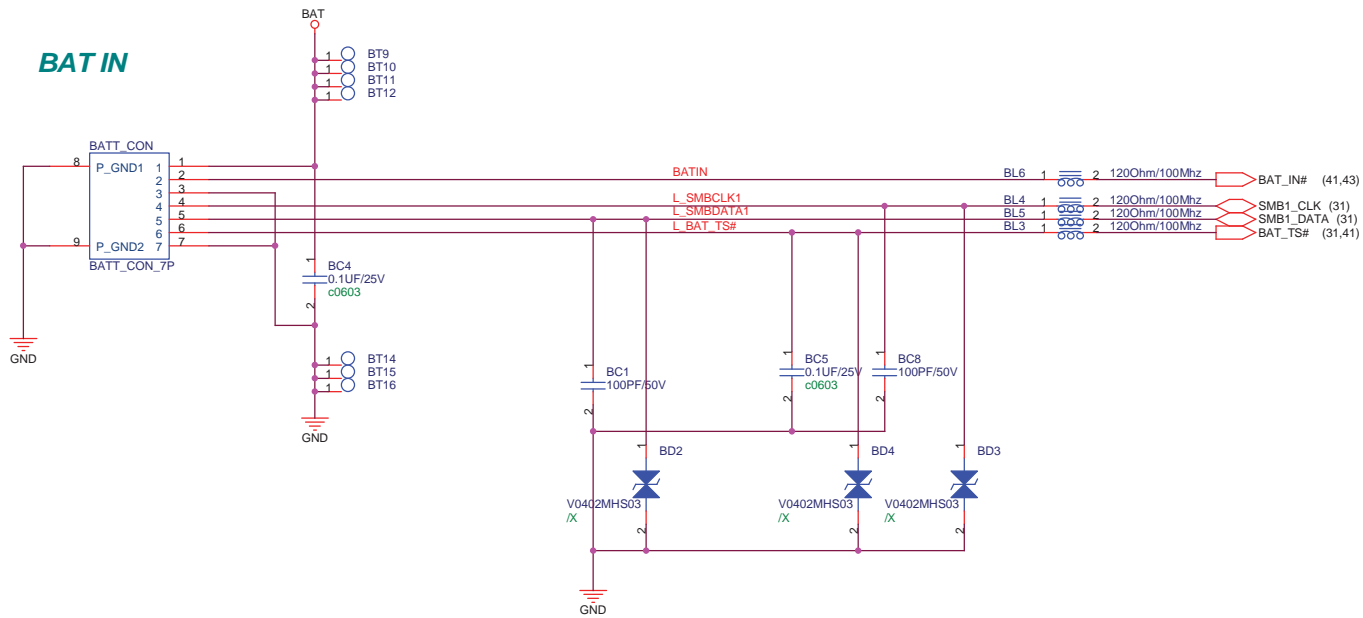
<Variant Name>		ASUS®		Title : Discharge	
ASUSTek Computer INC.		Engineer: Kell_Huang			
Size	Project Name			Rev	
A3	P704			R1.0G	
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# DC IN

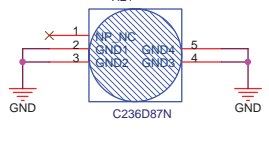
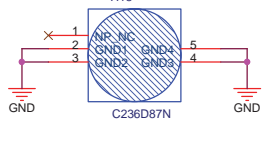
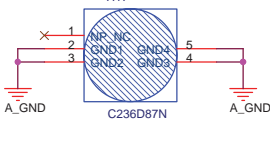
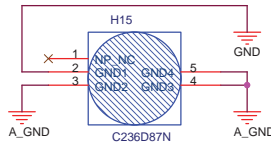
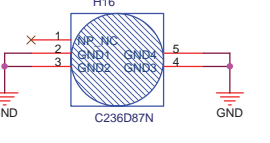
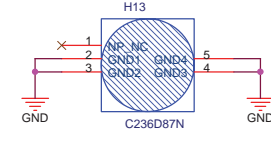
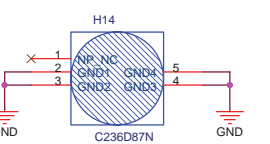
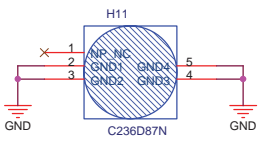
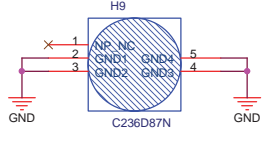
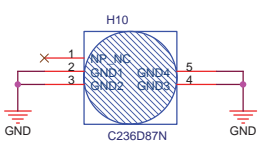
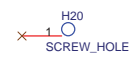
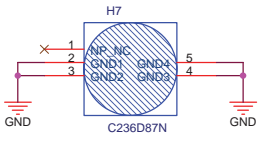
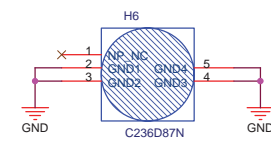
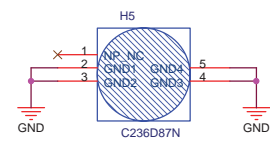


# BAT IN

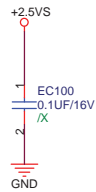
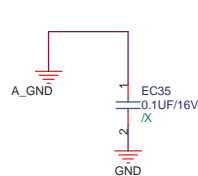
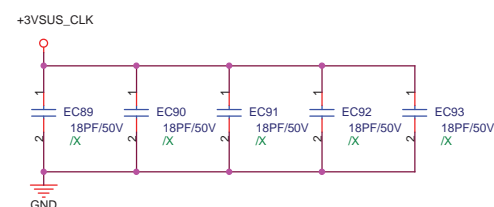
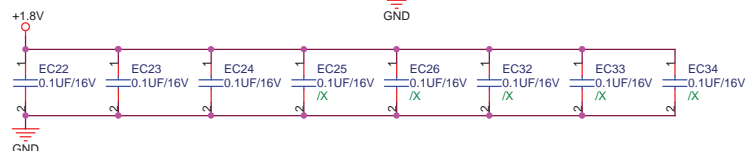
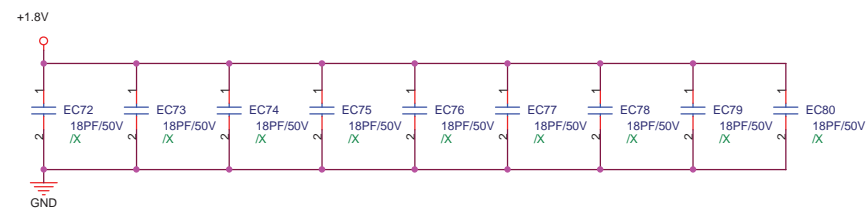
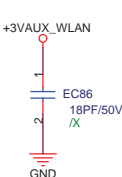
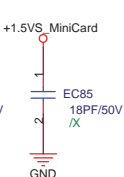
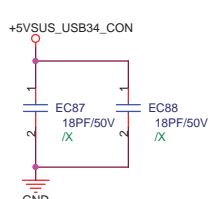
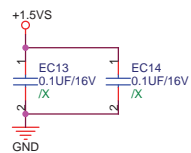
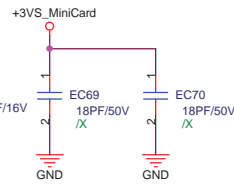
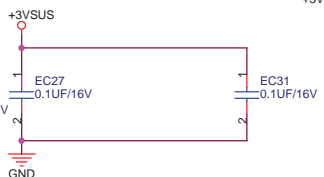
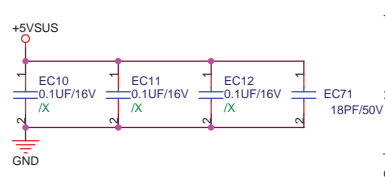
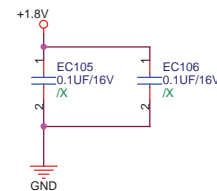
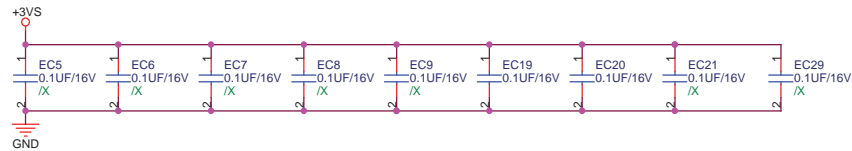
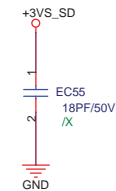
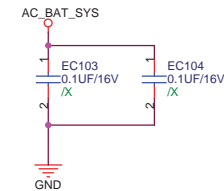
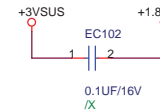
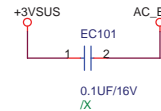
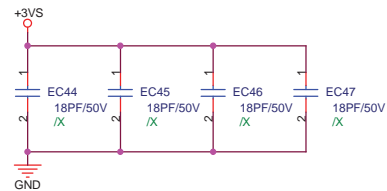
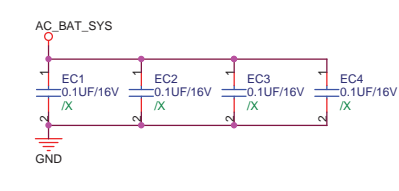


<Variant Name>

<b>ASUS</b>		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size A3	Project Name <b>P704</b>	Rev R1.0G	
Date: Friday, May 30, 2008		Sheet 37 of 47	

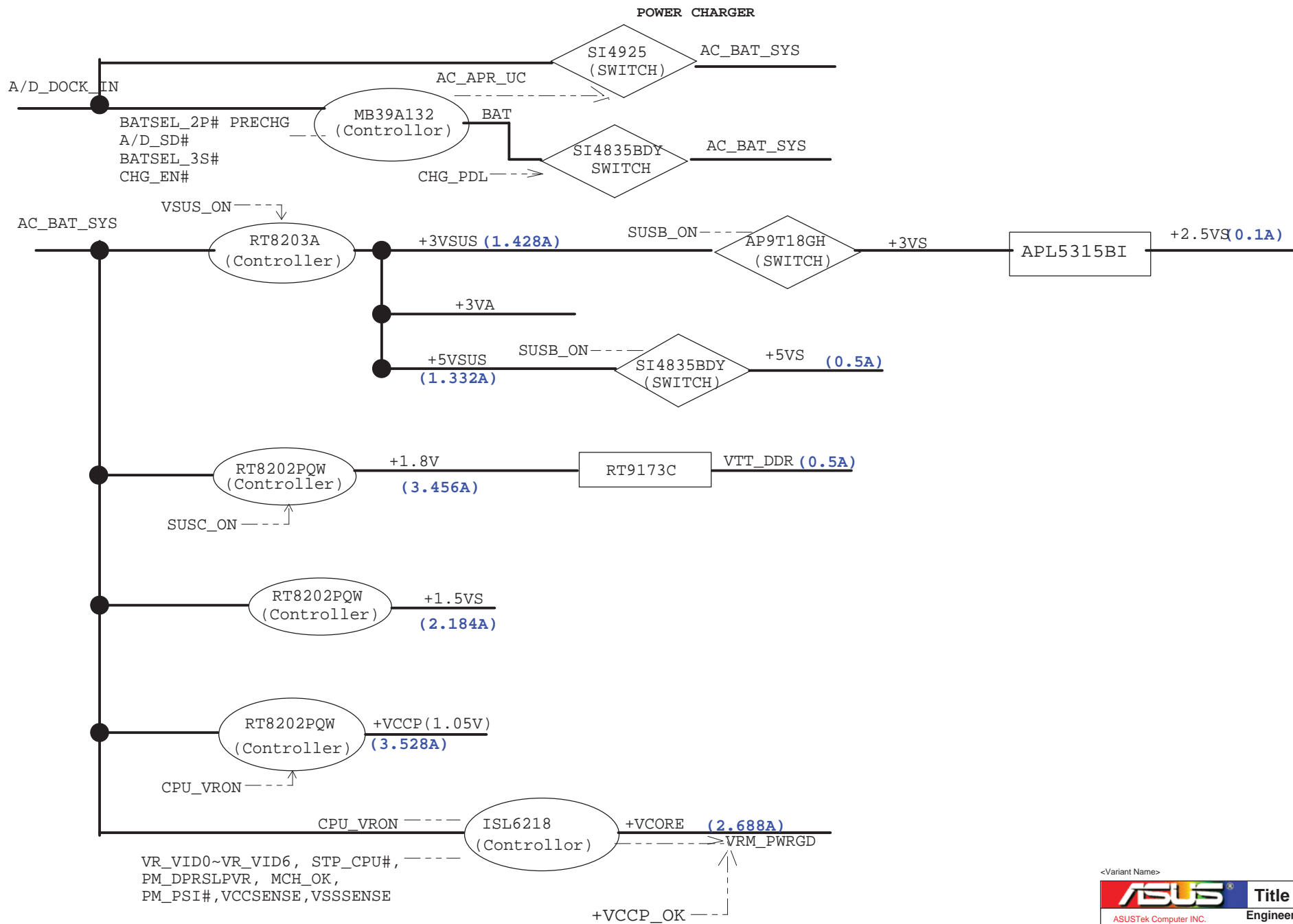


<Variant Name>		Title : Srew Hole	
ASUSTek Computer INC.		Engineer: Kell_Huang	
Size	Project Name	Rev	
A3	P704	R1.0G	
Date: Friday, May 30, 2008		Sheet	38 of 47

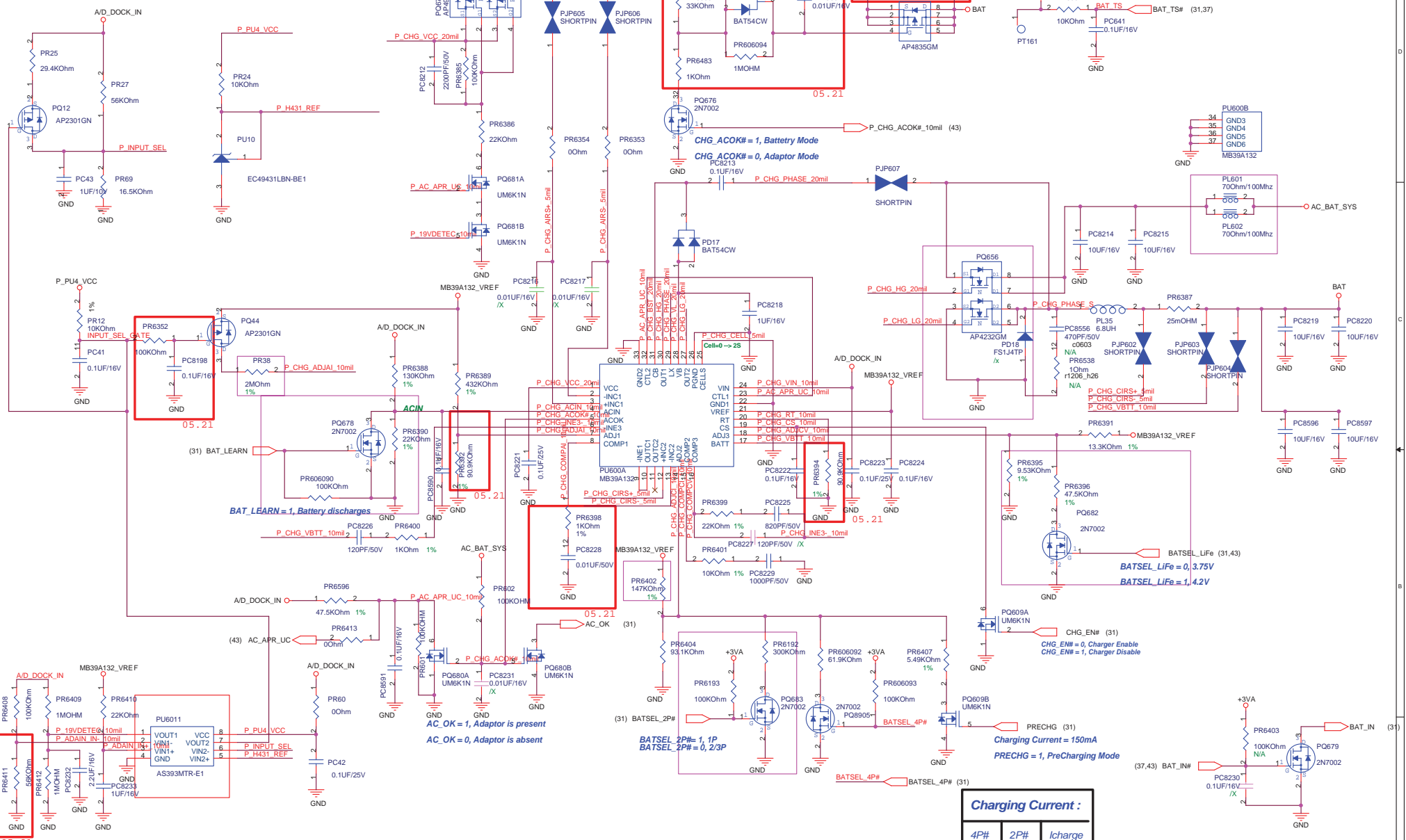


<Variant Name>

<b>ASUS</b>		<b>Title : EMI</b>	
ASUSTek Computer INC.		Engineer: <i>Kell_Huang</i>	
Size	Project Name		Rev
A3	<b>P704</b>		R1.0G
Date: Friday, May 30, 2008		Sheet	39 of 47



<Variant Name>		ASUS <sup>®</sup>		Title : Power Flow	
ASUSTek Computer INC.		Engineer: Joy_Zhou			
Size	Project Name			Rev	
A3	704			1.1G	
Date: Friday, May 30, 2008	Sheet	40	of	47	



**Battery Charging Voltage :**  
 $V_{adj3} > 4.1V \implies V_{bat} = 4.2V / cell$   
 $2.2V > V_{adj3} > 1.1V \implies V_{bat} = 2 * V_{adj3} / cell$

**Battery Charging Current :**  
 $4.4V > V_{adj2} > 0V \implies I_{chg} = (V_{adj2} - 0.075) / (25 * Rs)$

**Input Adaptor Max. Current Limit :**  
 $I_{limit\_current} = (V_{adj1} - 0.075) / (25 * Rs)$

**Pre-Charging Mode :**  
Precharging current = 150mA  
 $V_{adj2} = 168.75mV$

**Adaptor Max. Current :**  
 $PR600 = 235.8K; I_{limit} = 2.170A; 20.615W (9.5V/22W)$   
 $PR600 = 185.3K; I_{limit} = 2.677A; 32.124W (12V/36W)$

**ACIN Threshold = 1.25V**  
Adaptor > 8.63V, System Powered by Adaptor  
Adaptor < 8.63V, System Powered by Battery

**Prevent Input from 19V :**  
Adaptor > 13.06V, PQ603B Turn-off  
Adaptor < 13.06V, PQ603B Turn-on

**Battery Cell Selection :**  
 $BATSEL\_2P\# = 1, 2 \text{ Cells}; V_{adj2} = 0.997V \implies I_{charge} = 1.474A$   
 $BATSEL\_2P\# = 0, 4/6 \text{ Cells}; V_{adj2} = 1.636V \implies I_{charge} = 2.498A$

$V_{REF} = 5.0V$   
 $f_{osc}(KHz) = 17000 / RT (KOhm)$   
**Soft start:**  $t_s(s) = 0.13 * CS(uF)$   
 $V_{TH} \text{ of } -IN1: 5V / 62 * (100+62) = 13.06V$   
 $V_{TH} \text{ of } ACIN: 1.25V / 25 * (185+25) = 10.5V$   
Change PR607 and PR608 value

Charging Current :		
4P#	2P#	Icharge
1	0	1.5A
0	1	2.5A
0	0	3.0A

- (7) VR\_VID0 P\_VCORE\_VID0\_10m / PT100 TPC28T  
 (7) VR\_VID1 P\_VCORE\_VID1\_10m / PT101 TPC28T  
 (7) VR\_VID2 P\_VCORE\_VID2\_10m / PT102 TPC28T  
 (7) VR\_VID3 P\_VCORE\_VID3\_10m / PT103 TPC28T  
 (7) VR\_VID4 P\_VCORE\_VID4\_10m / PT104 TPC28T  
 (7) VR\_VID5 P\_VCORE\_VID5\_10m / PT105 TPC28T

