2012 S-Series Richie 13.3"
UMA/DIS Muxless Schematic

Intel Chief River Platform
Ivy Bridge (rPGA989)
Panther Point PCH

REV:-1
2012-03-15

DY:No stuff
DIS_PX:Only DIS install

<Core Design>

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Title: Cover Page		
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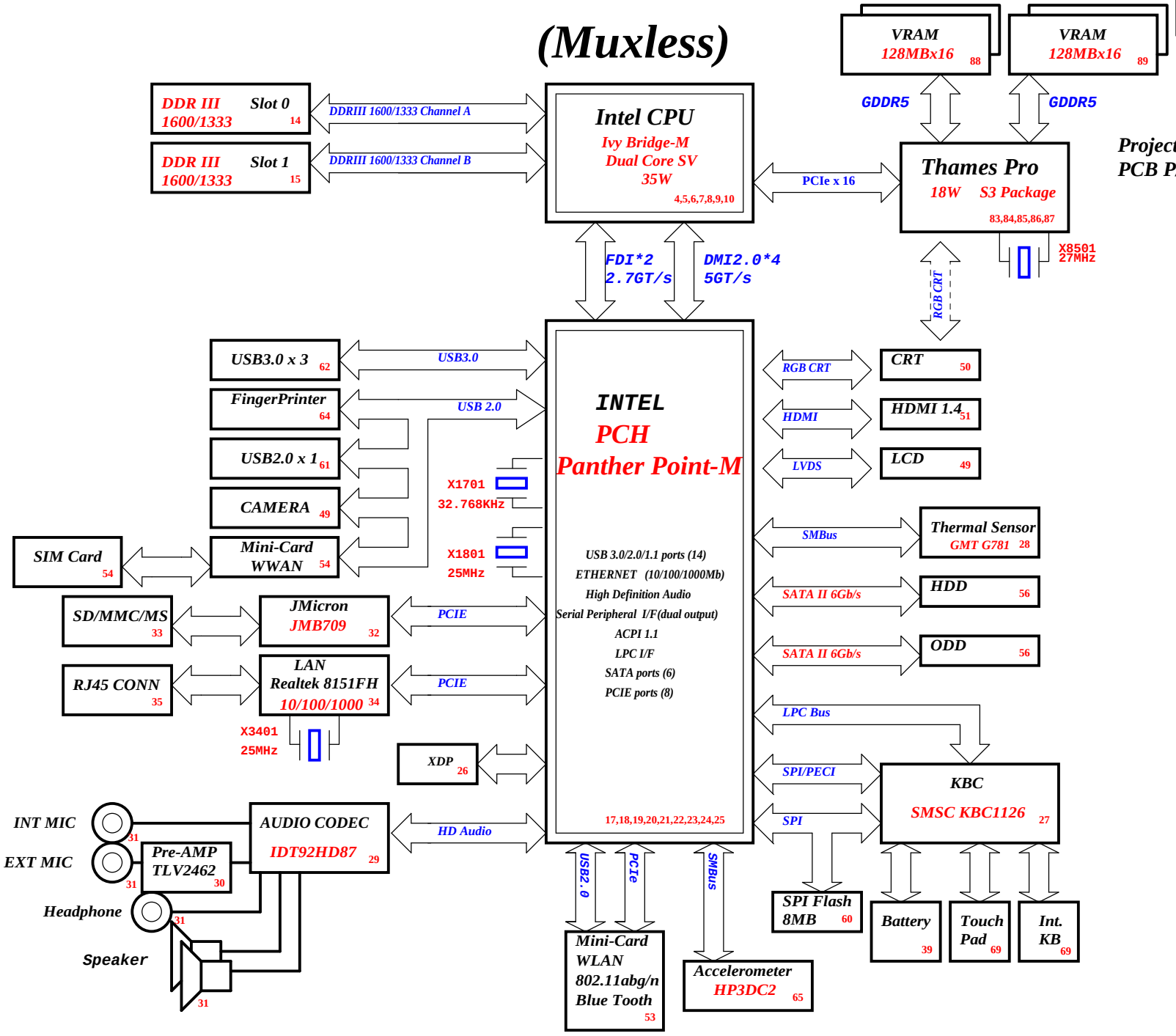
S-Series Richie Block Diagram (Muxless)



Project code:91.4RS01.001
PCB P/N:11241

SYSTEM DC/DC TPS51461RGER 48	
INPUTS	OUTPUTS
DCBATOUT	+VCCSA

CPU DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51211DSCR 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51123RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC TPS51216RUKR 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC ISL95832HRTZ 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA UP1527QQDD 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24736RGRR 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068AZQWID 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC FDMC7696 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB 8 LAYER

L1:	Top
L2:	GND
L3:	Signal
L4:	Signal
L5:	VCC
L6:	Signal
L7:	GND
L8:	Bottom

PCB LAYER

L1:Top	L5:Vcc
L2:GND	L6:Signal
L3:Signal	L7:GND
L4:Signal	L8:Bottom

<Core Design>

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Title: Block Diagram

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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Cougar Point will disable the TCO Timer system reboot feature).
INIT3_3V#	This signal has a weak internal pull-up. Note: The internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low. Leave as "No Connect".
INTVRMEN	Integrated 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high External 1.05 V VRM Enable / Disable. Integrated 1.05 V VRMs is enabled when Low. NOTE: This signal should be pulled down to GND through 330 kOhms resistor
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Used as GPIO only. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
DF_TVS	This signal is a strap for selecting DMI and FDI termination voltage. For Ivy Bridge processor only implementation: DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor. For future processor compatibility: It needs to be connected to PROC_SELECT through a 1.0 kOhms ±5% series resistor. The PROC_SELECT signal would need a 2.2 kOhms ±5% pull-up resistor to PCH VccDFTERM.
SATA1GP/ GPIO19	This Signal has a weak internal pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. This field determines the destination of accesses to the BIOS memory range. Also controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC NOTE: If option 00 LPC is selected BIOS may still be placed on LPC, but all platforms with Cougar Point require SPI flash connected directly to the Cougar Point's SPI bus with a valid descriptor in order to boot. NOTE: Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN. NOTE: PCI Boot BIOS destination is not supported on mobile.
SATA2GP/ GPIO36	Reserved. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled high when strap is sampled.
HDA_DOCK_EN# /GPIO33	High Definition Audio Dock Enable: This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel? HD Audio dock signals to the corresponding Cougar Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Signal has a weak internal pull-down. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default). If sampled high, the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing/debug environments ONLY. Note: The weak internal pull-down is disabled after PLTRST# deasserts. Asserting the HDA_SDO high on the rising edge of RSMRST# will also halt Intel Management Engine after chipset bring up and disable runtime Intel Management Engine features. This is a debug mode and must not be asserted after manufacturing/ debug.
HDA_SYNC	This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V from VCCVRM when sampled high, 1.8 V from VCCVRM when sampled low. Needs to be pulled High for Chief River platform.
GPIO15	TLS Confidentiality Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. NOTE: A strong pull-up may be needed for GPIO functionality
L_DDC_DATA	LVDS Detected. When '1'- LVDS is detected; When '0'- LVDS is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
SDVO_CTRLDATA	Port B Detected When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected. When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts
DDPD_CTRLDATA	Port D Detected. When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
GPIO28	The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail. Note: This signal has a weak internal pull-up. The internal pull-up is disabled after RSMRST# deasserts.
GPIO29/ SLP_LAN#	GPIO29 is multiplexed with SLP_LAN#. If Intel LAN is implemented on the platform, SLP_LAN# must be used to control the power to the PHY LAN (no other implementation is supported). If integrated Intel LAN is not supported on the platform, GPIO29 can be used as a normal GPIO. A soft strap determines the functionality of GPIO29, either as SLP_LAN# or GPIO. By default, the soft strap enables SLP_LAN# functionality on the pin. If the soft trap is changed to enable GPIO functionality, then SLP_LAN# functionality is no longer available, and the signal can be used as a normal GPIO (default to GPI).

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[0]		Connect a series 1K ohm resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.	
CFG[2] CFG2 is for the 16x	**PCIe Static x16 Lane Numbering Reversal.**	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed	1
CFG[4]	**Display Port Presence strap**	1:Disabled - No Physical Display Port attached to Embedded DisplayPort 0:Enabled - An external Display Port device is connected to the Embedded Display Port Pull down to GND through a 1KΩ ± 5% resistor to enable port	1
CFG[6:5]	**PCIE Port Bifurcation Straps**	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express	11
CFG[17:7]	**Reserved configuration lands. A test point may be placed on the board for these lands.**		

PCIe Routing

LANE1	X
LANE2	X
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	LAN
LANE7	X
LANE8	X

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA 0D75V_S0 VCC_CORE VCC_GFXCORE VGA_CORE 1D8V_VGA_S0 3D3V_VGA_S0 1D5V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
1D5V_S3 DDR_VREF_S3	5V 1.5V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	9V-14.1V 9V-19.5V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

USB 2.0 Table

Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	N/A
3	N/A
4	N/A
5	N/A

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address	Hex	Bus
DIMM1 DIMM2 Touch-Pad				PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA PCH_SMB_CLK/PCH_SMB_DATA
N/A				PCH_SML0_CLK/PCH_SML0_DATA
KBC G781_Thermal IC GPU_Thames PRO G-Sensor		 1001100 0X41 0X52		PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA PCH_SML1CLK/PCH_SML1DATA

<Core Design>

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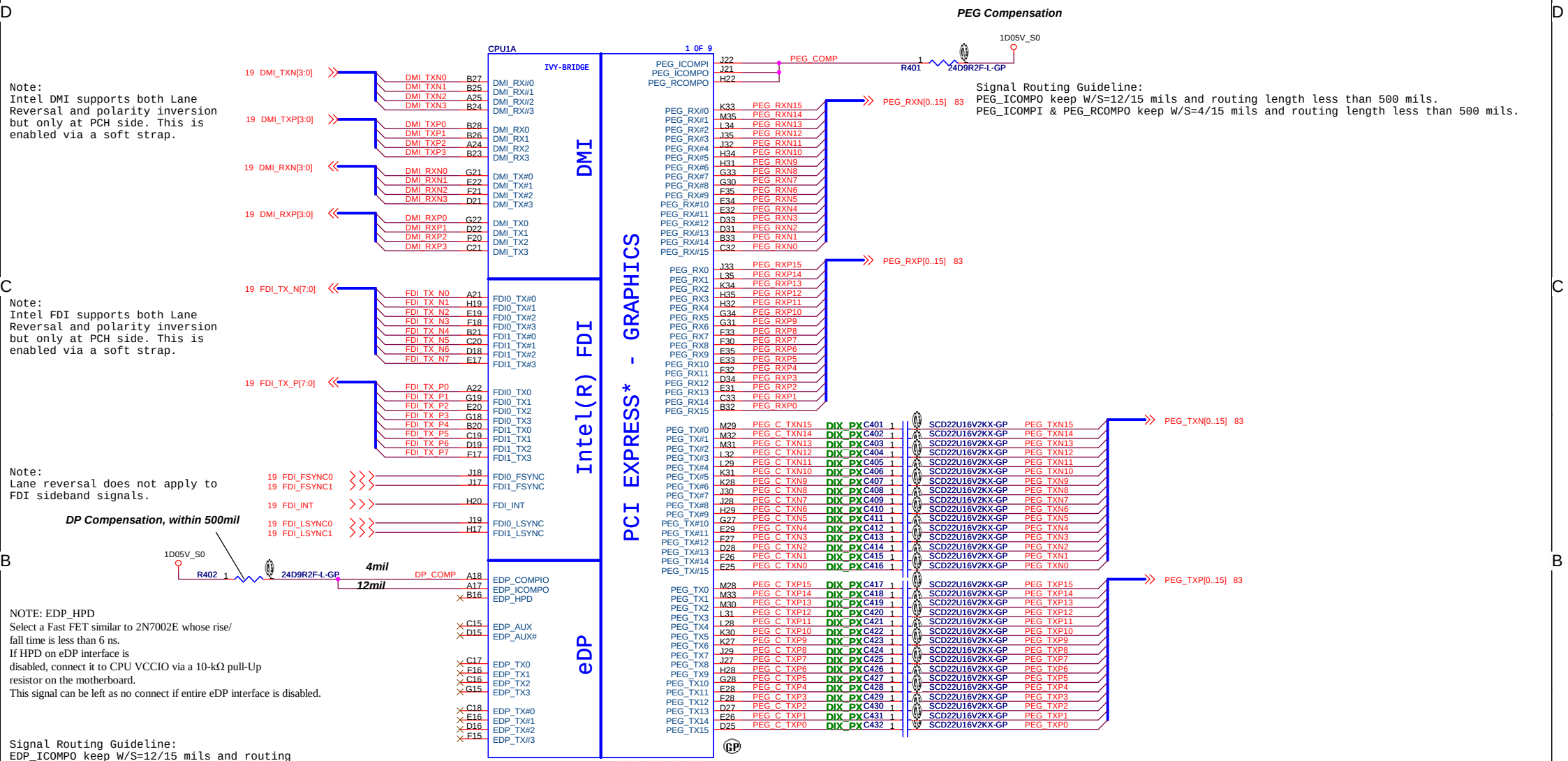
CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)



NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

62.10040.821
1ST = 62.10055.551
2nd = 62.10055.321
3rd = 62.10055.731

BOM Note:1st/2nd/3rd Add in BOM

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Title: **CPU(1/7): DMI/PEG/FDI**

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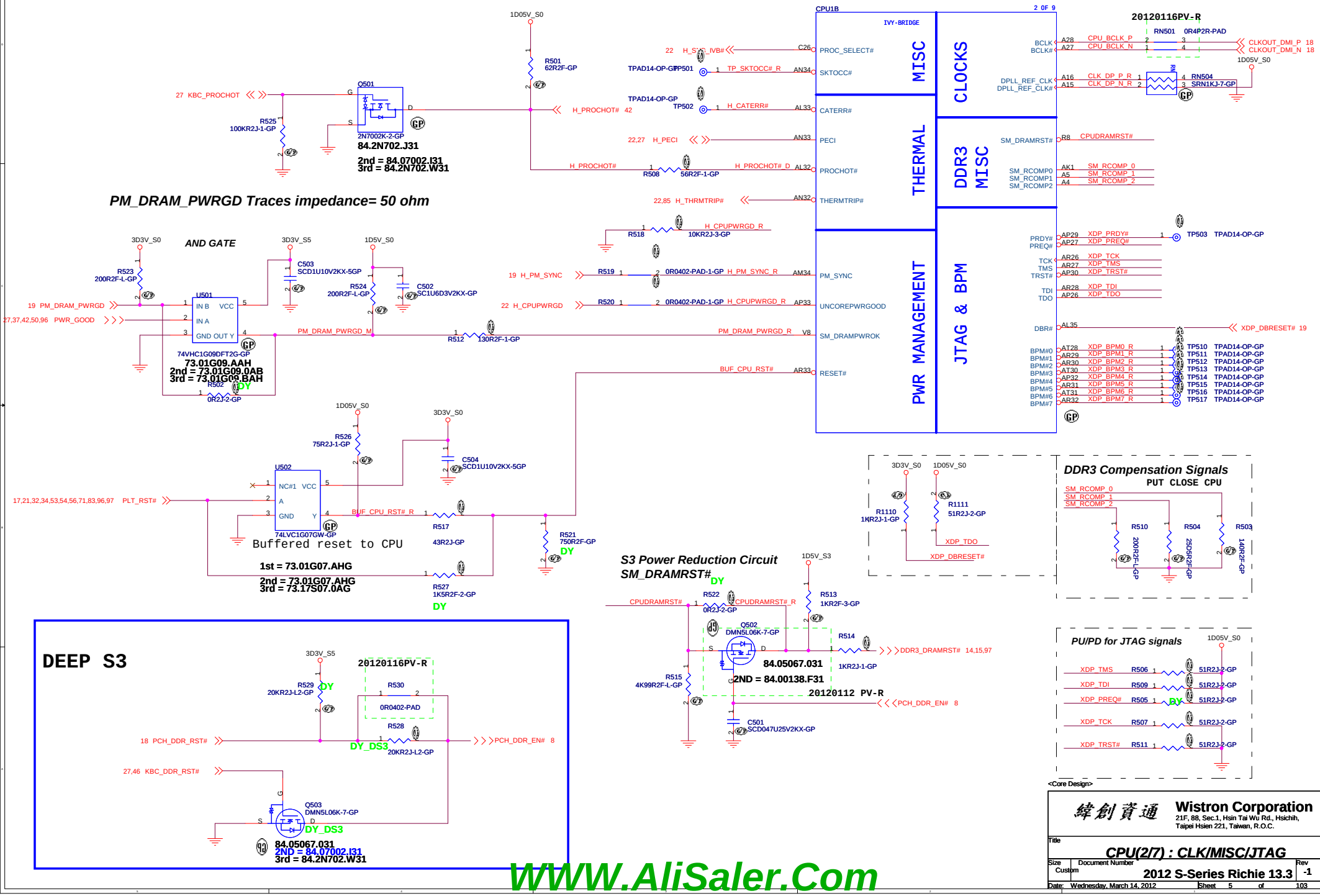
CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



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Title: CPU(2/7) : CLK/MISC/JTAG

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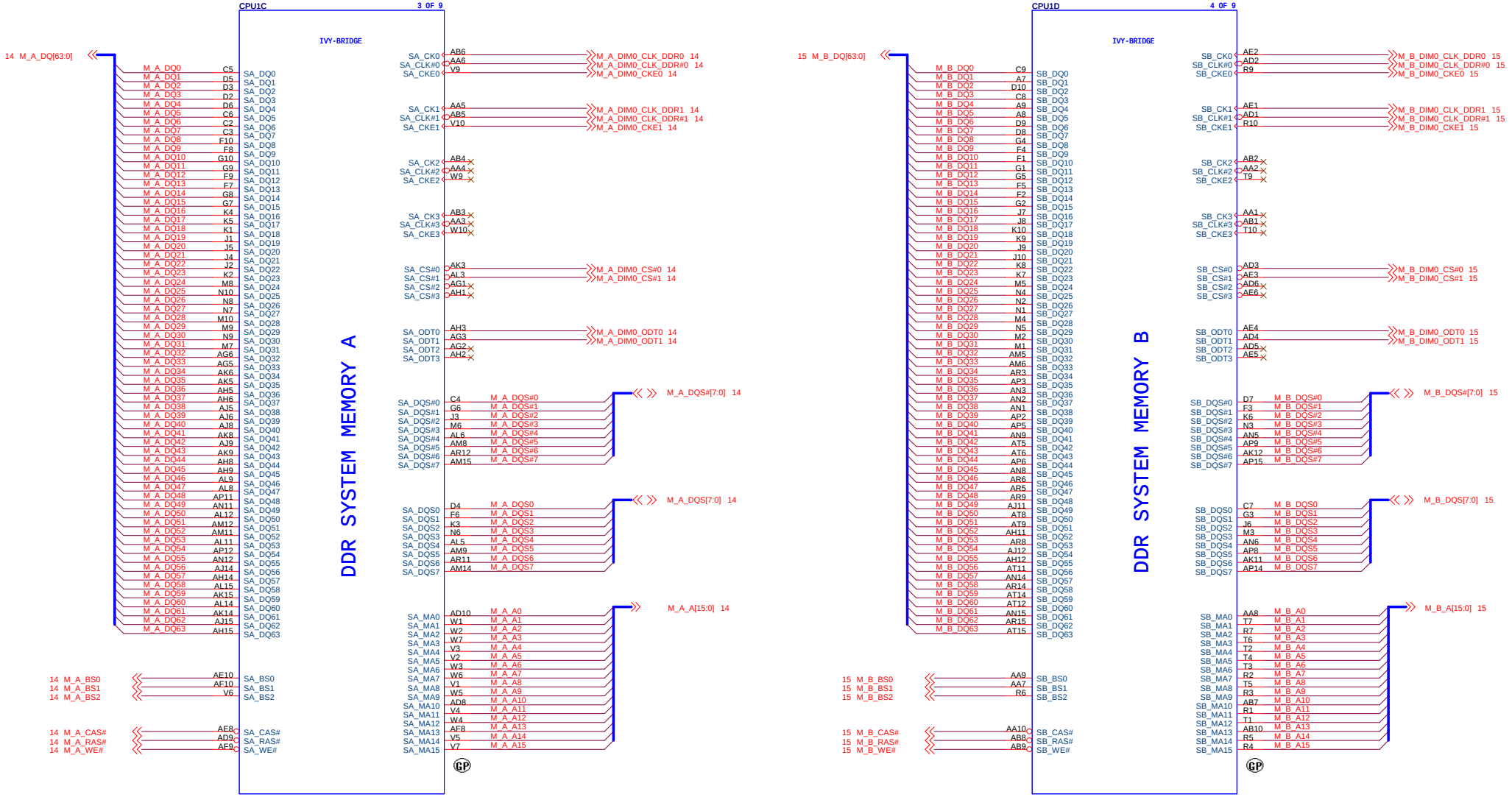
CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



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Title	CPU(3/7) : DDR3	
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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

POWER

CPU1F — 6 OF 9 — IVY-BRIDGE

PROCESSOR CORE POWER

53A

VCC_CORE

Place Bottom

Place Top

C713 C722 C727 C736 C714 — SC22U6D3V5MX-2GP / SC10U6D3V3MX-GP

C735 C721 C726 C728 C723 — SC22U6D3V5MX-2GP / SC10U6D3V3MX-GP

C742 C701 C741 C703 C709 — SC22U6D3V5MX-2GP / SC10U6D3V5KX-1GP / SC10U6D3V3MX-GP

C738 C702 C706 C707 C708 — SC10U6D3V5KX-1GP

C740 C739 C704 C712 C710 C711 — SC22U6D3V5MX-2GP

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

CORE SUPPLY

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C729 C730 C731 C732 C715 C716 C717 C718 C733 C734 C719 C720 — SC10U6D3V3MX-GP / SC22U6D3V5MX-2GP

PEG AND DDR

SVID

Route these three net together

VIDALERT# AJ29 H_CPU_SVIDALRT# — R705 1 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 H_CPU_SVIDCLK — H_CPU_SVIDCLK 42
VIDSOUT AJ28 H_CPU_SVIDDAT — H_CPU_SVIDDAT 42

R703 1 130R2F-1-GP 1D05V_S0

SENSE LINES

reserve PAD for ESD

DY 0R2J-2-GP D701
DY 0R2J-2-GP D702

VCC_CORE

PUT CLOSE CPU

R706 100R2F-L1-GP-U

VCC_SENSE AJ35 VCCSENSE — VCCSENSE 42
VSS_SENSE AJ34 VSSSENSE — VSSSENSE 42

R704 100R2F-L1-GP-U

VCCIO_SENSE B10 — VTT_SENSE 45
VSS_SENSE_VCCIO A10 — VSSP_SENSE 45

R707 10R2F-L-GP R708 10R2F-L-GP 1D05V_S0

PUT CLOSE CPU

Differential Sense feedback

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Title: CPU(4/7) : PWR

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CPU(5/7)

IVY BRIDGE PROCESSOR (GRAPHICS POWER)

33A

POWER

Under Socket and Closed to CPU

Closed to CPU Socket

CPU1G 7 OF 9

IVY-BRIDGE

GRAPHICS

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

1.8V RAIL

MISC

M3 - Processor Generated SO-DIMM VREF_DQ

reserve PAD for ESD

CAD Note: +V_SM_VREF should have 10 mil trace width

B4:VREF_DQ CHA
D1:VREF_DQ CHB

12~16A

330U*1 10U*6

1D5V_S0

TC803 ST330U2D5VBM-1-GP
80.3371V.A2L
2nd = 77.22771.00L
20120131PVR

6A

VCCSA

1st = 77.23371.13L
2ND = 79.33719.L01

R0801 need be close to pin H23.

1.5A

1D8V_S0

SNB: No Connect
IVB: VSS

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

S3 Power Reduction Circuit Processor VREF_DQ Implementation

20120112 PV-R

84.05067.031
1st = 84.2N702.J31
2ND = 84.07002.I31
3rd = 84.2N702.W31

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Title: CPU(5/7) : GFX/PWR

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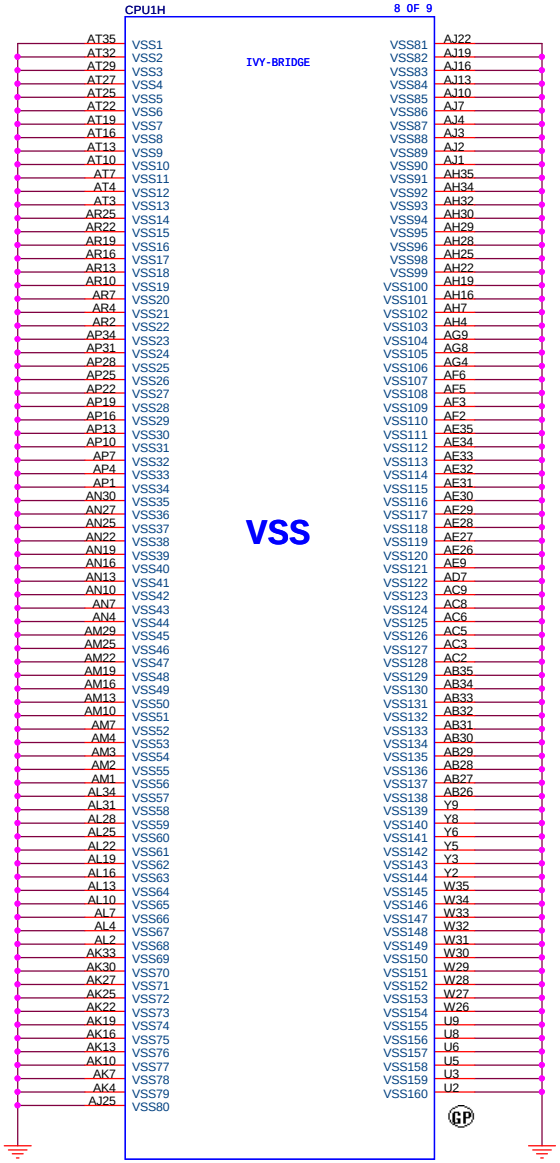
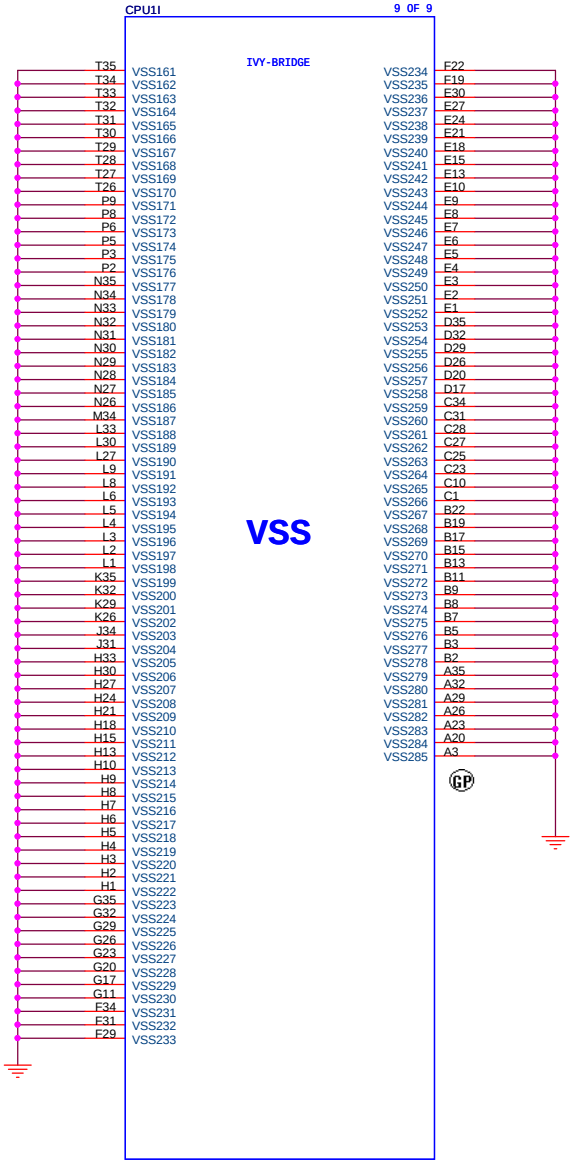
CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





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Title	CPU(6/7) : GND	
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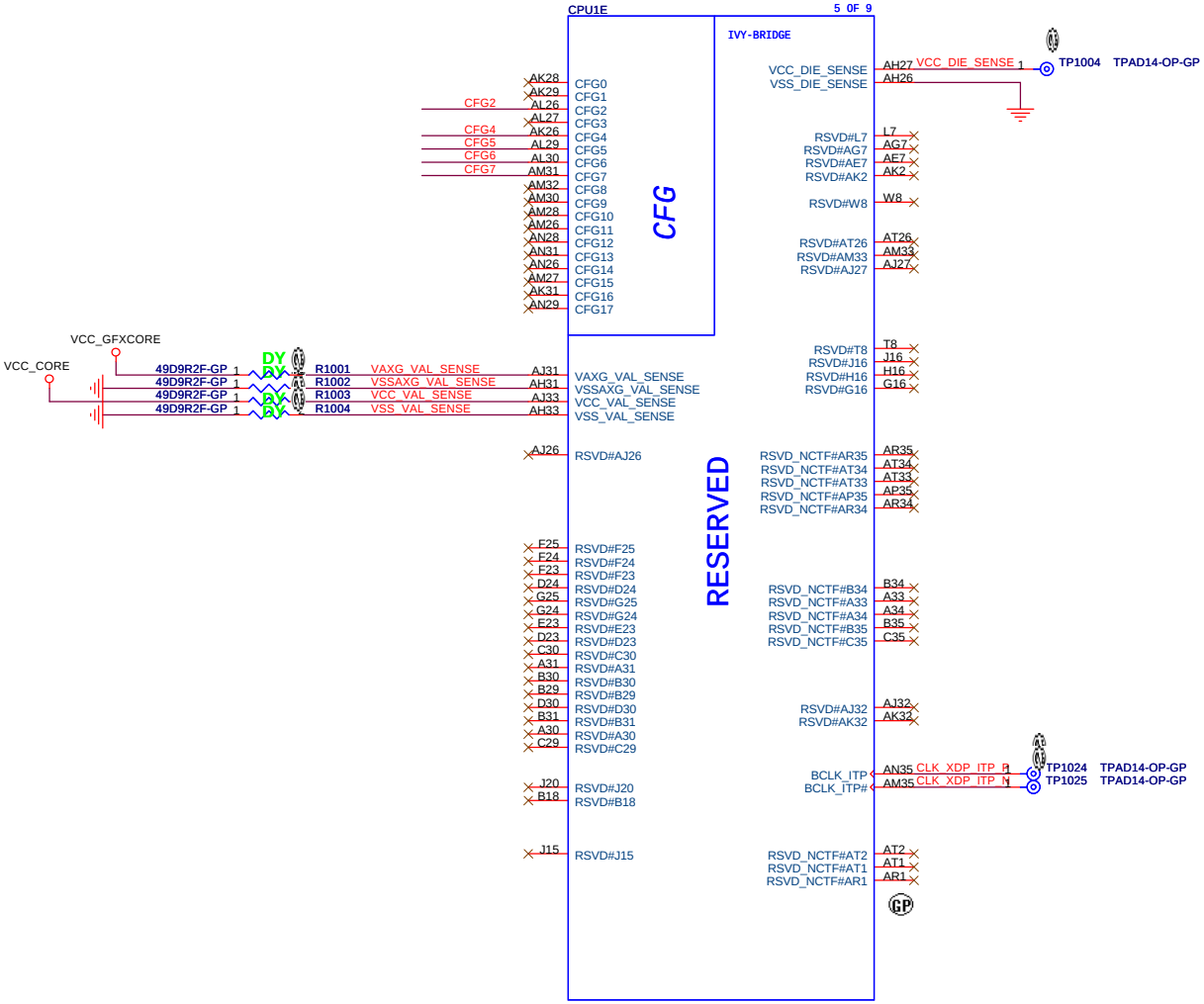
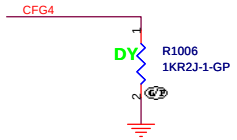
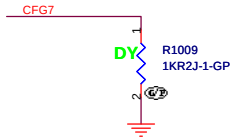
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

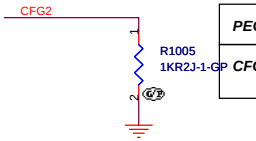




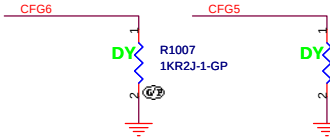
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(7/7): CFG/RSVD/DDR3_VREF

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 10 of 103

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<Core Design>

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Title: CPU XDP

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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Title: RESERVED

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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Title: ***RESERVED***

Size	Document Number	Rev
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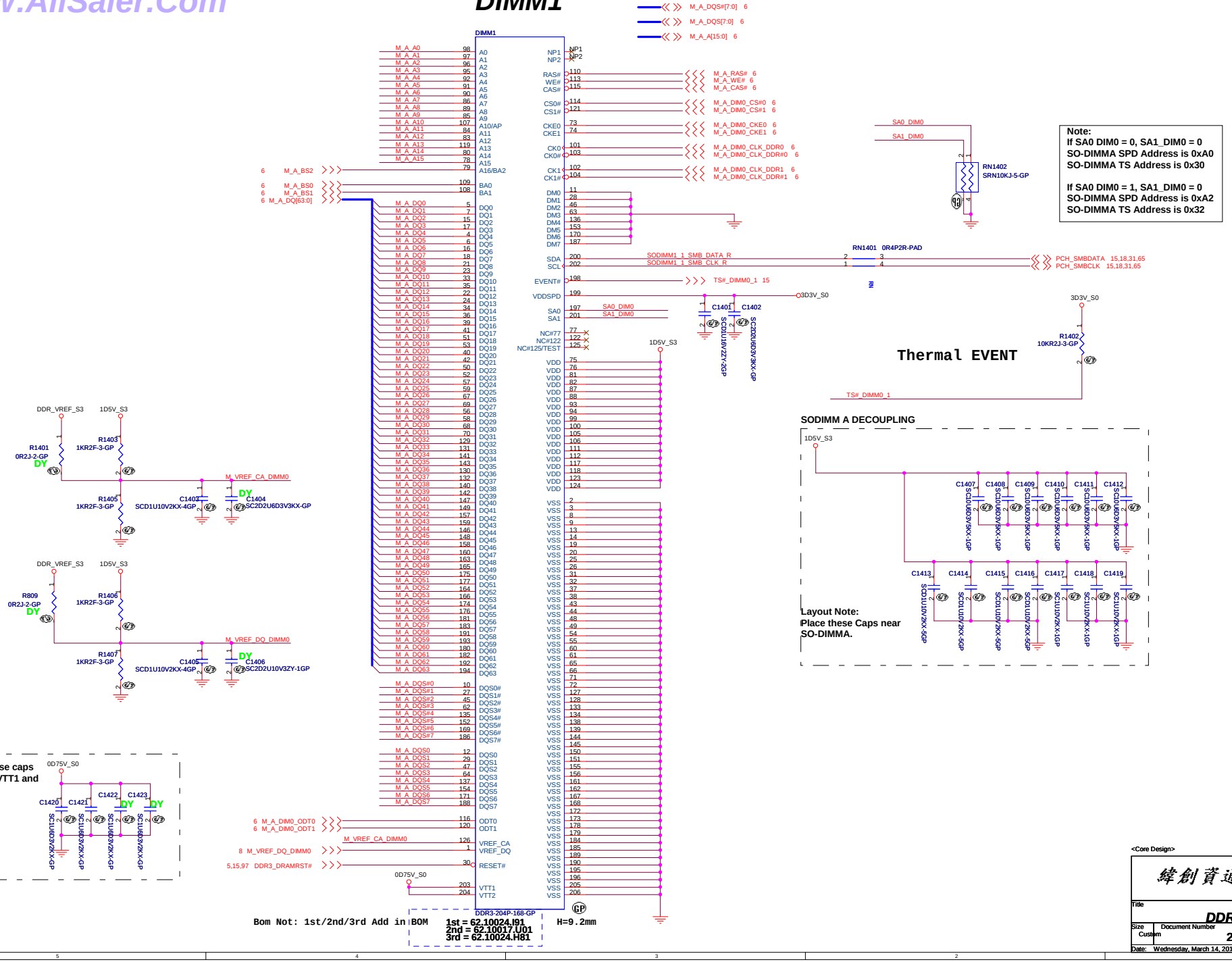
DIMM1



<Core Design>
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Title: DDR3 SO-DIMM1

Size	Document Number	Rev
Custom	2012 S-Series Richie 13.3	-1

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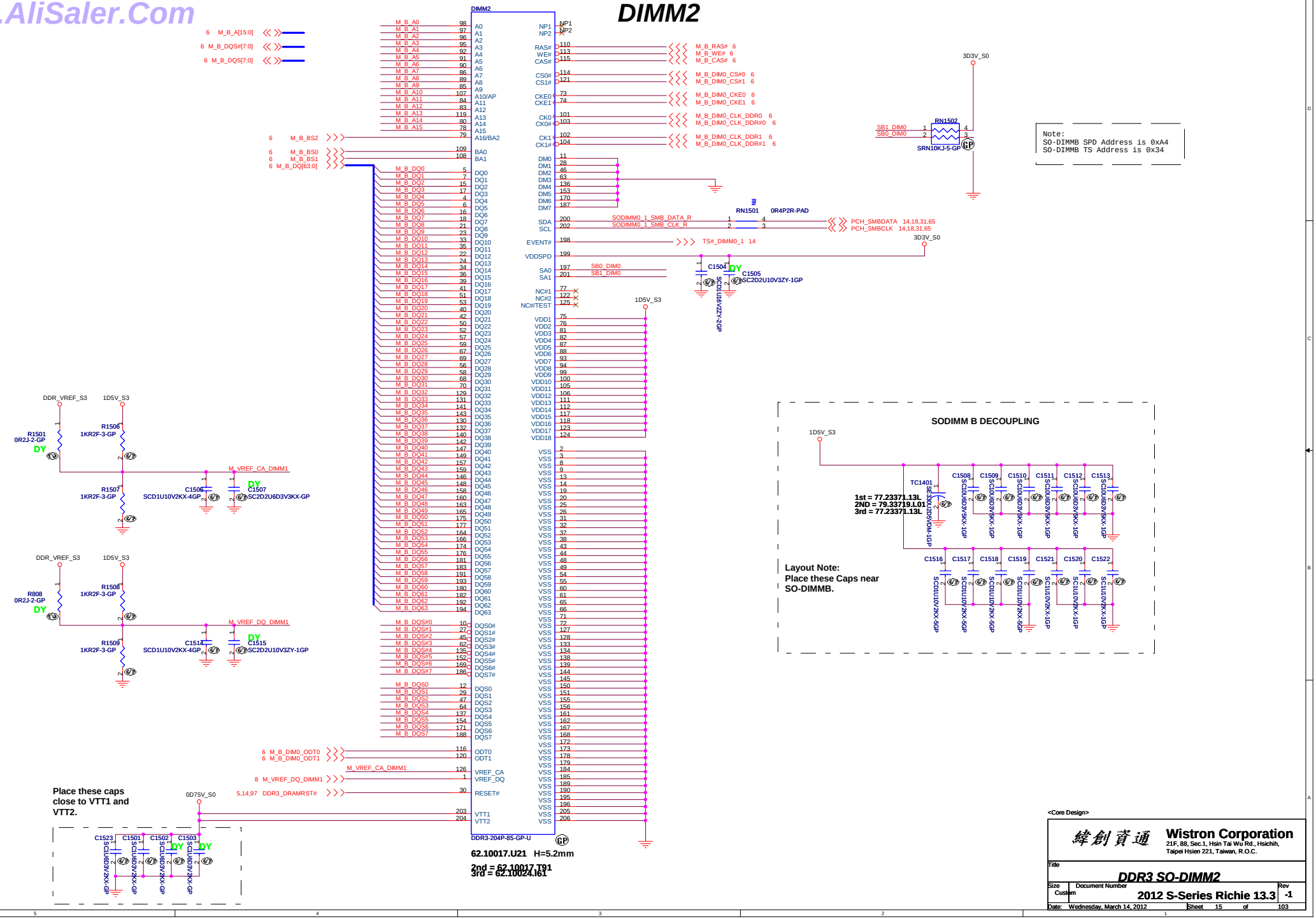
DIMM2



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Title: RESERVED

Size	Document Number	Rev
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PCH(1/9)

INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A 1 OF 10

RTC_X1 A20 RTCX1
RTC_X2 C20 RTCX2
RTC_RST# D20 RTCRST#
SRTC_RST# G22 SRTCRST#
54,97 INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

LPC_AD[3:0] 27,71
FWH0/LAD0 C38 LPC_AD0
FWH1/LAD1 A38 LPC_AD1
FWH2/LAD2 B37 LPC_AD2
FWH3/LAD3 C37 LPC_AD3
FWH4/LFRAME# D36 LPC_FRAME# R 1 R1726 22R2J-2-GP LPC_FRAME# 27,71
LDRQ0# E36
LDRQ1#/GPIO23 K36 PCH_GPIO23 1 TP1701 TPAD14-OP-GP
SERIRQ V5 SIRQ 27,71
LPC

29,97 HDA_SDOUT_CODEC
29,97 HDA_BITCLK_CODEC
29,97 HDA_RST#_CODEC
29 HDA_SYNC_CODEC
29 HDA_SPKR
HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
PCH_HDA_SPKR T10 SPKR
PCH_HDA_RST# K34 HDA_RST#
HDA_SYNC_C
E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDO_R
HDA_SDO A36 HDA_SDO
HDA_DOCK_EN#/GPIO33 C36
ISO_PREP# N32 HDA_DOCK_RST#/GPIO13
IHDA

SATA0RXN AM3 SATA_RXN0 56
SATA0RXP AM1 SATA_RXP0 56
SATA0TXN AP7 SATA_TXN0 56
SATA0TXP AP5 SATA_TXP0 56
HDD
SATA1RXN AM10 SATA_RXN1 56
SATA1RXP AM8 SATA_RXP1 56
SATA1TXN AP11 SATA_TXN1 56
SATA1TXP AP10 SATA_TXP1 56
ODD
SATA 6G

SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATA

PCH_JTAG_TCK_BUF J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

60 PCH_SPI_CLK T3 SPI_CLK
60 PCH_SPI_CS#0 Y14 SPI_CS0#
27,71 SPI_CS1# T1 SPI_CS1#
60 PCH_SPI_MOSI V4 SPI_MOSI
60 PCH_SPI_MISO U3 SPI_MISO
SPI

SATAICOMPO Y11
SATAICOMPI Y10 SATA_COMP R1713 1 2 37D4R2F-GP 1D05V_S0
SATA3RCOMPO AB12
SATA3COMPI AB13 SATA3_COMP R1714 1 2 49D9R2F-GP 1D05V_S0
SATA3RBIAS AH1 RBIAS_SATA3 R1715 1 2 750R2F-GP
NEED TO PLACE CLOSE TO PCH
SATALED# P3 SATA_LED# SATA_LED# 68
SATA0GP/GPIO21 V14 SATA0GP_GPIO21 22
SATA1GP/GPIO19 P1 SATA_ODD_DET# 56

PANTHER-GP-NF

RTC_X1 R1706 10MR2J-L-GP RTC_X2
X1701 X-32D768KHZ-34GPU
C1702 C1703 7pF20PPM SC68P50V2CN-1GP
82.30001.661
2ND = 82.30001.B21
20120312MV

RTC_AUX_S5 R1705 20KR2J-L2-GP C1701 SC1U10V2KX-1GP
R1708 20KR2J-L2-GP C1704 SC1U10V2KX-1GP G1701 GAP-OPEN
R1709 1MR2J-1-GP
R1710 330KR2J-L1-GP PCH_INTVRMEN
DY R1707 330KR2J-L1-GP PCH_INTVRMEN

RN1701 SRN33J-7-GP
R1711 0R0402-PAD
20120112 PV-R

3D3V_S5 R1725 1KR2J-1-GP
68 HDD_HALTLED
1KR2J-1-GP R1712 HDD_HALTLED_R

BAT_GRNLED# S
BAT_GRNLED# D
10KR2J-3-GP R1701
27,82 BAT_GRNLED# BAT_GRNLED# G
BSS84-7-F-GP Q1701
84.00084.F31
2nd = 84.BSS84.B31

10KR2J-3-GP R1702
5,21,32,34,53,54,56,71,83,96,97 PLT_RST# PLT_RST# G
BSS84-7-F-GP Q1702
84.00084.F31
2nd = 84.BSS84.B31

For Flash Descriptor Security Override HW strap

3D3V_S5 R1724 1KR2J-1-GP HDA_SYNC
R1729 10KR2J-3-GP ISO_PREP#

3D3V_S0 R1716 10KR2J-3-GP

RTC Battery

3D3V_AUX_S5 U1701 CH715FGP-GP-U RTC_AUX_S5
+RTC_VCC R1720 RTC_PWR 1KR2J-1-GP
C1705 SC1U10V3ZY-6GP
RTC1 PWR GND NP1 NP2 BAT-060003HA02M213ZL-GP-U
83.R0304.D81
2ND = 83.00040.E81
20120210PV-R
62.70014.001
2nd = 62.70001.061
20120314 MV
20120315 MV

NO REBOOT STRAP

No Reboot Strap R710	
HDA_SPKR	Low = Default High = No Reboot

3D3V_S0 R1722 10KR2J-3-GP HDA_SPKR
DY
R1723 10KR2J-3-GP SIRQ

5V_S0 RN1702 SRN10KJ-5-GP
HDA_SDO_G U1704 2N7002KDW-GP HDA_SDO_G
HDA_SYNC_C HDA_SYNC
HDA_SDO HDA_SDO_R
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

3D3V_S5
PCHXDP R1717 210R2F-L-GP PCH_JTAG_TMS
PCHXDP R1718 210R2F-L-GP PCH_JTAG_TDO
PCHXDP R1719 210R2F-L-GP PCH_JTAG_TDI
RN1703
PCHXDP
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TMS
SRN100J-4-GP
PCHXDP R1721 51R2J-2-GP PCH_JTAG_TCK_BUF
R1727 DY 1KR2J-1-GP HDD_HALTLED_R
R1728 20KR2J-L2-GP HDA_SDO

LAYOUT NOTE:
JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

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Title: PCH(1/9) : HDA/JTAG/SATA	
Size: A3	Document Number: 2012 S-Series Richie 13.3
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Date: Wednesday, March 14, 2012	Sheet 17 of 103

PCH(2/9)

PCH1B — 2 OF 10 — PANTHER-GP-NF

PCI-E*

Media	32 PCIE_RXN3_MEDIA	C1805	SCD1U10V2KX-5GP PCIE_TXN3_C
	32 PCIE_RXP3_MEDIA	C1806	SCD1U10V2KX-5GP PCIE_TXP3_C
	32 PCIE_TXN3_MEDIA		
	32 PCIE_TXP3_MEDIA		
WLAN	53 PCIE_RXN4_WLAN	C1809	SCD1U10V2KX-5GP PCIE_TXN4_C
	53 PCIE_RXP4_WLAN	C1807	SCD1U10V2KX-5GP PCIE_TXP4_C
	53 PCIE_TXN4_WLAN		
	53 PCIE_TXP4_WLAN		
LAN	34 PCIE_RXN6_LAN	C1810	SCD1U10V2KX-5GP PCIE_TXN6_C
	34 PCIE_RXP6_LAN	C1811	SCD1U10V2KX-5GP PCIE_TXP6_C
	34 PCIE_TXN6_LAN		
	34 PCIE_TXP6_LAN		

PERN1 PERP1 PETN1 PETP1 — PERN2 PERP2 PETN2 PETP2 — PERN3 PERP3 PETN3 PETP3 — PERN4 PERP4 PETN4 PETP4 — PERN5 PERP5 PETN5 PETP5 — PERN6 PERP6 PETN6 PETP6 — PERN7 PERP7 PETN7 PETP7 — PERN8 PERP8 PETN8 PETP8

SMBUS

SMBALERT#/GPIO11	E12	FPR_OFF 64,97
SMBCLK	H14	PCH_SMB_CLK
SMBDATA	C9	PCH_SMB_DATA
SML0ALERT#/GPIO60	A12	PCH_DDR_RST# 5
SML0CLK	C8	PCH_SML0_CLK
SML0DATA	G12	PCH_SML0_DATA
SML1ALERT#/PCHHOT#/GPIO74	C13	PCH_GPIO74
SML1CLK/GPIO58	E14	PCH_SML1CLK
SML1DATA/GPIO75	M16	PCH_SML1DATA

R1806 10KR2J-3-GP (3D3V_S5) — R1807 1KR2J-1-GP (3D3V_S5) — R1801 10KR2J-3-GP (3D3V_S5)

RN1803 SRN2K2J-1-GP (3D3V_S0) — U1801 2N7002KDW-GP (GP) — 84.2N702.A3F / 2nd = 84.2N702.E3F / 3rd = 84.2N702.F3F

14,15,31,65 PCH_SMBDATA — PCH_SMB_DATA — PCH_SMB_CLK — PCH_SMBCLK 14,15,31,65

Controller Link

CL_CLK1	M7	
CL_DATA1	T11	
CL_RST1#	P10	

84.2N702.J31 / 2nd = 84.07002.I31 / 3rd = 84.2N702.W31 — 2N7002K-2-GP — Q1801 — DIS_PX — PE_PWRGD 22,86,92,93,96,97

RN1802 SRN2K2J-4-GP (3D3V_AUX_S5, 3D3V_S5) — PCH_SML1DATA — PCH_SML1CLK

U1802 2N7002KDW-GP (GP) — PCH_SML1DATA — PCH_KBC_DATA 27,28,85 — PCH_SML1CLK — 27,28,85 PCH_KBC_CLK

84.2N702.A3F / 2nd = 84.2N702.E3F / 3rd = 84.2N702.F3F

RN1801 SRN2K2J-4-GP (3D3V_S5) — PCH_SML0_DATA — PCH_SML0_CLK — PCH_SMB_CLK — PCH_SMB_DATA

CLOCKS

PEG_A_CLKRQ#/GPIO47	M10	CLKREQ_PEG_A#
CLKOUT_PEG_A_N	AB37	CLKOUT_PEG_A_N
CLKOUT_PEG_A_P	AB38	CLKOUT_PEG_A_P
CLKOUT_DMI_N	AV22	CLKOUT_DMI_N 5
CLKOUT_DMI_P	AU22	CLKOUT_DMI_P 5
CLKOUT_DP_N	AM12	
CLKOUT_DP_P	AM13	
CLKIN_DMI_N	BF18	CLK_BUF_EXP_N
CLKIN_DMI_P	BE18	CLK_BUF_EXP_P
CLKIN_GND1_N	BJ30	CLK_BUF_CPYCLK_N
CLKIN_GND1_P	BG30	CLK_BUF_CPYCLK_P
CLKIN_DOT_96N	G24	CLK_BUF_DOT96_N
CLKIN_DOT_96P	E24	CLK_BUF_DOT96_P
CLKIN_SATA_N	AK7	CLK_BUF_CKSSCD_N
CLKIN_SATA_P	AK5	CLK_BUF_CKSSCD_P
REFCLK14IN	K45	CLK_BUF_REF14
CLKIN_PCILOOPBACK	H45	
XTAL25_IN	V47	XTAL25_IN
XTAL25_OUT	V49	XTAL25_OUT
XCLK_RCOMP	Y47	XCLK_RCOMP

R1808 10KR2J-3-GP — RN1810 0R4P2R-PAD — 20120116PV-R — CLK_PCIE_VGA# 83 / CLK_PCIE_VGA 83

CLOCK TERMINATION FOR FCIM

RN1806 SRN10KJ-5-GP — RN1807 SRN10KJ-5-GP — RN1808 SRN10KJ-5-GP — RN1809 SRN10KJ-5-GP

R1802 10KR2J-3-GP — All resistors need very close to PCH — CLK_PCI_FB 21

R1803 90D9R2F-1-GP (1D05V_S0)

CLKOUT_PCIE0N	Y40	
CLKOUT_PCIE0P	Y39	
PCIECLKRQ0#/GPIO73	J2	GPIO73
CLKOUT_PCIE1N	AB49	
CLKOUT_PCIE1P	AB47	
PCIECLKRQ1#/GPIO18	M1	54 WWAN_DET# — R1804 0R2J-2-GP — GPIO18
CLKOUT_PCIE2N	AA48	
CLKOUT_PCIE2P	AA47	
PCIECLKRQ2#/GPIO20	V10	GPIO20
CLKOUT_PCIE3N	Y37	32 CLK_PCIE_MEDIA#
CLKOUT_PCIE3P	Y36	32 CLK_PCIE_MEDIA
PCIECLKRQ3#/GPIO25	A8	32 CLKREQ_MEDIA#
CLKOUT_PCIE4N	Y43	53 CLK_PCIE_WLAN#
CLKOUT_PCIE4P	Y45	53 CLK_PCIE_WLAN
PCIECLKRQ4#/GPIO26	L12	53 CLKRQ_WLAN#
CLKOUT_PCIE5N	V45	
CLKOUT_PCIE5P	V46	
PCIECLKRQ5#/GPIO44	L14	GPIO44
CLKOUT_PEG_B_N	AB42	
CLKOUT_PEG_B_P	AB40	
PEG_B_CLKRQ#/GPIO56	E6	GPIO56
CLKOUT_PCIE6N	V40	34 CLK_PCIE_LAN#
CLKOUT_PCIE6P	V42	34 CLK_PCIE_LAN
PCIECLKRQ6#/GPIO45	T13	34 CLKREQ_LAN#
CLKOUT_PCIE7N	V38	
CLKOUT_PCIE7P	V37	
PCIECLKRQ7#/GPIO46	K12	CLKRQ_WWAN#
CLKOUT_ITPXDP_N	AK14	TPAD14-OP-GP TP1805 — PCIE_CLK_XDP_N
CLKOUT_ITPXDP_P	AK13	TPAD14-OP-GP TP1806 — PCIE_CLK_XDP_P

FLEX CLOCKS

CLKOUTFLEX0/GPIO64	K43	CLK_48_USB30 — TP1801 TPAD14-OP-GP
CLKOUTFLEX1/GPIO65	F47	CLK_27_NSSC — TP1802 TPAD14-OP-GP
CLKOUTFLEX2/GPIO66	H47	CLK_48_KBC_PCH_SIO — TP1803 TPAD14-OP-GP
CLKOUTFLEX3/GPIO67	K49	CLK_14M_KBC_P — TP1804 TPAD14-OP-GP

<Core Design>

RN1804 SRN10KJ-L3-GP (3D3V_S5): CLKREQ_LAN# PCH_GPIO74 GPIO44 CLKRQ_WWAN# — CLKRQ_WLAN# GPIO56 CLKREQ_MEDIA# GPIO73

RN1805 SRN10KJ-5-GP (3D3V_S0): GPIO18 GPIO20

XTAL25_IN — R1805 1MR2J-1-GP — X1801 XTAL-25MHZ-155-GP — 82.30020.D41 / 2nd = 82.30020.G71 / 3rd = 82.30020.G61 — C1801 SC15P50V2JN-2-GP — C1802 SC18P50V2JN-1-GP — XTAL25_OUT

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Title	PCH : PCI/USB/NVRAM/RSVD
Size A3	Document Number 2012 S-Series Richie 13.3
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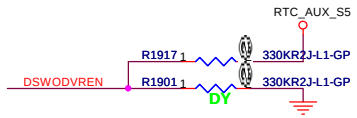
Date: Wednesday, March 14, 2012	Sheet 18 of 103

PCH(3/9)

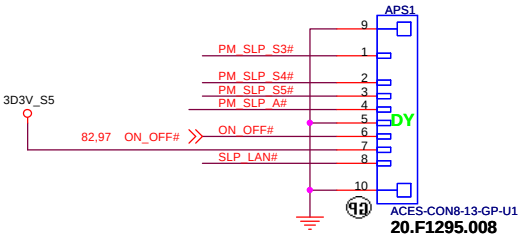
DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1901 STUFFED, R1917 UNSTUFFED	Disabled



Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

AMT/ME COMPLIANCY TEST CONN.



<Core Design>

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Title: PCH(3/9) : DMI/FDI/PM

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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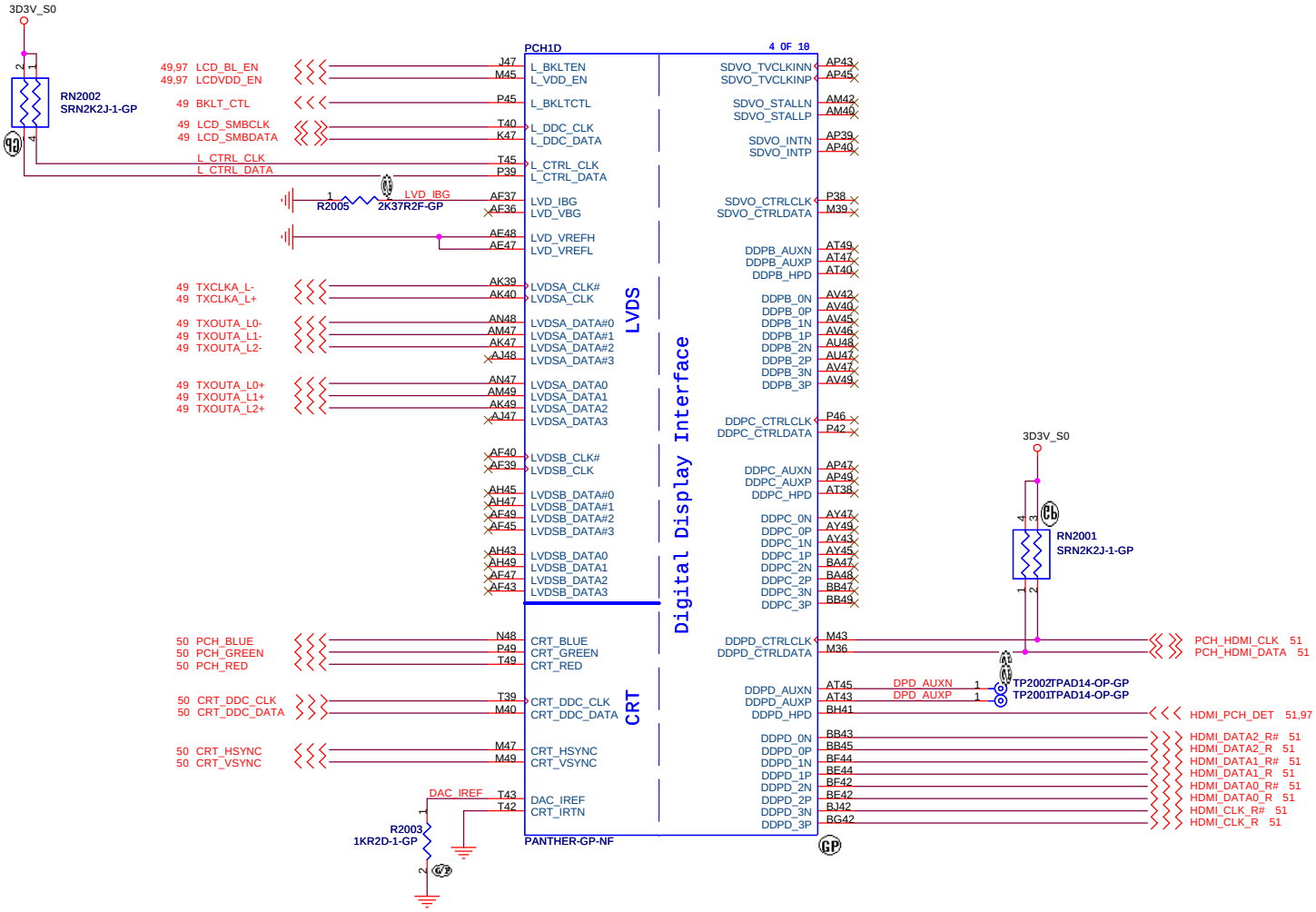
PCH(4/9)



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH(4/9) : LVDS/CRT/DDI**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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PCH(5/9)

GPIO Table

S 2012 Chief River	PCH GPIO 52
Richie U&D (13 inches)	1
Rocky U&D (14 inches)	1
Rocky U&D (15/17 inches)	0

Boot BIOS Strap

GNT1#/GPIO51	SATA1GP#/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI(Default)

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

USB3.0 Table

USB	
Pair	Device
1	FREE
2	I/O CONN. 1
3	I/O CONN. 2
4	I/O CONN. 3

USB2.0 Table

USB	
Pair	Device
0	FREE
1	USB 3.0 I/O CONN. 1
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN. 1
10	Camera
11	FREE
12	WWAN
13	FREE

PCH1E — 5 OF 10

RSVD: RSVD1 AY7, RSVD2 AV7, RSVD3 AU3, RSVD4 BG4, RSVD5 AT10, RSVD6 BC8, RSVD7 AU2, RSVD8 AT4, RSVD9 AT3, RSVD10 AT1, RSVD11 AY3, RSVD12 AT5, RSVD13 AV3, RSVD14 AV1, RSVD15 BB1, RSVD16 BA3, RSVD17 BB5, RSVD18 BB3, RSVD19 BB7, RSVD20 BE8, RSVD21 BD4, RSVD22 BF6, RSVD23 AV5, RSVD24 AV10, RSVD25 AT8, RSVD26 AY5, RSVD27 BA2, RSVD28 AT12, RSVD29 BF3

TP1 BG26, TP2 BJ26, TP3 BH25, TP4 BJ16, TP5 BG16, TP6 AH38, TP7 AH37, TP8 AK43, TP9 AK45, TP10 C18, TP11 N30, TP12 H3, TP13 AH12, TP14 AM4, TP15 AM5, TP16 Y13, TP17 K24, TP18 L24, TP19 AB46, TP20 AB45, TP21 B21, TP22 M20, TP23 AY16, TP24 BG46

USB3RN1 BE28, USB3RN2 BC30, USB3RN3 BE32, USB3RN4 BJ32, USB3RP1 BC28, USB3RP2 BE30, USB3RP3 BE32, USB3RP4 BG32, USB3TN1 AV26, USB3TN2 BB26, USB3TN3 AU28, USB3TN4 AY30, USB3TP1 AU26, USB3TP2 AY26, USB3TP3 AV28, USB3TP4 AW30

62 USB3_RXN2, 62 USB3_RXN3, 62 USB3_RXN4, 62 USB3_RXP2, 62 USB3_RXP3, 62 USB3_RXP4, 62 USB3_TXN2, 62 USB3_TXN3, 62 USB3_TXN4, 62 USB3_TXP2, 62 USB3_TXP3, 62 USB3_TXP4

USBP0N C24, USBP0P A24, USBP1N C25, USBP1P B25, USBP2N C26, USBP2P A26, USBP3N K28, USBP3P H28, USBP4N E28, USBP4P D28, USBP5N C28, USBP5P A28, USBP6N C29, USBP6P B29, USBP7N N28, USBP7P M28, USBP8N L30, USBP8P K30, USBP9N G30, USBP9P E30, USBP10N C30, USBP10P A30, USBP11N L32, USBP11P K32, USBP12N G32, USBP12P E32, USBP13N C32, USBP13P A32

USB_PN1 62, USB_PP1 62, USB_PN2 62, USB_PP2 62, USB_PN3 62, USB_PP3 62 — **USB 3.0 Conn. 1 / USB 3.0 Conn. 2 / USB 3.0 Conn. 3**

USB_PN5 53, USB_PP5 53 — **BT WLAN combo**

USB_PN8 64, USB_PP8 64, USB_PN9 61, USB_PP9 61, USB_PN10 49, USB_PP10 49 — **Fingerprint / USB 2.0 Conn. 1 / Camera**

USB_PN12 54, USB_PP12 54 — **WWAN**

USBRBIAS# C33 — USB_BIAS — R2101 1 — 22D6R2F-L1-GP

USBRBIAS B33

PCI: INT_PIRQA# K40, INT_PIRQB# K38, INT_PIRQC# H38, INT_PIRQD# G38, PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#

CLKOUT_PCI0 H49, CLKOUT_PCI1 H43, CLKOUT_PCI2 J48, CLKOUT_PCI3 K42, CLKOUT_PCI4 H40

OC0#/GPIO59 A14, OC1#/GPIO40 K20, OC2#/GPIO41 B17, OC3#/GPIO42 C16, OC4#/GPIO43 L16, OC5#/GPIO9 A16, OC6#/GPIO10 D14, OC7#/GPIO14 C14

PANTHER-GP-NF

3D3V_S0 — R2113 1 — 10KR2J-3-GP — PCH_GPIO51; R2109 1 — 10KR2J-3-GP — PCH_GPIO51; DY

3D3V_S0 — R2112 1 — 10KR2J-3-GP — PE_GPIO0; DY

3D3V_S0 — R2110 1 — 10KR2J-3-GP — CAMERA_ON; DY

RN2101 — ACCEL_INT, NMI_SMI_DBG# — SRN8K2J-GP

RN2102 — INT_PIRQA#, INT_PIRQD#, INT_PIRQB#, INT_PIRQC# — PE_GPIO1, PCH_GPIO2, PLT_DET_R, PCH_GPIO50 — SRN8K2J-2-GP

20120112 PV-R

27,69 PLT_DET — R2106 1 — 0R0402-PAD — PLT_DET_R

92,93 PE_GPIO1 — PE_GPIO1

PCH_GPIO50

49 CAMERA_ON — R2102 1 — DY — PME#

83 PE_GPIO0 — 10KR2J-3-GP

PCH_GPIO2

56,96 SATA_ODD_DA#

3D3V_S5 — 27,71 NMI_SMI_DBG# — R2103 1 — 22R2J-2-GP — CLK_PCI_SIO_R

65 ACCEL_INT — R2105 1 — 22R2J-2-GP — CLK_PCI_FB_R

TPAD14-OP-GP — TP2108 — CLK_OUT_PCI2

TPAD14-OP-GP — TP2106 — CLK_OUT_PCI3

27,97 CLK_PCI_KBC — 18 CLK_PCI_FB

71,97 CLK_PCI_DEBUG — R2107 1 — 22R2J-2-GP — CLK_PCI_KBC_R

PCI_PLTRST#

3D3V_S5 — U2101 — AND GATE — U74LVC1G08G-AL5-R-GP-U — 73.01G08.EHG / 2nd = 73.7SZ08.EAH / 3rd = 73.01G08.L04

PCI_PLTRST# — R2104 0R2J-2-GP — DY — PLT_RST# — PLT_RST# 5,17,32,34,53,54,56,71,83,96,97

R2108 100KR2J-1-GP — DY

RN2104 — OC4# GPIO43, OC1# GPIO40, OC2# GPIO41, OC3# GPIO42 — SRN10KJ-6-GP

RN2103 — OC5# GPIO9, LANLINK_STATUS, OC7# GPIO14, OC0# GPIO59 — SRN10KJ-6-GP

OC0# GPIO59, OC1# GPIO40, OC2# GPIO41, OC3# GPIO42, OC4# GPIO43, OC5# GPIO9, OC7# GPIO14 — LANLINK_STATUS 35

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

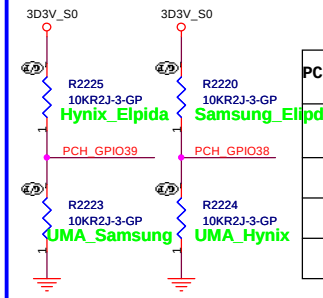
Title: PCH(5/9) : PCI/USB/NVM

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 21 of 103

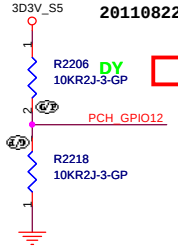
PCH(6/9)

VRAM ID TABLE



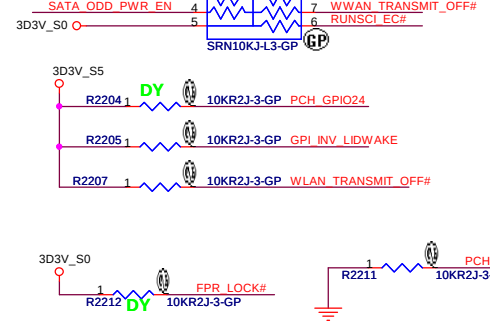
PCH_GPIO39	PCH_GPIO38	VENDER
0	1	Samsung
1	0	Hynix
1	1	Elpida
0	0	UMA

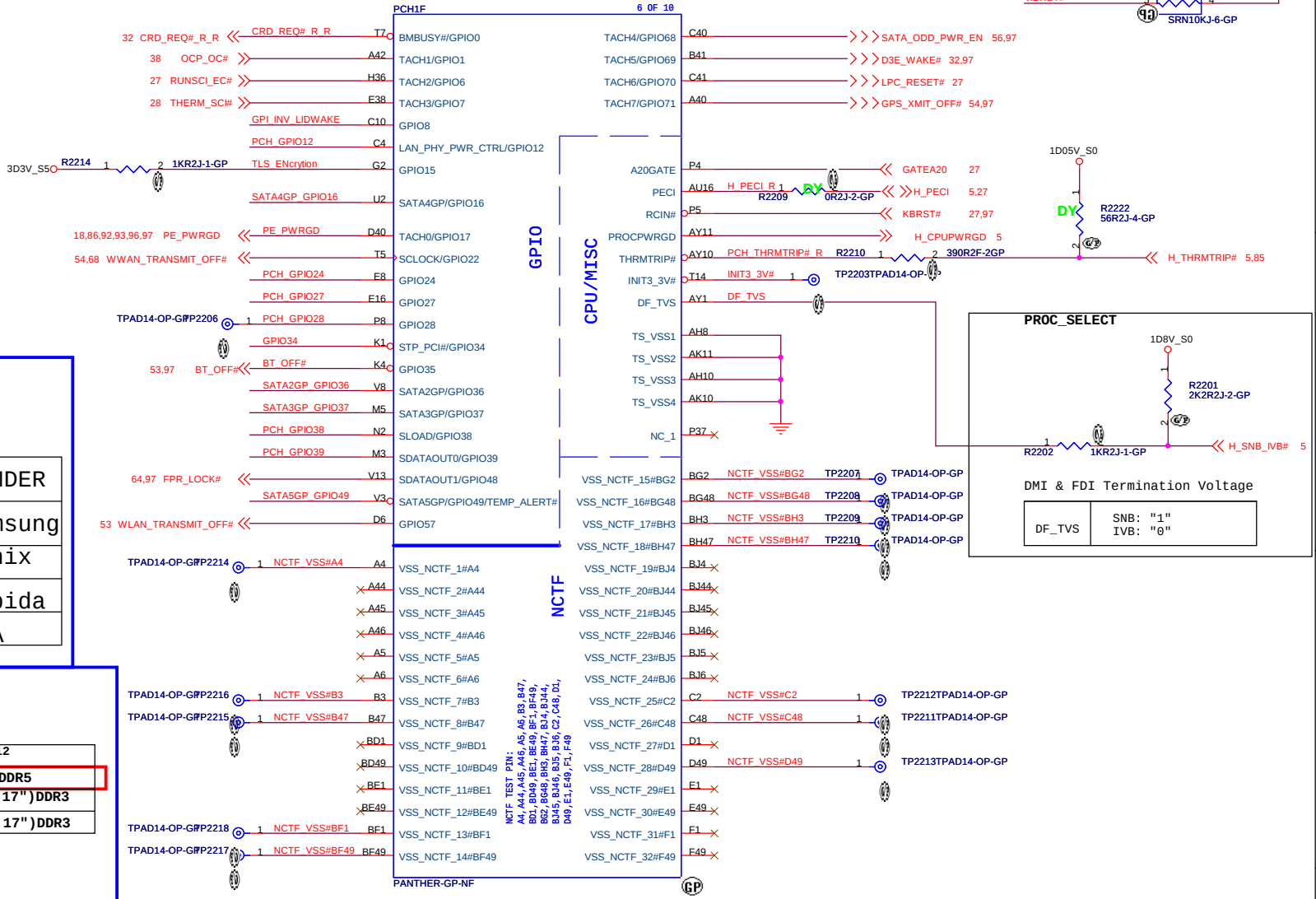
GDDR5/DDR3 TABLE

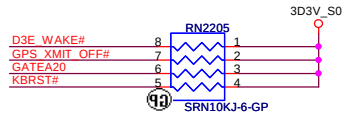


20110822SI

2012 Chief River	PCH GPIO 12
Richie U&D (13 inches)	0 (13") GDDR5
Rocky U&D (14 inches)	1(14",15",17")DDR3
Rocky U&D (15/17 inches)	1(14",15",17")DDR3







FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

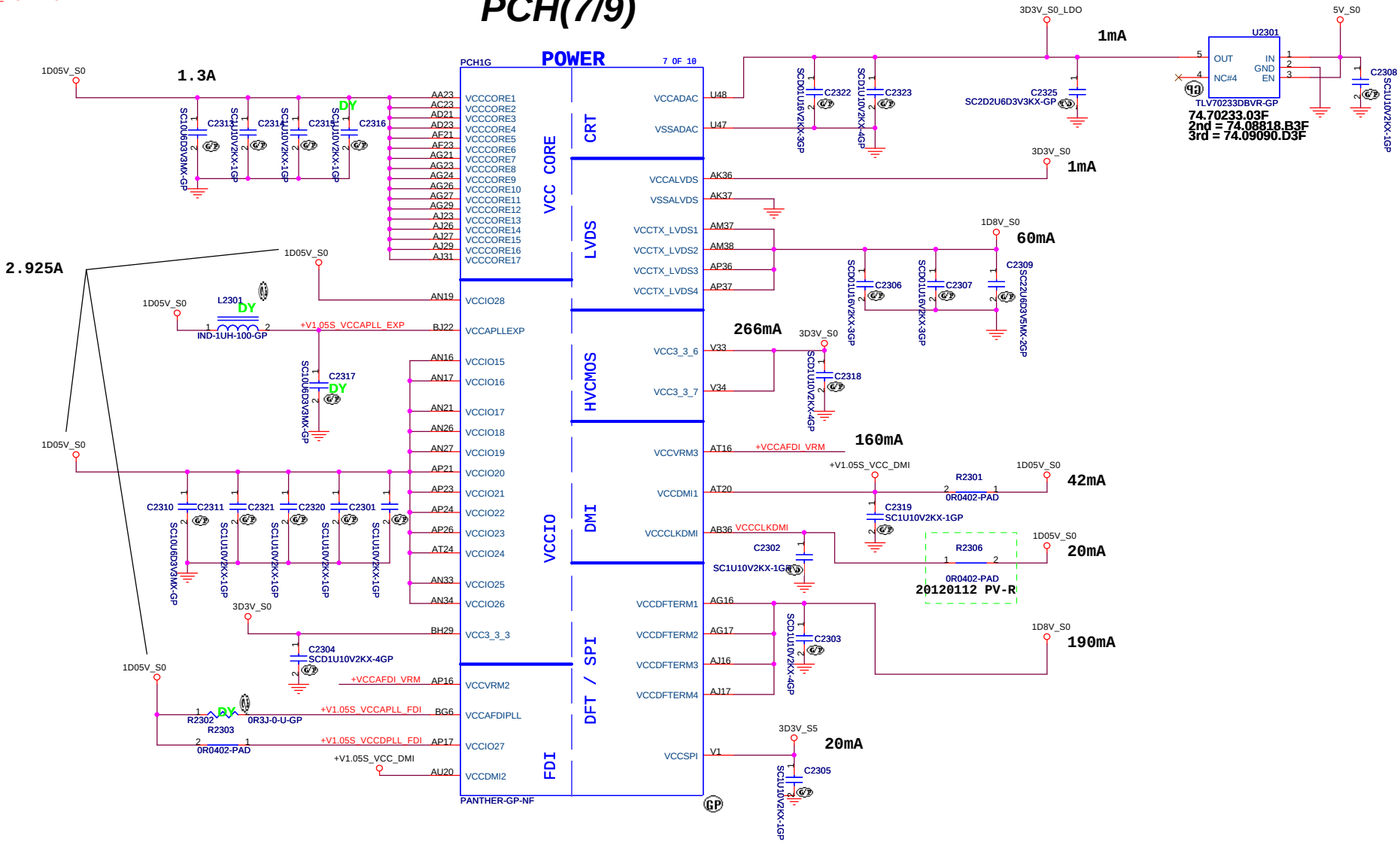
Title: PCH(6/9) : GPIO/NTCF/RSVD

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(7/9) : PWR1

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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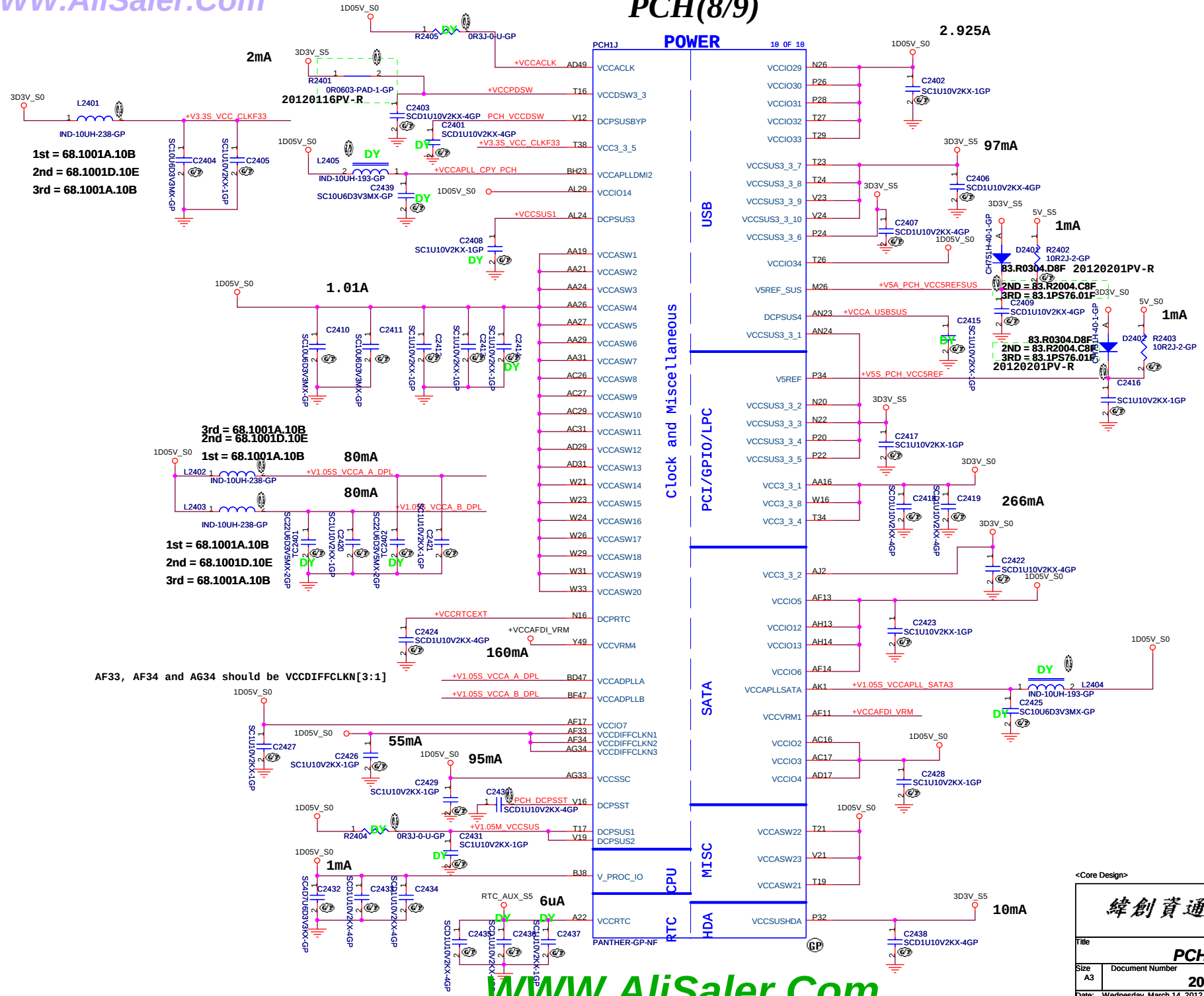
PCH(8/9)



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(8/9) : PWR2

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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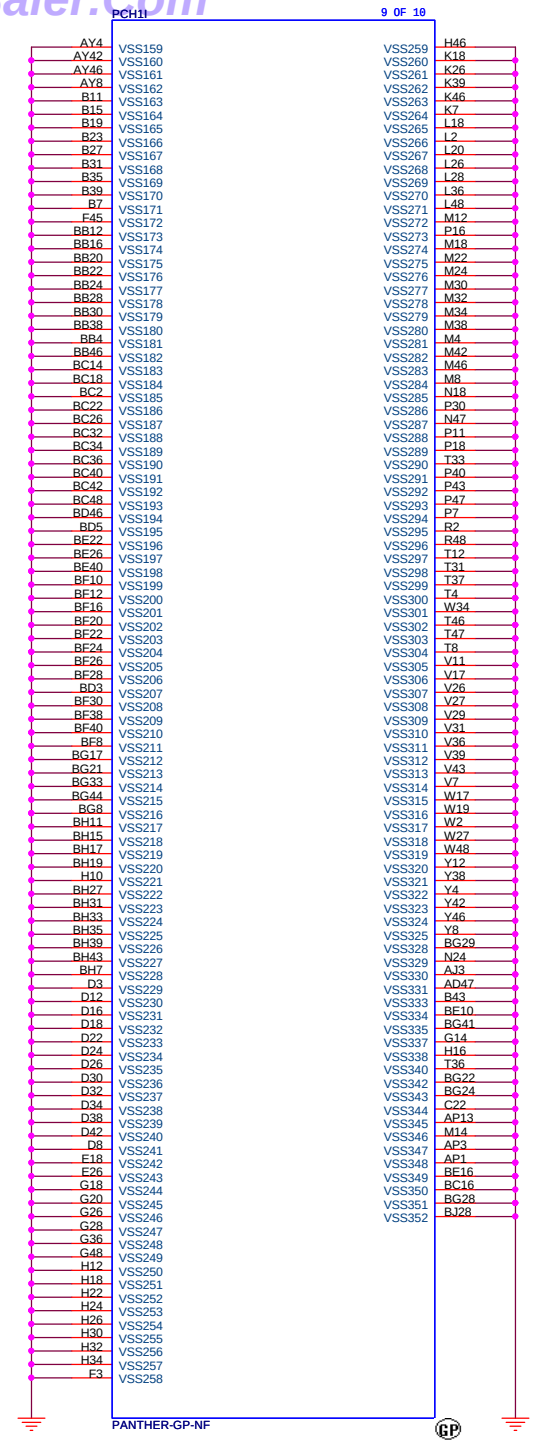
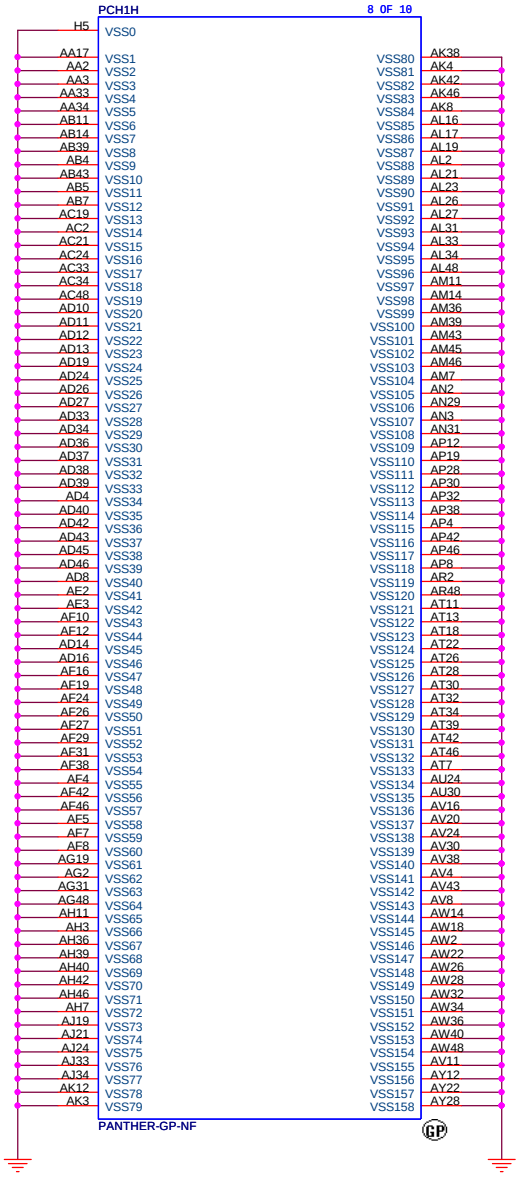
PCH(9/9)





<Core Design>

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Title: PCH(9/9) : GND

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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(Blanking)

<Core Design>

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Title: PCH XDP

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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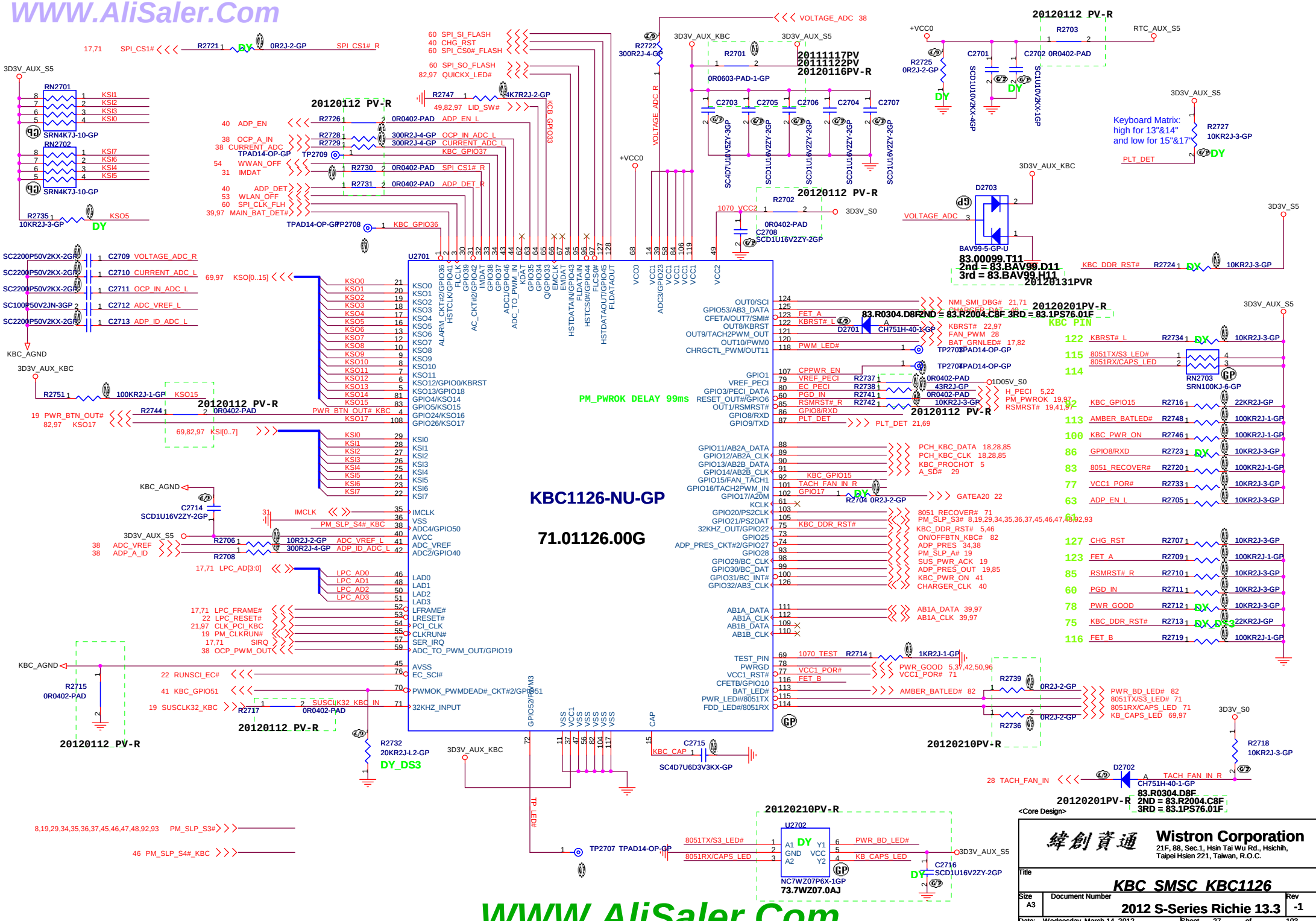


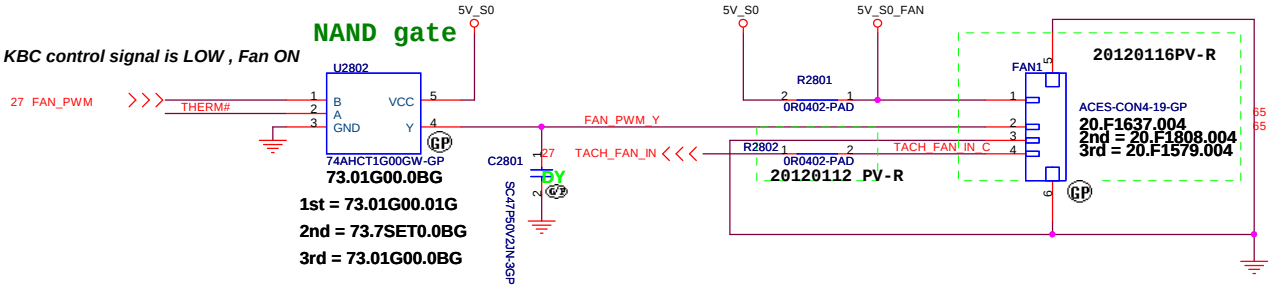
4 WIRE PWM Fan Control circuit

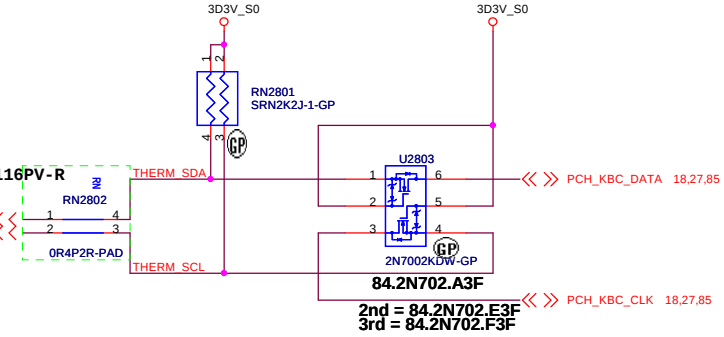
FAN PWM LEVEL = 5V

20mil

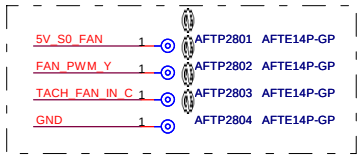
NAND gate

KBC control signal is LOW , Fan ON



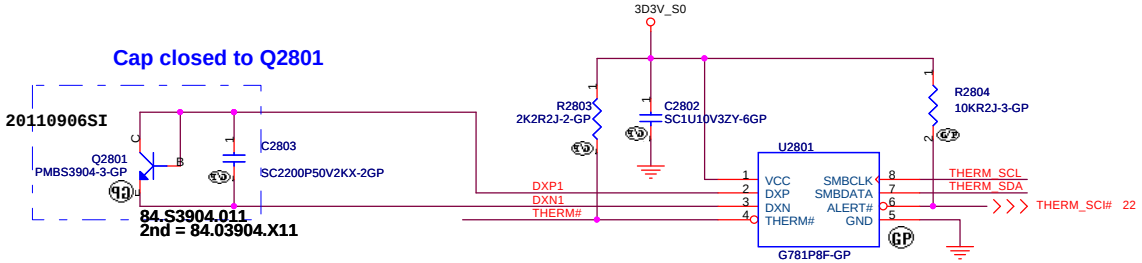


A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L



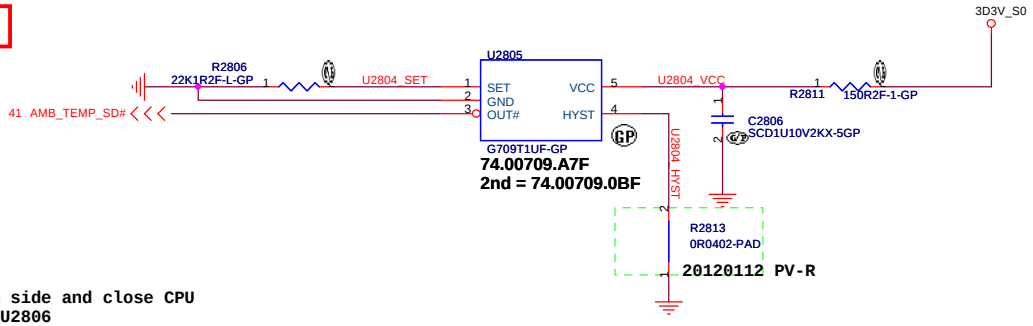
Thermal IC Control circuit

Cap closed to Q2801



T8 H/W Shutdown Control circuit

Degree	Rset
95	25.5K
90	22.1K
85	18.7K



Layout: PUT U2805 Bottom side and close CPU
PUT R2806 Close U2806

<Core Design>

緯創資通 Wistron Corporation
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Title: Thermal G781 / FAN

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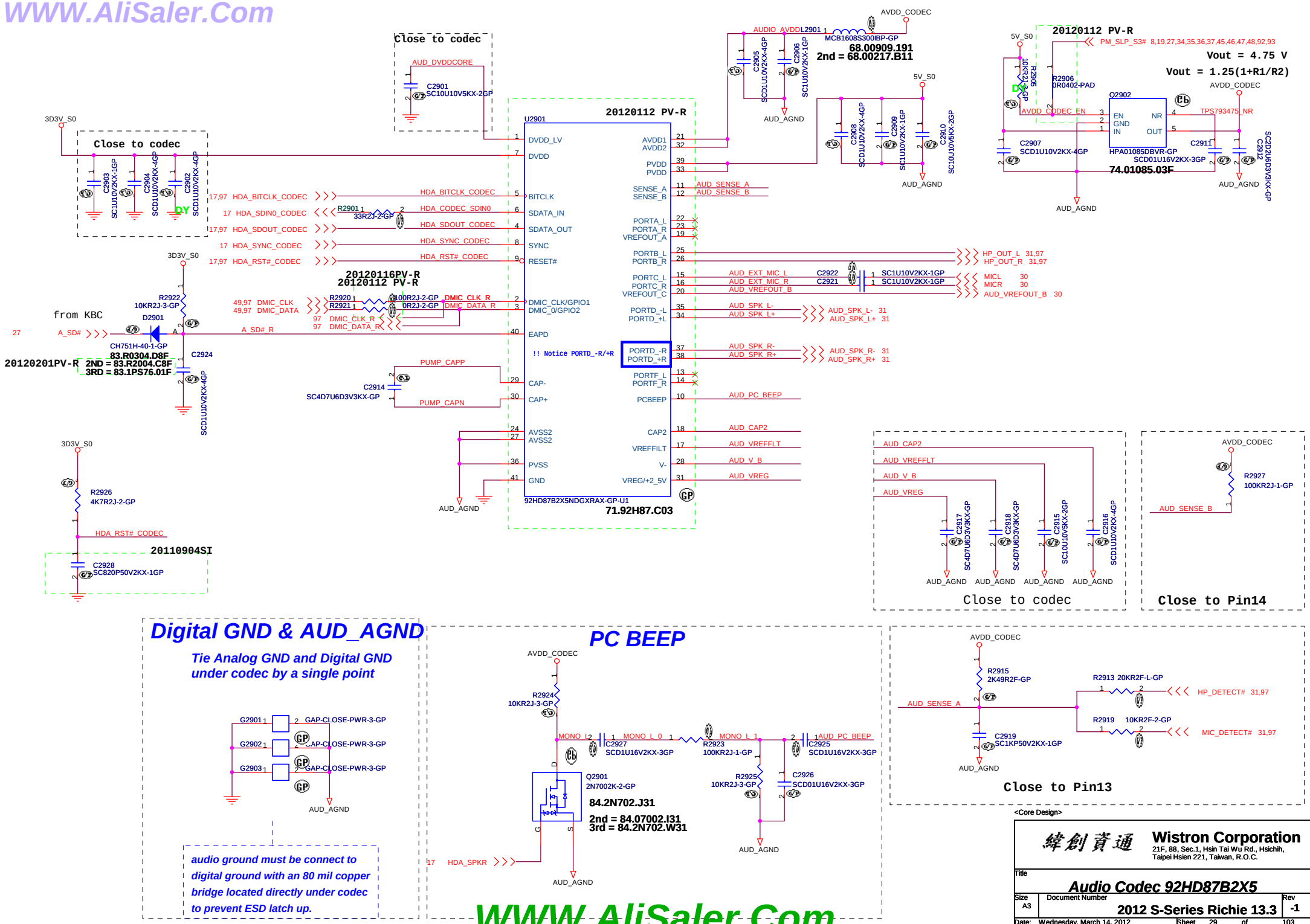

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD87B2X5

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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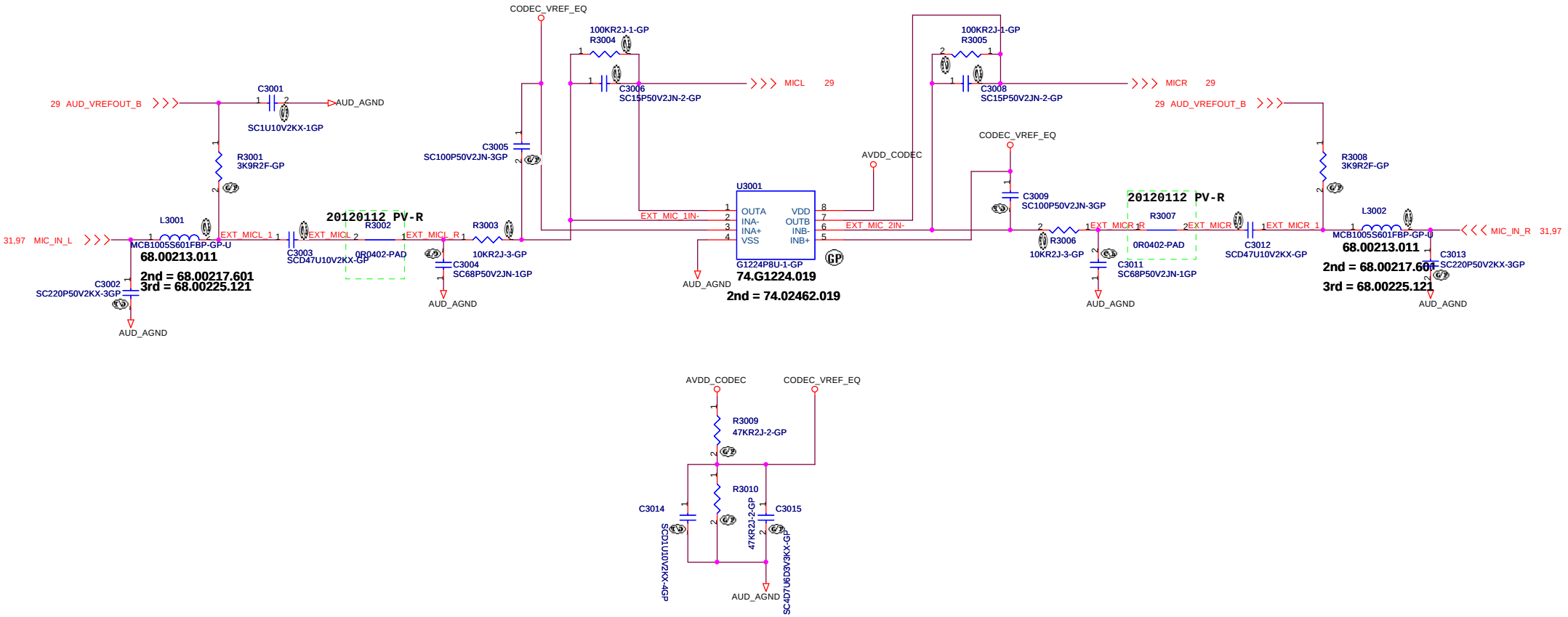
Pre-AMP. for External MIC



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: External MIC Pre-Amp

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A3	2012 S-Series Richie 13.3	-1

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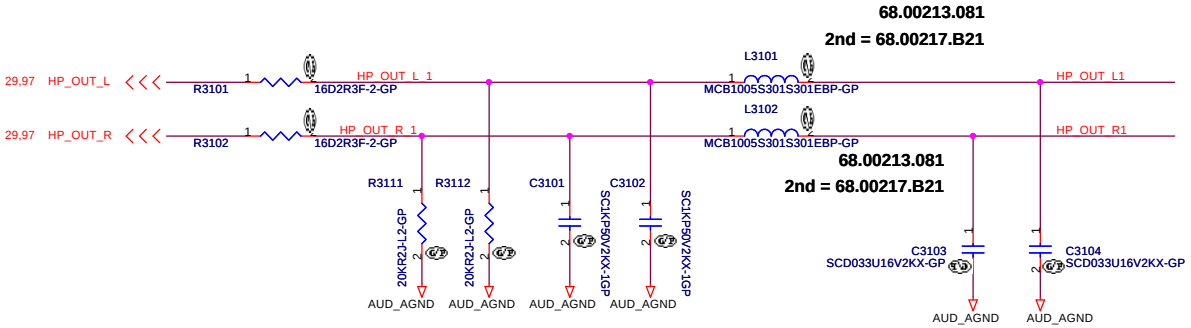
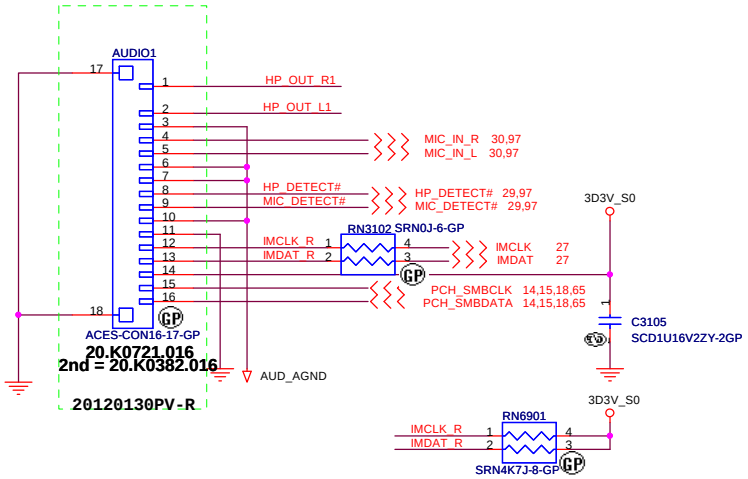
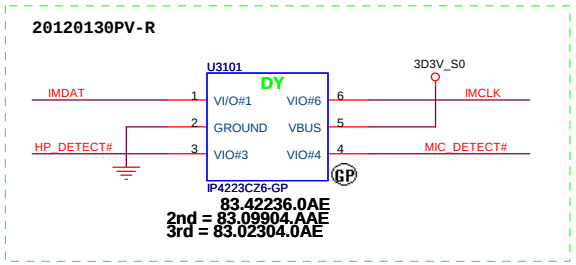
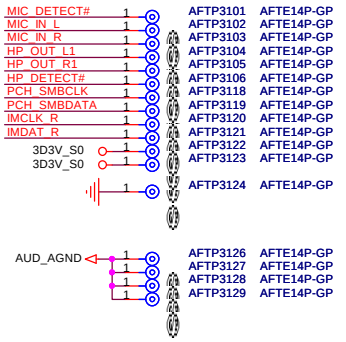
HeadPhone OUT



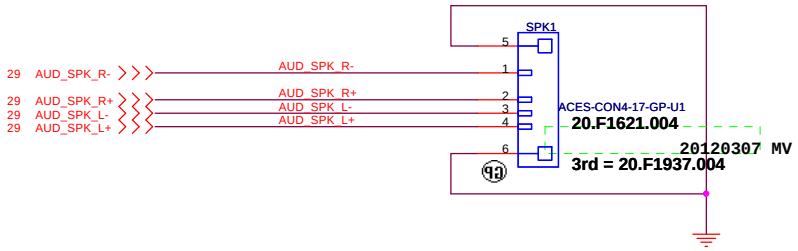
Audio Board +Touch Pad Connector

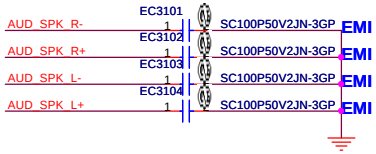


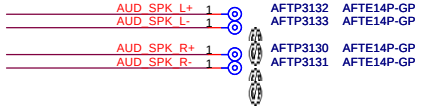




Speaker Connector







<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO Connector**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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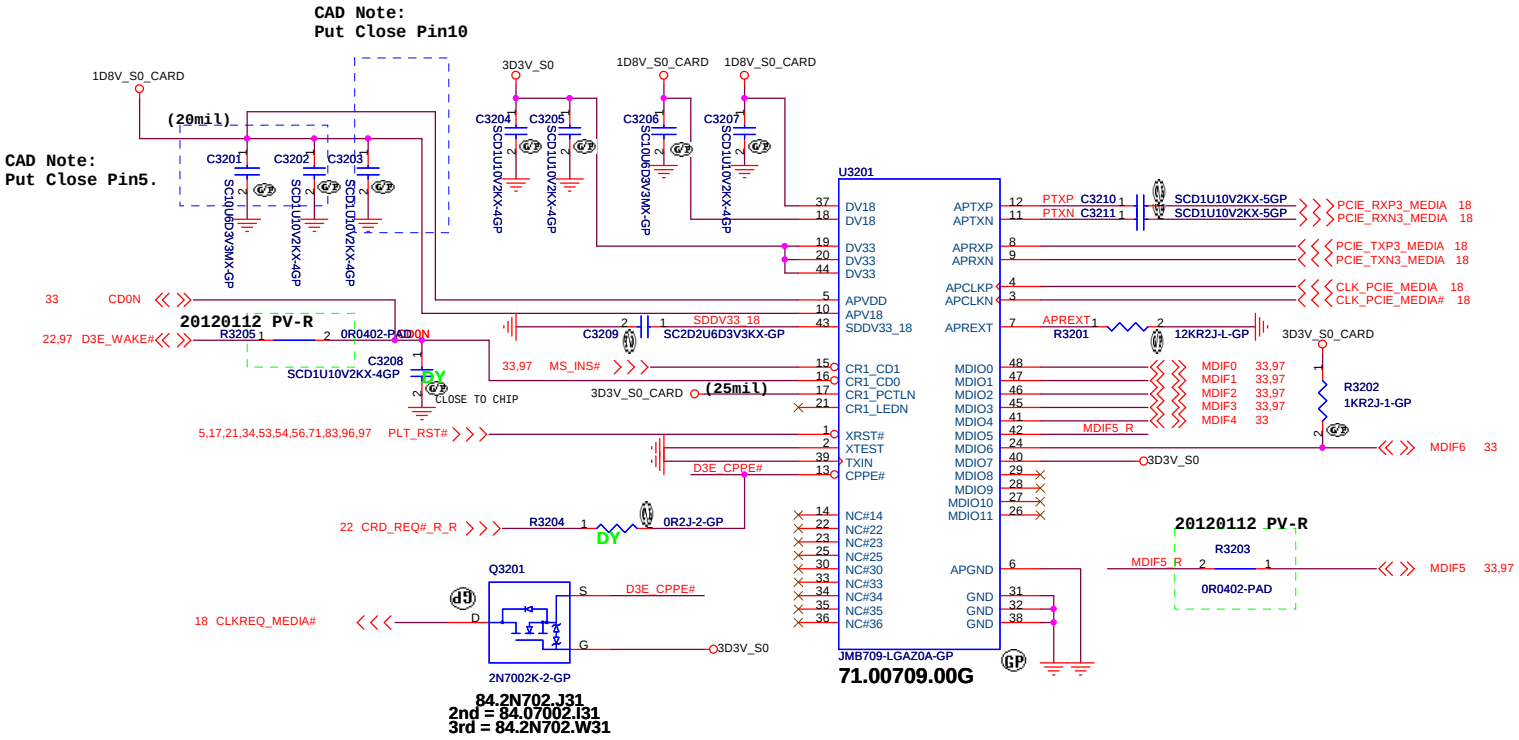
CardReader JMicron JMB709



D3E Detection Table

D3E_CPPE#	Status
H	D3E mode
L	Normal mode

CR1_CDxN Detection Table

CR1_CDxN		Card Type
1	0	
H	H	(No Card)
H	L	SD Card/MMC
L	H	MemoryStick
L	L	XD Card

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Card Reader-JMB 709**

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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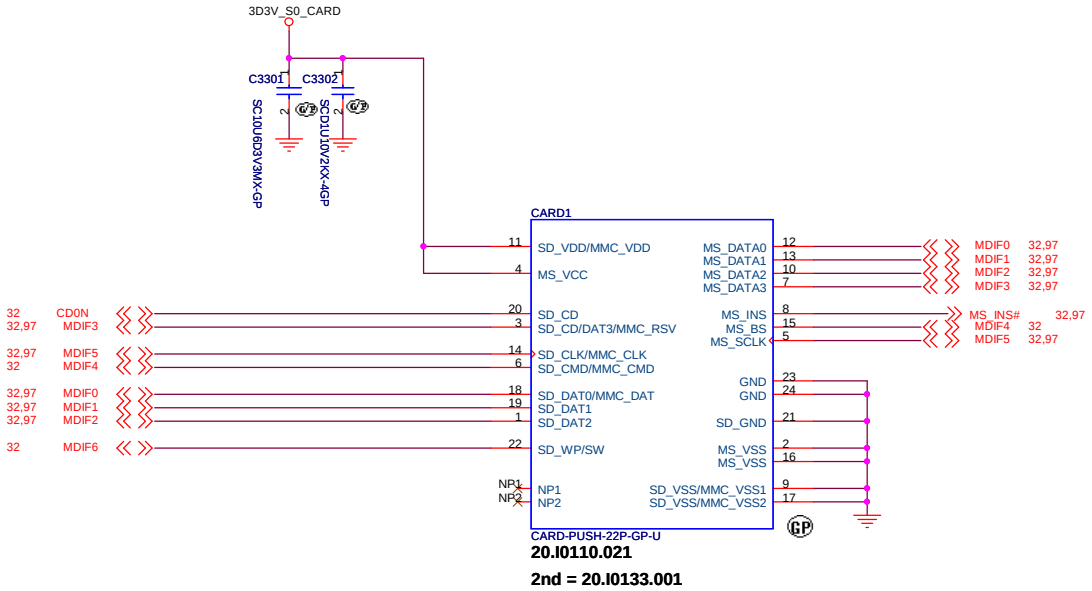

Pin Name	Default Mode	SD/MMC Card	MS Card
MDIO0	SD/MMC/MS	SD1_DAT0	MS1_DAT0
MDIO1		SD1_DAT1	MS1_DAT1
MDIO2		SD1_DAT2	MS1_DAT2
MDIO3		SD1_DAT3	MS1_DAT3
MDIO4		SD1_CMD	MS1_BS
MDIO5		SD1_CLK	MS1_CLK
MDIO6		SD1_WP	
MDIO7			
MDIO8		MMC_DAT4	MS1_DAT4
MDIO9		MMC_DAT5	MS1_DAT5
MDIO10		MMC_DAT6	MS1_DAT6
MDIO11		MMC_DAT7	MS1_DAT7
CR1_LEDN		SD1_LED#	MS1_LED#
CR1_PCTLN		SD1_PCTL#	MS1_PCTL#
CR1_CD0		SD1_CD#	
CR1_CD1			MS1_CD#

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SD/MS/MMC CONNECTOR***

Size	Document Number	Rev
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LAN CHIP-RTL8151FH

USE EFuse No ASF

3D3V_LAN_S5

LAN_GPO R3406 1K2R2J-1-GP
LAN_SMBDATA R3418 10KR2J-3-GP
EEDI R3408 10KR2J-3-GP
EECS R3409 10KR2J-3-GP

LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS

40 mils (average 100mA)

20120116PV-R
R3403 0R0603-PAD-1-GP
C3424 C3422 C3403 C3417 C3418 C3414 SCD1U10V2KX-5GP
C3419 C3406 SC4D7U6D3V4KX-GP
VDDREG
Place closed to Pin 34,35

cap near pin12,27,39,42,47,48 <200mils

Regout power plane(1D05V)

EVDD10
Put cap near pin21
R3417 0R0603-PAD-1-GP
C3412 SC1U6D3V2KX-GP
C3409 SCD1U16V2ZY-2GP

VDD10
cap near pin3,6,9,13,29,41,45
C3423 C3420 C3407 C3421 C3435 C3416 C3415
SCD1U10V2KX-5GP
SCD1U16V2ZY-2GP

60 mils (average 300mA)

L3401 IND-4D7UH-192-GP
2nd = 68.4R71E.10Q
3rd = 68.4R71G.10G
68.4R750.20C
REGOUT
C3401 SC4D7U6D3V3KX-GP
C3413 SCD1U10V2KX-5GP

Lan Power Inductance Spec
(1) IDC >= 600mA
(2) Tolerance < 20%
(3) RDC <= 0.8ohms(Max)
(4) Efficiency >= 80%

Put 4D7U L + 4D7U cap near pin36 <200mils
(2nd = 78.22610.81L)

EEPROM LED OPTION USE '00'
=> LED0 : ACT (Yellow)
=> LED1 : LINK (Green)
(BOTH 10/100 & GIGA CHIP)
(Power down => Kept high)

R3404 2K49R2F-GP RSET
YELLOW_LED# 35,97
GREEN_LED# 35,97
LAN_GPO

U3401 RTL8151FH-CG-1-GP
GND
MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3
AVDD10 AVDD33 VDD10
REGOUT VDDREG ENSWREG EEDI/SDA LED3/EEDO EECS/SCL DVDD10 LANWAKE# DVDD33 ISOLATE# PERST#
EEDI LAN_LED3# EECS VDD10 3D3V_LAN_S5 ISOLATE#
TP3401 TPAD14-OP-GP
PCIE_WAKE# 19,53
PLT_RST# 5,17,21,32,53,54,56,71,83,96,97
DVDD10 SMBCLK SMBDATA CLKREQ# HSIP HSIN REFCLK_P REFCLK_N EVDD10 HSOP HSON GND
71.08151.M04
Close to LanChip

Using Efuse
Without ASF

LAN_SMBDATA
PCIE_RXN6_R C3411 SCD1U10V2KX-5GP PCIE_RXN6_LAN 18
PCIE_RXP6_R C3410 SCD1U10V2KX-5GP PCIE_RXP6_LAN 18
18 CLKREQ_LAN#
CLK_PCIE_LAN# 18
CLK_PCIE_LAN 18
PCIE_TXN6_LAN 18
PCIE_TXP6_LAN 18

Regout Switch

3D3V_LAN_S5
20120112 PV-R
ENSWREG R3405 0R0402-PAD
R3407 0R2J-2-GP
DY
ENSWREG (REGOUT 1D05V)
PH = Enable
PL = Disable

3D3V_S5 3D3V_LAN_S5
Q3401 DMP2305U-7-GP
C3402 SC1U10V3ZY-6GP
R3401 100KR2J-1-GP
C3425 SCD1U10V2KX-5GP
84.02305.G31
2ND = 84.02377.031
3rd = 84.02035.031
20120210PV-R
LAN_POWER_EN# R
R3402 10KR2F-2-GP
Q3402 2N7002KDW-GP
27,38 ADP_PRES
PM_SLP_S3# 8,19,27,29,35,38,37,45,46,47,48,92,93
LAN_POWER_EN#
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.F3F

25MHz Crystal

C3404 SC18P50V2JN-1-GP
LANXOUT
X3401 XTAL-25MHZ-155-GP
82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61
C3405 SC18P50V2JN-1-GP
LANXIN
LANXIN 97

Isolate Strap Pin

3D3V_S0
R3411 1KR2J-1-GP
ISOLATE#
R3414 15KR2F-GP

<Core Design>

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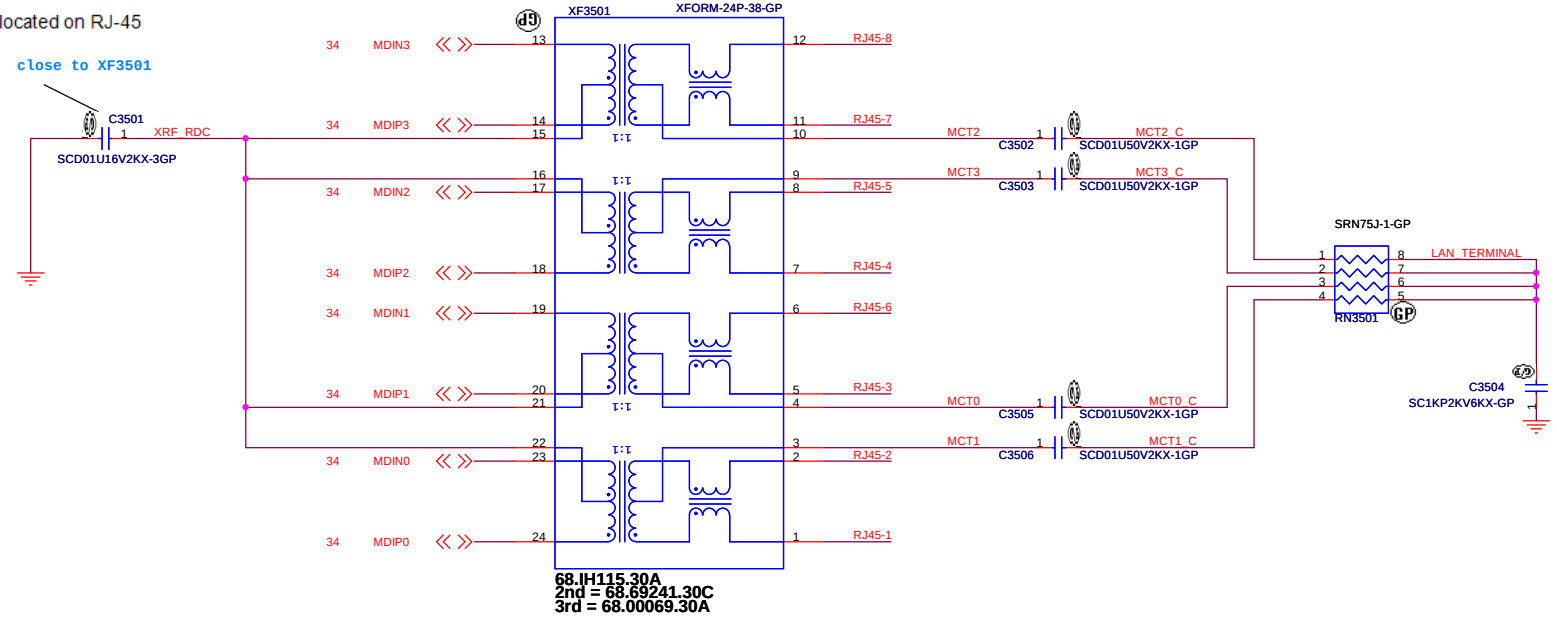
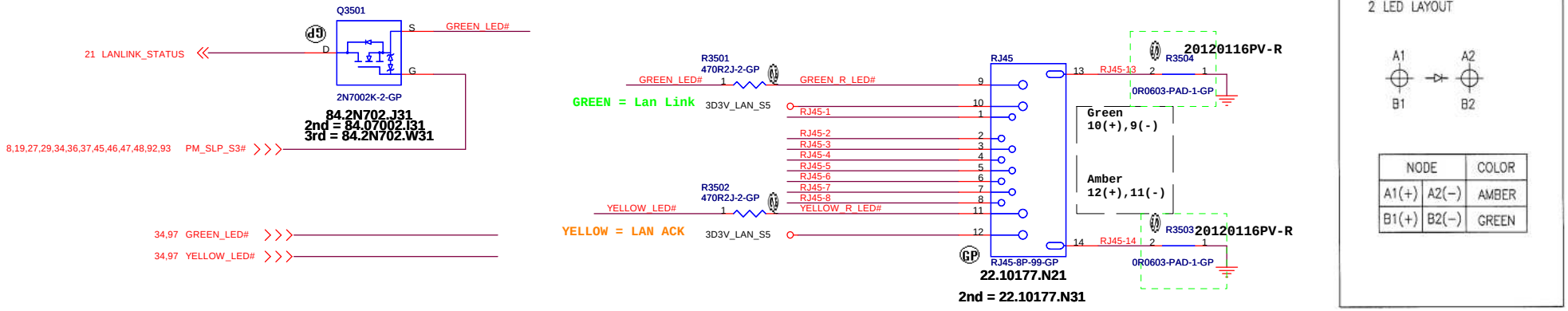
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

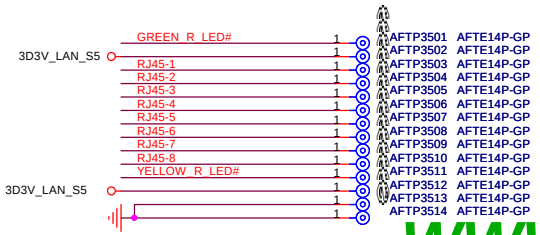
Title: Lan Realtek 8151FH
Size: A3
Document Number: 2012 S-Series Richie 13.3
Rev: -1
Date: Wednesday, March 14, 2012
Sheet 34 of 103

White LED for connectivity and Amber LED for activity located on RJ-45 connector



RJ45 Connector





(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

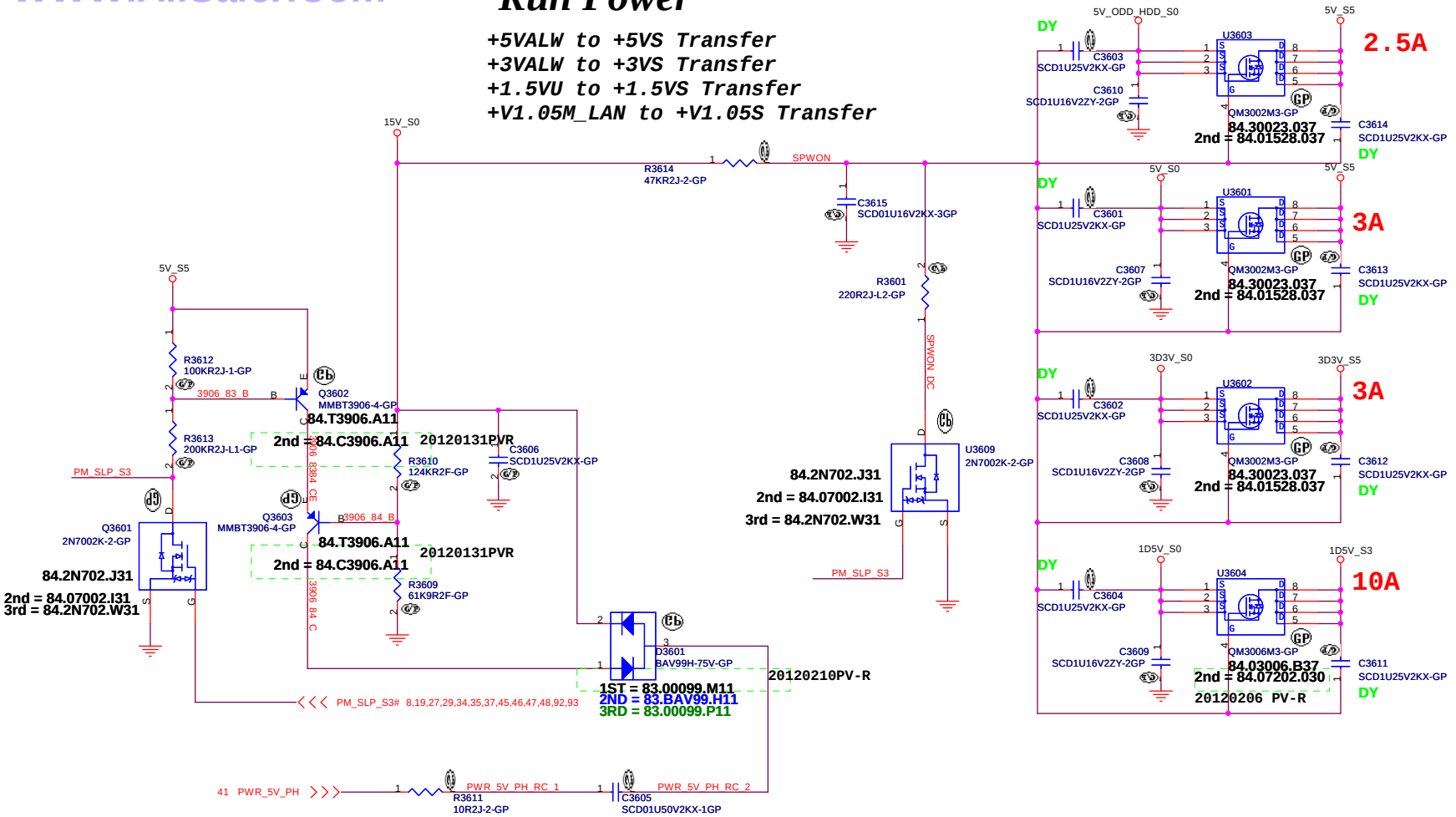
Title: LAN RJ45

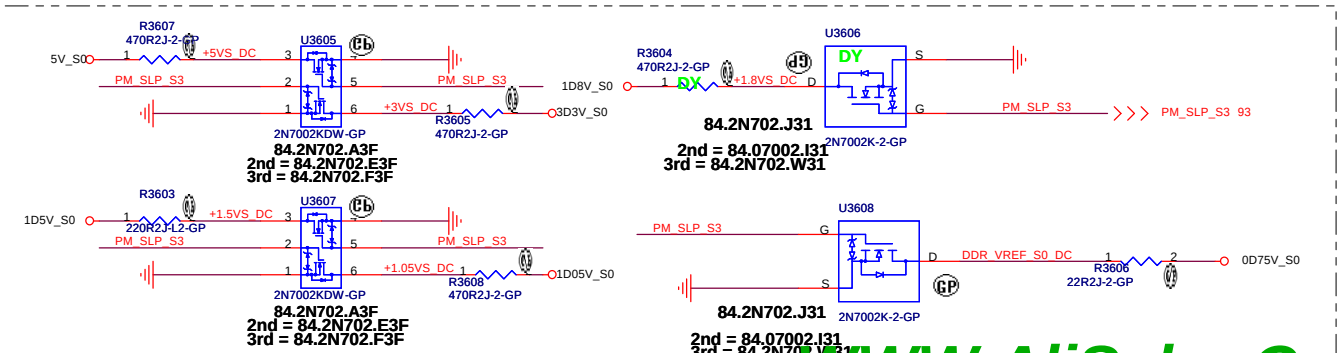
Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 35 of 103

Run Power

+5VALW to +5VS Transfer
+3VALW to +3VS Transfer
+1.5VU to +1.5VS Transfer
+V1.05M_LAN to +V1.05S Transfer





<Core Design>

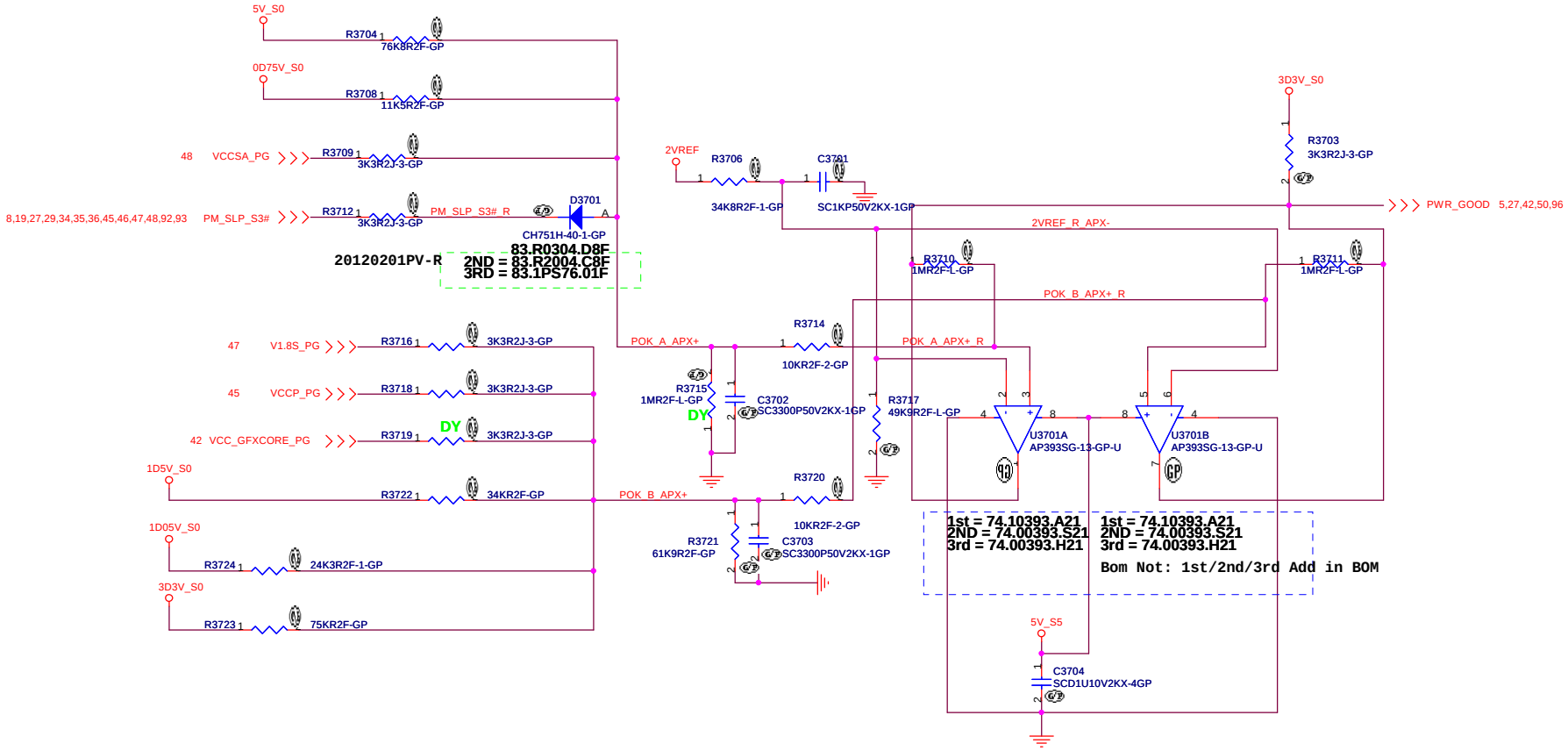
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 36 of 103

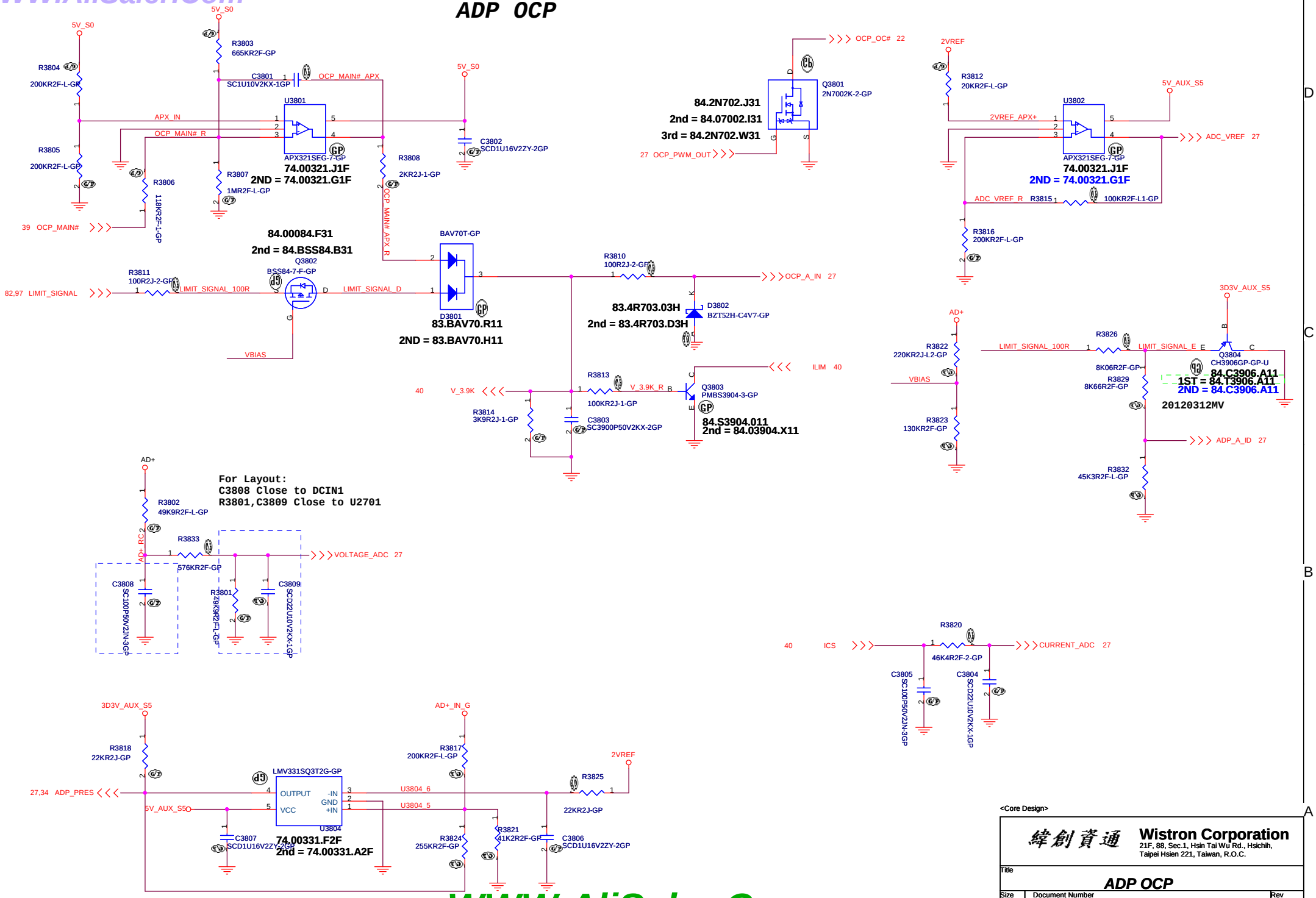
POK



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: POK		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
Date: Wednesday, March 14, 2012	Sheet 37 of 103	

ADP OCP



<Core Design>

緯創資通 Wistron Corporation
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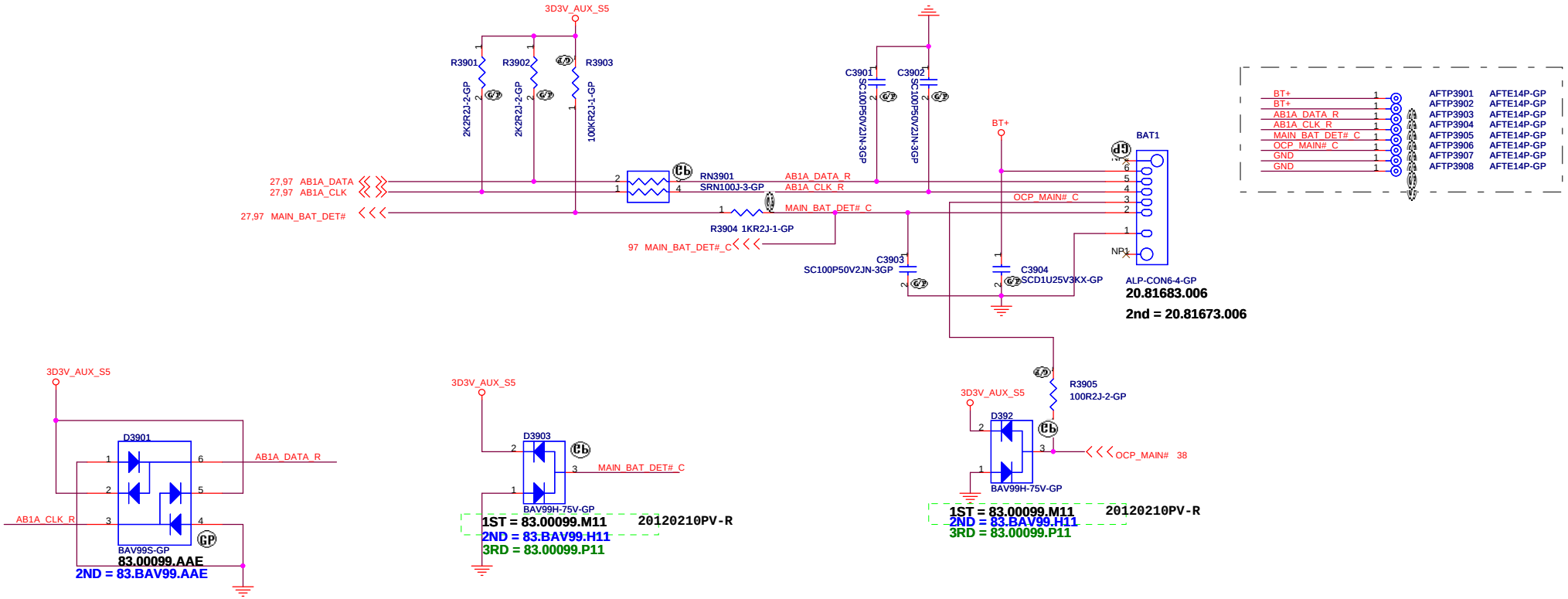
Taipei Hsien 221, Taiwan, R.O.C.

Title	ADP OCP	
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012	Sheet 38 of 103	

Battery Connector



<Core Design>

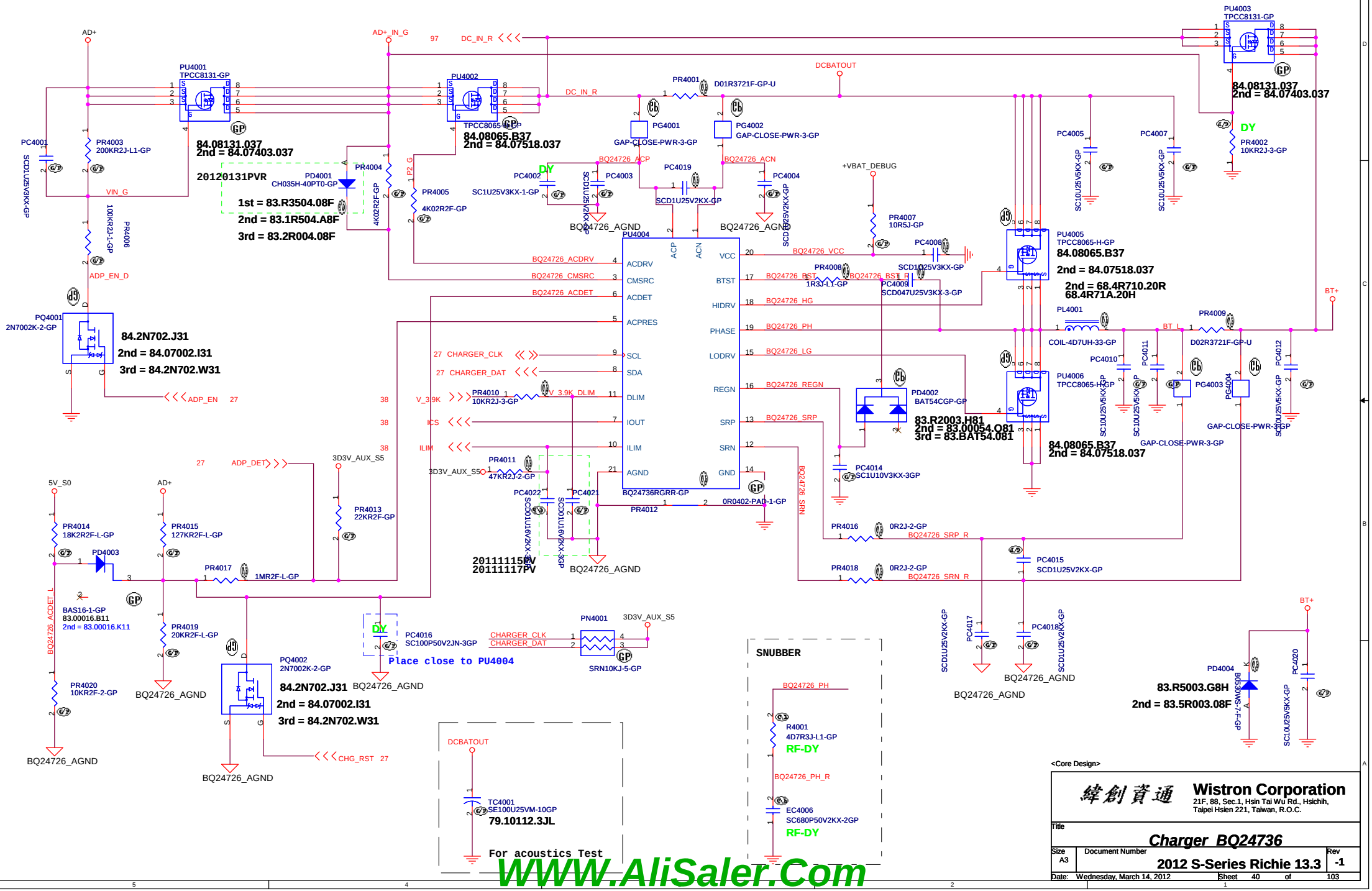
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 39 of 103

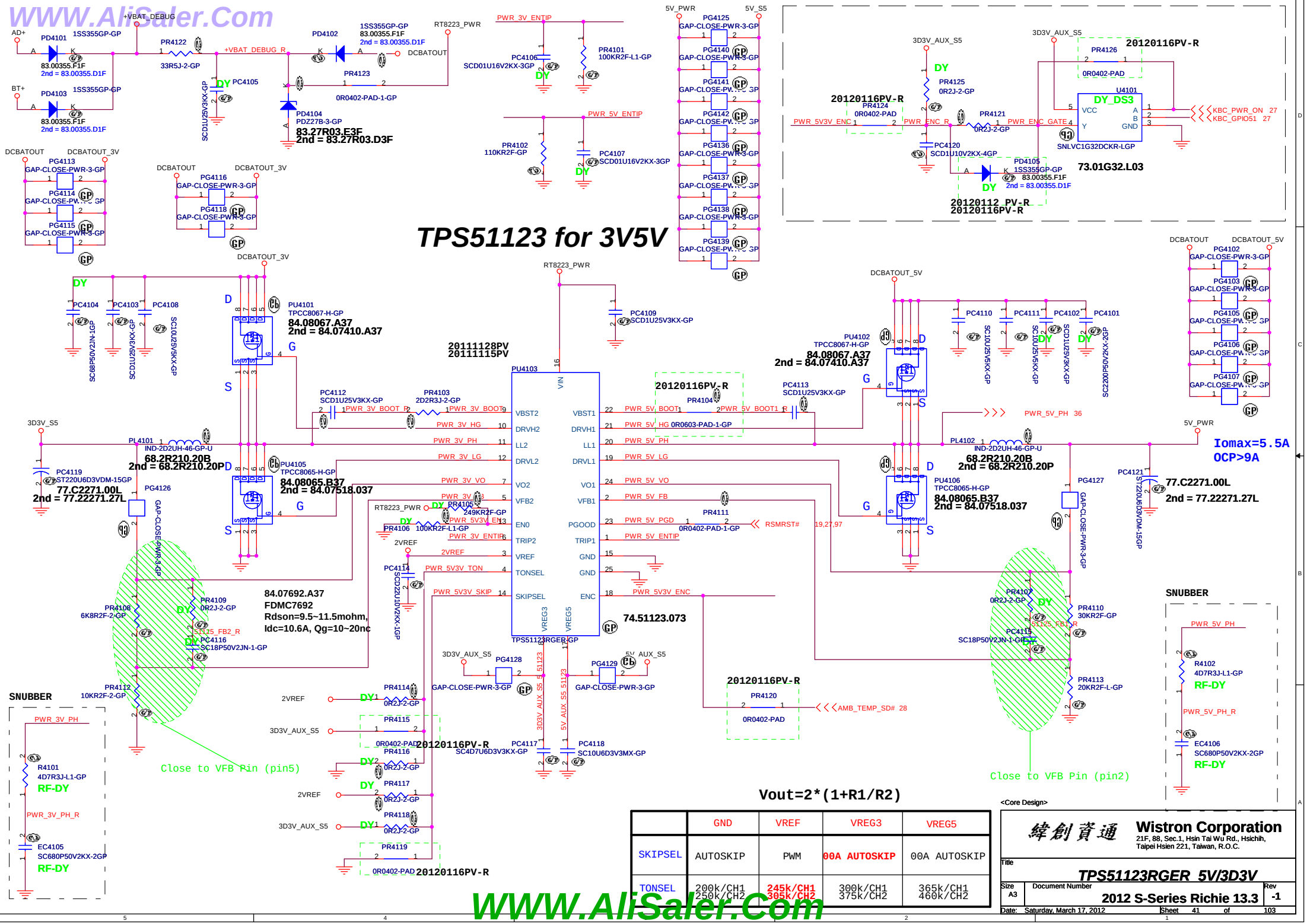
BQ24736 for CHARGER



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Charger BQ24736	
Size A3	Document Number 2012 S-Series Richie 13.3	Rev -1
Date: Wednesday, March 14, 2012	Sheet 40 of 103	

TPS51123 for 3V5V



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

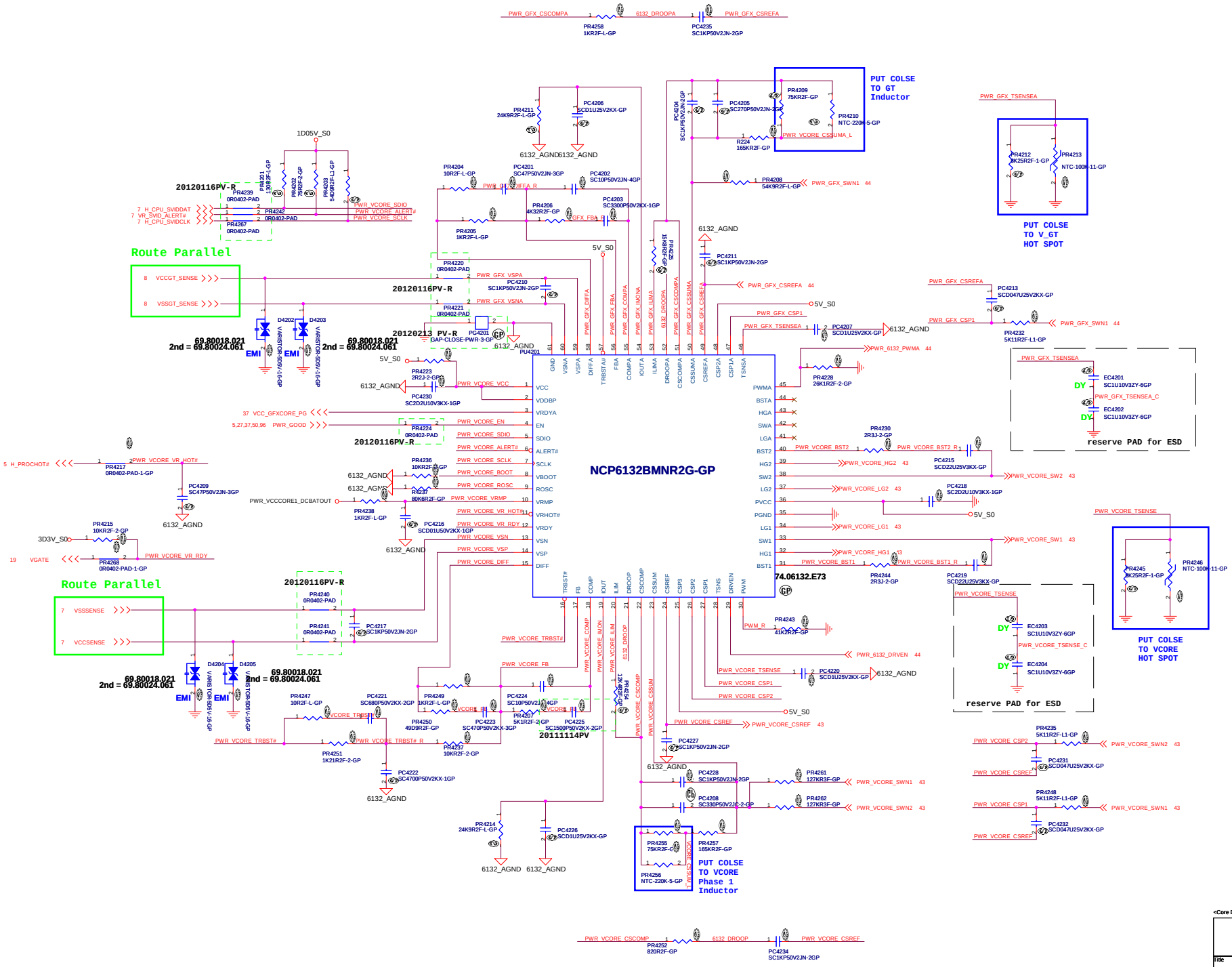
<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123RGER 5V/3D3V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Saturday, March 17, 2012 | Sheet 41 of 103

SSID = CPU.Regulator

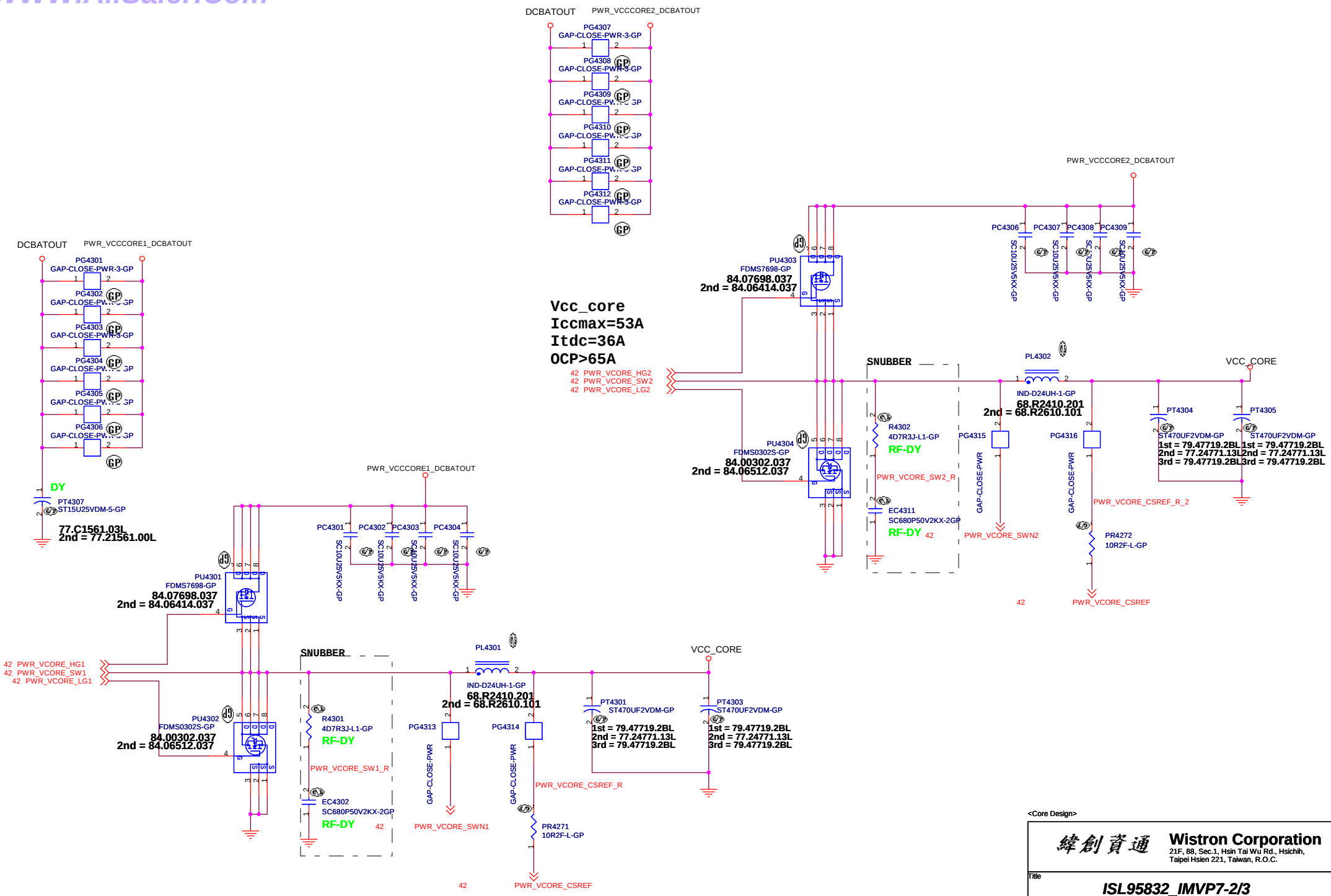


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832 IMVP7-1/3

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 42 of 103



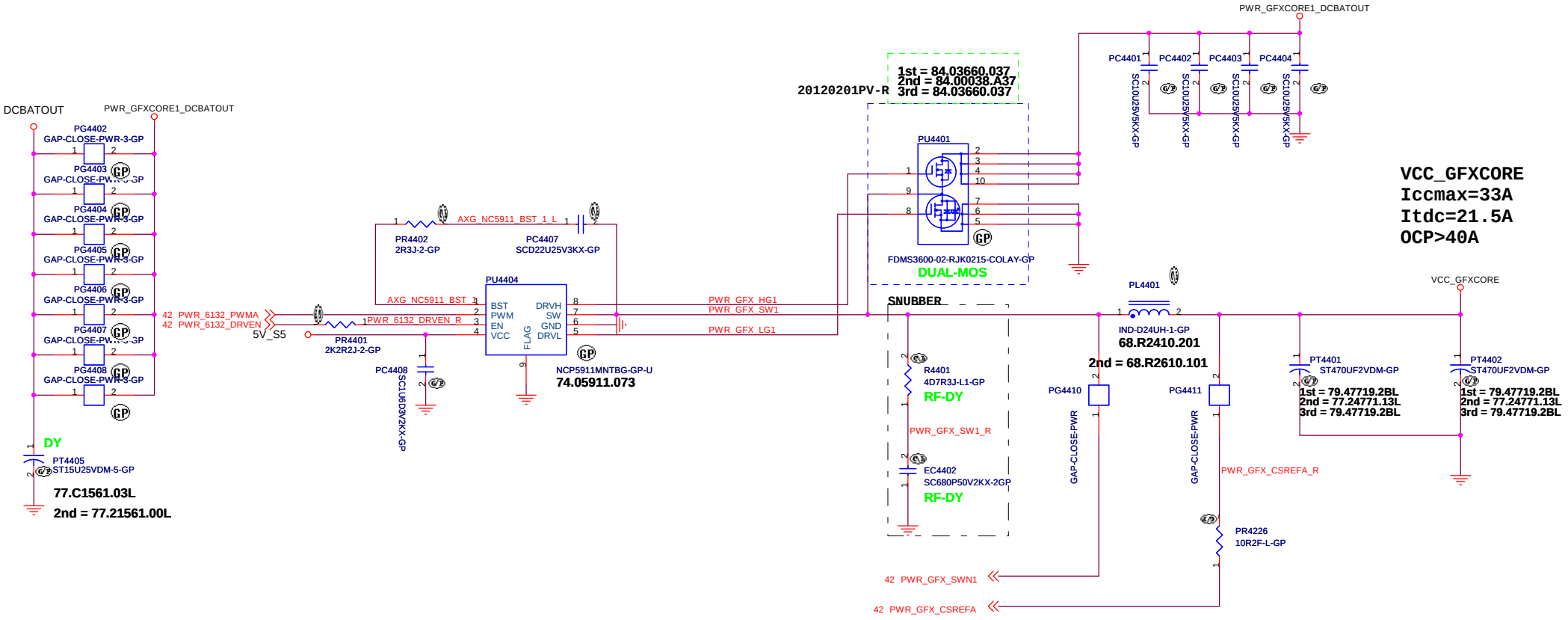
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95832_IMVP7-2/3

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

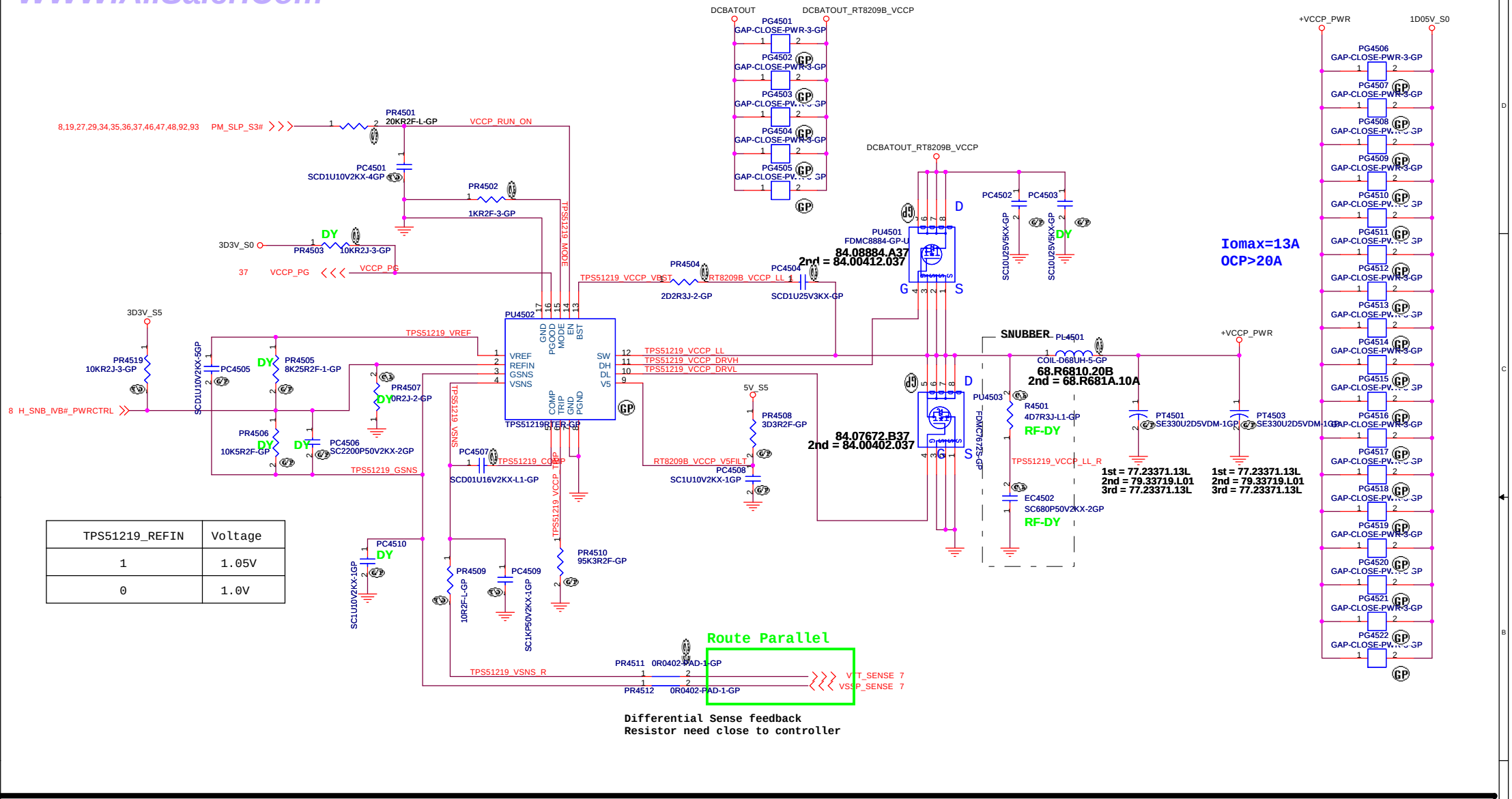
Date: Wednesday, March 14, 2012 Sheet 43 of 103



VCC_GFXCORE
Iccmax=33A
Itdc=21.5A
OCP>40A

<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL95832_IMVP7-3/3
Size: A3	Document Number: 2012 S-Series Richie 13.3
Rev: -1	
Date: Monday, March 19, 2012	Sheet 44 of 103



TPS51219_REFIN	Voltage
1	1.05V
0	1.0V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_1D05V / 1D0V

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 45 of 103

DEEP S3

PR4610 0R0402-PAD 20120116PV-R

PM_SLP_S4#_KBC 27

19,62,97 PM_SLP_S4#

5,27 KBC_DDR_RST#

PR4607 0R2J-2-GP DY_DS3

KBC_DDR_RST#_R

PD4601 BAT54CGP-GP DY_DS3

PR4611 0R2J-2-GP

PWR_1D5V_EN

PR4612 20KR2J-L2-GP DY_DS3

C4601 SCD1U10V2KX-5GP DY

83.R2003.H81
2nd = 83.R2003.Q81
3rd = 83.BAT54.081

DCBATOUT PG4601 GAP-CLOSE-PWR-3-GP DCBATOUT_1D5V

PG4602 GAP-CLOSE-PWR-3-GP
PG4603 GAP-CLOSE-PWR-3-GP
PG4604 GAP-CLOSE-PWR-3-GP
PG4605 GAP-CLOSE-PWR-3-GP

5V_S5

PC4801 SC1U10V3KX-3GP

PU4602 TPS51216RUKR-GP

PGOOD, VTTEN, EN/PSV, VREF, REFIN, MODE, TRIP, VTTREF, GND, GND, V5IN, VBST, DRVH, SW, DRVL, PGND, VDDQS, VTTIN, VTT, VTTS, VTTGND

PWR_0D75V_EN
PWR_1D5V_EN
PWR_1D5V_VREF
PWR_1D5V_REFIN
PWR_1D5V_MODE
PWR_1D5V_TRIP
DDR_VREF_S3
PWR_1D5V_VBST
PWR_1D5V_DRVH
PWR_1D5V_SW
TPS51216_DRVL
PWR_1D5V_VDDQS
0D75V_PWR

R1 PR4603 9K31R2F-GP
R2 PR4604 54K9R2F-L-GP
PR4605 200KR2F-L-GP
PR4606 2K2R5F-GP

PC4606 SCD1U10V2MX-3GP
PC4607 SCD01U16V2KX-3GP
PC4608 SCD22U10V2KX-1GP
PC4609 SCD1U10V2KX-4GP
PC4610 SC10U6D3V3MX-GP
PC4611 SC10U6D3V3MX-GP

PR4602 2D2R3J-2-GP VBST_R
PC4604 SCD1U25V3KX-GP

78.10413.5FL

DCBATOUT_1D5V

PU4601 FDMC8884-GP
PC4602 SC10U25V5KX-GP DY
PC4603 SC10U25V5KX-GP

84.08884.A37
2nd = 84.00412.037

PU4603 FDMC7672S-GP

84.07672.B37
2nd = 84.00402.037

SNUBBER

PL4601 COIL-D82UH-2-GP 68.R8210.10V
2nd = 68.R8210.10Z

R4601 4D7R3J-L1-GP RF-DY
EC4602 SC680P50V2KX-2GP RF-DY

PG4619 GAP-CLOSE-PWR-3-GP

PC4605 SCD1U10V2KX-5GP DY

1D5V_S3

PT4601 SE330U2D5VDM-1GP
1st = 77.23371.13L
2nd = 79.33719.L01
3rd = 77.23371.13L

1D5V_PWR
Iomax=13A
OCP>19A

Close to output Cap pin1

PWR_1D5V_SW_R

PWR_1D5V_VDDQS

78.10610.5BL78.10610.5BL

PC4612 SC1U6D3V2KX-GP
78.10520.5FL

Vout=1.8*(R2/(R1+R2))

3D3V_S0

PR4601 10KR2F-2-GP

D4601 CH751H-40-1-GP

8,19,27,29,34,35,36,37,45,47,48,92,93 PM_SLP_S3#

PWR_0D75V_EN

83.R0304.D8F
2ND = 83.R2004.C8F
3RD = 83.1PS76.01F
20120201PV-R

PC4613 SCD47U10V2KX-GP

0D75V_PWR

PG4620 GAP-CLOSE-PWR-3-GP
PG4621 GAP-CLOSE-PWR-3-GP

0D75V_S0

0D75V_PWR
Iomax=1A

<Core Design>

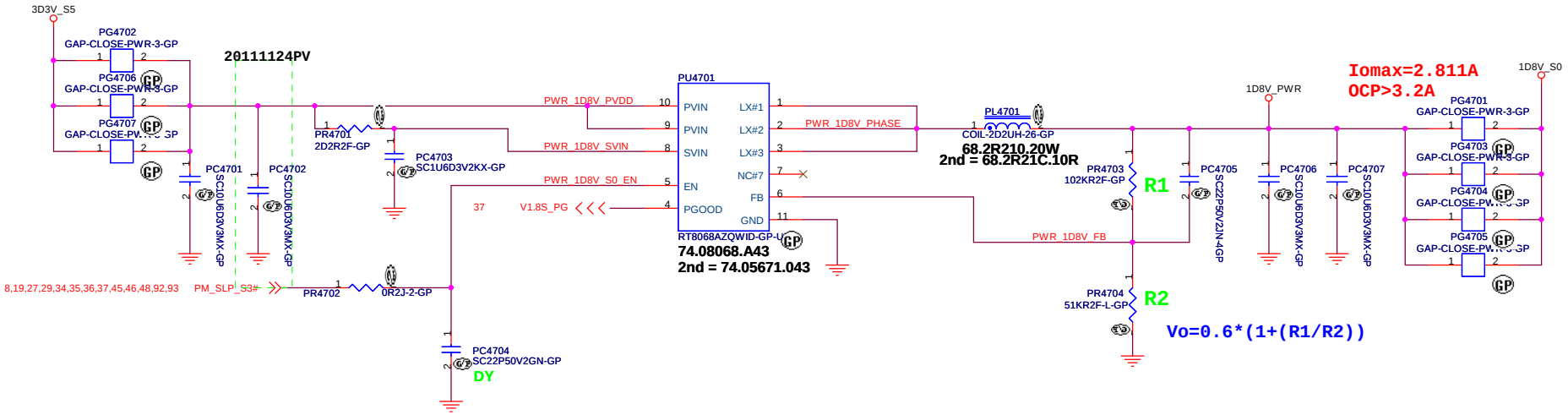
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UP1561_1D5V&0D75V

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 46 of 103

RT8068A for 1D8V_S0



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

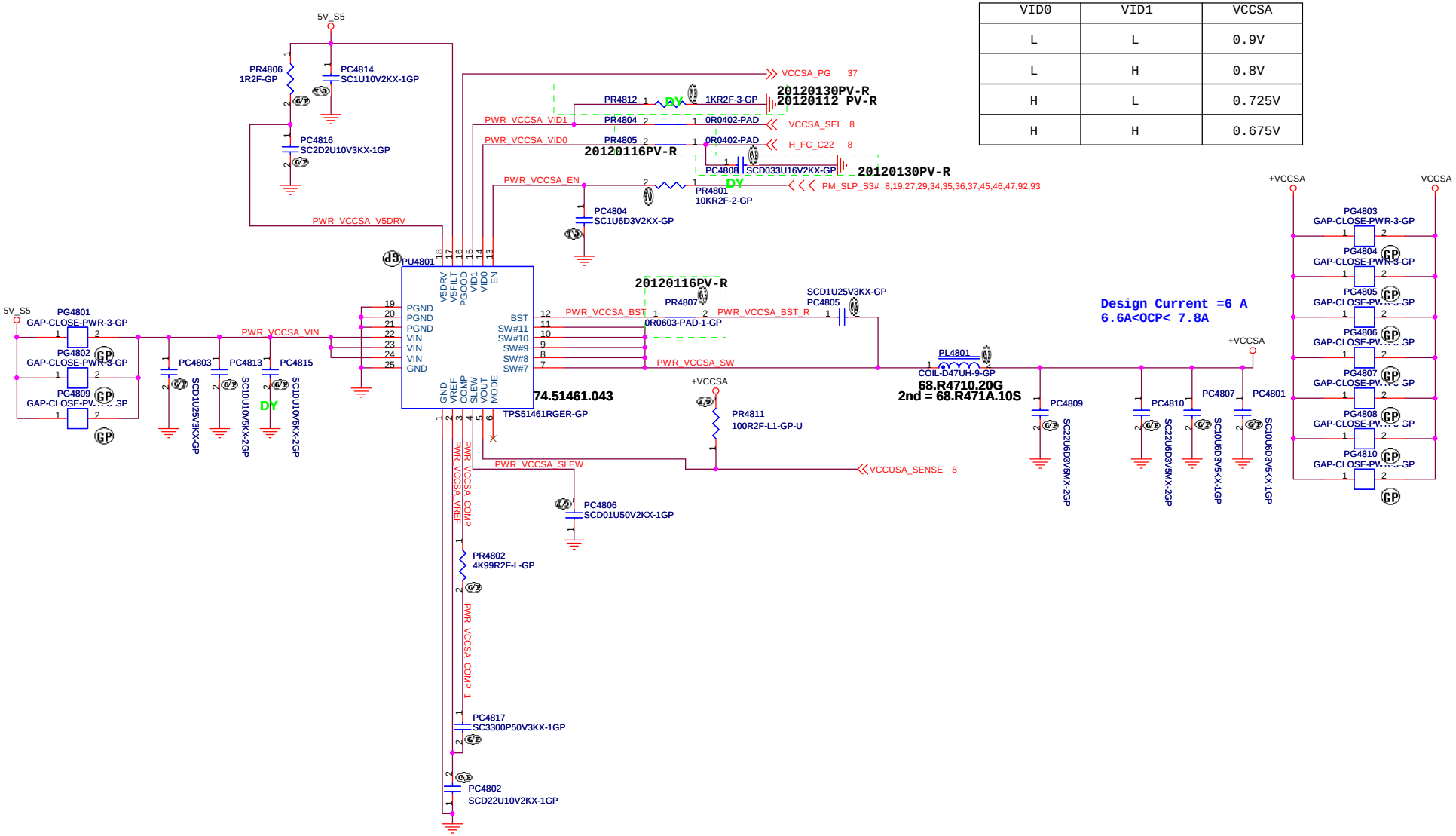
Title: 1D8V_S0

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

Date: Wednesday, March 14, 2012 Sheet 47 of 103

TPS51461 for VCCSA

VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL95870A VCCSA

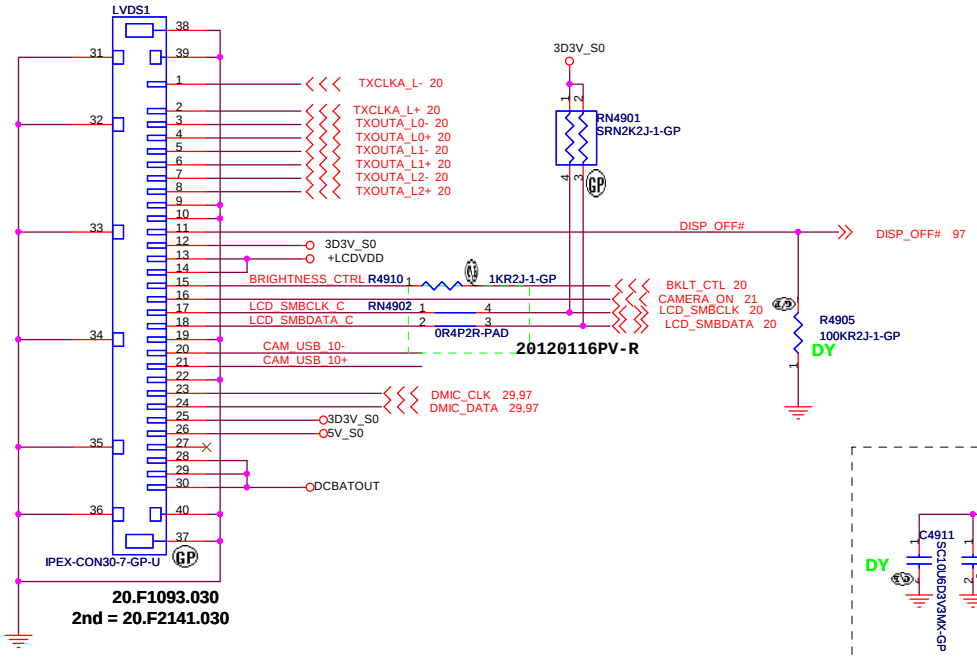
Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

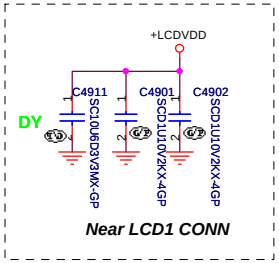
Date: Wednesday, March 14, 2012 | Sheet 48 of 103

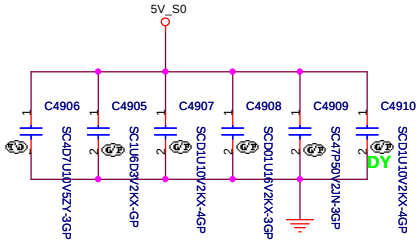
LCD Connector

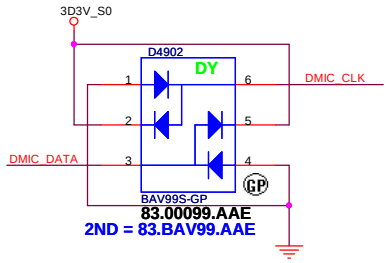
CARMER PINDEFINE

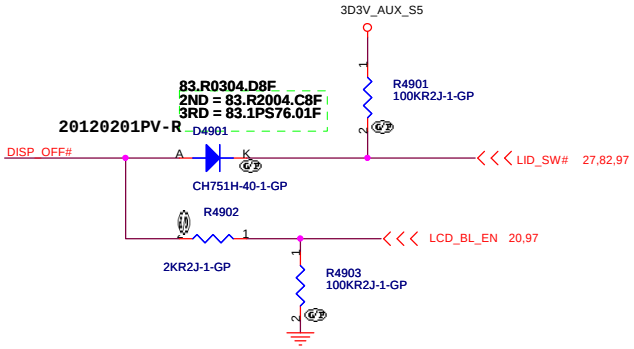
No.	Signal
1	DMIC_CLK
2	DMIC_DATA
3	GND
4	3.3V_MIC
5	5V_KBL
6	EN
7	VCC_5V
8	GND
9	D+
10	D-



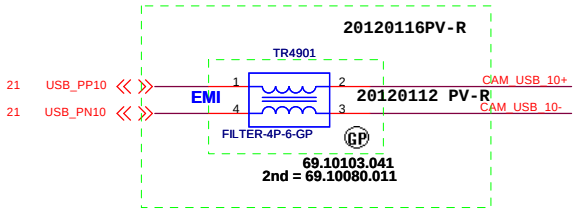




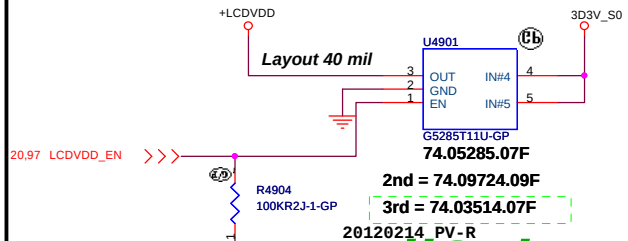




CAMERA



LCD POWER CIRCUIT



LED BACKLIGHT CONVERTER POWER

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

Date: Wednesday, March 14, 2012 | Sheet 49 of 103

CRT Connector

CRT1
Transmission line characteristic impedance for RGB signals Zo = 37.5 Ohm

Place these resistors as the closest components to connector CRT1

Transmission line characteristic impedance Zo= 50 Ohm

Transmission line characteristic impedance Zo = 50 Ohm

CRT RGB

68.00084.B61
2nd = 68.00245.051
3rd = 68.00226.141

MUX_R — L5001 BLM18BB470SN1D-GP — MUX_L_R — R5011 0R2J-2-GP — CRT_R
MUX_G — L5002 BLM18BB470SN1D-GP — MUX_L_G — R5012 0R2J-2-GP — CRT_G
MUX_B — L5003 BLM18BB470SN1D-GP — MUX_L_B — R5013 0R2J-2-GP — CRT_B

R1: R5001 R5002 R5003 75R2F-2-GP

C5001 C5002 C5003 SC22P50V2JN-4GP
C5004 C5005 C5006 SC22P50V2JN-4GP
C5007 C5008 C5009 SC22P50V2JN-4GP

DY DY DY 20120112 PV-R 20120116PV-R

DDC&HSYNC&VSYNC

3D3V_S0 — RN5007 SRN10KJ-5-GP — M_HSYNC, M_VSYNC

20120116PV-R
20 PCH_RED — R5006 0R0402-PAD — MUX_R
20 PCH_GREEN — R5007 0R0402-PAD — MUX_G
20 PCH_BLUE — R5008 0R0402-PAD — MUX_B

5V_S0_CRT — C5016 SCD1U16V2ZY-2GP

73.1G125.D0G
2nd = 73.07125.0AG
3rd = 73.1G125.0JH

U5001 U74AHCT1G125G-AL5-R-GP-U (OE# VCC A GND Y) — M_HSYNC
U5002 U74AHCT1G125G-AL5-R-GP-U (OE# VCC A GND Y) — M_VSYNC

20120116PV-R
20 CRT_HSYNC — RN5002 0R4P2R-PAD
20 CRT_VSYNC

5V @ ext. CRT side

HSYNC_5 — RN5003 SRN33J-5-GP — CRT_HSYNC_CON_1
VSYNC_5 — CRT_VSYNC_CON_1

DY DY C5018 C5017 SC10P50V2JN-4GP

3D3V_S0 — RN5004 SRN2K2J-1-GP

20120116PV-R
2011102PV
20120116PV-R
20 CRT_DDC_DATA — RN5008 0R4P2R-PAD
20 CRT_DDC_CLK

CRT_DDC_DATA_R — Q5003 2N7002KDW-GP — DDC_DATA_CON
CRT_DDC_CLK_R — DDC_CLK_CON

84.2N702.A3F
2nd = 84.2N702.B3F
3rd = 84.2N702.C3F

DDC

5V_S0_CRT — D5004 BAV99S-GP — CRT_VSYNC_CON_1
CRT_HSYNC_CON_1

83.00099.AAE
2ND = 83.BAV99.AAE

D5005 BAV99S-GP — DDC_CLK_CON, DDC_DATA_CON
83.00099.AAE
2ND = 83.BAV99.AAE

D5006 BAV99S-GP — CRT_R, CRT_G
83.00099.AAE
2ND = 83.BAV99.AAE

AFTP5001 AFTE14P-GP
CRT_R
CRT_G
CRT_B
DDC_DATA_CON
DDC_CLK_CON
CRT_VSYNC_CON_1
CRT_HSYNC_CON_1
5V_S0_CRT
AFTP5002 AFTE14P-GP
AFTP5003 AFTE14P-GP
AFTP5004 AFTE14P-GP
AFTP5005 AFTE14P-GP
AFTP5006 AFTE14P-GP
AFTP5007 AFTE14P-GP
AFTP5009 AFTE14P-GP
AFTP5011 AFTE14P-GP
AFTP5008 AFTE14P-GP
AFTP5010 AFTE14P-GP
AFTP5012 AFTE14P-GP

D5003 BAV99-5-GP-U — CRT_B
83.00099.T11
2nd = 83.B[illegible]9.D11
3rd = 83.BAV99.A11

3D3V_S0 — C5010 SCD1U10V2KX-4GP

5V_S0 — F5001 FUSE-1D1A6V-4GP-U — +5VS_CRT_F2 — Q5002 DMP2305U-7-GP — 5V_S0_CRT

1.1A/8V

84.02305.G31
2nd = 84.02377.031
3rd = 84.02035.031
20120210PV-R

69.50007.691
2nd = 69.50007.771
3rd = 69.60040.011

CRTVDD_EN# 1 — R5020 10KR2J-3-GP — CRTVDD_EN#
R5019 10KR2J-3-GP

C5020 SC4D7U10V5ZY-3GP DY
C5022 SCD1U16V2ZY-2GP

RN5001 SRN2K2J-1-GP

Q5001 2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31

5,27,37,42,96 PWR_GOOD

C5019 SCD1U16V2ZY-2GP

CRT1 D-SUB-15-123-GP
NC#4 NC#11
VCC_CRT
DDCDATA_ID1 DDCCLK_ID3 — DDC_DATA_CON, DDC_CLK_CON
CRT_RED CRT_GREEN CRT_BLUE — CRT_R, CRT_G, CRT_B
VSYNC HSYNC — CRT_VSYNC_CON_1, CRT_HSYNC_CON_1
GND ×8

20.20938.015
2nd = 20.20984.015

C5023 C5021 C5024 C5025 SC33P50V2JN-3GP
SC22P50V2JN-4GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
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HDMI Connector

HDMI CONN

20120130PV-R

TR5101
HDMI_CLK_R_C
HDMI_CLK_R_C#
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5103
HDMI_DATA1_R_C
HDMI_DATA1_R_C#
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5102
HDMI_DATA0_R_C
HDMI_DATA0_R_C#
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

TR5104
HDMI_DATA2_R_C
HDMI_DATA2_R_C#
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
COIL-90OHM-100MHZ-3-GP
68.11900.20A
2nd = 69.10098.031
3rd = 69.10118.021

HDMI_PLL_GND
DY
R5123
0R2J-2-GP
Q5103
2N7002K-2-GP
84.2N702.J31
2nd = 84.07002.I31
3rd = 84.2N702.W31
3D3V_S0
DY
R5113
100KR2J-1-GP

HDMI1
SKT-HDMI23-54-GP
22.10296.721
2nd = 22.10296.761
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
5V_S0_CRT
C5102
SCD1U10V2KX-5GP
HPD_HDMI_CON

Close to PCH

20 HDMI_CLK_R#
20 HDMI_CLK_R
C5103
C5104
SCD1U10V2KX-5GP
HDMI_CLK_R_C#
HDMI_CLK_R_C

20 HDMI_DATA0_R#
20 HDMI_DATA0_R
C5105
C5106
SCD1U10V2KX-5GP
HDMI_DATA0_R_C#
HDMI_DATA0_R_C

20 HDMI_DATA1_R#
20 HDMI_DATA1_R
C5110
C5107
SCD1U10V2KX-5GP
HDMI_DATA1_R_C#
HDMI_DATA1_R_C

20 HDMI_DATA2_R#
20 HDMI_DATA2_R
C5108
C5109
SCD1U10V2KX-5GP
HDMI_DATA2_R_C#
HDMI_DATA2_R_C

Close to HDMI Connector

RN5106
SRN680J-GP
RN5107
SRN680J-GP
HDMI_PLL_GND

3D3V_S0
84.03904.L06
2nd = 84.03904.X11
Q5102
PMBS3904-1-GP
HDMI_HPD_R1
HDMI_HPD_B1
R5111
150KR2J-L1-GP
DY
R5110
200KR2J-L1-GP
R5128
0R0402-PAD
HDMI_PCH_DET 20,97
R5112
20KR2F-L-GP
20120116PV-R

5V_S0_CRT
RN5101
SRN2K2J-1-GP
3D3V_S0
Q5104
2N7002KDW-GP
20 PCH_HDMI_CLK
20 PCH_HDMI_DATA
DDC_CLK_HDMI
DDC_DATA_HDMI
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 84.2N702.P3F

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Conn
Size: A3
Document Number: 2012 S-Series Richie 13.3
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(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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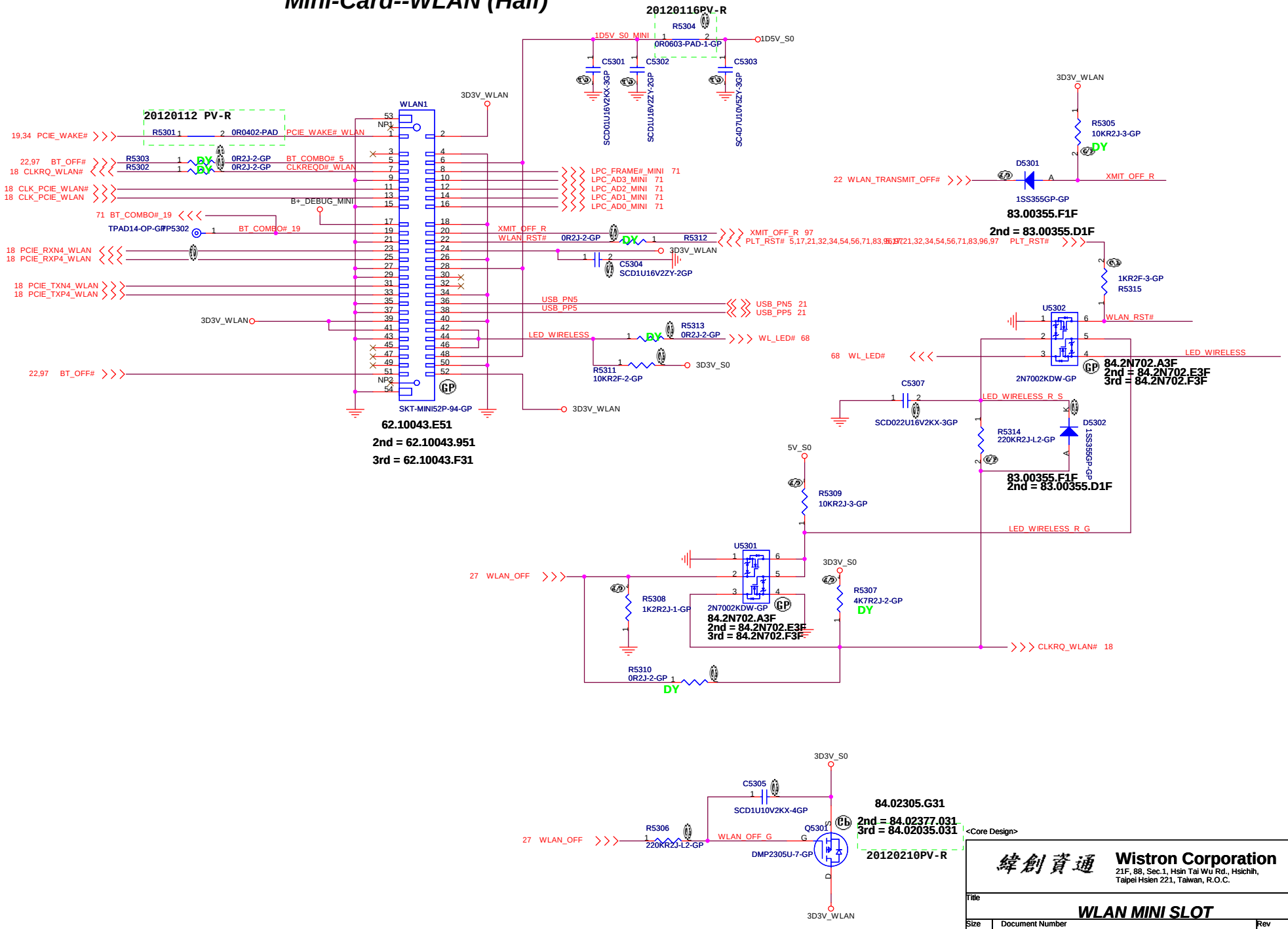
WLAN Connector

Mini-Card--WLAN (Half)



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	WLAN MINI SLOT
Size: A3	Document Number: 2012 S-Series Richie 13.3
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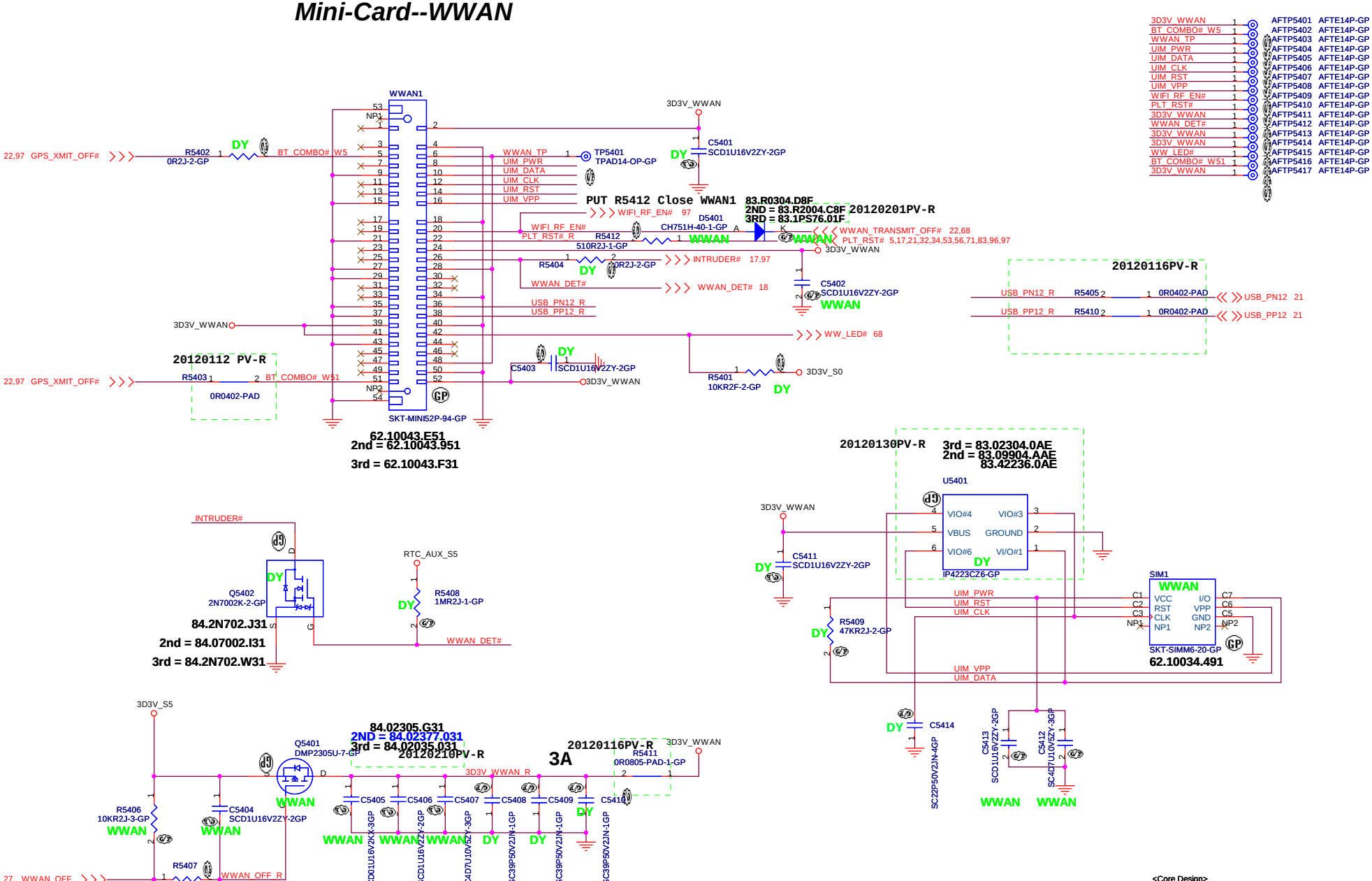
Date: Wednesday, March 14, 2012	Sheet 53 of 103

WWAN Connector

Mini-Card--WWAN



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	WWAN MINI SLOT/SIM
Size: A3	Document Number: 2012 S-Series Richie 13.3
Rev: -1	
Date: Wednesday, March 14, 2012	Sheet 54 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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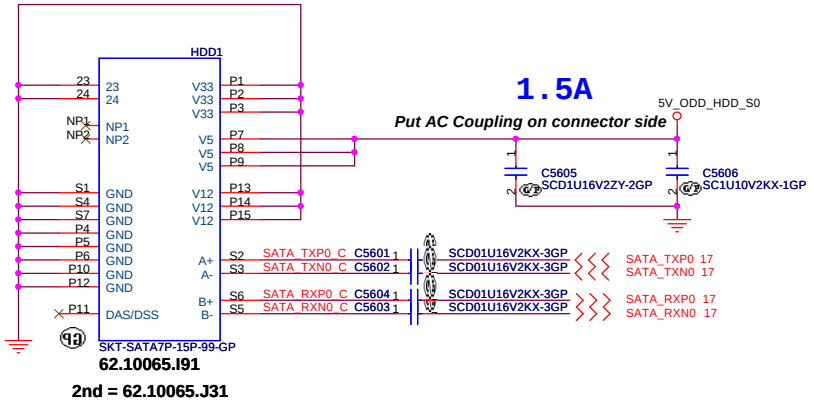
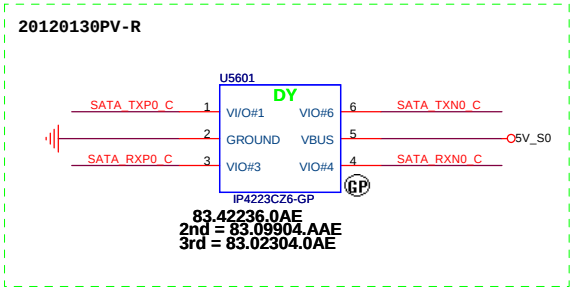
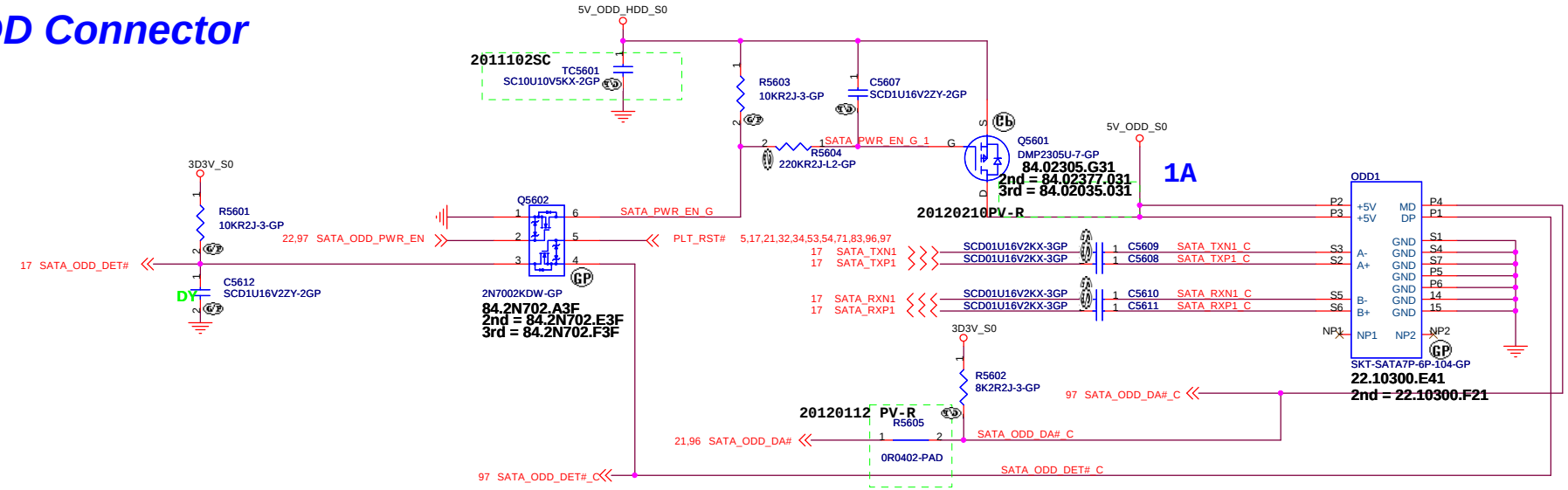
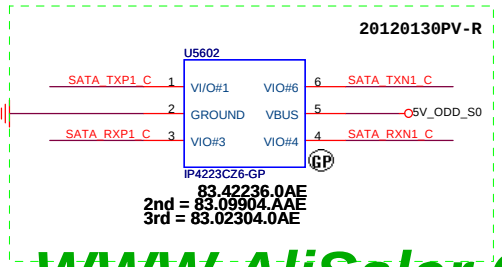
HDD Connector





ODD Connector





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

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<Core Design>

緯創資通 Wistron Corporation
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Title: *(Reserved)*

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<Core Design>

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Title: *(Reserved)*

Size	Document Number	Rev
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<Core Design>

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Title: *Reserved*

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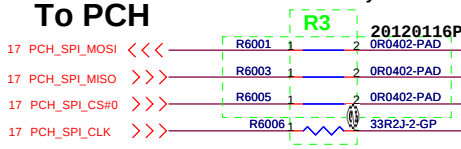
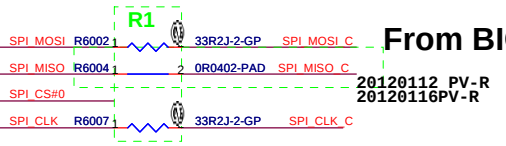
SSID = Flash.ROM

To PCH

R3 closley to PCH side

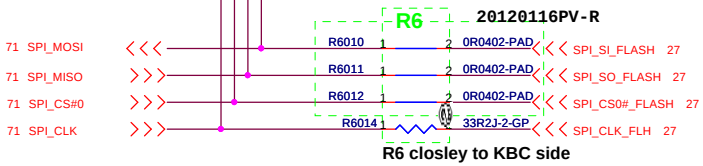


R1 closley to SPI ROM side



From BIOS

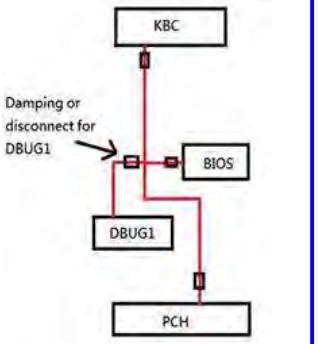
20120112_PV-R
20120116PV-R



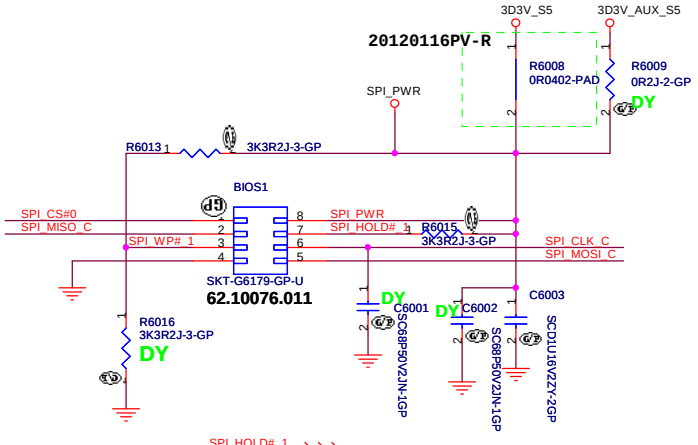
R6 closley to KBC side

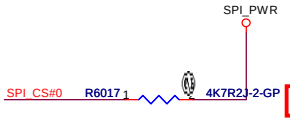
From KBC

SPI Layout Note



SYSTEM SPI ROM Socket





NOTE: SPI signal use GND reference

SPI ROM PART

72.25Q64.F01	W25Q64FVSSIG	WINBOND
72.25Q64.D01	N25Q064A13ESE40F	NUMONYX

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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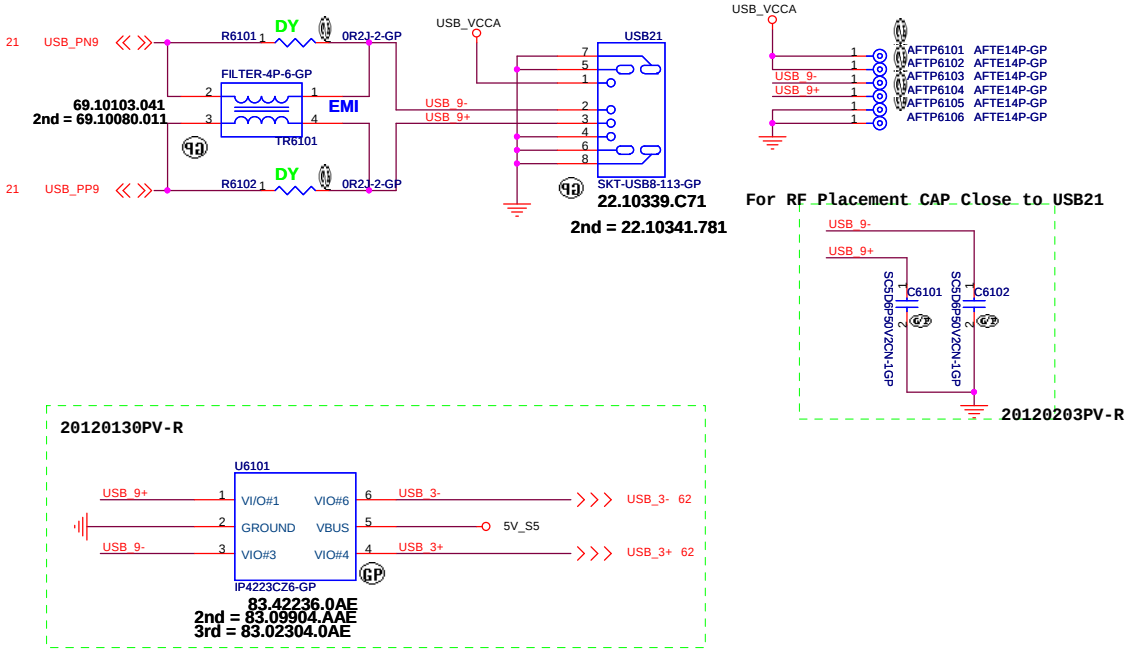
Right Side USB 2.0 Connector

Right Side USB 2.0



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: USB Power SW		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
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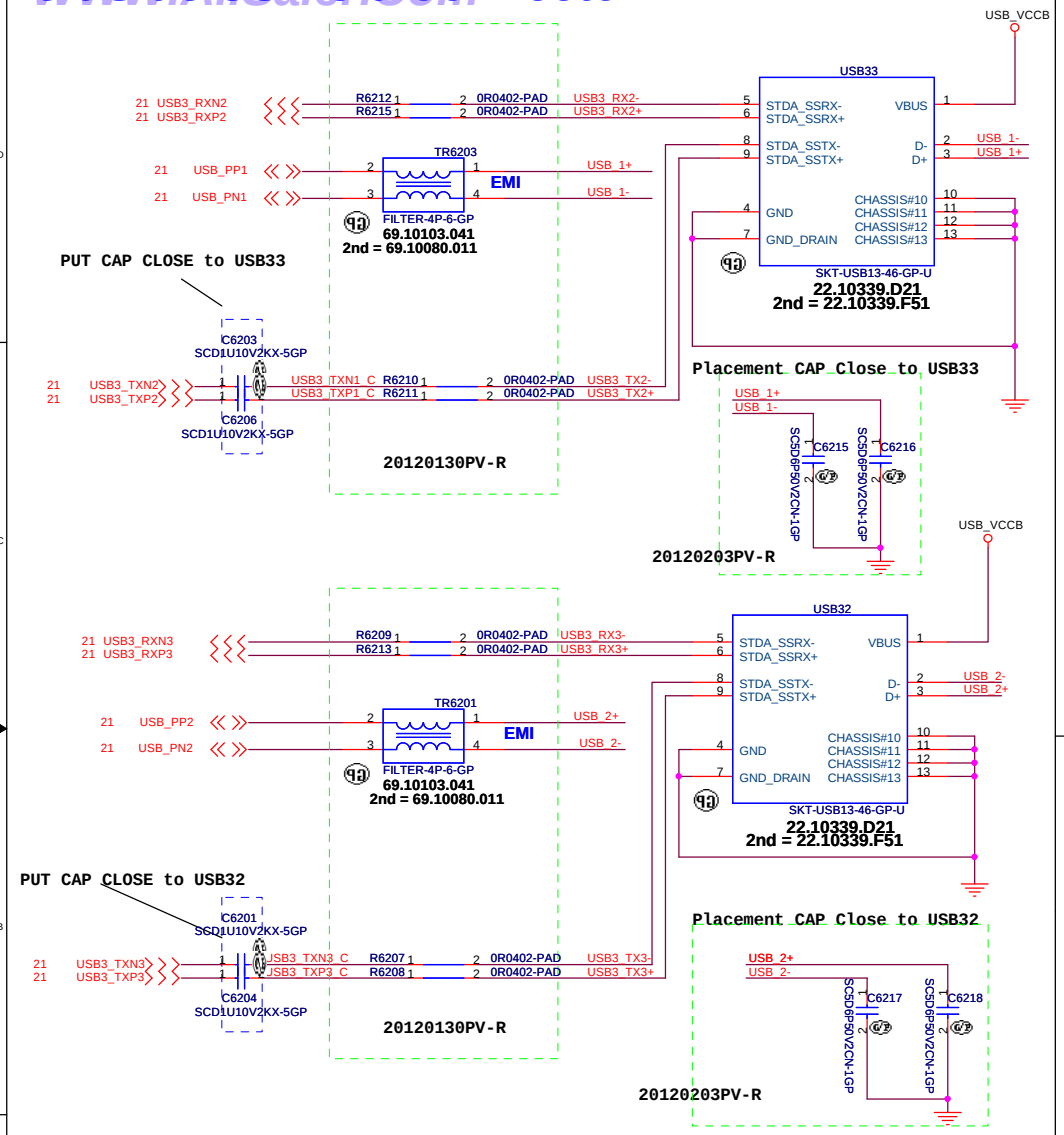
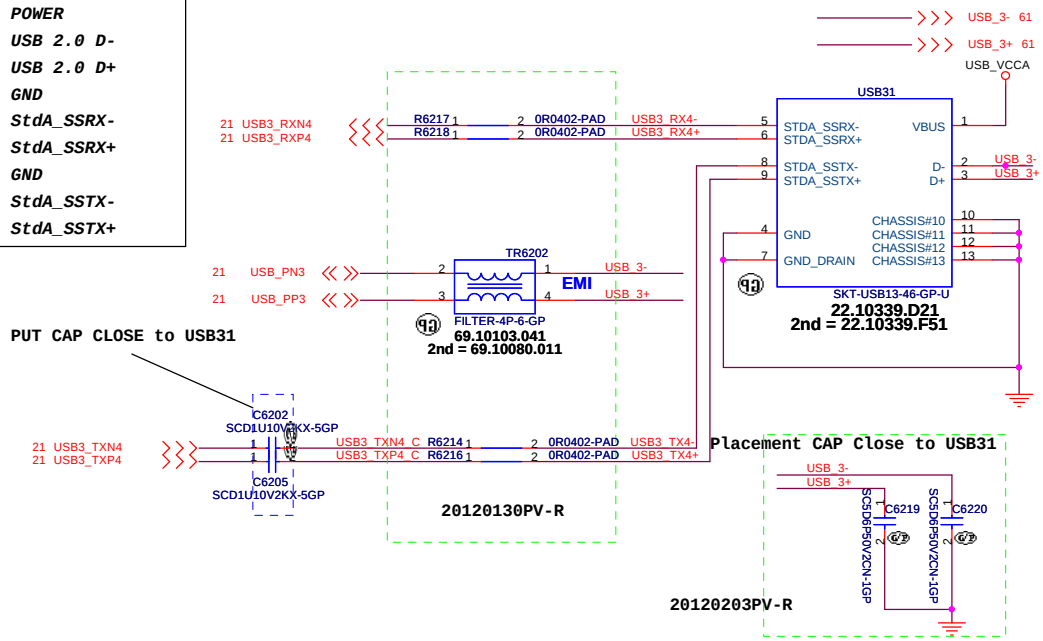
Left Side USB 3.0 Connector

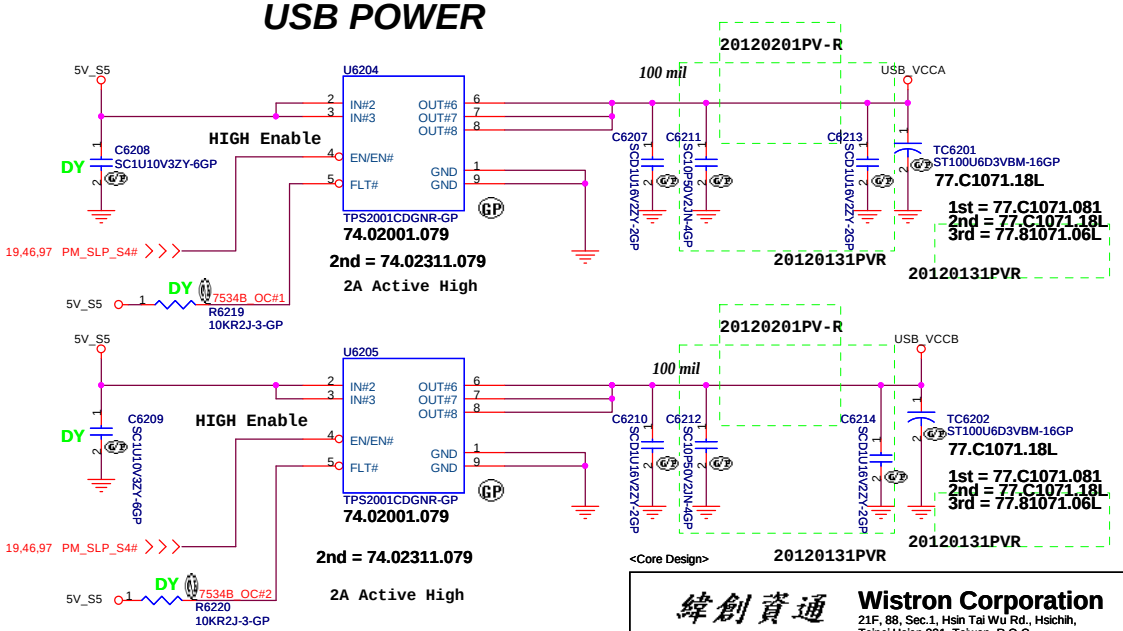


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+

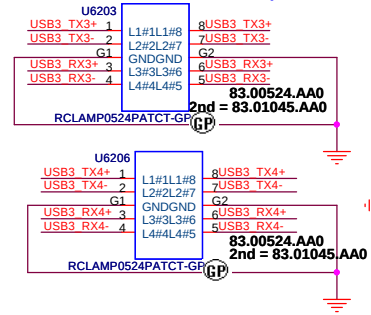
Right Side USB 3.0 Connector



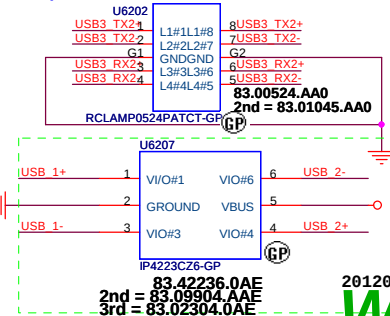
USB POWER



Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays
(Pin5.6.7.8 No Internal Connection)



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	USB3.0		
Size A3	Document Number 2012 S-Series Richie 13.3		Rev -1
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
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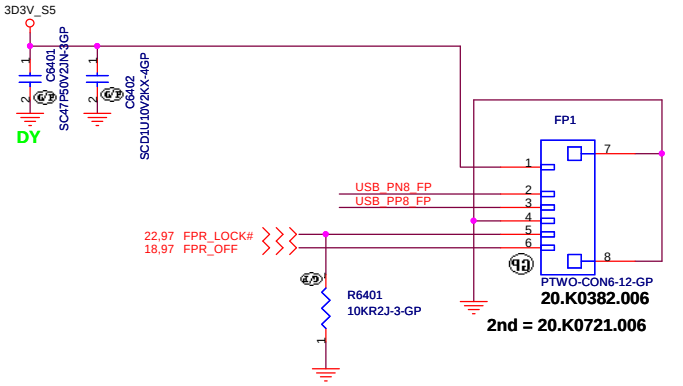
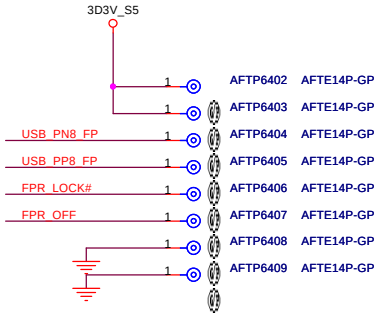
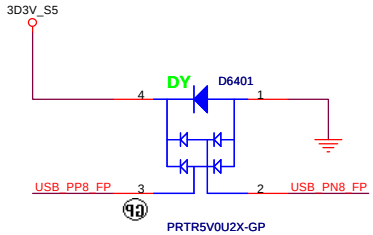
Finger Printer Connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Finger Print Conn		
Size: A3	Document Number: 2012 S-Series Richie 13.3	Rev: -1
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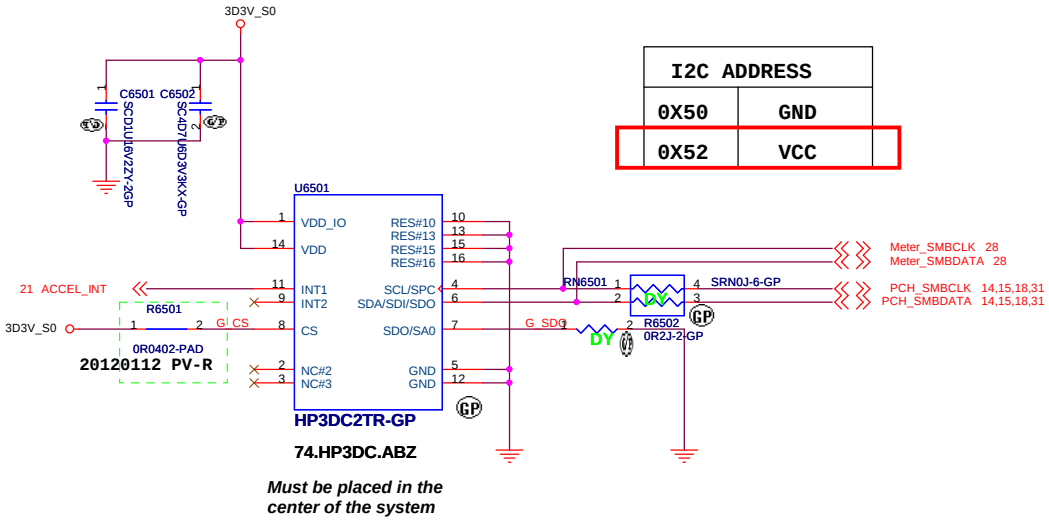
ACCELEROMETER



I2C ADDRESS	
0X50	GND
0X52	VCC

Must be placed in the center of the system

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ACCELEROMETER

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

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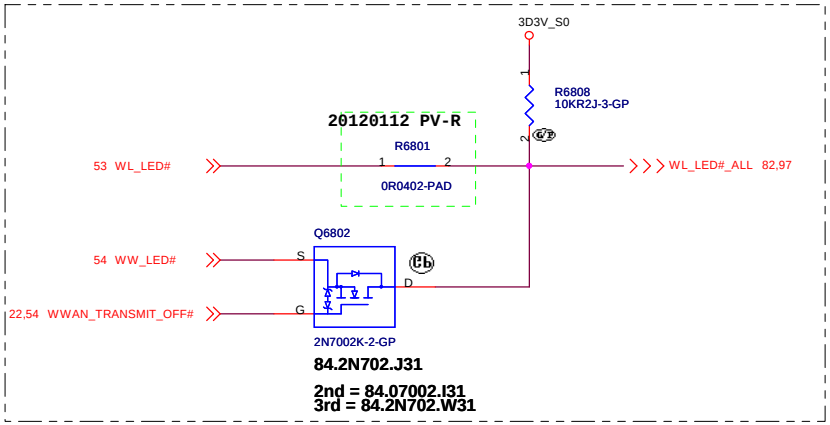
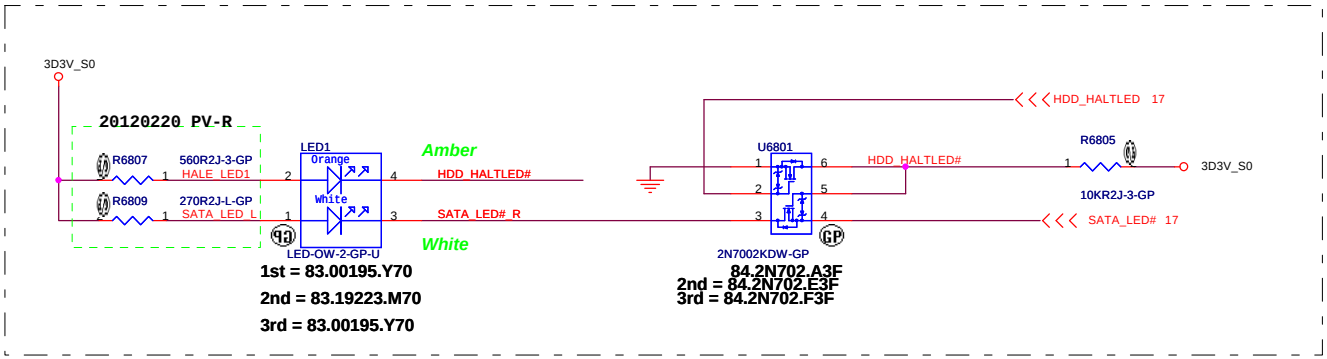
WLAN / WWAN POWER LED



HDD LED



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Control

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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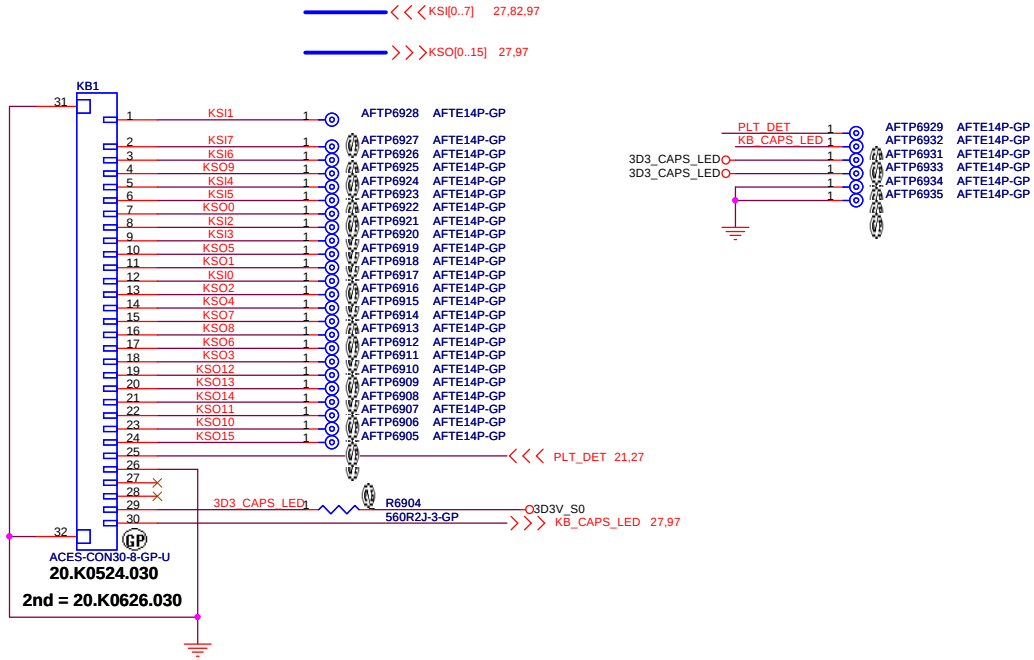
Keyboard Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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<Core Design>

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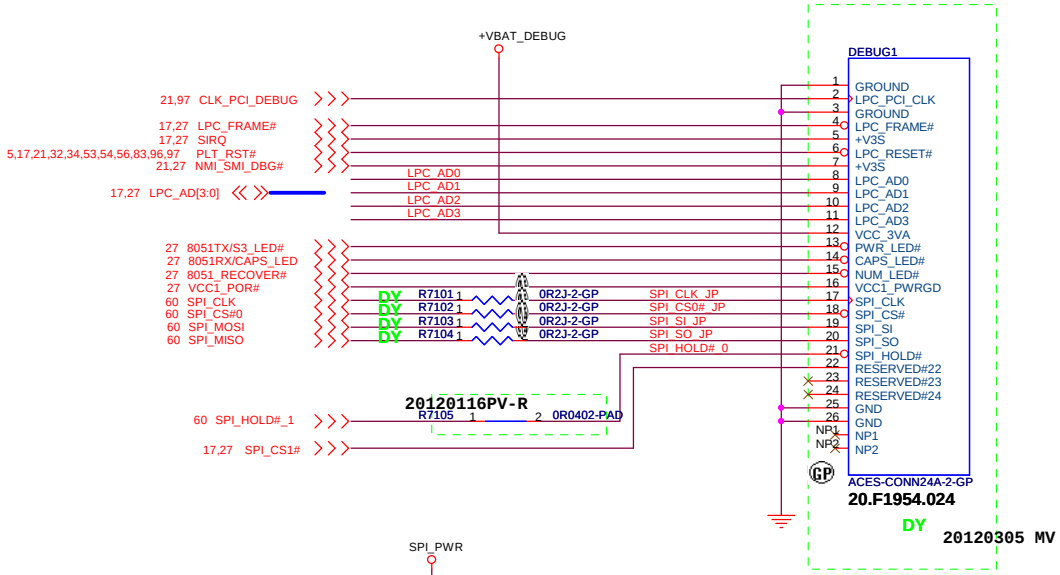
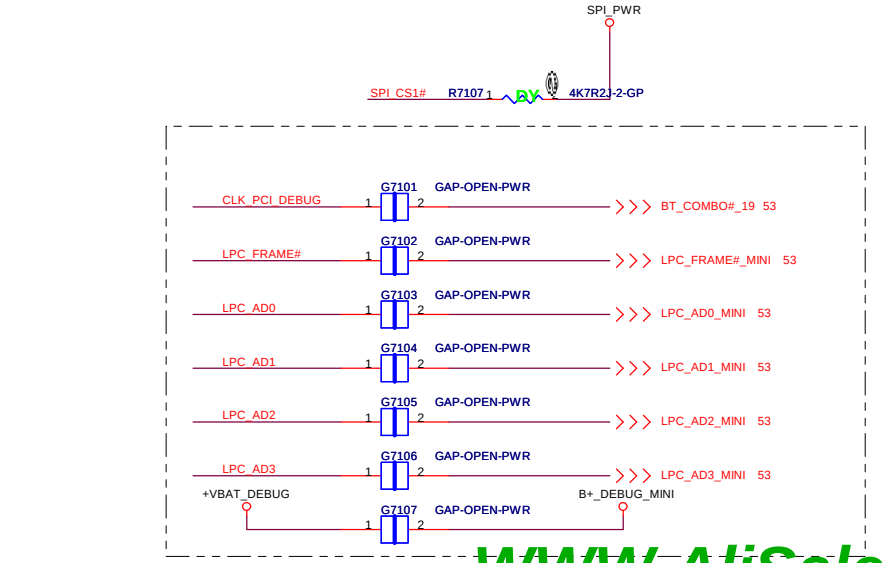
24 PIN LPC DEBUG CONN.





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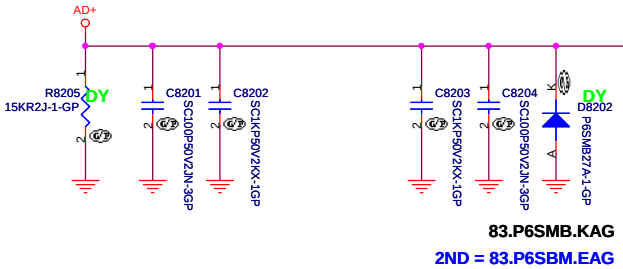
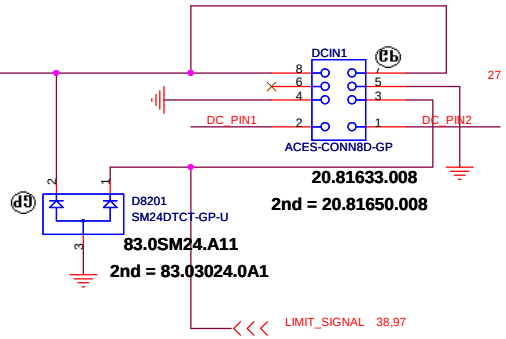
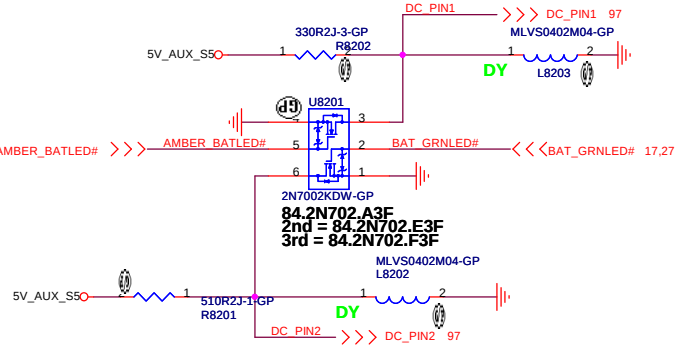
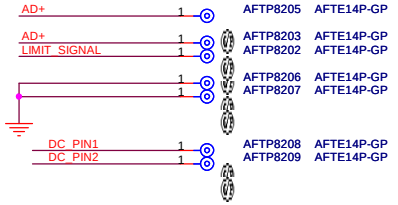
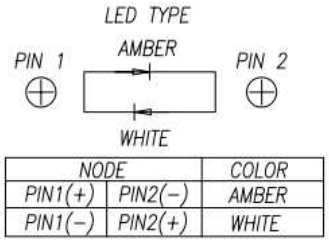
Adaptor in to generate DCBATOUT







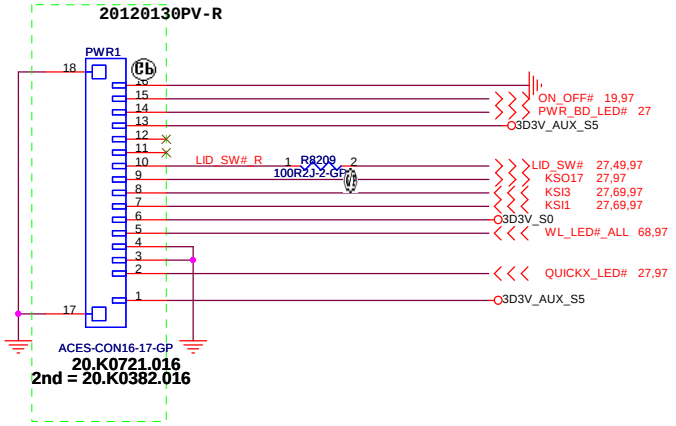


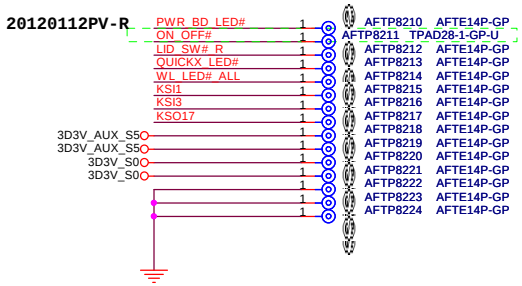


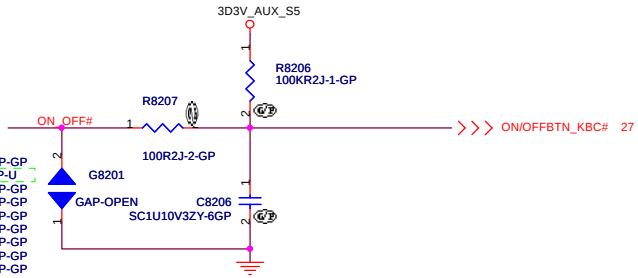
NODE		COLOR
PIN1(+)	PIN2(−)	AMBER
PIN1(−)	PIN2(+)	WHITE

	KBC pin 120 BAT_GRNLED#	KBC pin 113 AMBER_BATLED#
Amber	High	Low
White	Low	High
LED OFF	Low	Low

Power Button +Quick Lanch board







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Title: POWER Button/ DCIN Connector

Size	Document Number	Rev
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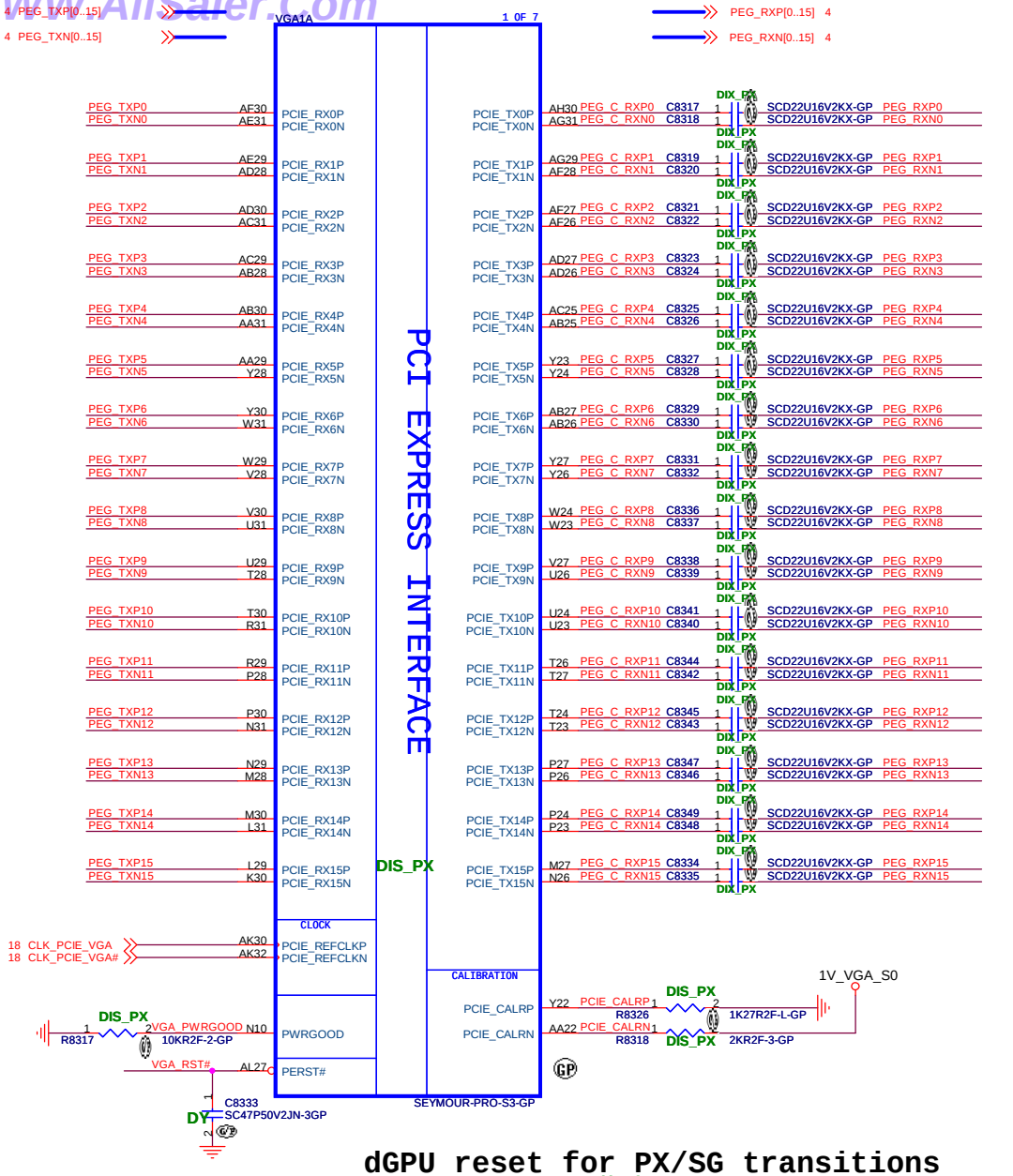
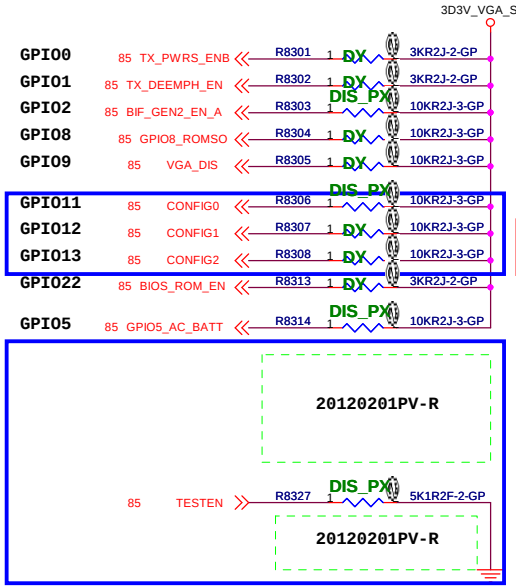


CONFIGURATION STRAPS

ALLOW FOR PULL-UP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

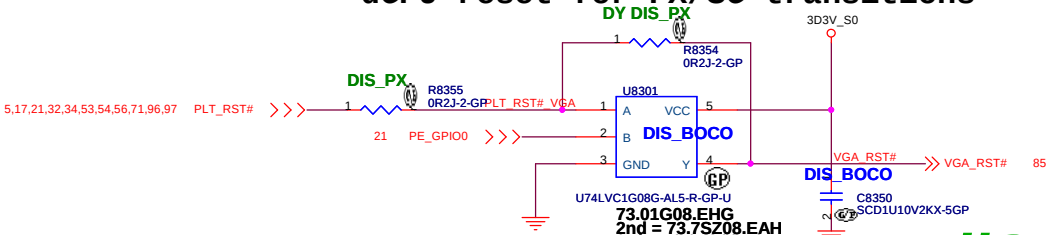


GPIO_13	GPIO_12	GPIO_11	Memory Aperture Size
0	0	1	512MB/256MB memory aperture (Default)
1	1	0	reserved

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

dGPU reset for PX/SG transitions



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Title: GPU PCIE/STRAPPING(1/5)

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A3	2012 S-Series Richie 13.3	-1

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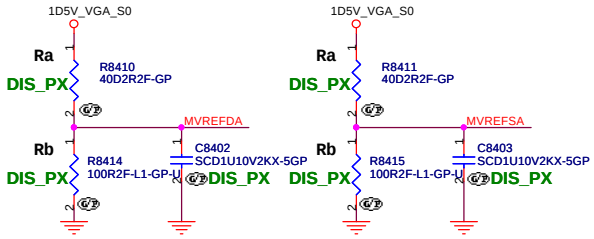
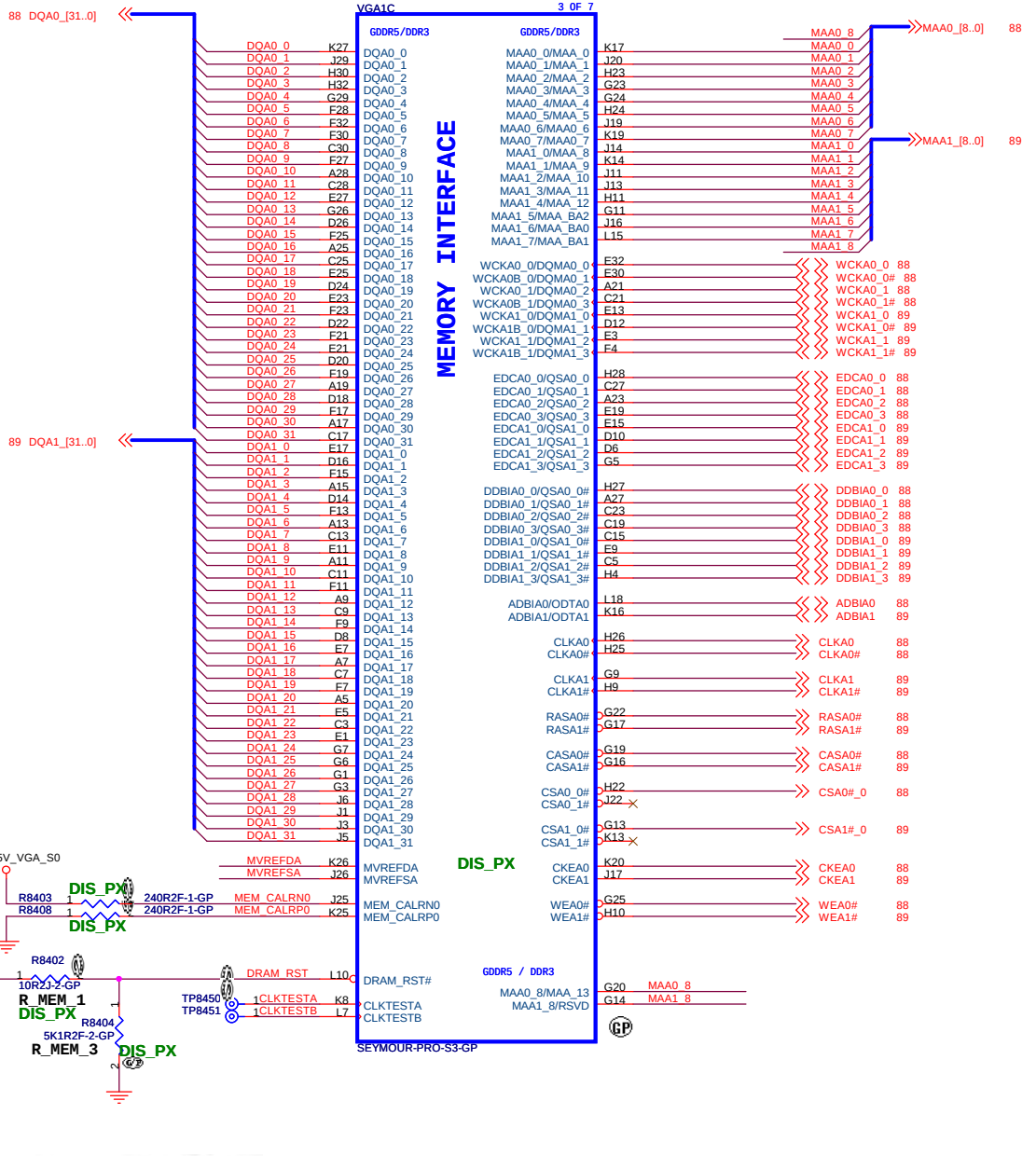
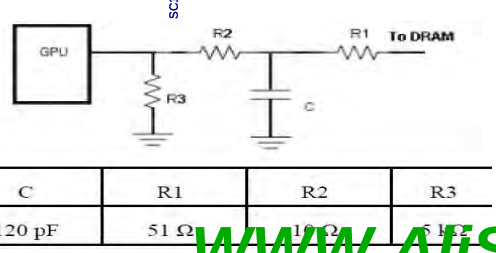


GDDR3/GDDR5 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R





C	R1	R2	R3
120 pF	51 Ω	10 Ω	5 kΩ

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Title: GPU Memory(2/5)

Size	Document Number	Rev
A3	2012 S-Series Richie 13.3	-1

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VRAM ID TABLE

MEM ID3	MEM ID2	MEM ID1	MEM ID0	MEM ID VALUE	Vendor & PN	DIE Ver
NC	NC	0	0	0	Samsung(128X16) K4G20325FC-HC04	C
NC	NC	1	0	2	Samsung(128X16) K4G20325FD-FC04	D
NC	NC	0	1	1	Hynix(128MX16) H5GQ2H24MFR-T2C	M
NC	NC	1	1	3	Hynix(128MX16) H5GQ2H24AFR-T2C	A
NC	NC	0	0	0	Elpida(128MX16) EDW2032BBBG-50-F	B
NC	NC	NC	NC	NC	UMA	

Reserve Pul-High Resistor for MEM_ID2/MEM_ID3

0= Old Die
1= New Die

VBIOS 1 : Samsung
VBIOS 2 : Hynix
VBIOS 3 : Elpida

GPU Power ID Table

GPU SIDE		UP1527QQDD
GPIO_15_PWRCNTL_0	GPIO_20_PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V

LVDS Interface

VGA1F 6 OF 7

LVDS CONTROL: VARY_BL, DIGON

LVTMDP: TXCLK_UP_DPF3P/N, TXOUT_U0P_DPF2P/N, TXOUT_U1P_DPF1P/N, TXOUT_U2P_DPF0P/N, TXOUT_U3P/N, TXCLK_LP_DPE3P/N, TXOUT_L0P_DPE2P/N, TXOUT_L1P_DPE1P/N, TXOUT_L2P_DPE0P/N, TXOUT_L3P/N

SEYMOUR-PRO-S3-GP

CTF setpoint is 118°C, and is programmed during ASIC initialization.

Intel is H_THERMTRIP#

SSEL1 (Pin 3)	SSEL0 (Pin 7)	Spread Percent (%) SSCLK (Pin 5)
Low (VSS)	Low (VSS)	Spread Off (No Spread)
Low (VSS)	Middle (Floating)	-0.50%
Low (VSS)	High (VDD)	-0.5%
Middle (Floating)	Low (VSS)	-0.25%
Middle (Floating)	Middle (Floating)	-0.75%
Middle (Floating)	High (VDD)	-1.0%
High (VDD)	Low (VSS)	-1.5%
High (VDD)	Middle (Floating)	-2.0%
High (VDD)	High (VDD)	-3.0%

Recommended Clock-Input Configurations

Memory Type	Description
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

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Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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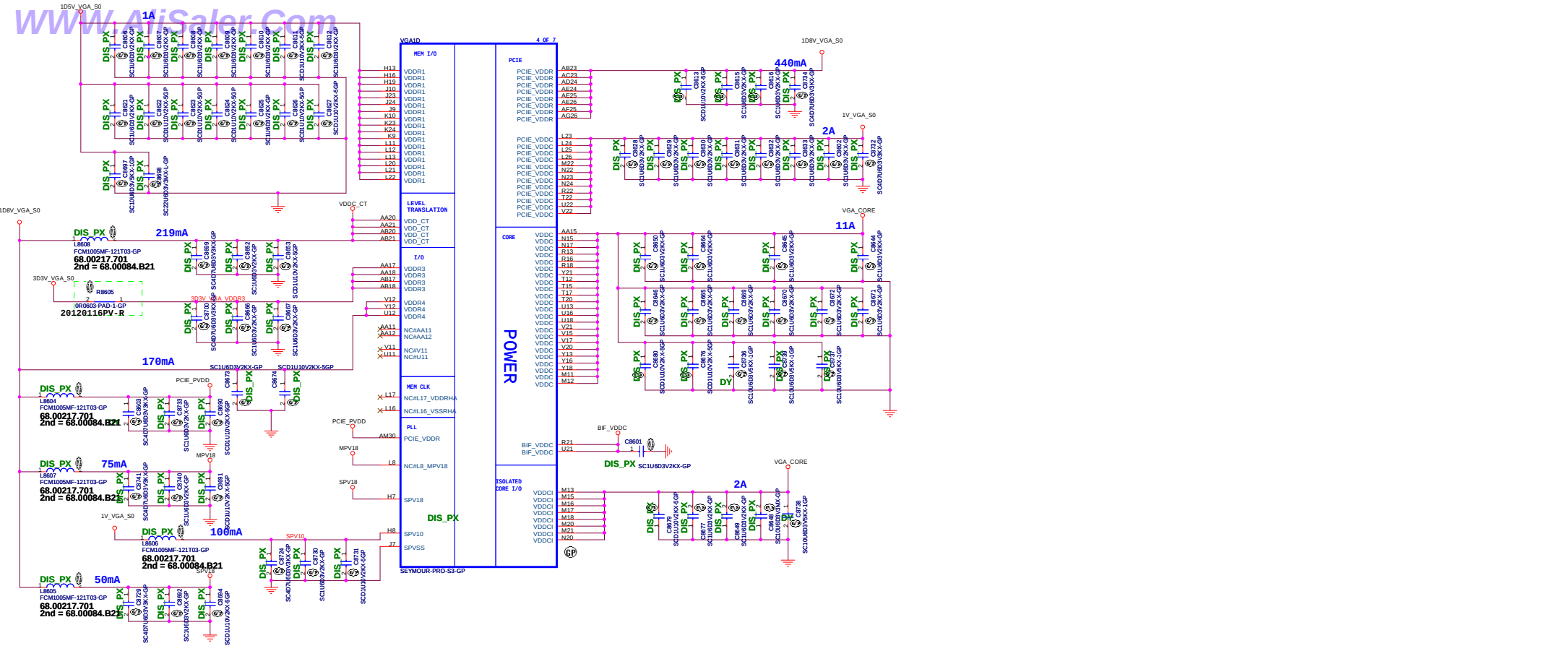
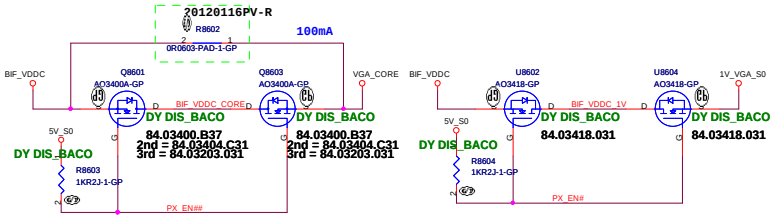
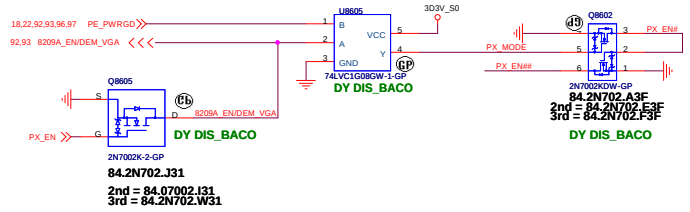




	PX_EN	8209A_EN/DEM_VGA	PX_MODE	PX_EN#	PX_EN##	BIF_VDDC
Non-BACO	0	1	1	0	1	VGA_Core
BACO	1	0	0	1	0	1V_VGA

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE



PX_EN	Mode	BIF_VDDC
0	Normal	VGA_Core
1	BACO	1V_VGA

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Title: GPU_POWER(4/5)

Size	Document Number	Rev
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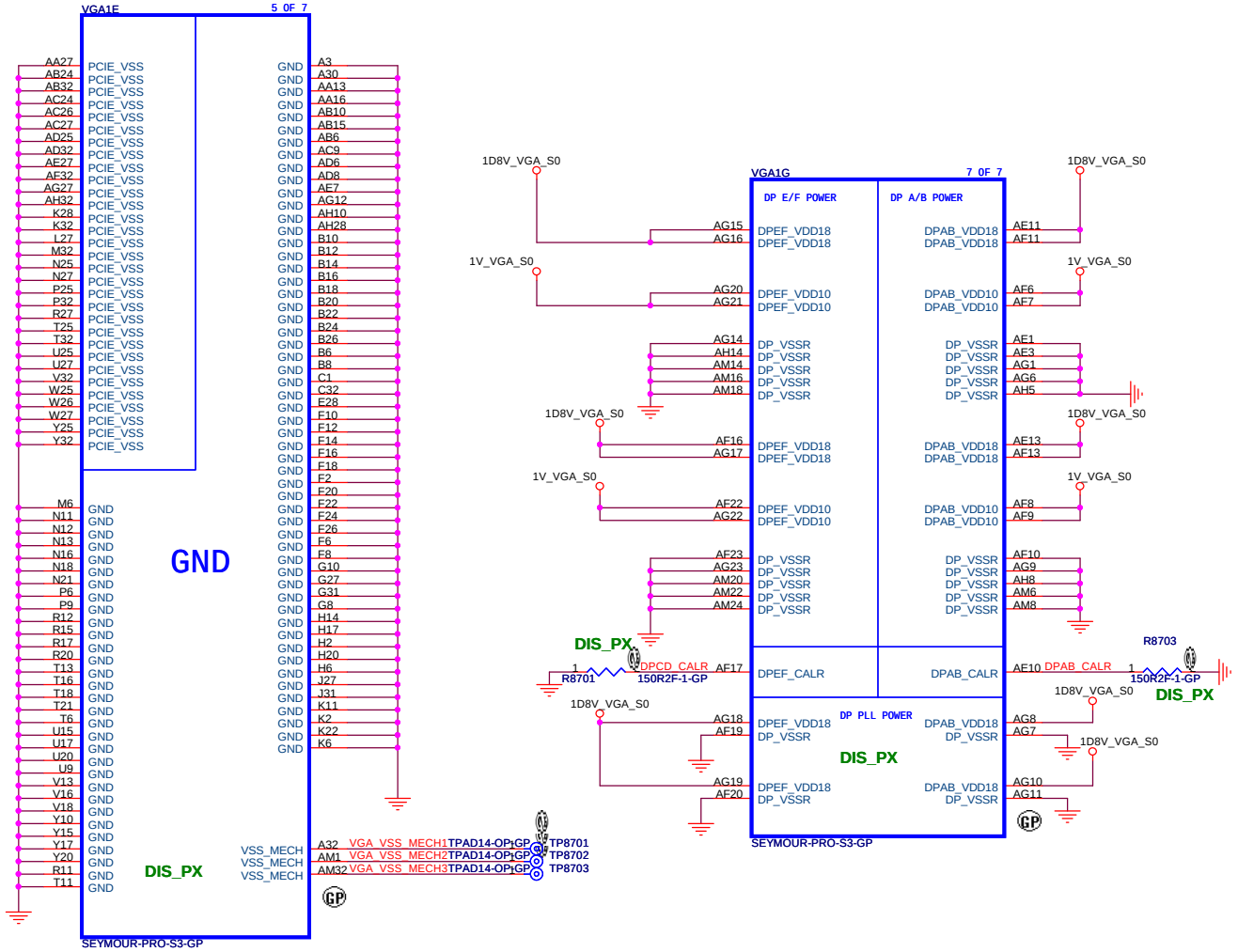

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Title: GPU_DPPWR/GND(5/5)

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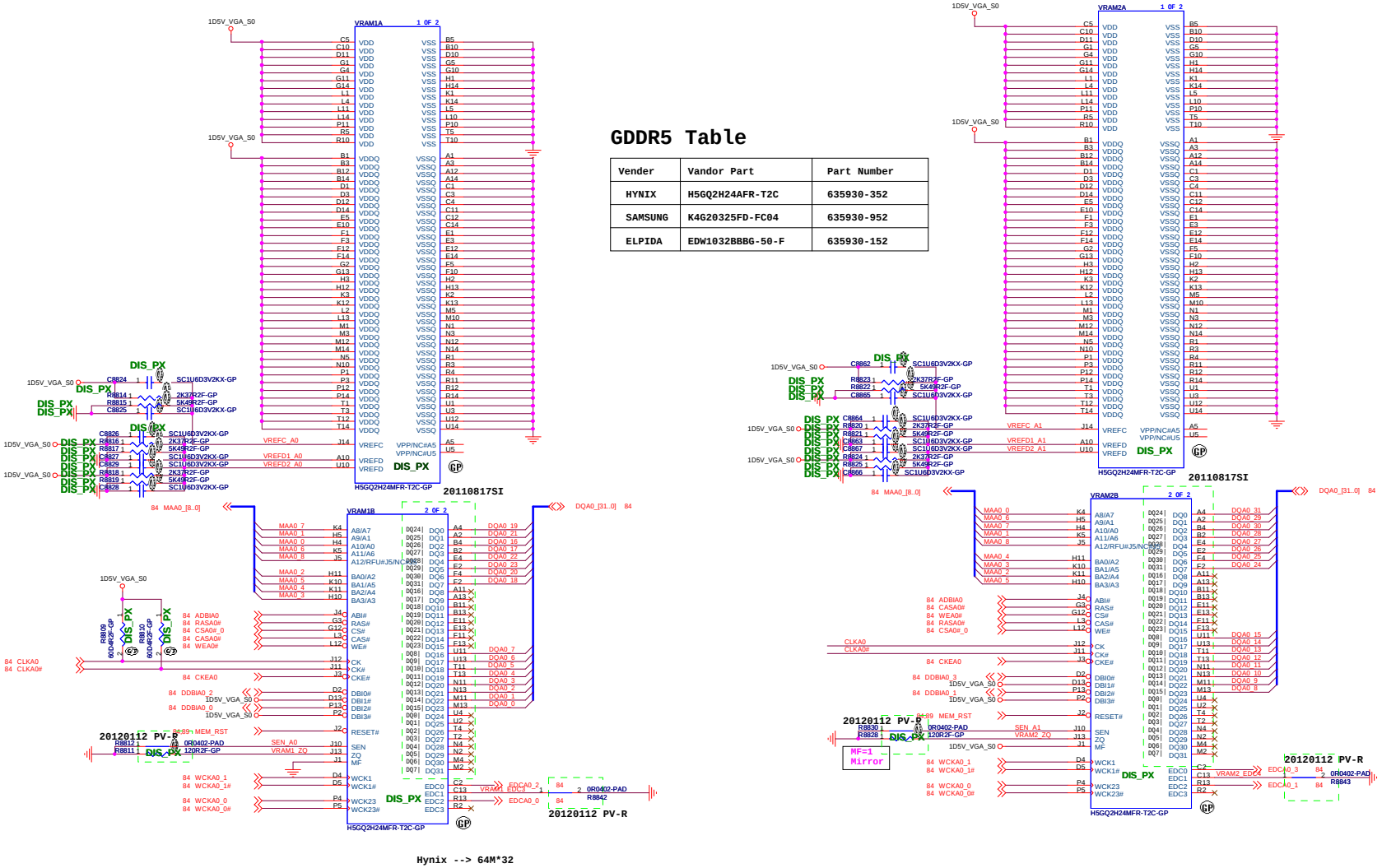
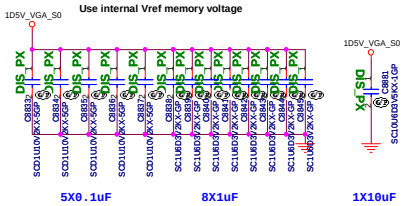
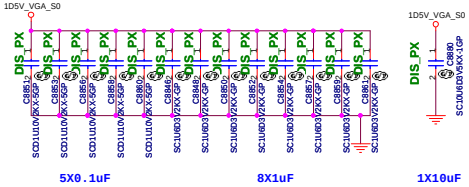
GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24AFR-T2C	635930-352
SAMSUNG	K4G20325FD-FC04	635930-952
ELPIDA	EDW1032BBBG-50-F	635930-152







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Title: GPU-VRAM1,2 (1/4)
Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1
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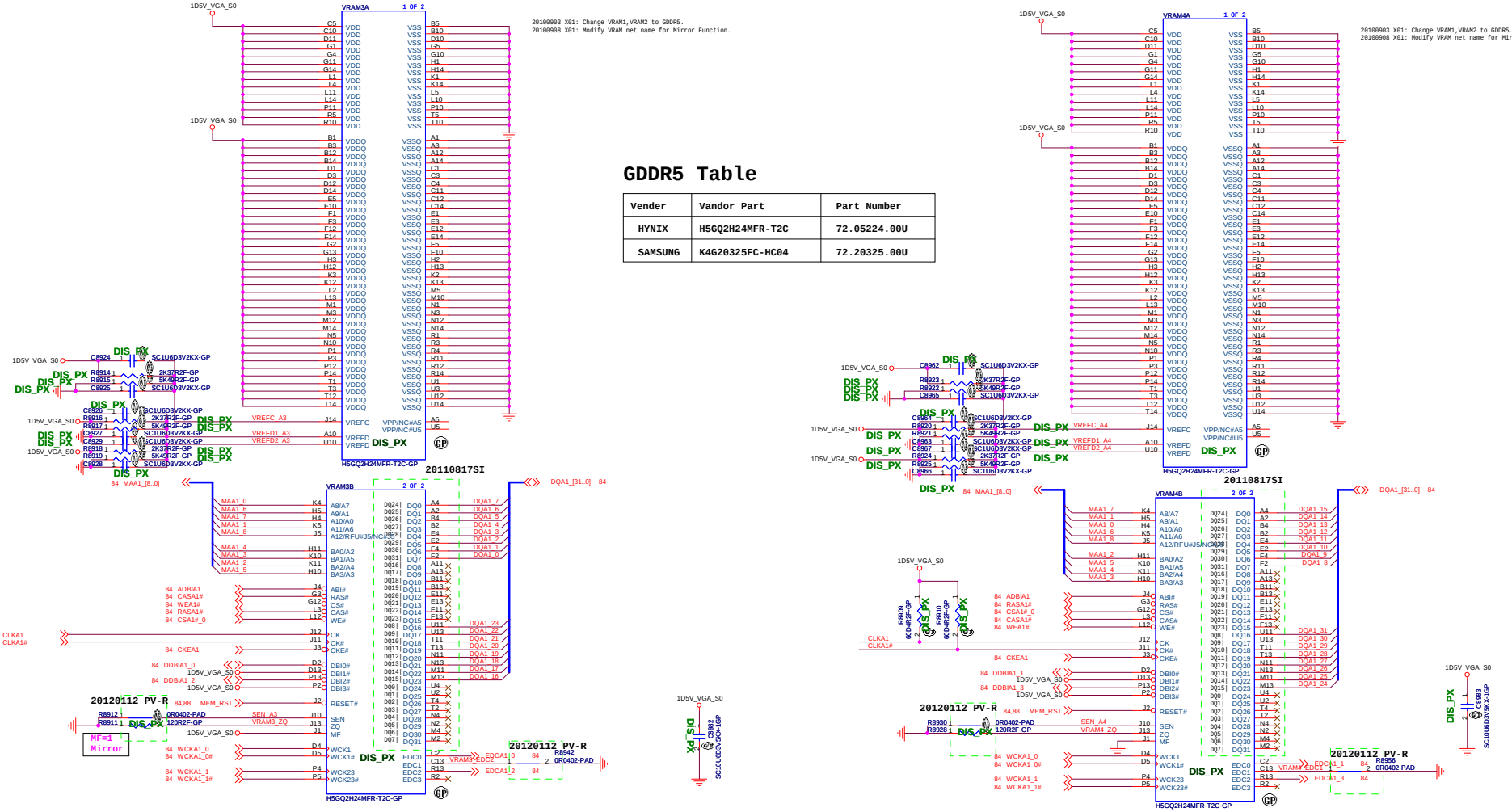
GDDR5 Table

Vender	Vandor Part	Part Number
HYNIX	H5GQ2H24MFR-T2C	72.05224.00U
SAMSUNG	K4G20325FC-HC04	72.20325.00U



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Title: GPU-VRAM3,4 (2/4)

Size: A2 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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Title: (Reserved) GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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Title: (Reserved) GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: 2012 S-Series Richie 13.3 | Rev: -1

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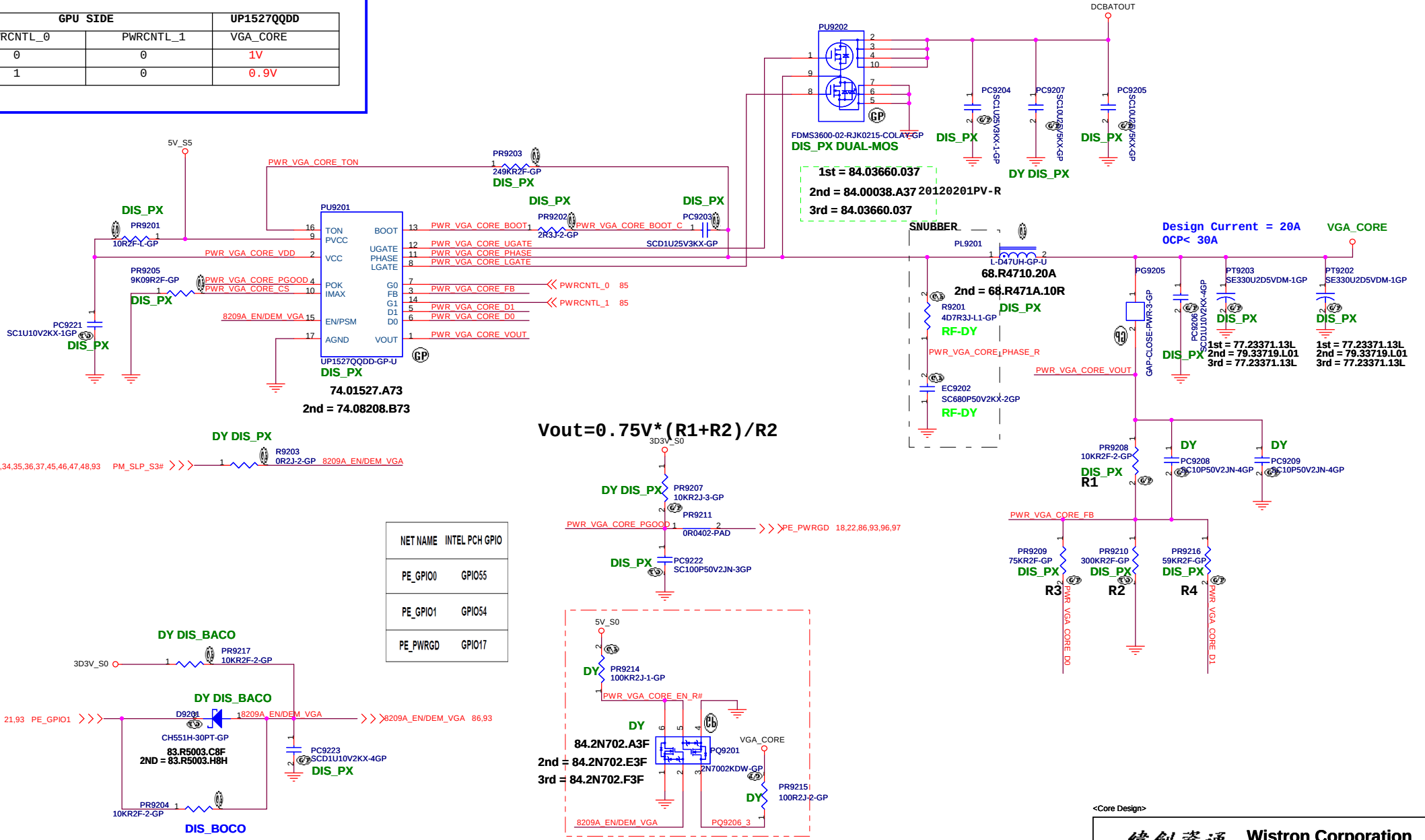
+VGA_CORE

GPU Power ID Table

Thames Pro S3 GDDR5

GPU SIDE		UP1527QQDD
PWRCNTL_0	PWRCNTL_1	VGA_CORE
0	0	1V
1	0	0.9V



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Title: VGA_ISL95870

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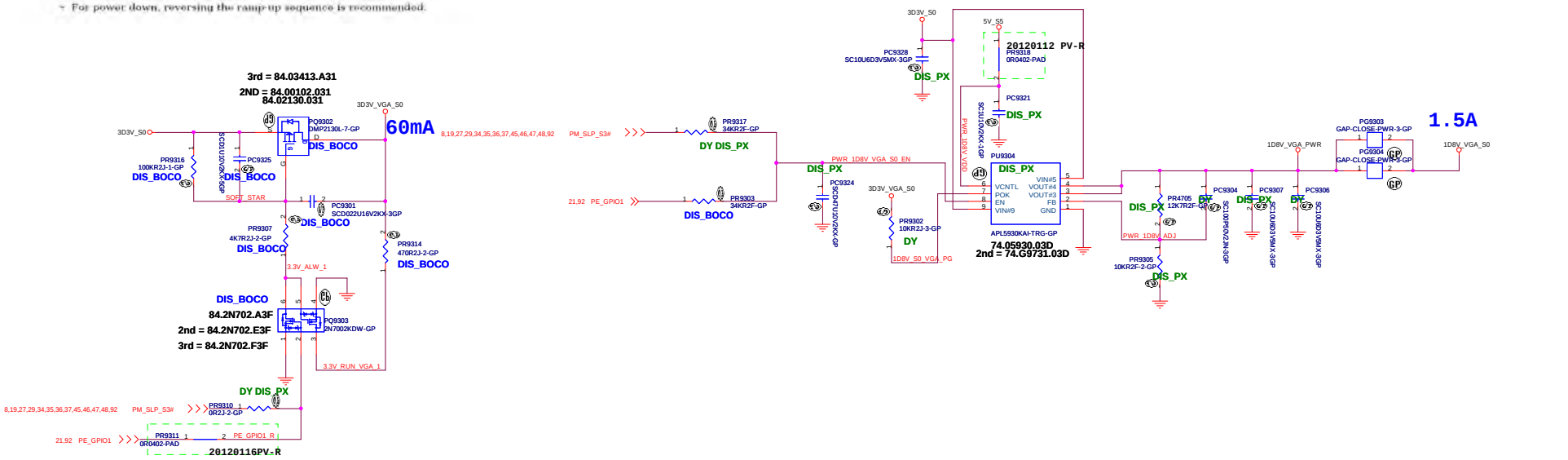
5.3 Power-Up/Down Sequence

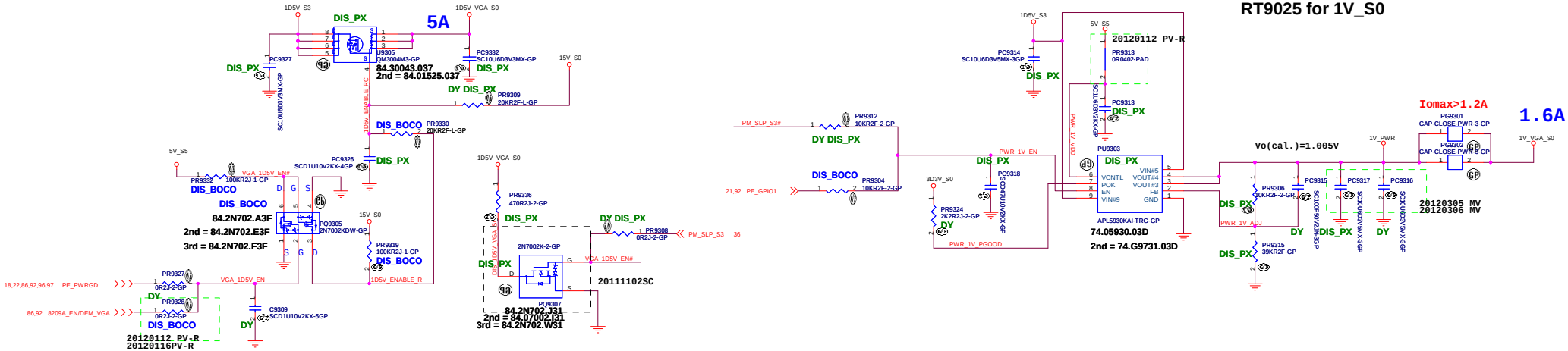
Seymour has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies, except for **VDDR3**, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of **VDDR3** relative to other power rails.
- The external pull-up resistors on the **DDC/AUX** signals (if applicable) should ramp up before or after both **VDDC** and **VDD_CT** have ramped up.
- **VDDC** and **VDD_CT** should not ramp up simultaneously. For example, **VDDC** should reach 90% before **VDD_CT** starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

3D3V_VGA_S0 > VGA_CORE > 1V_VGA_S0 > 1D5V_VGA_S0 > 1D8V_VGA_S0



1D5V_VGA_S0



<Variant Name>

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Title: DISCRETE VGA POWER

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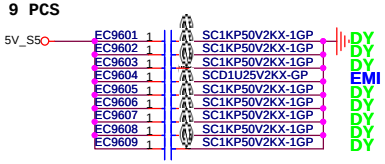
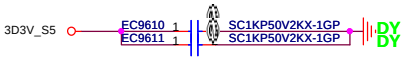
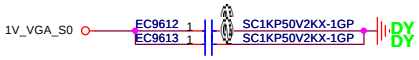
5V_S5 9 PCS



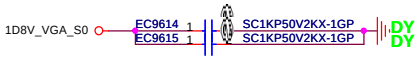
1D8V_PWR 2 PCS



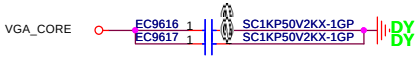
1V_VGA_S0 2 PCS



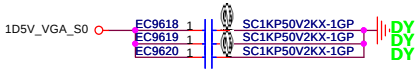
1D8V_VGA_S0 2 PCS



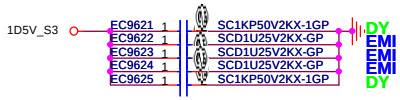
VGA_CORE 2 PCS



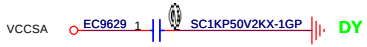
1D5V_VGA_S0 2 PCS



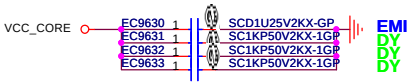
1D5V_S3 8 PCS



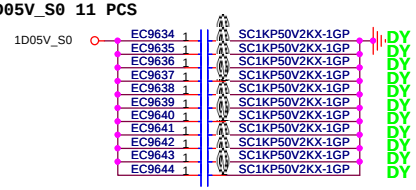
VCCSA 1 PCS



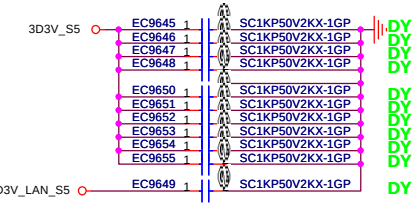
VCC_CORE 4 PCS



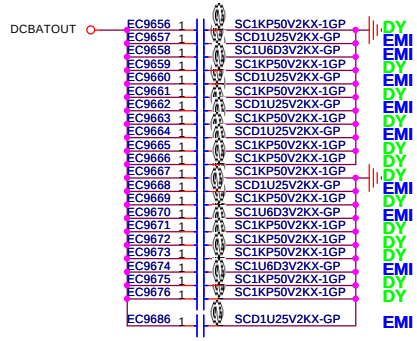
1D05V_S0 11 PCS

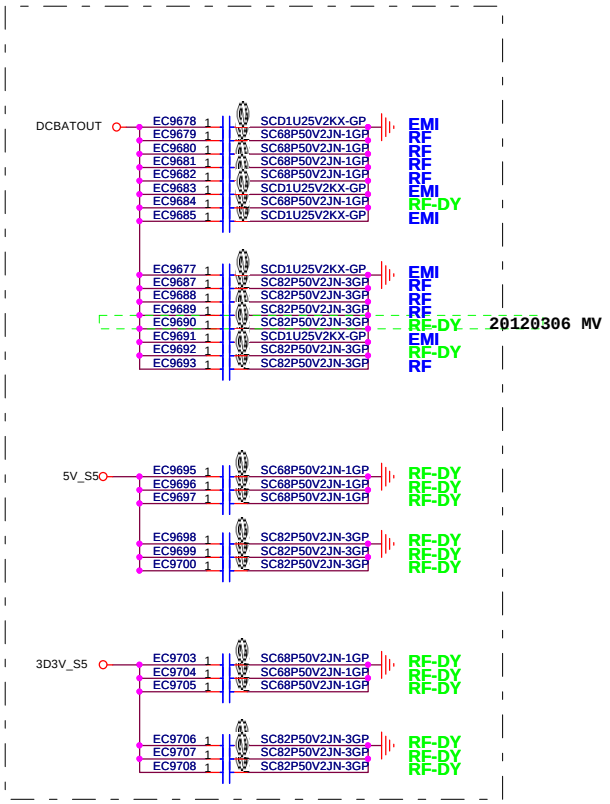


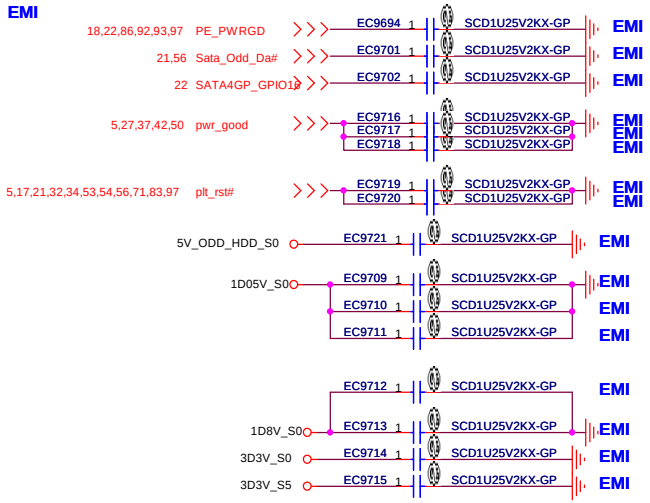
3D3V_S5 11 PCS



DCBATOUT 21 PCS







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PAGE 14_DIMM1 EMI CAP

5,14,15 DDR3_DRAMRST# — EC1428 — SC1KP50V2KX-1GP — DY

PAGE 15_DIMM1 EMI CAP

5,14,15 DDR3_DRAMRST# — EC1524 — SC1KP50V2KX-1GP — DY

PAGE 17_PCH(1/9)

17,29 HDA_BITCLK_CODEC — EC1701 — SC22P50V2JN-4GP — DY
17,29 HDA_SDOUT_CODEC — EC1702 — SC22P50V2JN-4GP — DY

PAGE 27_KBC

22,27 KBrst# — EC2701 — SC1KP50V2KX-1GP — DY
19,27 Pm_Pwrok — EC2702 — SC1KP50V2KX-1GP — DY
19,27,41 Rsmrst# — EC2703 — SC1KP50V2KX-1GP — DY

PAGE 29_AUDIO CODEC EMI CAP

17,29 HDA_RST#_CODEC — EC2901 — SC1KP50V2KX-1GP — DY

PAGE 31_AUDIO CONNECTOR EMI CAP

30,31 MIC_IN_R — EC3111 — SC100P50V2JN-1-GP — DY
30,31 MIC_IN_L — EC3112 — SC100P50V2JN-1-GP — DY
29,31 HP_OUT_L — EC3113 — SC100P50V2JN-1-GP — DY
29,31 HP_OUT_R — EC3114 — SC100P50V2JN-1-GP — DY — AUD_AGND

20120130PV-R

AVDD_CODEC — EC3115 — SC1U6D3V2KX-GP — AUD_AGND — DY
5V_S0 — EC3107 — SCD1U16V2ZY-2GP — DY

EC3108 — SC1KP50V2KX-1GP — DY
EC3109 — SC1KP50V2KX-1GP — DY
EC3110 — SC1KP50V2KX-1GP — DY — AUD_AGND

PAGE 32_Card Reader EMI CAP

32,33 MDIF5 — EC3201 — SC22P50V2JN-4GP — DY

CLOSE U3201 PIN1

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC3212 — SC100P50V2JN-L-GP — DY

Put Caps near DIMMA1 — 1D5V_S3 — EC1425 — EC1424 — SC68P50V2JN-1GP — RF-DY

Put Caps near DIMMA2 — 1D5V_S3 — EC1525 — EC1526 — SC68P50V2JN-1GP — RF-DY

3D3V_LAN_S5 — SCD1U10V2KX-5GP — EC3403 — EC3405 — EC3402 — SC82P50V2JN-3GP — SC56P50V2JN-2GP — RF-DY

34 LANXIN — EC3404 — SC56P50V2JN-2GP — RF-DY

DCBATOUT — EC4003 — EC4002 — EC4004 — EC4005 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY

DCBATOUT_3V — EC4101 — EC4102 — EC4103 — EC4104 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U25V2KX-GP — RF-DY / EMI

DCBATOUT_5V — EC4107 — EC4108 — EC4109 — EC4110 — SCD1U25V2KX-GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — EMI / RF-DY

PWR_VCCCORE1_DCBATOUT — EC4304 — EC4305 — EC4306 — EC4307 — SC68P50V2JN-1GP — SCD1U25V2KX-GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY / EMI

PAGE 33_SD/MS/MMC CONNECTOR EMI CAP

CLOSE CARD1

22,32 D3E_WAKE — EC3307 — SC1KP50V2KX-1GP — DY
32,33 MS_INS# — EC3308 — SC1KP50V2KX-1GP — DY
32,33 MDIF2 — EC3306 — SC22P50V2JN-4GP — DY
32,33 MDIF1 — EC3305 — SC22P50V2JN-4GP — DY
32,33 MDIF0 — EC3304 — SC22P50V2JN-4GP — DY
32,33 MDIF3 — EC3303 — SC22P50V2JN-4GP — DY

PAGE 34_Lan RTL8111E EMI CAP

CLOSE U3401 Pin25

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC3401 — SCD1U25V2KX-GP — EMI

PAGE 35_LAN RJ45 EMI CAP

34,35 GREEN_LED# — EC3502 — SCD1U16V2ZY-2GP — DY
34,35 YELLOW_LED# — EC3501 — SCD1U16V2ZY-2GP — DY

PAGE 39_BATT CONN EMI CAP

27,39 AB1A_DATA — EC3901 — SC22P50V2JN-4GP — DY
27,39 AB1A_CLK — EC3902 — SC22P50V2JN-4GP — DY
27,39 MAIN_BAT_DET# — EC3903 — SC1KP50V2KX-1GP — DY
39 MAIN_BAT_DET#_C — EC3904 — SC1KP50V2KX-1GP — DY

PAGE 49_LVDS EMI CAP

20,49 LCDVDD_EN — EC4911 — SC1KP50V2KX-1GP — DY
49 DISP_OFF# — EC4912 — SC1KP50V2KX-1GP — DY
27,49,82 LID_SW# — EC4913 — SC1KP50V2KX-1GP — DY
20,49 LCD_BL_EN — EC4914 — SC1KP50V2KX-1GP — DY
EC4904 — SC33P50V2JN-3GP — DY
29,49 DMIC_DATA — EC4905 — SC33P50V2JN-3GP — DY
29,49 DMIC_CLK

PUT CLOSE R4911

DCBATOUT — EC4915 — SCD1U50V3KX-GP — DY
+LCDVDD — EC4916 — SCD1U16V2ZY-2GP — DY
3D3V_S0 — EC4903 — SC1U6D3V2KX-GP — DY
EC4902 — SC1U6D3V2KX-GP — DY
EC4901 — SC1U6D3V2KX-GP — DY

PWR_VCCCORE2_DCBATOUT — EC4312 — EC4308 — EC4309 — EC4310 — SC68P50V2JN-1GP — SCD1U25V2KX-GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY / EMI

PWR_GFXCORE1_DCBATOUT — EC4403 — EC4404 — EC4405 — EC4406 — SC68P50V2JN-1GP — SCD1U25V2KX-GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY / EMI

DCBATOUT_RT8209B_VCCP — EC4503 — EC4504 — EC4505 — EC4506 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U25V2KX-GP — RF / RE

DCBATOUT_1D5V — EC4603 — EC4604 — EC4605 — EC4606 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SCD1U25V2KX-GP — RF-DY / EMI

+LCDVDD — EC4909 — EC4908 — SC68P50V2JN-1GP — SC1KP50V2KX-1GP — RF-DY

3D3V_WLAN — EC5304 — EC5305 — EC5306 — EC5307 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY

1D5V_S0 — EC5309 — EC5310 — EC5311 — EC5308 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY

3D3V_WWAN — EC5405 — EC5406 — EC5407 — EC5408 — SC68P50V2JN-1GP — SC82P50V2JN-3GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY

DCBATOUT — EC9203 — EC9204 — EC9205 — EC9206 — SC68P50V2JN-1GP — SCD1U25V2KX-GP — SC2200P50V2KX-2GP — SCD1U50V3KX-GP — RF-DY / EMI

40 DC_IN_R — AD+_IN_G — EC4007 — EC4008 — SC1U25V3KX-1-GP — SC1U25V3KX-1-GP — EMI

PAGE 50_CRT EMI CAP

5V_S0 — EC5011 — SCD1U50V3KX-GP — DY

PAGE 51_HDMI EMI CAP

20,51 HDMI_PCH_DET — EC5101 — SC1KP50V2KX-1GP — DY

PAGE 53_WLAN SLOT EMI CAP

5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — EC5303 — EC5301 — EC5302 — SC100P50V2JN-L-GP — SC1KP50V2KX-1GP — DY
53 XMIT_OFF_R — SC1KP50V2KX-1GP — DY
22,53 BT_OFF# — SC1KP50V2KX-1GP — DY

PAGE 54_WLAN SLOT EMI CAP

CLOSE WWAN1

22,54 GPS_XMIT_OFF# — EC5401 — EC5402 — EC5403 — EC5404 — SC1KP50V2KX-1GP — SC1KP50V2KX-1GP — SC1KP50V2KX-1GP — SC100P50V2JN-L-GP — DY
17,54 INTRUDER# — DY
54 WIFI_RF_EN# — DY
5,17,21,32,34,53,54,56,71,83,96 PLT_RST# — DY

PAGE 56_HDD/ODD EMI CAP

5V_S0 — EC5601 — EC5615 — EC5613 — EC5614 — SC1U10V3ZY-6GP — SC1KP50V2KX-1GP — SC1KP50V2KX-1GP — SC1KP50V2KX-1GP — DY
22,56 SATA_ODD_PWR_EN
56 SATA_ODD_DET#_C
56 SATA_ODD_DA#_C

PAGE 61_USB2.0 EMI CAP

CLOSE USB21

USB_VCCA — EC6102 — SCD1U16V2ZY-2GP — DY

PAGE 62_USB3.0 EMI CAP

USB_VCCA — EC6202 — SC1U10V3ZY-6GP — DY
USB_VCCB — EC6201 — EC6203 — SC1U10V3ZY-6GP — DY

PAGE 64_FINGER PRINT EMI CAP

22,64 FPR_LOCK# — EC6404 — EC6405 — SC1KP50V2KX-1GP — DY
18,64 FPR_OFF

PAGE 82_DCIN EMI CAP

38,82 LIMIT_SIGNAL — EC8206 — SC1KP50V2KX-1GP — EMI
82 DC_PIN1 — EC8209 — SC1U25V3KX-1-GP — EMI
82 DC_PIN2 — EC8210 — SC1U25V3KX-1-GP — EMI
27,82 QUICKX_LED# — EC8212 — SC1KP50V2KX-1GP — EMI
19,82 ON_OFF# — EC8213 — SC1KP50V2KX-1GP — EMI
27,49,82 LID_SW# — EC8214 — SC1KP50V2KX-1GP — EMI
68,82 WL_LED#_ALL — EC8215 — SCD1U16V2ZY-2GP — DY

AD+ — EC8202 — EC8201 — SC1U25V3KX-1-GP — DY / EMI

CLOSE PWR1

27,69,82 KSI1 — EC8216 — SC1KP50V2KX-1GP — EMI
27,69,82 KSI3 — EC8217 — SC1KP50V2KX-1GP — EMI
27,82 KSO17 — EC8218 — SC1KP50V2KX-1GP — EMI

3D3V_S0 — EC8207 — EC8211 — SC1KP50V2KX-1GP — SCD1U25V2KX-GP — EMI
3D3V_AUX_S5 — EC8205 — EC8208 — SC1KP50V2KX-1GP — SCD1U25V2KX-GP — EMI

PAGE 40-48,92_POWER EMI CAP

CLOSE TO PU4005 — DCBATOUT — EC4001 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4301 — DCBATOUT — EC4301 — SCD1U50V3KX-GP — DY
CLOSE TO PU4303 — DCBATOUT — EC4303 — SCD1U50V3KX-GP — DY
CLOSE TO PU4401 — DCBATOUT — EC4401 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4501 — DCBATOUT — EC4501 — SCD1U50V3KX-GP — DY
CLOSE TO PU4601 — DCBATOUT — EC4601 — SCD1U50V3KX-GP — DY
CLOSE TO PU4701 — DCBATOUT — EC4701 — SCD1U25V2KX-GP — EMI
CLOSE TO PU4801 — DCBATOUT — EC4801 — SCD1U25V2KX-GP — EMI
CLOSE TO PU9202 — DCBATOUT — EC9201 — SCD1U50V3KX-GP — DY

PAGE 62_USB3.0 CAP

CLOSE USB31 — USB_VCCA — EC6215 — SCD1U16V2ZY-2GP — DY
CLOSE USB32 — USB_VCCB — EC6214 — SCD1U16V2ZY-2GP — DY
CLOSE USB33 — USB_VCCB — EC6213 — SCD1U16V2ZY-2GP — DY
CLOSE U6204

19,46,62 PM_SLP_S4# — EC6212 — SC1KP50V2KX-1GP — DY

CLOSE U6205

19,46,62 PM_SLP_S4# — EC6211 — SC1KP50V2KX-1GP — DY

21,27 CLK_PCI_KBC — EC2101 — EC2102 — SC12P50V2JN-3GP — RF-DY
21,71 CLK_PCI_DEBUG — RF-DY

EC2904/EC2903 CLOSE U2901

29 DMIC_CLK_R — EC2904 — SC220P50V2KX-3GP — EMI
29 DMIC_DATA_R — EC2903 — SC220P50V2KX-3GP — EMI

18,22,86,92,93,96 PE_PWRGD

EC9207 — SC4750V2JN-3GP — EMI
EC9208 — SC4750V2JN-3GP — EMI

WLAN & WWAN

H1 ~ H16 --> ZZ.00PAD.D11
H17 ~ H22 --> ZZ.00PAD.N11
H23 ~ H26 --> 34.4Y824.001
H27 ~ H28 --> 34.4Q602.101

WWAN WWAN PCH

H23 H24 H25 H26 H27 H28
STF256R169H05-GP — STF256R169H05-GP — STF256R169H05-GP — STF256R169H05-GP — STF256R169H03-GP — STF256R169H03-GP
34.4KD36.001 34.4KD36.001 34.4KD36.001 34.4KD36.001

H19 H20 H11 H12
HOLE276R178-GP — HOLE276R178-GP — HOLE256R115-GP — HOLE256R115-GP
ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.D11 ZZ.00PAD.D11

H30 H31 H1 H2 H3 H4
HOLE276R178-GP — HOLE256R115-GP — HOLE256R115-GP — HOLE256R115-GP — HOLE256R115-GP — HOLE256R115-GP
ZZ.00PAD.N11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11 ZZ.00PAD.D11

H29 H17 H15 H16 H5 H8
HOLE276R178-GP — HOLE276R178-GP — HOLE276R178-GP — HOLE276R178-GP — HOLE256R115-GP — HOLE256R115-GP
ZZ.00PAD.D11 ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.N11 ZZ.00PAD.D11 ZZ.00PAD.D11

PAGE 69_KEYBOARD/TOUCH PAD EMI CAP

20120112 PV-R

SRC1KP50VM-GP EC6904 — KSI3 KSO5 KSO1 KSI0 — EMI
SRC1KP50VM-GP EC6903 — KSO2 KSO3 KSO7 KSO8 — EMI
SRC1KP50VM-GP EC6906 — KSO6 KSO3 KSO12 KSO13 — EMI
SRC1KP50VM-GP EC6905 — KSO14 KSO11 KSO10 KSO15 — EMI
SRC1KP50VM-GP EC6901 — KSI1 KSI7 KSI6 KSO9 — EMI
SRC1KP50VM-GP EC6902 — KSI4 KSI5 KSO0 KSI2 — EMI

KSI[0..7] 27,69,82
KSO[0..15] 27,69

27,69 KB_CAPS_LED — EC6907 — SC100P50V2JN-1-GP — DY

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
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Title: Change History

Size	Document Number	Rev
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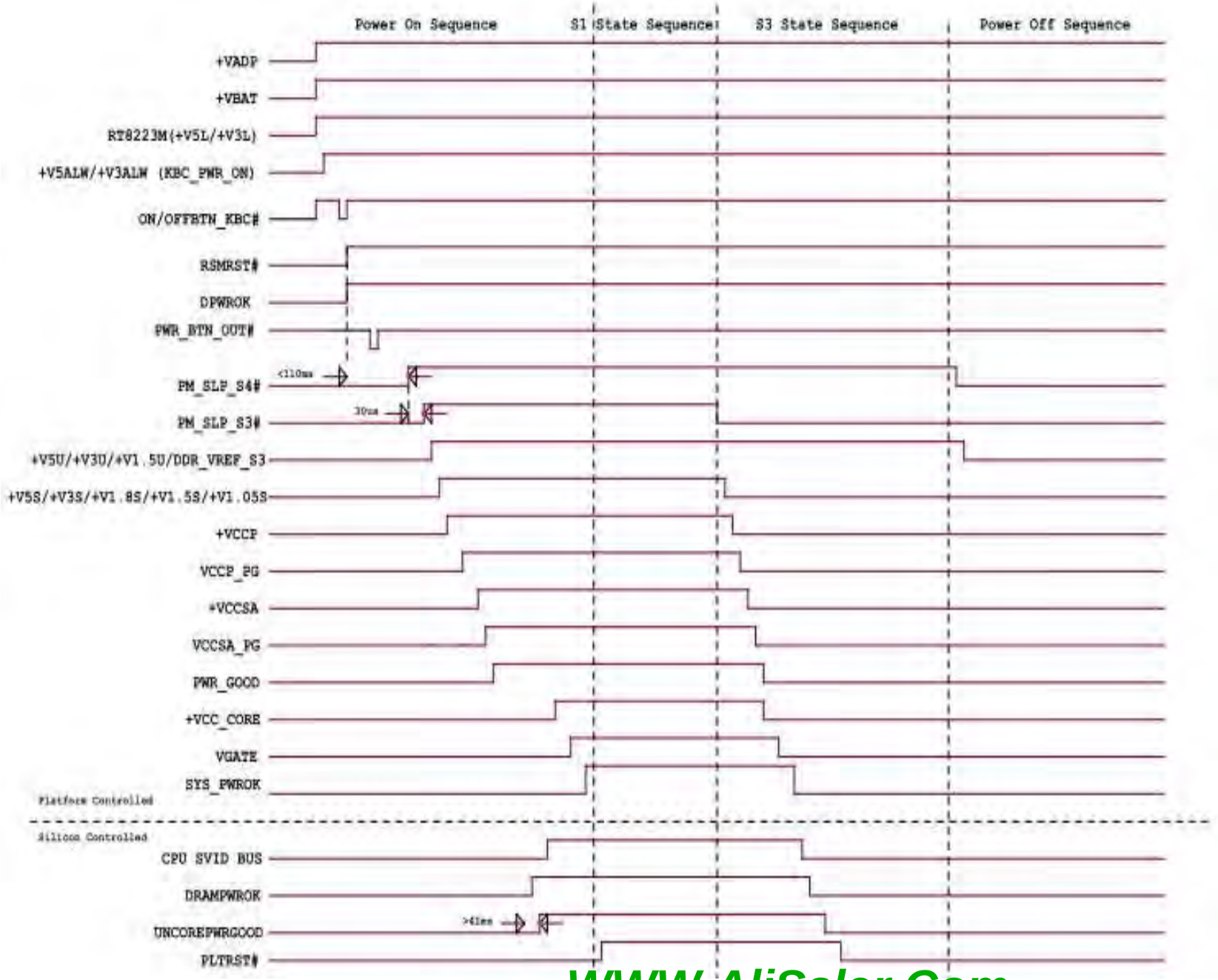
S-Series Power Sequence and Reset Signal Timing



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Title: ***Power Sequence***

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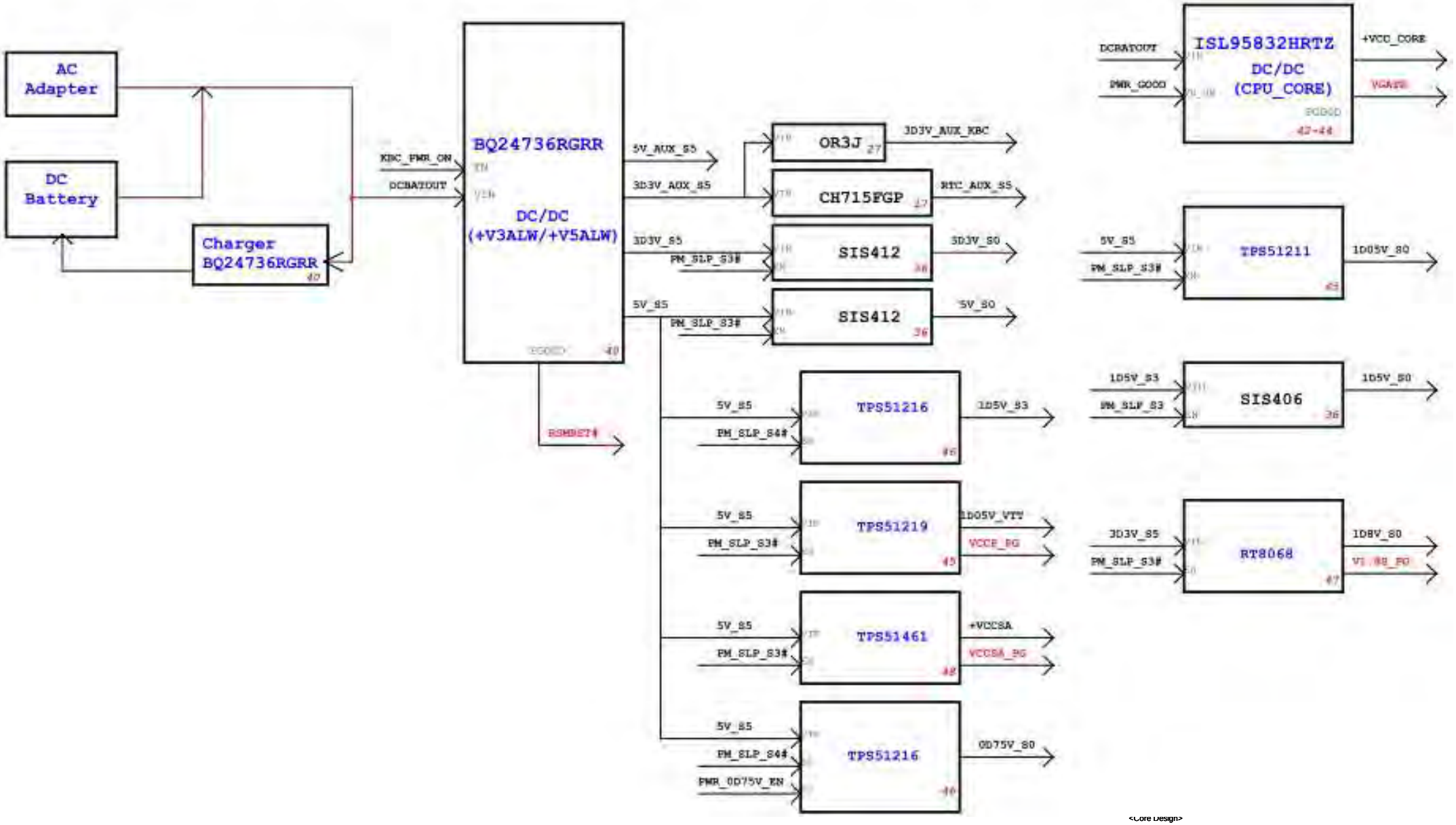
S-Series POWER BLOCK DIAGRAM



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Title: *Power Block Diagram*		
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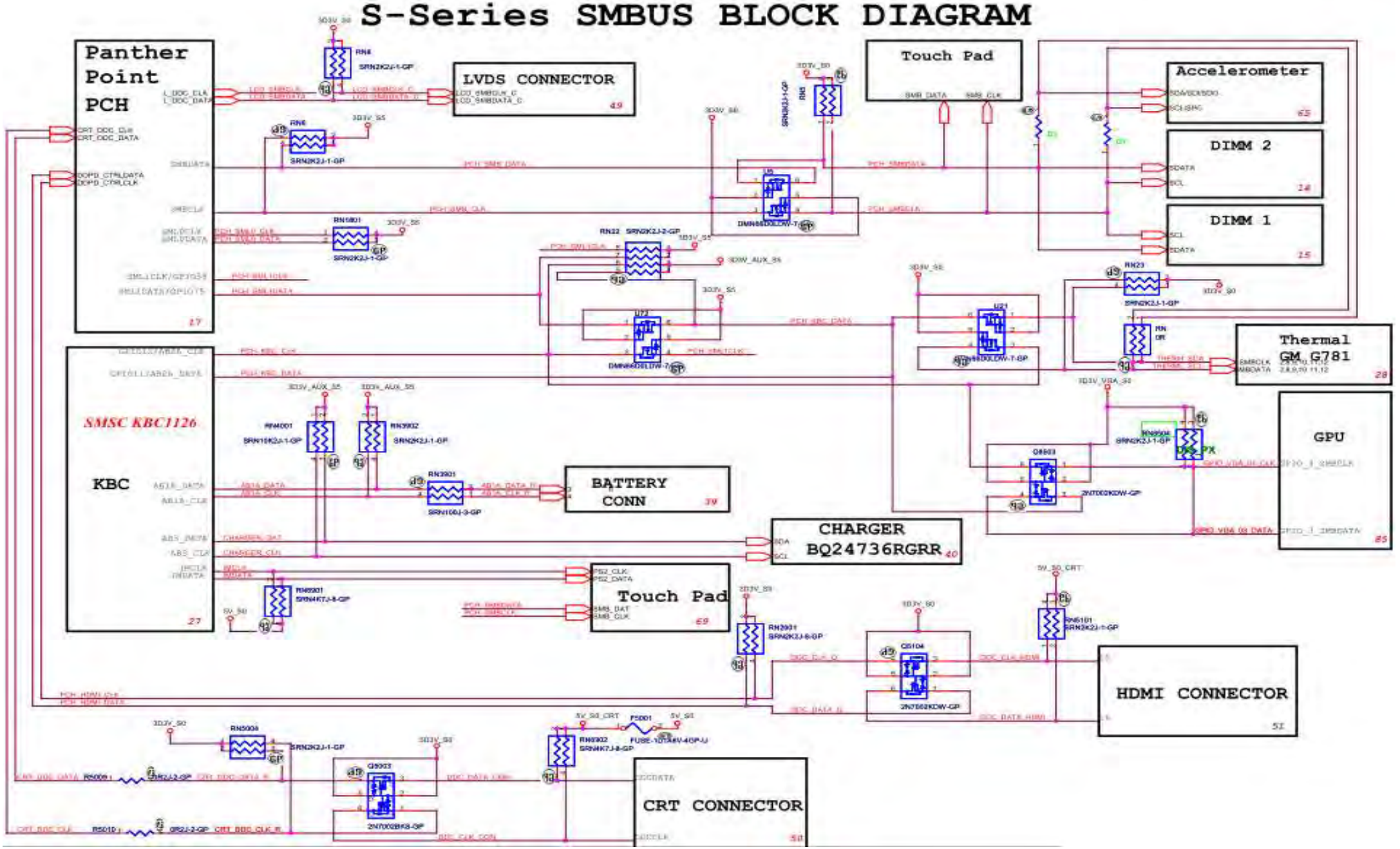
S-Series SMBUS BLOCK DIAGRAM



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Title: ***SMBUS Block Diagram***

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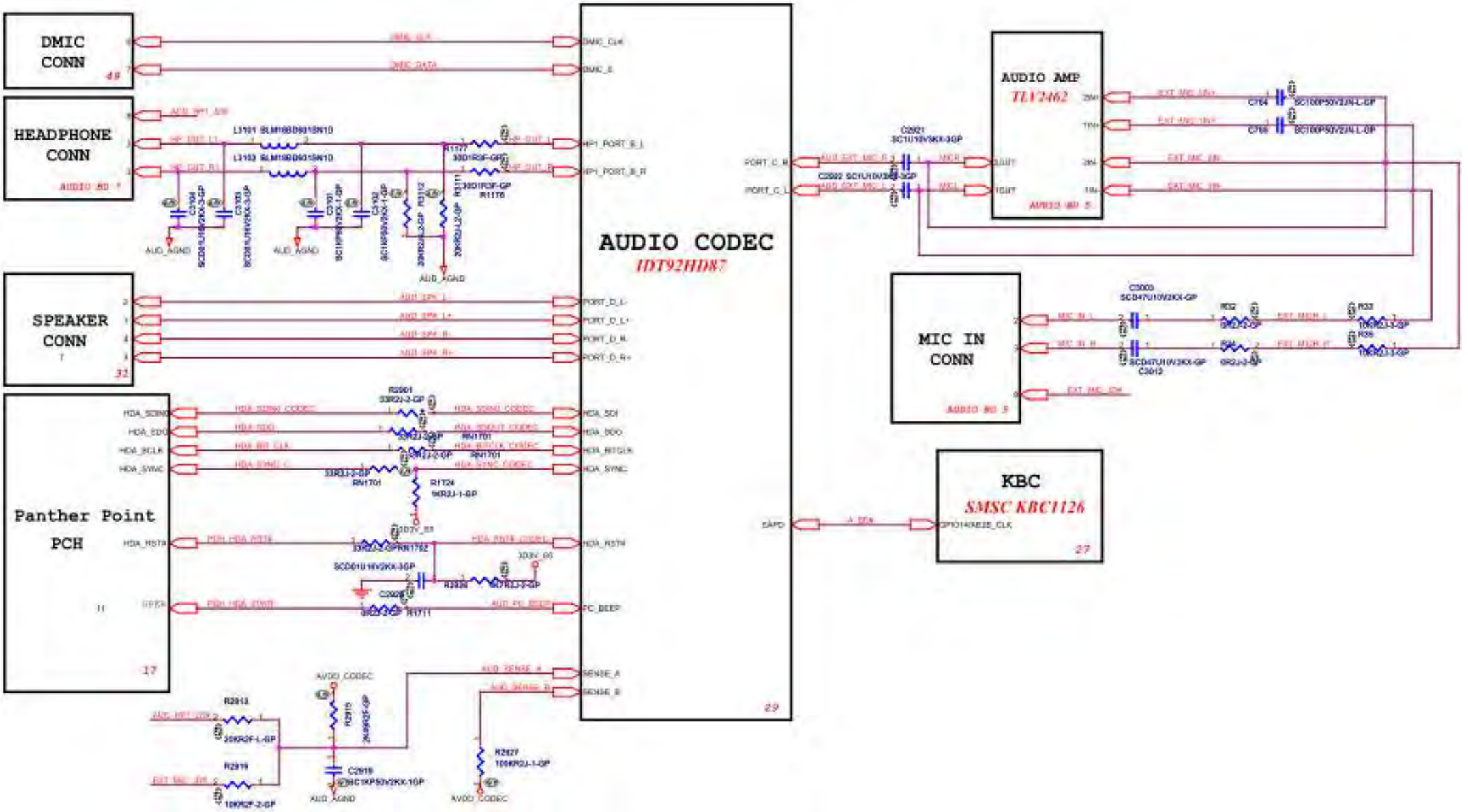
S-Series AUDIO BLOCK DIAGRAM



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Title: Thermal/Audio Block Diagram

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Title: mSATA

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