Compal Confidential

Intel MB Schematic Document

2019 OMEN 17.3" Santorini

FPC72 LA-H492PR01

Date : 2018/09/28

Version: v0.1

15.6": FPC54 LA-H481PR(N17)
LA-H482P(N18)
17" : FPC72 LA-H491P(N17)
FPC72 LA-H492P(N18)

15" to 17" different:
01. Add SSD#2
02. Combo HP Jack to separated MIC jack
03. JDIMM2 to STD. revision.
04. Screw Location
05. BATT from SMT to DIP
06. ACIN CONN
07. GPU Core from 6phase to 4phase

(Modified&Ref from: 01."DPF50_LA-F842PR1A_201800411(PPAV)")
02.GPU:"DPF50_LA-F863PR01_180723(PPAV)")
03.GPU reference:"EH78F_LA-G161PR01_0810")

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Title: Cover Page		
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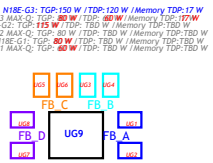
Model Name : OMEN N18E-G3

File Name :



UG108 OVR-M NCP45491XMNTWG P.22

UG2,UG1 8Gb_256Mx2Chx16 :2pcs P.35 — FBA x64

UG4,UG3 8Gb_256Mx2Chx16 :2pcs P.35 — FBB x64

UG6,UG5 8Gb_256Mx2Chx16 :2pcs P.36 — FBC x64

UG8,UG7 8Gb_256Mx2Chx16 :2pcs P.36 — FBD x64

UG9 GPU nVidia N18E-G3 256bits Two Channelsx16 (single sided) 37.5mm x 37.5mm P.27-34 *GB4B-256

PEG x16 P.9

UC1 Intel Coffee Lake- H 6C+GT2 P.7 P.8 P.9 P.6~13
TDP: 45W
42mm x 28mm
BGA 1440-Pin
14nm
0.65mm Ball Pitch
1 Die 6+2:16.5x9.1mm 8+2:19.4x9.1mm

DDR4_1.2V Interleaved (*1DPC)

AREA BACK
Ch0 (REV.) DDR4 SO-DIMM JDIMM1 P.23
Ch1 (STD.) DDR4 SO-DIMM JDIMM2 P.24
AREA FRONT
*(17" Ch1:JDIMM2 is REV. type)

JHDMI1 HDMI Conn. P.40 — UV3 HDMI Redriver PS8409 P.40 — HDMI 2.0 — IFPC

JmDP1 Mini_DP Conn. P.39 — UV43 DP Repeter TUSB546 P.40 — DP 1.4 — IFPA

JEDP1 eDP Conn. P.38 — eDP — IFPD

x4 DMI 3.0 P.16

UH1 HM370 Cannon Lake PCH-H 24mm x 25mm BGA 874-Pin 0.5mm Ball Pitch P.14~21

JTAG1 Debug

GPU IFPE — UT11 DP Repeter TUSB546 P.47 — U1 Thunderbolt Titan Ridge JHL7340 P.48 — JUSBC1 USB Type-C P.50

PCIex4, Port #17/18/19/20

Port #4 — UU4 Type-C PD TPS65987S P.50 — UU5 SPI ROM W25X20CLSNIG P.50

JRJ45 RJ-45 P.51 — UL1 GLAN RTL8118AS P.51 — x1, Port #14 — PCIe P.14 P.17

JUSB1 USB3.0 Conn.

JIO1 I/O Conn. P.71

UR1 Card Reader RTS5237S-GRT — x1, Port #15

HDD LED

US1 USB Charger TPS2546 P.71 — USB 2.0 Port #1

USB 3.0 Port #1

x1, Port #15

JWLAN1 WLAN+BT (M.2 Key E) P.52 — CNVi — USB 2.0 Port #14 — x1, Port #16

JSSD1 SSD#1 (M.2 Key M) P.67 — x4, Port #12/11/10/9 (SATA#1A)

JSSD2 SSD#2 (M.2 Key M) P.68 — *for 17" only — x4, Port #21/22/23/24 (SATA#4)

USB 3.0 P.17 — Port #2 — JUSB2 USB3.0 Conn. P.71

Port #3 — JUSB3 USB3.0 Conn. P.71

USB 2.0 P.14 — Port #5 — JEDP1 HD/IR Camera P.38

PJP1 ACIN Conn. P.82

JPWR1 PWR BTN Conn.

JKBL1 KBL Conn. P.63

PUB01 Charger P.84

PJPB1 Battery Conn. P.83

U9 G-Sensor HP2DCTR P.66

JHDD1 2.5" HDD P.67 — SATA Port #0b P.17

UK1 EC ENE KB9542Q-B P.58 — SMBus#1 — SMBus#2 — LPC P.17 — ESB — PS2#3 — SMBus P.18

JTP1 Touch Pad P.63

UG9 GPU P.25

JKB1 Int. KBD P.63

JFAN1 JFAN2 FAN P.77

U7 Hall Sensor P.63

UC3 Thermal Sensor P.66

SPI P.16

UT1 TPM 2.0 SLB9670VQ2.0 P.66

UH2 BIOS 16MB W25Q128JVSIQ P.16

HDA P.18 — UA1 Codec AL3292 P.56 — JHP1 Combo Jack P.56

JMIC1 *for 17" only — Stereo Mic Jack P.56

I2S — UAA1 ALC1305 P.57 — JSPK1 Speaker Conn. P.57

JLB1 RGB Conn. P62

UE1 RGB LED Driver TLC59116 P62

UK2 Extend I/O KC3810 P.59

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Title: Block Diagrams

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"OMEN17_BLOCK_DIAGRAM0817"

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
1 --> 0.2	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
2 --> 0.3	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
3 --> 0.4	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
4 --> 0.5					
5 --> 0.6					
6 --> 0.7					
7 --> 0.8					
8 --> 0.9					
9 --> 1.0					
10 --> 1.1					
11 --> 1.2					
12 --> 1.3					
13 --> 1.4					
14 --> 1.5					
15 --> 1.6					
16 --> 1.7					
17 --> 1.8					
18 --> 1.9					
19 --> 2.0					

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	---		
DDI2	---		
DDI3	---		
eDP	---		PCH_EDP_HPD_R

Power State

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM2	0X52	0XA4	0XA5
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x4F	0X9E	0X9F

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1	+3V_SMBUS	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
SMBUS Port2	+3VL	PCH	TBC		
		GPU	0x4F	0X9E	0X9F
		THERMAL	0x48	0X90	0x91
		PD (Default)	0x38	0X70	0x71
		Type-C MUX	0x10 0x11	0X20 0X22	0x21 0x23

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3V_PCH_PRIM				
I2C_1_SCL I2C_1_SDA	+3VS				

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
UMA	UMA@	
DIS	DIS@	
eSPI I/F	ESPI@	LPC@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	EMI@ VGAEMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1 Gen1/Gen2	1			USB3.1 Port 1		
1	USB3.1_2 Gen1/Gen2	2			USB3.1 Port 2		
2	USB3.1_3 Gen1/Gen2	3			USB3.1 Port 3		
3	USB3.1_4 Gen1/Gen2	4			USB Type-C Port		TBT
4	USB3.1_5 Gen1	5					
5	USB3.1_6 Gen1	6					
6	USB3.1_7 Gen1	7					
7	USB3.1_8 Gen1	8					
8	HM370 disable						
9	HM370 disable						
10	/ GbE						
11	HM370 disable						
12	HM370 disable						
13	HM370 disable						
14	PCIE_9 / GbE		9				
15	PCIE_10		10				
16	PCIE_11 / SATA_0A		11	0	SSD-1	CLK2 & CLKREQ#2	
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0	HDD		
19	PCIE_14 / SATA_1B		14	1	Ethernet	CLK5 & CLKREQ#5	
20	PCIE_15		15		Card Reader	CLK3 & CLKREQ#3	
21	PCIE_16		16		WLAN	CLK1 & CLKREQ#1	
22	PCIE_17 / SATA_4		17	4			
23	PCIE_18 / SATA_5		18	5	Thunderbolt	CLK0 & CLKREQ#0	
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21				
27	PCIE_22		22				
28	PCIE_23		23		SSD-2 or Optane	CLK6 & CLKREQ#6	
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 Port 1
2	USB3.1 Port 2
3	USB3.1 Port 3
4	USB3.1 Type-C Port
5	
6	Camera/IR Camera
7	
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

GPU IFPx Table

Port	Function
A	mDP
B	--
C	HDMI 2.0
D	eDP
E	DP source to TBT
F	--

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Option Table

BOM Number	Load BOM Option
431AAN32L01	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNCT@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@
431AAN32L02	3G@/XDP@/N17E_G1@/MP@/LPC@/DIS@/CNVI@/QNVH@/PCH@/DAX@/EMI@/ESD@/S3G@/H3G@

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Title: Notes List

Size: Custom | Document Number: FPC72 LA-H492P | Rev: v0.1

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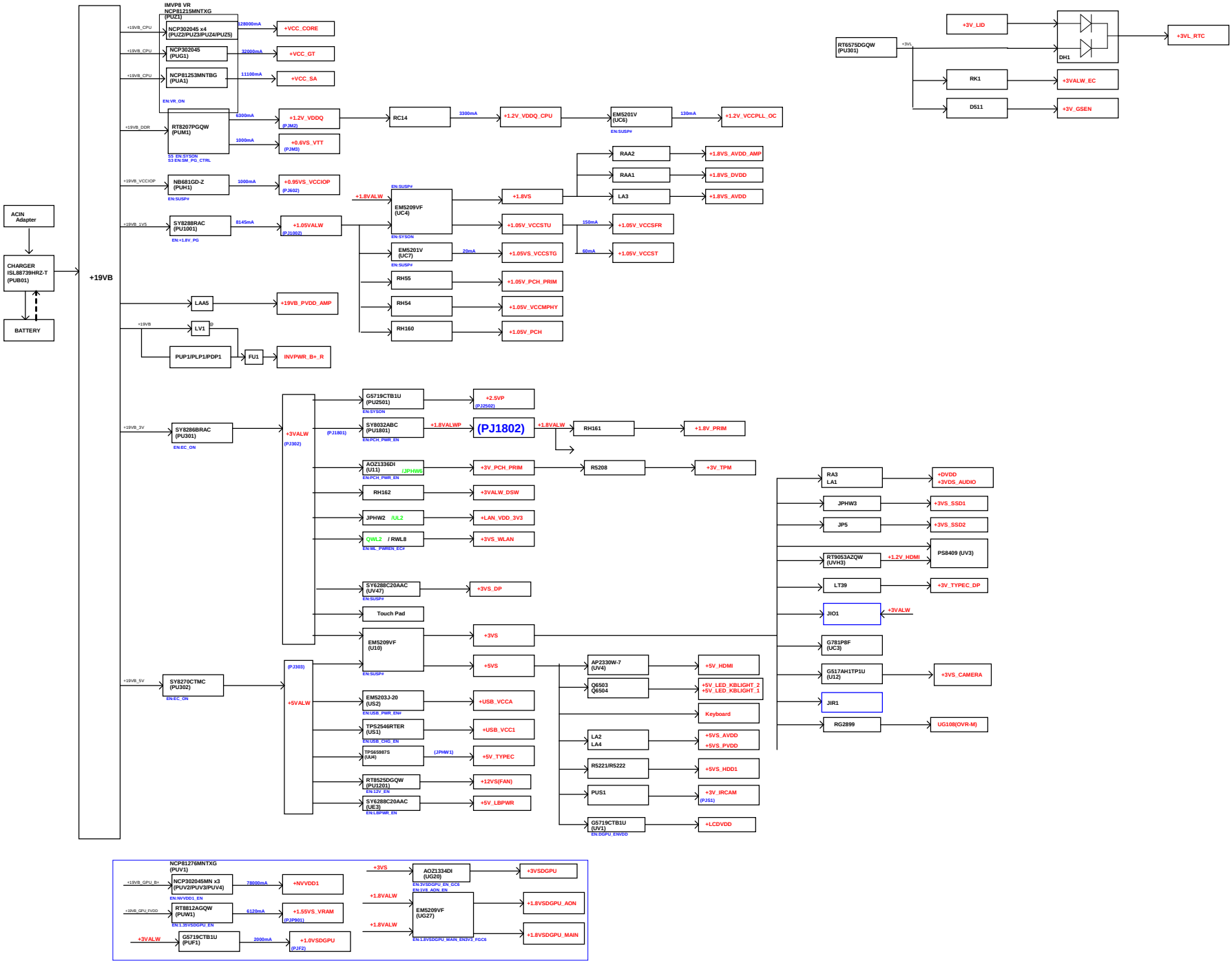

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Issued Date	2017/07/24	Deciphered Date	2018/08/24
Title	Power Map		
Size	Document Number		Rev
Custom	PPC54 LA-H482P		v0.1
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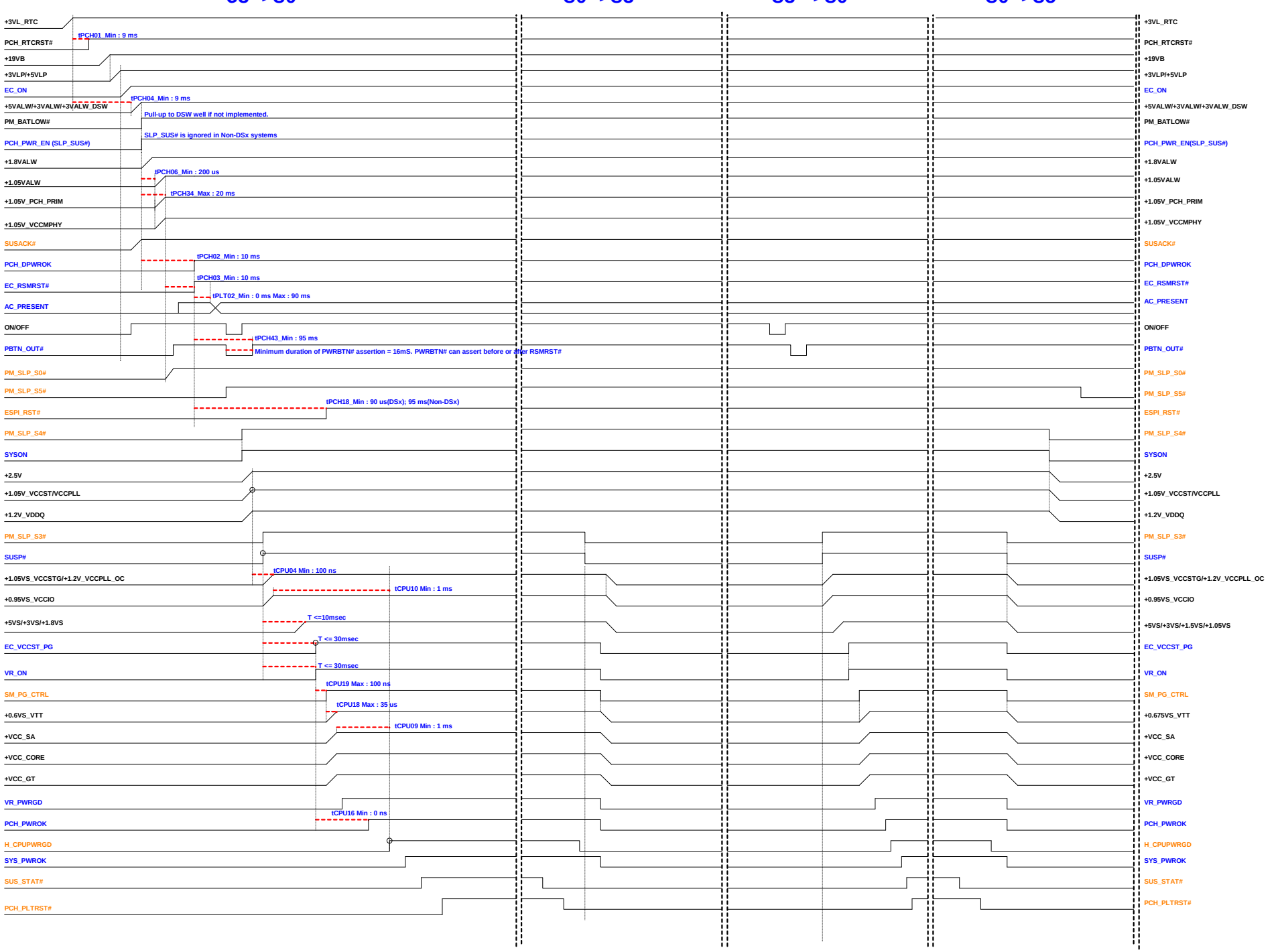
[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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Compal Electronics, Inc.

Title: Power Sequence

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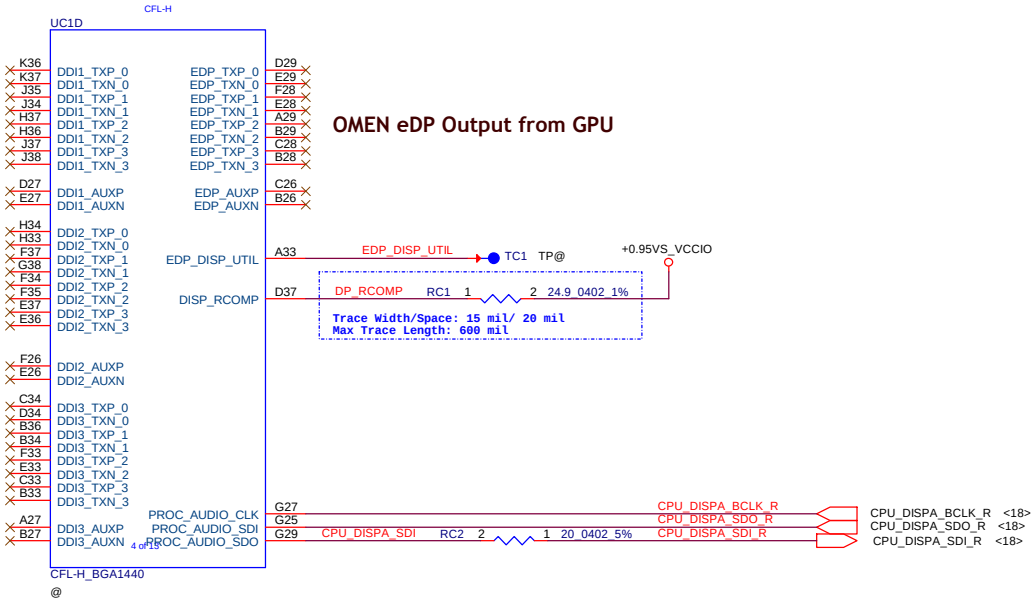
OMEN: TR DDI input from GPU for DP v1.4

OMEN eDP Output from GPU



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Title: CFL-H(1/8)DDI/eDP

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

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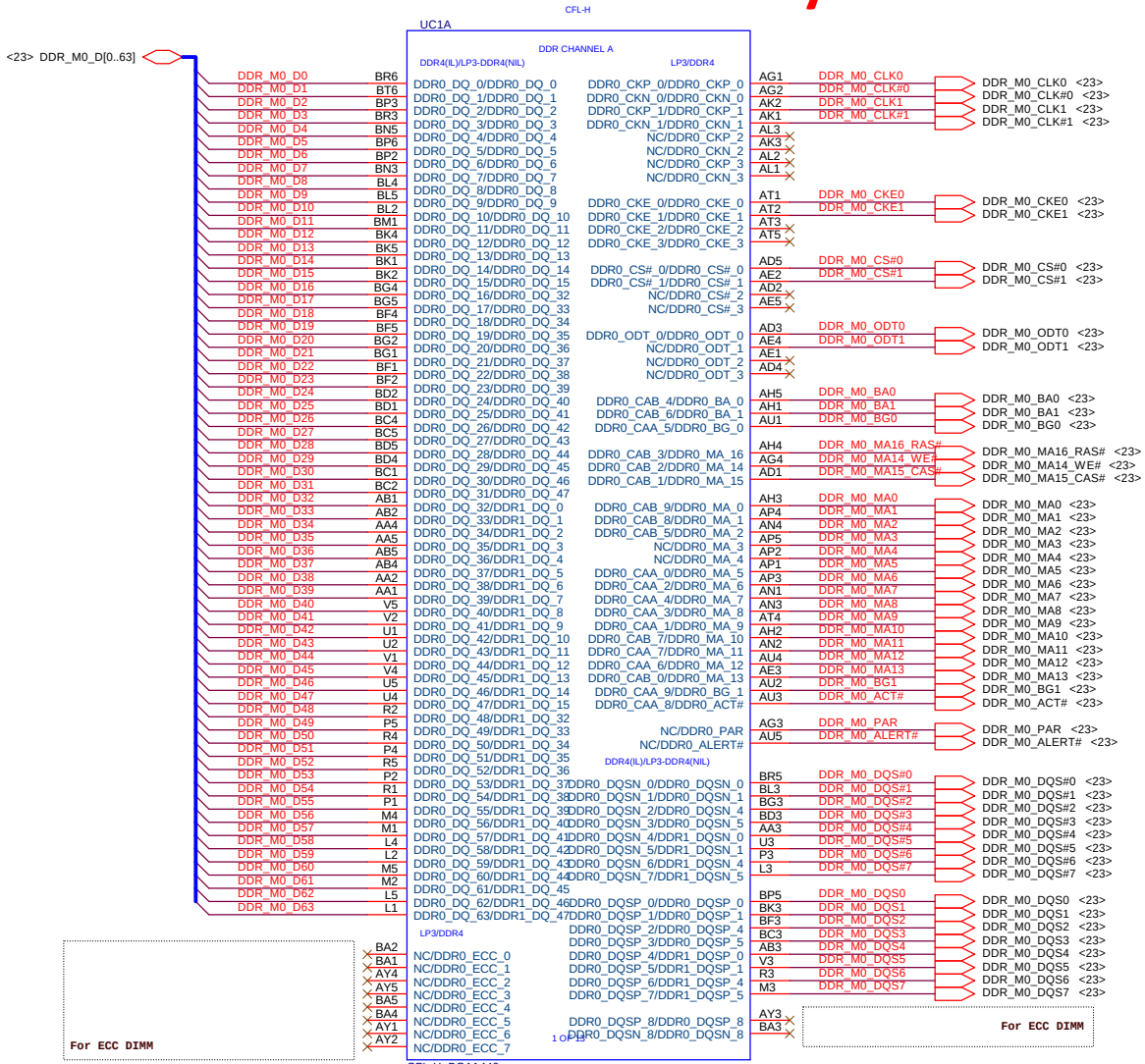
CHANNEL - A

Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title: CFL-H(2/8)DIMMA			
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
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CHANNEL - B

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title	CFL-H(3/8)DIMMB		
Size	Document Number		Rev
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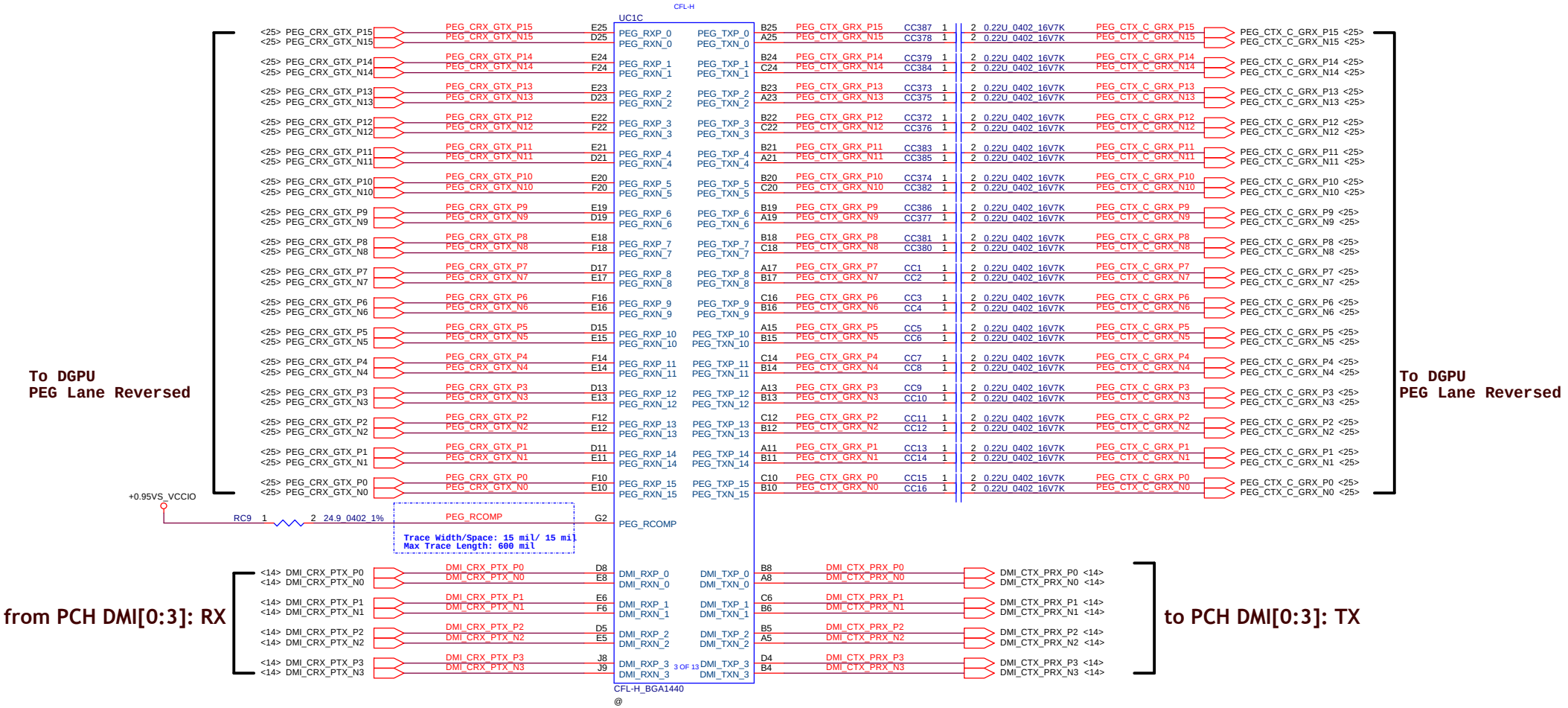

Security Classification	Compal Secret Data		
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Title: CFL-H(4/8)PEG

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

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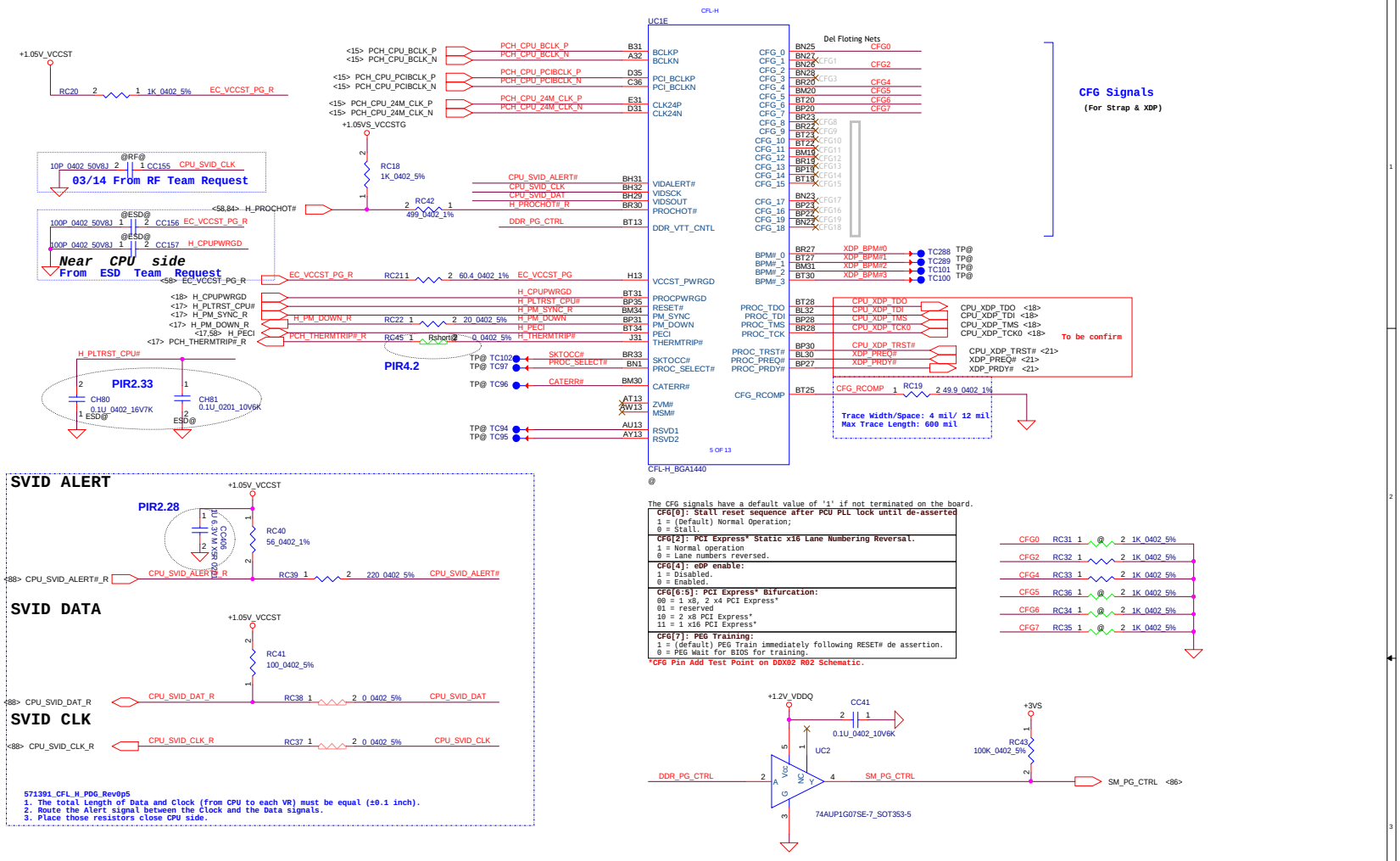
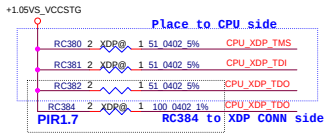
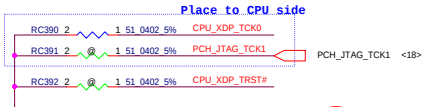


The CFG signals have a default value of '1' if not terminated on the board.

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted 1 = (Default) Normal Operation; 0 = Stall.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.
CFG[4]: eDP enable: 1 = Disabled. 0 = Enabled.
CFG[6:5]: PCI Express* Bifurcation: 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
CFG[7]: PEG Training: 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.

*CFG Pin Add Test Point on DDX02 R02 Schematic.





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Issued Date	2017/07/24	Deciphered Date 2018/08/24	Title CFL-H(5/8)CFG,SVID
Size Custom	Document Number FPC54 LA-H482P		Rev v0.1
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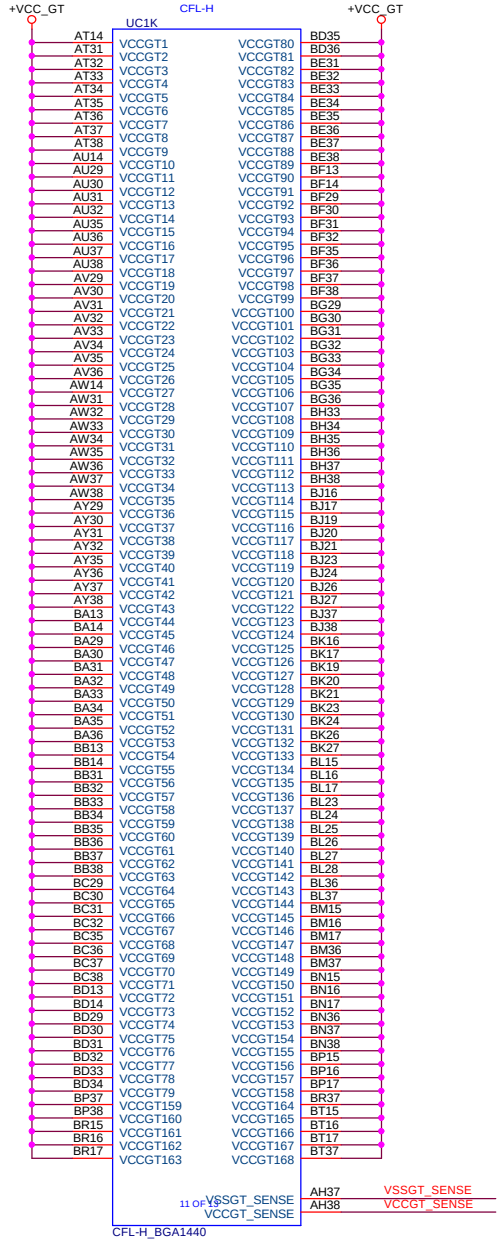
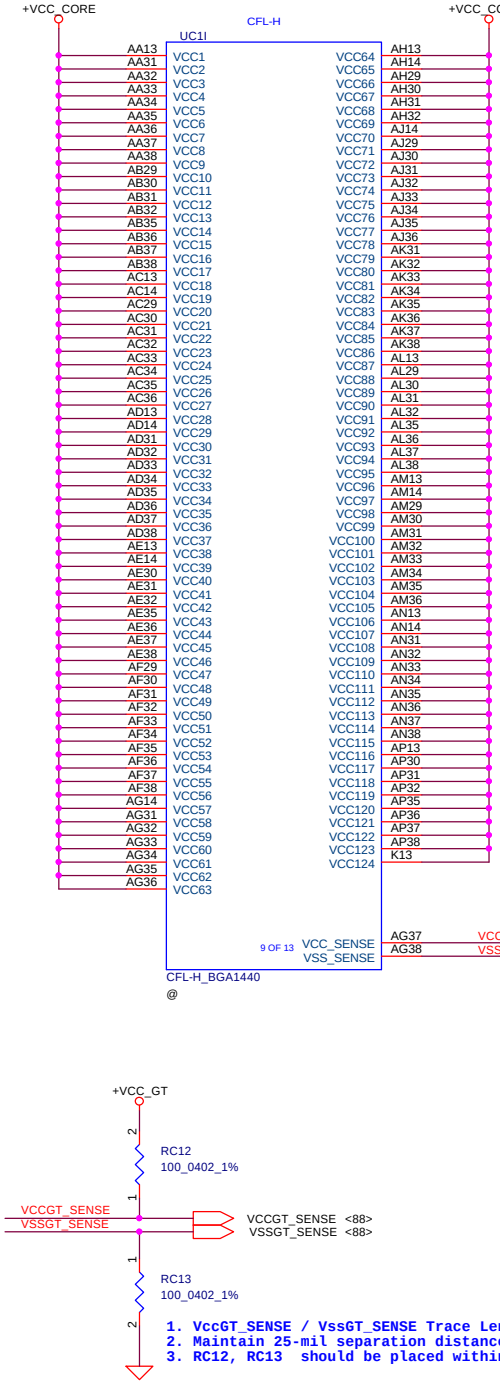
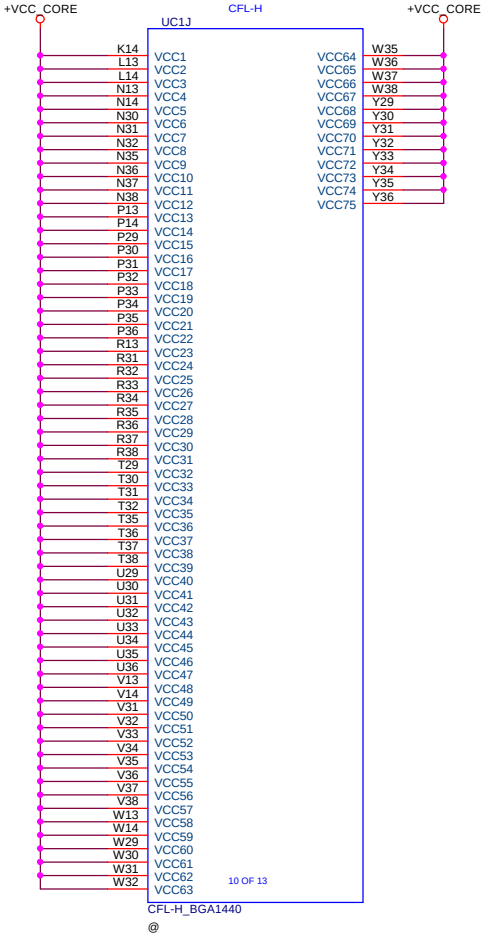
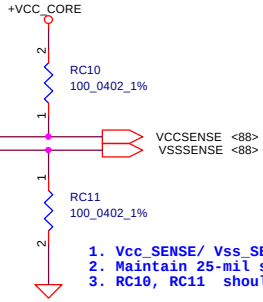
GT
55000mA(Hexa Core GT2)





96000mA(Hexa Core GT2)





1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

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Compal Electronics, Inc.

Title: CFL-H(6/8)VCC CORE/GT

Size	Document Number	Rev
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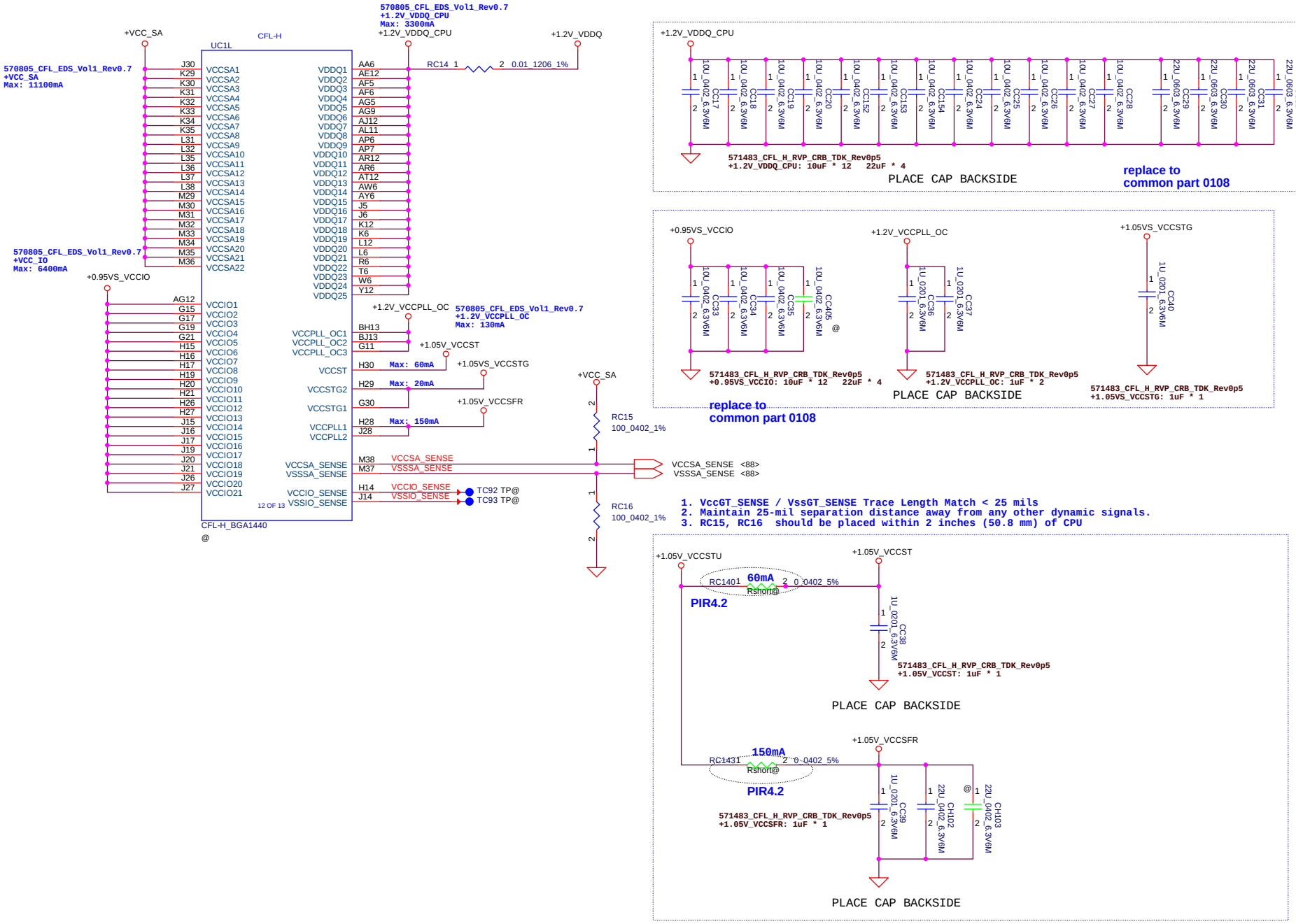

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Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

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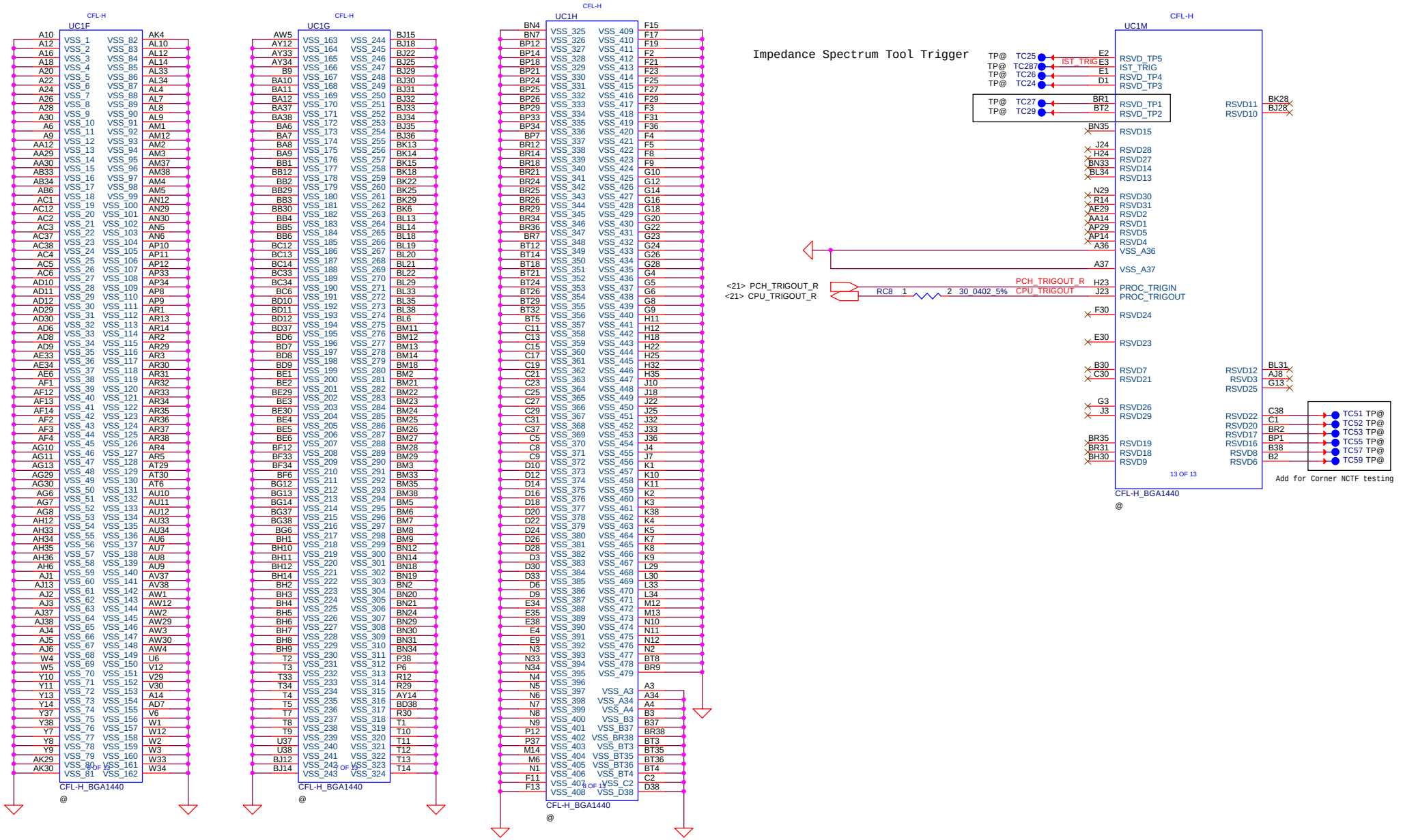

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Issued Date	2017/07/24	Deciphered Date	2018/08/24

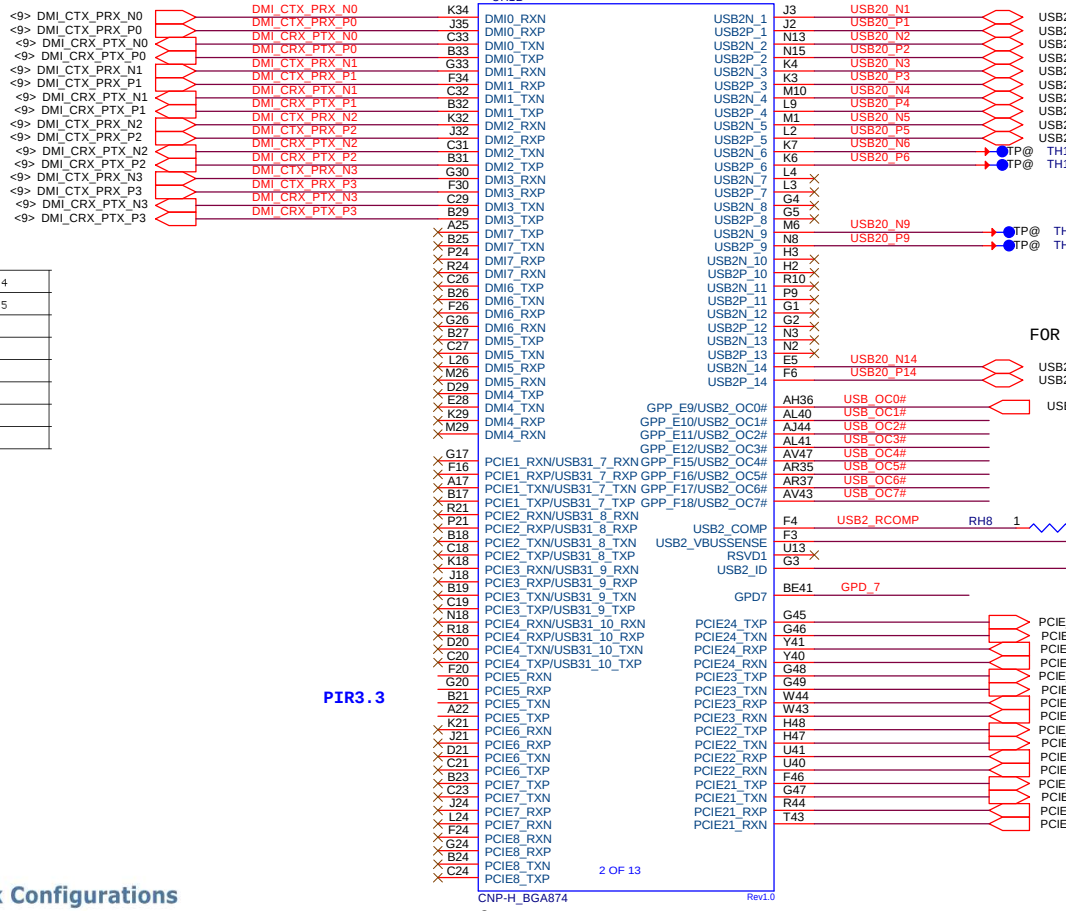
Compal Electronics, Inc.

Title: **CFL-H(8/8)GND/RSVD**

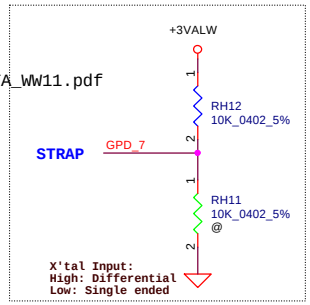
Size	Document Number	Rev
Custom	FPC54 LA-H482P	v0.1

Date: Friday, September 28, 2018 Sheet 13 of 100

from/to CPU DMI[0:3]:RX/TX



FOR CNVI follow 571906_CNL_PCH_TA_WW11.pdf



Flex I/O Lane	HM370
0	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2
4	USB3.1 Gen1
5	USB3.1 Gen1
6	USB3.1 Gen1
7	USB3.1 Gen1
8	N/A
9	N/A
10	GbE
11	N/A
12	N/A
13	N/A
14	PCIe*, GbE
15	PCIe*
16	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B
20	PCIe*
21	PCIe*

PCIE Port 5

22	PCIe*, SATA 4
23	PCIe*, SATA 5
24	PCIe*
25	PCIe*
26	PCIe*
27	PCIe*
28	PCIe*
29	PCIe*

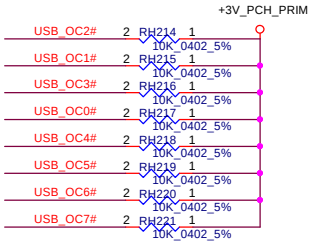
571182-CNL-PCH-H-EDS-Rev2p2 P.198

Figure 26-1. Supported PCI Express* Link Configurations

PCH-H Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 (Cycle Router #1)				PCIe* Controller #4				PCIe* Controller #5 (Cycle Router #3)				PCIe* Controller #6 (Cycle Router #2)			
Flex I/O Lane #		6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
HM370 HM375	1x4									RP 9 SSD#1				RP 13				SSD#2 RP 17				TR RP 21			
	1x4 LR									RP 9				RP 13				RP 17				RP 21			
	2x2									RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1									RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2									RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1									RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
QM370 QM375	1x4					RP 5				RP 9				RP 13				RP 17				RP 21			
	1x4 LR					RP 5				RP 9				RP 13				RP 17				RP 21			
	2x2					RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1					RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2					RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1					RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24
CM246 CM248	1x4	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
	1x4 LR	RP 1				RP 5				RP 9				RP 13				RP 17				RP 21			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11		RP 13		RP 15		RP 17		RP 19		RP 21		RP 23	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12	RP 13		RP 15	RP 16	RP 17		RP 19	RP 20	RP 21		RP 23	RP 24
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9		RP 16	RP 15	RP 13		RP 20	RP 19	RP 17		RP 24	RP 23	RP 21	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12	RP 13	RP 14	RP 15	RP 16	RP 17	RP 18	RP 19	RP 20	RP 21	RP 22	RP 23	RP 24

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
—A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
— PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
— A maximum of 6 SATA Ports (or devices) can be enabled
— SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
— SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
— A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
— A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
— x2 and x4 PCIe* NVMe SSD
— x2 IntelR Optane? Memory Device
— See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configurations , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.



Security Classification	Compal Secret Data		
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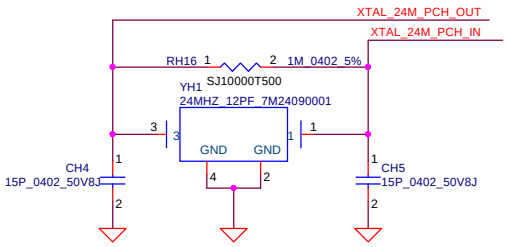
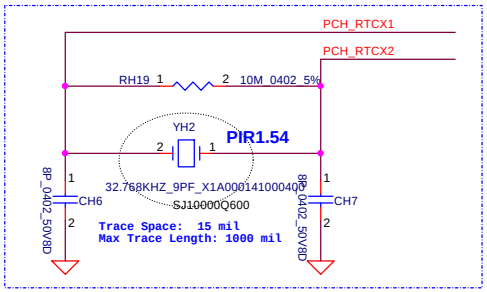
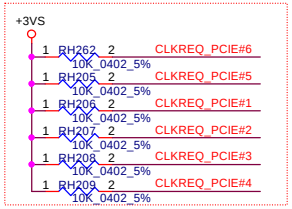
Compal Electronics, Inc.			
Title: PCH(1/8)DMI/PCIE/USB2			
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 14 of 100		

PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf







For DDX03 R02

+1.8V_PRIM **XTAL Frequency Select**

RH26 1 2 4.7K_0402_5% CNV_BRI_PTX_DRX **STRAP**

This signal has a weak internal pull-down.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8V_PRIM

RH93 2 @ 1 4.7K_0402_5% GPP_J9 **STRAP**

The signal has a weak internal pull-down
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

+1.8V_PRIM **M.2 CNV Mode Select**

RH167 2 1 20K_0402_5% CNV_RGI_PTX_DRX **STRAP**
RH168 2 @ 1 100K_0402_5%

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

CNP-H

UH1G

TH74 TP@ BE33 GPP_A16/CLKOUT_48

<10> PCH_CPU_24M_CLK_P PCH_CPU_24M_CLK_P D7 CLKOUT_CPUNSSC_P CLKOUT_ITPXDP# Y3
<10> PCH_CPU_24M_CLK_N PCH_CPU_24M_CLK_N C6 CLKOUT_CPUNSSC# CLKOUT_ITPXDP_P Y4

<10> PCH_CPU_BCLK_P PCH_CPU_BCLK_P B8 CLKOUT_CPUBCLK_P CLKOUT_CPUPCIBCLK# B6 PCH_CPU_PCIBCLK_N → PCH_CPU_PCIBCLK_N <10>
<10> PCH_CPU_BCLK_N PCH_CPU_BCLK_N C8 CLKOUT_CPUBCLK# CLKOUT_CPUPCIBCLK_P A6 PCH_CPU_PCIBCLK_P → PCH_CPU_PCIBCLK_P <10>

XTAL_24M_PCH_OUT RH17 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_OUT_R U9 XTAL_OUT CLKOUT_PCIE_N0 AJ6 CLK_PCIE_N0 → CLK_PCIE_N0 <48>
XTAL_24M_PCH_IN RH18 1 EMI@ 2 33_0402_5% XTAL_24M_PCH_IN_R U10 XTAL_IN CLKOUT_PCIE_P0 AJ7 CLK_PCIE_P0 → CLK_PCIE_P0 <48> **Thunderbolt**

RH20 1 EMI@ 2 60.4_0402_1% XCLK_BIASREF T3 XCLK_BIASREF CLKOUT_PCIE_N1 AH9 CLK_PCIE_N1 → CLK_PCIE_N1 <52>
CLKOUT_PCIE_P1 AH10 CLK_PCIE_P1 → CLK_PCIE_P1 <52> **WLAN (ON BOARD)**

XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PCH_RTCX1 BA49 RTCX1 CLKOUT_PCIE_N2 AE14 CLK_PCIE_N2 → CLK_PCIE_N2 <67>
PCH_RTCX2 BA48 RTCX2 CLKOUT_PCIE_P2 AE15 CLK_PCIE_P2 → CLK_PCIE_P2 <67> **NGFF SSD#1(Key.M)**

Thunderbolt <48> CLKREQ_PCIE#0 CLKREQ_PCIE#0 BF31 GPP_B5/SRCCLKREQ0# CLKOUT_PCIE_N3 AE6 CLK_PCIE_N3 → CLK_PCIE_N3 <71>
WLAN (NGFF) <52> CLKREQ_PCIE#1 CLKREQ_PCIE#1 BE31 GPP_B6/SRCCLKREQ1# CLKOUT_PCIE_P3 AE7 CLK_PCIE_P3 → CLK_PCIE_P3 <71> **Card Reader**
NGFF SSD#1(Key.M) <67> CLKREQ_PCIE#2 CLKREQ_PCIE#2 AR32 GPP_B7/SRCCLKREQ2#
Card Reader <71> CLKREQ_PCIE#3 CLKREQ_PCIE#3 BB30 GPP_B8/SRCCLKREQ3# CLKOUT_PCIE_N4 AC2 CLK_PEG_GPU_N4 → CLK_PEG_GPU_N4 <25>
GPU <25> CLKREQ_PCIE#4 CLKREQ_PCIE#4 BA30 GPP_B9/SRCCLKREQ4# CLKOUT_PCIE_P4 AC3 CLK_PEG_GPU_P4 → CLK_PEG_GPU_P4 <25> **GPU**
LAN <51> CLKREQ_PCIE#5 CLKREQ_PCIE#5 AN29 GPP_B10/SRCCLKREQ5#
NGFF SSD#2(Key.M) <68> CLKREQ_PCIE#6 CLKREQ_PCIE#6 AE47 GPP_H0/SRCCLKREQ6# CLKOUT_PCIE_N5 AB2 CLK_PCIE_N5 → CLK_PCIE_N5 <51>
AC48 GPP_H1/SRCCLKREQ7# CLKOUT_PCIE_P5 AB3 CLK_PCIE_P5 → CLK_PCIE_P5 <51> **LAN**
AE41 GPP_H2/SRCCLKREQ8#
AF48 GPP_H3/SRCCLKREQ9# CLKOUT_PCIE_N6 W4 CLK_PCIE_N6 → CLK_PCIE_N6 <68>
AC41 GPP_H4/SRCCLKREQ10# CLKOUT_PCIE_P6 W3 CLK_PCIE_P6 → CLK_PCIE_P6 <68> **NGFF SSD#1(Key.M)**
AC39 GPP_H5/SRCCLKREQ11#
AE39 GPP_H6/SRCCLKREQ12# CLKOUT_PCIE_N7 W7
AB48 GPP_H7/SRCCLKREQ13# CLKOUT_PCIE_P7 W6
AC44 GPP_H8/SRCCLKREQ14#
AC43 GPP_H9/SRCCLKREQ15# CLKOUT_PCIE_N8 AC14
CLKOUT_PCIE_P8 AC15
V2 CLKOUT_PCIE_N15 CLKOUT_PCIE_N9 U2
V3 CLKOUT_PCIE_P15 CLKOUT_PCIE_P9 U3
T2 CLKOUT_PCIE_N14 CLKOUT_PCIE_N10 AC9
T1 CLKOUT_PCIE_P14 CLKOUT_PCIE_P10 AC11
AA1 CLKOUT_PCIE_N13 CLKOUT_PCIE_N11 AE9
Y2 CLKOUT_PCIE_P13 CLKOUT_PCIE_P11 AE11
AC7 CLKOUT_PCIE_N12 CLKIN_XTAL R6 REFCLK_CNV → REFCLK_CNV <52>
AC6 CLKOUT_PCIE_P12

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CNP-H_BGA874 Rev1.0

@

+3V_PCH_PRIM

RH178 100K_0402_5%

RH173 10K_0402_5%

CNP-H

UH1M

<66> TPM_IRQ# TPM_IRQ# AW13 GPP_G0/SD_CMD CNV_WR_CLKN BD4 CLK_CNV_PRX_DTX_N → CLK_CNV_PRX_DTX_N <52>
BE9 GPP_G1/SD_DATA0 CNV_WR_CLKP BE3 CLK_CNV_PRX_DTX_P → CLK_CNV_PRX_DTX_P <52>
BF8 GPP_G2/SD_DATA1
BF9 GPP_G3/SD_DATA2 CNV_PRX_DTX_N0
BG8 GPP_G4/SD_DATA3 CNV_WR_D0N BB3 CNV_PRX_DTX_P0
BE8 GPP_G5/SD_CD# CNV_WR_D0P BB4 CNV_PRX_DTX_N1
BD8 GPP_G6/SD_CLK CNV_WR_D1N BA3 CNV_PRX_DTX_P1
AV13 GPP_G7/SD_WP CNV_WR_D1P BA2

CNV_WT_CLKN BC5 CLK_CNV_PTX_DRX_N → CLK_CNV_PTX_DRX_N <52>
AP3 GPP_I11/M2_SKT2_CFG0 CNV_WT_CLKP BB6 CLK_CNV_PTX_DRX_P → CLK_CNV_PTX_DRX_P <52>
AP2 GPP_I12/M2_SKT2_CFG1 3.3V
AN4 GPP_I13/M2_SKT2_CFG2 CNV_WT_D0N BE6 CNV_PTX_DRX_N0
AM7 GPP_I14/M2_SKT2_CFG3 CNV_WT_D0P BD7 CNV_PTX_DRX_P0 → CNV_PTX_DRX_P0 <52>
CNV_WT_D1N BG6 CNV_PTX_DRX_N1 → CNV_PTX_DRX_N1 <52>
No support S0ix TH4968TP@ AV6 GPP_J0/CNV_PA_BLANKING CNV_WT_D1P BF6 CNV_PTX_DRX_P1 → CNV_PTX_DRX_P1 <52>
TH135 TP@ CPU_C10_GATE# AY3 GPP_J1/CPU_C10_GATE# CNV_WT_RCOMP BA1 CNV_WT_RCOMP RH25 1 2 150_0402_1%
TH4969TP@ AR13 GPP_J11/A4WP_PRESENT
AV7 GPP_J10 PCIE_RCOMPN B12 PCIE_RCOMPN RH21 1 2 100_0402_1%
AW3 GPP_J_2 1.8V PCIE_RCOMPP A13 PCIE_RCOMPP
AT10 GPP_J_3 SD_1P8_RCOMP BE5 SD_RCOMP_1P8 RH22 1 2 200_0402_1%
AV4 SD_3P3_RCOMP BE4 SD_RCOMP_3P3 RH23 1 2 200_0402_1%
<52> CNV_BRI_PTX_DRX CNV_BRI_PTX_DRX AY2 GPP_J4/CNV_BRI_DT/UART0B_RTS# BD1
<52> CNV_BRI_PRX_DTX CNV_BRI_PRX_DTX BA4 GPP_J5/CNV_BRI_RSP/UART0B_RXD GPPJ_RCOMP_1P81 BE1 GPPJ_RCOMP_1P8 RH24 1 2 200_0402_1%
<52> CNV_RGI_PTX_DRX CNV_RGI_PTX_DRX AV3 GPP_J6/CNV_RGI_DT/UART0B_TXD GPPJ_RCOMP_1P82 BE2
<52> CNV_RGI_PRX_DTX CNV_RGI_PRX_DTX AW2 GPP_J7/CNV_RGI_RSP/UART0B_CTS# GPPJ_RCOMP_1P83
GPP_J9 GPP_J9 AU9 GPP_J8/CNV_MFUART2_RXD
GPP_J9/CNV_MFUART2_TXD RSVD2 Y35
RSVD3 Y36
RSVD1 BC1
TP AL35 TP@ TH101

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CNP-H_BGA874 Rev1.0

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#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

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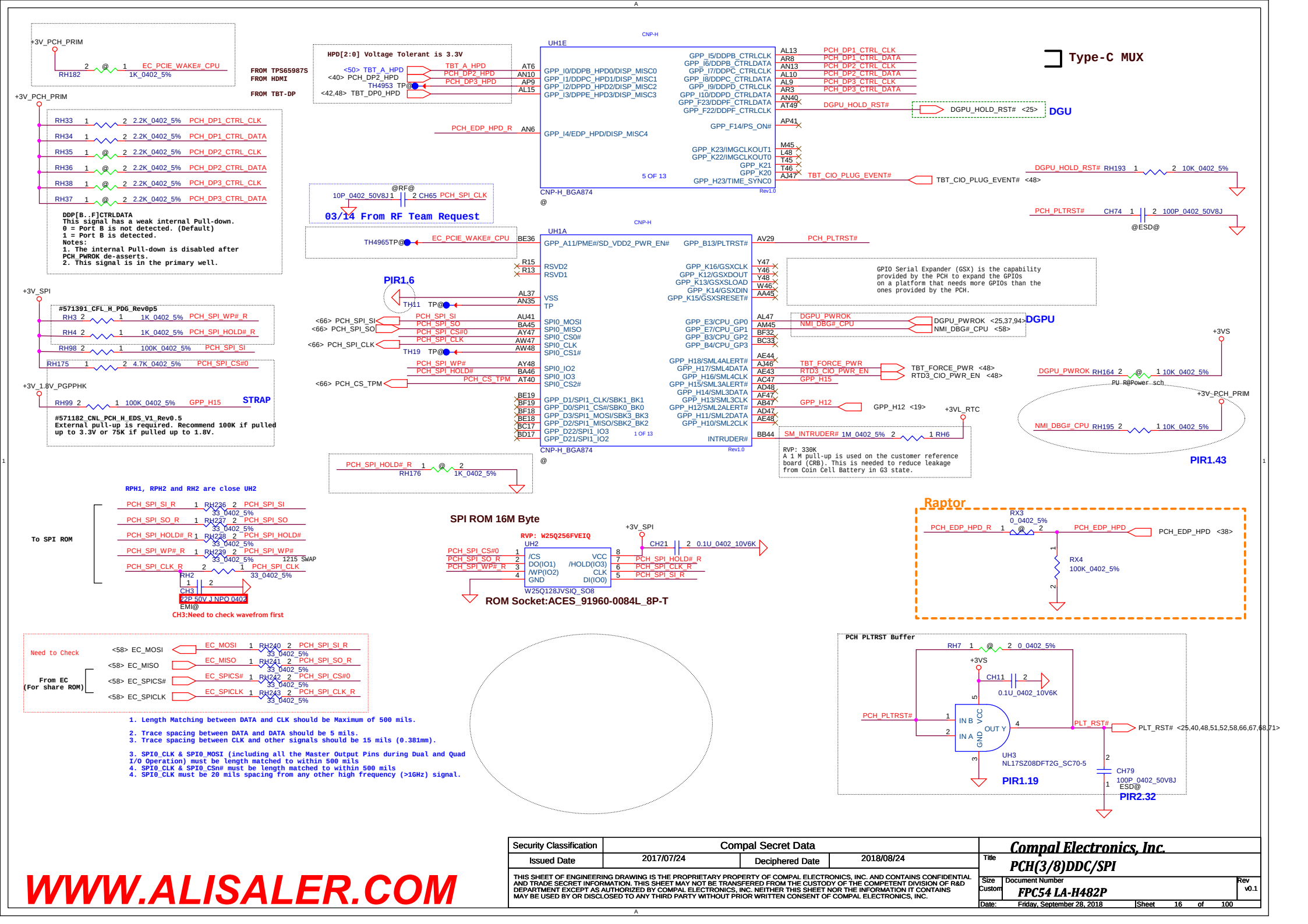
Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 15 of 100



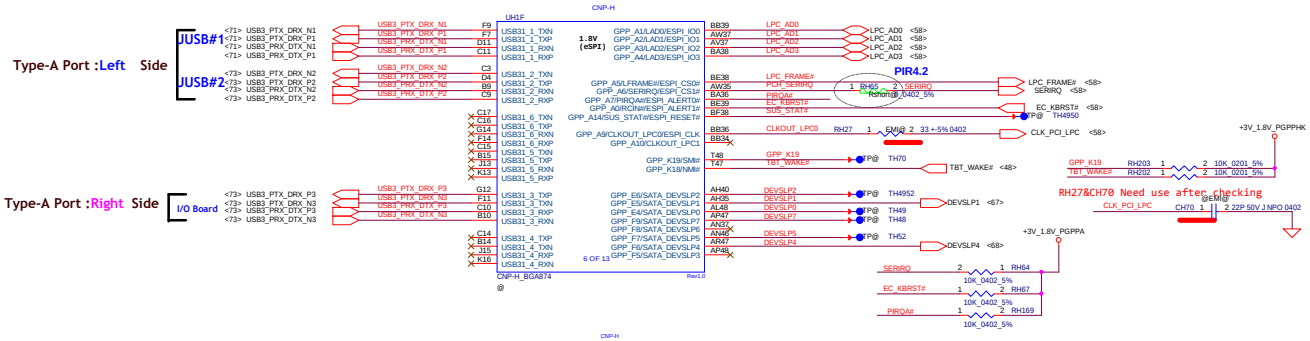
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

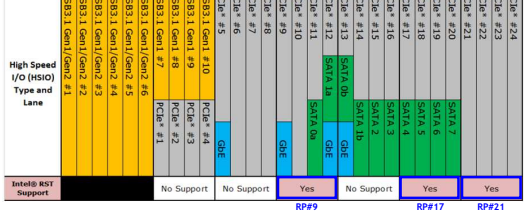
Compal Electronics, Inc.

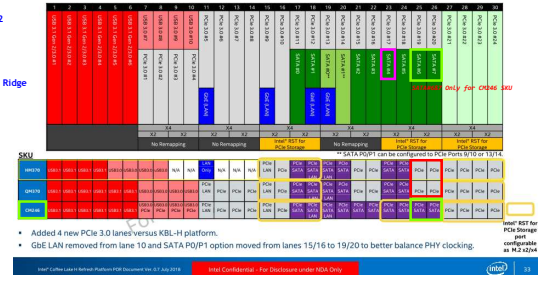
Title: PCH(3/8)DDC/SPI

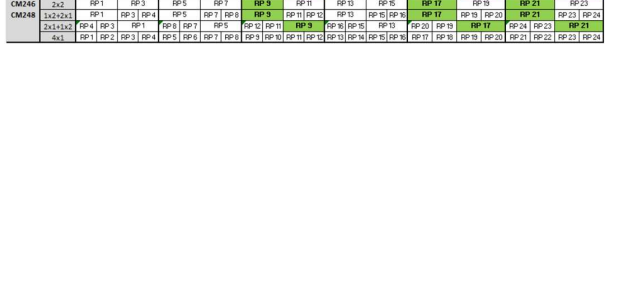
Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 16 of 100









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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Title: PCIE/SATA/USB3/eSPI

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

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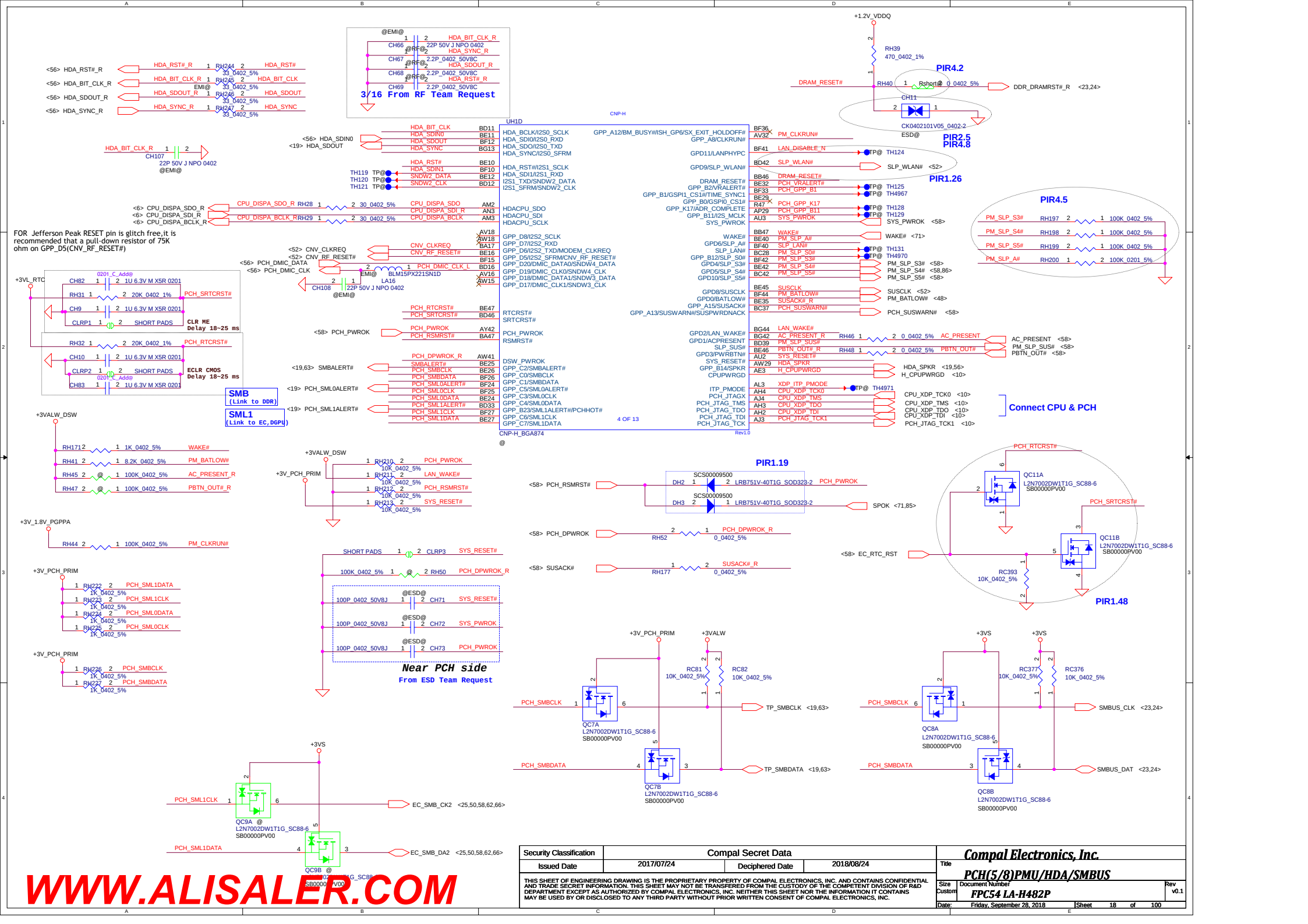

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title	PCH(5/8)PMU/HDA/SMBUS		
Size	Document Number		Rev
Custom	FPC54 LA-H482P		v0.1
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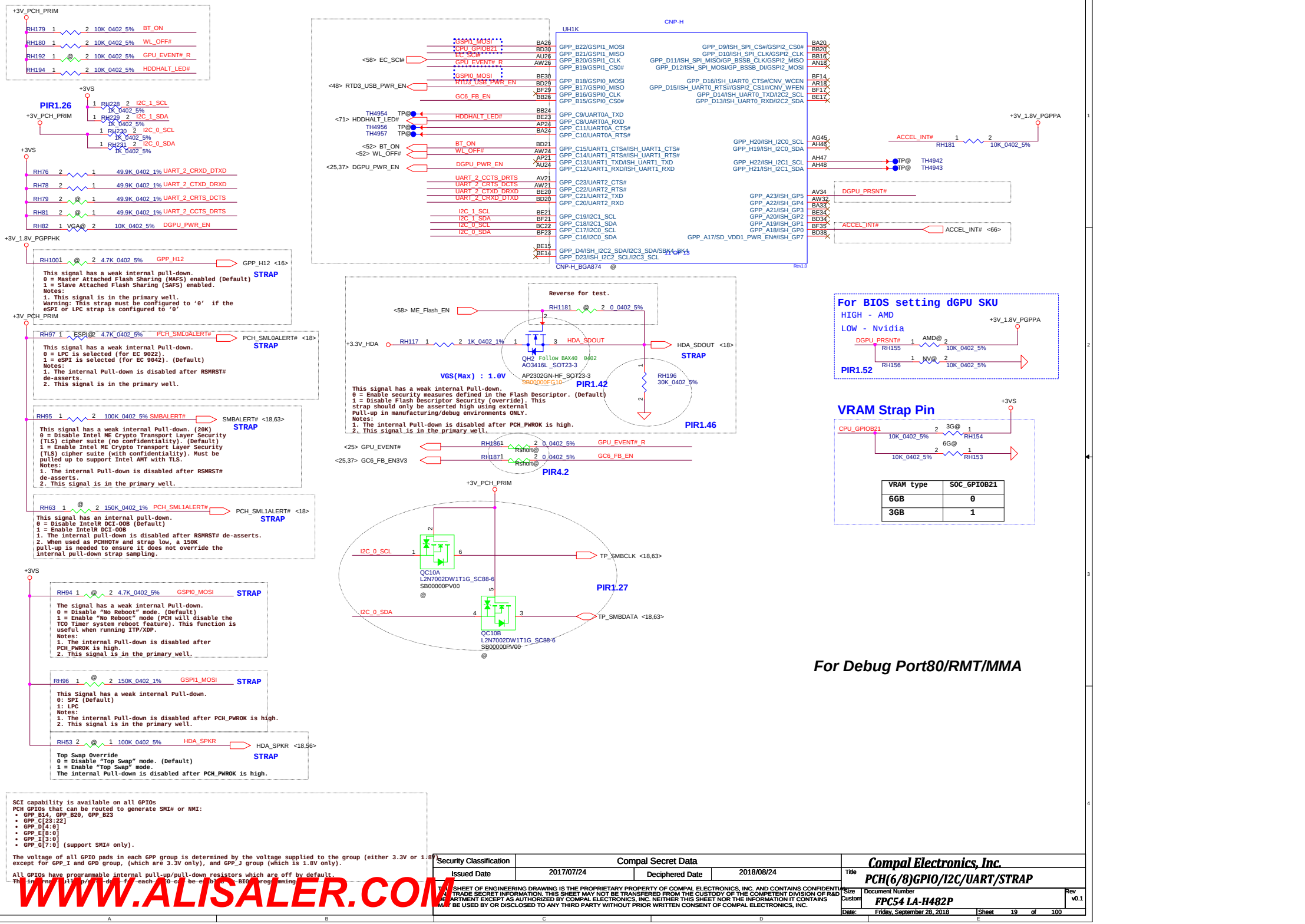

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	FPC54 LA-H482P	v0.1

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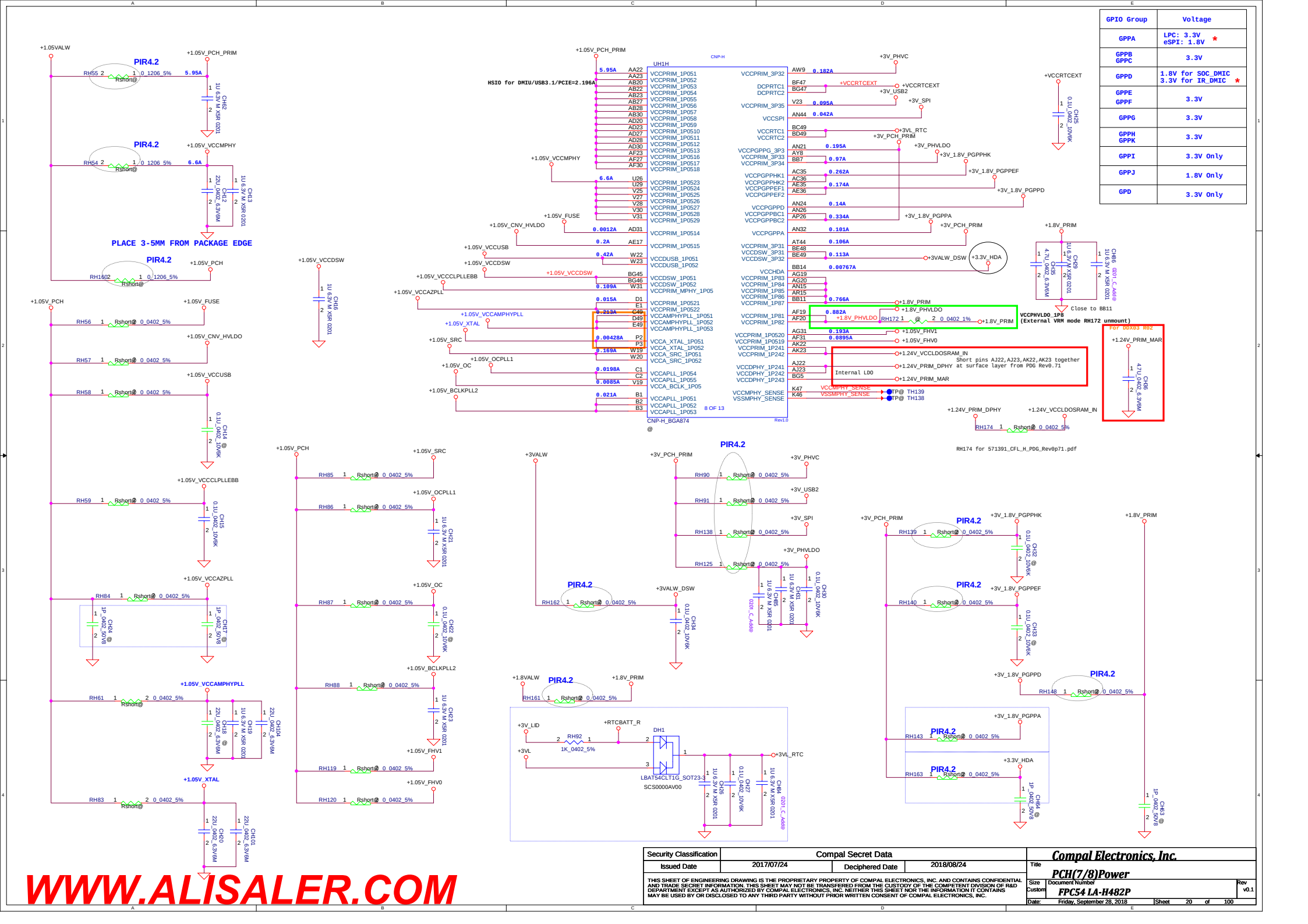
GPIO Group
Voltage
GPPA
LPC: 3.3V
eSPI: 1.8V *
GPPB
GPPC
3.3V
GPPD
1.8V for SOC_DMIC
3.3V for IR_DMIC *
GPPE
GPPF
3.3V
GPPG
3.3V
GPPH
GPPK
3.3V
GPPI
3.3V Only
GPPJ
1.8V Only
GPD
3.3V Only
PLACE 3-5MM FROM PACKAGE EDGE
HSIO for DMIU/USB3.1/PCIE=2.196A
VCCPHVLDO_1P8
(External VRM mode RH172 unmount)
Close to BB11
Short pins AJ22,AJ23,AK22,AK23 together
at surface layer from PDG Rev0.71
Internal LDO
RH174 for 571391_CFL_H_PDG_Rev0p71.pdf
WWW.ALISALER.COM
Compal Electronics, Inc.
PCH(7/8)Power
FPC54 LA-H482P
Compal Secret Data
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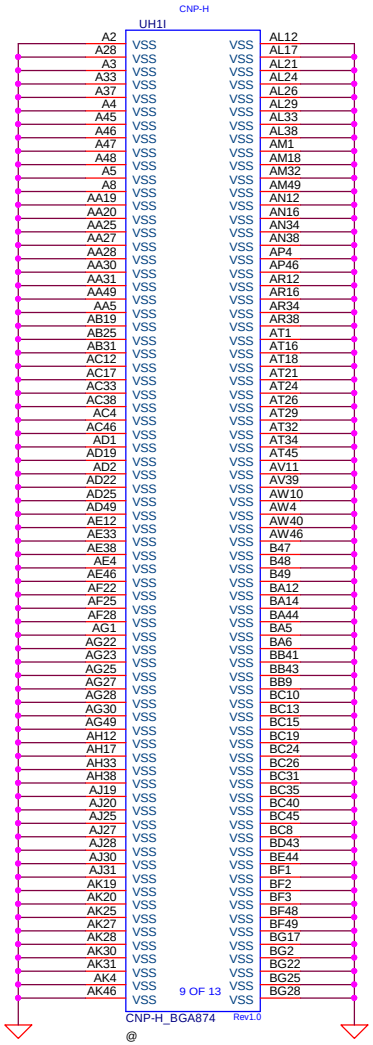
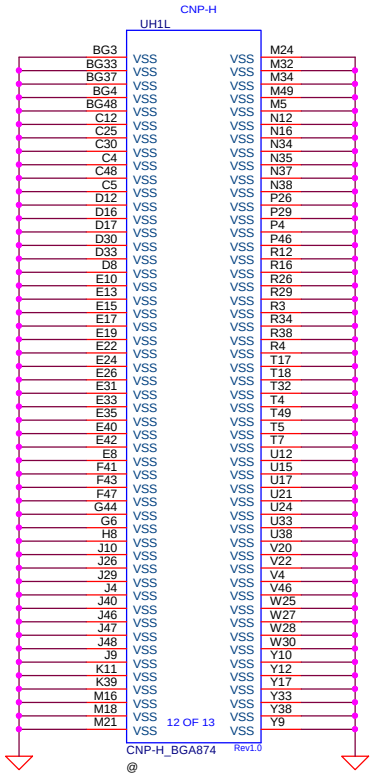
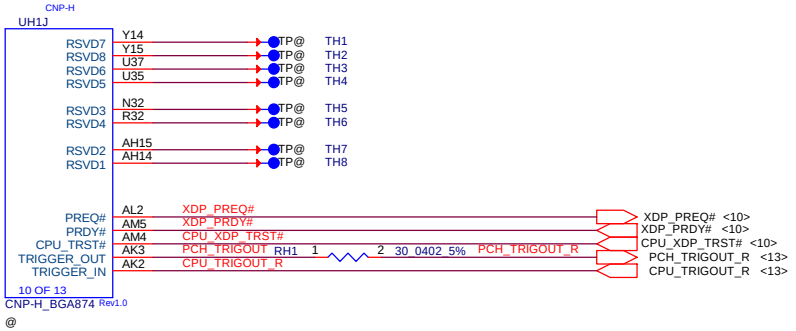






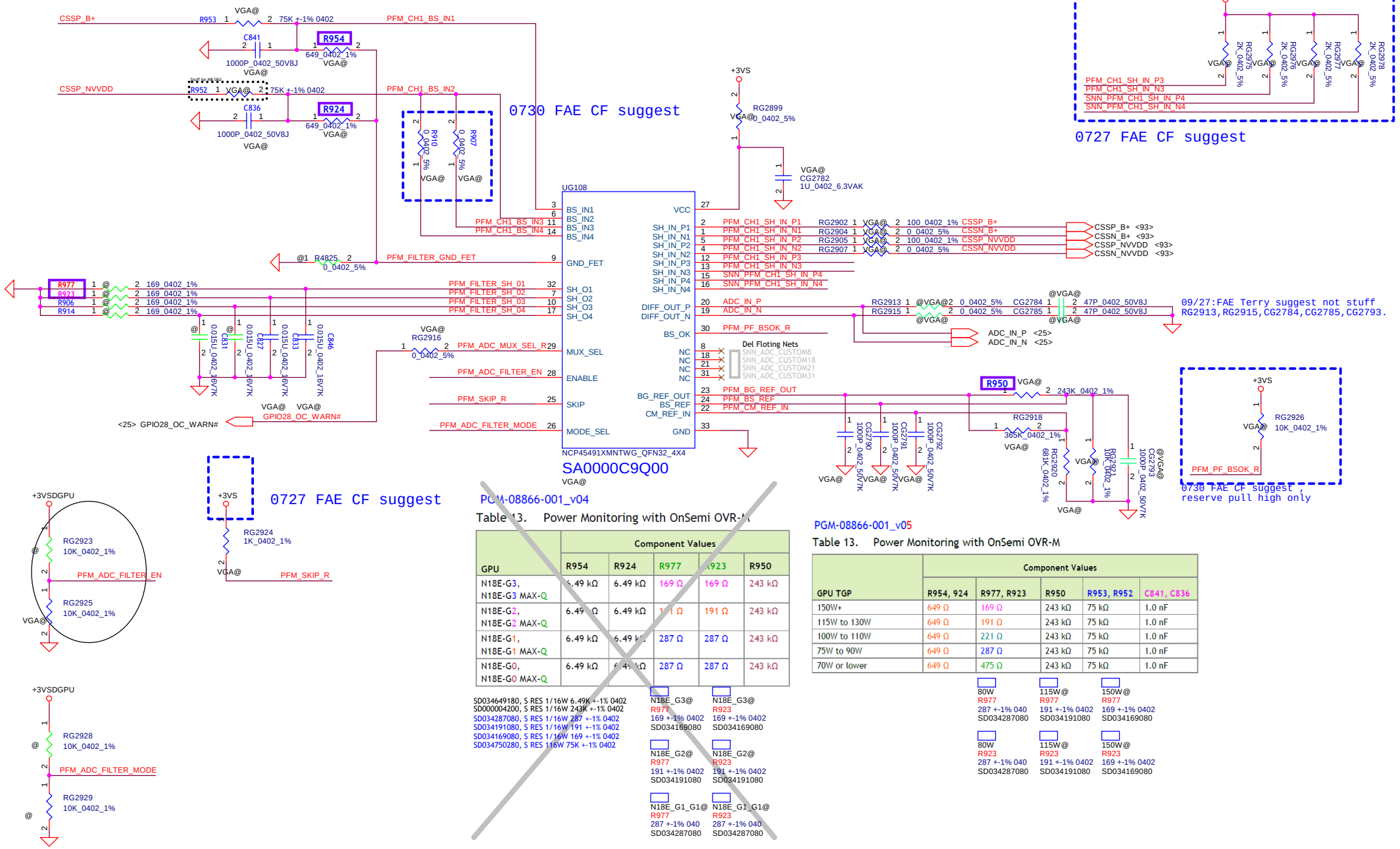
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(8/8)GND/RSVD

Size	Document Number	Rev
Custom	FPC54 LA-H482P	v0.1

Date: Friday, September 28, 2018 Sheet 21 of 100



PGM-08866-001_v04

Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954	R924	R977	R923	R950
N18E-G3, N18E-G3 MAX-Q	6.49 kΩ	6.49 kΩ	169 Ω	169 Ω	243 kΩ
N18E-G2, N18E-G2 MAX-Q	6.49 kΩ	6.49 kΩ	191 Ω	191 Ω	243 kΩ
N18E-G1, N18E-G1 MAX-Q	6.49 kΩ	6.49 kΩ	287 Ω	287 Ω	243 kΩ
N18E-G0, N18E-G0 MAX-Q	6.49 kΩ	6.49 kΩ	287 Ω	287 Ω	243 kΩ

SD034649180, S RES 1/16W 6.49K +-1% 0402
SD000004200, S RES 1/16W 243K +-1% 0402
SD034287080, S RES 1/16W 287 +-1% 0402
SD034191080, S RES 1/16W 191 +-1% 0402
SD034169080, S RES 1/16W 169 +-1% 0402
SD034750280, S RES 1/16W 75K +-1% 0402

N18E_G3@ R977 169 +-1% 0402 SD034169080
N18E_G3@ R923 169 +-1% 0402 SD034169080
N18E_G2@ R977 191 +-1% 0402 SD034191080
N18E_G2@ R923 191 +-1% 0402 SD034191080
N18E_G1_G1@ R977 287 +-1% 040 SD034287080
N18E_G1_G1@ R923 287 +-1% 040 SD034287080

PGM-08866-001_v05

Table 13. Power Monitoring with OnSemi OVR-M

GPU TGP	Component Values				
	R954, 924	R977, R923	R950	R953, R952	C841, C836
150W+	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
115W to 130W	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
100W to 110W	649 Ω	221 Ω	243 kΩ	75 kΩ	1.0 nF
75W to 90W	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
70W or lower	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF

80W R977 287 +-1% 040 SD034287080
115W@ R977 191 +-1% 0402 SD034191080
150W@ R977 169 +-1% 0402 SD034169080
80W R923 287 +-1% 040 SD034287080
115W@ R923 191 +-1% 0402 SD034191080
150W@ R923 169 +-1% 0402 SD034169080

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: OVR-M

Size: Custom | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

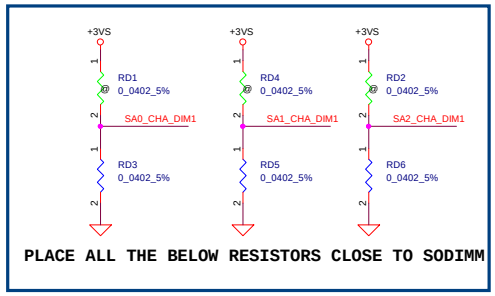
Date: Friday, September 28, 2018 | Sheet 22 of 100

CHANNEL-A

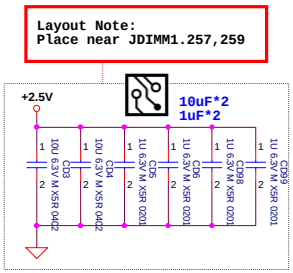
REVERSE TYPE (4 mm)

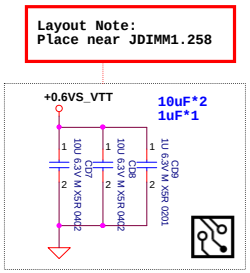
Interleaved Memory

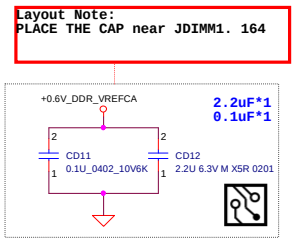
TOP: JDIMM1 CONN Non-ECC DIMM

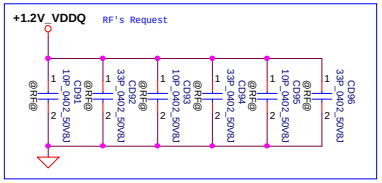


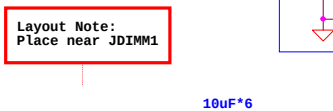
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

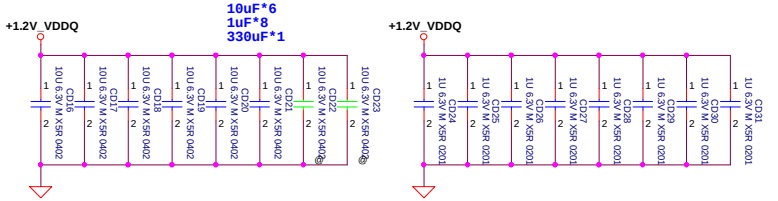


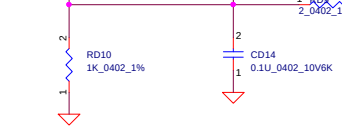


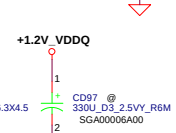


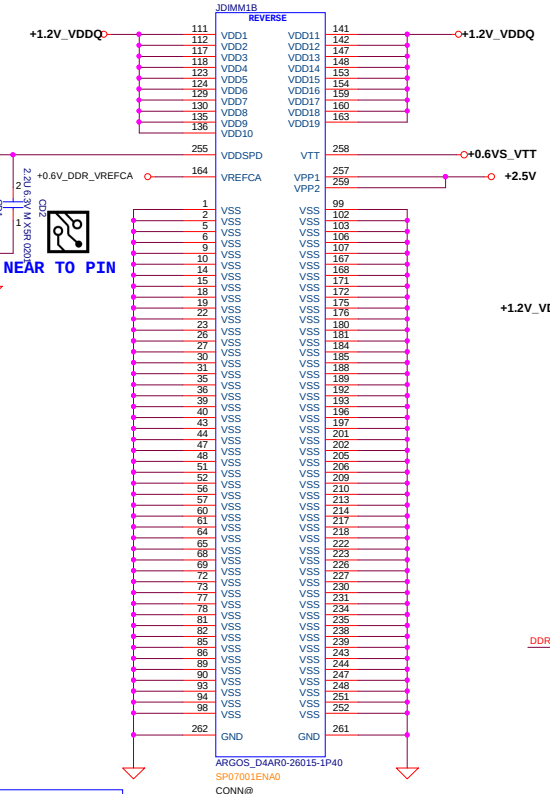




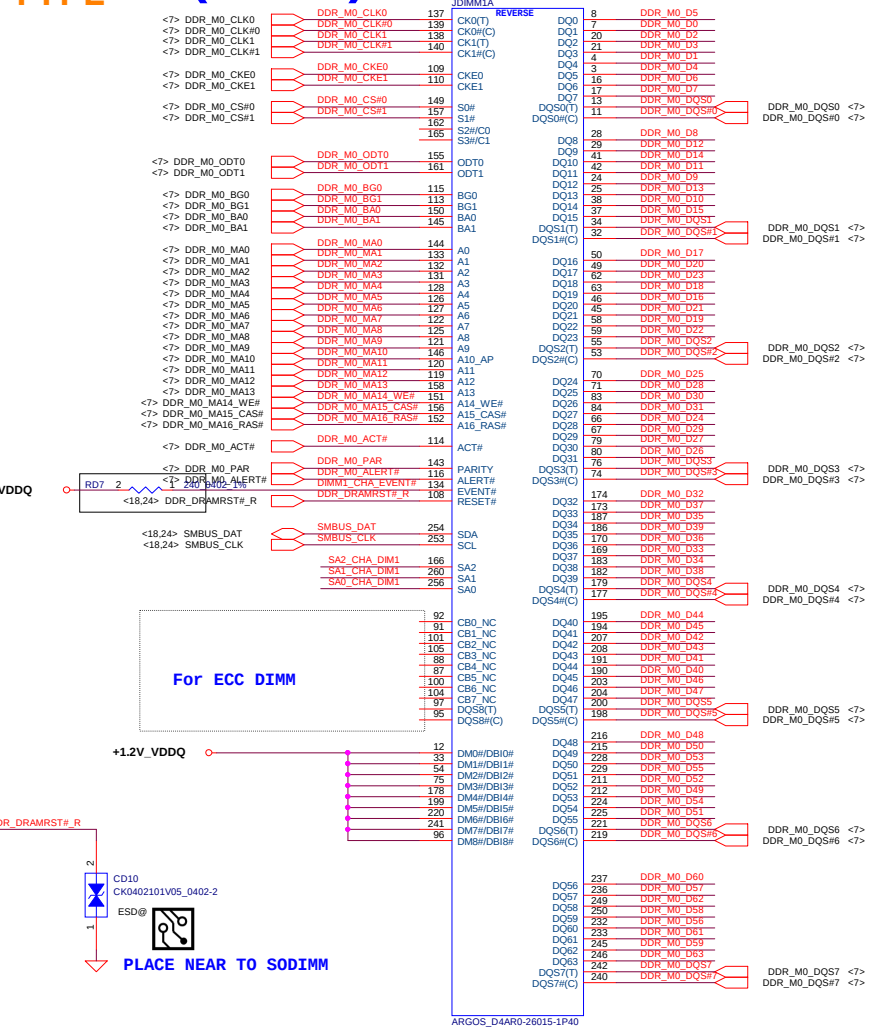








PLACE NEAR TO PIN



For ECC DIMM

DIMM Side

CPU Side

VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: DDRIV_CHA: DIMM0

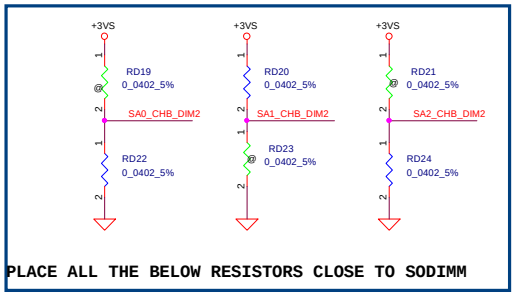
Size: | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 23 of 100

17.3"=>Reverse TYPE (8 mm)

Interleaved Memory

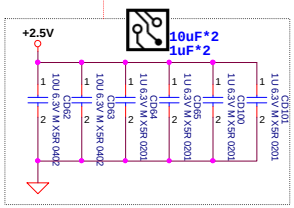
TOP: JDIMM2 CONN Non-ECC DIMM



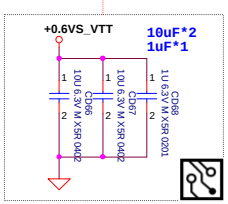
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

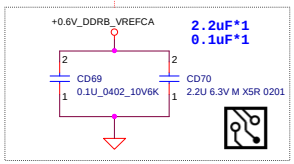
Layout Note:
Place near JDIMM2.257,259



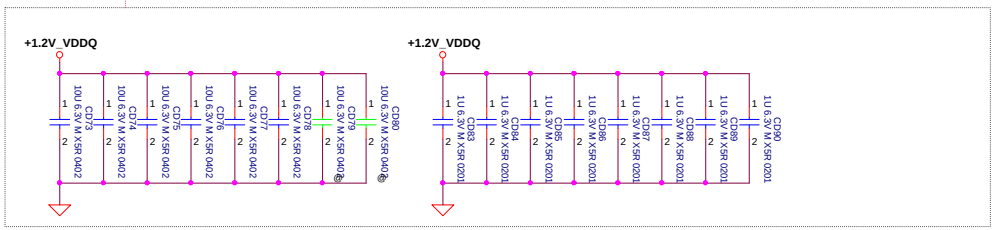
Layout Note:
Place near JDIMM2.258

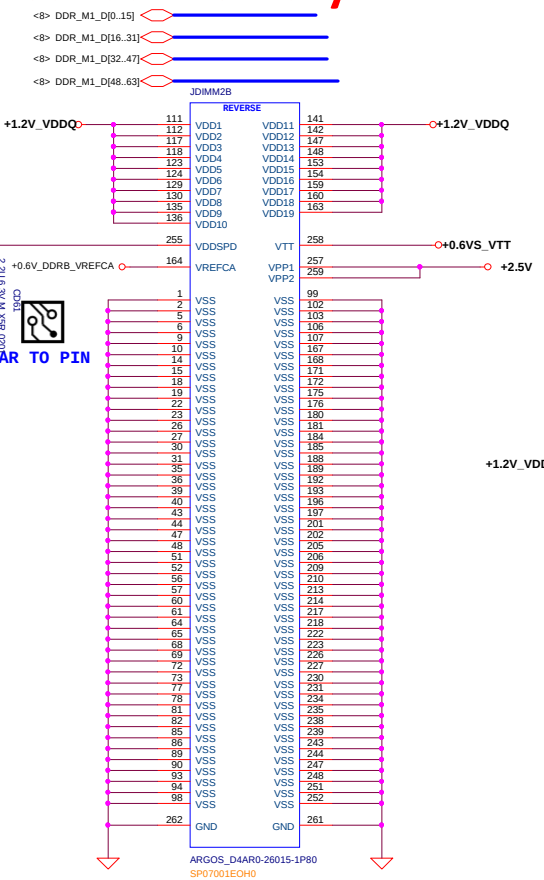


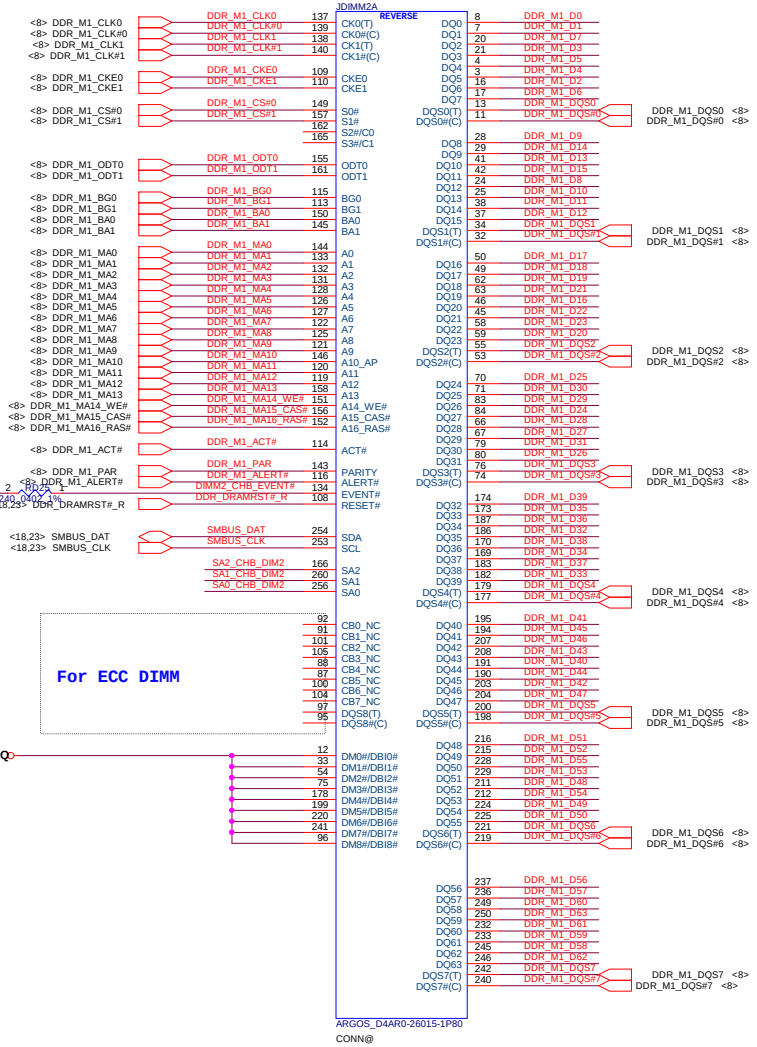
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

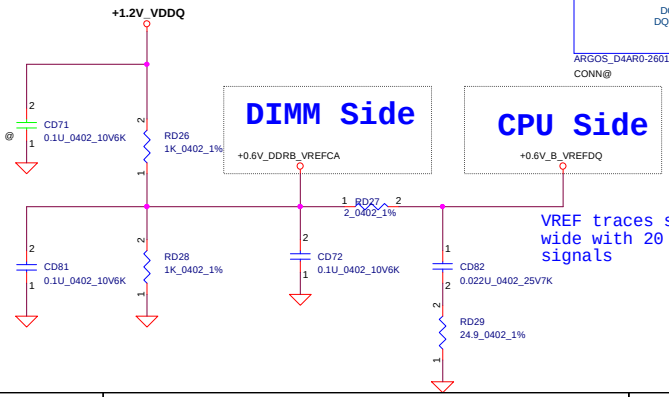


Layout Note:
Place near JDIMM2









VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

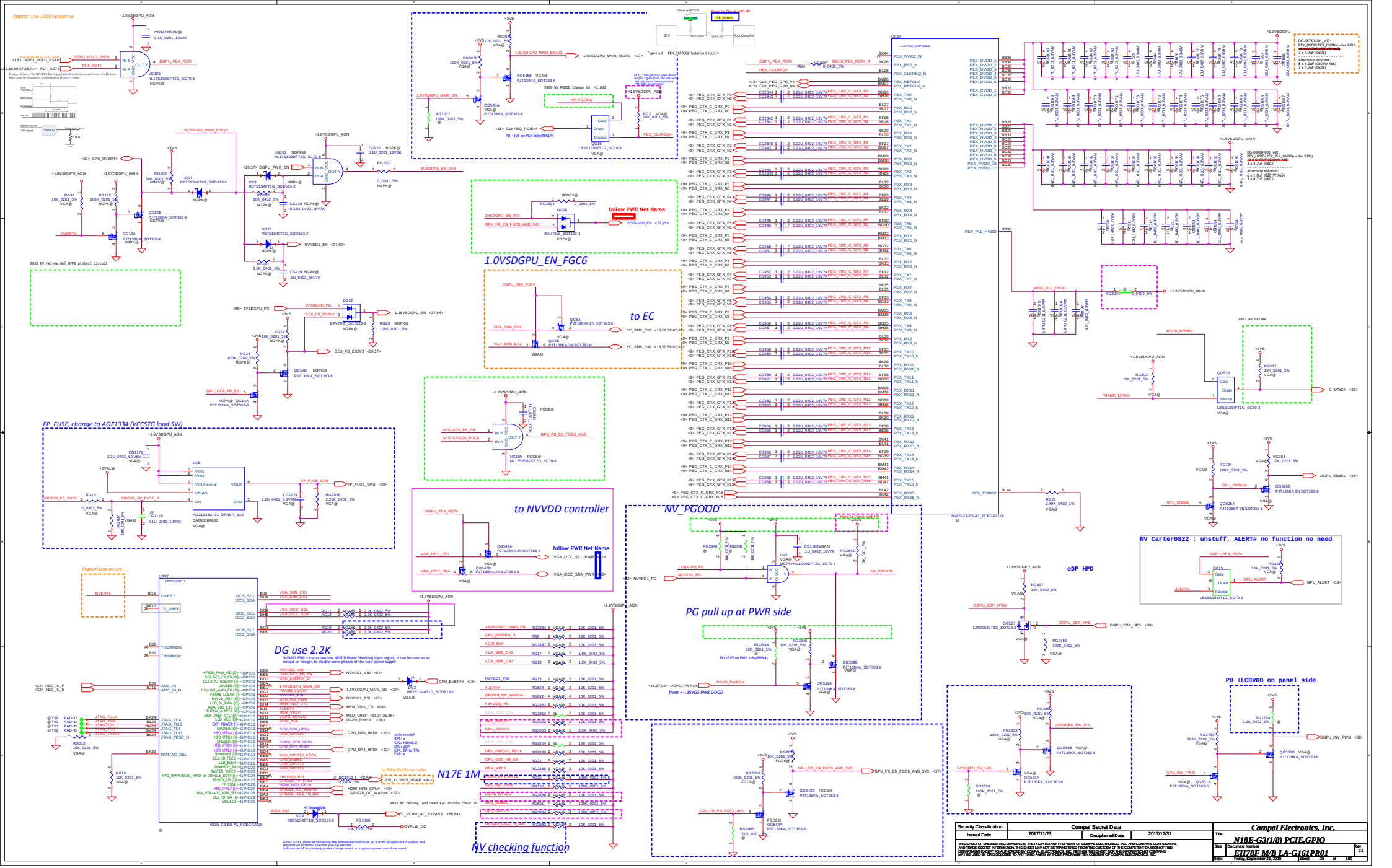
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: **DDRIV_CHB: DIMM0**

Size: | Document Number: **FPC72 LA-H492P** | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 24 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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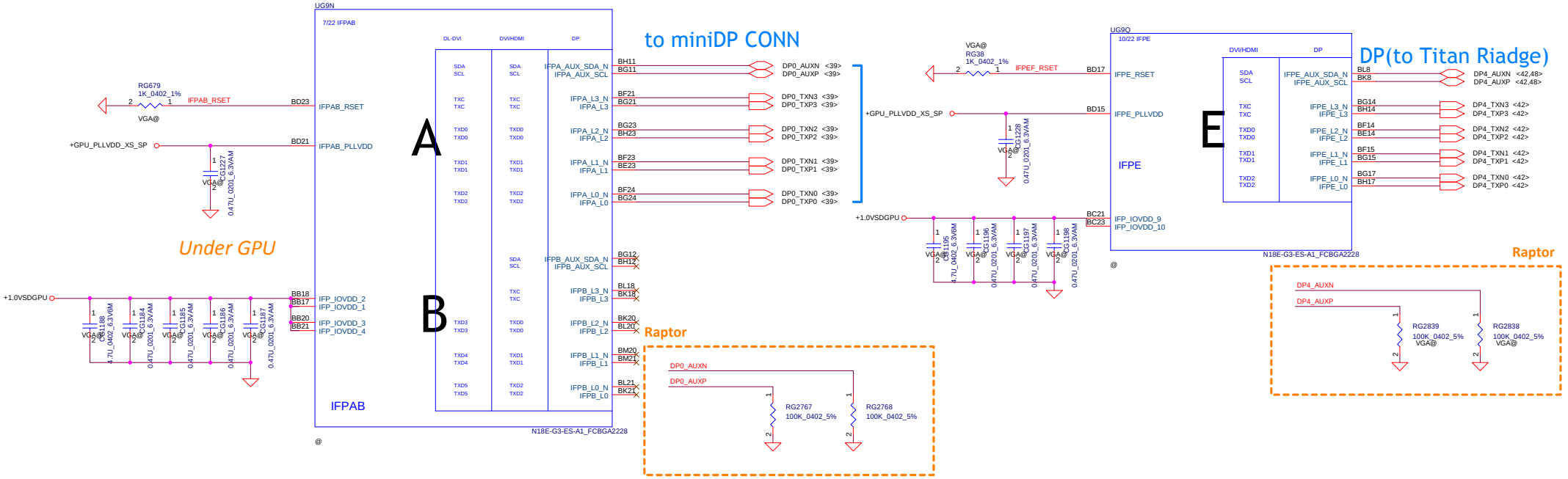
Compal Electronics, Inc.

Title: N18E-G3(1/8) PCIE,GPIO

Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1

Date: Friday, September 28, 2018 Sheet 25 of 100



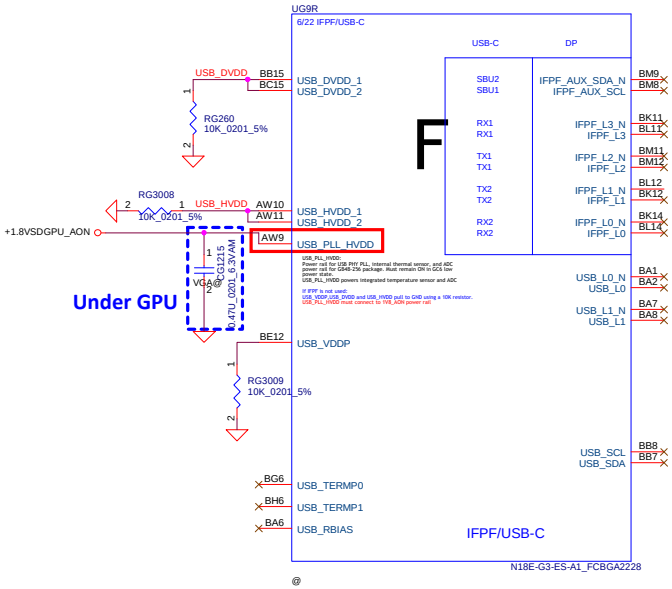


Table 9.1 PCB Display Link Summary (GB4B-256 packages)

Digital Display Link	Dual-Link DVI	HDMI	eDP	DisplayPort	USBC	
If USB-C is Implemented						
IFPA (Link A)	✓(Dual Link with IFPB)			✓		DP(typeC)
IFPB (Link B)	✓(Dual Link with IFPA)					
IFPC (Link C)		✓		✓		HDMI
IFPD (Link D)			✓	✓		
IFPE (Link E)		✓		✓		miniDP
IFPF (Link F)					✓	
If USB-C is Not Implemented						
IFPA (Link A)	✓(Dual Link with IFPB)			✓		DP(typeC)
IFPB (Link B)	✓(Dual Link with IFPA)			✓		
IFPC (Link C)		✓		✓		HDMI
IFPD (Link D)			✓			eDP
IFPE (Link E)		✓		✓		miniDP
IFPF (Link F)				✓		

OLD: DP(typeC), HDMI, miniDP
follow "EH78F_LA-G161PR01_0825": miniDP, x, HDMI, eDP, DP(typeC), x

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

Table 9.3 Display Link Power Rail Applicability

Display Link Rail	Display Links that Receive Power from This Rail					
	Link A	Link B	Link C	Link D	Link E	Link F
IFP_IOVDD	✓ miniDP	✓	HDMI ✓	eDP ✓	DP(typeC) ✓	✓
IFPAB_PLLVDD	✓ miniDP	✓				
IFPCD_PLLVDD			HDMI ✓	eDP ✓		
IFPEF_PLLVDD					✓ DP(typeC)	✓

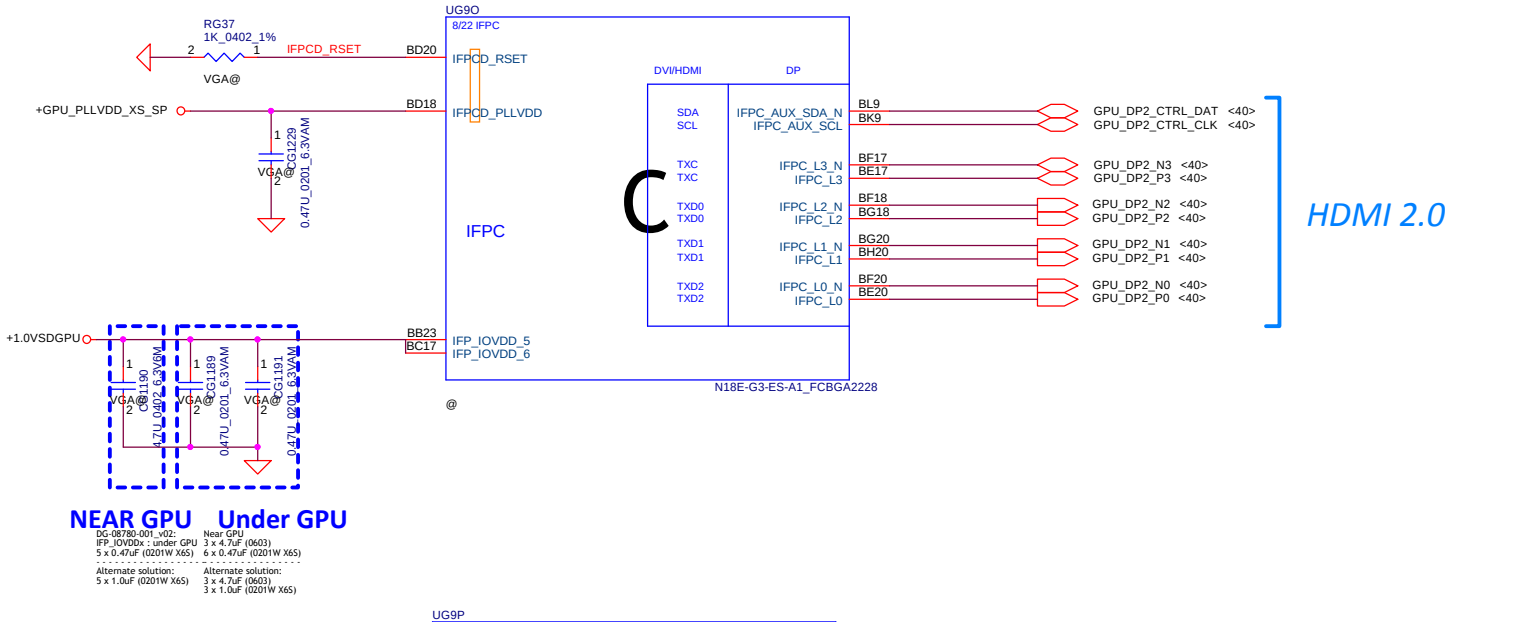
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.

Title: N18E-G3(2/8) DP

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 26 of 100



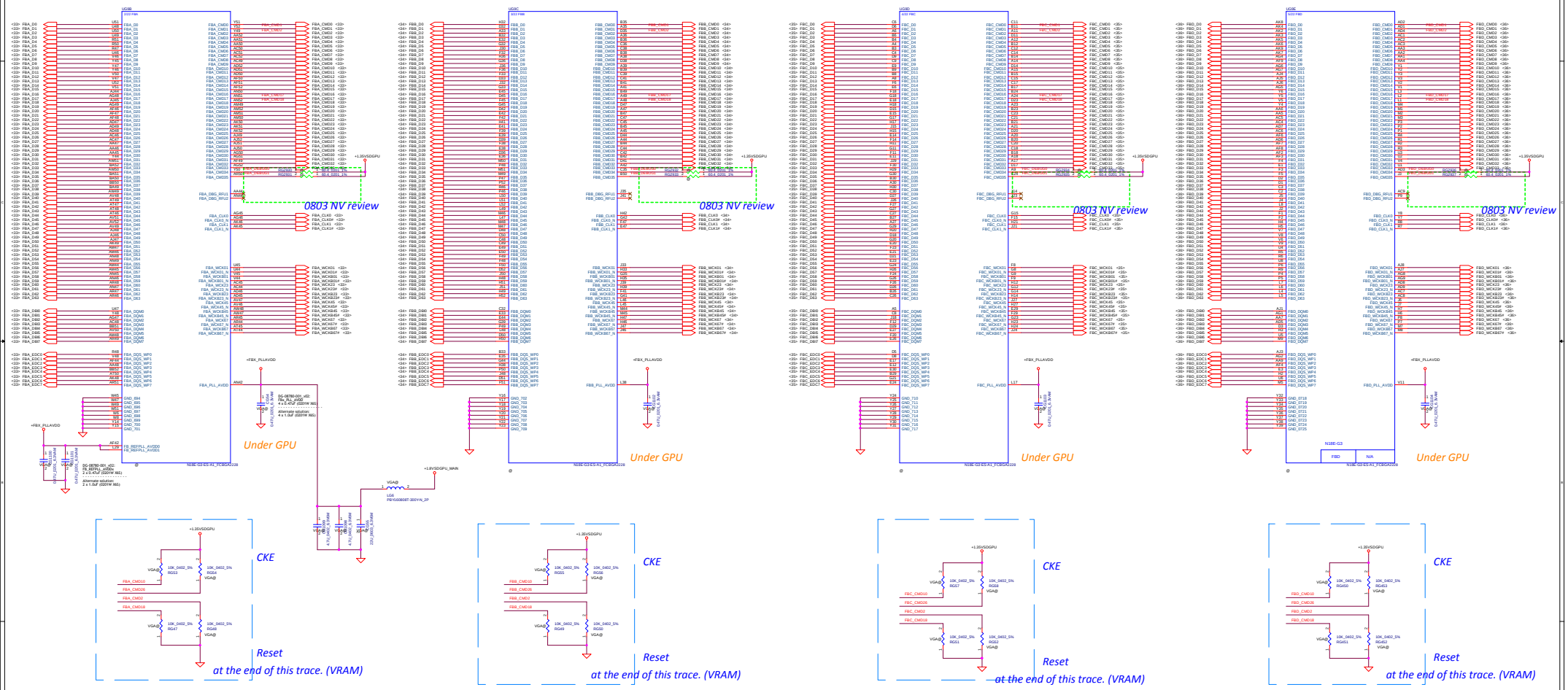
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.

Title: **N18E-G3(3/8) eDP,HDMI**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 27 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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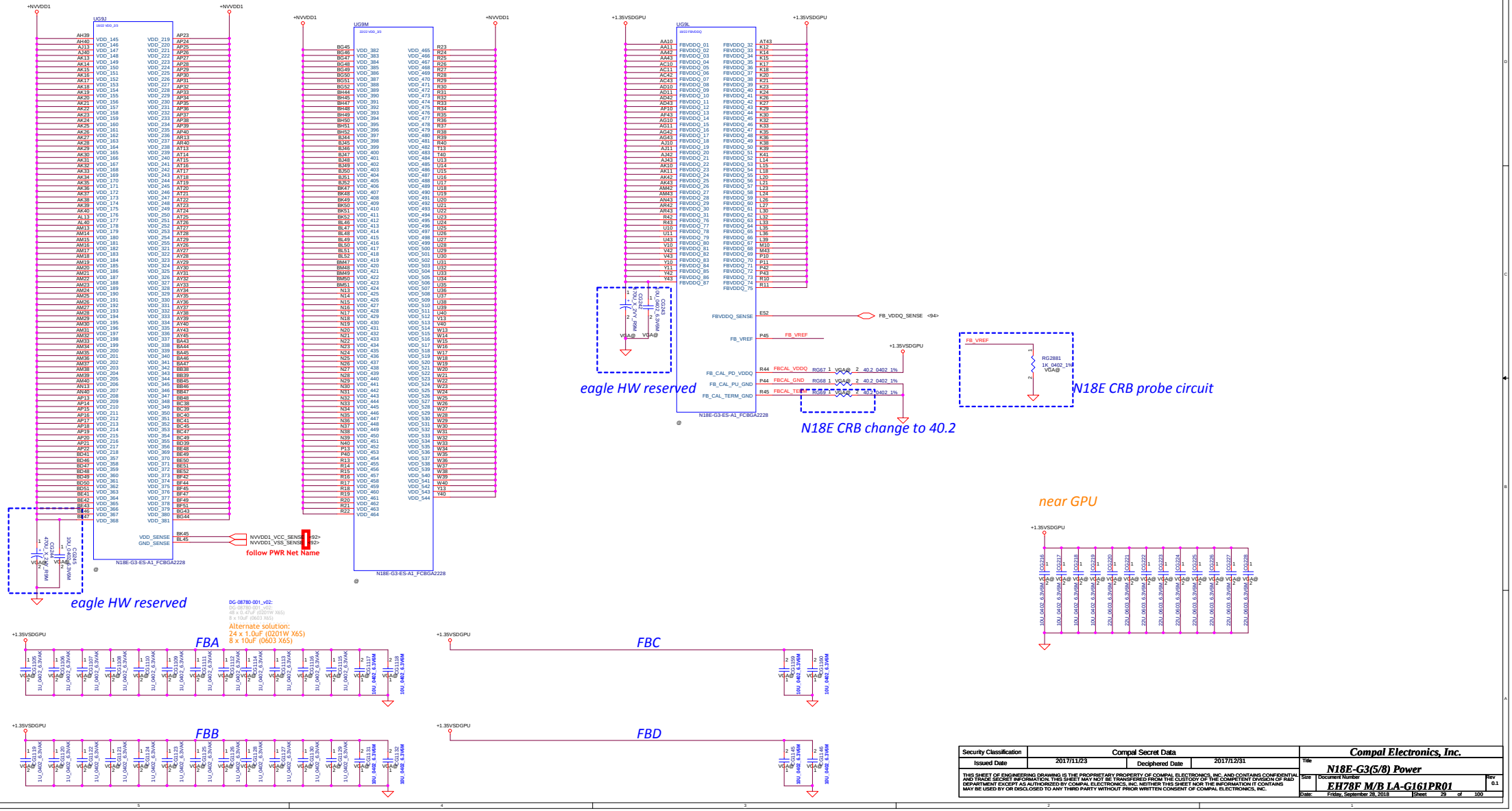
Title	N18E-G34(4/8) MEM		
Size	Document Number		Rev
	EH78F M/B LA-G161PR01		0.1
Date:	Tuesday, December 26, 2017	Sheet 38 of 106	



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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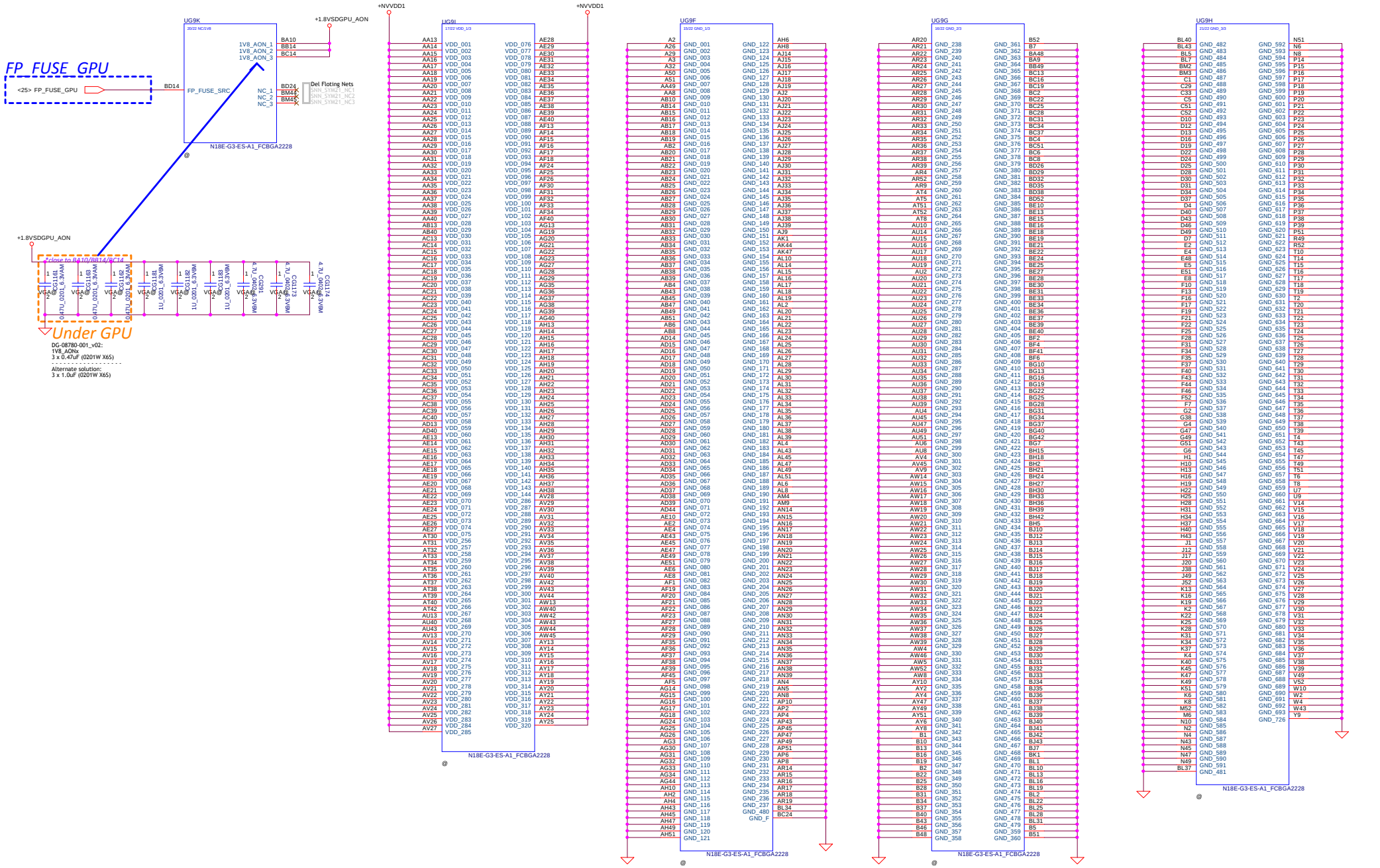
Compal Electronics, Inc.

Title: N18E-G3(5/8) Power

Size: | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 29 of 100



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.

Title: **N18E-G3(6/8) Power,GND**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 30 of 100

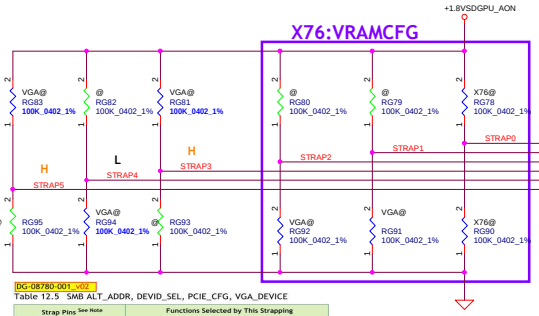
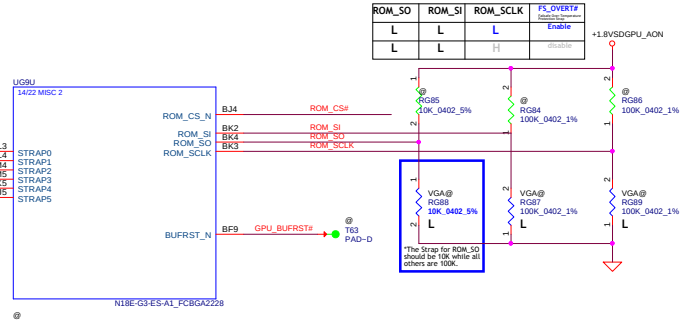


Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

DEVID_SEL:
0: Normal Panel
1:G-SYNC Panel

VGA_DEVICE:
0: No Display out
1:GPU Display out=1



ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT#
L	L	L	Enable
L	L	H	disable

N18E CS# add 33ohm

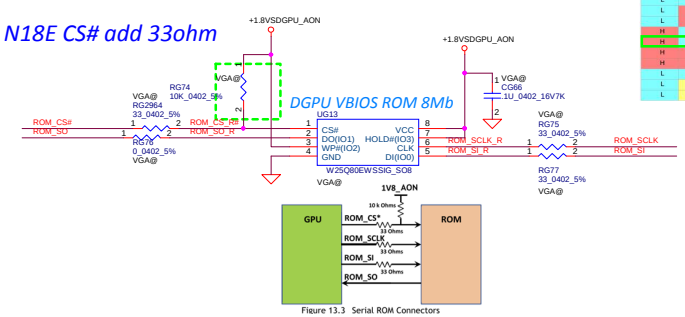
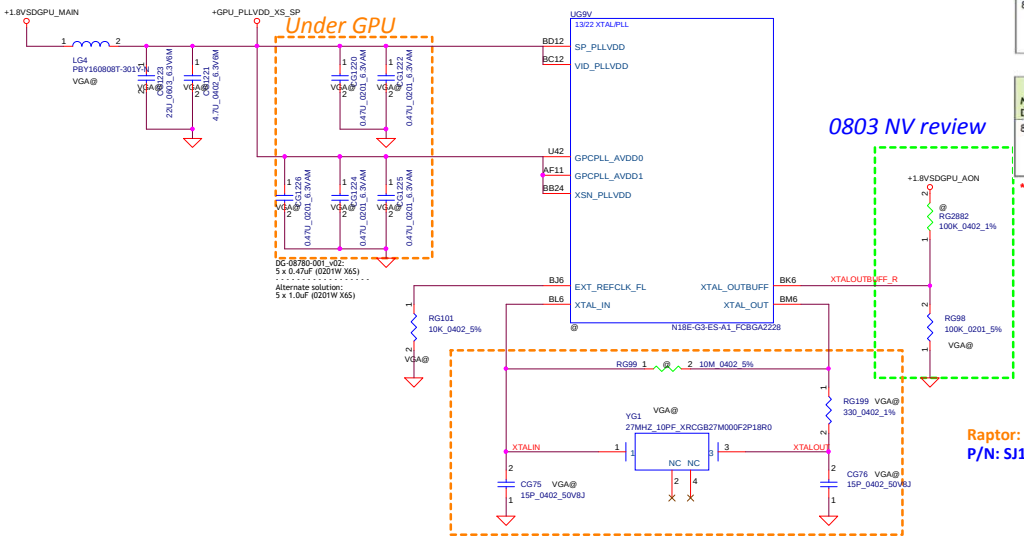


Figure 13.3 Serial ROM Connectors



0803 NV review

Raptor: change to follow 2018 VX SJ10000UI00
P/N: SJ10000UI00 (S CRYSTAL 27MHZ 10PF XRCGB27M000F2P18R0)

RVL-08928-001_v03	N18E G3	N18E G2	N18E G1	(MSB) Strap2	Strap1	(LSB) Strap0	(MSB) Strap5	Strap4	(LSB) Strap3	ROM_SO	ROM_SI	ROM_SCLK	Note
Micron MT61K256M32JE-14:A (0x1)	V	V	TBD	PD 100kOhm	PD 100kOhm	PU 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
Samsung K4Z80325BC-HC14 (0x0)	V	V	TBD	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
Hynix H56C8H24MJR-S2C (0x2)		V	TBD	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PD 100kOhm	PD 100kOhm	Support G-SYNC, GPU output eDP
TBD													

Note: GPU Discrete or Hybrid impact Strap3~Strap5 deisgn

RVL-08928-001_v04

Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Table 3. N18E-G0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[2]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

*DVS is required. WCK: TBD

Table 12.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	M	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

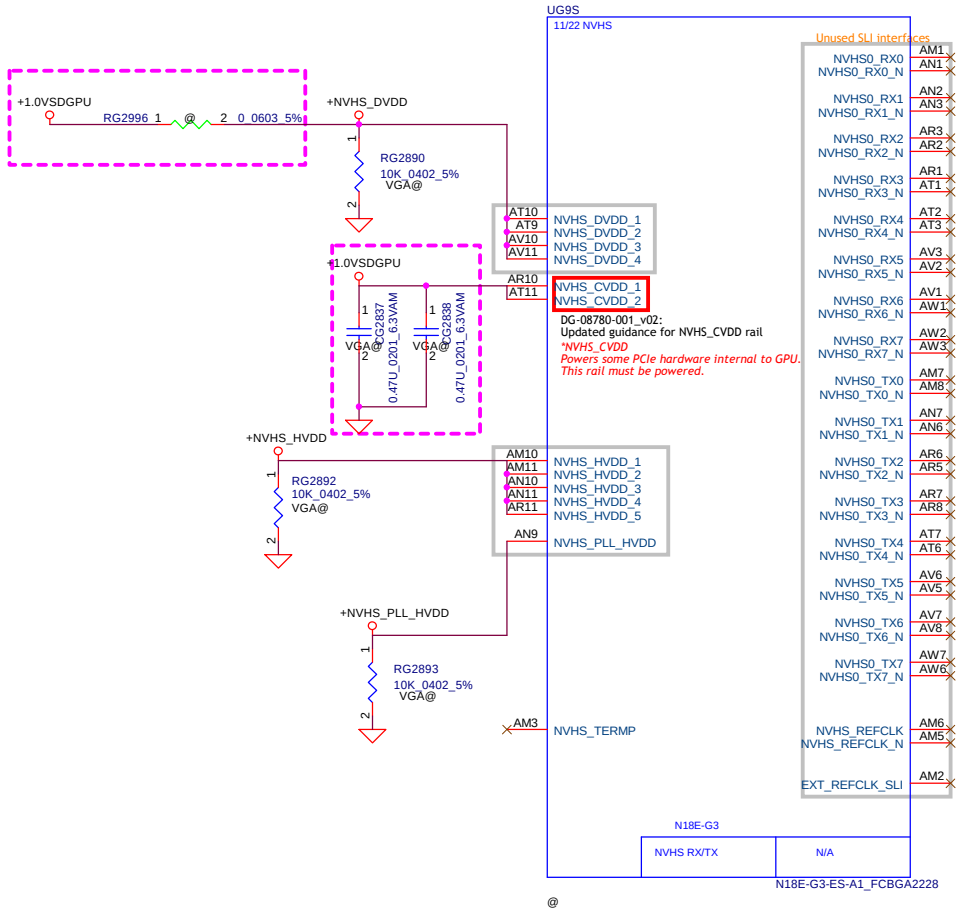
Compal Electronics, Inc.

Title: N18E-G3(7/8) Strap,ROM

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 31 of 100

Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, NVHS_PLL_HVDD rails to GND with 10K Resistor



Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.

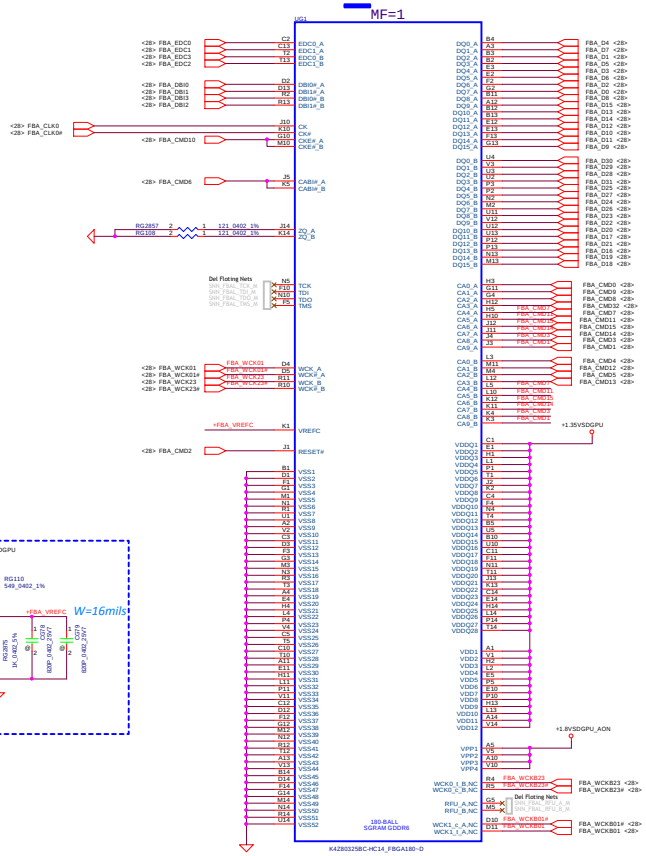
Title: **N18E-G3(8/8) NVLINK**

Size | Document Number: **EH78F M/B LA-G161PR01** | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 32 of 100

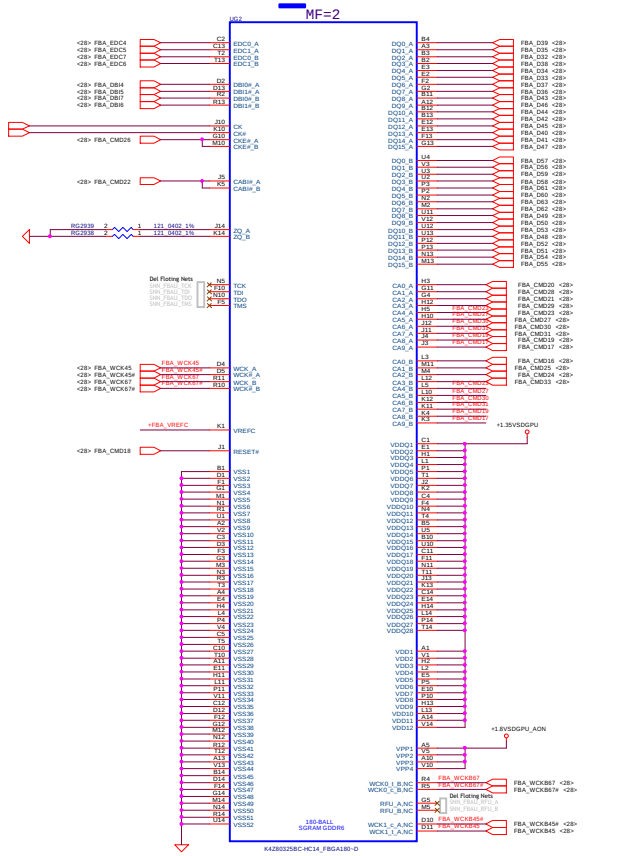
2_A#2

MF=1



1_A#1

MF=2



GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: -------	FBx_CMD16	Bytes 4, 5: ------- Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Byte 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------- Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: -------
FBx_CMD5	Bytes 0, 1: ------- Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: -------
FBx_CMD6	Bytes 0, 1: CA8I_A Bytes 2, 3: CA8I_B	FBx_CMD22	Bytes 4, 5: CA8I_A Bytes 6, 7: CA8I_B

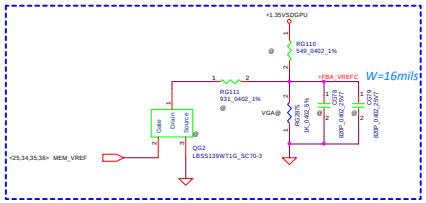
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: -------	FBx_CMD24	Bytes 4, 5: ------- Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: -------	FBx_CMD25	Bytes 4, 5: ------- Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------- Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: -------
FBx_CMD13	Bytes 0, 1: ------- Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: -------	FBx_CMD33	Bytes 4, 5: ------- Bytes 6, 7: CA3_B

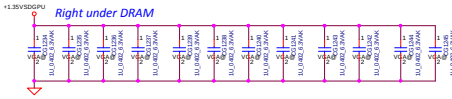
GB4B-256	GPU FB Channel 0 B ↑
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

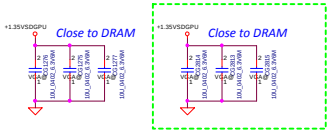
Checklist 0723 update
use GDDR6 internal, PD 1k to GND



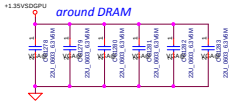
Right under DRAM



Close to DRAM

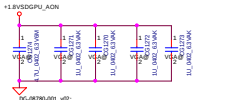


around DRAM



DG-08780-001_v02:
VDD/VDDQ Rail per DRAM device
NOTE 2:Alternatively, instead of using 36 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 18 capacitors of value 1.0uF (X6S, 0201W), one per VDD/VDDQ ball.

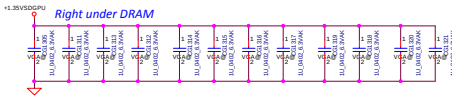
Close to VRAM:VDD/VDDQ



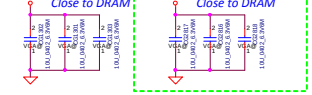
DG-08780-001_v02:
VPP Rail per DRAM device
NOTE 2:Alternatively, instead of using 4 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 4 capacitors of value 1.0 uF (X6S, 0201W), one per VPP ball.

Close to VRAM:

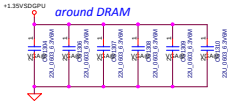
Right under DRAM



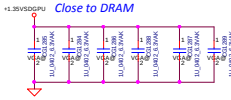
Close to DRAM

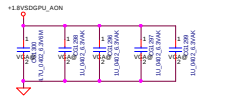


around DRAM



Close to DRAM





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Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

Title: *N18E-GDDR6_A*

Size: Document Number: *EH78F M/B LA-G161PR01* Rev: 0.1

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4_B#2

MF=1

3_B#1

MF=2

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: ------	FBx_CMD16	Bytes 4, 5: ------ Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------ Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: ------
FBx_CMD5	Bytes 0, 1: ------ Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: ------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: ------	FBx_CMD24	Bytes 4, 5: ------ Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: ------	FBx_CMD25	Bytes 4, 5: ------ Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------ Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: ------
FBx_CMD13	Bytes 0, 1: ------ Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: ------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [3]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: ------	FBx_CMD33	Bytes 4, 5: ------ Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Checklist 0723 update
use GDDR6 internal PD 1k to GND

W=16mils

Right under DRAM

Close to DRAM

around DRAM

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Title: N18E-GDDR6_B

Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1

Date: Friday, September 28, 2018 Sheet 34 of 105

6_C#2

MF=1

5_C#1

MF=2

Checklist 0723 update
use GDDR6 internal, PD 1k to GND

Right under DRAM

Close to DRAM

around DRAM

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD0	Bytes 0,1: CA0_A Bytes 2,3: -------	FBx_CMD16	Bytes 4,5: ------- Bytes 6,7: CA0_B
FBx_CMD1	Bytes 0,1: CA9_A Bytes 2,3: CA9_B	FBx_CMD17	Bytes 4,5: CA9_A Bytes 6,7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0,1: CA8_A Bytes 2,3: CA8_B	FBx_CMD19	Bytes 4,5: CA8_A Bytes 6,7: CA8_B
FBx_CMD4	Bytes 0,1: ------- Bytes 2,3: CA0_B	FBx_CMD20	Bytes 4,5: CA0_A Bytes 6,7: -------
FBx_CMD5	Bytes 0,1: ------- Bytes 2,3: CA2_B	FBx_CMD21	Bytes 4,5: CA2_A Bytes 6,7: -------
FBx_CMD6	Bytes 0,1: CABI_A Bytes 2,3: CABI_B	FBx_CMD22	Bytes 4,5: CABI_A Bytes 6,7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD7	Bytes 0,1: CA4_A Bytes 2,3: CA4_B	FBx_CMD23	Bytes 4,5: CA4_A Bytes 6,7: CA4_B
FBx_CMD8	Bytes 0,1: CA2_A Bytes 2,3: -------	FBx_CMD24	Bytes 4,5: ------- Bytes 6,7: CA2_B
FBx_CMD9	Bytes 0,1: CA1_A Bytes 2,3: -------	FBx_CMD25	Bytes 4,5: ------- Bytes 6,7: CA1_B
FBx_CMD10	Bytes 0,1: CKE*_A Bytes 2,3: CKE*_B	FBx_CMD26	Bytes 4,5: CKE*_A Bytes 6,7: CKE*_B
FBx_CMD11	Bytes 0,1: CA5_A Bytes 2,3: CA5_B	FBx_CMD27	Bytes 4,5: CA5_A Bytes 6,7: CA5_B
FBx_CMD12	Bytes 0,1: ------- Bytes 2,3: CA1_B	FBx_CMD28	Bytes 4,5: CA1_A Bytes 6,7: -------
FBx_CMD13	Bytes 0,1: ------- Bytes 2,3: CA3_B	FBx_CMD29	Bytes 4,5: CA3_A Bytes 6,7: -------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [1]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [1]]
FBx_CMD14	Bytes 0,1: CA7_A Bytes 2,3: CA7_B	FBx_CMD30	Bytes 4,5: CA6_A Bytes 6,7: CA6_B
FBx_CMD15	Bytes 0,1: CA6_A Bytes 2,3: CA6_B	FBx_CMD31	Bytes 4,5: CA7_A Bytes 6,7: CA7_B
FBx_CMD32	Bytes 0,1: CA3_A Bytes 2,3: -------	FBx_CMD33	Bytes 4,5: ------- Bytes 6,7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.			
Title: N18E-GDDR6_C			
Size:	Document Number: EH78F M/B LA-G161PR01		Rev: 0.1
Date: Friday, September 28, 2018		Sheet 35 of 105	

8_D#2

MF=1

7_D#1

MF=2

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD0	Bytes 0, 1: CA0_A Bytes 2, 3: ------	FBx_CMD16	Bytes 4, 5: ------ Bytes 6, 7: CA0_B
FBx_CMD1	Bytes 0, 1: CA9_A Bytes 2, 3: CA9_B	FBx_CMD17	Bytes 4, 5: CA9_A Bytes 6, 7: CA9_B
FBx_CMD2	Bytes 0-3: RST*	FBx_CMD18	Bytes 4-7: RST*
FBx_CMD3	Bytes 0, 1: CA8_A Bytes 2, 3: CA8_B	FBx_CMD19	Bytes 4, 5: CA8_A Bytes 6, 7: CA8_B
FBx_CMD4	Bytes 0, 1: ------ Bytes 2, 3: CA0_B	FBx_CMD20	Bytes 4, 5: CA0_A Bytes 6, 7: ------
FBx_CMD5	Bytes 0, 1: ------ Bytes 2, 3: CA2_B	FBx_CMD21	Bytes 4, 5: CA2_A Bytes 6, 7: ------
FBx_CMD6	Bytes 0, 1: CABI_A Bytes 2, 3: CABI_B	FBx_CMD22	Bytes 4, 5: CABI_A Bytes 6, 7: CABI_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD7	Bytes 0, 1: CA4_A Bytes 2, 3: CA4_B	FBx_CMD23	Bytes 4, 5: CA4_A Bytes 6, 7: CA4_B
FBx_CMD8	Bytes 0, 1: CA2_A Bytes 2, 3: ------	FBx_CMD24	Bytes 4, 5: ------ Bytes 6, 7: CA2_B
FBx_CMD9	Bytes 0, 1: CA1_A Bytes 2, 3: ------	FBx_CMD25	Bytes 4, 5: ------ Bytes 6, 7: CA1_B
FBx_CMD10	Bytes 0, 1: CKE*_A Bytes 2, 3: CKE*_B	FBx_CMD26	Bytes 4, 5: CKE*_A Bytes 6, 7: CKE*_B
FBx_CMD11	Bytes 0, 1: CA5_A Bytes 2, 3: CA5_B	FBx_CMD27	Bytes 4, 5: CA5_A Bytes 6, 7: CA5_B
FBx_CMD12	Bytes 0, 1: ------ Bytes 2, 3: CA1_B	FBx_CMD28	Bytes 4, 5: CA1_A Bytes 6, 7: ------
FBx_CMD13	Bytes 0, 1: ------ Bytes 2, 3: CA3_B	FBx_CMD29	Bytes 4, 5: CA3_A Bytes 6, 7: ------

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 0,1,2,3 [2]]	GB4B-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7 [2]]
FBx_CMD14	Bytes 0, 1: CA7_A Bytes 2, 3: CA7_B	FBx_CMD30	Bytes 4, 5: CA6_A Bytes 6, 7: CA6_B
FBx_CMD15	Bytes 0, 1: CA6_A Bytes 2, 3: CA6_B	FBx_CMD31	Bytes 4, 5: CA7_A Bytes 6, 7: CA7_B
FBx_CMD32	Bytes 0, 1: CA3_A Bytes 2, 3: ------	FBx_CMD33	Bytes 4, 5: ------ Bytes 6, 7: CA3_B

GB4B-256	GPU FB Channel 0 B 1
FBx_CMD34	DEBUG0[1]
FBx_CMD35	DEBUG1[1]

Note:
1. GPU debug pins; not connected to DRAM.
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

Checklist 0723 update
use GDDR6 internal, PD 1k to GND

W=16mils

Right under DRAM

Close to DRAM

around DRAM

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

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Compal Electronics, Inc.

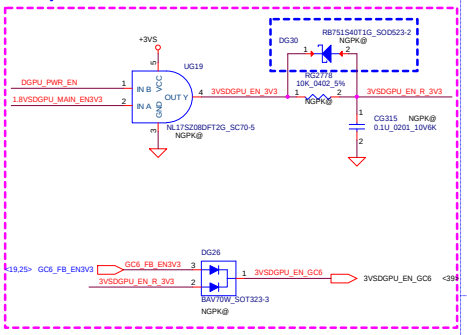
Title: N18E-GDDR6_D

Size: Document Number: EH78F M/B LA-G161PR01 Rev: 0.1

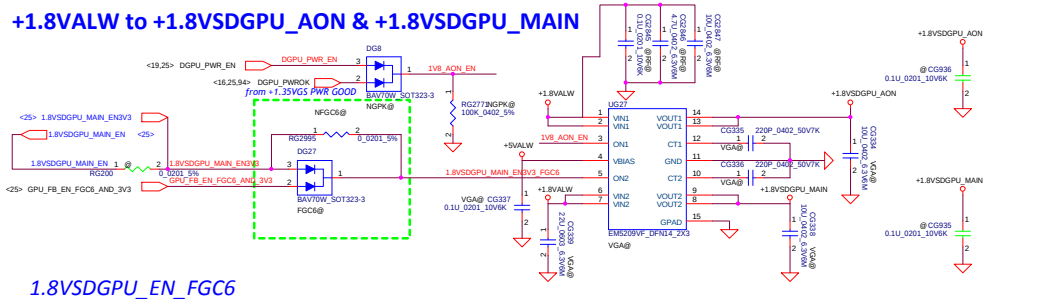
Date: Friday, September 28, 2018 Sheet 35 of 105

No Reserved NV Sequence IC: SILEGO GreenPAK
SA0000B9H00, S IC SLG4U41989VTR STQFN 20P LOGIC SOC

+3VS/+3VSDGPU

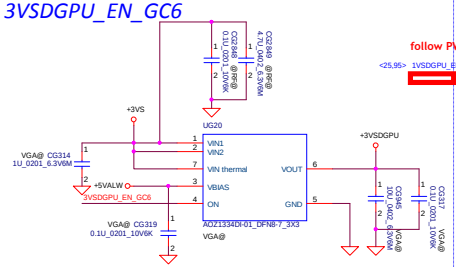


+1.8VALW to +1.8VSDGPU_AON & +1.8VSDGPU_MAIN

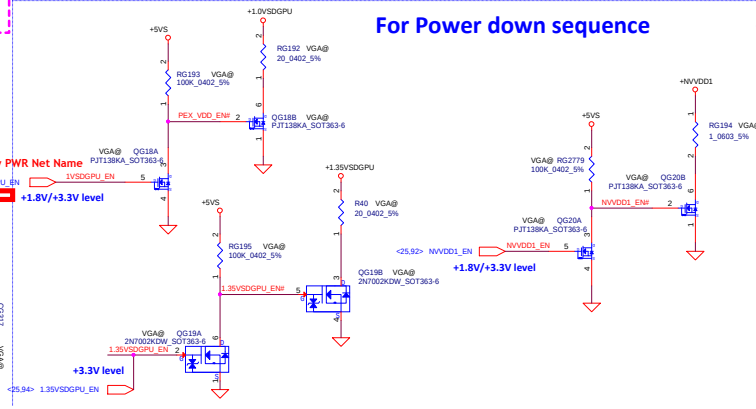


1.8VSDGPU_EN_FGC6

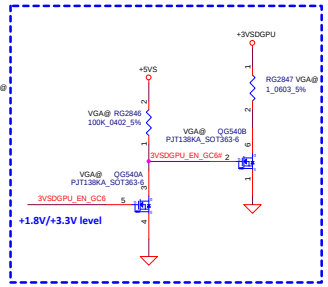
3VSDGPU_EN_GC6



For Power down sequence

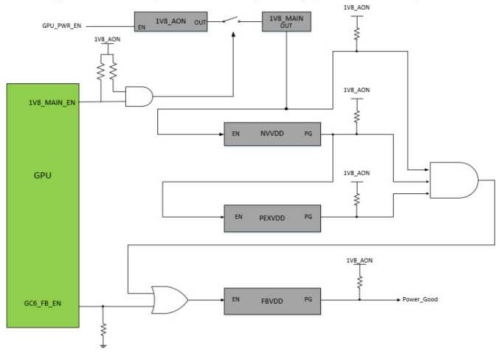


+3VSD_GPU discharge if need

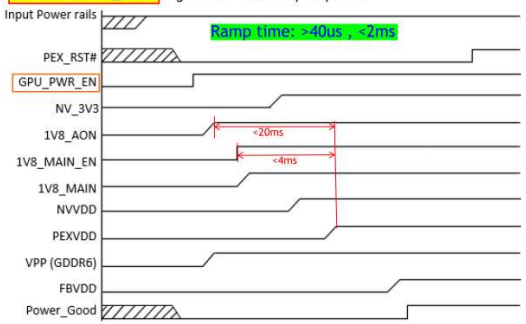


DG-08780-001_v02

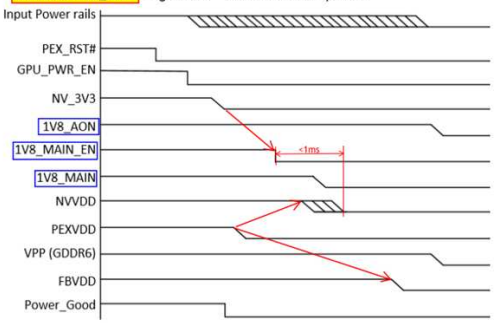
Figure 5.5 Example of Power Sequencing (GPU rails shown)



DG-08780-001_v02 Figure 5.6 Power-Up Sequence



DG-08780-001_v02 Figure 5.7 Power-Down Sequence



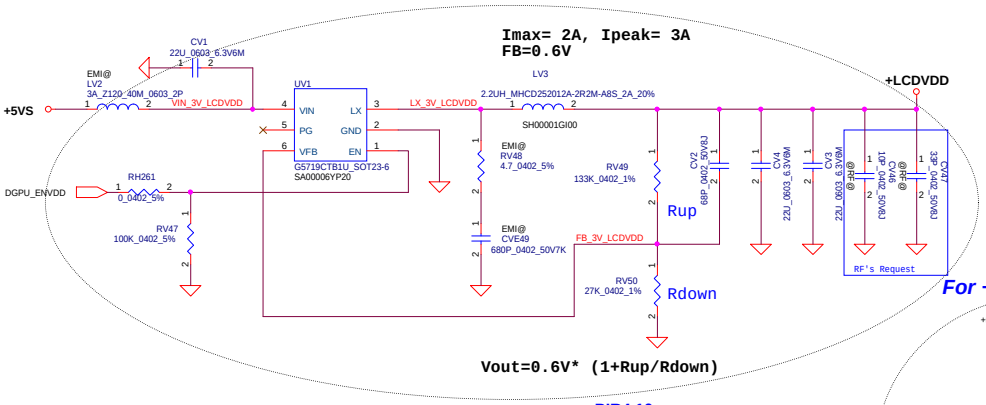
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/15

Compal Electronics, Inc.

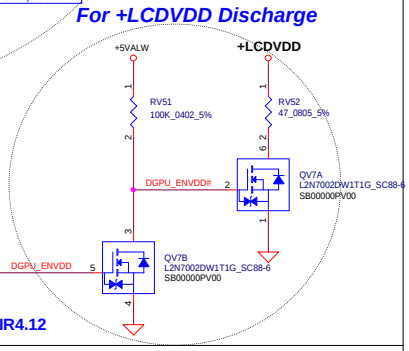
Title: N18E-GPU Power control

Size | Document Number: EH78F M/B LA-G161PR01 | Rev: 0.1

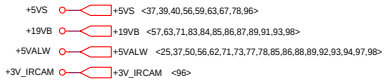
Date: Friday, September 28, 2018 | Sheet 37 of 100

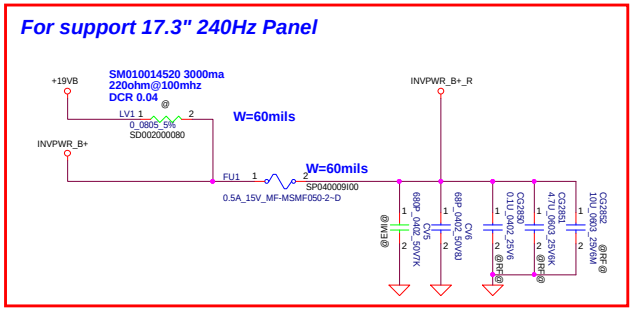


PIR4.10



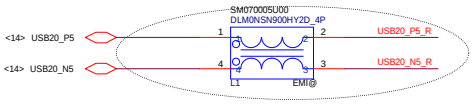
PIR4.12

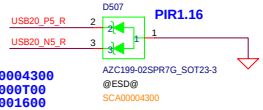




Camera

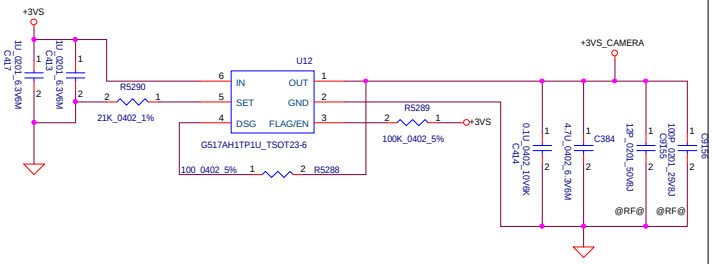
PIR4.9



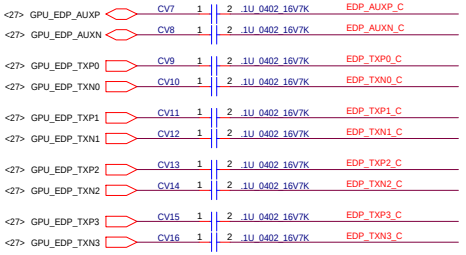


PIR1.16

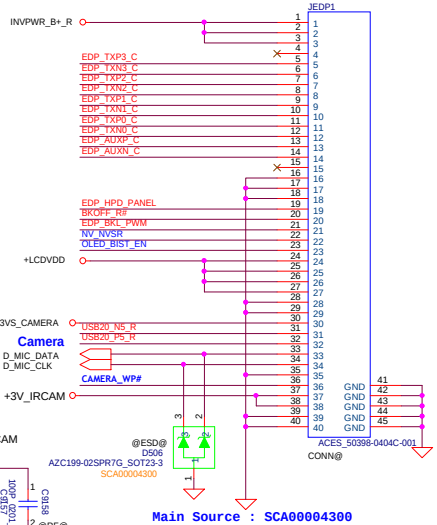
Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SC600001600



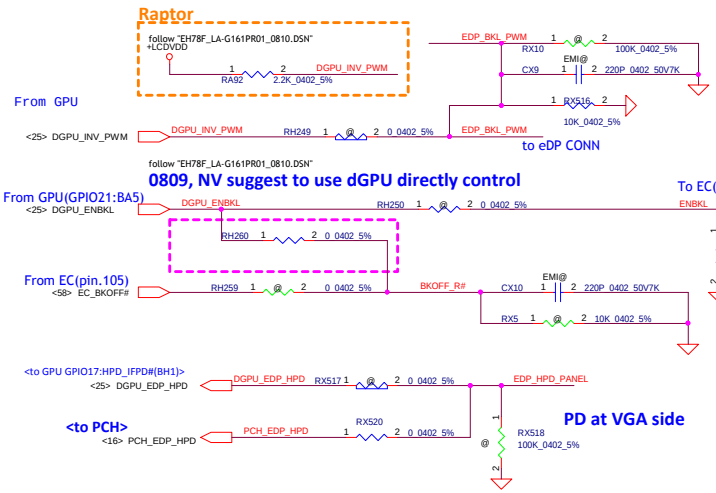
from GPU(IFP#D)

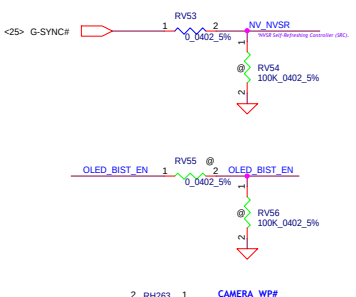


eDP



Raptor





Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
	LA-F842P	v0.1

Date: Friday, September 28, 2018 | Sheet 38 of 100

0 = GPIO mode (I2C disabled)

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

bit[2]H:1

bit[1]L:0

bit[1]L:0

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

Copy from "EH78F_LA-G161PR01_0810_P.41"

Simplified Schematics

DP only

DP only

Need Check

Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SC600001600

DP++ and isolated circuit

minDP HPD

4-bits 1-of-2 FET MUX

0:DP
1:HDMI

OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1 (0:DP)
L	H	B2	A=B2 (1:HDMI)
H	X	Z	NC

0921 change souce to +3VALW, CTRL to SUSP#

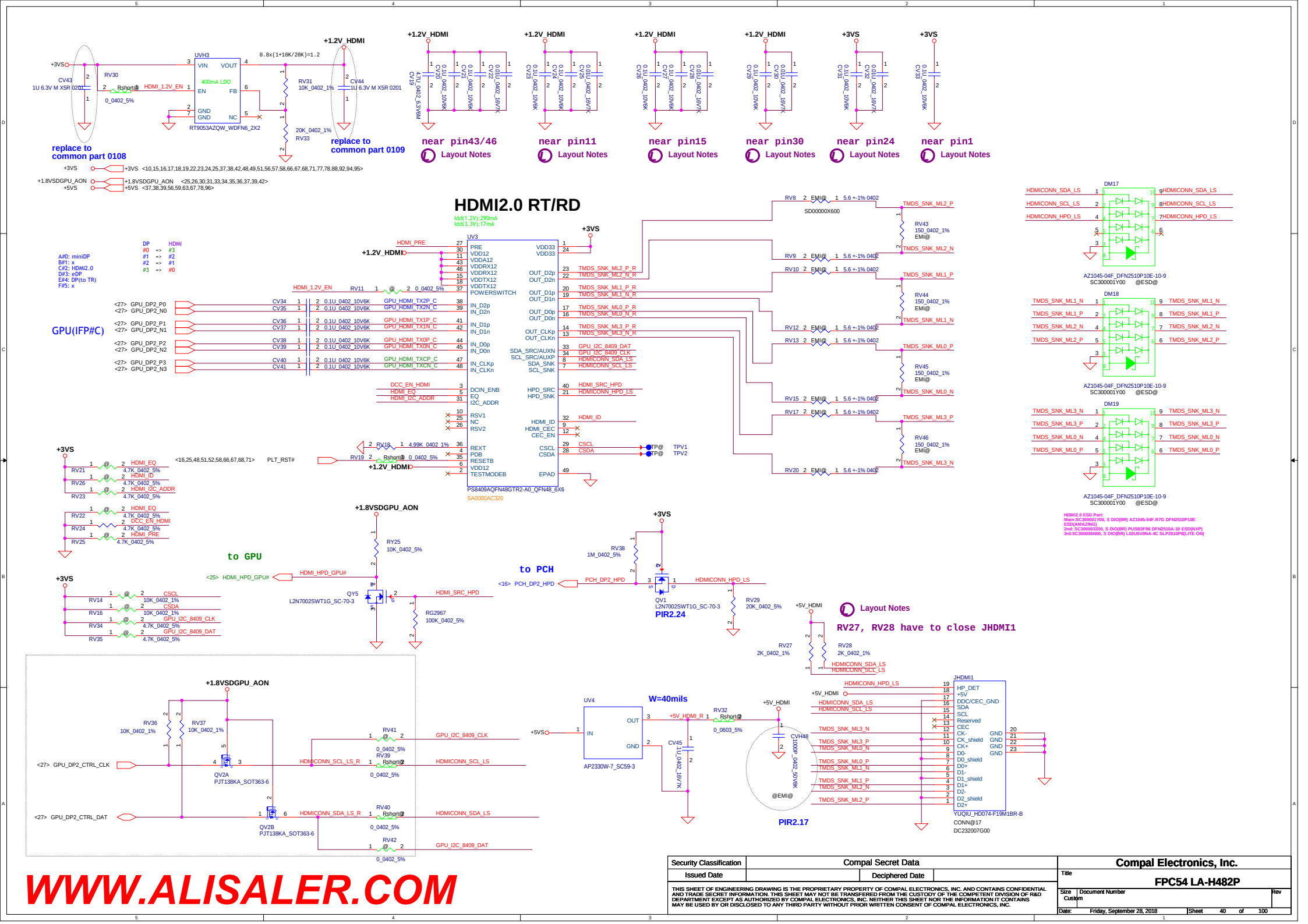
Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2018/09/01

Compal Electronics, Inc.

Title: mDP redriver(TUSB546)

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 39 of 100


+3VS
UVH3
VIN
VOUT
400mA LDO
EN
FB
GND
NC
RT9053AZQW_WDFN6_2X2
RV30
HDMI_1.2V_EN
0_0402_5%
0.8x(1+10K/20K)=1.2
+1.2V_HDMI
RV31
10K_0402_1%
20K_0402_1%
RV33
CV44
1U 6.3V M X5R 0201
CV43
1U 6.3V M X5R 0201
replace to common part 0108
replace to common part 0109
+1.8VSDGPU_AON
+5VS
near pin43/46
near pin11
near pin15
near pin30
near pin24
near pin1
Layout Notes
HDMI2.0 RT/RD
Idd(1.2V):290mA
Idd(3.3V):17mA
A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x
DP HDMI
#0 => #3
#1 => #2
#2 => #1
#3 => #0
GPU(IFP#C)
UV3
PS8409AQFN48GTR2-A0_QFN48_6X6
SA0000AC320
HDMI_PRE
HDMI_1.2V_EN
DCC_EN_HDMI
HDMI_EQ
HDMI_I2C_ADDR
HDMI_ID
HDMI_SRC_HPD
HDMI_HPD_GPU#
PLT_RST#
to GPU
to PCH
PCH_DP2_HPD
HDMICONN_HPD_LS
QV1
L2N7002SWT1G_SC-70-3
PIR2.24
RV27, RV28 have to close JHDMI1
W=40mils
UV4
AP2330W-7_SC59-3
QV2A
QV2B
PJT138KA_SOT363-6
PIR2.17
JHDMI1
YUQIU_HD074-F19M1BR-B
CONN@17
DC232007G00
DM17
DM18
DM19
AZ1045-04F_DFN2510P10E-10-9
SC300001Y00 @ESD@
HDMI2.0 ESD Part:
Main:SC300001Y00, S DIO(BR) AZ1045-04F.R7G DFN2510P10E ESD(AMAZING)
2nd: SC300003Z00, S DIO(BR) PUSB3F9E DFN2510A-10 ESD(NXP)
3rd:SC300005N00, S DIO(BR) L02U5V0NA-4C SLP2510P8(LITE ON)
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Compal Secret Data
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Deciphered Date
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Size Custom
Document Number
Rev
Date: Friday, September 28, 2018
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Issued Date	2017/07/24	Deciphered Date	2018/08/24

Title	TBD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 41 of 100		

1012 check Ti if need

+3VS — LT39 (1–2) — +3V_TYPEC_DP

PBY160808T-600Y-N_2P

TBT@

+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,48,49,51,56,57,58,66,67,68,71,77,78,88,92,94,95>

0 = GPIO mode (I2C disabled)

I2C_EN_TBT — RT8441 @ 2 1K_0402_5% — +3V_TYPEC_DP

RT8461 2 1K_0402_5% — TBT@

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

CTL1_TBT_HPDIN — RT8431 TBT@ 2 1K_0402_5% — +3V_TYPEC_DP
bit[2]H:1
RT8451 @ 2 1K_0402_5%

CTL0_TBT_SDA — RT9001 @ 2 1K_0402_5% — +3V_TYPEC_DP
bit[1]L:0
RT8471 2 1K_0402_5% — TBT@

FLIP_TBT_CLK — RT8481 @ 2 1K_0402_5% — +3V_TYPEC_DP
bit[1]L:0
RT8491 TBT@ 2 1K_0402_5%

Copy from "EH78F_LA-G161PR01_0810_P.42"

DPEQ0_A1_TBT — RT8501 TBT@ 2 1K_0402_5% — +3V_TYPEC_DP
RT8511 @ 2 1K_0402_5%

DPEQ1_TBT — RT8521 @ 2 1K_0402_5% — +3V_TYPEC_DP
RT8531 TBT@ 2 1K_0402_5%

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

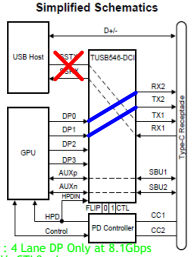
A0_TBT — RT8541 @ 2 1K_0402_5% — +3V_TYPEC_DP
RT8551 @ 2 1K_0402_5%

SSEQ0,SSEQ1 : USB receiver equalizer gain
for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

+3V_TYPEC_DP

CT305 1 10U_0402_6.3V6M 2 TBT@
CT306 1 @ 1U_0201_6.3V6K 2
CT307 1 0.1U_0201_10V6K 2 TBT@
CT320 1 0.1U_0201_10V6K 2 TBT@
CT308 1 0.1U_0201_10V6K 2 TBT@
CT309 1 0.1U_0201_10V6K 2 TBT@

Simplified Schematics



to TR sink port#1

from GPU(IFP#E)

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

UT11 660mW : 4 Lane DP Only at 8.1Gbps
CTL1 = H; CTL0 = L

VCC (1, 6, 20, 28)

<26> DP4_TXP0 — CT310 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP0_C — DP0p (9)
<26> DP4_TXN0 — CT311 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN0_C — DP0n (10)

<26> DP4_TXP1 — CT312 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP1_C — DP1p (12)
<26> DP4_TXN1 — CT313 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN1_C — DP1n (13)

<26> DP4_TXP2 — CT314 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP2_C — DP2p (15)
<26> DP4_TXN2 — CT315 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN2_C — DP2n (16)

<26> DP4_TXP3 — CT316 TBT@ 1 2 0.1U_0201_10V6K DP4_TXP3_C — DP3p (18)
<26> DP4_TXN3 — CT317 TBT@ 1 2 0.1U_0201_10V6K DP4_TXN3_C — DP3n (19)

<48> TRP_N3 — RX1n (31)
<48> TRP_P3 — RX1p (30)

<48> TRP_N0 — RX2n (39)
<48> TRP_P0 — RX2p (40)

DP only
Set to "4 Lane DP-No Flip"

EQ1 (35) TH41 TP@
EQ0 (38) TH40 TP@
I2C_EN (17) L:0 I2C_EN_TBT
DPEQ1 (2) DPEQ1_TBT
DPEQ0/A1 (14) DPEQ0_A1_TBT
SSEQ1 (3) TH42 TP@
SSEQ0/A0 (11) A0_TBT

bit[0] FLIP/SCL (21) L:0 FLIP_TBT_CLK
bit[1] CTL0/SDA (22) L:0 CTL0_TBT_SDA
bit[2] CTL1 (23) H:1 CTL1_TBT_HPDIN

TX1n (34) TRP_N2 <48>
TX1p (33) TRP_P2 <48>
TX2p (37) TRP_P1 <48>
TX2n (36) TRP_N1 <48>

DP only
SSTXp (8)
SSTXn (7)
SSRXp (5)
SSRXn (4)

+3V_TYPEC_DP — RT856 TBT@ 1 2 4.7K_0402_5%
RT857 @ 1 2 4.7K_0402_5%

RECVD1 (29) →CAD_SNK
RECVD2 (32) →HPDIN

<16,48> TBT_DP0_HPD — RT858 1 TBT@ 2 0_0402_5% TBT_DP0_HPD_R (41)

SBU1 (27) TH43 TP@
SBU2 (26) TH44 TP@

AUXp (24) RD_DP4_AUXP_C 0.1U_0201_10V6K TBT@ CT318 1 — DP4_AUXP <26,48>
AUXn (25) RD_DP4_AUXN_C 0.1U_0201_10V6K TBT@ CT319 1 — DP4_AUXN <26,48>

PAD

TUSB546_QFN40_4X6
TBT@

+1.8VSDGPU_AON — R810 TBT@ 10K_0402_5%

<25> GPU_DP4_HPD#

A#0: miniDP
B#1: x
C#2: HDMI2.0
D#3: eDP
E#4: DP(to TR)
F#5: x

QV97 L2N7002LT1G_SOT23-3 TBT@

TBT_DP0_HPD — R397 100K_0402_5% TBT@

+3V_TYPEC_DP — RT859 TBT@ 100K_0402_5%
RD_DP4_AUXN_C
RD_DP4_AUXP_C
RT860 TBT@ 100K_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2017/11/23	Deciphered Date	2017/12/31

Compal Electronics, Inc.

Title: TBT DP redriver

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 42 of 100

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Title	TBD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 43 of 100		

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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 44 of 100		

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Title: TBD		
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
Date: Friday, September 28, 2018	Sheet 45 of 100	

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Title	TBD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
Date: Friday, September 28, 2018	Sheet 46 of 100		

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Title	TBD	
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
Date: Friday, September 28, 2018	Sheet 47 of 100	

Copy from "DDX03_LS-F262PR02_0309A"

Titan Ridge SP (Single Port) - High Speed (CIO, USB and PCIe) Parts

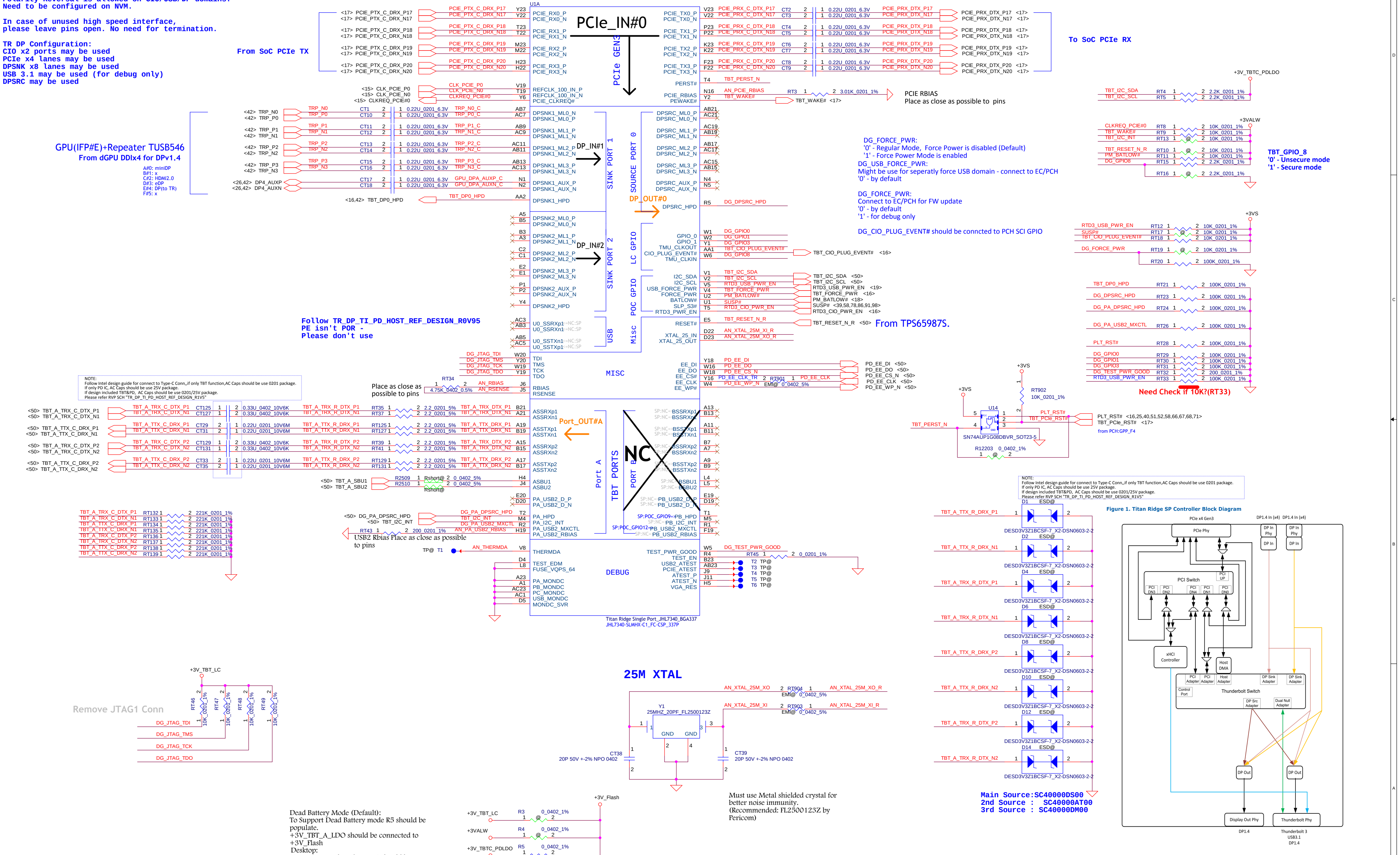
"559414-manufacturing-test-thunderbolt-mas-rev-2-3-from-9-21-2017"
CNL supports HBR3 (8.1G), but no DSC (so only DP1.3). DP1.4 supported in TR, but only via discrete GFX silicon w/ DP1.4 logic

Titan Ridge
Dual Port(TR-DP):JHL7540
Single Port(TR-SP):JHL7340

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface,
please leave pins open. No need for termination.

TR DP Configuration:
CIO x2 ports may be used
PCIe x4 lanes may be used
DPSNK x8 lanes may be used
USB 3.1 may be used (for debug only)
DPSRC may be used



NOTE:
Follow Intel design guide for connect to Type-C Conn.,if only TBT function,AC Caps should be use 0201 package.
If only PD IC, AC Caps should be use 25V package.
If design included TBT&PD, AC Caps should be use 0201/25V package.
Please refer RVP SCH "TR_DP_TI_PD_HOST_REF_DESIGN_R1V5"

Must use Metal shielded crystal for better noise immunity.
(Recommended: FL2500123Z by Pericom)

Dead Battery Mode (Default):
To Support Dead Battery mode R5 should be populate.
+3V_TBT_A_LDO should be connected to +3V_Flash
Desktop:
To support Desktop/RVP, R4 should be populate.
+3VALW should be connected to +3V_Flash

Security Classification	Compal Secret Data		
Issued Date	2017/06/26	Deciphered Date	2018/06/26

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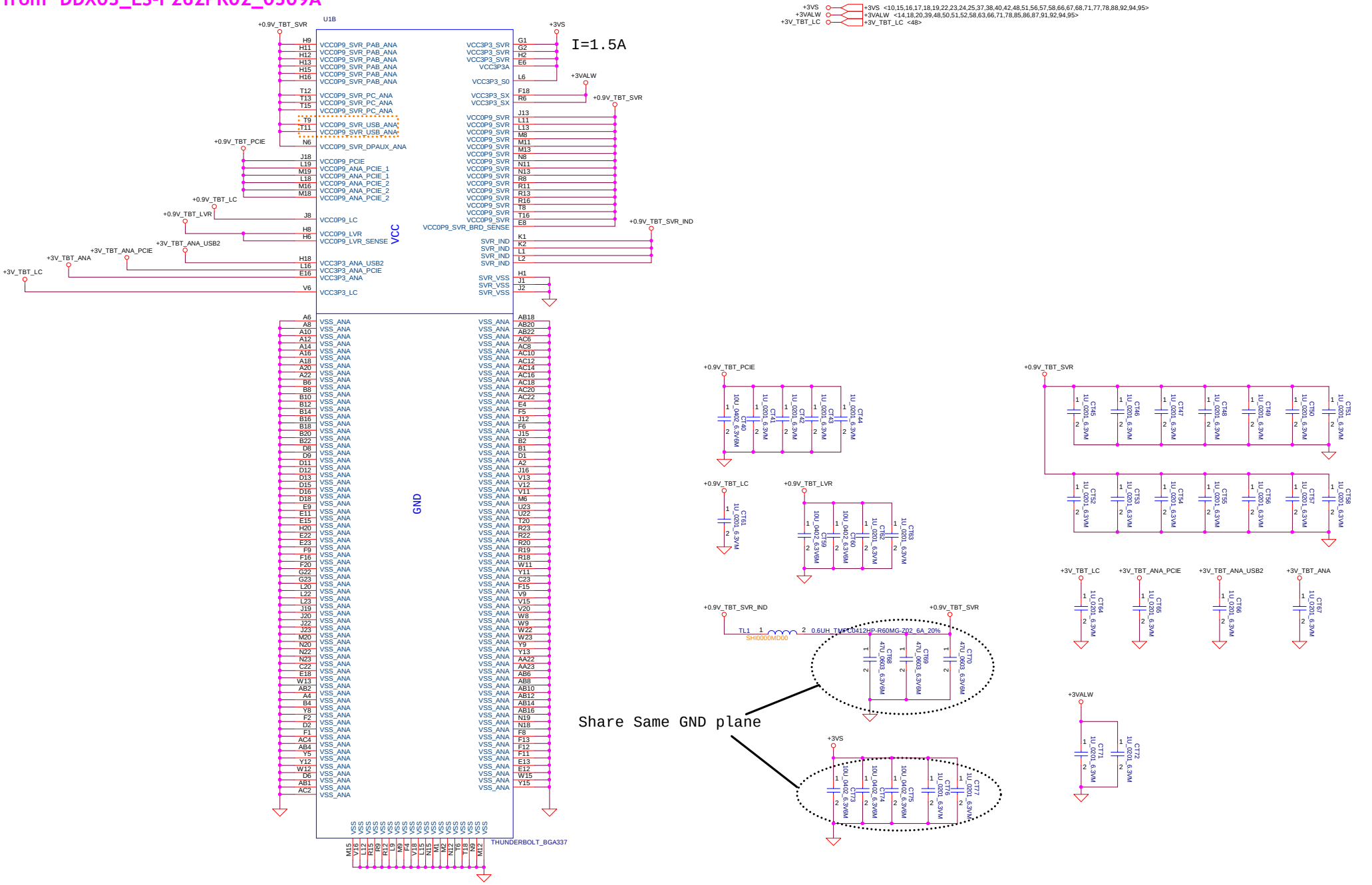
Compal Electronics, Inc.

Title: P04-Thunderbolt Titanrid (1/2)

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 48 of 100



Share Same GND plane

Security Classification	Compal Secret Data		
Issued Date	2017/06/26	Deciphered Date	2018/06/26

Compal Electronics, Inc.

Title: P05-Thunderbolt Titanrid (2/2)

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 49 of 100

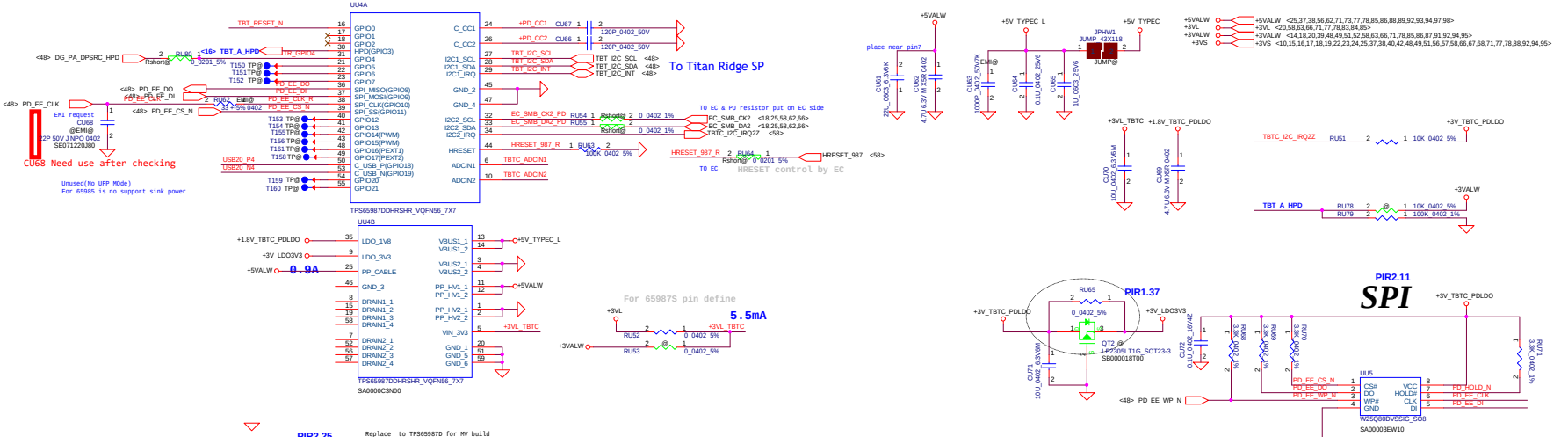


Table 8. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	0	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 9. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 7. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

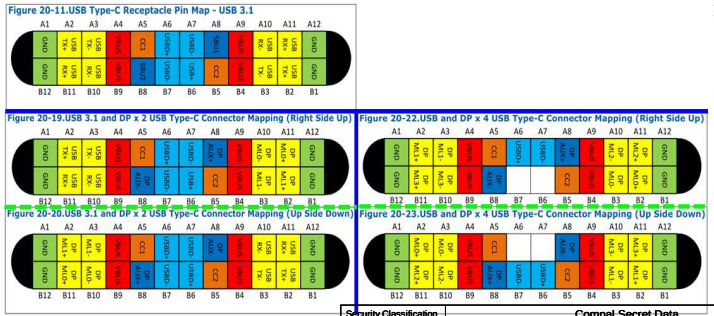
Figure 37. I²C Address Divider

Table 10 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 10. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed MIN and MAX values.



Security Classification	Compal Secret Data	
Issued Date	2017/03/07	Deciphered Date 2018/03/07

Compal Electronics, Inc.

Title: Type-C PORT3-DC IN

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

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+3VALW <14,18,20,39,48,49,50,52,58,63,66,71,78,85,86,87,91,92,94,95>

+LAN_VDD_3V3 Rising time (10~90%)
need>0.5mS and <100mS

JUMP@ JPHW2
JUMP_43X79
+3VALW
@ UL2
VIN VOUT GND EN /OC
+LAN_VDD_3V3
@ CL28 1500P_0402_50V7K
<59> LAN_PWR_EN
G524B1T11U_SOT23-5
SA00006Y800

CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

+LAN_REGOUT
LL2 2.2UH_MHCD252012A-2R2M-A8S_2A_20% SH00001GI00
PIR1.15
CL8 4.7U_0402_6.3V6M
CL23 0.1U_0201_10V6K
CL11 CL12 CL13 CL14 CL15 CL26 CL27 0.1U_0201_10V6K
+LAN_VDD_1V0
1U 6.3V M X5R 0201

+LAN_VDD_3V3
@ CL20 4.7U 6.3V M X5R 0402
@ CL19 4.7U_0402_6.3V6M
CL9 4.7U_0402_6.3V6M
CL5 0.1U_0201_10V6K
0.1U_0201_10V6K

+LAN_VDD_3V3
CL10 4.7U 6.3V M X5R 0402
CL16 0.1U_0201_10V6K

CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32
CL10& CL16 close to UL1: Pin 23

Note: CL19/CL20 are reserved for surge test

+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil

UL1
LAN_MDIP0 LAN_MDIN0 LAN_MDIP1 LAN_MDIN1 LAN_MDIP2 LAN_MDIN2 LAN_MDIP3 LAN_MDIN3
MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3
CLKREQB PERSTB REFCLK_P REFCLK_N HSIP HSIN HSOP HSON RSET
AVDD10 AVDD10 AVDD10 DVDD10 AVDD33 AVDD33 VDDREG REGOUT LANWAKEB ISOLATEB LED0 LED1/GPO LED2 CKXTAL1 CKXTAL2 GND
RTL8118ASH-CG_QFN32_4X4
SA0000B9F00
(SA000084T00) RTL8111HSH-CG Giga

<15> CLKREQ_PCIE#5
<16,25,40,48,52,58,66,67,68,71> PLT_RST#
CLKREQ_PCIE#5_R
PIR3.3
<15> CLK_PCIE_P5
<15> CLK_PCIE_N5
<17> PCIE_PTX_C_DRX_P14
<17> PCIE_PTX_C_DRX_N14
<17> PCIE_PRX_DTX_P14
<17> PCIE_PRX_DTX_N14
CR11 CR13 0.1U_0402_10V7K
RL6 Rshort@ 0_0201_5%
RL11 2.49K_0402_1%
RSET
+LAN_VDD_1V0
+LAN_VDD_3V3
RL15 10K_0402_5%
EC_PME# <58>
EC_LAN_ISOLATEB#_R
LAN_ACT#
LED1/GPO
LAN_LINK#
RL56 4.7K_0402_5%
RL57 0_0402_5%
XTLO
PIR2.26

EC_LAN_ISOLATEB#_R
1K_0402_5% RM6 +3VS
RM11 15K_0402_5%

SP050005L00 Footprint
TSL1
+V_DAC LAN_MDIP3 LAN_MDIN3 LAN_MDIP2 LAN_MDIN2 LAN_MDIP1 LAN_MDIN1 LAN_MDIP0 LAN_MDIN0
TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
NCT1 MX1+ MX1- NCT2 MX2+ MX2- NCT3 MX3+ MX3- NCT4 MX4+ MX4-
LANGND XGND
RJ45_TX3+ RJ45_TX3- RJ45_TX2+ RJ45_TX2- RJ45_RX1+ RJ45_RX1- RJ45_TX0+ RJ45_TX0-
RL55 Rshort@ 0_0805_5%
MCT1 MCT2 MCT3 MCT4 RC935 RC936 RC937 RC938 75_0402_1%
BOTH_GST5009-E-LF
SP050006B10
11/22 使用SP050006B10
CL1 0.01U_0402_16V7K
@EMI@ CL4 0.1U_0402_16V7K
CL2 SE167100J80 10P_1808_3KV
CL3 EMI@ 120P_0402_50V8J
ESD@ DL1 AZC199-02SPR7G_SOT23-3 SCA00004300
LANGND
PIR1.16

Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SC600001600

XTLI XTLO
RL7 1M_0402_5%
YL1 SJ10000UP00 25MHZ_10PF_XRCGB25M000F2P34R0
NC NC
CL25 CL27 10P_0402_50V8J

DM12
LAN_MDIN1 LAN_MDIN0 LAN_MDIP0 LAN_MDIP1
I/O4 I/O2 I/O3 I/O1 VDD GND
+LAN_VDD_3V3
powe rail need to check
AZC099-04S.R7G_SOT23-6
SC300001G00
@ESD@
PIR1.16

DM13
LAN_MDIN3 LAN_MDIN2 LAN_MDIP2 LAN_MDIP3
I/O4 I/O2 I/O3 I/O1 VDD GND
+LAN_VDD_3V3
powe rail need to check
AZC099-04S.R7G_SOT23-6
SC300001G00
@ESD@
PIR1.16

Main Source: SC300006000
2nd Source : SC300001G00
3rd Source : SC300003S00

JRJ45
RJ45_TX3- RJ45_TX3+ RJ45_RX1- RJ45_TX2- RJ45_TX2+ RJ45_RX1+ RJ45_TX0- RJ45_TX0+
PR4- PR4+ PR2- PR3- PR3+ PR2+ PR1- PR1+
GND GND GND GND
SANTA_130460-3400
CONN@
LANGND
PIR1.40

+LAN_VDD_3V3
Side Light
Vf=1.9~2.4V
SC5110UD000
LED4
HT-110UD_1204
LAN_ACT# RL31 220_0402_5% LAN_ACT#_R
BOT:Amber
LAN_LINK# RL30 20_0402_5% LAN_LINK#_R
TOP:White
LED5
B2591BS-05P-000132_WHITE
SC50000KT00
DM16 AZC199-02SPR7G_SOT23-3 @ESD@ SCA00004300
Side Light
Vf=2.9~3.15V
PIR2.21
PIR1.16
PIR1.44

Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SC600001600

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: LAN 8151/8166_ CR RTS5238

Size	Document Number	Rev
	FPC54 LA-H482P	v0.1

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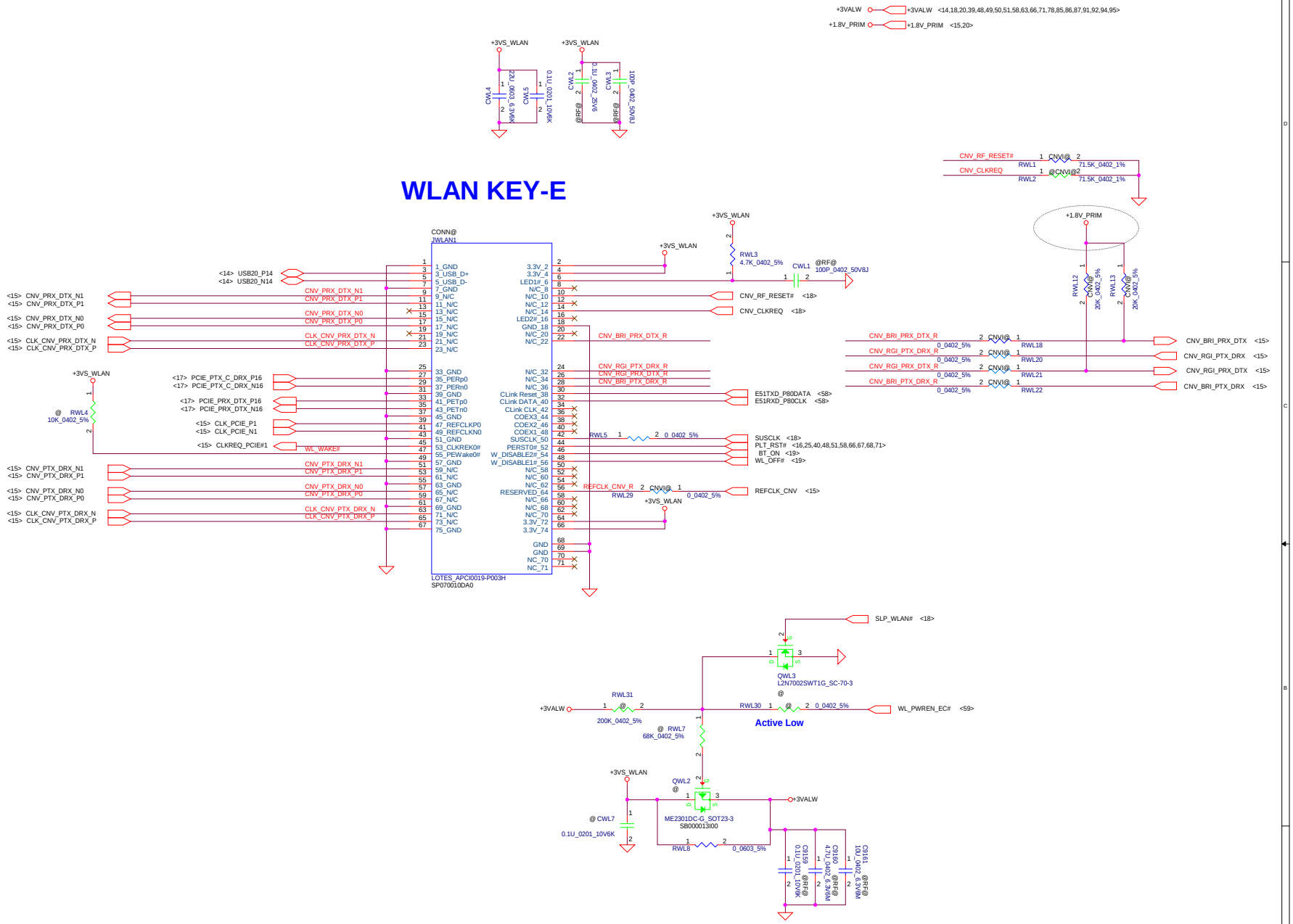
WLAN KEY-E



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: **WLAN-BT**

Size	Document Number	Rev
	FPC54 LA-H482P	v0.1

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Issued Date	2017/07/24	Deciphered Date	2018/08/24

Title	TBD		
Size: Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
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Title: TBD		
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
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Title: TBD		
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
Date: Friday, September 28, 2018	Sheet 55 of 100	

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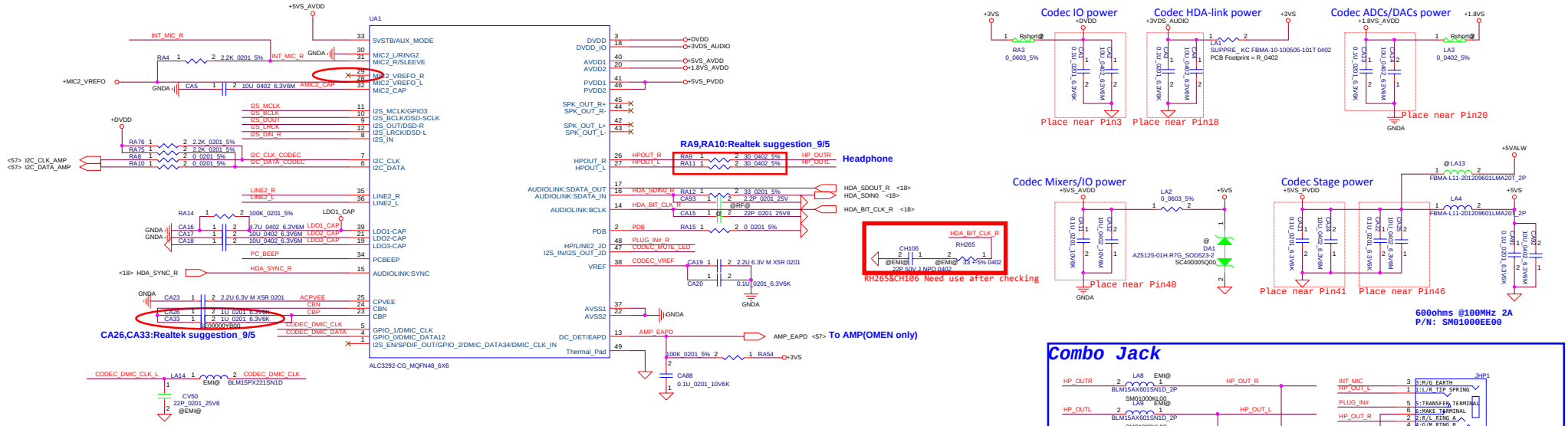
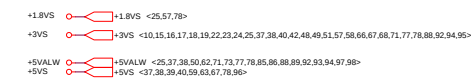
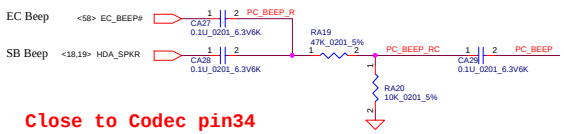




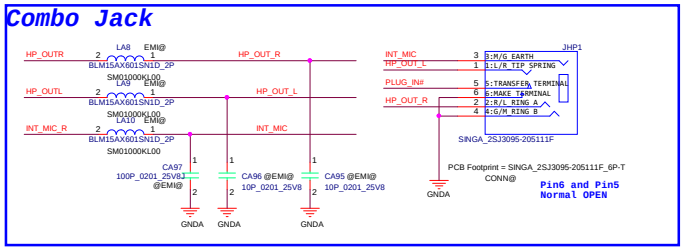
PC Beep



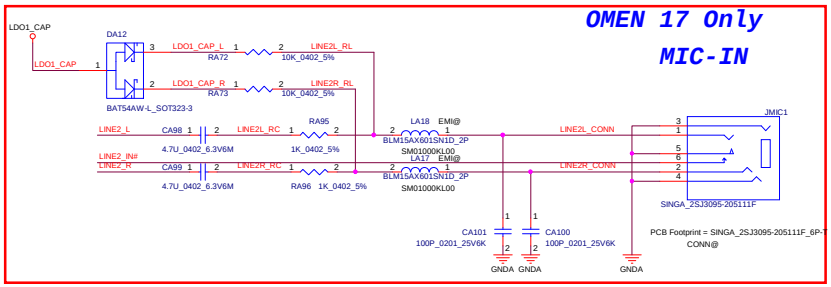
Jack Detect

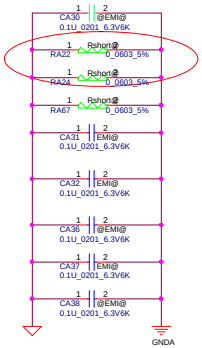
	RA16	RA17	RA74
OMEN_15	@	0_ohm	@
OMEN_17	100K	200K	100K

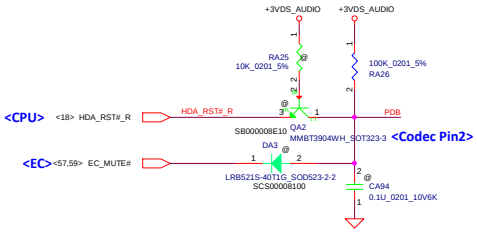
Combo Jack

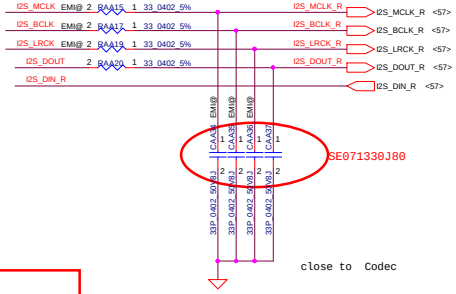


OMEN 17 Only MIC-IN









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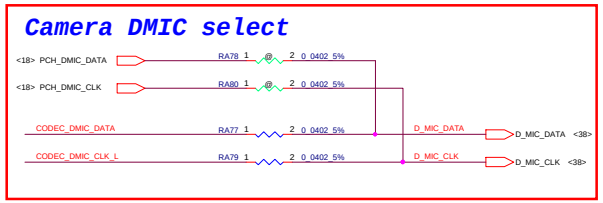

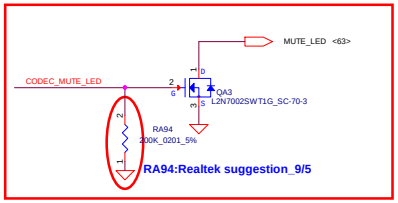

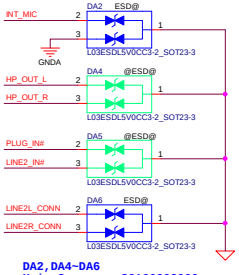

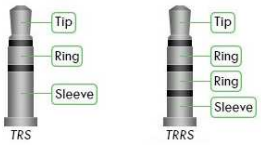

Headphone Jack Type

Audio jack must be plastic without conductive coatings (no chrome)

Individual Audio Jack for Headphone & Microphone

Audio jack pin configuration:
Combo Jack (Headset / Headphone compatible)
Tip = Left
1st ring = Right
2nd ring = Ground
Sleeve = Mono microphone

Microphone Jack (Milos/Santorini Only)
Tip = Left
Ring = Right
Sleeve = Ground

Security Classification	Compal Secret Data		
Issued Date	2017/03/20	Deciphered Date	2020/03/20

Compal Electronics, Inc.	
Title	AUDIO ALC3292-CG
Size: Custom	Document Number: FPC54 LA-H482P
Rev	v0.1
Date:	Friday, September 28, 2018
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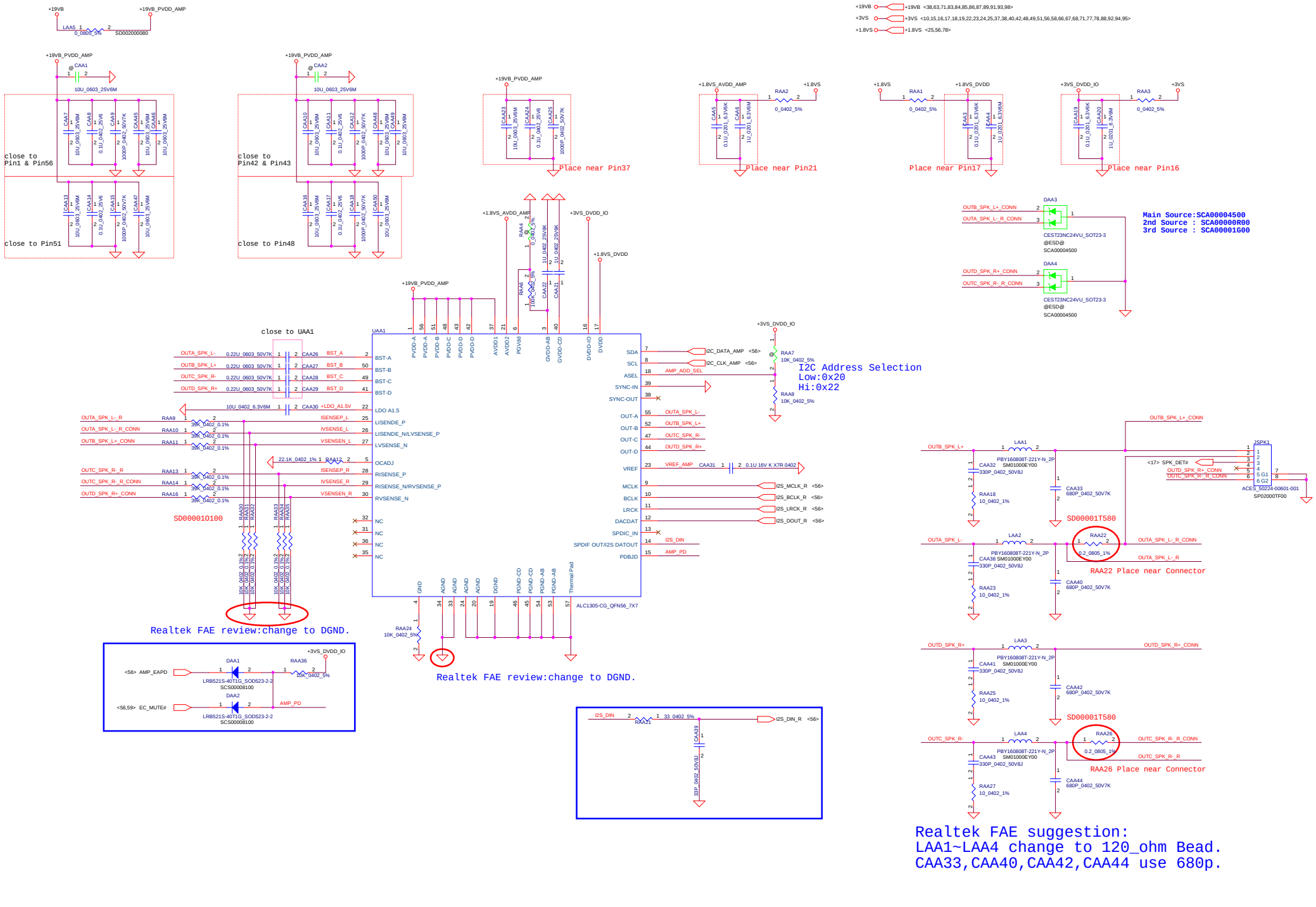

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Issued Date	2018/07/13	Deciphered Date 2020/7/13	Title: Speaker Amp:ALC1305H
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			Date: Friday, September 28, 2018; Sheet 57 of 100

EC Board ID (DIS, phase) control table

2018 PPAV

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N17E-G1	33K	43K	56K	75K
R17M-G1-70	100K	130K	160K	200K

2019 PPAV

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N18P-G0/G1	33K	43K	56K	75K
N18E-G1	100K	130K	160K	200K
R19M-G50-70	240K	270K	330K	430K

2019 OMEN

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N18P-G0/G1	33K	43K	56K	75K
N18E-G1/G2/G3	100K	130K	160K	200K

RH264&CH105 Need use after checking

PIR1.48

For Solve tPCH04(Min 9ms) Sequence Timing

PIR1.29
PIR2.3
PIR4.3

PIR2.31

replace to common part 0108

PIR1.38

Need Check

20mil

CC144/ RC369 place near EC Side

EMI request

KB9022QD LQFP 128P

S IC KB9022QD LQFP 128P EC CONTROLLER

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: EC ENE-KB9022

Size: Custom | Document Number: FPC54 LA-H482P | Rev: v0.1

Date: Friday, September 28, 2018 | Sheet 58 of 100

+3VALW_EC
+5VS

+3VALW_EC <25,58,82>
+5VS <37,38,39,40,56,63,67,78,96>

OMEN New ESB CLK&DAT for Extend I/O

Some EC GPIO maybe change to extend IO control:TBD

+3VALW_EC — RK201 2 — 1 330K_0402_5% — EC_RST#_KC3810

CK201 1 — 2 0.1U_0402_16V7K

UK2

<58> KC3810_ESB_CLK — KC3810_ESB_CLK — 1 ESB_CLK
<58> NMI_DBG# — NMI_DBG# 1 RK209 2 NMI_DBG#_KC3810 — KB9542@ 0_0402_5% — 2 GPIO00
*NMI_DBG#: is a debug pin for EC to Inform BIOS after press hot key.
EC_RST#_KC3810 — 3 RST#
<58> KC3810_ESB_DAT — KC3810_ESB_DAT — 4 ESB_DAT
*GP:15_Milos_OMENX_HP1X_RFQ_ODM_180518
TP OFF LED on F11 key
12V_EN_KC3810_GPIO01 — 5 GPIO01
<63> TP_LED_OFF# — TP_LED_OFF# — 6 GPIO02
<50> EC_TBT_RESET — EC_TBT_RESET — 7 GPIO03
<25> GPU_ALERT — GPU_ALERT — 8 GPIO04
<73> USB_ON# — USB_ON# — 9 GPIO05
<63> KB_GPO1# — 10 GPIO06
<63> KB_GPO2# — 11 GPIO07/CAS_CLK
12 GND

13 TEST_EN#
14 GPIO08/CAS_DAT
USB_CTL1 — 15 GPIO09 — USB_CTL1 <71>
USB_CTL2 — 16 GPIO0A — USB_CTL2 <71>
USB_CTL3 — 17 GPIO0B — USB_CTL3 <71>
USB_CHARGE_EN — 18 GPIO0C/PWM0 — USB_CHARGE_EN <71>
GPU_OVERT# — 19 GPIO0D/PWM1 — GPU_OVERT# <25>
LAN_PWR_EN — 20 GPIO0E/PWM2 — LAN_PWR_EN <51>
WL_PWREN_EC# — 21 GPIO0F/PWM3 — WL_PWREN_EC# <52>
EC_MUTE# — 22 GPIO10/ESB_RUN# — EC_MUTE# <56,57>
23 GPIO11/BaseAddOpt
24 VCC — +3VALW_EC

GND — 25

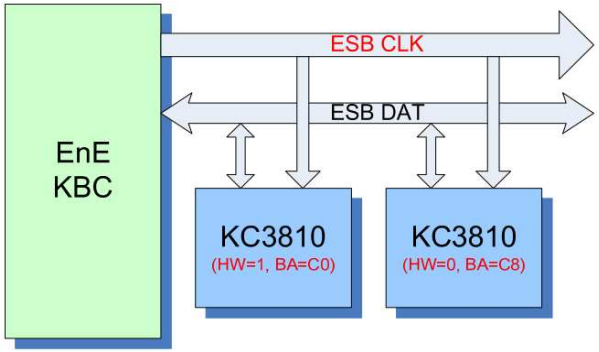
KC3810NF-A0_QFN24_4X4
SA00002AI00

CK202 1 — 2 0.1U_0201_10V6K

USB_CTL3 — 2 RK28 1 — 100K_0402_5%

以下14個Pin 建議可以接到external I/O 3810,
1. USB_CTL1(GPIO4B Pin84),
2. USB_CTL2(GPIO3F Pin72),
3. USB_CTL3(GPIO1D Pin38),
4. USB_CHARGE_EN(GPIO1A Pin36),
5. GPU_OVERT#(GPIO0D Pin19) => DPF50 NO USE
6. LAN_PWR_EN(GPIO4D Pin86),
7. WL_PWREN_EC#(GPIO61 Pin98),
8. DCHG_I(GPIO40 Pin73) => DPF50 NO USE
9. USB_ONH(GPIO37 Pin 121),
10. LED : 5 Pin.

Some EC GPIO maybe change to extend IO control:TBD



+5VS
1 RK210 2 0_0402_5%
<97> 12V_EN — 1 RK211 @ 2 0_0402_5% — 12V_EN_KC3810_GPIO01

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Title: TBD		
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
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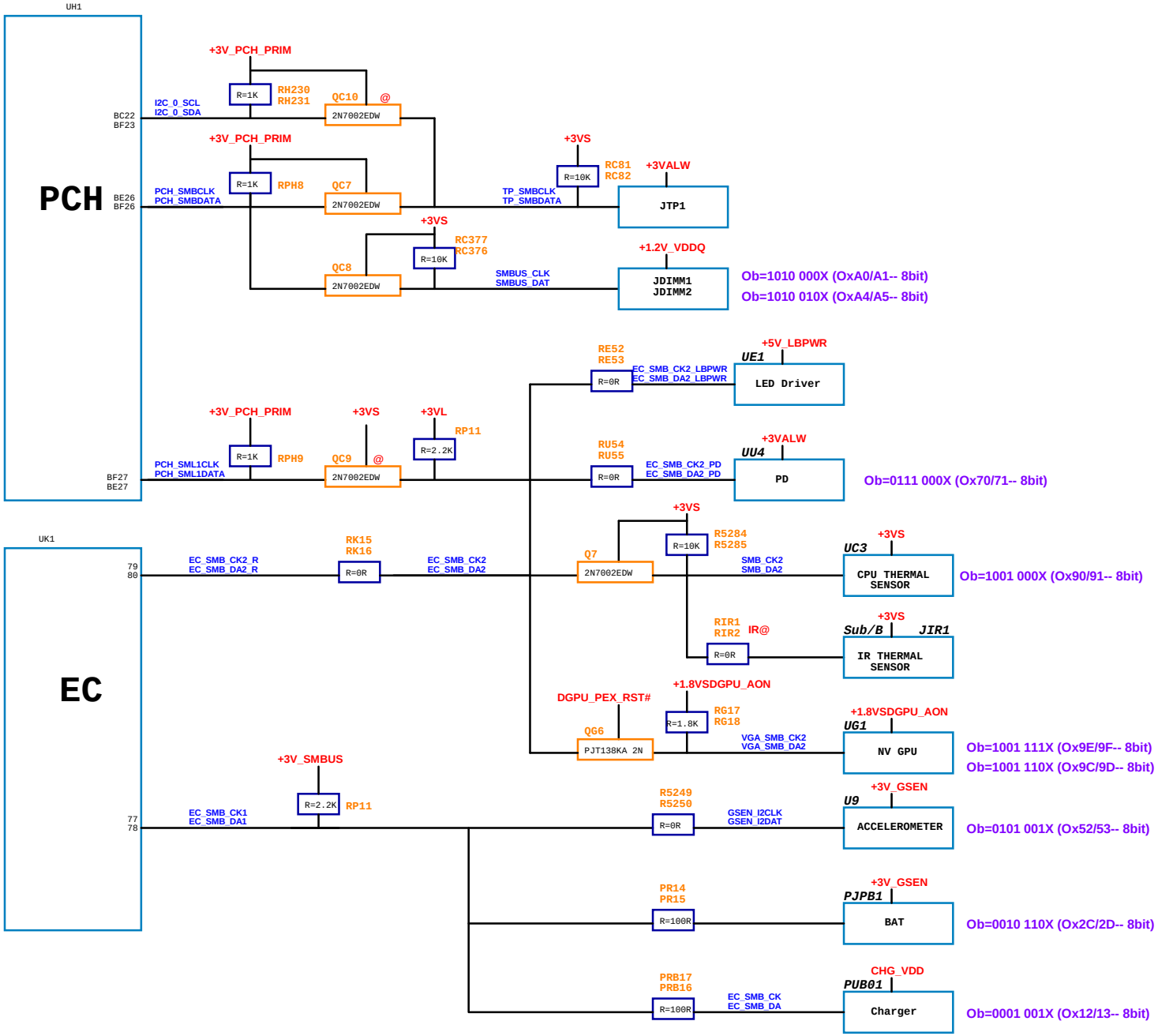

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.	
Title	SMBus Block Diagram
Size: Custom	Document Number: FPC54 LA-H482P
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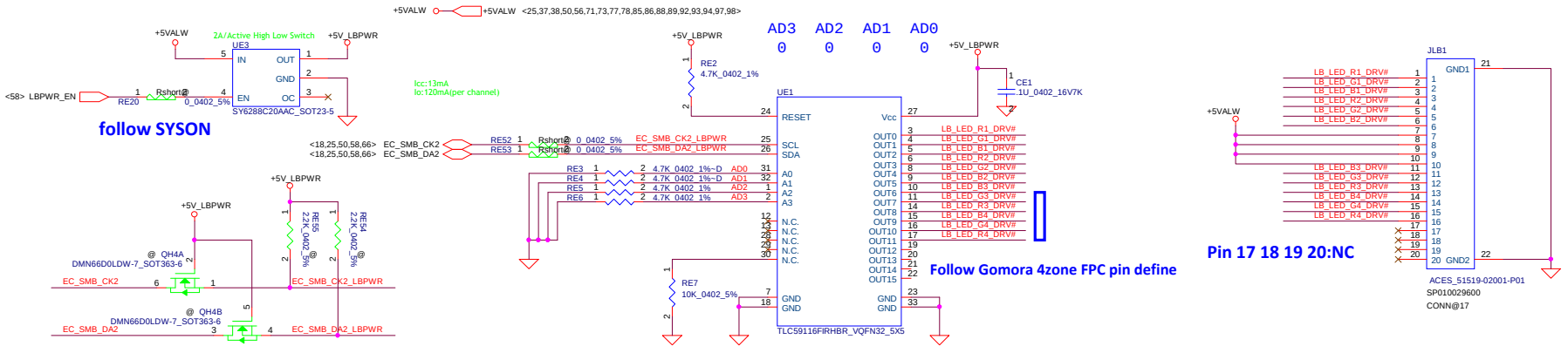

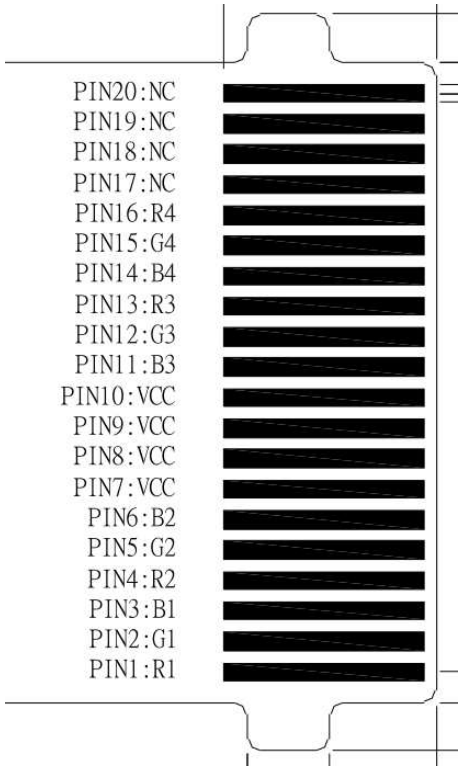

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Issued Date	2016/02/01	Deciphered Date	2017/12/31

Compal Electronics, Inc.			
Title	A Cover BKL		
Size	Document Number		Rev
Custom	FPC54 LA-H482P		v0.1
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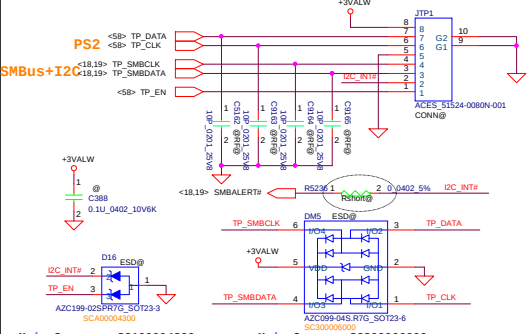
TP Button BD Connector

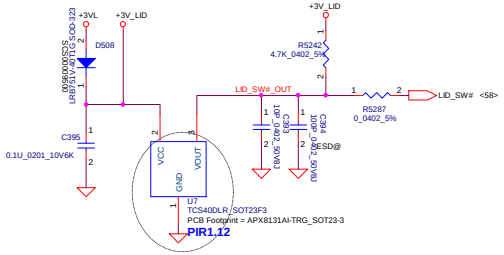


Main Source : SCA00004300
2nd Source : SCA00000T00
3rd Source : SC600001600

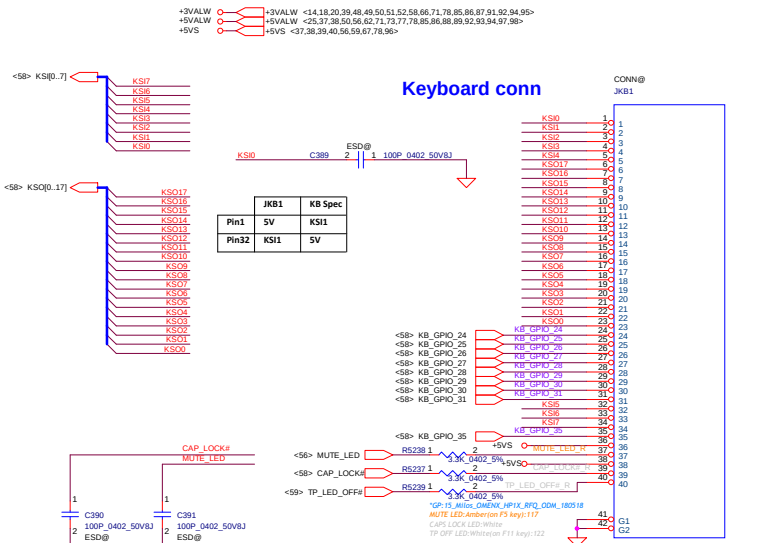
Main Source: SC300006000
2nd Source : SC300001600
3rd Source : SC300003S00

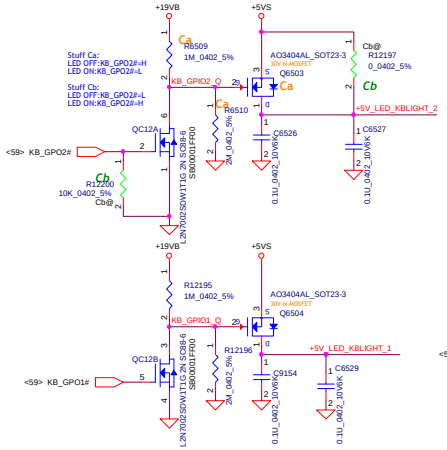
Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	PS2_DATA	I/O	PS2 data
3	PS2_CLK	I/O	PS2 clock
4	GND	GND	Ground
5	SMB_CLK	I/O	SMBUS clock I_{SINK} or I_{SRC}: 8 mA max.
6	SMB_DATA	I/O	SMBUS data. I_{SINK} or I_{SRC}: 8 mA max.
7	/INT (/ATTN)	O	For SMBus application, low active, indicates touchpad likes to send data to system (host) if go low.
8	LID_CLOSE (TP Disable/Enable)	I	Enable or disable touchpad, low active Low: Disable TP High: Enable TP

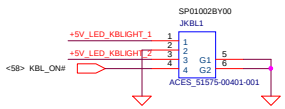
Lid Switch (Hall Effect Sensor)



Keyboard conn







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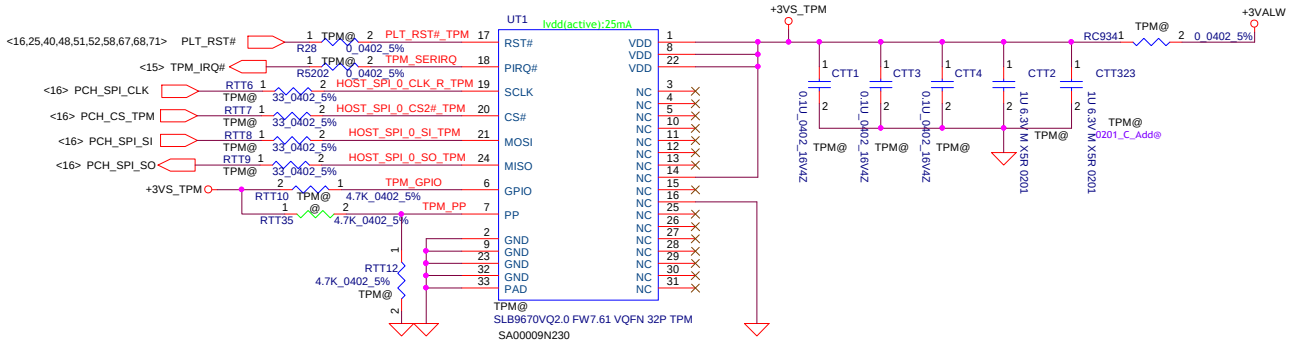
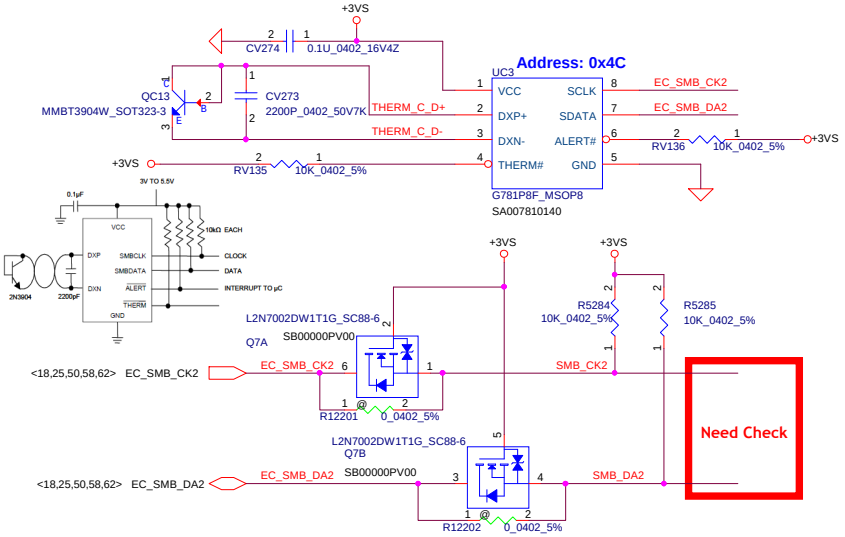
+3VALW <+3VALW <14,18,20,39,48,49,50,51,52,58,63,71,78,85,86,87,91,92,94,95>

+3VS <+3VS <10,15,16,17,18,19,22,23,24,25,37,38,40,42,48,49,51,56,57,58,67,68,71,77,78,88,92,94,95>

TPM2.0



CPU THERMAL SENSOR



ACCELEROMETER
ST Micro HP2DC

+3VL <+3VL <20,50,58,63,71,77,78,83,84,85>

Hmax=1.0mm

Idd(in normal mode):11uA

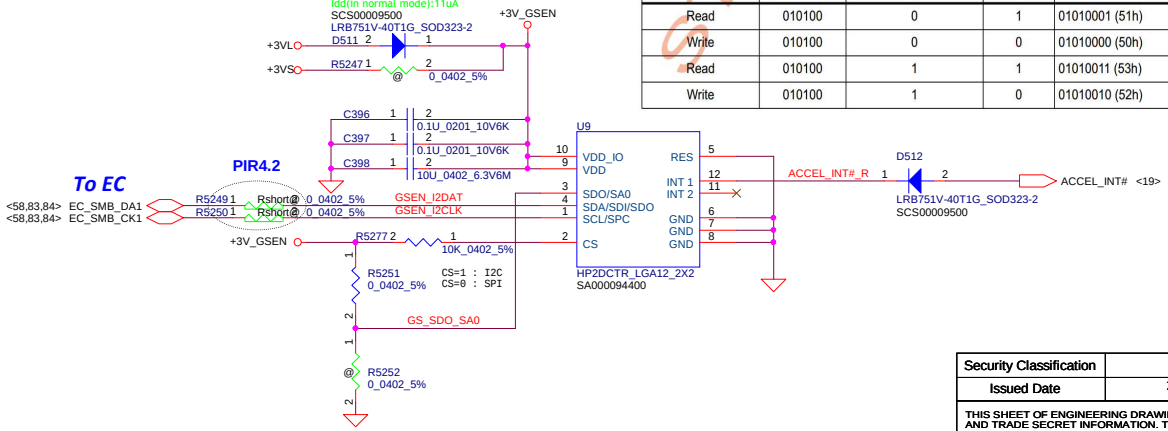
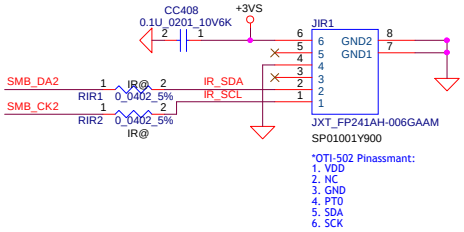


Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



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Compal Electronics, Inc.	
Title	TPM&Thermal&G-sensor
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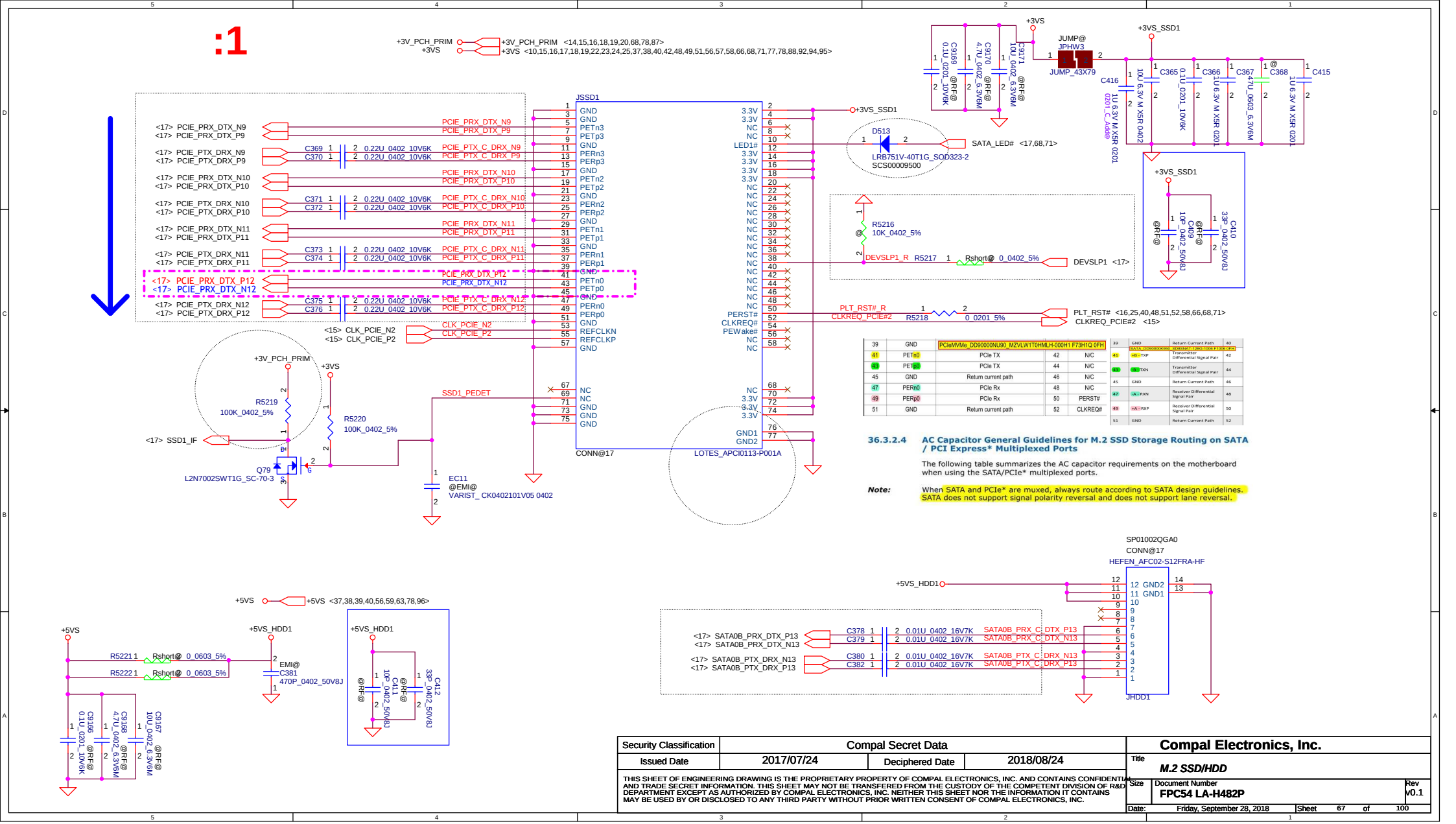
:1



39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH	42	N/C	
41	PETn0	PCIe TX	42	N/C	
43	PETp0	PCIe TX	44	N/C	
45	GND	Return current path	46	N/C	
47	PERn0	PCIe Rx	48	N/C	
49	PERp0	PCIe Rx	50	PERST#	
51	GND	Return current path	52	CLKREQ#	

36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

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Compal Electronics, Inc.

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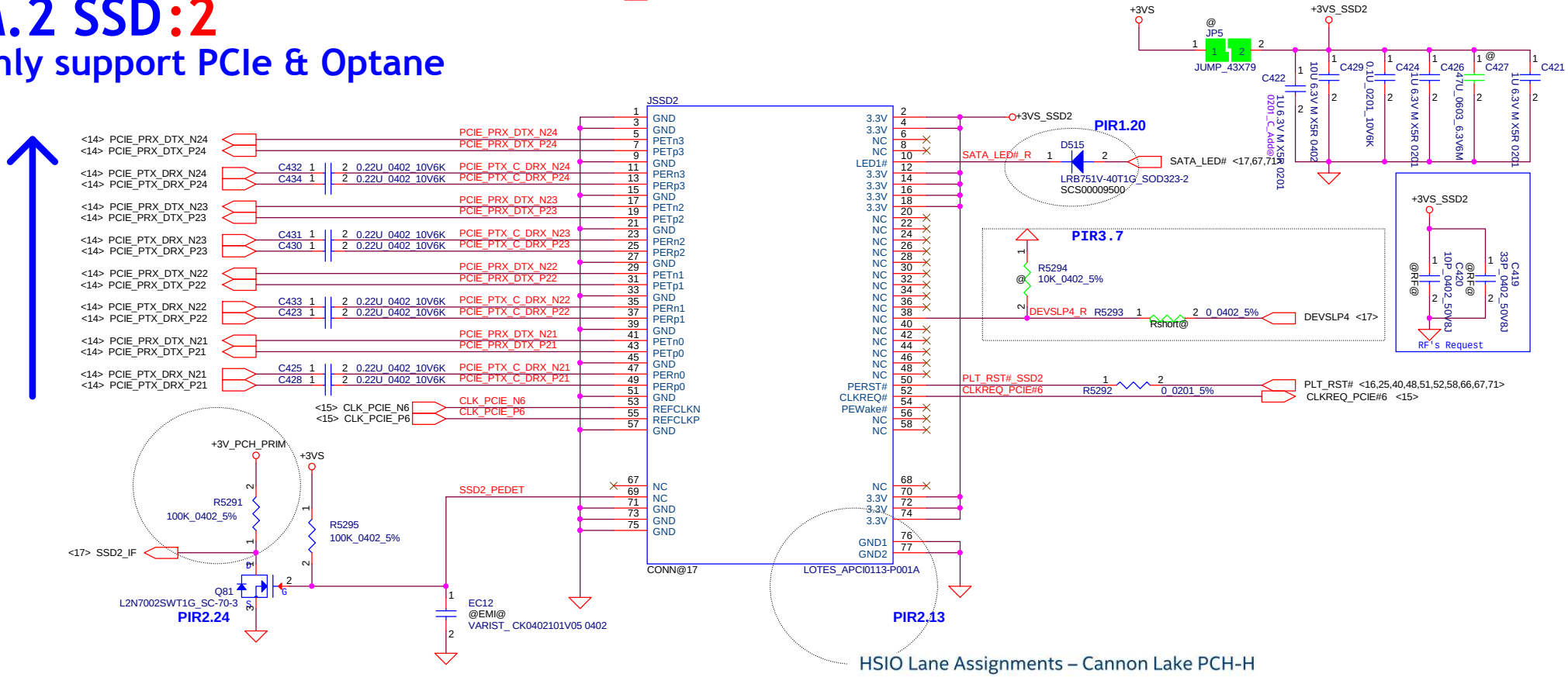
M.2 SSD:2

Only support PCIe & Optane



36.3.2.4 AC Capacitor General Guidelines for M.2 SSD Storage Routing on SATA / PCI Express* Multiplexed Ports

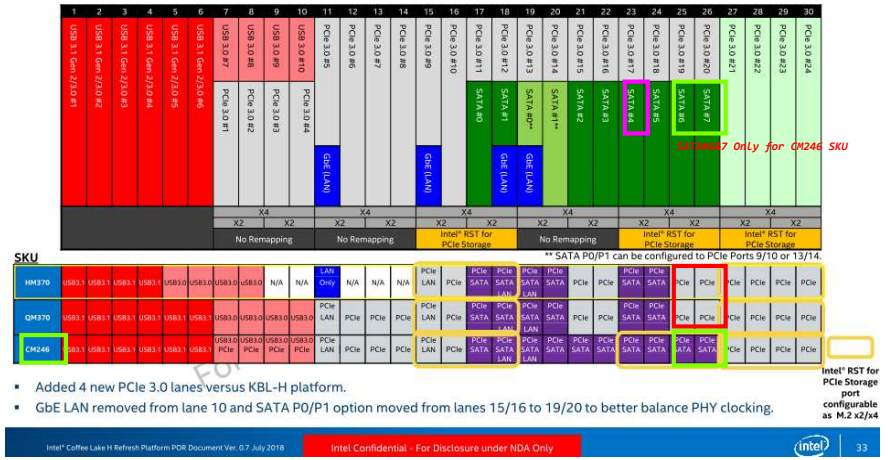
The following table summarizes the AC capacitor requirements on the motherboard when using the SATA/PCIe* multiplexed ports.

Note: When SATA and PCIe* are muxed, always route according to SATA design guidelines. SATA does not support signal polarity reversal and does not support lane reversal.

39	GND	Return Current Path	40		
41	+B TXP	Transmitter Differential Signal Pair	42		
43	-B TXN	Transmitter Differential Signal Pair	44		
45	GND	Return Current Path	46		
47	-A RXN	Receiver Differential Signal Pair	48		
49	+A RXP	Receiver Differential Signal Pair	50		
51	GND	Return Current Path	52		

39	GND	PCIeMVMe_DD90000NU90_MZVLW1T0HMLH-000H1 F73H1Q 0FH		
41	PETn0	PCIe TX	42	N/C
43	PETp0	PCIe TX	44	N/C
45	GND	Return current path	46	N/C
47	PERn0	PCIe Rx	48	N/C
49	PERp0	PCIe Rx	50	PERST#
51	GND	Return current path	52	CLKREQ#

HSIO Lane Assignments – Cannon Lake PCH-H



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Title	*M.2 SSD/HDD*		
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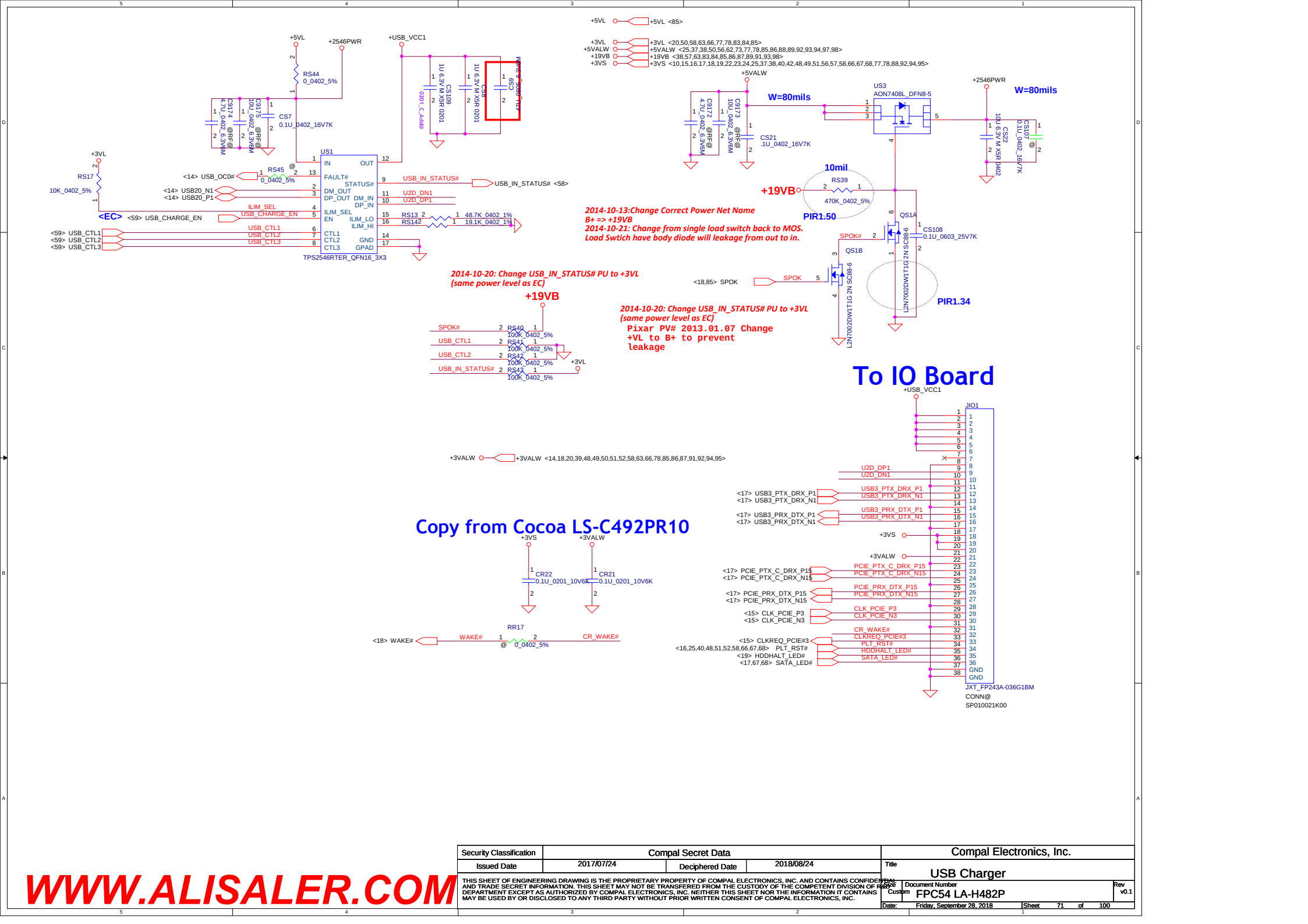

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Compal Electronics, Inc.

Title: USB Charger

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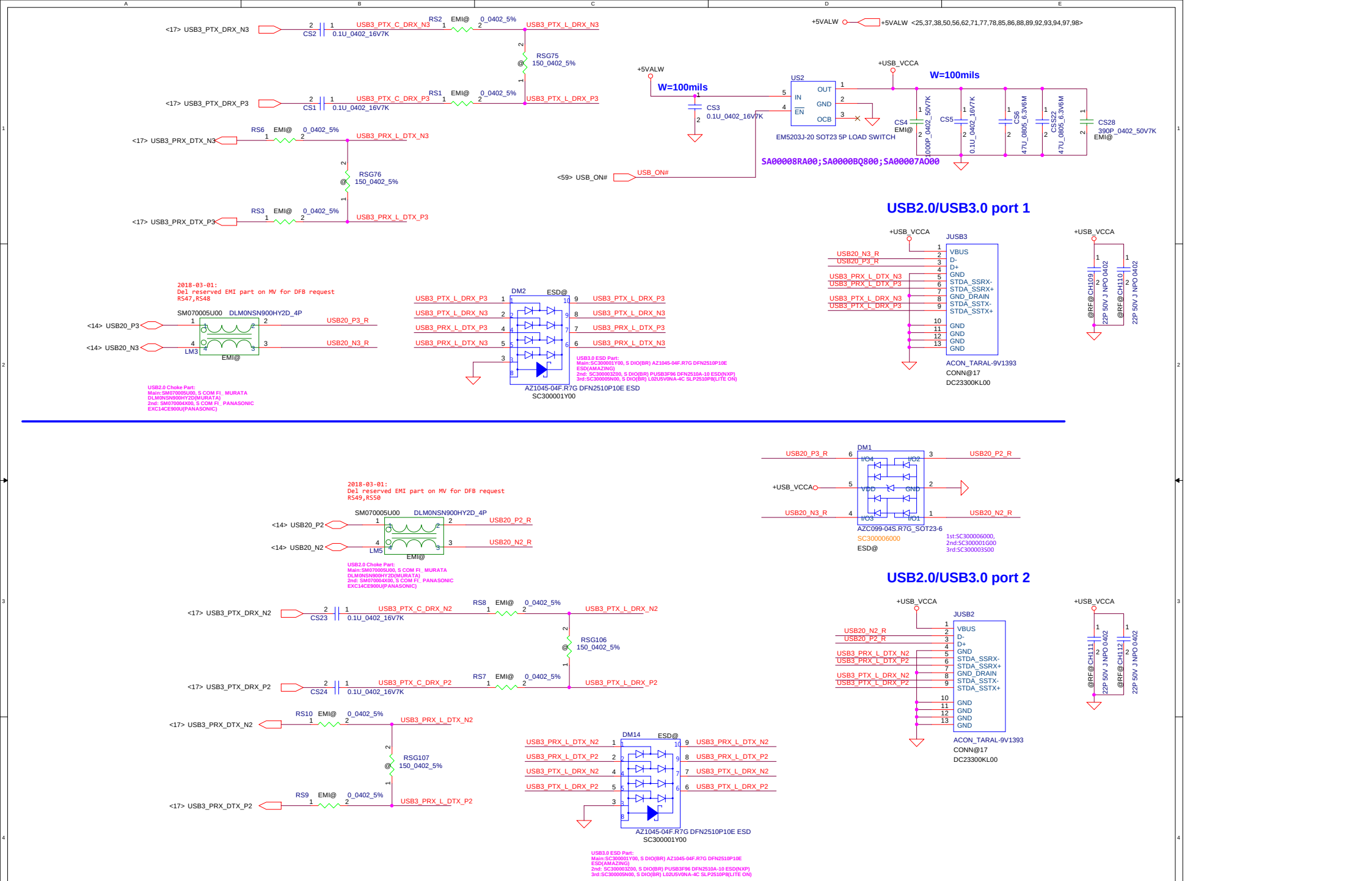

Security Classification	Compal Secret Data		
Issued Date	2017/08/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: USB 3.0/2.0 conn

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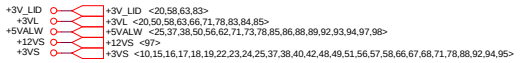
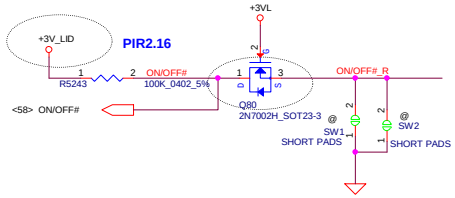
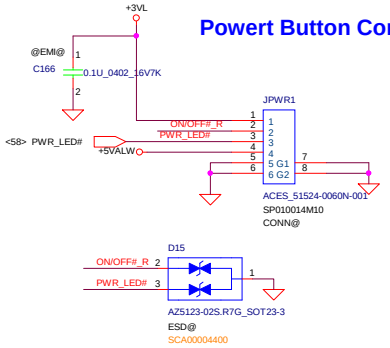


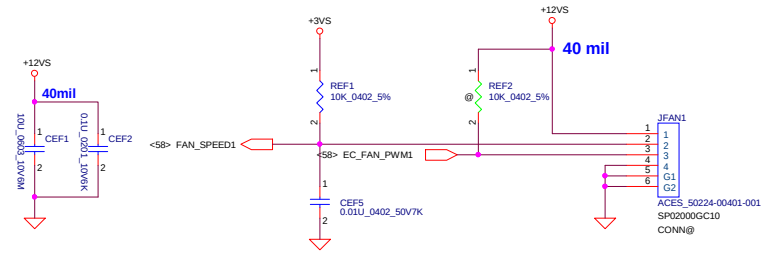


Powert Button Connector

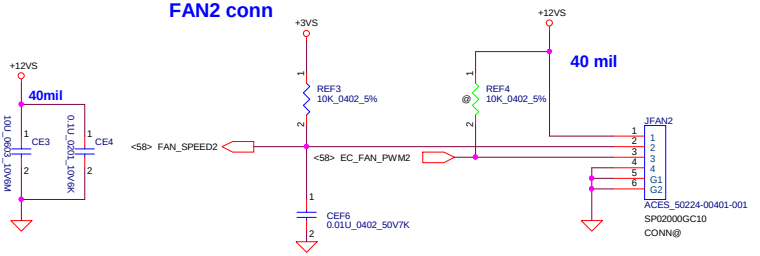


Main Source : SCA00004400
2nd Source : SCA00001B00
3rd Source : SCA00003400

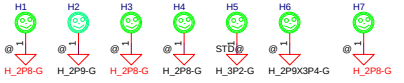
FAN1 conn



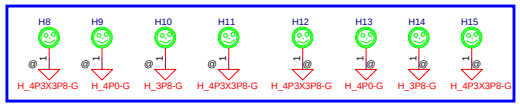
FAN2 conn

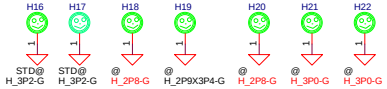


Screw Hole



CPU/GPU bracket





Fiducial Mark

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Compal Electronics, Inc.

Title: IO CON

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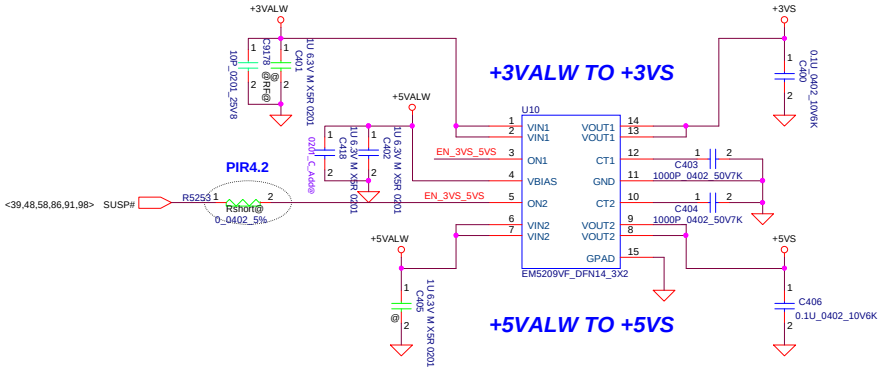

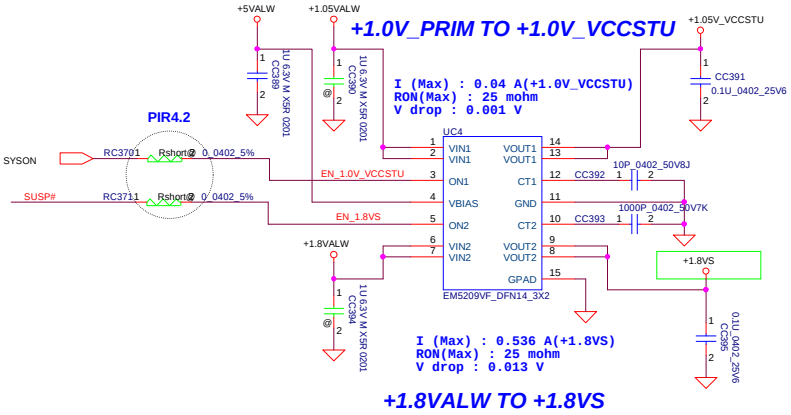

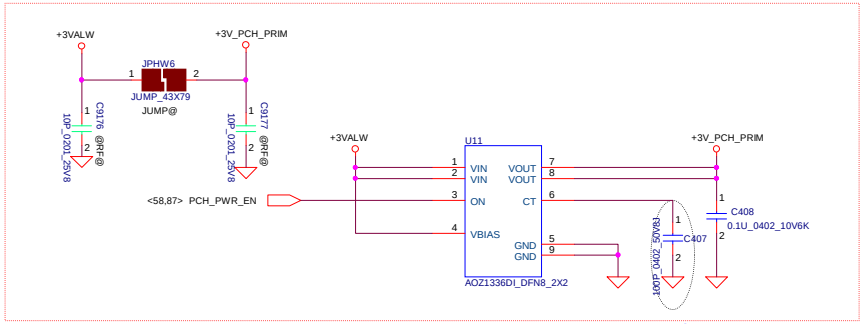

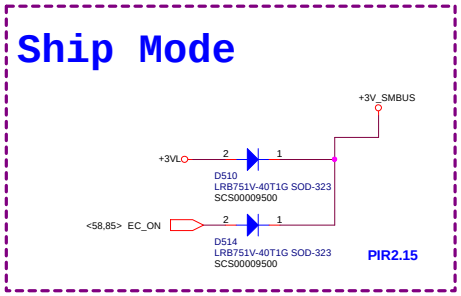

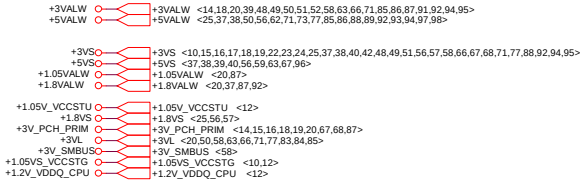

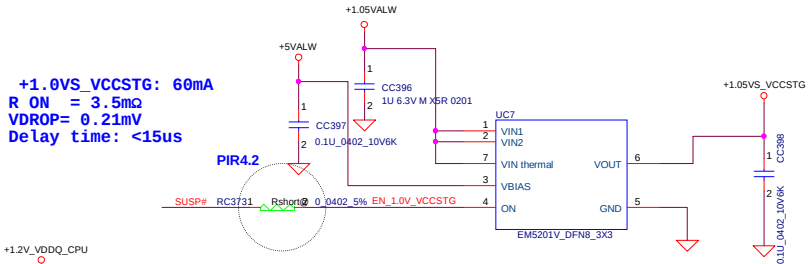

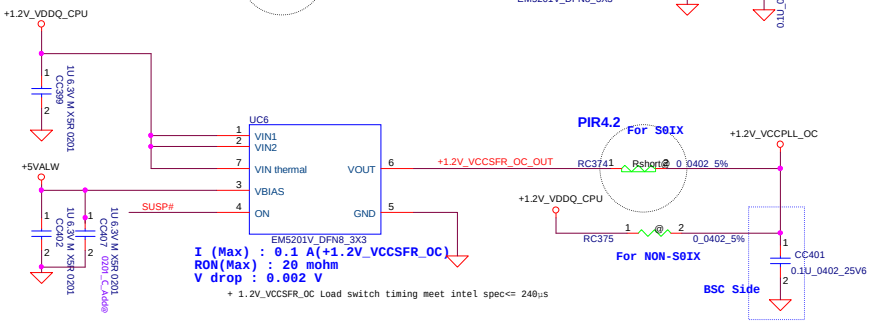

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: DC INTERFACE

Size | Document Number: FPC54 LA-H482P | Rev: v0.1

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TBD: Empty Page

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Title	TBD		
Size: C Custom	Document Number: FPC54 LA-H482P		Rev: v0.1
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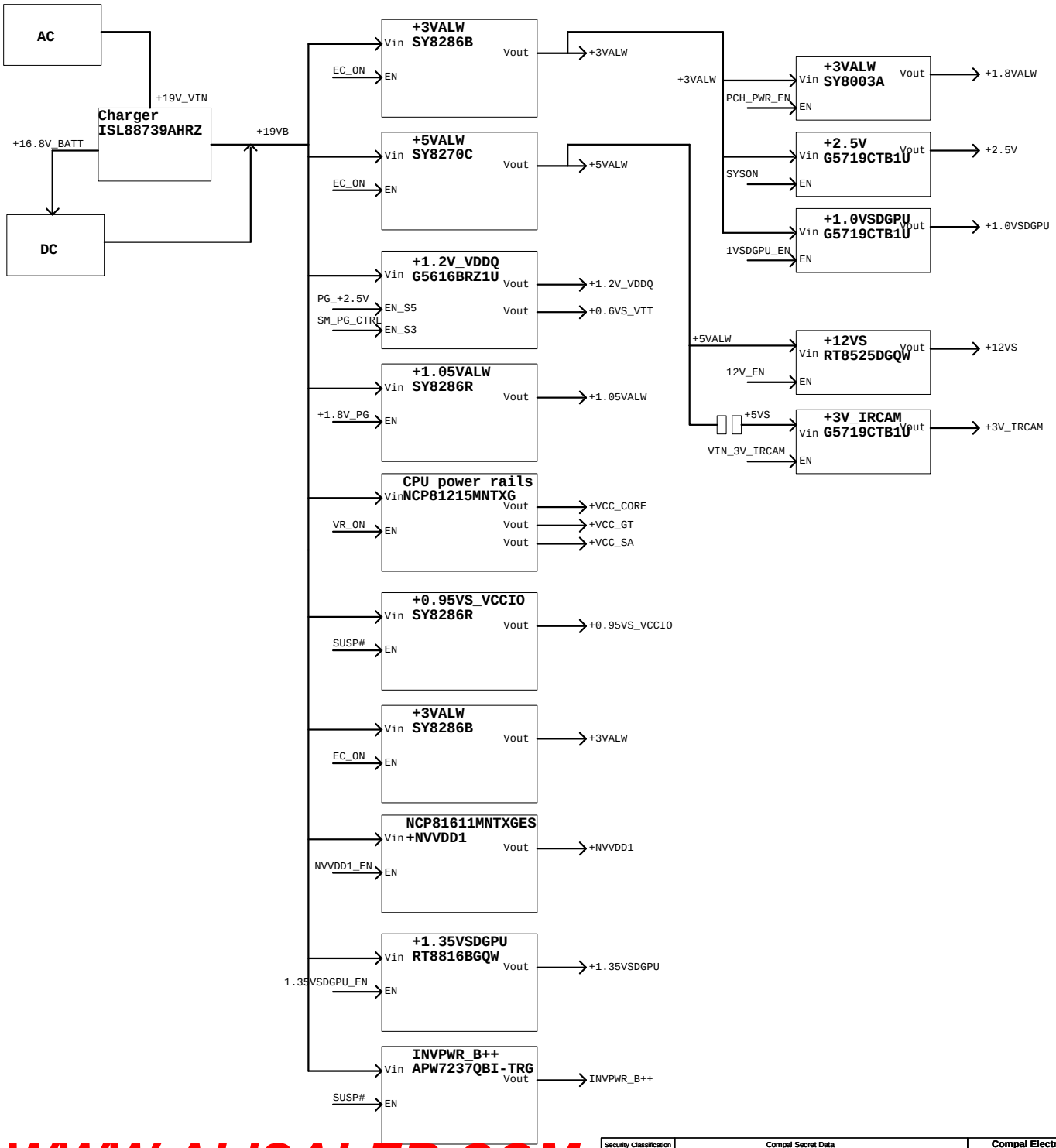
TBD: Empty Page

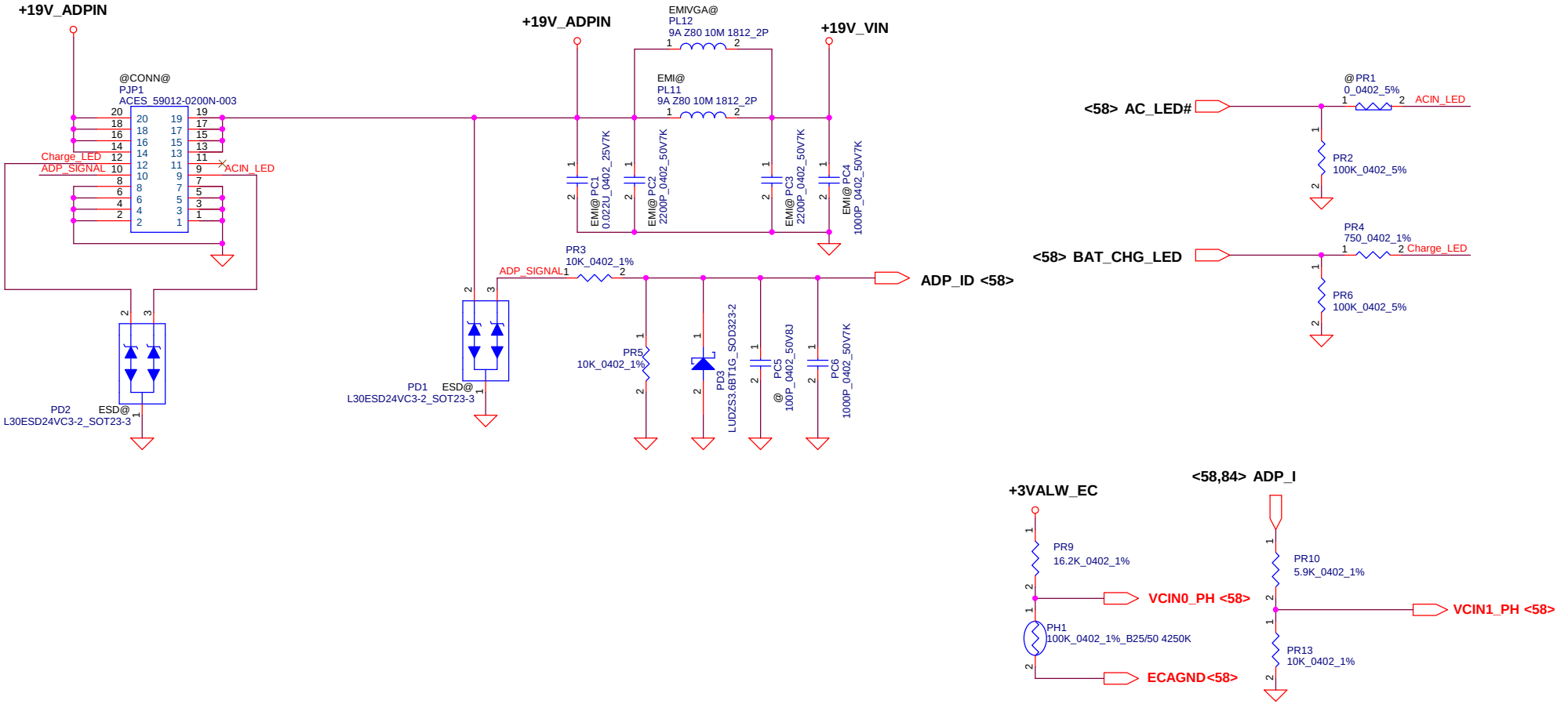
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Title: TBD		
Size: Custom	Document Number: FPC54 LA-H482P	Rev: v0.1
Date: Friday, September 28, 2018	Sheet 80 of 100	



Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

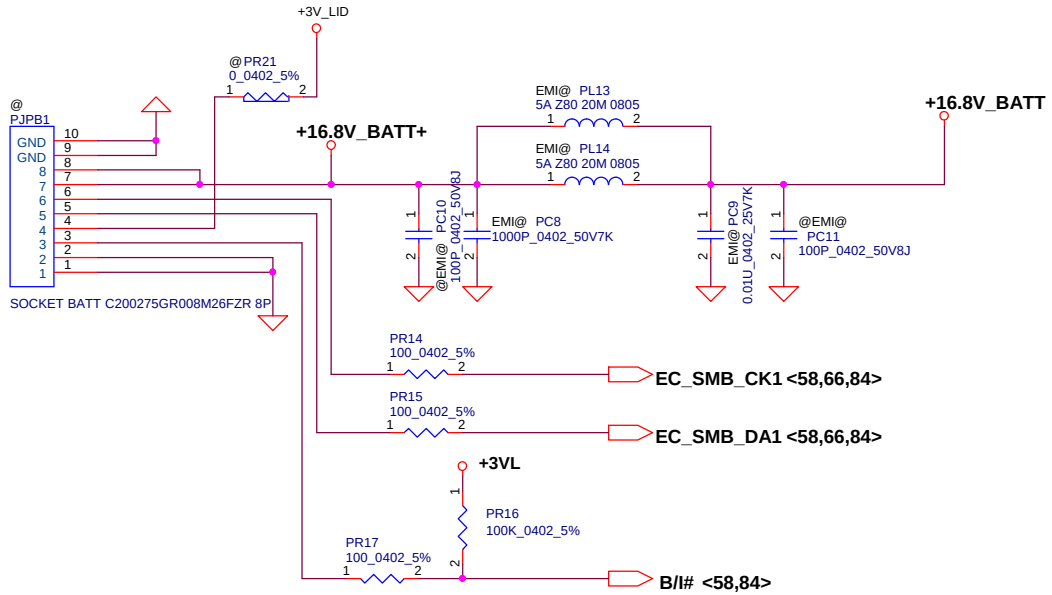
Compal Electronics, Inc.			
Title	Power Block Diagram		
Size	Document Number		Rev 0.1
Date: Friday, September 28, 2018		Sheet 61 of 100	

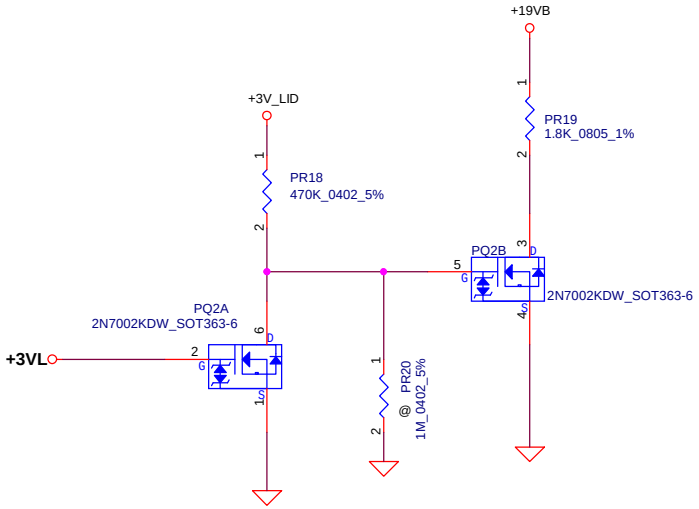


Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title	DC Conn		
Size	Document Number		Rev 0.1
Date: Friday, September 28, 2018	Sheet 82 of 100		





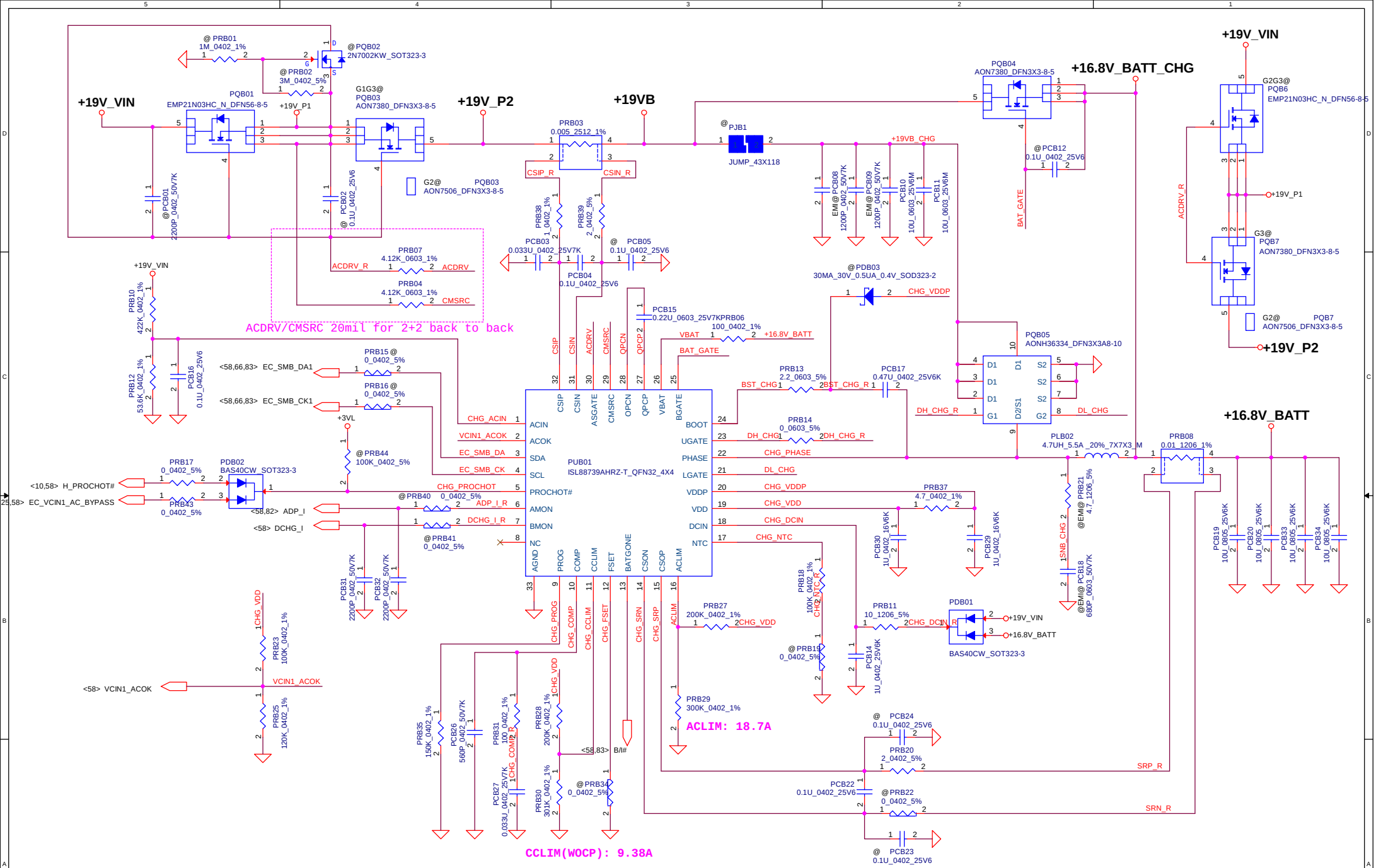
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: BATT Conn

Size | Document Number | Rev 0.1

Date: Friday, September 28, 2018 | Sheet 83 of 100



Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
Custom		0.1

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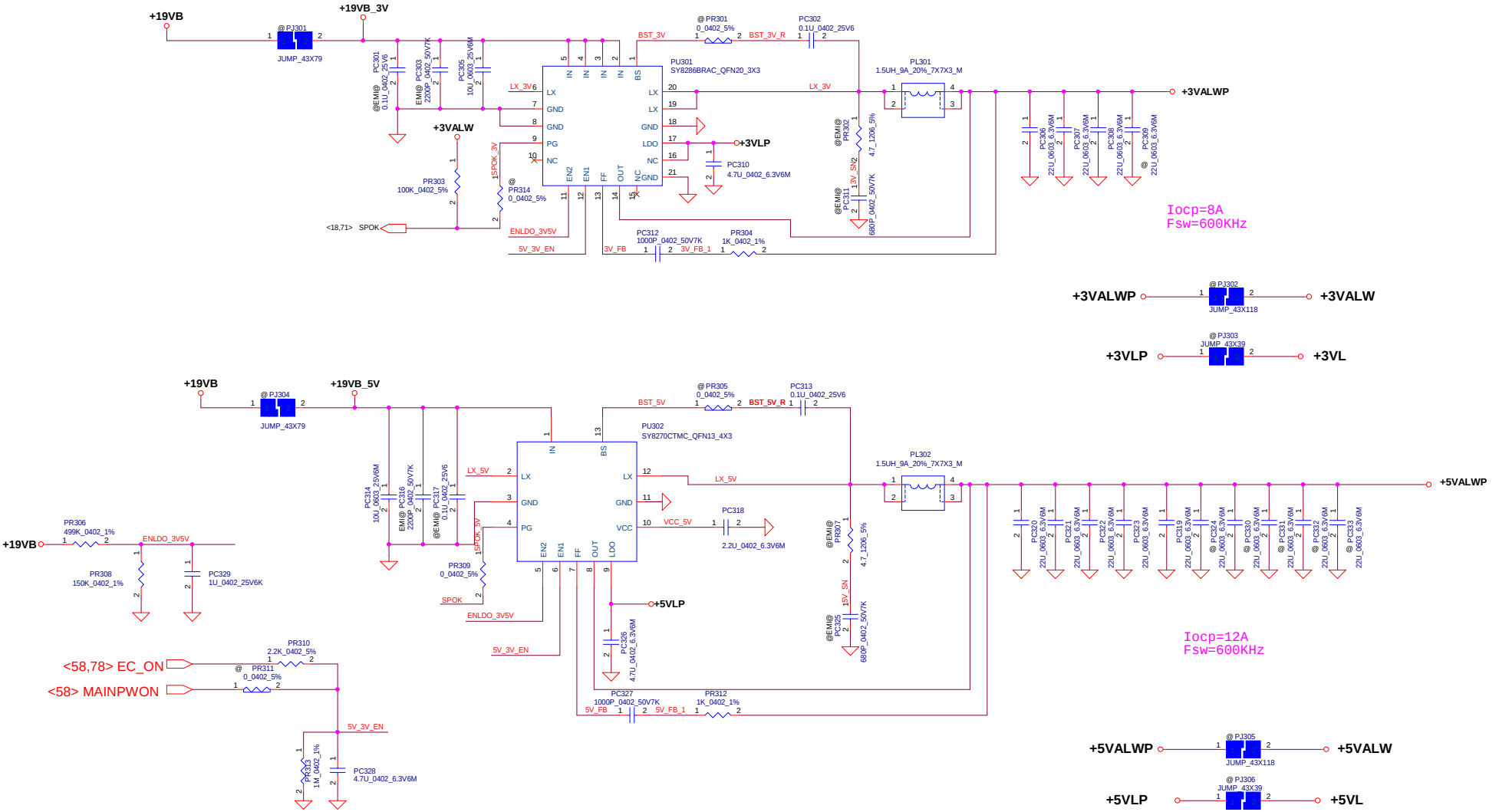

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Issued Date	2018/12/1	Deciphered Date	2020/08/24

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Title: 3VALW/5VALW

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Custom		0.1

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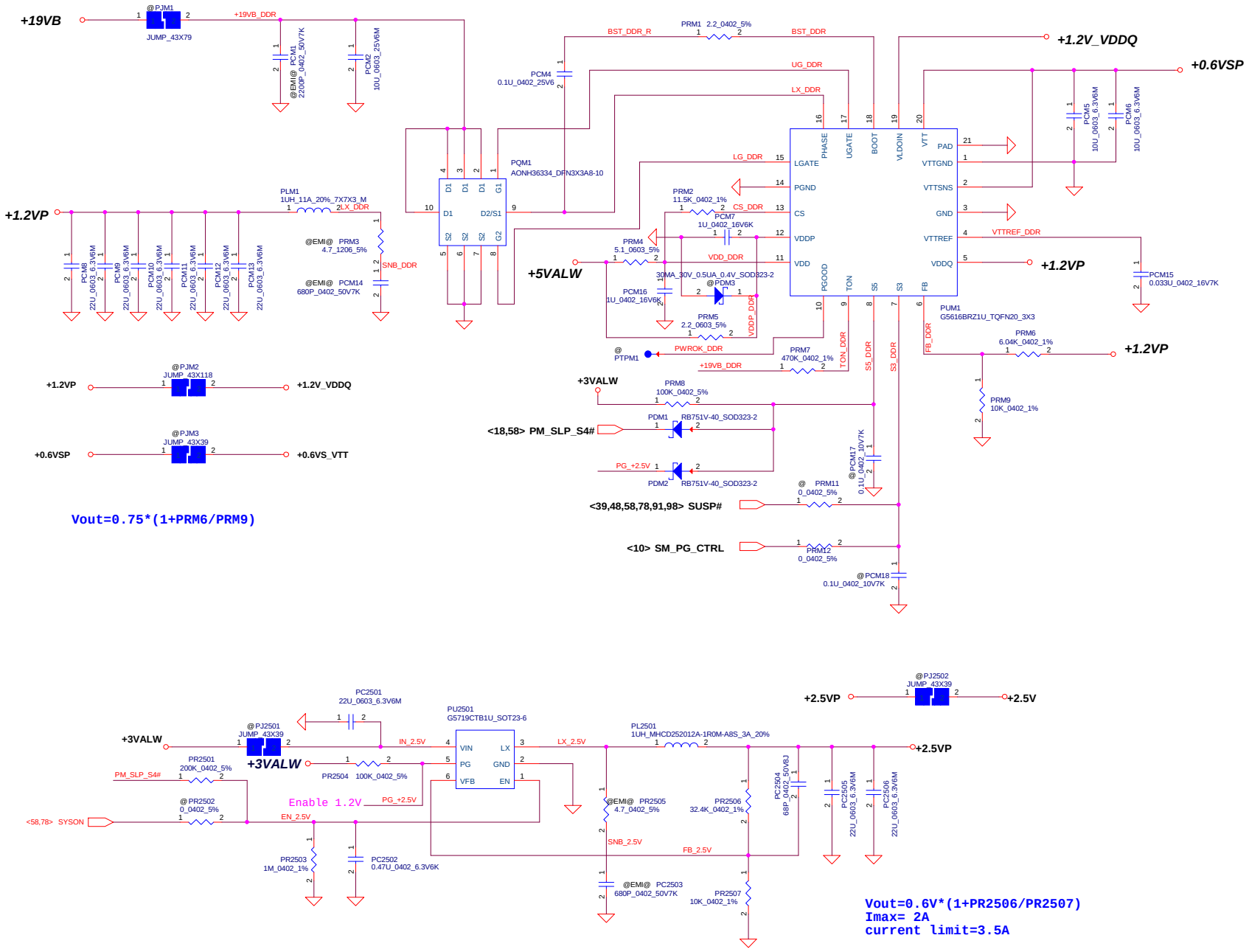

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5V

Size: Custom | Document Number | Rev: 0.1

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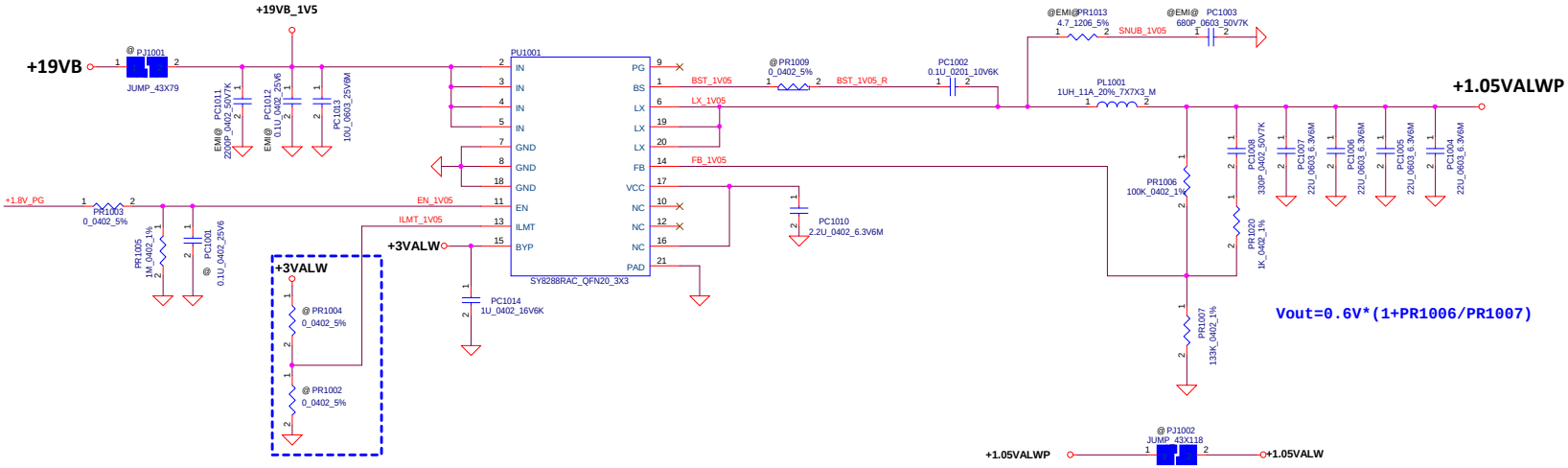

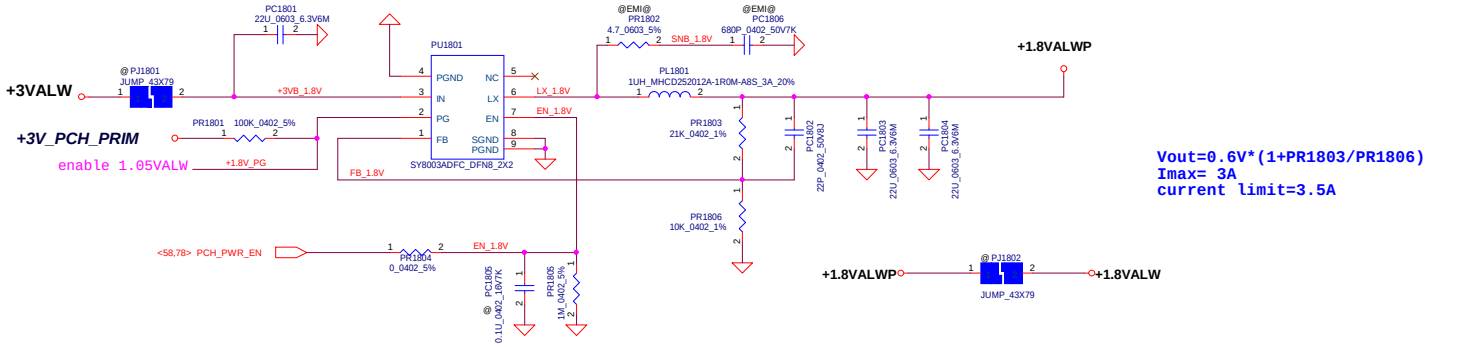

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: 1.05V/1.8V

Size: C | Document Number | Rev: 0.1

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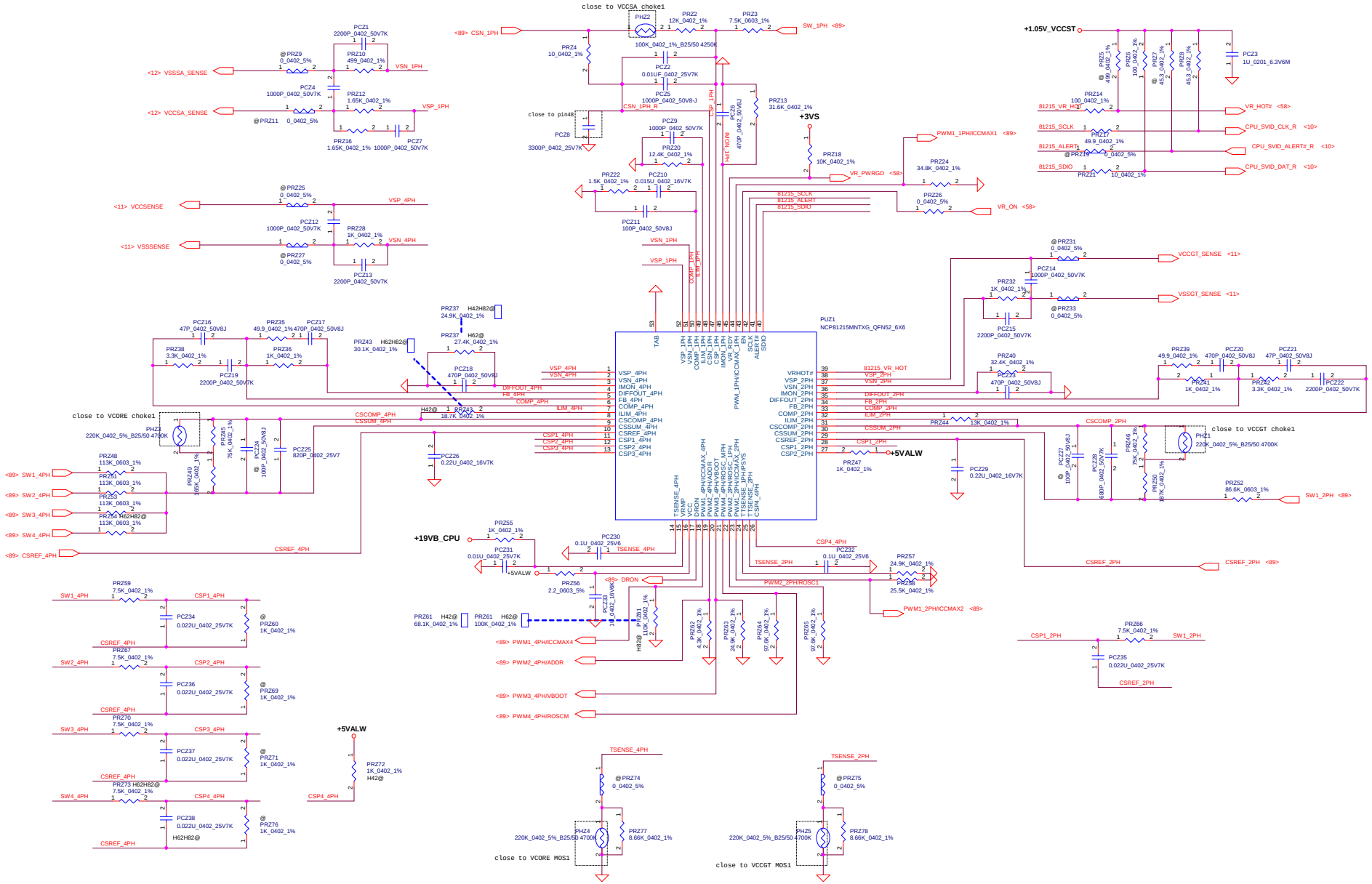

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/1	Deciphered Date 2020/08/24	Title: VCORE
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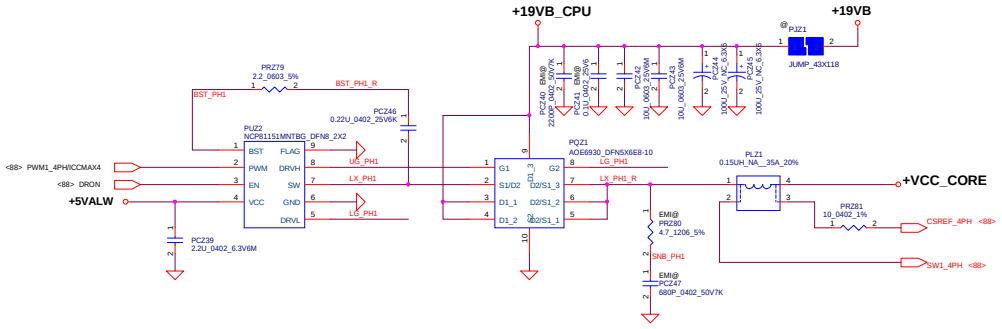
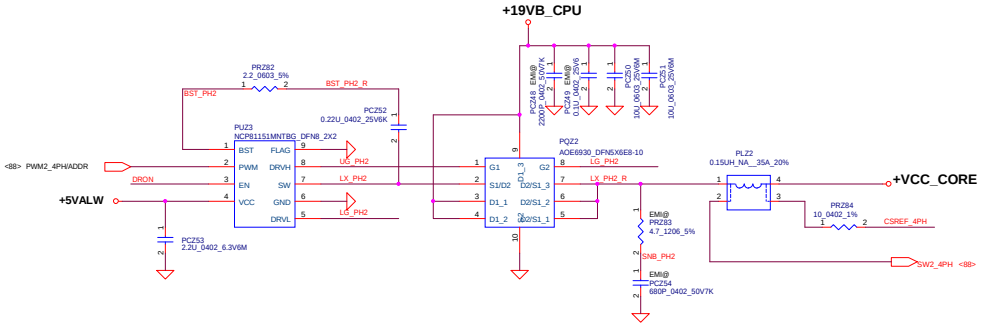
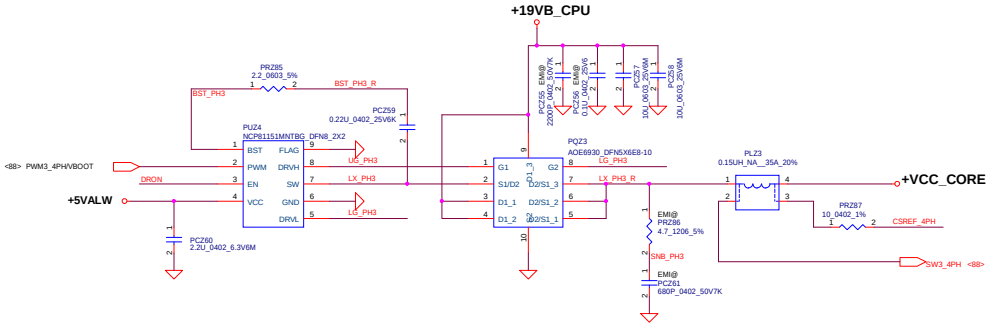
VCCCORE
H82 ICCMAX:140A
H82 OCP:168A
H62 ICCMAX:128A
H62 OCP:168A
H42 ICCMAX:86A
H42 OCP:103A
LL:1.8mohm
FSW:600kHz

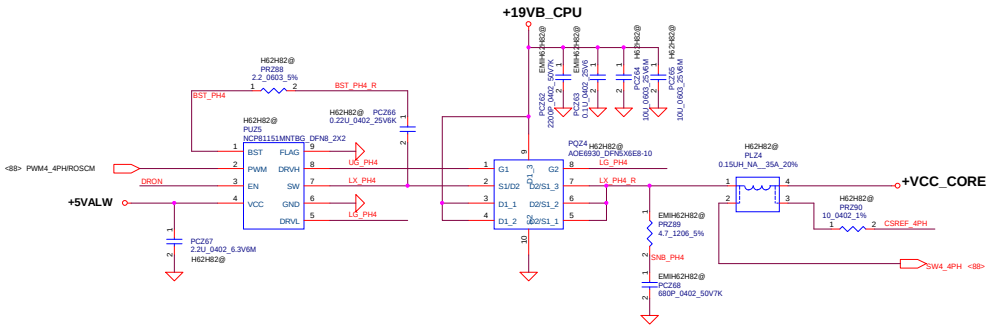
VCCGT
ICCMAX:32A
OCP:48A
LL:2.7mohm
FSW:600kHz

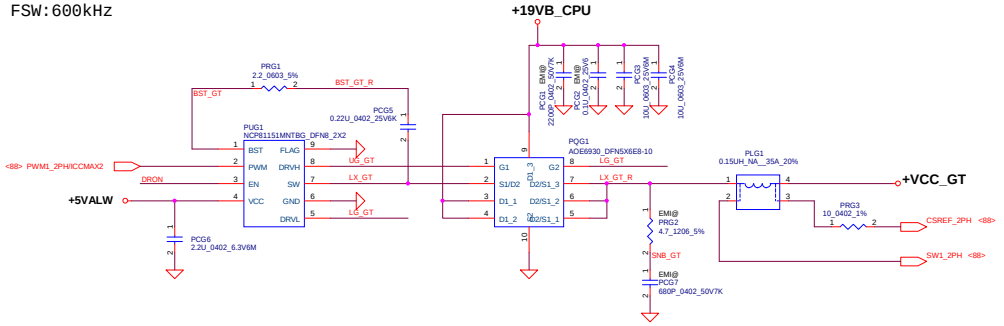
VCCSA
ICCMAX:11.1A
OCP:17.6A
LL:10.3mohm
FSW:600kHz

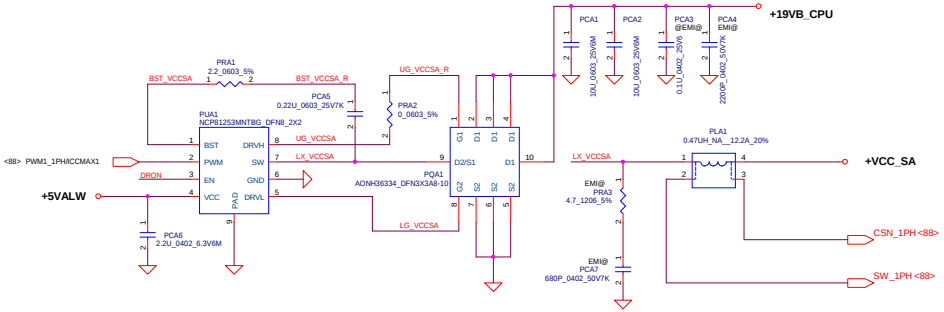




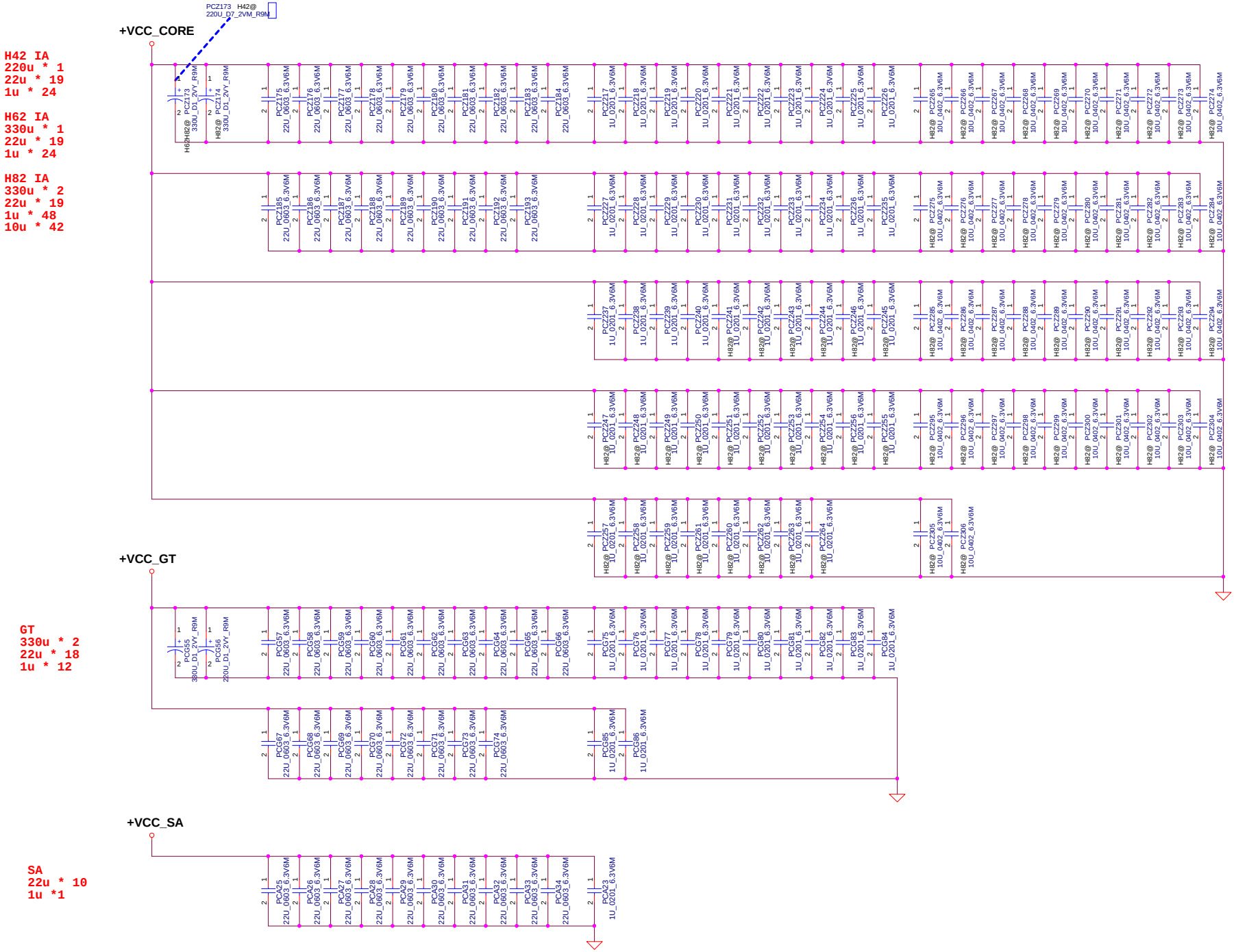








Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2018/12/1	Deciphered Date	2020/08/24
Title	VCORE SW		
Size: Custom	Document Number		Rev: 0.1
Date: Friday, September 28, 2018	Sheet 89 of 100		



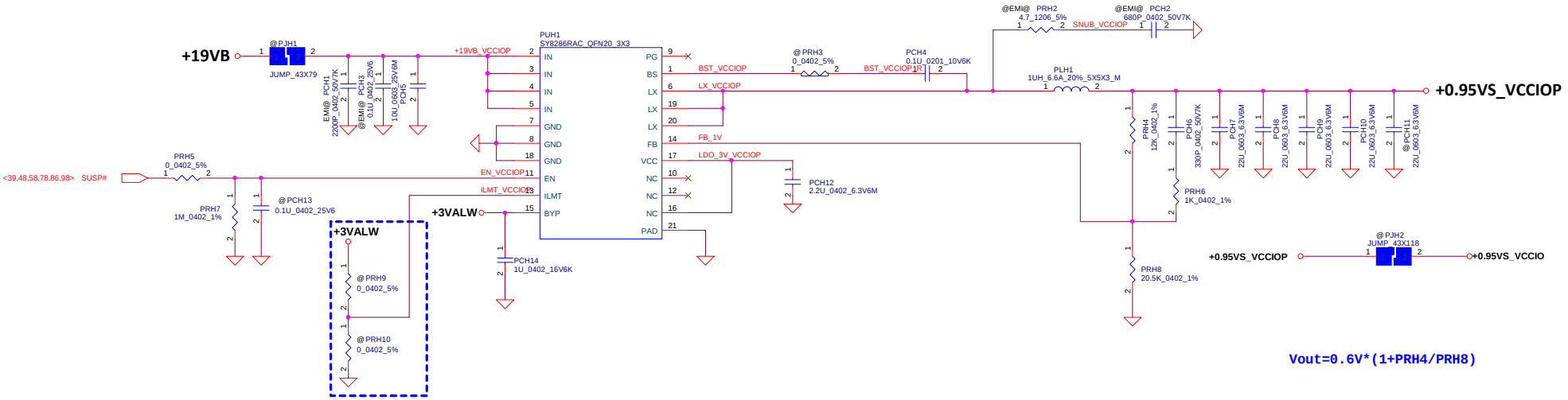
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: VCORE Decoupling

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 90 of 100



Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Title: **VCCIO**

Size	Document Number	Rev
Custom		0.1

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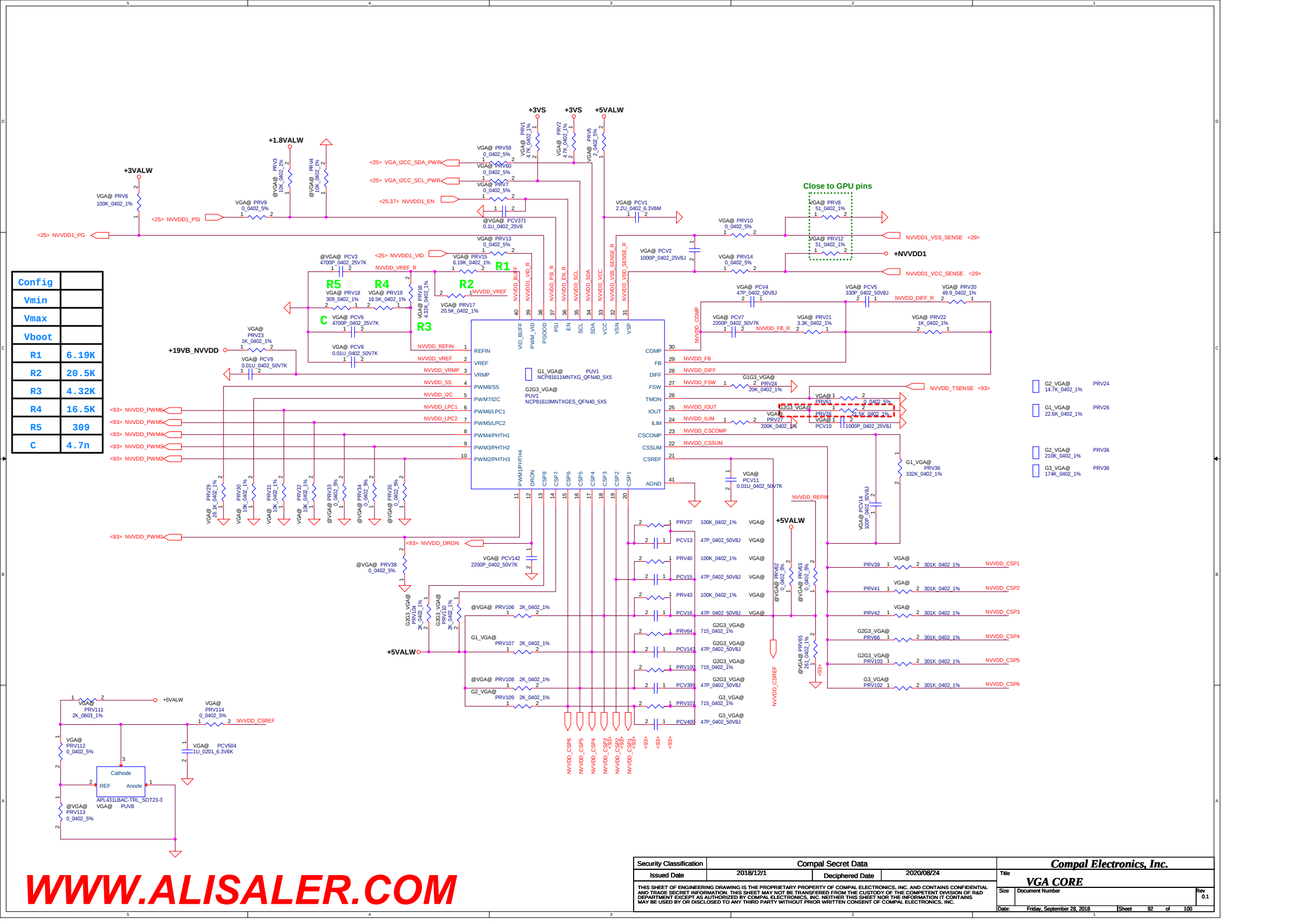


Config	
Vmin	
Vmax	
Vboot	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	309
C	4.7n

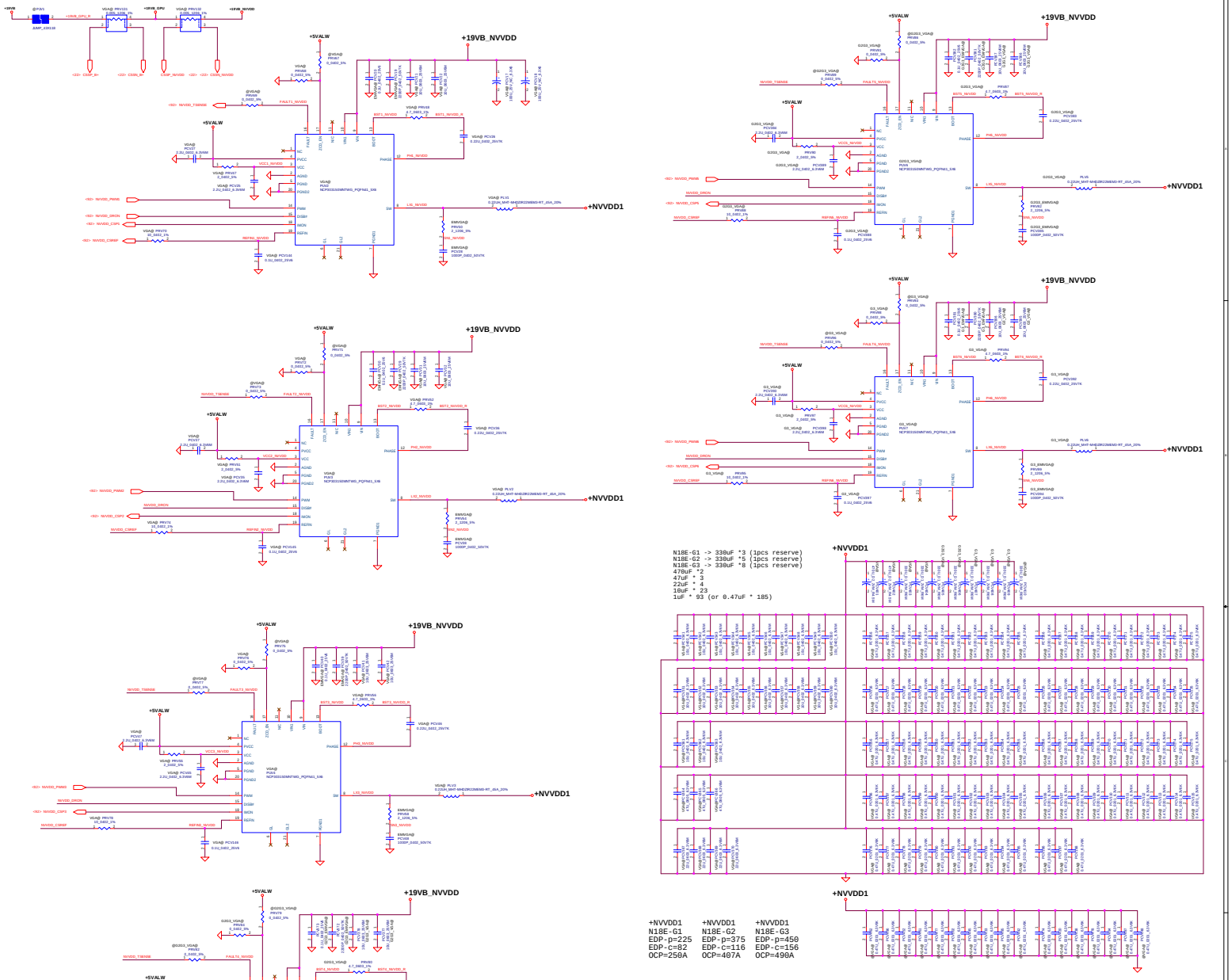
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **VGA CORE**

Size	Document Number	Rev
		0.1

Date: Friday, September 28, 2018 | Sheet 92 of 100



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/12/24	Deciphered Date	2020/09/24
			VGA CORE SW/DECOUPLING

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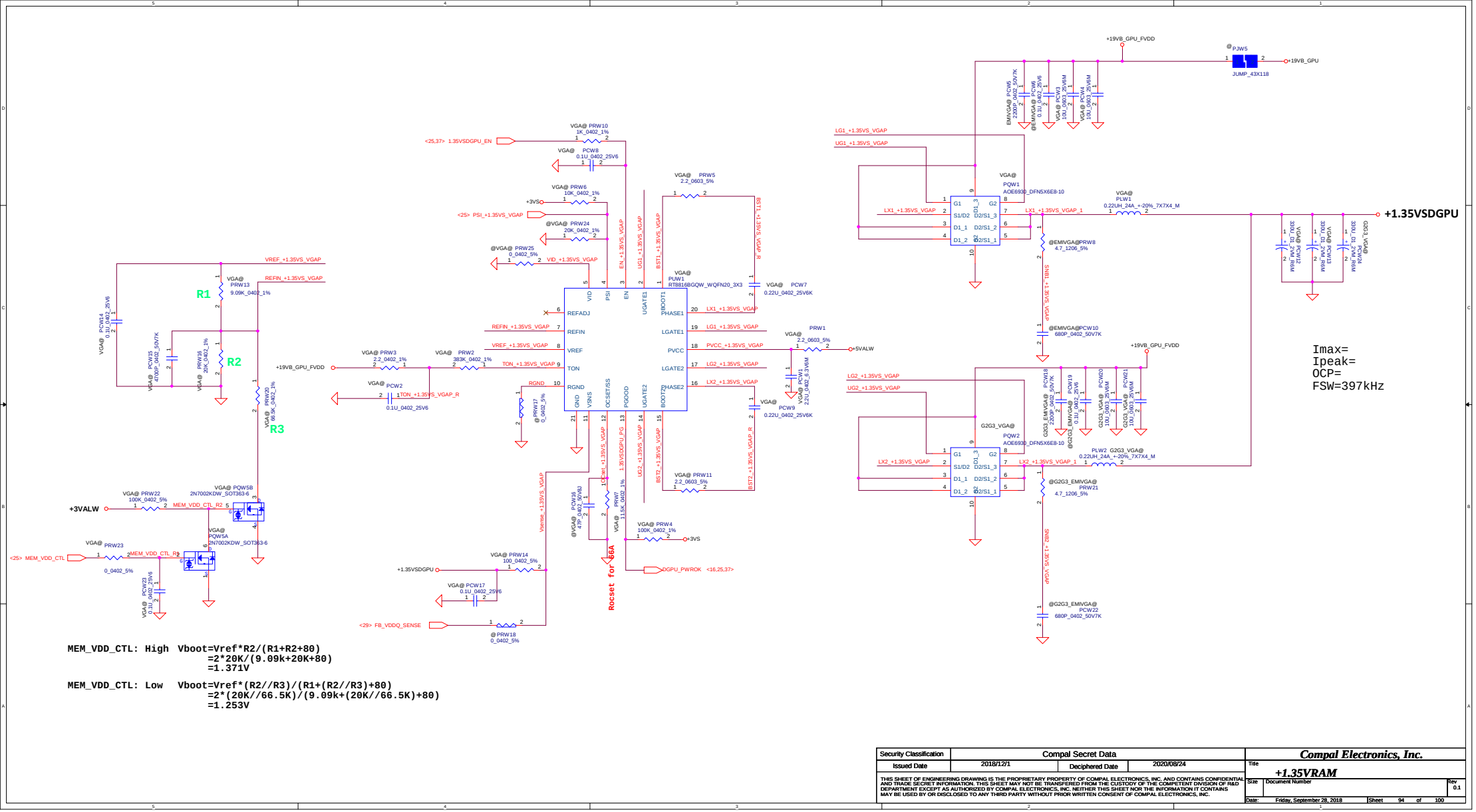
					0.4
Date:	Friday, September 06, 2013	Sheet	63	of	100



MEM_VDD_CTL: High Vboot=Vref*R2/(R1+R2+80)
=2*20K/(9.09k+20K+80)
=1.371V

MEM_VDD_CTL: Low Vboot=Vref*(R2//R3)/(R1+(R2//R3)+80)
=2*(20K//66.5K)/(9.09k+(20K//66.5K)+80)
=1.253V

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **+1.35VRAM**

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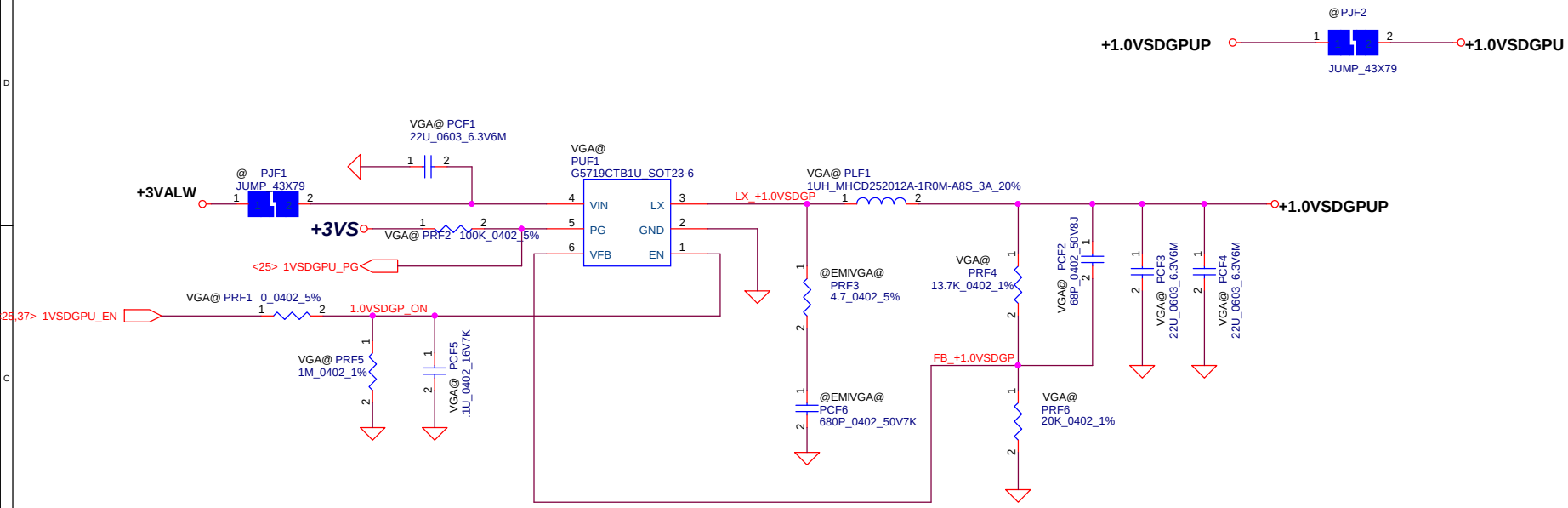
SKL_H 42



Vout=0.6V* (1+PRF4/PRF6)
Imax= 2A
Ipeak= 3A

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **+1.0VSDGPUP**

Size	Document Number	Rev
B		0.1

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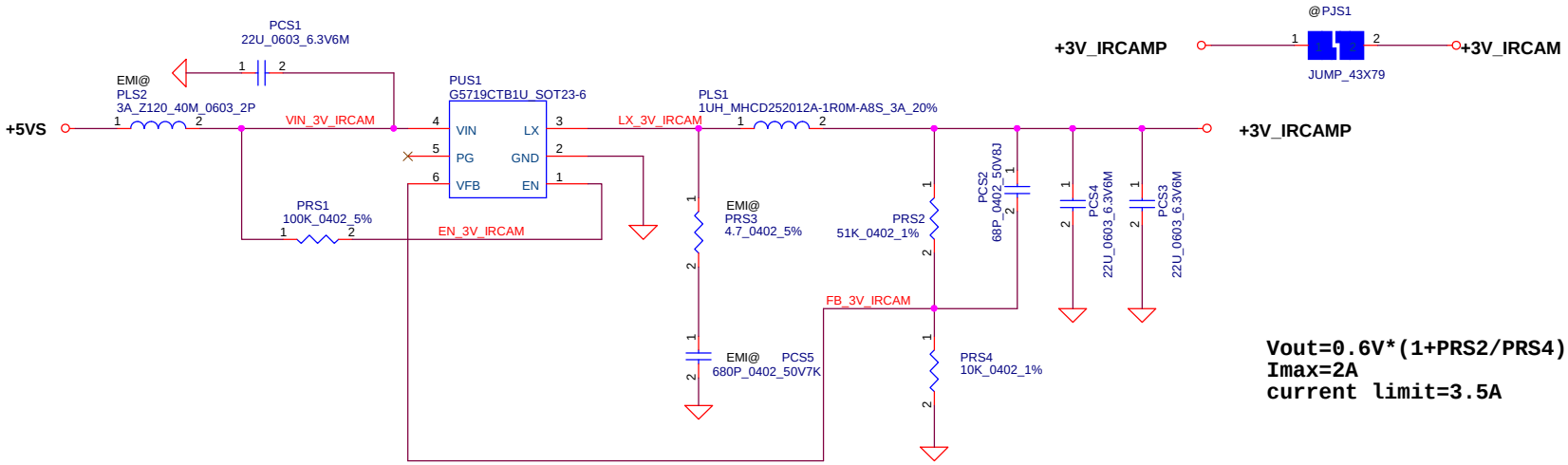


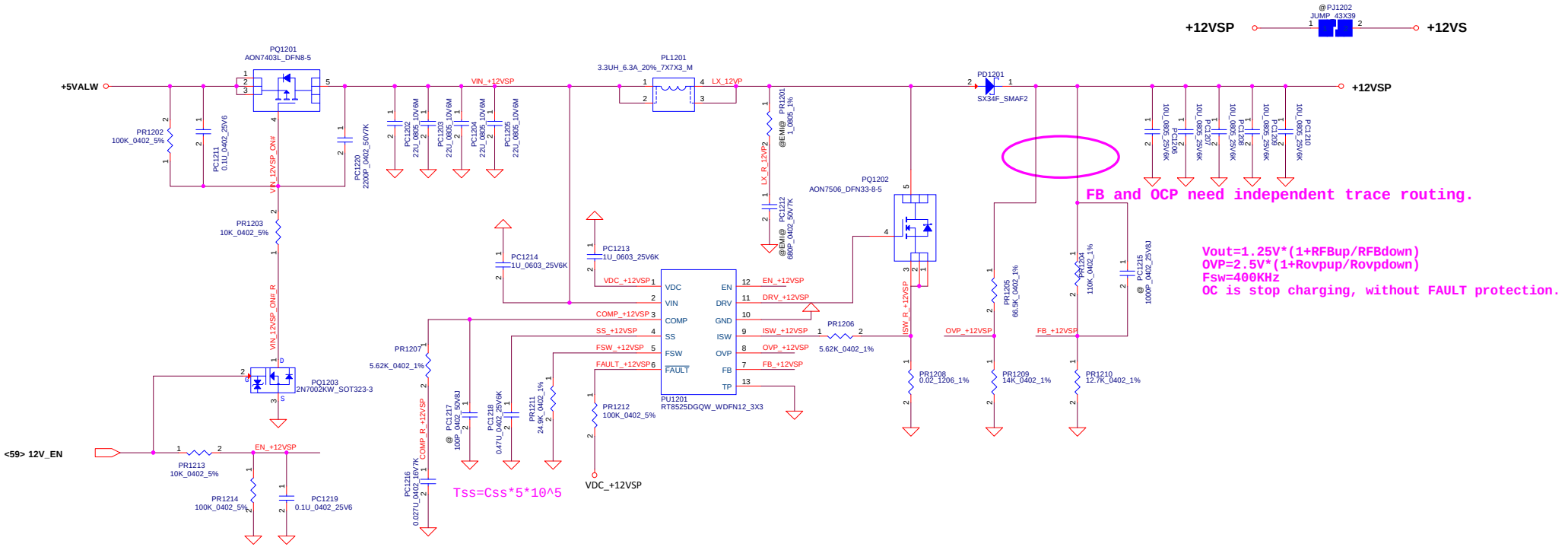
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: +3V_IRCAMP

Size	Document Number	Rev
B		0.1

Date: Friday, September 28, 2018 Sheet 96 of 100



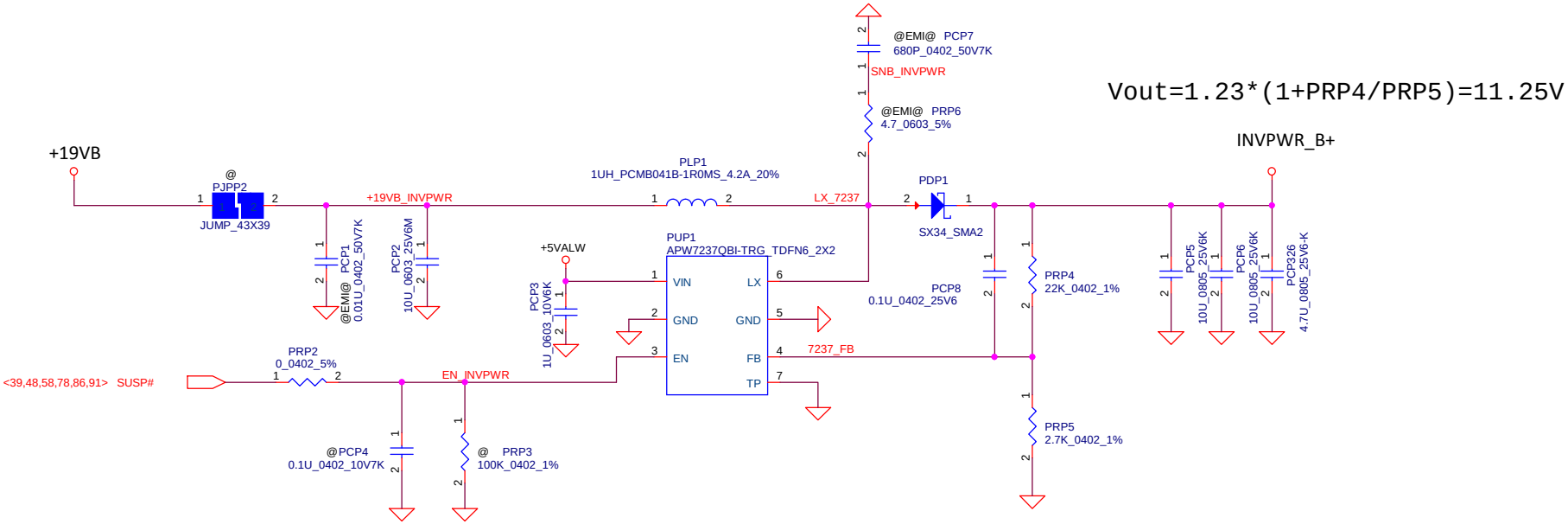
Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: +12VS

Size: Custom | Document Number | Rev: 0.1

Date: Friday, September 28, 2018 | Sheet 97 of 100



Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **INVPWR_B++**

Size	Document Number	Rev
B		0.1

Date: Friday, September 28, 2018 Sheet 98 of 100

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **PIR**

Size	Document Number	Rev
B		0.1

Date: Friday, September 28, 2018 Sheet 99 of 100

Security Classification	Compal Secret Data		
Issued Date	2018/12/1	Deciphered Date	2020/08/24

Compal Electronics, Inc.

Title: **Reserve for PWR**

Size	Document Number	Rev
B		0.1

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