

# POWER PAVILION PARFAIT INTEL SKL / KABY -H SYSTEM DIAGRAM

01

Charge	PG.40
DDR4	PG.42
CPU Core	PG.43~45
+1.0V/+1.2VSUS	PG.47~48
+3V/+5V S5	PG.41
+VGACORE	PG.49
+1.35V_GFX	PG.50

## Config#3 SODIMM 1DPC

<b>SODIMM1</b> Max. 8GB STD PG.17	DDR4 2133MHz Channel A
<b>SODIMM2</b> Max. 8GB RSV PG.18	DDR4 2133MHz Channel B

**INTEL**  
**Sky Lake - H4+2**  
**Kaby Lake - H4+2**

Processor : Quad Core  
Power : 45 (Watt)  
Package : BGA1440  
Size : 42 x 28 (mm)  
Die Size : 13.6 x 9.1 (mm)  
PG.2~8

**NVIDIA N16P-GX / N16E-GR**  
Package 29 x 29mm  
40W  
PG.19~23

**VRAM gDDR5 x 4pcs**  
256M x16 / 256M x32  
2.5GHz  
PG.14~25

**PS8409 re-driver IC**  
PG.27

**HDMI v2.0**  
PG.27

**17" eDP Panel**  
HD/FHD/UHD  
PG.26

STACKUP	
TOP	
GND	
IN1	
IN2	
VCC	
IN3	
GND	
BOT	

**M.2 2280-S3 SSD**  
PG.33

**HDD**  
PG.32

**HDD**  
PG.32

**ODD**  
PG.32

**INTEL PCH**  
**Lynx Point**

Power : Watt  
Package : FCBGA837  
Size : 23 x 23 (mm)  
PG.9~16

**USB 3.0**

**USB 3.0 Ports**  
PG.30

**USB 3.0 Ports (DB)**  
PG.30

**USB3.0 Re-Driver IC**  
PTN36241G  
PG.31

**3D CAM**  
Intel SR300 3D  
PG.31

**USB 2.0**

**USB 2.0 Ports (DB)**  
PG.30

**HD CAM**  
PG.26

**HD+ IR CAM (OPTION)**  
PG.26 + PG.34

**Touch Screen**  
Synaptics S7817  
PG.26

**LAN**  
RTL8111HSH/ Gbe  
PG.35

**Card Reader**  
RTS5237S-GR  
PG.36

**WLAN**  
BT COMBO  
PG.33

**G-Sensor**  
HP2DC  
PG.34

**ROM**  
PG.12

**KBC**  
ITE IT8987E/BX  
PG.37

**KB**  
PG.38

**TP**  
PG.38

**FAN**  
PG.38

**TPM 2.0 SLB9665TT2.0 (OPTION)**  
PG.34

**AUDIO CODEC**  
ALC3258-CG  
PG.28

**Headphone amplifier**  
HPA0022642RTJR  
PG.29

**Combo Jack (DB)**  
PG.30

**Speaker**  
PG.28

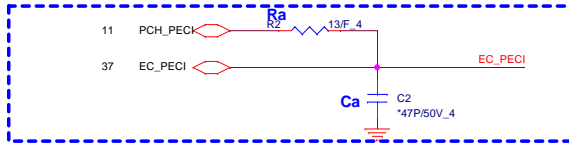
**Dual Digital MIC**  
PG.28

**3D CAM MIC / INT CAM MIC**  
PG.26

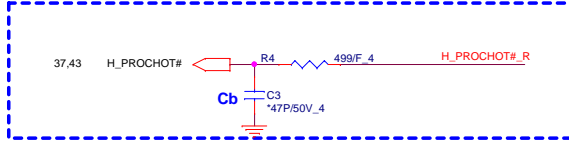
## SKYLAKE Processor (CLK,MISC,JTAG)

+1.0V 5,6,10,16,37,48  
+VCCSTPLL 6,43,47

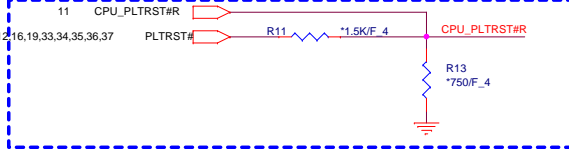
**H\_PECI (50ohm)**  
Trace Length: <0.5 inches  
Ra,Ca need placement close to PCH.



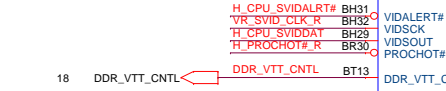
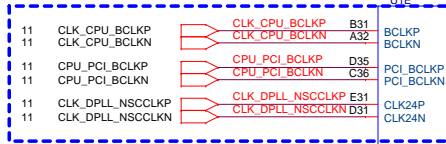
**PROCHOT# (50ohm)**  
Trace Length <11 inches  
Cb need placement near VR



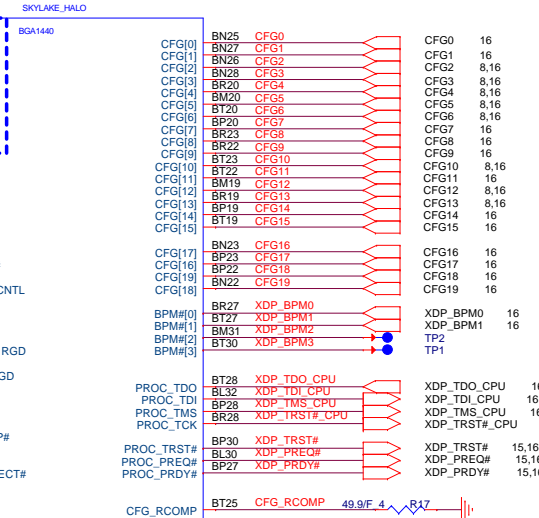
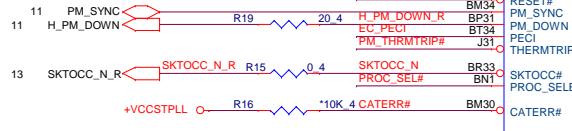
**CPU\_PLTRST# (50ohm)**  
Trace Length: 10~17 inches



**Host CLK:**  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedence 85 ohm

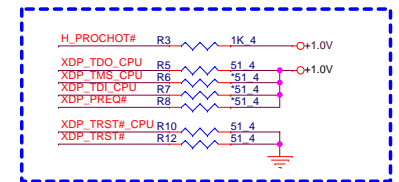


**PM\_SYNC (50ohm)**  
Trace Length: 1~11.25 inches



**Design Note(CFG\_RCOMP):**  
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

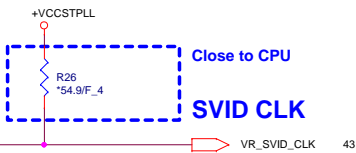
## Processor pull-up (CPU)



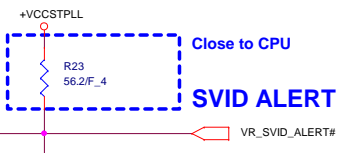
## CPU CORE SVID

Layout note:  
1.Need routing together  
2.ALERT need between CLK and DATA.

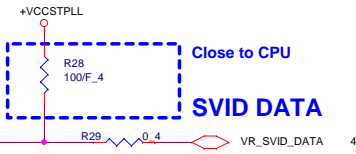
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



CLOSE TO CPU  
PLACE THE PU RESISTORS



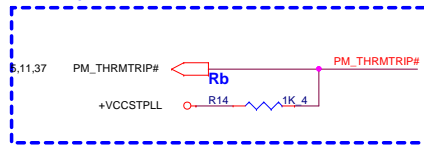
CLOSE TO CPU  
PLACE THE PU RESISTORS



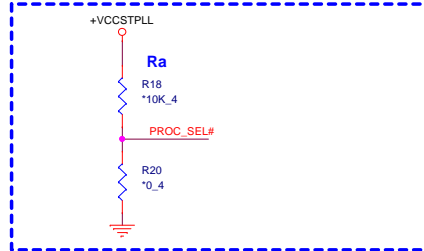
**PROCPWRGD (50ohm)**  
Trace Length: 1~11.25 inches



**THERMTRIP# (50ohm)**  
Trace Length: 1.1~12 inches  
Rb need placement near PCH

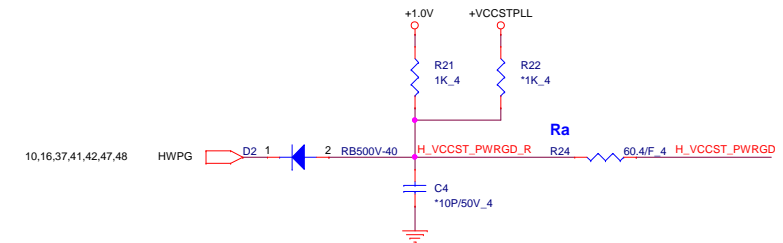


**Ra(R10804) Not install in SKL-H**



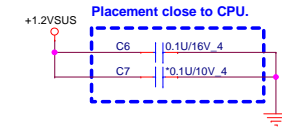
## HWPD

Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"

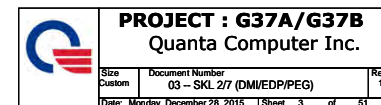


## CPU VDDQ

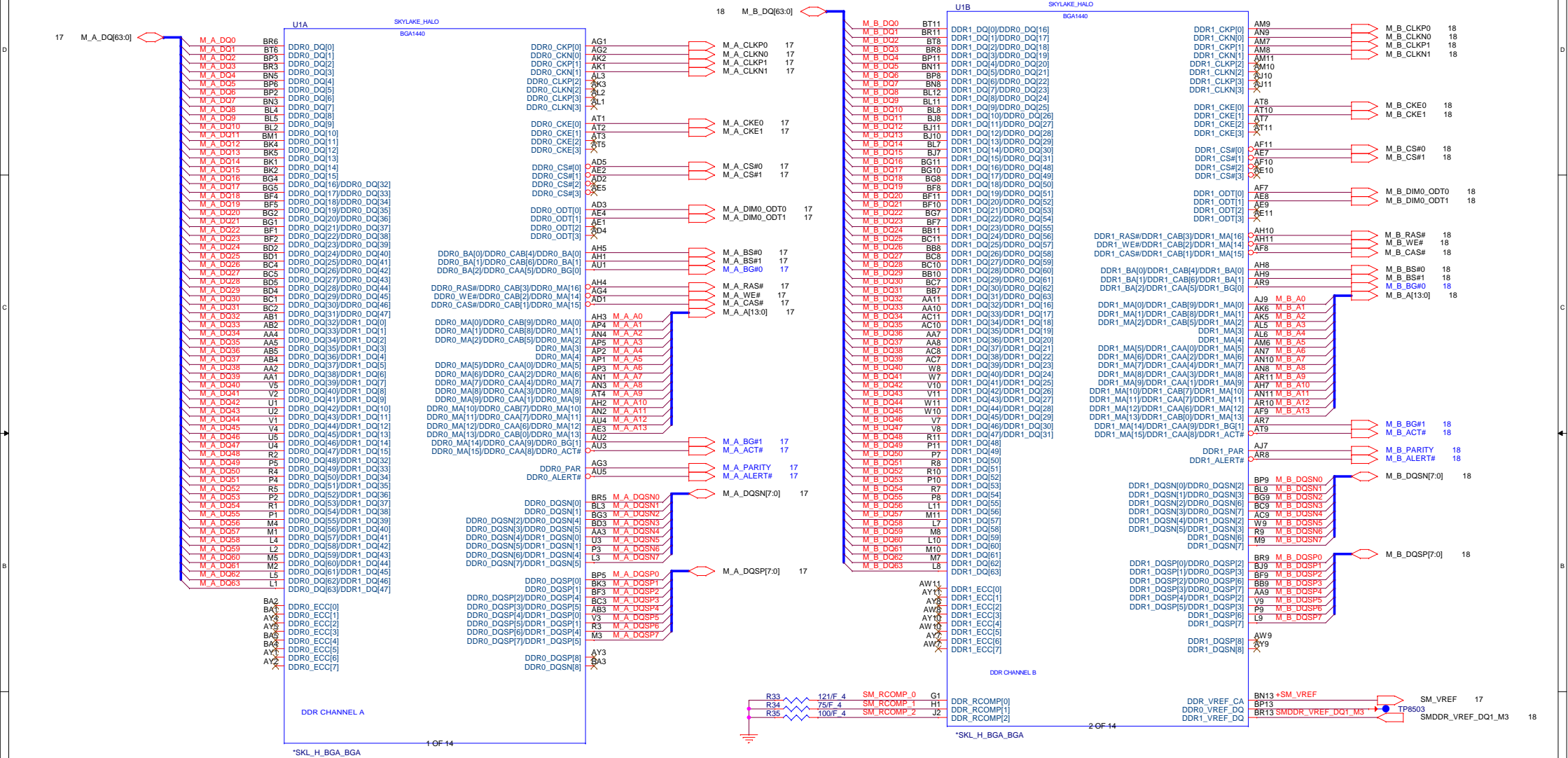
Note: please keep plane is enough for VDDQ 2.8A



PROJECT : G37A/G37B Quanta Computer Inc.		
Size Custom	Document Number 02 - SKL 1/7 (JTAG/MISC)	Rev 1A
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## SKYLAKE Processor (DDR4)



+3VPCU	10,30,33,37,38,40,41
+3V	9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.0V	2,6,10,16,37,48
+VCCGT	7,43,45

## SKYLAKE Processor (POWER)

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

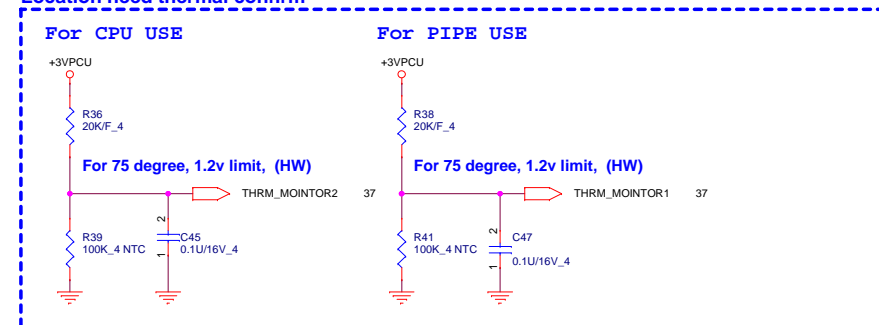
1123 Change C27, C29, C33 PN and FP from 0805 to 0603

1022 Change C27, C29, C33 PN and FP from 0603 to 0805



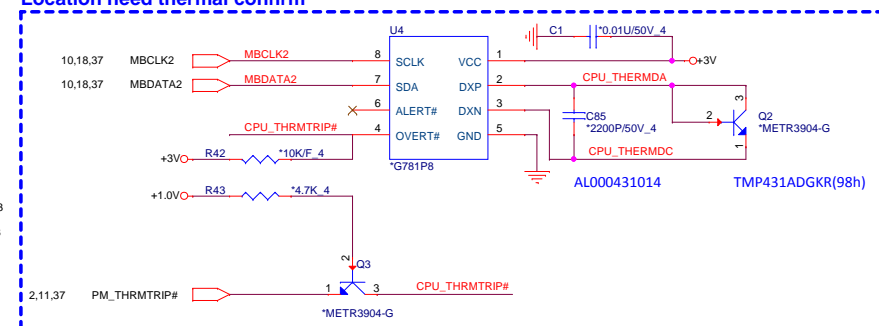
## IO Thrm Protect

Location need thermal confirm

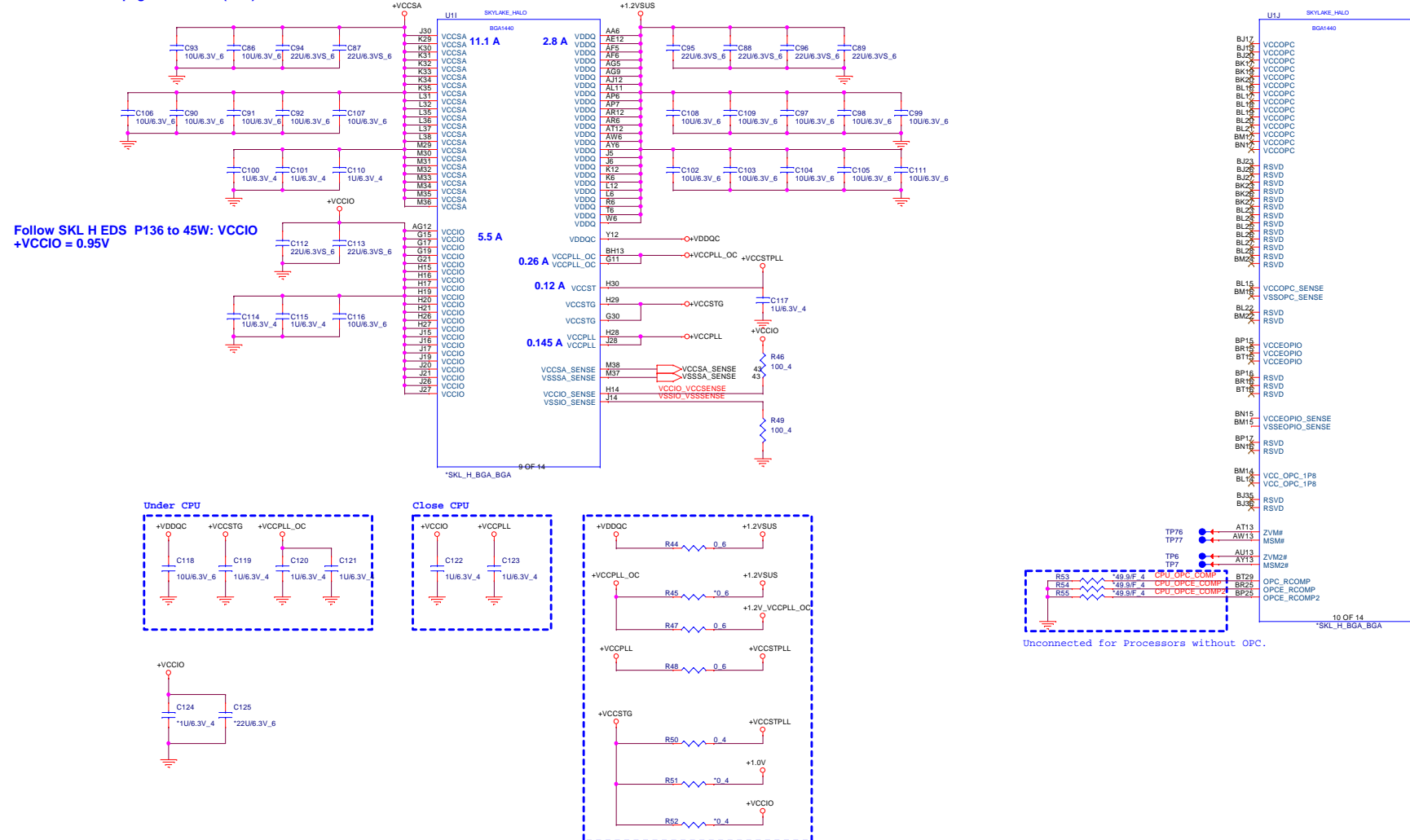


### CPU Thermal Sensor

Location need thermal confirm

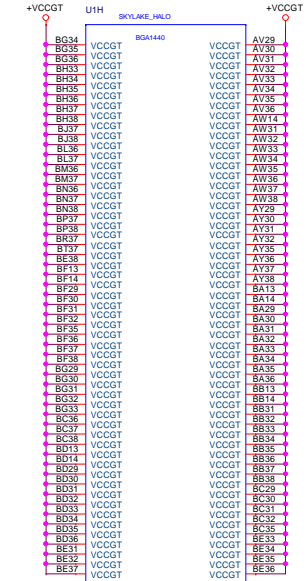
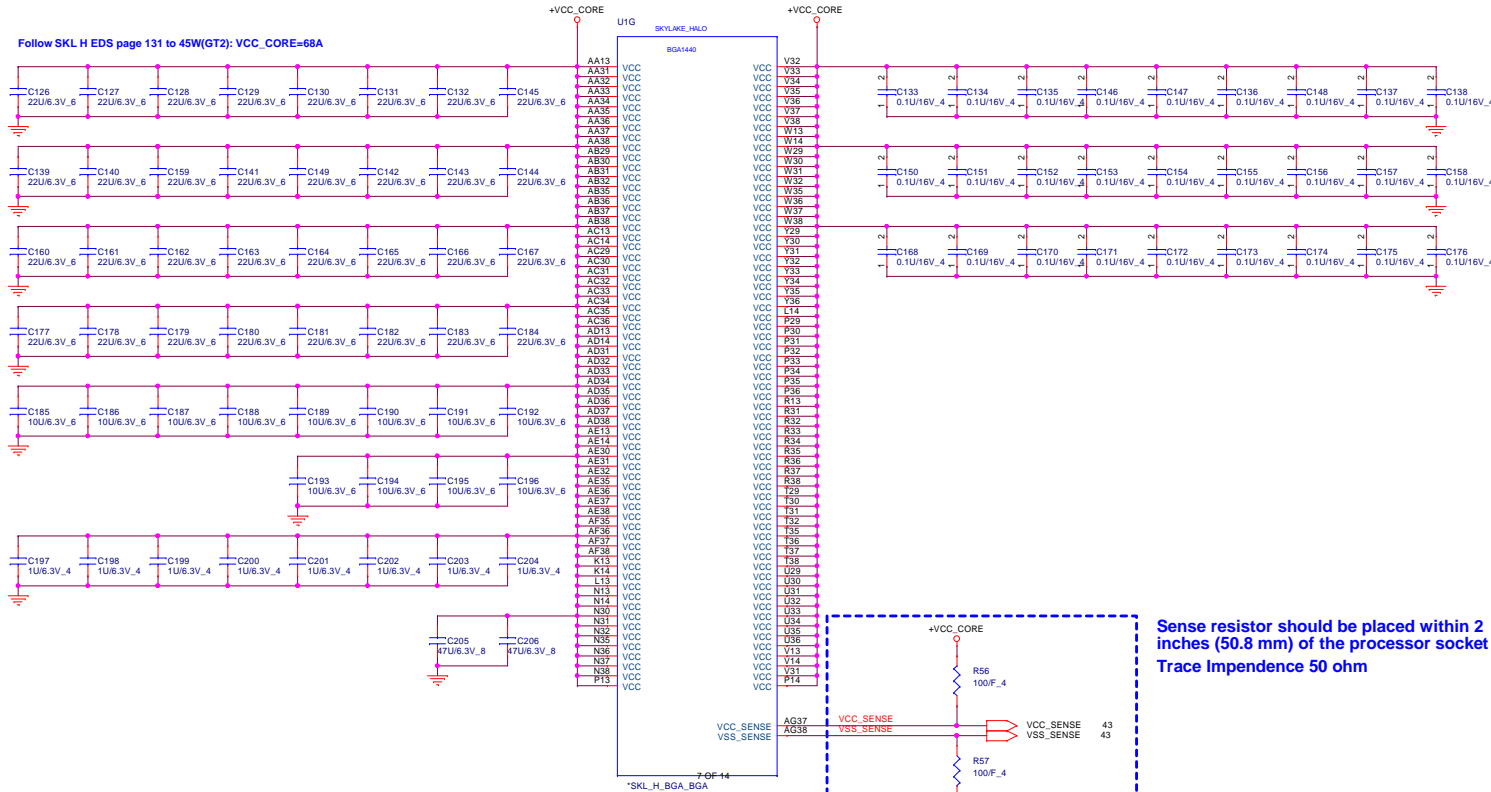


Follow SKL H EDS page 135 45W: VDDQ=2.8A



+VCC\_CORE 44  
+VCCGT 5,43,45

Follow SKL H EDS page 131 to 45W(GT2): VCC\_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm

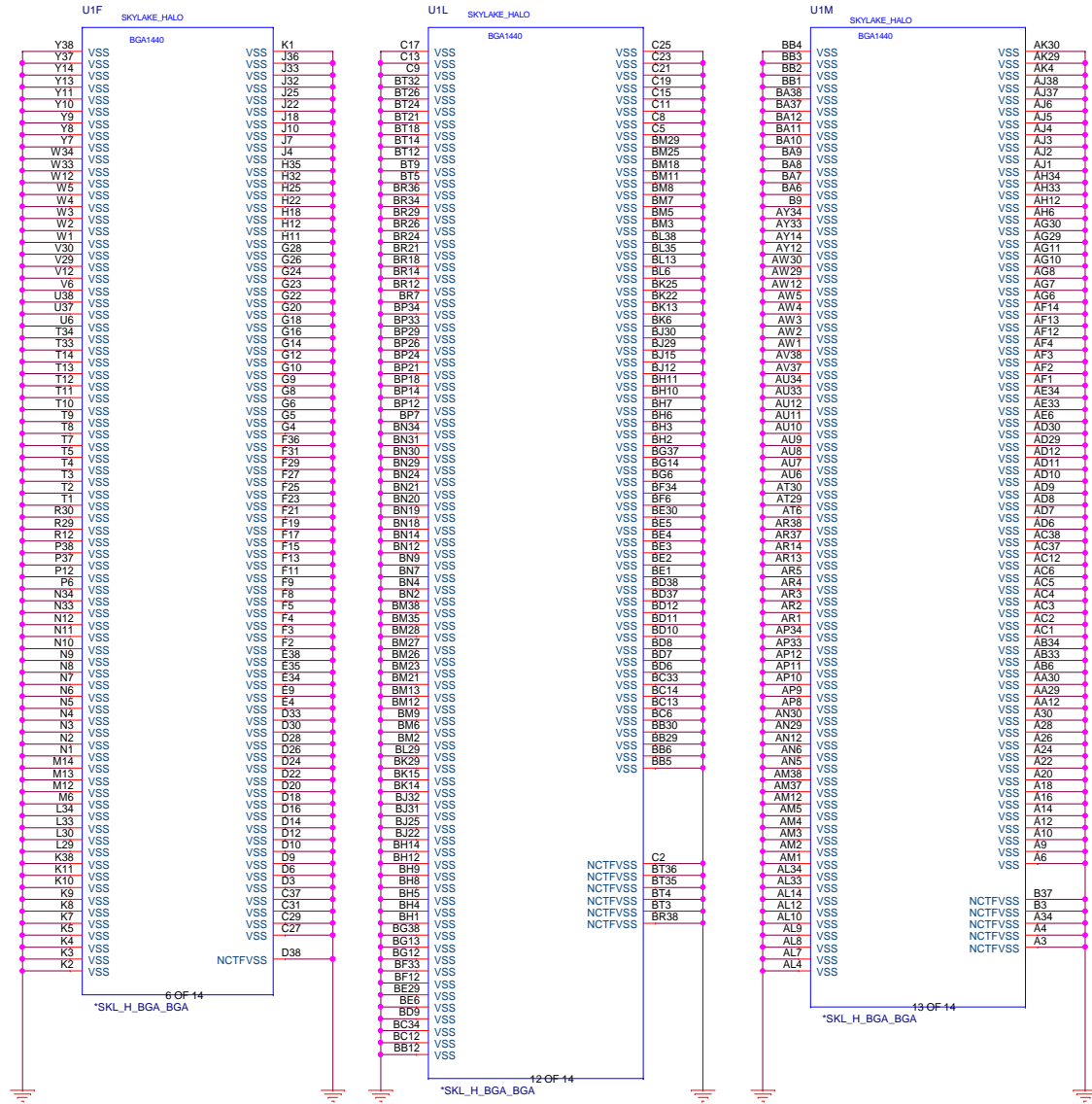


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

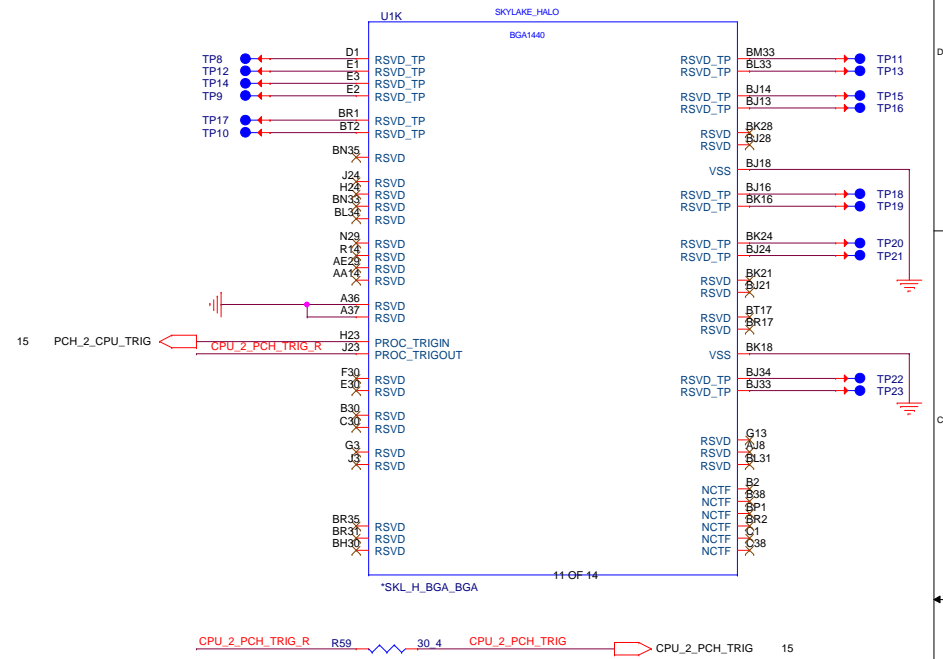
Size Custom	Document Number 07 -- SKL 6/7 (POWER&GND)	Rev 1A
Date: Monday, December 28, 2015		Sheet 7 of 51



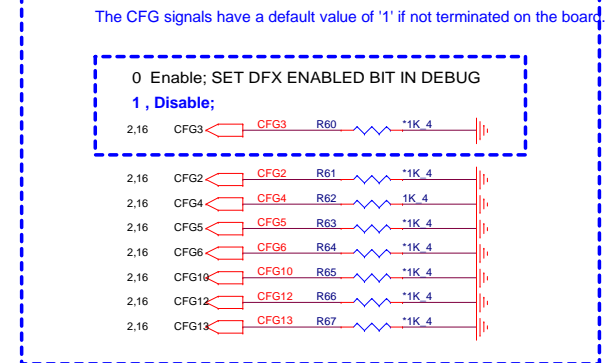
SKL-HProcessor (GND)



SKL-H Processor (RESERVED, CFG)



Processor Strapping







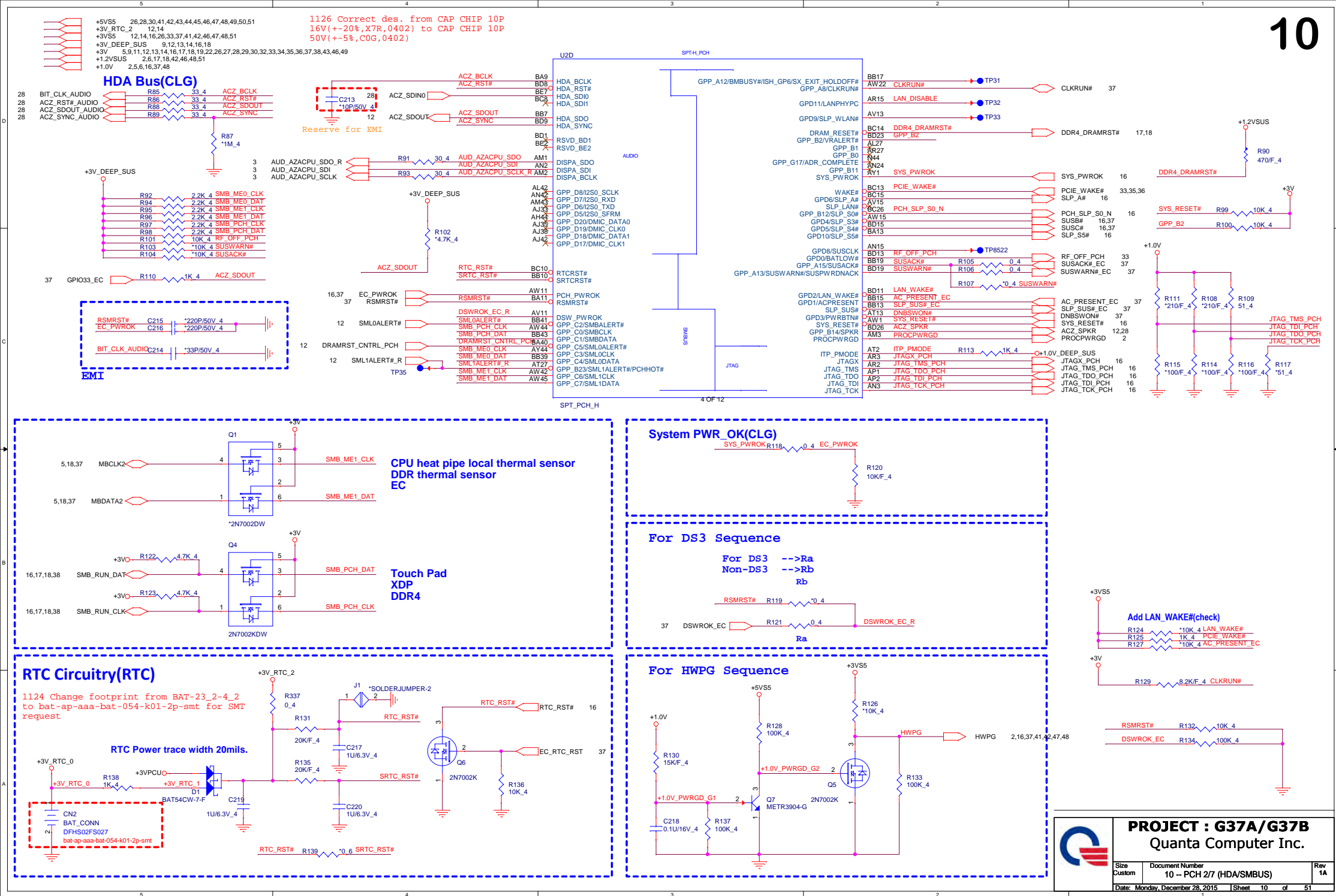
USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	NC
PORT4	3D CAMERA

**BOM: HW TPM need Ra, Rc Stuff**

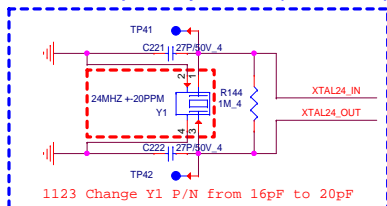


**PROJECT : G37A/G37B**  
Quanta Computer Inc.

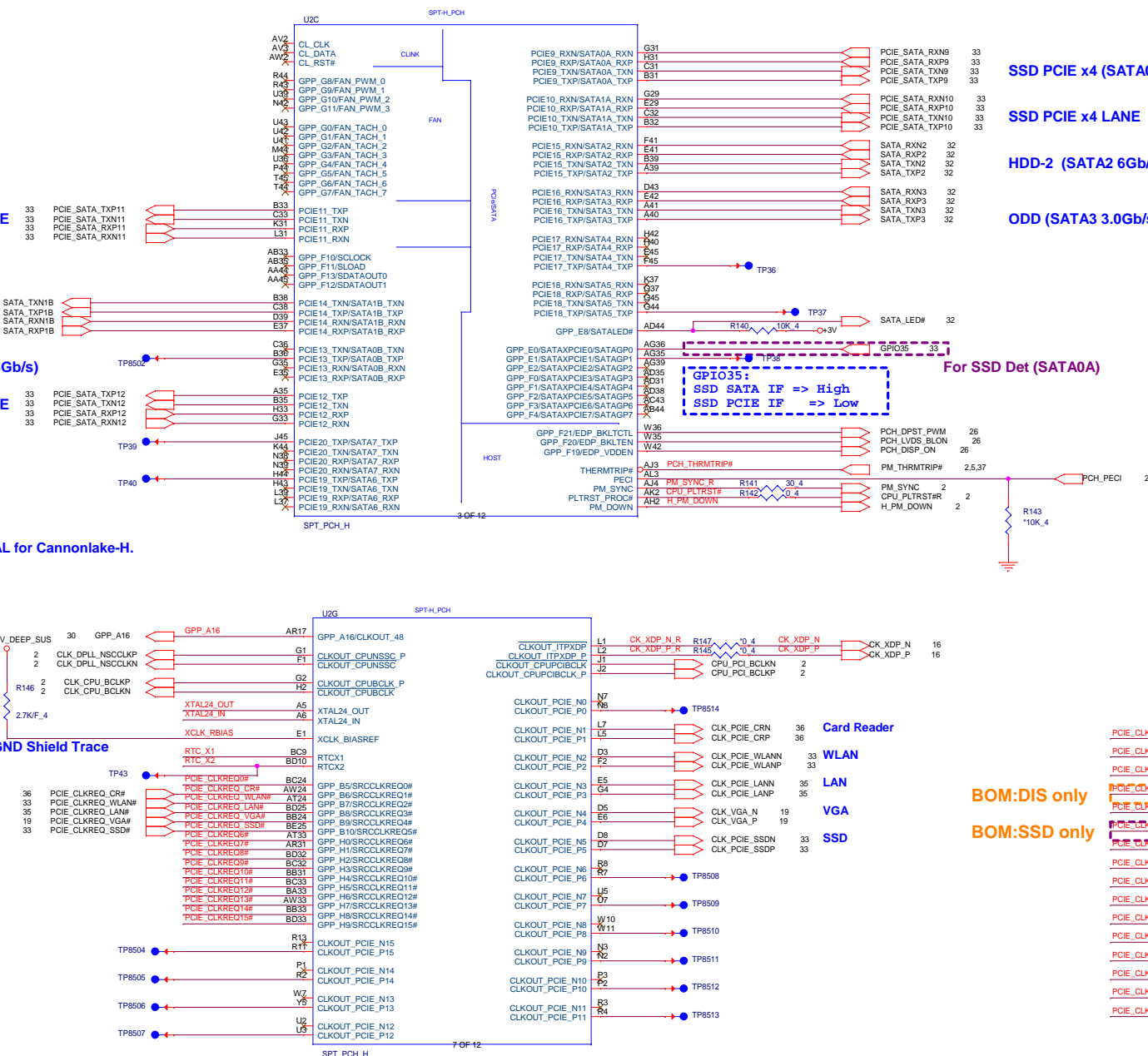
Size Custom	Document Number 09 -- PCH 1/7 (DMI/USB/PCIE)	Rev 1A
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HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	SSD PCIE x 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	HDD-1
PCIE15	HDD-2
PCIE16	ODD
PCIE17	NC
PCIE18-20	NC



12/28 Change C223, C224 PN from CH01806JB07 to CH01506JB06 for XTAL vendor suggest



ODD (SATA3 3.0Gb/s)

For SSD Det (SATA0A)

BOM:SSD only

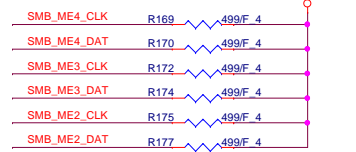
**BOM:SSD only**

PCIE_CLKREQ_WLAN#	R148	10K_4
PCIE_CLKREQ_LAN#	R149	10K_4
PCIE_CLKREQ_CR#	R151	10K_4
PCIE_CLKREQ_VGA#	R152	10K_4
PCIE_CLKREQ0#	R153	10K_4
PCIE_CLKREQ0_SSD	R154	10K_4
PCIE_CLKREQ0#	R155	10K_4
PCIE_CLKREQ07#	R156	10K_4
PCIE_CLKREQ08#	R157	10K_4
PCIE_CLKREQ09#	R158	10K_4
PCIE_CLKREQ10#	R159	10K_4
PCIE_CLKREQ11#	R160	10K_4
PCIE_CLKREQ12#	R161	10K_4
PCIE_CLKREQ13#	R163	10K_4
PCIE_CLKREQ14#	R164	10K_4
PCIE_CLKREQ15#	R165	10K_4



**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number 11 – PCH 3/7 (SATA/LPC/CLK)
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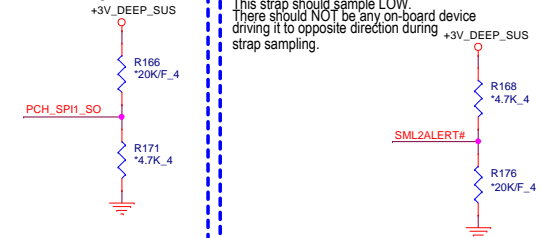
## RESERVED

- This strap should sample HIGH.
- There should NOT be any on-board device driving it to opposite direction during strap sampling.

+3V<sub>DEEP</sub>

ESPI FLASH SHARING MODE

HIGH: SLAVE ATTACHED FLASH SHARING  
 LOW: 0: MASTER ATTACHED FLASH SHARING  
 This strap should sample LOW.  
 There should NOT be any on-board device  
 driving it to opposite direction during +3V\_DEEP\_SUS  
 strap sampling.



TP47	PCH_SPI_CS0#_R
TP48	PCH_SPI1_CLK_R
TP49	PCH_SPI1_SI_R
TP50	PCH_SPI1_SO_R
TP51	BIOS_WP#
TP52	HOLD#

37 PCH\_SPI\_CS0#\_R PCH\_SPI\_CS0#\_R  
 37 PCH\_SPI\_CLK\_L PCH\_SPI\_CLK\_L  
 37 PCH\_SPI\_SI\_R PCH\_SPI\_SI\_R  
 37 PCH\_SPI\_SO\_R PCH\_SPI\_SO\_R

+3V5S R197 0.4  
 +3V\_DEEP\_SUS R200 0.4

PCH\_SPI\_CS0#\_R201 15/F 4 PCH\_SPI\_CS0#\_R  
 PCH\_SPI\_CLK\_L202 15/F 4 PCH\_SPI\_CLK\_L  
 PCH\_SPI\_SI\_R203 15/F 4 PCH\_SPI\_SI\_R  
 PCH\_SPI\_SO\_R205 15/F 4 PCH\_SPI\_SO\_R

C225 22P/50V\_4  
 C226 0.1U/16V

U5  
 1 VDD  
 6 CE#  
 5 SI  
 2 SO  
 7 HOLD#  
 3 WP#  
 4 VSS

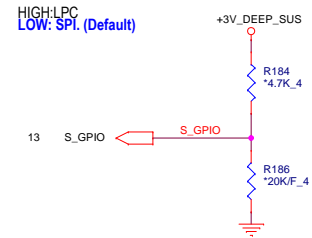
W25Q64FVSSIQ  
 AKE3EFPN07

R204 1K 4  
 R206 15/F 4  
 PCH\_SPI\_IO3

1U/6.3V\_4+3VSP R211 1K 4  
 PCH\_SPI\_IO2 R212 15/F 4 BIOS\_WP#

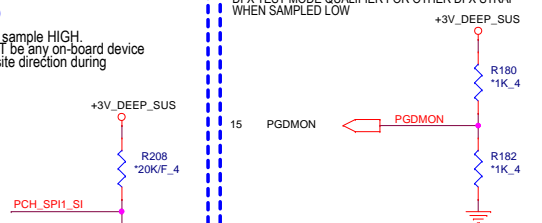
1123 Change U5 P/N from Socket to ROM

HIGH: LPC  
LOW: SPI. (Default)



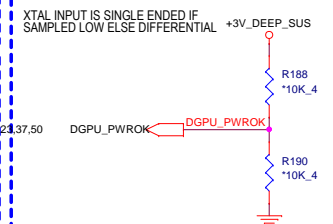
## RESERVED

- This strap should sample HIGH.
- There should NOT be any on-board device driving it to opposite direction during strap sampling.

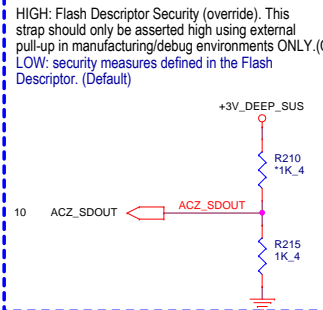


DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF  
SAMPLED LOW ELSE DIFFERENTIAL +3V\_DEEP\_SUS

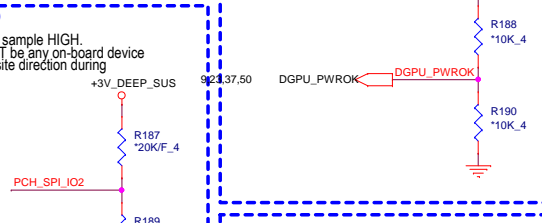


HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRB)  
LOW: security measures defined in the Flash Descriptor. (Default)

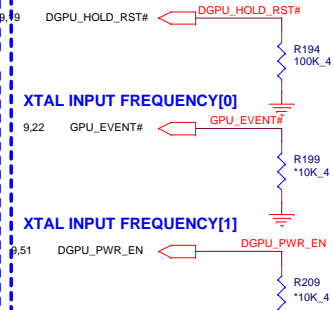


## RESERVED

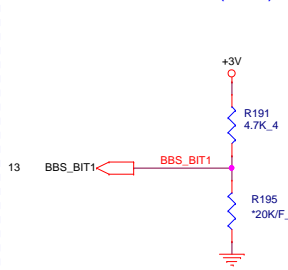
- This strap should sample HIGH.
- There should NOT be any on-board device driving it to opposite direction during strap sampling.
- +3V\_DEEP



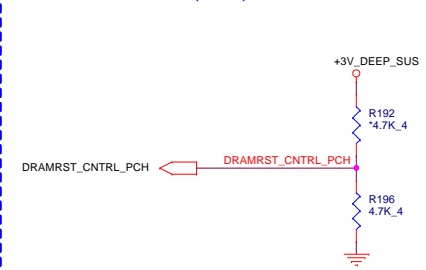
## RING OSCILLATOR BYPASS



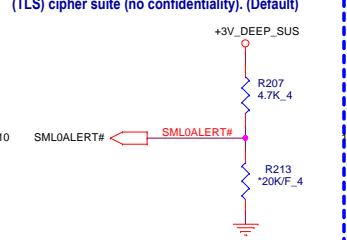
HIGH:TOP SWAP ENABLED (CRB)  
LOW: Disable "No Reboot" mode. (Default)



HIGH: eSPI Is selected for EC.  
LOW: LPC Is selected for EC. (Default)

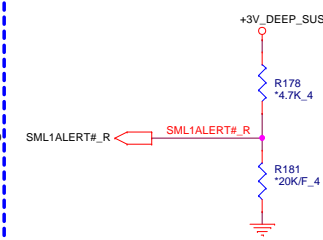


**LOW:** Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)



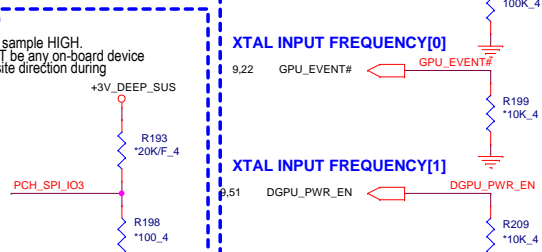
## RESERVED

This strap should sample LOW.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



## RESERVED

This strap should sample HIGH.  
 There should NOT be any on-board device  
 driving it to opposite direction during  
 strap sampling.

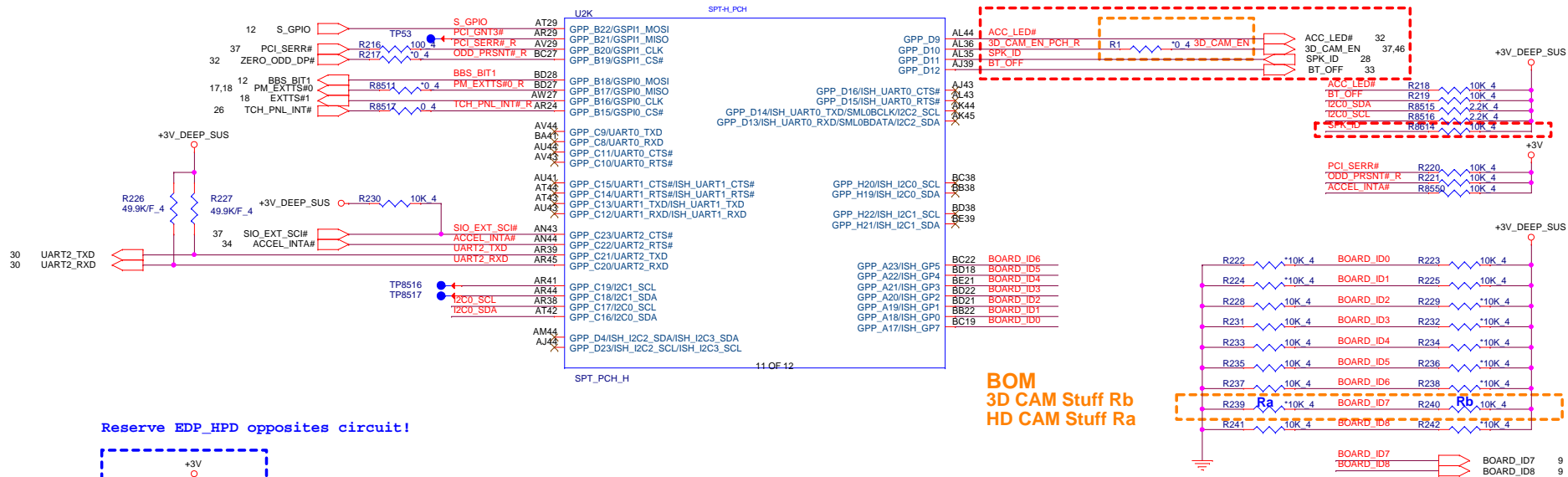


**PROJECT : G37A/G37B**  
Quanta Computer Inc.

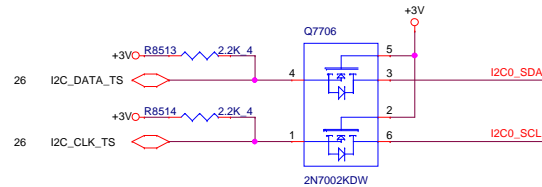
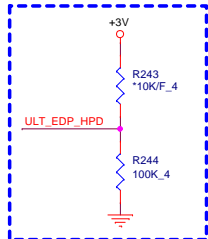
Size Custom	Document Number 12 -- PCH 4/7 (GPIO/MISC)	Rev 1A
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1123 Change PCH GPP\_D11 Net name from RF\_OFF to SPK\_ID and  
PU10K to +3V\_DEEP\_SUS for SPK Vendor ID used

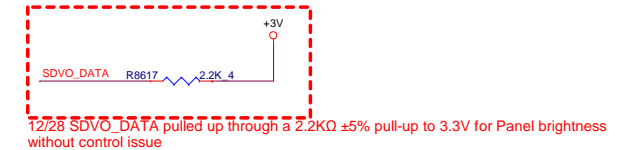
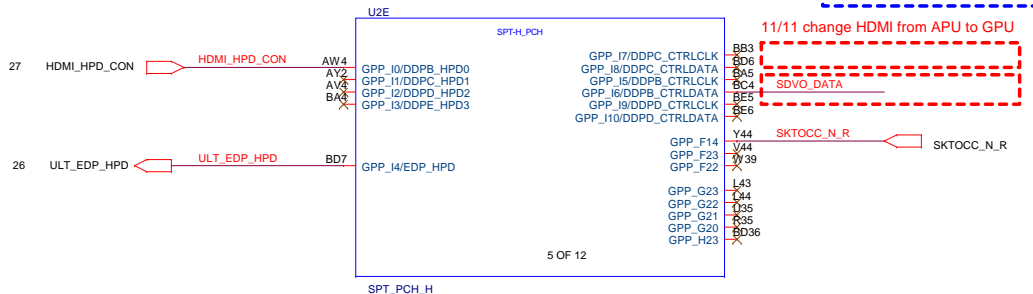
### 3D CAMERA BOM: 3D CAM Un-Stuff (EN will from EC control)



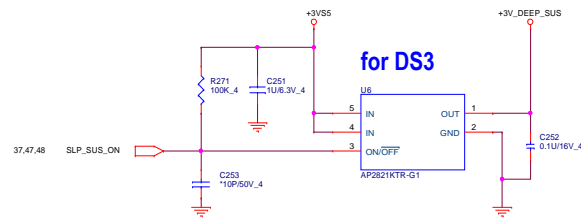
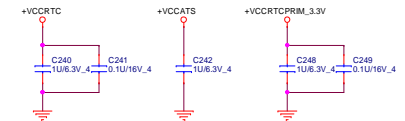
Reserve EDP\_HPD opposites circuit!



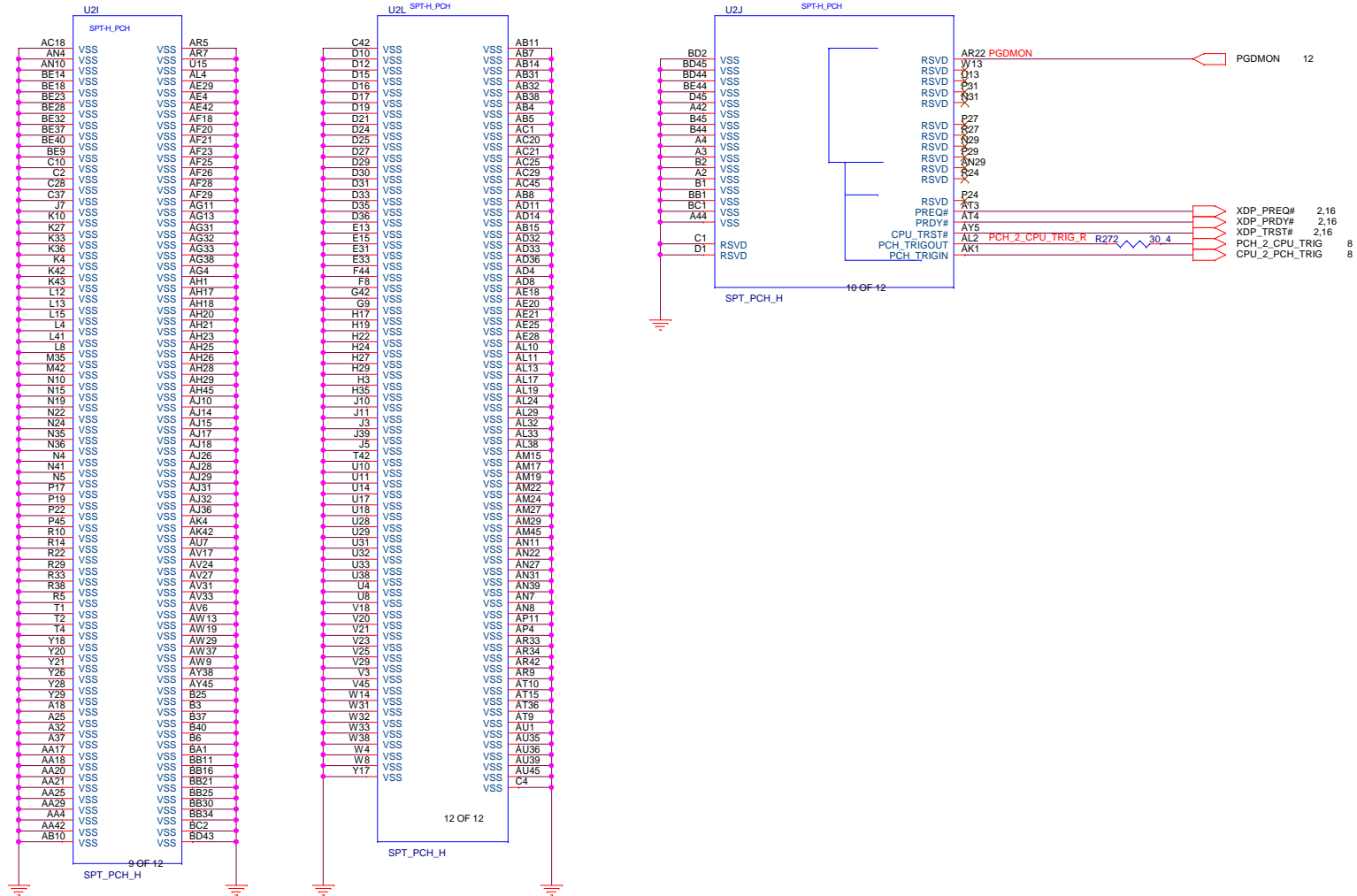
This signal has a weak internal pull-down.  
0 = Port C and D is not detected.  
1 = Port C and D is detected.



12/28 SDVO\_DATA pulled up through a 2.2KΩ ±5% pull-up to 3.3V for Panel brightness without control issue









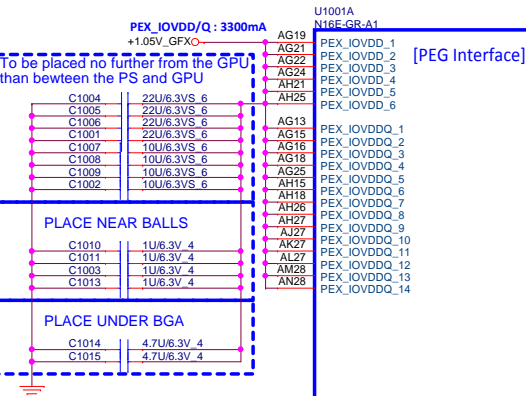


Size	Document Number <b>16 – XDP &amp; APS</b>	Rev 1A
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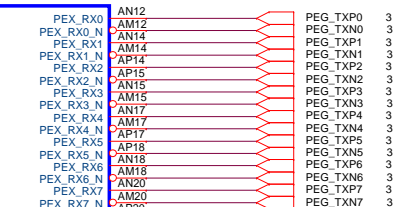
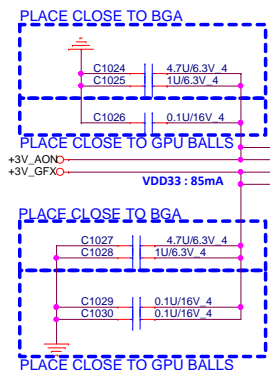




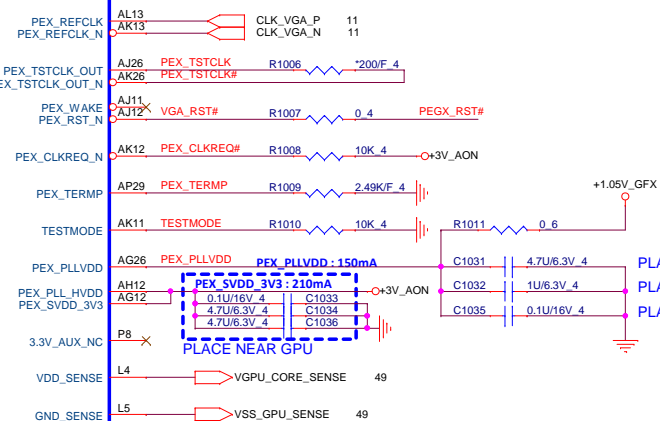
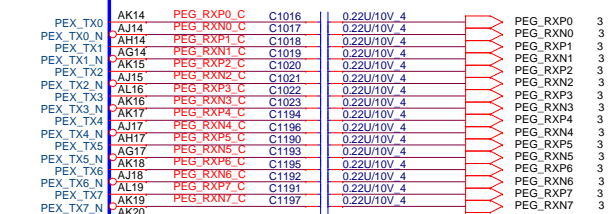
+3V 5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49  
 +3V\_AON 22,23,27,51  
 +3V\_GFX 20,21,22,23,49,51  
 +1.05V\_GFX 20,21,23,51



AC6 NC.1  
 AJ28 NC.2  
 NC.3  
 AJ5 NC.4  
 AL11 NC.5  
 C15 NC.6  
 D19 NC.7  
 NC.8  
 D23 NC.9  
 NC.10  
 H31 NC.11  
 T8 NC.12  
 NC.13  
 V32



1126 Change D1004,R1124 from I to NI  
 Change U1002,R1002,C1012 from NI to I

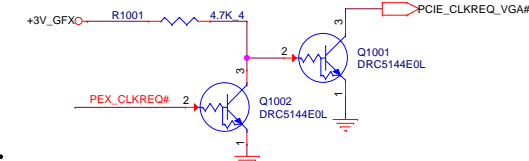
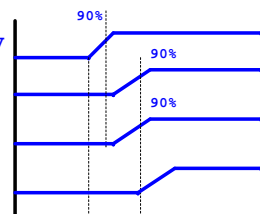


All 3.3V

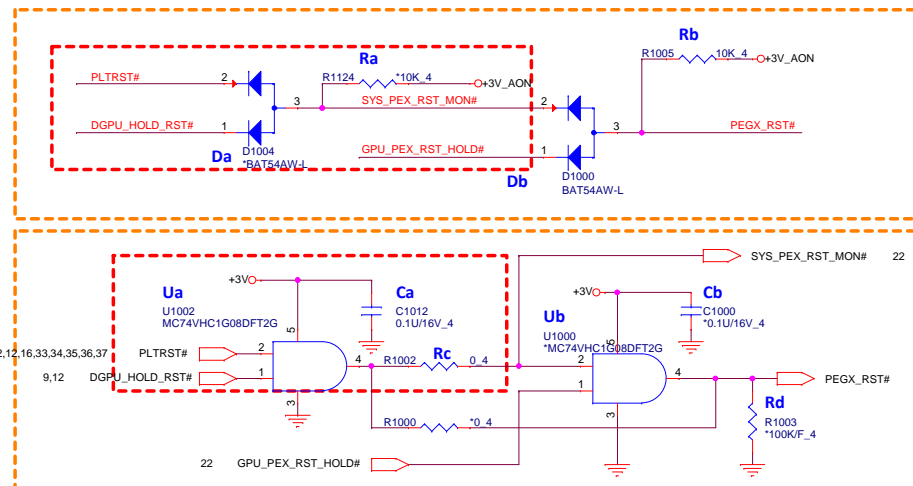
NVVDD

PEX\_VDD  
1.05V

FBVDD/Q



If stuff Da,Db,Ra,Rb, do not stuff Ua,Ub,Ca,Cb,Rc,Rd



GPU type	Part Number	Part Description	Where Used
N16P-GT	AJ0N16P0T05	IC CTRL(908P)N16P-GT-A2(BGA)TOPBSQ	G35A
	AJ0N16P0T06	IC CTRL(908P)N16P-GT-A2(BGA)QBCON	
N16P-GX	AJ0N16P0T14	IC CTRL(908P)N16P-GX-A2(BGA)TOPBSQ	G35A / G37A
	AJ0N16P0T15	IC CTRL(908P)N16P-GX-A2(BGA)QBCON	
N16E-GR	AJ0N16E0T02	IC CTRL(908P)N16E-GR-A1(BGA)TOPBSQ	G35A / G37A
	AJ0N16E0T03	IC CTRL(908P)N16E-GR-A1(BGA)QBCON	

+3V\_GFX 19,21,22,23,49,51  
+1.35V\_GFX 23,24,25,50  
+1.05V\_GFX 19,21,23,51  
NV\_PLLVDD 21

U1001B  
N16E-GR-A1

U1001C  
N16E-GR-A1

[MEMORY I/F A]

MEMORY I/F C

GDDR5 NO USE

GDDR5 NO USE

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

MUST BE on GPU ball

PROJECT : G37A/G37B  
Quanta Computer Inc.

Size Custom Document Number N16P-GX/GT - 2/5 (Memory) Rev 1A  
Date: Monday, December 28, 2015 Sheet 20 of 51





Resistor Values	PU to 3V3_MAIN	PD to GND
4.99K OHM	1000	0000
10K OHM	1001	0001
15K OHM	1010	0010
20K OHM	1011	0011
24.9K OHM	1100	0100
30.1K OHM	1101	0101
34.8K OHM	1110	0110
45.3K OHM	1111	0111

VRAM Table of N16P-GX      N16P-GX device ID = 0x139B

Vendor	TOP B/S	Mfr. P/N	SIZE	ROM_SI
	QBCON			
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8K
	AKG5PWUTW20			
Micron	AKG5PW0TL05	EDW4032BABG-60-F-D	256Mx32	0x4 0100 PD 24.9K
	AKG5PW0TL06			
Micron	AKG5LGUTL02	MT51J256M32HF-60:A	256Mx32	0x9 1001 PU 10K
	AKG5LGUTL03			
Samsung	AKG5QGDT503	K4G80325FB-HC03	256Mx32	0x8 1000 PU 4.99K
	AKG5QGDT504			

VRAM Table of N16E-GR      N16E-GR device ID = 0x1427

Vendor	TOP B/S	Mfr. P/N	SIZE	ROM_SI
	QBCON			
Hynix	AKG5PWUTW19	H5GC4H24AJR-T2C	256Mx16	0x0
	AKG5PWUTW20			0000 PD 4.99K
Micron	AKG5PW0TL05	EDW4032BABG-60-F-D		0x1
	AKG5PW0TL06			0001 PD 10K
Micron	<b>AKG5LGUTL02</b>	<b>MT51J256M32HF-60:A</b>	<b>256Mx32</b>	<b>0x4</b>
	AKG5LGUTL03			<b>0100</b> <b>PD 24.9K</b>
Samsung	AKG5QGDT503	K4G80325FB-HC03		0x3
	AKG5QGDT504			0011 PD 20K

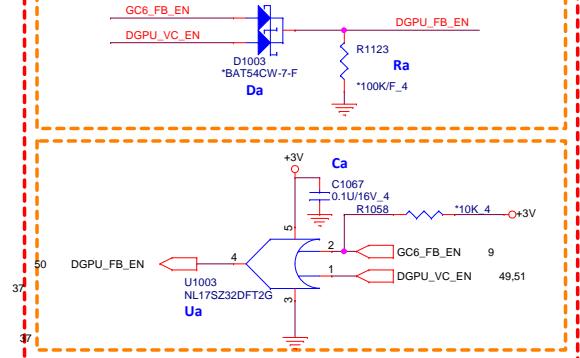
1126 Change D1003, R1123 from I to NI  
Change U1003, C1067 from NI to I

If stuff Da,Ra, do not stuff Ua,Ca

```

11 still da,ka, do not still ba,ca
12 -----

```

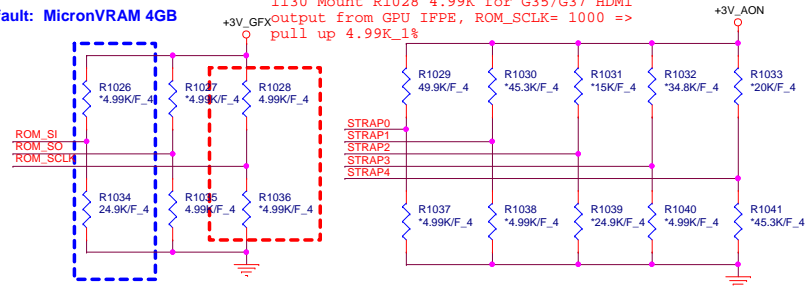


**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number N16E-GR - 4/5 (MISC)	Rev 1A
Date: Monday, December 28, 2015	Sheet 22 of 51	



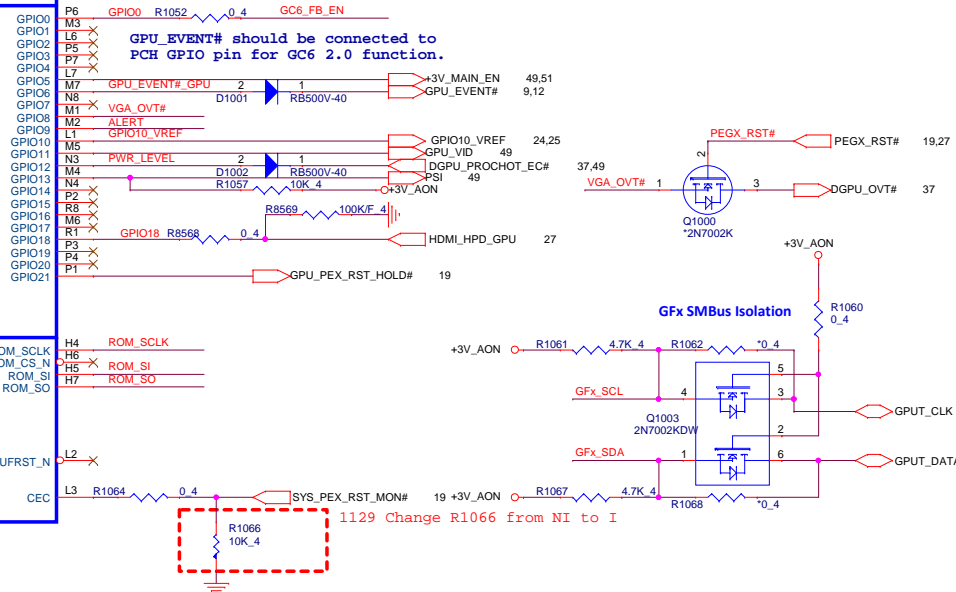
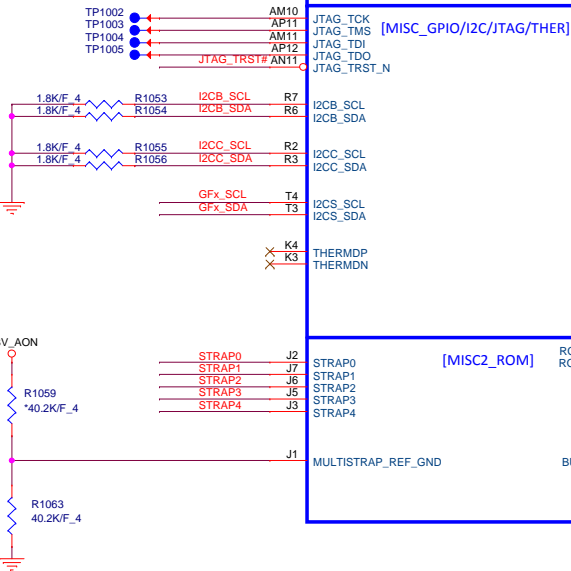
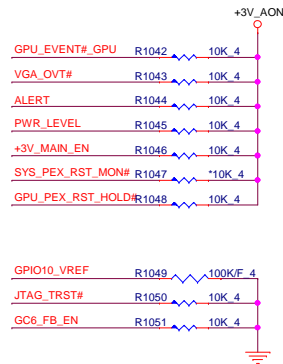
**Default: MicronVRAM 4GB**



GPU Netname	N16P-GT	N16P-GX	N16E-GX
ROM_SO	4.99K PD	4.99K PD	4.99K PD
ROM_SCLK	4.99K PU	4.99K PU	4.99K PU
STRAP0	49.9K PU	49.9K PU	49.9K PU
STRAP1	NC	NC	NC
STRAP2	NC	NC	NC
STRAP3	NC	NC	NC
STRAP4	NC	NC	NC

VRAM Table of N16P-GT      N16P-GT device ID = 0x139A

Vendor	TOP B/S	Mfr. P/N	SIZE	ROM_SIZE
	QBCON			
Hynix	AKG5PWUTW19 AKG5PWUTW20	H5GC4H24AJR-T2C	256Mx16	0x6 0110 PD 34.8
Micron	AKG5PW0TL05 AKG5PW0TL06	EDW4032BABG-60-F-D		0x4 0100 PD 24.9





**+VGACORE**

Part Number	Value	Location
C1068	1U/E.3V 4	PLACE UNDER GPU
C1069	1U/E.3V 4	
C1070	1U/E.3V 4	
C1071	1U/E.3V 4	
C1072	1U/E.3V 4	
C1073	1U/E.3V 4	
C1074	1U/E.3V 4	
C1075	1U/E.3V 4	
C1076	4.7U/E.3V 4	
C1077	4.7U/E.3V 4	
C1078	4.7U/E.3V 4	
C1079	4.7U/E.3V 4	
C1080	4.7U/E.3V 4	
C1081	4.7U/E.3V 4	
C1082	4.7U/E.3V 4	
C1083	4.7U/E.3V 4	
C1084	4.7U/E.3V 4	
C1085	4.7U/E.3V 4	
C1086	4.7U/E.3V 4	
C1087	4.7U/E.3V 4	
C1088	4.7U/E.3V 4	
C1089	4.7U/E.3V 4	
C1090	4.7U/E.3V 4	
C1091	22U/E.3VS 6	PLACE NEAR GPU
C1092	22U/E.3VS 6	
C1093	22U/E.3VS 6	
C1094	22U/E.3VS 6	
C1095	22U/E.3VS 6	
C1096	22U/E.3VS 6	
C1097	22U/E.3VS 6	
C1098	*4.7U/E.3V 6	
C1099	*4.7U/E.3V 6	
C1100	*4.7U/E.3V 6	
C1101	*4.7U/E.3V 6	
C1102	*4.7U/E.3V 6	
C1103	22U/E.3VS 6	Ca
C1104	22U/E.3VS 6	
C1105	22U/E.3VS 6	
C1106	22U/E.3VS 6	
C1107	22U/E.3VS 6	Cb
C1108	22U/E.3VS 6	
C1109	22U/E.3VS 6	
C1110	22U/E.3VS 6	

**GPU BOM:**

**N16E-GR: Ca Unstuff, Cb Stuff (Default)**

**N16P-GX/GT/N16S-GTR-B: Ca change 4.7u stuff , Cb unstuff**

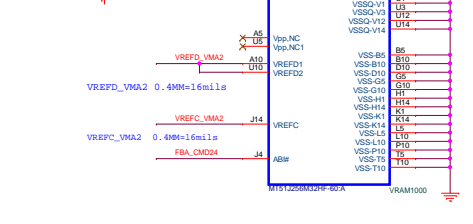
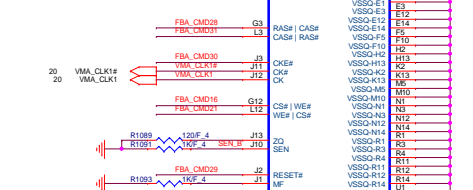
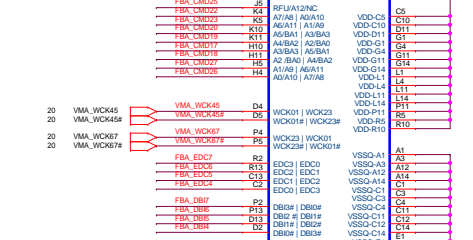
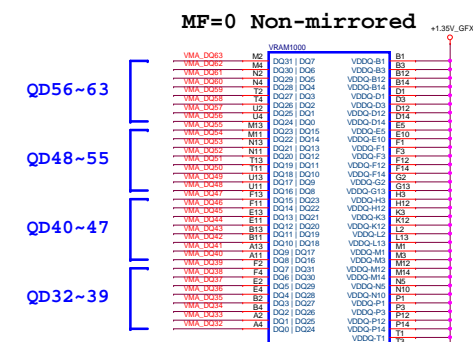
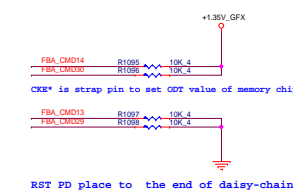
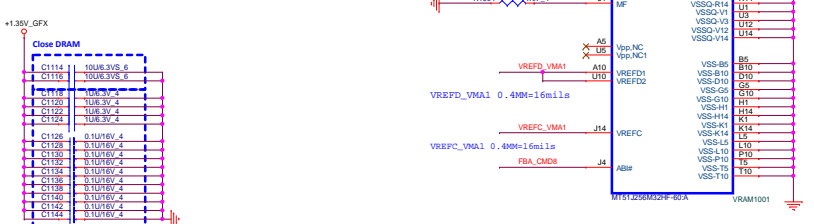
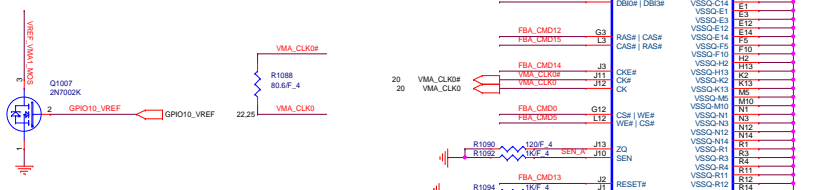
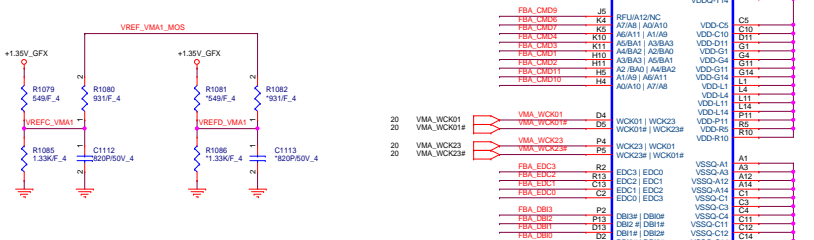
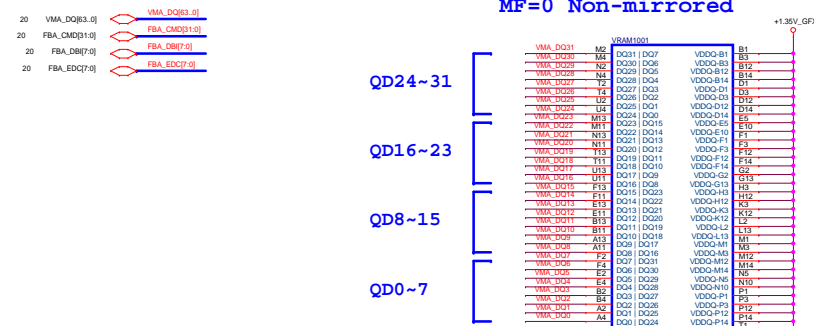
**4.7 uF : CH5471K9E07 CAP CHIP 4.7U 6.3V(+/-10%,X5R,0603)**

**PLACE TO GPU CENTER**

C1106 1 2 \*330U 2.5V 3528

4.7 uF : CH5471K9E07 CAP CHIP  
4.7U 6.3V(+10%,X5R,0603)

 +1.35V\_GFX 20,23,25,50



```
GDDR5 Mode H Mapping
< 0 - 31 > < 32 - 63 > Memory
CMD0 CMD16 CS*
CMD1 CMD17 A3_BA3
CMD2 CMD18 A2_BA0
CMD3 CMD19 A4_BA2
CMD4 CMD20 A5_BA1
CMD5 CMD21 WE*
CMD6 CMD22 A7_A8
CMD7 CMD23 A6_A11
CMD8 CMD24 AB1*
CMD9 CMD25 A12_RFU
CMD10 CMD26 A0_A10
CMD11 CMD27 A1_A9
CMD12 CMD28 RS*
CMD13 CMD29 RST*
CMD14 CMD30 CS*
CMD15 CMD31 CS*
```

## MF=0 Non-mirrored

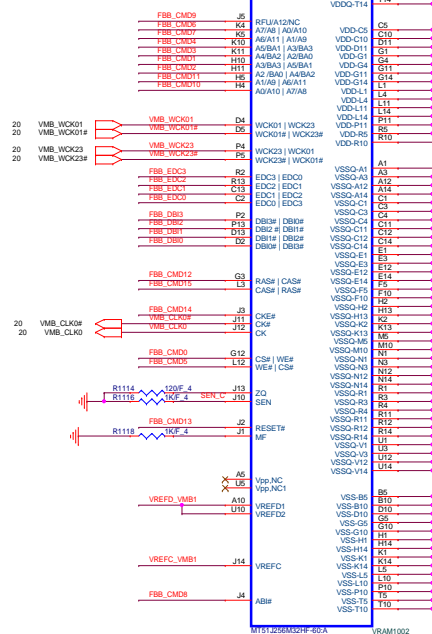
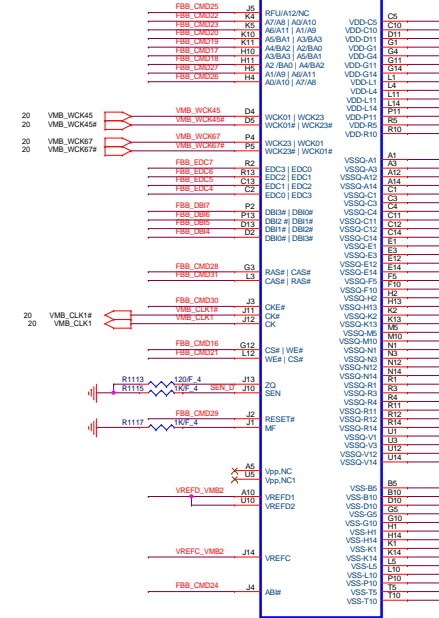


Figure 10 illustrates the RST PD connection. The circuit is divided into two main sections. The left section shows a 1.35V\_GFX input connected to a network of capacitors (C1186, C1187, C1188, C1189) and a 0.1µH/V\_4 inductor, which is then connected to a 10K\_4 resistor and a 10K\_4 resistor in series with a 1.35V\_GFX input. The right section shows a 1.35V\_GFX input connected to a network of capacitors (C1190, C1191, C1192) and a 0.1µH/V\_4 inductor, which is then connected to a 10K\_4 resistor and a 10K\_4 resistor in series with a 1.35V\_GFX input. The RST PD is connected to the output of the right section.

## MF=0 Non-mirrored



GDDR5 Mode H Mapping		
< 0-31	< 32-63	Memory
CM00	CM016	C5*
CM01	CM017	A13_BA3
CM02	CM018	A2_BA0
CM03	CM019	A4_BA2
CM04	CM020	A5_BA1
CM05	CM021	WE*
CM06	CM022	A7_A8
CM07	CM023	A6_A11
CM08	CM024	AB1*
CM09	CM025	A12_RP0
CM10	CM026	A0_A10
CM11	CM027	A1_A9
CM12	CM028	RAS*
CM13	CM029	RSY*
CM14	CM030	CKE*
CM15	CM031	CAS*

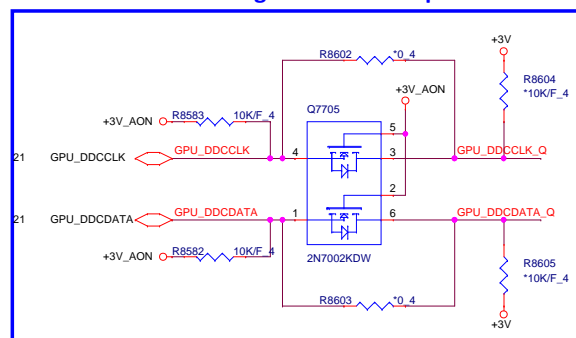
## LID Switch



**PROJECT : G37A/G37B**  
Quanta Computer Inc.

Size Custom	Document Number <b>26 -- LCD CONN/LID/CAM/D-MIC/TS1</b>	Re
Date: Monday, December 28, 2015	Sheet 26 of 51	

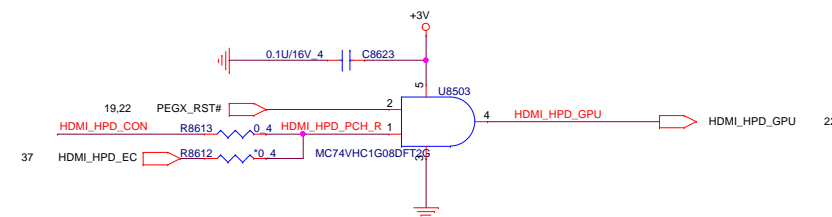
## Prevent current leakage when GPU is power off



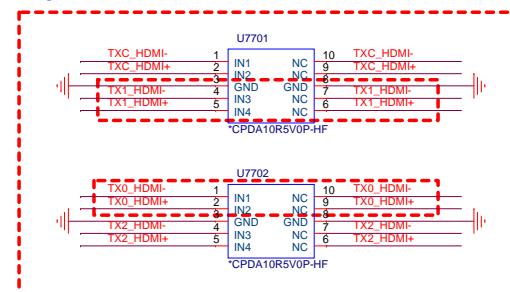
## EMI Solution



1127 Change P/N from CH+7506XB02 to CH+7506TB01

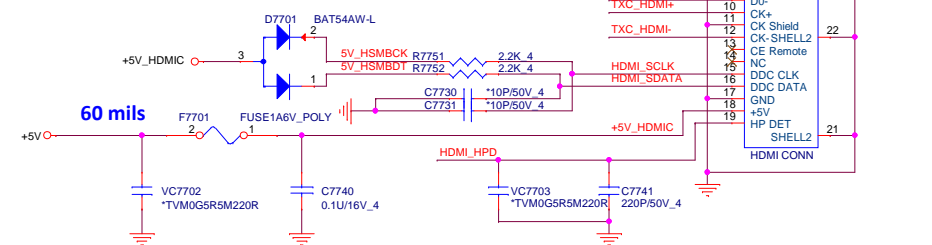


## ESD

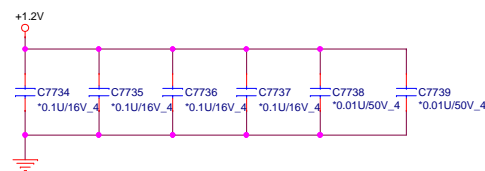
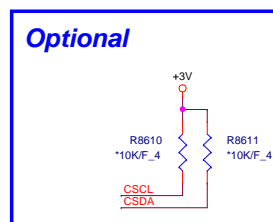


1124 Reserve ESD protection component

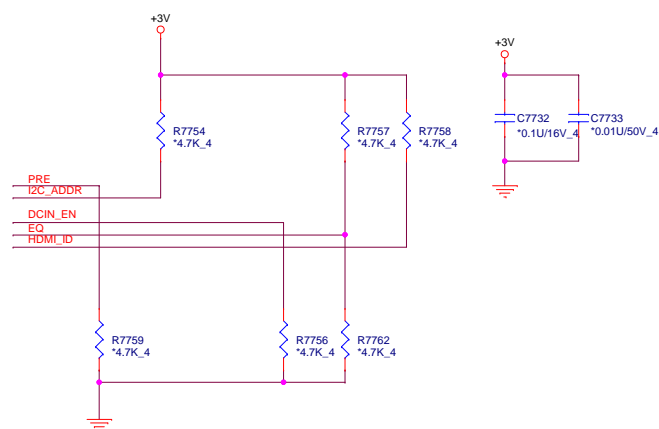
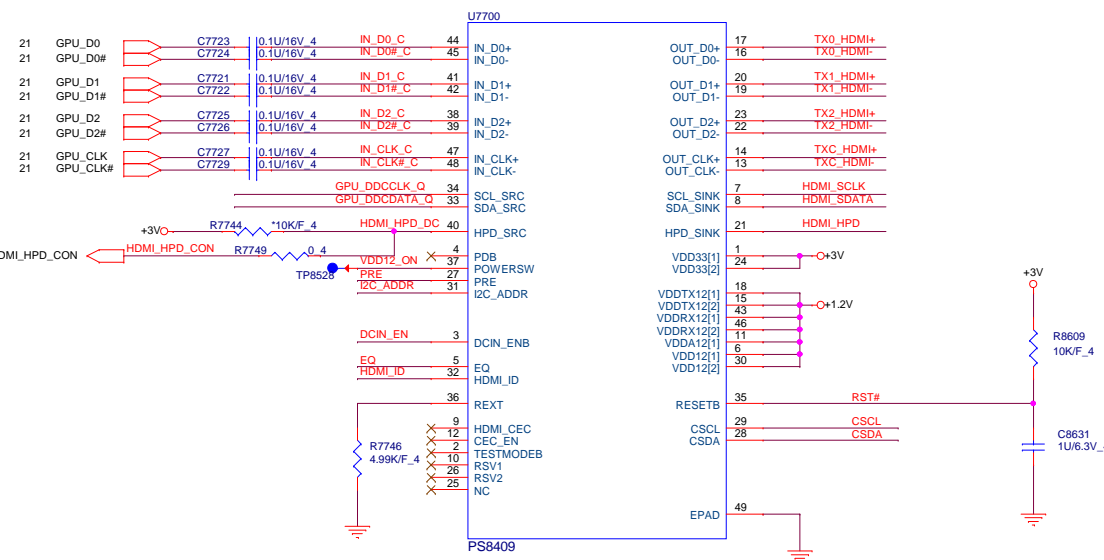
1124 SWAP for Layout



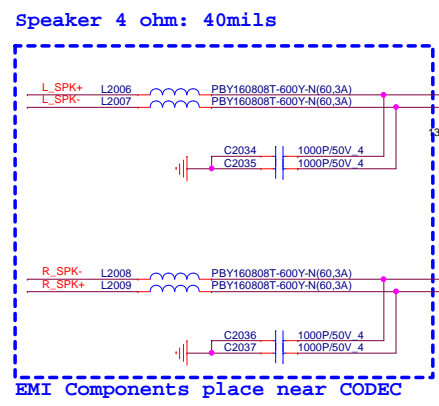
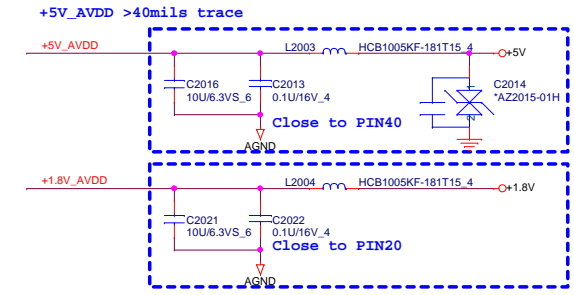
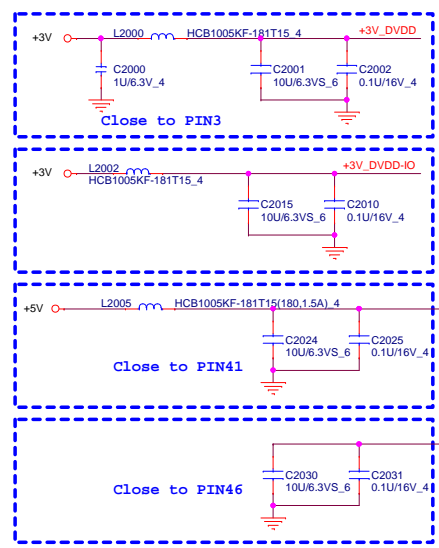
## Optional



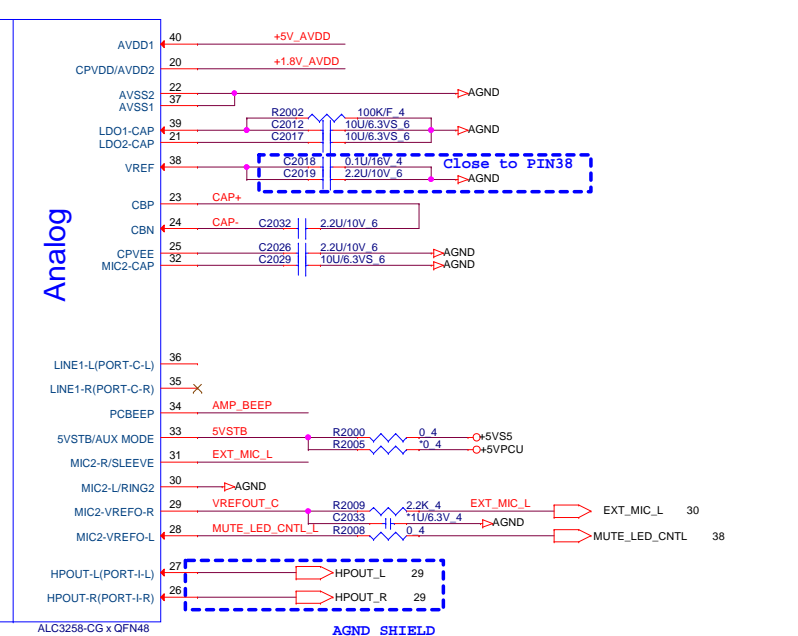
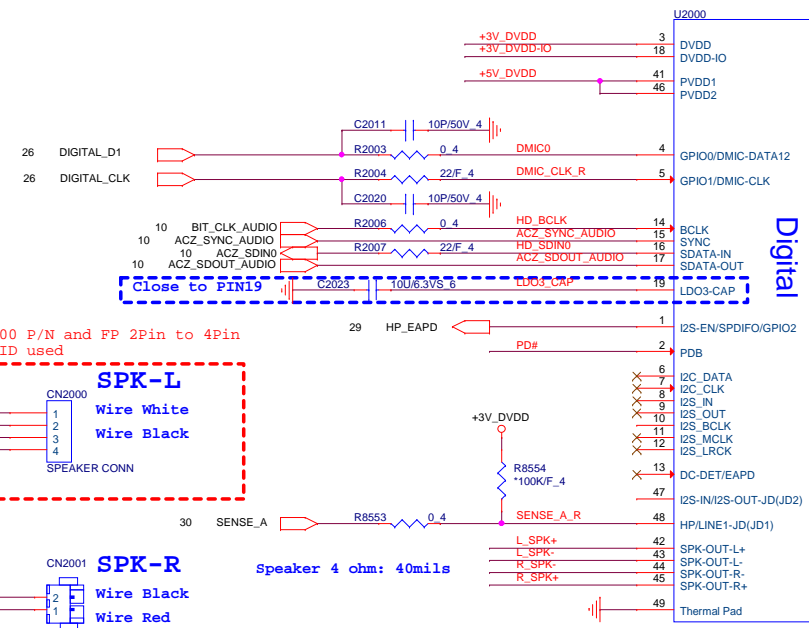
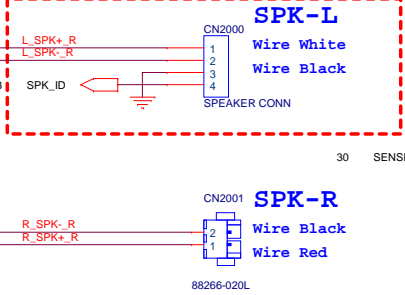
+5V 26,28,29,31,32,38,46,49  
+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,28,29,30,32,33,34,35,36,37,38,43,46,49  
+1.2V 46



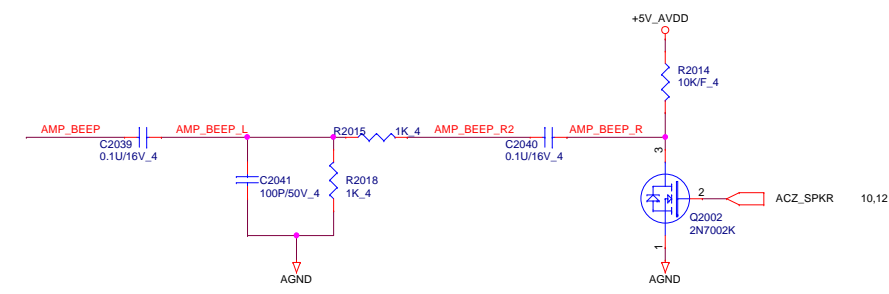
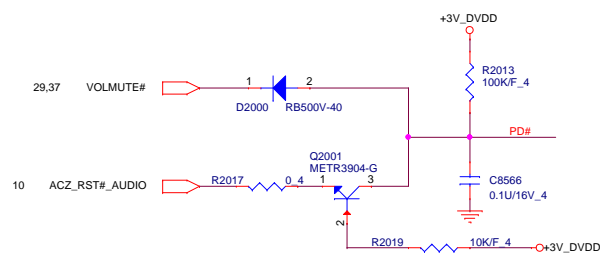
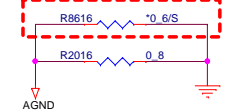
+5V	26,27,29,31,32,38,46,49
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,29,30,32,33,34,35,36,37,38,43,46,49
+1.8V	31,47



1123 Change CN2000 P/N and FP 2Pin to 4Pin for SPK Vendor ID used

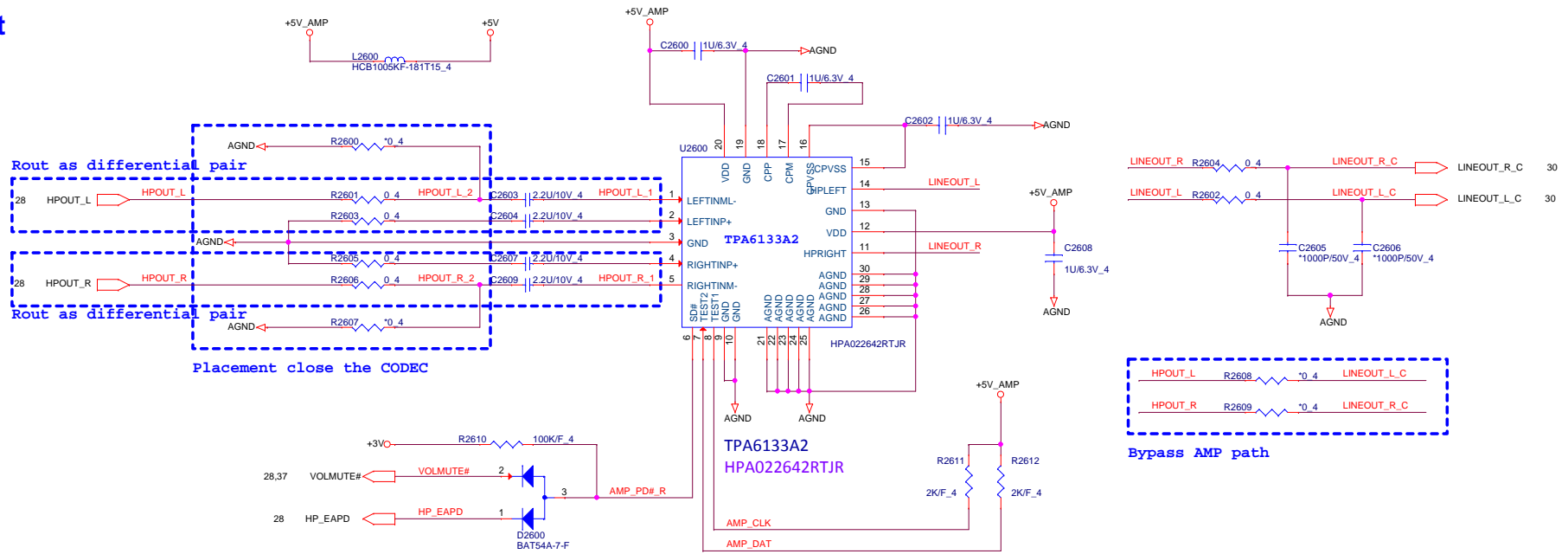


place to near or under codec  
1125 Add R8616 0603size short pad under codec for EMI request

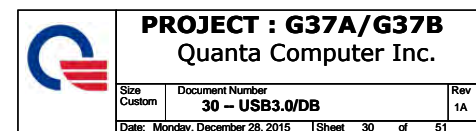
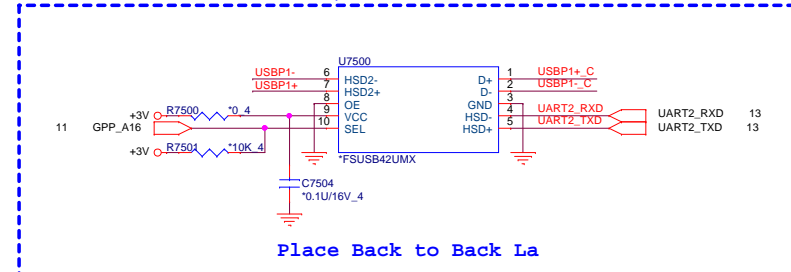
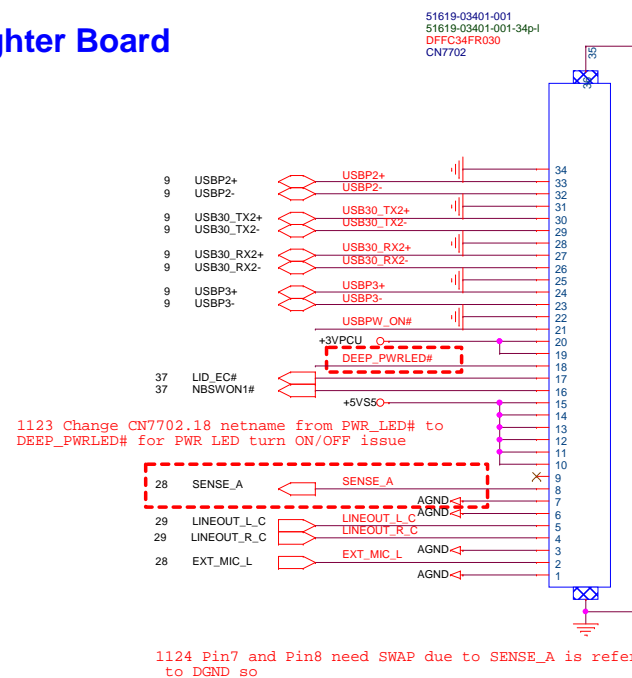
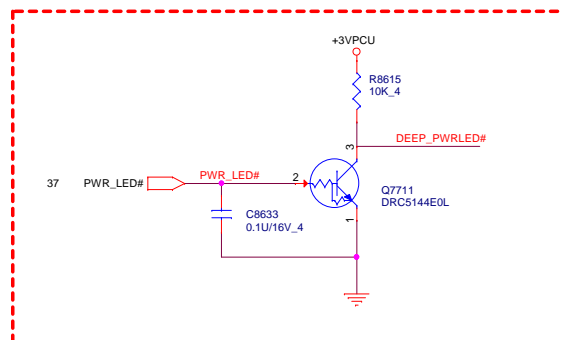


<b>PROJECT : G37A/G37B</b>		
<b>Quanta Computer Inc.</b>		
Size Custom	Document Number	Rev
	<b>28 - AUDIO CODEC ALC3258-C0</b>	<b>C0</b>
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## Head Phone out



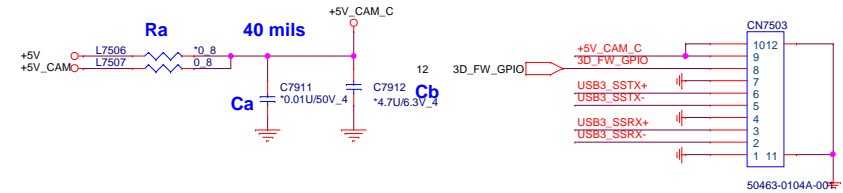




+5V	26,27,28,29,32,38,46,49
+3VPCU	5,10,30,33,37,38,40,41
+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,49
+1.8V	28,47

BOM: 3D CAM Stuff (except Ra,Ca,Cb)  
BOM: HD CAM Un- Stuff

## 3D Camera Conn.



BOM: 3D CAM Stuff (except Rb, Rc)

BOM: HD CAM Un-Stuff

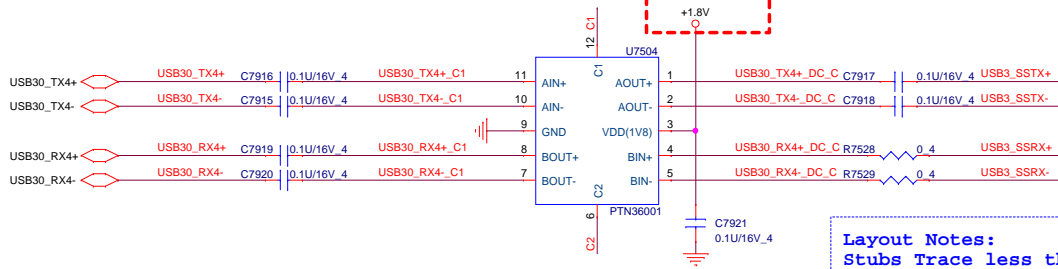
## USB3.0

### USB3.0 Re-driver IC

HOST

USB3.0 re-driver IC

DEVICE



Layout Notes:  
Stubs Trace less than 150mil

1123 Change UB3 re driver power rail  
from +1.8V\_DEEP\_SUS to +1.8V

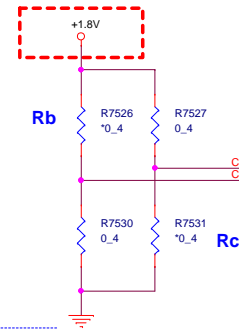


Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A
H	Long	H	EQ[1]	DE[2]
high-Z	Medium	high-Z	6 dB	-5.3 dB
L	Short	L	3 dB	0 dB

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B
H	Long	H	9 dB	-5.3 dB
high-Z	Medium	high-Z	6 dB	-3.1 dB
L	Short	L	3 dB	0 dB

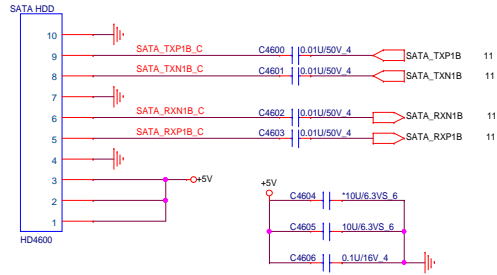


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

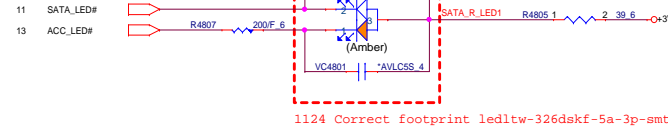
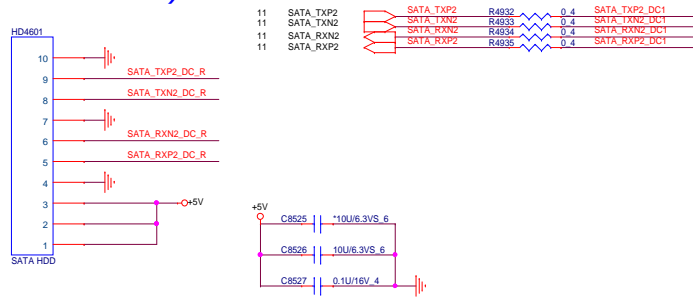
Size	Document Number	Rev
Custom	31 - 3D CAM/REDRIVER	1A
Date: Monday, December 28, 2015	Sheet 31 of 51	

26,38,39,40,41,42,43,44,45,47,48,49,50  
+5V 26,27,28,29,31,38,46,49  
+3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,33,34,35,36,37,38,43,46,49

## HDD



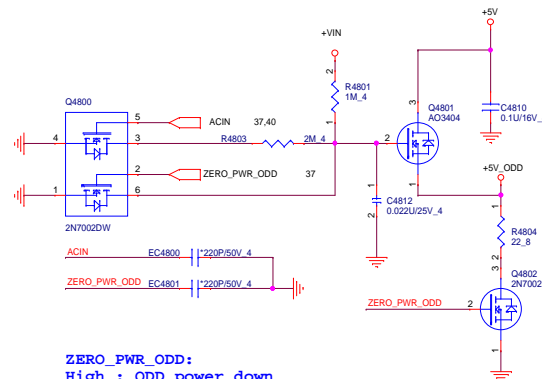
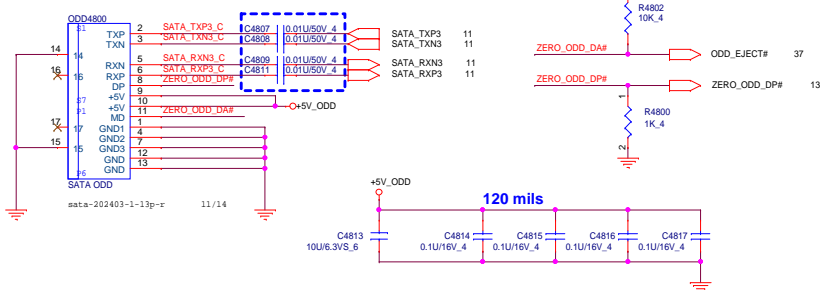
## SATA LED

HDD  
(Close to ODD)

SATA_TXP2_DC1	C4924	0.01U/50V_4	SATA_TXP2_DC_R
SATA_TXN2_DC1	C4925	0.01U/50V_4	SATA_TXN2_DC_R
SATA_RXN2_DC1	C4926	0.01U/50V_4	SATA_RXN2_DC_R
SATA_RXP2_DC1	C4927	0.01U/50V_4	SATA_RXP2_DC_R

## SATA ODD

Bypass CAP close CON



ZERO\_PWR\_ODD:  
High : ODD power down  
Low : ODD power on

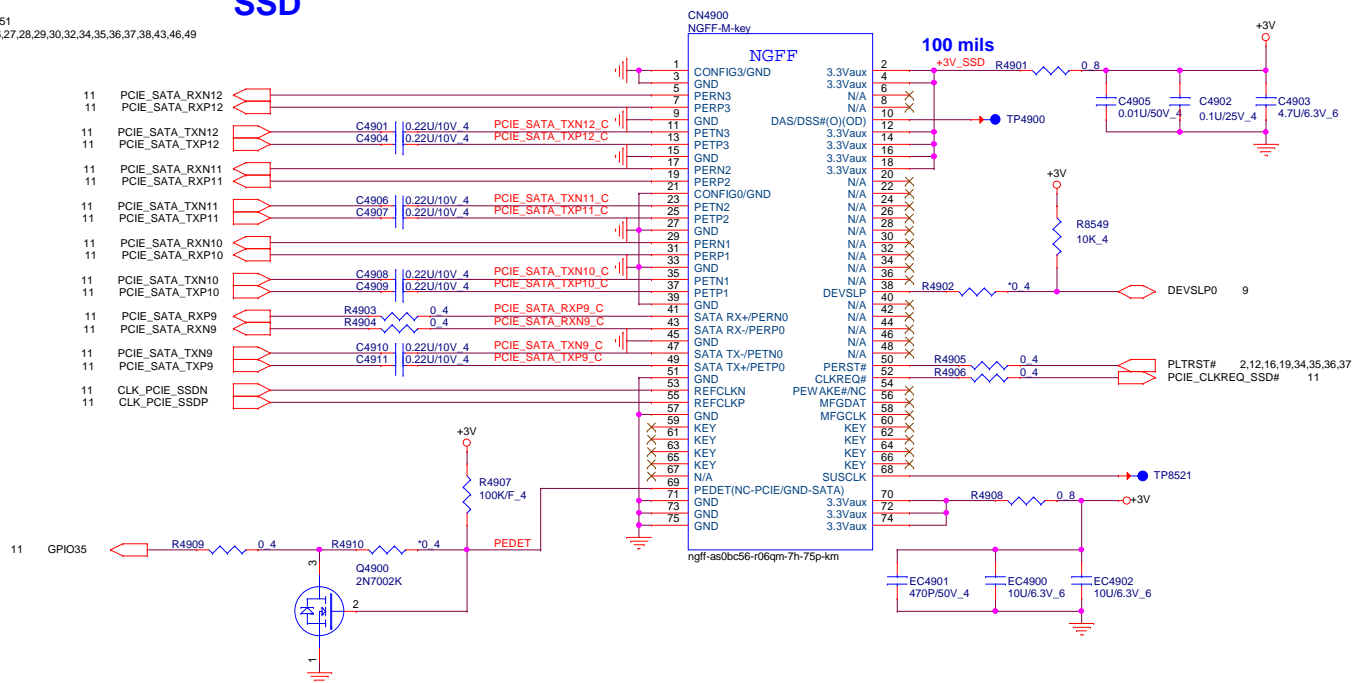
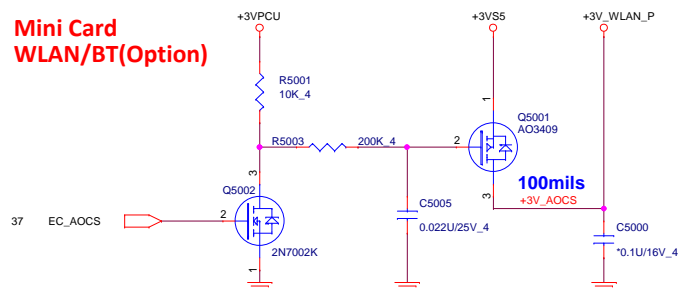


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

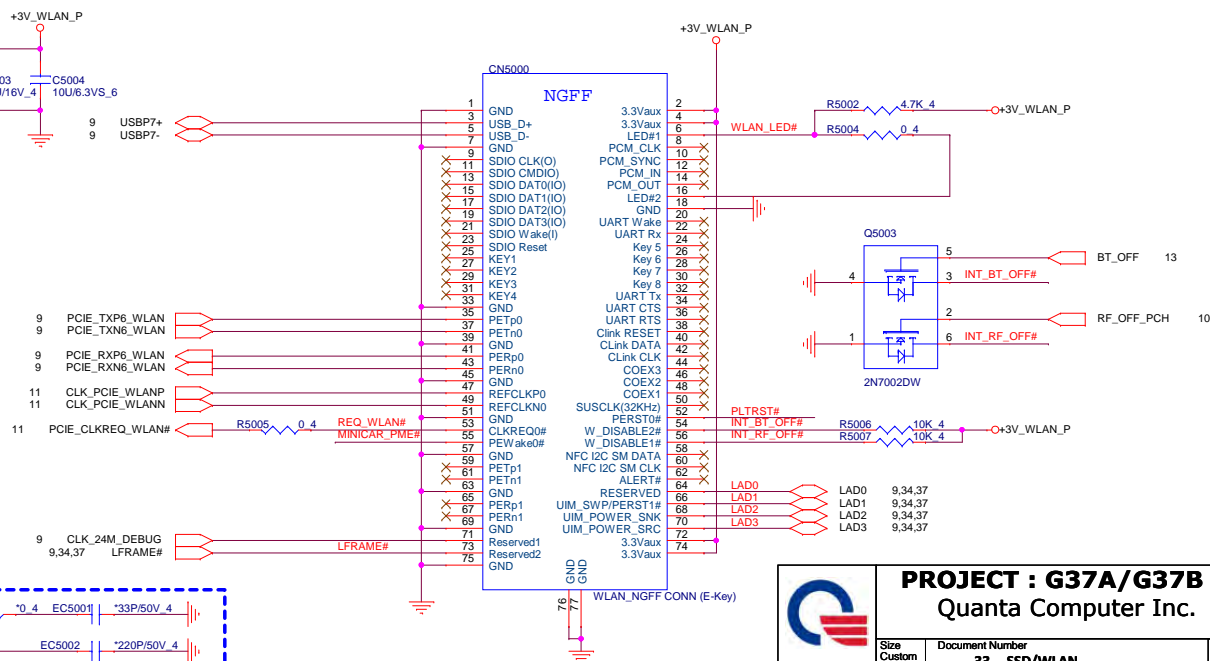
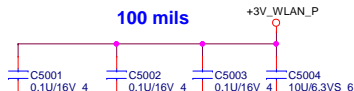
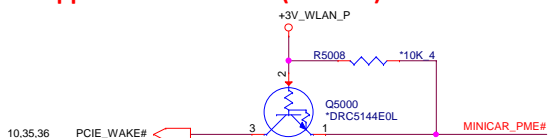
Size C	Document Number 32 - HDD/ODD	Rev 1A
Date: Monday, December 28, 2015	Sheet 32 of 51	

## SSD

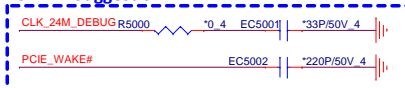
+3VPCU 5,10,30,37,38,40,41  
 +3VSS 10,12,14,16,26,37,41,42,46,47,48,51  
 +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,34,35,36,37,38,43,46,49

Mini Card  
WLAN/BT(Optional)

## Support Wake Function(Reserve)



## For EMI Suggestion

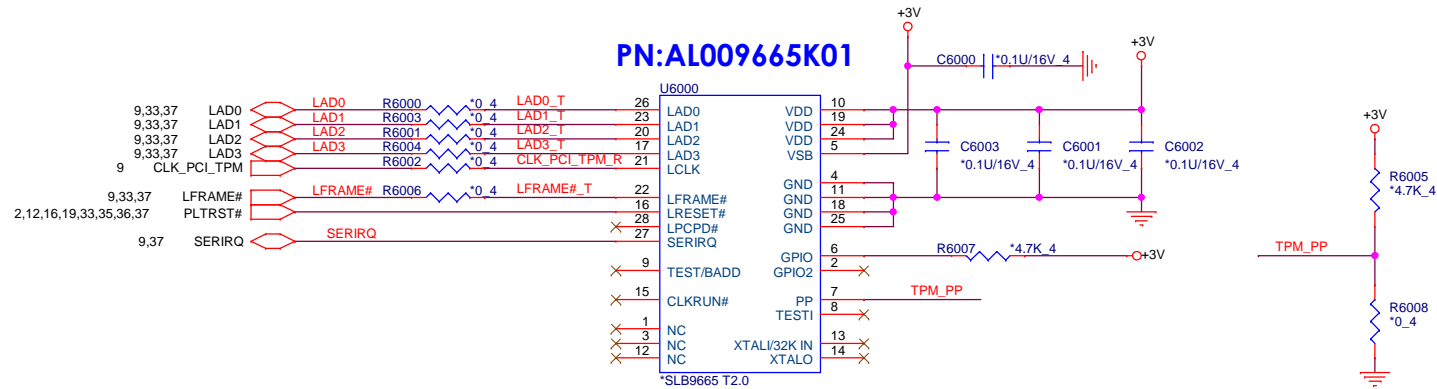


**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

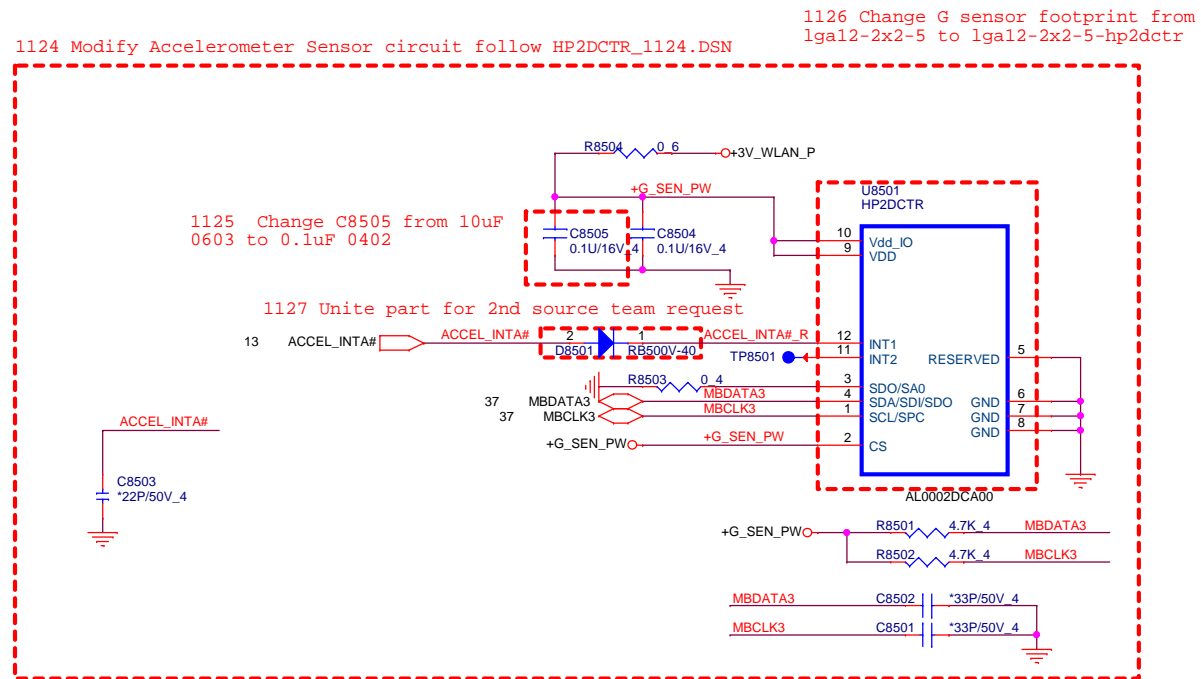
Size	Document Number	Rev
Custom	33 -- SSD/WLAN	1A

Date: Monday, December 28, 2015 | Sheet 33 of 51

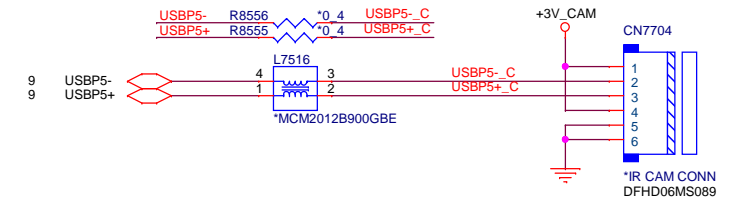
## TPM (2.0)



## Accelerometer Sensor



## IR CAM



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

<Title>		
Size B	Document Number 34 -- TPM/G-Sensor	Rev 1A
Date:	Monday, December 28, 2015	Sheet 34 of 51

## LAN & RJ45

For SWR mode support RTL8111HSH/RTL8107ES

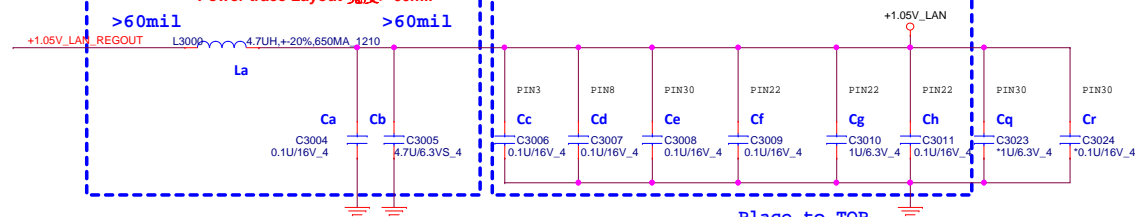
Stuff La, Ca, Cb

\* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S)  
close to each VDD10 pin-- 3, 22, 8, 30

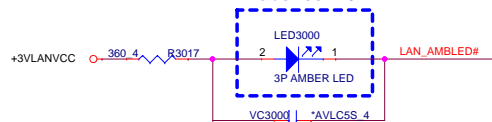
\* Place Cg,Ch for RTL8111H(S) & RTL8107E(S)  
close to each VDD10 pin-- 22(reserved)

Power trace Layout 宽度 > 60mil

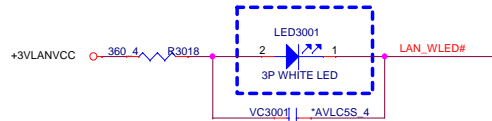
>60mil >60mil



Place to TOP

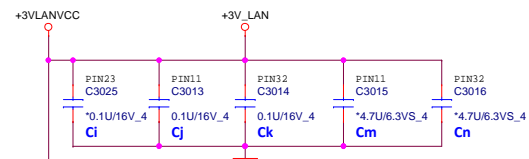


Place to BOT

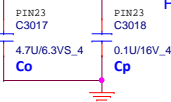


\* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

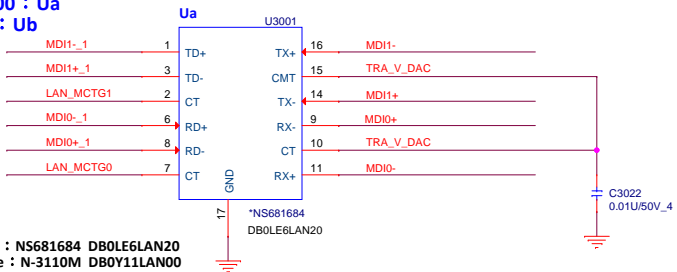
\* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



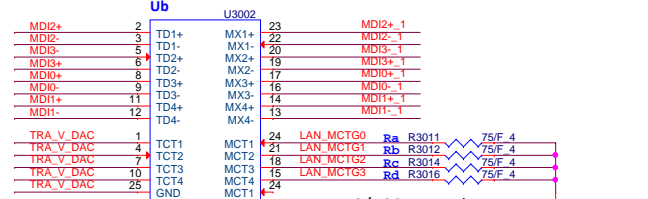
For SWR mode support RTL8111HSH/RTL8107ESH  
Stuff Co, Cp



For 10/100 : Ua  
For Giga : Ub



1st source : NS681684 DB0LE6LAN20  
2nd source : N-3110M DB0Y11LAN00



For GIGA BOT:GST5009B LF,DB0Z06LAN00

FCE : NS892407 , DB0LL1LAN00

For 10/100 : Ra,Rb  
For Giga : Ra,Rb,Rc,Rd

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

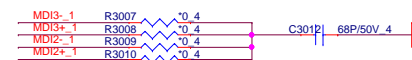
LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

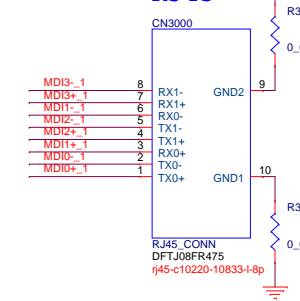
LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

LAN\_AMBLED# TP3000  
LAN\_LED1 TP3001  
LED2 TP3002

For 10/100 stuff only



RJ45



1125 Change CN3000 PN from DFTJ08FR335 to DFTJ08FR475



**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

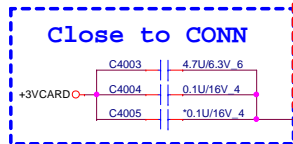
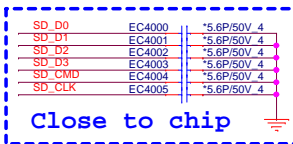
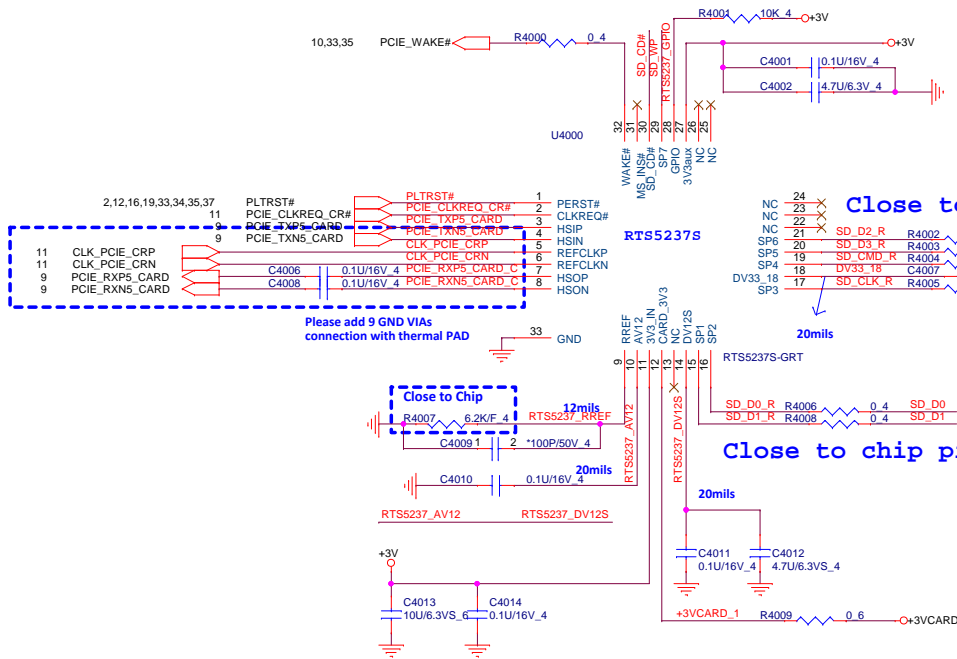
Size	Document Number	Rev
Custom	35 - LAN RTL8107ESH-CG/RJ45	1A
Date: Monday, December 28, 2015	Sheet 35 of 51	

# RTS5237S PCIE CARD READER Controller

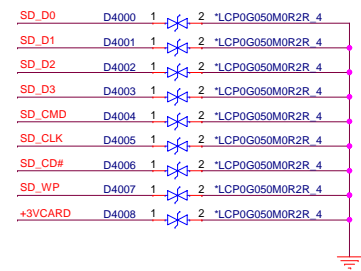
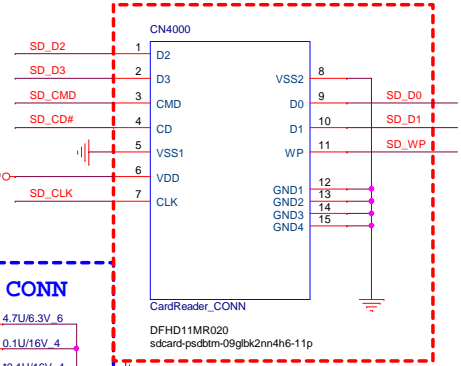
Share Pin


SD / MMC

SP1	SD_D1	MS_D1
SP2	SD_D0	MS_D0
SP3	SD_CLK	MS_D0
SP4	SD_CMD	MS_D2
SP5	SD_D3	MS_D3
SP6	SD_D2	MS_CLK
SP7	SD_WP	MS_DS



1126 Change CN4000 P/N from DFHD11MR053 to DFHD11MR020

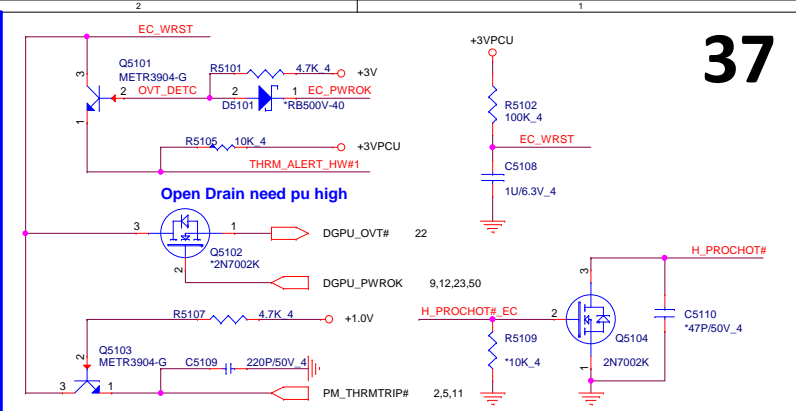
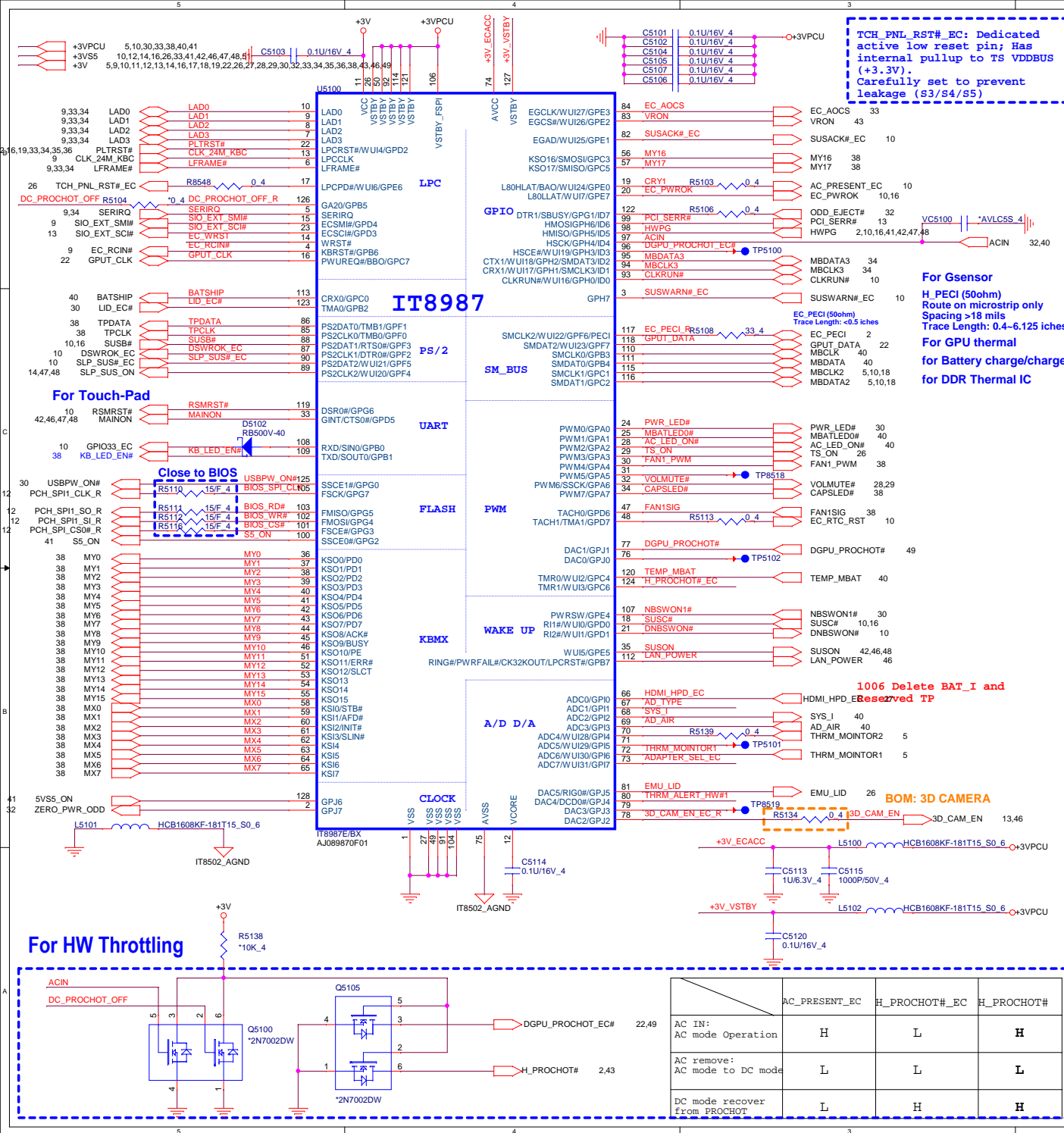




**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>36 - CR RTS5237S/CR SOCKET</b>	Rev 1A
Date: Monday, December 28, 2015		Sheet 36 of 51

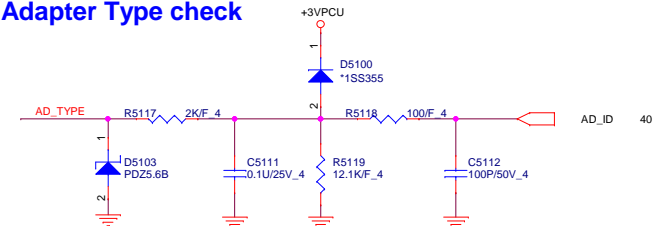




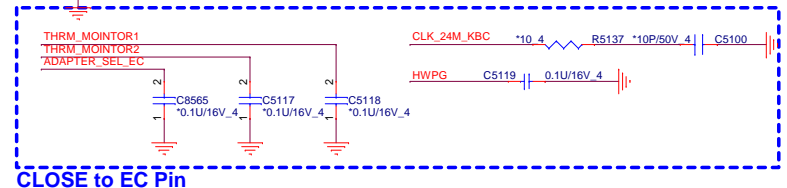
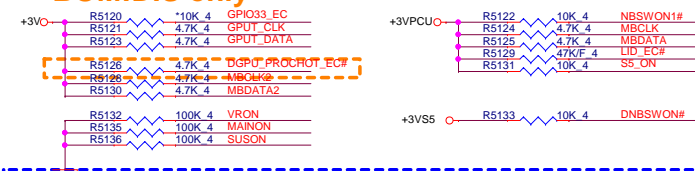
### Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	DIS
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	UMA
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

### Adapter Type check

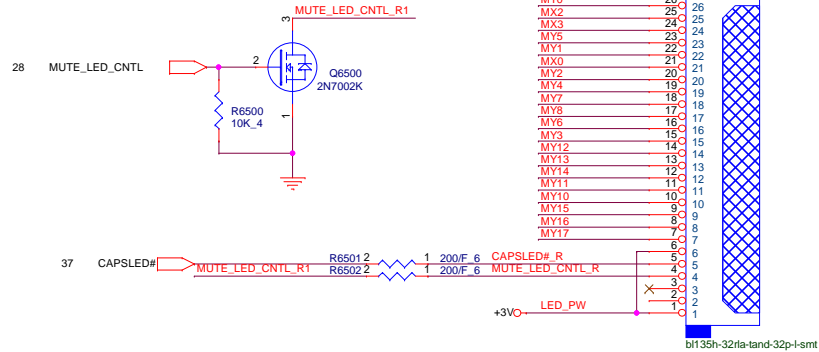


### BOM:DIS only

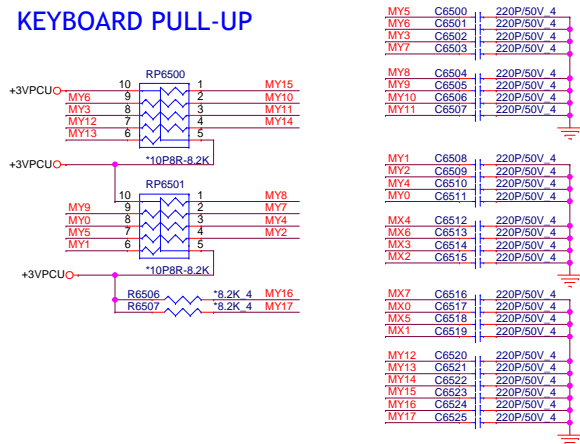


+VIN 26,32,39,40,41,42,43,44,45,47,48,49,50  
 +5V 26,27,28,29,31,32,46,49  
 +3VPCU 5,10,30,33,37,40,41  
 +3VS5 10,12,14,16,26,33,37,41,42,46,47,48,51  
 +3VSUS 46  
 +3V 5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,43,46,49

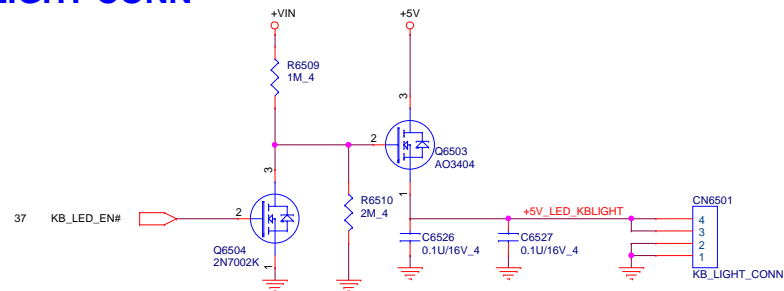
## KEYBOARD Con.



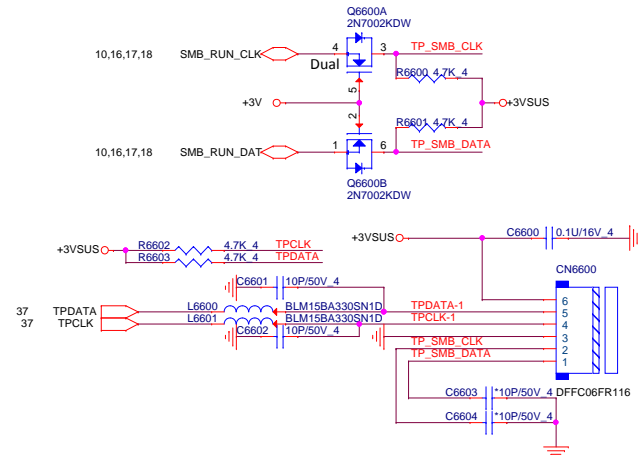
## KEYBOARD PULL-UP



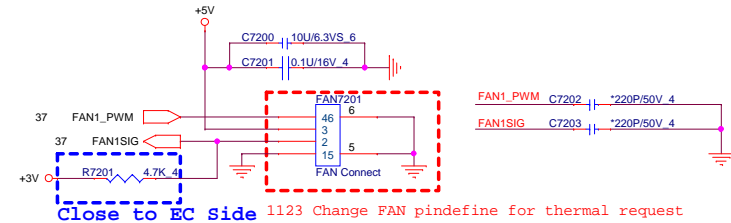
## KB LIGHT CONN



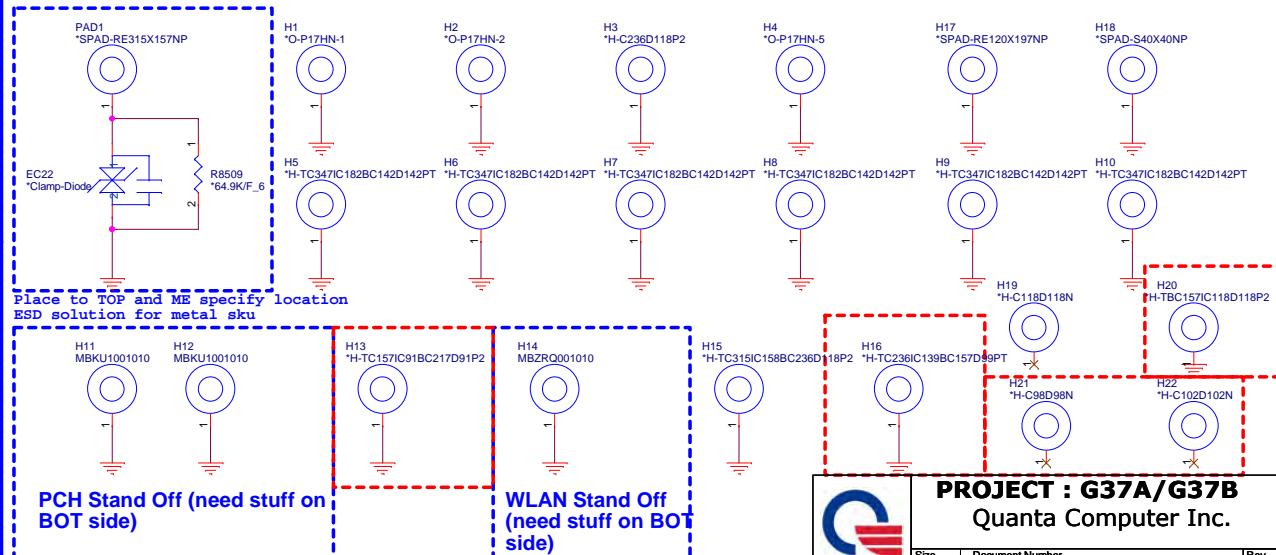
## Touch Pad Connector



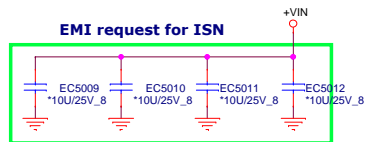
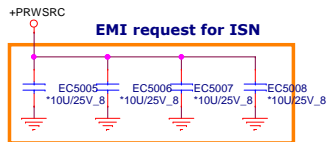
## FAN



## HOLE

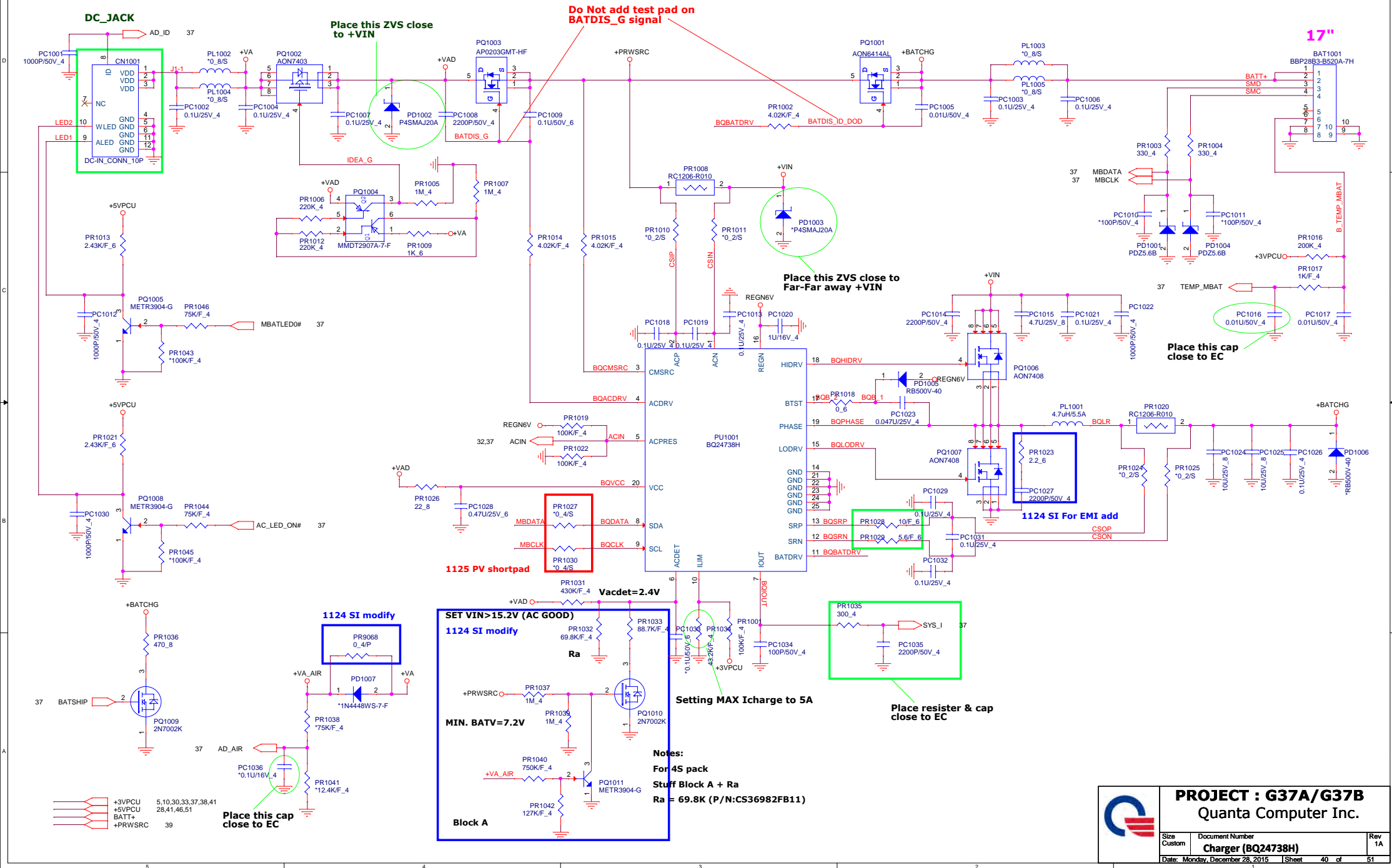


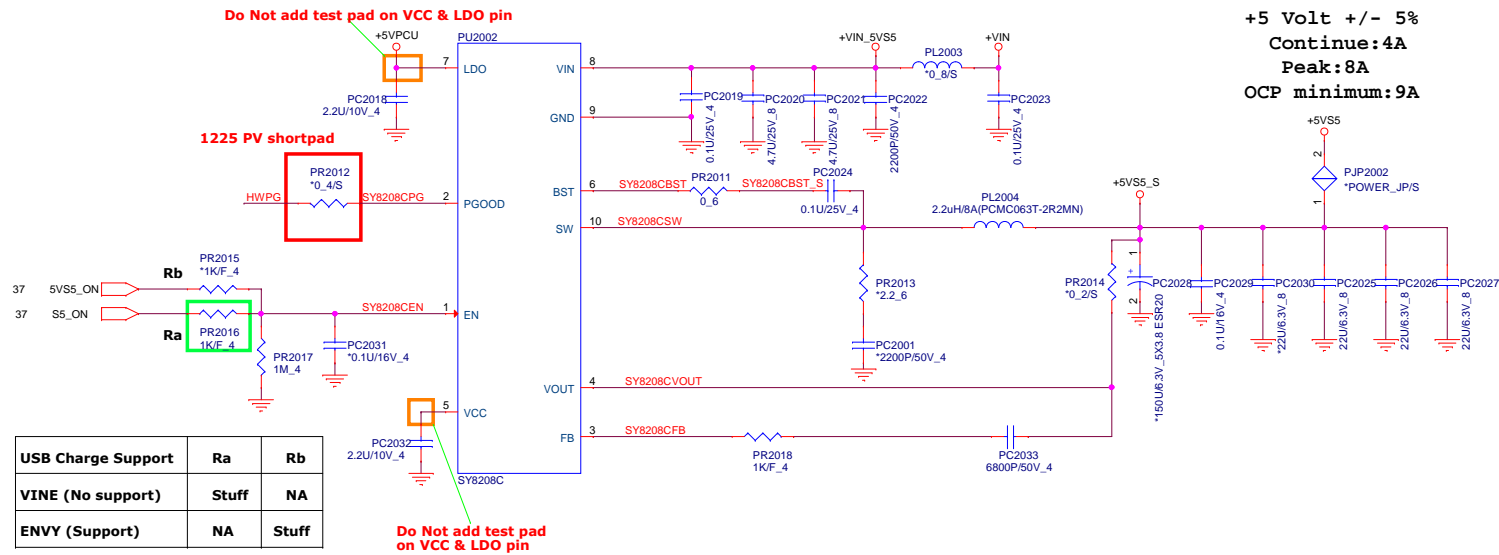
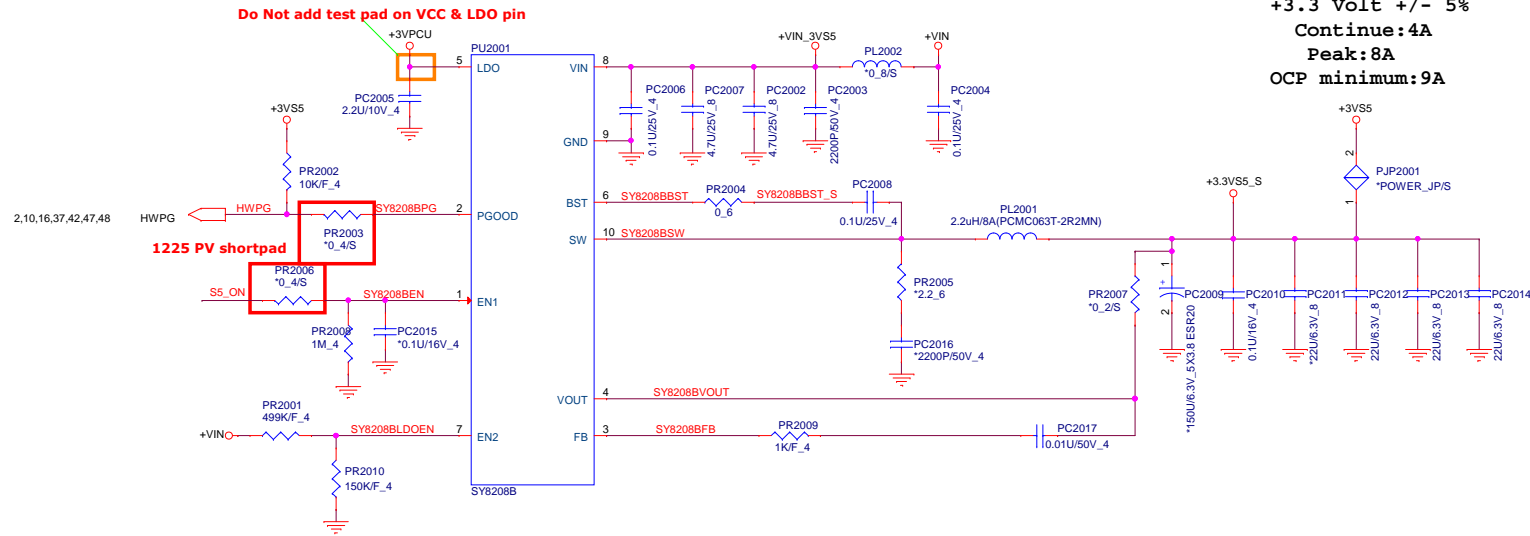
PROJECT : G37A/G37B		
Quanta Computer Inc.		
Size Custom	Document Number 38 -- KB/KBL/TP/FAN/HOLE	Rev 1A
Date: Monday, December 28, 2015	Sheet 38 of	51



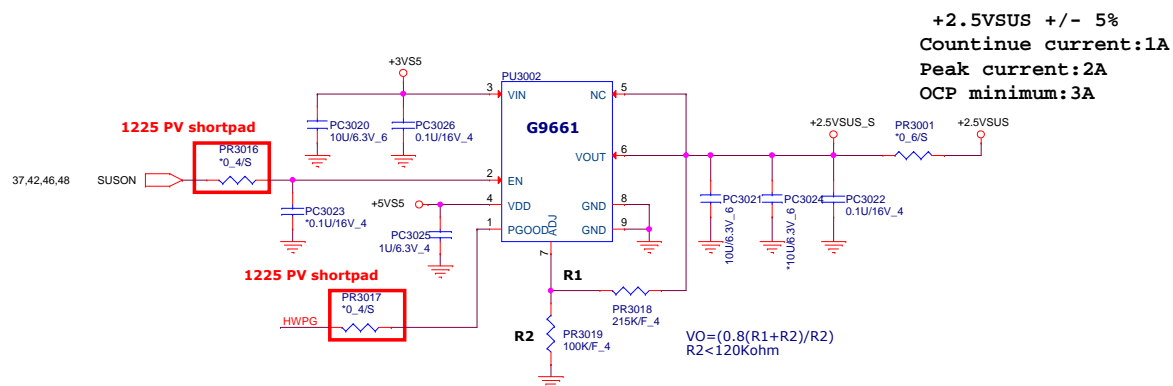
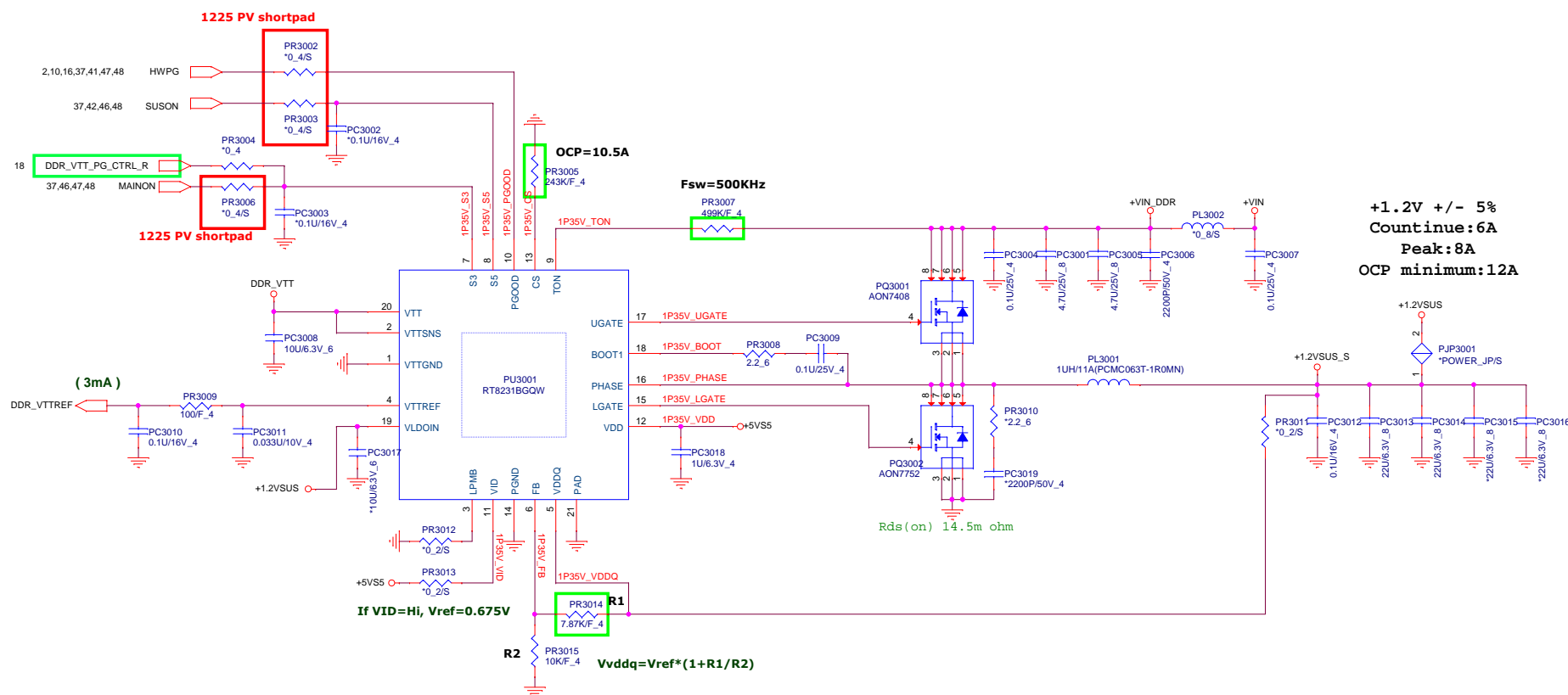
**PROJECT : G37A/G37B**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>RF Solution</b>	Rev 1A
Date: Monday, December 28, 2015		Sheet 39 of 51

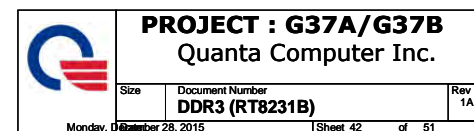




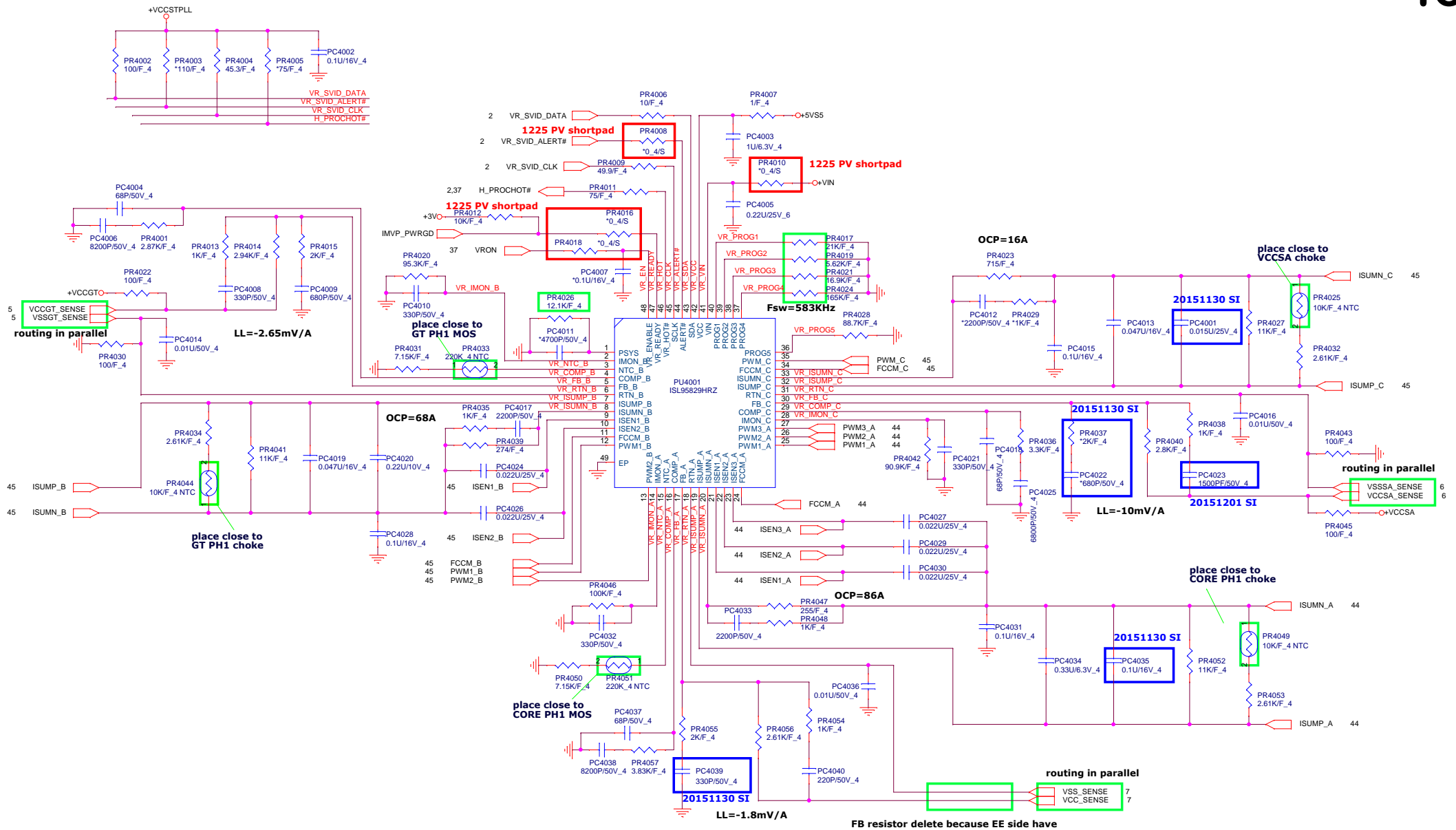
+VIN	26,32,38,39,40,42,43,44,45,47,48,49,50
+3VSS	10,12,14,16,26,33,37,42,46,47,48,51
+5VSS	10,26,28,30,42,43,44,45,46,47,48,49,50,51
+3VPCU	5,10,30,33,37,38,40
+5VPCU	28,40,46,51

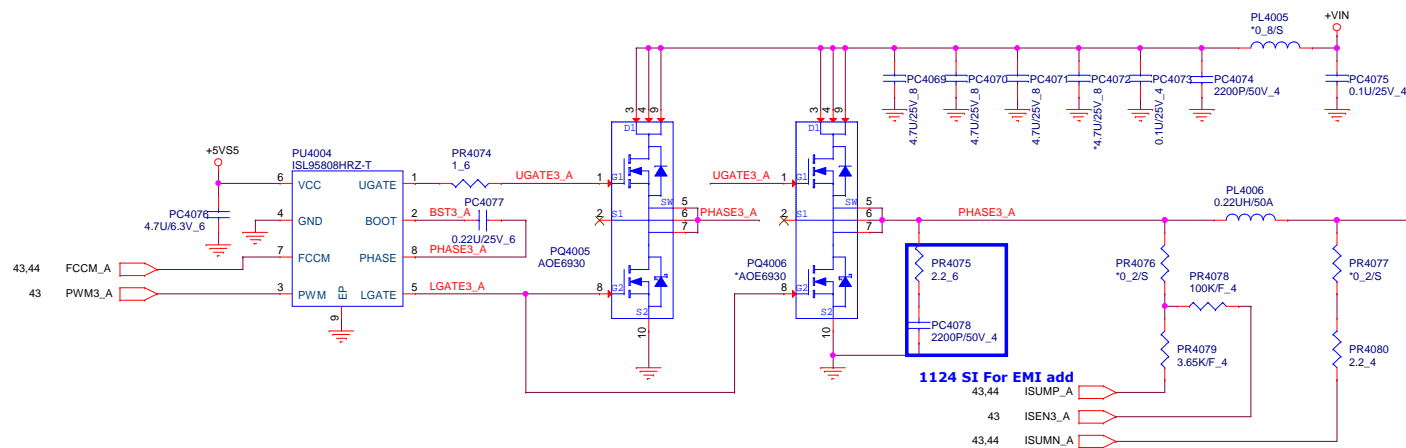
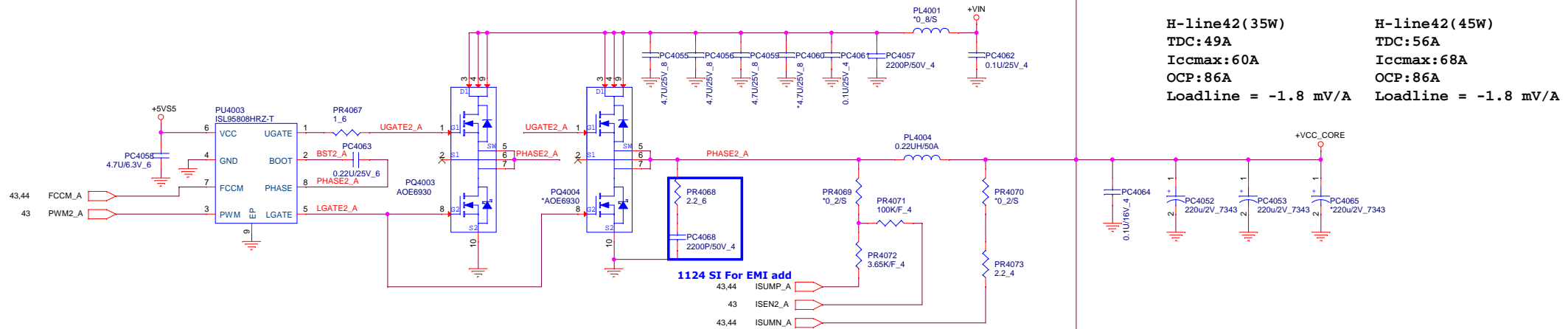
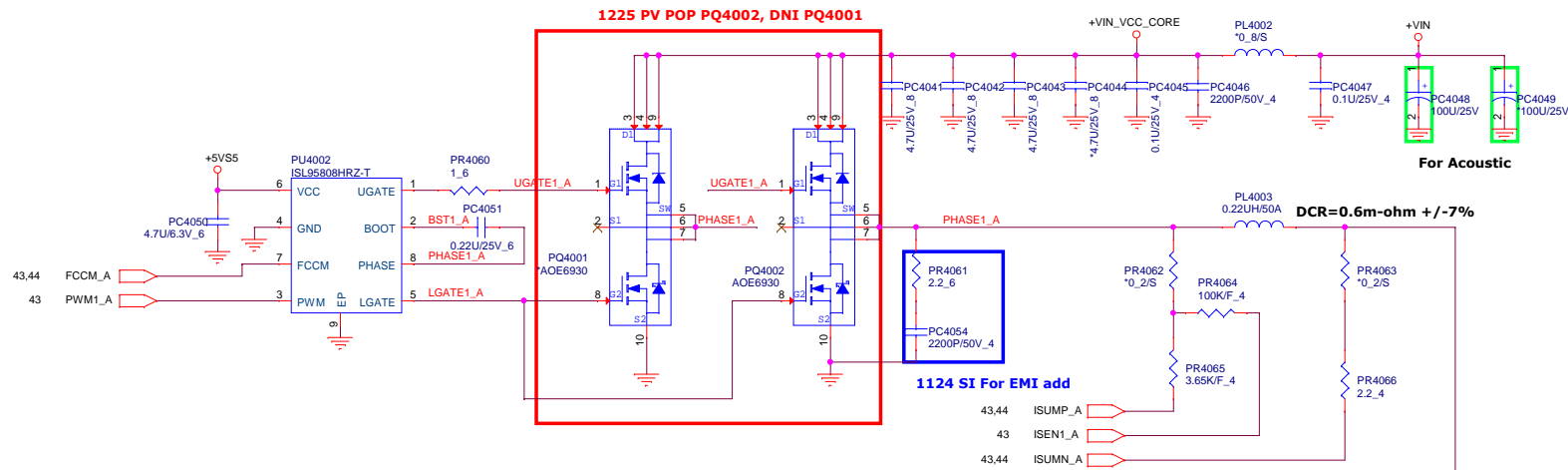



+VIN	26,32,38,39,40,41,43,44,45,47,48,49,50
+5VS5	10,26,28,30,41,43,44,45,46,47,48,49,50,51
+1.2VSUS	2,6,10,17,18,46,48,51
DDR_VTT	17,18
+2.5VSUS	17,18

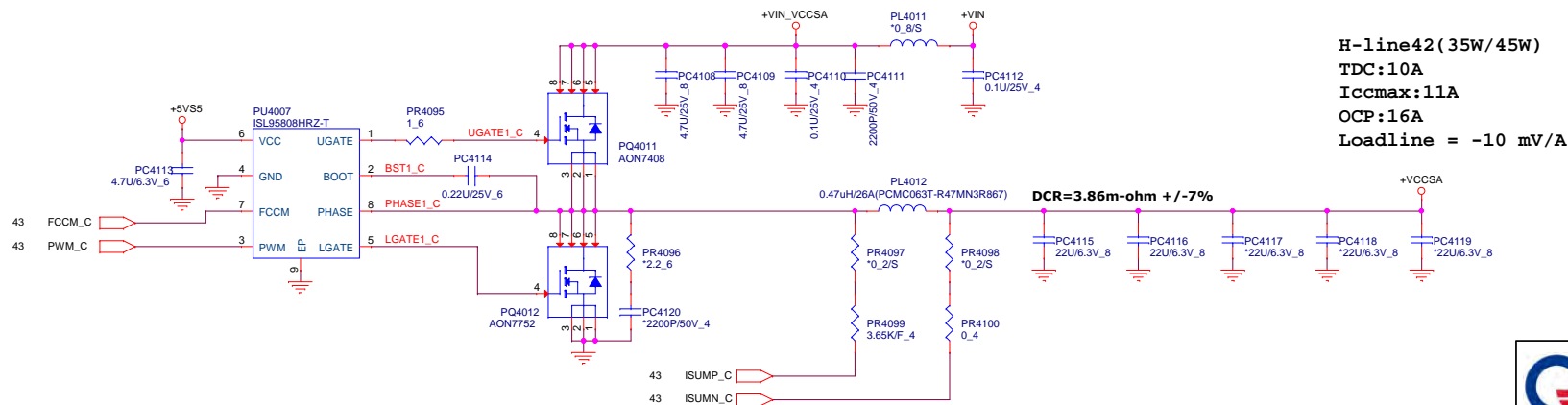
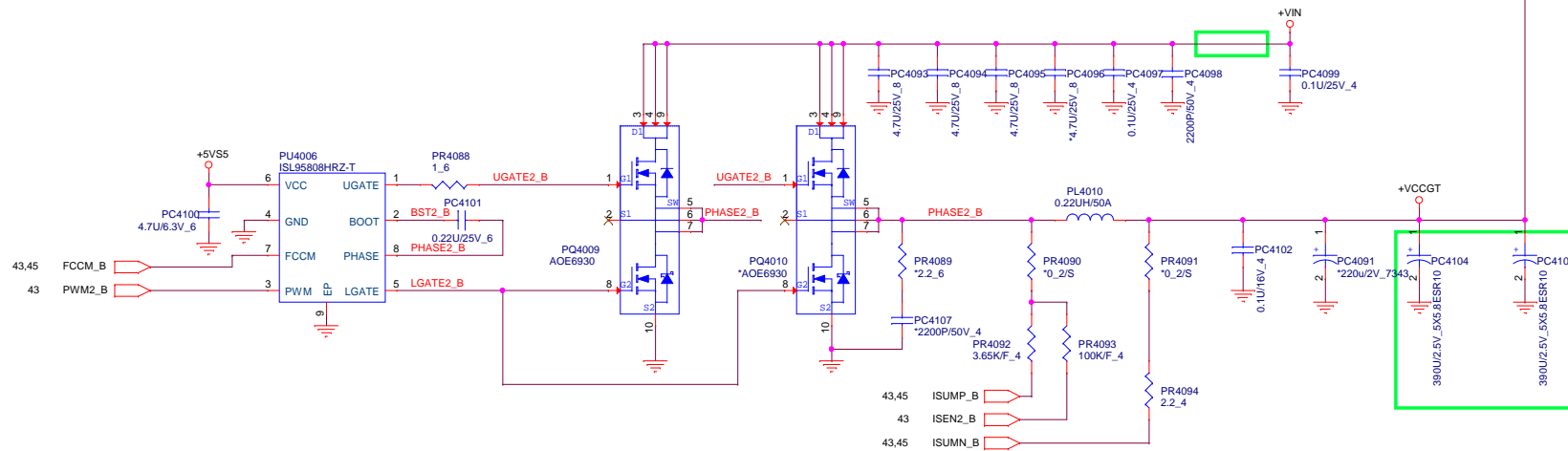
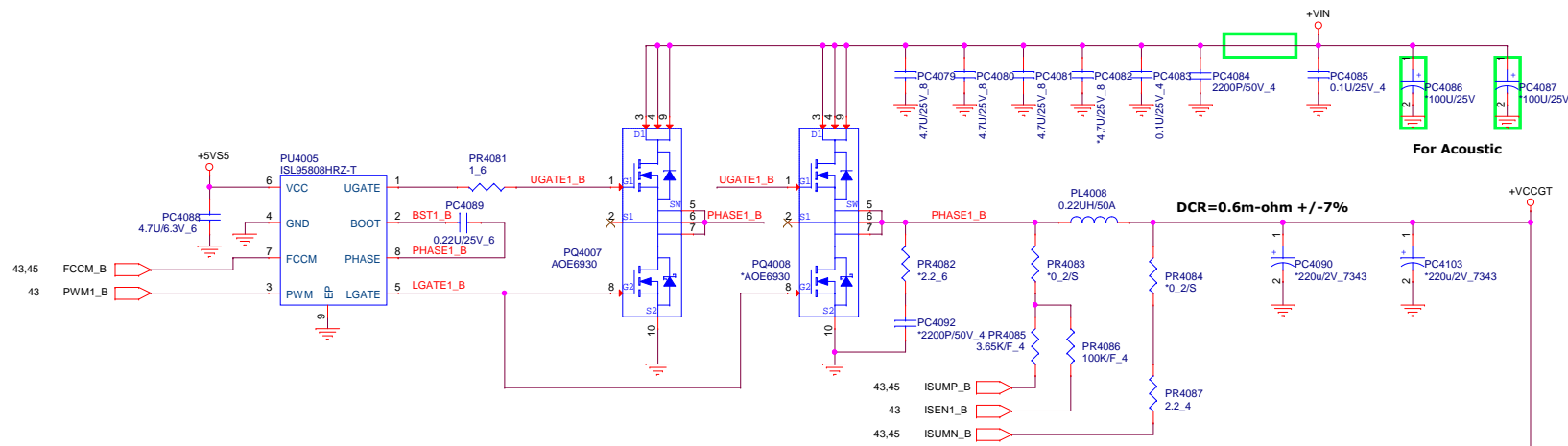


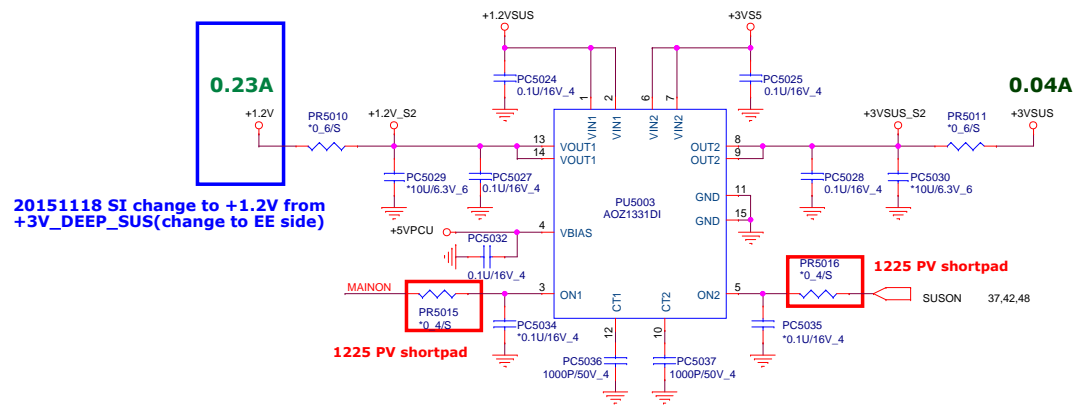
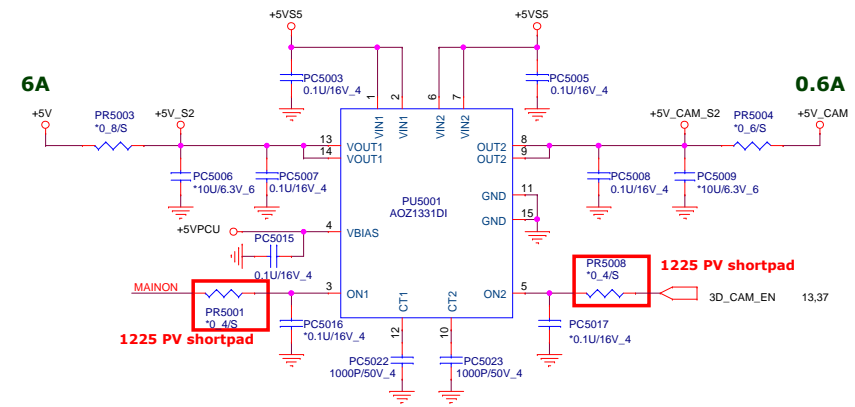
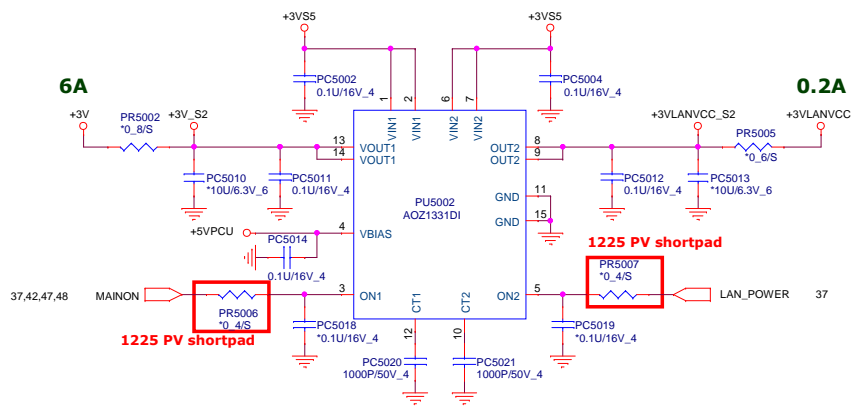






 <b>PROJECT : G37A/G37B</b> Quanta Computer Inc.		
Size Custom	Document Number <b>+VCC_CORE (ISL95808HRZ-T)</b>	Rev 1A
Date:	Monday, December 28, 2015	Sheet 44 of 51




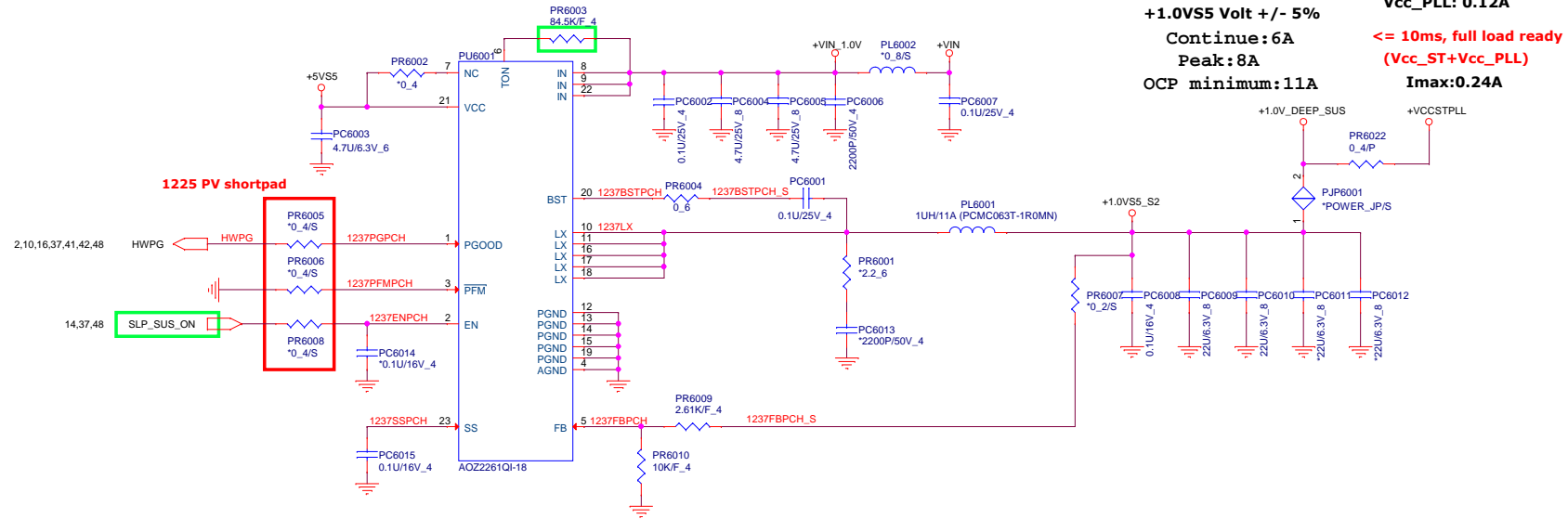


20151118 SI change to +1.2V from  
+3V\_DEEP\_SUS(change to EE side)

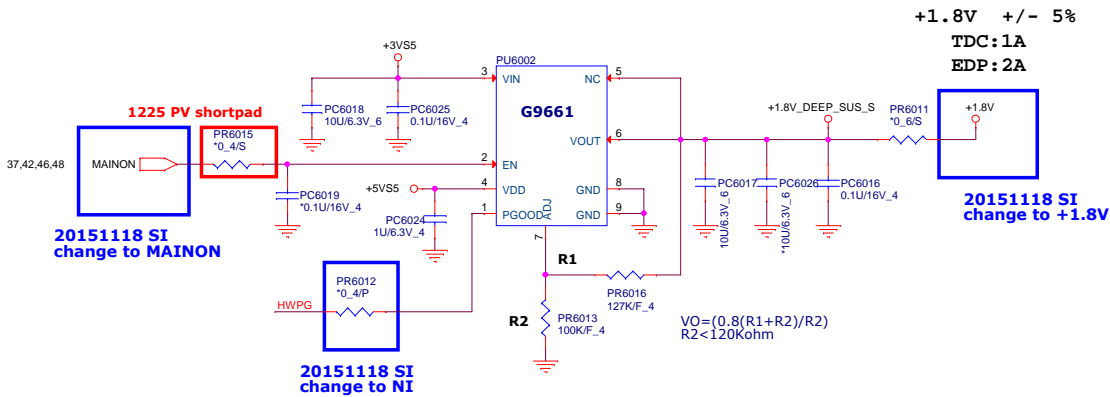
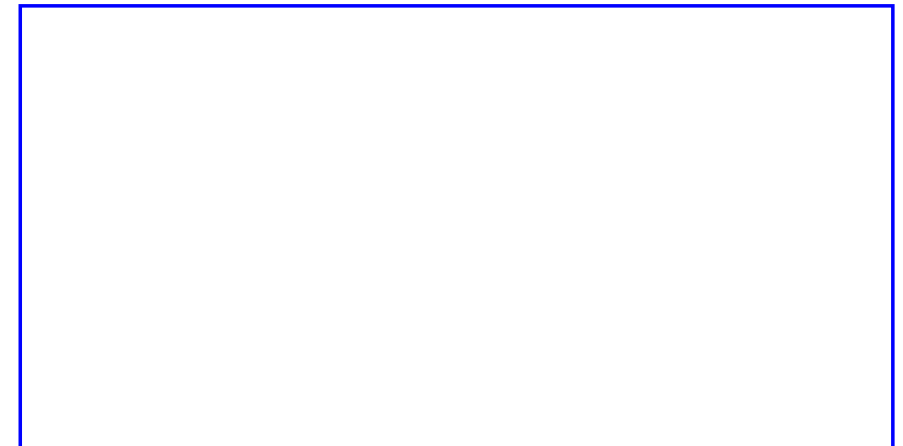
20151118 SI del +1.5V and add +1.2V

+3V	5,9,10,11,12,13,14,16,17,18,19,22,26,27,28,29,30,32,33,34,35,36,37,38,43,49
+5V	26,27,28,29,31,32,38,49
+3VS5	10,12,14,16,26,33,37,41,42,47,48,51
+5VS5	10,26,28,30,41,42,43,44,45,47,48,49,50,51
+3VSUS	38
+3VLAVCC	35
+5V_CAM	31
+1.2V	27
+3V_DEEP_SUS	9,10,12,13,14,16,18


 <b>PROJECT : G37A/G37B</b> Quanta Computer Inc.		
Size Custom	Document Number <b>Load switch IC (AOZ1331D)</b>	Rev 1A
Date: Monday, December 28, 2015	Sheet 46	of 51

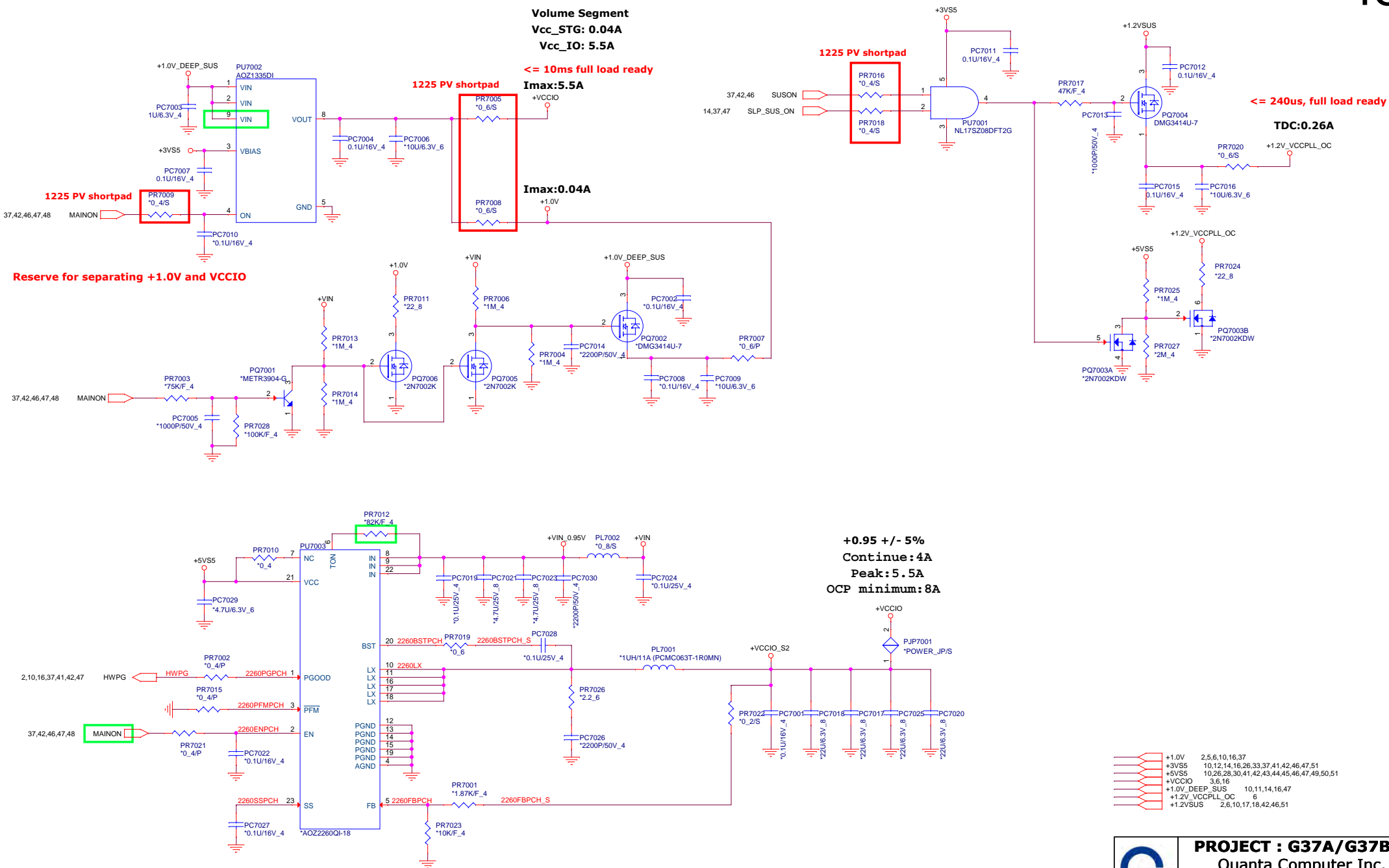


20151118 SI del

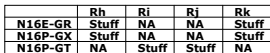



+VIN	26,32,38,39,40,41,42,43,44,45,48,49,50
+3VS5	10,12,14,16,26,33,37,41,42,46,48,51
+5VS5	10,26,28,30,41,42,43,44,45,46,48,49,50,51
+1.0V_DEEP_SUS	10,11,14,16,48
+1.8V	28,31
+VCCSTPLL	2,6,43

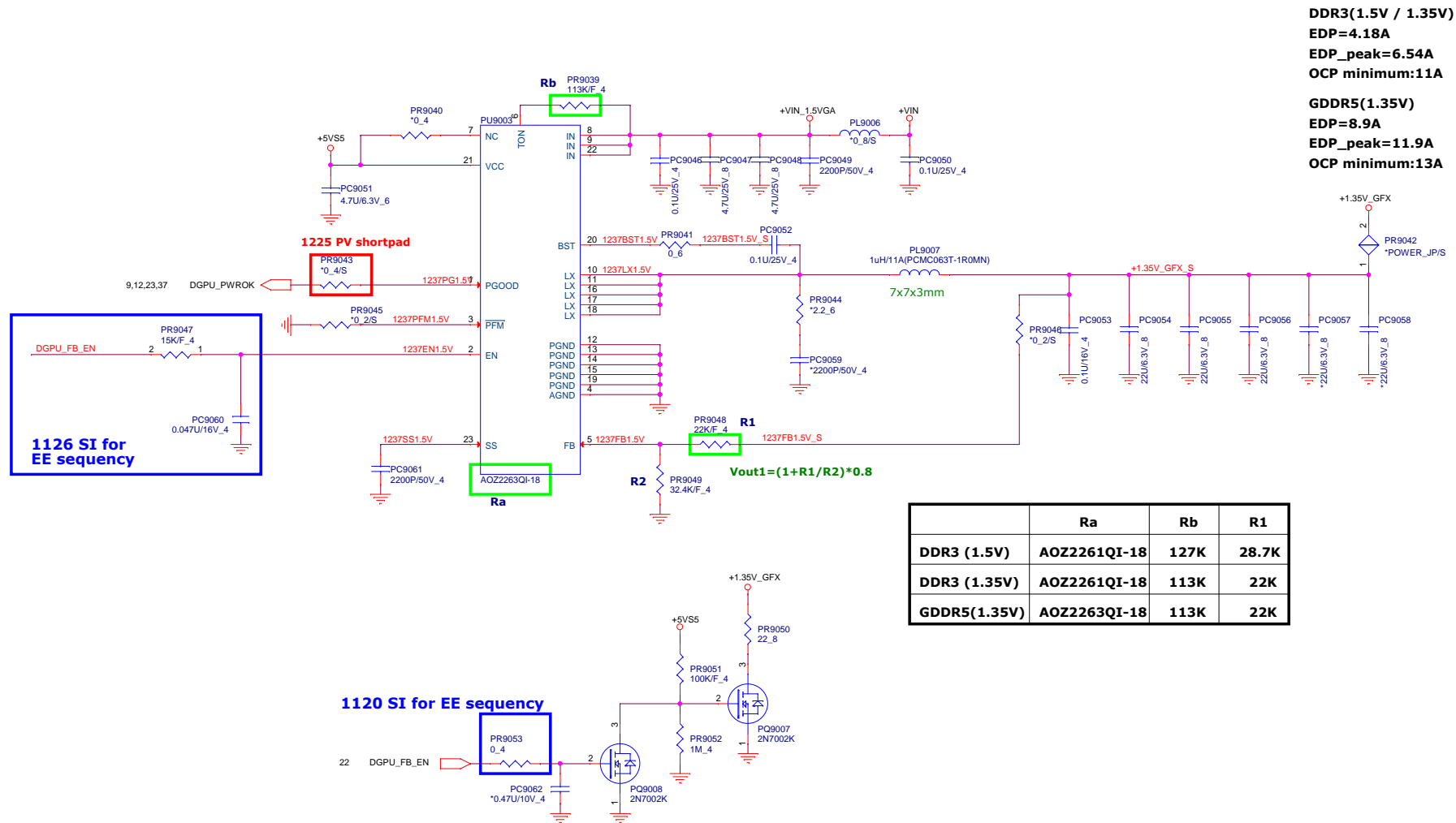
 <b>PROJECT : G37A/G37B</b> <b>Quanta Computer Inc.</b>		
Size Custom	Document Number <b>+1.0_DEEP_SUS</b>	Rev 1A
Date:	Monday, December 28, 2015	Sheet 47 of 51





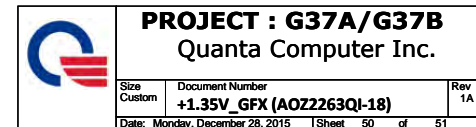


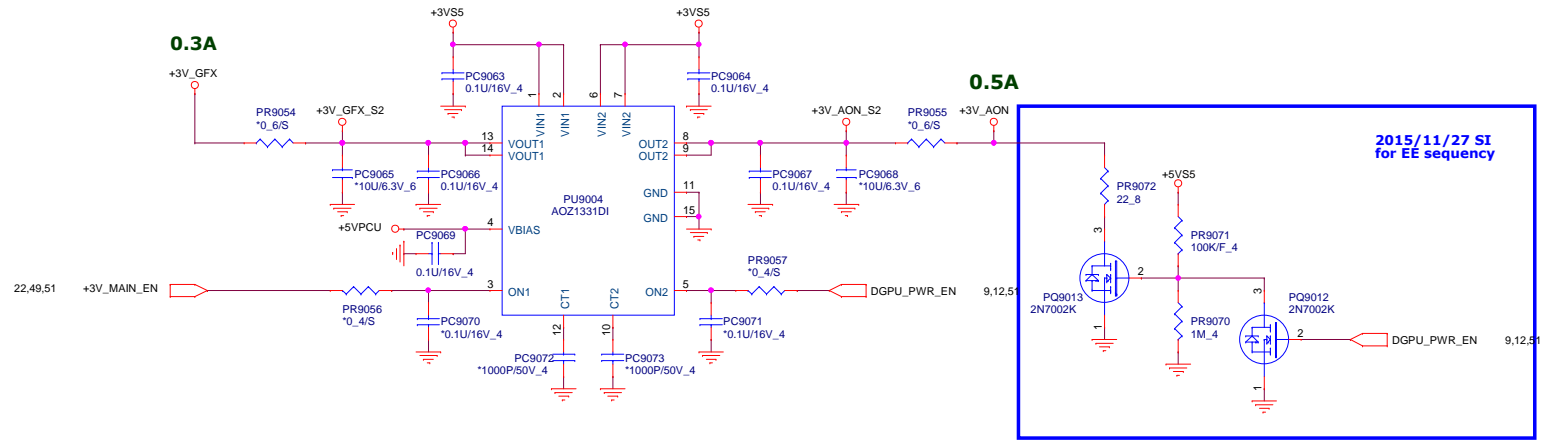
	<b>PROJECT : G37A/G37B</b> <b>Quanta Computer Inc.</b>		
	<b>Size</b> Custom	<b>Document Number</b> <b>+VGACORE (RT8813C)</b>	<b>Rev</b> 1A
	<b>Date:</b> Monday, December 28, 2015   <b>Sheet</b> 49 <b>of</b> 51		



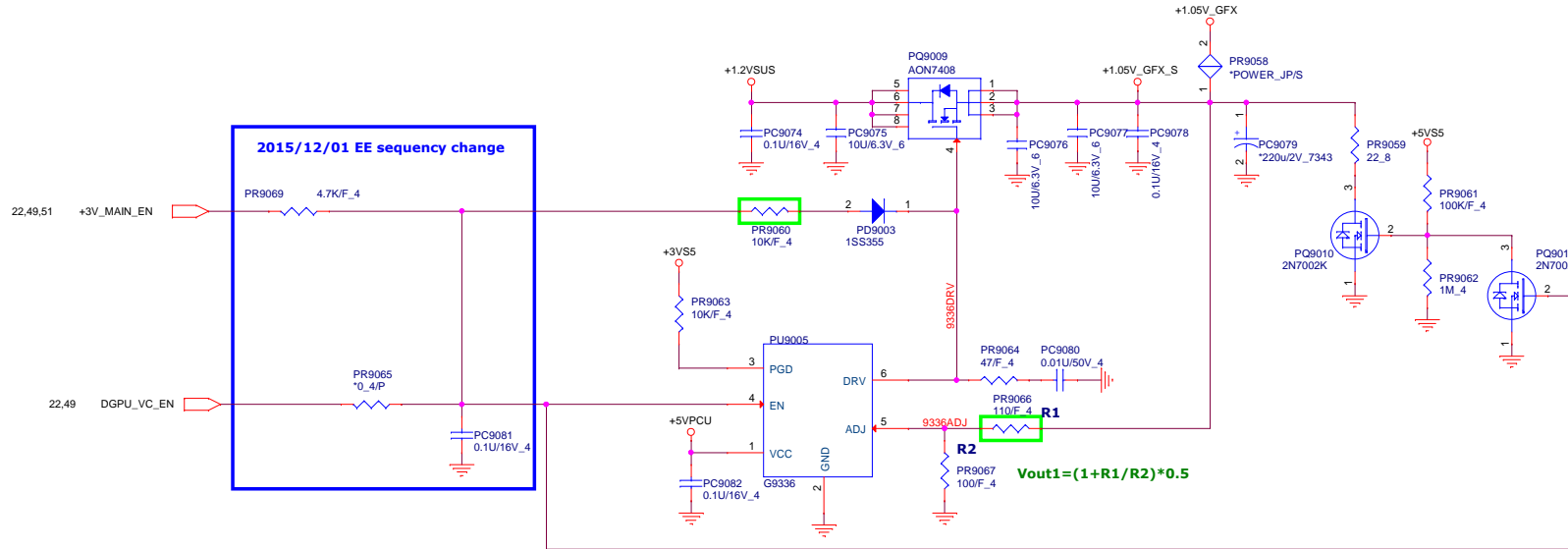
	Ra	Rb	R1
DDR3 (1.5V)	AOZ2261QI-18	127K	28.7K
DDR3 (1.35V)	AOZ2261QI-18	113K	22K
GDDR5(1.35V)	AOZ2263QI-18	113K	22K

+VIN	26,32,38,39,40,41,42,43,44,45,47,48,49
+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,49,51
+1.35V_GFX	20,23,24,25






**+1.05V\_GFX Volt +/- 5%**  
**EDP=2.38A**  
**EDP\_peak = 2.45A**



+VIN	26,32,38,39,40,41,42,43,44,45,47,48,49,50
+3VS5	10,12,14,16,26,33,37,41,42,46,47,48
+5VS5	10,26,28,30,41,42,43,44,45,46,47,48,49,50
+3V_GFX	19,20,21,22,23,49
+3V_AON	19,22,23,27
+1.2VSUS	2,6,10,17,18,42,46,48
+1.05V_GFX	19,20,21,23

 <b>PROJECT : G37A/G37B</b> Quanta Computer Inc.		
Size Custom	Document Number <b>+3V/+1.05V_GFX(AOZ1331DI)</b>	Rev 1A
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